

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

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PETITION FOR *INTER PARTES* REVIEW  
OF U.S. PATENT NO. 6,701,473

Case No. IPR2023-00517

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Patent Trial and Appeal Board  
U.S. Patent and Trademark Office  
P.O. Box 1450  
Alexandria, VA 22313-1450

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## EXHIBIT LIST

| Exhibit | Description                                                                                                             |
|---------|-------------------------------------------------------------------------------------------------------------------------|
| 1001    | U.S. Patent No. 6,701,473 (the “’473 Patent”)                                                                           |
| 1002    | Prosecution history of the ’473 Patent                                                                                  |
| 1003    | Declaration of Dr. Stephen Melvin                                                                                       |
| 1004    | Curriculum Vitae of Dr. Stephen Melvin                                                                                  |
| 1005    | U.S. Patent No. 5,072,138 to Slemmer (“Slemmer”)                                                                        |
| 1006    | U.S. Patent No. 6,308,232 to Gasbarro (“Gasbarro”)                                                                      |
| 1007    | Excerpts from the IEEE Standard Glossary of Computer Hardware Terminology, IEEE Standard 610.10-1994 (1995)             |
| 1008    | Excerpts from National Semiconductor Scan Databook                                                                      |
| 1009    | Excerpts from Bleeker et al., Boundary Scan Test: A Practical Approach                                                  |
| 1010    | Built-In Self-Test (BIST) Using Boundary Scan                                                                           |
| 1011    | U.S. Patent No. 5,784,331 to Lysinger (“Lysinger”)                                                                      |
| 1012    | U.S. Patent No. 5,559,753 to Kocis (“Kocis”)                                                                            |
| 1013    | U.S. Patent No. 5,136,185 to Fleming (“Fleming”)                                                                        |
| 1014    | First Amended Complaint, Polaris Innovations Limited v. Xilinx, Inc., 1:22-cv-00174-RGA, Docket No. 14 (April 28, 2022) |
| 1015    | Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions v3.0, User Guide (UG586 Apr. 6, 2016)                  |
| 1016    | U.S. Patent No. 4,558,236 to Burrows (“Burrows”)                                                                        |
| 1017    | U.S. Patent No. 4,910,417 to Gamal (“Gamal”)                                                                            |

| Exhibit | Description                                                                                                                                                                                                                                                                                                         |
|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1018    | Scheduling Order, Polaris Innovations Limited v. Xilinx, Inc., 1:22-cv-00174-RGA, Docket No. 20 (May 31, 2022)                                                                                                                                                                                                      |
| 1019    | United States District Courts — Federal Court Management Statistics, National Judicial Caseload Profile (June 30, 2022), available at <a href="https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf">https://www.uscourts.gov/sites/default/files/fcms_na_distprofile0630.2022_0.pdf</a> |
| 1020    | Motion Success for Stay Pending IPR before Judge Richard G. Andrews in the District of Delaware (Docket Navigator data from 2020 to 1/20/2023)                                                                                                                                                                      |

## LISTING OF CHALLENGED CLAIMS

| <b>Claim 1</b> |                                                                                                                                                                                                                                                                                                  |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [1.P]          | An electrical circuit comprising:                                                                                                                                                                                                                                                                |
| [1.1]          | a bus; and                                                                                                                                                                                                                                                                                       |
| [1.2]          | a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;                            |
| [1.3]          | said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation. |
| <b>Claim 2</b> |                                                                                                                                                                                                                                                                                                  |
| [2]            | The electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested.                                                   |
| <b>Claim 3</b> |                                                                                                                                                                                                                                                                                                  |
| [3]            | 3. The electrical circuit according to claim 2, wherein said output drivers are deactivated by a test unit which is testing said circuit component to be tested.                                                                                                                                 |
| <b>Claim 4</b> |                                                                                                                                                                                                                                                                                                  |
| [4.1]          | The electrical circuit according to claim 3, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring:                                                                             |

|                |                                                                                                                                                                                                                                                                                                                                                                                                           |
|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [4.2]          | that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus, and                                                                                                                                                         |
| [4.3]          | that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested.                                                                                                                                                                                                      |
| <b>Claim 5</b> |                                                                                                                                                                                                                                                                                                                                                                                                           |
| [5]            | The electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a test control signal.                                                                                                                                                                                      |
| <b>Claim 7</b> |                                                                                                                                                                                                                                                                                                                                                                                                           |
| [7]            | The electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested.                                                                                                                                                                                                               |
| <b>Claim 8</b> |                                                                                                                                                                                                                                                                                                                                                                                                           |
| [8]            | The electrical circuit according to claim 7, wherein, during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by a device selected from the group consisting of said bus control device and one of said others of said plurality of circuit components.                                                                                        |
| <b>Claim 9</b> |                                                                                                                                                                                                                                                                                                                                                                                                           |
| [9]            | The electrical circuit according to claim 1, wherein the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is data selected from the group consisting of infrequently changing data and non-changing data. |

|                 |                                                                                                                                                                                                                                                                                                      |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Claim 10</b> |                                                                                                                                                                                                                                                                                                      |
| [10.1]          | The electrical circuit according to claim 9, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device ensuring:                                                                                                                                   |
| [10.2]          | that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus, and                                                                                                                                                   |
| [10.3]          | that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested.                                                                                                                      |
| <b>Claim 13</b> |                                                                                                                                                                                                                                                                                                      |
| [13]            | The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for outputting data to said bus, and each one of said output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit. |
| <b>Claim 14</b> |                                                                                                                                                                                                                                                                                                      |
| [14]            | The electrical circuit according to claim 13, wherein each one of said output drivers receives an input signal that is an output signal of said respectively provided device.                                                                                                                        |
| <b>Claim 20</b> |                                                                                                                                                                                                                                                                                                      |
| [20.P]          | A method for testing a circuit component which is connected to other circuit components via a bus, the method which comprises:                                                                                                                                                                       |
| [20.1]          | providing a plurality of circuit components that are connected to a bus;                                                                                                                                                                                                                             |

|                 |                                                                                                                                                                                                                                                                                                                        |
|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [20.2]          | configuring at least one of the plurality of circuit components such that it can be tested independently from all others of said plurality of circuit components, the at least one of the plurality of circuit components defining a circuit component to be tested; and                                               |
| [20.3]          | while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation. |
| <b>Claim 21</b> |                                                                                                                                                                                                                                                                                                                        |
| [21.P]          | The method according to claim 20, which comprises:                                                                                                                                                                                                                                                                     |
| [21.1]          | providing the circuit component to be tested with output drivers for outputting data to the bus; and                                                                                                                                                                                                                   |
| [21.2]          | deactivating the output drivers during testing of the circuit component to be tested.                                                                                                                                                                                                                                  |
| <b>Claim 22</b> |                                                                                                                                                                                                                                                                                                                        |
| [22]            | The method according to claim 21, which comprises deactivating the output drivers by a test unit which is testing the circuit component to be tested.                                                                                                                                                                  |
| <b>Claim 23</b> |                                                                                                                                                                                                                                                                                                                        |
| [23.1]          | The method according to claim 22, which comprises:<br>providing a device for deactivating the output drivers;                                                                                                                                                                                                          |
| [23.2]          | selecting the device from the group consisting of a logic unit and a selection circuit;                                                                                                                                                                                                                                |

|                 |                                                                                                                                                                                                                                                                                                                                                                                  |
|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [23.3]          | using the device to ensure:<br>that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is supplied to the circuit component to be tested by a bus control device which controls the bus, and                                                                                                     |
| [23.4]          | that during testing of the circuit component to be tested, the output drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested.                                                                                                                                                                                |
| <b>Claim 24</b> |                                                                                                                                                                                                                                                                                                                                                                                  |
| [24]            | The method according to claim 23, which comprises using the logic unit to provide an output signal resulting from a logical combination of the enable signal and a test control signal.                                                                                                                                                                                          |
| <b>Claim 26</b> |                                                                                                                                                                                                                                                                                                                                                                                  |
| [26]            | The method according to claim 20, which comprises signaling a bus control device which controls the bus that the circuit component to be tested is undergoing a test.                                                                                                                                                                                                            |
| <b>Claim 27</b> |                                                                                                                                                                                                                                                                                                                                                                                  |
| [27]            | The method according to claim 26, which comprises using the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components.                                                                |
| <b>Claim 28</b> |                                                                                                                                                                                                                                                                                                                                                                                  |
| [28]            | The method according to claim 20, wherein the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation, and selecting the data output to the bus from the group consisting of infrequently changing data and non-changing data. |

| <b>Claim 29</b> |                                                                                                                                                                                      |
|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| [29.1]          | The method according to claim 28, which comprises:<br>selecting a device from the group consisting of a logic unit and a selection circuit;                                          |
| [29.2]          | using the device to ensure:<br>that during normal operation of the circuit component to be tested,<br>data that actually needs to be output to the bus are output to the bus,<br>and |
| [29.3]          | that during testing of the circuit component to be tested, the data<br>outputted to the bus is from a test unit carrying out the testing of the<br>circuit component to be tested.   |
| <b>Claim 32</b> |                                                                                                                                                                                      |
| [32.1]          | The method according to claim 29, which comprises:<br>providing the circuit component to be tested with output drivers for<br>outputting data to the bus; and                        |
| [32.2]          | providing each one of the output drivers with a device that is selected<br>from the group consisting of a logic unit and a selection circuit.                                        |
| <b>Claim 33</b> |                                                                                                                                                                                      |
| [33]            | The method according to claim 32, wherein each one of the output<br>drivers receives an input signal that is an output signal of the<br>respectively provided device.                |

## **I. INTRODUCTION**

Xilinx, Inc. (“Xilinx” or “Petitioner”) petitions for *Inter Partes* Review (“IPR”) of claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 of U.S. Patent 6,701,473 (the “’473 Patent”), assigned to Polaris Innovations Limited (“Polaris” or “Patent Owner”).

## **II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8**

### **A. Real Parties-In-Interest Under 37 C.F.R. § 42.8(b)(1)**

Petitioner Xilinx, Inc., Advanced Micro Devices, Inc. (“AMD”), and ATI Technologies ULC (“ATI”) are the real parties-in-interest. AMD is the parent of Xilinx and ATI is an indirect, wholly owned subsidiary of AMD.

### **B. Related Matters Under 37 C.F.R. § 42.8(b)(2)**

Polaris asserted four patents, including the ’473 Patent, against Xilinx in *Polaris Innovations Ltd. v. Xilinx, Inc.*, CA 1:22-CV-00174-RGA (D. Del.), in a complaint filed on February 8, 2022 and served on February 22, 2022. Xilinx is concurrently filing this Petition and IPR petitions for the other three asserted patents: IPR2023-00513, IPR2023-00514, and IPR2023-00516.

### **C. Lead and Back-Up Counsel under 37 C.F.R. § 42.8(b)(3)**

Petitioner provides the following designation of counsel.

| <b>Lead Counsel</b>                                                                                                                                               | <b>Backup Counsel</b>                                                                                                                                                     |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Brian W. Oaks (Reg. No. 44,981)<br>McDERMOTT WILL & EMERY LLP<br>303 Colorado Street, Suite 2200<br>Austin, TX 78701<br>TEL: 512-726-2574<br>EMAIL: boaks@mwe.com | Aashish G. Kapadia (Reg. No. 78,844)<br>McDERMOTT WILL & EMERY LLP<br>303 Colorado Street, Suite 2200<br>Austin, TX 78701<br>TEL: 512-298-6488<br>EMAIL: akapadia@mwe.com |

#### **D. Service Information**

Please address all correspondence to the address above. Petitioner consents to electronic service by email at xilinxMWETeam@mwe.com.

### **III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.103**

Petitioner authorizes the Office to charge Deposit Account No. 50-0417 for the petition fee set in 37 C.F.R. §42.15(a) and for any other required fees.

### **IV. REQUIREMENTS FOR IPR UNDER 37 C.F.R. § 42.104**

#### **A. Grounds for Standing Under 37 C.F.R. § 42.104(a)**

Petitioner certifies that the '473 Patent is available for IPR and that Petitioner is not barred or estopped from requesting IPR.

#### **B. Challenge under 37 C.F.R. § 42.104(b) and Relief Requested**

Petitioner requests IPR of claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 of the '473 Patent on the grounds listed below. In support, this petition includes a declaration of Dr. Stephen Melvin (EX1003).

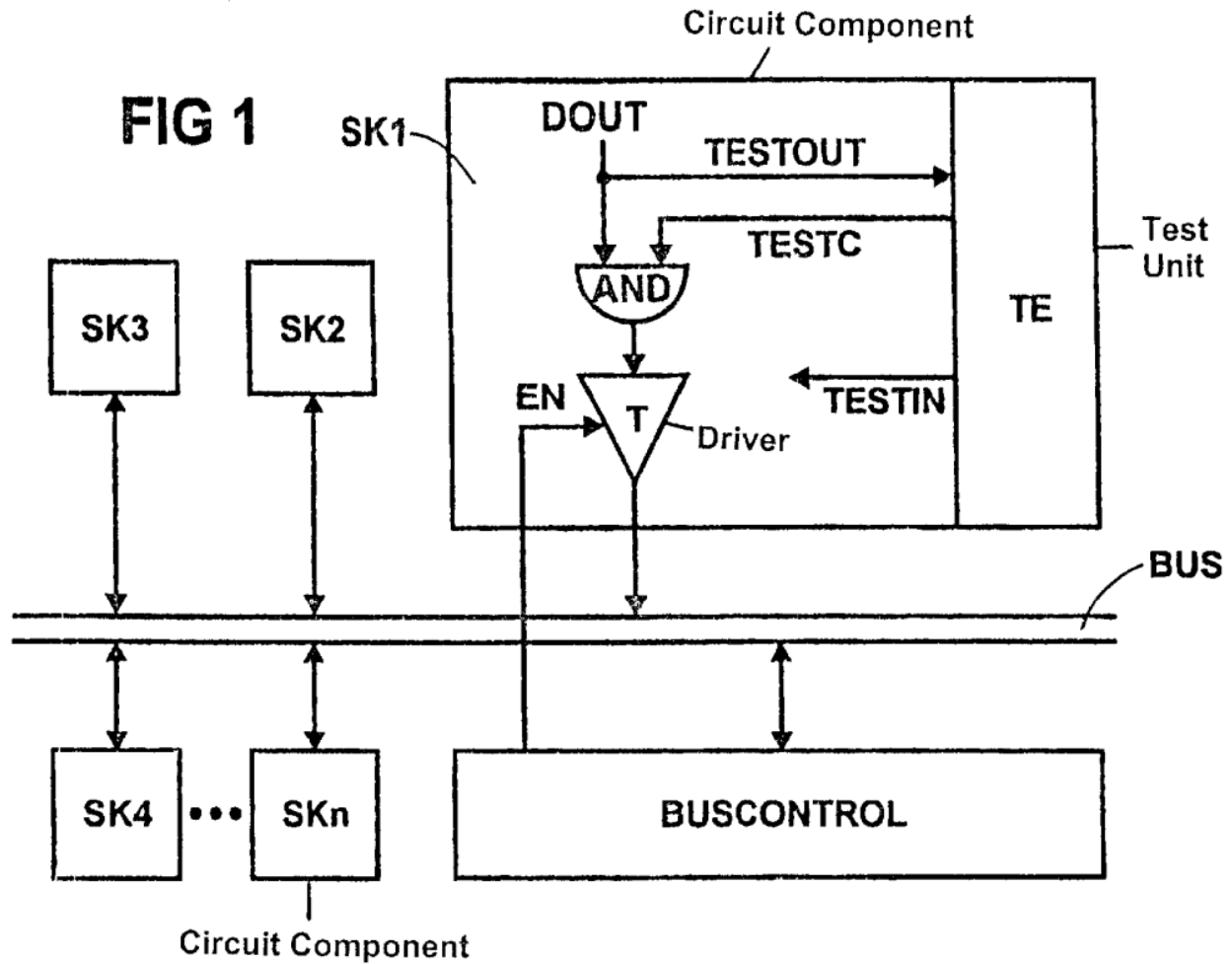
| Ground | Claims                                       | Basis for Rejection                             |
|--------|----------------------------------------------|-------------------------------------------------|
| 1      | 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33 | 35 U.S.C. §103 over Slemmer                     |
| 2      | 1-5, 7-10, 13-14, 20-24, 26-29, 32-33        | 35 U.S.C. §103 over Slemmer in view of Gasbarro |

## V. SUMMARY OF THE '473 PATENT

### A. Brief Description

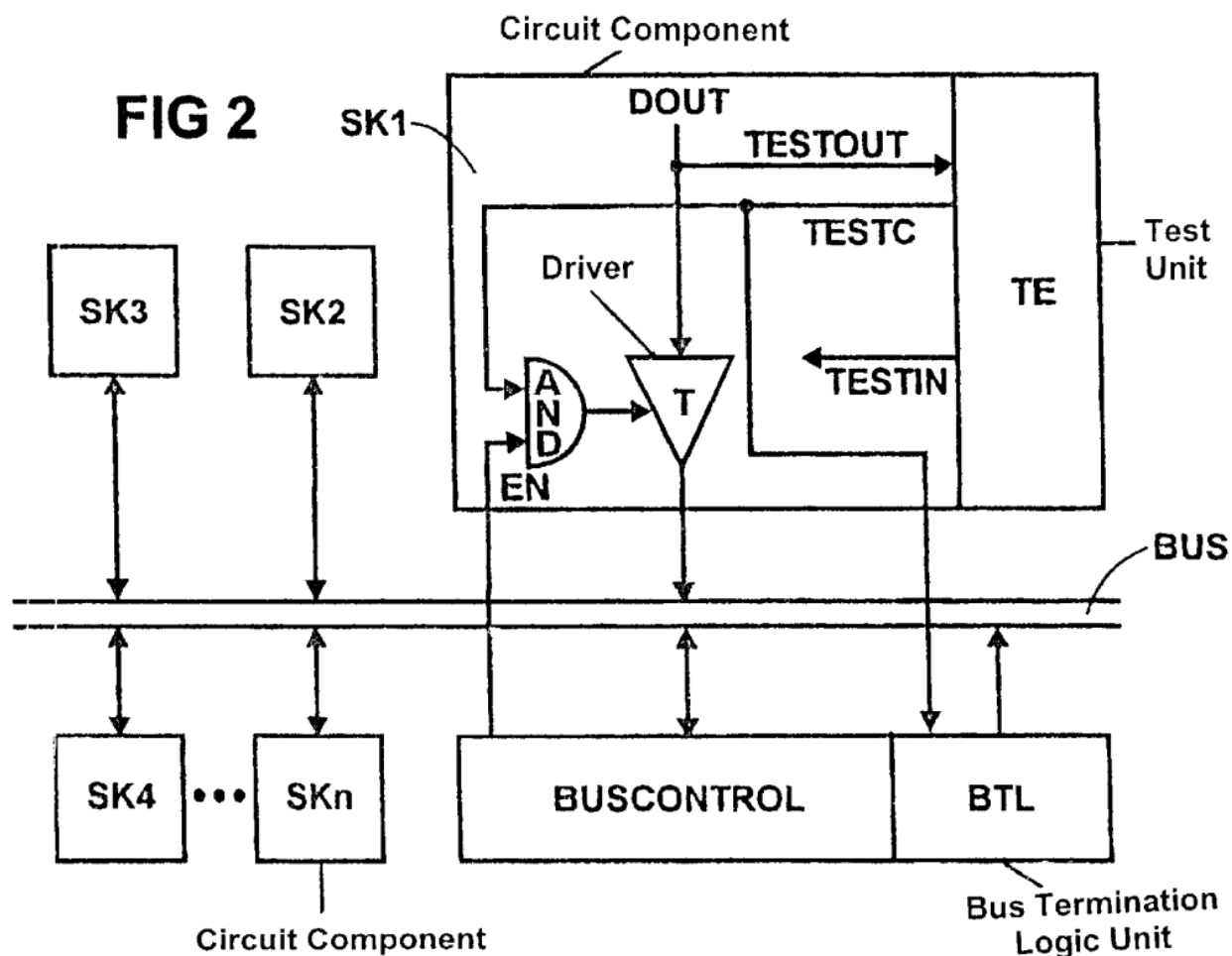
The '473 Patent relates to testing a circuit component of an electrical circuit independently from other circuit components connected via a bus. EX1001, Abstract, 1:8-16. During testing, the component outputs to the bus either no data or data other than that which would be output in normal operation, which purportedly ensures that the output drivers of the component consume little power. *Id.*, 1:40-51, 2:16-27.

As shown below, circuit components (SK1–SKn) and a bus control device (BUSCONTROL) are connected to a bus.



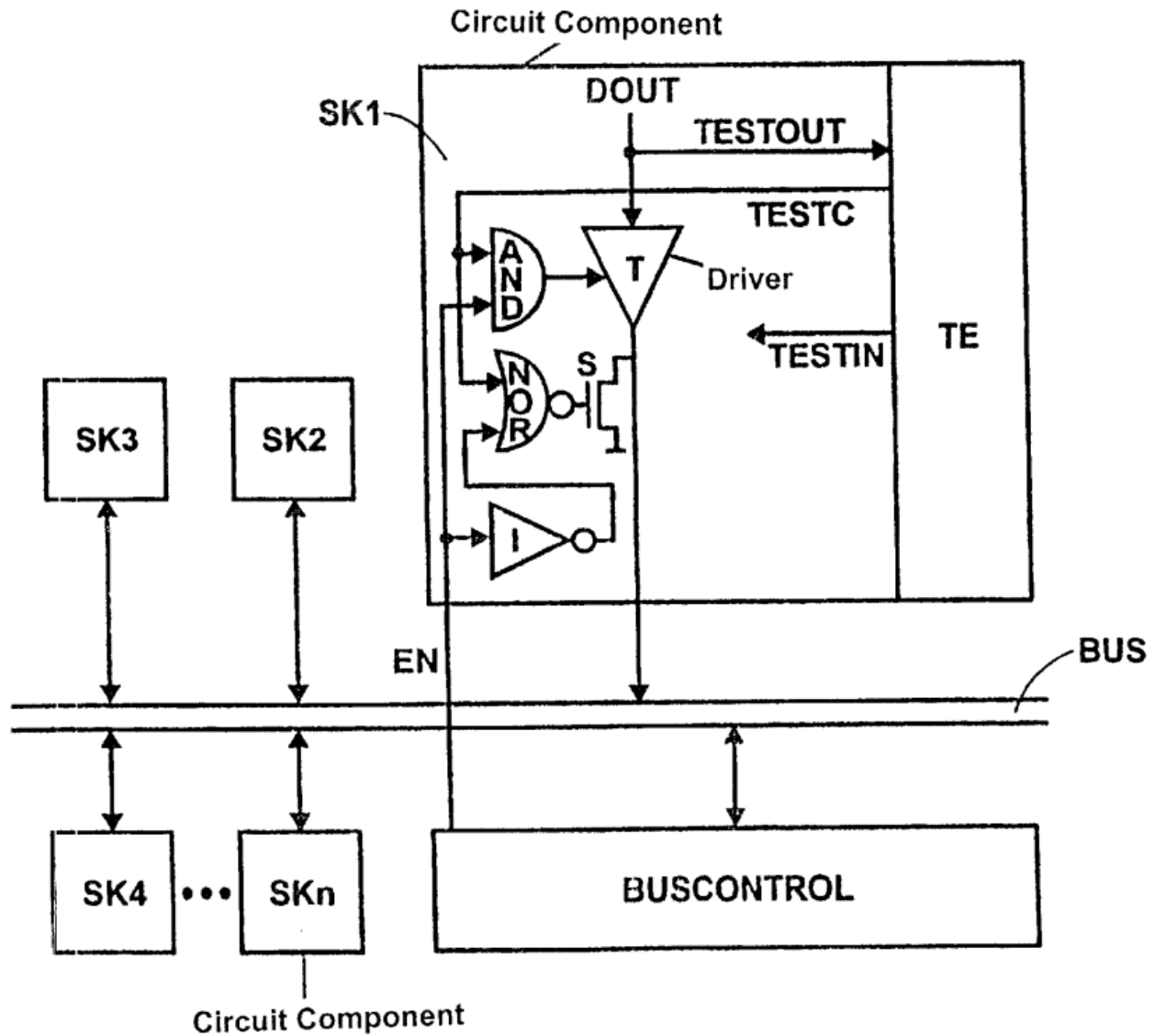
*Id.*, FIG. 1, 4:61-5:2. The circuit component SK1 includes a test unit (TE) that provides a test control signal (TESTC) and input test data (TESTIN) and that receives output test data (TESTOUT). *Id.*, 5:11-29. SK1 also includes an AND-gate that receives output data (DOUT) and TESTC and that provides DOUT during normal operation and a value of “0” during testing. *Id.*, 6:4-20. Finally, SK1 includes a tristate driver (T) that outputs the provided signal based on whether the driver is enabled (EN). *Id.*, 5:39-49.

Figure 2 adds a bus termination logic (BTL) unit to BUSCONTROL, as shown below.



*Id.*, FIG. 2, 8:10-28. The BTL receives TESTC and ensures that, during testing of SK1, the bus is terminated by one of the other components connected to the bus or BTL itself. *Id.*, 8:16-23. The driver is enabled to output DOUT on the bus based on the output of an AND-gate that receives TESTC and EN. *See id.*, 7:60-65.

Figure 3 modifies SK1 relative to Figures 1 and 2 to add circuitry for bus termination.



*Id.*, FIG. 3, 8:56-65, 9:24-47. The driver output is connected to a switch (S), which is connected by the TESTC and inverted EN signals and controls bus termination.

*Id.* The driver and bus termination are controlled by logic (AND, Inverter, and NOR), as shown below:

| TESTC | EN | Action                                                          |
|-------|----|-----------------------------------------------------------------|
| 0     | 0  | Test mode<br>Output drivers deactivated<br>Termination inactive |
| 0     | 1  | Test mode<br>Output drivers deactivated<br>Termination active   |
| 1     | 0  | Normal operation<br>Output drivers deactivated                  |
| 1     | 1  | Normal operation<br>Output drivers activated                    |

*Id.*, 9:66-10:15.

## **B. Summary of the Prosecution**

On January 26, 2001, the '473 Patent was filed as Application No. 09/771,391 (the "'391 Application"), which claims priority to German Patent Applications DE10003260, filed January 26, 2000, and DE10016127, filed March 31, 2000, and listed 38 claims. *See* EX1002, 3, 6, 36-49. A notice of allowance was issued in the '391 Application without any rejection. *See id.*, 52-59.

## **VI. THE BOARD SHOULD NOT DISCRETIONARILY DENY INSTITUTION**

### **A. Section 325(d)**

*Advanced Bionics* and §325(d) do not support discretionary denial. The references and combinations cited by Petitioner were not presented to the Office, and no similar references were evaluated during prosecution. Denial under §325(d) is thus unwarranted. *See Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18 at 8-9 (PTAB Aug. 12, 2021).

## **B. Fintiv (Section 314(a))**

The *Fintiv* factors favor institution. This petition presents compelling evidence showing the unpatentability of the challenged claims, and thus institution should not be discretionarily denied under *Fintiv*. Although there is a case pending with Xilinx involving the '473 Patent, it remains at an early stage. Initial discovery and contentions have been served, but the parties have not briefed or argued claim construction, and any final written decision will likely be issued before trial. The current trial date is November 18, 2024 and the median time-to-trial for the Delaware court suggests trial in February 2025. EX1018, 12; EX1019, 14. Further, Xilinx intends to request a stay pending IPR. EX1020 (showing the Delaware court grants majority of motions to stay).

## **VII. LEVEL OF ORDINARY SKILL IN THE ART**

A person of ordinary skill in the art (POSITA) would have had a Bachelor of Science degree in Electrical Engineering, Computer Engineering, or an equivalent field and two or three years of academic or industry experience in the use and testing of integrated circuits, or comparable experience. EX1003, ¶33. Additional work experience can substitute for educational or research experience, and vice versa. A POSITA would have been familiar with integrated circuit inputs/outputs (I/Os), including I/Os for memory devices and memory buses, common test

principles, and configuring driver outputs during testing and normal operation. *Id.*, ¶34.

### **VIII. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3)**

Petitioner submits that all claim terms should be construed according to the *Phillips* standard. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100. Construction of any terms is unnecessary because it is not dispositive—the art teaches the claims under any construction. *Cf. Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

### **IX. OVERVIEW OF THE PRIOR ART**

As of the filing date of the ’473 Patent, there were multiple types of memory available, including static random access memory (SRAM) and dynamic RAM (DRAM). EX1003, ¶¶44-48; *see* EX1005, 6:54-66, 2:60-66, 5:50-55 (SRAM), 2:9-21, 3:16-28 (DRAM). Typical memory systems included address, data, and control signals that connected a memory controller to memory devices. EX1003, ¶¶49-50; *see* EX1012, FIG. 1, 1:49-52. There were also several techniques for testing circuits, such as memory circuits, including techniques embedded in systems and used with external test equipment and techniques that handled bus contention issues. EX1003, ¶¶51-56; *see* EX1008, 18-21; EX1009, 45-48; EX1010, 5, 10-11.

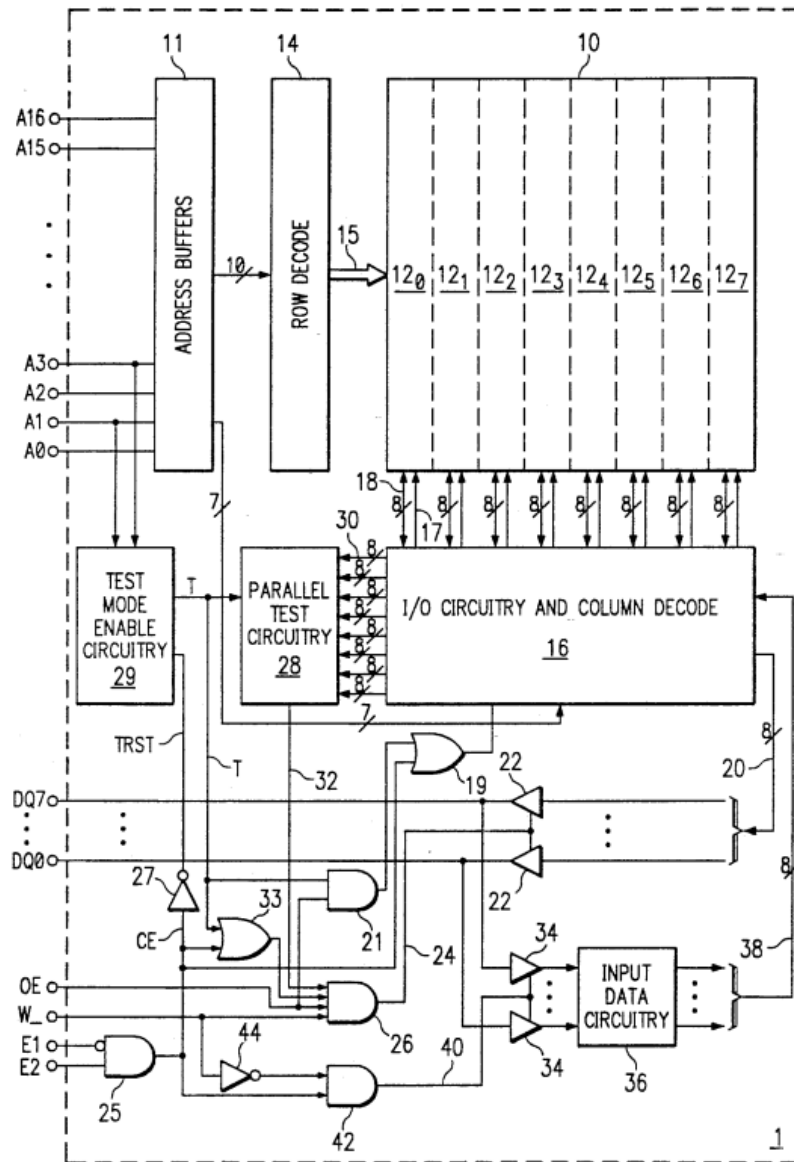
**A. Slemmer (EX1005)**

U.S. Patent No. 5,072,138 (“Slemmer”) was filed on August 17, 1990 and issued on December 10, 1991. EX1005, 1. Slemmer is prior art under 35 U.S.C. §102(b) because it issued and published more than a year prior to the U.S. filing date of the ’473 Patent on January 26, 2001. *See* EX1001, 1.

Slemmer discloses a system in which only one memory of many is tested at any one time in which a specific sequence of inputs, such as a sequence of codes, is required to avoid inadvertent entry into the test mode. EX1005, Abstract, 5:3-14, 10:35-47, 37:11-24. During testing, one or more output terminals (e.g., DQ0) may be placed in a high-impedance state, or in a low-impedance state to acknowledge entry into the test mode or a successful test. *See* EX1005, Abstract, 8:37-42, 35:22-36:68, Fig. 9; EX1003, ¶61. Slemmer also discloses a solution for bus contention issues during testing in which the output enable (OE) terminal of the memory serves as a chip enable while the memory is in a test mode. *See* EX1005, 36:58-68, 37:11-26.

Slemmer shows one of the memories 1 in the system with parallel address (e.g., A0–A16), parallel data (e.g., DQ0–DQ7), output enable (OE), write enable (W<sub>‾</sub>), and chip enable (e.g., E1, E2) terminals.

FIG. 1



*Id.*, FIG. 1, 8:59-61, 37:11-24. The memory includes test mode enable circuitry (TMEC) 29 that receives input signals on lines A1, A3, and TRST and that indicates to parallel test circuitry (PTC) 28 whether a test mode is enabled by generating a high logic level output signal on line T. *Id.*, 9:19-30, 9:44-48, FIGS. 1-2b. PTC 28 receives the signal on line T from TMEC 29 and data sets on lines 30

from input/output circuitry and column decoder 16, and generates a signal on line 32, which is input to AND-gate 26. *Id.*, FIGS. 1-2b, 7:35-8:58, 9:10-30. The signal on line 32 has a high logic level during normal operation and during testing when each of the data sets contains the same data (indicating no error), and a low logic level during testing when the data sets have different data (indicating an error). *Id.*; *see also* EX1003, ¶¶62-63.

AND-gate 26 logically combines four input signals into an output to control whether the output buffers/drivers 22 are activated or deactivated. *Id.* In normal operation, the output of AND-gate 26 controls whether the buffers 22 drive data terminals (e.g., DQ0 to DQ7) to output data from the internal output data bus 20, or whether the buffers 22 present a high-impedance state at the terminals. *Id.*, 7:26-35; EX1003, ¶64. While in a test mode, the memory provides an acknowledgement by presenting a low impedance state on one or more data terminals (e.g., DQ0), in which each terminal is driver by a driver 22, which is controlled by AND-gate 26. EX1005, Abstract, 36:36-67.

Although Slemmer does not illustrate his system, a POSITA would have understood that the conceptual figure below illustrates a system with multiple memory devices according to Slemmer's teachings:



memories are connected via their terminals to a bus that connects them to a controller, such as one in a system or test equipment. *Id.*

A POSITA would have understood from Slemmer's disclosure that circuitry, commonly known as a memory controller, must be connected to the multiple memories to control and use them, such as by sending signals to and receiving signals from the memories. EX1003, ¶¶66-68; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52. Consistent with a memory controller being a well-known structure for interfacing with memory, Slemmer teaches how the memory interfaces with the controller, including by receiving address information at the address terminals, receiving input data for write operations and sending output data for read operations or for testing at the data terminals, and receiving externally driven signals at the control or enable terminals. EX1003, ¶¶69-71; EX1005, FIG. 1, 6:9-11, 6:18-23 (address terminals), 1:33-38, 7:26-30, 8:59-67, 35:22-42 (data terminals), 8:4-5, 37:27-29, 37:33-37, 32:64-33:2 (control/enable terminals). Slemmer also teaches considerations for a system designer, such as the number of external terminals and support for inserting memory into a system already powered up. EX1005, 3:1-16, 3:39-60, 35:52-64; EX1003, ¶72. Moreover, Slemmer teaches that a system or test equipment is required to test the memory by, for example, controlling when testing is enabled

and receiving an acknowledgement of entry into a test mode. EX1005, 1:21-22, 3:11-16, 32:64-33:2, 35:22-42, 35:47-51; EX1003, ¶73.

A POSITA would also have understood from Slemmer's disclosure that the data and address terminals of the multiple memories are connected together and to the controller via signal lines, any combination of which is a bus. EX1003, ¶73; EX1005, FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 37:11-24, 37:27-29, 37:33-37. As illustrated above, data lines D0 through D7 and address lines A0 through A16 are connected between the multiple memories 1. EX1005, FIG. 1. Further, a POSITA would have understood from Slemmer's disclosure that the enable terminals (e.g., OE, E1, and E2) of multiple memories would not be connected together, because the controller must be able to avoid bus contention (including during testing) by enabling each of the multiple memories independently of the other memories, and thus the controller would be connected via separate lines to the enable terminals of each memory in the system. EX1003, ¶73; EX1005, 7:35-8:58, 8:59-6:9, 37:11-26, FIG. 1; *see* EX1009, 45-47.

#### **B. Gasbarro (EX1006)**

U.S. Patent No. 6,308,232 ("Gasbarro") was filed on September 1, 1999. EX1006, 1. Gasbarro is prior art under 35 U.S.C. §102(e) because the related application was filed before the invention by the applicant for the '473 Patent,

which was filed on January 26, 2001, claiming priority to German applications DE10003260, filed on January 26, 2000, and DE10016127, filed March 31, 2000. See EX1001, 1.

Gasbarro discloses a system with multiple memory devices each with an electronically activated terminator and a method for detecting the last memory device arranged along a bus connecting a memory controller to the memory devices and activating the last device's active terminator. EX1006, Abstract.

As shown below, Gasbarro discloses a conventional memory system that includes a memory controller (M) for writing data into and reading data from memory devices (D) via a bi-directional bus.

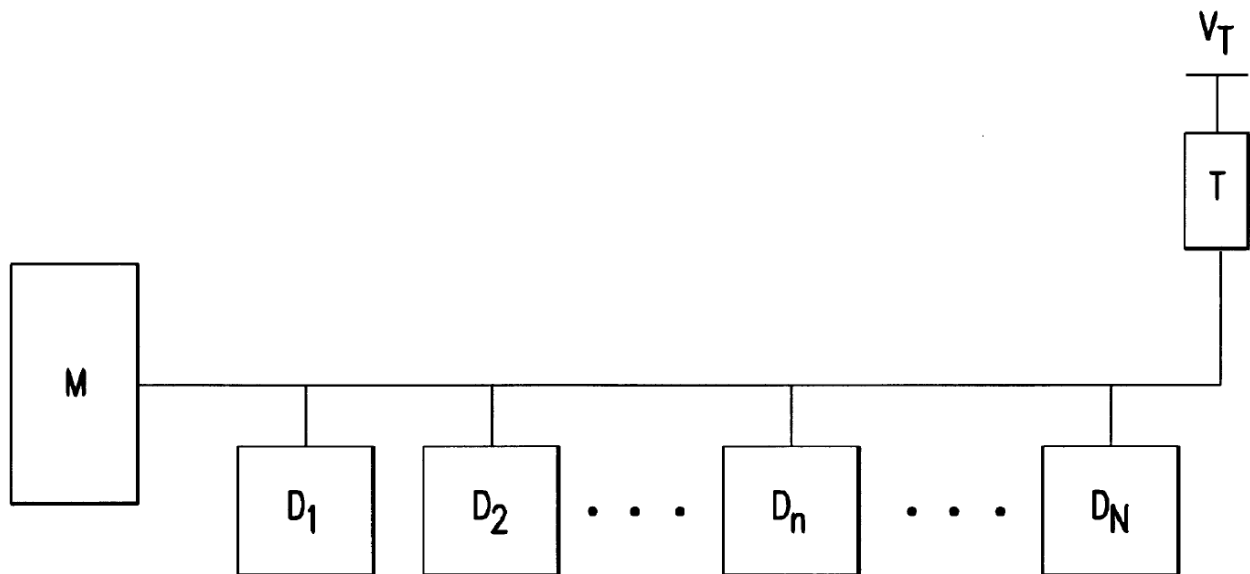


**FIG.1**  
PRIOR ART

EX1006, FIG. 1, 1:15-19, FIG. 2. The devices (D) connected to the bus have a predetermined characteristic impedance and each signal line of the bus terminates at an input/output pin of the controller (M) and a terminator (T). *Id.*, 1:19-27.

Gasbarro explains that without “balance between the various memory system components . . . the signal line impedance will depart from its desired impedance,” which “will result in unwanted signal reflections . . . and in increased signal line noise.” *Id.*, 2:59-64.

To enable impedance balance in an expandable memory system, Gasbarro discloses that the controller balances bus impedance by using an active terminator. *Id.*, 3:42-45. As shown below, the controller 70 uses a serial initialization line (SIL) 72 or channel 71 to communicate an active termination signal to any one of the devices (D).

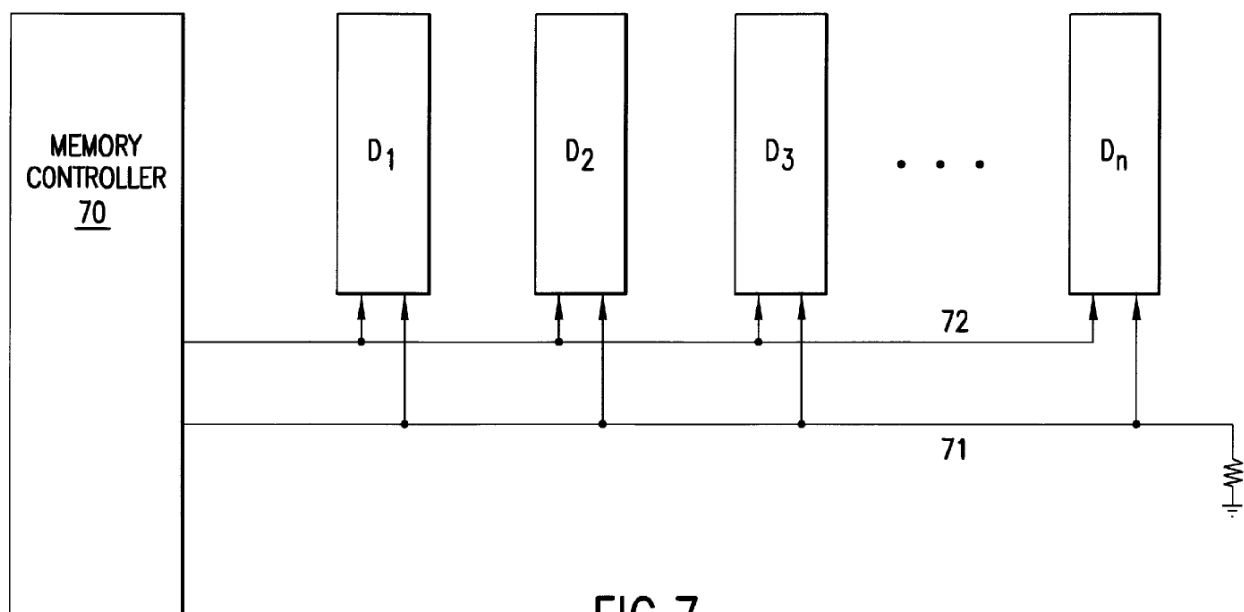


FIG.7

*Id.*, FIG. 7, 6:49-54. The controller determines which device is the last on the data bus ( $D_n$ ) during initialization and then enables its active terminator, to balance impedances in the memory system to avoid signal reflections on the bus. *Id.*, 6:55-7:14; *see* EX1003, ¶¶74-76.

**X. THERE IS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE**

**A. Ground 1: Claims 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, 32-33 are obvious over Slemmer**

**1. Claim 1**

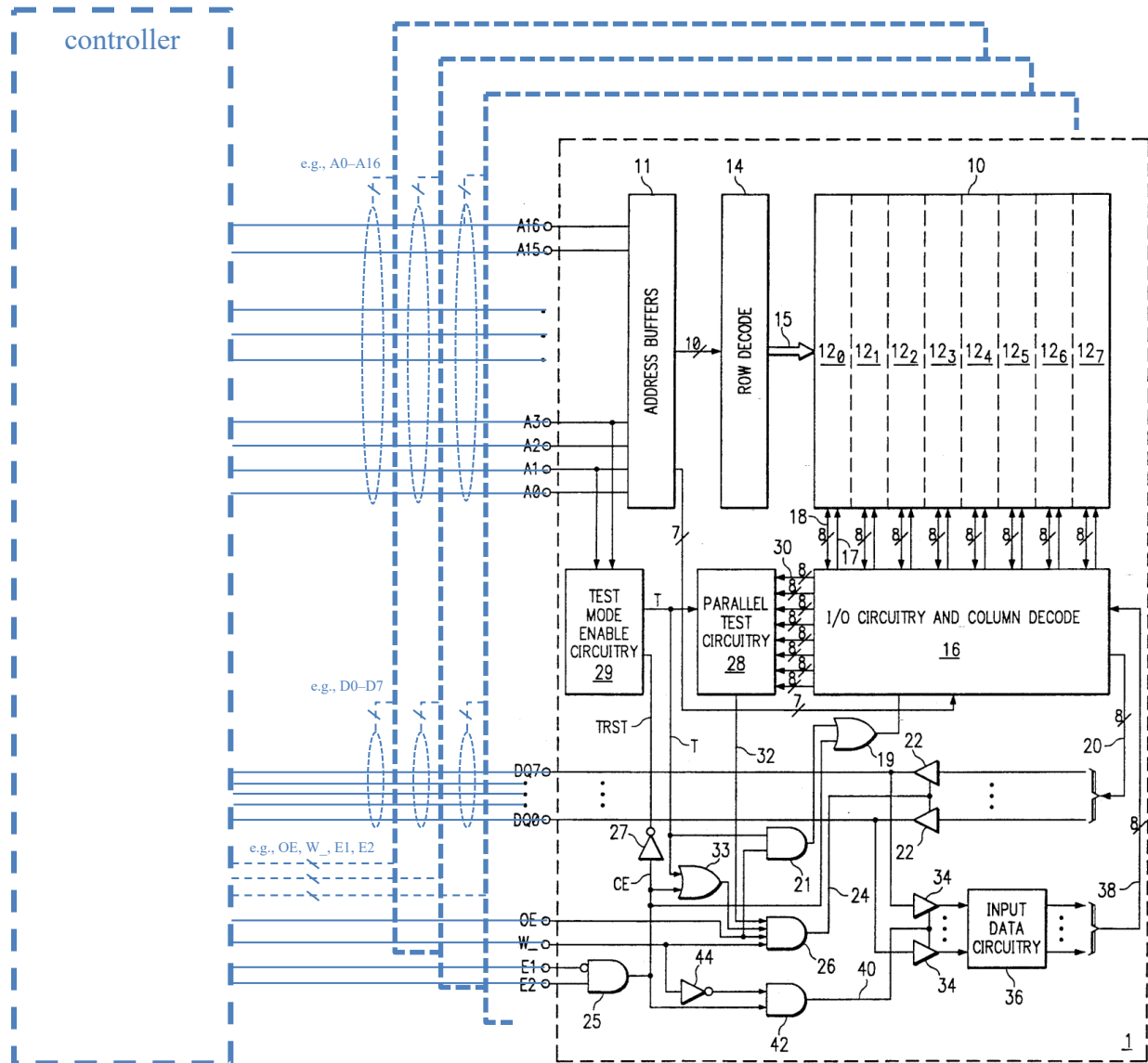
**a. [1.P] “An electrical circuit comprising:”**

Slemmer teaches the preamble to the extent it is limiting. Slemmer teaches and discloses multiple integrated circuit memories that are connected via a bus (collectively, an “*electrical circuit*”) such that only one of the memories is to be tested at a time, as detailed further below with respect to the limitations of claim 1. EX1005, 37:11-24, FIG. 1; EX1003, ¶78.

**b. [1.1] “a bus; and”**

Slemmer teaches data and/or address I/O connections that are connected to signal lines in which one or more signal lines is “*a bus*.” EX1003, ¶¶79-81; *see* EX1007, 9 (“bus” means “[o]ne or more conductors that are used for the transmission of signals, data, or power”). Although Slemmer does not illustrate his

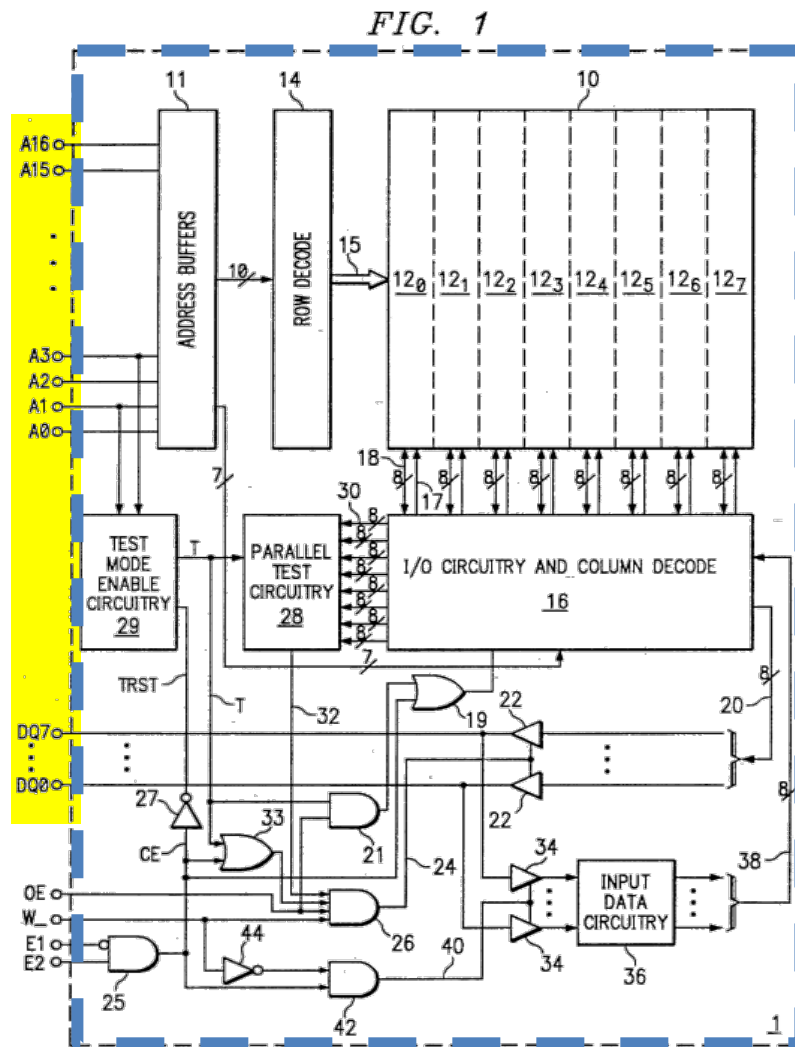
system, the conceptual figure below illustrates his system with multiple memory devices according to Slemmer's teachings:



EX1003, ¶79; EX1005, FIG. 1. As shown, Slemmer teaches that multiple memories are connected together, via their terminals and signal lines, and to a controller, such as one in a system or test equipment. *See* EX1005, FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-

67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 36:55-68, 37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52; *supra* §IX.A.

As shown below, Slemmer discloses that each memory 1 (annotated in blue) has multiple data input/output (I/O) terminals (e.g., DQ0–DQ7) and multiple address terminals (e.g., A0–A17) (in yellow). EX1005, 5:50-64, 6:9-29, 6:54-66, FIG. 1 (below); EX1003, ¶80.



Slemmer explains that the data I/O terminals receive input data during write operations and output data during read operations, and that the address terminals receive a unique memory address and/or a test mode enable signal. EX1005, 6:9-29, 7:15-34, 8:59-9:9, 9:19-30, FIG. 1; EX1003, ¶81. Slemmer also discloses that multiple memories are connected in parallel. EX1005, 37:17-18. Thus, it is obvious to a POSITA that Slemmer's data I/O connections and/or address connections are connected to signal lines and that one of more of the signal lines is "*a bus.*" EX1003, ¶¶79-81.

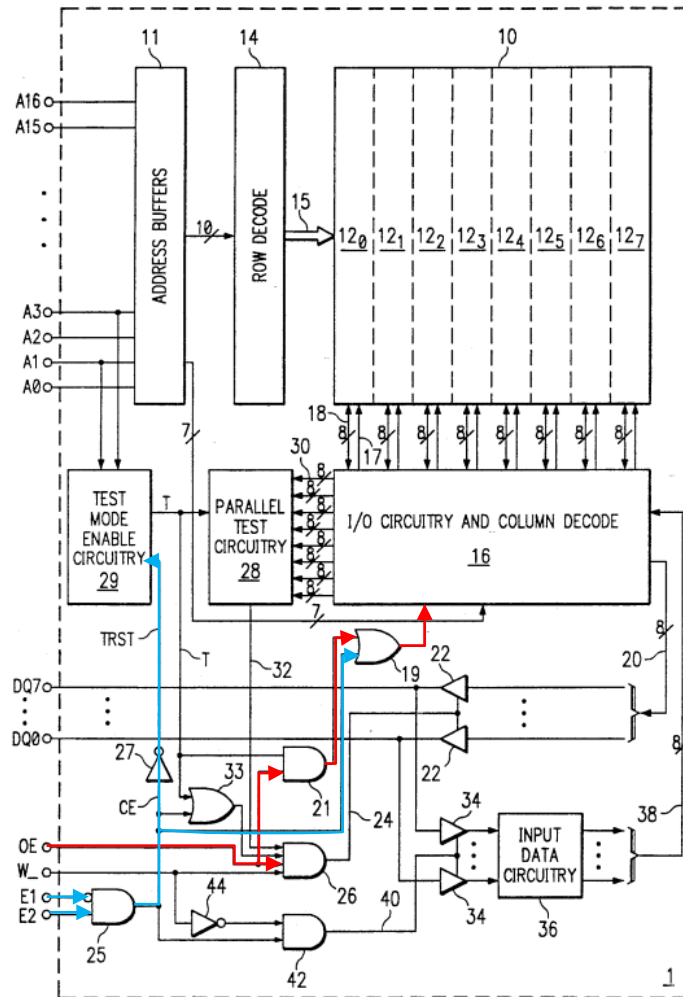
**c. [1.2] "a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;"**

As explained above for claim [1.1], Slemmer teaches that the data I/O and/or address connections are connected to signal lines and that one or more signal lines are a "*bus.*" *Supra* §X.A.1.b; *see, e.g.*, EX1005, 35:22-42, 37:11-37; EX1003, ¶82. Slemmer also teaches that multiple memories, each similar to memory 1, are connected in parallel via signal lines for the data I/O and address connections.



(E1, E2, and resulting CE), annotated in blue, and the output enable signal (OE), annotated in red, control whether a particular memory is enabled for testing.

FIG. 1



EX1005, Abstract, 36:57-68, 37:1-20, FIG. 1; EX1003, ¶85.

A POSITA would have understood that the chip enable terminals (E1 and E2) are used to enable or disable normal operation for each of the memories.

EX1003, ¶86; See EX1005, 36:2-25, 8:53-55, 37:19-23, 37:37-39, FIG. 9. For example, when E1 is logic low and E2 is logic level high, the CE signal output

from AND-gate 25 is logic high, which exits any testing of the memory and enables the operation of I/O circuitry and column decode 16 via AND-gate 21 and OR-gate 19. EX1005, 7:37-51, 7:56-64; *see also* EX1005, 8:47-58. A POSITA also would have understood that when one of the memories is enabled for testing, each of the other memories could receive signals on the chip enable terminals to disable normal operation or alternatively could receive signals on the chip enable terminals to allow normal operations. EX1003, ¶86; *see* EX1005, 36:2-25, 8:53-55, 37:15-25, 37:37-39, 18:46-53, FIG. 9.

Additionally, a POSITA would have understood that the output enable (OE) terminal is used to enable a memory during testing. EX1003, ¶87; EX1005, 37:15-19. Indeed, Slemmer explains that the output enable (OE) signal serves as a chip enable during testing, which is useful for systems in which multiple memories are installed. EX1005, 37:15-19. As shown in the figure above by the annotations in red, the OE signal is input into both AND-gate 26 and AND-gate 21. EX1005, FIG. 1. The output of AND-gate 26 controls the output buffers 22 via line 24 and the output of AND-gate 21 is an input to OR-gate 19, which provides an enable signal for the I/O circuitry and column decode 16. EX1005, FIG. 1, 37:1-15. A POSITA would have understood that the particular memory enabled for testing would receive an OE signal that is logic high, which can enable the output buffers 22 via AND-gate 26 and provide a chip enable to the I/O circuitry and column

decode 16 via AND-gate 21 and OR-gate 19. EX1003, ¶87; EX1005, FIG. 1, 37:1-15, 7:56-8:3. A POSITA would also have understood that the other memories disabled for testing would receive OE signals that are logic low, which disables the output buffers 22 via AND-gate 26 and can provide a chip disable to the I/O circuitry and column decode 16 via AND-gate 21 and OR-gate 19. *Id.*

Accordingly, a POSITA would have understood that one of the multiple memories 1 in Slemmer is enabled for testing whereas the remaining memories are disabled, and thus, the enabled memory is to be tested independent from the other memories (“*one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components*”) EX1003, ¶¶82-88; EX1005, 37:1-37, FIG. 1.

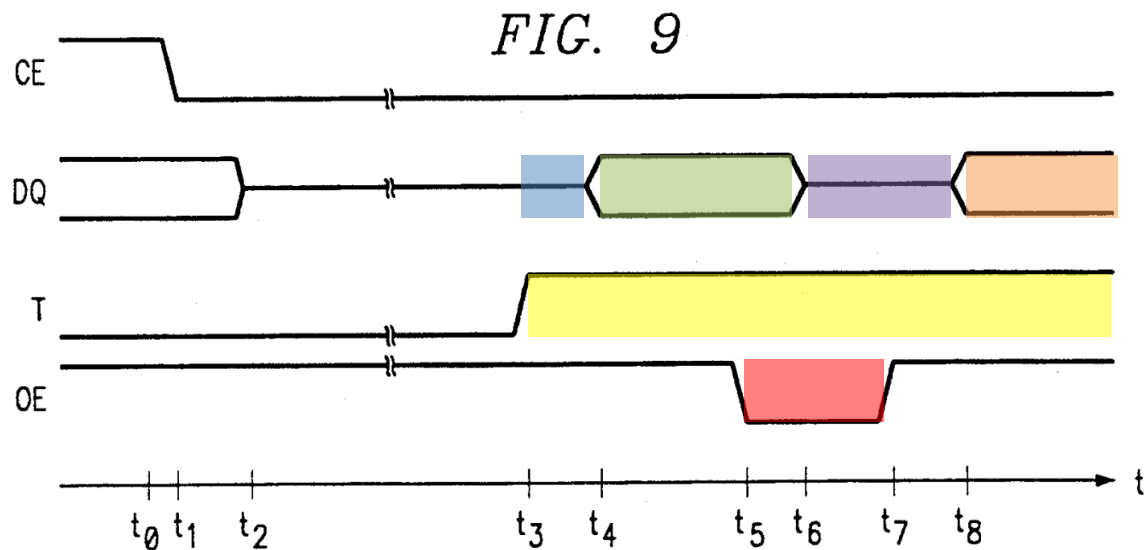
**d. [1.3] “said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.”**

Slemmer teaches that the memory 1 is configured to enter the special test mode during which a data I/O (DQ) terminal<sup>2</sup> is in a high-impedance state and certain times, in which no data is output to the bus via the terminal and the

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<sup>2</sup> Although Figure 9 shows one DQ terminal, Slemmer teaches one *or more* of the DQ terminals can be used during testing. EX1003, ¶89; EX1005, 36:49-54.

corresponding driver (“*outputting no data to said bus*”). EX1005, 36:10-25, FIG. 9; EX1003, ¶90; *see also* EX1001, 5:45-48; EX1013, 1:11-16. As shown in the figure below, testing is enabled at time  $t_3$  by the assertion of the ‘T’ signal to a high logic level (annotated in yellow) and the DQ terminal is initially in a high-impedance state (in blue).



EX1005, FIG. 9, 36:10-25. The DQ terminal is also in the high-impedance state between times  $t_6$  and  $t_8$  (in purple). *Id* at 37:27-32; EX1003, ¶¶90-91.

Further, to the extent the claimed phrase “*outputting data ... other than data which would be output ... during normal operation*” has objective boundaries<sup>3</sup>, it is taught by Slemmer. EX1003, ¶¶92-93. Although the ’473 Patent does not explain

<sup>3</sup> Xilinx reserves the right to challenge this claim limitation under 35 U.S.C. § 112 in other proceedings.

how to distinguish between data output to the bus “during normal operation” from “other” data output to the bus during testing (*see, e.g.*, EX1001, 3:32-38, 5:58-6:49, 5:56-57, 5:59-67, 6:22-26), Patent Owner has interpreted this limitation as data on the “DQ Feedback” line, as shown below:

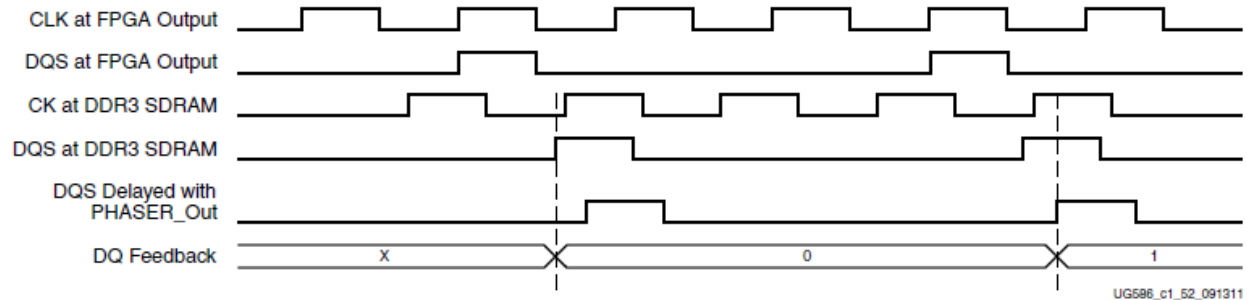
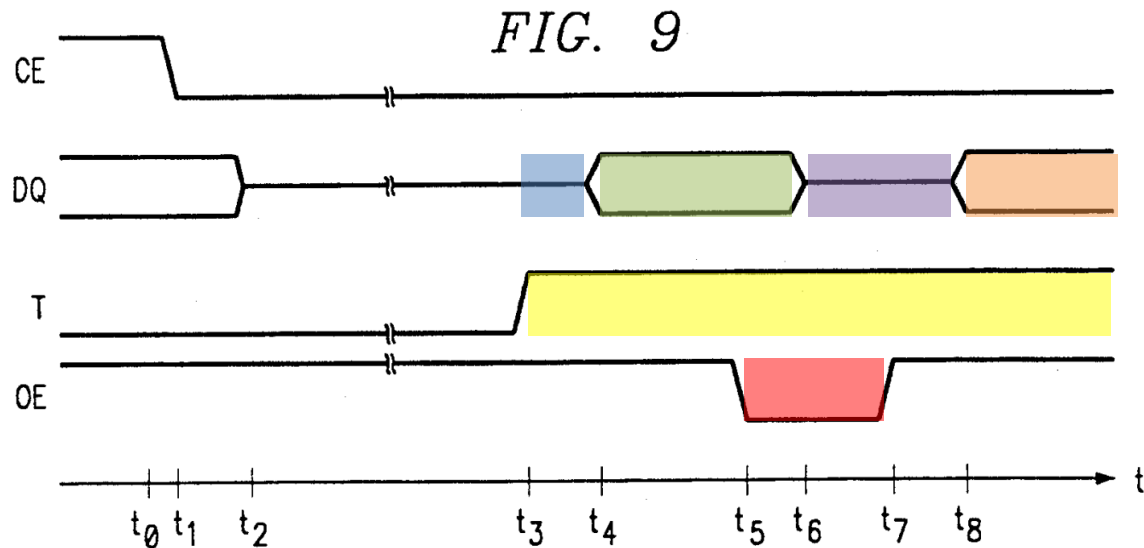


Figure 1-63: Write Leveling Timing Diagram

EX1015, 23 (FIG. 1-63) (cited by EX1014, 17); EX1003, ¶94. Specifically, the “DQ Feedback” has a don’t care value (‘X’), transitions to a ‘0’ value, and then transitions to a ‘1’ value. *Id.*

Under Patent Owner’s interpretation, Slemmer also teaches “*outputting data ... other than data which would be output ... during normal operation.*” As shown below, after testing is enabled (annotated in yellow), the DQ terminal transitions at time  $t_4$  to an active, low-impedance state (in green), in which data is output to the bus.



EX1005, 36:10-54, FIG. 9; EX1003, ¶95. The DQ terminal remains in this state until time  $t_6$ , and transitions to the same state again at time  $t_8$  (annotated above in orange) in response to the OE terminal going high at time  $t_7$ . EX1005, 37:33-37, FIG. 9. Slemmer explains that the data output is for acknowledging test information, such as an acknowledgement of test mode entry (*id.* at 36:41-45) or an “identification of which test mode has been enabled” (*id.* at 36:45-49). EX1003, ¶95. Further, the data output during Slemmer’s active state in testing is data that is different than the data which would be output during normal operation, because normal operation is a different mode of operation of the memory (*see, e.g.*, EX1005, 1:60-67), because Slemmer discloses that the terminals DQ have a different function in normal operation than during testing (*see, e.g.*, EX1005, 37:40-51, 5:58-61, 8:59-61), and because Slemmer’s disclosure is similar to Patent Owner’s allegations discussed above. *See* EX1003, ¶¶96-97.

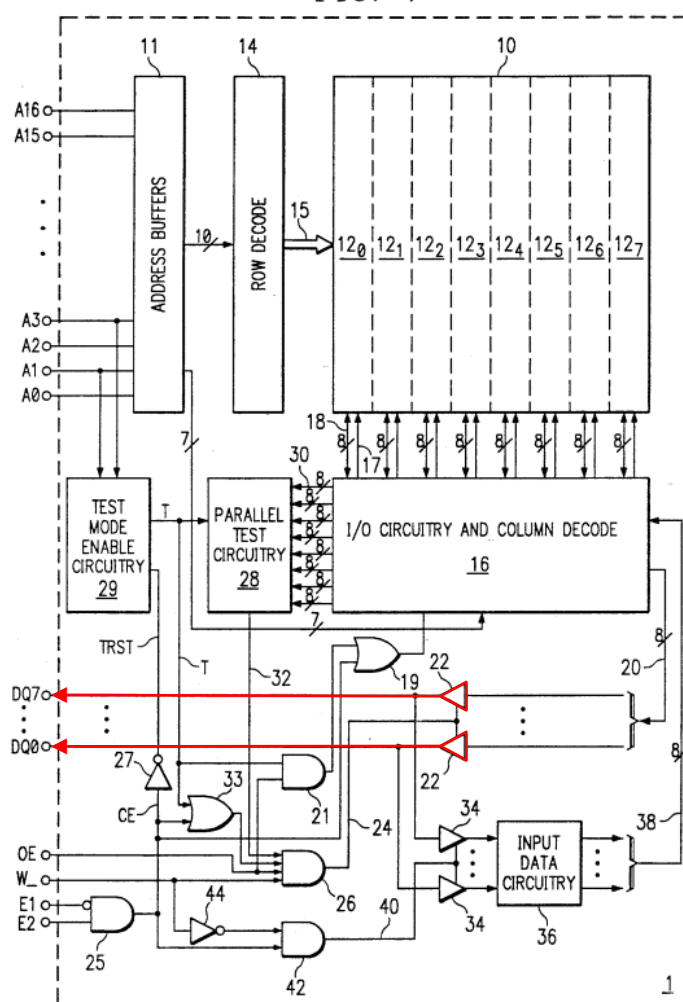
Thus, the memory to be tested in FIG. 9 is configured to perform several operations during testing, including an operation to output no data to the bus via the DQ terminal(s) (when in a high-impedance state) and an operation to output test information to the bus via the DQ terminal(s) (when in a low-impedance state). EX1003, ¶¶89-97. Accordingly, Slemmer teaches this limitation. *Id.*

**2. Claim 2: “The electrical circuit according to claim 1, wherein said circuit component to be tested includes output drivers for outputting data to said bus, said output drivers being deactivated during testing of said circuit component to be tested.”**

As explained above for claim [1.1], Slemmer teaches that the data I/O and/or address connections are connected to signal lines and that one or more signal lines are a “bus.” *Supra* §X.A.1.b; *see, e.g.*, EX1005, 35:22-42, 37:11-37; EX1003, ¶98.

Slemmer also teaches that the memory includes output drivers that output data to the bus (“*circuit component to be tested includes output drivers for outputting data to said bus*”). EX1003, ¶99. As shown below, each line of an internal data bus 20 of the memory is received by an output buffer 22 that drives the correct data to a data output terminal (e.g., DQ0), which is connected to the external bus.

FIG. 1



EX1005, FIG. 1, 7:26-30; EX1003, ¶99. A POSITA would have understood that the output buffers 22 in Slemmer are output drivers (of which any two or more are “*output drivers for outputting data to said bus*”) because they are responsible for driving input data to an output provided externally. EX1003, ¶99; *see, e.g.* EX1013, 1:11-16.

Further, Slemmer teaches that the output buffers 22 are “*deactivated during testing of said circuit component to be tested.*” EX1003, ¶100. Slemmer explains

“[e]ach of the output buffers 22 are enabled by a signal on line 24 from AND gate 26.” EX1005, 7:30-31. Specifically, the “signal on line 24 [] controls whether the logic level on output data bus 20 is presented at terminals DQ, or if output buffers 22 present a high-impedance state to terminals DQ.” *Id.*, 7:31-34. A POSITA would have understood that the output buffers 22 are not active (i.e., deactivated) when they present a high-impedance state at the terminals, because they do not output data to the terminal that is connected to the bus. EX1003, ¶100; *see, e.g.*, EX1001, 5:46-49, 6:52-53; EX1005, 36:27-35, Fig. 9; EX1013, 1:11-16.

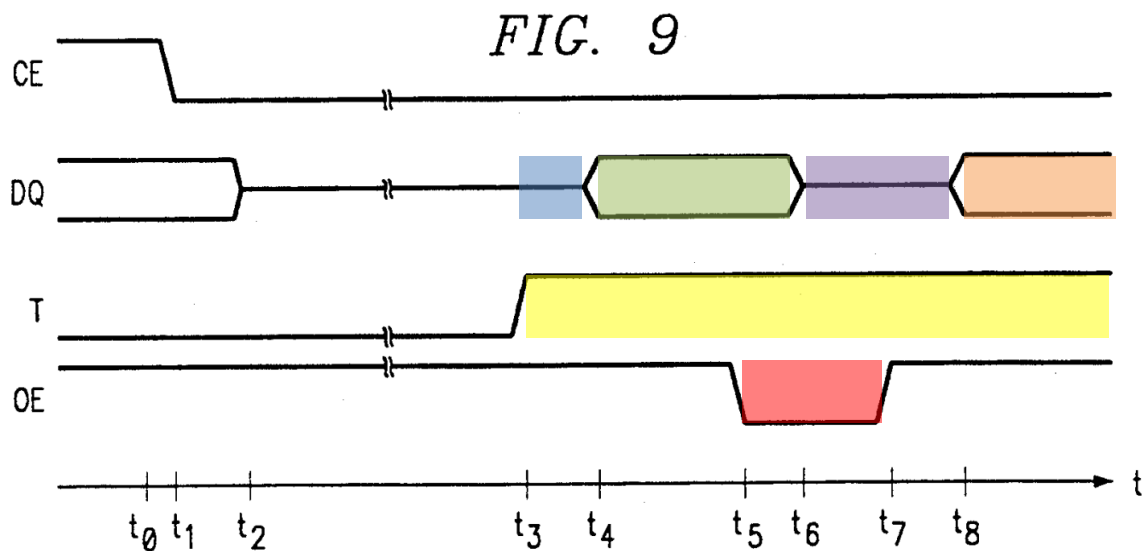
During testing, a POSITA would have understood that one or more output drivers in Slemmer would be activated to acknowledge the test mode entry (*see* EX1005, 36:49-54), whereas the remaining output drivers would remain deactivated. EX1003, ¶101; *see* EX1005, 36:22-54, FIG. 9. Slemmer explains that “not all of the output buffers . . . need be controlled” to acknowledge the test mode entry, as it “can be adequately communicated by a selected one of terminals DQ presenting a low impedance state.” EX1005, 36:49-54. Slemmer also explains that when memory 1 is selected for testing and not enabled for normal operation, the “terminals DQ are expected to remain in a high impedance state.” *Id.*, 36:31-36, 36:10-21. Accordingly, a POSITA would have understood that one of the terminals (e.g., DQ0) would be in a low-impedance state, with the output buffer 22 activated, to acknowledge the test mode entry, whereas the remaining terminals (e.g., DQ1 to

DQ7) would be in a high-impedance state, with the output buffers 22 deactivated.

EX1003, ¶¶99-101. Thus, Slemmer teaches claim 2 for this reason alone. *Id.*

Further, a POSITA would also have understood that even for the output buffers(s) in Slemmer that are activated at certain times during testing to acknowledge the test mode, they are deactivated at other times during testing.

EX1003, ¶102. As explained above for claim [1.3], the buffer(s) 22 for the DQ terminal(s) that are in a low-impedance state with activated buffers at certain times during testing, are in a high-impedance state with deactivated buffers at other times during testing, such as between times  $t_6$  and  $t_8$  as shown in purple in the figure below or when there is an error during testing. *Supra* §X.A.1.d; EX1005, 36:10-54 (times  $t_1$  to  $t_4$ ), 37:27-39 (times  $t_5$  to  $t_8$ ), FIG. 9 (below), 7:26-34, 8:20-42; EX1003, ¶¶102-03.



Thus, a POSITA would have understood that these one or more buffers (e.g., that are activated at certain times during testing to acknowledge test mode entry), are also deactivated (with a high-impedance state at the DQ terminal(s)) at other times during testing. EX1003, ¶¶102-03. For this additional reason, Slemmer teaches claim 2. *Id.*

**3. Claim 3: “The electrical circuit according to claim 2, wherein said output drivers are deactivated by a test unit<sup>4</sup> which is testing said circuit component to be tested.”**

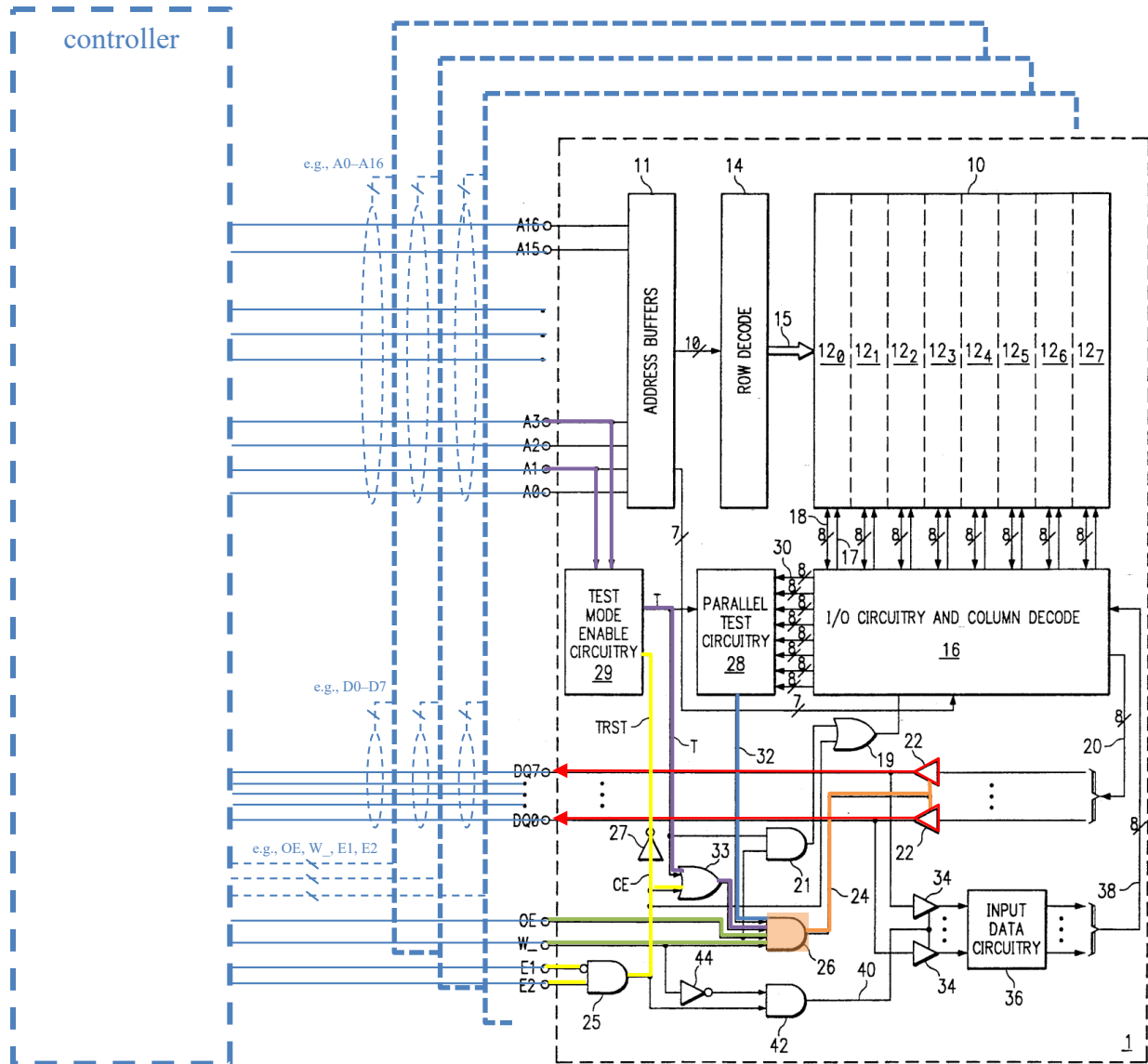
As explained for claim 2, Slemmer teaches the memory includes multiple output buffers 22 (“*output drivers*”) that are deactivated during testing. *Supra* §X.A.2; EX1005, 36:22-54, FIGS. 1, 9; EX1003, ¶104. As explained below, Slemmer also teaches that the output drivers are deactivated by an external controller, TMEC 29, and/or PTC 28, any one or combination of which is “*a test unit*” that is testing the memory 1 (“*which is testing said circuit component to be tested*”). EX1003, ¶105; EX1005, FIGS. 1, 9. Specifically, externally driven inputs from the controller configure the memory for testing, which results in the deactivation of the output drivers. EX1003, ¶106; *see* EX1005, 9:19-30, FIG. 1. In addition, the inputs are provided to TMEC 29, which controls entry into and exit

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<sup>4</sup> The test unit in the ’473 Patent can be part of the circuit component to be tested and is illustrated as such in all figures. *See, e.g.*, EX1001, 5:11-18, FIGS. 1-3.

from testing, and uses PTC 28 to determine results during testing and control the output of test information on one or more output driver(s). EX1003, ¶106; *see* EX1005, 8:32-47, 9:19-30, 18:46-57, 36:10-16, 36:27-41.

As shown below, Slemmer discloses that the output of AND-gate 26 via signal line 24 (annotated in orange) controls whether the output buffers 22 (in red) are activated to present output data with a low-impedance state or deactivated to present a high-impedance state at terminals DQ.



EX1003, ¶107; EX1005, FIG. 1, 7:30-35, 34:54-57.

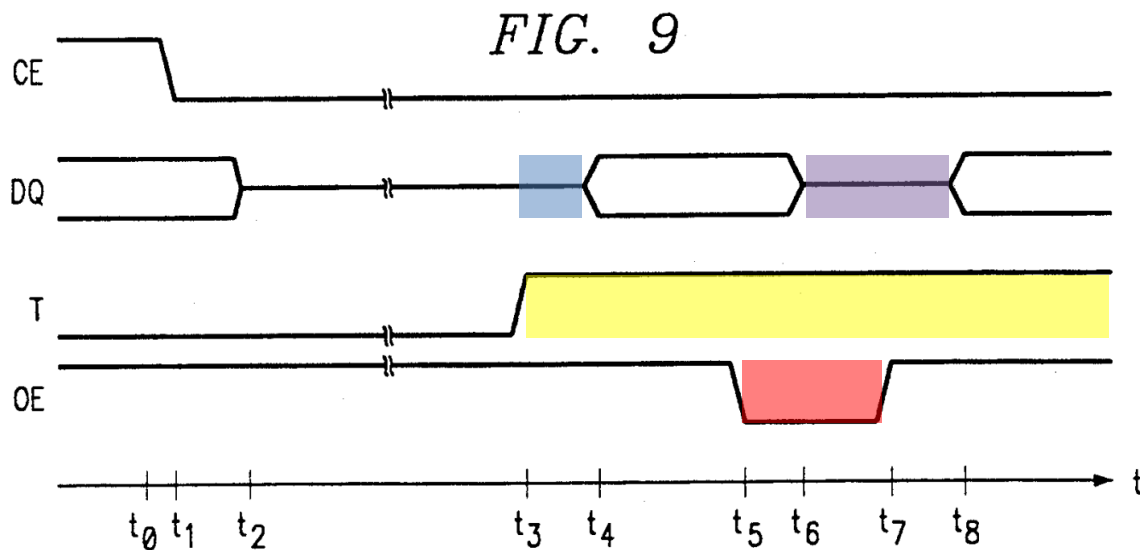
The output of AND-gate 26 is a function of its four inputs that are directly or indirectly provided by the controller, TMEC 29, or PTC 28. EX1003, ¶108. The controller directly provides the write enable (W\_) and output enable (OE) signals for two inputs (each annotated in green). See EX1005, 8:4-14, 35:65-36:2, 37:11-39. The controller also indirectly provides a third input (in purple) for the test (T)

and chip enable (CE) signals via external inputs (A1, A3, E1, and E2), in which the A1/A3 signals (in purple) enable testing and the E1/E2 signals (in yellow) disable normal operation of the chip for testing. EX1003, ¶108; *see* EX1005, 9:19-30, 18:46-57, 36:10-16.

The third input to the AND-gate (annotated in purple) is also provided indirectly by TMEC 29, which generates a signal (T) when testing is enabled via the A1/A3 terminals. EX1003, ¶109; EX1005, 9:19-30. Finally, the PTC 28 provides the fourth input (annotated in blue) via signal line 32 to signal test information. EX1003, ¶109; EX1005, 8:32-47, 36:27-41. Accordingly, a POSITA would have understood that any one or combination of the controller, TMEC 29, and/or PTC 28 are “*a test unit which is testing said circuit component to be tested.*” EX1003, ¶109.

A POSITA would also have understood that any one or combination of the controller, TMEC 29, and/or PTC 28, deactivate the output drivers during testing. EX1003, ¶110. As explained above for claim 2, a POSITA would have understood that one or more output drivers in Slemmer would be deactivated at certain times during testing to acknowledge the test mode, whereas the remaining output drivers would remain deactivated throughout testing. EX1003, ¶110; EX1005, 36:10-54, FIG. 9; *supra* §X.A.2. Specifically, the controller deactivates the one or more output drivers when the write (W\_) or output enable (OE) inputs are driven low.

EX1003, ¶110; EX1005, 8:4-14, 35:65-36:2, 37:11-39. For example, Slemmer teaches that the OE signal is used as a chip select during testing to activate or deactivate output driver(s) to provide test information, such as an acknowledgement of the test mode. EX1003, ¶110; EX1005, 7:68-8:3, 8:14-19, 8:55-58, 36:55-68, 37:11-39. As shown in the figure below, the OE terminal is driven low at time  $t_5$  (shown in red), which results in the output driver being deactivated at time  $t_6$  with a high-impedance state at the DQ terminal (shown in purple).



EX1005, 36:10-54, 37:27-39, FIG. 9; EX1003, ¶110. Thus, a POSITA would have understood that the output driver(s) deactivated at certain times during testing are deactivated externally by the controller. EX1003, ¶110.

In addition, a POSITA would have understood that the output drivers that remain deactivated throughout testing are deactivated by the controller.

Specifically, the controller deactivates the output drivers when the chip enable (CE) signal is low by driving specific values on the E1 and E2 inputs during testing. EX1003, ¶111; EX1005, 36:2-16, FIGS. 1, 9. As shown above, the CE signal is driven low at time  $t_1$  and in response the output driver is deactivated at time  $t_2$ . EX1005, 36:10-40, FIG. 9; EX1003, ¶111.

Further, Slemmer teaches that the PTC 28 deactivates the output drivers during testing when the test result indicates an error. EX1003, ¶112; EX1005, 7:30-35, 8:20-42, FIG. 1. Slemmer discloses that signal line 32 from PTC 28 is driven to a “low logic level in test mode when there is an error.” EX1005, 8:37-42. A POSITA would have understood that a low logic level on signal line 32 would result in the deactivation of the output buffer(s) 22, because signal line 32 is one of the four inputs to AND-gate 26 and because AND-gate 26 provides a signal on line 24 to control the output buffer(s). EX1003, ¶112; EX1005, FIG. 1, 7:30-35, 8:20-23.

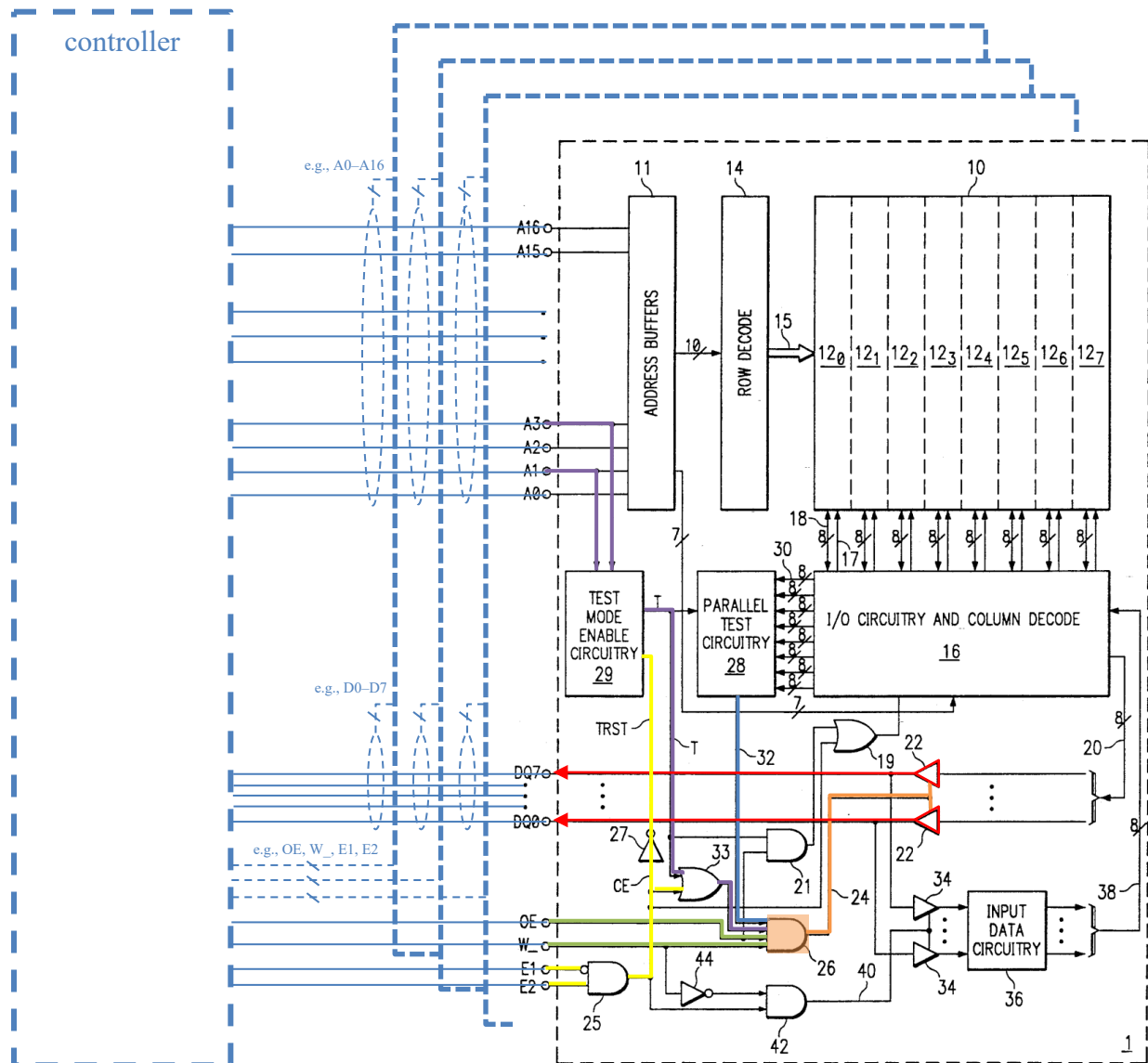
Thus, the output drivers are “*deactivated by*” any one or combination of the controller, TMEC 28, and/or PTC 29 ( “*a test unit*”). EX1003, ¶¶104-113.

#### **4. Claim 4**

**a. “The electrical circuit according to claim 3, comprising a device selected from the group consisting of a**

**logic unit and a selection circuit, said device for deactivating said output drivers, said device ensuring:” [4.1]**

As shown below, the electrical block diagram in Slemmer includes logic (annotated in orange below) that provides a signal on line 24 to activate or deactivate the output buffers 22.



EX1003, ¶114; EX1005, FIG. 1, 7:22-55, 8:47-55. The logic includes AND-gate 26, which receives four inputs and provides an output on line 24. *Id.* Accordingly,

a POSITA would have understood that Slemmer's logic is "*a device selected from the group consisting of a logic unit and a selection circuit*" because it discloses an AND-gate 26 that is "*a logic unit.*" EX1003, ¶¶114-16; *see* EX1001, 6:4-9, 7:60-65 (disclosing logic unit with an AND gate), FIGS. 1-2; EX1016, Abstract, 2:7-18, 3:17-23, 3:24-4:38, FIGS. 1, 2A-2F; EX1017, Title, 6:64-7:17, FIGS 2B-2C. A POSITA would also have understood that the logic deactivates the output drivers because its output is provided as the control input to Slemmer's output buffers 22 that disables the buffers when the control input has a low logic level. EX1003, ¶114; EX1005, FIG. 1, 7:26-34, 8:8-14. Thus, Slemmer teaches this limitation. EX1003, ¶¶114-17.

**b. "that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device which controls said bus, and" [4.2]**

Slemmer teaches this limitation. EX1003, ¶¶118-21. As explained above, the output drivers (buffers 22) are controlled via line 24 by AND-gate 26. *Supra* §X.A.4.a. As shown below, an external controller ("*bus control device*") drives an output enable (OE) signal ("*an enable signal*") to the memory ("*circuit component to be tested*") to control the output drivers via AND-gate 26.



*be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device”). Id.*

Additionally and alternatively, Slemmer teaches that the “*enable signal*” is any combination of OE, E1, E2, and/or W\_. EX1003, ¶120. As shown in the figure above, the external controller (“bus control device”) supplies the OE signal, the chip enable (E1/E2) signals, and a write enable (W\_) signal to control the output buffers 22 via AND-gate 26. EX1003, ¶120; EX1005, FIG. 1. As annotated in green, the output enable (OE) and write enable (W\_) signals provide two inputs to AND-gate 26 (annotated in orange). *Id.* During normal operation, the write enable signal has a high logic level for read operations and a low logic level for write operations, and the output enable signal enables and disables the output from the memory. EX1005, 8:4-19; EX1003, ¶120. Further, as shown by the annotations in yellow, the chip enable signals E1/E2 control a third input to AND-gate 26 via AND-gate 25 and OR-gate 33. EX1003, ¶120; EX1005, FIG. 1. During normal operations, when terminal E1 is logic low and terminal E2 is logic high, the CE signal that is output from AND-gate 25 is logic high. EX1003, ¶120; EX1005, FIG. 1, 7:35-51, 8:49-55. The CE signal is input to OR-gate 33, which outputs a logic high signal when the CE signal is logic high. *Id.* Thus, Slemmer teaches that during normal operation its output buffers are controlled based on any combination of the output enable (OE), chip enable (E1/E2), and/or write enable (W\_) signals which is

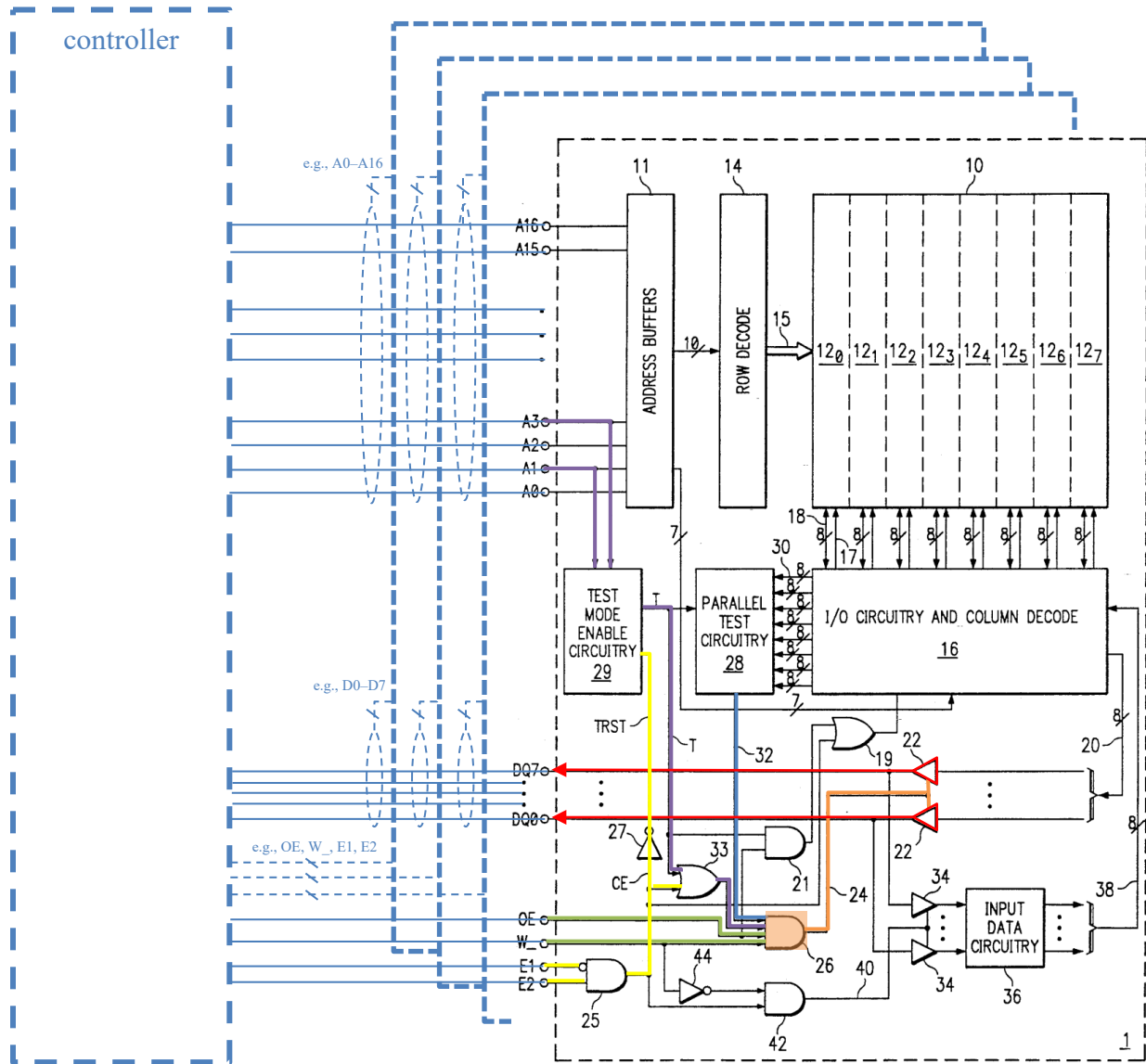
supplied to the memory to be tested by the memory controller (“*that during normal operation of said circuit component to be tested, said output drivers are controlled based upon an enable signal which is supplied to said circuit component to be tested by a bus control device*”).

Further, a POSITA would have understood that the controller taught by Slemmer is a bus control device “*which controls said bus*” because it outputs signals to control which devices connected to the bus are enabled or disabled (e.g., via the chip enable signals E1/E2), which device(s) connected to the bus are configured for read or write operations (e.g., via the W<sub>-</sub> signal), and which devices connected to the bus have their outputs enabled or disabled (e.g., via the OE signal). EX1003, ¶121; EX1005, FIG. 1, 7:35-51, 8:4-19, 8:49-55; *see also* EX1005, 36:55-64.

**c. “that during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested.” [4.3]**

As explained above for claim 3, Slemmer teaches that the output drivers are controlled (e.g., deactivated) by a test unit (any one or combination of an external controller, TMEC 29, and/or PTC 28) via AND-gate 26. *Supra* §X.A.3; EX1003, ¶122; EX1005, 7:30-35, 7:68-8:47, 8:55-58, 9:19-30, 18:46-57, 35:65-36:58, 37:11-39, FIGS. 1, 9.

As shown below, the TMEC 29 provides a test signal on line T (annotated in purple) that is input to OR-gate 33, which provides its output as an input to AND-gate 26.



EX1003, ¶123; EX1005, FIG. 1. When testing is enabled, TMEC 29 drives the test signal on line T to a high logic level. EX1005, 8:47-49. This causes the output of OR-gate 33 to go to high logic level, which is provided as an input to AND-gate

26. See EX1005, 8:49-55; EX1003, ¶123. Additionally, a high logic level on line T also causes PTC 28 to perform operations and controls the enabling of input/output circuit and column decoder 16 via AND-gate 21 and OR-gate 19. EX1005, 8:32-37, 7:56-68; EX1003, ¶123. Thus, Slemmer teaches that during testing of memory 1, the output buffers are controlled based upon a test signal on line T which the TMEC 29 supplies to the memory (“*during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested*”). EX1003, ¶123.

Additionally, as shown in the figure above, PTC 28 provides a signal on line 32 that is directly input to AND-gate 26 to control whether the output buffers 22 are activated or deactivated. EX1003, ¶124; EX1005, FIG. 1. For example, Slemmer explains that when there is an error during testing, PTC 28 drives line 32 to a logic low level, which would deactivate the output buffers. See EX1005, 8:38-42; EX1003, ¶124; *see also* EX1005, 8:32-37, 36:27-31, FIG. 9. Thus, Slemmer teaches that during testing of memory 1, the output buffers are controlled based upon a signal on line 32 which the parallel test circuitry (PTC) 28 supplies to the memory (“*during testing of said circuit component to be tested, said output drivers are controlled based upon a test control signal which the test unit supplies to said circuit component to be tested*”). EX1003, ¶124.

Thus, a POSITA would have understood the test signal on line T (output from TMEC 29) and the signal on line 32 (output from PTC 28) are individually and collectively a “*test control signal which the test unit supplies to said circuit component to be tested.*” EX1003, ¶¶122-25.

**5. Claim 5: “The electrical circuit according to claim 4, wherein said device is said logic unit, said logic unit providing an output signal resulting from a logical combination of the enable signal and a<sup>5</sup> test control signal.”**

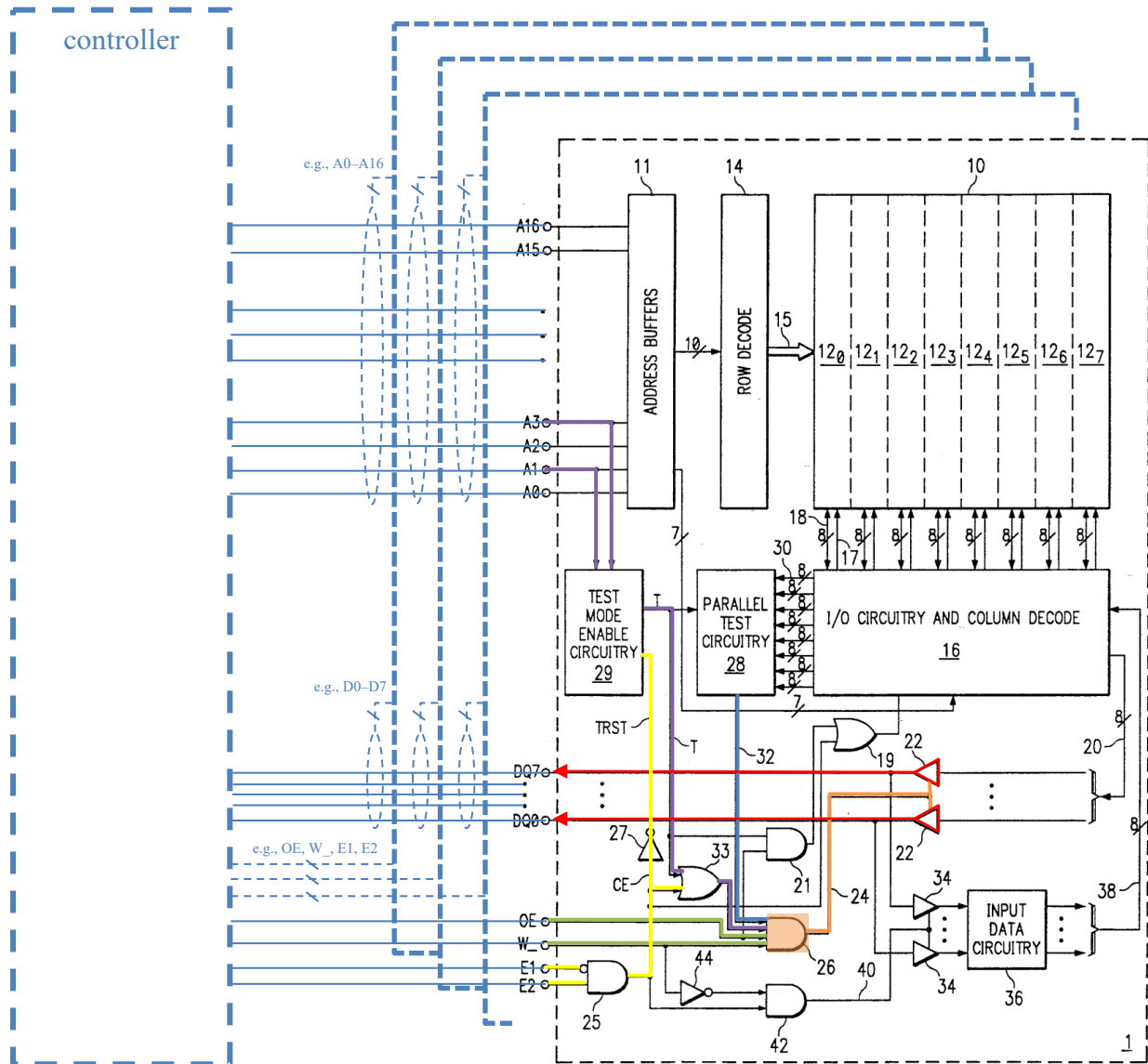
As explained for claim 4, the “*device*” in Slemmer is a “*logic unit*” that includes AND-gate 26. *Supra* §X.A.4.a; EX1003, ¶127. Also explained above for claim 4, the “*enable signal*” in Slemmer is the output enable (OE) signal or alternatively any combination of the chip enable signals (E1/E2), write enable signal (W<sub>-</sub>), and OE signal, and the “*test control signal*” is individually and collectively the test mode signal on line T and the signal on line 32. *Supra* §§X.A.4.b-X.A.4.c; EX1003, ¶127.

As shown below, the AND-gate 26 (included in “*logic unit*”) provides an output signal on line 24 (annotated in orange) that results from a “*logical*

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<sup>5</sup> Claim 5 depends from claim 4 and recites “*a test control signal*” but appears to be referring to claim 4’s “*test control signal.*” See EX1001, 11:32-33, 11:38. To the extent it does not, Xilinx reserves the right to challenge this claim limitation under 35 U.S.C. § 112.

combination of the enable signal” (E1/E2, W<sub>-</sub>, and/or OE) and “a test control signal” (signal on line T and/or signal on line 32).



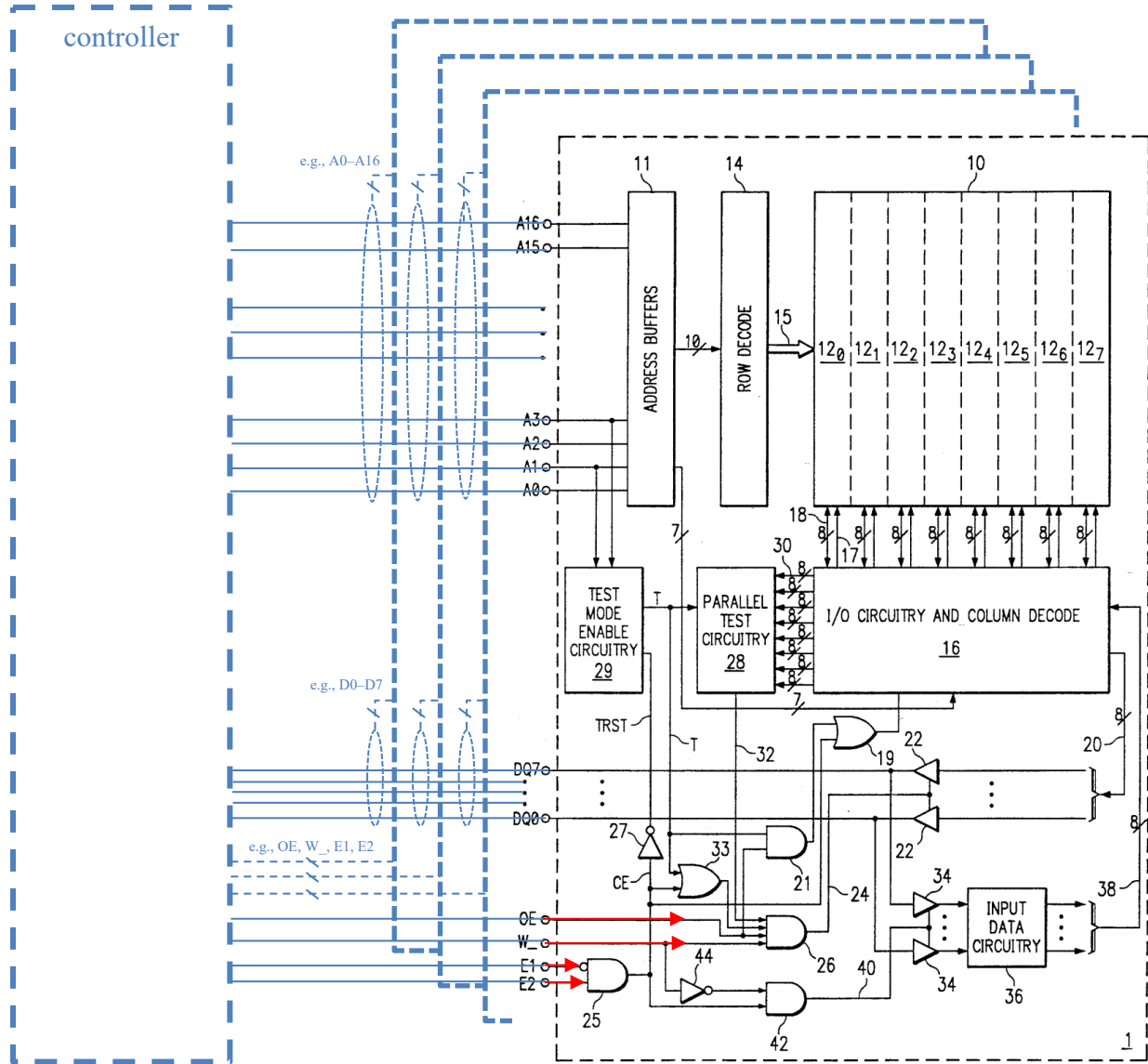
EX1003, ¶128; EX1005, FIG. 1, 7:22-55, 8:47-55. Slemmer explains that OR-gate 33 receives one input from the test mode signal on line T (annotated in purple) and another input that is based on the chip enable inputs E1 and E2, labeled chip enable (CE) (annotated in yellow). See EX1005, 36:10-16, 36:25-27, FIG. 1; EX1003,

¶128. Slemmer also explains that the AND-gate 26 receives four inputs: the signal on line 32 (annotated in blue), the output from OR-gate 33, the signal from the OE input (in green), and the signal from the W\_ input (also in green). *See* EX1005, 7:35-8:46, FIG. 1; EX1003, ¶128. Thus, Slemmer teaches claim 5. EX1003, ¶¶126-28.

**6. Claim 7: “The electrical circuit according to claim 1, comprising a bus control device for controlling said bus and for receiving a signal indicating testing of said circuit component to be tested.”**

As explained for claim [1.1], Slemmer teaches that multiple memories are connected via their terminals to a controller, such as one in a system or test equipment. *Supra* §X.A.1.b; EX1005, FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 36:55-68, 37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52; EX1003, ¶129.

Slemmer also teaches that the controller externally drives input signals that are received at the terminals of a memory 1. *Id.* As shown in the figure below, several terminals of memory 1 in Slemmer receive external input signals, including signals at the output enable (OE) terminal, write enable (W\_) terminal, and chip enable terminals (E1, E2).



EX1003, ¶130; EX1005, FIG. 1. Further, the address (e.g., A0–A16) and data (e.g., DQ0–DQ7) terminals of the memories are connected together and to the controller.

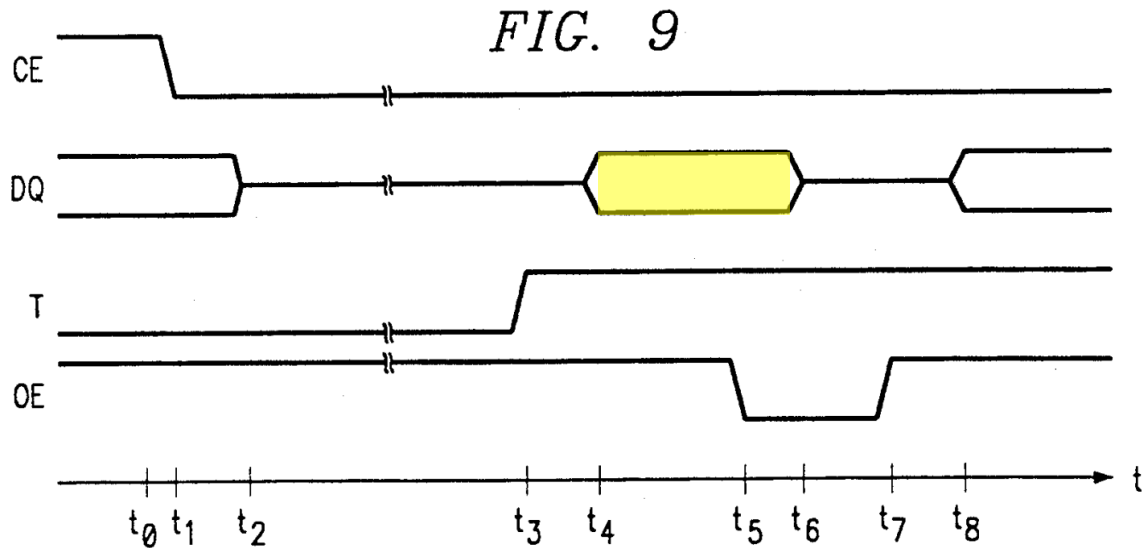
*Id.*

A POSITA would have understood that the external signals input to memory 1 that are driven by the controller serve to control the bus between the memory devices (“a bus control device for controlling said bus”). EX1003, ¶131. Slemmer

explains that the output enable (OE) terminal is “externally driv[en]” to “control the enabling and disabling of output buffers 22” and serve “as a chip enable terminal during a test mode.” EX1005, 37:11-15, 37:27-29. According to Slemmer, this function “is especially useful if a [test mode] is to be enabled when multiple memories 1 are connected in parallel and only one . . . of memories 1 is to be tested.” *Id.*, 37:15-19. Slemmer also explains that a high logic level at the write enable (W\_) terminal indicates a read operation and that a low logic level at the terminal indicates a write operation, which places “output buffers 22 in the high impedance state at their output.” *Id.*, 8:4-14. Further, Slemmer explains that the “normal operating modes [are] entered, upon selection of memory 1 by the chip enable inputs E1 and E2” (*id.*, 10:10-12) and that the “test modes may be enabled only when memory 1 is not enabled from chip enable terminals E1 and E2, i.e., when line CE at the output of AND gate 25 is at a low logic level” (*id.*, 36:3-6). Accordingly, Slemmer teaches that the OE, W\_, and E1/E2 terminals are externally driven by the controller to control the bus via, for example, enabling or disabling the memory and controlling whether the memory’s output drivers are placed in a high-impedance state or output data. EX1003, ¶131.

Further, Slemmer teaches that the controller receives “*a signal indicating testing of said circuit component to be tested.*” EX1003, ¶132. As explained for claim [1.3], Slemmer teaches that the memory communicates test information

(highlighted in yellow below), such as an acknowledgement of entry into a test mode and identification of which test mode has been enabled, via one or more DQ terminals. *Supra* X.A.1.d; EX1003, ¶132; EX1005, 36:10-54, FIG. 9 (below).



EX1005, FIG. 9. Slemmer explains that “not all of the output buffers . . . need be controlled” to acknowledge the test mode entry, as it “can be adequately communicated by a selected one of terminals DQ presenting a low impedance state.” EX1005, 36:49-54. Slemmer also explains that, if desired, additional information is output at terminals DQ, such as an “identification of which test mode has been enabled.” *Id.*, 36:45-49. For example, Slemmer discloses that the memory can support multiple testing modes (*id.*, 9:55-64), which are selected by a sequence of selection codes, such as “01011” (*id.*, 27:6-15, 4:53-56, 5:3-14). EX1003, ¶132. Accordingly, a POSITA would have understood that the controller would receive such test information, which indicates testing of the circuit

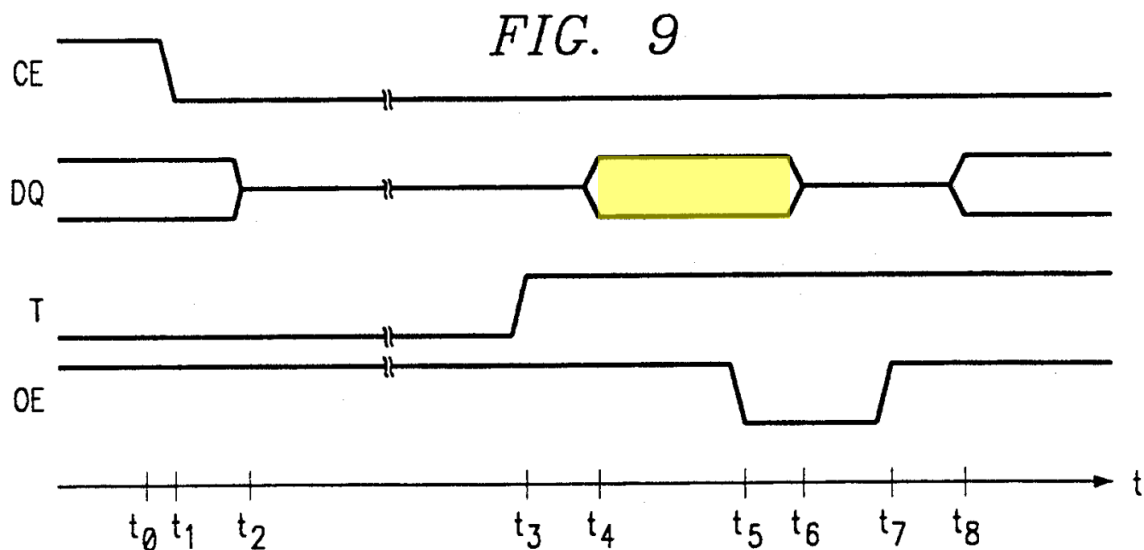
component by, for example, acknowledging entry into a test mode or identifying which test mode has been enabled, on one or more DQ terminals/lines connected between the controller and the memory. EX1003, ¶132; *see, e.g.*, EX1005, 8:14-19, 35:22-30, 36:55-64.

**7. Claim 9: “The electrical circuit according to claim 1, wherein the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is data selected from the group consisting of infrequently changing data and non-changing data.”**

To the extent this limitation has objective boundaries, it is taught by Slemmer. EX1003, ¶133; *supra* §X.A.1.d (claim [1.3]); *see, e.g.*, EX1001, 3:32-38, 5:58-6:49. As explained for claim 1, Patent Owner has pointed to data on the “DQ Feedback” line in its infringement allegations that transitions from a don’t care value to a ‘0’ value and then to a ‘1’ value. *Supra* §X.A.1.d; EX1015, 23 (FIG. 1-63) (cited by EX1014, 17); EX1003, ¶133. Patent Owner also alleges that the same data is “*infrequently changing data.*” *See id.*

Under Patent Owner’s interpretation, Slemmer also teaches “*the operation performed by said circuit component to be tested, during the testing thereof, is outputting data to said bus that is other than the data which would be output to said bus during normal operation, and the data outputted to said bus is ... infrequently changing data.*” In particular, Slemmer teaches that one or more data

terminals (e.g., DQ0-DQ7) outputs test information, such as an acknowledgement of the test mode entry, using an active state (in a low-impedance condition) (highlighted in yellow in the figure below) with either a ‘0’ or ‘1’ state. EX1003, ¶134; *see* EX1005, FIG. 9, 35:65-67, 36:41-45, 36:45-54. As explained for claim 1, the test information provided during Slemmer’s active state is different than the data which would be output during normal operation, because normal operation is a different operation mode and because the terminals have a different function in normal operation than during testing. *Supra* §X.A.1.d; EX1005, 1:60-67, 37:40-51; EX1003, ¶134. As shown below, the DQ terminal transitions from an inactive state (high-impedance condition) to an active state (low-impedance condition) at time  $t_4$  and back to an inactive state (high-impedance condition) at time  $t_6$ .



EX1005, FIG. 9, 36:22-54; EX1003, ¶134. This behavior is similar to the “DQ Feedback” line, as accused by Patent Owner, that transitions from a don’t care

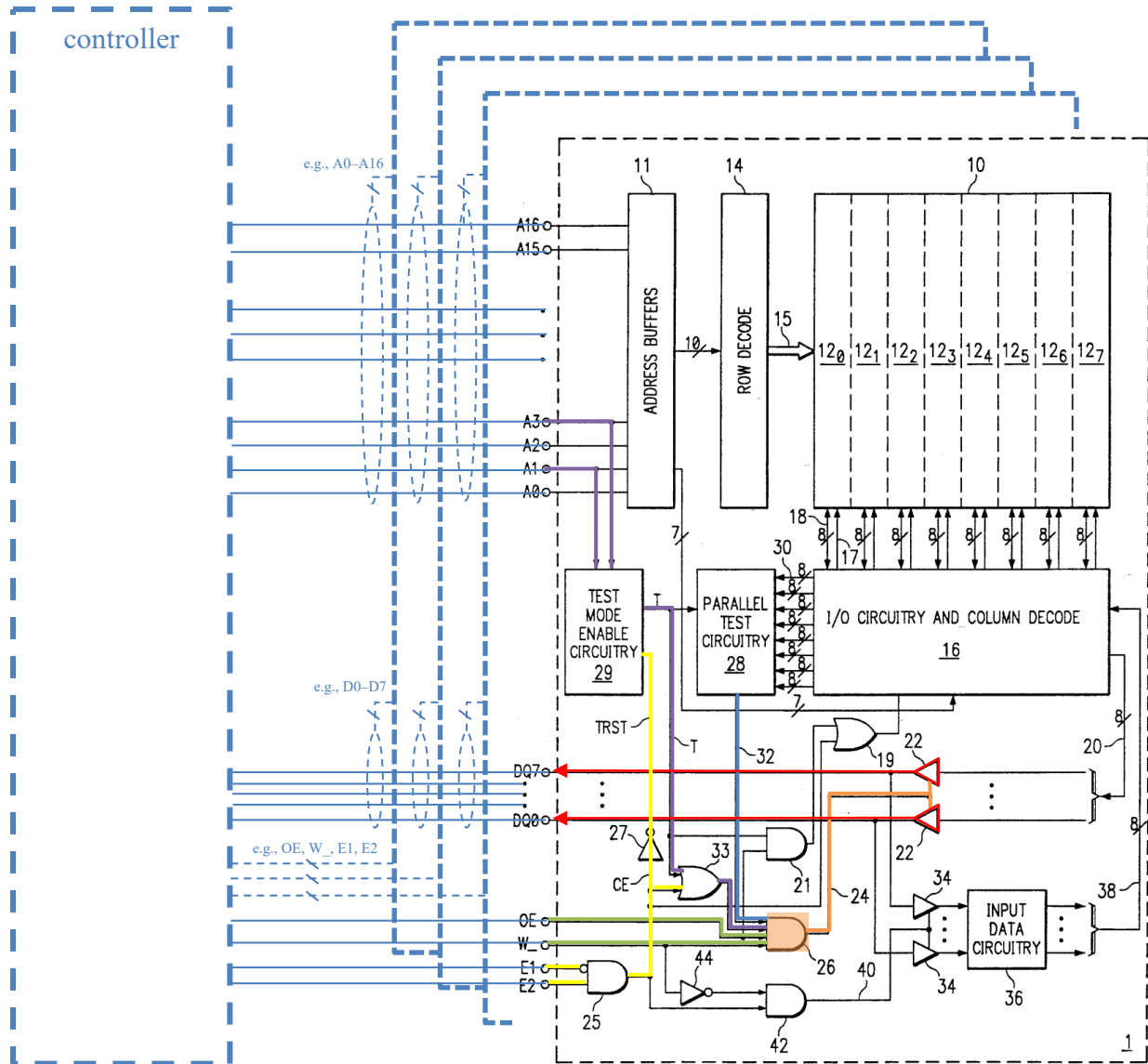
value to a ‘0’ value and then to a ‘1’ value. *See* EX1015, 23 (FIG. 1-63) (cited by EX1014, 17); EX1003, ¶134. Accordingly, Slemmer teaches claim 9 under Patent Owner’s claim interpretation.

Alternatively, Slemmer teaches that the data output to the bus is “*non-changing data*.” As shown above, the DQ terminal remains active between time  $t_4$  and time  $t_6$ . EX1005, FIG. 9. Slemmer teaches that the data state (e.g., ‘0’ or ‘1’) presented at terminal(s) DQ is unimportant because the entry into test mode is communicated by a low impedance condition on one of the terminals DQ. EX1005, 36:41-45, 36:49-54; EX1003, ¶135. Accordingly, Slemmer teaches that the logic state of the data that represents entry into testing does not change between time  $t_4$  and time  $t_6$ . EX1003, ¶135.

## **8. Claim 10**

**a. “The electrical circuit according to claim 9, comprising a device selected from the group consisting of a logic unit and a selection circuit, said device ensuring:”  
[10.1]**

As explained for claim 4, Slemmer teaches that the electrical circuit includes logic, including AND-gate 26, which is “*a device*” that is “*a logic unit*.”



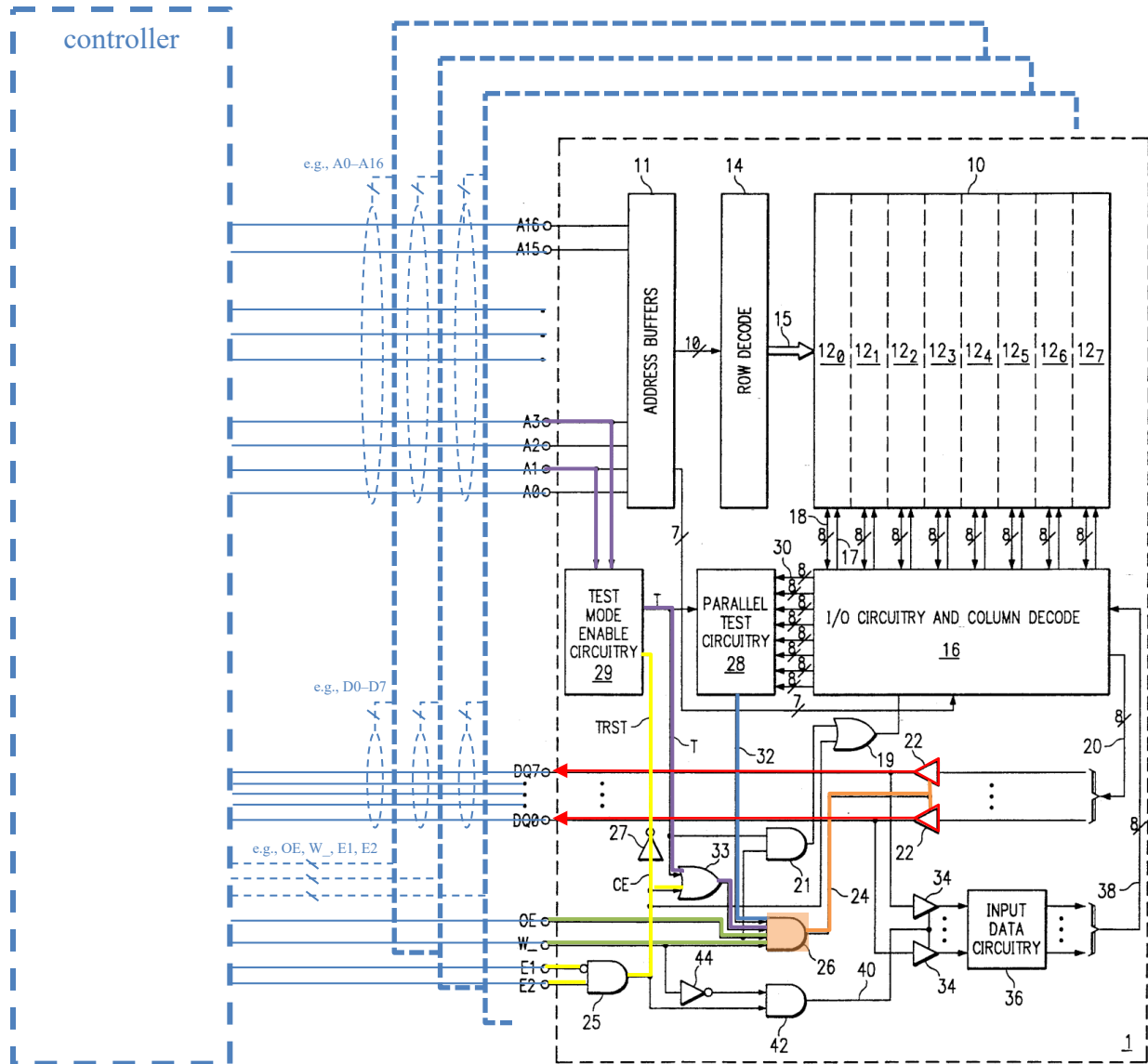
EX1003, ¶136; EX1005, FIG. 1; *supra* §X.A.4.a. Accordingly, Slemmer teaches claim [10.1] for the reasons provided above for claim [4.1]. *See id.*

**b. “that during normal operation of said circuit component to be tested, data that actually needs to be output to said bus are output to said bus, and” [10.2]**

As explained for claim 4, the output drivers of the circuit component to be tested are controlled during normal operation based on an enable signal, which is

an output enable (OE) signal or alternatively any combination of the OE signal, chip enable (E1/E2) signal, and/or write enable (W\_) signal. *Supra* §X.A.4.b; EX1003, ¶137; EX1005, FIG. 1.

Slemmer teaches that the output drivers are enabled during normal operation when the write enable signal has a high logic level for read operations, the output enable signal has a high logic level, and the chip enable signals have logical levels to enable the memory device. EX1005, 8:4-19, :35-51, 8:49-55, FIG. 1; EX1003, ¶138; *supra* §X.A.4.b. For a read operation, Slemmer teaches that the data to be output is read from the memory array and provided on internal output data bus 20 to the output buffers 22, which outputs the data because they are enabled by the enable signal.



EX1003, ¶138; EX1005, FIG. 1, 7:22-34. Thus, Slemmer teaches this limitation.

*Id.*

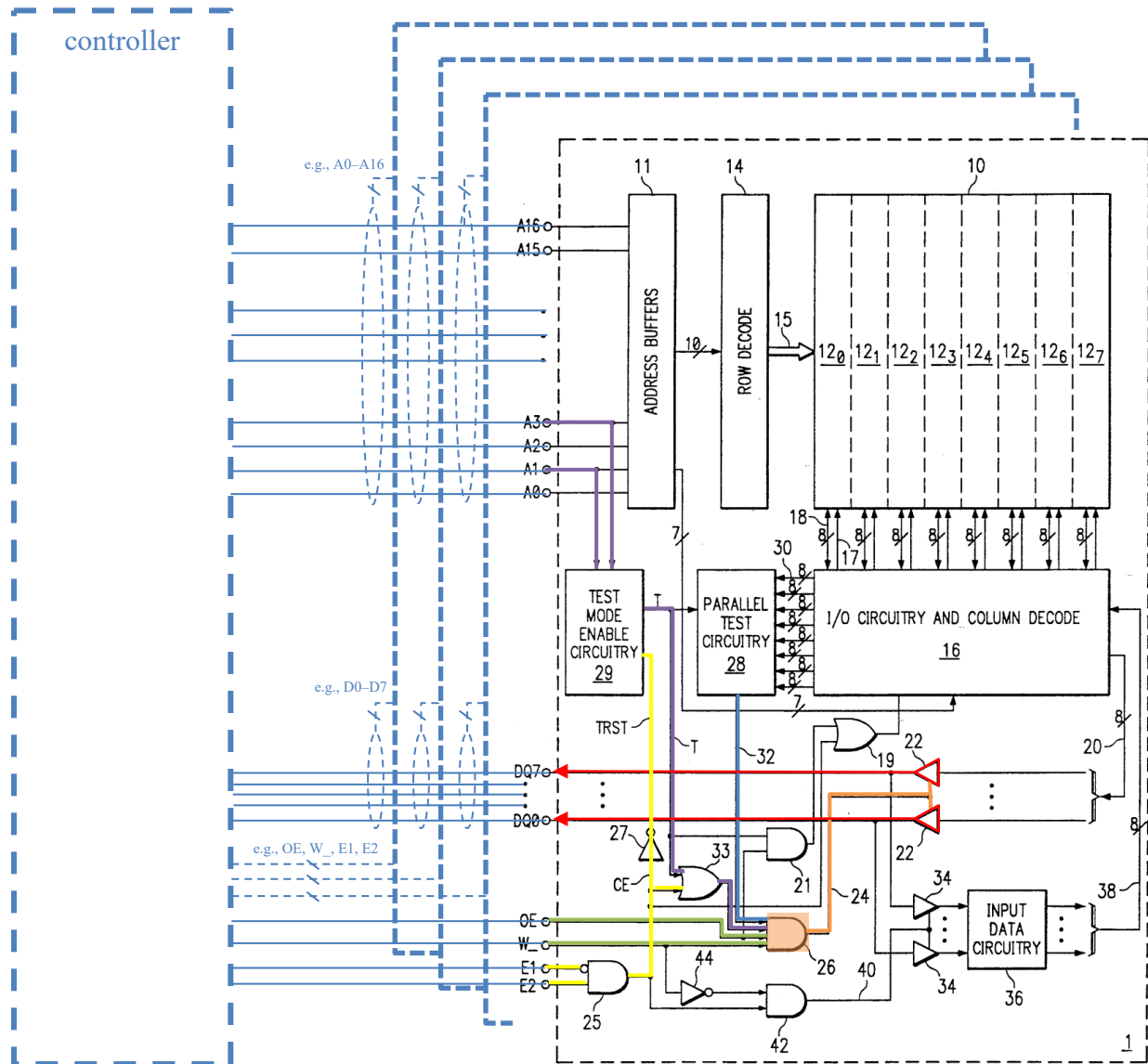
**c. “that during testing of said circuit component to be tested, the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested.” [10.3]**

As explained for claim 7, Slemmer teaches that additional information is output at terminals DQ, such as an “identification of which test mode has been

enabled” which is selected by a sequence of selection codes, such as “01011.”

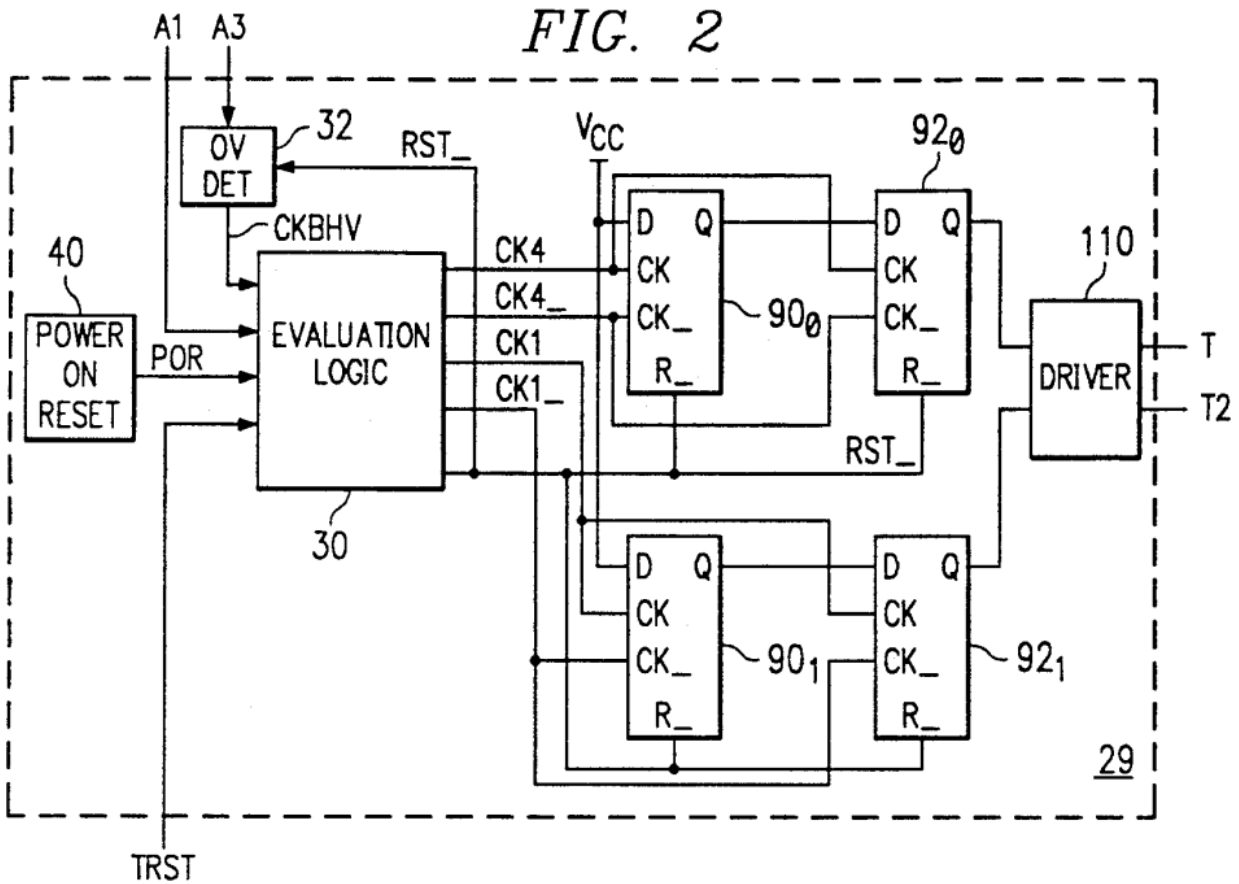
EX1005, 36:45-49, 9:55-64, 27:6-15, 4:53-56, 5:3-14; EX1003, ¶139; *supra*

§X.A.7. Further, as explained for claim 3, Slemmer teaches “a test unit” that is any one or combination of an external controller, TMEC 29, and/or PTC 28.



EX1003, ¶139; EX1005, FIG. 1; *supra* §X.A.3.

Slemmer also teaches that the test mode is determined by the test unit because TMEC 29 receives the test code and determines which of the test modes is enabled. For example, Figure 2 of Slemmer teaches that a TMEC 29 determines which of two test modes (T and T2) are enabled:



EX1005, FIG. 2; EX1003, ¶140. Slemmer also explains that many more test modes may be enabled by the logic of TMEC 29. EX1005, 9:55-64; EX1003, ¶140. For example, Slemmer discloses that five address terminals may be used with the sequence “01011” to select a particular test mode. See EX1005, 27:6-15, FIGS. 2a, 5a-5b.

Further, a POSITA would have understood from Slemmer's teachings that the identification of which test mode is enabled that is output to the bus during testing would be from the test unit (*"the data outputted to said bus is from a test unit carrying out the testing of said circuit component to be tested"*). As explained, the TMEC 29 determines which test mode is enabled. A POSITA would have understood that the sequence of selection codes, such as "01011," would provide the necessary identification of the test mode to the external controller of the memory. EX1003, ¶140; EX1005, 27:6-15, 9:55-64, FIGS. 2, 2a, 5a-5b. A POSITA would also have understood that because the TMEC 29 determines the test mode based on the selection codes, the TMEC 29 (*"test unit"*) also would provide the test mode information to be acknowledged to the external controller. EX1005, 36:45-49, 9:55-64, 27:6-15, 4:53-56, 5:3-14, FIG. 1; EX1003, ¶140; *supra* §X.A.7; *see also supra* §X.A.3 (discussing Slemmer's "test unit"). Indeed, Slemmer discloses that TMEC 29 outputs the test mode information. EX1005, 9:44-55, 7:35-45, 8:47-53, 34:58-35:6, FIGS. 1-2a; EX1003, ¶140. Thus, Slemmer teaches this limitation. EX1003, ¶¶139-40.

**9. Claim 13: "The electrical circuit according to claim 10, wherein said circuit component to be tested includes output drivers for outputting data to said bus, and each one of said**

**output drivers is provided with a device that is selected from the group consisting of a logic unit and a selection circuit.”**

**10. Claim 14: “The electrical circuit according to claim 13, wherein each one of said output drivers receives an input signal that is an output signal of said respectively provided device.”**

As explained for claim 2, Slemmer teaches that the memory includes output buffers that drive output data to the bus (“*circuit component to be tested includes output drivers for outputting data to said bus*”). *Supra* §X.A.2; EX1003, ¶141.

Further, as explained for claim 4, Slemmer teaches that the electrical circuit includes logic, including AND-gate 26, which is “*a device*” that is “*a logic unit.*”



output buffers (*“each one of said output drivers receives an input signal that is an output signal of said respectively provided device”*). Accordingly, Slemmer teaches this limitation. EX1003, ¶141.

Further, Slemmer teaches that the logic may be different between different ones of the output buffers. EX1003, ¶142. Slemmer discloses that the enabling of testing “can be adequately communicated by a selected one of terminals DQ presenting a low impedance state.” EX1005, 36:41-54. Slemmer also discloses that “additional information could be presented” at terminals DQ such as an “identification of which test mode has been enabled.” EX1005, 36:45-49. Slemmer also teaches that the terminals DQ are normally deactivated (in a high impedance state) when the chip is not enabled. EX1005, 36:31-40. Accordingly, a POSITA would have understood that other terminals DQ, that are not selected to communicate the enabling of testing, would be deactivated. EX1003, ¶142. To activate some drivers of DQ terminals while deactivating other drivers of DQ terminals, a POSITA would have understood that each of the drivers of DQ terminals would be controlled by different logic that outputs a different signal for its corresponding driver to implement its corresponding functionality during testing, such as activating or deactivating the driver of the DQ terminal (*“each one of said output drivers is provided with a device that is . . . a logic unit”*). EX1003,

¶142; *see, e.g.*, EX1005, 36:45-54. Accordingly, Slemmer teaches this limitation for this additional reason. *Id.*

## 11. Claim 20

**a. “A method for testing a circuit component which is connected to other circuit components via a bus, the method which comprises:” [20.P]**

Slemmer teaches the preamble, to the extent it is limiting, for the reasons provided above for claim limitations [1.P], [1.1], and 1.2]. *Supra* §§X.A.1.a-X.A.1.c; EX1003, ¶143.

**b. “providing a plurality of circuit components that are connected to a bus;” [20.1]**

Slemmer teaches this limitation for the reasons provided above for claim [1.2]. *Supra* §X.A.1.c; EX1003, ¶144. As explained, Slemmer teaches multiple memories connected to a bus. *Id.*; *see also* EX1005, 35:22-42, 37:11-37.

**c. “configuring at least one of the plurality of circuit components such that it can be tested independently from all others of said plurality of circuit components, the at least one of the plurality of circuit components defining a circuit component to be tested; and” [20.2]**

Slemmer teaches this limitation for the reasons provided above for claim [1.2]. *Supra* §X.A.1.c; EX1003, ¶145. As explained, Slemmer teaches that one of the memories is configured to be tested independent from the other memories by providing input signals to the terminals of the memory. *Id.*; *see also* EX1005, 36:2-25, 37:1-37, FIGS. 1, 9.

- d. “while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.” [20.3]**

Slemmer teaches this limitation for the reasons provided above for claim

[1.3]. *Supra* §X.A.1.d; EX1003, ¶146.

## **12. Claim 21**

- a. “The method according to claim 20, which comprises: providing the circuit component to be tested with output drivers for outputting data to the bus; and” [21.1]**
- b. “deactivating the output drivers during testing of the circuit component to be tested.” [21.2]**

Slemmer teaches limitations [21.1] and [21.2] for the reasons provided

above for claim 2. *Supra* §X.A.2; EX1003, ¶¶147-48.

- 13. Claim 22: “The method according to claim 21, which comprises deactivating the output drivers by a test unit which is testing the circuit component to be tested.”**

Slemmer teaches claim 22 for the reasons provided above for claim 3. *Supra* §X.A.3; EX1003, ¶149.

#### 14. Claim 23

a. **“The method according to claim 22, which comprises: providing a device for deactivating the output drivers;”** [23.1]

b. **“selecting the device from the group consisting of a logic unit and a selection circuit;”** [23.2]

Slemmer teaches limitations [23.1] and [23.2] for the reasons provided above for claim [4.1]. *Supra* §X.A.4.a; EX1003, ¶¶150-51.

c. **“using the device to ensure: that during normal operation of the circuit component to be tested, the output drivers are controlled based upon an enable signal which is supplied to the circuit component to be tested by a bus control device which controls the bus, and”** [23.3]

Slemmer teaches this limitation for the reasons provided above for claim [4.2]. *Supra* §X.A.4.b; EX1003, ¶152.

d. **“that during testing of the circuit component to be tested, the output drivers are controlled based upon a test control signal which the test unit supplies to the circuit component to be tested.”** [23.4]

Slemmer teaches this limitation for the reasons provided above for claim [4.3]. *Supra* §X.A.4.c; EX1003, ¶153.

**15. Claim 24: “The method according to claim 23, which comprises using the logic unit to provide an output signal resulting from a logical combination of the enable signal and a test control signal.”**

Slemmer teaches claim 24 for the reasons provided above for claim 5. *Supra* §X.A.5; EX1003, ¶154.

**16. Claim 26: “The method according to claim 20, which comprises signaling a bus control device which controls the bus that the circuit component to be tested is undergoing a test.”**

Slemmer teaches claim 26 for the reasons provided above for claim 7. *Supra* §X.A.6; EX1003, ¶155.

**17. Claim 28: “The method according to claim 20, wherein the operation performed by the circuit component to be tested, during the testing thereof, is outputting data to the bus that is other than the data which would be output to the bus during normal operation, and selecting the data output to the bus from the group consisting of infrequently changing data and non-changing data.”**

Slemmer teaches claim 28 for the reasons provided above for claim 9. *Supra* §X.A.7; EX1003, ¶156.

**18. Claim 29**

**a. “The method according to claim 28, which comprises: selecting a device from the group consisting of a logic unit and a selection circuit;” [29.1]**

Slemmer teaches this limitation for the reasons provided above for limitations [4.1] and [10.1]. *Supra* §§X.A.4.a, X.A.8.a; EX1003, ¶157.

**b. “using the device to ensure: that during normal operation of the circuit component to be tested, data that actually needs to be output to the bus are output to the bus, and” [29.2]**

Slemmer teaches this limitation for the reasons provided above for limitations [4.2] and [10.2]. *Supra* §§X.A.4.b, X.A.8.b; EX1003, ¶158.

**c. “that during testing of the circuit component to be tested, the data outputted to the bus is from a test unit**

**carrying out the testing of the circuit component to be tested.” [29.3]**

Slemmer teaches this limitation for the reasons provided above for claims 3, 7 and limitations [10.3]. *Supra* §§X.A.3, X.A.6, X.A.8.c; EX1003, ¶159.

**19. Claim 32**

**a. “The method according to claim 29, which comprises: providing the circuit component to be tested with output drivers for outputting data to the bus; and” [32.1]**

**b. “providing each one of the output drivers with a device that is selected from the group consisting of a logic unit and a selection circuit.” [32.2]**

**20. Claim 33: “The method according to claim 32, wherein each one of the output drivers receives an input signal that is an output signal of the respectively provided device.”**

Slemmer teaches the limitations of claims 32 and 33 for the reasons provided above for claims 2, 4, 13, and 14. *Supra* §§X.A.2-X.A.4, X.A.10, X.A.11; EX1003, ¶¶160-62.

**B. Ground 2: Claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 are obvious over Slemmer and Gasbarro**

**1. Motivation to Combine Slemmer and Gasbarro**

Ground 2 combines Slemmer with Gasbarro. As explained below, Gasbarro teaches how to implement a memory system that balances impedances to support expandable memory while avoiding signal reflections and increased line noise. EX1003, ¶163.

A POSITA would have been motivated to combine Slemmer with Gasbarro, and had a reasonable expectation of success in doing so. EX1003, ¶¶163-69. Both references relate to the field of memories and memory systems. *See* EX1005, 1:6-8, 3:7-16, 36:64-68; EX1006, 1:6-9, FIG. 1. Slemmer discloses a bus with bi-directional lines for data transfer to and from the memory. EX1005, 8:59-61, FIG. 1. Slemmer also teaches that multiple memories are connected via their terminals to a bus that connects them to a controller, such as a controller used in an end-user system for reads from and writes to the memories and for testing of the memories. EX1005, FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:4-5, 8:14-19, 8:59-67, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 36:55-68, 37:11-24, 37:27-29, 37:33-37; *see e.g.*, EX1011, 18:9-13, 18:51-54, 26:8-12, FIG. 24; EX1012, FIG. 1, 1:16-21, 1:49-52. ; EX1003, ¶164. Similarly, Gasbarro discloses that a conventional memory system includes a memory controller for writing data into and reading data from the memory devices via a bi-directional bus. EX1006, 1:15-19, 4:45-48. Slemmer teaches that his invention benefits many types of memories, including static random access memory (SRAM) and dynamic RAM (DRAM). EX1005, 6:54-66, 2:60-66, 5:50-55 (examples of SRAM), 2:9-21, 3:16-28 (examples of DRAM); EX1003, ¶165. Similarly, Gasbarro teaches that his invention benefits many configurations of memory systems, including those that include multiple memory devices, modules, or slots along a bus. EX1006, 3:39-42,

5:18-21; EX1003, ¶165. Further, Gasbarro teaches that his invention benefits “standard” memory devices that incorporate an active terminator. *See* EX1006, 5:1-8; EX1003, ¶165.

Although Slemmer teaches a controller to a POSITA and discloses multiple memories connected together, it does not expressly disclose certain details about a memory system that connects to the multiple memories. *See* EX1005, 8:14-19, 37:15-19; EX1003, ¶166. For example, Slemmer does not expressly illustrate the connection between multiple memories, a controller connected to communicate with the memories such as providing external inputs and receiving acknowledgements of testing, or discuss termination of the memory connections. EX1003, ¶166. However, Gasbarro does disclose these technical aspects. Gasbarro discloses an expandable memory system, such as one with customizable memory system capacity, that includes a memory controller connected to multiple memories via a bus, and that uses an active terminator for each of the memory devices, such that they balance the impedance on the bus. *See* EX1006, 3:28-45; EX1003, ¶166.

As shown in the figure below, Gasbarro discloses a memory system in which the memory controller 70, that is connected to the memory devices via a channel 71 that includes a bus, uses a serial initialization line (SIL) 71 or the channel 72 to communicate an active termination signal to any one of the devices.

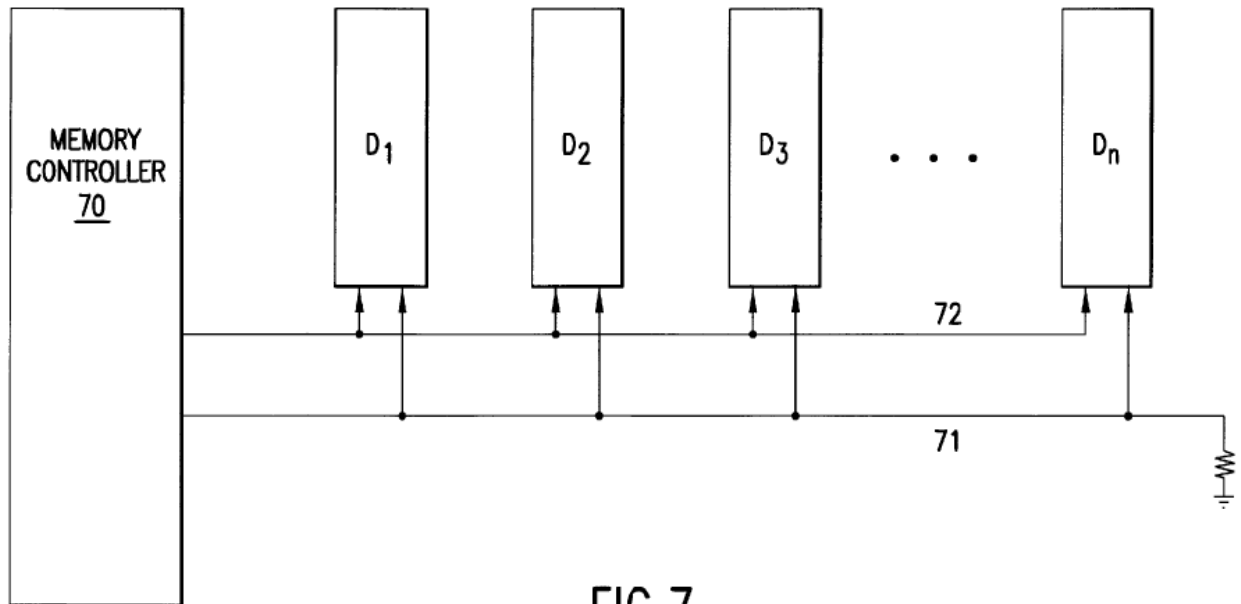


FIG.7

EX1006, FIG. 7, 6:49-54. Gasbarro explains that each of the memory devices is assigned and identified by a device identification (ID), such as via SIL 71, and that the memory controller recognizes the last device on the bus ( $D_n$  in the figure above) and turns on its corresponding active terminator. EX1006, 2:46-56, 5:63-66, 6:55-7:5. By switching on the active terminator in the last memory device, Gasbarro discloses that the memory devices on the bus benefit from balanced impedances to avoid undesired signal reflections and noise. EX1006, 7:6-14; EX1003, ¶167.

A POSITA looking to implement Slemmer's memory devices and testing architecture would have been motivated to look to a reference, like Gasbarro, which discloses a system with a memory controller for sending signals to and receiving signals from the memory devices and a termination architecture for

sending and receiving those signals. EX1003, ¶168. In the combination, Slemmer's memory devices and testing architecture would have been implemented using Gasbarro's teachings about a memory system, including Gasbarro's teachings that the memory devices are connected via a bus to a memory controller for read, write, and control operations and for active termination of the bus. EX1006, 1:16-19, 4:36-48, 6:8-12, FIG. 7; EX1003, ¶168. In the combination, the memory system would have been implemented with a memory controller to send and receive signals to Slemmer's multiple memories via a bus. *See id.* Further, the memories, such as memory 1, disclosed by Slemmer would have been implemented with active termination that is externally controlled, such as via SIL 71, and the controller would have been implemented to recognize the last memory device on the bus and turn on its corresponding active terminator, such as via SIL 71. *Id.*; *see also* EX1005, FIG. 1; EX1006, FIG. 7. This implementation of Slemmer in view of Gasbarro simply uses a known technique (e.g., active termination for expandable memory) to improve a similar device (e.g., Slemmer's memory devices with testing functionality) in the same way (e.g., by implementing a memory system with a bus connecting a controller to the memory devices, supporting active termination in the memory devices, supporting recognition of the last memory device in the controller, as well as the ability to turn on the corresponding active terminator for bus termination). EX1003, ¶168. Additionally, this implementation

of Slemmer in view of Gasbarro simply uses prior art elements (e.g., Slemmer's memory devices with testing functionality and Gasbarro's memory controller connected to those memory devices with active termination for the bus) according to known methods (e.g., using a conventional memory system controller and connection to the terminals of the memories and using active terminators for expandable memory support) to yield predictable results (e.g., a memory system with support for expandable memory that balances impedances to avoid signal reflections and noise). EX1003, ¶168.

Further, a POSITA would have been motivated to implement Slemmer in accordance with Gasbarro's teachings to ensure interoperability and proper operation with standard memory devices that already incorporate active termination, as taught by Gasbarro. EX1003, ¶169; *see* EX1006, 5:1-8.

Accordingly, a POSITA implementing Slemmer with such standard memory devices would have looked to Gasbarro's teachings of how to use the active terminator so that it supports an expandable memory system. EX1003, ¶169.

## **2. Claim limitations [1.P], [1.1], [1.2], and [1.3]**

As explained above for Ground 1, Slemmer teaches claim limitations [1.P], [1.1], [1.2], and [1.3]. *Supra* §X.A.1.a-X.A.1.d; EX1003, ¶¶78-97, 170; *see, e.g.*, EX1005, FIGS. 1, 9.

Further, in the combination, Slemmer and Gasbarro teach the limitations of claim 1. For example, Gasbarro discloses that between multiple memory devices and a memory controller is a channel (71) that includes a data bus, which is similar to Slemmer's disclosure of a memory with multiple terminals connected to signal lines (e.g., one or more of those signal lines are "a bus" of claim [1.1]) to send and/or receive data and Slemmer's teachings of multiple memories connected in parallel in a system. EX1006, FIG. 7, Abstract, 4:36-44, 6:65-7:1; EX1005, FIG. 1, 1:21-22, 1:33-38, 2:35-38, 3:1-16, 3:39-60, 6:9-11, 6:18-23, 7:26-30, 8:14-19, 32:64-33:2, 35:22-42, 35:47-51, 35:52-64, 37:11-24, 37:27-29, 37:33-37; EX1003, ¶171. A POSITA would have understood that in the combination, the multiple data terminals (e.g., DQ0 through DQ7) and multiple address terminals (e.g., A0 through A17) in Slemmer's memories would have been connected to signal lines (one of more of which is "*a bus*") that connect the memory devices to a memory controller. EX1003, ¶171; *supra* §X.A.1.b; EX1006, 1:16-19, 4:36-48, 6:8-12, FIG. 7. A POSITA would also have understood that the bus is part of a channel connecting the memory devices together, such as one disclosed by Gasbarro that includes signal lines for control information. *Id.* Further, a POSITA would have understood that the memory controller provides external inputs to the memory devices including control for active termination, such as via SIL 71 or channel 72

as disclosed by Gasbarro. EX1003, ¶171; EX1006, 2:46-56, 5:63-66, 6:55-7:5, FIG. 7.

### **3. Claim 2**

Claim 2 depends from claim 1, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claim 2. *Supra* §X.A.2; EX1003, ¶¶98-103, 172.

### **4. Claim 3**

As explained above for Ground 1, Slemmer teaches claim 3. *Supra* §X.A.3; EX1003, ¶173; *see, e.g.*, EX1005, FIGS. 1, 9.

Additionally, a POSITA would have understood that the memory controller in the combination of Slemmer and Gasbarro is the external controller that externally drives inputs to configure the memory for testing, which results in the deactivation of the output drivers. EX1003, ¶174; EX1005, 9:19-30, FIG. 1; *supra* §§X.A.4.b, X.B.1-X.B.2 (discussing memory controller in combination).

Accordingly, the output drivers are “*deactivated by*” any one or combination of the memory controller, TMEC 28, and/or PTC 29 (“*a test unit*”). EX1003, ¶175.

### **5. Claim 4**

As explained above for Ground 1, Slemmer teaches claim 4. *Supra* §X.A.4; EX1003, ¶176; *see, e.g.*, EX1005, FIGS. 1, 9.

Additionally, a POSITA would have understood that in the combination of Slemmer and Gasbarro, the memory controller is a “bus control device” (as recited in claim [4.2]) that provides control information, including the chip enable (E1/E2) signals, a write enable (W\_) signal, and an output enable (OE) signal to the memory (any one or combination of which is “*an enable signal*”), to control the output drivers Slemmer’s memory via AND-gate 26. EX1003, ¶177; EX1005, FIG. 1; *supra* §§X.A.4.b, X.B.1-X.B.2 (discussing combination’s memory controller). Further, as discussed above for Ground 2, the combination’s memory controller is the external controller discussed in Ground 1. *Supra* §X.B.4; EX1003, ¶177.

#### **6. Claim 5**

Claim 5 depends from claim 4, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claim 5. *Supra* §X.A.5; EX1003, ¶178.

#### **7. Claim 7**

Claim 7 depends from claim 1, whose limitations are above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claim 7. *Supra* §X.A.6; EX1003, ¶179.

Additionally, as discussed above, the memory controller in the combination is the “*bus control device*.” *Supra* §X.B.5; EX1003, ¶180. A POSITA would have

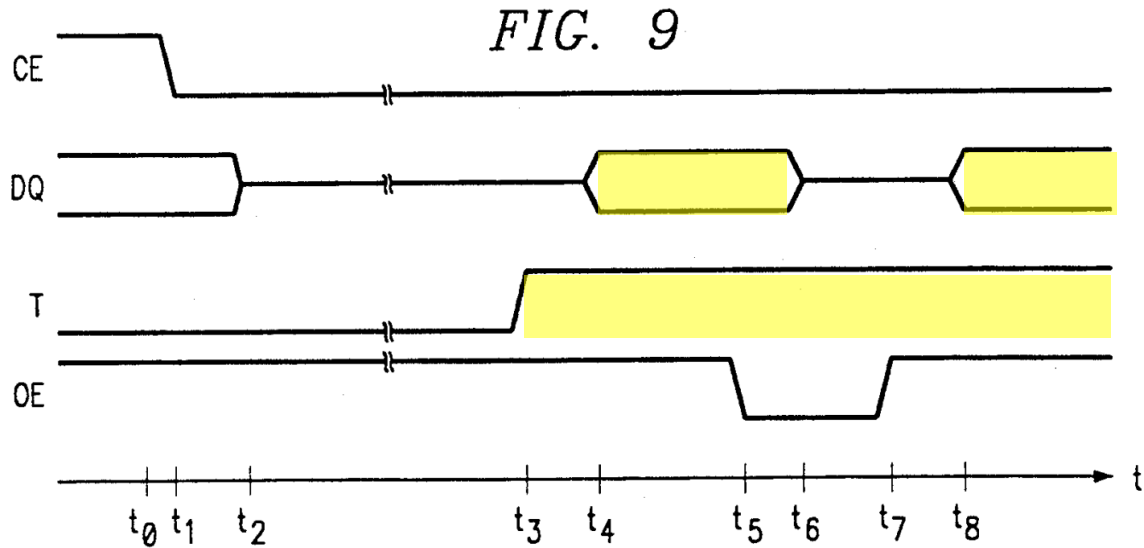
understood that the memory controller receives a signal indicating testing of the memory to be tested. *Supra* §§X.B.5, X.A.6; EX1003, ¶180.

**8. Claim 8: “The electrical circuit according to claim 7, wherein, during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by a device selected from the group consisting of said bus control device and one of said others of said plurality of circuit components.”**

As explained for Ground 1, Slemmer teaches claim 7, including a controller (“*bus control device*”) that receives test information on one or more DQ terminals/lines from the memory during testing. *Supra* §X.A.7; *see also supra* §X.A.4.b (discussing Slemmer’s “bus control device” for claim element [4.2]); EX1003, ¶181. Additionally, as explained for Ground 2, Slemmer and Gasbarro teaches claim 7, including teaching a memory controller (“*bus control device*”). *Supra* §X.B.7; EX1003, ¶181.

Further, Slemmer in view of Gasbarro also teaches that in order for the controller to receive the test information successfully from the memory 1 during testing, it must ensure that the DQ terminals/lines (“*bus*”) are terminated by the last memory device on the bus, as explained in more detail below. EX1003, ¶182.

As shown in the figure below, the memory 1 drives the DQ terminal during testing between times  $t_4$  and  $t_6$  and after time  $t_8$  (highlighted in yellow).



EX1005, FIG. 9. Slemmer explains that at time  $t_4$ , “[r]esponsive to line T at a high logic level, OR gate 33 will present a high logic level to AND gate 26.” *Id.*, 36:25-27. In addition, the “terminals OE and W\_ are at high logic levels” and “line 32 from parallel test circuitry 28 remains high.” *Id.*, 36:27-30. Accordingly, the terminal(s) DQ “go into an active state” (in a low-impedance) to communicate test information, such as whether a particular “test either passed, or has not taken place” during testing. *Id.*, 36:29-31, 36:32-40, 36:41-54; EX1003, ¶182. Similarly, at time  $t_8$ , responsive to “externally driving terminal OE to a high logic level,” the terminal(s) DQ again become active and present data. EX1005, 37:33-37; EX1003, ¶182.

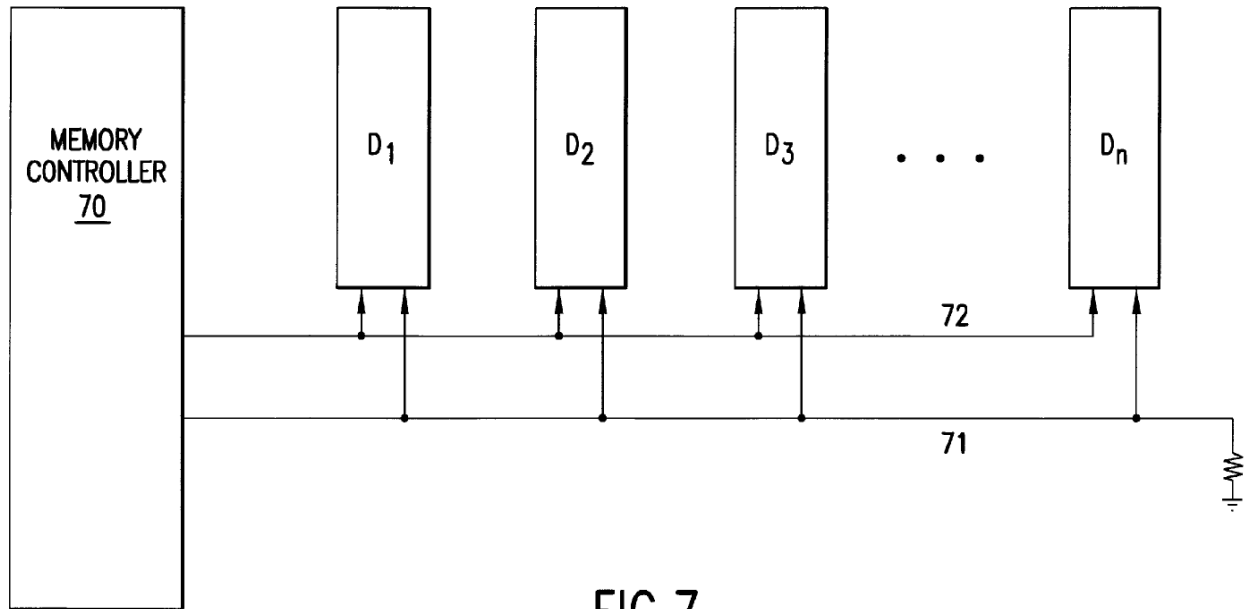
Further, Slemmer teaches that the controller, such as one in a system or test equipment, must receive the test information from the DQ terminal(s). EX1003, ¶183. For example, communication of the test information “allows detection of

[an] inadvertent entry into [a test] mode, so that the user may perform the necessary cycles to return to the normal operating mode of the device.” EX1005, 35:47-51. The information also allows “the test equipment and personnel” of a system to distinguish between “whether the memory actually failed the test or if it merely failed to enter the test mode.” *Id.*, 35:36-42; *see also id.*, 35:25-30.

Similarly, Gasbarro teaches a memory controller for receiving data from a memory device. EX1003, ¶183; EX1006, 1:16-19, 4:45-48, 6:8-12, FIG. 7.

A POSITA would have understood that for the controller to receive the test information from the DQ terminal(s), the controller must ensure that the bus is properly terminated. EX1003, ¶184. As explained above, in the combination, the memories disclosed by Slemmer would have been modified to be implemented with active termination that is externally controlled, and the controller, as taught by Slemmer and disclosed by Gasbarro, would have been modified to recognize the last memory device on the bus and turn on its corresponding active terminator. EX1003, ¶184; *supra* §X.B.1. Accordingly, a POSITA would have understood that when testing a memory that is not the last memory device on the bus, the memory controller (“*bus control device*”) would enable the active terminator of another memory device that is the last device on the bus (“*one of said others of said plurality of circuit components*”). EX1003, ¶184. Indeed, Gasbarro teaches that imbalance between memory components will result in unwanted signal reflections

and increased signal line noise. EX1006, 2:59-64. To enable balance of impedances in an expandable memory system, the controller in the combination (“*bus control device*”) controls active terminators in each of the memory devices, such as via serial initialization line (SIL) 72 or channel 71, as shown below:



EX1006, FIG. 7, 3:42-45, 6:49-54; EX1003, ¶184. Specifically, the controller determines which device is the last on the bus ( $D_n$  in the figure above) during initialization and then enables the active terminator on only that device to balance impedances. EX1006, 6:55-7:5; EX1003, ¶184; *see also* EX1006, 6:49-54, 7:6-14. Accordingly, Slemmer in view of Gasbarro teaches “*during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by . . . one of said others of said plurality of circuit components.*” EX1003, ¶¶181-84.

## **9. Claims 9-10 and 13-14**

Claims 9-10 and 13-14 depend from claim 1, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claims 9-10 and 13-14. *Supra* §§X.A.8-X.A.9, X.A.10-X.A.11; EX1003, ¶185. Moreover, as addressed in Ground 1, claim 10 contains limitations similar to limitations in claims 3, 4 and 7, and claims 13-14 contain limitations similar to limitations in claim 2 and 4. *Id.* The limitations of claims 2-4 and 7 are also discussed above in this ground. *Supra* §§X.B.3- X.B.5, X.B.7. For example, the memory controller provides control information, such as an enable signal to control the output drivers to output data during normal operation. *Supra* §X.B.5; EX1003, ¶185.

## **10. Claim limitations [20.P], [20.1], [20.2], and [20.3]**

As explained above for Ground 1, Slemmer teaches claim limitations [20.P], [20.1], [20.2], and [20.3]. *Supra* §§X.A.12.a-X.A.12.d; EX1003, ¶186; *see, e.g.*, EX1005, FIGS. 1, 9.

Further, in the combination, Slemmer as modified by Gasbarro's teachings of a memory controller and memory with support for expandable memory teach the limitations of claim 20. For the reasons explained above for claim 1, a POSITA would have understood that in the combination, a channel with a bus would have been implemented to connect a controller of the memory to multiple memory

devices to support expandable memory, such as by providing external inputs to the memory devices including control for active termination, such as via SIL 71 or channel 72 as disclosed by Gasbarro, as well as to support normal operation and test modes, as disclosed by Slemmer. *Supra* §X.B.2; EX1003, ¶187; EX1006, 2:46-56, 5:63-66, 6:55-7:5, FIG. 7; *see e.g.*, EX1005, FIGS. 1, 9.

#### **11. Claims 21-24 and 26**

Claims 21-24 and 26 depend from claim 20, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claims 21-24 and 26. *Supra* §§X.A.12-X.A.16; EX1003, ¶188. Further, the limitations of claims 21-24 and 26 are similar the limitations of claims 2-5 and 7, respectively. *Id.* Slemmer and Gasbarro teach claims 21-24 and 26 for the additional reasons provided above for this ground. *Supra* §§X.B.3-X.B.7; EX1003, ¶188.

**12. Claim 27: “The method according to claim 26, which comprises using the bus control device to ensure that, during testing of the circuit component to be tested, the bus is terminated by a device selected from the group consisting of the bus control device and one of the others of the plurality of circuit components.”**

As explained for claim 8 above, Slemmer and Gasbarro teach “*during testing of said circuit component to be tested, said bus control device ensures that said bus is terminated by . . . one of said others of said plurality of circuit*

*components,”* and thus also teach claim 27. *Supra* §X.B.2; EX1003, ¶189; EX1006, 6:49-7:14, FIG. 7.

### **13. Claims 28-29 and 32-33**

Claims 28-29 and 32-33 depend from claim 20, whose limitations are discussed above in this ground. Further, for the reasons explained above for Ground 1, Slemmer teaches the additional limitations of claims 28-29 and 32-33. *Supra* §§X.A.17-X.A.18, X.A.19-X.A.20; EX1003, ¶190. Moreover, as addressed in Ground 1, claim 29 contains limitations similar to limitations in claims 4 and 10, and claims 32 and 33 contain limitations similar to limitations in claims 2, 4, and 13-14. *Id.* The limitations of claims 2, 4, 10, and 13-14 are also discussed above in this ground. *Supra* §§X.B.3, X.B.5, X.B.9; EX1003, ¶190.

## **XI. CONCLUSION**

Accordingly, Petitioner requests *inter partes* review of claims 1-5, 7-10, 13-14, 20-24, 26-29, 32-33 pursuant to Grounds 1-2 set forth above.

Date: February 6, 2023

Respectfully submitted,

/Brian W. Oaks/

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Brian W. Oaks (Reg. No. 44,981)  
Aashish G. Kapadia (Reg. No. 78,844)  
McDERMOTT WILL & EMERY LLP  
303 Colorado Street, Suite 2200  
Austin, TX 78701  
TEL: 512-726-2600  
FAX: 512-532-0002  
boaks@mwe.com  
akapadia@mwe.com

*Attorneys for Petitioner,*  
Xilinx, Inc.

## **CERTIFICATE OF COMPLIANCE WITH WORD COUNT**

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,776 words which is less than the 14,000 allowed under 37 C.F.R. § 42.24(a)(1)(i).

/Brian W. Oaks/

Brian W. Oaks

Lead Counsel for Petitioner

## CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(a), the undersigned certifies that on February 6, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, cost prepaid, to the Patent Owner by serving the correspondence address of record and another address known to Petitioner as likely to effect service, as follows:

LERNER GREENBERG STEMER LLP  
P O BOX 2480  
HOLLYWOOD, FL 33022-2480  
*Patent Center Correspondence Address  
of Record for U.S. Patent No. 6,701,473*

Robert E. Freitas  
FREITAS & WEINBERG LLP  
303 TWIN DOLPHIN DRIVE, SUITE 600  
REDWOOD SHORES, CA 94065  
*Additional Address Known to Petitioner as  
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Additionally, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were served via e-mail on:

Robert E. Freitas  
FREITAS & WEINBERG LLP  
rfreitas@fawlaw.com

Petitioner knows this to be an additional address likely to effect service.

/Brian W. Oaks/  
Brian W. Oaks  
Lead Counsel for Petitioner