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UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner

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Case IPR2023-00517

Patent 6,701,473

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**PATENT OWNER'S PRELIMINARY RESPONSE**

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## I. INTRODUCTION

Pursuant to 35 U.S.C. § 313 and 37 C.F.R. § 42.107, Polaris Innovations Limited (“Polaris” or “Patent Owner”) submits this Preliminary Response to Xilinx, Inc.’s (“Xilinx” or “Petitioner”) Petition for *inter partes* review (“Petition”), challenging claims 1-5, 7-10, 13-14, 20-24, 26-29, and 32-33 of U.S. Patent No. 6,701,473 (the “’473 Patent”) (Ex. 1001).

Petitioner alleges that certain claims are invalid based on two different grounds. First, Petitioner argues that claims 1-5, 7, 9-10, 13-14, 20-24, 26, 28-29, and 32-33 are obvious over U.S. Patent No. 5,072,138 (Ex. 1005, “*Slemmer*”). Second, Petitioner argues that claims 1-5, 7-10, 13-14, 20-24, 26-29, and 32-33 are obvious over *Slemmer* in view of U.S. Patent No. 6,308,232 (Ex. 1006, “*Gasbarro*”).

The ’473 Patent and its challenged claims are directed to solutions that allow a circuit component to be tested reliably by minimizing the power, current, and heat generated by the circuit component and its electrical circuit by two different solutions: (i) outputting data to the bus that is other than data which would be output to the bus during normal operation; or (ii) outputting no data to the bus during testing.

Unlike the solutions disclosed in the challenged claims of the ’473 Patent, the Petition’s primary reference *Slemmer* is not concerned with minimizing the power, current, or heat generated by the circuit component and its electrical circuit. Indeed,

the solution disclosed by *Slemmer* for avoiding inadvertently entering into a testing mode of the component requires generating multiple overvoltage conditions of a component of the electrical circuit to enter into testing mode, which causes the electrical circuit and the component to be tested to generate high power, current, and heat. Thus, the solution provided by *Slemmer* of generating multiple overvoltage conditions is diametrically opposed to the claimed features of the '473 Patent directed to minimizing the power, current, and heat generated when a circuit component is tested.

Additionally, *Slemmer* does not disclose “*outputting data to the bus that is other than data which would be output to the bus during normal operation*” by a circuit component during/while testing the circuit component, as recited by independent claims 1 and 20. Furthermore, *Slemmer* does not disclose “*outputting no data to the bus*” by a circuit component during/while testing the circuit component, as recited by independent claims 1 and 20. Moreover, Petitioner wholly failed to meet its burden that *Slemmer* discloses or renders obvious the claim elements directed to an operation “*selected from the group,*” as recited by independent claims 1 and 20.

Because the Petition fails to show at least one element of each of the challenged independent claim in the asserted references or combinations, the

Petitioner cannot show that any of the challenged claims are reasonably likely to be found unpatentable. The Board should not institute *inter partes* review of the '473 Patent for at least this reason as described more fully herein.

In summary, each of Petitioner's grounds are deficient in that they fail to show that *Slemmer* or *Slemmer* in combination with *Gasbarro* teach or suggest every limitation of the Challenged Claims. Consequently, Petitioner cannot meet its burden for obviousness, and the Board should not institute IPR.

## **II. THE '473 PATENT AND THE CHALLENGED CLAIMS**

### **A. Overview of the '473 Patent**

The '473 Patent concerns testing at least one circuit component that is connected to other circuit components through a bus of an electrical circuit, where the circuit component(s) to be tested are tested independently of the other circuit components connected through the bus. Ex. 1001, 1:7-16. More particularly, the '473 Patent is directed to inventions that prevent unreliable test results of a circuit component due to very high currents and extreme heat that occurs during conventional testing taught by the prior art. *Id.*, 1:22-39

As the '473 Patent explains, a first solution to prevent unreliable test results is for the circuit component being tested to, “instead of the data which would need to be output to the bus during normal operation, output[] other data to the bus.” *Id.*, 2:6-9; 2:12-15. This first solution is recited in independent claim 1 as “said circuit

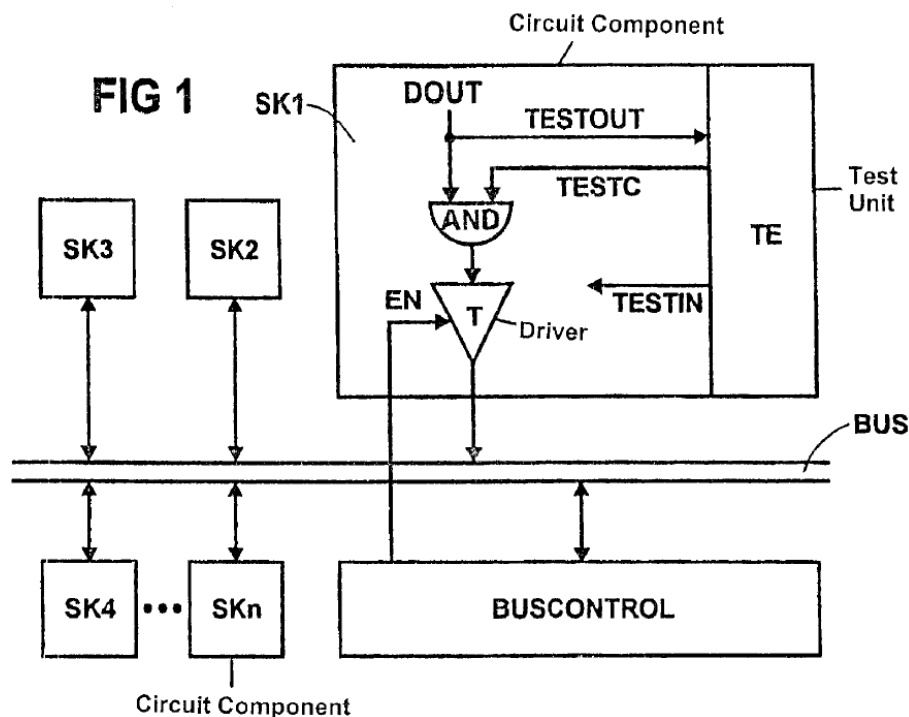
component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of ... outputting data to said bus that is other than data which would be output to said bus during normal operation,” and in claim 20 as “while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of ... outputting data to the bus that is other than data which would be output to the bus during normal operation.” *Id.*, 11:9-14, 12:62-67.

As the '473 Patent also explains, a second solution to prevent unreliable test results is for the circuit component being tested to “output[] no data to the bus.” *Id.*, 2:5-6; 11-12. This second solution is recited in independent claim 1 as “said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus,” and in claim 20 as “while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus.” *Id.*, 11:9-12, 12:62-65.

Each of these solutions “ensure that the output drivers of the circuit component which is to be tested do not consume any power at all or only very little power.” *Id.*, 2:16-18. The data “output to the bus by the circuit component which is tested, while it is being tested, are not the data which would be output to the bus by

the tested circuit component during normal operation.” *Id.*, 2:21-25. “The data can therefore be selected and output such that the power consumption of the output drivers is minimal.” *Id.*, 2:25-27. Each of the solutions described above provide reliable test results of the circuit component being tested by minimizing the power, current, and heat generated by the circuit component during testing, which eliminates the risk of obtaining unreliable test results due to high current or extreme heat. *See, e.g., Id.* 1:22-392, 2:1-27.

As to the first claimed solution concerning reliable testing of a circuit component by outputting data to the bus that is other than data which would be output to the bus during normal operation, the ’473 Patent describes an embodiment of such a solution with reference to Figure 1, which is illustrated below:



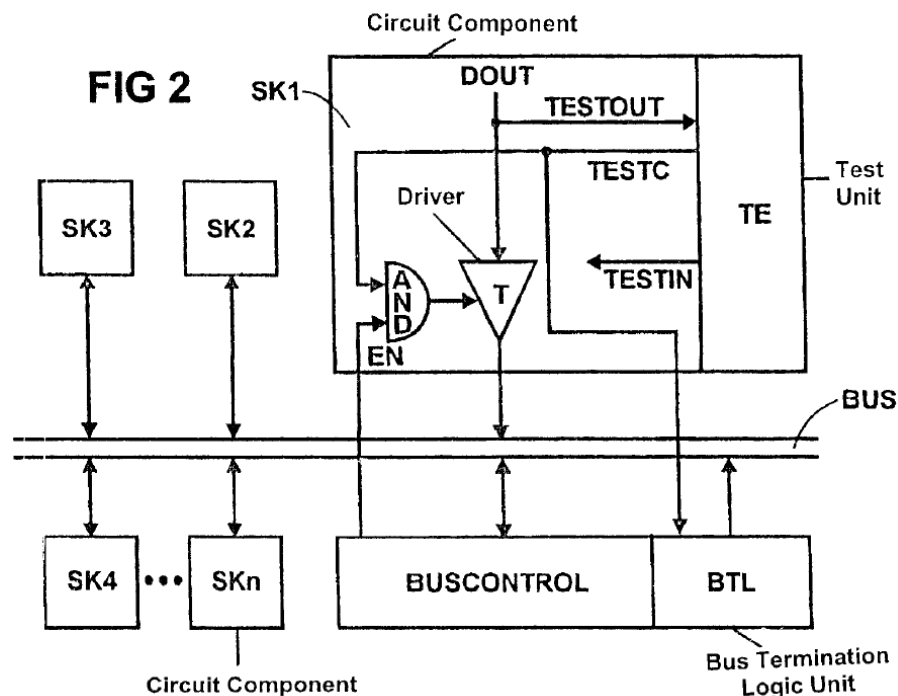
*Id.*, Fig. 1.

“During testing of the circuit component SK1, ... instead of the data normally output to the bus ‘BUS’, other data are output to the bus.” *Id.*, 5:50-57. “In the example under consideration, the data which are output to the bus ‘BUS’ while the circuit component SK1 is being tested are generated independently of the data which actually need to be output to the bus; they have the special feature that they do not change or change only very infrequently.” *Id.*, 5:59-64. “In the example under consideration, data which represent the level ‘0’ are continuously output to the bus ‘BUS’ while the circuit component SK1 is being tested.” *Id.*, 5:65-67. “Data continuously representing the level ‘1’ can also be output to the bus ‘BUS’.” *Id.*, 7:4-5. “The fact that, while it is being tested, the circuit component SK1 outputs data which never change or change only infrequently to the bus ‘BUS’ has the positive effect that the bus lines need never be reloaded or need be reloaded only infrequently.” *Id.*, 6:22-26. “This is advantageous because the output drivers T consequently consume only relatively little power, and the output drivers T and hence also the circuit component SK1 do not heat up excessively.” *Id.*, 6: 26-30.

“The low power consumption of the electrical circuit during testing and relatively low temperature of the electrical circuit during testing mean that the circuit component SK1 which is to be tested can be reliably tested with a minimum effort.”

*Id.*, 6:31-35. “In particular, it means that the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept small, and it is a comparatively simple matter to carry out low-temperature tests.” *Id.*, 6:35-40. “The fact that the data DOUT which actually need to be output to the bus ‘BUS’ are not output to the bus while circuit component SK1 is being tested, but instead other data are output to the bus, has no negative effect on the test result.” *Id.*, 6:41-44. Other details as to the functionality of the embodiment of Figure 1 are disclosed in the ’473 Patent at column 4, line 54 to column 7, line 23.

As to the second claimed solution concerning reliable testing of a circuit component by outputting no data to the bus, the ’473 Patent describes an embodiment of such a solution with reference to Figure 2, which is illustrated below:



*Id.*, Fig. 2.

“The electrical circuit can alternatively be designed such that, while it is being tested, the circuit component which is to be tested outputs no data the bus.” *Id.*, 7:24-26. “The electrical circuit show in FIG. 2 is largely consistent with the electrical circuit shown in FIG. 1.” *Id.*, 7:30-31. “Unlike the circuit component SK1 shown in FIG. 1, however, the circuit component SK2 shown in FIG. 2 outputs no data to the bus ‘BUS’ while it is being tested.” *Id.*, 7:48-50. “In the example under consideration, this is achieved in that the (control) connections of the output drivers T ..., which connections can be used to activate and deactivate the output drivers, no longer have the enable signal EN which is output by the bus control device BUSCONTROL applied to them, but instead have the output signal from a logic unit connected upstream of the control connection applied to them.” *Id.*, 7:51-59.

“The fact that no data are output to the bus ‘BUS’ while the circuit component SK1 is being tested has the positive effect that the output drivers T have no or only a negligibly low power consumption and consequently do not heat up at all, or heat up only to a very small extent.” *Id.*, 8:38-42. “The low power consumption of the electrical circuit during testing and the relatively low temperature of the electrical circuit during testing mean that the circuit component SK1 which is to be tested can be reliably tested with a minimum of effort.” *Id.*, 8:43-47. “In particular, this means

that the number and size of the elements (needles) used to supply the electrical circuit with power during testing can be kept small, and it is a comparatively simple matter to carry out low-temperature tests.” *Id.*, 8:47-52. Other details as to the operation of the embodiment of Figure 2 are disclosed in the ’473 Patent at column 7, line 24 to column 8, line 52.

The claimed inventions of the independent claims of the ’473 Patent thus allows a circuit component to be tested reliably by minimizing the power, current, and heat generated by the circuit component during testing by: (i) outputting data to the bus that is other than data which would be output to the bus during normal operation; or (ii) outputting no data to the bus during testing.

## **B. Claim Overview**

Independent claims 1 and 20 are reproduced below with emphasis on the particular limitations that are at issue in this Preliminary Response:

1. An electrical circuit comprising:

a bus; and

a plurality of circuit components which are connected via said bus, at least one of said plurality of circuit components defining a circuit component to be tested and configured to be tested independently from all others of said plurality of circuit components;

said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.

...

20. A method for testing a circuit component which is connected to other circuit components via a bus, the method which comprises:

providing a plurality of circuit components that are connected to a bus;

configuring at least one of the plurality of circuit components such that it can be tested independently from all others of said plurality of circuit components, the at least one of the plurality of circuit components defining a circuit component to be tested; and

while testing the circuit component to be tested, performing an operation with the circuit component to be tested, the operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.

The arguments in this Preliminary Response pertain to independent claims 1 and 20, but are equally applicable to claims 2-5, 7-10, 13-14 and claims 21-24, 26-29, and 32-33 because each of these claim sets depend from independent claim 1 or

20, respectively. As such, should the Board accept Patent Owner's arguments that trial should not be instituted on claims 1 and 20, it necessarily follows that trial should not be instituted on the dependent claims.

### **III. LEVEL OF ORDINARY SKILL**

For the limited purpose of this Preliminary Response, Patent Owner does not contest Petitioner's definition of a person of ordinary skill in the art, but it reserves the right to do so if trial is instituted.

### **IV. CLAIM CONSTRUCTION**

Patent Owner submits that the Board need not construe any claim terms in a particular manner to arrive at the conclusion that the Petition is substantively deficient. *See Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) ("need only be construed 'to the extent necessary to resolve the controversy'").

As to Petitioner's allegations that the claimed phrase of independent claims 1 and 20 of "outputting data to said bus that is other than data which would be output to said bus during normal operation" has no objective boundaries and that no explanation is provided by the '473 Patent as to how to distinguish between data output to the bus "during normal operation" from "other" data output to the bus during testing, Petitioner is wrong. *See* Petition, pp. 26-27; 65. In light of the repeated and consistent statements in the '473 Patent, a POSITA would understand

this claim phrase to mean “instead of the data which would be output to the bus by the circuit component during normal operation, outputting data to the bus that is other than the data which would be output to the bus during normal operation.” *See, e.g.,* Ex. 1001, 2:6-8 (“instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus (characterizing part of patent claim 1)”; 2:12-15 (“instead of the data which would need to be output to the bus during normal operation, outputs other data to the bus (characterizing part of patent claim 2)<sup>1</sup>”; 2:21-27 (“This is because the data which ... are output to the bus by the circuit component which is tested, while it is being tested, are not the data which would be output to the bus by the tested circuit component during normal operation. The data can therefore be selected and output such that the power consumption of the output drivers is minimal.”); 5:56-57 (“instead of the data normally output to the bus ‘BUS’, other data are output to the bus”); 6:41-44 (“The fact that the data DOUT which actually need to be output to the bus ‘BUS’ are not output to the bus while the circuit component SK1 is being tested, but instead other data are output to the bus”).

Furthermore, Petitioner has taken an unreasonably broad claim construction position that the claimed phrase of independent claims 1 and 20 of “outputting no data to the bus” means any fraction of time (nanoseconds, milliseconds, etc.) that no

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<sup>1</sup> Patent Owner believes this reference is directed to claim 20, not claim 2.

data is being transmitted between the time periods when data is being transmitted while the circuit component is being tested. *See* Petition, pp. 25-26; 65. Petitioner's construction is wholly divorced from the claim language when read in light of the specification.

The greater limitation of Claim 1 recites “said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.” Ex. 1001, 11:9-14 (emphasis added). The greater limitation of Claim 20 recites “while testing the circuit component to be tested, performing an operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.” *Id.*, 12:62-67 (emphasis added). The specification of the '473 Patent makes clear that “an operation” selected of either “outputting no data to said bus” or “outputting data to the data bus that is other than data which would be output to the bus during normal operations” are alternative solutions wholly separate from one another, such that “during the testing thereof” of the circuit component or “while testing the circuit component” the circuit component either selects the operation of “outputting no data to said bus” or “outputting data to the bus that is other than data

which would be output to the bus during normal operation” when and so long as the circuit component is being tested. *See supra*, Section II.A.

The specification makes clear that “during” or “while” refers to the entire period of: (i) testing by the first solution; (ii) testing by the second solution; or (iii) the normal operation. *See, e.g., id.*, 5:29-31 (“*During normal operation of the circuit component SK1, that is to say when and so long as the circuit component SK1 is not being tested.*”) (emphasis added); 5:50-57 (“During testing of the circuit component SK1, ... “instead of data normally output to the bus ‘BUS’, other data are output to the bus.”); 5:59-64 (“In the example under consideration, the data which are output to the bus “BUS” while the circuit component SK1 is being tested are generated independently of the data which actually need to be output to the bus”); 5:65-67 (“In the example under consideration, data which represent the level ‘0’ are continuously output to the bus ‘BUS’ while the circuit component SK1 is being tested.”); 6:16-21 (“During testing of the circuit component SK1, the test control signal has the value ‘0’ ... This means that the value ‘0’ is continuously output to the bus while the circuit component SK1 is being tested”); 6:22 26 (“The fact that, while it is being tested the circuit component SK1 outputs data which never change or change only infrequently to the bus ‘BUS’ has the positive effect that the bus lines need never be reloaded or need to be reloaded only infrequently.”); 6:41-44 (“The fact that the data DOUT

which actually need to be output to the bus 'BUS' are not output to the bus while the circuit component SK1 is being tested, but instead other data are output to the bus"); 7:1-3 ("It ought to be clear that it is not imperative for data continuously representing the level '0' to be output to the bus 'BUS' while the circuit component SK1 is being tested."); 7:5-8 ("Furthermore, provision may be made for data which do not continuously have one predetermined level, but instead change, to be output to the bus 'BUS' while the circuit component SK1 is being tested."); 7:48-50 ("Unlike the circuit component SK1 shown in FIG. 1, however, the circuit component SK2 shown in FIG. 2 outputs no data to the bus 'BUS' while it is being tested."); 8:10-16 ("The bus termination logic unit BTL ensures that, *during testing of the circuit component SK1 (when and so long as the test control signal TESTC is signaling that the circuit component SK1 is currently being tested)*, the bus 'BUS' is terminated by one of the other components connected to the bus 'BUS'") (emphasis added); 8:38-42 ("*The fact that no data are output to the bus 'BUS' while the circuit component SK1 is being tested* has the positive effect that the output drivers T have no or only a negligibly low power consumption and consequently do not heat up at all, or heat up only to a very small extent.") (emphasis added).

Furthermore, the specification discloses that in contrast to the first embodiment of an electrical circuit designed for the first testing solution of

“outputting data to the bus that is other data which would be output to the bus during normal operation,” “[t]he electrical circuit can *alternatively be designed* such that, *while it is being tested*, the circuit component which is to be tested *outputs no data to the bus*. An illustrative embodiment such an electric circuit is shown in FIG. 2 and is described below with reference thereto.” *Id.*, 7:24-29 (emphasis added). To reinforce this concept, the ’473 Patent further discloses that “[u]nlike the circuit component SK1 shown in FIG. 1, however, the circuit component SK2 shown in FIG. 2 *outputs no data to the bus ‘BUS’ while it is being tested.*” *Id.*, 7:48-50 (emphasis added).

Thus, the claims and the specification of the ’473 Patent makes clear that the claim limitations of claims 1 and 20 directed to the second, alternative testing solution of “outputting no data to the bus” means “outputting no data to the bus when and so long as the circuit component is being tested.”

## **V. APPLICABLE LEGAL STANDARDS**

The Board may only grant a petition for inter partes review where “the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a); 37 C.F.R. § 42.108(c). Petitioner bears the burden of showing that this statutory threshold has been met. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,756 (Aug. 14, 2012) (“The Board . . . may

institute a trial where the petitioner establishes that the standards for instituting the requested trial are met . . .”).

Each of Petitioner’s Grounds relies on obviousness. Section 103 of the Patent Act provides that “[a] patent may not be obtained . . . if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103(a). The obviousness analysis requires several threshold inquiries identified below.

**A. Claims cannot be found obvious if an element is missing.**

If a single element of the claim is absent from the prior art, the claim cannot be considered obvious. *See CFMT, Inc. v. YieldUp Int’l Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (“Obviousness requires a suggestion of all limitations in a claim.”) (citing *In re Royka*, 490 F.2d 981, 985 (C.C.P.A. 1974)); *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (reversing obviousness rejection where prior art did not teach or suggest all claim limitations); *Garmin Int’l, Inc. v. Patent of Cuozzo Speed Techs. LLC*, Case No. IPR2012-00001, Paper 15 at 15 (P.T.A.B. Jan. 9, 2013) (refusing to institute an IPR under 35 U.S.C. § 103 where prior art did not disclose all claim limitations).

**B. A petition must address the *Graham* factors.**

Obviousness is resolved on a number of factual determinations including: (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of ordinary skill in the art. *See Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). Petitions for IPR “must address the Graham factors.” *Eizo Corp. v. Barco N.V.*, No. IPR2014-00358, Paper 11 at 29-30 (P.T.A.B. July 23, 2014) (citing *Graham*, 383 U.S. at 17-18). For example, the Board faulted the petitioner in *Eizo Corporation* for failing to identify the differences between the claimed subject matter and the prior art. *Id.* at 29-30. In particular, the Board found insufficient the petitioner’s “conclusory assertion” that “[t]o the extent [the first reference] may not explicitly teach” the limitation, the second reference “explicitly teaches this limitation.” *Id.* at 30. The Board explained that “such an assertion *fails* to resolve the exact differences sought to be derived from” the second reference. *Id.* (finding that petitioner had not shown a reasonable likelihood of prevailing on that ground). Other Board decisions have reached the same result. *See, e.g., Moses Lake Indus., Inc. v. Enthone, Inc.*, Case No. IPR2014-00243, Paper 6 at 18 (P.T.A.B. June 18, 2014); *Moses Lake Indus., Inc. v. Enthone, Inc.*, No. IPR2014-00246, Paper 6 at 17 (P.T.A.B. June 18, 2014); *eBay, Inc. v. Paid, Inc.*, No. CBM2014-00125, Paper 15 at 21 (P.T.A.B. Sept. 30, 2014).

**C. A petition must provide articulated reasoning with rational underpinning to combine references.**

The conclusion of obviousness based on a combination of references must also be supported with explicit analysis of a reason to combine those references. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). The Federal Circuit has stated that such reasons must be more than “mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.” *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006); *accord Innogenetics, N.V. v. Abbott Labs.*, 512 F.3d 1363, 1374 (Fed. Cir. 2008) (agreeing with the district court’s reasoning that “some kind of motivation must be shown from some source, so that the jury can understand why a person of ordinary skill would have thought of either combining two or more references or modifying one to achieve the patented method”); *see also LG Elecs., Inc. v. Cellular Commc’ns Equip. LLC*, Case No. IPR2016-00197, Paper 7 at 7-11 (P.T.A.B. April 29, 2016) (faulting a petition’s obviousness analysis for lack of sufficient articulated reasons with rational underpinnings for modifying references to achieve particular elements required in the claims).

## VI. SUMMARY OF THE REFERENCES

### A. Summary of *Slemmer*

*Slemmer* is directed to a solution that prevents entering a test mode inadvertently. Ex. 1005, 4:39-61; 5:1-14. *Slemmer* achieves this solution by requiring multiple overvoltage conditions of a component of the electrical circuit to enter into testing mode, such that the usage of multiple overvoltage conditions helps to avoid inadvertently entering into a testing mode of the component. *Id.* “The invention may be incorporated into a memory device having circuitry which requires multiple overvoltage excursions of a particular terminal together with a sequence of selection codes, in order for a special operating mode, for example a test mode, to be enabled.” *Id.*, 5:1-7. “The circuitry includes multiple flip-flops, each of which are clocked with each overvoltage excursion together with a valid test selection code, with the last one in the series generating an internal test enable signal.” *Id.*, 5:8-11. “The valid codes differ for each of the overvoltage excursions in the sequence, so that the possibility of inadvertent entry into the special mode is significantly reduced.” *Id.*, 5:11-14.

When a memory component operates in normal operation, *Slemmer* explains that the output terminals DQ are presented with data states. *Id.*, 7:15-34. When a memory component operates in testing mode, *Slemmer* explains that the output terminals DQ are presented with the same data states as in normal operation, even

though the data states presented at terminals DQ are unimportant for purposes of communicating the fact that the memory component has entered into test mode. *Id.*, 36:41-45.

**B. Summary of *Gasbarro***

*Gasbarro* is directed to a solution for avoiding problems when installing additional memory components to a memory system. Ex. 1006, 3:27-45. *Gasbarro* achieves this solution by use of an active terminator. *Id.*, 3:42-45.

**VII. THE PETITION DOES NOT DEMONSTRATE THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE UNDER GROUND 1.**

Petitioner relies on *Slemmer* to advance single-reference obviousness arguments against every claim element of independent claims 1 and 20. Petitioner's arguments with respect to Ground 1 fail for several reasons.

The '473 Patent and its challenged claims are directed to solutions that allow a circuit component to be tested reliably by minimizing the power, current, and heat generated by the circuit component and its electrical circuit by two different solutions: (i) outputting data to the bus that is other than data which would be output to the bus during normal operation; or (ii) outputting no data to the bus during testing. *Supra* § II.A. Unlike the '473 Patent, *Slemmer* is not concerned with minimizing the power, current, or heat generated by the circuit component and its electrical circuit. Indeed, the solution disclosed by *Slemmer* for avoiding

inadvertently entering into a testing mode of the component requires generating multiple overvoltage conditions of a component of the electrical circuit to enter into testing mode, which causes the component to be tested to generate high power, current, and heat. *Supra* § VI.A. Thus, the solution provided by *Slemmer* of generating multiple overvoltage conditions is diametrically opposed to the claimed features of the '473 Patent directed to minimizing the power, current, and heat generated when a circuit component is tested.

Additionally, *Slemmer* does not disclose “*outputting data to the bus that is other than data which would be output to the bus during normal operation*” by a circuit component during/while testing the circuit component, as recited by independent claims 1 and 20. Furthermore, *Slemmer* does not disclose “*outputting no data to the bus*” by a circuit component during/while testing the circuit component, as recited by independent claims 1 and 20. Moreover, Petitioner wholly failed to meet its burden that *Slemmer* discloses or renders obvious the claim elements directed to an operation “*selected from the group,*” as recited by independent claims 1 and 20.

**A. *Slemmer* does not disclose “outputting data to said/the bus that is other than data which would be output to said/the bus during normal operation.”**

Independent claims 1 and 20 of the '473 Patent require “outputting data to said/the bus that is other than data which would be output to said/the bus during

normal operation.” Ex. 1001, 11:9-14; 12:62-67. *Slemmer* fails to disclose this claim limitation.

As to Petitioner’s allegations that the claimed phrase of independent claims 1 and 20 of “outputting data to said/the bus that is other than data which would be output to said/the bus during normal operation” has no objective boundaries, and that no explanation is provided by the ’473 Patent as to how to distinguish between data output to the bus “during normal operation” from “other” data output to the bus during testing, Petitioner is wrong. *See* Petition, pp. 26-27; 65. As explained in Section IV, this claimed phrase means “instead of the data which would be output to the bus by the circuit component during normal operation, outputting data to the bus that is other than the data which would be output to the bus during normal operation.” *See Supra* § IV. Indeed, the ’473 Patent makes repeated and consistent statements that this is the proper meaning of this claim phrase. Ex. 1001, 2:6-8; 2:12-15; 2:21-27; 5:56-57; 6:41-44. Thus, Petitioner’s allegations that the ’473 Patent provides no explanation as to how to distinguish between data output to the bus during normal operation from other data output to the bus during testing is meritless.

Petitioner correctly states that *Slemmer* discloses presenting data to DQ terminals at times  $t_4$  to  $t_6$  and at time  $t_8$ . Petition, 27-28; 65. However, Petitioner fails to acknowledge that *Slemmer* never discloses that this data is not the data which

would be output during normal operation. *Id.* Indeed, the disclosure of *Slemmer* shows that this data is the same data which would be output during normal operation. When a memory component operates in normal operation, *Slemmer* explains that the output terminals DQ are presented with data states. Ex. 1005, 7:15-34. When a memory component operates in testing mode, *Slemmer* explains that the output terminals DQ are presented with the same data states as in normal operation, even though the data states presented at terminals DQ are unimportant for purposes of communicating the fact that the memory component has entered into test mode. *Id.*, 36:41-45.

In an attempt to explain away this issue, Petitioner makes three allegations that fail to overcome the actual teaching of *Slemmer* that the data outputted at times  $t_4$  to  $t_6$  and at time  $t_8$  is the same data that would be output during normal operation. First, Petitioner alleges that this data is different than the data which would be output during normal operation, “because normal operation is a different mode of operation of the memory (*see, e.g.*, EX1005, 1:60-67).” Petition, pp. 28; 65. Petitioner fails to disclose that this passage of *Slemmer* is directed to one of a myriad of prior art techniques that *Slemmer* is disparaging and improving upon. For example, this passage characterizes this as a “solution which has been used in the past,” not a solution which is used by *Slemmer*. EX1005, 1:60-67. Furthermore, this passage

does not state that the data output to a bus by a circuit component in testing mode is different than the data output to a bus by a circuit component in normal operation. As previously discussed, *Slemmer* only discloses that the data output at those times is the same data output during a normal operation.

Second, Petitioner alleges that this data is different than the data which would be output during normal operation, “because Slemmer discloses that the terminals DQ have a different function in normal operation than during testing (*see, e.g.*, EX1005, 37:40-51, 5:58-61, 8:59-61).” Petition, pp. 28; 65. None of these passages of *Slemmer* even stand for the proposition made by Petitioner. *See* EX1005, 37:40-51, 5:58-61, 8:59-61. Furthermore, *Slemmer* explains that the output terminals DQ are presented with the same data states as in normal operation, even though the data states presented at terminals DQ are unimportant for purposes of communicating the fact that the memory component has entered into test mode because. *Id.*, 36:41-45. Even if the terminals DQ are performing a different role during testing mode than in normal operation, it does not change the fact that the terminals DQ output the same data in testing mode as in normal operation.

Third, Petitioner alleges that this data is different than the data which would be output during normal operation, “because Slemmer’s disclosure is similar to Patent Owner’s allegations.” Petition, pp. 28; 65. Unlike *Slemmer*’s disclosure that

teaches outputting the same data during testing at times  $t_4$  to  $t_6$  and at time  $t_8$  as the data that would be output during normal operation, Patent Owner's infringement allegations are directed to accused devices that require "outputting data said/the bus that is other than data which would be output to said/the bus during normal operation."

Petitioner next alleges that "Slemmer explains that the data output [during testing at times  $t_4$  to  $t_6$  and at time  $t_8$ ] is for acknowledging test information, such as an acknowledgement of test mode entry (*id.* at 36:41-45)." Petition, pp. 28; 65. Petitioner mischaracterizes this passage of *Slemmer* reproduced below:

It should be noted that, for purposes of communicating test mode entry, the data state presented at terminals DQ is unimportant; the entry into test mode is communicated, in this embodiment of the invention, by a low impedance condition at terminals DQ.

EX1005, 36:41-45. First, this passage explains that "for purposes of communicating test mode entry, the data state presented at terminals DQ is unimportant." *Id.* As previously discussed, the data state presented at terminals DQ during testing is no different than the data state presented at terminals DQ during normal operation as taught by *Slemmer*. Ex. 1005, 7:15-34. Second, this passage makes clear that "entry into test mode is communicated, in this embodiment of the invention, *by a low impedance condition* at terminals DQ," and not by the data state presented at

terminals DQ, which is the same data state presented at terminals DQ during normal operation. *Id.* (emphasis added).

Petitioner further alleges that “Slemmer explains that the data output [during testing at times  $t_4$  to  $t_6$  and at time  $t_8$ ] is for acknowledging test information, such as ... an ‘identification of which test mode as has been enabled.’ (*id.* at 36:45-49).”

Petition, pp. 28, 65. This passage of *Slemmer* reproduced below:

However, if desired, additional information could be presented at this time at terminals DQ, such additional information including, for example, identification of which test mode has been enabled.

EX1005, 36:45-49. Notably, this passage of *Slemmer* makes clear that information, such as identification of which test mode has been enabled, that could be presented at terminals DQ is “additional information” to the data states presented at terminals DQ, which are the same data states presented at terminals DQ during normal operation as previously discussed. *Id.*

As previously discussed, the claim phrase of “outputting data to said/the bus that is other than data which would be output to said/the bus during normal operation” means “instead of the data which would be output to the bus by the circuit component during normal operation, outputting data to the bus that is other than the data which would be output to the bus during normal operation.” *See Supra* § IV; Ex. 1001, 2:6-8; 2:12-15; 2:21-27; 5:56-57; 6:41-44. The disclosure of *Slemmer*

communicating “a low impedance condition” or “additional information, including, for example, identification of which test mode has been enabled” is data output *in addition* to the data that would be output during normal operation (i.e., the data states), not *instead of* the data that would be output during the normal operation. Indeed, communicating such information in addition to the data that is output during normal operation would generate even more power, current, and heat during testing above and beyond the extreme power, current, and heat generated by *Slemmer’s* multiple overvoltage excursions. As taught by the ’473 Patent, the fundamental purpose of this claim limitation is to minimize power, current, and heat during testing by not outputting the data to the bus that would be output to the bus during normal operation. *See, e.g.,* Ex. 1001, 2:21-27 (data “output to the bus by the circuit component which is tested, while it is being tested, are not the data which would be output to the bus by the tested circuit component during normal operation. The data can therefore be selected and output such that the power consumption of the output drivers is minimal.”).

For at least these reasons, *Slemmer* does not teach, suggest, or disclose “outputting data to said/the bus that is other than data which would be output to said/the bus during normal operation” as recited by independent claims 1 and 20 of

the '473 Patent. Accordingly, Petitioner cannot show a likelihood that the challenged claims are unpatentable over *Slemmer*, and Ground 1 should be denied.

**B. *Slemmer* does not disclose “said circuit component to be tested configured to perform an operation, during testing thereof, ... of outputting no data to said bus” of claim 1 or “while testing the circuit component to be tested, performing an operation with the circuit component to be tested ... of outputting no data to the bus” of claim 20.**

Independent claim 1 requires “said circuit component to be tested configured to perform an operation, during testing thereof, ... of outputting no data to said bus” and independent claim 20 requires “while testing the circuit component to be tested, performing an operation with the circuit component to be tested ... of outputting no data to the bus.” '473 Patent, 11:8-13; 12:62-65. *Slemmer* fails to disclose these claim limitations.

As previously discussed in Section IV, Petitioner has taken an unreasonably broad claim construction position that the claimed phrase of independent claims 1 and 20 of “outputting no data to the bus” to mean any fraction of time (nanoseconds, milliseconds, etc.) that no data is being transmitted between the time periods when data is being transmitted while the circuit component is being tested. *See* Petition, pp. 25-26; 65. Petitioner’s construction is wholly divorced from the claim language when read in light of the specification.

The greater limitation of Claim 1 recites “said circuit component to be tested configured to perform an operation, during testing thereof, that is selected from the

group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation.” Ex. 1001, 11:9-14 (emphasis added). The greater limitation of Claim 20 recites “while testing the circuit component to be tested, performing an operation selected from the group consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.” *Id.*, 12:62-67 (emphasis added). The specification of the ’473 Patent makes clear that “an operation” selected of either “outputting no data to said bus” or “outputting data to the data bus that is other than data which would be output to the bus during normal operations” are alternative solutions wholly separate from one another, such that “during the testing thereof” of the circuit component or “while testing the circuit component” the circuit component either selects the operation of “outputting no data to said bus” or “outputting data to the bus that is other than data which would be output to the bus during normal operation” when and so long as the circuit component is being tested. *See Supra* § II.A.

The specification of the ’473 Patent makes clear that “during” or “while” refers to the entire period of: (i) testing by the first solution; (ii) testing by the second solution; or (iii) the normal operation. *See, e.g., id.*, 5:29-31 (“*During normal operation of the circuit component SK1, that is to say when and so long as the circuit*

*component SK1 is not being tested.*”) (emphasis added); 5:50-57 (“During testing of the circuit component SK1, ... “instead of data normally output to the bus ‘BUS’, other data are output to the bus.”); 5:59-64 (“In the example under consideration, the data which are output to the bus “BUS” while the circuit component SK1 is being tested are generated independently of the data which actually need to be output to the bus”); 5:65-67 (“In the example under consideration, data which represent the level ‘0’ are continuously output to the bus ‘BUS’ while the circuit component SK1 is being tested.”); 6:16-21 (“During testing of the circuit component SK1, the test control signal has the value ‘0’ ... This means that the value ‘0’ is continuously output to the bus while the circuit component SK1 is being tested”); 6:22-26 (“The fact that, while it is being tested the circuit component SK1 outputs data which never change or change only infrequently to the bus ‘BUS’ has the positive effect that the bus lines need never be reloaded or need to be reloaded only infrequently.”); 6:41-44 (“The fact that the data DOUT which actually need to be output to the bus ‘BUS’ are not output to the bus while the circuit component SK1 is being tested, but instead other data are output to the bus”); 7:1-3 (“It ought to be clear that it is not imperative for data continuously representing the level ‘0’ to be output to the bus ‘BUS’ while the circuit component SK1 is being tested.”); 7:5-8 (“Furthermore, provision may be made for data which do not continuously have one predetermined level, but

instead change, to be output to the bus ‘BUS’ while the circuit component SK1 is being tested.”); 7:48-50 (“Unlike the circuit component SK1 shown in FIG. 1, however, the circuit component SK2 shown in FIG. 2 outputs no data to the bus ‘BUS’ while it is being tested.”); 8:10-16 (“The bus termination logic unit BTL ensures that, *during testing of the circuit component SK1 (when and so long as the test control signal TESTC is signaling that the circuit component SK1 is currently being tested)*, the bus ‘BUS’ is terminated by one of the other components connected to the bus ‘BUS’”) (emphasis added); 8:38-42 (“*The fact that no data are output to the bus ‘BUS’ while the circuit component SK1 is being tested* has the positive effect that the output drivers T have no or only a negligibly low power consumption and consequently do not heat up at all, or heat up only to a very small extent.”) (emphasis added).

Furthermore, the specification of the ’473 Patent discloses that in contrast to the first embodiment of an electrical circuit designed for the first testing solution of “outputting data to the bus that is other data which would be output to the bus during normal operation,” “[t]he electrical circuit can *alternatively be designed* such that, *while it is being tested*, the circuit component which is to be tested *outputs no data to the bus*. An illustrative embodiment such an electric circuit is shown in FIG. 2 and is described below with reference thereto.” *Id.*, 7:24-29 (emphasis added). To

reinforce this concept, the '473 Patent further discloses that “[u]nlike the circuit component SK1 shown in FIG. 1, however, the circuit component SK2 shown in FIG. 2 *outputs no data to the bus ‘BUS’ while it is being tested.*” *Id.*, 7:48-50 (emphasis added).

Thus, the claims and the specification of the '473 Patent make clear that the claim limitations of claims 1 and 20 directed to the second, alternative testing solution of “outputting no data to the bus” means “outputting no data to the bus when and so long as the circuit component is being tested.”

Petitioner does not and cannot show that *Slemmer* discloses “outputting no data to the bus when and so long as the circuit component is being tested.” *See* Petition, pp. 25-29; 65. Rather, *Slemmer* merely teaches that during the testing of a circuit component that is outputting data (the same data that would be output during *Slemmer*’s normal operation) there are small intervals of time where no data is output. *See* Petition, pp. 25-29; 65. There is no disclosure from *Slemmer* that discloses “outputting no data to the bus when and so long as the circuit component is being tested.”

For at least these reasons, *Slemmer* does not teach, suggest, or disclose “said circuit component to be tested configured to perform an operation, during testing thereof, ... of outputting no data to said bus” of claim 1 or “while testing the circuit

component to be tested, performing an operation with the circuit component to be tested ... of outputting no data to the bus” of claim 20. Accordingly, Petitioner cannot show a likelihood that the challenged claims are unpatentable over *Slemmer*, and Ground 1 should be denied.

**C. Petitioner wholly failed to meet its burden that *Slemmer* discloses the claim elements of independent claims 1 and 20 directed to an operation “selected from the group”.**

Independent claim 1 requires “said circuit component to be tested configured to *perform an operation*, during testing thereof, *that is selected from the group* consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation,” and independent claim 20 requires “while testing the circuit component to be tested, *performing an operation* with the circuit component to be tested, *the operation selected from the group* consisting of outputting no data to the bus, and outputting data to the bus that is other than data which would be output to the bus during normal operation.” ’473 Patent, 11:8-14; 12:62-67 (emphasis added).

Petitioner has failed to show how the claim term “selected” is disclosed or rendered obvious by *Slemmer*. See Petition, pp. 25-29; 65. Indeed, the Petition does not even mention the term “selected.” *Id.*

For at least these reasons, Ground 1 should be denied because Petitioner has wholly failed to provide any type of meaningful analysis in the Petition as to the

term “selected.” *See Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (“[T]he Petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.”); *SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) (“rather than create (another) agency-led, inquisitorial process for reconsidering patents, Congress opted for a party-directed, adversarial process”); 37 C.F.R. § 42.22(a)(2) (“Each petition ... must include ... a detailed explanation of the significance of the evidence including material facts, and the governing law, rules, and precedent.”); 37 C.F.R. § 42.104(b)(4) (“The petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon.”); 35 U.S.C. § 312(a)(3) (Petitioner bears the burden of identifying “in writing and with particularity . . . the evidence that supports the grounds for the challenge to each claim”); *TCL Communication Technology Holdings Ltd. v. Dataquill Limited*, IPR2020-00746, Paper 21 at 22 (Sep. 18, 2020) (“It is Petitioner’s responsibility to cite specific evidence to support its arguments, not the Board’s”—nor Patent Owner’s—“responsibility to piece together evidence or speculate as to Petitioner’s position.”); *see also Whole Space Industries Ltd. v. Zipshade Industrial (B.V.I.) Corp.*, IPR2015-00488 Paper 14 at 18 (July 24, 2015) (citations omitted).

Indeed, as emphasized by the Federal Circuit, “[i]t is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial

petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016).

For at least these reasons, *Slemmer* does not teach, suggest, or disclose claim limitations directed to “selected” as recited by claims 1 and 20. Accordingly, Petitioner cannot show a likelihood that the challenged claims are unpatentable over *Slemmer*, and Ground 1 should be denied.

#### **VIII. THE PETITION DOES NOT DEMONSTRATE THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE UNDER GROUND 2.**

With respect to Ground 2, Petitioner again relies on *Slemmer* for multiple elements of the challenged claims. In particular, Petitioner relies solely on *Slemmer* for the disclosure of the claim limitations addressed above in Section VII. *See* Petition, pp. 73-75; 81-82. *Gasbarro* does not cure these deficiencies in the primary reference *Slemmer*. *Id.* Thus, for the same reasons set forth in Section VII, the proposed combination of *Slemmer* and *Gasbarro* does not disclose the limitations of the challenged claims addressed above in Section VII as to Ground 1. As such, Ground 2 necessarily fails.

#### **IX. PATENT OWNER’S FINAL COMMENTS**

Patent Owner does not concede the legitimacy of any arguments in the Petition that are not specifically addressed herein, and expressly reserves the right to rebut

any such arguments in its Patent Owner Response if *inter partes* review is instituted. Similarly, Patent Owner also does not concede any underlying contentions in the Petition and reserves the right to rebut them later. Additionally, Patent Owner is not limited to the arguments presented here in this Preliminary Response, but expressly reserves the right to raise further arguments, including claim construction arguments, not presented in this Preliminary Response.

## **X. CONCLUSION**

For the foregoing reasons, Patent Owner respectfully requests that the Board decline to institute *inter partes* review of the '473 Patent.

Dated: June 21, 2023

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### **CERTIFICATE OF COMPLIANCE WITH WORD COUNT**

Pursuant to 37 C.F.R. § 42.24(d), I certify that this Preliminary Response complies with the type-volume limits of 37 C.F.R. § 42.24(b)(1) because it contains 8,594 words, excluding the parts of this Patent Owner's Preliminary Response that are exempted by 37 C.F.R. § 42.24(a), according to the word processing system used to prepare this Patent Owner's Preliminary Response.

Dated: June 21, 2023

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## **CERTIFICATE OF SERVICE**

The undersigned certifies that the foregoing Patent Owner's Preliminary Response was served on June 21, 2023, to Lead and Back-up Counsel for Petitioner at the service address provided in Petitioner's Mandatory Notices:

Email:       xilinxMWETeam@mwe.com

Dated: June 21, 2023

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