UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

XILINX, INC.,

Petitioner

v.

POLARIS INNOVATIONS LIMITED,

Patent Owner.

U.S. PATENT NO. 6,701,473

Case No. IPR2023-00517

PETITIONER'S REQUEST FOR REHEARING ON DECISION DENYING INSTITUTION PURSUANT TO 37 C.F.R. § 42.71(d)

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Pursuant to 37 C.F.R. § 42.71(d), Xilinx, Inc. ("Petitioner") respectfully requests rehearing of the Board's Decision denying institution of *inter partes* review (IPR) of U.S. Patent No. 6,701,473 ("the '473 Patent"). *See* Decision Denying Institution, IPR2023-00517, Paper No. 12 (Sept. 18, 2023) ("Decision").

I. INTRODUCTION AND STATEMENT OF RELIEF REQUESTED

Petitioner requested IPR of claims 1–5, 7–10, 13–14, 20–24, 26–29, 32–33 of the '473 Patent across two obviousness grounds: Slemmer (EX1005) and Slemmer and Gasbarro (EX1006). *See* Petition for IPR, IPR2023-00517, Paper No. 2, at 2–3 (Feb. 6, 2023) ("Petition" or "Pet.").

The Board denied institution based on a purported failure of the asserted grounds to teach limitation [1.3][1] that requires:

> said circuit component to be tested configured to perform an operation, ***during testing thereof***, that is selected from the group consisting of outputting no data to said bus, and outputting data to said bus that is other than data which would be output to said bus during normal operation,

Decision 16 (emphasis added); *see also id.* at 17–20.

[1] Independent claim 20 recites a similar limitation of "outputting no data to said bus" or "outputting data to said bus that is other than data which would be output to said bus during normal operation" "while testing." *See* Decision 20.

Although the Board did not "discern a need to construe explicitly any claim terms," the Board required that "during testing" and "while testing" in limitations [1.3] and [20.3], respectively, requires "test operations" and not just enabling a test mode. *See* Decision 8–9, 18–20. Under this interpretation, the Board concluded that the operations described by Slemmer are not performed during or while testing. *See id.* at 18–20.

But the Board's conclusion overlooks and misapprehends several portions of the evidentiary record. First, it overlooks Patent Owner's admissions that the time periods shown in Figure 9 of Slemmer and relied upon in the Petition are indeed "during testing." Thus, there is no dispute between the parties that certain operations shown in Figure 9 occur during testing. Second, the Board's claim interpretation overlooks the intrinsic record of the '473 Patent, which does not expressly require "test operations" for there to be "testing."

Third, the Board misapprehended Slemmer's disclosure in concluding that the operations described by Slemmer are not performed "during testing" and that Slemmer's "memory device may be returned to the normal operating mode without performing inadvertent test operations." *See* Decision 12–13 and 19–20. Respectfully, there is no such disclosure in Slemmer. Slemmer simply discloses that multiple tests are performed. Slemmer tests whether the integrated circuit memory enters a test mode—which is itself a test—and then runs additional test

operations in response to entering the test mode. These test operations in Figure 9 of Slemmer do not contradict other disclosures in Slemmer, which does not disclose returning the memory to normal operation without performing special test operations.

Accordingly, the Board should grant Petitioner's request for rehearing to consider overlooked evidence in the record that the parties do not dispute that Slemmer's Figure 9 illustrates operations "during testing," consider overlooked evidence in the intrinsic record of the '473 Patent that does not support a narrow interpretation of "during testing" or "while testing," and reconsider misapprehended evidence in the record regarding Slemmer's disclosure. In view of this overlooked and misapprehended evidence, Slemmer teaches all elements of claims 1 and 20, and the challenged dependent claims (claims 2–5, 7–10, 13–14, 21–24, 26–29, 32–33). *See* Decision 21–22.

II. THE BOARD OVERLOOKED PATENT OWNER'S ADMISSIONS WHEN CONCLUDING THAT SLEMMER'S OPERATIONS ARE NOT PERFORMED "DURING TESTING"

The Board's conclusion that Slemmer's operations are not performed during testing overlooks Patent Owner's own admissions. Specifically, the Board concluded that "none of the operations in Figure 9 of Slemmer cited by Petitioner describe any operation performed 'during testing' or 'while testing.'" Decision at 18 (citing Patent Owner's Preliminary Response, IPR2023-00517, Paper No. 11, at

29–34 (June 21, 2023) ("Prelim. Resp.")). However, the Board overlooks Patent Owner's own admissions in its Preliminary Response that Slemmer "teaches outputting the [] data ***during testing*** at times t_4 to t_6 and at time t_8" (Prelim. Resp. 25–26, emphasis added) and "that ***during the testing*** of [Slemmer's] circuit component" there are also "intervals of time where no data is output" (Prelim. Resp. 33, emphasis added), both referring to the Petition's reliance on Figure 9. Nowhere does the Board indicate that it considered Patent Owner's admissions that at least the time periods between t_4 and t_6 and at time t_8 and other intervals where no data is output in Figure 9 of Slemmer are during or while testing of the integrated circuit memory, as asserted in the Petition. *See, e.g.*, Pet. at 27–28; Decision 16–20. Thus, the Board overlooked Patent Owner's admissions on Slemmer's circuit component outputting data and outputting no data during testing.

III. THE BOARD OVERLOOKED THE INTRINSIC RECORD IN LIMITING "DURING TESTING" OR "WHILE TESTING" TO TEST OPERATIONS

Independent claims 1 and 20 recite similar limitations in that the "circuit component" must perform during/while testing "an operation" that is selected from the group consisting of "outputting no data" and "outputting data . . . that is other than data which would be output . . . during normal operation." EX1001, 11:9–14, 12:62–67. In concluding that these claim limitations ([1.3] and [20.3]) require performing a test operation and not just entering a test mode of the circuit

component to be tested, the Board overlooked the intrinsic record of the '473 Patent. *See* Decision 16, 20. Indeed, the Board does not cite to or discuss the intrinsic record when addressing limitations [1.3] and [20.3]. *See* Decision 16–20. The '473 Patent does not define or otherwise limit testing of the circuit component to require actively running test operations or distinguish that from enabling a test mode or control of the circuit component. *See, e.g.,* EX1001, 8:4–9 ("During testing of the circuit component SK1, the test control signal has the value '0'. …"). Nor does the '473 Patent mention the phrase "test operation."

Further, the '473 Patent describes "during testing" as including the enablement of a test mode of the circuit component. In describing the Figure 3 embodiment, the '473 Patent states that "the output drivers are deactivated ***during testing*** of the circuit component which is to be tested" (EX1001, 10:24–27, emphasis added) and provides the following table to summarize the actions or operations:

TESTC	EN	Action
0	0	Test mode Output drivers deactivated Termination inactive
0	1	Test mode Output drivers deactivated Termination active
1	0	Normal operation Output drivers deactivated
1	1	Normal operation Output drivers activated

(*Id.* at 10:5–15 (cited by Pet. 6–7)). During testing—when the test control signal (TESTC) has the value '0' and the output drivers are deactivated—the actions merely include entering a "Test mode" of the circuit component. *See id.* There is no additional requirement of actively running test operations during testing of the circuit component. Thus, "during testing" ***includes*** entering a test mode and does not further require actively running test operations.

Applying this understanding of the '473 Patent, even assuming for the sake of argument that Slemmer does not disclose actively running test operations in Figure 9 (it does, as explained in the following section), Figure 9 of Slemmer discloses multiple operations "during testing" or "while testing." The Board's contrary conclusion that no operation is "performed during the testing mode" misapprehends this evidence. *See* Decision 20, n.3. Specifically, after enabling of the test mode at time t_3 (assertion of the 'T' signal), Figure 9 of Slemmer shows multiple operations on the DQ terminal (outputting no data and data) occur while Slemmer's memory 1 ("circuit component to be tested") remains in the test mode. *See* Pet. at 25–26 (describing "outputting no data") and at 27–28 (describing "outputting data"). Accordingly, Slemmer teaches claims 1 and 20.

IV. THE BOARD MISAPPREHENDED SLEMMER'S DISCLOSURE

Even under a narrower interpretation of the claim, not advanced by Petitioner or Patent Owner, in which "testing" requires actively running test

operations and not simply enabling a test mode, the Board misapprehended the disclosure of Slemmer, which does disclose actively running testing operations in certain of the time periods shown in Figure 9. In its decision, the Board concluded that "none of the operations in Figure 9 . . . describe any operation performed 'during testing' or 'while testing,'" because the test mode is enabled at time t_3 before special test operations. *See* Decision 18–19. In support, the Board relies on the following portions of Slemmer:

> Control of output buffers 22 by the test mode enable signal on line T provides particularly advantageous functions in memory 1 constructed according to this embodiment of the invention. A first function of such construction is that memory 1 can communicate its special test mode status, providing the user (or the interrogating test equipment) acknowledgment that the device is in a special test mode, prior to such time as special test operations are performed.

EX1005 at 35:22–30; and

> Responsive to line T at a high logic level, OR gate 33 will present a high logic level to AND gate 26. Since terminals OE and W- are at high logic levels, and with line 32 from parallel test circuitry 28 remains high (i.e., the parallel test either passed, or has not taken place), terminals DQ go into an active state at time t_4.

EX1005 at 36:26–32.

However, these portions of Slemmer do not support the conclusion that there is no actively running testing operation in Figure 9. As explained above, the parties do not dispute that Figure 9 teaches the component outputs data and no data ***during testing***. *Supra* Section II; Pet. 25–29; Prelim. Resp. 25–26, 33. As explained

below, these and other portions of Slemmer cited to or relied upon in the record disclose performing multiple tests with respect to Figure 9—(1) determining successful entry into a test mode and providing an acknowledgement of such; and (2) performing additional test operations (including a parallel test)—any one of which satisfies the claim limitation of "during testing" or "while testing."

A. SLEMMER DISCLOSES THAT DETERMINING AND ACKNOWLEDGING SUCCESSFUL ENTRY INTO A TEST MODE IS A TEST

Slemmer discloses that determining and acknowledging successful entry into the test mode is a test itself. Like a special test operation, Slemmer describes entry into the test mode as a procedure that can pass or fail. *See* EX1005, 35:22–42 (cited in Pet. 10, 14–15); *see also* Pet. 79 (quoting EX1005, 35:36–42). Specifically, Slemmer explains that "it is not always certain that" the test mode is entered as desired because doing so may require extraordinary cycles such as overvoltage excursions. EX1005, 35:22–42 (cited in Pet. 14–15); *see also* Pet. 11 ("The memory includes test mode enable circuitry (TMEC) 29 that receives input signals on lines A1, A3, and TRST . . . .") (citing EX1005 at 9:19–30, 9:44–48, FIGS. 1–2b). To solve the problem of uncertain test mode entry, Slemmer describes that the memory provides an acknowledgement of test-mode entry for determining "whether the memory actually failed the test or if it merely failed to enter the test mode" (EX1005, 35:36–42 (quoted by Pet. 79)) and for identifying

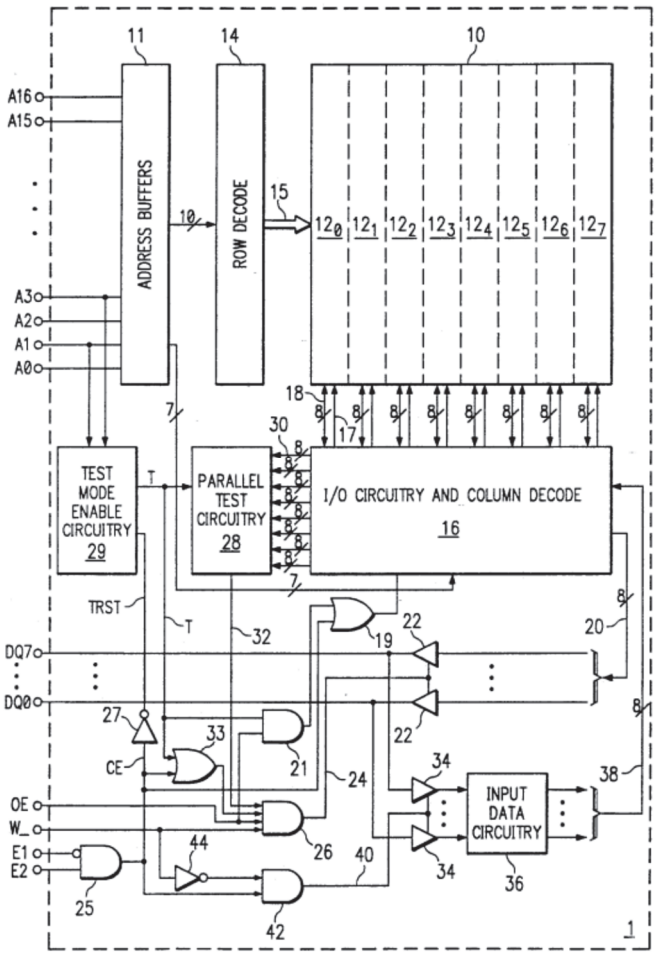
"which test mode has been enabled" (EX1005, 36:45–49 (quoted by Pet. 28)). Thus, actively determining and acknowledging successful test-mode entry is testing of Slemmer's integrated circuit memory. *See* Pet. 28.

B. SLEMMER DISCLOSES ADDITIONAL TEST OPERATIONS THAT START IN RESPONSE TO TEST MODE ENTRY

In addition to this test, Slemmer discloses additional test operations are performed on the memory array (10) of Slemmer's integrated circuit memory (1). *See* EX1005, FIG. 1, 35:25–30. Specifically, multiple test data sets are received, decoded, and provided by "I/O Circuitry and Column Decode" (circuit 16) and then the test data sets are compared by "Parallel Test Circuitry" (circuit 28) to determine if they all contain the same data, which indicates the test passed with no error. *See* Pet. 11–12 (citing EX1005, FIGS. 1–2B, 7:35–8:58, 9:10–30).

These separate test operations each start in response to the integrated circuit memory entering a test mode, which corresponds to line 'T' transitioning to a high logic level (assertion of 'T'). *See* Pet. 11 (EX1005, 9:19–30, 9:44–48, FIGS. 1–2b). Besides the assertion of 'T,' there is no other control or mechanism shown in Figure 1 and corresponding Figure 9 of Slemmer (*see* EX1005, 5:44–46 (cited by Decision 13)) that starts, delays the start, or determines whether to start test operations after acknowledgement of test mode entry. As shown in Figure 1 of Slemmer, circuit 16 is only enabled in response to a signal provided by gate 19.

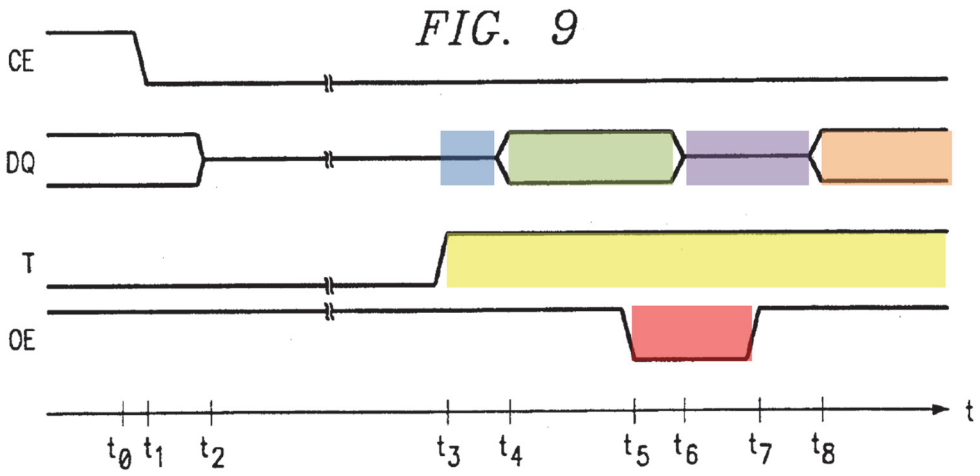
FIG. 1



EX1005, FIG. 1; Pet. 21, 23–25 (citing EX1005, FIG. 1, 37:1–20, 7:56–8:3, 8:59–9:9; EX1003, ¶¶81, 86–87); Pet. 11–12 (citing EX1005 at 7:35–8:58, 9:10–30, 9:44–48, FIGS. 1–2b). In response to the assertion of 'T' and a chip enable for testing (OE), circuit 16 is enabled via gates 21 and 19 to perform test operations by providing test data sets to circuit 28. *See id.* Figure 1 also shows that circuit 28 is only enabled in response to the assertion of 'T' to compare the test data sets received from circuit 16 via lines 30. *See* Pet. 11–12 (citing EX1005, 7:35–8:58, 9:10–30, 9:44–48, FIG. 1); *see also* EX1005, 8:20–23 (performing comparison

"when memory 1 is placed into a special test mode"), 8:23–31 (describing circuit 28). Thus, the assertion of 'T' is the only control to enable circuit 16 for providing test data sets when the chip is enabled for testing and the only control to enable circuit 28 for comparing the data sets provided. There is no other control disclosed in Slemmer that starts, delays the start, or determines whether to start test operations shown in Figure 9.

Against this backdrop, Figure 9 of Slemmer discloses the performance of multiple test operations that are each performed "during testing" or "while testing."



EX1005, FIG. 9 (reproduced in Pet. 26, 28). At time t_3, the memory 1 is testing whether it successfully entered a test mode, which is represented by the assertion of the 'T' signal to a high logic level (annotated in yellow above) (Pet. 25–26) and acknowledged by time t_4 by the DQ terminal transitioning to an active, low-impedance state (annotated in green) (Pet. 27–28).

Although Slemmer discloses that it can "communicate its special mode status," which occurs at time t_4, before "special test operations are performed" (EX1005, 35:25–30 (cited by Decision 12, 18)), that statement merely describes the relative timing between communicating the acknowledgement of successful test mode entry and performing parallel test operations (by comparing test data sets) in circuit 28. *See* EX1005, 36:26–32 (line 32 from circuit 28 "remains high (i.e., the parallel test either passed, or has not taken place)") (cited by Decision 13–14, 18). However, these statements only refer to Slemmer's special, parallel test operation of comparing the data sets by circuit 28. Nowhere does Slemmer indicate that this operation is the only test operation, nor could it be the only test operation given that circuit 16 must provide the test data sets to circuit 28—a separate test operation—*before* the comparison between them in circuit 28. *See* Pet. 11–12 (citing EX1005, 7:35–8:58, FIG. 1).

Accordingly, Figure 9 of Slemmer shows that additional test operations start in response to enabling the test mode at time t_3. First, the assertion of 'T' enables circuit 16, which performs test operations by providing the test data sets to circuit 28 when the "OE" signal is asserted, as it is at times t_3 and t_4 among other times in Figure 9. *See* Pet. 21, 23–25 (citing EX1005, FIG. 1, 37:1–20, 7:56–8:3, 8:59–9:9; EX1003, ¶¶81, 86–87); Pet. 11–12 (citing EX1005, 7:35–8:58). And second, after circuit 16 provides the test data sets to circuit 28, the assertion of 'T' enables

circuit 28 to perform parallel test operations by comparing the data sets. *See* Pet. 10–12 (citing EX1005, Abstract, 7:35–8:58, 35:22–36:68, FIGS. 1, 9; EX1003, ¶¶61–63). Thus, test operations for providing the test data sets begins just after time t_3 and further test operations for parallel testing (by comparing the test data sets) begins just after the test data sets are provided. *See id.* As shown in Figure 9, memory 1 continues to provide a low-impedance state on DQ until time t_6, which indicates that the parallel test may have passed. *See id.*; *see also* EX1005, 36:26–32. Thus, there are multiple test operations disclosed by Figure 9 of Slemmer that all occur during or while testing.

C. THE TEST OPERATIONS SHOWN IN FIGURE 9 OF SLEMMER DO NOT CONTRADICT SLEMMER'S DISCLOSURE OF ENABLING THE TEST MODE BEFORE PERFORMING SPECIAL TEST OPERATIONS

The Board also misapprehended the purposes of Slemmer's disclosure for enabling the test mode before performing special test operations when it concluded that the test operations in Figure 9 "directly contradict key disclosures in Slemmer."[2] Decision 20. This procedure is not performed, as the Board concluded,

[2] Similarly, the Board misapprehends the benefit of communicating test-mode entry, which merely provides ***detection*** of test-mode entry and does not ***avoid*** inadvertent entry. *See* Decision 20; EX1005, 35:47–51. Other features in

"so that the memory device may be returned to the normal operating mode without performing inadvertent test operations." *Id.* at 12–13 and 19–20 (citing EX1005, 35:47–51). There is no disclosure in Slemmer of returning to normal operating mode (or exiting test mode) *before* test operations are performed. *See* Pet. 21–25; EX1005, FIGS. 1, 9. Nor does Slemmer disclose any mechanism to decide whether to proceed with further test operations after analyzing the acknowledgement of test-mode entry. Slemmer merely states that the memory may "return to the normal operating mode" if the test mode entry was inadvertent and provides a mechanism for exiting the test mode via the assertion of chip enable (CE). EX1005, 35:47–51 (cited by Pet. 20), FIGS. 1, 9; *see also* Pet. 21–25. As shown by the first signal "CE" in Figure 9—a disclosure overlooked in the Board's Decision—the memory is not enabled for normal operation and never exits the test mode because CE remains de-asserted after time t_1. *See* EX1005, FIG. 9; Pet. 22–24 (explaining operation of CE). Thus, there is no contradiction between the test operations in Figure 9 and other disclosures in Slemmer.

Slemmer's memory, such as requiring a series of signals with a unique code to enable the test mode and disabling the ability to enter the test mode during power-up, avoid inadvertent entry. *See* EX1005, 5:3–7, Abstract (cited by Decision 20).

V. CONCLUSION

The Board's conclusion that Figure 9 of Slemmer does not disclose any operation performed "during testing" or "while testing" overlooks Patent Owner's admissions to the contrary. Further, by implicitly construing "during testing" or "while testing" to require actively running test operations and exclude simply enabling a test mode, the Board improperly interpreted the claims without consulting the intrinsic record, which does not support imposing such a limitation. In addition, the Board misapprehended Slemmer, which discloses multiple tests performed during time periods illustrated in Figure 9. Additionally, Petitioner's interpretation of Figure 9 does not contradict Slemmer as the Board concluded. That conclusion overlooks Figure 9 which does not exit the test mode and is based on a misapprehension of Slemmer, which does not enable returning to normal operation before performing test operations.

In view of the overlooked and misapprehended evidence, Slemmer teaches all elements of challenged independent claims 1 and 20, and the challenged dependent claims (claims 2–5, 7–10, 13–14, 21–24, 26–29, 32–33). Accordingly, Petitioner requests institution of inter partes review.

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Respectfully submitted,

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.*, the undersigned certifies that on October 18, 2023, a complete and entire copy of this PETITIONER'S REQUEST FOR REHEARING ON DECISION DENYING INSTITUTION was provided via electronic mail to the counsel of record for the Patent Owner as follows:

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