AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22cv352	9/12/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Taiwan Semiconductor Manufacturing Company Limited

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	8,775,833	7/8/2014	Daedalus Prime LLC
2	8,898,494	11/25/2014	Daedalus Prime LLC
3	10,049,080	8/14/2018	Daedalus Prime LLC
4	10,705,588	7/7/2020	Daedalus Prime LLC
5	9,831,306	11/28/2017	Daedalus Prime LLC

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

SAMSUNG 1002

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

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☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
2:22cv352	9/12/2022	Eastern District of Texas

PLAINTIFF	DEFENDANT
Daedalus Prime LLC	Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Taiwan Semiconductor Manufacturing Company Limited

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,319,812	6/11/2019	Daedalus Prime LLC
2	10,700,178	6/30/2020	Daedalus Prime LLC
3	11,251,281	2/15/2022	Daedalus Prime LLC
4			
5			

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1

CONFIRMATION NO. 9752

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

POWER OF ATTORNEY NOTICE

OC000000129715796

Date Mailed: 11/12/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/04/2021.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nbekele/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1

CONFIRMATION NO. 9752

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

POA ACCEPTANCE LETTER

OC000000129715804

Date Mailed: 11/12/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/04/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/nbekele/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/789,315
Filing Date	October 20, 2017
First Named Inventor	Milton Clair Webb
Title	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
Art Unit	2822
Examiner Name	Roy Karl Potter
Attorney Docket Number	D480-012057

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	November 4, 2021
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
15/789,315	October 20, 2017

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 00164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	
Name	Lisa Hopkinson		
Title	Administrator of Patents		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Name | Lisa Hopkinson

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
15/789,315	**11/04/2021 04:30:09 PM ET**	**P60397US-C1**

Title of Invention

SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	10319812
CONFIRMATION #	9752	FILED BY	Ian MacKinnon
PATENT CENTER #	60385432	FILING DATE	10/20/2017
CUSTOMER #	31817	FIRST NAMED INVENTOR	Milton Clair WEBB
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2021-11-04_POA_D480-012057.pdf	2	Power of Attorney	1258 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
2021-11-04_POA_D480-012057.pdf	C0D2A5687B58A3285E77CCB59B1714AA8876C0183BA8ED9AF36BD737B836FC2395CE7EEEDD86FE69960F92990D41A308849A4014854EBBCE4E80FEA730B8CEEB

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Patent Application Fee Transmittal	
Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	36101688
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Receipt Date:	23-MAY-2019
Filing Date:	20-OCT-2017
Time Stamp:	18:44:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	052419INTEFSW00005169500393
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US_PLACE-IN-FILE_IDS_05-23-19.pdf	103112 e04875f7a4c00709cf25d6f8a108ba10f7239224	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	Ref_P60397CN-OA2_05-08-19.pdf	19314808 035201d1d04fec971fdb70d2eb7986ccdbe0cbef	no	14
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30556 d142087fd2e1757c7dfbd0f9e8e5fd8073ad5566	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	19448476		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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New International Application Filed with the USPTO as a Receiving Office

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Webb et al.** Application No: 15/789,315 Filed: October 20, 2017 For: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME	Examiner: Potter, Roy Karl Art Unit: 2822 Atty Docket No.: P60397US-C1 Confirmation No.: 9752

Mail Stop Issue Fee
Assistant Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT AFTER ALLOWANCE

In accordance with Applicant's duty of disclosure, this Information Disclosure Statement, substitute for form 1449A/PTO (based on PTO/SB/08A), and cited reference(s) are being submitted subsequent to payment of the Issue Fee but prior to issuance. It is respectfully requested that the cited reference(s) be placed in the file and that the subject application not be withdrawn from issuance.

The fee for submission of the Information Disclosure Statement is enclosed herewith.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

The Commissioner is authorized to charge any deficiencies or credit any overpayments in connection with this submission to Deposit Account No. 50-0393, and is requested to notify us of same.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT P.C.

Date: May 23, 2019

/Justin K. Brask/
Justin K. Brask, Reg. #61080

Schwabe, Williamson & Wyatt P.C.
1211 SW 5th Ave., Ste. 1900
Portland, Oregon 97204
Telephone: (503) 222-9981
Facsimile: (503) 796-2900

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	06/11/2019	10319812	P60397US-C1	9752

31817 7590 05/22/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Intel Corporation, Santa Clara, CA;
Milton Clair WEBB, Aloha, OR;
Mark BOHR, Aloha, OR;
Tahir GHANI, Portland, OR;
Szuya S. LIAO, Portland, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	2822
	Examiner Name	POTTER, ROY KARL
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

Change(s) applied to document, /N.W.S./ 3/29/2019

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		US-20070090443	04/26/2007	Byung-Yong Choi et al.	
/R.K.P/		US-20130065371	03/14/2013	Andy C. Wei et al.	
/R.K.P/		US-20090242986	10/01/2009	Yukio Nakabayashi et al.	
/R.K.P/		US-20060141706	06/29/2006	Seung-Wan Hong	
/R.K.P/		US-20120211808	08/23/2012	Andy Wei et al.	
/R.K.P/		US-7,820,551	10/26/2010	~~Kabushiki Kaisha Toshiba~~	Yagishita, et al.
/R.K.P/		US-7,026,199	04/11/2006	~~Hynix Semiconductor Inc.~~ Lee	

Change(s) applied to document, /U.F./ 3/21/2019

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
		JP-2008172082	07/24/2008	TOSHIBA CORP		
		JP-2005136376	05/26/2005	Hynix Semiconductor Inc.		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		Office Action for Taiwan Patent Application No. 107113364 (Attorney Docket No. P60397TW-D2-D1) mailed October 18, 2018, 5 pgs., no translation.	
/R.K.P/		Notice of Allowance for Taiwan Patent Application No. 106120024 (Attorney Docket No. P60397TW-D2) mailed March 19, 2018, 2 pgs., no translation.	X
/R.K.P/		Notice of Allowance and Search Report for Taiwan Patent Application No. 105134078 (Attorney Docket No. P60397TW-D) mailed May 19, 2017, 3 pgs., no translation.	
/R.K.P/		Notice of Allowance for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed September 19, 2016, 2 pgs., no translation.	
/R.K.P/		Office Action and Search Report for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed May 17, 2016, 3 pgs., no translation.	
/R.K.P/		Notice of Allowance for Japanese Patent Application No. 2016-526912 (Attorney Docket No. P60397JP) mailed March 13, 2018, 1 Pg., no translation.	
/R.K.P/		Office Action for European Patent Application No. 13899890.1 (Attorney Docket No. P60397EP) mailed July 11, 2017, 2 pgs.	

EXAMINER /ROY K POTTER/ **DATE CONSIDERED** 02/01/2019

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	TDB
	Filing Date	Herewith
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	
	Examiner Name	TDB
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		US-2007 /0054464	03-08-2007	ZHANG, Guowei	
/R.K.P/		US-2008/0080380	04-03-2008	LEE, Kwang il, et al.	
/R.K.P/		US-20110021027	01-27-2011	JOHNSON, Frank S.	
/R.K.P/		US-2013/0020615	01-24-2013	FAN, Su Chen, et al.	
/R.K.P/		US-20070080380	04-12-2007	CHANG.PETER	
/R.K.P/		US-20110291188	12-01-2011	CHENG, KANGGUO, et al.	
/R.K.P/		US-20130134506	05-30-2013	YAGISHITA, ATSUSHI	
/R.K.P/		US-20050056888	03-17-2005	YOUN, JAE-MAN	
/R.K.P/		US-20130214364	08-22-2013	JAGANNATHAN, HEMANTH, ET AL.	
/R.K.P/		US-6,515,319	02-04-2003	~~INFINEON TECHNOLOGIES AG~~ Widmann, et al.	
/R.K.P/		US-7,781,274	08-24-2010	NAKABAYASHI, YUKIO, ET AL.	

Change(s) applied to document, /N.W.S./ 3/29/2019

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
/R.K.P/		KR-20050082099	08-22-2005	CHOI, Jung A., et al.		
/R.K.P/		TW-201017772	05-01-2010	WEI, ANDY, et al.		
/R.K.P/		JP-2009260221	11-05-2009	TOSHIBA CORP		
/R.K.P/		JP-2004-356472	12-16-2004	RENESAS TECH CORP		
/R.K.P/		JP-2002-530872	09-17-2002	INFINCON TECHNOLOGIES AG		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		International Search Report and Written Opinion from PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) Mailed September 26, 2014, 10 pages.	
/R.K.P/		International Preliminary Report on Patentability for PCT Application No. PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) mailed June 30, 2016, 7 pages.	
/R.K.P/		Non-Final Office Action and Search Report for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed June 3, 2016, 3 pgs.'	
/R.K.P/		Notice of Reasons for Refusal from Japanese Patent Application No. 2016-526912 (Attorney Docket No. P60397JP) mailed July 26 2017, ·10 Pgs., English translation.	
/R.K.P/		Non-Final Office Action for U.S. Patent Application No. 15/024,750 (Attorney Docket No. P60397US) mailed February 13, 2017, 6 pgs.	

EXAMINER /ROY K POTTER/ **DATE CONSIDERED** 01/30/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 000197

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	15/789,315

Completed by (check one):

☐ Applicant/Inventor — /Justin K. Brask/ (Signature)

☑ Attorney or Agent of record 61080 (Reg. No.) — Justin K. Brask (Typed or printed name)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) — 503-222-9981 (Requester's telephone number)

☐ Assignee recorded at Reel _____ Frame_____ — 4/30/2019 (Date)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask/Lisa Puccinelli
Attorney Docket Number:	P60397US-C1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt	
EFS ID:	35876234
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Receipt Date:	30-APR-2019
Filing Date:	20-OCT-2017
Time Stamp:	20:10:58
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	050119INTEFSW00007874500393
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P60397US-C1_Issue_Fee_04-30-19.pdf	93715 b3e563843756dea8ee28aad86a7740219b4e5e83	no	1
Warnings:					
Information:					
2	Maintenance Fee Address Change	P60397US-C1_Maintenance_Fees.pdf	312398 7c2fd83fa88f19324386d4644fa28886e133ac0f	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30450 8b7a7440fd9207fbfb8193aa89b623156ba776c7	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	436563		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 02/12/2019
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Lisa Puccinelli	(Typed or printed name)
/Lisa Puccinelli/	(Signature)
April 30, 2019	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1	9752

TITLE OF INVENTION: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-369000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwabe, Williamson & Wyatt, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Intel Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-0393

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Justin K. Brask/ Date April 30, 2019

Typed or printed name Justin K. Brask Registration No. 61080

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1	9752

31817 7590 04/24/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
POTTER, ROY KARL	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
04/24/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
15/789,315	10/20/2017	WEBB et al.	P60397US-C1

	EXAMINER	
SCHWABE, WILLIAMSON & WYATT, P.C. 1211 SW 5th Avenue, Suite 1600 Portland, OR 97204	ROY K POTTER	
	ART UNIT	PAPER
	2822	20190419

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The communication is being sent with a copy of the Information Disclosure Statement of 4/10/18.

/ROY K POTTER/
Primary Examiner, Art Unit 2822

PTO-90C (Rev.04-03)

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Webb, et al.
	Group Art Unit	2822
	Examiner Name	Potter, Roy Karl
Sheet 1 of 1	Attorney Docket No: P60397US-C1	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		Office Action from Singapore Patent Application No. 11201603813Q (Attorney Docket No. P60397SG), mailed March 8, 2019, 5 pgs.	
/R.K.P/		Office Action from Japanese Patent Application No. 2018-077178 (Attorney Docket No. P60397JP-D1), mailed March 26, 2019, 8 pgs.	X
/R.K.P/		Office Action from Taiwan Patent Application No. 107113364 (Attorney Docket No. P60397TW-D2-D1), mailed February 25, 2019, 2 pgs.	

EXAMINER /ROY K POTTER/ **DATE CONSIDERED** 04/19/2019

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Webb, et al.
	Group Art Unit	2822
	Examiner Name	Potter, Roy Karl
Sheet 1 of 1	Attorney Docket No: P60397US-C1	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action from Singapore Patent Application No. 11201603813Q (Attorney Docket No. P60397SG), mailed March 8, 2019, 5 pgs.	
		Office Action from Japanese Patent Application No. 2018-077178 (Attorney Docket No. P60397JP-D1), mailed March 26, 2019, 8 pgs.	X
		Office Action from Taiwan Patent Application No. 107113364 (Attorney Docket No. P60397TW-D2-D1), mailed February 25, 2019, 2 pgs.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal	
Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask/Lisa Puccinelli
Attorney Docket Number:	P60397US-C1
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	35691185
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Receipt Date:	10-APR-2019
Filing Date:	20-OCT-2017
Time Stamp:	20:45:07
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	041119INTEFSW00006553500393
Deposit Account	500393
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US-C1_IDS_04-10-19.pdf	293985 7e1b872c2e6b18cf64bffde63c3e1b3188ae8965	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
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2	Other Reference-Patent/App/Search documents	Ref_P60397JP-D1_03-26-19.pdf	133238 de83cacf47873c112c4ff58c93dd9c3f0b7db5ef	no	8
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3	Other Reference-Patent/App/Search documents	Ref_SG_OA_02-26-19.pdf	297816 7a550b7ee92b90ad718d0ff3643001af3929f582	no	5
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4	Other Reference-Patent/App/Search documents	Ref_TW-D2-D1_NOA_02-25-19.pdf	95543 f11a919222c38c9082fd4ff069ab087b496abe71	no	2
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5	Fee Worksheet (SB06)	fee-info.pdf	30600 f1c48a1a6d452bfa6cf9a7a0a99114797863 9d21	no	2
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application No.	15/789,315
	Filing Date	October 20, 2017
	First Inventor	Webb, et al.
	Art Unit	2822
	Examiner Name	Potter, Roy Karl
	Attorney Docket No.	P60397US-C1 Conf. No. 9752

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Name/Print	Justin K. Brask	Registration Number	61080

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1	9752

31817 7590 04/10/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
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EXAMINER	
POTTER, ROY KARL	

ART UNIT	PAPER NUMBER
2822	

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15/789,315	10/20/2017	WEBB et al.	P60397US-C1

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SCHWABE, WILLIAMSON & WYATT, P.C. 1211 SW 5th Avenue, Suite 1600 Portland, OR 97204		ROY K POTTER	
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PTO-90C (Rev.04-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Webb, et al.
	Group Art Unit	2822
	Examiner Name	Potter, Roy Karl
Sheet 1 of 1	Attorney Docket No: P60397US-C1	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
/R.K.P/		CN101952948	01-19-2011	Werner, Juengling		X
/R.K.P/		CN103137445	6/5/2013	Yuguobin Yu		X

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/R.K.P/		Office Action from Chinese Patent Application No. 201380081048.3 (Attorney Docket No. P60397CN), mailed November 27, 2019, 6 pgs.	

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	Examiner Name	Potter, Roy Karl
Sheet 1 of 1	Attorney Docket No: P60397US-C1	

US PATENT DOCUMENTS					
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		CN101952948	01-19-2011	Werner, Juengling		x
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Bibliographic data: CN101952948 (A) — 2011-01-19

Devices including fin transistors robust to gate shorts and methods of making the same

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Applicant(s): MICRON TECHNOLOGY INC ± (MICRON TECHNOLOGY INC)

Classification: - international: ***H01L21/336; H01L21/8242; H01L29/78***
- cooperative: **H01L27/0886**; **H01L27/10823**; **H01L27/10826**; **H01L27/10876**; **H01L27/10879**; **H01L29/4236**; **H01L29/66795**; **H01L29/7851**

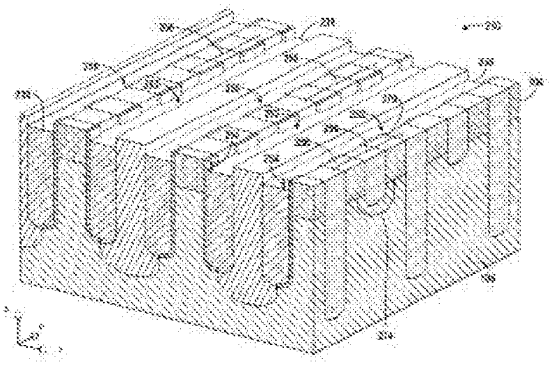
Application number: CN200980105433 20090129

Priority number(s): WO2009US32357 20090129 ; US20080033780 20080219

Also published as: CN101952948 (B) EP2243154 (A1) EP2243154 (B1) KR101603353 (B1) KR20100125253 (A) SG188792 (A1) TW200947567 (A) TWI408752 (B) US2009206443 (A1) US2015008535 (A1) US8866254 (B2) US9087721 (B2) WO2009105317 (A1) less

Abstract of CN101952948 (A)

Disclosed are methods, systems and devices, including a method that includes the acts of etching an inter-row trench (144, 220) in a substrate (102, 210), substantially or entirely filling the inter-row trench (144, 220) with a dielectric material (150, 222), and forming a fin (190, 258) and an insulating projection (168, 242) at least in part by etching a gate trench (164, 238) in the substrate (102, 210). In some embodiments, the insulating projection (168, 242) includes at least some of the dielectric material (150, 222) in the inter-row trench (144, 220).



Patents 101952948 Sign in

Devices including fin transistors robust to gate shorts and methods of making the same

Abstract

Disclosed are methods, systems and devices, including a method that includes the acts of etching an inter-row trench (144, 220) in a substrate (102, 210), substantially or entirely filling the inter-row trench (144, 220) with a dielectric material (150, 222), and forming a fin (190, 258) and an insulating projection (168, 242) at least in part by etching a gate trench (164, 236) in the substrate (102, 210). In some embodiments, the insulating projection (168, 242) includes at least some of the dielectric material (150, 222) in the inter-row trench (144, 220).

Classifications

H ELECTRICITY
H01 BASIC ELECTRIC ELEMENTS
H01L SEMICONDUCTOR DEVICES; ELECTRIC SOLID STATE DEVICES NOT OTHERWISE PROVIDED FOR
H01L27/00 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate
H01L27/02 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier
H01L27/04 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier the substrate being a semiconductor body
H01L27/08 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier the substrate being a semiconductor body including only semiconductor components of a single kind
H01L27/085 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier the substrate being a semiconductor body including only semiconductor components of a single kind including field-effect components only
H01L27/088 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier the substrate being a semiconductor body including only semiconductor components of a single kind including field-effect components only the components being field-effect transistors with insulated gate
H01L27/0886 Devices consisting of a plurality of semiconductor or other solid-state components formed in or on a common substrate including semiconductor components specially adapted for rectifying, oscillating, amplifying or switching and having at least one potential-jump barrier or surface barrier; including integrated passive circuit elements with at least one potential-jump barrier or surface barrier the substrate being a semiconductor body including only semiconductor components of a single kind including field-effect components only the components being field-effect transistors with insulated gate including transistors with a horizontal current flow in a vertical sidewall of a semiconductor body, e.g. FinFET, MuGFET

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CN101952948B
China

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Other languages: Chinese

Inventor: [illegible]

Worldwide applications

2008 US 2009 EP SG KR CN WO TW 2014 US

Application CN 200980105433 events

2008-02-19 Priority to US12/033,780
2008-02-19 Priority to US12/033,780
2009-01-29 Application filed by [illegible]
2009-01-29 Priority to PCT/US2009/032357
2011-01-19 Publication of CN101952948A
2012-10-03 Application granted
2012-10-03 Publication of CN101952948B

Info: Patent citations (89), Cited by (50), Legal events, Similar documents, Priority and Related Applications

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Claims (23)

translated from Chinese

A device manufacturing method comprising a fin transistor gate resistance short circuit, comprising: etching the trench in the substrate lines; dielectric material partially or completely filling the inter-row groove; and at least and a fin part formed by etching the gate insulating projection trench in the substrate, wherein the projecting portion comprises at least some of the insulating dielectric material in the trench in the dielectric material between the lines; gate with a gate electrode material filling said trench; and the recessed gate material below the top surface of the fin.

2. The method of claim i, wherein the etching the trench line comprising: a sacrificial region on said substrate forming a plurality of trenches precursor; and forming a spacer in said precursor trench wherein said spacer member trench narrows the precursor.

3. The method according to claim 2, wherein said spacer member so that said groove is narrowed to a width less than the resolution limit of photolithography.

4. The method according to claim 2, which comprises using the sidewall spacers and sacrificial region as a mask to etch the inter-row groove.

The method according to claim i, wherein the substrate comprises etching the trench etching the row line trenches through the upper doped region and at least partially into the lower portion of the doped region.

6. The method of claim i, wherein the dielectric material is partially or completely filling the inter-row trenches comprises: forming a trench in a first row between the liner; and the spin-on dielectric is applied to the said substrate.

7. The method according to claim i, comprising: a shield between the rows of the trench with a sacrificial material is etched and the first sidewall spacer; and with the dielectric material partially or completely fill the between said line trenches after removing the sacrificial material.

8. The method according to claim 7, comprising: after removing the sacrificial sidewall spacer material is formed on a second surface of the first sidewall spacer; and the second at least partially with two of said shield sidewall spacer etching the gate trench.

9. The method according to claim i, wherein at least a portion of the partially formed by the fin and the insulating projection comprises etching the dielectric material in said gate trench etching of the substrate.

10. The method according to claim i, wherein the fin is formed at least in part by the protruding portion and the insulating etching the gate trench in said substrate and comprising a plurality of fin rows are formed simultaneously by etching a plurality of gate trenches and a plurality of insulating protrusions.

11. The method according to claim 10, wherein: the insulation between the protruding portion of each of the plurality of insulating projecting portions inserted in the plurality of rows of fins of one pair of fins row; and the plurality on either side of the trench gate trench gate disposed in the plurality of fins each fin row line of the plurality of fin rows between said insulating projecting portions adjacent the insulating projection .

12. The method of claim i, wherein: forming a trench comprises etching between the rows of the substrate by a photolithography step on the substrate a first mask, and at least partially through said liner etching the gate trench is formed in the bottom of the fin and the insulating portion comprises a projection forming a second mask on the substrate by a second photolithography step.

13. The method according to claim 12, wherein the second mask is displaced relative to the first mask a distance equal to half the pitch of the first mask.

14. The method according to claim 13, wherein: said first mask comprises forming a first lithographic tools formed by the first mask; forming said second mask means comprises a second forming lithographic tools the second mask, or more than twice as large as the first lithography tool resolution twice the resolution of the second resolution lithography tool wherein the first lithography tool.

15. The method according to claim 13, wherein forming said second mask comprises a mask pitch precursor times

16. The method according to claim i, wherein the gate material filling the trench comprises the gate material completely fills the gate trench.

17. The method according to claim i, wherein the gate material is recessed below the top surface of the fin is less than or equal to 1000 Angstroms.

18. The method according to claim i, wherein the gate material partially overlap the upper doped region.

19. An apparatus fin transistor comprises a short circuit resistance of the gate, comprising: a semiconductor fin; the gate trench, which is disposed on either side of the semiconductor fin; insulating projection, which is disposed in said semiconductor separated from the semiconductor fin and the gate trenches by a least in part on either side of the fin; and a gate, which is disposed in each gate trench, wherein each gate recess by and below the top of the semiconductor fin.

20. The apparatus according to claim 19, wherein said semiconductor fin comprises two legs separated by a U-shaped void.

21. A method for manufacturing a fin-type transistor includes a gate resistance of the short-circuit device, comprising: a first plurality of trenches are formed parallel to each other in a substrate; formed parallel to one another in the longitudinal direction in the substrate and a second plurality of grooves perpendicular to the longitudinal direction of the first plurality of trenches' and are formed in the substrate parallel to the second plurality of grooves and relative to the second plurality of grooves said second plurality of grooves third offset is smaller than the distance of the plurality of trench grooves period; wherein said dielectric material is formed in at least a first plurality of substantially filling the trench before the third plurality of trenches and a second plurality of the two trenches.

22. The method of claim 21, wherein said third plurality of grooves forming comprises simultaneously forming a plurality of gate trenches, the plurality of insulating portions and a plurality of fins protruding rows.

23. The method according to claim 21, comprising: forming at least partially conductive region disposed at said plurality of gate trenches; and the recessed conductive area of said plurality of gate trenches in.

Description

translated from Chinese

Apparatus and manufacturing method comprising fin transistor gate resistance short

FIELD

Example [0001] The present invention relates generally to electronic devices, and more specifically, to fin transistors in certain embodiments.

Background technique

[0002] Fin field-effect transistors (the finFET) are often built around a substantially vertical fin rising from the substrate (e.g., a high and thin semiconductive member). Typically, the gate travels upwardly through the top of a climb side conformally along the other side of the fin and the fin along further downstream across the fin. in some examples, the gate electrode is disposed over and against the fin does not extend crossing the top side. Generally, a source and a drain electrode located on the opposite side of the gate near the ends of the fin. In operation, by selectively energizing the gate to control the current through the fin between the source and the drain.

[0003] Some f inFET includes a gate sidewall spacer formed by the process. in some versions of this procedure, by treatment with a conformal, conductive film covers the fin and then anisotropically etching the conductive film to form the gate. During the etching, is removed faster than from the vertical surface from the horizontal surface of the conductive material. Thus, the remaining portion of the conductive material against the vertical sidewalls of the fin, thereby forming a gate. The advantage of this process with respect to alignment and resolution constraints are often subjected to a relatively narrow gates can be formed by photolithographic patterning of the gate.

[0004] Although the process avoids some of the problems by forming a gate sidewall spacer process, but it can introduce other failure mechanisms. Angled sidewalls of the fin often not perpendicular, since the fin is less than fully by anisotropic etching. These angled sidewalls can sidewall spacer process window becomes narrower, and it is closed in some cases. The angle of the substrate so that adjacent fins are placed closer to each other, and when the conformal film is deposited in this narrower gap, the film covering the adjacent portion of the sidewall may be combined, thus formed in the gap a film having a larger vertical thickness. in the film the gap may become so thick that the sidewall spacer etch does not remove all of the conductive film between adjacent gates. The resulting conductive residue finFET may be formed so that the adjacent short circuit and reduces the yield of the joists.

BRIEF DESCRIPTION

[0005] FIG. I to 27 illustrate the manufacturing process of an embodiment of the present invention; and

[0006] FIGS 28-37 Illustrate another embodiment of a manufacturing process according to the embodiment of the present invention.

Detailed ways

[0007] Illustrated in FIG. I, illustrating the manufacturing process to provide substrate 102 begins. The substrate 102 can comprise a semiconductive material, e.g., monocrystalline or polycrystalline silicon, gallium arsenide, indium phosphide, or other materials with semiconductor properties. Alternatively or additionally, the substrate 102 may comprise a non-semiconductor body on which the electronic device may be configured, for example, plastic or ceramic work surface like body. The term "substrate" encompasses these structures in various stages of manufacture, and may comprise any material comprising semiconductive material, including unprocessed whole wafer, the entire wafer processing portion, the entire wafer is fully processed, the wafer is cut or a portion a portion of the cut wafer by the electronic device package.

[0008] In this embodiment, the substrate 102 includes an upper doped region 104 and the lower doped region 106. The upper doped region 104 and the lower doped region 106 may be differently doped. For example, the upper doped region 104 may include n + material and the lower doped region 106 may include a p- material. The depth of the upper doped region 104 on a significant portion of the substrate 102 may be substantially uniform, e.g. over a significant portion of the array area of the memory device. The upper doped region 104 and the lower doped region 106 may be doped by implantation or diffusion of the dopant material. Alternatively, or additionally, the doped region may be a 104 or 106 or both in the growth or deposition of all of the substrate 102 during or in part, for example from cut or growth during the epitaxial deposition of a semiconductive material during the semiconductive wafer cut ingot. As explained below, the upper doped region 104 may provide a source for forming a transistor and a drain electrode material and the lower doped region 106 may provide material used to form the channel of the transistor.

[0009] The deep isolation trenches 108 may be formed and the shallow trench 110 in the substrate 102, illustrated in FIG 2. These trenches 108 and 110 may extend substantially in the Y direction. One or more shallow trench 110 may be inserted between a plurality of deep isolation trenches 108. In some embodiments, the shallow trench 104 deeper than the upper doped region 110 separated from the source and drain to the subsequently formed. Further, how deep deep isolation transistor to isolate the subsequently formed trench 108 than the shallow trenches 110.

[0010] The deep isolation trenches 108 and shallow trenches 110 may define a number of size of the substrate 102. Shallow trench 110 has a width substantially equal to or less than F (the patterned deep trench isolation device resolution, e.g., photolithography resolution limits) of 112. Similarly, the deep isolation trenches 108 may be less than or substantially equal to the width of 114 F, and the deep isolation trenches 108 and shallow trenches Opening 110 is smaller than the spacing or width substantially equal to 116 F. in some embodiments, the widths 112, 114 and 116 of one or more or all of substantially equal to or less than 3 / 4F „ 1 / 2F or 1 / 4F. Grooves 108 and 110 to 118 cycles is repeated, the cycle is substantially equal to or less than 118 4F, 2F 1F or in some embodiments. Deep isolation trenches 108 and shallow trenches 110 may have a generally rectangular or trapezoidal cross-section, and in some embodiments, the cross section may span a distance in the Y direction (for example, spanning more than one, two , (from e.g., corresponding to the maximum size of the subsequently formed transistors) from the length of the five or more transistors) is substantially uniform.

[0011] The deep isolation trenches 108 and shallow trenches 110 may be various dielectric materials (such as (for example) a high density plasma (HDP) oxide, tetraethylorthosilicate (TEOS) or spin-on glass (SOG)) is partially or completely filled with an electrically isolated features. Further, the deep isolation trenches 108 or shallow trenches 110 may include various liner materials (e.g., (for example), silicon nitride) to release the film stress, or as improved adhesion barrier material. In some embodiments, prior to filling, in order to further isolate with the selected dopant is then implanted transistors are formed at the bottom 108 of the deep isolation trenches.

[0012] Next, a buffer 120, illustrated in FIG. 3. it may be (e.g.) in an oven by exposing the substrate 102 to oxygen for the growth of the oxide buffer 120. Alternatively, or additionally, may be (for example) is deposited in the buffer 120 a chemical vapor deposition (CVD) chamber. The buffer 120 is illustrated by an oxide growth, therefore, mainly through the upper doped region 104 disposed on the exposed portion. Buffer 120 may have a thickness of less than 300, for example, between 30 A and 150. In some embodiments, the buffer film 120 may be reduced during the subsequent risk of stress-induced defects formed in the upper doped region 104 or lower doped region 106.

[0013] may be formed conformally termination region 122, illustrated in FIG. 4 in the buffer 120. The termination region 122 may be a nitride layer, and it may have a thickness of less than 1000 A, for example, between 500 A 100 A. As explained below, in some embodiments, termination region 122 may be used in the process of etching or CMP stop penetration before the upper doped region 104 (e.g., which can etch or chemical mechanical planarization (CMP) process is slow). Further, in some embodiments, the transition to termination region 122 may indicate a suitable time to stop the process of one of the.

[0014] Next, the lower portion of the sacrificial region 124 may be formed in the termination region 122, illustrated in FIG. 5. In some embodiments, with between 200 and 5000 A (e.g., between 3,000 and 500A) of the lower portion of the blanket of the film thickness by sacrificial region 124 made of polysilicon. As explained below, the material from region 124 may be formed of a substantially vertical sidewall spacers formed thereon. [0015] As illustrated in FIG. 6, the upper portion of the sacrificial region 126 may be formed on the lower sacrificial region 124. In this embodiment, different from the lower portion 126 is made of a sacrificial material of the upper region of the sacrificial zone 124 to facilitate selective removal of the upper portion of the sacrificial region 126 during a subsequent step. The upper portion 126 may be made of various materials the sacrificial region, such as an oxide, and it may have (for example between 500 A and 1500 A) a thickness between 200 A and 3000 A in. Additionally, or alternatively, in some embodiments, it may be an amorphous carbon layer on the upper portion of the sacrificial masking region 126. in other embodiments, the upper region in the sacrificial masking region 126 may be omitted, this does not imply that any of the other features discussed herein in can not be omitted.

[0016] Next, the fin mask 128 is formed on the upper sacrificial area 126, illustrated in FIG. 7. Fin mask 128 may be patterned by a variety of lithography systems, such as photolithography systems, e-beam system or nanoimprinting system. In some embodiments, the fin is formed using a mask having a wavelength of 128 to 193nm

lithography light source system. Fin mask 128 comprises a shielding region having a width 130 and exposed regions having a width of 132. In some embodiments, the width 130 and 132 is substantially equal to one another and each substantially equal to 1F. Fin mask 128 may be substantially equal to 2F period 134 is repeated. The exposed area and the shielding area can be substantially parallel to one another and substantially perpendicular to both the deep isolation trenches 108 and shallow trenches 110. Further, in some embodiments, the exposed area and the shielding area in a significant distance in the X direction may have a substantially uniform cross-section, corresponding to, for example, five or more than five transistors distance . In some embodiments, the fin mask 128 is deposited and do not extend to the peripheral portion of the substrate 102 in the array portion of the substrate 102. As explained below, the fin mask 128 may define a generally fin subsequently formed, isolated location and spacing of the trench and the gate.

[0017] In certain embodiments, as compared to some conventional processes, the fin mask 128 having a relatively large alignment limits. Many conventional structure (e.g. deep isolation trenches 108 and shallow trenches 110) on the substrate 102 in the Y direction is substantially uniform. Thus, in some embodiments, the mask 128 may be slightly displaced in the Y-axis, or offset, this had no significant effect on the final shape of the transistor. Similarly, since the mask 128 is substantially uniform in the X direction, so the mask 128 in the X direction offset must be acceptable. I believe align limit increase will increase the yield and reduce costs.

[0018] Next, the precursor may be formed in the trench 136, illustrated in FIG. 8. By etching the substrate 102 is not the fin mask 128 of the area protected precursor to the trench 136 is formed. Thus, the shape of the groove 136 is generally the precursor may be the fin 128 is complementary to the shape of the mask. The etch may be an anisotropic plasma etch, and the sacrificial removably exposed upper region below a significant portion of the area 126 or all of the sacrificial region 124 and a lower portion. The etching may stop or termination region 122 in the vicinity. In some embodiments, changes in the chemical composition of the product gas during the etching of the etching time may indicate termination region 122 has been reached or timing the etch.

[0019] After the trench is formed in the precursor, the fin mask 128 may be removed, 9 illustrated in FIG. May be removed by various techniques fin mask 128, contained in a furnace or a plasma etch chamber in the fin mask 128 is exposed to oxygen.

[0020] Next, spacers 138 may be formed, 10 illustrated in FIG. The illustrated spacer 138 is deposited substantially conformally on the substrate 102 (e.g., when applying a material having a substantially uniform thickness in the horizontal and vertical structure) oxide. In some embodiments, the spacer 138 may be the same with the upper sacrificial material region 126, but different from the lower portion 124 of the sacrificial material region. The spacer 138 may have a thickness of greater than or substantially equal to 1 / 16FU / 8F or 1 / 4F 140. Spacer member 138 so that the trench width 142,136 precursor narrowed substantially less than or equal to 1F, a width of 3 / 4F or 1 / 2F of. As explained below, this narrow width of the fin 142 may generally define the width of the subsequently formed.

[0021] After forming spacers 138, the substrate 102 may be etched, 11 illustrated in FIG. The anisotropic etch may be a plasma etch substantially along the Z axis, resulting in the spacer 138 material is removed from horizontal surfaces. For example, the spacer 126 above the bottom of the trench precursor sacrificial region 136 and the upper portion 126 of the sacrificial region portion 138 of the two. This removed material may form a sidewall spacer, the sidewall spacer may further serve as a mask during the etching progress to form a trench 144 between the lines. Penetrate the etch stop region 122, a buffer 120, a lower portion of the upper doped region 104 and doped region 106. In some embodiments, the shallow trench 110 is etched deeper than the deep isolation trenches 108 but not as deep. The etching may be defined between a substantially straight and substantially parallel to the row trenches 144, the trenches 144 between the lines having a substantially uniform cross-section over a significant distance in the X direction, for example, a distance greater than five transistors. Between row trenches 144 may have a width 146 substantially equal to or less than 1F, 3 / 4F or 1 / 2F of. In some embodiments, trenches 144 between the lines may be between 1,000 and 10,000 A depth, for example between 2000 and 5000A. During the subsequent steps, inter-row trenches 144 may generally define a shape and a position disposed between adjacent rows of transistors of the dielectric.

[0022] Next, trenches 144 may be between the lines 146 formed in the outer liner 12 illustrated in FIG. The illustrated outer liner 146 may be an oxide grown on the exposed portions of the upper doped region 104 and the lower doped region 106. In other embodiments, the outer liner 146 may be deposited by methods known in the art. The liner may have a thickness of less than 150, for example, 20 to 7GA, and in some embodiments, it may protect the upper doped region 104 and the lower doped region 106 from stress-induced defects.

[0023] FIG 13 illustrates, the inner liner 148 may be formed on the substrate 102. Inner liner 148 may be a nitride layer 102 is deposited on the substrate. Inner liner 148 may have a thickness of less than 200 A, for example, between 30 A and 100 A. In some embodiments, the liner may be further formed on the inner liner 148, for example, a TEOS liner with a thickness between 300 A 100 A's.

[0024] Next, 14 illustrated may be formed between the dielectric lines 150 on the substrate 102 as shown in FIG. Dielectric between the lines 150 may be made of various dielectric materials or comprise various dielectric materials, such as spin-on dielectric (SOD). In some embodiments, by heating the substrate 102 to densified dielectric line between SOD 150 150 to electrically drive volatile compounds from the inter-line medium. During densification, the liner 146 or 148 in one or more of the film stress may lead to reduce from crystal plane or a slip dislocation in the substrate 102 or 150 between the dielectric lines shrinkage.

[0025] As illustrated in FIG. 15, a top portion of the substrate 102 may be removed after forming the dielectric 150 rows. In some embodiments, the sacrificial region 124 on the lower or stop the CMP process in which the removal of the top portion. It may indicate that the CMP process to reach the end through phenomenon during the transition to a lower portion of the sacrificial region 124. Examples of this phenomenon comprises changing optical characteristics (e.g., color or reflectance) of the substrate 102, the mechanical properties (e.g., compounds in waste slurry) to change the chemical properties of the waste or substrate 102 (e.g., sliding friction) changes. Alternatively, or additionally, by the sacrificial region 124 on the lower or top part of the substrate 102 is removed in the stop-etch.

[0026] This step of removing the exposed sacrificial for the lower region 124, sidewall spacers may be formed so that, as explained in its position. In some embodiments, be generally removed by wet etching selective to the material of the lower portion of the lower portion of the sacrificial region 124 of the sacrificial region 124, for example, usually selected wet etching polysilicon, for example, tetramethylammonium hydroxide (TMAH) etch . A lower region 124 by removing the sacrificial left interval 152 may have a width generally corresponding to the width 132 (FIG. 7) of the fin by the mask area 128 (e.g., substantially equal to or proportional to) a. Vertical spacer member 138, and a sidewall spacer to locate the gate and the fin shaped surfaces formed thereon may be provided on the exposed.

[0027] Next, 154 may be formed, Figure 17 illustrates another spacer member 102 on the substrate. This spacer member 154 may be different from earlier spacer 138, inner liner 148, made between the lines 150 and dielectric material 122 termination region. In some embodiments, the second spacer 154 made of the same material as the lower sacrificial 124, such as polysilicon. The spacer 154 may be deposited on the substrate iO2 between 100 and 1000 A (e.g., between 200 and 600 A) is generally conformal film thickness of I56. In some embodiments, thickness 156 may be greater than, less than or substantially equal to 1 / 8F or 1 / 4F, and the spacer member 154 may define a gap 158 having a width substantially equal to or less than 1 / 4FU / 2F or iF 160 . As explained below, the thickness 156 may generally define the width of the subsequently formed gate electrode and the width of fin 160 may generally define the width of the subsequently formed.

[0028] As illustrated in FIG. 18, a second spacer member may be an anisotropic etch to form sidewall spacers 154. The etching may be performed in a plasma etch chamber, and typically a significant portion of the removable spacer member 154 from the horizontal surfaces while leaving all or a significant portion disposed on the spacer 154 in the vertical surface. The termination region may be etched 122, the buffer 120 or the upper doped region 104 or stops therein.

[0029] After the etching of the spacer 154, another sacrificial region 162 may be formed on the substrate 102, illustrated in FIG. 19. I62 illustrated sacrificial region may be deposited between 100 and 1000 A (e.g., between 200 A and 600 A) of oxide thickness. Sacrificial region 162 may be partially, substantially or completely fill the void

158. In some embodiments, the sacrificial material area 162 may be different from the second spacer 154 to facilitate selective removal of the spacers 154 formed by the second spacer.

[0030] Next, the removable top portion 102 of the substrate 20 as illustrated in FIG. The top portion may be removed by a variety of processes including the etching or CMP. In some embodiments, the polishing of the substrate 102 until the exposed top portion of the second sidewall spacers from the spacers 154 is formed.

[0031] As illustrated in Figure 21, the second spacer 154 is removed from the substrate 102. The second spacer 154 may be removed by etching, wet etching, for example, usually have the choice of material of the second spacer 154. For example, in embodiments where the second spacer 154 made of polysilicon in the embodiment, may be removed by a second spacer 154 TMAH wet etching.

[0032] Next, etching may remove material by removing the exposed portion 154 of the second spacer member 102 from the substrate 22 as illustrated in FIG. Etching the gate trench 164 may be formed, the fin rows 166 and the insulating portion 168 protrudes. Between each of the gate trenches 164 may be disposed in each row of fins 166 projecting each of the insulating portions 168. Substrate 102 for each row of fins 166 and 168 of each insulating protrusion 164 may comprise two gate trenches. The gate trench 164 illustrated disposed between the fin rows 166 and the insulating portion 168 protrudes. In the illustrated embodiment, the etching is not interlaced between the dielectric material 150 is removed, and the insulating portion protruding lines that is sandwiched between two portions of the upper doped region 104 and the lower doped region 106 The dielectric 150. In other embodiments, although the etch consumable upper doped region 104 and these portions of the lower doped region 106, the dielectric material from the inter-row portion 150 may define the gate trench 164.

Between [0033] may be etched into the substrate by 102 500 A and 4000 A (e.g., between 2500 to 1300 A)

Substantially anisotropic etching characteristics 164, 166 and 168 are formed. The gate trench 164, the fin rows 166 and the insulating protrusion 168 may be substantially straight in the X direction and across a significant distance having a substantially uniform cross-sectional shape, for example, spanning a distance greater than five transistors. Structure 164, 166 and 168 may be substantially parallel to each other and substantially perpendicular to the shallow trench 110 and the deep isolation trenches 108. The gate trench 164, the fin rows 166 and the insulating protrusion 168 may have a width 170, 172 and 174, respectively, the width is substantially equal to or less than 1 / 4F, 1 / 2F or 1F. In some embodiments, the gate trench 164, the fin rows 166 and the insulating projection pattern 168 may be substantially equal to or less than 3F, 2F, or 3 / 2F is repeated 176 cycles.

[0034] Next, the substrate 102 is planarized by CMP, 23 illustrated in FIG. In some embodiments, the CMP can be removed and the remaining portion of the sacrificial region 162 of the liner 138, and in some embodiments, it may also be removed between the lines of the dielectric 150, a top portion of the inner liner 146 and termination region 122. The planarization may stop on the termination region 122 or in the vicinity thereof. In some embodiments, after planarization, the substrate 102 may be cleaned to remove CMP slurry residue. Cleaning the substrate 102, some of the hydrofluoric acid by preferentially etching the crystal upper doped region 104 and the lower doped region 106 in the case of some embodiments, the substrate 102 may not be exposed to the hydrofluoric acid orienting can form pits. [0035] 24 illustrated in FIG., The gate dielectric 178 may be formed in the gate trench 164. In some embodiments, by chemical vapor deposition (CVD) or atomic layer deposition (ALD) deposited gate dielectric 178, or may be (for example) the substrate 102 is exposed to oxygen gate dielectric 178 is grown. A gate electrode 178 may be made of various dielectric materials medium, such as an oxide (e.g., silicon oxide, Ni), oxynitride or a high dielectric constant material, such as Ni oxide, hafnium oxide, zirconium oxide and ni ni titanium. In some embodiments, the gate dielectric 178 may have a thickness of less than 300, for example, between 30 and 150 people.

[0036] Next, a gate material 180 may be formed on the substrate 102, illustrated in FIG. 25. The gate material may be a variety of electrically conductive material of one or more of, for example, doped polysilicon, tungsten, titanium, titanium nitride, or other suitable material, and which may be formed by various processes, such as physical vapor deposition (PVD) or CVD.

[0037] After the formation of gate material 180, the gate material may be removed from the top portion 180 of the substrate 102, illustrated in FIG. 26. The gate material 180 may be removed by various processes, for example, the CMP, plasma etching, wet etching, or groups thereof, combined. In some embodiments, the gate material 180 is substantially concave or less 1000 A (e.g., between 200 and 500 A) from 182. From the top of the gate material 182 may allow the upper doped region 180 is higher than the bottom portion 104, i.e., the gate material 180 and the upper doped region 104 may be at least partially overlap. In one embodiment, the gate material 180 to the gates 184 and 186 recessed gate trench 164 is formed. Gates 184 and 186 may be disposed on opposite sides of the fin rows 166 and 186 and the gate 184 may be described by an electrically insulating projecting portion 168 and the spacer adjacent to the gate 184 or 186 illustrated.

Small gate 184 [0038] The illustrated and gate 186 than some conventional designs the possibility of a short circuit to one another. In one embodiment, the insulating projecting portion 168 defining a portion (e.g. about half) of the gate trench 164, thereby forming at least — along directions (e.g., the direction of the closest adjacent fin rows 166) of the insulating trench 164. Thus, by making the recessed gate material 180 to the gate trench 164 is formed in the pre-isolation gates 184 and 186 illustrated. I believe this embodiment is less likely to short-circuit the gate 184 and gate 186 cases than the conventional design, the conventional design often include a gate shape of the gate after defining a substantially isolated. In other words, in some conventional designs —, at least in part determines the shape of the gate between the gate dielectric, while the embodiments described in the embodiment illustrated, between the gate insulating structure (i.e., the insulating projecting portion 168) determining a shape at least partially the shape of the gate 184 and 186. It is believed that this will increase the utility of the insulating protrusion 168, projecting portions 168 because the insulating barrier between the gate 184 and paths 186 and 186 before the gate electrode 184 is formed in some embodiments.

[0039] The illustrated fin rows 166 illustrated may each — 184 and 186 adjacent to the gate and cooperate to form a plurality of transistors 188. FIG 27 illustrates a shape of the portion of the transistor 188, illustrating the shape of a semi-conductive portion 188 of the individual transistors. The illustrated transistor 188 includes a rising from the base 192 of the fin 190. The illustrated fin 190 includes end portion having two legs by a substantially U-shaped separation gap 198 and 194 196. In this embodiment, a void 198 is formed by a shallow trench 110 and the void 198 extends below the depth of the upper doped region 104. Both legs 194 and 196 illustrated includes an upper doped region 104 and the lower doped region 106 of the top portion illustrated. The illustrated fin 190 further comprises two opposing sides 200 and 202, the opposite side may be substantially parallel to one another, an angle with respect to each other substantially, or substantially curved with respect to each other. Fin 188 and edge 204 206 and 200 may be substantially perpendicular to side 202 and substantially parallel to each other substantially with respect to one another or relative to an angle to each other substantially curved.

[0040] In operation, the two legs 194 and 196 act as source and drain, and the transistor 188 (FIG. 26) of the voltage source in accordance with selectively controlling the gate electrode 184 and the electrode 186 current flow between the drain. When turned on, the illustrated transistor 188 illustrated substantially vertical passage established by arrow 208 represented by arrow 208 illustrates the flow of current between the source and drain described. Channel 208 can be established by the electric field originating from the two gates 184 and 186. Gates 184 and 186 to be energized in accordance with various modes: generally simultaneously to both the gates 184 and 186 energized; can give — 186 and gate 184 is energized, but not to another current passage —; independently of one another or gates 184 and 186 to energize. in some embodiments, the gates 184 and 186 may partially or completely surround the fin rows 166, 184 and 186 may, for example, a gate connected to one end of the fin rows 166 — or both ends. The illustrated transistors 188 may be referred to as a double gate transistors or multi-gate transistors, because each of side walls 200 and 202 — gates 184 and 186 have adjacent.

[0041] Example embodiments previously described to form a structure extending in the X direction with reference to a single photolithography step described in FIG. 7, g Jie, the fin rows 166, 184 and 186 and the gate insulating projecting portion 168. Other embodiments may, but fewer overall steps 166, 184 and 186 of these structures

are formed by two or more photolithography steps. FIGS. 28-37 illustrates an example of this manufacturing process. As explained below, the embodiment above this embodiment compared to the embodiment comprises fewer process steps, but contains --- additional photolithography step.

[0042] As illustrated in FIG. 28, this embodiment is to provide the substrate 210 begins. The substrate 210 may be initially subjected to I above with reference to FIG. 2 and the process described. Thus, the substrate 210 may include an upper doped region 104, the lower doped region 106, the deep isolation trenches 108 and shallow trenches 110. On top of these features, a first fin mask 212 may be formed. A first fin mask 212 may be made of photoresist, hard mask, or may be touched. A first fin mask 212 may be patterned by a photolithography system described hereinabove lithography techniques or any one of, for example, resist reflow, or mask undercut enlargement of the spacing member via fold sidewall spacers. In some embodiments, the first fin mask 212 has a width substantially defining the exposed regions having a width 214 and a shielding region 216. In certain embodiments, the widths 214 and 216 are substantially equal and Farm --- less than or substantially equal to 1F. A first fin mask 212 may be substantially equal to or less than the cycle was repeated 218 2F. The illustrated shielding region and the exposed region is substantially straight and substantially parallel to the adjacent mask structure and substantially perpendicular to both the deep isolation trenches 108 and shallow trenches 110. A first fin mask 212 and exposed regions may span shielding region in the X direction --- significantly from having a substantially uniform cross-section, for example a distance greater than five transistors.

[0043] Next, etching the row trenches 220, as illustrated in FIG. 29. Etching the trenches may be 220 rows by substantially anisotropic plasma etching, and which may extend into the substrate 210 is greater than the depth of the shallow trench 108 but not as deep isolation trenches 110 from deep. In other embodiments, the inter-row trenches 220 may be substantially as deep as the deep isolation trenches 110 or deeper than the deep isolation trenches 110. By field isolation implant (not shown) between the bottom line of the groove 220 is implanted to isolate the subsequently formed transistor.

[0044] As illustrated in Figure 30, in row after etching the trench 220, a first fin mask 212 may be removed, and the inter-line dielectric 222 may be formed in the channel 220 between the lines. In some embodiments, by CVD, ALD, spin-on dielectric or other suitable processes and dielectric materials between the lines 222. The dielectric between the lines 222 may be an oxide, for example, according to one of the above oxides and, in some embodiments --- embodiment, which may include an upper doped region adjacent to the lower doped region 104 and a thin oxide liner 106 and the line between the oxide liner and nitride liner both the dielectric between the remaining portion 222. In some embodiments, the dielectric between the lines 222 and a cover layer deposited, the covering layer is removed by CMP or etching to a generally planar surface of the substrate 210.

[0045] Next, illustrated in FIG. 31, the second fin mask 224 may be formed. The second fin mask 224 relative to the first fin mask 212 offset distance 225, the fin mask 212 is substantially equal to the first half cycle 218 a distance 225. For example, a midpoint, a midpoint of the first fin mask 224 may shield region 212 and second fin mask shielding region 225 of the separation distance. Furthermore, the midpoint of the second fin mask masking regions 224 may generally fall on the edge of the first fin mask 212 of shielding region or the vicinity thereof, such as the second fin mask 224 with respect to the channel 220 between the lines between the edge 222 of the dielectric-line position illustrated. The second fin mask 224 may generally define a width 226 and exposed regions having a width 228 of the shielding region. These features may be repeated 230 cycles. In some embodiments, period 230 is substantially equal to the first fin mask 212 218 cycles. The width of the shielding region 228 may be substantially equal to or less than 1F, 1 / 2F or 1 / 4F. In certain embodiments, the width of the second fin mask masking region 224 is part of the width of the first fin mask 212 of shielding region 216, for example, substantially equal to or less 1/4 or 1/2 of the width 216 . The second fin mask 224 and exposed regions of the shield may be substantially straight region substantially parallel to the adjacent mask structure, substantially parallel to the line between the dielectric 222, and substantially perpendicular to the deep isolation trenches 108 and shallow trenches both 110. --- significant distance across the second fin mask 224 may be the X direction has a substantially uniform cross section, e.g. a distance greater than five transistors.

[0046] The second fin mask 224 may be formed by various techniques. For example, in some embodiments, the second fin mask 224 made of photoresist is patterned by a photolithography system. In other embodiments, it is formed by passing the second fin mask 224 defining a mask by photolithography times enlargement of the pitch. For example, a mask may be patterned by masking areas with precursor disposed between the illustrated substantially every second fin mask --- shielding region 224 and second fin mask 224 is then formed into the sidewall spacers on the side of the mask precursor to the second fin mask 224 is formed.

[0047] Next, the sidewall spacer 32 illustrated member 232, as shown on the side of the second fin mask 224. May be formed in the sidewall 210 of the substrate and then depositing a blanket coating film is formed by anisotropically etching the spacer 232. In some embodiments, sidewall spacers 232 may be made of carbon, and which may have a width 234 substantially equal to or less than 1F, 1 / 2F or 1 / 4F of. Sidewall spacers 232 may define a gap having a width of 236, a width 236 substantially equal to or less than 1F, 1 / 2F or 1 / 4F.

[0048] Next, a second fin mask 224 may be removed and may be 238, as illustrated in FIG. 33 In etching the gate trench 210 of the substrate. Gate trenches 238 may be formed by generally anisotropically etched sidewall spacer member 232 by a shielded. In some embodiments, the gate trench 238 deeper than the shallow trenches 110, but not as good as the dielectric 222 or the inter-row deep isolation trenches 108 deep. Gate trenches 238 may be between 500 and 3,000 deep, for example; between 1300 A and 1700. The gate trench 238 may be substantially parallel, substantially straight and substantially perpendicular to both the deep isolation trenches 108 and shallow trenches 110. Embodiment, the gate trench 238 in the X direction across --- significantly from having a substantially uniform cross-section, for example a distance greater than five transistors in this embodiment.

[0049] In some embodiments, the gate trench 238 may be formed substantially simultaneously projecting fin rows 240 and the insulating portion 242 is formed. Insulating the illustrated projection 242 is inserted between the fins of each row are --- 240 illustrated in the description, and in some embodiments, each row 240 --- fin adjacent to the gate trench 238 and on either side ---separating the insulating portion 242 protrudes. Cheung a previous embodiment, since the position and shape of the gate trench 238 illustrated explained at least in part to form the insulating material 242 by removing the protruding portions to define, therefore believed gate is formed in the gate trench 238 less likely to short-circuit one another.

[0050] Next, gate dielectric 244 may be formed, illustrated in FIG. 34 in the gate trench 238. May be deposited or grown a gate dielectric 244 and which may be made of various dielectric materials, e.g., oxides (e.g., silicon oxide, Ni), oxynitride or a high dielectric constant material, such as Ni oxide, hafnium oxide, zirconium oxide, and ni ni dioxide. In some embodiments, the gate dielectric 244 has a thickness of less than 300A (e.g., between 30 A and 150 A) of.

[0051] After the formation of gate dielectric medium 244, gate material 246 may be formed on the substrate 210, illustrated in FIG. 35. The gate material 246 may be a conductive material by CVD, PVD or other suitable deposition process. In some embodiments, the gate material 246 comprises a conductive material of the above listed one. The gate material 246 may have a cover layer 248 is deposited to increase the likelihood of all of the gate trench 238 is filled and planarized substrate 210. The gate material 246 may be formed on the substrate 210 before or after removal of the spacer 232.

[0052] Next, the removable cover layer 248 and the gate material 246 to form recessed gates 250 and 252, illustrated in FIG. 36. Gates 250 and 252 may be recessed a distance 254, the distance 254 is selected to reduce the likelihood of residual gate insulating gate material 238 projecting on opposite sides of the connection portions 242 and 250 252. And the gate 250 may be concave 252 by the CMP, dry etching, wet etching, or a combination thereof. In some embodiments, the gates 250 and 252 overlap the upper doped region 104 and through the recess is not less than the upper doped region 104 of the bottom.

[0053] At this stage, the substrate 210 may comprise a plurality of transistors 256. Figure 37 illustrates a portion 256 of the shape of the semiconductor transistors. The illustrated transistor 256 each comprise 260 rising from the base of the fin 258. Side fins 261 and 258 may comprise 262, 264 and the edge 266, the legs 268 and 270

and a generally U-shaped void 272. Channel 274 may be established in any — fin 260 and the side 258 of the previous embodiment 262 a Cheung, illustrated legs 268 and 270 used as the source and drain electrode Xi explained, and an electric field from the gate 252 and 254 .

[0054] While the invention is susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and described in detail herein. However, it should be understood that the present invention is not intended to be limited to the particular forms shown kei. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as claimed in the appended claims, as defined in the above.

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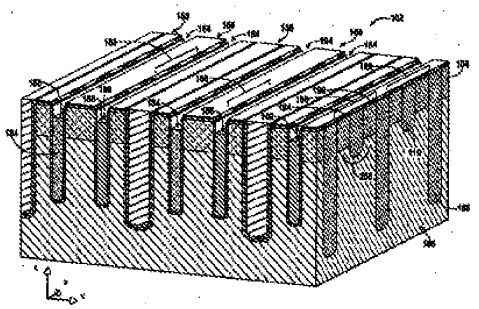
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(54)发明名称

包含耐栅极短路的鳍式晶体管的装置及其制作方法

(57)摘要

本发明揭示方法、系统及装置，其包含一种包含以下动作的方法：在衬底(102、210)中蚀刻行间沟槽(144、220)；用电介质材料(150、222)大致或完全地填充所述行间沟槽(144、220)；及至少部分地通过在所述衬底(102、210)中蚀刻栅极沟槽(164、238)来形成鳍(190、258)及绝缘突出部(168、242)。在一些实施例中，所述绝缘突出部(168、242)包含所述行间沟槽(144、220)中的所述电介质材料(150、222)中的至少一些电介质材料。



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1. 一种方法，其包括：

在衬底中蚀刻行间沟槽；

用电介质材料大致或完全地填充所述行间沟槽；及

至少部分地通过在所述衬底中蚀刻栅极沟槽来形成鳍及绝缘突出部，其中所述绝缘突出部包含所述行间沟槽中的所述电介质材料中的至少一些电介质材料。

2. 根据权利要求 1 所述的方法，其中蚀刻所述行间沟槽包括：

在所述衬底上的牺牲区中形成若干前驱物沟槽；及

在所述前驱物沟槽中形成间隔件，其中所述间隔件使所述前驱物沟槽变窄。

3. 根据权利要求 2 所述的方法，其中所述间隔件使所述沟槽变窄到小于光刻分辨率限制的宽度。

4. 根据权利要求 2 所述的方法，其包括使用所述牺牲区及侧壁间隔件作为掩模来蚀刻所述行间沟槽。

5. 根据权利要求 1 所述的方法，其中在衬底中蚀刻行间沟槽包括蚀刻行间沟槽穿过上部掺杂区且至少部分地进入到下部掺杂区中。

6. 根据权利要求 1 所述的方法，其中用电介质材料大致或完全地填充所述行间沟槽包括：

在所述行间沟槽中形成第一衬里；及

将旋涂电介质施加到所述衬底。

7. 根据权利要求 1 所述的方法，其包括：

用牺牲材料及第一侧壁间隔件遮蔽所述行间沟槽的所述蚀刻；及

在用所述电介质材料大致或完全地填充所述行间沟槽之后移除所述牺牲材料。

8. 根据权利要求 7 所述的方法，其包括：

在移除所述牺牲材料之后在所述第一侧壁间隔件的表面上形成第二侧壁间隔件；及

至少部分地用所述第二侧壁间隔件遮蔽所述栅极沟槽的所述蚀刻。

9. 根据权利要求 1 所述的方法，其中至少部分地通过在所述衬底中蚀刻栅极沟槽形成鳍及绝缘突出部包括蚀刻所述电介质材料的一部分。

10. 根据权利要求 1 所述的方法，其中至少部分地通过在所述衬底中蚀刻栅极沟槽形成鳍及绝缘突出部包括通过蚀刻多个栅极沟槽而大体上同时地形成多个鳍行及多个绝缘突出部。

11. 根据权利要求 10 所述的方法，其中：

将所述多个绝缘突出部中的每一绝缘突出部插入在所述多个鳍行中的一对鳍行之间；且

将所述多个栅极沟槽中的栅极沟槽安置于所述多个鳍行中的每一鳍行的任一侧上所述鳍行与所述多个绝缘突出部中的邻近绝缘突出部之间。

12. 根据权利要求 1 所述的方法，其中：

在所述衬底中蚀刻行间沟槽包括通过光刻步骤在所述衬底上形成第一掩模，且

至少部分地通过在所述衬底中蚀刻栅极沟槽形成鳍及绝缘突出部包括通过第二光刻步骤在所述衬底上形成第二掩模。

13. 根据权利要求 12 所述的方法，其中使所述第二掩模相对于所述第一掩模移位大体

上等于所述第一掩模的间距的一半的距离。

14. 根据权利要求 13 所述的方法，其中：

形成所述第一掩模包括借助第一光刻工具形成所述第一掩模；

形成所述第二掩模包括借助第二光刻工具形成所述第二掩模，其中所述第二光刻工具的分辨率大体上与所述第一光刻工具的分辨率的两倍一样大或大于所述第一光刻工具的分辨率的两倍。

15. 根据权利要求 13 所述的方法，其中形成所述第二掩模包括使前驱物掩模间距倍增。

16. 一种装置，其包括：

半导体鳍；

栅极沟槽，其安置于所述半导体鳍的任一侧上；及

绝缘突出部，其安置于所述半导体鳍的任一侧上且通过所述栅极沟槽中的一者至少部分地与所述半导体鳍分离。

17. 根据权利要求 16 所述的装置，其进一步包括：

栅极，其安置于每一栅极沟槽中，其中每一栅极经凹入而低于所述半导体鳍的顶部。

18. 根据权利要求 16 所述的装置，其中所述半导体鳍包括通过大体上 U 形空隙分离的两个支腿。

19. 一种方法，其包括：

在衬底中形成彼此大体上平行的第一多个沟槽；

在所述衬底中形成彼此大体上平行且大体上垂直于所述第一多个沟槽的第二多个沟槽；及

在所述衬底中形成大体上平行于所述第二多个沟槽且相对于所述第二多个沟槽错位小于所述第二多个沟槽的周期的距离的第三多个沟槽。

20. 根据权利要求 19 所述的方法，其包括在形成所述第三多个沟槽之前用电介质材料至少大致填充所述第一多个沟槽及所述第二多个沟槽两者。

21. 根据权利要求 19 所述的方法，其中形成所述第三多个沟槽包括大体上同时形成多个栅极沟槽、多个绝缘突出部及多个鳍行。

22. 根据权利要求 21 所述的方法，其包括：

形成至少部分地安置于所述多个栅极沟槽中的导电区；及

使所述导电区凹入到所述多个栅极沟槽中。

包含耐栅极短路的鳍式晶体管的装置及其制作方法

技术领域

[0001] 本发明的实施例一般来说涉及电子装置，且更具体来说，在某些实施例中涉及鳍式晶体管。

背景技术

[0002] 鳍式场效晶体管（finFET）经常围绕从衬底大体上垂直上升的鳍（例如，高且薄的半导电部件）构建。通常，栅极通过沿鳍的一个侧保形地向上行进翻越顶部并沿鳍的另一侧向下行进而跨越所述鳍。在一些实例中，所述栅极经安置倚靠所述鳍的侧且并不延伸翻越顶部。一般来说，源极及漏极位于栅极的对置侧上，靠近鳍的两端。在操作中，通过选择性地给栅极通电来控制穿过源极与漏极之间的鳍的电流。

[0003] 一些 finFET 包含通过侧壁间隔件过程形成的栅极。在此过程的一些版本中，通过用保形、导电膜覆盖鳍且然后各向异性蚀刻所述导电膜来形成栅极。在所述蚀刻期间，比从垂直表面快地从水平表面移除所述导电材料。因此，所述导电材料的一部分残留倚靠鳍的垂直侧壁，由此形成栅极。此过程的优点为相对于经常经受对准及分辨率约束的通过光刻图案化的栅极可形成相对窄的栅极。

[0004] 尽管通过侧壁间隔件过程形成栅极避免了一些过程问题，但其可引入其它失效机制。鳍的侧壁经常成角度而非垂直，因为所述鳍通过小于完全各向异性的蚀刻而形成。这些成角度的侧壁可使侧壁间隔件的过程窗口变窄，且在一些情况下使其闭合。所述角度使邻近鳍的基底彼此更靠近地放置，且当保形膜沉积于此较窄间隙中时，所述膜的覆盖所述邻近侧壁的部分可联合，因此在所述间隙中形成具有较大垂直厚度的膜。在所述间隙中所述膜可变得如此厚以至于侧壁间隔件蚀刻不会移除邻近栅极之间的所有导电膜。所得导电残余物可形成使邻近 finFET 短路且降低合格率的衍条。

附图说明

[0005] 图 1 到 27 图解说明根据本发明的实施例的制造过程；及

[0006] 图 28 到 37 图解说明根据本发明的实施例的另一制造过程。

具体实施方式

[0007] 如图 1 所图解说明，制造过程以提供衬底 102 开始。衬底 102 可包含半导电材料，例如，单晶或多晶硅、砷化镓、磷化铟或具有半导体特性的其它材料。另一选择为或另外，衬底 102 可包含电子装置可构造于其上的非半导体本体，例如，塑胶或陶瓷工作表面等本体。术语“衬底”囊括处于各个制造阶段的这些结构，且可包含任何包括半导电材料的材料，包含未处理的整个晶片、部分处理的整个晶片、完全处理的整个晶片、经切割晶片的一部分或经封装电子装置中的经切割晶片的一部分。

[0008] 在此实施例中，衬底 102 包含上部掺杂区 104 及下部掺杂区 106。上部掺杂区 104 及下部掺杂区 106 可经不同掺杂。举例来说，上部掺杂区 104 可包含 n+ 材料且下部掺杂区

106 可包含 p- 材料。上部掺杂区 104 的深度在衬底 102 的一显著部分上可大体上均匀，例如遍及存储器装置的阵列区域的一显著部分。上部掺杂区 104 及下部掺杂区 106 可通过植入或扩散掺杂剂材料来掺杂。另一选择为，或另外，可在生长或沉积衬底 102 的全部或部分期间掺杂这些区 104 或 106 中的一者或两者，例如在外延沉积半导电材料期间或在生长从其割切晶片的半导电晶锭期间。如下文所阐释，上部掺杂区 104 可提供用于形成晶体管的源极及漏极的材料且下部掺杂区 106 可提供用于形成所述晶体管的通道的材料。

[0009] 可在衬底 102 中形成深隔离沟槽 108 及浅沟槽 110，如图 2 所图解说明。这些沟槽 108 及 110 大体上可沿 Y 方向延伸。一个或一个以上浅沟槽 110 可插入于若干对深隔离沟槽 108 之间。在一些实施例中，浅沟槽 110 可比上部掺杂区 104 深以分离随后形成的源极及漏极。另外，深隔离沟槽 108 可比浅沟槽 110 深得多以隔离随后形成的晶体管。

[0010] 深隔离沟槽 108 及浅沟槽 110 可界定衬底 102 的若干尺寸。浅沟槽 110 具有小于或大体上等于 F（图案化所述深隔离沟槽的设备的分辨率，例如，光刻分辨率限制）的宽度 112。类似地，深隔离沟槽 108 可具有小于或大体上等于 F 的宽度 114，且深隔离沟槽 108 可与浅沟槽 110 间隔开小于或大体上等于 F 的宽度 116。在一些实施例中，这些宽度 112、114 及 116 中的一者或一者以上或全部小于或大体上等于 3/4F、1/2F 或 1/4F。沟槽 108 及 110 以周期 118 重复，周期 118 在一些实施例中小于或大体上等于 4F、2F 或 1F。深隔离沟槽 108 及浅沟槽 110 可具有大体上矩形或梯形横截面，且在一些实施例中，其横截面可跨越沿 Y 方向的某一距离（举例来说，跨越大于一个、两个、五个或多个晶体管长度的距离（例如，对应于随后形成晶体管的最大尺寸的距离））大体上均匀。

[0011] 深隔离沟槽 108 及浅沟槽 110 可用各种电介质材料（例如（举例来说）高密度等离子体 (HDP) 氧化物、原硅酸四乙酯 (TEOS) 或旋涂玻璃 (SOG)）部分地或完全地进行填充以电隔离特征。另外，深隔离沟槽 108 或浅沟槽 110 可包含各种衬里材料（例如（举例来说）氮化硅）以释放膜应力、改善粘附力或用作阻挡材料。在一些实施例中，在填充之前，用选定以进一步隔离随后形成的晶体管的掺杂剂植入深隔离沟槽 108 的底部。

[0012] 接下来，形成缓冲区 120，如图 3 所图解说明。可（例如）在炉中通过将衬底 102 暴露于氧进行氧化物生长缓冲区 120。另一选择为，或另外，可（例如）在化学气相沉积 (CVD) 室中沉积缓冲区 120。所图解说明的缓冲区 120 为经生长氧化物，因此，其主要安置于上部掺杂区 104 的经暴露部分上。缓冲区 120 可具有小于**300 Å**的厚度，例如在**30 Å**与**150 Å**之间。在一些实施例中，缓冲区 120 可减少随后的膜及过程在上部掺杂区 104 或下部掺杂区 106 中形成应力诱发的缺陷的可能性。

[0013] 可在缓冲区 120 上保形地形成终止区 122，如图 4 所图解说明。终止区 122 可为氮化物层，且其可具有小于**1000 Å**的厚度，例如在**100 Å**与**500 Å**之间。如下文所阐释，在一些实施例中，终止区 122 在过程穿透上部掺杂区 104 之前可用作蚀刻或 CMP 终止（例如，其可使蚀刻或化学机械平面化 (CMP) 过程缓慢）。另外，在一些实施例中，过渡到终止区 122 可预示停止这些过程中的一者的适当时间。

[0014] 接下来，可在终止区 122 上形成下部牺牲区 124，如图 5 所图解说明。在一些实施例中，下部牺牲区 124 为由多晶硅制成的具有在**200 Å**与**5000 Å**之间（例如，在**500 Å**与**3,000 Å**之间）的厚度的毯覆膜。如下文所阐释，来自此区 124 的材料可形成侧壁间隔件形成于其上的大体上垂直面。

[0015] 如图 6 所图解说明，可在下部牺牲区 124 上形成上部牺牲区 126。在此实施例中，上部牺牲区 126 由不同于下部牺牲区 124 的材料制成以方便在随后步骤期间选择性地移除上部牺牲区 126。上部牺牲区 126 可由各种材料制成，例如氧化物，且其可具有在**200 Å**与**3000 Å**之间（例如，在**500 Å**与**1500 Å**之间）的厚度。另外，或另一选择为，在一些实施例中，可在上部牺牲区 126 上形成无定形碳遮蔽层。在其它实施例中，在遮蔽区中的上部牺牲区 126 可省略，此并非暗示本文中所论述的其它特征中的任一者也不可省略。

[0016] 接下来，在上部牺牲区 126 上形成鳍掩模 128，如图 7 所图解说明。鳍掩模 128 可通过各种光刻系统来图案化，例如光刻系统、电子束系统或纳米压印系统。在一些实施例中，使用具有其波长为 193nm 的光源的光刻系统形成鳍掩模 128。鳍掩模 128 包含具有宽度 130 的暴露区及具有宽度 132 的遮蔽区。在一些实施例中，宽度 130 及 132 彼此大体上相等且每一者大体上等于 1F。鳍掩模 128 可以大体上等于 2F 的周期 134 重复。暴露区及遮蔽区可彼此大体上并行且大体上垂直于深隔离沟槽 108 及浅沟槽 110 两者。另外，在一些实施例中，所述暴露区及所述遮蔽区在沿 X 方向的一显著距离上可具有大体上均匀的横截面，例如在对应于五个或多于五个晶体管的距离上。在一些实施例中，将鳍掩模 128 沉积在衬底 102 的阵列部分中且不延伸到衬底 102 的外围部分中。如下文所阐释，鳍掩模 128 大体上可界定随后形成的鳍、隔离沟槽及栅极的位置及间隔。

[0017] 在某些实施例中，与一些常规过程相比，鳍掩模 128 具有相对大的对准限度。衬底 102 上的许多现有结构（例如深隔离沟槽 108 及浅沟槽 110）沿 Y 方向大体上均匀。因此，在一些实施例中，掩模 128 可沿 Y 轴稍微移位，或错位，此对晶体管的最终形状没有显著影响。类似地，由于掩模 128 沿 X 方向大体上均匀，因此掩模 128 的沿 X 方向的一定错位是可接受的。相信增加对准限度将增加合格率且降低成本。

[0018] 接下来，可形成前驱物沟槽 136，如图 8 所图解说明。通过蚀刻衬底 102 的未被鳍掩模 128 保护的区来形成前驱物沟槽 136。因此，前驱物沟槽 136 的形状通常可与鳍掩模 128 的形状互补。所述蚀刻可为各向异性等离子体蚀刻，且其可移除暴露区下方的上部牺牲区 126 及下部牺牲区 124 的一显著部分或全部。所述蚀刻可在终止区 122 上或其附近停止。在一些实施例中，蚀刻期间产物气体的化学组成的变化可预示蚀刻已到达终止区 122 的时间或可对所述蚀刻定时。

[0019] 在形成于前驱物沟槽中之后，可移除鳍掩模 128，如图 9 所图解说明。可通过各种技术来移除鳍掩模 128，包含在炉中或等离子体蚀刻室中将鳍掩模 128 暴露于氧。

[0020] 接下来，可形成间隔件 138，如图 10 所图解说明。所图解说明的间隔件 138 为沉积于衬底 102 上的大体上保形（例如，当施加时在水平及垂直结构上具有大体上均匀厚度的材料）氧化物。在一些实施例中，间隔件 138 可为与上部牺牲区 126 相同的材料，但为不同于下部牺牲区 124 的材料。间隔件 138 可具有大体上大于或等于 1/16F、1/8F 或 1/4F 的厚度 140。间隔件 138 使前驱物沟槽 136 的宽度 142 变窄到大体上小于或等于 1F、3/4F 或 1/2F 的宽度。如下文所阐释，此较窄宽度 142 可大体上界定随后形成的鳍的宽度。

[0021] 在形成间隔件 138 之后，可蚀刻衬底 102，如图 11 所图解说明。所述蚀刻可为沿 Z 轴的大体上各向异性等离子体蚀刻，从而导致从水平表面移除间隔件材料 138。举例来说，前驱物沟槽 136 的底部中的牺牲区 126 的部分及上部牺牲区 126 上方的间隔件 138 的部分两者。移除此材料可形成侧壁间隔件，所述侧壁间隔件可在所述蚀刻进展以形成行间沟槽

144 时进一步担当掩模。所述蚀刻可穿透终止区 122、缓冲区 120、上部掺杂区 104 及下部掺杂区 106。在一些实施例中，所述蚀刻可比浅沟槽 110 深但不如深隔离沟槽 108 深。所述蚀刻可界定大体上笔直及大体上平行的行间沟槽 144，行间沟槽 144 在沿 X 方向的一显著距离上具有大体上均匀的横截面，例如大于五个晶体管的距离。行间沟槽 144 可具有大体上等于或小于 1F、3/4F 或 1/2F 的宽度 146。在一些实施例中，行间沟槽 144 可在1000 Å与10,000 Å之间深，例如在2000 Å与5000Å之间。在随后步骤期间，行间沟槽 144 可大体上界定安置于邻近晶体管行之间的电介质的形状及位置。

[0022] 接下来，可在行间沟槽 144 中形成外衬里 146，如图 12 所图解说明。所图解说明的外衬里 146 可为生长于上部掺杂区 104 及下部掺杂区 106 的暴露部分上的氧化物。在其它实施例中，可通过此项技术中已知的方法沉积外衬里 146。所述衬里可具有小于150 Å的厚度，例如20Å到70 Å，且在一些实施例中，其可保护上部掺杂区 104 及下部掺杂区 106 免于应力诱发的缺陷。

[0023] 如图 13 所图解说明，可在衬底 102 上形成内衬里 148。内衬里 148 可为沉积在衬底 102 上的氮化物层。内衬里 148 可具有小于200 Å的厚度，例如在30 Å与100 Å之间。在一些实施例中，可在内衬里 148 上形成另一衬里，例如具有在100 Å与300 Å之间的厚度的 TEOS 衬里。

[0024] 接下来，可在衬底 102 上形成行间电介质 150，如图 14 所图解说明。行间电介质 150 可由各种电介质材料制成或包含各种电介质材料，例如旋涂电介质 (SOD)。在一些实施例中，可通过加热衬底 102 来稠密化 SOD 行间电介质 150 以从行间电介质 150 驱动挥发性化合物。在稠密化期间，衬里 146 或 148 中的一者或一者以上可减轻来自收缩行间电介质 150 的否则可在衬底 102 中导致晶面的滑移或错位的膜应力。

[0025] 如图 15 所图解说明，可在形成行间电介质 150 之后移除衬底 102 的顶部部分。在一些实施例中，通过在下部牺牲区 124 上或在其中停止的 CMP 过程移除所述顶部部分。可通过在过渡到下部牺牲区 124 中期间出现的现象指示所述 CMP 过程到达终点。此种现象的实例包含衬底 102 的光学特性（例如，色彩或反射率）的改变、废料的化学特性（例如，废浆中的化合物）的改变或衬底 102 的机械特性（例如，滑动摩擦）的改变。另一选择为，或另外，可通过在下部牺牲区 124 上或在其中停止的蚀刻来移除衬底 102 的顶部部分。

[0026] 此步骤暴露用于移除的下部牺牲区 124，以便可在其位置中形成侧壁间隔件，如下文所阐释。在一些实施例中，通过通常对制成下部牺牲区 124 的材料有选择的湿式蚀刻来移除下部牺牲区 124，例如通常对多晶硅有选择的湿式蚀刻，例如氢氧化四甲铵 (TMAH) 蚀刻。通过移除下部牺牲区 124 所留下的间隔可具有通常与鳍掩模 128 的遮蔽区的宽度 132（图 7）对应（例如，大体上等于或成比例）的宽度 152。间隔件 138 的垂直、暴露表面可提供在其上可形成侧壁间隔件以定位及定形栅极及鳍的表面。

[0027] 接下来，可在衬底 102 上形成另一间隔件 154，如图 17 所图解说明。此间隔件 154 可由不同于早期间隔件 138、内衬里 148、行间电介质 150 及终止区 122 的材料制成。在一些实施例中，第二间隔件 154 由与下部牺牲 124 相同的材料制成，例如多晶硅。间隔件 154 可为在衬底 102 上沉积到在100 Å与1000 Å之间（例如，在200 Å与600 Å之间）的厚度 156 的大体上保形膜。在一些实施例中，厚度 156 可大于、小于或大体上等于 1/8F 或 1/4F，且间

隔件 154 可界定间隙 158，其具有大体上小于或等于 1/4F、1/2F 或 1F 的宽度 160。如下文所阐释，厚度 156 可大体上界定随后形成的栅极的宽度且宽度 160 可大体上界定随后形成的鳍的宽度。

[0028] 如图 18 所图解说明，可各向异性蚀刻第二间隔件 154 以形成侧壁间隔件。所述蚀刻可在等离子体蚀刻室中执行，且其通常可从水平表面移除间隔件 154 的一显著部分或全部同时留下安置于垂直表面上的间隔件 154 的一显著部分。所述蚀刻可在终止区 122、缓冲区 120 或上部掺杂区 104 上或在其中停止。

[0029] 在蚀刻间隔件 154 之后，可在衬底 102 上形成另一牺牲区 162，如图 19 所图解说明。所图解说明的牺牲区 162 可为沉积到在100 Å与1000 Å之间（例如，在200 Å与600 Å之间）的厚度的氧化物。牺牲区 162 可部分地、大致或完全地填充空隙 158。在一些实施例中，牺牲区 162 可为不同于第二间隔件 154 的材料以方便选择性地移除通过第二间隔件 154 形成的间隔件。

[0030] 接下来，可移除衬底 102 的顶部部分，如图 20 所图解说明。可通过各种过程来移除所述顶部部分，包含蚀刻或 CMP。在一些实施例中，抛光衬底 102 直到暴露从第二间隔件 154 形成的侧壁间隔件的顶部部分。

[0031] 如图 21 所图解说明，从衬底 102 移除第二间隔件 154。可通过蚀刻移除第二间隔件 154，例如通常对制成第二间隔件 154 的材料有选择的湿式蚀刻。举例来说，在其中第二间隔件 154 由多晶硅制成的实施例中，可通过 TMAH 湿式蚀刻来移除第二间隔件 154。

[0032] 接下来，蚀刻可从衬底 102 的通过移除第二间隔件 154 所暴露的部分移除材料，如图 22 所图解说明。所述蚀刻可形成栅极沟槽 164、鳍行 166 及绝缘突出部 168。栅极沟槽 164 可每一者安置于鳍行 166 中的每一者与绝缘突出部 168 中的每一者之间。衬底 102 针对每一鳍行 166 及每一绝缘突出部 168 可包含两栅极沟槽 164。所图解说明的栅极沟槽 164 安置于鳍行 166 与绝缘突出部 168 之间。在所图解说明的实施例中，所述蚀刻不会从行间电介质 150 移除材料，且绝缘突出部包含夹在上部掺杂区 104 及下部掺杂区 106 的两个部分之间的行间电介质 150。在其它实施例中，尽管所述蚀刻可消耗上部掺杂区 104 及下部掺杂区 106 的这些部分，但来自行间电介质 150 的材料可界定栅极沟槽 164 的部分。

[0033] 可通过蚀刻进入衬底102 500 Å与4000 Å之间（例如，在1300 Å到2500 Å之间）的大体上各向异性蚀刻来形成特征 164、166 及 168。栅极沟槽 164、鳍行 166 及绝缘突出部 168 可大体上笔直且跨越沿 X 方向的一显著距离具有大体上均匀的横截面形状，例如跨越大于五个晶体管的距离。结构 164、166 及 168 可彼此大体上平行且大体上垂直于浅沟槽 110 及深隔离沟槽 108。栅极沟槽 164、鳍行 166 及绝缘突出部 168 可分别具有宽度 170、172 及 174，所述宽度大体上等于或小于 1/4F、1/2F 或 1F。在一些实施例中，栅极沟槽 164、鳍行 166 及绝缘突出部 168 的图案可以大体上等于或小于 3F、2F 或 3/2F 的周期 176 重复。

[0034] 接下来，通过 CMP 平面化衬底 102，如图 23 所图解说明。在一些实施例中，CMP 可移除牺牲区 162 及衬里 138 的残留部分，且在一些实施例中，其也可移除行间电介质 150、内衬里 148 及终止区 122 的顶部部分。所述平面化可在终止区 122 上或在其附近停止。在一些实施例中，在平面化之后，可清洁衬底 102 以移除 CMP 浆残余物。在一些实施例中，可在不将衬底 102 暴露于氢氟酸的情况下清洁衬底 102，所述氢氟酸因优先地蚀刻上部掺杂区 104 及下部掺杂区 106 的某些晶体定向面可形成凹坑。

[0035] 如图 24 所图解说明，可在栅极沟槽 164 中形成栅极电介质 178。在一些实施例中，可通过化学气相沉积 (CVD) 或原子层沉积 (ALD) 来沉积栅极电介质 178，或可通过（举例来说）将衬底 102 暴露于氧来生长栅极电介质 178。栅极电介质 178 可由各种电介质材料制成，例如氧化物（例如，二氧化硅）、氧氮化物或高介电常数材料，如二氧化铪、二氧化锆及二氧化钛。在一些实施例中，栅极电介质 178 可具有小于300Å的厚度，例如在30 Å与150 Å之间。

[0036] 接下来，可在衬底 102 上形成栅极材料 180，如图 25 所图解说明。所述栅极材料可为各种导电材料中的一者或一者以上，例如经掺杂多晶硅、钨、钛、氮化钛或其它适当材料，且其可通过各种过程来形成，例如物理气相沉积 (PVD) 或 CVD。

[0037] 在形成栅极材料 180 之后，可从衬底 102 移除栅极材料 180 的顶部部分，如图 26 所图解说明。可通过各种过程移除栅极材料 180，例如 CMP、等离子体蚀刻、湿式蚀刻或其组合。在一些实施例中，使栅极材料 180 凹入大体上小于或等于1000 Å（例如，在200 Å与500 Å之间）的距离 182。距离 182 可允许栅极材料 180 的顶部高于上部掺杂区 104 的底部，即，栅极材料 180 可与上部掺杂区 104 至少部分地重叠。在一个实施例中，使栅极材料 180 凹入到栅极沟槽 164 中形成栅极 184 及 186。栅极 184 及 186 可安置于鳍行 166 的相对侧上，且所图解说明的栅极 184 及 186 可通过绝缘突出部 168 与邻近栅极 184 或 186 电隔离。

[0038] 所图解说明的栅极 184 及 186 可比一些常规设计中的栅极彼此短路的可能性小。在一个实施例中，绝缘突出部 168 界定栅极沟槽 164 的一部分（例如，大约一半），由此形成沿至少一个方向（例如，最靠近的邻近鳍行 166 的方向）绝缘的沟槽 164。因此，通过使栅极材料 180 凹入到预隔离的栅极沟槽 164 中形成所图解说明的栅极 184 及 186。相信此实施例的栅极 184 及 186 比常规设计的栅极短路的可能性小，常规设计经常包含在大体上界定栅极的形状之后隔离的栅极。换句话说，在一些常规设计中，栅极至少部分地确定栅极间电介质的形状，而在所图解说明的实施例中，栅极之间的绝缘结构（即，绝缘突出部 168）的形状至少部分地确定栅极 184 及 186 的形状。在一些实施例中相信此将增加绝缘突出部 168 的效用，因为绝缘突出部 168 在栅极 184 及 186 形成之前阻隔栅极 184 与 186 之间的路径。

[0039] 所图解说明的鳍行 166 中的每一者可与邻近栅极 184 及 186 协作以形成多个晶体管 188。图 27 图解说明了晶体管 188 的部分的形状，其图解说明单个晶体管 188 的半导电部分的形状。所图解说明的晶体管 188 包含从基底 192 上升的鳍 190。所图解说明的鳍 190 包含末端部分，其具有通过大体上 U 形空隙 198 分离的两个支腿 194 及 196。在此实施例中，空隙 198 通过浅沟槽 110 形成且空隙 198 延伸低于上部掺杂区 104 的深度。所图解说明的支腿 194 及 196 包含上部掺杂区 104 及下部掺杂区 106 的顶部部分两者。所图解说明的鳍 190 还包含两个相对侧 200 及 202，所述相对侧可彼此大体上平行，相对于彼此大体上成角度，或相对于彼此大体上弯曲。鳍 188 的边缘 204 及 206 可大体上垂直于侧 200 及 202 且大体上彼此平行，相对于彼此大体上成角度或相对于彼此大体上弯曲。

[0040] 在操作中，两个支腿 194 及 196 可用作源极及漏极，且晶体管 188 可根据栅极 184 及 186（图 26）的电压选择性地控制所述源极与所述漏极之间的电流流动。当接通时，所图解说明的晶体管 188 建立由箭头 208 所表示的大体上垂直通道，箭头 208 图解说明源极与

漏极之间的电流流动。可通过源自两个栅极 184 及 186 的电场建立通道 208。可根据各种模式给栅极 184 及 186 通电；通常可同时给栅极 184 及 186 两者通电；可给一个栅极 184 及 186 通电，但不给另一个通电；或可彼此独立地给栅极 184 及 186 通电。在一些实施例中，栅极 184 及 186 可部分地或完全地围绕鳍行 166，例如栅极 184 及 186 可连接在鳍行 166 的一个端或两个端处。所图解说明的晶体管 188 可称作双栅极晶体管或多栅极晶体管，因为其在邻近每一侧壁 200 及 202 处具有栅极 184 及 186。

[0041] 先前所描述的实施例通过参照图 7 所描述的单个光刻步骤来形成沿 X 方向延伸的结构，即，鳍行 166、栅极 184 及 186 以及绝缘突出部 168。其它实施例可通过两个或多于两个光刻步骤但较少总步骤来形成这些结构 166、184 及 186。图 28 到 37 图解说明此制造过程的实例。如下文所阐释，此实施例与上文所述实施例相比包含较少过程步骤，但包含一个额外光刻步骤。

[0042] 如图 28 所图解说明，此实施例以提供衬底 210 开始。衬底 210 可初始地经受上文参照图 1 及 2 所描述的过程。因此，衬底 210 可包含上部掺杂区 104、下部掺杂区 106、深隔离沟槽 108 及浅沟槽 110。在这些特征的顶部上，可形成第一鳍掩模 212。第一鳍掩模 212 可由光致抗蚀剂制成，或其可为硬掩模。第一鳍掩模 212 可通过上文所述的光刻系统或次光刻技术中的任一者来图案化，例如抗蚀剂回流、掩模底切或经由侧壁间隔件的间距倍增。在一些实施例中，第一鳍掩模 212 大体上界定具有宽度 214 的暴露区及具有宽度 216 的遮蔽区。在某些实施例中，这些宽度 214 及 216 大体上相等且每一者大体上等于或小于 1F。第一鳍掩模 212 可以大体上等于或小于 2F 的周期 218 重复。所图解说明的暴露区及遮蔽区大体上笔直、大体上平行于相邻掩模结构及大体上垂直于深隔离沟槽 108 及浅沟槽 110 两者。第一鳍掩模 212 的暴露区及遮蔽区可跨越沿 X 方向的一显著距离具有大体上均匀的横截面，例如大于五个晶体管的距离。

[0043] 接下来，蚀刻行间沟槽 220，如图 29 所图解说明。可通过大体上各向异性等离子体蚀刻来蚀刻行间沟槽 220，且其可延伸到衬底 210 中大于浅沟槽 108 的深度但不如深隔离沟槽 110 深的距离。在其它实施例中，行间沟槽 220 可大体上如深隔离沟槽 110 那么深或比深隔离沟槽 110 深。可通过场隔离植入（未显示）对行间沟槽 220 的底部进行植入以隔离随后形成的晶体管。

[0044] 如图 30 所图解说明，在蚀刻行间沟槽 220 之后，可移除第一鳍掩模 212，且行间电介质 222 可形成于行间沟槽 220 中。在一些实施例中，可通过 CVD、ALD、旋涂电介质或其它适当过程及材料形成行间电介质 222。行间电介质 222 可为氧化物，例如上文所述的氧化物中的一者，且在一些实施例中，其可包含邻近上部掺杂区 104 及下部掺杂区 106 的薄氧化物衬里及在氧化物衬里与行间电介质 222 的剩余部分之间的氮化物衬里两者。在一些实施例中，行间电介质 222 经沉积而具有覆盖层，所述覆盖层通过 CMP 或蚀刻移除以大体上平面化衬底 210 的表面。

[0045] 接下来，如图 31 所图解说明，可形成第二鳍掩模 224。第二鳍掩模 224 可相对于第一鳍掩模 212 错位距离 225，所述距离 225 大体上等于第一鳍掩模 212 的周期 218 的一半。举例来说，第一鳍掩模 224 的遮蔽区的中点可与第二鳍掩模 212 的遮蔽区的中点分离距离 225。另外，第二鳍掩模 224 的遮蔽区的中点可大体上落在第一鳍掩模 212 的遮蔽区的边缘上或其附近，如第二鳍掩模 224 相对于行间沟槽 220 中的行间电介质 222 的边缘的

位置所图解说明。第二鳍掩模 224 可大体上界定具有宽度 226 的暴露区及具有宽度 228 的遮蔽区。这些特征可以周期 230 重复。在一些实施例中，周期 230 大体上等于第一鳍掩模 212 的周期 218。所述遮蔽区的宽度 228 可大体上等于或小于 1F、1/2F 或 1/4F。在某些实施例中，第二鳍掩模 224 的遮蔽区的宽度为第一鳍掩模 212 的遮蔽区的宽度 216 的一部分，例如大体上等于或小于宽度 216 的 1/4 或 1/2。第二鳍掩模 224 的暴露区及遮蔽区可大体上笔直，大体上平行于相邻掩模结构，大体上平行于行间电介质 222，及大体上垂直于深隔离沟槽 108 及浅沟槽 110 两者。第二鳍掩模 224 可跨越沿 X 方向的一显著的距离具有大体上均匀的横截面，例如大于五个晶体管的距离。

[0046] 可通过各种技术形成第二鳍掩模 224。举例来说，在一些实施例中，第二鳍掩模 224 由用光刻系统图案化的光致抗蚀剂制成。在其它实施例中，通过使通过光刻界定的掩模间距倍增来形成第二鳍掩模 224。举例来说，可通过用安置于所图解说明的第二鳍掩模 224 的大致每隔一遮蔽区之间的遮蔽区图案化前驱物掩模且然后将第二鳍掩模 224 形成为所述前驱物掩模的侧上的侧壁间隔件来形成第二鳍掩模 224。

[0047] 接下来，在第二鳍掩模 224 的侧上形成侧壁间隔件 232，如图 32 所图解说明。可通过在衬底 210 上沉积毯覆膜且然后各向异性地蚀刻所述膜来形成侧壁间隔件 232。在一些实施例中，侧壁间隔件 232 可由碳制成，且其可具有大体上等于或小于 1F、1/2F 或 1/4F 的宽度 234。侧壁间隔件 232 可界定具有宽度 236 的间隙，宽度 236 大体上等于或小于 1F、1/2F 或 1/4F。

[0048] 接下来，可移除第二鳍掩模 224 且可在衬底 210 中蚀刻栅极沟槽 238，如图 33 所图解说明。可通过由侧壁间隔件 232 遮蔽的大体上各向异性蚀刻来形成栅极沟槽 238。在一些实施例中，栅极沟槽 238 比浅沟槽 110 深但不如行间电介质 222 或者深隔离沟槽 108 深。栅极沟槽 238 可在500 Å与3000 Å之间深，例如在1300 Å与1700 Å之间。栅极沟槽 238 可大体上平行，大体上笔直且大体上垂直于深隔离沟槽 108 及浅沟槽 110 两者。在此实施例中，栅极沟槽 238 跨越沿 X 方向的一显著距离具有大体上均匀的横截面，例如大于五个晶体管的距离。

[0049] 在一些实施例中，形成栅极沟槽 238 也可大体上同时形成鳍行 240 及绝缘突出部 242。所图解说明的绝缘突出部 242 插入于所图解说明的鳍行 240 中的每一者之间，且在一些实施例中，每一鳍行 240 通过栅极沟槽 238 与任一侧上的邻近绝缘突出部 242 分离。与先前实施例一样，由于所图解说明的栅极沟槽 238 的位置及形状至少部分地通过移除材料以形成绝缘突出部 242 来界定，因此相信形成于栅极沟槽 238 中的栅极彼此短路的可能性较小。

[0050] 接下来，可在栅极沟槽 238 中形成栅极电介质 244，如图 34 所图解说明。可沉积或生长栅极电介质 244 且其可由各种电介质材料制成，例如，氧化物（例如，二氧化硅）、氧氮化物或高介电常数材料，如二氧化铪、二氧化锆及二氧化钛。在一些实施例中，栅极电介质 244 具有小于300 Å（例如在30 Å与150 Å之间）的厚度。

[0051] 在形成栅极电介质 244 之后，可在衬底 210 上形成栅极材料 246，如图 35 所图解说明。栅极材料 246 可为通过 CVD、PVD 或其它适当过程沉积的导电材料。在一些实施例中，栅极材料 246 包含上文所列出的导电材料中的一者。栅极材料 246 可经沉积而具有覆盖层 248 以增加所有栅极沟槽 238 被填充的可能性且平面化衬底 210。栅极材料 246 可在移除

间隔件 232 之前或之后形成于衬底 210 上。

[0052] 接下来，可移除覆盖层 248 且使栅极材料 246 凹入以形成栅极 250 及 252，如图 36 所图解说明。栅极 250 及 252 可凹入距离 254，所述距离 254 经选择以减小残余栅极材料 238 连接绝缘突出部 242 的相对侧上的栅极 250 及 252 的可能性。可通过 CMP、干式蚀刻、湿式蚀刻或其组合来使栅极 250 及 252 凹入。在一些实施例中，栅极 250 及 252 与上部掺杂区 104 重叠且经凹入不低于上部掺杂区 104 的底部。

[0053] 在此阶段处，衬底 210 可包含多个晶体管 256。图 37 图解说明这些晶体管 256 的半导体部分的形状。每一所图解说明的晶体管 256 包含从基底 260 上升的鳍 258。鳍 258 可包含侧 261 及 262、边缘 264 及 266、支腿 268 及 270 及大体上 U 形空隙 272。与先前实施例一样，所图解说明的支腿 268 及 270 可用作源极及漏极，且源自栅极 252 及 254 的电场可在鳍 258 的任一侧 260 及 262 中建立通道 274。

[0054] 虽然本发明可容许有各种修改及替代形式，但具体实施例已以举例方式显示于所述图式中并详细描述于本文中。然而，应理解，并不打算将本发明限定于所揭示的特定形式。相反，本发明将涵盖属于上文所附权利要求书所界定的本发明的精神及范围内的所有修改、等效形式及替代方案。

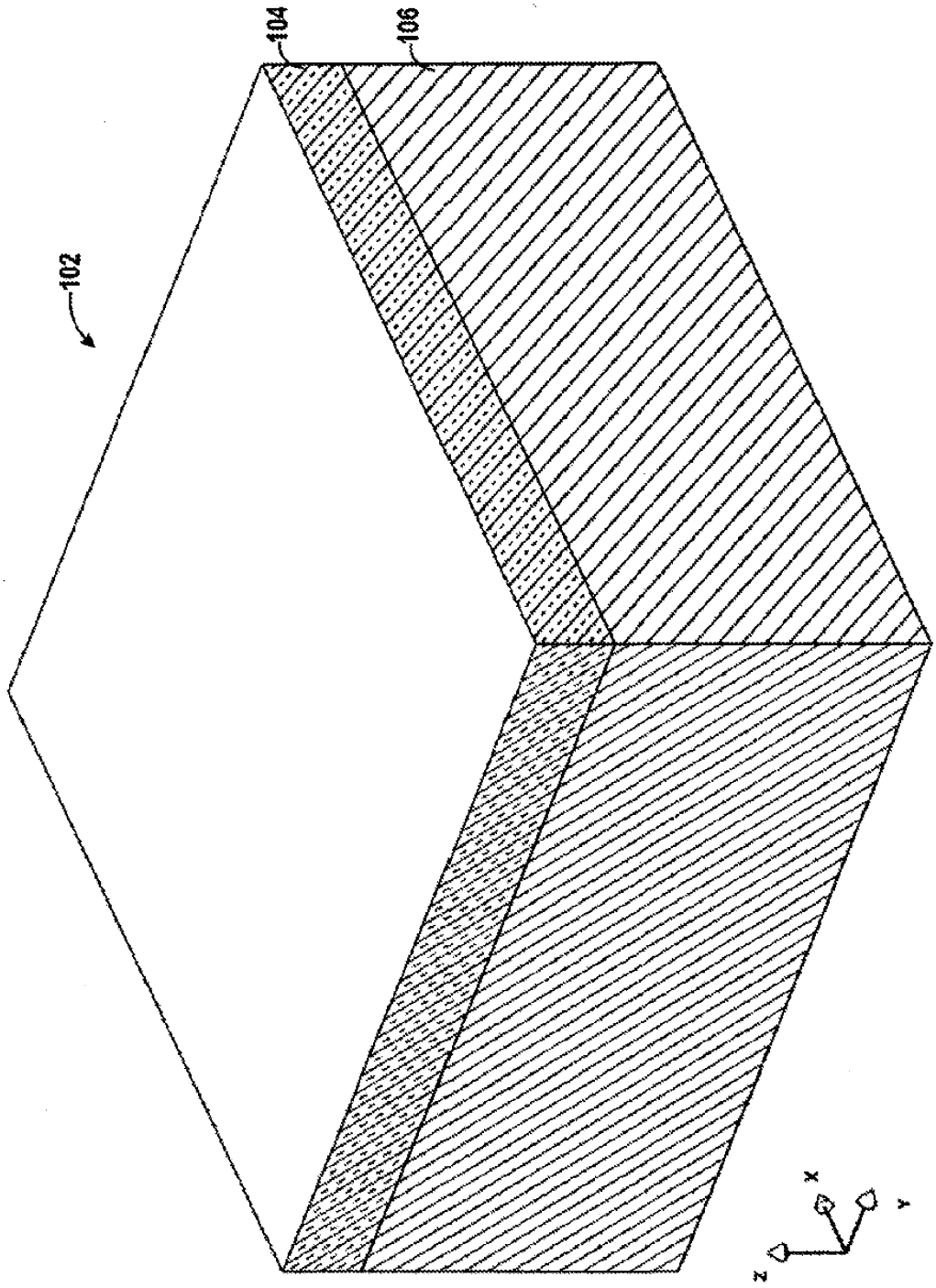


图 1

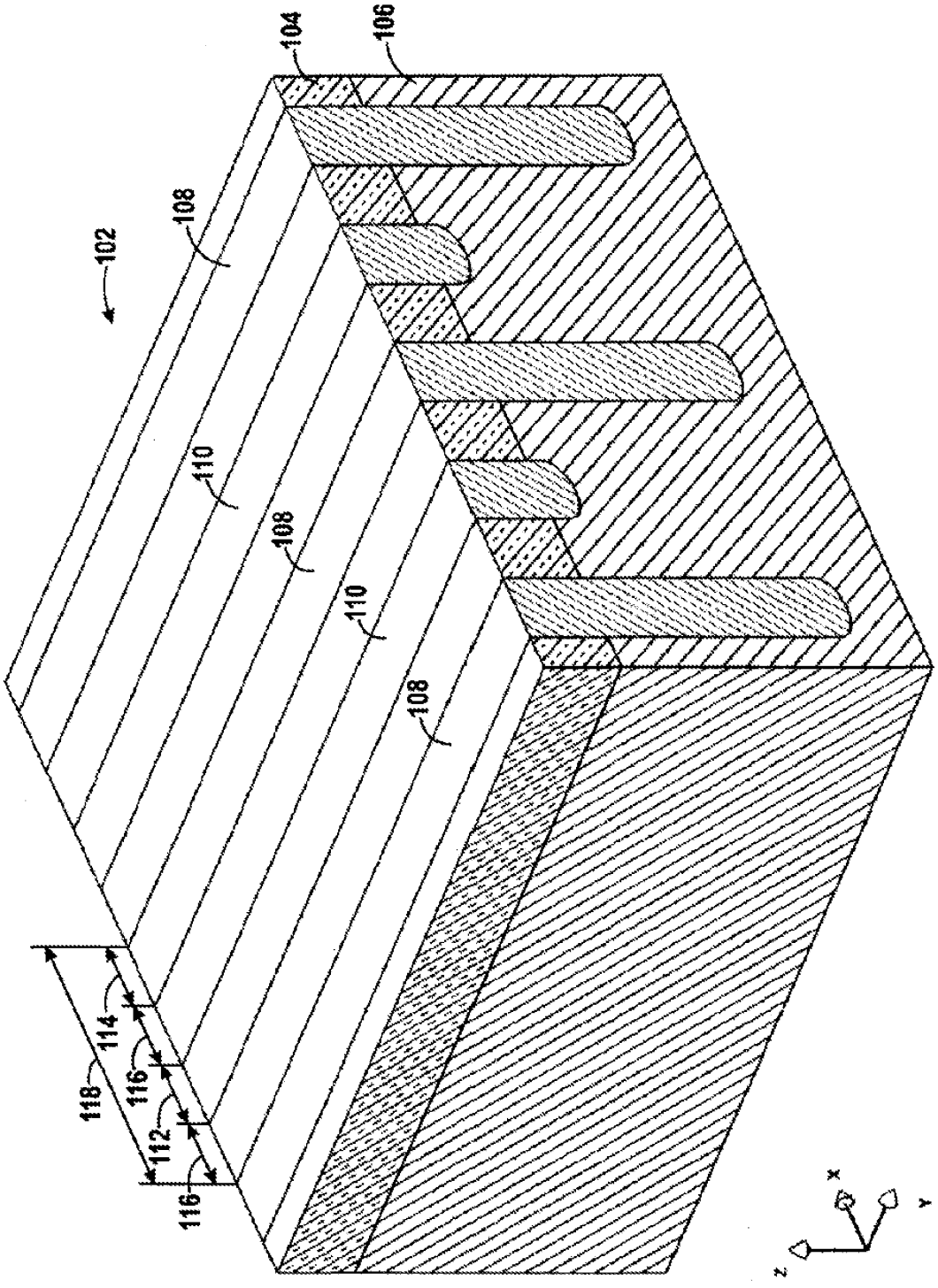


图 2

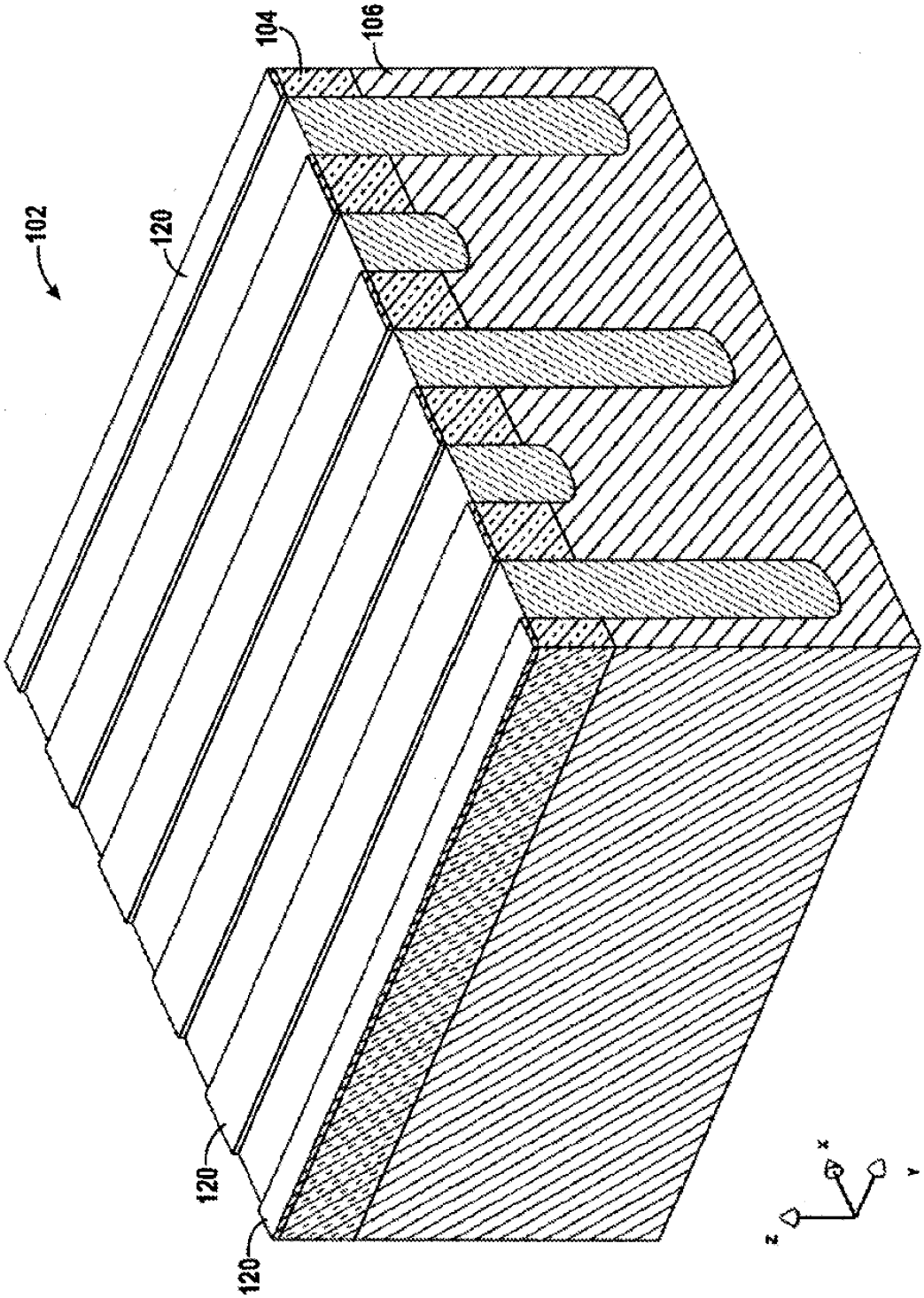


图 3

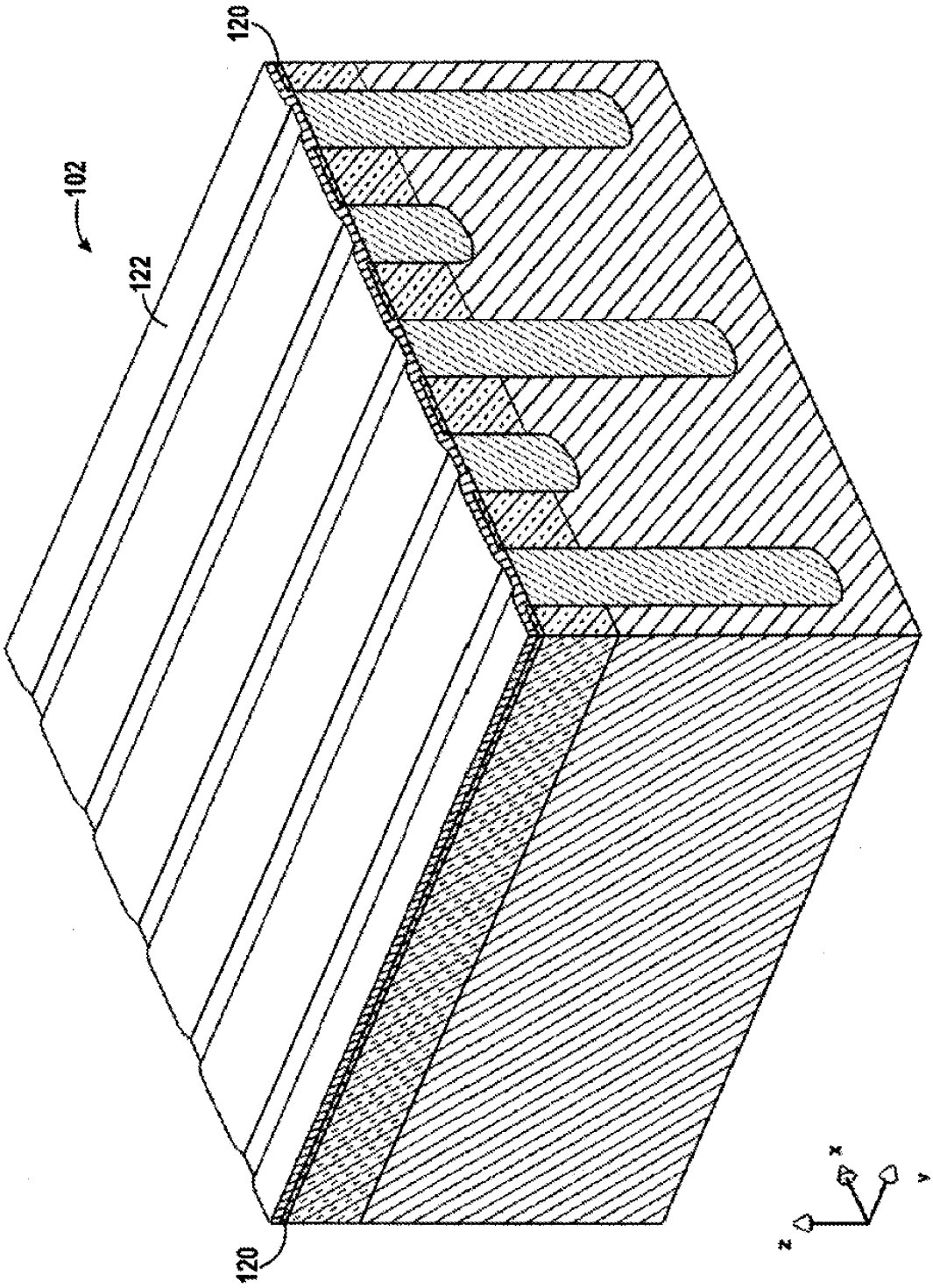


图 4

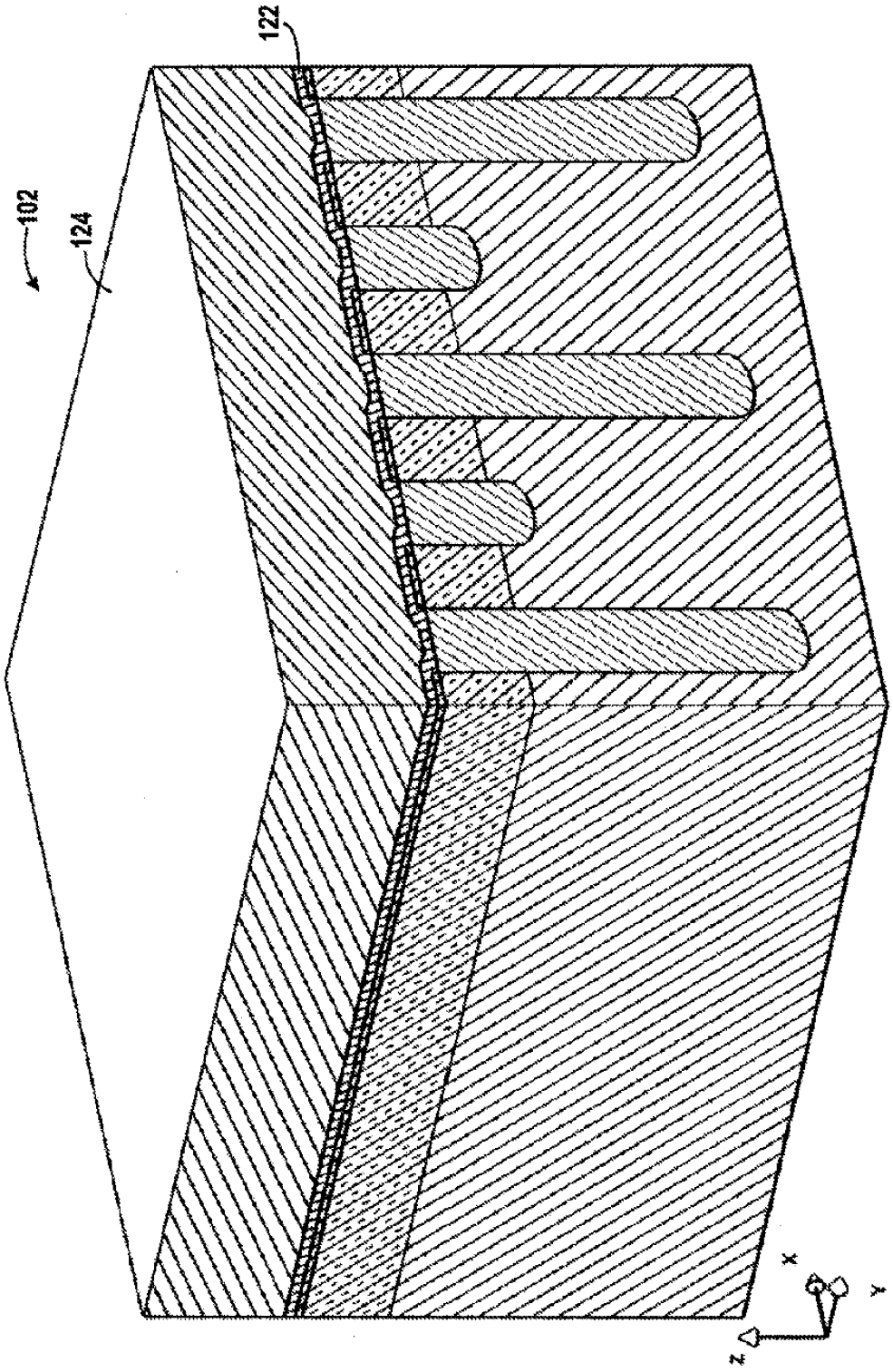


图 5

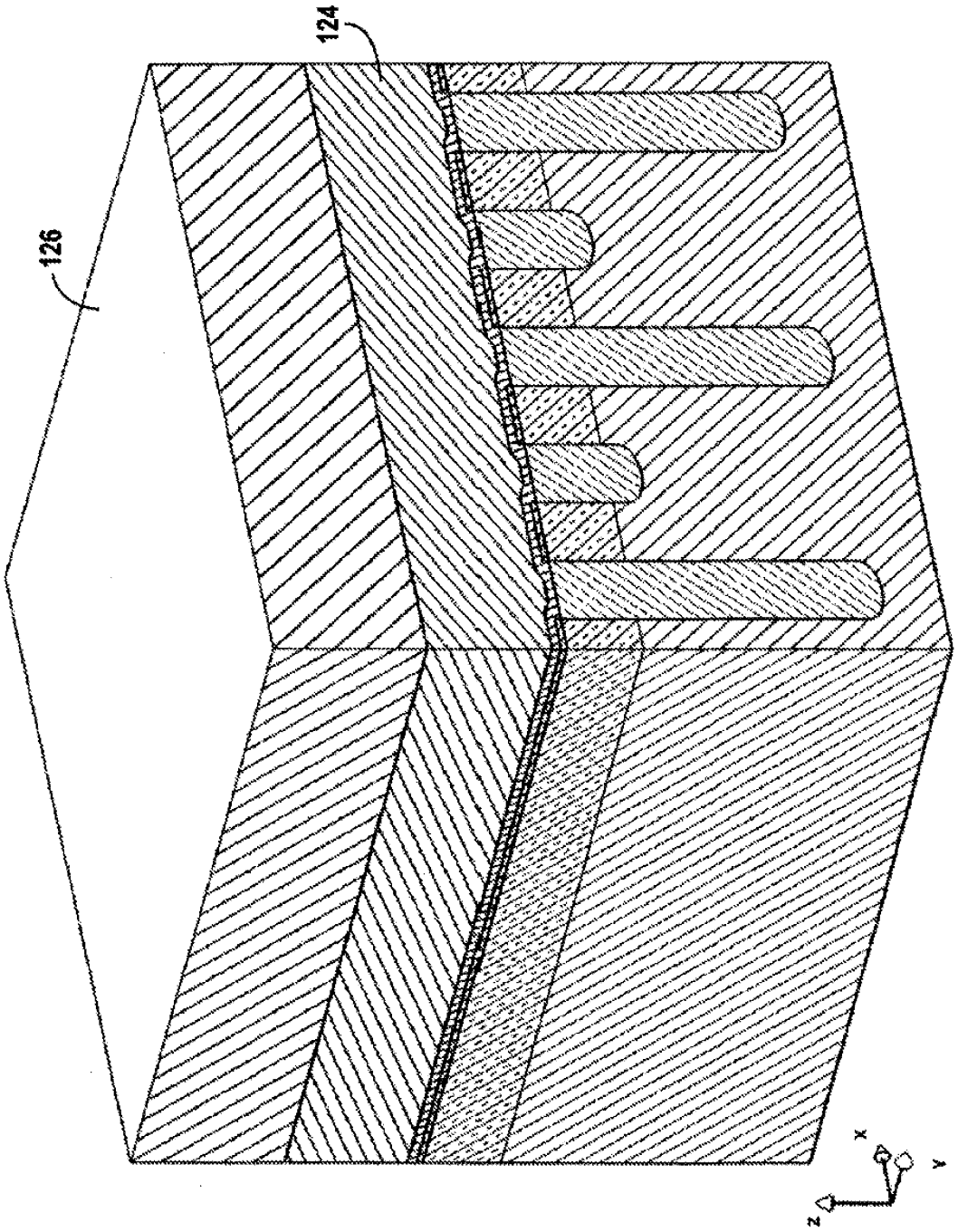


图 6

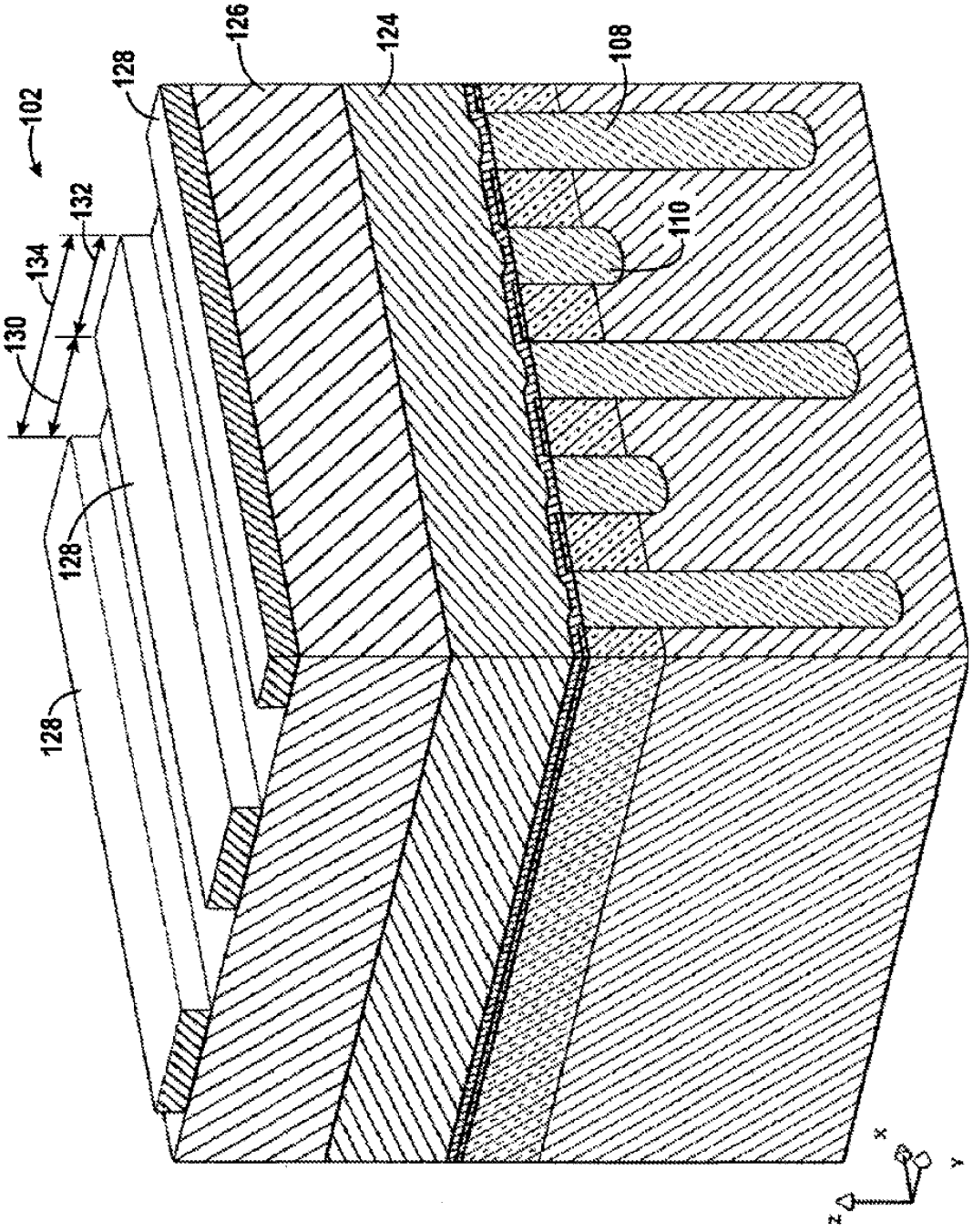


图 7

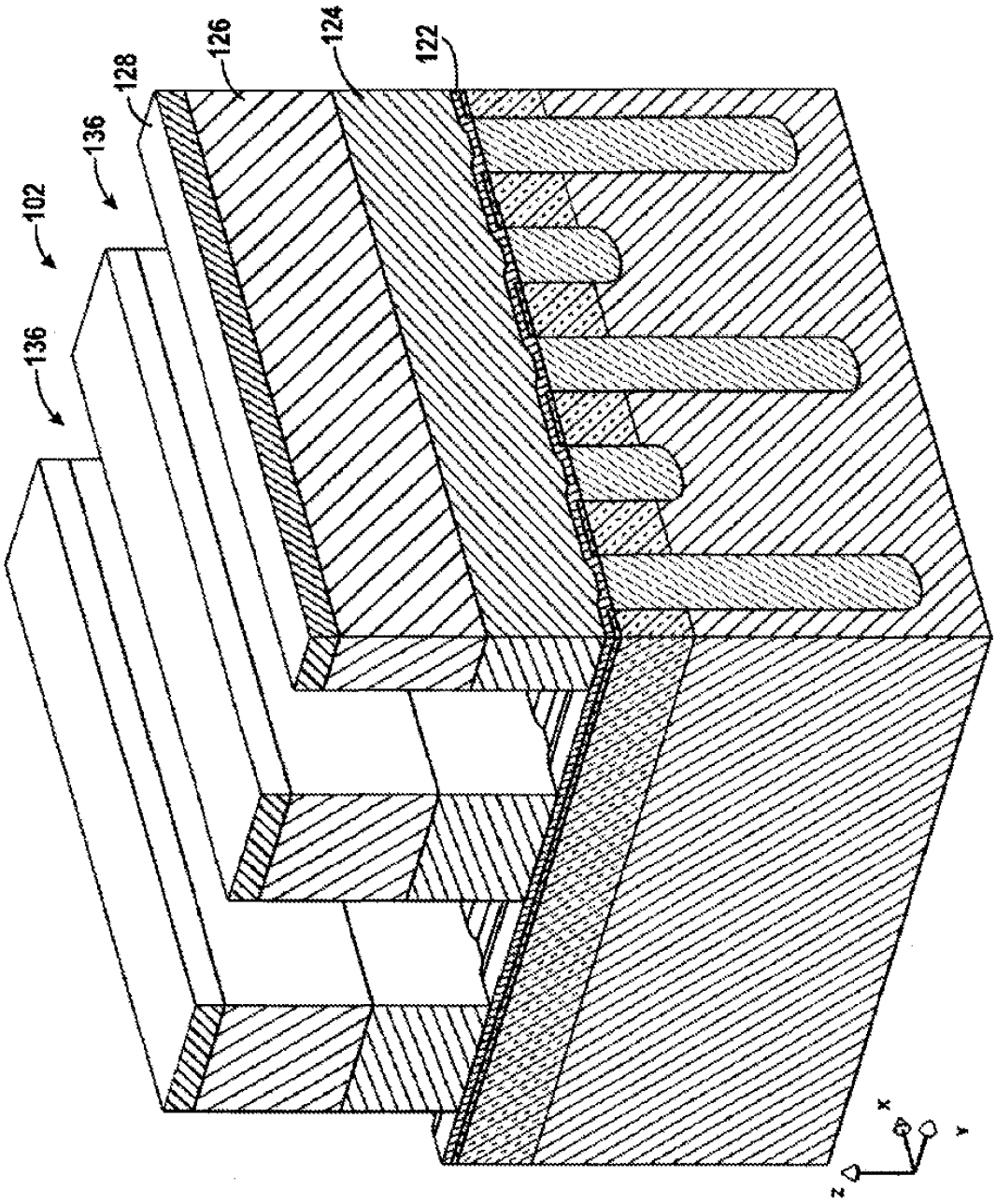


图 8

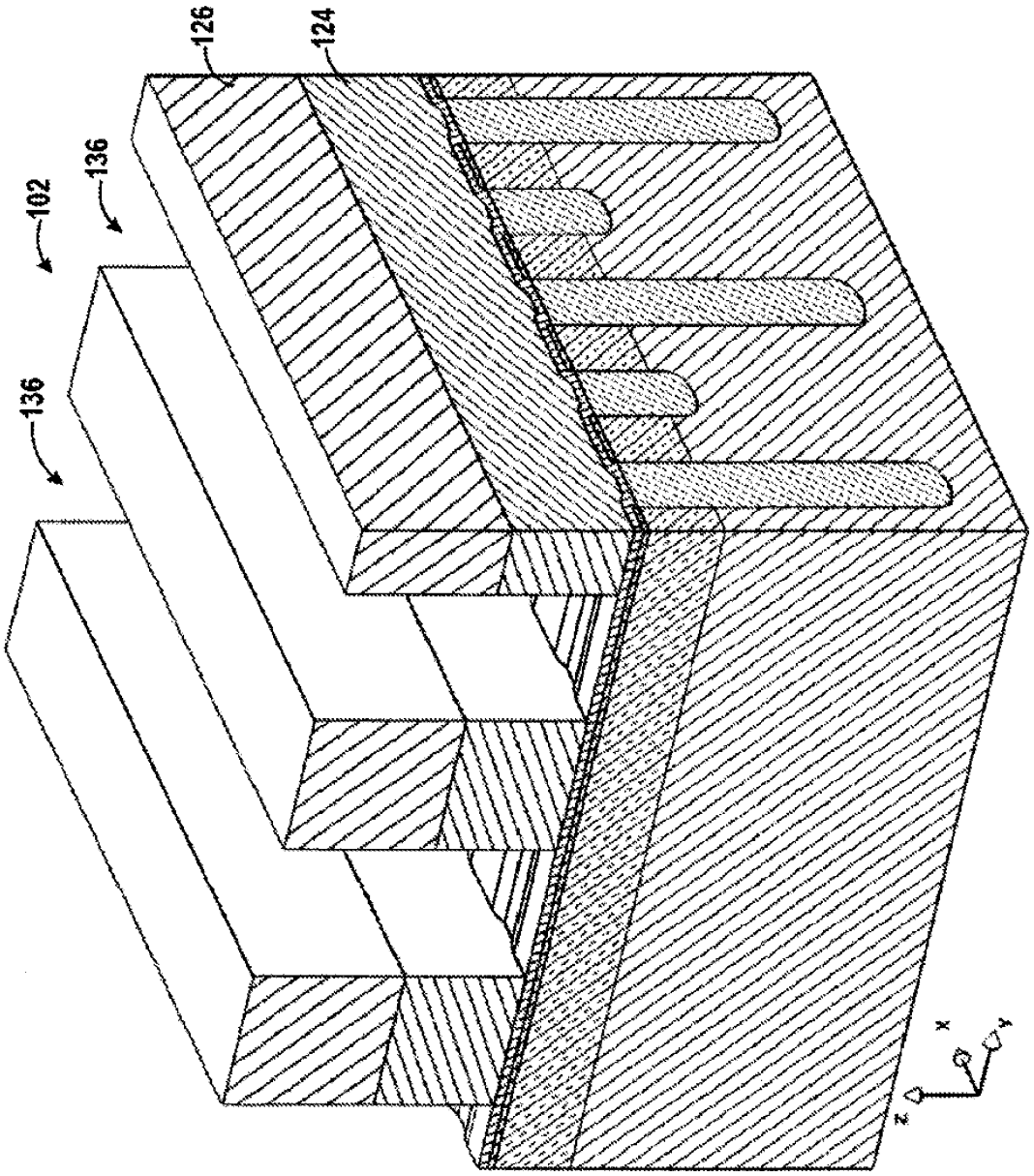


图 9

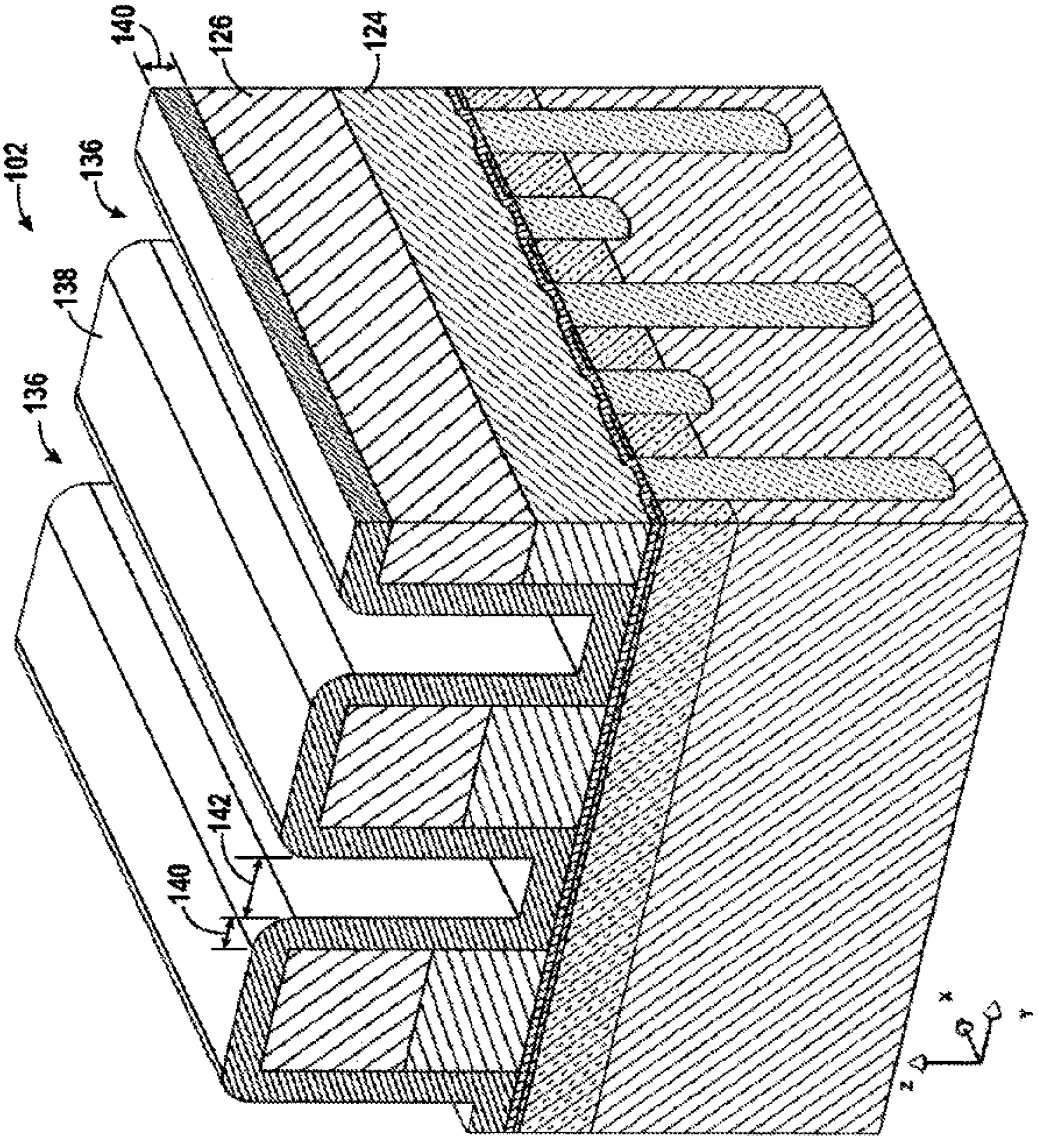


图 10

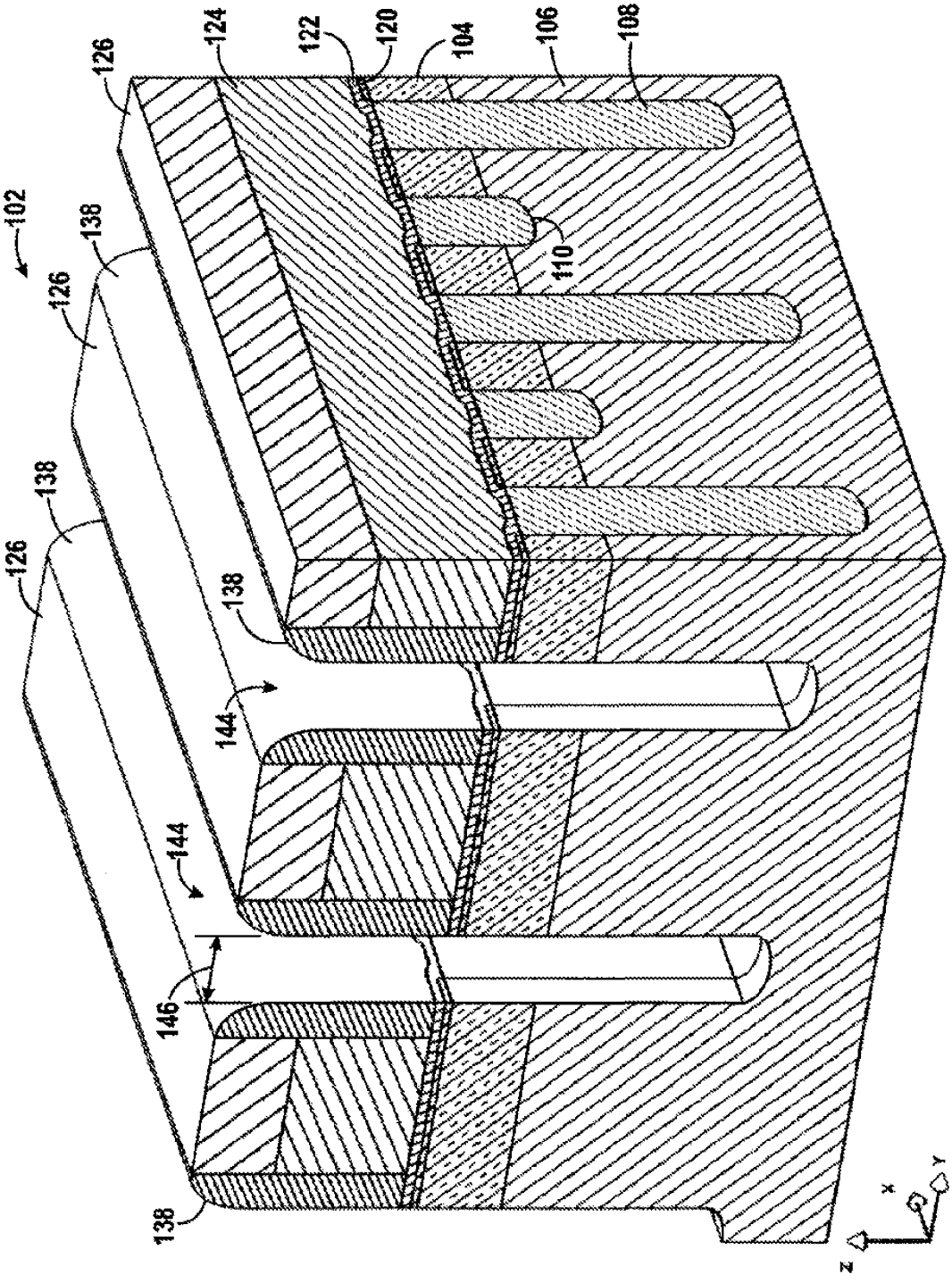


图 11

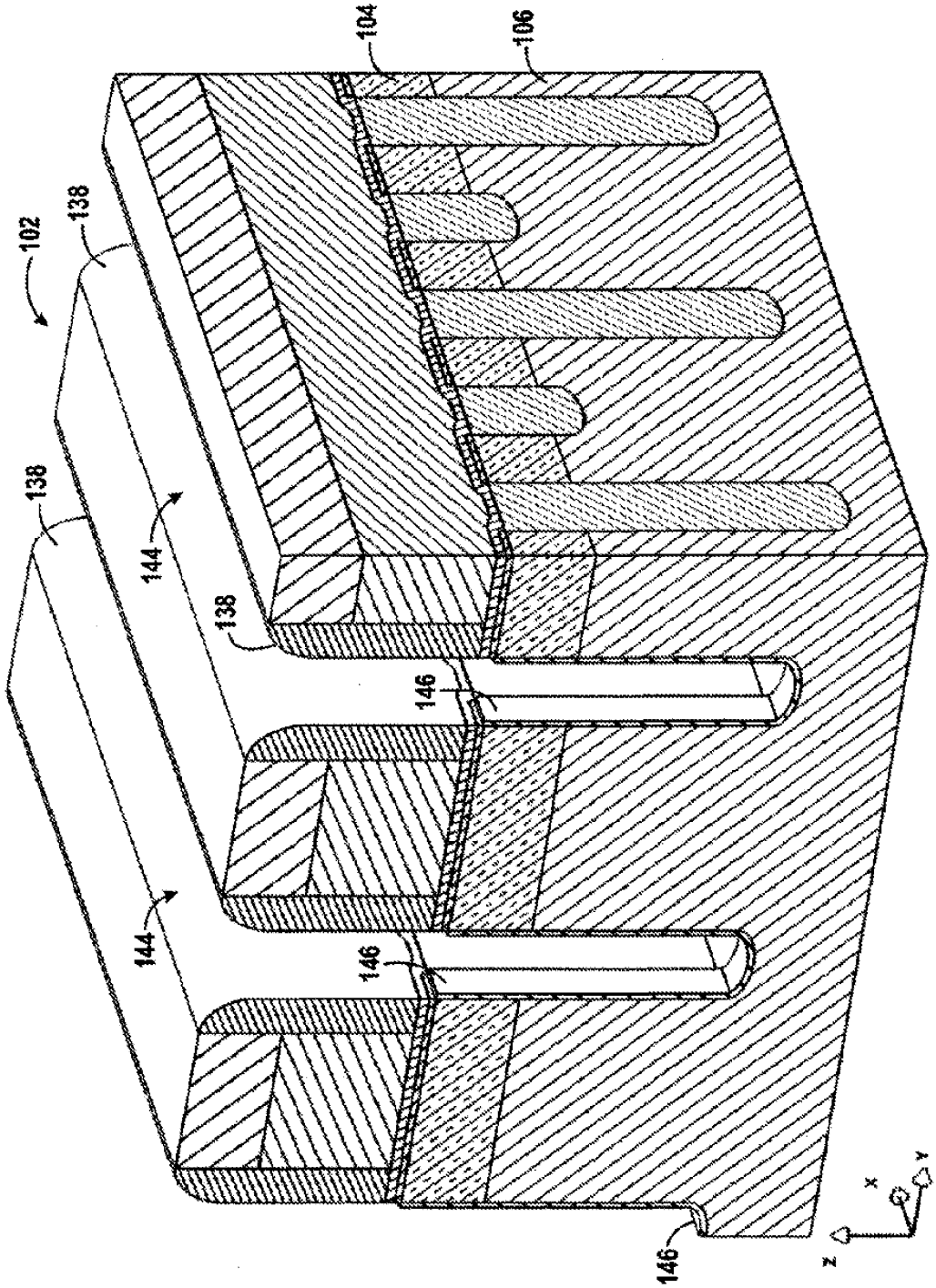


图 12

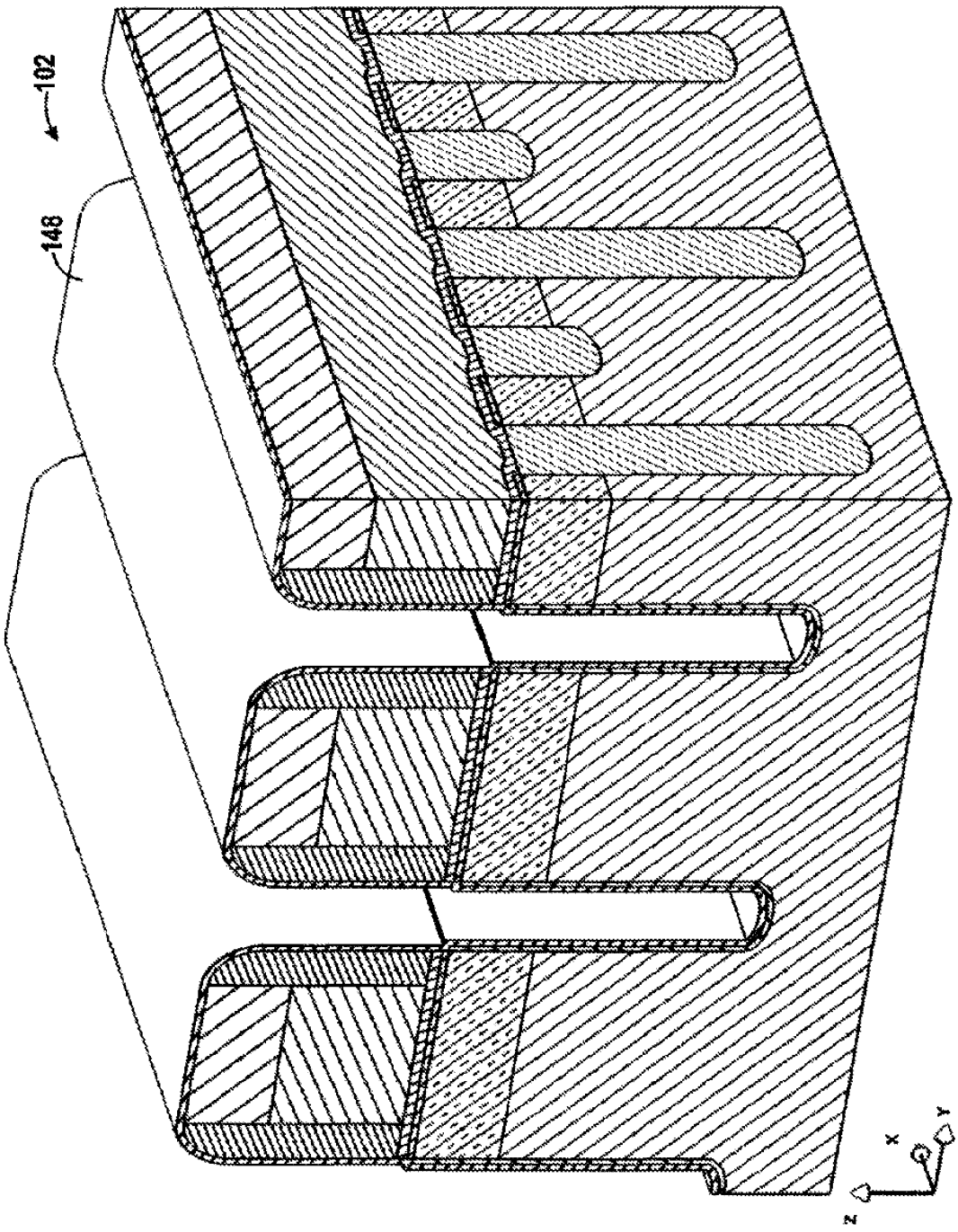


图 13

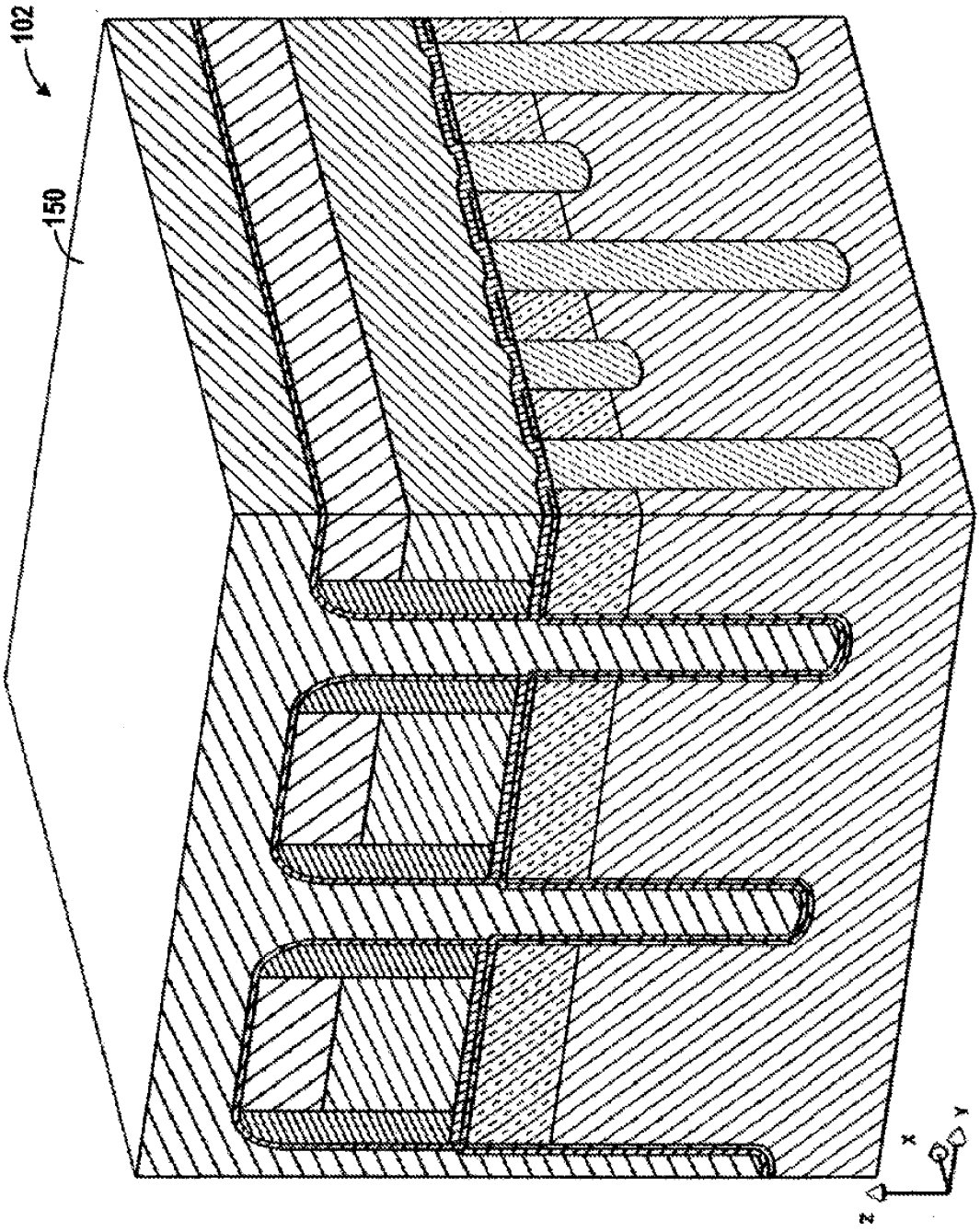


图 14

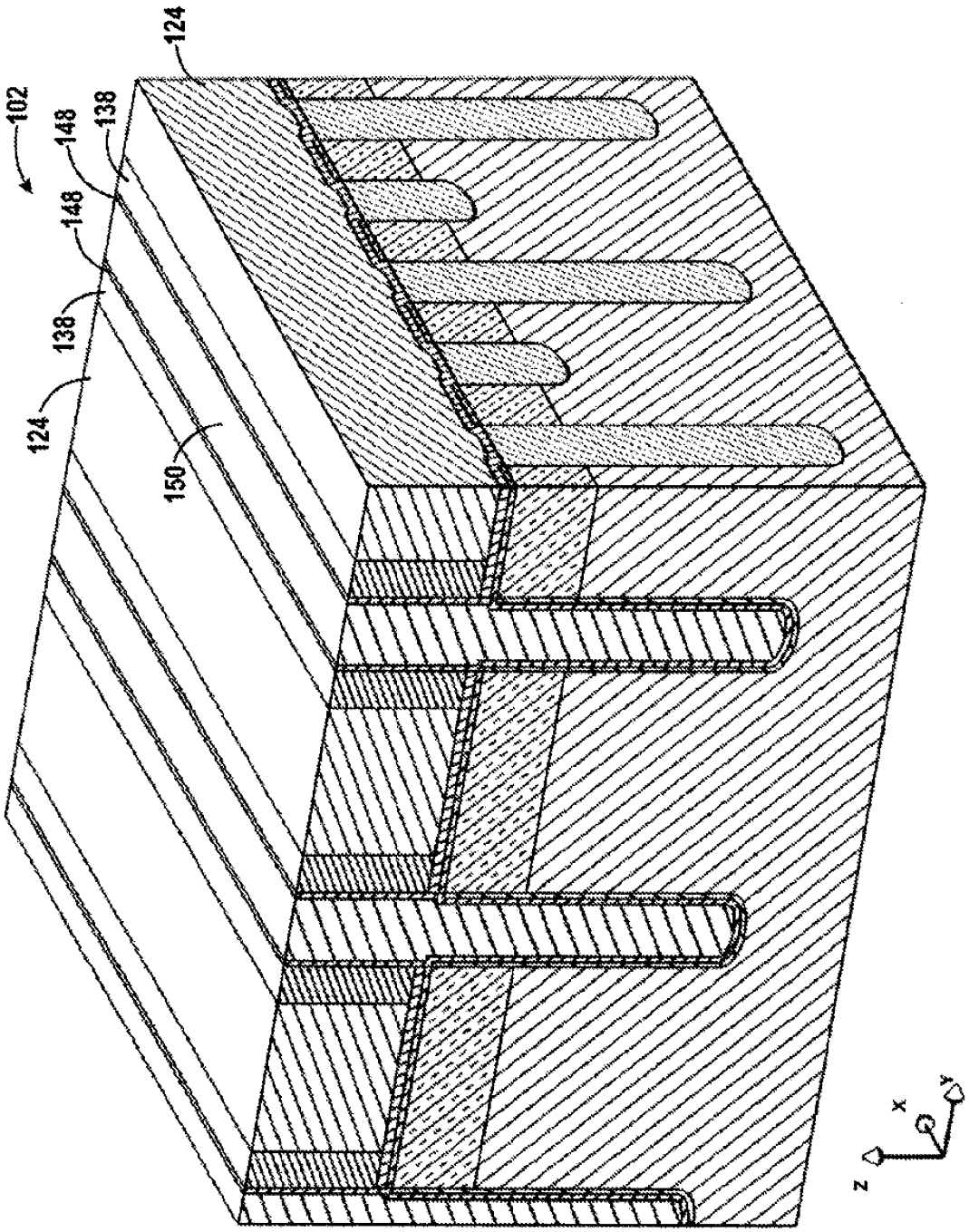


图 15

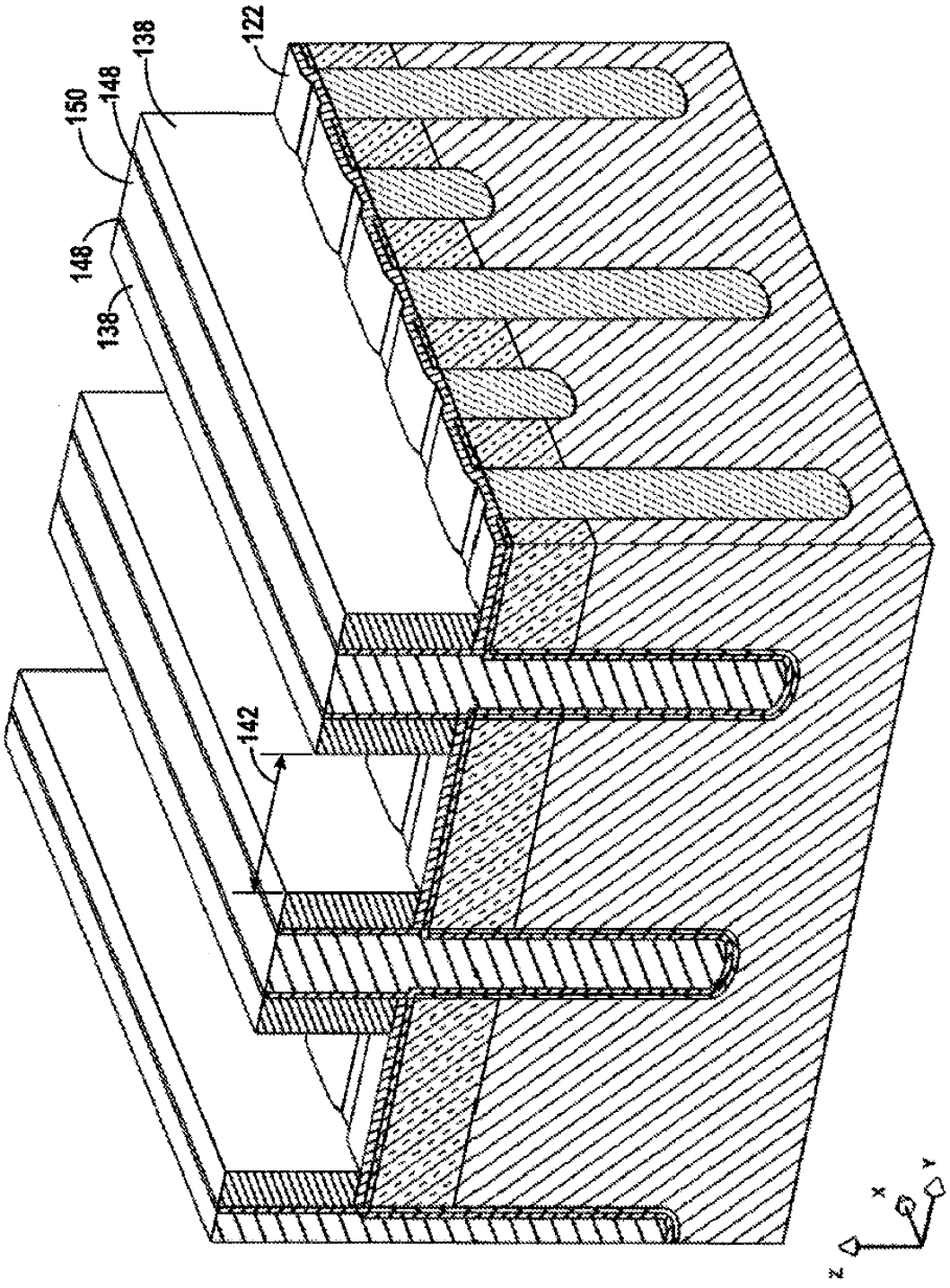


图 16

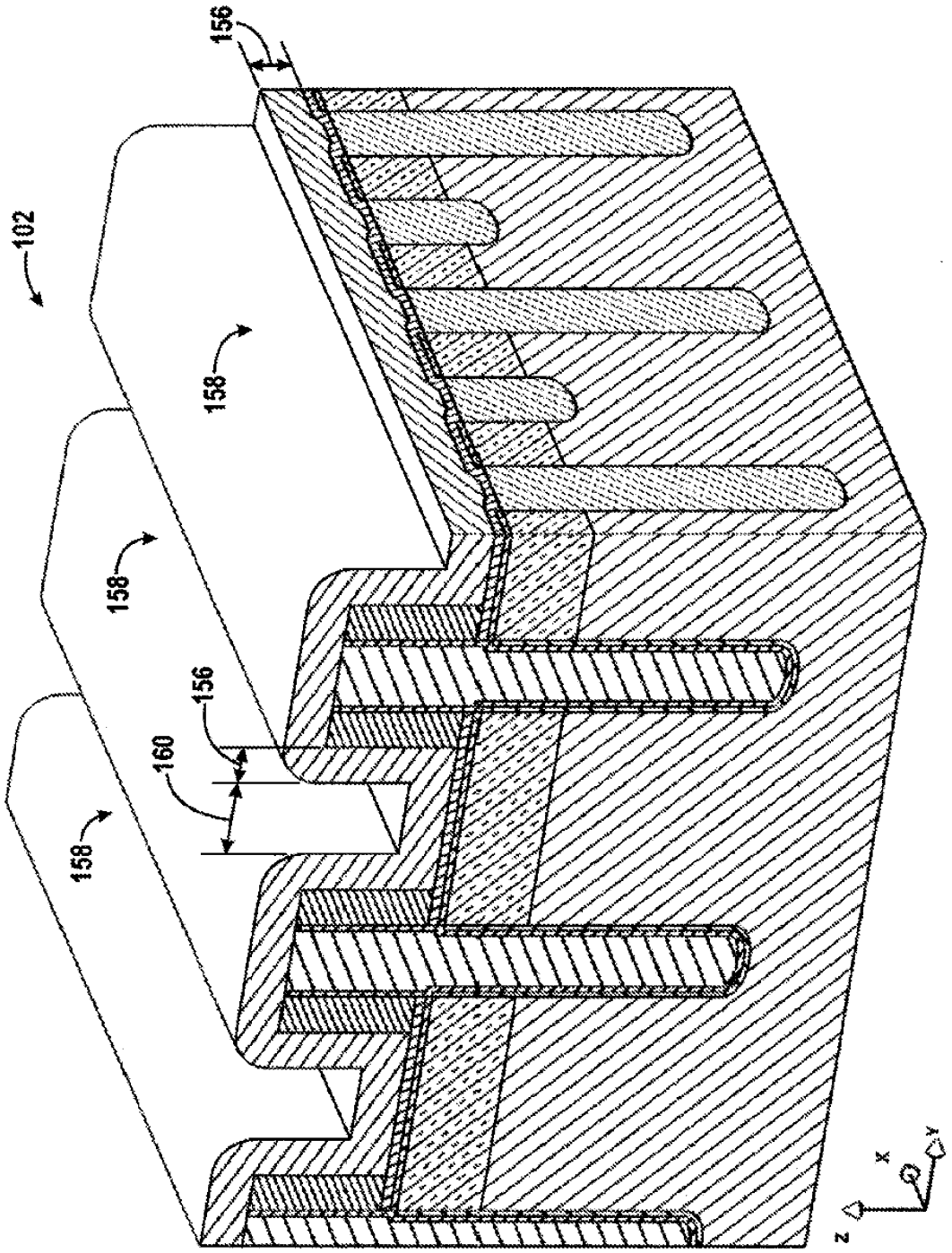


图 17

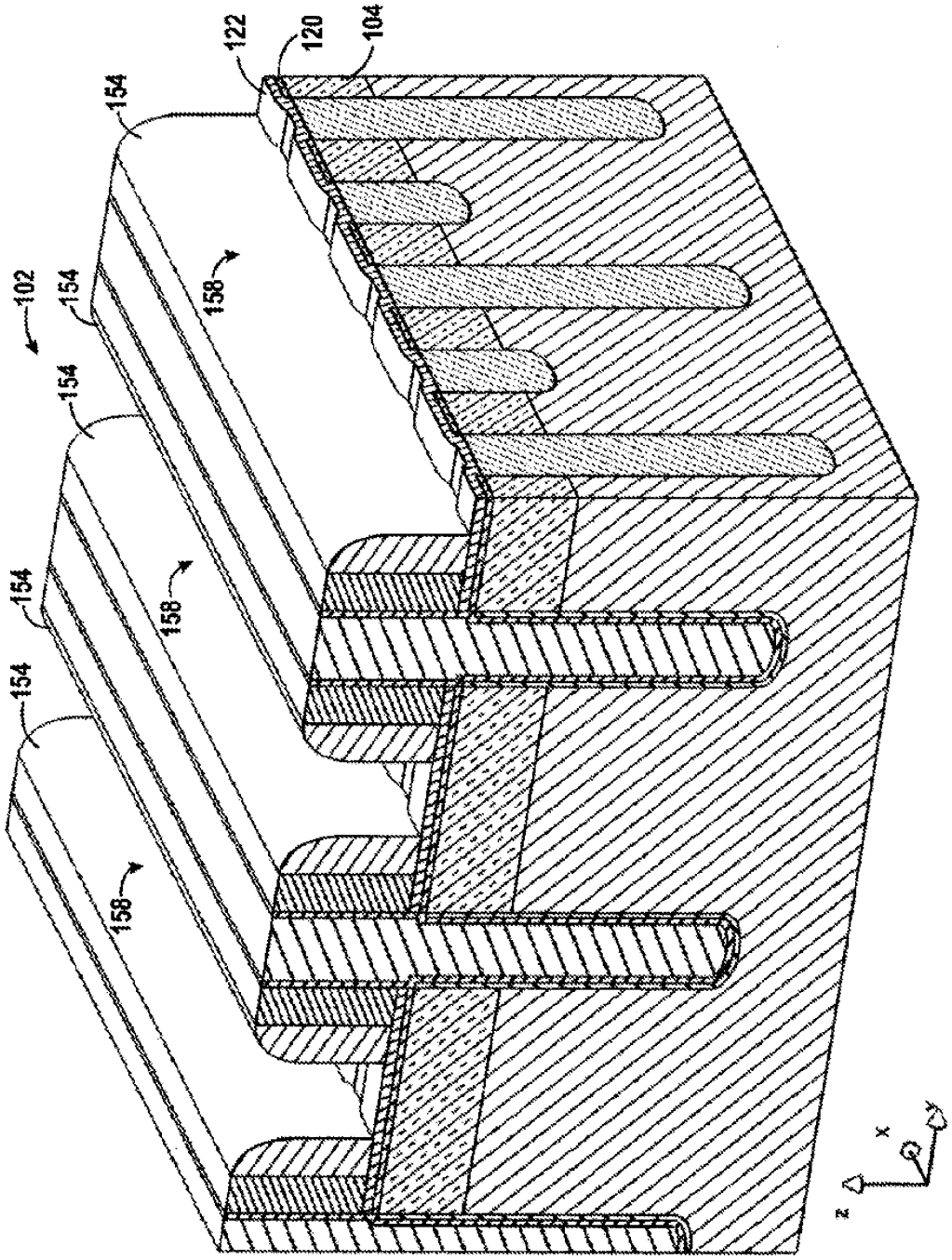


图 18

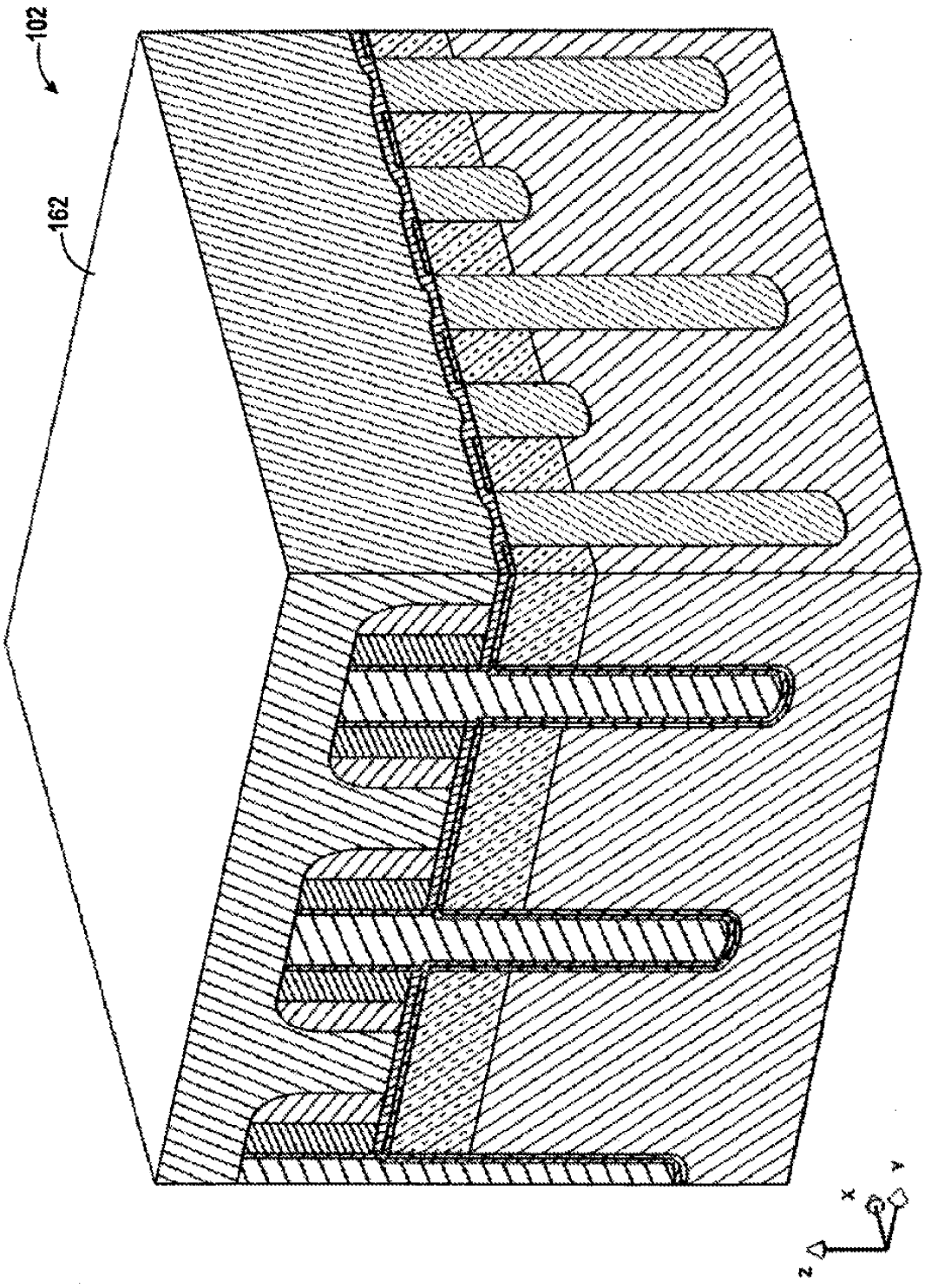


图 19

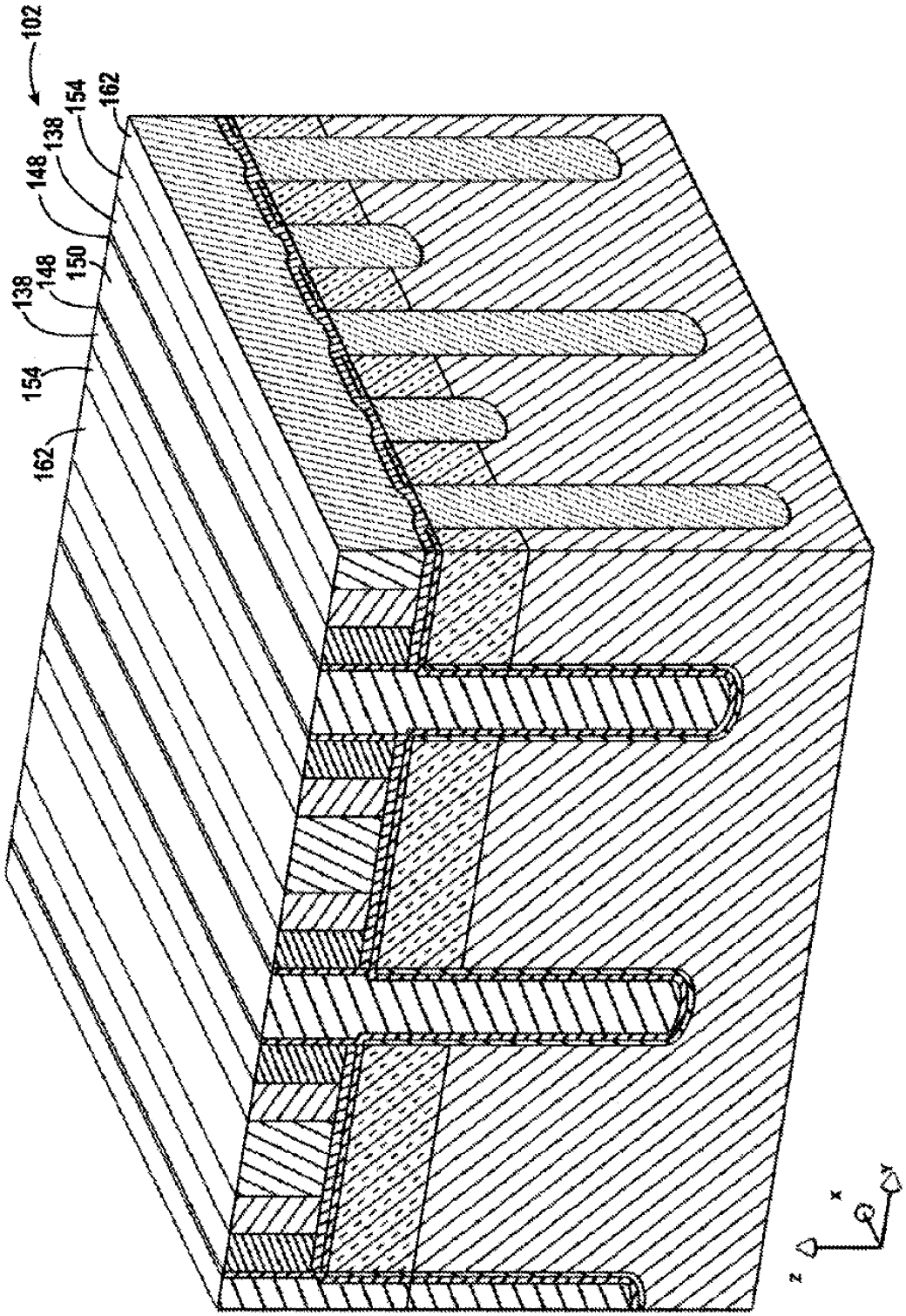


图 20

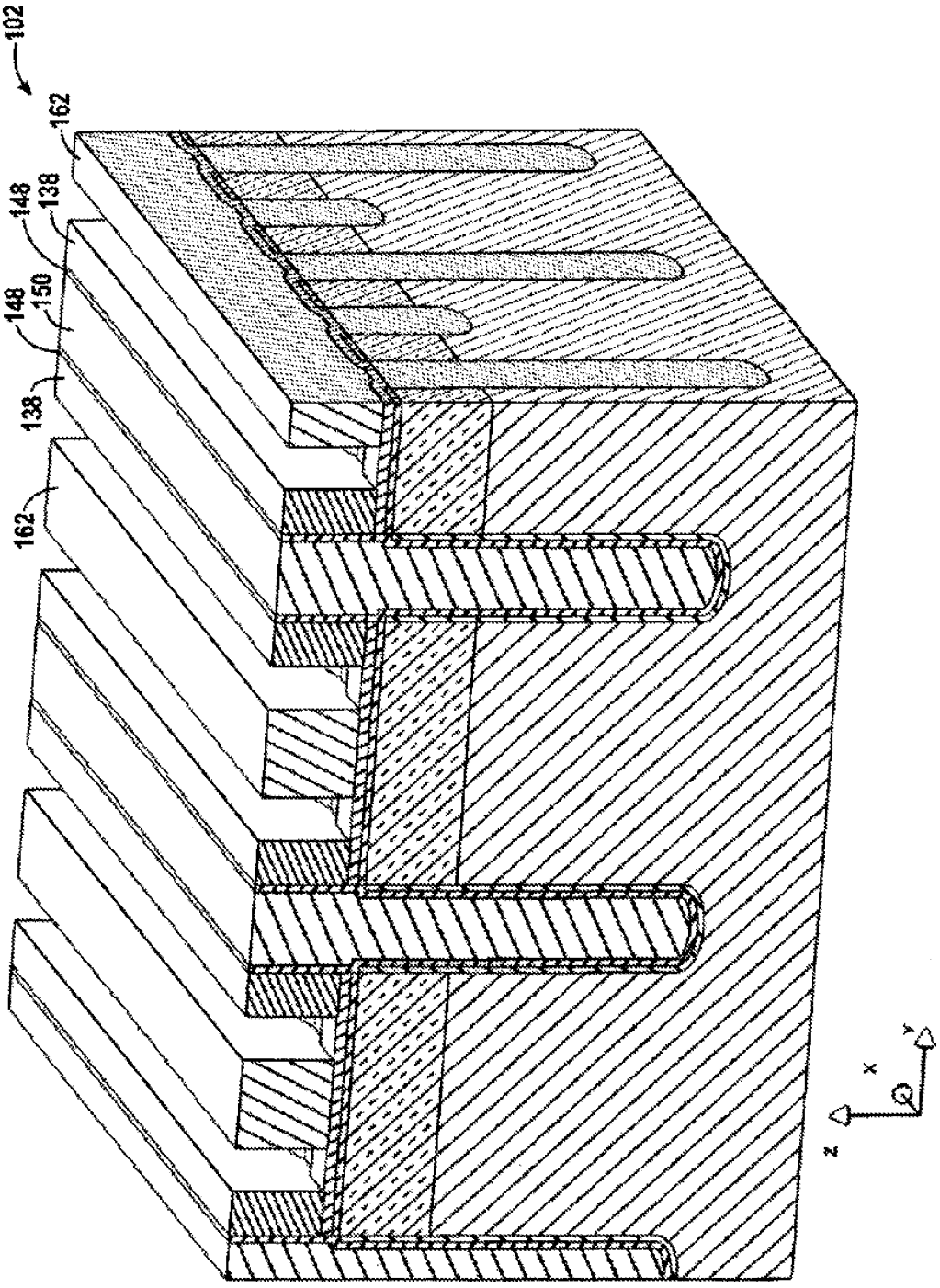


图 21

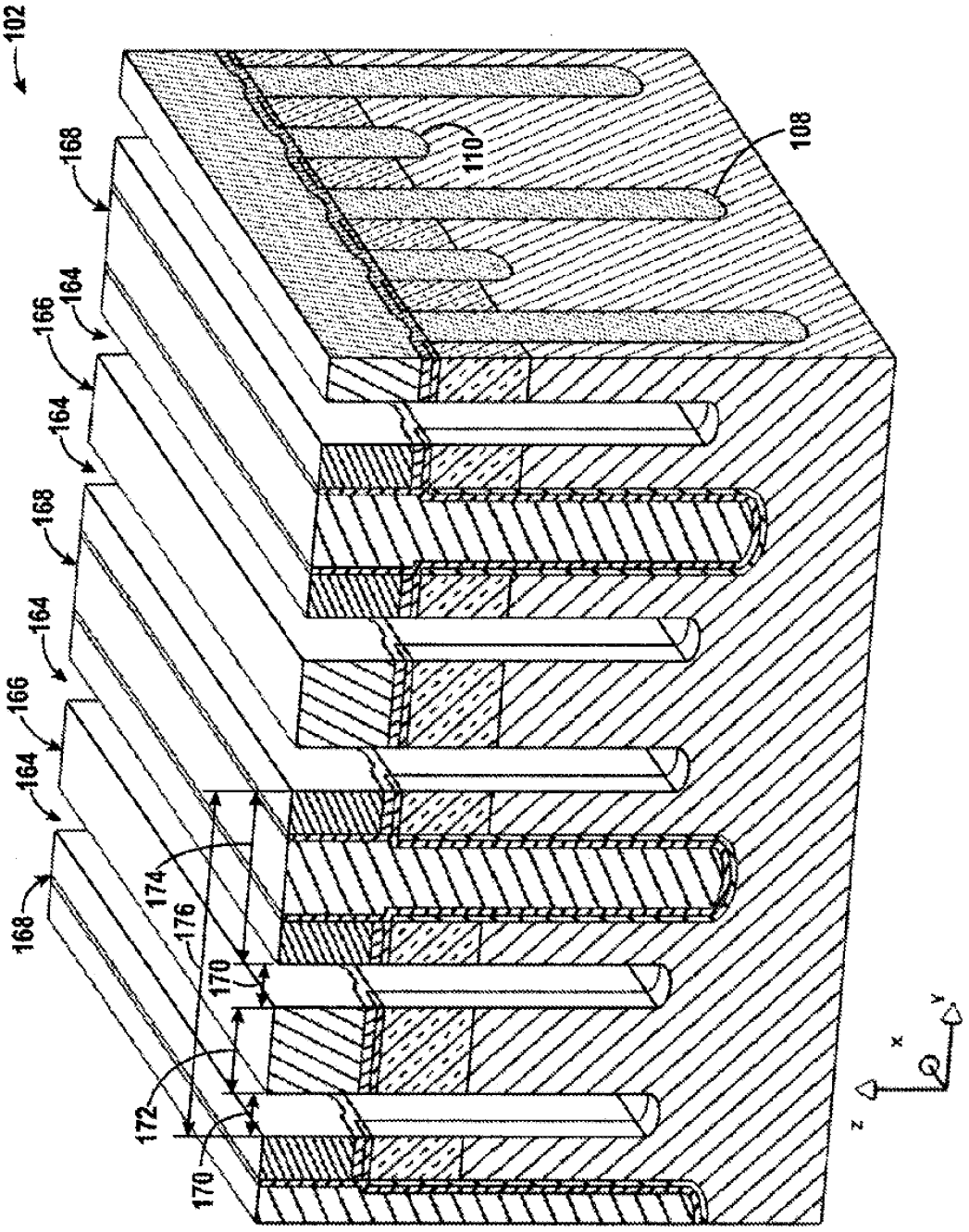

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图 22

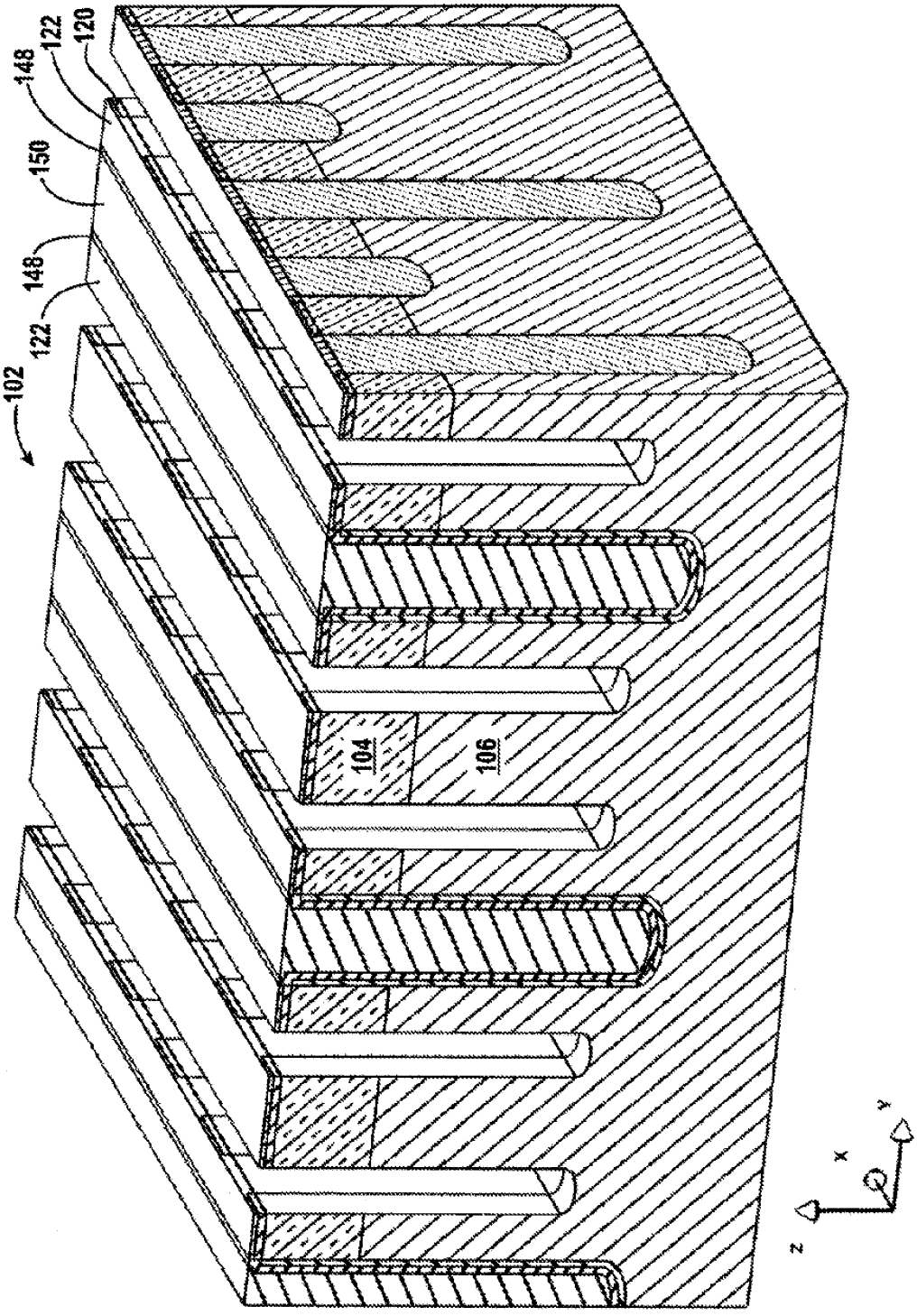


图 23

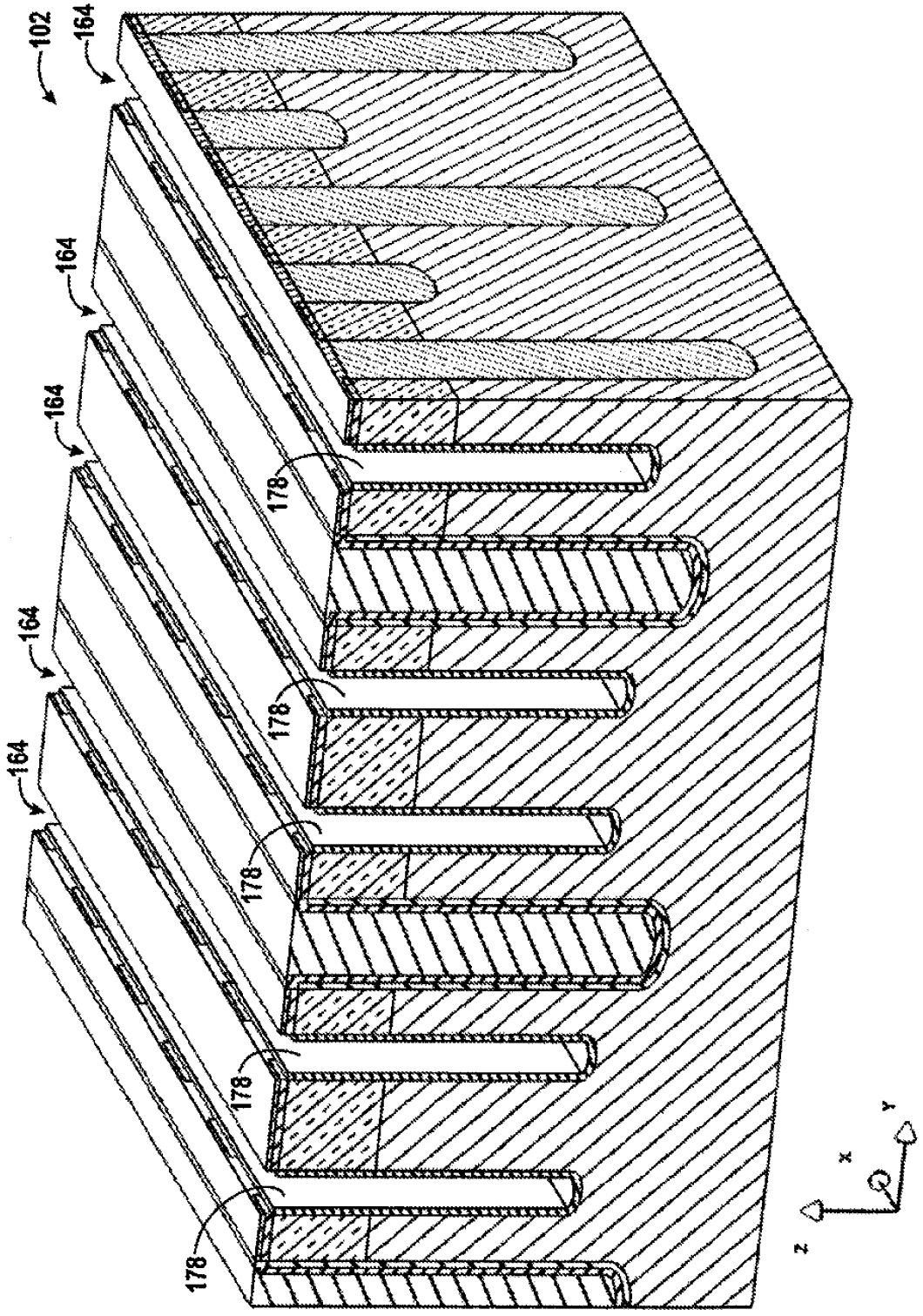


图 24

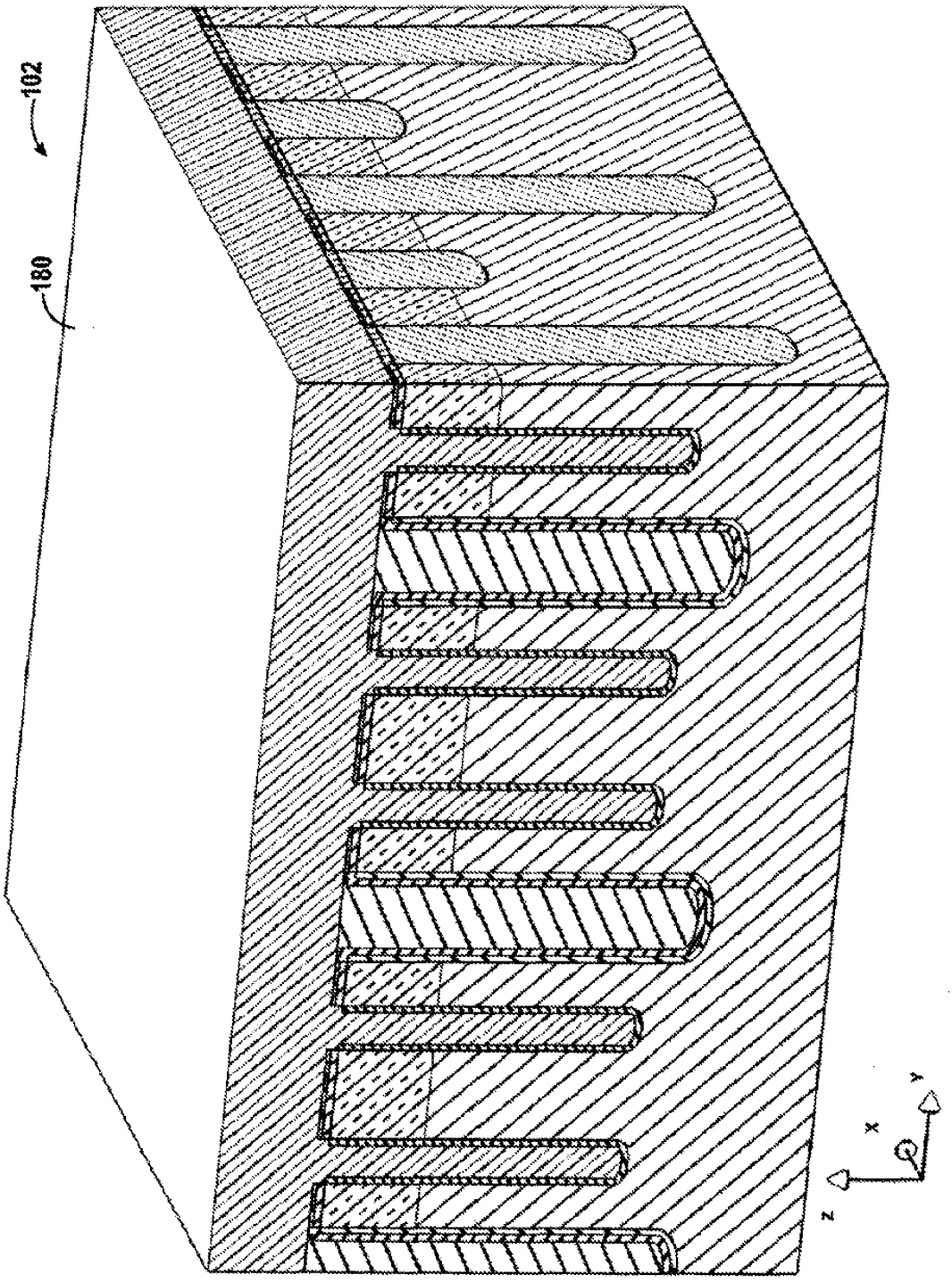


图 25

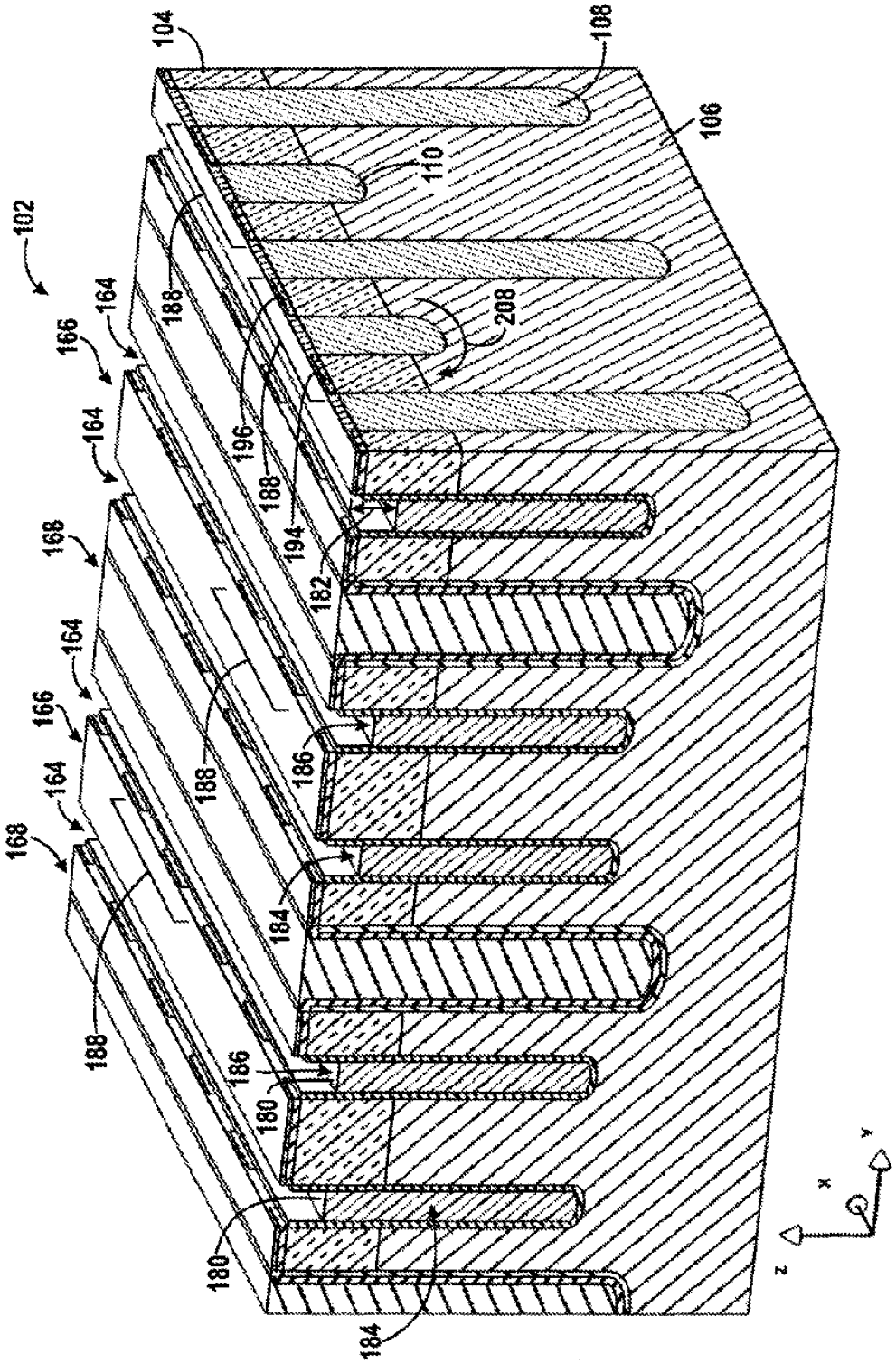

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188
186
184
188
186
180
180
184
x
y
z

图 26

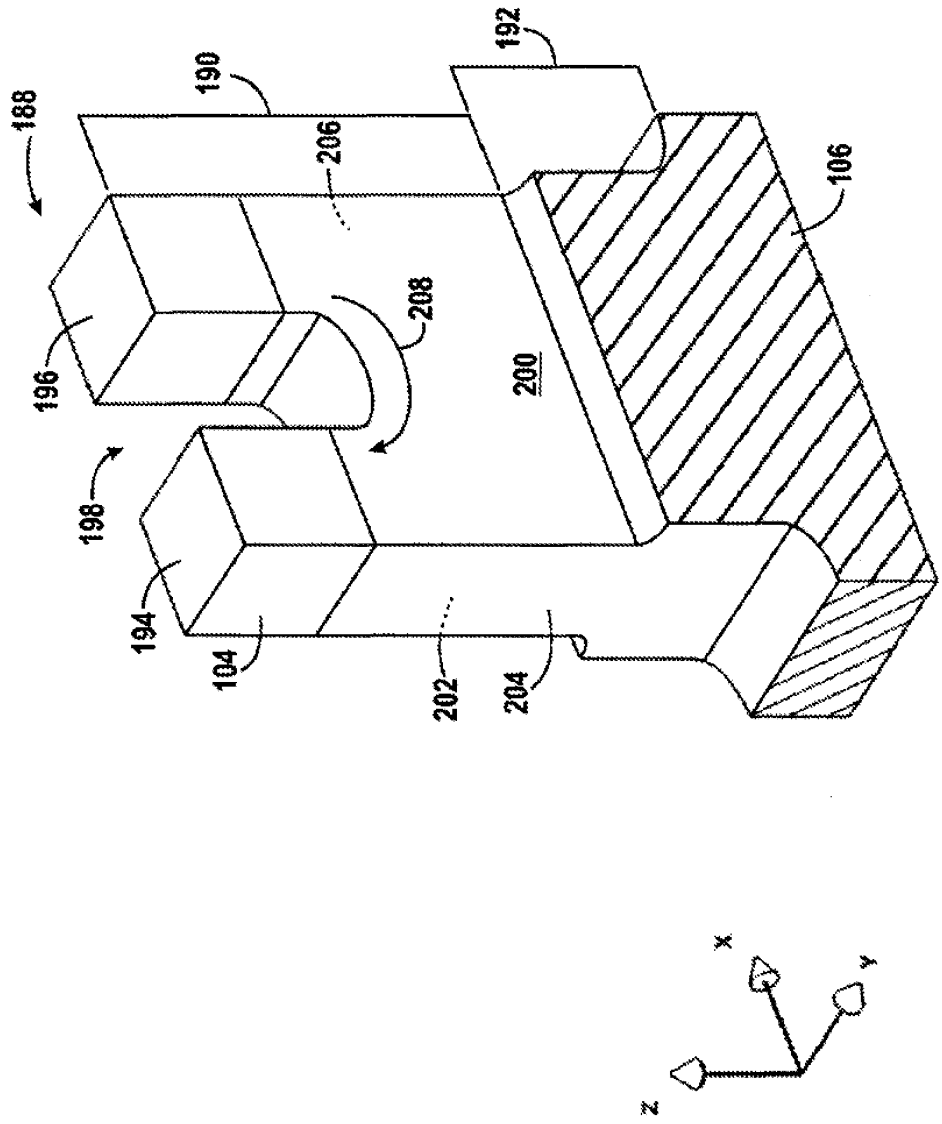


图 27

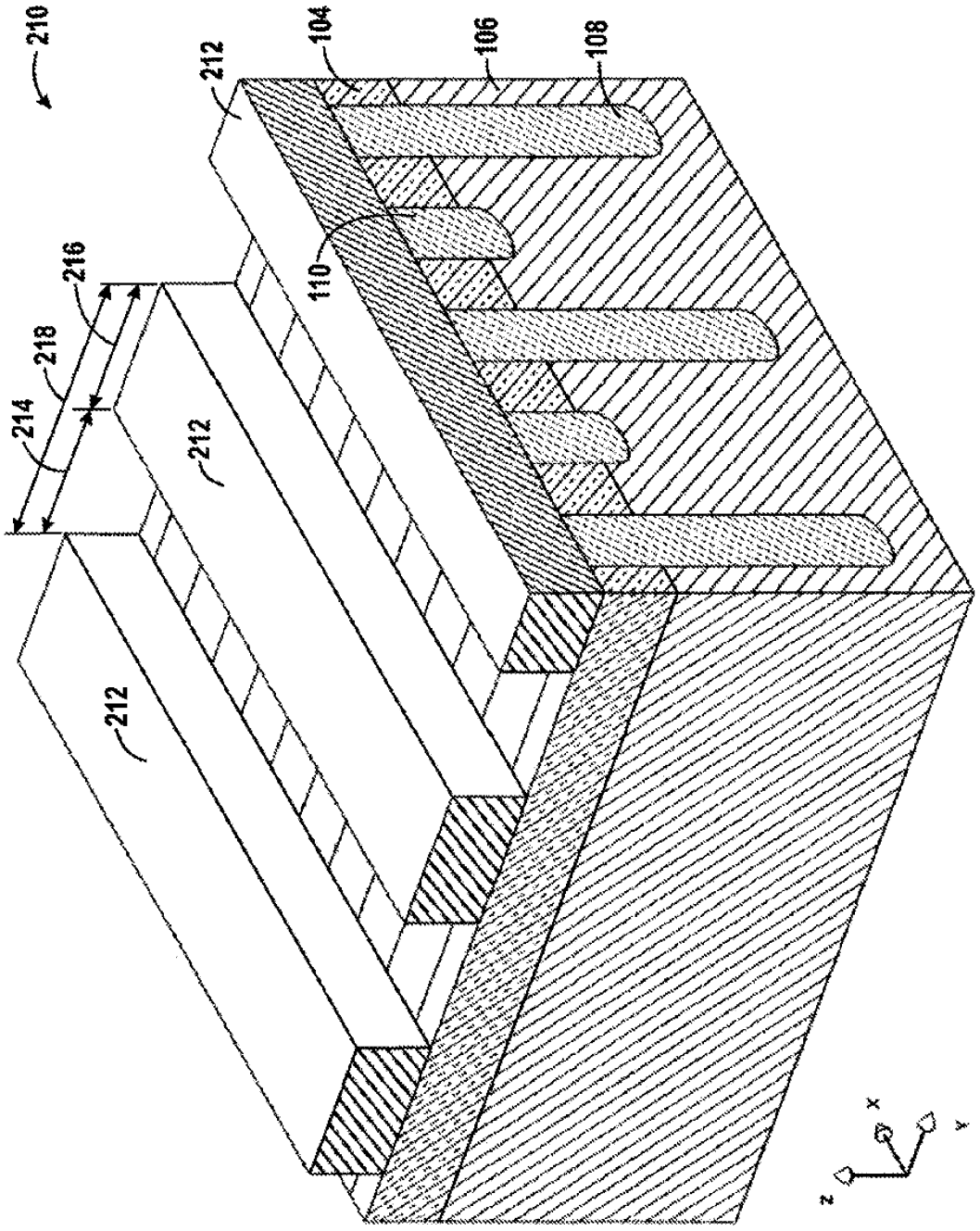


图 28

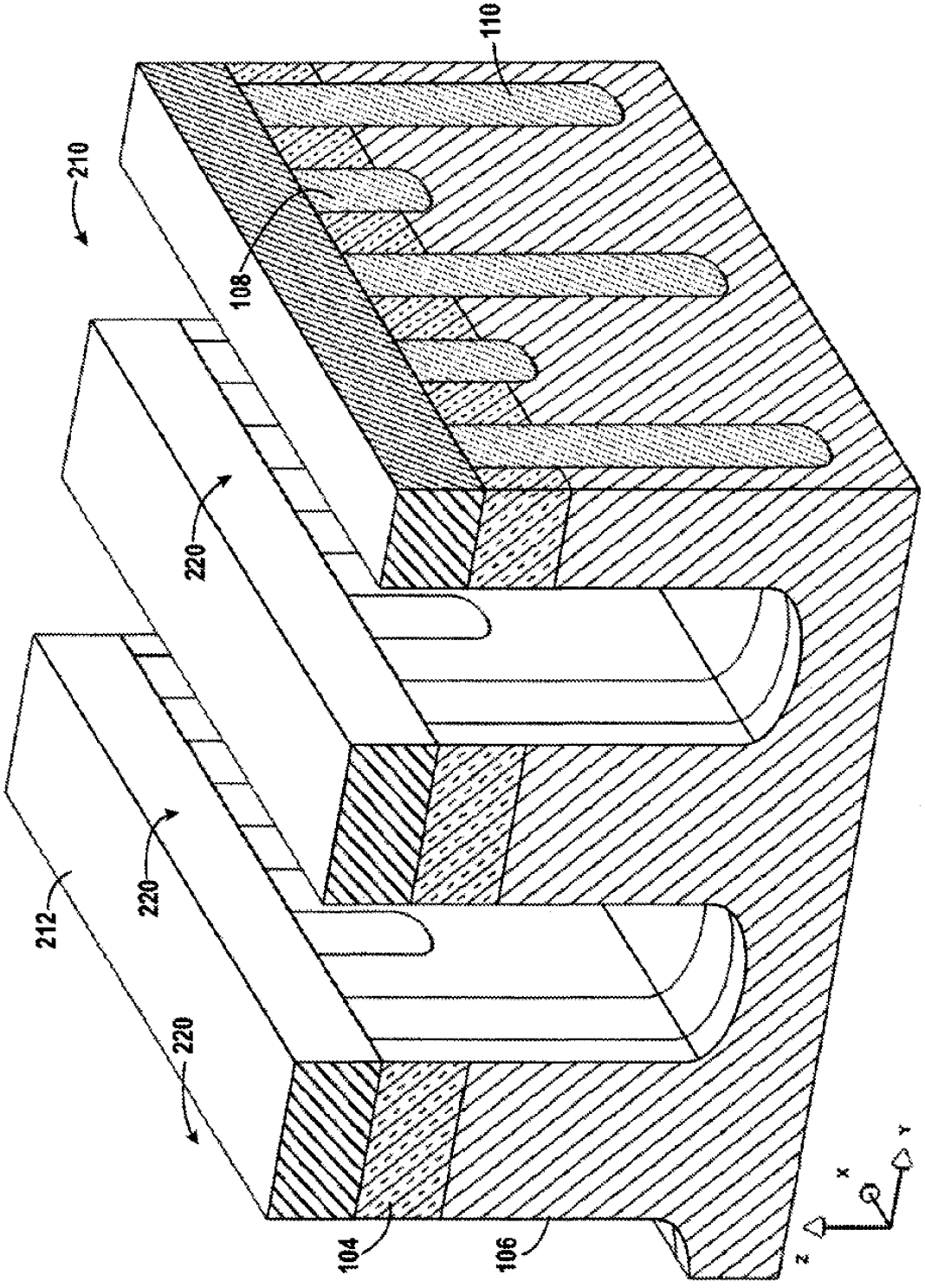


图 29

41

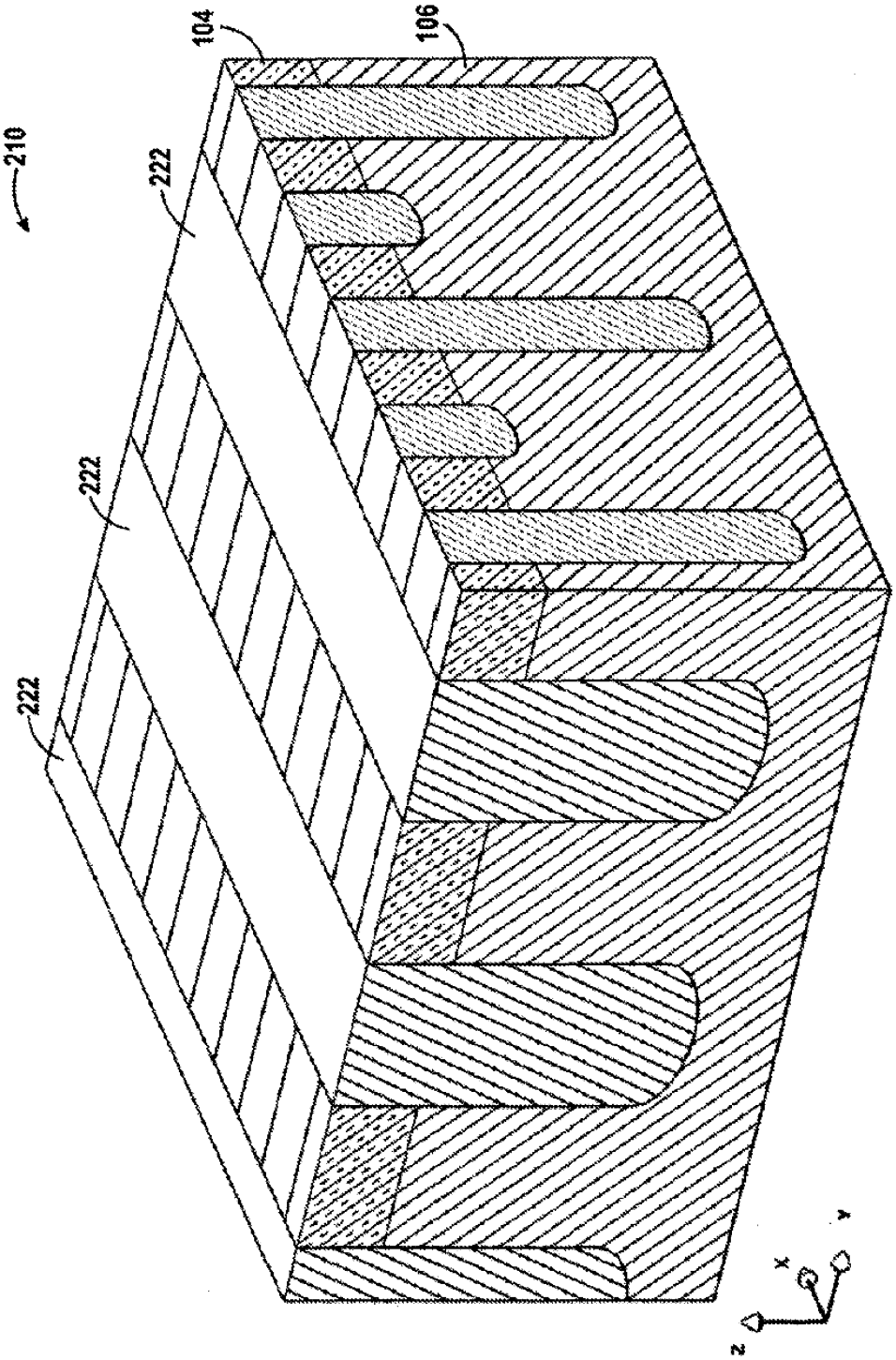


图 30

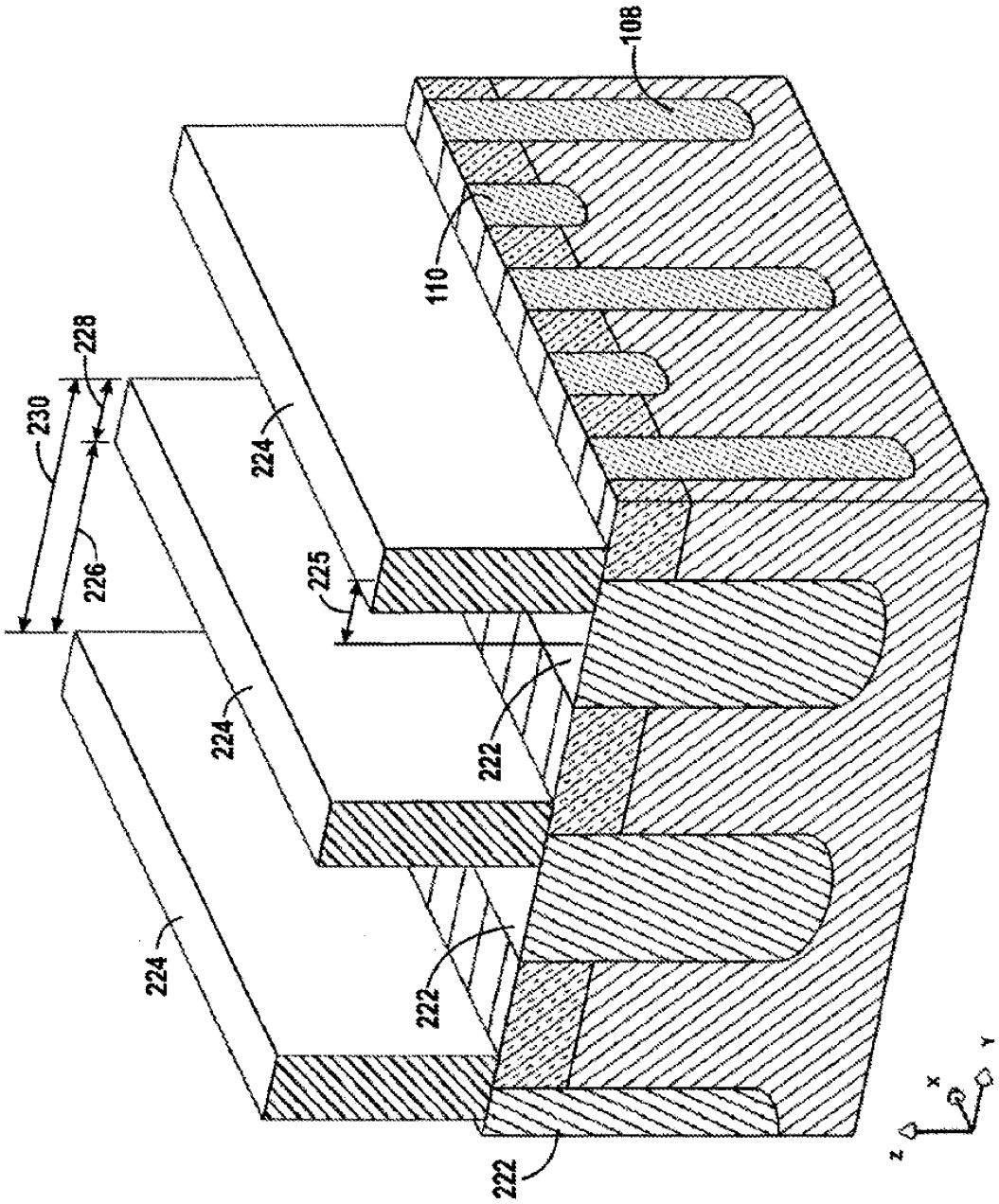


图 31

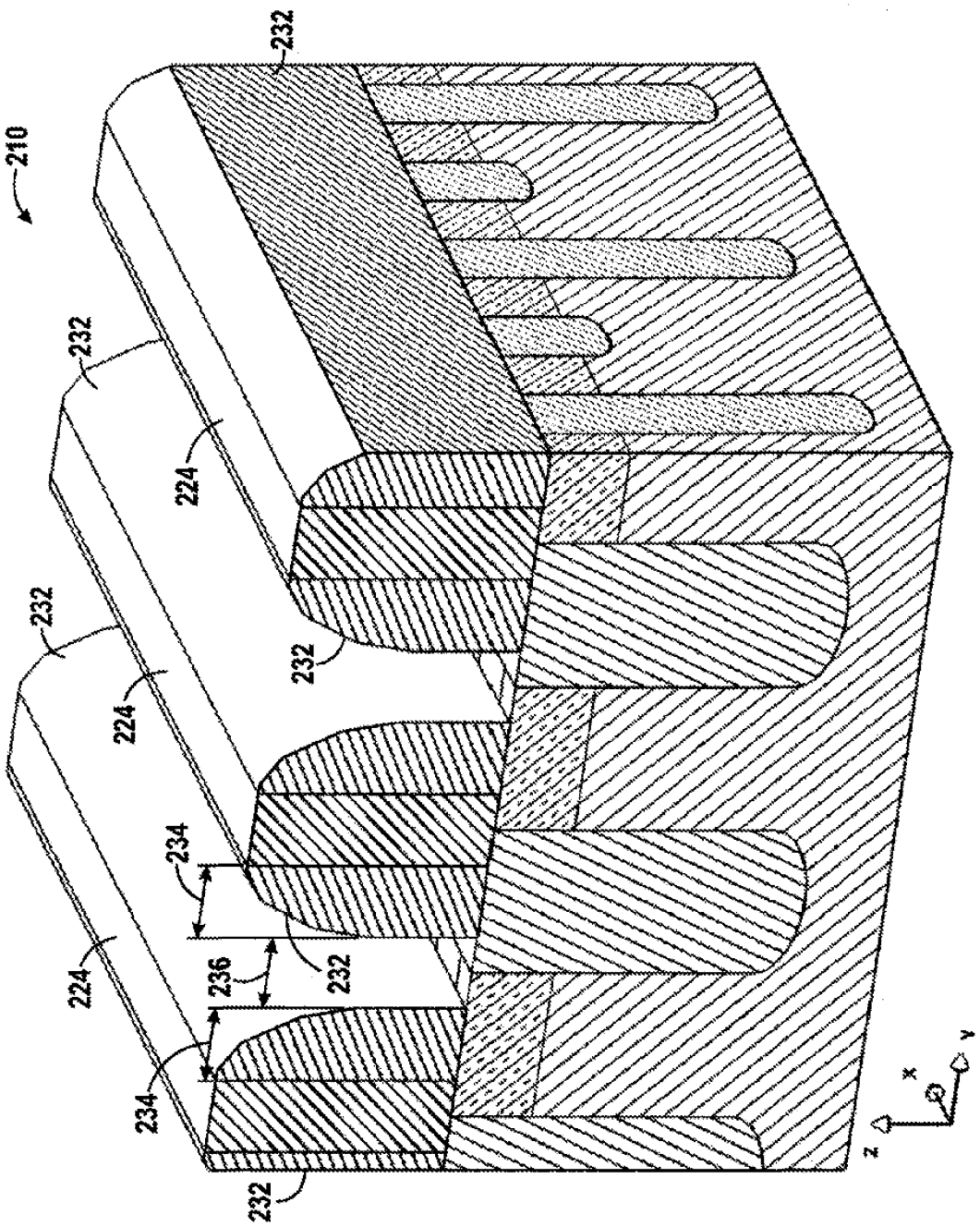


图 32

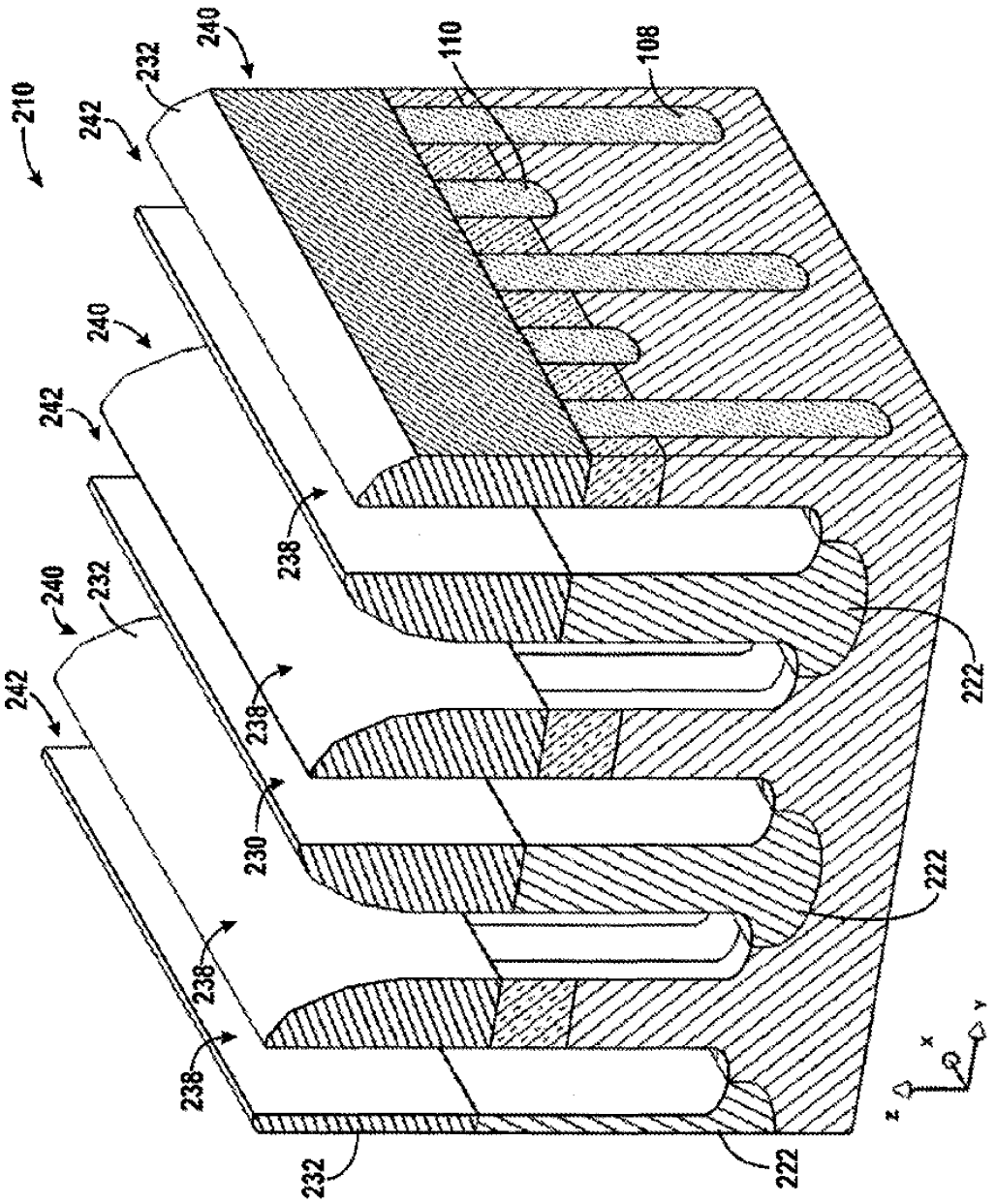

210
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238
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222
z
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y

图 33

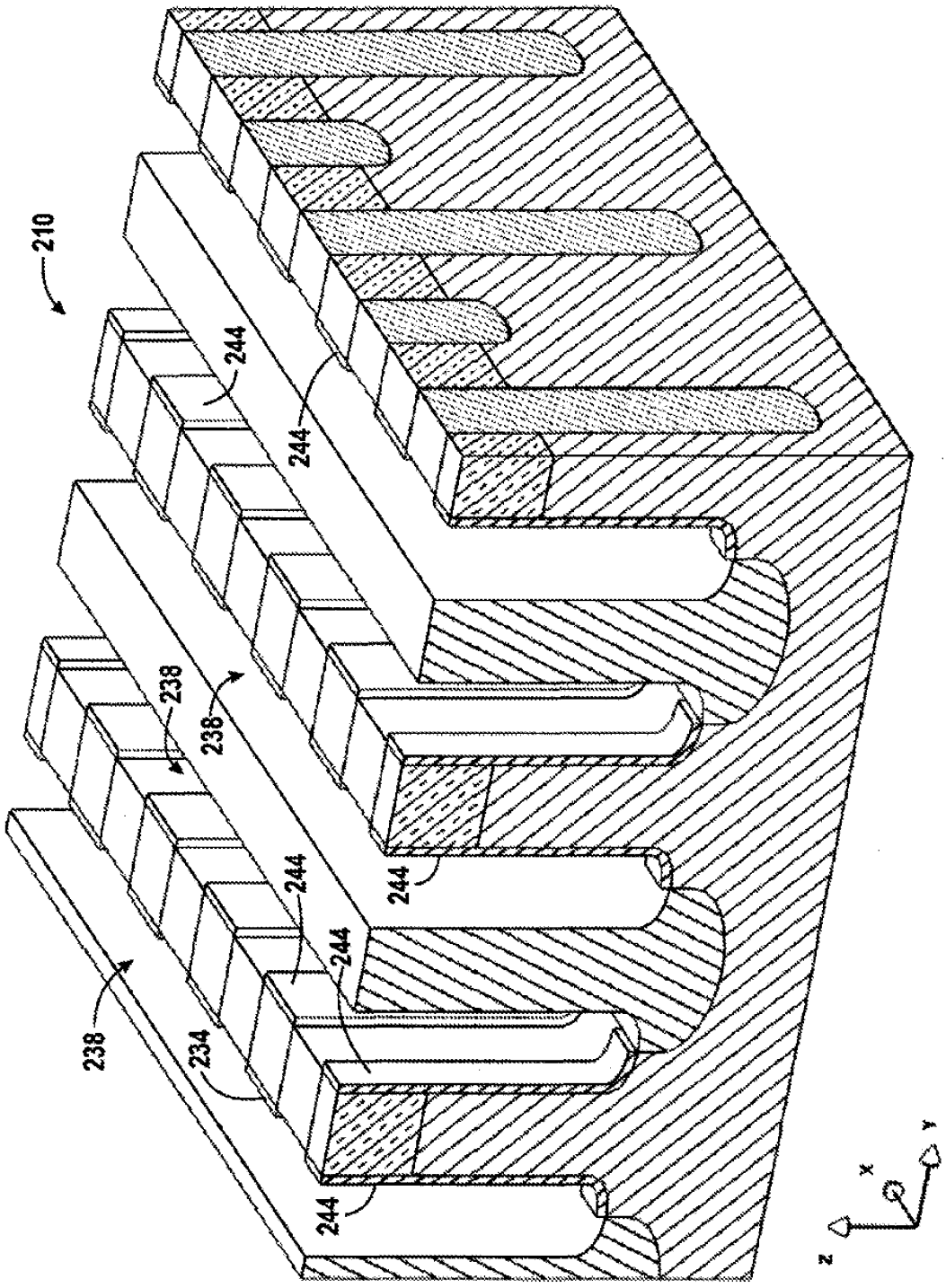


图 34

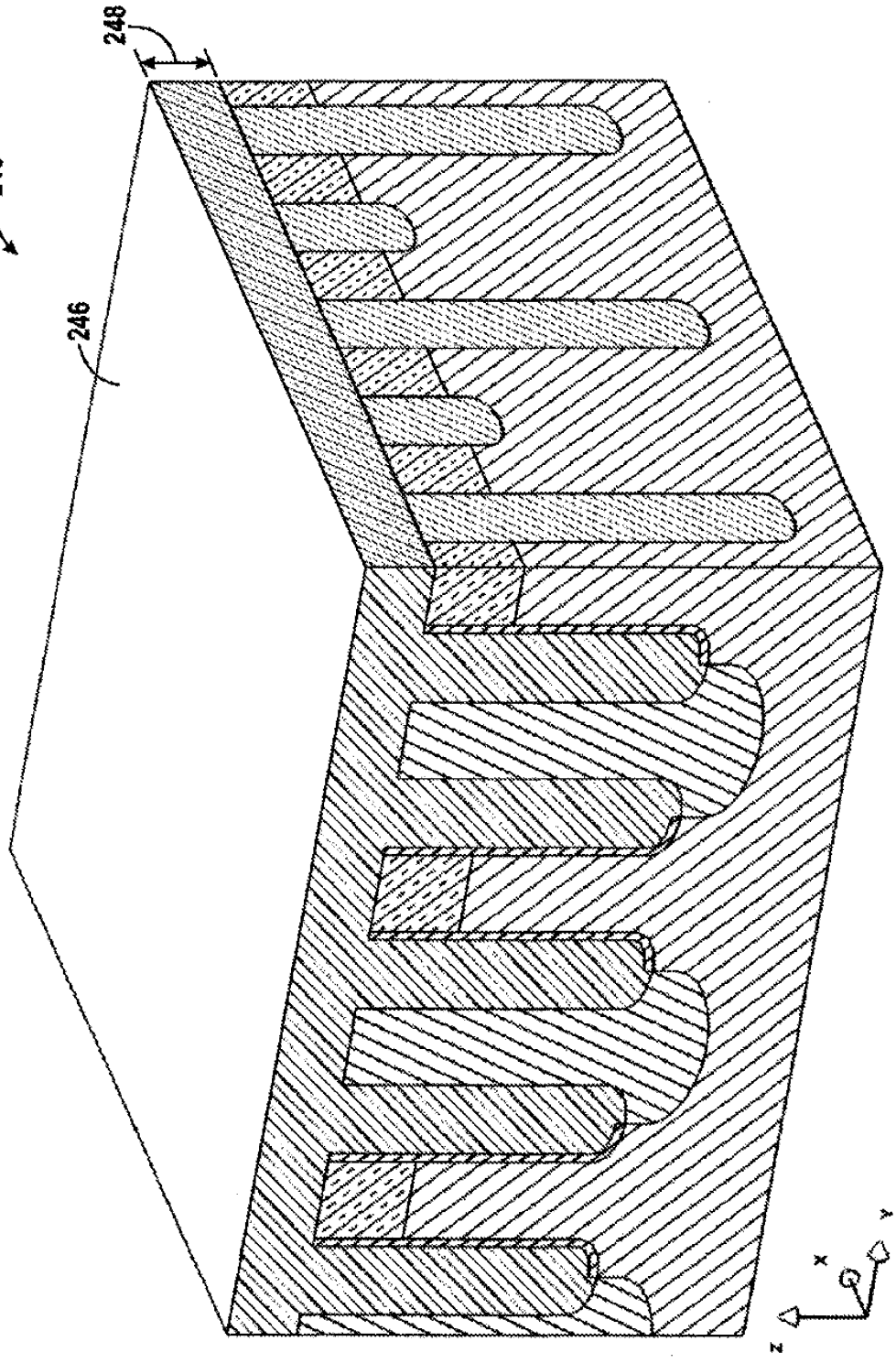


图 35

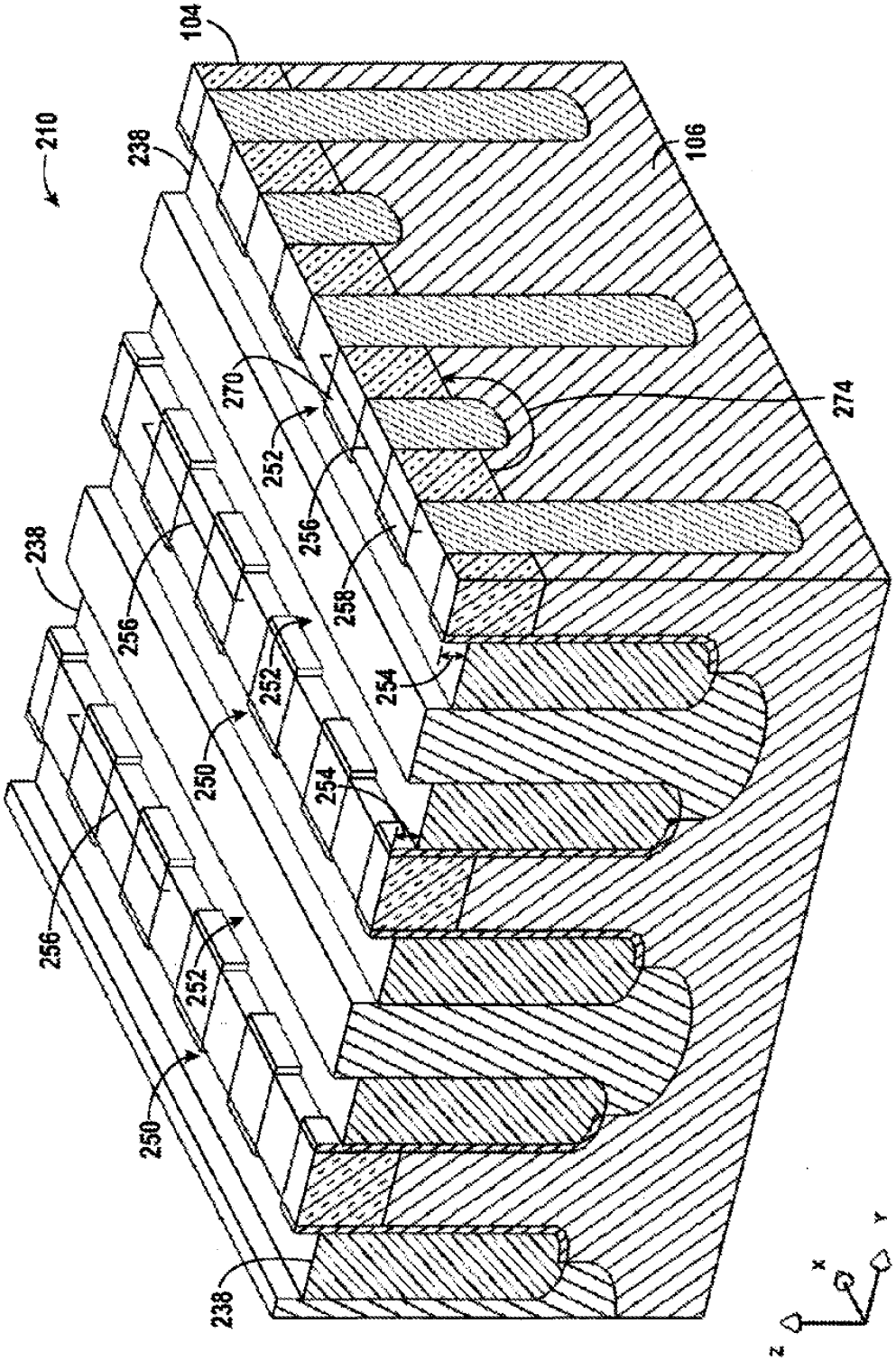


图 36

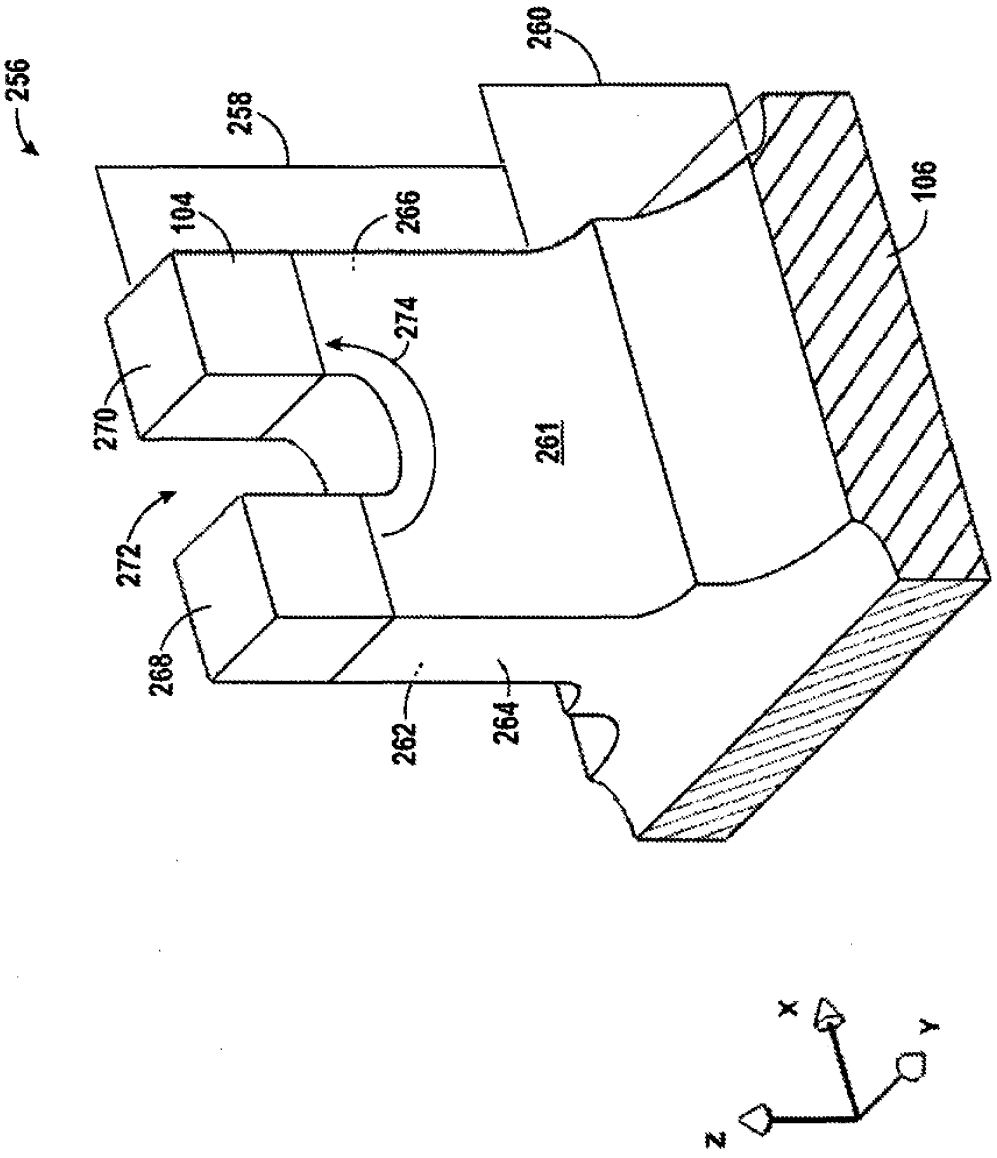


图 37

Espacenet

Bibliographic data: CN103137445 (A) — 2013-06-05

Method of forming finfet doping fins

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Classification: - international: *C30B25/02; H01L21/205; H01L21/336*
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Application number: CN20111398431 20111205 Global Dossier

Priority number (s): CN20111398431 20111205

Also published as: CN103137445 (B)

Abstract of CN103137445 (A)

The invention provides a method of forming finfet doping fins. The method comprises that a semiconductor substrate is provided, and a hard patterning mask is formed on the semiconductor substrate; a plurality of semiconductor lateral walls and grooves between two neighboring semiconductor lateral walls are formed after the semiconductor substrate is etched, and the hard patterning mask is removed; insulator oxide is formed in the grooves; the semiconductor lateral walls are etched to ensure that the heights of the semiconductor lateral walls are lower than the height of the insulator oxide; doped semiconductor fins grow on the tops of the etched semiconductor lateral walls in an epitaxial mode; and the insulator oxide is etched to ensure that the end surfaces of the tops of the insulator oxide are lower than the end surfaces of the tops of the semiconductor fins. Therefore, ion implantation doping needs not conducting on the semiconductor fins, doped fins are directly generated on the semiconductor substrate in an epitaxial mode, all the tops of the formed and doped semiconductor fins and all the lateral walls of the formed and doped semiconductor fins have evenly doping effect, and integral performance of finfet is improved.

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DESCRIPTION CN103137445

The present invention provides a method of forming a Finfet doped fin comprising providing a semiconductor substrate and forming a patterned hard mask on the semiconductor substrate; etching the semiconductor substrate to form a plurality of semiconductor sidewalls, and adjacent two semiconductors a trench between the sidewalls, removing the patterned hard mask; forming an insulator oxide in the trench; etching the sidewall of the semiconductor such that the sidewall height of the semiconductor is lower than the height of the insulating oxide; the sidewall of the semiconductor after etching The doped semiconductor fin is epitaxially grown on top; the insulator oxide is etched such that the top end of the insulator oxide is lower than the top end of the semiconductor fin. Therefore, instead of ion implantation doping of the semiconductor fins, the doped fins are directly epitaxially grown on the semiconductor substrate, and the formed doped semiconductor fins are uniform regardless of the top and side walls thereof. The doping effect improves the overall performance of the Finfet.

本发明提供了一种形成Finfet掺杂鳍状物的方法，包括提供半导体基底，并在半导体基底上形成图案化硬掩膜；刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除图案化硬掩膜；在沟槽内形成绝缘体氧化物；刻蚀半导体侧壁，使半导体侧壁高度低于绝缘氧化物高度；在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；刻蚀绝缘体氧化物，使绝缘体氧化物顶部端面低于半导体鳍状物的顶部端面。因此，不需要对半导体鳍状物进行离子注入掺杂，而是在半导体基底上直接外延生成掺杂了的鳍状物，形成的掺杂的半导体鳍状物无论其顶部和侧壁都具有均匀的掺杂效果，提高了Finfet的整体性能。

Method of forming Finfet doped fins

形成Finfet掺杂鳍状物的方法

Technical field

技术领域

Field of the Invention This invention relates to the field of semiconductor fabrication, and more particularly to a method of forming a doped fin in a Finfet transistor.

本发明涉及半导体制造领域，尤其涉及形成Finfet晶体管中掺杂鳍状物 (fin)的方法。

Background technique

背景技术

Field effect transistors (FETs) have long been the dominant semiconductor technology used to make products such as application-specific integrated circuit chips, static random access memory (SRAM) chips. With the increasing miniaturization of semiconductor devices, the short channel effect of FETs has become more serious. In order to solve the short channel effect such as when the FET enters the 22nm node, three-dimensional FETs such as Finfet (FinFET) have been developed. . Fig. 1a shows a schematic view showing the appearance of a Finfet on which a semiconductor oxide 1 is formed with an insulator oxide 3, a long and thin semiconductor fin 3 protruding from the insulator oxide 2, and a polysilicon gate 5 surrounding the three of the fins 3. On the side, the semiconductor fins 3 are doped, and source/drain regions (not shown) are formed at both ends of the fins 3, and the gate oxide 4 separates the polysilicon or metal gates 5 from the semiconductor fins 2 On, the polysilicon or metal gate 5 is capable of inducing a conductive channel on three sides of the semiconductor fin 3 when the Finfet is operating. Finfet has received wide attention due to its ability to avoid short channel effects and simple processes.

场效应晶体管(FET)一直是用来制造专用集成电路芯片、静态随机存 储器(SRAM)芯片等产品的主导半导体技术。随着半导体器件的日趋小型 化，FET短沟道效应愈发严重，为解决如当FET进入22nm节点后的短沟道 效应，进而发展出三维的FET，如Finfet(鳍片式场效应晶体管)。 图1a展 示出现有Finfet的结构示意图，半导体基底1上形成有绝缘体氧化物3，长 而薄的半导体鳍状物3从绝缘体氧化物2中突起，多晶硅栅极5包围鳍状物 3的三个侧面，将半导体鳍状物3掺杂，并在鳍状物3的两端生成源/漏极区 (未示出)，栅氧化物4将多晶硅或者金属栅极5与半导体鳍状物2隔开， 当Finfet工作时，多晶硅或者金属栅极5能够在半导体鳍状物3的三个侧面 上感应出导电沟道。 Finfet由于其能避免短沟道效应以及工艺简单而被广泛 关注。

Figure 1b shows a schematic view of the structure of the Finfet manufacturing process. In the Finfet fabrication, when forming a doped semiconductor fin, the usual process is as follows, providing a semiconductor substrate 1, such as a single crystal silicon substrate, and a single crystal silicon substrate. Forming a patterned SiN hard mask

6 on the first surface, etching the single crystal silicon substrate 1, forming a plurality of semiconductor sidewalls 8, and a high aspect ratio trench 7 between adjacent two semiconductor sidewalls 8 to be insulated The oxide 2 is deposited in the trench 7, and the height of the insulating oxide 2 is lower than the height of the trench 7, so that the semiconductor fin 3 is formed on the insulating oxide 2, and the SiN hard mask 6 is removed, The semiconductor fin 3 is doped with ion implantation. However, when ion implantation doping is performed on the semiconductor fin 3, the top of the semiconductor fin 3 and its side wall are made due to the random variation of the implanted ions and because the topography of the semiconductor fin 3 is strip-shaped. There is a difference in doping, as shown in Fig. 1c, uneven doping may result in deterioration of the overall performance of the Finfet. Therefore, the doping uniformity of the Finfet fin is an urgent problem to be solved in the manufacture of Finfet.

图1b显示了Finfet制造过程中的结构示意图，在进行Finfet制造中，形 成掺杂的半导体鳍状物时，常用的过程如下，提供半导体基底1，如单晶硅 基底，并在单晶硅基底1上形成图案化的SiN硬掩膜6，刻蚀单晶硅基底1， 形成多个半导体侧壁8，以及相邻两个半导体侧壁8之间的高纵深比的沟槽7，将绝缘氧化物2沉积于沟槽7中，且绝缘氧化物2的高度低于沟槽7的高度， 因此，即在绝缘氧化物2上形成了半导体鳍状物3，去除SiN硬掩膜6，对 半导体鳍状物3进行离子注入掺杂。 然而，当对半导体鳍状物3进行离子注 入掺杂时，由于注入离子的随机变化，并且由于半导体鳍状物3的形貌为条 状，就会使得半导体鳍状物3的顶部与其侧壁存在掺杂差异，如图1c所示， 不均匀的掺杂会导致Finfet整体性能的变差，因此，Finfet鳍状物的掺杂均 匀性是现在Finfet制造时亟待解决的问题。

Summary of the invention

发明内容

The invention provides a method for forming a Finfet doped fin, which solves the problem of poor uniformity of doping when the existing Finfet fin is doped by ion implantation.

本发明提供了一种形成Finfet掺杂鳍状物的方法，解决现有Finfet鳍状 物进行离子注入掺杂时，掺杂均匀性差的问题。

The technical means adopted by the present invention are as follows: A method for forming a Finfet doped fin, comprising:

本发明采用的技术手段如下：一种形成Finfet掺杂鳍状物的方法，包括：

Providing a semiconductor substrate and forming a patterned hard mask on the semiconductor substrate;

提供半导体基底，并在所述半导体基底上形成图案化硬掩膜；

Etching the semiconductor substrate to form a plurality of semiconductor sidewalls, and trenches between adjacent two semiconductor sidewalls, removing the patterned hard mask;

刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的 沟槽，去除所述图案化硬掩膜；

Forming an insulator oxide in the trench, the insulator oxide having a height equal to the trench height;

在所述沟槽内形成绝缘体氧化物，所述绝缘体氧化物高度等于所述沟槽高 度；

Etching the semiconductor sidewall such that the semiconductor sidewall height is lower than the insulating oxide height;

刻蚀所述半导体侧壁，使所述半导体侧壁高度低于所述绝缘氧化物高度；

Epitaxially growing a doped semiconductor fin on top of the etched semiconductor sidewall;

在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；

The insulator oxide is etched such that the top end of the insulator oxide is lower than the top end surface of the semiconductor fin.

刻蚀所述绝缘体氧化物，使所述绝缘体氧化物顶部端面低于所述半导体鳍状 物的顶部端面。

Further, the semiconductor substrate material is single crystal silicon, and the insulator oxide material is SiO2; wherein, the semiconductor sidewall is wet-etched, and the etchant is NH3 H2O or tetramethylammonium hydroxide; The insulator oxide is wet etched, and the etchant is a diluted HF solution.

进一步，所述半导体基底材料为单晶硅，所述绝缘体氧化物材料为SiO2；其 中，利用湿法刻蚀所述半导体侧壁，刻蚀剂为NH3 H2O或者四甲基氢氧化铵； 利用湿法刻蚀所述绝缘体氧化物，刻蚀剂为稀释的HF溶液。

Further, the epitaxially grown semiconductor fin is one of SiB, SiGe, SiC, SiP, SiAs, SiGeB, SiCB, GaN, InAs, InP.

进一步，所述外延生长的所述半导体鳍状物为SiB，SiGe，SiC，SiP，SiAs，SiGeB，SiCB，GaN，InAs，InP之一。

Further, the atomic ratio of Si to Ge in the SiGe is from 20:1 to 6:4.

进一步，所述SiGe中Si与Ge的原子比为20：1至6：4。

Further, the concentration of B in the SiB, SiGeB, and SiBi is 10<14> to 8×10<21>atoms/cm<3>.

进一步，所述SiB，SiGeB，SiCB中B的浓度为10<14>至8×10<21>atoms/cm<3>。

Further, the atomic ratio of Si to C in the SiC is from 100:1 to 20:1.

进一步，所述SiC中Si与C的原子比为100：1至20：1。

According to the method provided by the present invention, ion doping doping is not required for the semiconductor fin, but the doped fin is directly epitaxially grown on the semiconductor substrate, and thus the semiconductor fin thus formed is regardless of its top and The sidewalls have a uniform doping effect, which improves the overall performance of the Finfet.

依据本发明提供的方法，不需要对半导体鳍状物进行离子注入掺杂，而 是在半导体基底上直接外延生成掺杂了的鳍状物，因此，如此生成的半导体 鳍状物无论其顶部和侧壁都具有均匀的掺杂效果，提高了Finfet的整体性能。

DRAWINGS

附图说明

Figure 1a is a schematic view of the structure of Finfet;

图1a为Finfet的结构示意图；

Figure 1b is a schematic structural view of the Finfet manufacturing process;

图1b为Finfet制造过程中的结构示意图；

Figure 1c is a schematic diagram of ion implantation doping of a semiconductor fin of Finfet;

图1c为对Finfet的半导体鳍状物进行离子注入掺杂的示意图；

2 is a flow chart of a method for forming a Finfet doped fin according to the present invention;

图2为本发明一种形成Finfet掺杂鳍状物的方法流程图；

3a-3d are schematic diagrams showing the structure of a Finfet doped fin according to the present invention.

图3a～图3d为本发明制作Finfet掺杂鳍状物的流程结构示意图。

Detailed ways

具体实施方式

The principles and features of the present invention are described with reference to the accompanying drawings, which are intended to illustrate the invention and not to limit the scope of the invention.

以下结合附图对本发明的原理和特征进行描述，所举实例只用于解释本 发明，并非用于限定本发明的范围。

The present invention provides a method of forming a Finfet doped fin, as shown in Figure 2, comprising the following steps:

本发明提供了一种形成Finfet掺杂鳍状物的方法，如图2所示，包括如 下步骤：

Providing a semiconductor substrate and forming a patterned hard mask on the semiconductor substrate;

提供半导体基底，并在所述半导体基底上形成图案化硬掩膜；

Etching the semiconductor substrate to form a plurality of semiconductor sidewalls, and trenches between adjacent two semiconductor sidewalls, removing the patterned hard mask;

刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除所述图案化硬掩膜；

Forming an insulator oxide in the trench;

在所述沟槽内形成绝缘体氧化物；

Etching the semiconductor sidewall such that the semiconductor sidewall height is lower than the insulating oxide height;

刻蚀所述半导体侧壁，使所述半导体侧壁高度低于所述绝缘氧化物高度；

Epitaxially growing a doped semiconductor fin on top of the etched semiconductor sidewall;

在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；

The insulator oxide is etched such that the top end of the insulator oxide is lower than the top end surface of the semiconductor fin.

刻蚀所述绝缘体氧化物，使所述绝缘体氧化物顶部端面低于所述半导体鳍状物的顶部端面。

The process of making a Finfet doped fin of the present invention is described in detail below with reference to Figures 3a - 3d.

以下结合附图3a～3d详细描述本发明制作Finfet掺杂鳍状物的方法过程。

As shown in FIG. 3a, a semiconductor substrate 11 is provided. The material of the semiconductor substrate 11 is generally a single crystal silicon material. A patterned hard mask 14 is formed on the semiconductor substrate 11. The hard mask 14 is generally SiN, patterned hard mask. 14 is a long, thin strip.

如图3a所示，提供半导体基底11，半导体基底11的材料一般为单晶硅 材料，在半导体基底11上形成图案化的硬掩膜14，硬掩膜14一般为SiN，图案化硬掩膜14为长而薄的条状。

The semiconductor substrate 11 is etched through the hard mask 14, a plurality of semiconductor sidewalls 13 and trenches 15 between the sidewalls 13 are formed; an insulator oxide 12 is formed in the trenches 15, and the insulator oxide 12 material is preferably SiO2.

通过硬掩膜14刻蚀半导体基底11，形成多个半导体侧壁13，以及侧壁13之间的沟槽15；在沟槽15中形成绝缘体氧化物12，绝缘体氧化物12材 料优选为SiO2。

Referring to FIG. 3b, the hard mask 14 is removed, and a portion of the semiconductor sidewall 13 is removed by wet etching, preferably with NH3.H2O or tetramethylammonium hydroxide as the etchant, since the material of the semiconductor sidewall 13 is monocrystalline silicon. The insulator oxide 12 is SiO2, NH3.H2O or tetramethylammonium hydroxide is an etchant which is inert to SiO2 and has an etching effect only on the single crystal silicon, so that the etched semiconductor can be made after etching. The top end surface of the sidewall 13' is lower than the top end surface of the insulating oxide 12 even if the semiconductor sidewall 13 is recessed;

参照图3b，去除硬掩膜14，利用湿法刻蚀去除部分半导体侧壁13，优 选以NH3 H2O或者四甲基氢氧化铵为刻蚀剂，由于半导体侧壁13的材料为 单晶硅，绝缘体氧化物12为SiO2，NH3 H2O或者四甲基氢氧化铵为刻蚀剂 相对于SiO2为惰性，只对单晶硅具有刻蚀作用，因而、刻蚀后可使得刻蚀后的半导体侧壁13’的顶部端面低于绝缘氧化物12的顶部端面，即使半导体侧 壁13凹陷；

Doped semiconductor fins 14 are epitaxially grown on top of the etched semiconductor sidewalls 13', as shown in FIG. 3c, wherein the doped semiconductor fins may be SiB, SiGe, SiC, SiP, One of SiAs, SiGeB, SiCB, GaN, InAs, InP, etc., and preferably, the atomic ratio of Si to Ge in SiGe is 20:1 to 6:4, and the concentration of B in SiB, SiGeB, and SiCB is 10< 14> to 8×10<21>atoms/cm<3>, the atomic ratio of Si to C in SiC is from 100:1 to 20:1; as a technical means well known to those skilled in the art, how to epitaxially grow doping The semiconductor fin 14 is not limited, and an appropriate epitaxial growth parameter can be selected according to the specific situation when implemented.

在刻蚀后的半导体侧壁13’的顶部外延生长掺杂的半导体鳍状物14，如 图3c所示，其中，掺杂的半导体鳍状物的材料可以是SiB，SiGe，SiC，SiP， SiAs，SiGeB，SiCB，GaN，InAs，InP等中的一种，且优选的、SiGe中Si与 Ge的原子比为20：1至6：4，SiB，SiGeB，SiCB中B的浓度为10<14>至8×10<21>atoms/cm<3>，SiC中Si与C的原子比为100：1至20：1；作为本领域技术人 员公知的技术手段，对如何外延生长掺杂的半导体鳍状物14不做限定，在实 现时可根据具体情况选择合适的外延生长参数。

As shown in FIG. 3d, after the epitaxially grown doped semiconductor fins 14, the insulator oxide 12 is wet etched, preferably the etchant is a diluted HF solution, since the HF solution is inert to Si, The insulator oxide 12 made of SiO2 may be optionally removed, and thus, the top end face of the insulator oxide may be made lower than the top end face of the semiconductor fin, such that the doped semiconductor fin 14 is exposed to the surface of the insulator oxide.

如图3d所示，在外延生长了掺杂的半导体鳍状物14后，对绝缘体氧化 物12进行湿法刻蚀，优选刻蚀剂为稀释的HF溶液，由于HF溶液相对于Si呈 惰性，可选择去除以SiO2为材料的绝缘体氧化物12，因此，可以使得绝缘体 氧化物顶部端面低于半导体鳍状物的顶部端面，如此，即将掺杂的半导体鳍 状物14露出绝缘体氧化物表面。

According to the method provided by the present invention, ion doping doping is not required for the semiconductor fin, but the doped fin is directly epitaxially grown on the semiconductor substrate, and thus the semiconductor fin thus formed is regardless of its top and The sidewalls have a uniform doping effect, which improves the overall performance of the Finfet.

依据本发明提供的方法，不需要对半导体鳍状物进行离子注入掺杂，而 是在半导体基底上直接外延生成掺杂了的鳍状物，因此，如此生成的半导体 鳍状物无论其顶部和侧壁都具有均匀的掺杂效果，提高了Finfet的整体性能。

The above is only the preferred embodiment of the present invention, and is not intended to limit the present invention. Any modifications, equivalents, improvements, etc., which are made within the spirit and principles of the present invention, should be included in the present invention. Within the scope of protection.

以上所述仅为本发明的较佳实施例而已，并不用以限制本发明，凡在本 发明的精神和原则之内，所做的任何修改、等同替换、改进等，均应包含在 本发明保护的范围之内。

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CLAIMS CN103137445

1.
A method of forming a Finfet doped fin comprising:

一种形成Finfet掺杂鳍状物的方法，包括：

Providing a semiconductor substrate and forming a patterned hard mask on the semiconductor substrate;

提供半导体基底，并在所述半导体基底上形成图案化硬掩膜；

Etching the semiconductor substrate to form a plurality of semiconductor sidewalls, and trenches between adjacent two semiconductor sidewalls, removing the patterned hard mask;

刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除所述图案化硬掩膜；

Forming an insulator oxide in the trench;

在所述沟槽内形成绝缘体氧化物；

Etching the semiconductor sidewall such that the semiconductor sidewall height is lower than the insulating oxide height;

刻蚀所述半导体侧壁，使所述半导体侧壁高度低于所述绝缘氧化物高度；

Epitaxially growing a doped semiconductor fin on top of the etched semiconductor sidewall;

在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；

The insulator oxide is etched such that the top end of the insulator oxide is lower than the top end surface of the semiconductor fin.

刻蚀所述绝缘体氧化物，使所述绝缘体氧化物顶部端面低于所述半导体鳍状 物的顶部端面。

2.

The method according to claim 1, wherein the semiconductor base material is single crystal silicon, and the insulator oxide material is SiO2; wherein the semiconductor sidewall is wet etched, the etchant is NH3 H2O or tetramethylammonium hydroxide; the insulator oxide is wet etched, and the etchant is a diluted HF solution.

根据权利要求1所述的方法，其特征在于，所述半导体基底材料为单晶 硅，所述绝缘体氧化物材料为SiO2；其中，利用湿法刻蚀所述半导体侧壁，刻蚀 剂为NH3 H2O或者四甲基氢氧化铵；利用湿法刻蚀所述绝缘体氧化物，刻蚀剂 为稀释的HF溶液。

3.

The method according to claim 1 or 2, wherein said epitaxially grown semiconductor fin is one of SiB, SiGe, SiC, SiP, SiAs, SiGeB, SiCB, GaN, InAs, InP.

根据权利要求1或2所述的方法，其特征在于，所述外延生长的所述半 导体鳍状物为SiB，SiGe，SiC，SiP，SiAs，SiGeB，SiCB，GaN，InAs，InP 之一。

4.

The method according to claim 3, wherein the SiGe has an atomic ratio of Si to Ge of from 20:1 to 6:4.

根据权利要求3所述的方法，其特征在于，所述SiGe中Si与Ge的原子 比为20：1至6：4。

5.

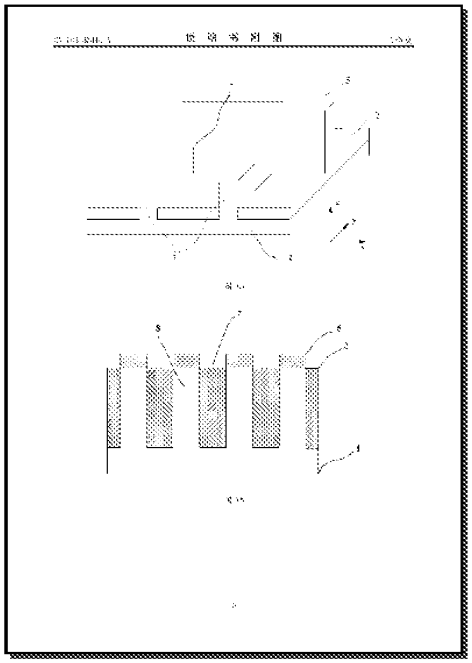
The method according to claim 3, wherein the concentration of B in the SiB, SiGeB, and SiCB is 10<14> to 8×10<21>atoms/cm<3>.

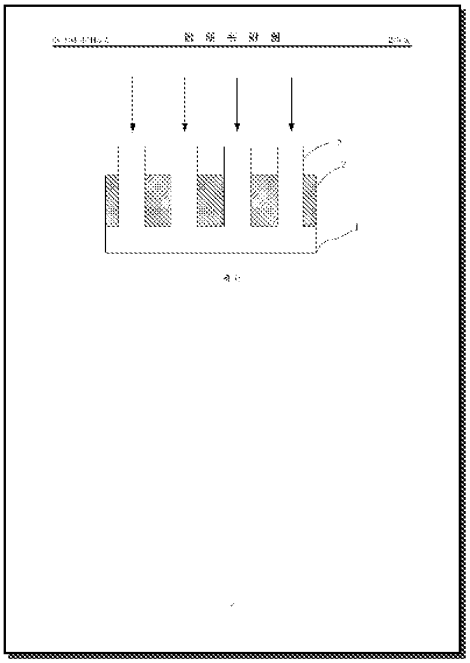
根据权利要求3所述的方法，其特征在于，所述SiB、SiGeB、SiCB中B 的浓度为10<14>至8×10<21>atoms/cm<3>。

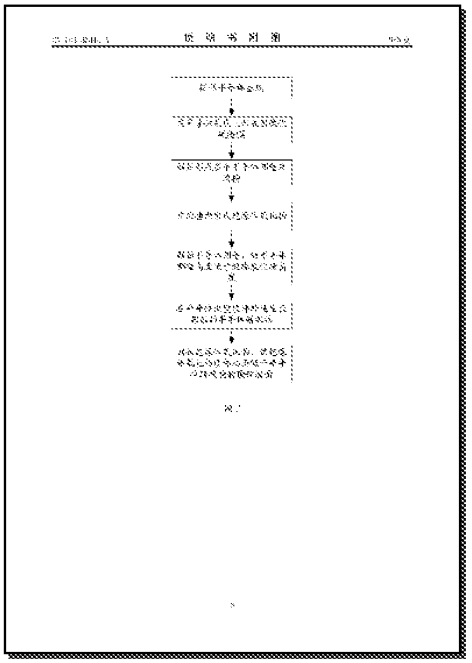
6.

The method according to claim 3, wherein the atomic ratio of Si to C in the SiC is from 100:1 to 20:1.

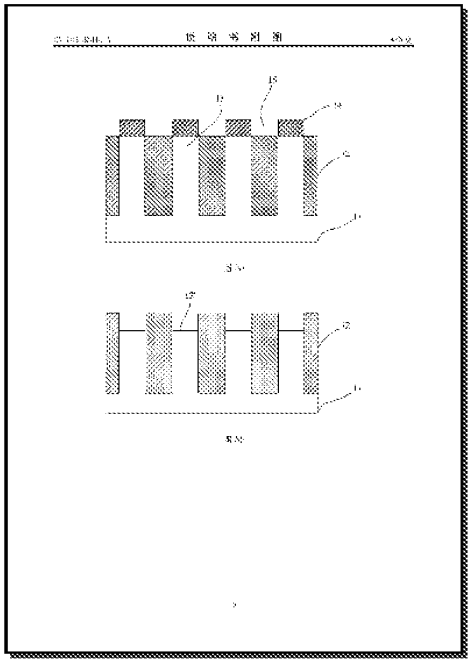
根据权利要求3所述的方法，其特征在于，所述SiC中Si与C的原子 比为100：1至20：1。

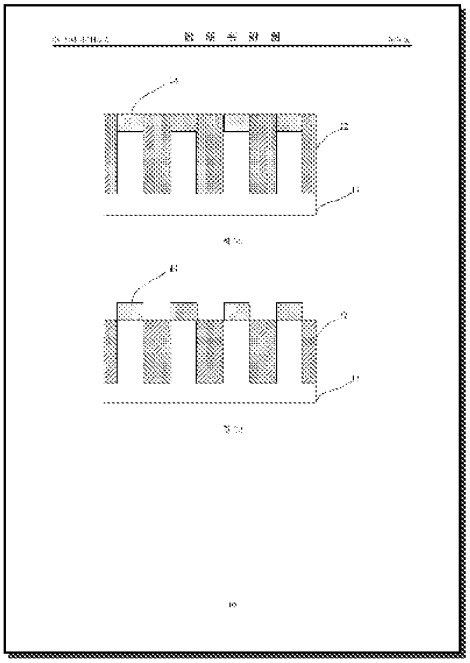






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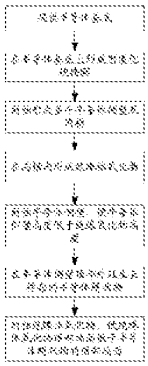
权利要求书1页 说明书3页 附图5页

(54)发明名称

形成Finfet掺杂鳍状物的方法

(57)摘要

本发明提供了一种形成Finfet掺杂鳍状物的方法，包括提供半导体基底，并在半导体基底上形成图案化硬掩膜；刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除图案化硬掩膜；在沟槽内形成绝缘体氧化物；刻蚀半导体侧壁，使半导体侧壁高度低于绝缘氧化物高度；在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；刻蚀绝缘体氧化物，使绝缘体氧化物顶部端面低于半导体鳍状物的顶部端面。因此，不需要对半导体鳍状物进行离子注入掺杂，而是在半导体基底上直接外延生成掺杂了的鳍状物，形成的掺杂的半导体鳍状物无论其顶部和侧壁都具有均匀的掺杂效果，提高了Finfet的整体性能。



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1. 一种形成 Finfet 掺杂鳍状物的方法，包括：

提供半导体基底，并在所述半导体基底上形成图案化硬掩膜；

刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除所述图案化硬掩膜；

在所述沟槽内形成绝缘体氧化物；

刻蚀所述半导体侧壁，使所述半导体侧壁高度低于所述绝缘氧化物高度；

在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；

刻蚀所述绝缘体氧化物，使所述绝缘体氧化物顶部端面低于所述半导体鳍状物的顶部端面。

2. 根据权利要求 1 所述的方法，其特征在于，所述半导体基底材料为单晶硅，所述绝缘体氧化物材料为 SiO_2；其中，利用湿法刻蚀所述半导体侧壁，刻蚀剂为 $NH_3 \cdot H_2O$ 或者四甲基氢氧化铵；利用湿法刻蚀所述绝缘体氧化物，刻蚀剂为稀释的 HF 溶液。

3. 根据权利要求 1 或 2 所述的方法，其特征在于，所述外延生长的所述半导体鳍状物为 SiB，SiGe，SiC，SiP，SiAs，SiGeB，SiCB，GaN，InAs，InP 之一。

4. 根据权利要求 3 所述的方法，其特征在于，所述 SiGe 中 Si 与 Ge 的原子比为 20 ： 1 至 6 ： 4。

5. 根据权利要求 3 所述的方法，其特征在于，所述 SiB，SiGeB，SiCB 中 B 的浓度为 10^{14} 至 $8\times10^{21}atoms/cm^3$。

6. 根据权利要求 3 所述的方法，其特征在于，所述 SiC 中 Si 与 C 的原子比为 100 ： 1 至 20 ： 1。

形成 Finfet 掺杂鳍状物的方法

技术领域

[0001] 本发明涉及半导体制造领域，尤其涉及形成Finfet晶体管中掺杂鳍状物（fin）的方法。

背景技术

[0002] 场效应晶体管（FET）一直是用来制造专用集成电路芯片、静态随机存储器（SRAM）芯片等产品的主导半导体技术。随着半导体器件的日趋小型化，FET短沟道效应愈发严重，为解决如当FET进入22nm节点后的短沟道效应，进而发展出三维的FET，如Finfet（鳍片式场效应晶体管）。图1a展示出现有Finfet的结构示意图，半导体基底1上形成有绝缘体氧化物3，长而薄的半导体鳍状物3从绝缘体氧化物2中突起，多晶硅栅极5包围鳍状物3的三个侧面，将半导体鳍状物3掺杂，并在鳍状物3的两端生成源/漏极区（未示出），栅氧化物4将多晶硅或者金属栅极5与半导体鳍状物2隔开，当Finfet工作时，多晶硅或者金属栅极5能够在半导体鳍状物3的三个侧面上感应出导电沟道。Finfet由于其能避免短沟道效应以及工艺简单而被广泛关注。

[0003] 图1b显示了Finfet制造过程中的结构示意图，在进行Finfet制造中，形成掺杂的半导体鳍状物时，常用的过程如下，提供半导体基底1，如单晶硅基底，并在单晶硅基底1上形成图案化的SiN硬掩膜6，刻蚀单晶硅基底1，形成多个半导体侧壁8，以及相邻两个半导体侧壁8之间的高纵深比的沟槽7，将绝缘氧化物2沉积于沟槽7中，且绝缘氧化物2的高度低于沟槽7的高度，因此，即在绝缘氧化物2上形成了半导体鳍状物3，去除SiN硬掩膜6，对半导体鳍状物3进行离子注入掺杂。然而，当对半导体鳍状物3进行离子注入掺杂时，由于注入离子的随机变化，并且由于半导体鳍状物3的形貌为条状，就会使得半导体鳍状物3的顶部与其侧壁存在掺杂差异，如图1c所示，不均匀的掺杂会导致Finfet整体性能的变差，因此，Finfet鳍状物的掺杂均匀性是现在Finfet制造时亟待解决的问题。

发明内容

[0004] 本发明提供了一种形成Finfet掺杂鳍状物的方法，解决现有Finfet鳍状物进行离子注入掺杂时，掺杂均匀性差的问题。

[0005] 本发明采用的技术手段如下：一种形成Finfet掺杂鳍状物的方法，包括：

[0006] 提供半导体基底，并在所述半导体基底上形成图案化硬掩膜；

[0007] 刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除所述图案化硬掩膜；

[0008] 在所述沟槽内形成绝缘体氧化物，所述绝缘体氧化物高度等于所述沟槽高度；

[0009] 刻蚀所述半导体侧壁，使所述半导体侧壁高度低于所述绝缘氧化物高度；

[0010] 在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；

[0011] 刻蚀所述绝缘体氧化物，使所述绝缘体氧化物顶部端面低于所述半导体鳍状物的顶部端面。

[0012] 进一步，所述半导体基底材料为单晶硅，所述绝缘体氧化物材料为 SiO_2；其中，利用湿法刻蚀所述半导体侧壁，刻蚀剂为 $NH_3 \cdot H_2O$ 或者四甲基氢氧化铵；利用湿法刻蚀所述绝缘体氧化物，刻蚀剂为稀释的 HF 溶液。

[0013] 进一步，所述外延生长的所述半导体鳍状物为 SiB，SiGe，SiC，SiP，SiAs，SiGeB，SiCB，GaN，InAs，InP 之一。

[0014] 进一步，所述 SiGe 中 Si 与 Ge 的原子比为 20 ： 1 至 6 ： 4。

[0015] 进一步，所述 SiB，SiGeB，SiCB 中 B 的浓度为 10^{14} 至 8×10^{21}atoms/cm^3。

[0016] 进一步，所述 SiC 中 Si 与 C 的原子比为 100 ： 1 至 20 ： 1。

[0017] 依据本发明提供的方法，不需要对半导体鳍状物进行离子注入掺杂，而是在半导体基底上直接外延生成掺杂了的鳍状物，因此，如此生成的半导体鳍状物无论其顶部和侧壁都具有均匀的掺杂效果，提高了 Finfet 的整体性能。

附图说明

[0018] 图 1a 为 Finfet 的结构示意图；

[0019] 图 1b 为 Finfet 制造过程中的结构示意图；

[0020] 图 1c 为对 Finfet 的半导体鳍状物进行离子注入掺杂的示意图；

[0021] 图 2 为本发明一种形成 Finfet 掺杂鳍状物的方法流程图；

[0022] 图 3a ～图 3d 为本发明制作 Finfet 掺杂鳍状物的流程结构示意图。

具体实施方式

[0023] 以下结合附图对本发明的原理和特征进行描述，所举实例只用于解释本发明，并非用于限定本发明的范围。

[0024] 本发明提供了一种形成 Finfet 掺杂鳍状物的方法，如图 2 所示，包括如下步骤：

[0025] 提供半导体基底，并在所述半导体基底上形成图案化硬掩膜；

[0026] 刻蚀半导体基底形成多个半导体侧壁，以及相邻两个半导体侧壁之间的沟槽，去除所述图案化硬掩膜；

[0027] 在所述沟槽内形成绝缘体氧化物；

[0028] 刻蚀所述半导体侧壁，使所述半导体侧壁高度低于所述绝缘氧化物高度；

[0029] 在刻蚀后的半导体侧壁顶部外延生长掺杂的半导体鳍状物；

[0030] 刻蚀所述绝缘体氧化物，使所述绝缘体氧化物顶部端面低于所述半导体鳍状物的顶部端面。

[0031] 以下结合附图 3a ～ 3d 详细描述本发明制作 Finfet 掺杂鳍状物的方法过程。

[0032] 如图 3a 所示，提供半导体基底 11，半导体基底 11 的材料一般为单晶硅材料，在半导体基底 11 上形成图案化的硬掩膜 14，硬掩膜 14 一般为 SiN，图案化硬掩膜 14 为长而薄的条状。

[0033] 通过硬掩膜 14 刻蚀半导体基底 11，形成多个半导体侧壁 13，以及侧壁 13 之间的沟槽 15；在沟槽 15 中形成绝缘体氧化物 12，绝缘体氧化物 12 材料优选为 SiO_2。

[0034] 参照图 3b，去除硬掩膜 14，利用湿法刻蚀去除部分半导体侧壁 13，优选以 $NH_3 \cdot H_2O$ 或者四甲基氢氧化铵为刻蚀剂，由于半导体侧壁 13 的材料为单晶硅，绝缘体氧化物 12 为

SiO_2，$NH_3 \cdot H_2O$或者四甲基氢氧化铵为刻蚀剂相对于SiO_2为惰性，只对单晶硅具有刻蚀作用，因而，刻蚀后可使得刻蚀后的半导体侧壁 13' 的顶部端面低于绝缘氧化物 12 的顶部端面，即使半导体侧壁 13 凹陷；

[0035] 在刻蚀后的半导体侧壁 13' 的顶部外延生长掺杂的半导体鳍状物 14，如图 3c 所示，其中，掺杂的半导体鳍状物的材料可以是 SiB，SiGe，SiC，SiP，SiAs，SiGeB，SiCB，GaN，InAs，InP 等中的一种，且优选的，SiGe 中 Si 与 Ge 的原子比为 20 ： 1 至 6 ： 4，SiB，SiGeB，SiCB 中 B 的浓度为 10^{14} 至 8×10^{21} atoms/cm^3，SiC 中 Si 与 C 的原子比为 100 ： 1 至 20 ： 1；作为本领域技术人员公知的技术手段，对如何外延生长掺杂的半导体鳍状物 14 不做限定，在实现时可根据具体情况选择合适的外延生长参数。

[0036] 如图 3d 所示，在外延生长了掺杂的半导体鳍状物 14 后，对绝缘体氧化物 12 进行湿法刻蚀，优选刻蚀剂为稀释的 HF 溶液，由于 HF 溶液相对于 Si 呈惰性，可选择去除以 SiO_2 为材料的绝缘体氧化物 12，因此，可以使得绝缘体氧化物顶部端面低于半导体鳍状物的顶部端面，如此，即将掺杂的半导体鳍状物 14 露出绝缘体氧化物表面。

[0037] 依据本发明提供的方法，不需要对半导体鳍状物进行离子注入掺杂，而是在半导体基底上直接外延生成掺杂了的鳍状物，因此，如此生成的半导体鳍状物无论其顶部和侧壁都具有均匀的掺杂效果，提高了 Finfet 的整体性能。

[0038] 以上所述仅为本发明的较佳实施例而已，并不用以限制本发明，凡在本发明的精神和原则之内，所做的任何修改、等同替换、改进等，均应包含在本发明保护的范围之内。

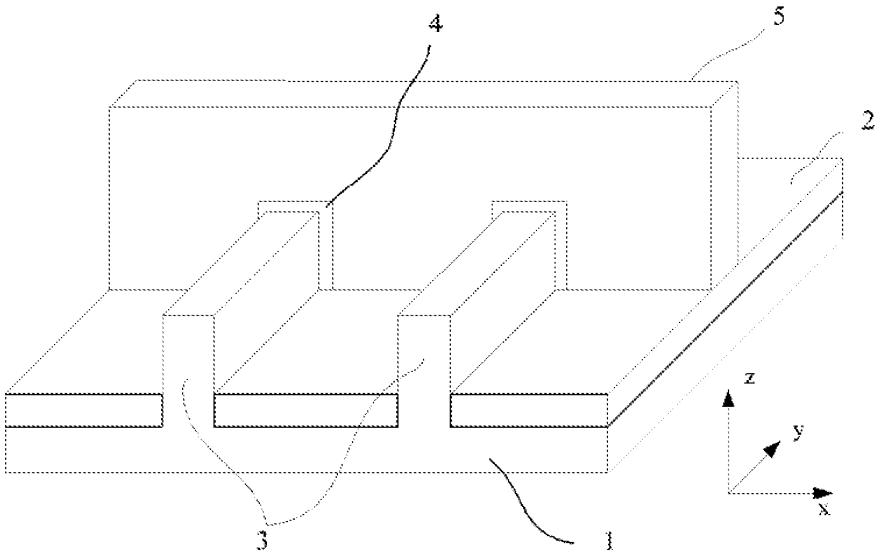


图 1a

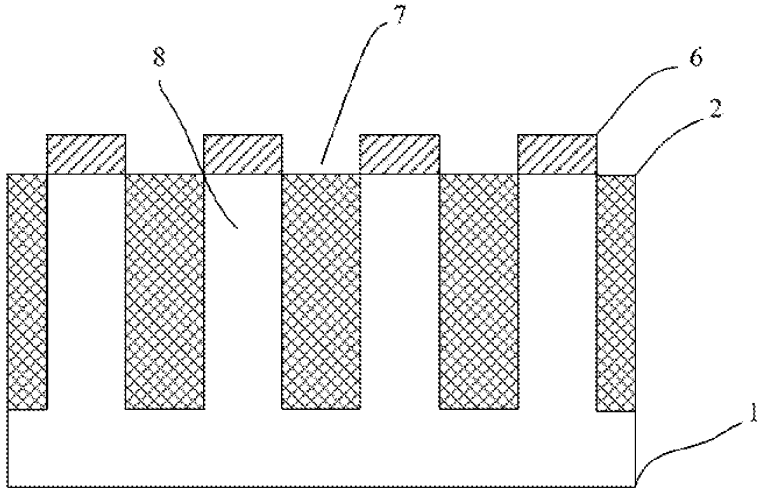


图 1b

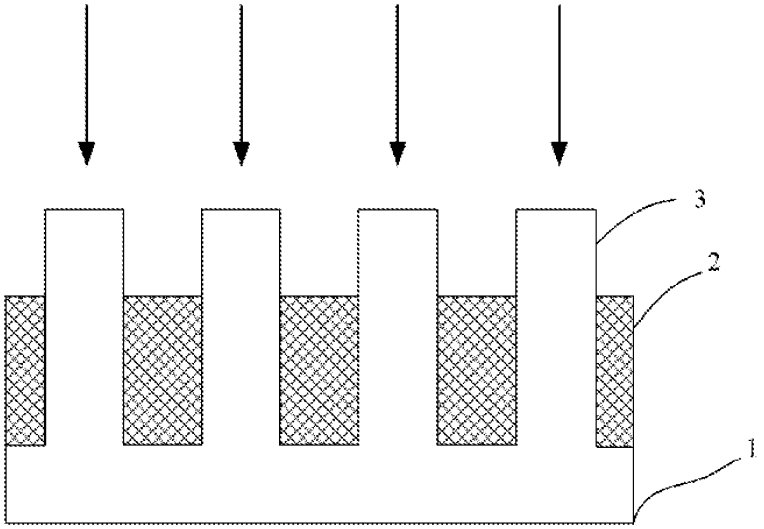


图 1c

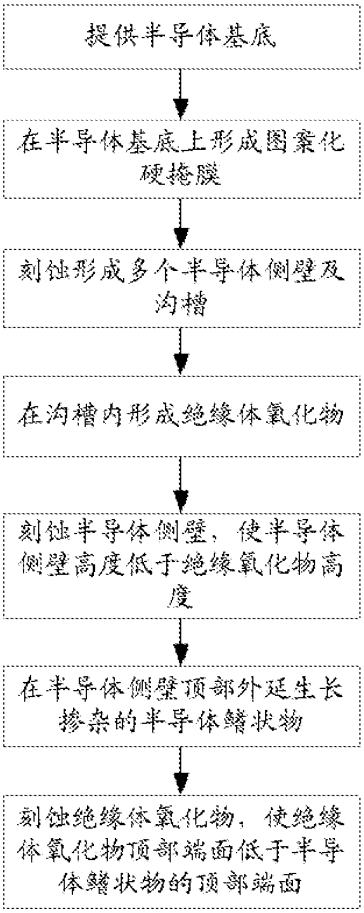

提供半导体基底
在半导体基底上形成图案化硬掩膜
刻蚀形成多个半导体侧壁及沟槽
在沟槽内形成绝缘体氧化物
刻蚀半导体侧壁，使半导体侧壁高度低于绝缘氧化物高度
在半导体侧壁顶部外延生长掺杂的半导体鳍状物
刻蚀绝缘体氧化物，使绝缘体氧化物顶部端面低于半导体鳍状物的顶部端面

图 2

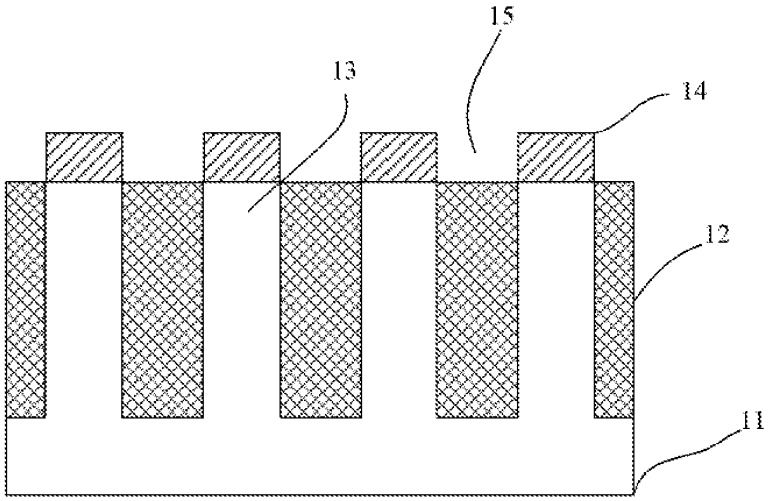


图 3a

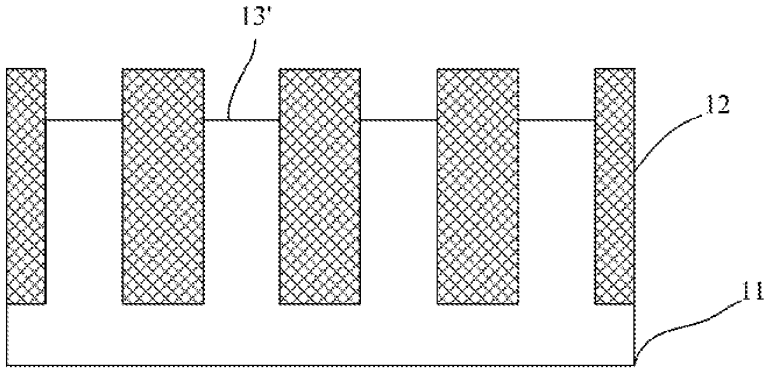


图 3b

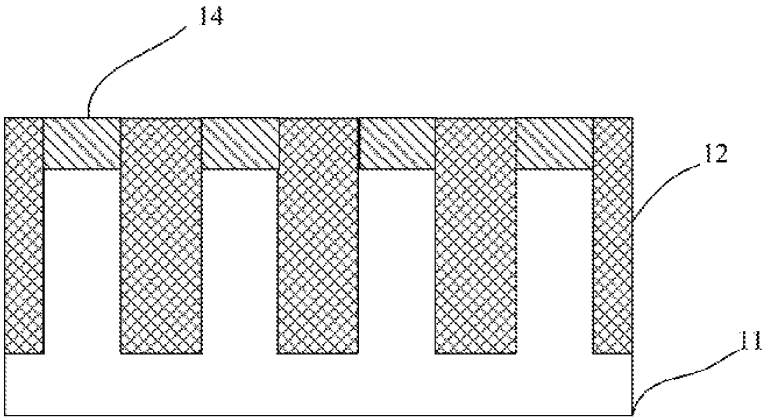


图 3c

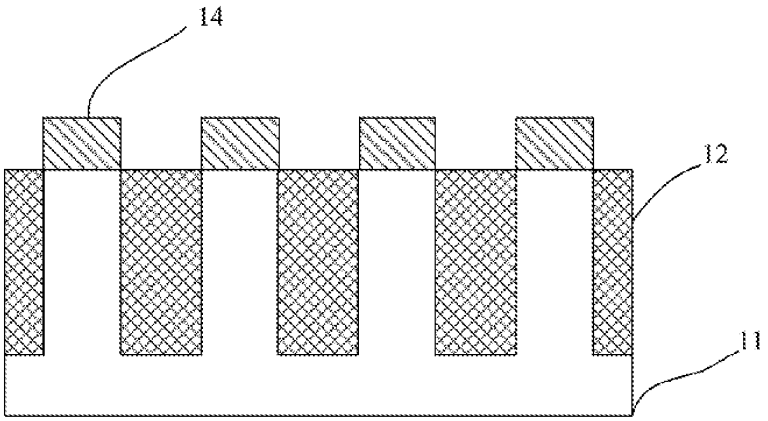


图 3d

Electronic Patent Application Fee Transmittal	
Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	35276119
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Receipt Date:	27-FEB-2019
Filing Date:	20-OCT-2017
Time Stamp:	21:43:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	022819INTEFSW00007401500393
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US-C1_IDS_02-27-19.pdf	477269 6c54442624b27aaeb50a8e857c7f04bc9245edd9	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	Ref_P60397CN-OA1-11-27-18.pdf	534863 ca4b86ff13f49ef7d867b1bd261741adb674f26e	no	6
Warnings:					
Information:					
3	Foreign Reference	Ref_CN101952948_w_English_machine_translation.pdf	6700430 a5f6f2bfeb85d226a230431d389183200e68ff5c	no	58
Warnings:					
Information:					
4	Foreign Reference	Ref_CN103137445_w_English_machine_translation.pdf	5660377 6cc8b8c5911ddf5b3f253463c819c83efb24becc	no	24
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30556 e97d9368fb6e75657e5223ab4a7d3c63e44dede0	no	2
Warnings:					
Information:					

Total Files Size (in bytes):	13403495

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/789,315
Filing Date	October 20, 2017
First Inventor	Webb et al.
Art Unit	2822
Examiner Name	Potter, Roy Karl
Attorney Docket No.	P60397US-C1 Conf. No. 9752

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted after Allowance but prior to payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☒ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	02-27-2019
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* Date 02-27-19

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

31817 7590 02/12/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
POTTER, ROY KARL	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 02/12/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1	9752

TITLE OF INVENTION: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/13/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 02/12/2019
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1	9752

TITLE OF INVENTION: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
POTTER, ROY KARL	2822	257-369000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1	9752

31817 7590 02/12/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
POTTER, ROY KARL	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 02/12/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/789,315	Applicant(s) WEBB et al.	
	Examiner ROY K POTTER	Art Unit 2822	AIA Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to the amendment of 10/3/18.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/18/2019.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/ROY K POTTER/
Primary Examiner, Art Unit 2822

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/789,315	WEBB et al.
	Examiner	Art Unit
	ROY K POTTER	2822

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L29/66795, H01L29/785, H01L27/0886, H01L21/823821, H01L21/845, H01L27/1211, H01L27/0924, H01L29/41791	1/30/18	RP
H01L29/66795, H01L29/785, H01L27/0886, H01L21/823821, H01L21/845, H01L27/1211, H01L27/0924, H01L29/41791	6/22/2018	RP
H01L29/0649, H01L29/785, H01L29/66795, H01L29/66545 , H01L29/41791, H01L23/535, H01L21/76895, H01L21/823821, H01L21/823878, H01L27/0924	01/30/2019	RP

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
H01L29/0649, H01L29/785, H01L29/66795, H01L29/66545 , H01L29/41791, H01L23/535, H01L21/76895, H01L21/823821, H01L21/823878, H01L27/0924	01/30/2019	RP

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
	H01L29/0649, H01L29/785, H01L29/66795, H01L29/66545 , H01L29/41791, H01L23/535, H01L21/76895, H01L21/823821, H01L21/823878, H01L27/0924	02/01/2019	RP

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/789,315	WEBB et al.
	Examiner	Art Unit
	ROY K POTTER	2822

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/789,315	WEBB et al.
	Examiner	**Art Unit**
	ROY K POTTER	2822

CPC						
Symbol					**Type**	**Version**
H01L	/	29	/	0649	F	2013-01-01
H01L	/	29	/	66545	I	2013-01-01
H01L	/	29	/	66795	I	2013-01-01
H01L	/	29	/	785	I	2013-01-01
H01L	/	21	/	76895	I	2013-01-01
H01L	/	21	/	823821	I	2013-01-01
H01L	/	21	/	823878	I	2013-01-01
H01L	/	23	/	535	I	2013-01-01
H01L	/	27	/	0924	I	2013-01-01
H01L	/	29	/	41791	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/ROY K POTTER/ Primary Examiner, Art Unit 2822	30 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7D

U.S. Patent and Trademark Office — Part of Paper No.: 20190130

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/789,315	WEBB et al.
	Examiner	Art Unit
	ROY K POTTER	2822

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	29	/	06
H01L	/	29	/	66

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/ROY K POTTER/ Primary Examiner, Art Unit 2822	30 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7D

U.S. Patent and Trademark Office — Part of Paper No.: 20190130

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/789,315	WEBB et al.
	Examiner	**Art Unit**
	ROY K POTTER	2822

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☑ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	19	19	28	28								
2	2	11	11	20	20	29	29								
3	3	12	12	21	21	30	30								
4	4	13	13	22	22										
5	5	14	14	23	23										
6	6	15	15	24	24										
7	7	16	16	25	25										
8	8	17	17	26	26										
9	9	18	18	27	27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/ROY K POTTER/ Primary Examiner, Art Unit 2822	30 January 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	7D

U.S. Patent and Trademark Office — Part of Paper No.: 20190130

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/789,315	WEBB et al.
	Examiner	**Art Unit**
	ROY K POTTER	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/22/2018	01/30/2019							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
7	7	✓	=							
8	8	✓	=							
9	9	✓	=							
10	10	✓	=							
11	11	=	=							
12	12	=	=							
13	13	=	=							
14	14	=	=							
15	15	=	=							
16	16	=	=							
17	17	=	=							
18	18	=	=							
19	19	=	=							
20	20	=	=							
21	21	=	=							
22	22	=	=							
23	23	=	=							
24	24	=	=							
25	25	=	=							
26	26	=	=							
27	27	=	=							
28	28	=	=							
29	29	=	=							
30	30	=	=							

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	2822
	Examiner Name	POTTER, ROY KARL
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
/R.K.P/		US-20070090443	04/26/2007	Byung-Yong Choi et al.	
/R.K.P/		US-20130065371	03/14/2013	Andy C. Wei et al.	
/R.K.P/		US-20090242986	10/01/2009	Yukio Nakabayashi et al.	
/R.K.P/		US-20060141706	06/29/2006	Seung-Wan Hong	
/R.K.P/		US-20120211808	08/23/2012	Andy Wei et al.	
/R.K.P/		US-7,820,551	10/26/2010	Kabushiki Kaisha Toshiba	
/R.K.P/		US-7,026,199	04/11/2006	Hynix Semiconductor Inc.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		JP-2008172082	07/24/2008	TOSHIBA CORP		
		JP-2005136376	05/26/2005	Hynix Semiconductor Inc.		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
/R.K.P/		Office Action for Taiwan Patent Application No. 107113364 (Attorney Docket No. P60397TW-D2-D1) mailed October 18, 2018, 5 pgs., no translation.	
/R.K.P/		Notice of Allowance for Taiwan Patent Application No. 106120024 (Attorney Docket No. P60397TW-D2) mailed March 19, 2018, 2 pgs., no translation.	X
/R.K.P/		Notice of Allowance and Search Report for Taiwan Patent Application No. 105134078 (Attorney Docket No. P60397TW-D) mailed May 19, 2017, 3 pgs., no translation.	
/R.K.P/		Notice of Allowance for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed September 19, 2016, 2 pgs., no translation.	
/R.K.P/		Office Action and Search Report for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed May 17, 2016, 3 pgs., no translation.	
/R.K.P/		Notice of Allowance for Japanese Patent Application No. 2016-526912 (Attorney Docket No. P60397JP) mailed March 13, 2018, 1 Pg., no translation.	
/R.K.P/		Office Action for European Patent Application No. 13899890.1 (Attorney Docket No. P60397EP) mailed July 11, 2017, 2 pgs.	

EXAMINER /ROY K POTTER/ **DATE CONSIDERED** 02/01/2019

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	21	"9831306"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/01 19:22
L2	12	("20050056888" | "20070054464" | "20070080380" | "20080080380" | "20110021027" | "20110291188" | "20130020615" | "20130134506" | "20130214364" | "6515319" | "7781274").PN. OR ("9831306").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/01 19:23
L3	37873	(H01L29/0649 or H01L29/785 or H01L29/66795 or H01L29/66545 or H01L29/41791 or H01L23/535 or H01L21/76895 or H01L21/823821 or H01L21/823878 or H01L27/0924)".cpc"	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/01 19:50
L10	544	fin same second with gate and fin same direction and second with gate same (separate or discontinuous)same first with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/01 19:53
L11	285	l3 and l10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/01 19:54
L12	11	("20150261894" | "8772109" | "8785285" | "8816444" | "8823065" | "8860148" | "9105490" | "9236267" | "9236300" | "9520482" | "9576814").PN. OR ("10090325").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/01 19:58
L13	174	("20090283837" | "20110068375" | "20110121406" | "20110269287" | "20130069144" | "20130244387" | "7719043").PN. OR ("8860148").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/02/01 20:04

2/ 1/ 2019 8:05:57 PM
C:\ Users\ rpotter\ Documents\ EAST\ Workspaces\ 012319.wsp

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"15789315"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/30 11:10
L2	543	fin same second with gate and fin same direction and second with gate same (separate or discontinuous)same first with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/30 11:12
L3	438	finfet and second with gate and fin same direction and second with gate same (separate or discontinuous)same first with gate	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/30 11:15
L4	82245	(H01L29/0649 or H01L29/785 or H01L29/66795 or H01L29/66545 or H01L29/41791 or H01L23/535 or H01L21/76895 or H01L21/823821 or H01L21/823878 or H01L27/0924).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/30 11:19
L5	409	l2 and l4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/30 11:19
L6	360	l3 and l4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/01/30 11:19

1/ 30/ 2019 11:20:07 AM
C:\ Users\ rpotter\ Documents\ EAST\ Workspaces\ 012319.wsp

EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	37311	(H01L29/0649 or H01L29/785 or H01L29/66795 or H01L29/66545 or H01L29/41791 or H01L23/535 or H01L21/76895 or H01L21/823821 or H01L21/823878 or H01L27/0924)".cpc"	US-PGPUB; USPAT	OR	OFF	2019/02/01 19:51
L5	37311	(H01L29/0649 or H01L29/785 or H01L29/66795 or H01L29/66545 or H01L29/41791 or H01L23/535 or H01L21/76895 or H01L21/823821 or H01L21/823878 or H01L27/0924)".cpc"	US-PGPUB; USPAT	OR	OFF	2019/02/01 19:51
L6	310	fin same second with gate and fin same direction and second with gate same (separate or discontinuous)same first with gate	US-PGPUB; USPAT	OR	OFF	2019/02/01 19:51
L7	505	fin same second with gate and fin same direction and second with gate same (separate or discontinuous)same first with gate	US-PGPUB; USPAT	OR	ON	2019/02/01 19:52
L8	505	fin same second with gate and fin same direction and second with gate same (separate or discontinuous)same first with gate	US-PGPUB; USPAT	OR	ON	2019/02/01 19:52
L9	285	l5 and l8	US-PGPUB; USPAT	OR	ON	2019/02/01 19:53
L14	5	("20120025319" | "20150380519" | "20170012000" | "20170103986" | "7285831").PN. OR ("10008599").URPN.	US-PGPUB; USPAT	OR	OFF	2019/02/01 20:08

2/1/2019 8:08:57 PM
C:\Users\rpotter\Documents\EAST\Workspaces\012319.wsp

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 9752

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/789,315	10/20/2017 RULE	257	2822	P60397US-C1

APPLICANTS
Intel Corporation, Santa Clara, CA;

INVENTORS
Milton Clair WEBB, Aloha, OR;
Mark BOHR, Aloha, OR;
Tahir GHANI, Portland, OR;
Szuya S. LIAO, Portland, OR;

**** CONTINUING DATA ***************************
This application is a CON of 15/024,750 03/24/2016 PAT 9831306
which is a 371 of PCT/US2013/076673 12/19/2013

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
11/01/2017

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
❑ Yes ☑ No	❑ Yes ☑ No	/ROY KARL POTTER/ Examiner's Signature	❑ Initials	OR	15	30	3

ADDRESS
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204
UNITED STATES

TITLE
SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
2680	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

BIB (Rev. 05/07).

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	2822
	Examiner Name	POTTER, ROY KARL
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-20070090443	04/26/2007	Byung-Yong Choi et al.	
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Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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TRANSISTOR OF SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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Classification: - international: ***H01L21/336; H01L21/76; H01L21/762; H01L21/8234; H01L21/8242; H01L27/08; H01L27/088; H01L27/108; H01L29/78; H01L29/786;*** (IPC1-7): H01L21/336; H01L21/76; H01L21/762; H01L21/8234; H01L21/8242; H01L27/08; H01L27/088; H01L27/108; H01L29/78; H01L29/786

- cooperative: **H01L29/41791**; **H01L29/66795**; **H01L29/7851**; H01L2029/7858

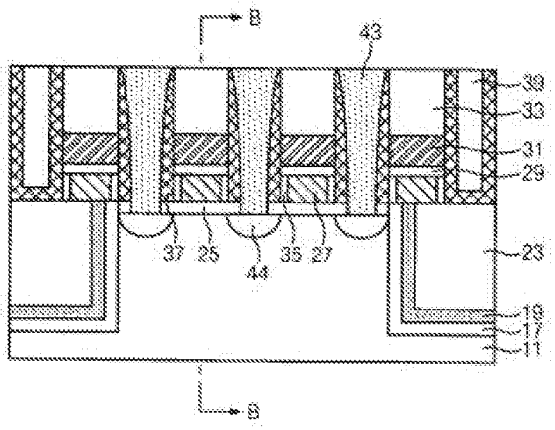
Application number: JP20040190757 20040629 Global Dossier

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Abstract of JP2005136376 (A)

PROBLEM TO BE SOLVED: To provide a transistor of semiconductor device in which a channel region is formed on a sidewall of an active region that protrudes above a device isolation film, and a contact to a landing plug is extended to the sidewall in the direction of the major axis of the protruding active region to improve short channel effect as well as to reduce contact resistance, and to provide a method of manufacturing the same. ;SOLUTION: A device isolation oxide film is etched to form a silicon fin that



protrudes, and then a gate electrode and a source/drain region, of which tops are flattened, are formed after a channel region being formed on a sidewall of the silicon fin by means of inclined ion implantation. ;COPYRIGHT: (C)2005,JPO&NCIPI

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DESCRIPTION JP2005136376

Kind Code: A1 A method of forming a channel region on a side wall of an active region projected on an upper portion of a device isolation film, extending a contact with a landing plug to a side wall in a long axis direction of the projected active region, A transistor of a semiconductor device capable of reducing a contact resistance and a method of forming the same are provided. SOLUTION: A silicon fins is formed by etching an element isolating oxide film, a channel region is formed on a side wall of a silicon fin by gradient ion implantation, and then a gate electrode whose upper part is planarized and a source / drain region are formed Form. (FIG.

【課題】チャンネル領域を素子分離膜の上部に突出された活性領域の側壁に形成し、ランディングプラグとのコンタクトを突出した活性領域の長軸方向の側壁まで拡張してショートチャンネル効果を改善し、コンタクト抵抗を減少させることができる半導体素子のトランジスタおよびその形成方法を提供する。【解決手段】素子分離酸化膜を食刻して突出されたシリコンフィンを形成し、傾斜イオン注入でシリコンフィンの側壁にチャンネル領域を形成したあと上部が平坦化したゲート電極とソース／ドレイン領域を形成する。【選択図】図２５

Transistor of semiconductor device and method of forming the same

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半導体素子のトランジスタおよびその形成方法

[0001]

According to the present invention, the channel region is formed on the side wall of the active region projected to the top of the isolation film, the contact with the landing plug is extended to the side wall in the long axis direction of the protruded active region to improve the short channel effect , A transistor of a semiconductor device capable of reducing a contact resistance, and a method of forming the same.

本発明は、チャンネル領域を素子分離膜の上部に突出された活性領域の側壁に形成し、ランディングプラグとのコンタクトを突出した活性領域の長軸方向の側壁まで拡張してショートチャンネル効果を改善し、コンタクト抵抗を減少させることができる半導体素子のトランジスタおよびその形成方法に関する。

[0002]
The DRAM is composed of one transistor and one capacitor, and the channel length of the above-mentioned transistor is decreased as the design rule decreases.

ＤＲＡＭは１つのトランジスタと１つのキャパシタで構成され、前記のトランジスタはデザインルールの減少に伴いセルトランジスタのチャンネル長さが減少することになった。

As a result of the decrease in the channel length, the short channel effect is increased and the characteristics of the cell transistor are changed.

前記のチャンネル長さの減少によりショートチャンネル効果が増加し、セルトランジスタの特性を変化させることになった。

[0003]
FIG. 1 is a layout diagram of a conventional semiconductor device. This shows that the element isolation region 300 defining the active region 200 is formed, but the major axis end portion of the active region 200 is adjacent to the gate region 400. 2 to 9 are diagrams showing a method of forming a transistor of a semiconductor element according to the conventional technique of FIG. 1. 2 to 8 are cross-sectional views taken along the line A - A in FIG. 1. FIG. 9 is a cross-sectional view taken along the line B - B of FIG. 8. As shown in FIG. 2, a well (not shown) is formed in the semiconductor substrate 11. Next, a pad oxide film 13 and a pad nitride film 15 are sequentially formed on the semiconductor substrate 11. Next, in a photolithography process using an element isolation mask (not shown), the pad nitride film 15, the pad oxide film 13, and the semiconductor substrate 11 of a predetermined thickness in the element isolation region are etched to form a trench 21 are formed.

図１は、従来の技術に係る半導体素子のレイアウト図である。これは、活性領域２００を定義する素子分離領域３００を形成するが、活性領域２００の長軸端部がゲート領域４００と隣接することを示したものである。図２～図９は、図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す図である。図２～図８は、図１のＡ－Ａ切断面に沿って示す断面図である。図９は、図８のＢ－Ｂ切断面に沿って示す断面図である。図２に示されているように、半導体基板１１にウェル（図示省略）を形成する。次には、半導体基板１１上にパッド酸化膜１３およびパ

ッド窒化膜１５を順次形成する。次に、素子分離マスク（図示省略）を用いた写真食刻工程で素子分離領域に予定された部分のパッド窒化膜１５、パッド酸化膜１３および所定厚さの半導体基板１１を食刻してトレンチ２１を形成する。

[0004]
Next, a trench thermal oxide film 17 is formed on the surface of the trench 21, and a liner nitride film 19 is formed on the entire surface including the trench 21. As shown in FIG. 3, an element isolation oxide film filling the trench 21 is formed on the entire surface, planarized by the CMP method until the pad nitride film 15 is exposed, and the element isolation film 23 is etched Form. As shown in FIG. 4, the pad nitride film 15 and the liner nitride film 19 exposed by the device isolation film 23 are preferably removed by a wet etching process. At this time, the wet etching process is performed using a phosphoric acid solution. Next, ion implantation processes for forming wells and channels are performed on the semiconductor substrate 11. As shown in FIG. 5, the pad oxide film 13 is removed by a wet method to form a gate oxide film 25 in the active region on the exposed surface of the semiconductor substrate 11. A gate electrode polysilicon layer 27, a barrier metal layer 29 including a WN layer, a metal layer 31 including a tungsten layer, and a hard mask layer 33 made of a nitride film are sequentially formed on the gate oxide film 25. As shown in FIG. 6, in the photolithography process using a gate electrode mask (not shown), the hard mask layer 33, the metal layer 31, the barrier metal layer 29 and the gate electrode polysilicon layer 27 are sequentially etched To form a gate electrode. Next, an oxide film 35 is selectively formed only on the side wall of the gate electrode polysilicon layer 27.

次には、トレンチ２１の表面にトレンチ熱酸化膜１７を形成してトレンチ２１を含む全体表面の上部にライナー窒化膜１９を形成する。図３に示されているように、トレンチ２１を埋め込む素子分離用酸化膜を全体表面の上部に形成し、パッド窒化膜１５が露出するまでＣＭＰ方法で平坦化食刻して素子分離膜２３を形成する。図４に示されているように、素子分離膜２３により露出したパッド窒化膜１５およびライナー窒化膜１９を、好ましくは湿式食刻工程で除去する。このとき、前記の湿式食刻工程はリン酸溶液を用いて行う。次には、半導体基板１１にウェルおよびチャンネル形成用イオン注入工程を行う。図５に示されているように、パッド酸化膜１３を湿式方法で除去して露出した半導体基板１１の表面の活性領域にゲート酸化膜２５を形成する。ゲート酸化膜２５上にゲート電極用ポリシリコン層２７、ＷＮ層を含む障壁金属層２９、タングステン層を含む金属層３１および窒化膜からなるハードマスク層３３を順次形成する。図６に示されているように、ゲート電極マスク（図示省略）を用いた写真食刻工程でハードマスク層３３、金属層３１、障壁金属層２９およびゲート電極用ポリシリコン層２７を順次食刻してゲート電極を形成する。次には、ゲート電極用ポリシリコン層２７の側壁にのみ選択的に酸化膜３５を形成する。

[0005]
Next, a nitride film 37 is formed on the entire surface including the gate electrode to have a

certain thickness, and then a flattened lower insulating layer 39 is formed on the entire surface. At this time, the lower insulating layer 39 is formed of an insulating oxide material having excellent fluidity such as BPSG (Boron Phosphorus Silicate Glass). A CMP process is performed on the nitride film 37 as an etching barrier to planarize and etch the lower insulating layer 39 so that the nitride film 37 is exposed. As shown in FIG. 7, by anisotropically etching the lower insulating layer 39 and the nitride film 37 in a photolithography process using a landing plug contact mask (not shown), self-alignment with the nitride film spacer Like landing plug contact hole 41 is formed. Next, an LDD ion implantation step and a halo ion implantation step are performed on the semiconductor substrate exposed by the landing plug contact hole 41 to form source / drain regions 44. As shown in FIGS. 8 and 9, a landing plug polysilicon layer (not shown) filling the landing plug contact hole 41 is formed on the entire upper surface so that the hard mask layer 33 is exposed Thereby forming the landing plug 43 that fills the landing plug contact hole 41.

次に、前記のゲート電極を含む全体表面の上部に窒化膜３７を一定の厚さに形成した後、全体表面の上部に平坦化した下部絶縁層３９を形成する。このとき、下部絶縁層３９はＢＰＳＧ（Boron Phosphorus Silicate Glass）のように流動性に優れた絶縁酸化物質で形成する。窒化膜３７を食刻障壁にＣＭＰ工程を行って窒化膜３７が露出するよう下部絶縁層３９を平坦化食刻する。図７に示されているように、ランディングプラグコンタクトマスク（図示省略）を用いた写真食刻工程で下部絶縁層３９および窒化膜３７を異方性食刻することにより、窒化膜スペーサと自己整合的なランディングプラグコンタクトホール４１を形成する。次に、ランディングプラグコンタクトホール４１により露出した半導体基板にＬＤＤイオン注入工程とハローイオン注入工程を行ってソース／ドレイン領域４４を形成する。図８および図９に示されているように、ランディングプラグコンタクトホール４１を埋め込むランディングプラグ用ポリシリコン層（図示省略）を全体表面の上部に形成し、ハードマスク層３３が露出するよう平坦化食刻してランディングプラグコンタクトホール４１を埋め込むランディングプラグ４３を形成する。

[0006]

In the above-described conventional semiconductor device forming method according to the prior art, the channel length decreases with the reduction of the design rule, and a short channel effect occurs. In order to solve such problems, a method of increasing the impurity concentration of the channel has been proposed, but the method of increasing the impurity concentration increases the leakage current as a result of increasing the electric field, and the refresh time characteristic of the DRAM And there is a problem that it deteriorates. In addition, the reduction of the channel width due to the reduction of the design rule lowers the current driving force. As the design rule decreases, the connection area between the landing plug, which is the source / drain electrode of the cell transistor, and the substrate surface decreases, so that the contact resistance increases and the drive current further decreases.

前述の従来の技術に係る半導体素子の形成方法では、デザインルールの減少に伴いチャンネル長

さが減少することになり、ショートチャンネル効果が発生することになる。このような問題点を改善するためチャンネルの不純物濃度を増加させる方法が提案されたが、不純物の濃度を増加させる方法は電界を増加させて結果的に漏洩電流を増加させ、ＤＲＡＭのリフレッシュタイム特性を悪化させるという問題点がある。さらに、デザインルールの減少に伴うチャンネル幅の減少は電流駆動力を低下させる。デザインルールの減少に伴い、セルトランジスタのソース／ドレイン電極であるランディングプラグと基板表面の接続面積が減少することになるので、コンタクト抵抗が増加して駆動電流をさらに減少させることになる。

[0007]
FIG. 10 is a layout diagram of a semiconductor device according to another conventional technique. This is a fin type field effect transistor formed on an SOI (Silicon On Insulator) substrate. As shown in FIG. 10, a silicon fin region 600 connecting the source / drain regions 500 is used for the channel, and a gate electrode region 700 is provided on the silicon fin region 600.

図１０は、他の従来の技術に係る半導体素子のレイアウト図である。これはＳＯＩ（Silicon On Insulator）基板に形成したフィン型電界効果トランジスタを示したものである。図１０に示されているように、ソース／ドレイン領域５００の間を連結するシリコンフィン領域６００がチャンネルに用いられ、シリコンフィン領域６００の上部にゲート電極領域７００が備えられている。

[0008]
11 to 16 are diagrams showing a method for forming a transistor of a semiconductor element according to the conventional technique of FIG. 11 to 15 are cross-sectional views taken along the line A - A of FIG. 10. FIG. 16 is a cross-sectional view taken along the line B - B of FIG. 15. As shown in FIG. 11, a first nitride film (not shown) and a first oxide film (not shown) are formed on an SOI wafer on which a buried oxide film 53 and a silicon body 55 are stacked on a semiconductor substrate 51 Then, the first oxide film pattern and the first nitride film are patterned to form a first oxide film pattern 59 and a first nitride film pattern 57. As shown in FIG. 12, the silicon body 55 is etched using the first oxide film pattern 59 as a mask to form a silicon fin (Si-fin) 61. The silicon fin 61 acts as a channel of the transistor. As shown in FIG. 13, a polysilicon layer 63 and a second oxide film 65 are sequentially formed on the entire surface. Here, the polysilicon layer 63 is used for the source / drain junction region of the transistor. As shown in FIG. 14, the stacked structure of the second oxide film 65 and the polysilicon layer 63 is patterned to form a trench 69 defining a gate region.

図１１～図１６は、図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す図である。図１１～図１５は、図１０のＡ－Ａ切断面に沿って示す断面図である。図１６は、図１５のＢ－Ｂ切断面に沿って示す断面図である。図１１に示されているように、半導体基板５１上に埋込み酸化膜５３およびシリコンボディ５５が積層されているＳＯＩウェーハ上に第１の窒化膜

（図示省略）および第１の酸化膜（図示省略）を順次形成した後、前記第１の酸化膜および第１の窒化膜をパターニングして第１の酸化膜パターン５９および第１の窒化膜パターン５７を形成する。図１２に示されているように、第１の酸化膜パターン５９をマスクとしてシリコンボディ５５を食刻してシリコンフィン（Ｓｉ－ｆｉｎ）６１を形成する。シリコンフィン６１は、トランジスタのチャンネルの役割を果たす。図１３に示されているように、全体表面の上部にポリシリコン層６３と第２の酸化膜６５を順次形成する。ここで、ポリシリコン層６３はトランジスタのソース／ドレイン接合領域に用いられる。図１４に示されているように、第２の酸化膜６５およびポリシリコン層６３の積層構造をパターニングしてゲート領域を定義する溝６９を形成する。

[0009]
Next, a third oxide film (not shown) is deposited on the entire surface and anisotropically etched to form oxide film spacers 67 on the side walls of the trench 69. In the anisotropic etching step, the first oxide film 59 and the first nitride film 57 exposed by the oxide film spacer 67 are etched to expose the silicon fins 61 and a predetermined thickness The buried oxide film 53 is etched. As shown in FIGS. 15 and 16, a gate oxide film 71 is formed on the exposed silicon fin 61, and then a gate electrode 73 burying the trench 69 is formed in polycrystalline SiGe. Although the short channel effect can be reduced by the above-described other conventional method of forming a semiconductor device, the use of an SOI wafer increases the wafer cost, decreases the refresh characteristics of the device, There is a problem that it deteriorates.

次には、全体表面の上部に第３の酸化膜（図示省略）を蒸着し、異方性食刻して溝６９の側壁に酸化膜スペーサ６７を形成する。前記の異方性食刻工程は過度食刻工程で、酸化膜スペーサ６７により露出した第１の酸化膜５９および第１の窒化膜５７を食刻してシリコンフィン６１を露出させると共に所定厚さの埋込み酸化膜５３を食刻する。図１５および図１６に示されているように、前記露出したシリコンフィン６１上にゲート酸化膜７１を形成したあと溝６９を埋め込むゲート電極７３を多結晶ＳｉＧｅに形成する。前述の他の従来の技術に係る半導体素子の形成方法ではショートチャンネル効果を減少させることはできるが、ＳＯＩウェーハを用いることによりウェーハ費用が増加し、素子のリフレッシュ特性が減少して素子の特性が劣化するという問題点がある。

[0010]
The present invention provides a transistor of a semiconductor device and a method of forming the same, which can improve the short channel effect characteristics and current driving power while using a single crystal silicon substrate and can improve refresh characteristics of the device There is a purpose in doing.

本発明は、単結晶シリコン基板を用いながらもショートチャンネル効果特性を改善して電流駆動力を増加させることができ、素子のリフレッシュ特性を向上させることができる半導体素子のト

ランジスタおよびその形成方法を提供することに目的がある。

[0011]
A method of forming a transistor of a semiconductor device according to the present invention comprises the steps of: (a) forming a trench type device isolation film defining an I type active region by patterning a semiconductor substrate having a stacked structure of a pad oxide film and a pad nitride film (B) etching the device isolation layer to a predetermined thickness to form silicon fins protruding above the device isolation layer, (c) implanting impurities into side walls of the silicon fins by gradient ion implantation (D) forming a gate oxide film on a sidewall of the silicon fin; (e) forming a planarized conductive layer for a gate electrode on an entire surface of the silicon fin; (F) patterning the conductive layer for the gate electrode and the pad nitride film to form a gate electrode, (g) forming a lower insulating layer having a landing plug contact hole (H) performing an ion implantation process to form an impurity implanted region at the bottom of the landing plug contact hole: (i) etching the pad oxide film exposed through the landing plug contact hole Exposing the silicon fin; and (j) forming a landing plug to fill the landing plug contact hole.

本発明に係る半導体素子のトランジスタ形成方法は、（ａ）パッド酸化膜とパッド窒化膜の積層構造を有する半導体基板をパターニングしてＩ型活性領域を定義するトレンチ型素子分離膜を形成する段階と、（ｂ）前記素子分離膜を所定の厚さに食刻して前記素子分離膜の上部に突出されるシリコンフィンを形成する段階と、（ｃ）前記シリコンフィンの側壁に不純物を傾斜イオン注入してチャンネル領域を形成する段階と、（ｄ）前記シリコンフィンの側壁にゲート酸化膜を形成する段階と、（ｅ）全体表面の上部に平坦化したゲート電極用導電層を形成する段階と、（ｆ）前記ゲート電極用導電層および前記パッド窒化膜をパターニングしてゲート電極を形成する段階と、（ｇ）ランディングプラグコンタクトホールを備えた下部絶縁層を形成する段階と、（ｈ）イオン注入工程を行って前記ランディングプラグコンタクトホールの底部に不純物注入領域を形成する段階と、（ｉ）前記ランディングプラグコンタクトホールを介して露出したパッド酸化膜を食刻してシリコンフィンを露出させる段階、および（ｊ）前記ランディングプラグコンタクトホールを埋め込むランディングプラグを形成する段階を含むことを特徴とする。

[0012]
The transistor of the semiconductor device according to the present invention is defined by a trench type element isolation film and includes an I type active region including silicon fins protruding above the trench type device isolation film, a gate provided on a side wall of the silicon fin A pad insulating film provided at an interface between an upper surface of the silicon fin and a lower surface of the gate electrode, the gate insulating film extending in a direction perpendicular to the I-type active region, Source / drain regions provided on side faces of the silicon fins between the gate electrodes and on the sidewalls of the ends of the silicon fins, and channel regions provided on sidewalls of the silicon fins below the gate electrodes.

本発明に係る半導体素子のトランジスタはトレンチ型素子分離膜により定義され、前記トレンチ型素子分離膜の上部に突出されるシリコンフィンを含むＩ型活性領域と、前記シリコンフィンの側壁に備えられたゲート酸化膜と、前記Ｉ型活性領域と垂直の方向に延びられその上部が平坦なゲート電極と、前記シリコンフィンの上部面とゲート電極の下部面との界面に備えられたパッド絶縁膜と、前記ゲート電極の間のシリコンフィンおよび前記シリコンフィンの端部の側壁に備えられたソース／ドレイン領域、および前記ゲート電極の下部のシリコンフィンの側壁に備えられるチャンネル領域を含むことを特徴とする。

[0013]

A transistor of a semiconductor device and a method of forming the same according to the present invention are characterized in that a channel region is formed on a side wall of an active region protruding above the device isolation film and a side wall in the long axis direction of the active region So that the short channel effect can be improved and the contact resistance can be reduced.

本発明に係る半導体素子のトランジスタおよびその形成方法は、チャンネル領域を素子分離膜の上部に突出された活性領域の側壁に形成し、ランディングプラグとのコンタクトを突出した活性領域の長軸方向の側壁まで拡張してショートチャンネル効果を改善し、コンタクト抵抗を減少させることができるという効果がある。

[0014]

DESCRIPTION OF THE PREFERRED EMBODIMENTS Hereinafter, one embodiment of a transistor of a semiconductor element and a method of forming the same according to the present invention will be described in detail with reference to the drawings.

以下、本発明に係る半導体素子のトランジスタおよびその形成方法の一実施形態を図面を参考にして詳しく説明する。

FIG. 17 is a layout diagram of a semiconductor device according to the embodiment of the present invention.

図１７は、本発明の実施の形態に係る半導体素子のレイアウト図である。

As shown in FIG. 17, the semiconductor device includes an element isolation region 900 that defines an active region 800 including a contact region 1100 including a source / drain junction region, and a major axis end portion of the active region 800 is a gate So as not to come into

contact with the region 1000.

図１７に示されているように、前記の半導体素子はソース／ドレイン接合領域からなるコンタクト領域１１００を含む活性領域８００を定義する素子分離領域９００を含み、活性領域８００の長軸端部はゲート領域１０００と接触しないよう備えられている。

At this time, the reason why the active region 800 is spaced apart from contact with the adjacent gate electrode is that short-circuiting occurs due to contact between the gate electrode formed in the gate region 1000 and the projected active region 800 in the form of a silicon fin This is to prevent it.

このとき、活性領域８００が隣接するゲート電極と接触しないよう離隔させたのは、ゲート領域１０００に形成されるゲート電極とシリコンフィン形態の突出された活性領域８００の接触による短絡が発生することを防止するためである。

[0015]

Further, the landing plug comes into contact with the projected side wall of the active region 800, and the contact characteristics can be improved by increasing the contact area.

さらに、ランディングプラグが活性領域８００の突出された側壁と接触することになり、接触面積の増加によりコンタクト特性を向上させることができる。

FIG. 18 is a perspective view showing a transistor of a semiconductor element formed according to the embodiment of the present invention, and shows a hatched portion a in FIG. 17. In FIG. 18, only the silicon fins 82, the channel region 97, the source / drain region 123, the pad insulating films 83 and 85, and the gate electrode 110 of the active region formed in the semiconductor substrate 81 are shown. The semiconductor device of FIG. 18 includes a semiconductor substrate 81 and silicon fins 82 of an active region provided on a semiconductor substrate. The I-type silicon fins 82 are protruded from the upper part of the semiconductor substrate 81 and are spaced apart from the gate electrodes 110 adjacent to each other in the longitudinal direction of the long axis at regular intervals. On the side wall of the silicon fin 82, the channel region 97 formed by the gradient ion implantation step is located. A gate oxide film (not shown) is provided on the surface of the channel region 97, that is, the side wall of the silicon fin 82. A pad oxide film 83 of a pad insulating film and a pad nitride film 85 are laminated on the interface between the upper surface of the silicon fin 82 and the gate electrode 110 to prevent the upper surface of the silicon fin 82 from functioning as a channel region.

図１８は、本発明の実施の形態に基づき形成された半導体素子のトランジスタを示す斜視図であ

り、図１７の斜線部ａを示したものである。図１８には半導体基板８１に形成された活性領域のシリコンフィン８２、チャンネル領域９７、ソース／ドレイン領域１２３、パッド絶縁膜８３、８５およびゲート電極１１０だけが示されている。図１８の半導体素子は、半導体基板８１と半導体基板上に備えられた活性領域のシリコンフィン８２を含む。Ｉ型のシリコンフィン８２は半導体基板８１の上部に突出されており、長軸の長手方向に隣接するゲート電極１１０と一定の間隔で離隔されている。シリコンフィン８２の側壁には傾斜イオン注入工程で形成されたチャンネル領域９７が位置する。チャンネル領域９７の表面、すなわちシリコンフィン８２の側壁にゲート酸化膜（図示省略）が備えられている。シリコンフィン８２の上部面とゲート電極１１０との界面には、パッド絶縁膜のパッド酸化膜８３とパッド窒化膜８５が積層されてシリコンフィン８２の上部面がチャンネル領域に機能することを防止する。

[0016]

The gate electrode 110 having the flattened upper surface extends in a direction perpendicular to the silicon fin 82 and comes into contact with the upper side and the side wall of the silicon fin 82. At this time, the width of the channel region 97 is twice the height of the silicon fins 82. 19 to 26 are diagrams showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. 19 to 25 are cross-sectional views taken along the line AA in FIG. 17. FIG. 26 is a cross-sectional view taken along the line B - B of FIG. 25. As shown in FIG. 19, a well (not shown) is formed in the semiconductor substrate 81. Next, a pad insulating film having a laminated structure of a pad oxide film 83 and a pad nitride film 85 is formed on the semiconductor substrate 81.

平坦化した上部面を有するゲート電極１１０は、シリコンフィン８２と垂直の方向に延びられてシリコンフィン８２の上側および側壁と接触することになる。このとき、チャンネル領域９７の幅はシリコンフィン８２の高さの２倍となる。図１９～図２６は、本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す図である。図１９～図２５は、図１７のＡ－Ａ切断面に沿った断面図である。図２６は、図２５のＢ－Ｂ切断面に沿った断面図である。図１９に示されているように、半導体基板８１にウェル（図示省略）を形成する。次には、半導体基板８１上にパッド酸化膜８３およびパッド窒化膜８５の積層構造でなるパッド絶縁膜を形成する。

[0017]

Next, a photoresist pattern (not shown) defining an I type active region is performed by performing an exposure and development process using an exposure mask (not shown) defining an active region so as not to be adjacent to a gate electrode formed in a subsequent process, , The pad nitride film 85, the pad oxide film 83 and the semiconductor substrate 81 having a predetermined thickness are etched using the photoresist pattern as an etching mask to form element isolating trenches 87. The exposure mask defines the length of the long axis of the active region to be shorter than 5 F, for example, when the width of the line pattern of the minimum size is F. It is preferable to form the pad oxide film 83 to have a thickness of 50 to 200 Å and the

pad nitride film 85 to have a thickness of 100 to 400 Å. Here, as a method for forming the I-type active region so that the gate electrode formed in the subsequent process and the end portion of its long axis are spaced apart from each other by a predetermined distance, in addition to the method using the separate element isolation mask, 28, or the method shown in FIG. 29.

次に、後続工程で形成されるゲート電極と隣接しないよう活性領域を定義する露光マスク（図示省略）を用いた露光および現像工程を行い、Ｉ型活性領域を定義するフォトレジストパターン（図示省略）を形成した後、前記のフォトレジストパターンを食刻マスクとしてパッド窒化膜８５、パッド酸化膜８３および所定厚さの半導体基板８１を食刻して素子分離用トレンチ８７を形成する。前記の露光マスクは、たとえば最小の大きさのラインパターンの幅がＦの場合、活性領域の長軸の長さを５Ｆより短く定義する露光マスクである。パッド酸化膜８３は５０～２００Åの厚さに形成し、パッド窒化膜８５は１００～４００Åの厚さに形成するのが好ましい。ここで、後続工程で形成されるゲート電極とその長軸の端部が所定距離離隔するようＩ型活性領域を形成する方法として、別途の前記の素子分離マスクを用いる方法以外に図２７～図２８の工程、または図２９の工程のような方法で形成することもできる。

[0018]

27 and 28 are a cross sectional view and a plan view showing one embodiment of a method of forming an active region according to the present invention having a major axis smaller than the major axis length of a conventional active region . As shown in FIGS. 27 and 28, a pad oxide film 83 and a pad nitride film 85 and a CVD oxide film (not shown) for determining an active region are stacked on the semiconductor substrate 81. The CVD oxide film pattern 131 is formed by patterning the CVD oxide film for determining an active region in a photolithography process using a normal element isolation mask and then the surface of the CVD oxide film 131 is wet etched. At this time, the structure of the active region determining CVD oxide film 131 formed at the width of W 1 and the length of L 1 is first formed in the structure of the width of W 2 and the length of L 2. Therefore, a gate electrode (not shown) adjacent to the long axis end portion of the active region is spaced apart from the wet-etched region 133 during the wet etching process.

図２７および図２８は、従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の１つの実施の形態を示す断面図および平面図である。図２７および図２８に示されているように、半導体基板８１の上部にパッド酸化膜８３およびパッド窒化膜８５と活性領域決定用ＣＶＤ酸化膜（図示省略）を積層する。通常の素子分離マスクを用いた写真食刻工程で、前記の活性領域決定用ＣＶＤ酸化膜をパターニングしてＣＶＤ酸化膜パターン１３１を形成した後、ＣＶＤ酸化膜１３１の表面を湿式食刻する。このとき、最初にＷ１の幅とＬ１の長さに形成された前記の活性領域決定用ＣＶＤ酸化膜１３１の構造がＷ２の幅とＬ２の長さ構造に形成される。したがって、前記の湿式食刻工程時に湿式食刻された領域１３３ほど活性領域の長軸端部と隣接するゲート電極（図示省略）が離隔される。

[0019]
As a subsequent process, the semiconductor substrate 81 is etched using the wet etched active region determining CVD oxide film 131 as an etching mask to form the trench 87 of FIG. FIG. 29 is a cross-sectional view and a plan view showing another embodiment of the method of forming an active region according to the present invention having a major axis smaller than the long axis length of the active region of FIG. 19 to the prior art . As shown in FIG. 29, a pad oxide film 83 and a pad nitride film (not shown) are deposited on a semiconductor substrate 81, and a pad nitride film pattern 85 is formed in a photolithography process using a normal element isolation mask Form. Next, the surface of the pad nitride film 85 pattern is etched by a wet method, and the semiconductor substrate 81 is etched using this as an etching mask to form the trench 87 of FIG. 19. At this time, a gate electrode (not shown) adjacent to the long axis end portion of the active region is spaced apart from the wet etched region 86 during the wet etching process. Referring again to FIG. 19, a trench thermal oxide film 89 is formed on the surface of the trench 87, and a liner nitride film 91 is formed on the entire surface including the trench 87. The four sides of the active region are surrounded by the trench thermal oxide film 89 and the liner nitride film 91. As shown in FIG. 20, an element isolation oxide film (not shown) filling the trench 87 is formed on the entire surface, and is planarized until the pad nitride film 85 is exposed, thereby forming an element isolation film 93 . It is preferable that the planarization etching step is a chemical mechanical polishing method.

後続工程として、湿式食刻された活性領域決定用ＣＶＤ酸化膜１３１を食刻マスクとして半導体基板８１を食刻して図１９のトレンチ８７を形成する。図２９は、図１９乃至従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の他の実施の形態を示す断面図および平面図である。図２９に示されているように、半導体基板８１上にパッド酸化膜８３およびパッド窒化膜（図示省略）を蒸着し、通常の素子分離マスクを用いた写真食刻工程でパッド窒化膜パターン８５を形成する。次には、パッド窒化膜８５パターンの表面を湿式方法で食刻し、これを食刻マスクとして半導体基板８１を食刻して図１９のトレンチ８７を形成する。このとき、湿式食刻工程時に湿式食刻された領域８６ほど活性領域の長軸端部と隣接するゲート電極（図示省略）が離隔される。再び図１９を参照すれば、トレンチ８７の表面にトレンチ熱酸化膜８９を形成し、トレンチ８７を含む全体表面の上部にライナー窒化膜９１を形成する。活性領域の４つの側面は、トレンチ熱酸化膜８９およびライナー窒化膜９１により取り囲まれることになる。図２０に示されているように、トレンチ８７を埋め込む素子分離用酸化膜（図示省略）を全体表面の上部に形成し、パッド窒化膜８５が露出するまで平坦化食刻して素子分離膜９３を形成する。前記の平坦化食刻工程は、化学機械研磨（chemical mechanical polishing）方法であるのが好ましい。

[0020]
As shown in FIG. 21, the element isolation film 93 is etched to a predetermined thickness to protrude the active region to the upper part of the isolation film 93. Hereinafter, the protruding portion of the active region is referred to as a silicon fin 82. The liner nitride film 91 formed on

the four side walls of the silicon fin 82 is exposed by the above etching process. Impurity 95 is ion implanted into the four side walls of the silicon fin 82 in a slanted manner to form a channel region ("97" in FIG. 18). Here, the gradient ion implantation step is preferably performed at a concentration of 10E16 to 10E19 / cm <3>. The liner nitride film 91 and the trench thermal oxide film 89 on the four side walls of the silicon fin 82 are removed as shown in FIG. Next, a gate oxide film 99 is formed on the four side walls of the silicon fins 82 exposed by removing the liner nitride film 91 and the trench thermal oxide film 89.

図２１に示されているように、素子分離膜９３を所定の厚さに食刻して活性領域を素子分離膜９３の上部に突出させる。以下で、前記活性領域の突出された部分をシリコンフィン８２という。前記の食刻工程によりシリコンフィン８２の４つの側壁に形成されたライナー窒化膜９１が露出する。次には、シリコンフィン８２の４つの側壁に不純物９５を傾斜イオン注入してチャンネル領域（図１８の「９７」）を形成する。ここで、前記の傾斜イオン注入工程は１０Ｅ１６～１０Ｅ１９／ｃｍ<3>の濃度で行うのが好ましい。図２２に示されているように、シリコンフィン８２の４つの側壁上のライナー窒化膜９１およびトレンチ熱酸化膜８９を除去する。次には、ライナー窒化膜９１およびトレンチ熱酸化膜８９が除去されて露出したシリコンフィン８２の４つの側壁にゲート酸化膜９９を形成する。

[0021]

Next, a planarized gate electrode polysilicon layer 101 is formed to fill the trench 87 on the entire surface. The silicon fin 82 has a form in which the side wall and the upper portion are surrounded by the gate electrode polysilicon layer 101. Next, a barrier metal layer 103, a metal layer 105, a hard mask nitride film 107, and a hard mask oxide film 109 are sequentially formed on the gate electrode polysilicon layer 101. As shown in FIG. 23, in a photolithography process using a gate electrode mask (not shown), a hard mask oxide film 109, a hard mask nitride film 107, a metal layer 105, a barrier metal layer 103, a poly The silicon layer 101 and the pad nitride film pattern 85 are sequentially etched to form a gate electrode ("110" in FIG. 18) perpendicular to the major axis direction of the silicon fin 82. At this time, the gate electrode 110 on the active region has a laminated structure of the pad nitride film pattern 85, the gate electrode polysilicon layer 101, the barrier metal layer 103, the metal layer 105, the hard mask nitride film 107 and the hard mask oxide film 109 And the gate electrode 110 on the element isolation film 93 has a laminated structure of the gate electrode polysilicon layer 101, the barrier metal layer 103, the metal layer 105, the hard mask nitride film 107, and the hard mask oxide film 109.

次に、全体表面の上部にトレンチ８７を埋め込む平坦化したゲート電極用ポリシリコン層１０１を形成する。シリコンフィン８２は、ゲート電極用ポリシリコン層１０１により側壁および上部が取り囲まれた形態となる。次には、ゲート電極用ポリシリコン層１０１の上部に障壁金属層１０３、金属層１０５、ハードマスク窒化膜１０７およびハードマスク酸化膜１０９を順次形成する。図２３に示されているように、ゲート電極マスク（図示省略）を用いた写真食刻工程

でハードマスク酸化膜１０９、ハードマスク窒化膜１０７、金属層１０５、障壁金属層１０３、ゲート電極用ポリシリコン層１０１およびパッド窒化膜パターン８５を順次食刻してシリコンフィン８２の長軸方向と垂直のゲート電極（図１８の「１１０」）を形成する。このとき、活性領域の上部のゲート電極１１０はパッド窒化膜パターン８５、ゲート電極用ポリシリコン層１０１、障壁金属層１０３、金属層１０５およびハードマスク窒化膜１０７およびハードマスク酸化膜１０９の積層構造でなり、素子分離膜９３上のゲート電極１１０はゲート電極用ポリシリコン層１０１、障壁金属層１０３、金属層１０５およびハードマスク窒化膜１０７およびハードマスク酸化膜１０９の積層構造でなる。

[0022]
Next, after the oxide film 111 is formed on the surface of the gate electrode polysilicon layer 101, a nitride film 113 is formed on the entire surface including the gate electrode 110 to have a constant thickness. Next, an insulating film (not shown) is formed on the entire surface by a material having excellent flowability like BPSG, and then planarization etching is performed until the nitride film 113 is exposed to form the lower insulating film 115 . As shown in FIG. 24, the lower insulating layer 115 and the nitride film 113 are anisotropically etched in a photolithography process using a landing plug contact mask (not shown), thereby exposing the pad oxide film 83 To form self-aligned landing plug contact hole 117. The anisotropic etching step is performed in an over-etching process so that the hard mask oxide film 109 and the nitride film 113 on the surface of the gate oxide film 99 are all removed. Spacers are formed on the side walls of the gate electrode by the anisotropic etching process. Next, LDD impurities and halo impurities are ion-implanted into the bottom of the landing plug contact hole 117. At this time, the halo impurity ion implantation step may not be performed in some cases.

次には、ゲート電極用ポリシリコン層１０１の表面に酸化膜１１１を形成した後、ゲート電極１１０を含む全体表面の上部に窒化膜１１３を一定の厚さに形成する。次に、全体表面の上部にＢＰＳＧのように流動性に優れた物質で絶縁膜（図示省略）を形成した後、窒化膜１１３が露出するまで平坦化食刻して下部絶縁膜１１５を形成する。図２４に示されているように、ランディングプラグコンタクトマスク（図示省略）を用いた写真食刻工程で下部絶縁層１１５および窒化膜１１３を異方性食刻することにより、パッド酸化膜８３を露出させる自己整合的なランディングプラグコンタクトホール１１７を形成する。前記の異方性食刻工程は、ハードマスク酸化膜１０９およびゲート酸化膜９９表面の窒化膜１１３が全て除去されるよう過度食刻工程で行う。前記の異方性食刻工程によりゲート電極の側壁にはスペーサが形成される。次に、ランディングプラグコンタクトホール１１７の底部にＬＤＤ不純物およびハロー不純物をイオン注入する。このとき、ハロー不純物のイオン注入工程は行わないこともある。

[0023]
The pad oxide film 83 on the upper surface of the semiconductor substrate 81 and the gate oxide film 99 on the side wall of the pad oxide film 83 exposed between the nitride film 113 spacers

are removed by a wet etching process as shown in FIG. 25 . Next, a landing plug polysilicon layer (not shown) filling the landing plug contact hole 117 is formed on the entire surface, planarized so as to expose the hard mask nitride film 107 to form a landing plug 121 . It is preferable that the planarization etching step is performed by a CMP step or an etch-back step. Impurities contained in the landing plug 121 are diffused into the silicon fins 82 to form the source / drain regions 123. The transistor of the semiconductor element in FIG. 25 is defined by a trench type element isolation film 93 and includes an I type active region including a silicon fin 82 protruding above the trench type element isolation film 93. A gate oxide film 99 is formed on the side wall of the silicon fin 82. A pad insulating film having a laminated structure of a pad oxide film 83 and a pad nitride film 85 is formed at the interface between the upper surface of the silicon fin 82 and the lower surface of the gate electrode Are provided. Further, the gate electrode extends in a direction perpendicular to the I-type active region, and the upper part thereof is planarized. Source / drain regions 123 are provided on the silicon fins 82 between the gate electrodes and on the sidewalls of the ends of the silicon fins, and the channel regions are provided on the side walls of the silicon fins 82 below the gate electrodes .

図２５に示されているように、窒化膜１１３スペーサの間に露出する半導体基板８１表面の上部のパッド酸化膜８３とパッド酸化膜８３の側壁のゲート酸化膜９９を湿式食刻工程で除去する。次には、ランディングプラグコンタクトホール１１７を埋め込むランディングプラグ用ポリシリコン層（図示省略）を全体表面の上部に形成し、ハードマスク窒化膜１０７が露出するよう平坦化食刻してランディングプラグ１２１を形成する。前記の平坦化食刻工程は、ＣＭＰ工程またはエッチバック工程で行うのが好ましい。ランディングプラグ１２１に含まれた不純物がシリコンフィン８２に拡散されてソース／ドレイン領域１２３が形成される。図２５の半導体素子のトランジスタは、トレンチ型素子分離膜９３により定義され、トレンチ型素子分離膜９３の上部に突出されるシリコンフィン８２を含むＩ型活性領域を含む。シリコンフィン８２の側壁にはゲート酸化膜９９が形成されており、シリコンフィン８２の上部面とゲート電極の下部面の界面にはパッド酸化膜８３およびパッド窒化膜８５の積層構造でなるパッド絶縁膜が備えられている。さらに、ゲート電極はＩ型活性領域と垂直の方向に延びられてその上部が平坦化されている。前記ゲート電極の間のシリコンフィン８２および前記シリコンフィンの端部の側壁にはソース／ドレイン領域１２３が備えられており、チャンネル領域は前記ゲート電極の下部のシリコンフィン８２の側壁に備えられている。

[0024]

FIG. 26 is a cross-sectional view taken along the line B - B of FIG. 25. As shown in FIG. 26, the channel width of the transistor of the semiconductor element according to the present invention is twice (2 h) the height (h) of the silicon fin 82 protruding above the element isolation film 93, The channel width is larger than that of the conventional transistor in which the shortened length of the active region is the channel width, the current driving capability is increased, and the short channel effect can be prevented.

図２６は、図２５のＢ－Ｂ切断面に沿った断面図である。図２６に示されているように、本発明に係る半導体素子のトランジスタのチャンネル幅は、素子分離膜９３の上部に突出されたシリコンフィン８２の高さ（ｈ）の２倍（２ｈ）となり、活性領域の短縮長さがチャンネル幅になる従来のトランジスタよりチャンネル幅が大きくなり、電流駆動力が増加してショートチャンネル効果を防止することができる。

[0025]
1 is a layout diagram of a semiconductor device according to a conventional technique. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 1. FIG. 2 is a layout diagram of a semiconductor device according to another conventional technique. FIG. 10 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 10. FIG. 10 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 10. FIG. 10 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 10. FIG. 10 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 10. FIG. 10 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 10. FIG. 10 is a cross-sectional view showing a transistor forming method of a semiconductor element according to the conventional technique of FIG. 10. 1 is a layout diagram of a semiconductor device according to the present invention. FIG. 2 is a perspective view showing a transistor of a semiconductor element formed according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present

invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. FIG. 1 is a cross-sectional view showing a transistor forming method of a semiconductor element according to an embodiment of the present invention. Sectional view showing one embodiment of a method of forming an active region according to the present invention having a major axis smaller than the major axis length of the active region of the prior art.

従来の技術に係る半導体素子のレイアウト図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 他の従来の技術に係る半導体素子のレイアウト図である。 図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明に係る半導体素子のレイアウト図である。 本発明の実施の形態に基づき形成された半導体素子のトランジスタを示す斜視図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。 従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の１つの実施の形態を示す断面図である。

1 is a plan view showing one embodiment of a method of forming an active region according to the invention with a major axis smaller than the length of the major axis of the active region of the prior art. Sectional view showing another embodiment of a method for forming an active region according to the present invention having a major axis smaller than the major axis length

of the active region of FIG.

従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の１つの実施の形態を示す平面図である。図１９乃至従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の他の実施の形態を示す断面図である。

Explanation of sign

符号の説明

[0026]

81 semiconductor substrate 82 silicon fin 83, 85 pad insulation film 86, 133 wet etched region 87 element isolation trench 89 trench thermal oxide film 91 liner nitride film 93 element isolation film 95 impurity 97 channel region 99 gate oxide film 101 gate Electrode polysilicon layer 103 barrier metal layer 105 metal layer 107 hard mask nitride film 109 hard mask oxide film 110 gate electrode 111 oxide film 113 nitride film 115 lower insulating layer 117 landing plug contact hole 121 landing plug 123 source / drain region 131 CVD Oxide pattern 800 active region 900 element isolation region 1000 gate region 1100 contact region

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８１ 半導体基板 ８２ シリコンフィン ８３、８５ パッド絶縁膜 ８６、１３３ 湿式食刻された領域 ８７ 素子分離用トレンチ ８９ トレンチ熱酸化膜 ９１ ライナー窒化膜 ９３ 素子分離膜 ９５ 不純物 ９７ チャンネル領域 ９９ ゲート酸化膜 １０１ ゲート電極用ポリシリコン層 １０３ 障壁金属層 １０５ 金属層 １０７ ハードマスク窒化膜 １０９ ハードマスク酸化膜 １１０ ゲート電極 １１１ 酸化膜 １１３ 窒化膜 １１５ 下部絶縁層 １１７ ランディングプラグコンタクトホール １２１ ランディングプラグ １２３ ソース／ドレイン領域 １３１ ＣＶＤ酸化膜パターン ８００ 活性領域 ９００ 素子分離領域 １０００ ゲート領域 １１００ コンタクト領域

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CLAIMS JP2005136376

1.

(A) patterning a semiconductor substrate having a stacked structure of a pad oxide film and a pad nitride film to form a trench type element isolation film defining an I type active region, (b) forming a trench isolation film having a predetermined thickness (C) forming a channel region by gradient ion implantation of an impurity into a side wall of the silicon fin; (d) forming a channel region of the silicon Forming a gate oxide film on the side wall of the fin, (e) forming a planarized conductive layer for the gate electrode on the entire surface, (f) patterning the conductive layer for the gate electrode and the pad nitride film (G) forming a lower insulating layer having a landing plug contact hole, (h) performing an ion implantation process to form the Randy (I) exposing the pad oxide film exposed through the landing plug contact hole to expose the silicon fin, and (j) exposing the landing plug And forming a landing plug to fill the contact hole.

（ａ）パッド酸化膜とパッド窒化膜の積層構造を有する半導体基板をパターニングしてＩ型活性領域を定義するトレンチ型素子分離膜を形成する段階、（ｂ）前記素子分離膜を所定の厚さに食刻して前記素子分離膜の上部に突出されるシリコンフィンを形成する段階、（ｃ）前記シリコンフィンの側壁に不純物を傾斜イオン注入してチャンネル領域を形成する段階、（ｄ）前記シリコンフィンの側壁にゲート酸化膜を形成する段階、（ｅ）全体表面の上部に平坦化したゲート電極用導電層を形成する段階、（ｆ）前記ゲート電極用導電層および前記パッド窒化膜をパターニングしてゲート電極を形成する段階、（ｇ）ランディングプラグコンタクトホールを備えた下部絶縁層を形成する段階、（ｈ）イオン注入工程を行って前記ランディングプラグコンタクトホールの底部に不純物注入領域を形成する段階、（ｉ）前記ランディングプラグコンタクトホールを介して露出したパッド酸化膜を食刻してシリコンフィンを露出させる段階、および（ｊ）前記ランディングプラグコンタクトホールを埋め込むランディングプラグを形成する段階 を含むことを特徴とする半導体素子のトランジスタ形成方法。

2.

The step (a) may include forming a stacked structure of a pad oxide film and a pad nitride film on a semiconductor substrate, using an exposure mask defining an active region spaced apart from the region planned as an adjacent gate electrode by a predetermined distance Forming a photoresist pattern defining an I-type active region by performing an exposure and development process that has been performed, etching the semiconductor substrate using the photoresist pattern as an etching mask, forming a trench, And forming the trench type device isolation film to fill the trenches for the semiconductor device according to claim 1.

前記（ａ）段階は、 半導体基板上にパッド酸化膜とパッド窒化膜の積層構造を形成する段階、 隣接するゲート電極として予定された領域と所定距離離隔された活性領域を定義する露光マスクを用いた露光および現像工程を行い、 Ｉ型活性領域を定義するフォトレジストパターンを形成する段階、 前記フォトレジストパターンを食刻マスクとして前記半導体基板を食刻し、トレンチを形成する段階、および 前記素子分離用トレンチを埋め込む前記トレンチ型素子分離膜を形成する段階 を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

3.

The step (a) may include forming a stacked structure of a pad oxide film and a pad nitride film on a semiconductor substrate, forming a CVD oxide film on the pad nitride film, performing a photolithography process using an element isolation mask Etching the CVD oxide film to form a CVD oxide film pattern, wet etching the surface of the CVD oxide film pattern, using the wet etched CVD oxide film pattern as a mask, Forming a trench having a predetermined depth by etching a pad nitride film, a pad oxide film, and a semiconductor substrate; and forming a trench type device isolation film filling the trench And forming a gate insulating film on the semiconductor layer.

前記（ａ）段階は、 半導体基板上にパッド酸化膜とパッド窒化膜の積層構造を形成する段階、 前記パッド窒化膜の上部にＣＶＤ酸化膜を形成する段階、 素子分離マスクを用いた写真食刻工程で前記ＣＶＤ酸化膜を食刻し、ＣＶＤ酸化膜パターンを形成する段階、 前記ＣＶＤ酸化膜パターンの表面を湿式食刻する段階、 前記表面が湿式食刻されたＣＶＤ酸化膜パターンをマスクとして前記パッド窒化膜、パッド酸化膜および半導体基板を食刻して所定深さのトレンチを形成する段階、および 前記トレンチを埋め込むトレンチ型素子分離膜を形成する段階 を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

4.

The step (a) may include forming a stacked structure of a pad oxide layer and a pad nitride layer on a semiconductor substrate, etching the pad nitride layer in a photolithography process using an isolation mask, Wet etching the surface of the pad nitride film pattern, wet etching the surface of the pad nitride film pattern, etching the pad oxide film and the semiconductor substrate using the wet-etched pad nitride film pattern as a mask, 2. The method of claim 1, further comprising:

forming a trench; and forming the trench type device isolation layer to fill the trench.

前記（ａ）段階は、 半導体基板上にパッド酸化膜とパッド窒化膜の積層構造を形成する段階、 素子分離マスクを用いた写真食刻工程で前記パッド窒化膜を食刻し、パッド窒化膜パターンを形成する段階、 前記パッド窒化膜パターンの表面を湿式食刻する段階、 前記表面が湿式食刻されたパッド窒化膜パターンをマスクとして前記パッド酸化膜および半導体基板を食刻して所定深さのトレンチを形成する段階、および 前記トレンチを埋め込む前記トレンチ型素子分離膜を形成する段階、 を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

5.

5. The method of claim 2, further comprising the step of forming a thermal oxide film and a liner nitride film on the surface of the trench after forming the trench.

前記トレンチを形成した後、トレンチの表面に熱酸化膜およびライナー窒化膜を形成する段階をさらに含むことを特徴とする請求項２～４の何れかに記載の半導体素子のトランジスタ形成方法。

6.

2. The method of claim 1, wherein the gradient ion implantation process is performed at a doping concentration of 10E16 to 10E19 / cm <3>.

前記傾斜イオン注入工程は１０Ｅ１６～１０Ｅ１９／ｃｍ<3>のドーピング濃度で行うことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

7.

2. The method of claim 1, wherein the gate oxide film has a thickness of 50 to 100 Å.

前記ゲート酸化膜の厚さは５０～１００Åであることを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

8.

The step (h) may include forming an LDD region by implanting an LDD impurity into a bottom portion of the landing plug contact hole, and forming a halo impurity region by ion implanting a halo impurity 2. The method for forming a transistor of a semiconductor device according to claim 1,

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前記（ｈ）段階は、前記ランディングプラグコンタクトホールの底部にＬＤＤ用不純物を注入し

てＬＤＤ領域を形成する段階、およびハロー不純物をイオン注入してハロー不純物領域を形成する段階を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

9.
The method according to claim 1, wherein the step (j) further comprises diffusing an impurity contained in the landing plug with the silicon fin to form a source / drain region. 6.

前記（ｊ）段階は、前記ランディングプラグに含まれた不純物を前記シリコンフィンで不純物を拡散させ、ソース／ドレイン領域を形成する段階をさらに含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

10.
The method of claim 1, wherein the gate electrode further includes a stacked structure of a barrier metal layer, a metal layer, a hard mask nitride film, and a hard mask oxide film planarized thereon .

前記ゲート電極は、その上部に平坦化した障壁金属層、金属層、ハードマスク窒化膜およびハードマスク酸化膜の積層構造をさらに含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

11.
The step (g) may include forming a spacer nitride layer on the entire surface, forming a planarized insulating layer on the spacer nitride layer, and performing a full surface etching process by the SAC method 2. The method of claim 1, further comprising forming a lower insulating layer having a nitride film spacer and a landing plug contact hole.

前記（ｇ）段階は、 全体表面の上部にスペーサ用窒化膜を形成する段階、 前記スペーサ用窒化膜の上部に平坦化した絶縁層を形成する段階、およびＳＡＣ方法で全面食刻工程を行って窒化膜スペーサおよびランディングプラグコンタクトホールを備えた下部絶縁層を形成する段階 を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

12.
The method of claim 11, wherein the entire surface etching step is an over-etching step of removing all of the pad oxide film and the nitride film above the gate oxide film.

前記全面食刻工程は、前記パッド酸化膜およびゲート酸化膜の上部の窒化膜を全て除去する過度食刻工程であることを特徴とする請求項１１に記載の半導体素子のトランジスタ形成方法。

13.

2. The method of claim 1, wherein the pad oxide layer has a thickness of 50 to 200 Å.

前記パッド酸化膜の厚さは５０～２００Åであることを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

14.

2. The method of claim 1, wherein the pad nitride film has a thickness of 100 to 400 Å.

前記パッド窒化膜の厚さは１００～４００Åであることを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。

15.

An I type active region defined by a trench type device isolation film and including silicon fins protruding above the trench type device isolation film, a gate oxide film provided on a side wall of the silicon fin, , A pad insulating film provided at the interface between the upper surface of the silicon fin and the lower surface of the gate electrode, a silicon fin between the gate electrode and the silicon fin between the gate electrode and the silicon fin A source / drain region provided on a sidewall of the end portion, and a channel region provided on a sidewall of the silicon fin below the gate electrode.

トレンチ型素子分離膜により定義され、前記トレンチ型素子分離膜の上部に突出されるシリコンフィンを含むＩ型活性領域、前記シリコンフィンの側壁に備えられたゲート酸化膜、前記Ｉ型活性領域と垂直の方向に延びられ、その上部が平坦なゲート電極、前記シリコンフィンの上部面とゲート電極の下部面との界面に備えられたパッド絶縁膜、前記ゲート電極の間のシリコンフィンおよび前記シリコンフィンの端部の側壁に備えられたソース／ドレイン領域、および 前記ゲート電極の下部のシリコンフィンの側壁に備えられるチャンネル領域 を含むことを特徴とする半導体素子のトランジスタ。

16.

16. The transistor of a semiconductor device according to claim 15, further comprising a thermal oxide film and a liner nitride film at an interface between the trench type element isolation film and the I type active region.

前記トレンチ型素子分離膜と前記Ｉ型活性領域との界面に熱酸化膜およびライナー窒化膜をさらに有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。

17.

16. The transistor of a semiconductor device according to claim 15, wherein the pad insulating film has a stacked structure of a pad oxide film and a pad nitride film.

前記パッド絶縁膜は、パッド酸化膜とパッド窒化膜の積層構造を有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。

18.

The transistor of claim 17, wherein the pad oxide layer and the pad nitride layer have thicknesses of 50 to 200 Å and 100 to 400 Å, respectively.

前記パッド酸化膜およびパッド窒化膜の厚さは、それぞれ５０～２００Åおよび１００～４００Åであることを特徴とする請求項１７に記載の半導体素子のトランジスタ。

19.

16. The transistor of a semiconductor device according to claim 15, further comprising an insulating film spacer on a side wall of the gate electrode.

前記ゲート電極の側壁に絶縁膜スペーサをさらに有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。

20.

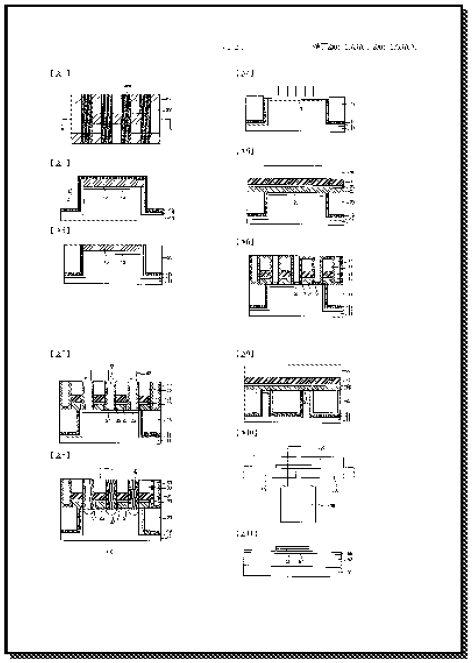
16. The transistor of a semiconductor device according to claim 15, wherein the gate electrode has a stacked structure of a polysilicon layer, a barrier metal layer, a metal layer, a hard mask nitride film, and a hard mask oxide film.

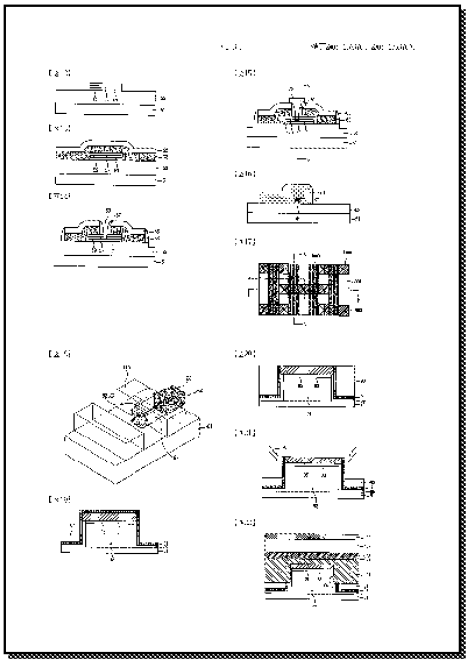
前記ゲート電極はポリシリコン層、障壁金属層、金属層、ハードマスク窒化膜およびハードマスク酸化膜の積層構造を有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。

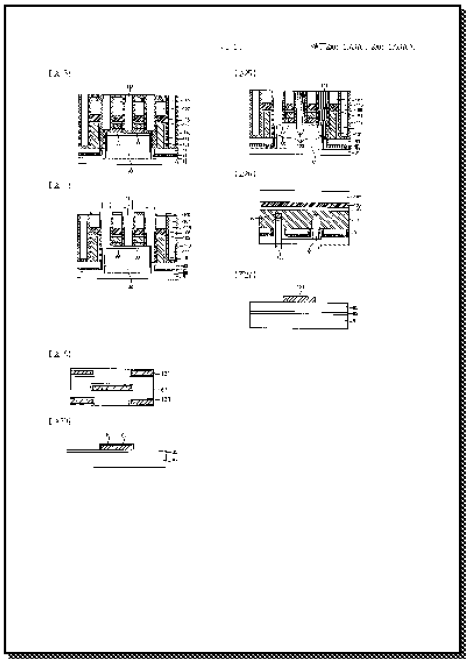
21.

16. The transistor of claim 15, wherein the thickness of the gate oxide film is 50 to 100 Å.

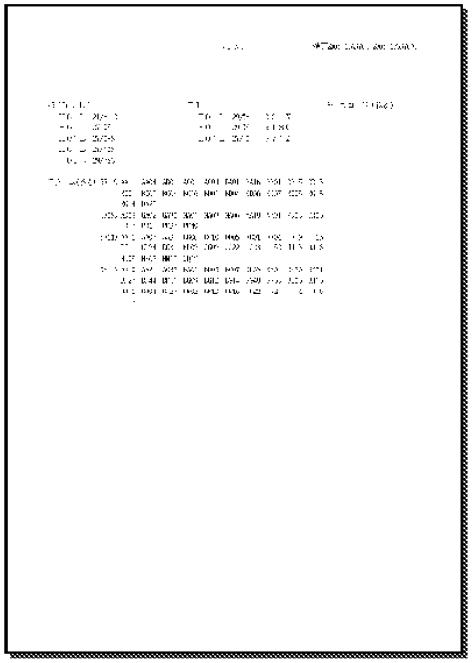
前記ゲート酸化膜の厚さは５０～１００Åであることを特徴とする請求項１５に記載の半導体素子のトランジスタ。







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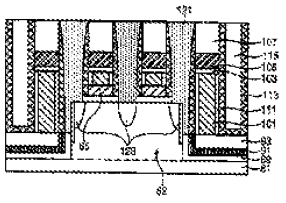
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(54)【発明の名称】半導体素子のトランジスタおよびその形成方法

(57)【要約】
【課題】チャンネル領域を素子分離膜の上部に突出された活性領域の側壁に形成し、ランディングプラグとのコンタクトを突出した活性領域の長軸方向の側壁まで拡張してショートチャンネル効果を改善し、コンタクト抵抗を減少させることができる半導体素子のトランジスタおよびその形成方法を提供する。
【解決手段】素子分離酸化膜を食刻して突出されたシリコンフィンを形成し、傾斜イオン注入でシリコンフィンの側壁にチャンネル領域を形成したあと上部が平坦化したゲート電極とソース／ドレイン領域を形成する。
【選択図】図２５



【特許請求の範囲】
【請求項1】
（ａ）パッド酸化膜とパッド窒化膜の積層構造を有する半導体基板をパターニングしてＩ型活性領域を定義するトレンチ型素子分離膜を形成する段階、
（ｂ）前記素子分離膜を所定の厚さに食刻して前記素子分離膜の上部に突出されるシリコンフィンを形成する段階、
（ｃ）前記シリコンフィンの側壁に不純物を傾斜イオン注入してチャンネル領域を形成する段階、
（ｄ）前記シリコンフィンの側壁にゲート酸化膜を形成する段階、
（ｅ）全体表面の上部に平坦化したゲート電極用導電層を形成する段階、
（ｆ）前記ゲート電極用導電層および前記パッド窒化膜をパターニングしてゲート電極を形成する段階、
（ｇ）ランディングプラグコンタクトホールを備えた下部絶縁層を形成する段階、
（ｈ）イオン注入工程を行って前記ランディングプラグコンタクトホールの底部に不純物注入領域を形成する段階、
（ｉ）前記ランディングプラグコンタクトホールを介して露出したパッド酸化膜を食刻してシリコンフィンを露出させる段階、および
（ｊ）前記ランディングプラグコンタクトホールを埋め込むランディングプラグを形成する段階
を含むことを特徴とする半導体素子のトランジスタ形成方法。
【請求項2】
前記（ａ）段階は、
半導体基板上にパッド酸化膜とパッド窒化膜の積層構造を形成する段階、
隣接するゲート電極として予定された領域と所定距離離隔された活性領域を定義する露光マスクを用いた露光および現像工程を行い、Ｉ型活性領域を定義するフォトレジストパターンを形成する段階、
前記フォトレジストパターンを食刻マスクとして前記半導体基板を食刻し、トレンチを形成する段階、および
前記素子分離用トレンチを埋め込む前記トレンチ型素子分離膜を形成する段階
を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項3】
前記（ａ）段階は、
半導体基板上にパッド酸化膜とパッド窒化膜の積層構造を形成する段階、
前記パッド窒化膜の上部にＣＶＤ酸化膜を形成する段階、
素子分離マスクを用いた写真食刻工程で前記ＣＶＤ酸化膜を食刻し、ＣＶＤ酸化膜パターンを形成する段階、
前記ＣＶＤ酸化膜パターンの表面を湿式食刻する段階、
前記表面が湿式食刻されたＣＶＤ酸化膜パターンをマスクとして前記パッド窒化膜、パッド酸化膜および半導体基板を食刻して所定深さのトレンチを形成する段階、および
前記トレンチを埋め込むトレンチ型素子分離膜を形成する段階
を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項4】
前記（ａ）段階は、
半導体基板上にパッド酸化膜とパッド窒化膜の積層構造を形成する段階、
素子分離マスクを用いた写真食刻工程で前記パッド窒化膜を食刻し、パッド窒化膜パターンを形成する段階、
前記パッド窒化膜パターンの表面を湿式食刻する段階、
前記表面が湿式食刻されたパッド窒化膜パターンをマスクとして前記パッド酸化膜および半導体基板を食刻して所定深さのトレンチを形成する段階、および

前記トレンチを埋め込む前記トレンチ型素子分離膜を形成する段階、
を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項5】
前記トレンチを形成した後、トレンチの表面に熱酸化膜およびライナー窒化膜を形成する段階をさらに含むことを特徴とする請求項２～４の何れかに記載の半導体素子のトランジスタ形成方法。
【請求項6】
前記傾斜イオン注入工程は１０Ｅ１６～１０Ｅ１９／ｃｍ^{3}のドーピング濃度で行うことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項7】
前記ゲート酸化膜の厚さは５０～１００Åであることを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項8】
前記（ｈ）段階は、前記ランディングプラグコンタクトホールの底部にＬＤＤ用不純物を注入してＬＤＤ領域を形成する段階、およびハロー不純物をイオン注入してハロー不純物領域を形成する段階を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項9】
前記（ｊ）段階は、前記ランディングプラグに含まれた不純物を前記シリコンフィンで不純物を拡散させ、ソース／ドレイン領域を形成する段階をさらに含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項10】
前記ゲート電極は、その上部に平坦化した障壁金属層、金属層、ハードマスク窒化膜およびハードマスク酸化膜の積層構造をさらに含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項11】
前記（ｇ）段階は、
全体表面の上部にスペーサ用窒化膜を形成する段階、
前記スペーサ用窒化膜の上部に平坦化した絶縁層を形成する段階、および
ＳＡＣ方法で全面食刻工程を行って窒化膜スペーサおよびランディングプラグコンタクトホールを備えた下部絶縁層を形成する段階
を含むことを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項12】
前記全面食刻工程は、前記パッド酸化膜およびゲート酸化膜の上部の窒化膜を全て除去する過度食刻工程であることを特徴とする請求項１１に記載の半導体素子のトランジスタ形成方法。
【請求項13】
前記パッド酸化膜の厚さは５０～２００Åであることを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項14】
前記パッド窒化膜の厚さは１００～４００Åであることを特徴とする請求項１に記載の半導体素子のトランジスタ形成方法。
【請求項15】
トレンチ型素子分離膜により定義され、前記トレンチ型素子分離膜の上部に突出されるシリコンフィンを含むＩ型活性領域、
前記シリコンフィンの側壁に備えられたゲート酸化膜、
前記Ｉ型活性領域と垂直の方向に延びられ、その上部が平坦なゲート電極、
前記シリコンフィンの上部面とゲート電極の下部面との界面に備えられたパッド絶縁膜、
前記ゲート電極の間のシリコンフィンおよび前記シリコンフィンの端部の側壁に備えら

れたソース／ドレイン領域、および
　前記ゲート電極の下部のシリコンフィンの側壁に備えられるチャンネル領域
を含むことを特徴とする半導体素子のトランジスタ。
【請求項16】
　前記トレンチ型素子分離膜と前記Ｉ型活性領域との界面に熱酸化膜およびライナー窒化膜をさらに有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。
【請求項17】
　前記パッド絶縁膜は、パッド酸化膜とパッド窒化膜の積層構造を有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。
【請求項18】
　前記パッド酸化膜およびパッド窒化膜の厚さは、それぞれ５０～２００Åおよび１００～４００Åであることを特徴とする請求項１７に記載の半導体素子のトランジスタ。
【請求項19】
　前記ゲート電極の側壁に絶縁膜スペーサをさらに有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。
【請求項20】
　前記ゲート電極はポリシリコン層、障壁金属層、金属層、ハードマスク窒化膜およびハードマスク酸化膜の積層構造を有することを特徴とする請求項１５に記載の半導体素子のトランジスタ。
【請求項21】
　前記ゲート酸化膜の厚さは５０～１００Åであることを特徴とする請求項１５に記載の半導体素子のトランジスタ。
【発明の詳細な説明】
【技術分野】
【0001】
　本発明は、チャンネル領域を素子分離膜の上部に突出された活性領域の側壁に形成し、ランディングプラグとのコンタクトを突出した活性領域の長軸方向の側壁まで拡張してショートチャンネル効果を改善し、コンタクト抵抗を減少させることができる半導体素子のトランジスタおよびその形成方法に関する。
【背景技術】
【0002】
　ＤＲＡＭは１つのトランジスタと１つのキャパシタで構成され、前記のトランジスタはデザインルールの減少に伴いセルトランジスタのチャンネル長さが減少することになった。
　前記のチャンネル長さの減少によりショートチャンネル効果が増加し、セルトランジスタの特性を変化させることになった。
【0003】
　図１は、従来の技術に係る半導体素子のレイアウト図である。これは、活性領域２００を定義する素子分離領域３００を形成するが、活性領域２００の長軸端部がゲート領域４００と隣接することを示したものである。
　図２～図９は、図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す図である。図２～図８は、図１のＡ－Ａ切断面に沿って示す断面図である。図９は、図８のＢ－Ｂ切断面に沿って示す断面図である。
　図２に示されているように、半導体基板１１にウェル（図示省略）を形成する。次には、半導体基板１１上にパッド酸化膜１３およびパッド窒化膜１５を順次形成する。
　次に、素子分離マスク（図示省略）を用いた写真食刻工程で素子分離領域に予定された部分のパッド窒化膜１５、パッド酸化膜１３および所定厚さの半導体基板１１を食刻してトレンチ２１を形成する。
【0004】
　次には、トレンチ２１の表面にトレンチ熱酸化膜１７を形成してトレンチ２１を含む全体表面の上部にライナー窒化膜１９を形成する。

図３に示されているように、トレンチ２１を埋め込む素子分離用酸化膜を全体表面の上部に形成し、パッド窒化膜１５が露出するまでＣＭＰ方法で平坦化食刻して素子分離膜２３を形成する。

図４に示されているように、素子分離膜２３により露出したパッド窒化膜１５およびライナー窒化膜１９を、好ましくは湿式食刻工程で除去する。このとき、前記の湿式食刻工程はリン酸溶液を用いて行う。

次には、半導体基板１１にウェルおよびチャンネル形成用イオン注入工程を行う。

図５に示されているように、パッド酸化膜１３を湿式方法で除去して露出した半導体基板１１の表面の活性領域にゲート酸化膜２５を形成する。

ゲート酸化膜２５上にゲート電極用ポリシリコン層２７、ＷＮ層を含む障壁金属層２９、タングステン層を含む金属層３１および窒化膜からなるハードマスク層３３を順次形成する。

図６に示されているように、ゲート電極マスク（図示省略）を用いた写真食刻工程でハードマスク層３３、金属層３１、障壁金属層２９およびゲート電極用ポリシリコン層２７を順次食刻してゲート電極を形成する。

次には、ゲート電極用ポリシリコン層２７の側壁にのみ選択的に酸化膜３５を形成する。

【0005】

次に、前記のゲート電極を含む全体表面の上部に窒化膜３７を一定の厚さに形成した後、全体表面の上部に平坦化した下部絶縁層３９を形成する。このとき、下部絶縁層３９はＢＰＳＧ（Boron Phosphorus Silicate Glass）のように流動性に優れた絶縁酸化物質で形成する。

窒化膜３７を食刻障壁にＣＭＰ工程を行って窒化膜３７が露出するよう下部絶縁層３９を平坦化食刻する。

図７に示されているように、ランディングプラグコンタクトマスク（図示省略）を用いた写真食刻工程で下部絶縁層３９および窒化膜３７を異方性食刻することにより、窒化膜スペーサと自己整合的なランディングプラグコンタクトホール４１を形成する。

次に、ランディングプラグコンタクトホール４１により露出した半導体基板にＬＤＤイオン注入工程とハローイオン注入工程を行ってソース／ドレイン領域４４を形成する。

図８および図９に示されているように、ランディングプラグコンタクトホール４１を埋め込むランディングプラグ用ポリシリコン層（図示省略）を全体表面の上部に形成し、ハードマスク層３３が露出するよう平坦化食刻してランディングプラグコンタクトホール４１を埋め込むランディングプラグ４３を形成する。

【0006】

前述の従来の技術に係る半導体素子の形成方法では、デザインルールの減少に伴いチャンネル長さが減少することになり、ショートチャンネル効果が発生することになる。このような問題点を改善するためチャンネルの不純物濃度を増加させる方法が提案されたが、不純物の濃度を増加させる方法は電界を増加させて結果的に漏洩電流を増加させ、ＤＲＡＭのリフレッシュタイム特性を悪化させるという問題点がある。

さらに、デザインルールの減少に伴うチャンネル幅の減少は電流駆動力を低下させる。デザインルールの減少に伴い、セルトランジスタのソース／ドレイン電極であるランディングプラグと基板表面の接続面積が減少することになるので、コンタクト抵抗が増加して駆動電流をさらに減少させることになる。

【0007】

図１０は、他の従来の技術に係る半導体素子のレイアウト図である。これはＳＯＩ（Silicon On Insulator）基板に形成したフィン型電界効果トランジスタを示したものである。

図１０に示されているように、ソース／ドレイン領域５００の間を連結するシリコンフィン領域６００がチャンネルに用いられ、シリコンフィン領域６００の上部にゲート電極領域７００が備えられている。

【0008】
図１１～図１６は、図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す図である。図１１～図１５は、図１０のＡ－Ａ切断面に沿って示す断面図である。図１６は、図１５のＢ－Ｂ切断面に沿って示す断面図である。
図１１に示されているように、半導体基板５１上に埋込み酸化膜５３およびシリコンボディ５５が積層されているＳＯＩウェーハ上に第１の窒化膜（図示省略）および第１の酸化膜（図示省略）を順次形成した後、前記第１の酸化膜および第１の窒化膜をパターニングして第１の酸化膜パターン５９および第１の窒化膜パターン５７を形成する。
図１２に示されているように、第１の酸化膜パターン５９をマスクとしてシリコンボディ５５を食刻してシリコンフィン（Ｓｉ－ｆｉｎ）６１を形成する。シリコンフィン６１は、トランジスタのチャンネルの役割を果たす。
図１３に示されているように、全体表面の上部にポリシリコン層６３と第２の酸化膜６５を順次形成する。ここで、ポリシリコン層６３はトランジスタのソース／ドレイン接合領域に用いられる。
図１４に示されているように、第２の酸化膜６５およびポリシリコン層６３の積層構造をパターニングしてゲート領域を定義する溝６９を形成する。
【0009】
次には、全体表面の上部に第３の酸化膜（図示省略）を蒸着し、異方性食刻して溝６９の側壁に酸化膜スペーサ６７を形成する。前記の異方性食刻工程は過度食刻工程で、酸化膜スペーサ６７により露出した第１の酸化膜５９および第１の窒化膜５７を食刻してシリコンフィン６１を露出させると共に所定厚さの埋込み酸化膜５３を食刻する。
図１５および図１６に示されているように、前記露出したシリコンフィン６１上にゲート酸化膜７１を形成したあと溝６９を埋め込むゲート電極７３を多結晶ＳｉＧｅに形成する。
前述の他の従来の技術に係る半導体素子の形成方法ではショートチャンネル効果を減少させることはできるが、ＳＯＩウェーハを用いることによりウェーハ費用が増加し、素子のリフレッシュ特性が減少して素子の特性が劣化するという問題点がある。
【発明の開示】
【発明が解決しようとする課題】
【0010】
本発明は、単結晶シリコン基板を用いながらもショートチャンネル効果特性を改善して電流駆動力を増加させることができ、素子のリフレッシュ特性を向上させることができる半導体素子のトランジスタおよびその形成方法を提供することに目的がある。
【課題を解決するための手段】
【0011】
本発明に係る半導体素子のトランジスタ形成方法は、（ａ）パッド酸化膜とパッド窒化膜の積層構造を有する半導体基板をパターニングしてＩ型活性領域を定義するトレンチ型素子分離膜を形成する段階と、（ｂ）前記素子分離膜を所定の厚さに食刻して前記素子分離膜の上部に突出されるシリコンフィンを形成する段階と、（ｃ）前記シリコンフィンの側壁に不純物を傾斜イオン注入してチャンネル領域を形成する段階と、（ｄ）前記シリコンフィンの側壁にゲート酸化膜を形成する段階と、（ｅ）全体表面の上部に平坦化したゲート電極用導電層を形成する段階と、（ｆ）前記ゲート電極用導電層および前記パッド窒化膜をパターニングしてゲート電極を形成する段階と、（ｇ）ランディングプラグコンタクトホールを備えた下部絶縁層を形成する段階と、（ｈ）イオン注入工程を行って前記ランディングプラグコンタクトホールの底部に不純物注入領域を形成する段階と、（ｉ）前記ランディングプラグコンタクトホールを介して露出したパッド酸化膜を食刻してシリコンフィンを露出させる段階、および（ｊ）前記ランディングプラグコンタクトホールを埋め込むランディングプラグを形成する段階を含むことを特徴とする。
【0012】
本発明に係る半導体素子のトランジスタはトレンチ型素子分離膜により定義され、前記

トレンチ型素子分離膜の上部に突出されるシリコンフィンを含むＩ型活性領域と、前記シリコンフィンの側壁に備えられたゲート酸化膜と、前記Ｉ型活性領域と垂直の方向に延びられその上部が平坦なゲート電極と、前記シリコンフィンの上部面とゲート電極の下部面との界面に備えられたパッド絶縁膜と、前記ゲート電極の間のシリコンフィンおよび前記シリコンフィンの端部の側壁に備えられたソース／ドレイン領域、および前記ゲート電極の下部のシリコンフィンの側壁に備えられるチャンネル領域を含むことを特徴とする。

【発明の効果】

【0013】

本発明に係る半導体素子のトランジスタおよびその形成方法は、チャンネル領域を素子分離膜の上部に突出された活性領域の側壁に形成し、ランディングプラグとのコンタクトを突出した活性領域の長軸方向の側壁まで拡張してショートチャンネル効果を改善し、コンタクト抵抗を減少させることができるという効果がある。

【発明を実施するための最良の形態】

【0014】

以下、本発明に係る半導体素子のトランジスタおよびその形成方法の一実施形態を図面を参考にして詳しく説明する。

図１７は、本発明の実施の形態に係る半導体素子のレイアウト図である。

図１７に示されているように、前記の半導体素子はソース／ドレイン接合領域からなるコンタクト領域１１００を含む活性領域８００を定義する素子分離領域９００を含み、活性領域８００の長軸端部はゲート領域１０００と接触しないよう備えられている。このとき、活性領域８００が隣接するゲート電極と接触しないよう離隔させたのは、ゲート領域１０００に形成されるゲート電極とシリコンフィン形態の突出された活性領域８００の接触による短絡が発生することを防止するためである。

【0015】

さらに、ランディングプラグが活性領域８００の突出された側壁と接触することになり、接触面積の増加によりコンタクト特性を向上させることができる。

図１８は、本発明の実施の形態に基づき形成された半導体素子のトランジスタを示す斜視図であり、図１７の斜線部ａを示したものである。

図１８には半導体基板８１に形成された活性領域のシリコンフィン８２、チャンネル領域９７、ソース／ドレイン領域１２３、パッド絶縁膜８３、８５およびゲート電極１１０だけが示されている。

図１８の半導体素子は、半導体基板８１と半導体基板上に備えられた活性領域のシリコンフィン８２を含む。Ｉ型のシリコンフィン８２は半導体基板８１の上部に突出されており、長軸の長手方向に隣接するゲート電極１１０と一定の間隔で離隔されている。シリコンフィン８２の側壁には傾斜イオン注入工程で形成されたチャンネル領域９７が位置する。チャンネル領域９７の表面、すなわちシリコンフィン８２の側壁にゲート酸化膜（図示省略）が備えられている。シリコンフィン８２の上部面とゲート電極１１０との界面には、パッド絶縁膜のパッド酸化膜８３とパッド窒化膜８５が積層されてシリコンフィン８２の上部面がチャンネル領域に機能することを防止する。

【0016】

平坦化した上部面を有するゲート電極１１０は、シリコンフィン８２と垂直の方向に延びられてシリコンフィン８２の上側および側壁と接触することになる。このとき、チャンネル領域９７の幅はシリコンフィン８２の高さの２倍となる。

図１９～図２６は、本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す図である。図１９～図２５は、図１７のＡ－Ａ切断面に沿った断面図である。図２６は、図２５のＢ－Ｂ切断面に沿った断面図である。

図１９に示されているように、半導体基板８１にウェル（図示省略）を形成する。次には、半導体基板８１上にパッド酸化膜８３およびパッド窒化膜８５の積層構造でなるパッド絶縁膜を形成する。

【0017】

次に、後続工程で形成されるゲート電極と隣接しないよう活性領域を定義する露光マスク（図示省略）を用いた露光および現像工程を行い、Ｉ型活性領域を定義するフォトレジストパターン（図示省略）を形成した後、前記のフォトレジストパターンを食刻マスクとしてパッド窒化膜８５、パッド酸化膜８３および所定厚さの半導体基板８１を食刻して素子分離用トレンチ８７を形成する。前記の露光マスクは、たとえば最小の大きさのラインパターンの幅がＦの場合、活性領域の長軸の長さを５Ｆより短く定義する露光マスクである。パッド酸化膜８３は５０～２００Åの厚さに形成し、パッド窒化膜８５は１００～４００Åの厚さに形成するのが好ましい。

ここで、後続工程で形成されるゲート電極とその長軸の端部が所定距離離隔するようＩ型活性領域を形成する方法として、別途の前記の素子分離マスクを用いる方法以外に図２７～図２８の工程、または図２９の工程のような方法で形成することもできる。

【0018】

図２７および図２８は、従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の１つの実施の形態を示す断面図および平面図である。

図２７および図２８に示されているように、半導体基板８１の上部にパッド酸化膜８３およびパッド窒化膜８５と活性領域決定用ＣＶＤ酸化膜（図示省略）を積層する。

通常の素子分離マスクを用いた写真食刻工程で、前記の活性領域決定用ＣＶＤ酸化膜をパターニングしてＣＶＤ酸化膜パターン１３１を形成した後、ＣＶＤ酸化膜１３１の表面を湿式食刻する。

このとき、最初にＷ１の幅とＬ１の長さに形成された前記の活性領域決定用ＣＶＤ酸化膜１３１の構造がＷ２の幅とＬ２の長さ構造に形成される。したがって、前記の湿式食刻工程時に湿式食刻された領域１３３ほど活性領域の長軸端部と隣接するゲート電極（図示省略）が離隔される。

【0019】

後続工程として、湿式食刻された活性領域決定用ＣＶＤ酸化膜１３１を食刻マスクとして半導体基板８１を食刻して図１９のトレンチ８７を形成する。

図２９は、図１９乃至従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の他の実施の形態を示す断面図および平面図である。

図２９に示されているように、半導体基板８１上にパッド酸化膜８３およびパッド窒化膜（図示省略）を蒸着し、通常の素子分離マスクを用いた写真食刻工程でパッド窒化膜パターン８５を形成する。

次には、パッド窒化膜８５パターンの表面を湿式方法で食刻し、これを食刻マスクとして半導体基板８１を食刻して図１９のトレンチ８７を形成する。

このとき、湿式食刻工程時に湿式食刻された領域８６ほど活性領域の長軸端部と隣接するゲート電極（図示省略）が離隔される。

再び図１９を参照すれば、トレンチ８７の表面にトレンチ熱酸化膜８９を形成し、トレンチ８７を含む全体表面の上部にライナー窒化膜９１を形成する。活性領域の４つの側面は、トレンチ熱酸化膜８９およびライナー窒化膜９１により取り囲まれることになる。

図２０に示されているように、トレンチ８７を埋め込む素子分離用酸化膜（図示省略）を全体表面の上部に形成し、パッド窒化膜８５が露出するまで平坦化食刻して素子分離膜９３を形成する。前記の平坦化食刻工程は、化学機械研磨（chemical mechanical polishing）方法であるのが好ましい。

【0020】

図２１に示されているように、素子分離膜９３を所定の厚さに食刻して活性領域を素子分離膜９３の上部に突出させる。以下で、前記活性領域の突出された部分をシリコンフィン８２という。前記の食刻工程によりシリコンフィン８２の４つの側壁に形成されたライナー窒化膜９１が露出する。

次には、シリコンフィン８２の４つの側壁に不純物９５を傾斜イオン注入してチャンネル領域（図１８の「９７」）を形成する。ここで、前記の傾斜イオン注入工程は１０Ｅ１

６～１０Ｅ１９／ｃｍ^{3}の濃度で行うのが好ましい。

図２２に示されているように、シリコンフィン８２の４つの側壁上のライナー窒化膜９１およびトレンチ熱酸化膜８９を除去する。

次には、ライナー窒化膜９１およびトレンチ熱酸化膜８９が除去されて露出したシリコンフィン８２の４つの側壁にゲート酸化膜９９を形成する。

【0021】

次に、全体表面の上部にトレンチ８７を埋め込む平坦化したゲート電極用ポリシリコン層１０１を形成する。シリコンフィン８２は、ゲート電極用ポリシリコン層１０１により側壁および上部が取り囲まれた形態となる。次には、ゲート電極用ポリシリコン層１０１の上部に障壁金属層１０３、金属層１０５、ハードマスク窒化膜１０７およびハードマスク酸化膜１０９を順次形成する。

図２３に示されているように、ゲート電極マスク（図示省略）を用いた写真食刻工程でハードマスク酸化膜１０９、ハードマスク窒化膜１０７、金属層１０５、障壁金属層１０３、ゲート電極用ポリシリコン層１０１およびパッド窒化膜パターン８５を順次食刻してシリコンフィン８２の長軸方向と垂直のゲート電極（図１８の「１１０」）を形成する。このとき、活性領域の上部のゲート電極１１０はパッド窒化膜パターン８５、ゲート電極用ポリシリコン層１０１、障壁金属層１０３、金属層１０５およびハードマスク窒化膜１０７およびハードマスク酸化膜１０９の積層構造でなり、素子分離膜９３上のゲート電極１１０はゲート電極用ポリシリコン層１０１、障壁金属層１０３、金属層１０５およびハードマスク窒化膜１０７およびハードマスク酸化膜１０９の積層構造でなる。

【0022】

次には、ゲート電極用ポリシリコン層１０１の表面に酸化膜１１１を形成した後、ゲート電極１１０を含む全体表面の上部に窒化膜１１３を一定の厚さに形成する。

次に、全体表面の上部にＢＰＳＧのように流動性に優れた物質で絶縁膜（図示省略）を形成した後、窒化膜１１３が露出するまで平坦化食刻して下部絶縁膜１１５を形成する。

図２４に示されているように、ランディングプラグコンタクトマスク（図示省略）を用いた写真食刻工程で下部絶縁層１１５および窒化膜１１３を異方性食刻することにより、パッド酸化膜８３を露出させる自己整合的なランディングプラグコンタクトホール１１７を形成する。前記の異方性食刻工程は、ハードマスク酸化膜１０９およびゲート酸化膜９９表面の窒化膜１１３が全て除去されるよう過度食刻工程で行う。前記の異方性食刻工程によりゲート電極の側壁にはスペーサが形成される。

次に、ランディングプラグコンタクトホール１１７の底部にＬＤＤ不純物およびハロー不純物をイオン注入する。このとき、ハロー不純物のイオン注入工程は行わないこともある。

【0023】

図２５に示されているように、窒化膜１１３スペーサの間に露出する半導体基板８１表面の上部のパッド酸化膜８３とパッド酸化膜８３の側壁のゲート酸化膜９９を湿式食刻工程で除去する。

次には、ランディングプラグコンタクトホール１１７を埋め込むランディングプラグ用ポリシリコン層（図示省略）を全体表面の上部に形成し、ハードマスク窒化膜１０７が露出するよう平坦化食刻してランディングプラグ１２１を形成する。前記の平坦化食刻工程は、ＣＭＰ工程またはエッチバック工程で行うのが好ましい。

ランディングプラグ１２１に含まれた不純物がシリコンフィン８２に拡散されてソース／ドレイン領域１２３が形成される。

図２５の半導体素子のトランジスタは、トレンチ型素子分離膜９３により定義され、トレンチ型素子分離膜９３の上部に突出されるシリコンフィン８２を含むＩ型活性領域を含む。シリコンフィン８２の側壁にはゲート酸化膜９９が形成されており、シリコンフィン８２の上部面とゲート電極の下部面の界面にはパッド酸化膜８３およびパッド窒化膜８５の積層構造でなるパッド絶縁膜が備えられている。さらに、ゲート電極はＩ型活性領域と垂直の方向に延びられてその上部が平坦化されている。前記ゲート電極の間のシリコンフ

ィン８２および前記シリコンフィンの端部の側壁にはソース／ドレイン領域１２３が備えられており、チャンネル領域は前記ゲート電極の下部のシリコンフィン８２の側壁に備えられている。

【0024】

図２６は、図２５のＢ－Ｂ切断面に沿った断面図である。

図２６に示されているように、本発明に係る半導体素子のトランジスタのチャンネル幅は、素子分離膜９３の上部に突出されたシリコンフィン８２の高さ（ｈ）の２倍（２ｈ）となり、活性領域の短縮長さがチャンネル幅になる従来のトランジスタよりチャンネル幅が大きくなり、電流駆動力が増加してショートチャンネル効果を防止することができる。

【図面の簡単な説明】

【0025】

【図1】従来の技術に係る半導体素子のレイアウト図である。

【図2】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図3】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図4】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図5】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図6】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図7】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図8】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図9】図１の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図10】他の従来の技術に係る半導体素子のレイアウト図である。

【図11】図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図12】図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図13】図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図14】図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図15】図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図16】図１０の従来の技術に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図17】本発明に係る半導体素子のレイアウト図である。

【図18】本発明の実施の形態に基づき形成された半導体素子のトランジスタを示す斜視図である。

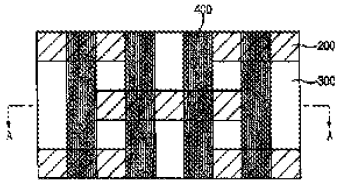
【図19】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図20】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。

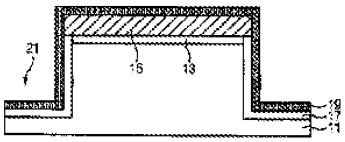
【図21】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。

【図22】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。
【図23】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。
【図24】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。
【図25】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。
【図26】本発明の実施の形態に係る半導体素子のトランジスタ形成方法を示す断面図である。
【図27】従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の１つの実施の形態を示す断面図である。
【図28】従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の１つの実施の形態を示す平面図である。
【図29】図１９乃至従来の技術の活性領域の長軸の長さより小さい長軸を有する、本発明に係る活性領域を形成する方法の他の実施の形態を示す断面図である。
【符号の説明】
【0026】
８１　半導体基板
８２　シリコンフィン
８３、８５　パッド絶縁膜
８６、１３３　湿式食刻された領域
８７　素子分離用トレンチ
８９　トレンチ熱酸化膜
９１　ライナー窒化膜
９３　素子分離膜
９５　不純物
９７　チャンネル領域
９９　ゲート酸化膜
１０１　ゲート電極用ポリシリコン層
１０３　障壁金属層
１０５　金属層
１０７　ハードマスク窒化膜
１０９　ハードマスク酸化膜
１１０　ゲート電極
１１１　酸化膜
１１３　窒化膜
１１５　下部絶縁層
１１７　ランディングプラグコンタクトホール
１２１　ランディングプラグ
１２３　ソース／ドレイン領域
１３１　ＣＶＤ酸化膜パターン
８００　活性領域
９００　素子分離領域
１０００　ゲート領域
１１００　コンタクト領域

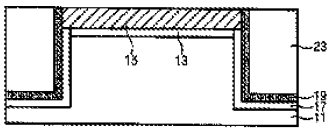
【図1】



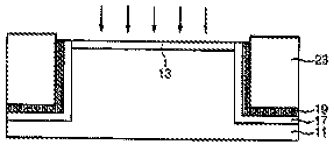
【図2】



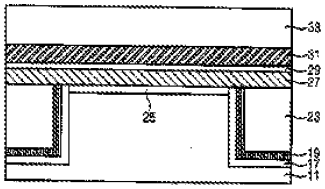
【図3】



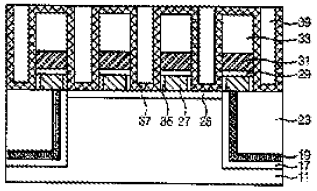
【図4】



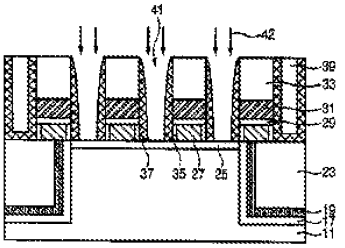
【図5】



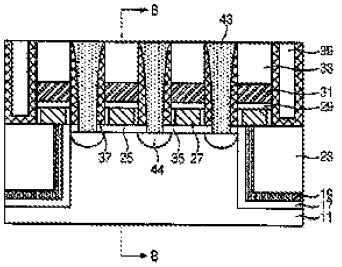
【図6】



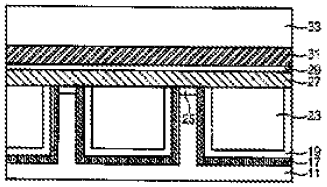
【図7】



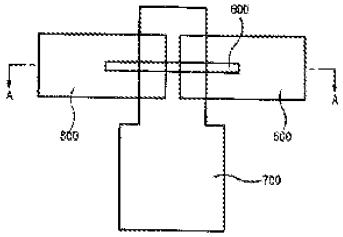
【図8】



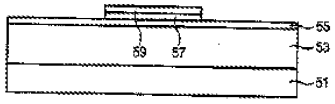
【図9】



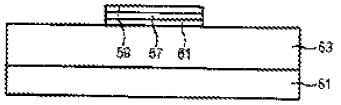
【図10】



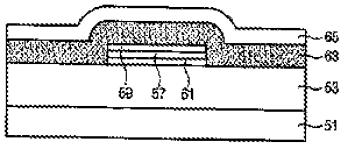
【図11】



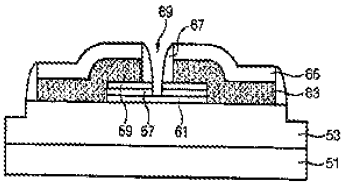
【図12】



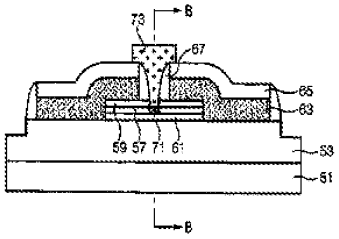
【図13】



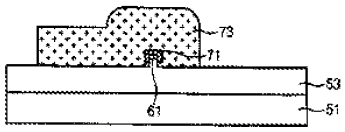
【図14】



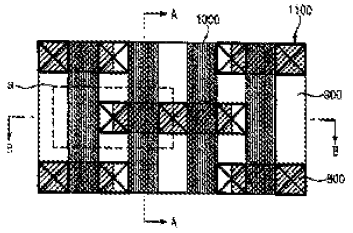
【図15】



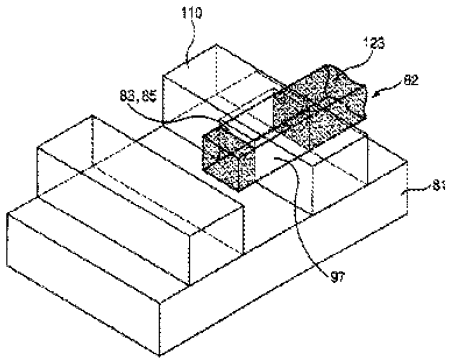
【図16】



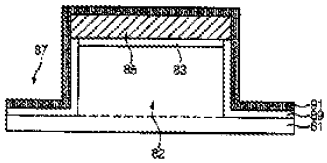
【図17】



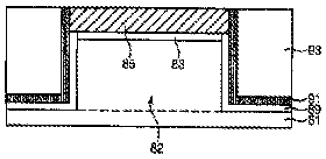
【図18】



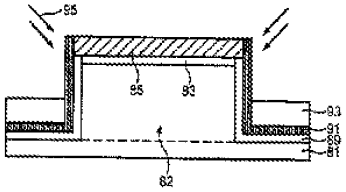
【図19】



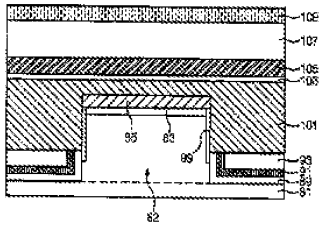
【図20】



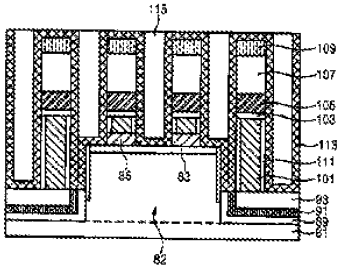
【図21】



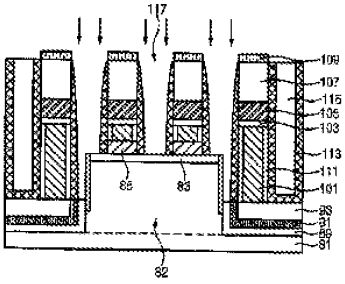
【図22】



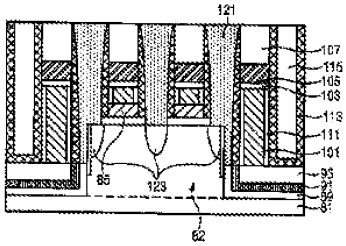
【図23】



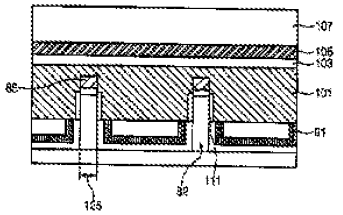
【図24】



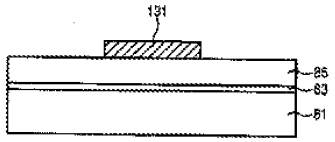
【図25】



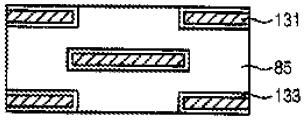
【図26】



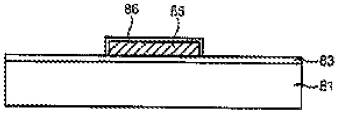
【図27】



【図28】



【図29】



(51)Int.Cl.⁷	FI		テーマコード（参考）
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5F140 AA10 AA21 AC32 BA01 BB05 BC07 BE03 BF04 BF20 BF21 BF27 BF44 BF51 BG09 BG12 BG14 BG49 BG53 BH05 BH15 BJ01 BJ04 BJ27 BK02 BK13 BK16 BK22 BK27 CB04 CB08 CE07

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SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

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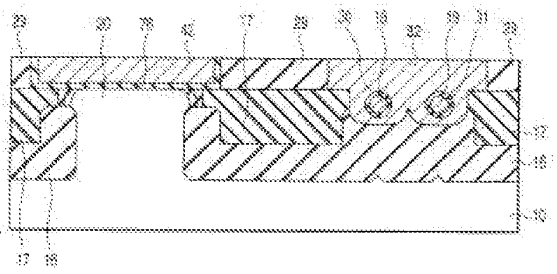
Classification: - international: ***H01L21/28; H01L21/76; H01L21/762; H01L21/768; H01L21/8234; H01L27/08; H01L27/088; H01L27/12; H01L29/78; H01L29/786***
- cooperative: **H01L29/0673**; **H01L29/42392**; **H01L29/66795**; **H01L29/785**; **H01L29/7854**; H01L29/78639

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Abstract of JP2008172082 (A)



PROBLEM TO BE SOLVED: To provide the method of manufacturing a semiconductor device comprising a fin-type field-effect transistor which can be mounted together with a planer region easily and at a low cost. ;SOLUTION: The method of manufacturing a semiconductor device comprises the steps of forming a line-shaped insulating film on the principal surface of a substrate 10, etching the substrate using the insulating film as a mask and forming a first groove in both sides of the insulating film, forming a sidewall insulating film on the sidewall of the first groove, etching the substrate using the insulating film and the sidewall insulating film as masks and forming a second groove in the bottom of the first groove, oxidizing the substrate using the insulating film and the sidewall insulating film as oxidation-resistant masks and allowing oxide regions 16 formed on the sidewalls adjacent to each other while the

substrate therebetween of the second groove is in contact with each other, removing the insulating film and the sidewall insulating film, forming a gate insulating film 21 on the surface of a semiconductor region 18 of the substrate exposed by removal, forming a gate electrode 24 on the gate insulating film, and forming a fin-type field-effect transistor which uses the semiconductor region as a line-shaped fin. ;COPYRIGHT: (C) 2008,JPO&INPIT

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DESCRIPTION JP2008172082

PROBLEM TO BE SOLVED: To provide a manufacturing method of a semiconductor device including a fin type field effect transistor which can be mixed with a planar region conveniently and at low cost. A method of manufacturing a semiconductor device includes forming a line-shaped insulating film on a main surface of a substrate, etching the substrate with the insulating film as a mask to form first grooves on both sides of the insulating film, Side wall insulating film is formed on the side wall of each of the trenches and the substrate is etched by using the insulating film and the side wall insulating film as a mask to form a second trench in each of the bottom portions of the first trenches and the insulating film and the side wall insulating film Is used as an oxidation resistant mask to oxidize the substrate to bring the oxidized regions 16 formed on the adjacent side walls of the substrate of the second trench into contact with each other, remove the insulating film and the side wall insulating film, A step of forming a gate insulating film 21 on the surface of the semiconductor region 18 of the substrate and a gate electrode 24 thereon to form a fin type field effect transistor in which the semiconductor region is a line shaped fin. (FIG.

【課題】簡便かつ低コストにプレーナ領域と混載することが可能なフィン型電界効果トランジスタを含んだ半導体装置の製造方法を提供すること。【解決手段】半導体装置の製造方法は、基板10の主表面にライン状の絶縁膜を形成し、絶縁膜をマスクに基板をエッチングして絶縁膜の両側に第１の溝を形成し、第１の溝それぞれの側壁に側壁絶縁膜を形成し、絶縁膜及び側壁絶縁膜をマスクに基板をエッチングして第１の溝の底部それぞれに第２の溝を形成し、絶縁膜及び側壁絶縁膜を耐酸化性マスクとして基板を酸化して第２の溝の基板を挟んで隣接する側壁それぞれに形成される酸化領域16を互いに接触させ、絶縁膜及び側壁絶縁膜を除去し、除去によって露出した基板の半導体領域18の表面にゲート絶縁膜21を、その上にゲート電極24を形成し、半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程を含む。【選択図】図１４

Semiconductor device and method of manufacturing semiconductor device

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半導体装置及び半導体装置の製造方法

[0001]
TECHNICAL FIELD The present invention relates to a semiconductor device including a fin-type FET (Field Effect Transistor) and a manufacturing method thereof.

本発明は、フィン型ＦＥＴ（電界効果トランジスタ）を含んだ半導体装置およびその製造方法に関する。

[0002]
A FinFET fabricated on a fin type FET (FinFET), particularly a bulk Si substrate, is a device with a good cutoff characteristic at low cost, and therefore is considered promising as a next generation transistor structure (For example, see Patent Document 1).

フィン（Ｆｉｎ）型ＦＥＴ（ＦｉｎＦＥＴ）、特にバルク（Bulk）Ｓｉ基板上に作製されたＦｉｎＦＥＴは、低コストでカットオフ特性が良好なデバイスであるため、次世代トランジスタ構造として有望視されている（例えば、特許文献１参照）。

[0003]
However, planar devices are simpler and lower cost to realize multi-threshold voltage and analog devices, so in actual LSI, it is necessary to combine conventional planar type MOSFET and fin type FET is necessary.

しかしながら、マルチ閾値電圧の実現やアナログデバイスに対応するには、プレーナ（planar）デバイスの方が簡単で低コストであるため、実際のＬＳＩでは、従来のプレーナ型ＭＯＳＦＥＴとフィン型ＦＥＴを混載することが必要である。

Therefore, a simple manufacturing process of mixing both is required.

そのため、両者を混載する簡単な製造プロセスが求められていた。

[0004]
However, when a planar type MOSFET and a fin type FET are mixedly mounted, the surface of the gate becomes irregular, it becomes difficult to perform lithography for manufacturing a fine

gate, and processing of the gate of the fin region and the planar region is performed It can not be done at the same time.

ところが、プレーナ型ＭＯＳＦＥＴとフィン型ＦＥＴを混載すると、ゲートの表面が凸凹となって、微細なゲートを作製するためのリソグラフィを行なうことが困難になったり、フィン領域、プレーナ領域のゲートの加工を同時に行なえない等の問題があった。

In addition, there is also a problem that the number of steps increases and the manufacturing cost increases. Japanese Unexamined Patent Application Publication No. 2005-229107

また、工程数が多くなり製造コストが増加するという問題もあった。特開２００５－２２９１０７号公報

[0005]

The present invention provides a semiconductor device including a fin type field effect transistor which can be mixed with a planar region conveniently and at low cost, and a manufacturing method thereof.

本発明は、簡便かつ低コストにプレーナ領域と混載することが可能なフィン型電界効果トランジスタを含んだ半導体装置及びその製造方法を提供する。

[0006]

A method for manufacturing a semiconductor device according to a first aspect of the present invention comprises the steps of: forming a line-shaped insulating film on a main surface of a semiconductor substrate; etching the semiconductor substrate with the line- A step of forming two adjacent first grooves on both sides of the linear insulating film, a step of forming side wall insulating films on side walls of each of the adjacent first grooves, a step of forming a line- Forming a second trench in each of bottoms of adjacent first trenches by etching the semiconductor substrate using the sidewall insulating film as a mask, oxidizing the linear insulating film and the sidewall insulating film to oxidation Contacting oxidized regions formed on respective side walls adjacent to each other with the semiconductor substrate in the second trench interposed therebetween by oxidizing the semiconductor substrate as a sex mask; Forming a gate insulating film on the surface of the semiconductor region of the semiconductor substrate exposed by the removal; forming a gate electrode on the gate insulating film And forming a fin field effect transistor having the semiconductor region as a line shaped fin.

この発明の第１の態様に係る半導体装置の製造方法は、半導体基板の主表面にライン状の絶縁膜を形成する工程と、前記ライン状の絶縁膜をマスクとして前記半導体基板をエッチングすること

により前記ライン状の絶縁膜の両側に２つの隣接する第１の溝を形成する工程と、隣接する前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより隣接する前記第１の溝の底部それぞれに第２の溝を形成する工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させる工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜を除去する工程と、前記除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成する工程と、前記ゲート絶縁膜の上にゲート電極を形成する工程と、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程とを含む。

[0007]
According to a second aspect of the present invention, there is provided a method of manufacturing a semiconductor device, comprising: forming a line-shaped first insulating film on a main surface of a semiconductor substrate and a second insulating film thicker than the first insulating film at the same time ; Forming a plurality of first grooves on both sides of the first and second insulating films by etching the semiconductor substrate using the first and second insulating films as a mask; Forming a sidewall insulating film on sidewalls of each of the first trenches; etching the semiconductor substrate using the first and second insulating films and the sidewall insulating film as a mask to form a plurality of the first trenches Forming a second trench in each of the bottom portions of the first insulating film and the second insulating film; and oxidizing the semiconductor substrate using the first and second insulating films and the sidewall insulating film as an oxidation- The above-mentioned second groove of the both sides is guided Oxidizing regions formed on the side walls adjacent to each other with the body substrate interposed therebetween are brought into contact with each other and the oxidation regions formed on the adjacent side walls of the second trench on both sides of the second insulating film with the semiconductor substrate therebetween A step of removing the first and second insulating films and the side wall insulating film from the surface of the semiconductor region of the semiconductor substrate exposed by removing the first insulating film; Forming a fin-shaped field effect transistor in which the semiconductor region is formed as a line-shaped fin by forming a gate insulating film on the gate insulating film and forming a gate electrode on the gate insulating film; And forming a planar field effect transistor or a planar region in another semiconductor region of the exposed semiconductor substrate.

この発明の第２の態様に係る半導体装置の製造方法は、半導体基板の主表面にライン状の第１の絶縁膜と前記第１の絶縁膜より線幅の太い第２の絶縁膜を同時に形成する工程と、前記第１及び第２の絶縁膜をマスクとして前記半導体基板をエッチングすることにより前記第１及び第２の絶縁膜の両側に複数の第１の溝を形成する工程と、複数の前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより複数の前記第１の溝の底部それぞれに第２の溝を形成する工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸

化することにより、前記第１の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させ、前記第２の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域は互いに接触させない工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜を除去する工程と、前記第１の絶縁膜の除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成し、前記ゲート絶縁膜の上にゲート電極を形成することにより、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程と、前記第２の絶縁膜の除去によって露出した前記半導体基板の別の半導体領域にプレーナ型電界効果トランジスタ或いはプレーナ領域を形成する工程とを含む。

[0008]
According to a third aspect of the present invention, there is provided a semiconductor device comprising: a silicon oxide film formed on a bulk silicon substrate; line-shaped fins formed on the silicon oxide film; And a planar region which is a part of the substrate which is connected to each other and has a width in a direction perpendicular to the extending direction larger than the fin and a height of the upper surface coinciding with a height of the upper surface of the fin.

この発明の第３の態様に係る半導体装置は、バルクシリコン基板の上に形成されたシリコン酸化膜と、前記シリコン酸化膜上に形成されたライン状のフィンと、前記フィンの延伸方向の両端にそれぞれ接続され、前記延伸方向と垂直な方向の幅が前記フィンよりも大きく、上面の高さが前記フィンの上面の高さと一致している前記基板の一部であるプレーナ領域とを具備する。

[0009]
According to the present invention, it is possible to provide a semiconductor device including a fin field effect transistor which can be mixed with a planar region conveniently and at low cost, and a manufacturing method thereof.

本発明によれば、簡便かつ低コストにプレーナ領域と混載することが可能なフィン型電界効果トランジスタを含んだ半導体装置及びその製造方法を提供することができる。

[0010]
Hereinafter, embodiments of the present invention will be described in detail with reference to the drawings.

以下、図面を参照して本発明の実施形態について詳細に説明する。

[0011]

FIG. 1 is a diagram showing a three-dimensional structure of a nano wire-fin FET according to the following embodiment.

図１は以下の実施形態に係るナノワイヤー（nano wire）-フィン型ＦＥＴの３次元構造を示した図である。

A MOS (Metal Oxide Semiconductor) FET in which the aspect ratio (fin height / fin width) is reduced to about 1 by reducing the height of a fin having a width of 10 nm or less is generally called a nanowire-fin type FET , Not only the side faces but also the upper faces are also used as channel faces.

幅１０nm以下のフィンの高さを低くしてアスペクト比（フィンの高さ／フィンの幅）を１程度に小さくしたＭＯＳ（Metal Oxide Semiconductor)ＦＥＴが、一般に、ナノワイヤー-フィン型ＦＥＴと呼ばれ、通常、フィン側面だけでなく上面もチャネル面として使用する。

In particular, if not only the side fins but also the top and bottom faces are used as channels, they are called gate all-around nanowire-fin type FETs.

特に、チャネルとしてフィンの側面だけでなく、上面と底面も使うようにすると、ゲートオールアラウンド（Gate-all-around）ナノワイヤー-フィン型ＦＥＴと呼ばれる。

[0012]

Advantages of the nanowire-fin type FET include (1) resistance to shorter channel effect than ordinary fin type FET, miniaturization is possible by that, (2) effective mass and scatter probability due to quantum confinement The mobility is improved as a result of the reduction of the impurity concentration, and (3) the variation in the threshold voltage due to impurity fluctuation is reduced.

ナノワイヤー-フィン型ＦＥＴのメリットとしては、（１）通常のフィン型ＦＥＴよりも短チャネル効果耐性があり、その分、微細化が可能であること、（２）量子閉じ込めによる有効質量と散乱確率の低減の結果、移動度が向上すること、（３）不純物ゆらぎ起因の閾値電圧バラツキが低減すること、等が挙げられる。

[0013]

First Embodiment A method of manufacturing a semiconductor device according to a first embodiment of the present invention will be described below with reference to FIGS. 2 to 14 which are sectional views of manufacturing steps.

(第１の実施形態) 本発明の第１の実施形態に係る半導体装置の製造方法を、各製造工程の断面図である図２乃至図１４を用いて以下に説明する。

[0014]
In the present embodiment, the nanowire-fin type FET as shown in FIG. 1 is mounted on the same substrate as the planar type MOSFET.

本実施形態においては、図１に示したようなナノワイヤー-フィン型ＦＥＴをプレーナ型ＭＯＳＦＥＴと同じ基板上に混載する。

[0015]
First, as shown in FIG. 2, a hard mask material 15 made of SiN having a thickness of about 50 nm is deposited on a bulk Si substrate 10 with a thin oxide film (not shown) having a thickness of about 2 nm interposed therebetween.

まず図２に示すように、バルクＳｉ基板１０の上に厚さ２nm程度の薄い酸化膜（図示せず）を介して、膜厚５０nm程度のＳｉＮからなるハードマスク材１５を堆積する。

As the hard mask material 15, a laminated film of SiO 2, SiON, or even SiN / SiO 2 / SiN, or another insulating film may be used.

ハードマスク材１５としては、ＳｉＯ２、あるいはＳｉＯＮ、更にはＳｉＮ／ＳｉＯ２／ＳｉＮ等の積層膜、その他の絶縁膜であってもかまわない。

[0016]
Next, as shown in FIG. 3, the active (channel) regions of the planar type MOSFET and the nanowire-fin type FET are patterned to form the hard mask 11 and the hard masks 12 and 13 for each.

次に、図３に示すように、プレーナ型ＭＯＳＦＥＴ及びナノワイヤー-フィン型ＦＥＴの活性（チャネル）領域をパターンニングして、それぞれに対するハードマスク１１及びハードマスク１２、１３を形成する。

Here, the line widths of the line-shaped hard masks 12 and 13 for forming the nano wire-fin type FET having fins having a width of about 10 nm or less are determined by the line width of the

hard mask 11 for forming the planar type MOSFET .

ここで、１０nm程度以下の幅のフィンを有するナノワイヤー-フィン型ＦＥＴを形成するためのライン状のハードマスク１２、１３の線幅は、プレーナ型ＭＯＳＦＥＴを形成するためのハードマスク１１の線幅よりも小さくしておく。

[0017]

Thereafter, as shown in FIG. 4, a first trench 50 having a depth of about 20 nm is formed in the bulk Si substrate 10 by performing RIE (reactive ion etching) processing using the hard masks 11, 12, and 13 as a mask .

その後、ハードマスク１１、１２、１３をマスクとしてＲＩＥ（反応性イオンエッチング）加工を行なうことにより図４に示すように、２０nm程度の深さの第１の溝５０がバルクＳｉ基板１０に形成される。

[0018]

Next, as shown in FIG. 5, an SiN film 14 is formed on the entire surface, and then etched back as shown in FIG. 6 to form side walls of SiN having a thickness of about 20 nm on the side faces of the first trenches 50 Thereby forming the insulating film 14.

次に、図５に示すように、この上からＳｉＮ膜１４を全面に形成した後、図６に示すようにエッチバックすることにより第１の溝５０の側面に厚さ２０nm程度のＳｉＮの側壁絶縁膜１４を形成する。

As the side wall insulating film 14, SiO 2, SiON, or another insulating film may be used.

側壁絶縁膜１４としては、ＳｉＯ２、ＳｉＯＮ、或いはその他の絶縁膜を用いてもかまわない。

[0019]

Subsequently, as shown in FIG. 7, the Si substrate 10 is etched using the hard masks 11, 12, 13 and the sidewall insulating film 14 as a mask to further deeply bore the bottom of the first trench 50 to form a second trench 60 .

次いで、図７に示すようにハードマスク１１、１２、１３と側壁絶縁膜１４をマスクとしてＳｉ基板１０をエッチングして第１の溝５０の底部をさらに深く掘って第２の溝６０を形成する。

[0020]
Next, as shown in FIG. 8, the surface of the Si substrate 10 exposed at the bottom of the second trench 60 is oxidized using the hard masks 11, 12, 13 and the sidewall insulating film 14 as an oxidation resistant mask to form the oxide film 16 Form.

次に、図８に示すようにハードマスク１１、１２、１３と側壁絶縁膜１４を耐酸化性マスクとして第２の溝６０の底部に露出したＳｉ基板１０の表面を酸化して酸化膜１６を形成する。

At this time, the thickness of the oxide film is adjusted so that the oxide films 16 from the side walls of the second trenches 60 on both sides of the hard masks 12, 13 are brought into contact with each other under the region to be the fins below the hard masks 12, 13.

その際、ハードマスク１２、１３の下のフィンとなるべき領域の下においてその両側の第２の溝６０側壁からの酸化膜１６が互いに接触するように酸化膜厚を調整する。

[0021]
As a result, a structure in which the fin regions 18 and 19, which are semiconductor regions, remain partially on the oxide film 16, that is, the SOI (Silicon On Insulator) structure is formed only partially in the fin type FET region.

その結果フィン型ＦＥＴ領域のみ部分的に、酸化膜１６の上に半導体領域であるフィン領域１８、１９が残存する構造、即ちＳＯＩ(Silicon On Insulator)構造が形成される。

On the other hand, in the planar type MOSFET region formed so that the channel width under the hard mask 11 is widened, the oxide film from both side walls of the second trench 60 does not come into contact, so that the SOI structure is not obtained.

他方、ハードマスク１１の下のチャネル幅が広くなるように形成したプレーナ型ＭＯＳＦＥＴ領域では、第２の溝６０の両側壁からの酸化膜が接触しないのでＳＯＩ構造とはならない。

[0022]
Next, as shown in FIG. 9, an element isolation insulating film (STI: shallow trench isolation) 17 made of an SiO 2 -based insulating film is deposited on the entire surface by HDP (High Density Plasma: High Density Plasma) Chemical Mechanical Polishing: Planarization is carried out to expose the SiN hard masks 11, 12, 13.

次に図９に示すように、ＨＤＰ(High Density Plasma：高密度プラズマ)などを用いてＳｉＯ２系絶縁膜からなる素子分離絶縁膜(ＳＴＩ:shallow trench isolation)１７を全面に堆積し、更にＣＭＰ(Chemical Mechanical Polishing：化学的機械的研磨)平坦化を実行して、ＳｉＮハードマスク１１、１２、１３を露出させる。

[0023]
Then, as shown in FIG. 10, the element isolation insulating film 17 is etched so that the surface height of the element isolation insulating film (STI) 17 is made equal to the surface height of the fin regions 18 and 19.

そしてさらに、図１０に示すように素子分離絶縁膜１７をエッチングすることにより、素子分離絶縁膜（ＳＴＩ）１７の表面高さをフィン領域１８、１９の表面高さに揃える。

[0024]
11, by removing the SiN hard masks 11, 12, and 13 and the SiN sidewall insulating film 14 with hot phosphoric acid or the like, in the fin type FET region, the upper surface and both side surfaces of the fins 18 and 19 are exposed .

次いで、図１１に示すように、ＳｉＮハードマスク１１、１２、１３及びＳｉＮ側壁絶縁膜１４をホットリン酸などで除去することにより、フィン型ＦＥＴ領域においてはフィン１８、１９の上面および両側面が露出する。

[0025]
Thereafter, as shown in FIG. 12, by performing annealing at a temperature of 800 ° C. in an atmosphere containing hydrogen (H 2), the cross-sectional shapes of the nanowire-fins 18 and 19 are rounded and at the same time, planar type MOSFET Sectional shape of the edge portion adjacent to the element isolation insulating film (STI) 17 in the planar region 20 of FIG.

その後、図１２に示すように、水素（Ｈ２）を含んだ雰囲気中において温度８００°Cでアニールを行なうことにより、ナノワイヤー-フィン１８、１９の断面形状を丸め、同時に、プレーナ型ＭＯＳＦＥＴのプレーナ領域２０の素子分離絶縁膜（ＳＴＩ）１７に隣接したエッジ部分の断面形状を丸める。

[0026]
By rounding the cross-sectional shape of the nanowire-fins 18, 19, the surface of the channel region becomes smooth, scattering of carriers is reduced, and the mobility is improved.

ナノワイヤー-フィン１８、１９の断面形状を丸めることにより、チャネル領域の表面がスムーズになりキャリアの散乱が減少して移動度が向上する。

In addition, the annealing may be performed in an atmosphere containing nitrogen or the like.

また、上記アニールは、窒素等を含んだ雰囲気中で実行されてもよい。

[0027]

Next, as shown in FIG. 13, an exposed surface (corresponding to the upper surface and both side surfaces before rolling) of the nanowire-fins 18 and 19 and the surface of the active region 20 of the planar type MOSFET are formed with an oxynitride film (SiON The gate insulating films 21, 22, and 23 are formed.

次いで、図１３に示すように、ナノワイヤー-フィン１８、１９の露出した表面（丸める前の上面及び両側面に相当）、及びプレーナ型ＭＯＳＦＥＴの活性領域２０の表面、それぞれに酸窒化膜（ＳｉＯＮ）からなるゲート絶縁膜２１、２２、２３を形成する。

[0028]

Further, a gate electrode material such as polysilicon or metal is deposited thereon, and gate electrodes 24 and 25 are formed by lithography and RIE as shown in FIG.

更に、その上に、ポリシリコン或いはメタル等のゲート電極材料を堆積し、図１４に示すように、リソグラフィとＲＩＥでゲート電極２４、２５を形成する。

[0029]

In the present embodiment, the height of the gate electrode 24 of the fin type FET region and the height of the gate electrode 25 of the planar type MOSFET region are substantially the same, so that the depth of focus (DOF) of the gate lithography A process margin is obtained.

本実施形態においては、フィン型ＦＥＴ領域のゲート電極２４の高さと、プレーナ型ＭＯＳＦＥＴ領域のゲート電極２５の高さがほぼ同じになるので、ゲートのリソグラフィの焦点深度（ＤＯＦ：Depth Of Focus）にプロセス余裕が得られる。

In addition, RIE processing of fin type FET and planar type MOSFET can be performed at the same time.

また、フィン型ＦＥＴとプレーナ型ＭＯＳＦＥＴのＲＩＥ加工を同時に行うことができる。

Furthermore, since the gate surface is flat, a sidewall pattern transfer process may be used to process the gate pattern.

さらにまた、ゲート表面が平坦なので、ゲートパターンの加工にサイドウォールパターントランスファー(Sidewall pattern transfer)プロセスを用いてもよい。

[0030]
The fin type FET manufactured in this embodiment is similar to Ω gate fin type FET and Tri gate type FET because the upper surface and both side surfaces of the fin are channels.

本実施形態で製造されるフィン型ＦＥＴにおいては、フィンの上面及び両側面がチャネルになるため、Ωゲートフィン型ＦＥＴやトライゲート（Tri gate）フィン型ＦＥＴに類似している。

[0031]
Thereafter, spacers are formed on both side surfaces of the gate electrode 24 in the direction perpendicular to the paper surface of FIG. 14, and a source / drain is formed by ion implantation or silicide bonding (not shown).

その後、図１４のゲート電極２４の紙面垂直方向の両側面にスペーサを形成し、ソース／ドレインをイオン注入やシリサイド貼り付けによって形成する（図示せず）。

The aspect ratio of the nanowire-fin 18, 19 is small.

ナノワイヤー-フィン１８、１９のアスペクト比は小さい。

Therefore, the doping for forming the source / drain diffusion layers in the fins 18 and 19 is different from ordinary high-aspect-ratio fins, and ion implantation is performed such that the angle formed by the direction perpendicular to the substrate is 0 to 7 degrees Good.

従って、フィン１８、１９にソース／ドレイン拡散層を形成するためのドーピングは、通常の高アスペクト比のフィンとは異なり、基板に垂直な方向とのなす角度が０～７度となるイオン注入でよい。

Therefore, it is unnecessary to use expensive techniques such as oblique ion implantation technique and plasma doping technique, which are necessary for uniformly doping the fin of high aspect in the channel width direction (fin height direction). Therefore, Cost reduction can be achieved.

従って、高アスペクトのフィンに対して、チャネル幅方向（フィン高さ方向）に均一にドーピングするために必要となる斜めイオン注入技術やプラズマドーピング技術等の高価な技術が不要となるので、プロセスの低コスト化が図れる。

[0032]
The subsequent manufacturing process is the same as the manufacturing process of ordinary LSI.

その後の製造工程は通常のＬＳＩの製造工程と同様である。

That is, an interlayer insulating film is deposited, a contact hole is formed, and an upper layer wiring (Cu or the like) is formed by a damascene process or the like (not shown).

すなわち、層間絶縁膜を堆積し、コンタクトホールを形成し、上層配線（Ｃｕなど）をダマシンプロセス等を用いて形成する（図示せず）。

[0033]
In the manufacturing method of the semiconductor device according to the present embodiment, (1) lithography and RIE processing of the gate of the fin region and the planar region can be simultaneously processed; (2) in the fabrication of the fin type FET on the bulk Si substrate It is not necessary to etch the element isolation insulating film (STI) around the fin region, which is necessary for getting out fins, (3) since the portion directly under the fin is an oxide insulating film, punch It becomes unnecessary to form a high-concentration impurity layer as a through stopper, and (4) lithography or the like for making fins and planar becomes unnecessary, etc., it becomes possible to reduce the number of steps .

本実施形態に係る半導体装置の製造方法においては、（１）フィン領域、プレーナ領域のゲートのリソグラフィ、ＲＩＥ加工を同時に処理可能であること、（２）バルクＳｉ基板上のフィン型ＦＥＴの製造においてフィンを出すために必要であった、フィン領域まわりの素子分離絶縁膜（ＳＴＩ）のリセスエッチングが不要になること、（３）フィン下部直下が酸化絶縁膜となっているので、フィン下部にパンチスルーストッパとして高濃度不純物層を形成することが不要になること、さらに（４）フィンとプレーナの作りわけのためのリソグラフィ等が不要となること、等から工程数を削減することが可能となる。

[0034]
In addition, despite using an inexpensive bulk Si substrate as the substrate, since it is possible to form a nanowire-fin type FET of the SOI structure, there is an advantage that cost reduction can be achieved since it is not necessary to use an expensive SOI substrate is there.

また、基板として安価なバルクＳｉ基板を用いているにもかかわらず、ＳＯＩ構造のナノワイヤー-フィン型ＦＥＴを形成できるので、高価なＳＯＩ基板を利用しないで済むので低コスト化が図れるというメリットがある。

[0035]
Furthermore, a deep element isolation insulating film (STI) and a nanowire having a small diameter can be formed on the bulk substrate so as to have the same surface height.

さらにまた、深い素子分離絶縁膜（ＳＴＩ）と直径の小さいナノワイヤーをバルク基板上で表面高さを揃えて形成することができる。

When the heights of the two are aligned, there is an advantage that the subsequent manufacturing process is facilitated.

両者の高さが揃っていると、その後の製造プロセスが容易になるという長所がある。

For example, the requirement for the depth of focus (DOF) of lithography can be relaxed, so that the resolution can be increased.

例えば、リソグラフィの焦点深度（ＤＯＦ）に対する要求を緩めることができるので、解像度を高めることができる。

[0036]
Further, since the over-etching amount with respect to the gate insulating film can be reduced by the RIE process of the gate electrode, the reliability of the film can be improved.

また、ゲート電極のＲＩＥ工程で、ゲート絶縁膜に対するオーバーエッチング量を低減できるので、その膜の信頼性を改善することができる。

This is because the difference between the thickness of the gate in the fin region (particularly in the vicinity of both side faces of the fin) and the thickness of the gate in the planer type MOSFET region is smaller than in the case of the conventional fin type FET, so that when the gate of the fin type FET is processed by RIE , The time for overetching the gate insulating film in the planar type MOSFET region can be shortened.

なぜなら、フィン領域（特にフィン両側面近傍）のゲートの厚さとプレーナ型ＭＯＳＦＥＴ領域のゲートの厚さの差が従来のフィン型ＦＥＴの場合よりも小さいので、フィン型ＦＥＴのゲートをＲＩＥ加工する際、プレーナ型ＭＯＳＦＥＴ領域のゲート絶縁膜がオーバーエッチングされる時間を短縮できるからである。

[0037]

As described above, according to the present embodiment, it is possible to mix the nano wire-fin FET and the planar MOSFET device by a simple process at low cost.

以上説明したように、本実施形態によれば、ナノワイヤー-フィン型ＦＥＴ、プレーナ型ＭＯＳＦＥＴデバイスを簡便なプロセスで、かつ低コストに混載させることが可能となる。

[0038]

Second Embodiment A method of manufacturing a semiconductor device according to a second embodiment of the present invention will be described below with reference to FIGS. 15 to 21 which are sectional views of respective manufacturing steps.

（第２の実施形態） 本発明の第２の実施形態に係る半導体装置の製造方法を、各製造工程の断面図である図１５乃至図２１を用いて以下に説明する。

[0039]

Also in the present embodiment, the nanowire-fin type FET is mounted on the same substrate as the planar type MOSFET, but the damascene process is used for forming the gate of the nanowire-fin type FET, and the gate all It is different from the first embodiment in that it is a round type.

本実施形態においても、ナノワイヤー-フィン型ＦＥＴをプレーナ型ＭＯＳＦＥＴと同じ基板上に混載するが、ナノワイヤー-フィン型ＦＥＴのゲート形成にダマシンプロセスを用い、フィンの周り全体をチャネルとするゲートオールアラウンドタイプにするところが第１の実施形態とは異なっている。

[0040]
Also in the present embodiment, the steps up to FIG. 12 are the same as in the first embodiment, so the description is omitted.

本実施形態においても図１２までの工程は、第１の実施形態と同様であるので説明を省略する。

Thereafter, as shown in FIG. 15, on the exposed surface of the exposed surfaces (corresponding to the upper surface and both side surfaces before rolling) of the nanowire-fins 18 and 19 and the surface of the planar region 20, a dummy gate insulating film 26, 27, and 62.

その後、図１５に示すように、ナノワイヤー-フィン１８、１９の露出した表面（丸める前の上面及び両側面に相当）の活性領域表面、及びプレーナ領域２０の表面にＳｉＯ２からなるダミーゲート絶縁膜２６、２７、及び６２を形成する。

[0041]
Further, a dummy gate electrode material such as polysilicon is deposited thereon, and dummy gate electrode patterns 28 and 63 are formed by lithography and RIE as shown in FIG.

更に、その上にポリシリコン等のダミーゲート電極材料を堆積し、図１６に示すように、リソグラフィとＲＩＥでダミーゲート電極パターン２８及び６３を形成する。

The dummy gates 28 and 63 are to be removed in a later process and are necessary for executing the gate formation by the damascene process.

このダミーゲート２８及び６３は後の工程で除去するものであり、ゲート形成をダマシンプロセスで実行するために必要となる。

[0042]
Thereafter, spacers are formed on both side surfaces of the dummy gates 28 and 63 in FIG. 16 in the direction perpendicular to the paper surface, and a source / drain is formed by ion implantation or silicide bonding (not shown).

その後、図１６のダミーゲート２８及び６３の紙面垂直方向の両側面にスペーサを形成し、ソース／ドレインをイオン注入やシリサイド貼り付けによって形成する（図示せず）。

Also in the present embodiment, the doping for forming the source / drain diffusion layers in the

fins 18 and 19 having a small aspect ratio may be ion implantation in which the angle formed with the direction perpendicular to the substrate is 0 to 7 degrees, Cost reduction can be achieved.

本実施形態においても、アスペクト比が小さいフィン１８、１９にソース／ドレイン拡散層を形成するためのドーピングは、基板に垂直な方向とのなす角度が０～７度となるイオン注入でよく、プロセスの低コスト化が図れる。

[0043]

Next, as shown in FIG. 17, on the entire surface including the dummy gates 28 and 63, a SiO 2 film (hereinafter referred to as a TEOS film) 29 is deposited to a thickness of about 300 nm by using TEOS, and flattened by CMP as shown in FIG. 18 And the tops of the dummy gates 28 and 63 are exposed.

次に、図１７に示すようにダミーゲート２８及び６３を含んだ全面に、ＴＥＯＳを用いてＳｉＯ２膜（以下、ＴＥＯＳ膜）２９を厚さ３００nm程度堆積し、図１８に示すようにＣＭＰで平坦化して、ダミーゲート２８及び６３のトップを露出させる。

[0044]

Next, as shown in FIG. 19, the dummy gates 28 and 63 are etched away by CDE (Chemical Dry Etching) or the like.

次いで、図１９に示すようにダミーゲート２８及び６３をＣＤＥ（ケミカル・ドライ・エッチング）などでエッチング除去する。

Furthermore, when etching is performed with a HF (hydrofluoric acid) chemical solution, as shown in FIG. 20, etching progresses also to the bottoms of the Si - nanowires 18 and 19 in the channel region, and a hollow structure is formed.

更に、ＨＦ（フッ酸）薬液でエッチングすると、図２０に示すように、チャネル領域のＳｉ-ナノワイヤー１８、１９の底部にもエッチングが進み、中空構造が形成される。

That is, the nanowires 18, 19 are structured to float in the air like a bridge.

即ち、ナノワイヤー１８、１９が橋のように空中に浮く構造となる。

The state of FIG. 20 is shown in a bird's eye view as shown in FIG.

図２０の状態を鳥瞰図で示すと図２１のようになる。

[0045]

However, since the source / drain regions existing on the front side and the back side in the direction perpendicular to the paper of FIG. 20 support the nanowires 18, 19, there is no concern that the nanowires 18, 19 are lifted off.

ただし、図２０の紙面垂直方向の手前と奥側に存在するソース・ドレイン領域がナノワイヤー１８、１９を支えているので、ナノワイヤー１８、１９がリフトオフする心配はない。

This state is shown in FIG. 22 which is a cross-sectional view along the dotted line in FIG. 21.

この様子を、図２１の点線に沿った断面図である図２２に示す。

[0046]

Then, as shown in FIG. 23, oxynitride film (SiON) gate insulating films 30, 31, and 64 are formed on the entire surface of the nanowires 18, 19 (upper surface, side surface, bottom surface of the fin) and the surface of the planar region 20 And gate electrode materials 32 and 65 which are, for example, metal materials are deposited thereon. Finally, CMP planarization is performed to remove the unnecessary portion of the gate electrode material.

そして、図２３に示すように、ナノワイヤー１８、１９の表面全面（フィンの上面、側面、底面）、及びプレーナ領域２０の表面に酸窒化膜（ＳｉＯＮ）ゲート絶縁膜３０、３１、及び６４を形成し、さらにその上から例えばメタル材料であるゲート電極材料３２及び６５を堆積する。最後に、ＣＭＰ平坦化して不要部分のゲート電極材料を除去する。

[0047]

The gate electrodes 32 and 65 may be pure metal or metal silicide. Further, FUSI (completely silicided) gate electrode may be used. That is, after forming the gate trench, a gate insulating film is formed, polysilicon (Poly-Si) is deposited over the entire surface, CMP is performed, polysilicon is buried in the trench, and Ni or the like is sputtered to form the entire polysilicon May be silicided.

このゲート電極３２及び６５はピュアメタルでも良いしメタルシリサイドでも良い。また、ＦＵＳＩ(fully silicided：完全にシリサイド化した)ゲート電極にしても良い。すなわち、ゲート

溝形成後、ゲート絶縁膜を形成し、全面にポリシリコン（Poly-Si）を堆積してＣＭＰを行ない、溝内にポリシリコンを埋め込んだ後、Ｎｉなどをスパッタしてポリシリコン全体をシリサイド化させても良い。

[0048]
In the case of this embodiment, since the entire periphery of the nanowire-fins 18 and 19 is a channel, a gate all-around-fin type FET can be formed.

本実施形態の場合、ナノワイヤー-フィン１８、１９の周り全体がチャネルになるため、ゲートオールアラウンド-フィン型ＦＥＴを形成することができる。

[0049]
The subsequent manufacturing process is the same as the manufacturing process of ordinary LSI.

その後の製造工程は通常のＬＳＩの製造工程と同様である。

That is, an interlayer insulating film is deposited, a contact hole is formed, and an upper layer wiring (Cu or the like) is formed by a damascene process or the like (not shown).

すなわち、層間絶縁膜を堆積し、コンタクトホールを形成し、上層配線（Ｃｕなど）をダマシンプロセス等を用いて形成する（図示せず）。

[0050]
Also in the method of manufacturing a semiconductor device according to this embodiment, it is possible to reduce the number of steps for the same reason as in the first embodiment. Likewise, since the nanowire-fin type FET having the SOI structure can be formed on an inexpensive bulk Si substrate, it is not necessary to use an expensive SOI substrate, so cost reduction can be achieved.

本実施形態に係る半導体装置の製造方法においても、第１の実施形態と同様の理由によって、工程数を削減することが可能となる。また同様に、安価なバルクＳｉ基板にＳＯＩ構造のナノワイヤー-フィン型ＦＥＴを形成できるので、高価なＳＯＩ基板を利用しないで済むので低コスト化が図れる。

[0051]

Furthermore, since it is possible to form a deep element isolation insulating film (STI) and a nanowire having a small diameter on the bulk substrate with the same height, the subsequent manufacturing process is facilitated. For example, the requirement for the depth of focus (DOF) of lithography can be relaxed, so that the resolution can be increased. Further, since the over-etching amount with respect to the gate insulating film can be reduced by the RIE process of the gate electrode, the reliability of the film can be improved.

さらにまた、深い素子分離絶縁膜（ＳＴＩ）と直径の小さいナノワイヤーをバルク基板上で表面高さを揃えて形成することができるので、その後の製造プロセスが容易になる。例えば、リソグラフィの焦点深度（ＤＯＦ）に対する要求を緩めることができるので、解像度を高めることができる。また、ゲート電極のＲＩＥ工程で、ゲート絶縁膜に対するオーバーエッチング量を低減できるので、その膜の信頼性を改善することができる。

[0052]

Furthermore, since the entire periphery of the nanowire-fin becomes a channel, it is possible to form a gate all around-fin type FET, which can push forward the miniaturization and high performance of the transistor.

さらにまた、ナノワイヤー-フィンの周り全体がチャネルになるため、ゲートオールアラウンド-フィン型ＦＥＴを形成することができ、トランジスタの微細化、高性能化を押し進めることができる。

[0053]

As described above, according to the present embodiment, it is possible to mix the nano wire-fin FET and the planar MOSFET device by a simple process at low cost.

以上説明したように、本実施形態によれば、ナノワイヤー-フィン型ＦＥＴ、プレーナ型ＭＯＳＦＥＴデバイスを簡便なプロセスで、かつ低コストに混載させることが可能となる。

[0054]

In the above embodiment, the fabrication cost is reduced when the nano wire-fin type FET is mounted on the same substrate as the planar type MOSFET, while applying the damascene process to the gate formation of the nanowire-fin type FET.

上記実施形態においては、ナノワイヤー-フィン型ＦＥＴのゲート形成にダマシンプロセスを適用しつつ、ナノワイヤー-フィン型ＦＥＴをプレーナ型ＭＯＳＦＥＴと同じ基板上に混載する際の製造コストを削減している。

Therefore, the following variations can also be mentioned.

したがって、以下のような変形例も挙げられる。

[0055]

First, a first modified example will be described with reference to FIGS. 24 to 28.

まず、第１の変形例を、図２４乃至図２８を用いて説明する。

In the first modified example, the process up to FIG. 18 is the same as in the above embodiment. Thereafter, a dopant is ion-implanted into the dummy gates 28 and 63 made of polysilicon or the like, and then activation annealing is performed (not shown).

第１の変形例は、図１８までの工程は上記実施形態と同じである。そのあと、ポリシリコン等からなるダミーゲート２８及び６３にドーパントをイオン注入し、その後、活性化アニールを行う（図示せず）。

[0056]

Further, as shown in FIG. 24, the polysilicon planar region is covered with a resist 66, and the dummy gate 28 is etched away by CDE (Chemical Dry Etching) or the like to open the fin region. Thereafter, when the resist 66 is peeled off and etched with a HF (hydrofluoric acid) chemical solution, as shown in FIG. 25, etching progresses also to the bottom portions of the Si - nanowires 18 and 19 in the channel region, and a hollow structure is formed . The state of FIG. 25 is shown in a bird's eye view as shown in FIG. 26.

さらに、図２４に示すように、ポリシリコンプレーナ領域をレジスト６６で覆い、ダミーゲート２８をＣＤＥ（ケミカル・ドライ・エッチング）などでエッチング除去することによりフィン領域を開口する。その後、レジスト６６を剥離して、ＨＦ（フッ酸）薬液でエッチングすると、図２５に示すように、チャネル領域のＳｉ-ナノワイヤー１８、１９の底部にもエッチングが進み、中空構造が形成される。図２５の状態を鳥瞰図で示すと図２６のようになる。

[0057]

Then, as shown in FIG. 27, oxynitride film (SiON) gate insulating films 30 and 31 are formed on the entire surface of the nano wires 18 and 19 (upper surface, side surface, bottom surface of the fin), and a metal material Is deposited on the gate electrode material 32. Finally, by flattening the CMP and removing the unnecessary portion of the gate electrode material 32, as shown in FIG.

28, the planar region becomes the polysilicon electrode 63 and the fin region becomes the metal electrode 32. The subsequent manufacturing process is the same as the manufacturing process of ordinary LSI.

そして、図２７に示すように、ナノワイヤー１８、１９の表面全面（フィンの上面、側面、底面）に酸窒化膜（ＳｉＯＮ）ゲート絶縁膜３０、３１を形成し、さらにその上から例えばメタル材料であるゲート電極材料３２を堆積する。最後に、ＣＭＰ平坦化して不要部分のゲート電極材料３２を除去すると、図２８に示すように、プレーナ領域がポリシリコン電極６３で、フィン領域がメタル電極３２となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

[0058]

Next, a second modified example will be described with reference to FIGS. 29 to 30. In the second modification, the process up to FIG. 28 is the same as in the first modification, the planar region is a polysilicon electrode and the fin region is a metal electrode FET. However, it is not necessary to perform doping on the dummy gates 28 and 63 made of polysilicon or the like performed in the first modified example in FIG.

次に、第２の変形例を、図２９乃至図３０を用いて説明する。第２の変形例も、図２８までの工程は第１の変形例と同じで、プレーナ領域がポリシリコン電極で、フィン領域がメタル電極のＦＥＴある。ただし、図１８において第１の変形例で行ったポリシリコン等からなるダミーゲート２８及び６３へのドーピングは行わなくとも良い。

[0059]

First, in the state of FIG. 28, Ni 70 is sputtered as shown in FIG. 29, and then annealing is performed. Next, as shown in FIG. 30, surplus Ni 70 is removed with a mixed solution of sulfuric acid and hydrogen peroxide water. The polysilicon region 63 is Ni silicide 71 by the above annealing. The annealing temperature at this time is desirably about 300 ° C. to 600 ° C., typically 500 ° C.

まず、図２８の状態で、図２９に示すようにＮｉ７０をスパッタし、その後、アニールする。次に、図３０に示すように、硫酸と過酸化水素水の混合溶液で余剰のＮｉ７０を剥離する。ポリシリコン領域６３は上記アニールによってＮｉシリサイド７１になっている。この時のアニール温度は３００°Ｃ～６００°Ｃ程度が望ましく、典型的には５００°Ｃである。

[0060]

At this time, from the viewpoint of ease of fabrication, it is desirable that the metal electrode 32 of the fin region is made of a material which hardly reacts with Ni 70 by annealing at 500 ° C. From the viewpoint of work function control, when using a material capable of reacting with Ni

at the annealing temperature at the time of silicide, it is desirable to form a two-layered structure using a material which does not easily react with Ni at an annealing temperature as a cap film. Examples of the material which is difficult to react with Ni include TiN, TaN, WN, AlN, HfC, HfB, TaC, and mixtures thereof.

このとき、作り易さの点から、フィン領域のメタル電極３２は５００°Cのアニールで
ＮｉＳｉと反応しにくい材料が望ましい。また、仕事関数制御の点から、シリサイド時のアニール温度でＮｉと反応しうる材料を用いる際には、アニール温度でＮｉと反応しにくい材料をキャップ膜として、２層構造にすることが望ましい。Ｎｉと反応しにくい材料としては、例えば、ＴｉＮ、ＴａＮ、ＷＮ、ＡｌＮ、ＨｆＣ、ＨｆＢ、ＴａＣ及びこれらの混合物などが挙げられる。

[0061]

Further, C, Cr, Fe, Ge, B, P, As, Sn, Ga, In, P, Sb, S, Cl, F, etc. are added for improving the thermal stability and adjusting the work function Also good. Examples of materials that can react with Ni include Co, Ni, Pt, Ti, Hf, Zr, Ta, W, Mo, Al and alloys thereof, and mixtures of these materials with Si. In order to adjust the work function, the same additives as described above may be mixed.

さらに、熱的安定性の向上、仕事関数の調整のため、Ｃ、Ｃｒ、Ｆｅ、Ｇｅ、Ｂ、Ｐ、Ａｓ、Ｓｎ、Ｇａ、Ｉｎ、Ｐ，Ｓｂ、Ｓ、Ｃｌ、Ｆなどを添加しても良い。Ｎｉと反応しうる材料としては、例えば、Ｃｏ、Ｎｉ、Ｐｔ、Ｔｉ、Ｈｆ、Ｚｒ、Ｔａ、Ｗ、Ｍｏ、Ａｌ及びこれらの合金、これらの材料とＳｉとの混合物が挙げられる。仕事関数の調整のため、上述の同様の添加剤を混ぜても良い。

[0062]

According to this modification, as shown in FIG. 30, the planar region is the Ni silicide electrode 71 and the fin region is the metal electrode 32. The subsequent manufacturing process is the same as the manufacturing process of ordinary LSI.

本変形例によると、図３０に示すように、プレーナ領域がＮｉシリサイド電極７１で、フィン領域がメタル電極３２となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

[0063]

Further, a third modified example will be described with reference to FIGS. 31 to 33. In the third modified example, the process up to FIG. 28 is the same as in the first modification, the planar region is a polysilicon electrode and the fin region is a metal electrode FET. However, it is not necessary to perform doping on the dummy gates 28 and 63 made of polysilicon or the like

performed in the first modified example in FIG.

さらに、第３の変形例を図３１乃至図３３を用いて説明する。第３の変形例も、図２８までの工程は第１の変形例と同じで、プレーナ領域がポリシリコン電極で、フィン領域がメタル電極のＦＥＴである。ただし、図１８において第１の変形例で行ったポリシリコン等からなるダミーゲート２８及び６３へのドーピングは行わなくとも良い。

[0064]

First, in the state of FIG. 28, the polysilicon 63 in the planar region is peeled off with CDE or the like as shown in FIG. 31. Next, as shown in FIG. 32, a planar metal electrode 33 is formed. The material of the metal electrode 33 can be selected from the materials listed as the metal material used for the gate electrode material of the fin region and may be the same as or different from the fin region.

まず、図２８の状態で、図３１に示すようにＣＤＥなどでプレーナ領域のポリシリコン６３を剥離する。次に、図３２に示すように、プレーナ用のメタル電極３３を成膜する。メタル電極３３の材料は、フィン領域のゲート電極材料に用いるメタル材料として挙げたものから選択することができ、フィン領域と同じでも、異なっても構わない。

[0065]

Further, as shown in FIG. 33, planarization is performed by CMP. As a result, the planar region and the fin region are both metal electrodes. The subsequent manufacturing process is the same as the manufacturing process of ordinary LSI.

さらに、図３３に示すようにＣＭＰで平坦化する。その結果、プレーナ領域、フィン領域がともにメタル電極となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

[0066]

Further, a fourth modified example will be described with reference to FIGS. 34 to 42. FIG. The fourth modification is similar to the present (second) embodiment up to the point where the dummy gate insulating films 26, 27, and 62 are formed in FIG. 15.

さらに、第４の変形例を、図３４乃至４２を用いて説明する。第４の変形例は、図１５でダミーゲート絶縁膜２６、２７、及び６２を形成するところまでは、本（第２の）実施形態と同様である。

[0067]

Thereafter, as shown in FIG. 34, the dummy gate polysilicon 28 of the fin region is processed and formed, and as shown in FIG. 35, the TEOS film 29 is formed. Further, as shown in FIG. 36, planarization is performed by CMP. Then, as shown in FIG. 37, the dummy gate 28 of the fin region is peeled off with CDE, and further etching is performed with HF chemical liquid as shown in FIG.

その後、図３４に示すようにフィン領域のダミーゲートポリシリコン２８を加工形成し、図３５に示すように、ＴＥＯＳ膜２９を成膜する。さらに、図３６に示すように、ＣＭＰで平坦化する。次いで、図３７に示すようにフィン領域のダミーゲート２８をＣＤＥで剥離し、さらに、図３８に示すように、ＨＦ薬液でエッチングする。

[0068]

Thereafter, oxynitride film (SiON) gate insulating films 30 and 31 are formed on the entire surfaces of the nano wires 18 and 19, a metal material 32 is formed, flattened by CMP, and at the same time, surplus metal in the planar region is peeled off To obtain the structure of FIG.

その後、ナノワイヤー１８、１９の表面全面に酸窒化膜（ＳｉＯＮ）ゲート絶縁膜３０、３１を形成し、メタル材料３２を成膜して、ＣＭＰで平坦化すると同時に、プレーナ領域の余剰メタルを剥離することにより、図３９の構造を得る。

[0069]

Next, as shown in FIG. 40, a groove 75 is formed in the TEOS film 29 in the gate shape of the planar region.

次いで、図４０に示すように、プレーナ領域のゲート形状にＴＥＯＳ膜２９に溝７５を形成する。

The groove 75 is obtained by opening a resist (not shown) in a gate shape on the planar region by lithography, and etching the TEOS film 29 by RIE. It may be combined with etching by HF as well as RIE.

溝７５は、リソグラフィ法を用いて、プレーナ領域上にゲート形状にレジスト（図示せず）を開口し、ＲＩＥでＴＥＯＳ膜２９をエッチングすることで得られる。ＲＩＥだけでなく、ＨＦによるエッチングと組み合わせても良い。

[0070]

Next, as shown in FIG. 41, the gate insulating film 76 and the metal electrode 42 are formed.

Finally, as shown in FIG. 42, at the same time as flattening by CMP, excess metal in the fin region is peeled off. As a result, the planar region and the fin region are both the metal electrodes 42 and 32. The subsequent manufacturing process is the same as the manufacturing process of ordinary LSI.

次いで、図４１に示すように、ゲート絶縁膜７６とメタル電極４２を成膜する。最後に、図４２に示すように、ＣＭＰで平坦化すると同時に、フィン領域の余剰メタルを剥離する。その結果、プレーナ領域、フィン領域がともにメタル電極４２、３２となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

[0071]

As described above, according to the modification of the present embodiment, the nanowire-fin FET and the planar MOSFET device can be mixedly mounted at a low cost by a simple process.

以上説明したように、本実施形態の変形例によっても、ナノワイヤー-フィン型ＦＥＴ、プレーナ型ＭＯＳＦＥＴデバイスを簡便なプロセスで、かつ低コストに混載させることが可能となる。

[0072]

Third Embodiment A method of manufacturing a semiconductor device according to a third embodiment of the present invention will be described below with reference to FIGS. 43 to 57.

(第３の実施形態) 本発明の第３の実施形態に係る半導体装置の製造方法を、図４３乃至図５７を用いて以下に説明する。

[0073]

In the present embodiment, planar regions are simultaneously formed at both ends of the fin of the nanowire-fin type FET as shown in FIG. 1.

本実施形態においては、図１に示したようなナノワイヤー-フィン型ＦＥＴのフィンの両端にプレーナ領域を同時形成する。

[0074]

Also in the present embodiment, basically the same steps as the steps of FIGS. 2 to 11 of the first embodiment are executed.

本実施形態においても、第１の実施形態の図２乃至図１１までの工程と基本的に同様な工程が実行される。

However, in the present embodiment, unlike FIG. 3, a hard mask 35 having a shape in which a planer region having a larger lateral width than the fin is connected to both ends of the nanowire-fin as shown in the top view of FIG. 43 Is formed on the bulk Si substrate 10.

しかし、本実施形態においては図３とは異なって、図４３の上面図に示すような、ナノワイヤー-フィンの両端に当該フィンより横幅の広いプレーナ領域が接続された形状であるハードマスク３５をバルクＳｉ基板１０の上に形成する。

[0075]

Here, the hard mask 35 is, for example, a SiN film having a film thickness of about 50 nm, but it may be a laminated film of SiO 2, SiON, or even SiN / SiO 2 / SiN, or another insulating film.

ここで、ハードマスク３５は例えば、膜厚５０nm程度のＳｉＮ膜であるが、ＳｉＯ２、あるいはＳｉＯＮ、更にはＳｉＮ／ＳｉＯ２／ＳｉＮ等の積層膜、その他の絶縁膜であってもかまわない。

FIG. 44 is a cross-sectional view taken along line BB 'of FIG. 43 and a cross-sectional view taken along line AA'.

図４３のＢ－Ｂ’線に沿った断面図及びＡ－Ａ’線に沿った断面図を図４４に示す。

[0076]

Thereafter, as in the steps of FIGS. 4 to 11 of the first embodiment, the cross section (planar region) along the line BB 'of FIG. 43 and the cross section (fin region) along the line AA' The processes shown in FIGS. 45 to 52 are executed.

その後、第１の実施形態の図４乃至図１１までの工程と同様に、図４３のＢ－Ｂ’線に沿った断面（プレーナ領域）及びＡ－Ａ’線に沿った断面（フィン領域）で見た図４５乃至図５２に示される工程が実行される。

[0077]

First, RIE processing is performed using the hard mask 35 as a mask, whereby a groove having a depth of about 20 nm is formed in the bulk Si substrate 10 as shown in FIG.

まず、ハードマスク３５をマスクとしてＲＩＥ加工を行なうことにより図４５に示すように、

２０nm程度の深さの溝がバルクＳｉ基板１０に形成される。

In FIG. 45 (a) and FIG. 45 (b), only the middle of the groove on both sides is shown here.

ここでは、図４５（a)、(b)共に両側の溝の途中までしか示していない。

In FIGS. 45 (a) and 45 (b), for example, a plurality of hard masks 35 shown in FIG. 43 are juxtaposed, so that structures similar to those shown in FIGS. 45 (a) and 45 (b) , And may show a cross section of a part thereof. The same shall apply hereinafter.

図４５（a)、(b)は、例えば、図４３で示したハードマスク３５が複数並列しており、そのため図４５（a)、(b)の左右にそれと同様な構造が並列していて、その一部の断面を示しているとしてもよい。以下も同様とする。

[0078]

Next, as shown in FIG. 46, after forming the SiN film 14 on the entire surface from above, etching is performed as shown in FIG. 47 to form the side wall insulating film 14 of SiN having a thickness of about 20 nm on the side surface of the groove Form. As the side wall insulating film 14, SiO 2, SiON, or another insulating film may be used.

次に、図４６に示すように、この上からＳｉＮ膜１４を全面に形成した後、図４７に示すようにエッチバックすることにより溝の側面に厚さ２０nm程度のＳｉＮの側壁絶縁膜１４を形成する。側壁絶縁膜１４としては、ＳｉＯ２、ＳｉＯＮ、或いはその他の絶縁膜を用いてもかまわない。

[0079]

Then, as shown in FIG. 48, the Si substrate 10 is etched using the hard mask 35 and the sidewall insulating film 14 as a mask to further dig deeply the trench.

次いで、図４８に示すようにハードマスク３５と側壁絶縁膜１４をマスクとしてＳｉ基板１０をエッチングして溝をさらに深く掘る。

[0080]

Next, as shown in FIG. 49, the surface of the Si substrate 10 exposed at the bottom of the groove is oxidized using the hard mask 35 and the sidewall insulating film 14 as an oxidation resistant mask to form an oxide film 16.

次に、図４９に示すようにハードマスク３５と側壁絶縁膜１４を耐酸化性マスクとして溝底部に露出したＳｉ基板１０の表面を酸化して酸化膜１６を形成する。

At that time, the thickness of the oxide film is adjusted so that oxide films 16 from both side surfaces of the silicon fin bottoms are in contact with each other in the fin type FET region.

その際、フィン型ＦＥＴ領域においてシリコンフィン底部の両側面からの酸化膜１６が互いに接するように酸化膜厚を調整する。

[0081]

As a result, a structure in which the fin region 18, which is a semiconductor region, remains partially on the oxide film 16, that is, an SOI structure is formed only in the fin type FET region. On the other hand, in the planar region formed so as to have a wider width, the oxide film from both side walls does not come into contact with the planar region, so that the SOI structure can not be obtained.

その結果フィン型ＦＥＴ領域のみ部分的に、酸化膜１６の上に半導体領域であるフィン領域１８が残存する構造、即ちＳＯＩ構造が形成される。他方、幅が広くなるように形成したプレーナ領域では、両側壁からの酸化膜が接しないのでＳＯＩ構造とはならない。

[0082]

Next, as shown in FIG. 50, an element isolation insulating film (STI) 17 made of an SiO 2 -based insulating film is deposited on the entire surface by HDP (High Density Plasma: High Density Plasma) or the like, and CMP (Chemical Mechanical Polishing: Chemical mechanical polishing) Planarization is performed to expose the SiN hard mask 35. Then, as shown in FIG. 51, the element isolation insulating film (STI) 17 is etched.

次に図５０に示すように、ＨＤＰ(High Density Plasma：高密度プラズマ)などを用いてＳｉＯ２系絶縁膜からなる素子分離絶縁膜(ＳＴＩ)１７を全面に堆積し、更にＣＭＰ(Chemical Mechanical Polishing：化学的機械的研磨)平坦化を実行して、ＳｉＮハードマスク３５を露出させる。そしてさらに、図５１に示すように素子分離絶縁膜(ＳＴＩ)１７をエッチングする。

[0083]

Next, as shown in FIG. 52, the SiN hard mask 35 and the SiN sidewall insulating film 14 are removed with hot phosphoric acid or the like, so that the upper surface and both side surfaces of the fin 18 are exposed in the fin type FET region.

次いで、図５２に示すように、ＳｉＮハードマスク３５及びＳｉＮ側壁絶縁膜１４をホットリン酸などで除去することにより、フィン型ＦＥＴ領域においてはフィン１８の上面および両側面が露出する。

[0084]
As described above, also in the present embodiment, it is possible to simultaneously perform the RIE processing of the fin-type FET and the planar region.

以上のように本実施形態においても、フィン型ＦＥＴとプレーナ領域のＲＩＥ加工を同時に行なうことができる。

[0085]
FIG. 53 is a perspective view showing the three-dimensional structure of the semiconductor device taken along line CC 'shown in FIGS. 52 (a) and 52 (b) when proceeding to the step of FIG. 52.

図５３は、図５２の工程まで進んだ時の、図５２（ａ）及び（ｂ）に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図である。

A planar region 20 having a lateral width larger than that of the fin 18 is connected to both ends of the nanowire-fin 18, respectively.

ナノワイヤー-フィン１８の両端には、フィン１８より横幅が大きいプレーナ領域２０がそれぞれ接続されている。

[0086]
Thereafter, as shown in FIG. 54 which is a cross-sectional view taken along the line AA ', a gate insulating film 36 made of, for example, an oxynitride film (SiON) or the like is formed on the upper surface and both side surfaces of the nanowire-fin 18 .

この後、Ａ－Ａ’線に沿った断面図である図５４に示すようにナノワイヤー-フィン１８の上面及び両側面に、例えば、酸窒化膜（ＳｉＯＮ）等からなるゲート絶縁膜３６を形成する。

[0087]
Further, a gate electrode material such as polysilicon or metal is deposited thereon, and gate electrodes 37 are formed by lithography and RIE as shown in FIG. 55.

更にその上に、ポリシリコン或いはメタル等のゲート電極材料を堆積し、図５５に示すように、リソグラフィとＲＩＥでゲート電極３７を形成する。

56 is a perspective view showing a three-dimensional structure of the semiconductor device taken along line CC 'shown in FIG. 55. FIG.

図５６は、図５５に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図である。

[0088]
Thereafter, spacers are formed on both side surfaces of the gate electrode 37 in FIG. 55 in the direction perpendicular to the paper surface, and a source / drain is formed by ion implantation or silicide bonding (not shown).

その後、図５５のゲート電極３７の紙面垂直方向の両側面にスペーサを形成し、ソース／ドレインをイオン注入やシリサイド貼り付けによって形成する（図示せず）。

Since the aspect ratio of the fin 18 of the nanowire-fin type FET is small, the doping for forming the source / drain diffusion layer may be ion implantation in which the angle formed with the direction perpendicular to the substrate is 0 to 7 degrees. Therefore, expensive techniques such as oblique ion implantation technique and plasma doping technique are unnecessary, so that the cost of the process can be reduced.

ナノワイヤー-フィン型ＦＥＴのフィン１８のアスペクト比は小さいので、ソース／ドレイン拡散層を形成するためのドーピングは、基板に垂直な方向とのなす角度が０～７度となるイオン注入でよい。従って、斜めイオン注入技術やプラズマドーピング技術等の高価な技術が不要となるので、プロセスの低コスト化が図れる。

[0089]
The fin type FET manufactured in this embodiment is a tri-gate fin type FET since the upper surface and both side surfaces of the fin are channels.

本実施形態で製造されるフィン型ＦＥＴは、フィンの上面及び両側面がチャネルになるため、トライゲート（Tri gate）フィン型ＦＥＴとなっている。

[0090]
Thereafter, as shown in FIG. 57, an interlayer insulating film is deposited (not shown), and a contact 38 for connection with an upper layer wiring (Cu or the like) is formed.

その後、図５７に示すように、層間絶縁膜を堆積し（図示せず）、上層配線（Ｃｕなど）と接続するためのコンタクト３８を形成する。

Here, since the lateral width of the planar region 20 is formed to be larger than the lateral width of the nanowire-fin 18, the interface resistance between the contact 38 and the source / drain region 40 can be reduced.

ここで、プレーナ領域２０の横幅がナノワイヤー-フィン１８の横幅より大きくなるように形成されているため、コンタクト３８とソース／ドレイン領域４０との界面抵抗を小さくすることができる。

[0091]
Further, even if the contacts are misaligned to form contacts 39, the contact with the planar region 20 is maintained and the structure is resistant to alignment misalignment.

また、コンタクトの位置合わせにずれが生じてコンタクト３９のように形成されたとしても、プレーナ領域２０との接触が維持され、合わせずれに強い構造となっている。

[0092]
As described above, according to the present embodiment in which the fin-type FET and the planar region are formed at the same time, it is possible to reduce the number of processes and reduce the cost similarly to the first and second embodiments, and at the same time, It is possible to manufacture a semiconductor device including a nanowire-fin type FET which is small and resistant to misalignment.

以上述べたように、フィン型ＦＥＴとプレーナ領域を同時形成する本実施形態によって、第１及び第２の実施形態と同様な工程の削減と低コスト化が図れると同時に、コンタクトとの界面抵抗が小さく、合わせずれに強いナノワイヤー-フィン型ＦＥＴを備えた半導体装置の製造が可能となる。

[0093]
It is to be noted that the present invention is not limited to the above-described embodiment, and various modifications can be made in the implementation stage without departing from the gist

thereof.

なお、本願発明は上記実施形態に限定されるものではなく、実施段階ではその要旨を逸脱しない範囲で種々に変形することが可能である。

Furthermore, the above embodiments include inventions at various stages, and various inventions can be extracted by appropriately combining a plurality of disclosed constitutional requirements.

更に、上記実施形態には種々の段階の発明が含まれており、開示される複数の構成要件における適宜な組み合わせにより種々の発明が抽出されうる。

For example, even if some constituent requirements are deleted from all the constituent features shown in the embodiment, the problem described in the section of the problem to be solved by the invention can be solved and the effect described in the effect of the invention , A configuration in which the constituent requirements are deleted can be extracted as an invention.

例えば、実施形態に示される全構成要件からいくつかの構成要件が削除されても、発明が解決しようとする課題の欄で述べた課題が解決でき、発明の効果の欄で述べられている効果が得られる場合には、この構成要件が削除された構成が発明として抽出されうる。

[0094]

FIG. 2 is a view showing a three-dimensional structure of a nanowire-fin FET according to an embodiment of the present invention. FIG. 4 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device according to the first embodiment of the present invention. FIG. 4 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 2. FIG. 3 is a cross-sectional view showing one step of a method of manufacturing a semiconductor device continued from FIG. 3. FIG. 4 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 4. FIG. 5 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 5. FIG. 6 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 6. FIG. 7 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 7. FIG. 8 is a cross-sectional view showing one step of a method of manufacturing a semiconductor device continued from FIG. 8. 9 is a cross-sectional view showing one step of a method of manufacturing a semiconductor device continued from FIG. 10, which is a cross-sectional view showing one step of a method of

manufacturing a semiconductor device continued from FIG. 9. FIG. 11 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 11. FIG. 12 is a cross-sectional view showing one step of the method for manufacturing the semiconductor device continued from FIG. 12. FIG. 13 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 13. FIG. 7 is a cross-sectional view showing one step of a method of manufacturing a semiconductor device according to a second embodiment of the present invention. 15 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 15; FIG. FIG. 16 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 16. FIG. 17 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 17. FIG. 18 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 18. 19 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 19; FIG. FIG. 20 is a view showing the state of FIG. 20 in a bird's-eye view. FIG. 21 is a cross-sectional view taken along a dotted line in FIG. 21. FIG. 20 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 20. FIG. 7 is a cross-sectional view showing one step of a method for manufacturing a semiconductor device according to a first modification of the second embodiment of the present invention. 24 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 24. FIG. FIG. 25 is a view showing the state of FIG. 25 in a bird's-eye view. FIG. 26 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 26. FIG. 27 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 27. FIG. 7 is a cross-sectional view showing one step of a method for manufacturing a semiconductor device according to a second modification of the second embodiment of the present invention. FIG. 29 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 29. Sectional view showing one step of a method of manufacturing a semiconductor device according to a third modification of the second embodiment of the present invention. FIG. 31 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 31. FIG. 32 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 32. FIG. 7 is a cross-sectional view showing one step of a method of manufacturing a semiconductor device according to a fourth modification of the second embodiment of the present invention. FIG. 34 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 34.

本発明の実施形態に係るナノワイヤー-フィン型ＦＥＴの３次元構造を示した図。 本発明の第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図。 図２に続く半導体装置の製造方法の一工程を示す断面図。 図３に続く半導体装置の製造方法の一工程を示す断面図。 図４に続く半導体装置の製造方法の一工程を示す断面図。 図５に続く半導体装置の製造方法の一工程を示す断面図。 図６に続く半導体装置の製造方法の一工程を示す断面図。 図７に続く半導体装置の製

造方法の一工程を示す断面図。図８に続く半導体装置の製造方法の一工程を示す断面図。図９に続く半導体装置の製造方法の一工程を示す断面図図１０に続く半導体装置の製造方法の一工程を示す断面図。図１１に続く半導体装置の製造方法の一工程を示す断面図。図１２に続く半導体装置の製造方法の一工程を示す断面図。図１３に続く半導体装置の製造方法の一工程を示す断面図。本発明の第２の実施形態に係る半導体装置の製造方法の一工程を示す断面図。図１５に続く半導体装置の製造方法の一工程を示す断面図。図１６に続く半導体装置の製造方法の一工程を示す断面図。図１７に続く半導体装置の製造方法の一工程を示す断面図。図１８に続く半導体装置の製造方法の一工程を示す断面図。図１９に続く半導体装置の製造方法の一工程を示す断面図。図２０の状態を鳥瞰図で示した図。図２１の点線に沿った断面図。図２０に続く半導体装置の製造方法の一工程を示す断面図。本発明の第２の実施形態の第１の変形例に係る半導体装置の製造方法の一工程を示す断面図。図２４に続く半導体装置の製造方法の一工程を示す断面図。図２５の状態を鳥瞰図で示した図。図２６に続く半導体装置の製造方法の一工程を示す断面図。図２７に続く半導体装置の製造方法の一工程を示す断面図。本発明の第２の実施形態の第２の変形例に係る半導体装置の製造方法の一工程を示す断面図。図２９に続く半導体装置の製造方法の一工程を示す断面図。本発明の第２の実施形態の第３の変形例に係る半導体装置の製造方法の一工程を示す断面図。図３１に続く半導体装置の製造方法の一工程を示す断面図。図３２に続く半導体装置の製造方法の一工程を示す断面図。本発明の第２の実施形態の第４の変形例に係る半導体装置の製造方法の一工程を示す断面図。図３４に続く半導体装置の製造方法の一工程を示す断面図。

FIG. 35 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 35. FIG. 36 is a cross-sectional view showing one step of the method for manufacturing the semiconductor device continued from FIG. 36. FIG. 37 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 37. FIG. 38 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 38. FIG. 39 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 39. FIG. 40 is a cross-sectional view showing one step of the method for manufacturing the semiconductor device continued from FIG. 40. FIG. 41 is a cross-sectional view showing one step of the method of manufacturing the semiconductor device continued from FIG. 41. FIG. 7 is a top view showing one step of a method of manufacturing a semiconductor device according to a third embodiment of the present invention. (A) is a cross-sectional view taken along line BB 'of FIG. 43, and (b) is a cross-sectional view taken along line AA' of FIG. 43. (A) is a cross-sectional view taken along line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 44, and (b) is a cross-sectional view taken along line AA'. (A) is a cross-sectional view taken along the line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 45, and (b) is a cross-sectional view taken along the line AA'. (A) is a cross-sectional view taken along the line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 46, and (b) is a cross-sectional view taken along the line AA'. (A) is a cross-sectional view taken along the line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 47, and (b) is

a cross-sectional view taken along the line AA'. (A) is a cross-sectional view taken along the line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 48, and (b) is a cross-sectional view taken along the line AA'. (A) is a cross-sectional view taken along the line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 49, and (b) is a cross-sectional view taken along line AA'. (A) is a cross-sectional view taken along the line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 50, and (b) is a cross-sectional view taken along the line AA'. (A) is a cross-sectional view taken along line BB 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 51, and (b) is a cross-sectional view taken along line AA'. FIG. 52 is a perspective view showing a three-dimensional structure of the semiconductor device taken along line CC 'shown in FIGS. 52 (a) and 52 (b). 52 is a cross-sectional view taken along the line A-A 'showing one step of the manufacturing method of the semiconductor device continued from FIG. 52. FIG. 54 is a cross-sectional view taken along line A-A 'showing one step of the method of manufacturing the semiconductor device continued from FIG. 54. FIG. FIG. 55 is a perspective view showing a three-dimensional structure of the semiconductor device taken along line C - C 'shown in FIG. 55. 56 is a perspective view showing a three-dimensional structure when a contact is formed in the semiconductor device shown in FIG. 56; FIG.

図３５に続く半導体装置の製造方法の一工程を示す断面図。図３６に続く半導体装置の製造方法の一工程を示す断面図。図３７に続く半導体装置の製造方法の一工程を示す断面図。図３８に続く半導体装置の製造方法の一工程を示す断面図。図３９に続く半導体装置の製造方法の一工程を示す断面図。図４０に続く半導体装置の製造方法の一工程を示す断面図。図４１に続く半導体装置の製造方法の一工程を示す断面図。本発明の第３の実施形態に係る半導体装置の製造方法の一工程を示す上面図。（ａ）は図４３のＢ－Ｂ’線に沿った断面図、（ｂ）は図４３のＡ－Ａ’線に沿った断面図。（ａ）は図４４に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図４５に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図４６に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図４７に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図４８に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図４９に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図５０に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。（ａ）は図５１に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。図５２（ａ）及び（ｂ）に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図。図５２に続く半導体装置の製造方法の一工程を示すＡ－Ａ’線に沿った断面図。図５４に続く半導体装置の製造方法の一工程を示すＡ－Ａ’線に沿った断面図。図５５に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図。図５６で示した半導体装置にコンタクトを形成したときの３次元構造を示した斜視図。

Explanation of sign

符号の説明

[0095]

10: bulk Si substrate, 11, 12, 13, 35 ... hard mask, 14 side wall insulating film, 15 ... SiN hard mask material, 16 ... oxide film, 17 element isolation insulating film (STI), 18, 19 ... nano Wire-fin 20, planar region 21, 22, 23, 36, 76 gate insulating film, 24, 25, 32, 33, 37, 42, 65 gate electrode, 26, 27, 62 dummy gate insulating film , 28, 63 ... dummy gate, 29 ... TEOS film 30, 31, 64 ... oxynitride film gate insulating film, 38, 39 ... contact, 40 ... drain region, 50 ... first groove, 60 ... second groove, 66 ... resist, 70 ... Ni, 71 ... Ni silicide, 75 ... groove, metal electrode.

１０…バルクＳｉ基板、１１、１２、１３、３５…ハードマスク、１４…側壁絶縁膜、１５…ＳｉＮハードマスク材、１６…酸化膜、１７…素子分離絶縁膜（ＳＴＩ）、１８、１９…ナノワイヤー-フィン、２０…プレーナ領域、２１、２２、２３、３６、７６…ゲート絶縁膜、２４、２５、３２、３３、３７、４２、６５…ゲート電極、２６、２７、６２…ダミーゲート絶縁膜、２８、６３…ダミーゲート、２９…ＴＥＯＳ膜３０、３１、６４…酸窒化膜ゲート絶縁膜、３８、３９…コンタクト、４０…ドレイン領域、５０…第１の溝、６０…第２の溝、６６…レジスト、７０…Ｎｉ、７１…Ｎｉシリサイド、７５…溝、メタル電極。

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CLAIMS JP2008172082

1.

Forming a line-shaped insulating film on a main surface of a semiconductor substrate; etching the semiconductor substrate with the line-shaped insulating film as a mask to form two adjacent first side Forming a trench, forming a sidewall insulating film on a sidewall of each of the adjacent first trenches, etching the semiconductor substrate using the line-shaped insulating film and the sidewall insulating film as a mask, Forming a second trench in each of the bottoms of the first trenches so as to form the second trench, oxidizing the semiconductor substrate using the linear insulating film and the sidewall insulating film as an oxidation resistant mask, A step of bringing oxidized regions formed on respective side walls adjacent to each other across the semiconductor substrate of the groove into contact with each other, a step of removing the linear insulating film and the side wall insulating film , Forming a gate insulating film on the surface of the semiconductor region of the semiconductor substrate exposed by the removal, forming a gate electrode on the gate insulating film, forming the semiconductor region as a line-shaped fin And a step of forming a fin type field effect transistor.

半導体基板の主表面にライン状の絶縁膜を形成する工程と、前記ライン状の絶縁膜をマスクとして前記半導体基板をエッチングすることにより前記ライン状の絶縁膜の両側に２つの隣接する第１の溝を形成する工程と、隣接する前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより隣接する前記第１の溝の底部それぞれに第２の溝を形成する工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させる工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜を除去する工程と、前記除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成する工程と、前記ゲート絶縁膜の上にゲート電極を形成する工程と、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程と を含むことを特徴とする半導体装置の製造方法。

2.

A step of simultaneously forming a line-shaped first insulating film and a second insulating film thicker than the first insulating film on the main surface of the semiconductor substrate, using the first and second insulating films as a mask Forming a plurality of first trenches on both sides of the first and second insulating films by etching the semiconductor substrate, forming a sidewall insulating film on sidewalls of the plurality of first trenches, Forming a second trench in each of bottom portions of the plurality of first trenches by etching the semiconductor substrate using the first and second insulating films and the sidewall insulating film as masks, 1 and the second insulating film and the sidewall insulating film as oxidation resistant masks so as to sandwich the semiconductor substrate of the second trench on both sides of the first insulating film and adjoin each other The acid formed on each sidewall Contacting oxidized regions formed on the side walls adjacent to each other with the semiconductor substrate of the second groove on both sides of the second insulating film interposed therebetween not to be in contact with each other; A gate insulating film is formed on a surface of a semiconductor region of the semiconductor substrate exposed by removing the first insulating film, a gate insulating film is formed on the gate insulating film, Forming a fin-shaped field effect transistor having the semiconductor region as a line shaped fin by forming an electrode on the semiconductor substrate; forming a fin type field effect transistor in another semiconductor region of the semiconductor substrate exposed by removing the second insulating film; And a step of forming a field effect transistor or a planar region.

半導体基板の主表面にライン状の第１の絶縁膜と前記第１の絶縁膜より線幅の太い第２の絶縁膜を同時に形成する工程と、前記第１及び第２の絶縁膜をマスクとして前記半導体基板をエッチングすることにより前記第１及び第２の絶縁膜の両側に複数の第１の溝を形成する工程と、複数の前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより複数の前記第１の溝の底部それぞれに第２の溝を形成する工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第１の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させ、前記第２の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域は互いに接触させない工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜を除去する工程と、前記第１の絶縁膜の除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成し、前記ゲート絶縁膜の上にゲート電極を形成することにより、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程と、前記第２の絶縁膜の除去によって露出した前記半導体基板の別の半導体領域にプレーナ型電界効果トランジスタ或いはプレーナ領域を形成する工程と を含むことを特徴とする半導体装置の製造方法。

3.

After the removing step and before forming the gate insulating film, a step of removing a portion

of the oxidized region under the semiconductor region to be the fin, which is in contact with the semiconductor region 3. The method of manufacturing a semiconductor device according to claim 1,

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前記除去する工程の後であって、前記ゲート絶縁膜を形成する前において、前記フィンとなるべき前記半導体領域の下の前記酸化領域の前記半導体領域に接している部分を除去する工程を 更に含むことを特徴とする請求項 1 又は 2 に記載の半導体装置の製造方法。

4.

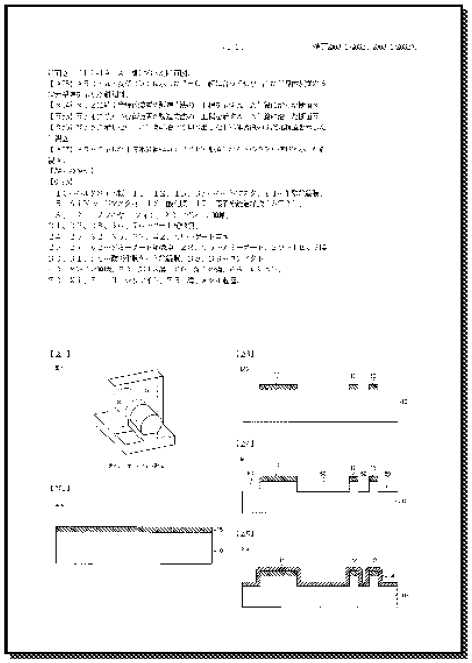
Further comprising a step of rounding the sectional shape of the semiconductor region to be the fin by annealing in an atmosphere containing hydrogen after the removing step and before forming the gate insulating film 4. The method for manufacturing a semiconductor device according to claim 1, which is characterized by the following features.

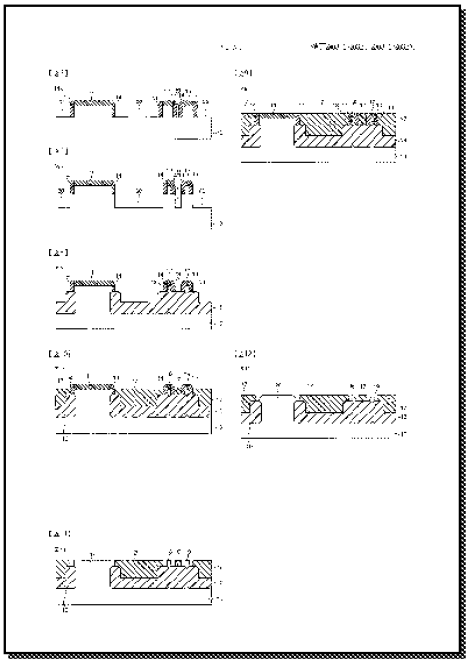
前記除去する工程の後であって、前記ゲート絶縁膜を形成する前において、水素を含んだ雰囲気中でアニールすることにより前記フィンとなるべき前記半導体領域の断面形状を丸める工程を更に含むことを特徴とする請求項 1 乃至 3 のいずれか 1 項に記載の半導体装置の製造方法。

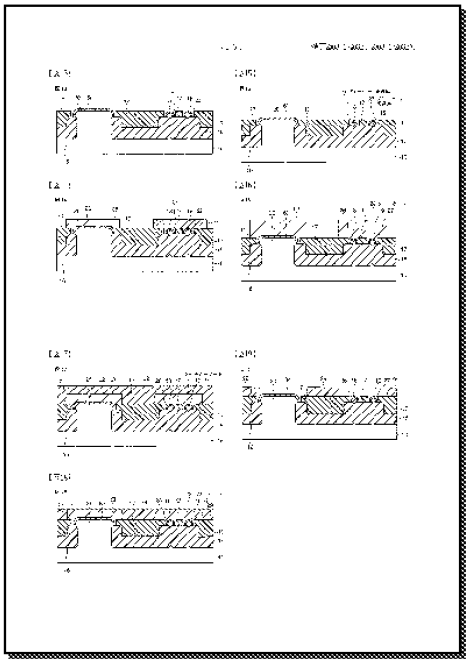
5.

What is claimed is: 1. A semiconductor device comprising: a silicon oxide film formed on a bulk silicon substrate; line-shaped fins formed on the silicon oxide film; And a planar region which is a part of the substrate in which a height of an upper surface of the fin is larger than a height of an upper surface of the fin.

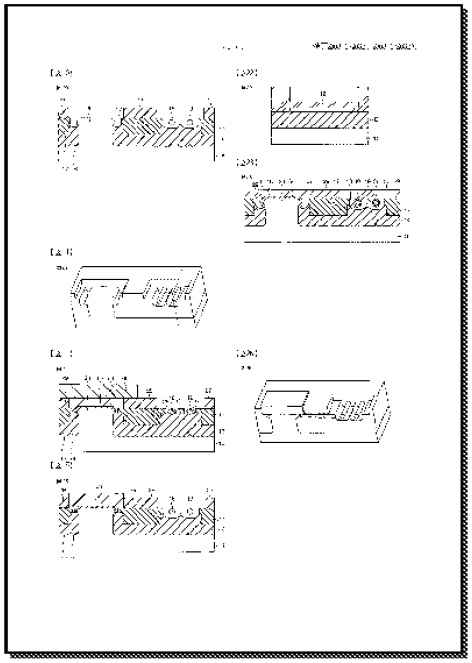
バルクシリコン基板の上に形成されたシリコン酸化膜と、前記シリコン酸化膜上に形成されたライン状のフィンと、前記フィンの延伸方向の両端にそれぞれ接続され、前記延伸方向と垂直な方向の幅が前記フィンよりも大きく、上面の高さが前記フィンの上面の高さと一致している前記基板の一部であるプレーナ領域と を具備することを特徴とした半導体装置。

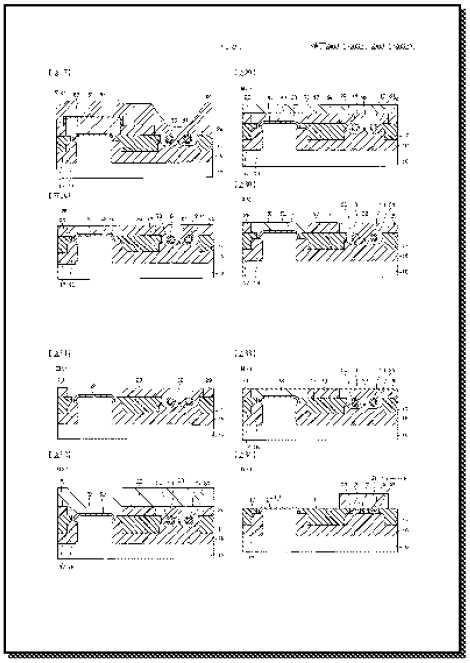


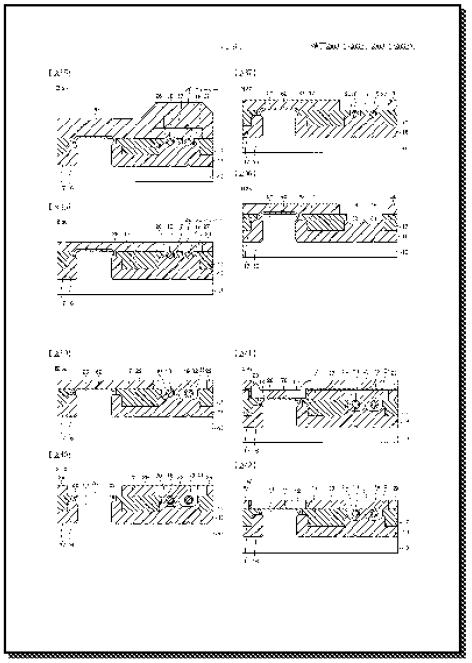


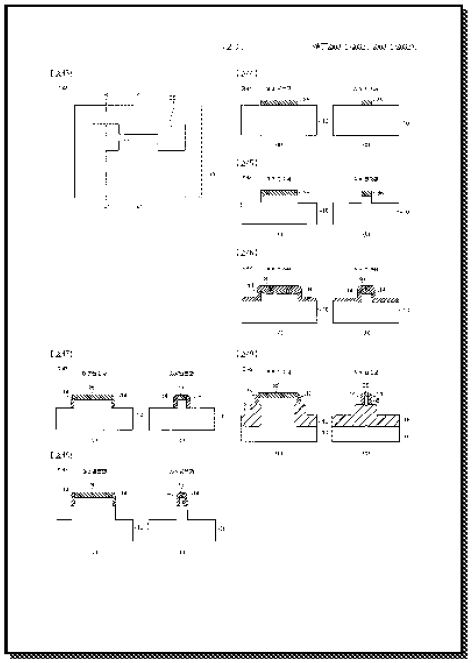


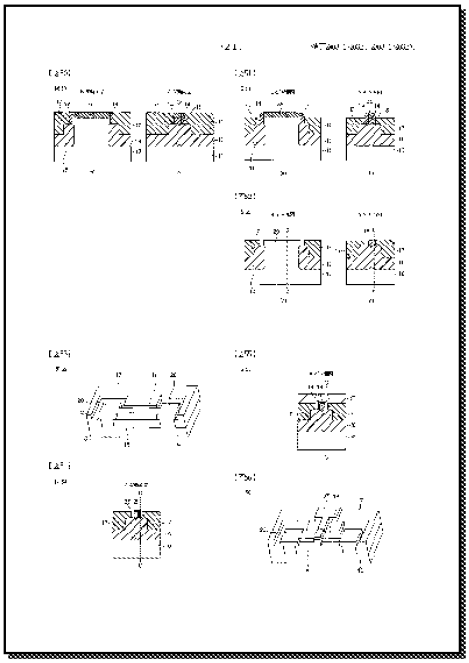
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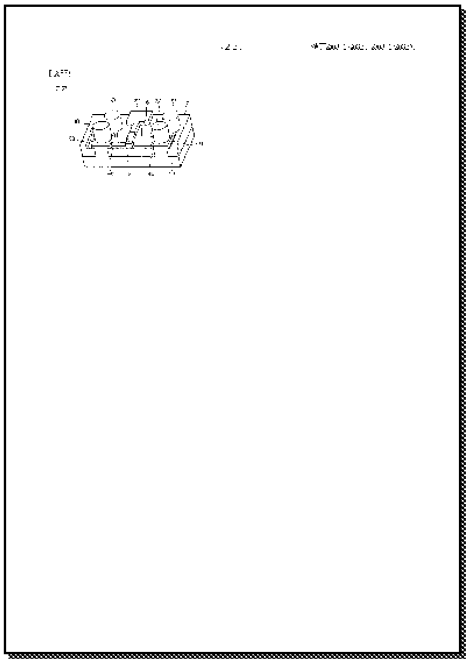




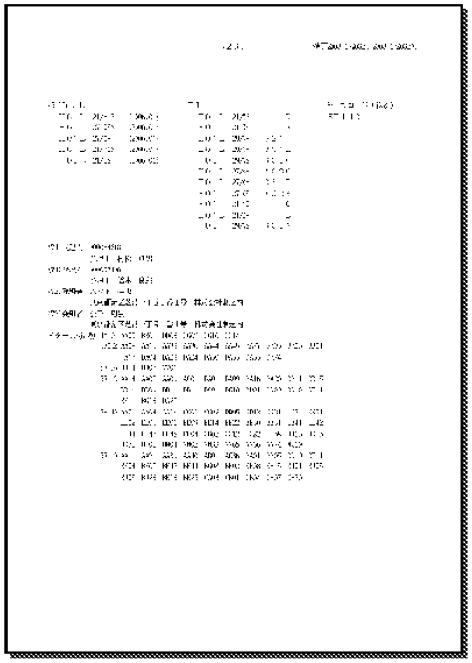








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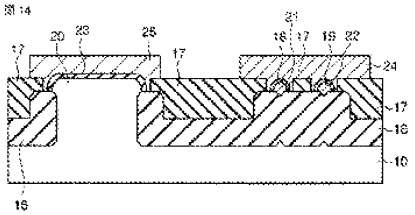
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最終頁に続く

(54)【発明の名称】半導体装置及び半導体装置の製造方法

(57)【要約】
【課題】簡便かつ低コストにプレーナ領域と混載することが可能なフィン型電界効果トランジスタを含んだ半導体装置の製造方法を提供すること。
【解決手段】半導体装置の製造方法は、基板10の主表面にライン状の絶縁膜を形成し、絶縁膜をマスクに基板をエッチングして絶縁膜の両側に第１の溝を形成し、第１の溝それぞれの側壁に側壁絶縁膜を形成し、絶縁膜及び側壁絶縁膜をマスクに基板をエッチングして第１の溝の底部それぞれに第２の溝を形成し、絶縁膜及び側壁絶縁膜を耐酸化性マスクとして基板を酸化して第２の溝の基板を挟んで隣接する側壁それぞれに形成される酸化領域16を互いに接触させ、絶縁膜及び側壁絶縁膜を除去し、除去によって露出した基板の半導体領域18の表面にゲート絶縁膜21を、その上にゲート電極24を形成し、半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程を含む。
【選択図】　図１４



【特許請求の範囲】
【請求項1】
半導体基板の主表面にライン状の絶縁膜を形成する工程と、
前記ライン状の絶縁膜をマスクとして前記半導体基板をエッチングすることにより前記ライン状の絶縁膜の両側に２つの隣接する第１の溝を形成する工程と、
隣接する前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、
前記ライン状の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより隣接する前記第１の溝の底部それぞれに第２の溝を形成する工程と、
前記ライン状の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させる工程と、
前記ライン状の絶縁膜及び前記側壁絶縁膜を除去する工程と、
前記除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成する工程と、
前記ゲート絶縁膜の上にゲート電極を形成する工程と、
前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程と
を含むことを特徴とする半導体装置の製造方法。
【請求項2】
半導体基板の主表面にライン状の第１の絶縁膜と前記第１の絶縁膜より線幅の太い第２の絶縁膜を同時に形成する工程と、
前記第１及び第２の絶縁膜をマスクとして前記半導体基板をエッチングすることにより前記第１及び第２の絶縁膜の両側に複数の第１の溝を形成する工程と、
複数の前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、
前記第１及び第２の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより複数の前記第１の溝の底部それぞれに第２の溝を形成する工程と、
前記第１及び第２の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第１の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させ、前記第２の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域は互いに接触させない工程と、
前記第１及び第２の絶縁膜及び前記側壁絶縁膜を除去する工程と、
前記第１の絶縁膜の除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成し、前記ゲート絶縁膜の上にゲート電極を形成することにより、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程と、
前記第２の絶縁膜の除去によって露出した前記半導体基板の別の半導体領域にプレーナ型電界効果トランジスタ或いはプレーナ領域を形成する工程と
を含むことを特徴とする半導体装置の製造方法。
【請求項3】
前記除去する工程の後であって、前記ゲート絶縁膜を形成する前において、
前記フィンとなるべき前記半導体領域の下の前記酸化領域の前記半導体領域に接している部分を除去する工程を
更に含むことを特徴とする請求項１又は２に記載の半導体装置の製造方法。
【請求項4】
前記除去する工程の後であって、前記ゲート絶縁膜を形成する前において、
水素を含んだ雰囲気中でアニールすることにより前記フィンとなるべき前記半導体領域の断面形状を丸める工程を更に含むことを特徴とする請求項１乃至３のいずれか１項に記載の半導体装置の製造方法。
【請求項5】

バルクシリコン基板の上に形成されたシリコン酸化膜と、
前記シリコン酸化膜上に形成されたライン状のフィンと、
前記フィンの延伸方向の両端にそれぞれ接続され、前記延伸方向と垂直な方向の幅が前記フィンよりも大きく、上面の高さが前記フィンの上面の高さと一致している前記基板の一部であるプレーナ領域と
【発明の詳細な説明】"徴とした半導体装置。
【技術分野】
【0001】
本発明は、フィン型ＦＥＴ（電界効果トランジスタ）を含んだ半導体装置およびその製造方法に関する。
【背景技術】
【0002】
フィン（Ｆｉｎ）型ＦＥＴ（ＦｉｎＦＥＴ）、特にバルク（Ｂｕｌｋ）Ｓｉ基板上に作製されたＦｉｎＦＥＴは、低コストでカットオフ特性が良好なデバイスであるため、次世代トランジスタ構造として有望視されている（例えば、特許文献１参照）。
【0003】
しかしながら、マルチ閾値電圧の実現やアナログデバイスに対応するには、プレーナ（planar）デバイスの方が簡単で低コストであるため、実際のＬＳＩでは、従来のプレーナ型ＭＯＳＦＥＴとフィン型ＦＥＴを混載することが必要である。そのため、両者を混載する簡単な製造プロセスが求められていた。
【0004】
ところが、プレーナ型ＭＯＳＦＥＴとフィン型ＦＥＴを混載すると、ゲートの表面が凸凹となって、微細なゲートを作製するためのリソグラフィを行なうことが困難になったり、フィン領域、プレーナ領域のゲートの加工を同時に行なえない等の問題があった。また、工程数が多くなり製造コストが増加するという問題もあった。
【特許文献1】特開２００５－２２９１０７号公報
【発明の開示】
【発明が解決しようとする課題】
【0005】
本発明は、簡便かつ低コストにプレーナ領域と混載することが可能なフィン型電界効果トランジスタを含んだ半導体装置及びその製造方法を提供する。
【課題を解決するための手段】
【0006】
この発明の第１の態様に係る半導体装置の製造方法は、半導体基板の主表面にライン状の絶縁膜を形成する工程と、前記ライン状の絶縁膜をマスクとして前記半導体基板をエッチングすることにより前記ライン状の絶縁膜の両側に２つの隣接する第１の溝を形成する工程と、隣接する前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより隣接する前記第１の溝の底部それぞれに第２の溝を形成する工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させる工程と、前記ライン状の絶縁膜及び前記側壁絶縁膜を除去する工程と、前記除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成する工程と、前記ゲート絶縁膜の上にゲート電極を形成する工程と、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程とを含む。
【0007】
この発明の第２の態様に係る半導体装置の製造方法は、半導体基板の主表面にライン状の第１の絶縁膜と前記第１の絶縁膜より線幅の太い第２の絶縁膜を同時に形成する工程と、
前記第１及び第２の絶縁膜をマスクとして前記半導体基板をエッチングすることにより

前記第１及び第２の絶縁膜の両側に複数の第１の溝を形成する工程と、複数の前記第１の溝それぞれの側壁に側壁絶縁膜を形成する工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜をマスクとして前記半導体基板をエッチングすることにより複数の前記第１の溝の底部それぞれに第２の溝を形成する工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜を耐酸化性マスクとして前記半導体基板を酸化することにより、前記第１の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域を互いに接触させ、前記第２の絶縁膜の両側の前記第２の溝の前記半導体基板を挟んで隣接する側壁それぞれに形成される酸化領域は互いに接触させない工程と、前記第１及び第２の絶縁膜及び前記側壁絶縁膜を除去する工程と、前記第１の絶縁膜の除去によって露出した前記半導体基板の半導体領域の表面にゲート絶縁膜を形成し、前記ゲート絶縁膜の上にゲート電極を形成することにより、前記半導体領域をライン状のフィンとするフィン型電界効果トランジスタを形成する工程と、前記第２の絶縁膜の除去によって露出した前記半導体基板の別の半導体領域にプレーナ型電界効果トランジスタ或いはプレーナ領域を形成する工程とを含む。

【0008】

この発明の第３の態様に係る半導体装置は、バルクシリコン基板の上に形成されたシリコン酸化膜と、前記シリコン酸化膜上に形成されたライン状のフィンと、前記フィンの延伸方向の両端にそれぞれ接続され、前記延伸方向と垂直な方向の幅が前記フィンよりも大きく、上面の高さが前記フィンの上面の高さと一致している前記基板の一部であるプレーナ領域とを具備する。

【発明の効果】

【0009】

本発明によれば、簡便かつ低コストにプレーナ領域と混載することが可能なフィン型電界効果トランジスタを含んだ半導体装置及びその製造方法を提供することができる。

【発明を実施するための最良の形態】

【0010】

以下、図面を参照して本発明の実施形態について詳細に説明する。

【0011】

図１は以下の実施形態に係るナノワイヤー（nano wire）-フィン型ＦＥＴの３次元構造を示した図である。幅１０nm以下のフィンの高さを低くしてアスペクト比（フィンの高さ／フィンの幅）を１程度に小さくしたＭＯＳ（Metal Oxide Semiconductor)ＦＥＴが、一般に、ナノワイヤー-フィン型ＦＥＴと呼ばれ、通常、フィン側面だけでなく上面もチャネル面として使用する。特に、チャネルとしてフィンの側面だけでなく、上面と底面も使うようにすると、ゲートオールアラウンド（Gate-all-around）ナノワイヤー-フィン型ＦＥＴと呼ばれる。

【0012】

ナノワイヤー-フィン型ＦＥＴのメリットとしては、（１）通常のフィン型ＦＥＴよりも短チャネル効果耐性があり、その分、微細化が可能であること、（２）量子閉じ込めによる有効質量と散乱確率の低減の結果、移動度が向上すること、（３）不純物ゆらぎ起因の閾値電圧バラツキが低減すること、等が挙げられる。

【0013】

（第１の実施形態）

本発明の第１の実施形態に係る半導体装置の製造方法を、各製造工程の断面図である図２乃至図１４を用いて以下に説明する。

【0014】

本実施形態においては、図１に示したようなナノワイヤー-フィン型ＦＥＴをプレーナ型ＭＯＳＦＥＴと同じ基板上に混載する。

【0015】

まず図２に示すように、バルクＳｉ基板１０の上に厚さ２nm程度の薄い酸化膜（図示せず）を介して、膜厚５０nm程度のＳｉＮからなるハードマスク材１５を堆積する。ハード

マスク材１５としては、SiO_2、あるいはＳｉＯＮ、更にはＳｉＮ／SiO_2／ＳｉＮ等の積層膜、その他の絶縁膜であってもかまわない。

【0016】

次に、図３に示すように、プレーナ型ＭＯＳＦＥＴ及びナノワイヤーフィン型ＦＥＴの活性（チャネル）領域をパターンニングして、それぞれに対するハードマスク１１及びハードマスク１２、１３を形成する。ここで、１０nm程度以下の幅のフィンを有するナノワイヤーフィン型ＦＥＴを形成するためのライン状のハードマスク１２、１３の線幅は、プレーナ型ＭＯＳＦＥＴを形成するためのハードマスク１１の線幅よりも小さくしておく。

【0017】

その後、ハードマスク１１、１２、１３をマスクとしてＲＩＥ（反応性イオンエッチング）加工を行なうことにより図４に示すように、２０nm程度の深さの第１の溝５０がバルクＳｉ基板１０に形成される。

【0018】

次に、図５に示すように、この上からＳｉＮ膜１４を全面に形成した後、図６に示すようにエッチバックすることにより第１の溝５０の側面に厚さ２０nm程度のＳｉＮの側壁絶縁膜１４を形成する。側壁絶縁膜１４としては、SiO_2、ＳｉＯＮ、或いはその他の絶縁膜を用いてもかまわない。

【0019】

次いで、図７に示すようにハードマスク１１、１２、１３と側壁絶縁膜１４をマスクとしてＳｉ基板１０をエッチングして第１の溝５０の底部をさらに深く掘って第２の溝６０を形成する。

【0020】

次に、図８に示すようにハードマスク１１、１２、１３と側壁絶縁膜１４を耐酸化性マスクとして第２の溝６０の底部に露出したＳｉ基板１０の表面を酸化して酸化膜１６を形成する。その際、ハードマスク１２、１３の下のフィンとなるべき領域の下においてその両側の第２の溝６０側壁からの酸化膜１６が互いに接触するように酸化膜厚を調整する。

【0021】

その結果フィン型ＦＥＴ領域のみ部分的に、酸化膜１６の上に半導体領域であるフィン領域１８、１９が残存する構造、即ちＳＯＩ(Silicon On Insulator)構造が形成される。他方、ハードマスク１１の下のチャネル幅が広くなるように形成したプレーナ型ＭＯＳＦＥＴ領域では、第２の溝６０の両側壁からの酸化膜が接触しないのでＳＯＩ構造とはならない。

【0022】

次に図９に示すように、ＨＤＰ(High Density Plasma：高密度プラズマ)などを用いてSiO_2系絶縁膜からなる素子分離絶縁膜(ＳＴＩ:shallow trench isolation)１７を全面に堆積し、更にＣＭＰ(Chemical Mechanical Polishing：化学的機械的研磨)平坦化を実行して、ＳｉＮハードマスク１１、１２、１３を露出させる。

【0023】

そしてさらに、図１０に示すように素子分離絶縁膜１７をエッチングすることにより、素子分離絶縁膜（ＳＴＩ）１７の表面高さをフィン領域１８、１９の表面高さに揃える。

【0024】

次いで、図１１に示すように、ＳｉＮハードマスク１１、１２、１３及びＳｉＮ側壁絶縁膜１４をホットリン酸などで除去することにより、フィン型ＦＥＴ領域においてはフィン１８、１９の上面および両側面が露出する。

【0025】

その後、図１２に示すように、水素（H_2）を含んだ雰囲気中において温度８００℃でアニールを行なうことにより、ナノワイヤーフィン１８、１９の断面形状を丸め、同時に、プレーナ型ＭＯＳＦＥＴのプレーナ領域２０の素子分離絶縁膜（ＳＴＩ）１７に隣接したエッジ部分の断面形状を丸める。

【0026】
ナノワイヤーフィン１８、１９の断面形状を丸めることにより、チャネル領域の表面がスムーズになりキャリアの散乱が減少して移動度が向上する。また、上記アニールは、窒素等を含んだ雰囲気中で実行されてもよい。
【0027】
次いで、図１３に示すように、ナノワイヤーフィン１８、１９の露出した表面（丸める前の上面及び両側面に相当）、及びプレーナ型ＭＯＳＦＥＴの活性領域２０の表面、それぞれに酸窒化膜（ＳｉＯＮ）からなるゲート絶縁膜２１、２２、２３を形成する。
【0028】
更に、その上に、ポリシリコン或いはメタル等のゲート電極材料を堆積し、図１４に示すように、リソグラフィとＲＩＥでゲート電極２４、２５を形成する。
【0029】
本実施形態においては、フィン型ＦＥＴ領域のゲート電極２４の高さと、プレーナ型ＭＯＳＦＥＴ領域のゲート電極２５の高さがほぼ同じになるので、ゲートのリソグラフィの焦点深度（ＤＯＦ：Depth Of Focus）にプロセス余裕が得られる。また、フィン型ＦＥＴとプレーナ型ＭＯＳＦＥＴのＲＩＥ加工を同時に行うことができる。さらにまた、ゲート表面が平坦なので、ゲートパターンの加工にサイドウォールパターントランスファー(Sidewall pattern transfer)プロセスを用いてもよい。
【0030】
本実施形態で製造されるフィン型ＦＥＴにおいては、フィンの上面及び両側面がチャネルになるため、Ωゲートフィン型ＦＥＴやトライゲート（Tri gate）フィン型ＦＥＴに類似している。
【0031】
その後、図１４のゲート電極２４の紙面垂直方向の両側面にスペーサを形成し、ソース／ドレインをイオン注入やシリサイド貼り付けによって形成する（図示せず）。ナノワイヤーフィン１８、１９のアスペクト比は小さい。従って、フィン１８、１９にソース／ドレイン拡散層を形成するためのドーピングは、通常の高アスペクト比のフィンとは異なり、基板に垂直な方向とのなす角度が０～７度となるイオン注入でよい。従って、高アスペクトのフィンに対して、チャネル幅方向（フィン高さ方向）に均一にドーピングするために必要となる斜めイオン注入技術やプラズマドーピング技術等の高価な技術が不要となるので、プロセスの低コスト化が図れる。
【0032】
その後の製造工程は通常のＬＳＩの製造工程と同様である。すなわち、層間絶縁膜を堆積し、コンタクトホールを形成し、上層配線（Ｃｕなど）をダマシンプロセス等を用いて形成する（図示せず）。
【0033】
本実施形態に係る半導体装置の製造方法においては、（１）フィン領域、プレーナ領域のゲートのリソグラフィ、ＲＩＥ加工を同時に処理可能であること、（２）バルクＳｉ基板上のフィン型ＦＥＴの製造においてフィンを出すために必要であった、フィン領域まわりの素子分離絶縁膜（ＳＴＩ）のリセスエッチングが不要になること、（３）フィン下部直下が酸化絶縁膜となっているので、フィン下部にパンチスルーストッパとして高濃度不純物層を形成することが不要になること、さらに（４）フィンとプレーナの作りわけのためのリソグラフィ等が不要となること、等から工程数を削減することが可能となる。
【0034】
また、基板として安価なバルクＳｉ基板を用いているにもかかわらず、ＳＯＩ構造のナノワイヤーフィン型ＦＥＴを形成できるので、高価なＳＯＩ基板を利用しないで済むので低コスト化が図れるというメリットがある。
【0035】
さらにまた、深い素子分離絶縁膜（ＳＴＩ）と直径の小さいナノワイヤーをバルク基板上で表面高さを揃えて形成することができる。両者の高さが揃っていると、その後の製造

プロセスが容易になるという長所がある。例えば、リソグラフィの焦点深度（ＤＯＦ）に対する要求を緩めることができるので、解像度を高めることができる。

【0036】

また、ゲート電極のＲＩＥ工程で、ゲート絶縁膜に対するオーバーエッチング量を低減できるので、その膜の信頼性を改善することができる。なぜなら、フィン領域（特にフィン両側面近傍）のゲートの厚さとプレーナ型ＭＯＳＦＥＴ領域のゲートの厚さの差が従来のフィン型ＦＥＴの場合よりも小さいので、フィン型ＦＥＴのゲートをＲＩＥ加工する際、プレーナ型ＭＯＳＦＥＴ領域のゲート絶縁膜がオーバーエッチングされる時間を短縮できるからである。

【0037】

以上説明したように、本実施形態によれば、ナノワイヤーフィン型ＦＥＴ、プレーナ型ＭＯＳＦＥＴデバイスを簡便なプロセスで、かつ低コストに混載させることが可能となる。

【0038】

（第２の実施形態）

本発明の第２の実施形態に係る半導体装置の製造方法を、各製造工程の断面図である図１５乃至図２１を用いて以下に説明する。

【0039】

本実施形態においても、ナノワイヤーフィン型ＦＥＴをプレーナ型ＭＯＳＦＥＴと同じ基板上に混載するが、ナノワイヤーフィン型ＦＥＴのゲート形成にダマシンプロセスを用い、フィンの周り全体をチャネルとするゲートオールアラウンドタイプにするところが第１の実施形態とは異なっている。

【0040】

本実施形態においても図１２までの工程は、第１の実施形態と同様であるので説明を省略する。その後、図１５に示すように、ナノワイヤーフィン１８、１９の露出した表面（丸める前の上面及び両側面に相当）の活性領域表面、及びプレーナ領域２０の表面にSiO_2からなるダミーゲート絶縁膜２６、２７、及び６２を形成する。

【0041】

更に、その上にポリシリコン等のダミーゲート電極材料を堆積し、図１６に示すように、リソグラフィとＲＩＥでダミーゲート電極パターン２８及び６３を形成する。このダミーゲート２８及び６３は後の工程で除去するものであり、ゲート形成をダマシンプロセスで実行するために必要となる。

【0042】

その後、図１６のダミーゲート２８及び６３の紙面垂直方向の両側面にスペーサを形成し、ソース／ドレインをイオン注入やシリサイド貼り付けによって形成する（図示せず）。本実施形態においても、アスペクト比が小さいフィン１８、１９にソース／ドレイン拡散層を形成するためのドーピングは、基板に垂直な方向とのなす角度が０～７度となるイオン注入でよく、プロセスの低コスト化が図れる。

【0043】

次に、図１７に示すようにダミーゲート２８及び６３を含んだ全面に、ＴＥＯＳを用いてＳｉＯ２膜（以下、ＴＥＯＳ膜）２９を厚さ３００nm程度堆積し、図１８に示すようにＣＭＰで平坦化して、ダミーゲート２８及び６３のトップを露出させる。

【0044】

次いで、図１９に示すようにダミーゲート２８及び６３をＣＤＥ（ケミカル・ドライ・エッチング）などでエッチング除去する。更に、ＨＦ（フッ酸）薬液でエッチングすると、図２０に示すように、チャネル領域のＳｉ-ナノワイヤー１８、１９の底部にもエッチングが進み、中空構造が形成される。即ち、ナノワイヤー１８、１９が橋のように空中に浮く構造となる。図２０の状態を鳥瞰図で示すと図２１のようになる。

【0045】

ただし、図２０の紙面垂直方向の手前と奥側に存在するソース・ドレイン領域がナノワ

イヤー１８、１９を支えているので、ナノワイヤー１８、１９がリフトオフする心配はない。この様子を、図２１の点線に沿った断面図である図２２に示す。

【0046】

そして、図２３に示すように、ナノワイヤー１８、１９の表面全面（フィンの上面、側面、底面）、及びプレーナ領域２０の表面に酸窒化膜（ＳｉＯＮ）ゲート絶縁膜３０、３１、及び６４を形成し、さらにその上から例えばメタル材料であるゲート電極材料３２及び６５を堆積する。最後に、ＣＭＰ平坦化して不要部分のゲート電極材料を除去する。

【0047】

このゲート電極３２及び６５はピュアメタルでも良いしメタルシリサイドでも良い。また、ＦＵＳＩ(fully silicided：完全にシリサイド化した)ゲート電極にしても良い。すなわち、ゲート溝形成後、ゲート絶縁膜を形成し、全面にポリシリコン（Poly-Si）を堆積してＣＭＰを行ない、溝内にポリシリコンを埋め込んだ後、Ｎｉなどをスパッタしてポリシリコン全体をシリサイド化させても良い。

【0048】

本実施形態の場合、ナノワイヤーフィン１８、１９の周り全体がチャネルになるため、ゲートオールアラウンドフィン型ＦＥＴを形成することができる。

【0049】

その後の製造工程は通常のＬＳＩの製造工程と同様である。すなわち、層間絶縁膜を堆積し、コンタクトホールを形成し、上層配線（Ｃｕなど）をダマシンプロセス等を用いて形成する（図示せず）。

【0050】

本実施形態に係る半導体装置の製造方法においても、第１の実施形態と同様の理由によって、工程数を削減することが可能となる。また同様に、安価なバルクＳｉ基板にＳＯＩ構造のナノワイヤーフィン型ＦＥＴを形成できるので、高価なＳＯＩ基板を利用しないで済むので低コスト化が図れる。

【0051】

さらにまた、深い素子分離絶縁膜（ＳＴＩ）と直径の小さいナノワイヤーをバルク基板上で表面高さを揃えて形成することができるので、その後の製造プロセスが容易になる。例えば、リソグラフィの焦点深度（ＤＯＦ）に対する要求を緩めることができるので、解像度を高めることができる。また、ゲート電極のＲＩＥ工程で、ゲート絶縁膜に対するオーバーエッチング量を低減できるので、その膜の信頼性を改善することができる。

【0052】

さらにまた、ナノワイヤーフィンの周り全体がチャネルになるため、ゲートオールアラウンドフィン型ＦＥＴを形成することができ、トランジスタの微細化、高性能化を押し進めることができる。

【0053】

以上説明したように、本実施形態によれば、ナノワイヤーフィン型ＦＥＴ、プレーナ型ＭＯＳＦＥＴデバイスを簡便なプロセスで、かつ低コストに混載させることが可能となる。

【0054】

上記実施形態においては、ナノワイヤーフィン型ＦＥＴのゲート形成にダマシンプロセスを適用しつつ、ナノワイヤーフィン型ＦＥＴをプレーナ型ＭＯＳＦＥＴと同じ基板上に混載する際の製造コストを削減している。したがって、以下のような変形例も挙げられる。

【0055】

まず、第１の変形例を、図２４乃至図２８を用いて説明する。第１の変形例は、図１８までの工程は上記実施形態と同じである。そのあと、ポリシリコン等からなるダミーゲート２８及び６３にドーパントをイオン注入し、その後、活性化アニールを行う（図示せず）。

【0056】

さらに、図２４に示すように、ポリシリコンプレーナ領域をレジスト６６で覆い、ダミーゲート２８をＣＤＥ（ケミカル・ドライ・エッチング）などでエッチング除去することによりフィン領域を開口する。その後、レジスト６６を剥離して、ＨＦ（フッ酸）薬液でエッチングすると、図２５に示すように、チャネル領域のＳｉ-ナノワイヤー１８、１９の底部にもエッチングが進み、中空構造が形成される。図２５の状態を鳥瞰図で示すと図２６のようになる。

【0057】

そして、図２７に示すように、ナノワイヤー１８、１９の表面全面（フィンの上面、側面、底面）に酸窒化膜（ＳｉＯＮ）ゲート絶縁膜３０、３１を形成し、さらにその上から例えばメタル材料であるゲート電極材料３２を堆積する。最後に、ＣＭＰ平坦化して不要部分のゲート電極材料３２を除去すると、図２８に示すように、プレーナ領域がポリシリコン電極６３で、フィン領域がメタル電極３２となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

【0058】

次に、第２の変形例を、図２９乃至図３０を用いて説明する。第２の変形例も、図２８までの工程は第１の変形例と同じで、プレーナ領域がポリシリコン電極で、フィン領域がメタル電極のＦＥＴある。ただし、図１８において第１の変形例で行ったポリシリコン等からなるダミーゲート２８及び６３へのドーピングは行わなくとも良い。

【0059】

まず、図２８の状態で、図２９に示すようにＮｉ７０をスパッタし、その後、アニールする。次に、図３０に示すように、硫酸と過酸化水素水の混合溶液で余剰のＮｉ７０を剥離する。ポリシリコン領域６３は上記アニールによってＮｉシリサイド７１になっている。この時のアニール温度は３００℃～６００℃程度が望ましく、典型的には５００℃である。

【0060】

このとき、作り易さの点から、フィン領域のメタル電極３２は５００℃のアニールでＮｉ７０と反応しにくい材料が望ましい。また、仕事関数制御の点から、シリサイド時のアニール温度でＮｉと反応しうる材料を用いる際には、アニール温度でＮｉと反応しにくい材料をキャップ膜として、２層構造にすることが望ましい。Ｎｉと反応しにくい材料としては、例えば、ＴｉＮ、ＴａＮ、ＷＮ、ＡｌＮ、ＨｆＣ、ＨｆＢ、ＴａＣ及びこれらの混合物などが挙げられる。

【0061】

さらに、熱的安定性の向上、仕事関数の調整のため、Ｃ、Ｃｒ、Ｆｅ、Ｇｅ、Ｂ、Ｐ、Ａｓ、Ｓｎ、Ｇａ、Ｉｎ、Ｐ，Ｓｂ、Ｓ、Ｃｌ、Ｆなどを添加しても良い。Ｎｉと反応しうる材料としては、例えば、Ｃｏ、Ｎｉ、Ｐｔ、Ｔｉ、Ｈｆ、Ｚｒ、Ｔａ、Ｗ、Ｍｏ、Ａｌ及びこれらの合金、これらの材料とＳｉとの混合物が挙げられる。仕事関数の調整のため、上述の同様の添加剤を混ぜても良い。

【0062】

本変形例によると、図３０に示すように、プレーナ領域がＮｉシリサイド電極７１で、フィン領域がメタル電極３２となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

【0063】

さらに、第３の変形例を図３１乃至図３３を用いて説明する。第３の変形例も、図２８までの工程は第１の変形例と同じで、プレーナ領域がポリシリコン電極で、フィン領域がメタル電極のＦＥＴである。ただし、図１８において第１の変形例で行ったポリシリコン等からなるダミーゲート２８及び６３へのドーピングは行わなくとも良い。

【0064】

まず、図２８の状態で、図３１に示すようにＣＤＥなどでプレーナ領域のポリシリコン６３を剥離する。次に、図３２に示すように、プレーナ用のメタル電極３３を成膜する。メタル電極３３の材料は、フィン領域のゲート電極材料に用いるメタル材料として挙げた

ものから選択することができ、フィン領域と同じでも、異なっても構わない。

【0065】

さらに、図３３に示すようにＣＭＰで平坦化する。その結果、プレーナ領域、フィン領域がともにメタル電極となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

【0066】

さらに、第４の変形例を、図３４乃至４２を用いて説明する。第４の変形例は、図１５でダミーゲート絶縁膜２６、２７、及び６２を形成するところまでは、本（第２の）実施形態と同様である。

【0067】

その後、図３４に示すようにフィン領域のダミーゲートポリシリコン２８を加工形成し、図３５に示すように、ＴＥＯＳ膜２９を成膜する。さらに、図３６に示すように、ＣＭＰで平坦化する。次いで、図３７に示すようにフィン領域のダミーゲート２８をＣＤＥで剥離し、さらに、図３８に示すように、ＨＦ薬液でエッチングする。

【0068】

その後、ナノワイヤー１８、１９の表面全面に酸窒化膜（ＳｉＯＮ）ゲート絶縁膜３０、３１を形成し、メタル材料３２を成膜して、ＣＭＰで平坦化すると同時に、プレーナ領域の余剰メタルを剥離することにより、図３９の構造を得る。

【0069】

次いで、図４０に示すように、プレーナ領域のゲート形状にＴＥＯＳ膜２９に溝７５を形成する。溝７５は、リソグラフィ法を用いて、プレーナ領域上にゲート形状にレジスト（図示せず）を開口し、ＲＩＥでＴＥＯＳ膜２９をエッチングすることで得られる。ＲＩＥだけでなく、ＨＦによるエッチングと組み合わせても良い。

【0070】

次いで、図４１に示すように、ゲート絶縁膜７６とメタル電極４２を成膜する。最後に、図４２に示すように、ＣＭＰで平坦化すると同時に、フィン領域の余剰メタルを剥離する。その結果、プレーナ領域、フィン領域がともにメタル電極４２、３２となる。その後の製造工程は通常のＬＳＩの製造工程と同様である。

【0071】

以上説明したように、本実施形態の変形例によっても、ナノワイヤーフィン型ＦＥＴ、プレーナ型ＭＯＳＦＥＴデバイスを簡便なプロセスで、かつ低コストに混載させることが可能となる。

【0072】

（第３の実施形態）

本発明の第３の実施形態に係る半導体装置の製造方法を、図４３乃至図５７を用いて以下に説明する。

【0073】

本実施形態においては、図１に示したようなナノワイヤーフィン型ＦＥＴのフィンの両端にプレーナ領域を同時形成する。

【0074】

本実施形態においても、第１の実施形態の図２乃至図１１までの工程と基本的に同様な工程が実行される。しかし、本実施形態においては図３とは異なって、図４３の上面図に示すような、ナノワイヤーフィンの両端に当該フィンより横幅の広いプレーナ領域が接続された形状であるハードマスク３５をバルクＳｉ基板１０の上に形成する。

【0075】

ここで、ハードマスク３５は例えば、膜厚５０nm程度のＳｉＮ膜であるが、SiO_2、あるいはＳｉＯＮ、更にはＳｉＮ／SiO_2／ＳｉＮ等の積層膜、その他の絶縁膜であってもかまわない。図４３のＢ－Ｂ’線に沿った断面図及びＡ－Ａ’線に沿った断面図を図４４に示す。

【0076】

その後、第１の実施形態の図４乃至図１１までの工程と同様に、図４３のＢ－Ｂ’線に沿った断面（プレーナ領域）及びＡ－Ａ’線に沿った断面（フィン領域）で見た図４５乃至図５２に示される工程が実行される。

【0077】

まず、ハードマスク３５をマスクとしてＲＩＥ加工を行なうことにより図４５に示すように、２０nm程度の深さの溝がバルクＳｉ基板１０に形成される。ここでは、図４５（a）、(b)共に両側の溝の途中までしか示していない。図４５（a）、(b)は、例えば、図４３で示したハードマスク３５が複数並列しており、そのため図４５（a）、(b)の左右にそれと同様な構造が並列していて、その一部の断面を示しているとしてもよい。以下も同様とする。

【0078】

次に、図４６に示すように、この上からＳｉＮ膜１４を全面に形成した後、図４７に示すようにエッチバックすることにより溝の側面に厚さ２０nm程度のＳｉＮの側壁絶縁膜１４を形成する。側壁絶縁膜１４としては、SiO_2、ＳｉＯＮ、或いはその他の絶縁膜を用いてもかまわない。

【0079】

次いで、図４８に示すようにハードマスク３５と側壁絶縁膜１４をマスクとしてＳｉ基板１０をエッチングして溝をさらに深く掘る。

【0080】

次に、図４９に示すようにハードマスク３５と側壁絶縁膜１４を耐酸化性マスクとして溝底部に露出したＳｉ基板１０の表面を酸化して酸化膜１６を形成する。その際、フィン型ＦＥＴ領域においてシリコンフィン底部の両側面からの酸化膜１６が互いに接するように酸化膜厚を調整する。

【0081】

その結果フィン型ＦＥＴ領域のみ部分的に、酸化膜１６の上に半導体領域であるフィン領域１８が残存する構造、即ちＳＯＩ構造が形成される。他方、幅が広くなるように形成したプレーナ領域では、両側壁からの酸化膜が接しないのでＳＯＩ構造とはならない。

【0082】

次に図５０に示すように、ＨＤＰ(High Density Plasma：高密度プラズマ)などを用いてSiO_2系絶縁膜からなる素子分離絶縁膜（ＳＴＩ）１７を全面に堆積し、更にＣＭＰ(Chemical Mechanical Polishing：化学的機械的研磨)平坦化を実行して、ＳｉＮハードマスク３５を露出させる。そしてさらに、図５１に示すように素子分離絶縁膜（ＳＴＩ）１７をエッチングする。

【0083】

次いで、図５２に示すように、ＳｉＮハードマスク３５及びＳｉＮ側壁絶縁膜１４をホットリン酸などで除去することにより、フィン型ＦＥＴ領域においてはフィン１８の上面および両側面が露出する。

【0084】

以上のように本実施形態においても、フィン型ＦＥＴとプレーナ領域のＲＩＥ加工を同時に行なうことができる。

【0085】

図５３は、図５２のＩＩ程まで進んだ時の、図５２（ａ）及び（ｂ）に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図である。ナノワイヤーフィン１８の両端には、フィン１８より横幅が大きいプレーナ領域２０がそれぞれ接続されている。

【0086】

この後、Ａ－Ａ’線に沿った断面図である図５４に示すようにナノワイヤーフィン１８の上面及び両側面に、例えば、酸窒化膜（ＳｉＯＮ）等からなるゲート絶縁膜３６を形成する。

【0087】

更にその上に、ポリシリコン或いはメタル等のゲート電極材料を堆積し、図５５に示すように、リソグラフィとＲＩＥでゲート電極３７を形成する。図５６は、図５５に示したＣ－Ｃ' 線に沿って切り出した半導体装置の３次元構造を示した斜視図である。

【0088】

その後、図５５のゲート電極３７の紙面垂直方向の両側面にスペーサを形成し、ソース／ドレインをイオン注入やシリサイド貼り付けによって形成する（図示せず）。ナノワイヤーフィン型ＦＥＴのフィン１８のアスペクト比は小さいので、ソース／ドレイン拡散層を形成するためのドーピングは、基板に垂直な方向とのなす角度が０～７度となるイオン注入でよい。従って、斜めイオン注入技術やプラズマドーピング技術等の高価な技術が不要となるので、プロセスの低コスト化が図れる。

【0089】

本実施形態で製造されるフィン型ＦＥＴは、フィンの上面及び両側面がチャネルになるため、トライゲート（Tri gate）フィン型ＦＥＴとなっている。

【0090】

その後、図５７に示すように、層間絶縁膜を堆積し（図示せず）、上層配線（Ｃｕなど）と接続するためのコンタクト３８を形成する。ここで、プレーナ領域２０の横幅がナノワイヤーフィン１８の横幅より大きくなるように形成されているため、コンタクト３８とソース／ドレイン領域４０との界面抵抗を小さくすることができる。

【0091】

また、コンタクトの位置合わせにずれが生じてコンタクト３９のように形成されたとしても、プレーナ領域２０との接触が維持され、合わせずれに強い構造となっている。

【0092】

以上述べたように、フィン型ＦＥＴとプレーナ領域を同時形成する本実施形態によって、第１及び第２の実施形態と同様な工程の削減と低コスト化が図れると同時に、コンタクトとの界面抵抗が小さく、合わせずれに強いナノワイヤーフィン型ＦＥＴを備えた半導体装置の製造が可能となる。

【0093】

なお、本願発明は上記実施形態に限定されるものではなく、実施段階ではその要旨を逸脱しない範囲で種々に変形することが可能である。更に、上記実施形態には種々の段階の発明が含まれており、開示される複数の構成要件における適宜な組み合わせにより種々の発明が抽出されうる。例えば、実施形態に示される全構成要件からいくつかの構成要件が削除されても、発明が解決しようとする課題の欄で述べた課題が解決でき、発明の効果の欄で述べられている効果が得られる場合には、この構成要件が削除された構成が発明として抽出されうる。

【図面の簡単な説明】

【0094】

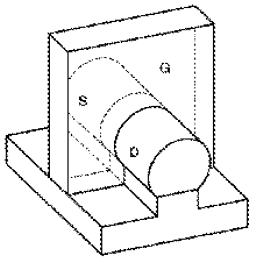
【図1】本発明の実施形態に係るナノワイヤーフィン型ＦＥＴの３次元構造を示した図。
【図2】本発明の第１の実施形態に係る半導体装置の製造方法の一工程を示す断面図。
【図3】図２に続く半導体装置の製造方法の一工程を示す断面図。
【図4】図３に続く半導体装置の製造方法の一工程を示す断面図。
【図5】図４に続く半導体装置の製造方法の一工程を示す断面図。
【図6】図５に続く半導体装置の製造方法の一工程を示す断面図。
【図7】図６に続く半導体装置の製造方法の一工程を示す断面図。
【図8】図７に続く半導体装置の製造方法の一工程を示す断面図。
【図9】図８に続く半導体装置の製造方法の一工程を示す断面図。
【図10】図９に続く半導体装置の製造方法の一工程を示す断面図
【図11】図１０に続く半導体装置の製造方法の一工程を示す断面図。
【図12】図１１に続く半導体装置の製造方法の一工程を示す断面図。
【図13】図１２に続く半導体装置の製造方法の一工程を示す断面図。
【図14】図１３に続く半導体装置の製造方法の一工程を示す断面図。

【図15】本発明の第２の実施形態に係る半導体装置の製造方法の一工程を示す断面図。
【図16】図１５に続く半導体装置の製造方法の一工程を示す断面図。
【図17】図１６に続く半導体装置の製造方法の一工程を示す断面図。
【図18】図１７に続く半導体装置の製造方法の一工程を示す断面図。
【図19】図１８に続く半導体装置の製造方法の一工程を示す断面図。
【図20】図１９に続く半導体装置の製造方法の一工程を示す断面図。
【図21】図２０の状態を鳥瞰図で示した図。
【図22】図２１の点線に沿った断面図。
【図23】図２０に続く半導体装置の製造方法の一工程を示す断面図。
【図24】本発明の第２の実施形態の第１の変形例に係る半導体装置の製造方法の一工程を示す断面図。
【図25】図２４に続く半導体装置の製造方法の一工程を示す断面図。
【図26】図２５の状態を鳥瞰図で示した図。
【図27】図２６に続く半導体装置の製造方法の一工程を示す断面図。
【図28】図２７に続く半導体装置の製造方法の一工程を示す断面図。
【図29】本発明の第２の実施形態の第２の変形例に係る半導体装置の製造方法の一工程を示す断面図。
【図30】図２９に続く半導体装置の製造方法の一工程を示す断面図。
【図31】本発明の第２の実施形態の第３の変形例に係る半導体装置の製造方法の一工程を示す断面図。
【図32】図３１に続く半導体装置の製造方法の一工程を示す断面図。
【図33】図３２に続く半導体装置の製造方法の一工程を示す断面図。
【図34】本発明の第２の実施形態の第４の変形例に係る半導体装置の製造方法の一工程を示す断面図。
【図35】図３４に続く半導体装置の製造方法の一工程を示す断面図。
【図36】図３５に続く半導体装置の製造方法の一工程を示す断面図。
【図37】図３６に続く半導体装置の製造方法の一工程を示す断面図。
【図38】図３７に続く半導体装置の製造方法の一工程を示す断面図。
【図39】図３８に続く半導体装置の製造方法の一工程を示す断面図。
【図40】図３９に続く半導体装置の製造方法の一工程を示す断面図。
【図41】図４０に続く半導体装置の製造方法の一工程を示す断面図。
【図42】図４１に続く半導体装置の製造方法の一工程を示す断面図。
【図43】本発明の第３の実施形態に係る半導体装置の製造方法の一工程を示す上面図。
【図44】（ａ）は図４３のＢ－Ｂ’線に沿った断面図、（ｂ）は図４３のＡ－Ａ’線に沿った断面図。
【図45】（ａ）は図４４に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図46】（ａ）は図４５に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図47】（ａ）は図４６に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図48】（ａ）は図４７に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図49】（ａ）は図４８に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図50】（ａ）は図４９に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図51】（ａ）は図５０に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図52】（ａ）は図５１に続く半導体装置の製造方法の一工程を示すＢ－Ｂ’線に沿った

断面図、（ｂ）はＡ－Ａ’線に沿った断面図。
【図53】図５２（ａ）及び（ｂ）に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図。
【図54】図５２に続く半導体装置の製造方法の一工程を示すＡ－Ａ’線に沿った断面図。
【図55】図５４に続く半導体装置の製造方法の一工程を示すＡ－Ａ’線に沿った断面図。
【図56】図５５に示したＣ－Ｃ’線に沿って切り出した半導体装置の３次元構造を示した斜視図。
【図57】図５６で示した半導体装置にコンタクトを形成したときの３次元構造を示した斜視図。
【符号の説明】
【0095】
１０…バルクＳｉ基板、１１、１２、１３、３５…ハードマスク、１４…側壁絶縁膜、
１５…ＳｉＮハードマスク材、１６…酸化膜、１７…素子分離絶縁膜（ＳＴＩ）、
１８、１９…ナノワイヤーフィン、２０…プレーナ領域、
２１、２２、２３、３６、７６…ゲート絶縁膜、
２４、２５、３２、３３、３７、４２、６５…ゲート電極、
２６、２７、６２…ダミーゲート絶縁膜、２８、６３…ダミーゲート、２９…ＴＥＯＳ膜
３０、３１、６４…酸窒化膜ゲート絶縁膜、３８、３９…コンタクト、
４０…ドレイン領域、５０…第１の溝、６０…第２の溝、６６…レジスト、
７０…Ｎｉ、７１…Ｎｉシリサイド、７５…溝、メタル電極。

【図1】

図1



ナノワイヤー・フィン型FET

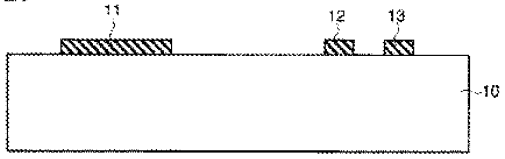
【図2】

図2



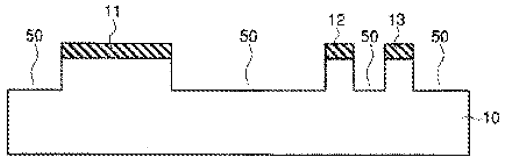
【図3】

図3



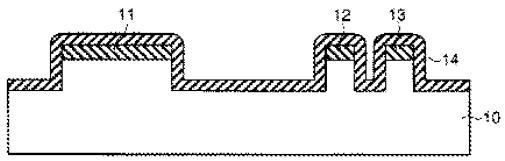
【図4】

図4



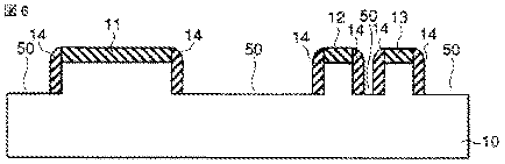
【図5】

図5



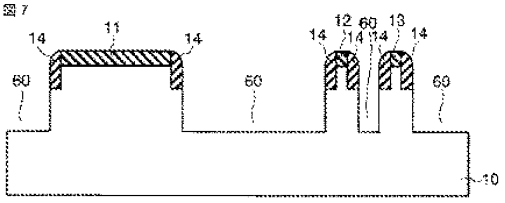
【図6】

図６



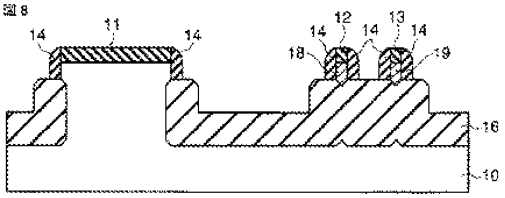
【図7】

図７



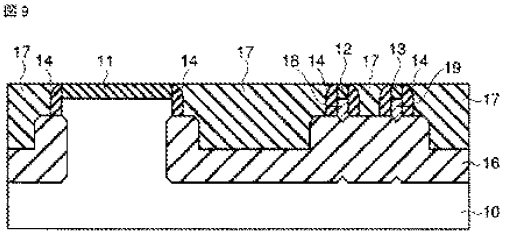
【図8】

図８



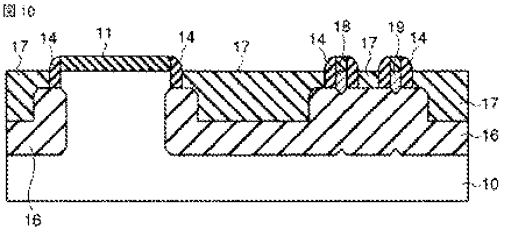
【図9】

図９



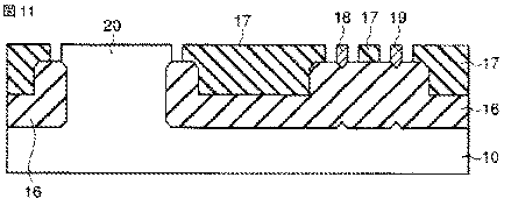
【図10】

図１０



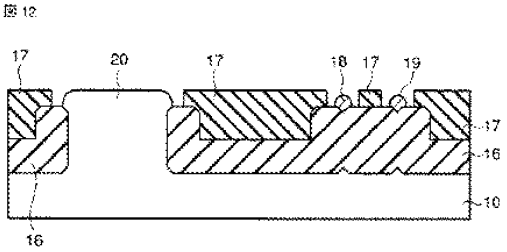
【図11】

図１１

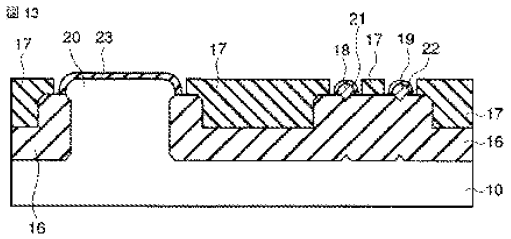


【図12】

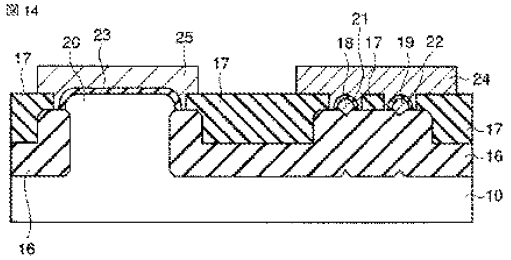
図１２



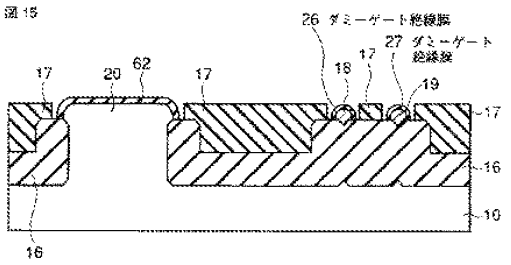
【図13】



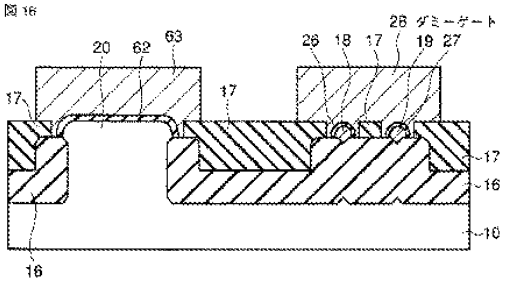
【図14】



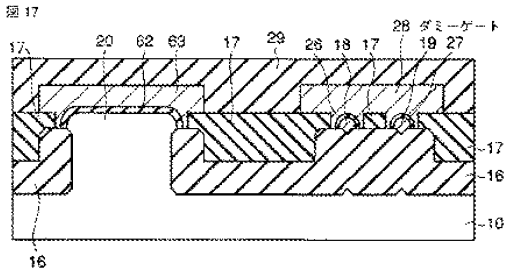
【図15】



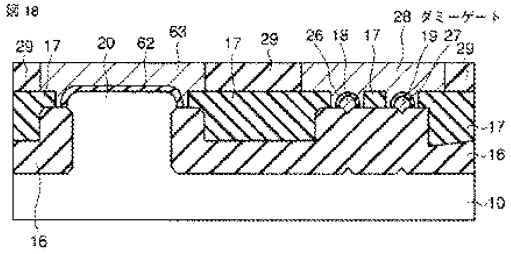
【図16】



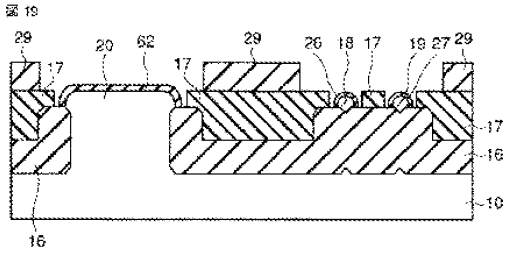
【図17】



【図18】

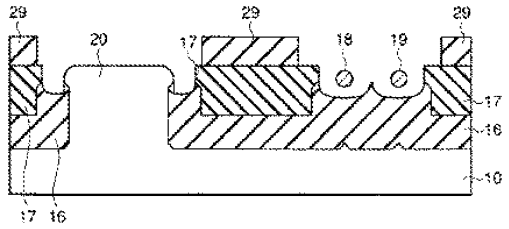


【図19】



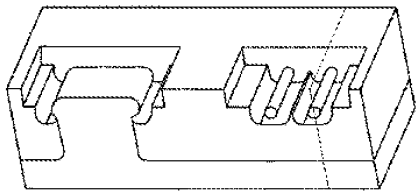
【図20】

図20



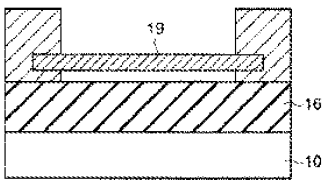
【図21】

図21



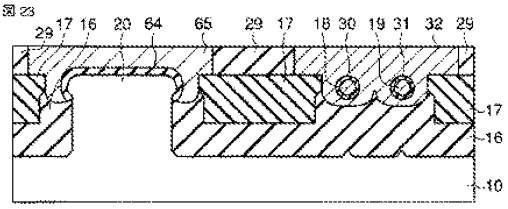
【図22】

図22



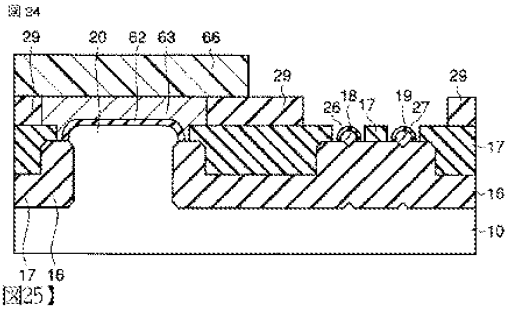
【図23】

図23



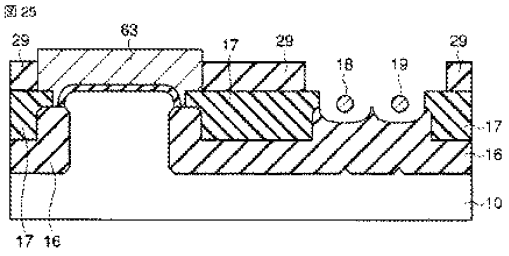
【図24】

図24



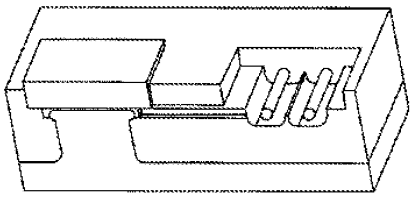
【図25】

図25

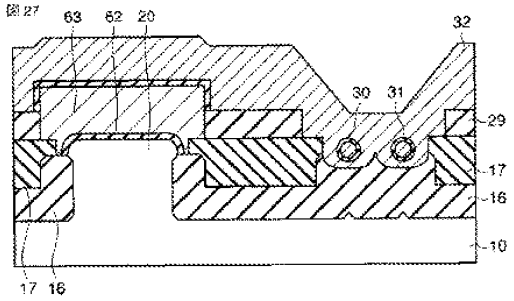


【図26】

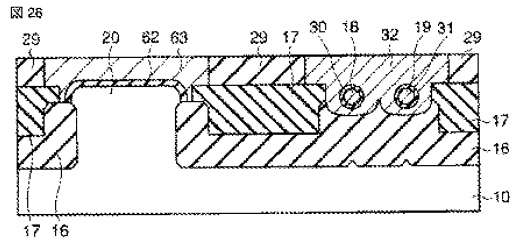
図26



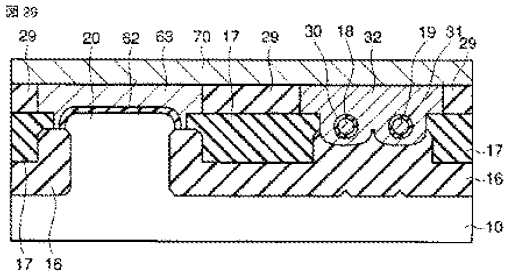
【図27】



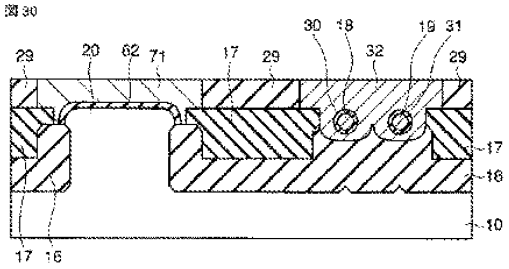
【図28】



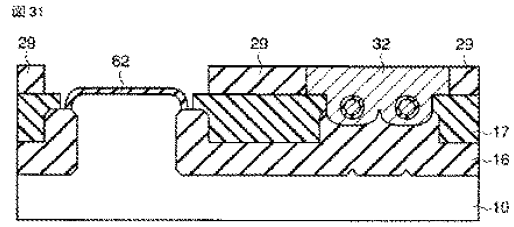
【図29】



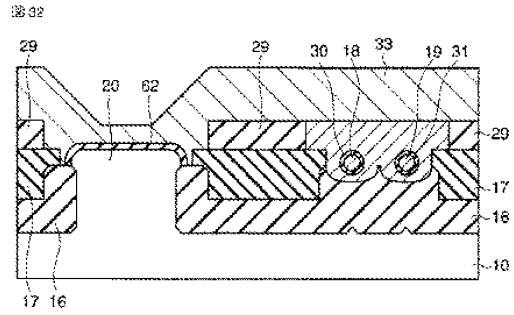
【図30】



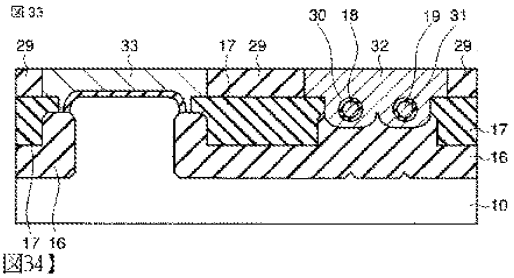
【図31】



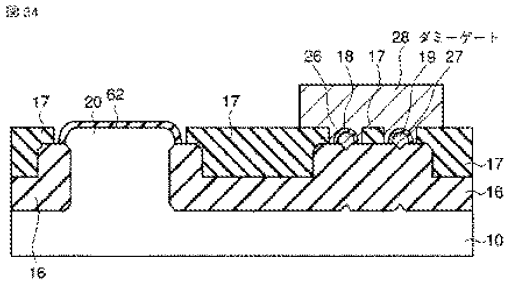
【図32】



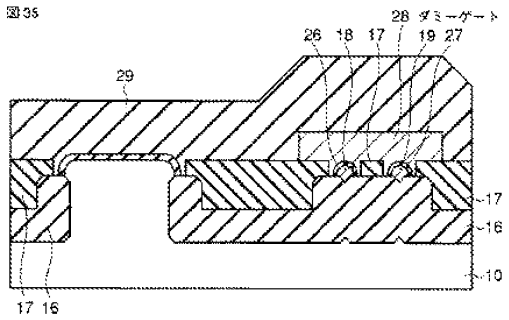
【図33】



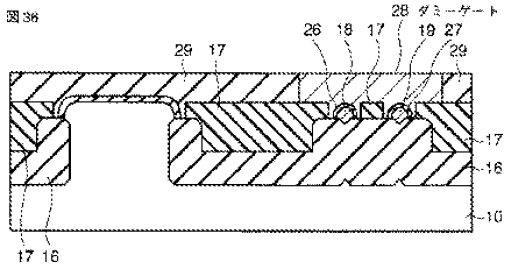
【図34】



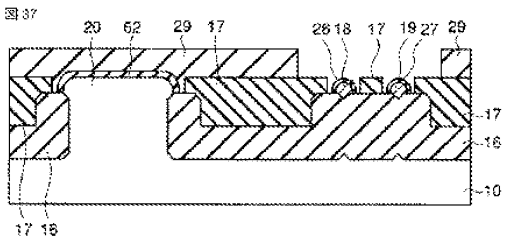
【図35】



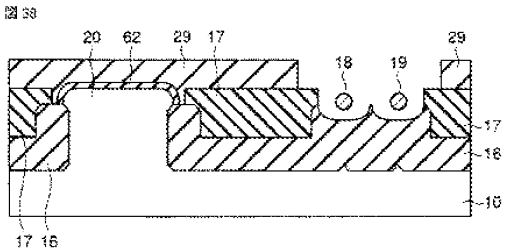
【図36】



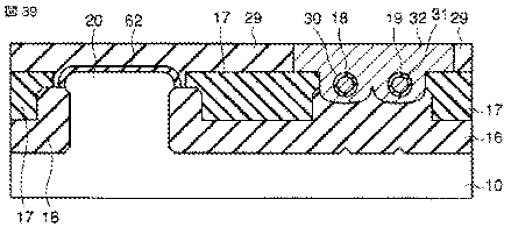
【図37】



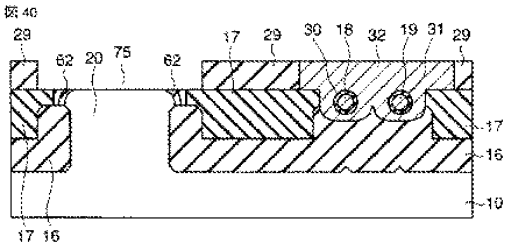
【図38】



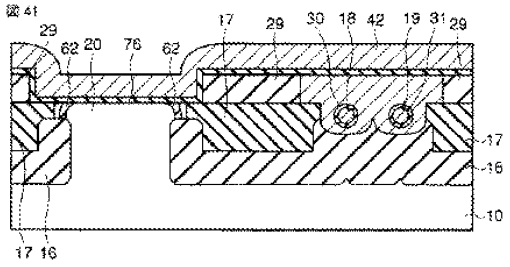
【図39】



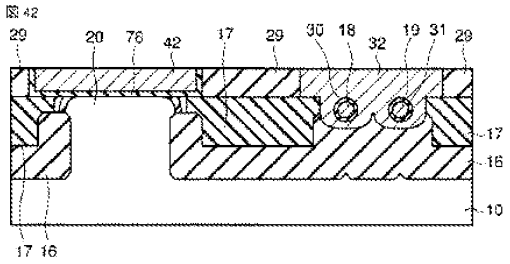
【図40】



【図41】

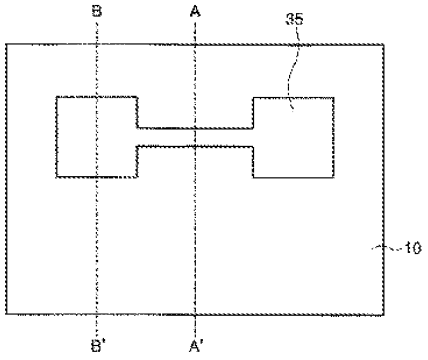


【図42】



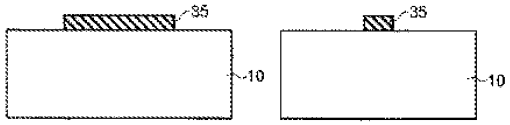
【図43】

図43



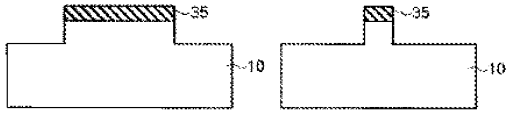
【図44】

図44　B-B'断面図　A-A'断面図



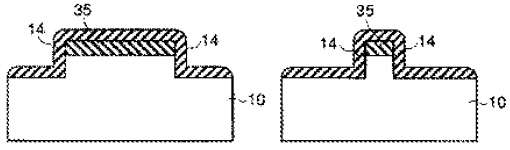
【図45】

図45　B-B'断面図　A-A'断面図



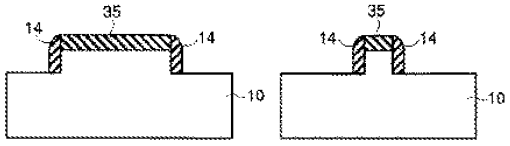
【図46】

図46　B-B'断面図　A-A'断面図



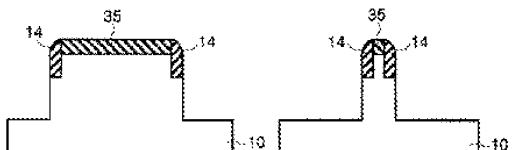
【図47】

図47　B-B'断面図　A-A'断面図



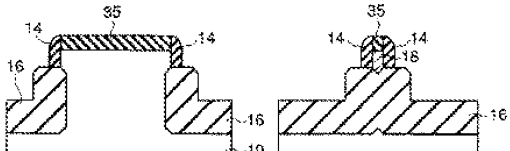
【図48】

図48　B-B'断面図　A-A'断面図

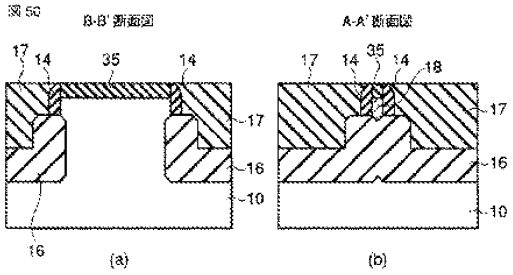


【図49】

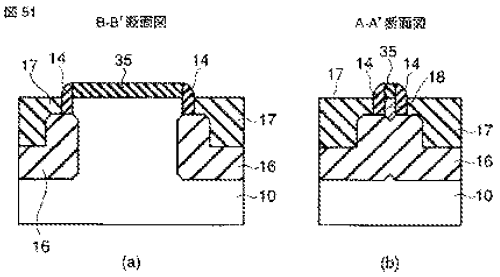
図49　B-B'断面図　A-A'断面図



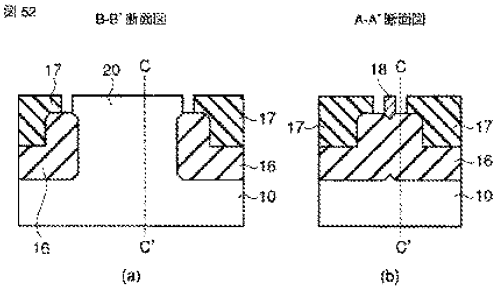
【図50】



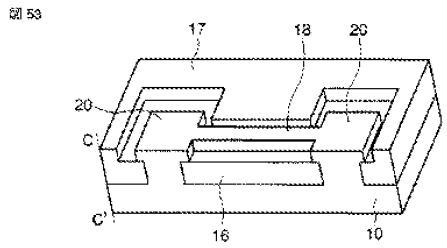
【図51】



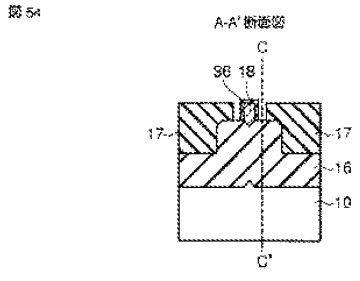
【図52】



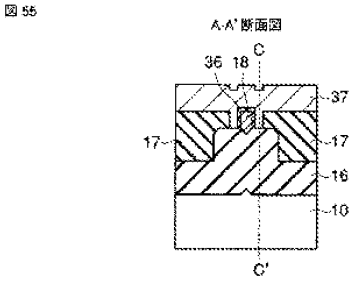
【図53】



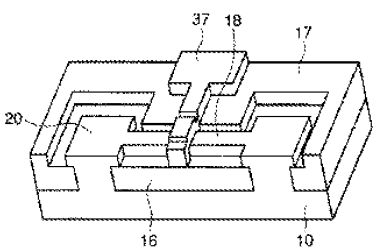
【図54】



【図55】

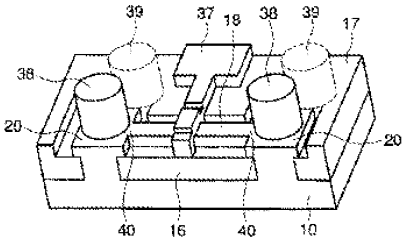


【図56】



【図57】

図57



(51)Int.Cl.			FI			テーマコード（参考）
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			Ｈ０１Ｌ	27/08	３３１Ｅ	
			Ｈ０１Ｌ	27/08	１０２Ｂ	
			Ｈ０１Ｌ	21/90	Ｃ	
			Ｈ０１Ｌ	21/28	Ｌ	
			Ｈ０１Ｌ	29/78	３０１Ｘ	

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Ｆターム(参考)　4M104 AA09 BB01 DD03 GG09 GG10 GG14
5F032 AA08 AA15 AA33 AA36 AA44 AA45 AA77 BA05 BA06 BB01
CA17 DA04 DA23 DA24 DA30 DA33 DA53 DA74
5F033 HH04 HH07 VV06
5F048 AA04 AA07 AA09 AC01 BA01 BA09 BA16 BA20 BB01 BB05
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BF11 BG13 DA25
5F110 AA01 AA04 AA16 CC01 CC02 DD05 DD13 DD21 DD24 EE01
EE02 EE05 EE06 EE09 EE14 EE22 EE30 EE31 EE41 EE42
EE44 EE47 EE48 FF04 GG02 GG12 GG22 GG58 HJ13 HK05
HK32 HL02 HM04 NN02 NN33 NN65 NN66 NN74 QQ19
5F140 AA01 AA21 AA39 AA40 AB01 AC36 BA01 BB05 BD09 BF01
BF04 BF05 BF42 BF44 BG08 BH02 BH08 BH45 BJ01 BJ05
BJ08 BJ23 BK13 BK25 CA03 CB01 CB04 CE07 CE20

Electronic Patent Application Fee Transmittal

Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask/Sheri Villarreal
Attorney Docket Number:	P60397US-C1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
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Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1
Receipt Date:	18-JAN-2019
Filing Date:	20-OCT-2017
Time Stamp:	19:21:07
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Deposit Account	500393
Authorized User	Sheri Villarreal
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US-C1_IDS_01_18_19.pdf	359972 e011b3a65bbf2ef57e2a5380c21a06a7cf43ad64	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Foreign Reference	JP2005136376_w_English_translation.pdf	15904229 0a237d5c753221411fd688941a1749231041b523a	no	43
Warnings:					
Information:					
3	Foreign Reference	JP2008172082_w_English_translation.pdf	21954262 b0539e583a1171b783b1b0f95fe9866a0a899f11	no	67
Warnings:					
Information:					
4	Non Patent Literature	P60397EP_OA_07_11_17.pdf	209694 6bc0907683458157086bc6129934178ba9450091	no	2
Warnings:					
Information:					
5	Non Patent Literature	P60397JP_NOA_03_13_18.pdf	254790 5526a3fcf597c8ed697fb52221f329889534 7e86	no	1
Warnings:					
Information:					

6	Non Patent Literature	P60397TW_NOA_09_19_16.pdf	538596 2012bcddcfe90f30a3a5ae87a71876f601a03157	no	2
Warnings:					
Information:					
7	Non Patent Literature	P60397TW_OA_05_17_16.pdf	821602 7943b1ad543de505c0e398f149775073c06a2239	no	4
Warnings:					
Information:					
8	Non Patent Literature	P60397TW-D_NOA_05_19_17.pdf	772161 9be147e7a8acf65e6b3a6743e8f347e3074f8f60	no	3
Warnings:					
Information:					
9	Non Patent Literature	P60397TW-D2_NOA_03_19_18.pdf	549274 d89ccf0426ccc5475e2ceec56ffaea622e07458e	no	2
Warnings:					
Information:					
10	Non Patent Literature	P60397TW-D2-D1_OA.pdf	1507357 e314fe69b4a6971cb28001029154fd9c2d8668ad	no	5
Warnings:					
Information:					
11	Fee Worksheet (SB06)	fee-info.pdf	30705 9b95085045033ef8fed89c94784d86286246f07d	no	2
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/789,315
Filing Date	October 20, 2017
First Inventor	Milton Clair WEBB, et al.
Art Unit	2822
Examiner Name	POTTER, ROY KARL
Attorney Docket No.	P60397US-C1/111548-235422 Conf. No. 9752

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the Final Office Action or Notice Of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☒ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	01-18-2019
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal /Sheri Villarreal/ Date 01-18-19

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1

CONFIRMATION NO. 9752

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

POA ACCEPTANCE LETTER

OC000000103058632

Date Mailed: 10/16/2018

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/03/2018.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/qtran/

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	15/789,315	WEBB ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 03 October, 2018	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

PAMELA YOUNG

Technology Center: PLRC

Telephone: _____

U.S. Patent and Trademark Office

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/789,315	Filing Date 10/20/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	10/03/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 30	Minus	** 30	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	terrance R lawrence
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Webb et al.	Examiner: Potter, Roy
Application No.: 15/789,315	Art Unit: 2822
Filed: October 20, 2017	Confirmation No.: 9752
For: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.111

Dear Examiner:

This is in response to the Office Action mailed July 3, 2018. Applicants respectfully request the Examiner to enter this Amendment and consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) An integrated circuit structure, comprising:

a first fin having a longest dimension along a first direction;

a second fin having a longest dimension along the first direction;

a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction;

a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction;

a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure having a length along the first direction greater than a length of the first gate structure and the second gate structure along the first direction; and

a dielectric material laterally adjacent to and in contact with the gate edge isolation structure, and the dielectric material having a composition different than a composition of the gate edge isolation structure.

2. (Original) The integrated circuit structure of claim 1, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode, and wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode.

3. (Original) The integrated circuit structure of claim 2, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

4. (Original) The integrated circuit structure of claim 3, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

5. (Original) The integrated circuit structure of claim 2, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

6. (Original) The integrated circuit structure of claim 1, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

7. (Original) The integrated circuit structure of claim 6, further comprising:

a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

8. (Original) The integrated circuit structure of claim 7, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

9. (Original) The integrated circuit structure of claim 8, further comprising:

a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

10. (Original) The integrated circuit structure of claim 1, wherein the gate edge isolation structure comprises silicon and nitrogen.

11. (Original) A method of fabricating and integrated circuit structure, the method comprising:

forming a first fin having a longest dimension along a first direction;

forming a second fin having a longest dimension along the first direction;

forming a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction;

forming a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction;

forming a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure having a length along the first direction greater than a length of the first gate structure and the second gate structure along the first direction; and

forming a dielectric material laterally adjacent to and in contact with the gate edge isolation structure, and the dielectric material having a composition different than a composition of the gate edge isolation structure.

12. (Original) The method of claim 11, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode, and wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode.

13. (Original) The method of claim 12, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

14. (Original) The method of claim 13, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

15. (Original) The method of claim 12, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

16. (Original) The method of claim 11, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

17. (Original) The method of claim 16, further comprising:

forming a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

18. (Original) The method of claim 17, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

19. (Original) The method of claim 18, further comprising:

forming a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

20. (Original) The method of claim 11, wherein the gate edge isolation structure comprises silicon and nitrogen.

21. (Original) A method of fabricating an integrated circuit structure, the method comprising:

forming a first fin comprising silicon, the first fin having a longest dimension along a first direction;

forming a second fin comprising silicon, the second fin having a longest dimension along the first direction;

forming an isolation material between the first fin and the second fin;

forming a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

forming a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

forming a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

forming a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

22. (Original) The method of claim 21, wherein the gate edge isolation structure comprises silicon and nitrogen.

23. (Original) The method of claim 21, wherein the dielectric material is in contact with the gate edge isolation structure.

24. (Original) The method of claim 21, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

25. (Original) The method of claim 24, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

26. (Original) The method of claim 24, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

27. (Original) The method of claim 21, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

28. (Original) The method of claim 27, further comprising:

forming a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

29. (Original) The method of claim 28, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

30. (Original) The method of claim 28, further comprising:

forming a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

REMARKS

The following remarks are provided in response to the office action mailed July 3, 2018 ("Office Action") in which the Office Action:

- rejected claims 1-10 on the ground of nonstatutory double patenting as being unpatentable over claims 26-35 of US Patent No. 9,831,306 to Webb (hereinafter Webb).
- indicated claims 11-30 as allowable.

The Applicants respectfully request reconsideration of the above referenced patent application for the following reasons:

Claims 1-10 rejection for nonstatutory double patenting

Claims 1-10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 26-35 of Webb.

Applicant herein submits a terminal disclaimer in accordance with 37 C.F.R. § 1.321, and respectfully request the Examiner withdraw the nonstatutory double patenting rejection to claims 1-10.

Allowance of claims 11-30

Applicant respectfully acknowledges the allowance of claims 11-30.

CONCLUSION

The Applicants submit that they have overcome the Office Action's rejections of the claims and that they have the right to claim the invention as set forth in the listed claims. The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 50-0393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

October 3, 2018
Date

/Justin K. Brask/
Justin K. Brask
Reg. No. 61,080

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Portland, OR 97204
Telephone: (503) 222-9981
Facsimile: (503) 796-2900

PTO/AIA/26 (04-14)
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) P60397US-C1

In re Application of: Webb et al.

Application No.: 15/789,315

Filed: October 20, 2017

For: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

The applicant, Intel Corporation, owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 9831306 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the applicant does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the **prior patent**, "as the term of said **prior patent** is presently shortened by any terminal disclaimer," in the event that said **prior patent** later:

expires for failure to pay a maintenance fee;
is held unenforceable;
is found invalid by a court of competent jurisdiction;
is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
has all claims canceled by a reexamination certificate;
is reissued; or
is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

Check either box 1 or 2 below, if appropriate.

1. ☐ The undersigned is the applicant. If the applicant is an assignee, the undersigned is authorized to act on behalf of the assignee.

I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 61080

/Justin K. Brask/ — Signature
10/3/2018 — Date

Justin K. Brask — Typed or printed name

Attorney for Applicant — Title
503-222-9981 — Telephone Number

☑ Terminal disclaimer fee under 37 CFR 1.20(d) included.

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: PA..
Document Description: Power of Attorney

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Application Number	15/789,315
Filing Date	October 20, 2017
First Named Inventor	Webb et al.
Title	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
Art Unit	2822
Examiner Name	Potter, Roy Karl
Attorney Docket Number	P60397US-C1

SIGNATURE of Applicant or Patent Practitioner

Signature	/Justin K. Brask/	Date (Optional)	10-03-2018
Name	Justin K. Brask	Registration Number	61080
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

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☑ *Total of 1 forms are submitted.

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

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☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 31817

OR

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Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	
Name	Lisa Hopkinson		
Title	Administrator of Patents		

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☐ Total of forms are submitted.

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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Intel Corporation

Application No./Patent No.: 15/789,315 Filed/Issue Date: October 20, 2017

Titled: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Intel Corporation, a Corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 032781, Frame 0116, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Justin K. Brask/	October 3, 2018
Signature	Date
Justin K. Brask	61080
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask/Lisa Puccinelli
Attorney Docket Number:	P60397US-C1/111548-235422

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
		Total in USD ($)		**160**

Electronic Acknowledgement Receipt	
EFS ID:	33910555
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1/111548-235422
Receipt Date:	03-OCT-2018
Filing Date:	20-OCT-2017
Time Stamp:	19:23:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$160
RAM confirmation Number	100418INTEFSW00006120500393
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Intel_P60397US-C1_ROA_10_03_18.pdf	122215 59875e48f3000b48730e573009b27030d1cc0be6	yes	10
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	8	
	Applicant Arguments/Remarks Made in an Amendment		9	10	
Warnings:					
Information:					
2	Terminal Disclaimer Filed	P60397US-C1_TD-Post-AIA_Patent.pdf	160388 02b58ba4d51ff53371042ef1bef93ead0e543045	no	2
Warnings:					
Information:					
3	Power of Attorney	P60397US-C1_POA_US_Coversheet_aia0082A.pdf	156018 92354d984b9447d04fbb730ded38c4b87f785a1d	no	1
Warnings:					
Information:					
4	Power of Attorney	P60397US-C1_POA.pdf	778039 05dc104347da070198a89bed233f800729d0a22b	no	1
Warnings:					
Information:					
5	Assignee showing of ownership per 37 CFR 3.73	P60397US-C1_Statement_Under_373c_AIA0096.pdf	118163 4c060e31273e5d645021e92046c412ad31b31569	no	3

Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	30638 a829b2404cdd13bb0c63df2f58dc3bafce19aa02	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1365461		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1/111548-235422	9752

31817 7590 07/03/2018

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER
POTTER, ROY KARL

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
07/03/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

Office Action Summary	Application No. 15/789,315	Applicant(s) WEBB ET AL.	
	Examiner ROY POTTER	Art Unit 2822	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-30* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *11-30* is/are allowed.

7)☒ Claim(s) *1-20* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *3/5/18, 10/20/17*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claims 1 – 30 are pending. Claims 1 – 10 are directed to an integrated circuit structure. Claims 11 – 30 are directed to a method of fabricating an integrated circuit structure.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory

double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l) (1) - 706.02(l) (3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1 – 10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claim 26 - 35 of U.S. Patent No. 9,831,306. Although the claims at issue are not identical, they are not patentably distinct from each other because both are directed to an integrated circuit structure comprising first and second fins along a first direction, first and second gate structures which are discontinuous and along a second direction orthogonal to the first and second fins, a gate edge isolation

structure between and in contact with the edge of each gate structure and a dielectric material laterally adjacent to and in contact with the gate edge isolation structure.

Claim 2 recites that each gate structure comprises a gate dielectric and a gate electrode. These are well known elements of a gate structure.

Dependent claim 3 recites the same limitation as patented claim 29.

Dependent claim 4 recites the same limitation as patented claim 30.

Dependent claim 5 recites the same limitation as patented claim 31.

Dependent claim 6 recites the same limitation as patented claim 32.

Dependent claim 7 recites the same limitation as patented claim 33.

Depended claim 8 recites the same limitation as patented claim 34.

Dependent claim 9 recites the same limitation as patented claim 35.

Dependent claim 10 recites the same limitation as patented claim 27.

Allowable Subject Matter

Claims 11 – 30 are allowed.

The prior art does not teach or suggest the recited method of fabricating an integrated circuit comprising forming parallel fins with discontinuous dummy spacers adjacent to the sidewalls of each fin, forming isolation structures between the dummy spacers, removing the dummy spacers and forming gate structures separated by the isolation structures.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ROY POTTER whose telephone number is (571)272-1842. The examiner can normally be reached on M-F.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on 571 270 5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ROY POTTER/
Primary Examiner, Art Unit 2822

Notice of References Cited	Application/Control No. 15/789,315	Applicant(s)/Patent Under Reexamination WEBB ET AL.	
	Examiner ROY POTTER	Art Unit 2822	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,831,306 B2	11-2017	Webb; Milton Clair	H01L23/535	1/1
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15789315	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	06/22/2018								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
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	29	=								
	30	=								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	121	second adj fin same gate with second and dielectric and gate with edge	US-PGPUB; USPAT; USOCR	OR	OFF	2018/01/30 17:21
L2	15871	((H01L29/66795 OR H01L29/785 OR H01L27/0886 OR H01L21/823821 OR H01L21/845 OR H01L27/1211 OR H01L27/0924 OR H01L29/41791).CPC.)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/01/30 17:23
L3	2043	second adj fin same gate with second	US-PGPUB; USPAT; USOCR	OR	OFF	2018/01/30 17:23
L4	2174	second adj fin same gate with second	US-PGPUB; USPAT; USOCR	OR	ON	2018/01/30 17:23
L5	202	second adj fin same gate with second and dielectric and gate with edge	US-PGPUB; USPAT; USOCR	OR	ON	2018/01/30 17:23
L6	1823	l2 and l3	US-PGPUB; USPAT; USOCR	OR	ON	2018/01/30 17:24
L7	174	l2 and l5	US-PGPUB; USPAT; USOCR	OR	ON	2018/01/30 17:24

1/30/2018 5:34:00 PM

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	TDB
	Filing Date	Herewith
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	
	Examiner Name	TDB
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
/R.K.P/		US-2007 /0054464	03-08-2007	ZHANG, Guowei	
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/R.K.P/		KR-20050082099	08-22-2005	CHOI, Jung A., et al.		
/R.K.P/		TW-201017772	05-01-2010	WEI, ANDY, et al.		
/R.K.P/		JP-2009260221	11-05-2009	TOSHIBA CORP		
/R.K.P/		JP-2004-356472	12-16-2004	RENESAS TECH CORP		
/R.K.P/		JP-2002-530872	09-17-2002	INFINCON TECHNOLOGIES AG		

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Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
/R.K.P/		International Search Report and Written Opinion from PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) Mailed September 26, 2014, 10 pages.	
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EXAMINER /ROY K POTTER/ **DATE CONSIDERED** 01/30/2018

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L7	2418	second with fin and fin with gate and dummy with spacer	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/22 18:39
L8	35277	(H01L29/66795 or H01L29/785 or H01L27/0886 or H01L21/823821 or H01L21/845 or H01L27/1211 or H01L27/0924 or H01L29/41791).cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/22 18:40
L9	2082	l7 and l8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/22 18:41
L10	718	second with fin and fin with gate and dummy with spacer same fin with sidewall	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/22 18:41
L11	620	l8 and l10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/06/22 18:41

6/22/2018 6:42:24 PM

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/789,315
	Filing Date	October 20, 2017
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	2822
	Examiner Name	POTTER, ROY KARL
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

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Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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/R.K.P/		WO-2013101007	07-04-2013	Intel Corporation		
/R.K.P/		CN-103258823	08-21-2013	Hemanth JAGANNATHAN		X

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Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/R.K.P/		Extended European Search Report for European Patent Application No. 13899890.1 (Attorney Docket No. P60397EP) mailed December 4, 2017, 8 pgs.	
/R.K.P/		Office Action for Taiwan Patent Application No. 106120024 (Attorney Docket No. P60397TW-D2) mailed September 21, 2017, 26 pgs., with English translation.	X

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	TDB
	Filing Date	Herewith
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	
	Examiner Name	TDB
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

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/R.K.P/		US-7,781,274	08-24-2010	NAKABAYASHI, YUKIO, ET AL.	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15789315	WEBB ET AL.
	Examiner	Art Unit
	ROY POTTER	2822

CPC- SEARCHED		
Symbol	Date	Examiner
H01L29/66795, H01L29/785, H01L27/0886, H01L21/823821, H01L21/845, H01L27/1211, H01L27/0924, H01L29/41791	1/30/18	RP
H01L29/66795, H01L29/785, H01L27/0886, H01L21/823821, H01L21/845, H01L27/1211, H01L27/0924, H01L29/41791	6/22/2018	RP

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

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SEARCH NOTES		
Search Notes	Date	Examiner

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

Substitute for form 1449A/PTO	*Complete if Known*	
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		US-20130277758	10-24-2013	Josephine B. CHANG et al.	
		US-20130187235	07-25-2013	Yuan-sheng HUANG et al.	
		US-20130214364	08-22-2013	Hamanth JAGANNATHAN et al.	

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		WO-2013101007	07-04-2013	Intel Corporation		
		CN-103258823	08-21-2013	Hemanth JAGANNATHAN		X

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Bibliographic data: CN103258823 (A) — 2013-08-21

Semiconductor structure and formation method thereof

Inventor(s): JAGANNATHAN HEMANTH; PARUCHURI VAMSI K ± (JAGANNATHAN HEMANTH, ; PARUCHURI VAMSI K)

Applicant(s): IBM ± (IBM)

Classification: - international:***H01L21/28; H01L21/8238; H01L27/092; H01L29/49***
- cooperative: **H01L21/823821; H01L21/823842; H01L21/84; H01L27/0924; H01L27/1203; H01L29/4966;** H01L29/517; H01L29/518; H01L29/66545

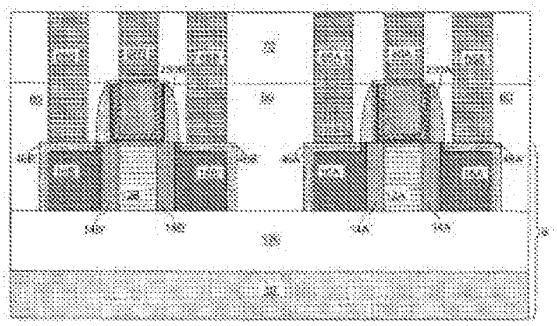
Application number: CN2013149984 20130208 Global Dossier

Priority number (s): US201213398314 20120216

Also published as: US2013214364 (A1) US2013217220 (A1)

Abstract of CN103258823 (A)

The invention refers to a semiconductor structure and a formation method thereof. A tantalum alloy layer is employed as a work function metal for field effect transistors. The tantalum alloy layer can be selected from TaC, TaAl, and TaAlC. When used in combination with a metallic nitride layer, the tantalum alloy layer and the metallic nitride layer provides two work function values that differ by 300 mV-500 mV, thereby enabling multiple field effect transistors having different threshold voltages. The tantalum alloy layer can be in contact with a first gate dielectric in a first gate, and the metallic nitride layer can be in contact with a second gate dielectric having a same composition and thickness as the first gate dielectric and located in a second gate.



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DESCRIPTION CN103258823

The present invention relates to a semiconductor structure and a method of forming the same. The tantalum alloy layer is used as the work function metal of the field effect transistor. The tantalum alloy layer may be selected from TaC, TaAl and TaAlC. When used in combination with a metal nitride layer, the tantalum alloy layer and the metal nitride layer provide two work function values that differ from 300 mV to 500 mV to achieve multiple field effect transistors with different threshold voltages. The tantalum alloy layer may be in contact with a first gate dielectric in the first gate and the metal nitride layer may be in contact with a second gate dielectric having the same composition and thickness as the first gate dielectric And located in the second gate.

本发明涉及半导体结构及其形成方法。钽合金层被用作场效应晶体管的功函数金属。该钽合金层可以选自TaC、TaAl和TaAlC。在与金属氮化物层组合使用时，钽合金层和金属氮化物层提供相差300mV-500mV的两个功函数值，从而实现具有不同阈值电压的多个场效应晶体管。钽合金层可以与第一栅极中的第一栅极电介质接触，且金属氮化物层可以与第二栅极电介质接触，该第二栅极电介质具有与第一栅极电介质相同的组成和厚度并位于第二栅极中。

Semiconductor structure and method of forming the same

半导体结构及其形成方法

Technical field

技术领域

This disclosure relates generally to semiconductor devices and, more particularly, to semiconductor structures that include a tantalum alloy layer and a metal nitride layer and methods of making the same.

本公开一般涉及半导体器件，更具体地，涉及包括钽合金层和金属氮化物层的半导体结构及其制造方法。

Background technique

背景技术

The good operation of p-type field effect transistors (PFETs) and n-type field effect transistors (NFETs) in CMOS circuits requires that the gate electrodes have a work function that is at least 300mV ~ 400mV apart. To provide multiple work functions with different work functions, multiple work function metals are used in alternative gate integration schemes. However, such work function metals tend not to provide a sufficiently low resistivity, thereby requiring the deposition of additional filler metal with low resistivity. Thus, a typical replacement gate electrode includes a stack of about 4-5 layers of different metals. As semiconductor devices are scaled down to 22nm nodes and 14nm nodes, it becomes even more challenging to fill narrow gate cavities with a stack of different conductive metal layers.

CMOS电路中的p型场效应晶体管（PFET）和n型场效应晶体管（NFET）的良好运行要求栅极电极具有相差至少300mV~400mV的功函数（work function）。为了提供具有不同功函数的多个功函数，在替代栅极集成方案中使用多种功函数金属。但是，这样的功函数金属倾向于无法提供足够低的电阻率，由此要求沉积具有低电阻率的额外的填充金属。因此，典型的替代栅极电极包括不同金属的大约4-5个层的叠层。随着半导体器件按比例缩小到22nm节点和14nm节点，使用不同导电金属层的叠层来填充窄栅极腔变得更具挑战性。

Content of the invention

发明内容

The tantalum alloy layer is used as the work function metal of the field effect transistor. The tantalum alloy layer may be selected from TaC, TaAl and TaAlC. When used in combination with a metal nitride layer, the tantalum alloy layer and the metal nitride layer provide two work function values that differ from 300 mV to 500 mV, thereby enabling the plurality of field effect transistors to have different threshold voltages. The tantalum alloy layer may be in contact with a first gate dielectric in the first gate and the metal nitride layer may be in contact with a second gate dielectric having the same composition and thickness as the first gate dielectric And located in the second gate.

钽合金层被用作场效应晶体管的功函数金属。钽合金层可以选自TaC、TaAl和TaAlC。在与金属氮

化物层组合使用时，钽合金层和金属氮化物层提供相差300mV~500mV的两个功函数值，由此使得多个场效应晶体管能够具有不同阈值电压。钽合金层可以与第一栅极中的第一栅极电介质接触，且金属氮化物层可以与第二栅极电介质接触，该第二栅极电介质具有与第一栅极电介质相同的组成和厚度并位于第二栅极中。

According to a first aspect of the present disclosure, there is provided a semiconductor structure including at least two field effect transistors. The semiconductor structure includes a first field effect transistor including a first gate dielectric and a first gate electrode, wherein the first gate electrode includes a conductive tantalum alloy layer in contact with the first gate dielectric And a second field effect transistor including a second gate dielectric and a second gate electrode, wherein the second gate electrode includes a metal nitride layer in contact with the second gate dielectric.

根据本公开的第一方面，提供了一种包括至少两个场效应晶体管的半导体结构。所述半导体结构包括：第一场效应晶体管，其包括第一栅极电介质和第一栅极电极，其中，所述第一栅极电极包括与所述第一栅极电介质接触的导电钽合金层；以及第二场效应晶体管，其包括第二栅极电介质和第二栅极电极，其中，所述第二栅极电极包括与所述第二栅极电介质接触的金属氮化物层。

According to another aspect of the present invention, a method of forming a semiconductor structure is provided. The method includes forming a first gate cavity and a second gate cavity over a semiconductor portion, wherein each of the first gate cavity and the second gate cavity is planarized with a dielectric layer Laterally surrounded, wherein a top surface of the semiconductor portion is exposed at a bottom of each of the first and second gate cavities; a second gate cavity is formed in the first and second gate cavities Forming a gate dielectric layer; forming a first work function material layer directly on a first portion of the gate dielectric layer in the first gate cavity and directly over the gate dielectric layer, A second work function material layer is formed on a second portion of the second gate cavity, wherein one of the first and second work function material layers is a conductive tantalum alloy layer, and the first and second And the other of the work function material layers is a metal nitride layer; and filling the first gate cavity and the second gate cavity with a conductive material, wherein a first gate electrode is formed in the first gate cavity Conductive material portion and forming a second conductive material portion in the second gate cavity.

根据本发明的另一方面，提供了一种形成半导体结构的方法。所述方法包括：在半导体部分之上形成第一栅极腔和第二栅极腔，其中，所述第一栅极腔和所述第二栅极腔中的每一者被平面化电介质层侧向（laterally）包围，其中，在所述第一和第二栅极腔中的每一者的底部处，所述半导体部分的顶表面被暴露；在所述第一和第二栅极腔中形成栅极电介质层；直接在所述栅极电介质层的位于所述第一栅极腔中的第一部分上形成第一功函数材料层，并直接在所述栅极电介质层的位于所述第二栅极腔中的第二部分上形成第二功函数材料层，其中，所述第一和第二功函数材料层中的一者是导电钽合金层，且所述第一和第二功函数材料层中的另一者是金属氮化物层；以及用导电材料填充所述第一栅极腔和所述第二栅极腔，其中，在所述第一栅极腔中形成第一导电材料部分，并在所述第二栅极腔中形成第二导电材料部分。

BRIEF DESCRIPTION OF THE DRAWINGS FIG

附图说明

Figure 1 is a vertical cross-sectional view of a first exemplary semiconductor structure after forming a disposable gate level layer in accordance with a first embodiment of the present disclosure;

图1是根据本公开的第一实施例在形成一次性（disposable）栅极级层（level layer）之后的第一示例性半导体结构的垂直截面图；

Figure 2 is a vertical cross-sectional view of a first exemplary semiconductor structure after patterning a disposable gate structure and forming a source extension / drain extension region according to a first embodiment of the present disclosure;

图2是根据本公开的第一实施例在对一次性栅极结构进行构图并形成源极扩展区域/漏极扩展区域之后的第一示例性半导体结构的垂直截面图；

Figure 3 is a vertical cross-sectional view of a first exemplary semiconductor structure after forming a spacer and a source / drain region in accordance with a first embodiment of the present disclosure;

图3是根据本公开的第一实施例在形成间隔物（spacer）和源极区域/漏极区域之后的第一示例性半导体结构的垂直截面图；

Figure 4 is a vertical cross-sectional view of a first exemplary semiconductor structure after deposition and planarization of a planarization dielectric layer in accordance with a first embodiment of the present disclosure;

图4是根据本公开的第一实施例在平面化电介质层的沉积和平面化之后的第一示例性半导体结构的垂直截面图；

Figure 5 is a vertical cross-sectional view of a first exemplary semiconductor structure after removing a disposable gate structure in accordance with a first embodiment of the present disclosure;

图5是根据本公开的第一实施例在去除一次性栅极结构之后的第一示例性半导体结构的垂直截面图；

6 is a vertical cross-sectional view of a first exemplary semiconductor structure after forming a gate dielectric layer and a first work function material layer according to a first embodiment of the present disclosure;

图6是根据本公开的第一实施例在形成栅极电介质层和第一功函数材料层之后的第一示例性半导体结构的垂直截面图；

7 is a vertical cross-sectional view of a first exemplary semiconductor structure after removing an exposed portion of a first work function material layer from a second field effect transistor region according to the first embodiment of the present disclosure;

图7是根据本公开的第一实施例在从第二场效应晶体管区域去除第一功函数材料层的暴露部分之后的第一示例性半导体结构的垂直截面图；

Figure 8 is a vertical cross-sectional view of a first exemplary semiconductor structure after forming a second work function material layer in accordance with a first embodiment of the present disclosure;

图8是根据本公开的第一实施例在形成第二功函数材料层之后的第一示例性半导体结构的垂直截面图；

Figure 9 is a vertical cross-sectional view of a first exemplary semiconductor structure after depositing a layer of conductive material according to a first embodiment of the present disclosure;

图9是根据本公开的第一实施例在沉积导电材料层之后的第一示例性半导体结构的垂直截面图；

Figure 10 is a vertical cross-sectional view of a first exemplary semiconductor structure after planarization in accordance with a first embodiment of the present disclosure;

图10是根据本公开的第一实施例在平面化之后的第一示例性半导体结构的垂直截面图；

Figure 11 is a vertical cross-sectional view of a first exemplary semiconductor structure after formation of a contact-level dielectric layer and a contact via structure in accordance with a first embodiment of the present disclosure;

图11是根据本公开的第一实施例在形成接触级电介质层和接触过孔结构（contact via structure）之

后的第一示例性半导体结构的垂直截面图；

12 is a cross-sectional view of a semiconductor device according to a second embodiment of the present disclosure in forming a semiconductor fin, a disposable gate structure, a source extension / drain extension region, a source / drain region, a source metal semiconductor alloy portion / A second exemplary semiconductor structure after the drain metal semiconductor alloy portion;

图12是根据本公开的第二实施例在形成半导体鳍（fin）、一次性栅极结构、源极扩展区域/漏极扩展区域、源极区域/漏极区域、源极金属半导体合金部分/漏极金属半导体合金部分之后的第二示例性半导体结构的垂直截面图；

Figure 13 is a vertical cross-sectional view of a second exemplary semiconductor structure after deposition and planarization of a planarization dielectric layer in accordance with a second embodiment of the present disclosure;

图13是根据本公开的第二实施例在平面化电介质层的沉积和平面化之后的第二示例性半导体结构的垂直截面图；

Figure 14 is a vertical cross-sectional view of a second exemplary semiconductor structure after forming a contact-level dielectric layer and a contact via structure in accordance with a second embodiment of the present disclosure;

图14是根据本公开的第二实施例在形成接触级电介质层和接触过孔结构之后的第二示例性半导体结构的垂直截面图；

Figure 15 is a vertical cross-sectional view of the second exemplary semiconductor structure of Figure 14 along the vertical plane XX 'in Figure 13;

图15是图14中的第二示例性半导体结构沿着图13中的垂直平面X-X’的垂直截面图；

Figure 16 is a vertical cross-sectional view of a third exemplary semiconductor structure after patterning a second work function material layer according to a third embodiment of the present disclosure;

图16是根据本公开的第三实施例在对第二功函数材料层进行构图之后的第三示例性半导体结构的垂直截面图；

Figure 17 is a vertical cross-sectional view of a third exemplary semiconductor structure after depositing a conductive material layer in accordance with a third embodiment of the present disclosure;

图17是根据本公开的第三实施例在沉积导电材料层之后的第三示例性半导体结构的垂直截面图；

Figure 18 is a vertical cross-sectional view of a third exemplary semiconductor structure after planarization in accordance with a third embodiment of the present disclosure;

图18是根据本公开的第三实施例在平面化之后的第三示例性半导体结构的垂直截面图；

Figure 19 is a vertical cross-sectional view of a third exemplary semiconductor structure after formation of contact-level dielectric layers and contact via structures in accordance with a third embodiment of the present disclosure; and

图19是根据本公开的第三实施例在形成接触级电介质层和接触过孔结构之后的第三示例性半导体结构的垂直截面图；以及

FIG. 20 is a vertical sectional view of a fourth exemplary semiconductor structure according to a fourth embodiment of the present disclosure. FIG.

图20是根据本公开的第四实施例的第四示例性半导体结构的垂直截面图。

detailed description

具体实施方式

As described above, the present disclosure relates to a semiconductor device, and more particularly, to a semiconductor structure including a tantalum alloy layer and a metal nitride layer, which will be described in detail with reference to the drawings, and a method of manufacturing the same. The same and corresponding elements mentioned herein and exemplified in the figures are denoted by the same reference numerals. The drawings are not necessarily to scale.

如上所述，本公开涉及半导体器件，更具体地，涉及将通过附图来详细地描述的包括钽合金层和金属氮化物层的半导体结构及其制造方法。本文中提到的和在图中示例的相同和相应的要素由相同的参考标号表示。附图未必按比例绘制。

The use of "a", "one", "another", "another", "another", "further another" or other grammatical qualifiers as used herein is used to distinguish one element from another. Thus, an element identified by a specific grammatical qualifier in a claim may or may not correspond to an element of the specification that employs the same grammatical qualifier.

本文中使用的“一”、“一个”、“另一个”、“再一个”、“又一个”、“进一步另一个”或者其他文法限定词被用于区分一个要素与另一个要素。这样，在权利要求中用特定的文法限定词来标识的要素可以或可以不对应于说明书中采用相同的文法限定词的要素。

As used herein, "first," "second," "third," and other ordinal numbers are used to distinguish one element from another. As such, elements identified with a particular ordinal number in the claims may or may not correspond to elements employing the same ordinals in the specification.

本文中使用的“第一”、“第二”、“第三”和其他序数被用于区分一个要素与另一个要素。这样，在权利要求中用特定的序数来标识的要素可以或可以不对应于说明书中采用相同序数的要素。

Referring to FIG. 1, a first exemplary semiconductor structure according to an embodiment of the present disclosure includes a semiconductor substrate 8 on which respective components of a field-effect transistor are sequentially formed. The semiconductor substrate 8 may be a bulk substrate or a semiconductor-on-insulator (SOI) substrate (not shown) that entirely contains a bulk semiconductor material, the SOI substrate includes a top semiconductor layer, a buried buried insulator layer, and a bottom semiconductor layer underlying the buried insulator layer.

参考图1，根据本公开的实施例的第一示例性半导体结构包括半导体衬底8、场效应晶体管的各个部件相继在其上形成。半导体衬底8可以是整个地包含体半导体材料的体衬底或者是绝缘体上半导体（SOI）衬底（未示出），所述SOI衬底包含顶部半导体层、位于顶部半导体层下面的掩埋（buried）绝缘体层、以及位于掩埋绝缘体层下面的底部半导体层。

Various portions of the semiconductor material in the semiconductor substrate 8 may be doped with n-type or p-type electrical dopants at different doping levels. For example, the semiconductor substrate 8 may include an underlying semiconductor layer 10, a first doped well 12A formed in a first device region (a left region in FIG. 1), and a second doped region 12A in a second device region 1). The second doped well 12B is formed in the right-side region of FIG. In one embodiment, the second doped well 12B may be doped with a dopant of a first conductivity type, which may be n-type or p-type, and may be doped with a dopant of a second conductivity type To dope the first doped well 12A, the second conductivity type being opposite to the first conductivity type. If the first conductivity type is p-type, then the second conductivity type is n-type, and vice versa.

可以用n型或p型的电气掺杂剂以不同的掺杂浓度水平来掺杂半导体衬底8中的半导体材料的各个部分。例如，半导体衬底8可以包括下伏的（underlying）半导体层10、在第一器件区域（图1中左侧的区域）中形成的第一掺杂阱12A、以及在第二器件区域（图1中右侧的区域）中形成的第二掺杂阱12B。在一个实施例中，可以用第一导电类型的掺杂剂来掺杂第二掺杂阱12B，该第一导电类型可以是n型或p型，并可以用第二导电类型的掺杂剂来掺杂第一掺杂阱12A，该第二导电类型与第一导电类型相反。如果第一导电类型为p型，则第二导电类型为n型，且反之亦然。

Shallow trench isolation structures 20 are formed such that each of the second doped well 12B and the first doped well 12A is laterally separated. Typically, each of the second doped well 12B and the first doped well 12A is laterally surrounded by a contiguous portion of the shallow trench isolation structure 20. If the semiconductor substrate 8 is a semiconductor-on-insulator substrate, the bottom surface of the second doped well 12B and the first doped well 12A may contact a buried insulator layer (not shown), which, together with the shallow trench isolation structure 20, Each of the second doped well 12B and the first doped well 12A is electrically isolated from the other semiconductor portions of the semiconductor substrate 8. In one embodiment, the topmost surface of the shallow trench isolation structure 20 may be substantially coplanar with the topmost surfaces of the second doped well 12B and the first doped well 12A.

浅沟槽隔离结构20被形成为使第二掺杂阱12B和第一掺杂阱12A中的每一者被侧向分隔。典型地，第二掺杂阱12B和第一掺杂阱12A中的每一者被浅沟槽隔离结构20的邻接（contiguous）部分侧向包围。如果半导体衬底8是绝缘体上半导体衬底，第二掺杂阱12B和第一掺杂阱12A的底表面可以接触掩埋的绝缘体层（未示出），其连同浅沟槽隔离结构20将第二掺杂阱12B和第一掺杂阱12A中的每一者与半导体衬底8的其他半导体部分电隔离。在一个实施例中，浅沟槽隔离结构20的最顶表面可以与第二掺杂阱12B和第一掺杂阱12A的最顶表面基本上共面。

The disposable gate level layer is deposited on the semiconductor substrate 8 as a blanket layer, ie as a non-patterned continuous layer. Disposable gate level layers may include, for example, vertical stacks of a disposable gate dielectric layer 23L, a disposable gate material layer 27L, and a disposable gate cap dielectric layer 29L. Disposable gate dielectric layer 23L may be, for example, a layer of silicon oxide, silicon nitride, or silicon oxynitride. The thickness of the disposable gate dielectric layer 23L may be from 1 nm to 10 nm, although smaller or larger thicknesses may also be used. The disposable gate material layer 27L includes a material that is subsequently selectively removed from the dielectric material of the planarization dielectric layer to be subsequently formed. For example, the disposable gate material layer 27L may include a semiconductor material such as a polycrystalline semiconductor material or an amorphous semiconductor material. The thickness of the disposable gate material layer 27L may be from 30 nm to 300 nm, but a smaller or larger thickness may also be employed. The disposable gate cap dielectric layer 29L may include a dielectric material such as silicon oxide, silicon nitride, or silicon oxynitride. The thickness of the disposable gate cap dielectric layer 29L may be from 3 nm to 30 nm, although smaller or larger thicknesses may also be employed. Although the present disclosure illustrates the present disclosure as a vertical gate stack that includes the vertical stacks of the disposable gate

dielectric layer 23L, the disposable gate material layer 27L, and the disposable gate cap dielectric layer 29L, any other A disposable gate level layer may be used as long as the material in the disposable gate level layer can be selectively removed for the planarized dielectric layer to be subsequently formed.

一次性栅极级层被沉积在半导体衬底8上作为毯覆（blanket）层，即，作为未被构图的连续层。一次性栅极级层可以包括例如一次性栅极电介质层23L、一次性栅极材料层27L和一次性栅极帽盖（cap）电介质层29L的垂直叠层。一次性栅极电介质层23L可以是例如氧化硅、氮化硅或氧氮化硅的层。一次性栅极电介质层23L的厚度可以为从1nm到10nm，但还可以使用更小或更大的厚度。一次性栅极材料层27L包括随后对随后将形成的平面化电介质层的电介质材料具有选择性地去除的材料。例如，一次性栅极材料层27L可以包括诸如多晶半导体材料或非晶半导体材料的半导体材料。一次性栅极材料层27L的厚度可以为从30nm到300nm，但还可以采用更小或更大的厚度。一次性栅极帽盖电介质层29L可以包括诸如氧化硅、氮化硅或氧氮化硅的电介质材料。一次性栅极帽盖电介质层29L的厚度可以为从3nm到30nm，但还可以采用更小或更大的厚度。尽管以包括一次性栅极电介质层23L、一次性栅极材料层27L和一次性栅极帽盖电介质层29L的垂直叠层的一次性栅极级层示例了本公开，但也可以采用任何其他一次性栅极级层，只要可以对随后将形成的平面化电介质层具有选择性地去除该一次性栅极级层中的材料即可。

Referring to FIG. 2, the disposable gate level layers (29L, 27L, 23L) are lithographically patterned to form a disposable gate structure. Specifically, a photoresist (not shown) is applied to the topmost surface of the disposable gate level (29L, 27L, 23L) and lithographically patterned by photolithographic exposure and development. The patterns in the photoresist are transferred by etching to the disposable gate level (29L, 27L, 23L), which can be anisotropic etching, such as reactive ion etching. The remaining portion of the disposable gate level (29L, 27L, 23L) after the pattern transfer constitutes a disposable gate structure.

参考图2，一次性栅极级层（29L、27L、23L）被光刻构图以形成一次性栅极结构。具体地，光致抗蚀剂（未示出）被施加到一次性栅极级层（29L、27L、23L）的最顶表面上，并通过光刻曝光和显影而被光刻构图。光致抗蚀剂中的图形通过蚀刻而被转移（transfer）到一次性栅极级层（29L、27L、23L），该蚀刻可以是各向异性蚀刻，例如反应离子蚀刻。在图形转移之后的一次性栅极级层（29L、27L、23L）的剩余部分构成了一次性栅极结构。

The disposable gate stack may include, for example, a first disposable gate structure formed over the first doped well 12A in the first device region and over the second doped well 12B in the second device region The second disposable gate structure is formed. The first disposable gate structure is a stack of the first disposable gate dielectric portion 23A, the first disposable gate material portion 27A, and the first disposable gate cap portion 29A, and the second one The secondary gate structure is a stack of a second disposable gate dielectric portion 23B, a second disposable gate material portion 27B, and a second disposable gate cap portion 29B. The first disposable gate cap portion 29A and the second disposable gate cap portion 29B are the remaining portions of the disposable gate cap dielectric layer 29L. The first disposable gate material portion 27A and the second disposable gate material portion 27B are the remaining portions of the disposable gate material layer 27L. The first

disposable gate dielectric portion 23A and the second disposable gate dielectric portion 23B are the remaining portions of the disposable gate dielectric layer 23L.

一次性栅极叠层可以包括例如在第一器件区域中的第一掺杂阱12A之上形成的第一一次性栅极结构以及在第二器件区域中的第二掺杂阱12B之上形成的第二一次性栅极结构。第一一次性栅极结构是第一一次性栅极电介质部分23A、第一一次性栅极材料部分27A和第一一次性栅极帽盖部分29A的叠层，并且第二一次性栅极结构是第二一次性栅极电介质部分23B、第二一次性栅极材料部分27B和第二一次性栅极帽盖部分29B的叠层。第一一次性栅极帽盖部分29A和第二一次性栅极帽盖部分29B是一次性栅极帽盖电介质层29L的剩余部分。第一一次性栅极材料部分27A和第二一次性栅极材料部分27B是一次性栅极材料层27L的剩余部分。第一一次性栅极电介质部分23A和第二一次性栅极电介质部分23B是一次性栅极电介质层23L的剩余部分。

Masked ion implantation can be used to form various source extension / drain extension regions. For example, a dopant of the first conductivity type may be implanted into a portion of the first doped well 12A that is not covered by the first disposable gate structure (23A, 27A, 29A) to form a portion of the first doped structure having a first conductivity type Doped first source extension region / drain extension region 14A. During this implantation, the second doped well 12B may be masked with a patterned photoresist (not shown) to prevent the addition of additional dopants of the first conductivity type therein. As used herein, "source extension region / drain extension region" collectively refers to a source extension region and a drain extension region. Similarly, a dopant of the second conductivity type may be implanted into a portion of the second doped well 12B that is not covered by the second disposable gate structure (23B, 27B, 29B) to form a second source extension Area / drain extension area 14B. During this implantation, the first doped well 12A may be masked with another patterned photoresist (not shown) to prevent implantation of additional dopants of the second conductivity type therein.

可以采用掩蔽离子注入来形成各种源极扩展区域/漏极扩展区域。例如，第一导电类型的掺杂剂可被注入到第一掺杂阱12A的未被第一一次性栅极结构（23A、27A、29A）覆盖的部分，以形成具有第一导电类型的掺杂的第一源极扩展区域/漏极扩展区域14A。在该注入过程中，可以通过经构图的光致抗蚀剂（未示出）来掩蔽第二掺杂阱12B，以防止在其中注入额外的第一导电类型的掺杂剂。本文中使用的“源极扩展区域/漏极扩展区域”共同地表示源极扩展区域和漏极扩展区域。类似地，第二导电类型的掺杂剂可被注入到第二掺杂阱12B的未被第二一次性栅极结构（23B、27B、29B）覆盖的部分，以形成第二源极扩展区域/漏极扩展区域14B。在该注入过程中，可以通过另一经构图的光致抗蚀剂（未示出）来掩蔽第一掺杂阱12A，以防止在其中注入额外的第二导电类型的掺杂剂。

Referring to FIG. 3, gate spacers are formed on the sidewalls of each of the disposable gate structures, for example, by deposition of a conformal dielectric material layer and anisotropic etching. The gate spacer may include a first gate spacer 52A formed around the first disposable gate structure (23A, 27A, 29A) and a second gate spacer formed around the second disposable gate structure (23B, 27B, 29B) The second gate spacer 52B is formed.

参考图3，例如，通过保形的（conformal）电介质材料层的沉积和各向异性蚀刻，在一次性栅极结构中的每一者的侧壁上形成栅极间隔物。栅极间隔物可以包括在第一一次性栅极结构（23A、27A、29A）周围形成的第一栅极间隔物52A以及在第二一次性栅极结构（23B、27B、29B）周围形成的第二栅极间隔物52B。

The first source / drain regions 16A and 16B are formed in the first doped well 12A and the second doped well 12B, respectively, by injecting an electrical dopant that may be a p-type dopant or an n-type dopant, Two source / drain regions 16B. The first source / drain regions 16A and the second source / drain regions 16B may be formed using masked ion implantation. Alternatively, the first source electrode (eg, silicon germanium alloy or silicon carbon alloy) may be replaced by replacing the physically exposed portion of the first doped well 12A or the second doped well 12B with a stress-generating semiconductor material The region / drain region 16A and the second source / drain region 16B are formed as source / drain regions. The buried stress producing semiconductor material may be epitaxially aligned with the remaining portion of the first doped well 12A or the remaining portion of the second doped well 12B.

通过注入可以是p型掺杂剂或n型掺杂剂的电气掺杂剂，分别在第一掺杂阱12A和第二掺杂阱12B中形成第一源极区域/漏极区域16A和第二源极区域/漏极区域16B。可以采用掩蔽离子注入来形成第一源极区域/漏极区域16A和第二源极区域/漏极区域16B。或者，可以通过用应力产生（stress-generating）半导体材料（例如硅锗合金或硅碳合金）来替换第一掺杂阱12A或第二掺杂阱12B的物理暴露部分，来将第一源极区域/漏极区域16A和第二源极区域/漏极区域16B形成为源极区域/漏极区域。掩埋的应力产生半导体材料可以与第一掺杂阱12A的剩余部分或第二掺杂阱12B的剩余部分外延对准。

Referring to FIG. 4, a first metal semiconductor alloy portion 46A and a second metal semiconductor alloy portion 46B may be formed on the exposed semiconductor material on the top surface of the semiconductor substrate 8, for example, by deposition and annealing of a metal layer (not shown). The reactive portion of the metal layer has a selective removal of unreacted portions of the metal layer. The reactive portion of the metal layer constitutes a metal semiconductor alloy portion (46A, 46B) that may include metal silicide if the semiconductor material of the first and second source and drain regions (16A, 16B) includes silicon Part

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参考图4，可以例如通过金属层（未示出）的沉积和退火，在半导体衬底8的顶表面上的暴露半导体材料上形成第一金属半导体合金部分46A和第二金属半导体合金部分46B。对金属层的反应部分具有选择性地去除该金属层的未反应部分。金属层的反应部分构成金属半导体合金部分（46A、46B），如果第一和第二源极和漏极区域（16A、16B）的半导体材料包括硅，则所述金属半导体合金部分可以包括金属硅化物部分。

Each of the metal semiconductor alloy portions 46A, 46B includes a first source-side metal semiconductor alloy portion (one of 46A) formed on the first source region (one of 16A), a second source- (The other one of 16A)

formed on the other of the first source region and the second source side metal semiconductor alloy portion (46B) formed on the other one of the second source regions) And a second drain-side metal semiconductor alloy portion (the other of 16B) formed on the second drain region (the other one of 16B).

各金属半导体合金部分46A、46B包括：在第一源极区域（16A中的一个）上形成的第一源极侧金属半导体合金部分（46A中的一个）、在第一漏极区域（16A中的另一个）上形成的第一漏极侧金属半导体合金部分（16A中的另一个）、在第二源极区域（16B中的一个）上形成的第二源极侧金属半导体合金部分（46B中的一个）、以及在第二漏极区域（16B中的另一个）上形成的第二漏极侧金属半导体合金部分（16B中的另一个）。

Alternatively, the first and second gate spacers may be formed over the metal semiconductor alloy portion (46A, 46B), the first and second disposable gate structures (23A, 27A, 29A, 23B, 27B, 29B) (52A, 52B) a dielectric liner (not shown) is deposited. Alternatively, a first stress-generating liner (not shown) may be respectively formed over the first disposable gate structure (23A, 27A, 29A) and the second disposable gate structure (23B, 27B, 29B)) And a second stress-producing liner (not shown). The first and second stress-generating liners may include a dielectric material that produces compressive or tensile stress to the underlying structure and may be deposited by plasma-enhanced chemical vapor deposition under various plasma conditions Silicon nitride layer.

可选地，可以在金属半导体合金部分（46A、46B）、第一和第二一次性栅极结构（23A、27A、29A、23B、27B、29B）以及第一和第二栅极间隔物（52A、52B）之上沉积电介质衬里（liner）（未示出）。可选地，可以在第一一次性栅极结构（23A、27A、29A）和第二一次性栅极结构（23B、27B、29B）之上分别形成第一应力产生衬里（未示出）和第二应力产生衬里（未示出）。第一应力产生衬里和第二应力产生衬里可以包括产生对下伏的结构的压缩应力或张伸应力的电介质材料，并且可以是在各种等离子体条件下通过等离子体增强化学气相沉积来沉积的氮化硅层。

The planarization dielectric layer 60 may be deposited over the first stress-generating liner and / or the second stress-generating liner (if present) or deposited on the metal semiconductor alloy portions (46A, 46B), first and second time Above the first and second gate spacers (52A, 52B) (if no stress-producing liner is present) between the first and second gate spacers (23A, 27A, 29A, 23B, 27B, 29B). Preferably, planarization dielectric layer 60 is a dielectric material that can be easily planarized. For example, the planarization dielectric layer 60 may be doped silicate glass or undoped silicate glass (silicon oxide).

平面化电介质层60可以被沉积在第一应力产生衬里和/或第二应力产生衬里（如果存在）之上，或者被沉积在金属半导体合金部分（46A、46B）、第一和第二一次性栅极结构（23A、27A、29A、23B、27B、29B）以及第一和第二栅极间隔物（52A、52B）之上（如果不存在应力产生衬里）。优选地，平面化电介质层60是可以被容易地平面化的电介质材料。例如，平面化电介质层60可以是经掺杂的硅酸盐玻璃或未掺杂的硅酸盐玻璃（氧化硅）。

Over the topmost surfaces of the first and second disposable gate structures (23A, 27A, 29A, 23B, 27B, 29B), ie, between the first and second disposable gate cap portions , 29B), the planarization dielectric layer 60 and any additional layers of dielectric material, including any one of the existing first stress-generating liner, second stress-generating liner, and dielectric liner, are planarized . For example, planarization can be done by chemical mechanical planarization (CPM). The planar topmost surface of planarization dielectric layer 60 is referred to herein as planar dielectric surface 63. After planarization, the topmost surface of the disposable gate cap portion (29A, 29B) is coplanar with the planar dielectric surface 63.

在第一和第二一次性栅极结构（23A、27A、29A、23B、27B、29B）的最顶表面之上，即，在第一和第二一次性栅极帽盖部分（29A、29B）的最顶表面上方，对平面化电介质层60和任何额外的电介质材料层（其包括存在的第一应力产生衬里、第二应力产生衬里和电介质衬里中的任一者）进行平面化。例如可以通过化学机械平面化（CPM）来进行平面化。平面化电介质层60的平面最顶表面在这里被称为平面电介质表面63。在平面化之后，一次性栅极帽盖部分（29A、29B）的最顶表面与平面电介质表面63共面。

The combination of the first source and drain extension region 14A, the first source and drain region 16A, and the first doped well 12A may be used to subsequently form a first field effect transistor. The combination of the second source and drain extension region 14B, the second source and drain region 16B, and the second doped well 12B may be used to subsequently form a second field effect transistor

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第一源极和漏极扩展区域14A、第一源极和漏极区域16A以及第一掺杂阱12A的组合可被用于随后形成第一场效应晶体管。第二源极和漏极扩展区域14B、第二源极和漏极区域16B以及第二掺杂阱12B的组合可被用于随后形成第二场效应晶体管

Referring to FIG. 5, the first disposable gate structure (23A, 27A, 29A) and the second disposable gate structure (23B, 27B, 29B) are removed by at least one etch. The first and second disposable gate structures (23A, 27A, 29A, 23B, 27B, 29B) may be removed, for example, by at least one etch that may include anisotropic etching, isotropic etching, or a combination thereof. The at least one etching may include dry etching and / or wet etching. The at least one etch that is used to remove the first and second disposable gate structures (23A, 27A, 29A, 23B, 27B, 29B) is preferably performed on the dielectric material of the planarization dielectric layer 60 and on the surface of the semiconductor substrate Any other dielectric material layer present above 8 is selective.

参考图5，通过至少一次蚀刻，去除第一一次性栅极结构（23A、27A、29A）和第二一次性栅极结构（23B、27B、29B）。例如可以通过可包括各向异性蚀刻、各向同性蚀刻或其组合的至少一次蚀刻，去除第一和第二一次性栅极结构（23A、27A、29A、23B、27B、29B）。所述至少一次蚀刻可以包括干法蚀刻和/或湿法蚀刻。被用于去除第一和第二一次性栅极结构（23A、27A、29A、23B、27B、29B）的所述至少一次蚀刻优选地对平面化电介质层60的电介质材料以及在半导体衬底8之上存在的任何其他电介质材料层具有选择性。

The first gate cavity 25A is formed in a volume from which the first disposable gate structure (23A, 27A, 29A) is removed and after the second disposable gate structure (23B , 27B, 29B), a second gate cavity 25B is formed. The semiconductor surface of the semiconductor substrate 8, ie, the top surface of the first doped well 12A, is exposed at the bottom of the first gate cavity 25A. The other semiconductor surface of the semiconductor substrate 8, that is, the top surface of the second doped well 12B is exposed at the bottom of the second gate chamber 25B. Each of the first and second gate cavities (25A, 25B) is laterally surrounded by a planarization dielectric layer 60. The first gate spacer 52A laterally surrounds the first gate cavity 25A and the second gate spacer 52B laterally surrounds the second gate cavity 25B. The inner sidewalls of the first gate spacer 52A may be substantially perpendicular and extend from the top surface of the first doped well 12A to the planar dielectric surface 63 of the planarization dielectric layer 60, ie, the topmost surface. In addition, the inner sidewalls of the second gate spacer 52B may be substantially perpendicular and extend from the top surface of the second doped well 12B to the planar dielectric surface 63 of the planarization dielectric layer 60.

在从其中去除了第一一次性栅极结构（23A、27A、29A）的体积（volume）中形成第一栅极腔25A，并在从其中去除了第二一次性栅极结构（23B、27B、29B）的体积中形成第二栅极腔25B。半导体衬底8的半导体表面，即，第一掺杂阱12A的顶表面被暴露在第一栅极腔25A的底部。半导体衬底8的另一半导体表面，即，第二掺杂阱12B的顶表面被暴露在第二栅极腔25B的底部。第一和第二栅极腔（25A、25B）中的每一者被平面化电介质层60侧向包围。第一栅极间隔物52A侧向包围第一栅极腔25A，且第二栅极间隔物52B侧向包围第二栅极腔25B。第一栅极间隔物52A的内侧壁可以基本垂直，并从第一掺杂阱12A的顶表面延伸到平面化电介质层60的平面电介质表面63，即，最顶表面。此外，第二栅极间隔物52B的内侧壁可以基本垂直，并从第二掺杂阱12B的顶表面延伸到平面化电介质层60的平面电介质表面63。

Referring to FIG. 6, a gate dielectric layer 32L is deposited on the bottom and sidewalls of the gate cavity (25A, 25B) and on the topmost surface of the planarization dielectric layer 60. The gate dielectric layer 32L may be a high dielectric constant (high-k) material layer having a dielectric constant greater than 3.9. The gate dielectric layer 32L may include a dielectric metal oxide, which is a high-k material containing metal and oxygen, and is known in the art as a high-k gate dielectric material. May be formed by any method known in the art including, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), molecular beam deposition (MBD), pulsed laser deposition (PLD), liquid source atomization chemical deposition (LSMCD)), And the like, to deposit the dielectric metal oxide. Exemplary high-k dielectric materials include HfO 2, ZrO 2, La 2 O 3, Al 2 O 3, TiO 2, SrTiO 3, LaAlO 3, Y 2 O 3, HfO x N y, ZrO x N y, La 2 O x N y, Al 2 O x N y, TiO x N y, SrTiO x N y, LaAlO x N y, Y 2 O x N y, silicates thereof, and alloys thereof. Each value of x is independently from 0.5 to 3, and each value of y is independently from 0 to 2. The thickness of the gate dielectric layer 32L measured at the horizontal portion may be from 0.9 nm to 6 nm, and preferably from 1.0 nm to 3 nm. The gate dielectric layer 32L may have an effective oxide thickness on the order of 2 nm or less. In one embodiment, the gate dielectric layer 32L is a hafnium oxide (HfO 2) layer.

参考图6，将栅极电介质层32L沉积在栅极腔（25A、25B）的底表面和侧壁上以及平面化电介质层

60的最顶表面上。栅极电介质层32L可以是具有大于3.9的介电常数的高介电常数（高k）材料层。栅极电介质层32L可以包括介电金属氧化物（其是包含金属和氧的高k材料），并在本领域中被已知为高k栅极电介质材料。可通过本领域中包括例如化学气相沉积（CVD）、物理气相沉积（PVD）、分子束沉积（MBD）、脉冲激光沉积（PLD）、液态源雾化化学沉积（LSMCD）、原子层沉积（ALD）等的众所周知的方法，来沉积介电金属氧化物。示例性高k电介质材料包括Hf0 2、ZrO 2、La 2 O 3、Al 2 O 3、TiO 2、SrTiO 3、LaAlO 3、Y 2 O 3、HfO x N y、ZrO x N y、La 2 O x N y、Al 2 O x N y、TiO x N y、SrTiO x N y、LaAlO x N y、Y 2 O x N y、其硅酸盐及其合金。x的每个值独立地为从0.5到3，且y的每个值独立地为从0到2。在水平部分处测量的栅极电介质层32L的厚度可以为从0.9nm到6nm，且优选地从1.0nm到3nm。栅极电介质层32L可以具有2nm量级或更小的有效氧化物厚度。在一个实施例中，栅极电介质层32L是氧化铪（Hf0 2）层。

A first work function material layer 34L comprising a first metal material is deposited, the first metal material having a first work function. The first work function material layer 34L may be a p-type work function material layer or an n-type work function material layer. As used herein, "p-type work function material" refers to a material having a work function between the valence band level of silicon and the mid-bandgap level of silicon that is the same as the valence band of silicon The energy level is equal to the energy level of the conduction band. As used herein, "n-type work function material" refers to a material having a work function between the conduction band level of silicon and the mid-band gap energy of silicon.

沉积包括第一金属材料的第一功函数材料层34L，该第一金属材料具有第一功函数。第一功函数材料层34L可以是p型功函数材料层或n型功函数材料层。这里所使用的“p型功函数材料”是指具有在硅的价带能级与硅的中间带隙能级之间的功函数的材料，该中间带隙能级即为与硅的价带能级和导带能级相等分隔的能级。这里所使用的“n型功函数材料”是指具有在硅的导带能级与硅的中间带隙能级之间的功函数的材料。

In one embodiment, the first work function material layer 34L is a conductive tantalum alloy layer. The conductive tantalum alloy layer may include a material selected from the group consisting of an alloy of tantalum and aluminum, an alloy of tantalum and carbon, and an alloy of tantalum, aluminum and carbon. A first example of a conductive tantalum alloy layer is a tantalum-aluminum alloy layer that includes an alloy of tantalum and aluminum. In tantalum and aluminum alloys, the atomic percentage of tantalum may be from 10% to 99%, and the atomic percentage of aluminum may be from 1% to 90%. The tantalum-aluminum alloy layer can consist essentially of tantalum and aluminum.

在一个实施例中，第一功函数材料层34L是导电钽合金层。该导电钽合金层可以包括选自钽和铝的合金、钽和碳的合金、以及钽、铝和碳的合金的材料。导电钽合金层的第一实例是钽-铝合金层，其包括钽和铝的合金。在钽和铝的合金中，钽的原子百分比可以为从10%到99%，且铝的原子百分比可以为从1%到90%。钽-铝合金层可以基本由钽和铝组成。

A second example of a conductive tantalum alloy layer is a tantalum carbide layer that includes an alloy of tantalum and carbon. In tantalum and carbon alloys, the atomic percentage of tantalum may be from 20% to 80%, and the atomic percentage of carbon may be from 20% to 80%. The tantalum carbide layer may consist essentially of tantalum and carbon.

导电钽合金层的第二实例是碳化钽层，其包括钽和碳的合金。在钽和碳的合金中，钽的原子百分比可以为从20%到80%，且碳的原子百分比可以为从20%到80%。碳化钽层可以基本由钽和碳组成。

A third example of a conductive tantalum alloy layer is a tantalum aluminum carbide layer that includes an alloy of tantalum, aluminum, and carbon. In tantalum, aluminum and carbon alloys, the atomic percentage of tantalum may be from 15% to 80%, the atomic percentage of aluminum may be from 1% to 60%, and the atomic percentage of carbon may be from 15% to 80%.

导电钽合金层的第三实例是碳化钽铝层，其包括钽、铝和碳的合金。在钽、铝和碳的合金中，钽的原子百分比可以为从15%到80%，铝的原子百分比可以为从1%到60%，且碳的原子百分比可以为从15%到80%。

In another embodiment, the first work function material layer 34L is a conductive metal nitride layer. For example, the first work function material layer 34L may be a titanium nitride layer consisting essentially of titanium nitride. In the titanium nitride layer, the atomic percentage of titanium may be from 30% to 90%, and the atomic percentage of nitrogen may be from 10% to 70%.

在另一实施例中，第一功函数材料层34L是导电金属氮化物层。例如，第一功函数材料层34L可以是基本由氮化钛组成的氮化钛层。在氮化钛层中，钛的原子百分比可以为从30%到90%，且氮的原子百分比可以为从10%到70%。

The first work function material layer 34L may be deposited by, for example, atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD). The first workfunction material layer 34L may or may not be conformal. In other words, the vertical portion of the first work function material layer 34L may or may not have the same thickness as the horizontal portion of the first work function material layer 34L. The thickness of the horizontal portion of the first work function material layer 34L at the bottoms of the first and second gate cavities (25A, 25B) may be from 1.0 nm to 10 nm, but smaller or larger thicknesses may also be employed.

第一功函数材料层34L例如可以通过原子层沉积（ALD）、物理气相沉积（PVD）或化学气相沉积（CVD）来沉积。第一功函数材料层34L可以是或可以不是保形的。换句话说，第一功函数材料层34L的垂直部分可以或可以不与第一功函数材料层34L的水平部分具有相同的厚度。第一功函数材料层34L的水平部分的在第一和第二栅极腔（25A、25B）的底部处的厚度可以为从1.0nm到10nm，但还

可以采用更小或更大的厚度。

Referring to FIG. 7, a photoresist 39 is applied and photolithographically patterned so that the photoresist 39 covers the area above the first doped well 12A while the first work function material layer 34L is over the second doped Above the trap 12B is exposed. The exposed portion of the first work function material layer 34L may be removed from the second gate cavity 25B by etching, which etching may be wet etching or dry etching. A portion of the gate dielectric layer 32L is physically exposed at the bottom and sidewalls of the second gate cavity 25B. For example, the photoresist 39 may be removed by ashing or wet etching.

参考图7，光致抗蚀剂39被施加并被光刻构图，以便光致抗蚀剂39覆盖位于第一掺杂阱12A之上的区域，而第一功函数材料层34L在第二掺杂阱12B之上暴露。可以通过蚀刻从第二栅极腔25B中去除第一功函数材料层34L的暴露部分，该蚀刻可以是湿法蚀刻或干法蚀刻。栅极电介质层32L的一部分在第二栅极腔25B的底部和侧壁处被物理暴露。例如可以通过灰化（ashing）或湿法蚀刻来去除光致抗蚀剂39。

Referring to FIG. 8, a second work function material layer 36L containing a second metal material having a second work function is deposited.

参考图8，沉积包含第二金属材料的第二功函数材料层36L，该第二金属材料具有第二功函数。

In one embodiment, the first work function material layer 34L is a conductive tantalum alloy layer and the second work function material layer 36L is a conductive metal nitride layer. For example, the second work function material layer 36L may be a titanium nitride layer consisting essentially of titanium nitride. In this titanium nitride layer, the atomic percentage of titanium may be from 30% to 90%, and the atomic percentage of nitrogen may be from 10% to 70%. A portion of the metal nitride layer is formed directly on the conductive tantalum alloy layer in the first gate cavity 25A.

在一个实施例中，第一功函数材料层34L是导电钽合金层，第二功函数材料层36L是导电金属氮化物层。例如，第二功函数材料层36L可以是基本由氮化钛组成的氮化钛层。在该氮化钛层中，钛的原子百分比可以为从30%到90%，且氮的原子百分比可以为从10%到70%。该金属氮化物层的一部分被直接形成在第一栅极腔25A中的导电钽合金层上。

In another embodiment, the first work function material layer 34L is a conductive metal nitride layer and the second work function material layer 36L is a conductive tantalum alloy layer. The conductive tantalum alloy layer may include a material selected from the group consisting of an alloy of tantalum and aluminum, an alloy of tantalum and carbon, and an alloy of tantalum, aluminum and carbon. The conductive tantalum alloy layer may be any of a tantalum aluminum alloy layer, a tantalum carbide layer and a tantalum aluminum carbide layer, each

of which may have the same composition as described above. A portion of the conductive tantalum alloy layer is formed directly on the metal nitride layer in the first gate cavity 25A.

在另一实施例中，第一功函数材料层34L是导电金属氮化物层，第二功函数材料层36L是导电钽合金层。导电钽合金层可以包括选自钽和铝的合金、钽和碳的合金、以及钽、铝和碳的合金的材料。导电钽合金层可以是钽铝合金层、碳化钽层和碳化钽铝层中的任一者，其中每一者可以具有与上述相同的组成。导电钽合金层的一部分被直接形成在第一栅极腔25A中的金属氮化物层上。

The second work function material layer 36L may be deposited by, for example, atomic layer deposition (ALD), physical vapor deposition (PVD), or chemical vapor deposition (CVD). The second work function material layer 36L may or may not be conformal. The thickness of the horizontal portion of the second work function material layer 36L at the bottoms of the first and second gate cavities (25A, 25B) may be from 1.0 nm to 50 nm, although a smaller or larger thickness may also be employed.

第二功函数材料层36L例如可以通过原子层沉积（ALD）、物理气相沉积（PVD）或化学气相沉积（CVD）来沉积。第二功函数材料层36L可以是或可以不是保形的。第二功函数材料层36L的水平部分的在第一和第二栅极腔（25A、25B）的底部处的厚度可以为从1.0nm到50nm，但还可以采用更小或更大的厚度。

Thus, the first work function material layer 34L is formed directly on the first portion of the gate dielectric layer 32L located in the first gate cavity 25A, and directly in the second gate cavity 25B of the gate dielectric layer 32L A second work function material layer 36L is formed on the second portion. One of the first and second work function material layers (34L, 36L) is a conductive tantalum alloy layer and the other of the first and second work function material layers (34L, 36L) is a metal nitride layer.

由此，直接在栅极电介质层32L的位于第一栅极腔25A中的第一部分上形成第一功函数材料层34L，且直接在栅极电介质层32L的位于第二栅极腔25B中的第二部分上形成第二功函数材料层36L。第一和第二功函数材料层（34L、36L）中的一者是导电钽合金层，且第一和第二功函数材料层（34L、36L）中的另一者是金属氮化物层。

Referring to FIG. 9, the gate cavities (25A, 25B) are filled with the conductive material layer 40L. The conductive material layer 40L is formed directly on the tungsten barrier layer 38L. The conductive material layer 40L includes a metal that can be deposited by physical vapor deposition or chemical vapor deposition. For example, the conductive material layer 40L may be an aluminum layer or a tungsten layer or an aluminum alloy layer or a tungsten alloy layer deposited by physical vapor deposition. The thickness of the conductive material layer 40L measured in the planar region of the conductive material layer 40L above the top surface of the planarization dielectric layer 60 may be from 100 nm to 500 nm, but a smaller or larger thickness may also be employed. In one embodiment, the conductive material layer 40L may include at least one material selected from the group

consisting of W and Al. In addition, the conductive material layer 40L may basically consist of a single elemental metal such as W or Al.

参考图9，用导电材料层40L来填充栅极腔（25A、25B）。直接在钨阻挡层38L上形成导电材料层40L。导电材料层40L包括可以通过物理气相沉积或化学气相沉积来沉积的金属。例如，导电材料层40L可以是通过物理气相沉积来沉积的铝层或钨层或者铝合金层或钨合金层。在导电材料层40L的位于平面化电介质层60的顶表面上方的平面区域中测量的导电材料层40L的厚度可以为从100nm到500nm，但还可以采用更小或更大的厚度。在一个实施例中，导电材料层40L可以包括选自W和Al的至少一种材料。此外，导电材料层40L可以基本上由诸如W或Al的单种元素金属组成。

Referring to FIG. 10, the conductive material layer 40L, the second work function material layer 36L, the first work function material layer 34L and the gate dielectric layer 32L are planarized, for example, by chemical mechanical planarization. Specifically, the conductive material layer 40L, the second work function material layer 36L, the first work function material layer 34L, and the gate dielectric layer 32L are removed from above the planar dielectric surface 63 of the planarization dielectric layer 60 at the end of the planarization step part. The remaining portion of the gate dielectric layer 32L in the first device region forms the first gate dielectric 32A and the remaining portion of the gate dielectric layer 32L in the second device region forms the second gate dielectric 32B. The remaining portion of the first work function material layer 34L located in the first device region forms the first work function material portion 34. The remaining portion of the second work function material layer 36L in the first device region forms a second work function material portion 36A. The remaining portion of the second work function material layer 36L located in the second device region forms the work function material portion 36B. The remaining portion of the conductive material layer 40L in the first device region constitutes the first metal portion 40A and the remaining portion of the conductive material layer in the second device region constitutes the second metal portion 40B. The first and second gate dielectrics (32A, 32B), the first and second work function material portions (34, 36A), the work function material portion 36B, and the topmost of the first and second metal portions (40A, 40B) The surface is coplanar with the topmost surface of the planarization dielectric layer 60.

参考图10，例如通过化学机械平面化来对导电材料层40L、第二功函数材料层36L、第一功函数材料层34L和栅极电介质层32L进行平面化。具体地，在平面化步骤结束时，从平面化电介质层60的平面电介质表面63上方去除了导电材料层40L、第二功函数材料层36L、第一功函数材料层34L和栅极电介质层32L的部分。栅极电介质层32L的位于第一器件区域中的剩余部分形成第一栅极电介质32A，且栅极电介质层32L的位于第二器件区域中的剩余部分形成第二栅极电介质32B。第一功函数材料层34L的位于第一器件区域中的剩余部分形成第一功函数材料部分34。第二功函数材料层36L的位于第一器件区域中的剩余部分形成第二功函数材料部分36A。第二功函数材料层36L的位于第二器件区域中的剩余部分形成功函数材料部分36B。导电材料层40L的位于第一器件区域中的剩余部分构成第一金属部分40A，且导电材料层的位于第二器件区域中的剩余部分构成第二金属部分40B。第一和第二栅极电介质（32A、32B）、第一和第二功函数材料部分（34、36A）、功函数材料部分36B以及第一和第二金属部分（40A、40B）的最顶表面与平面化电介质层60的最顶表面共面。

As such, the replacement gate stack was previously formed in the volume occupied by the first and second gate cavities (25A, 25B) in the step of FIG. 6. The replacement gate stack includes a first replacement gate stack 230A in the first device region and a second replacement gate stack 230B in the second device region. Each replacement gate stack (230A, 230B) overlies the channel region of the field effect transistor. The first replacement gate stack 230A and the second replacement gate stack 230B are formed simultaneously.

由此，之前在图6的步骤中被第一和第二栅极腔（25A、25B）占据的体积中形成替换栅极叠层。该替换栅极叠层包括位于第一器件区域中的第一替换栅极叠层230A以及位于第二器件区域中的第二替换栅极叠层230B。每一个替换栅极叠层（230A、230B）覆盖在场效应晶体管的沟道区域上。第一替换栅极叠层230A和第二替换栅极叠层230B被同时形成。

A first field effect transistor is formed in the first device region. The first field effect transistor includes a first doped well 12A, a first source / drain extension region 14A, a first source / drain region 16A, a first metal semiconductor alloy portion 46A, a first replacement gate Stack 230A and first gate spacer 52A. The first replacement gate stack 230A includes a first gate dielectric 32A, a first work function material portion 34, a second work function material portion 36A, and a first metal portion 40A.

在第一器件区域中形成第一场效应晶体管。第一场效应晶体管包括第一掺杂阱12A、第一源极扩展区域/漏极扩展区域14A、第一源极区域/漏极区域16A、第一金属半导体合金部分46A、第一替换栅极叠层230A和第一栅极间隔物52A。第一替换栅极叠层230A包括第一栅极电介质32A、第一功函数材料部分34、第二功函数材料部分36A和第一金属部分40A。

A second field effect transistor is formed in the second device region. The second field effect transistor includes a second doped well 12B, a second source / drain extension region 14B, a second source / drain region 16B, a second metal semiconductor alloy portion 46B, a second replacement gate Stack 230B and second gate spacer 52B. The second replacement gate stack 230B includes a second gate dielectric 32B, a work function material portion 36B, and a second metal portion 40B. The second work function material portion 36A in the first replacement gate stack 230A and the work function material portion 36B in the second replacement gate stack 230B have the same material composition and the same thickness.

在第二器件区域中形成第二场效应晶体管。第二场效应晶体管包括第二掺杂阱12B、第二源极扩展区域/漏极扩展区域14B、第二源极区域/漏极区域16B、第二金属半导体合金部分46B、第二替换栅极叠层230B和第二栅极间隔物52B。第二替换栅极叠层230B包括第二栅极电介质32B、功函数材料部分36B和第二金属部分40B。第一替换栅极叠层230A中的第二功函数材料部分36A和第二替换栅极叠层230B中的功函数材料部分36B具有相同的材料组成和相同的厚度。

Each of the first and second field effect transistors is a planar field effect transistor having a channel underlying a

topmost surface of the semiconductor substrate. One of the first and second field effect transistors includes a gate electrode that includes a conductive tantalum alloy layer and is in contact with the gate dielectric. The other of the first and second field effect transistors includes another gate electrode that includes a metal nitride layer and is in contact with another gate dielectric.

第一和第二场效应晶体管中的每一者是平面场效应晶体管，其具有位于半导体衬底的最顶表面下方的沟道。第一和第二场效应晶体管中的一者包括这样的栅极电极：该栅极电极包括导电钽合金层并与栅极电介质接触。第一和第二场效应晶体管中的另一者包括另一栅极电极，该栅极电极包含金属氮化物层并与另一栅极电介质接触。

In one embodiment, one of the first gate electrode and the second gate electrode may have a first work function that is closer to the conduction band of silicon than the mid-bandgap energy level of silicon, and the The other one of the gate electrode and the second gate electrode may have a second work function that is closer to the valence band of silicon than the mid-bandgap energy level of silicon.

在一个实施例中，第一栅极电极和第二栅极电极中的一者可以具有第一功函数，该第一功函数比硅的中间带隙能级更靠近硅的导带，且第一栅极电极和第二栅极电极中的另一者可以具有第二功函数，该第二功函数比硅的中间带隙能级更靠近硅的价带。

The first gate electrode 230A includes a first conductive material portion 40A in contact with a second work function material portion 36A, which is one of a metal nitride layer and a conductive tantalum alloy layer. The second gate electrode 230B includes a second conductive material portion 40B in contact with the other one of the metal nitride layer and the conductive tantalum alloy layer. The second conductive material portion 40B may have the same composition as the first conductive material portion 40A.

第一栅极电极230A包括与第二功函数材料部分36A接触的第一导电材料部分40A，该第二功函数材料部分36A是金属氮化物层和导电钽合金层中的一者。第二栅极电极230B包括与金属氮化物层和导电钽合金层中的另一者接触的第二导电材料部分40B。第二导电材料部分40B可以具有与第一导电材料部分40A相同的组成。

In one embodiment, the second gate electrode 230B includes a conductive tantalum alloy layer as the work function material portion 36B and the first gate electrode 230A includes another conductive tantalum alloy having the same composition and thickness as the conductive tantalum alloy layer Layer as the second work function material portion 36A. The conductive tantalum alloy layer in the first gate electrode 230A is in contact with the metal nitride layer in the first gate electrode 230A, ie, the first work function material portion 34, and is in contact with the first conductive material portion 40A. The conductive tantalum alloy layer is in contact with the second conductive material portion 40B having the same composition as the first conductive material portion 40A.

在一个实施例中，第二栅极电极230B包括导电钽合金层作为功函数材料部分36B，且第一栅极电极230A包括具有与该导电钽合金层相同的组成和厚度的另一导电钽合金层作为第二功函数材料部分36A。第一栅极电极230A中的导电钽合金层与第一栅极电极230A中的金属氮化物层即第一功函数材料部分34接触，并与第一导电材料部分40A接触。该导电钽合金层与第二导电材料部分40B接触，该第二导电材料部分40B具有与第一导电材料部分40A相同的组成。

In another embodiment, the second gate electrode 230B includes a metal nitride layer that is a work function material portion 36B, and the first gate electrode 230A includes another metal nitrogen having the same composition and thickness as the metal nitride layer Layer as the second work function material portion 36A. The metal nitride layer in the first gate electrode 230A is in contact with the first work function material portion 34, which is a conductive tantalum alloy layer in the first gate electrode 230A, and is in contact with the first conductive material portion 40A. The conductive tantalum alloy layer is in contact with the second conductive material portion 40B having the same composition as the first conductive material portion 40A.

在另一实施例中，第二栅极电极230B包括金属氮化物层为功函数材料部分36B，且第一栅极电极230A包括具有与该金属氮化物层相同的组成和厚度的另一金属氮化物层作为第二功函数材料部分36A。第一栅极电极230A中的金属氮化物层与第一栅极电极230A中的导电钽合金层即第一功函数材料部分34接触，并与第一导电材料部分40A接触。该导电钽合金层与第二导电材料部分40B接触，该第二导电材料部分40B具有与第一导电材料部分40A相同的组成。

Each of the first and second gate dielectrics (32A, 32B) is a U-shaped gate dielectric including a horizontal gate dielectric portion and a vertical gate dielectric portion extending upwardly from a peripheral region of the horizontal gate dielectric portion . In the first field-effect transistor, the first work function material portion 34 is in contact with the inner sidewall of the vertical gate dielectric portion of the first gate dielectric 32A. In the second field-effect transistor, the work function material portion 36B is in contact with the inner sidewall of the vertical gate dielectric portion of the second gate dielectric 32B. Each U-shaped gate dielectric is on the semiconductor substrate 8 and is buried in the planarization dielectric layer 60.

第一和第二栅极电介质（32A、32B）中的每一者是U形栅极电介质，其包括水平栅极电介质部分以及从水平栅极电介质部分的周边区域向上延伸的垂直栅极电介质部分。在第一场效应晶体管中，第一功函数材料部分34与第一栅极电介质32A的垂直栅极电介质部分的内侧壁接触。在第二场效应晶体管中，功函数材料部分36B与第二栅极电介质32B的垂直栅极电介质部分的内侧壁接触。每一个U形栅极电介质位于半导体衬底8上并被掩埋在平面化电介质层60中。

As the U-shaped gate dielectric, each of the gate dielectrics (32A, 32B) includes a horizontal gate dielectric portion and a vertical gate dielectric portion. The vertical gate dielectric portion extends continuously from the horizontal gate dielectric portion to the topmost surface of the planarization dielectric layer 60.

作为U形栅极电介质，每一个栅极电介质（32A、32B）包括水平栅极电介质部分和垂直栅极电介质部分。垂直栅极电介质部分从水平栅极电介质部分连续地延伸到平面化电介质层60的最顶表面。

If the second work function material portion 36A and the work function material portion 36B include a metal nitride, each of the first and second conductive material portions (40A, 40B) contacts a portion of the metal nitride layer when formed. If the second work function material portion 36A and the work function material portion 36B include a conductive tantalum alloy, each of the first and second conductive material portions (40A, 40B) contacts a portion of the conductive tantalum alloy layer when formed.

如果第二功函数材料部分36A和功函数材料部分36B包括金属氮化物，则第一和第二导电材料部分（40A、40B）中的每一者在形成时接触金属氮化物层的一部分。如果第二功函数材料部分36A和功函数材料部分36B包括导电钽合金，则第一和第二导电材料部分（40A、40B）中的每一者在形成时接触导电钽合金层的一部分。

Referring to FIG. 11, a contact-level dielectric layer 70 is deposited over the planarization dielectric layer 60. For example, contact vias may be formed by a combination of photolithographic patterning and anisotropic etching, followed by planarization of the metal deposition and removal of excess portions of the metal from above the contact-level dielectric layer 70 to form various contact vias structure. Various contact via structures may include, for example, first source contact via / drain contact via structures (ie, at least one first source contact via structure and at least one first drain contact via structure) 66A , A second source contact via structure / drain contact via structure (ie, at least one second source contact via structure and at least one second drain contact via structure) 66B, a first gate contact via The structure 68A and the second gate contact via structure 68B. Each of the source contact via structures (66A, 66B) and each of the drain contact via structures (66A, 66B) are buried in the planarization dielectric layer 60 and the contact level dielectric material layer 70. Each of the source contact via structures (one of 66A and 66B) contacts the source side metal semiconductor alloy portion (one of 46A and 46B), and each of the drain contact via structures (66A and 66B)) Contacts the drain-side metal semiconductor alloy portion (the other of 46A and 46B).

参考图11，在平面化电介质层60之上沉积接触级电介质层70。例如，可以通过光刻图形形成和各向异性蚀刻的组合而形成接触过孔腔，然后进行金属沉积和从接触级电介质层70上方去除金属的过量部分的平面化，来形成各种接触过孔结构。各种接触过孔结构可以包括例如第一源极接触过孔结构/漏极接触过孔结构（即，至少一个第一源极接触过孔结构和至少一个第一漏极接触过孔结构）66A、第二源极接触过孔结构/漏极接触过孔结构（即，至少一个第二源极接触过孔结构和至少一个第二漏极接触过孔结构）66B、第一栅极接触过孔结构68A和第二栅极接触过孔结构68B。每一个源极接触过孔结构（66A、66B）和每一个漏极接触过孔结构（66A、66B）被掩埋在平面化电介质层60和接触级电介质材料层70中。每一个源极接触过孔结构（66A和66B中的一个）接触源极侧金属半导体合金部分（46A和46B中的一个），且每一个漏极接触过孔结构（66A和66B中的另一个）接触漏极侧金属半导体合金部分（46A和46B中的另一个）。

Referring to FIG. 12, a second exemplary semiconductor structure may be formed, for example, by patterning a semiconductor-on-insulator (SOI) substrate. Specifically, an SOI substrate including a top semiconductor layer, a buried insulator layer 120, and a handle substrate 10 'is provided. The top semiconductor layer is patterned to form a first semiconductor fin in the first device region and a second semiconductor fin in the second device region.

参考图12，可以例如通过对绝缘体上半导体（SOI）衬底进行构图，来形成第二示例性半导体结构。具体地，提供包括顶部半导体层、掩埋绝缘体层120、以及处理衬底（handle substrate）10’的SOI衬底。顶部半导体层被构图为形成第一器件区域中的第一半导体鳍和第二器件区域中的第二半导体鳍。

Using the same method as in the first embodiment, a one-time gate stack is formed on the first and second semiconductor fins. In addition, a first source extension region / drain extension region 14 'is formed in the first semiconductor fin and a second source extension region / drain extension region 14B' is formed in the second semiconductor fin. A first gate spacer 52A is formed around the first disposable gate structure (23A, 27A, 29A) and a second gate is formed around the second disposable gate structure (23B, 27B, 29B) Pole spacer 52B. A first source and drain region 16A 'is formed in the first semiconductor fin using the first disposable gate structure (23A, 27A, 29A) and the first gate spacer 52A as part of an implantation mask. A second source and drain region 16A 'is formed in the second semiconductor fin using the second disposable gate structure (23B, 27B, 29B) and the second gate spacer 52B as part of an implantation mask. The non-implanted portion of the semiconductor material in each semiconductor fin constitutes a first body portion 12A 'and a second body portion 12B'. Various metal semiconductor alloy portions (46A ', 46B') may be formed on the first and second source and drain regions (16A ', 16B') using the same processing method as in the first embodiment.

使用与第一实施例中相同的方法，在第一和第二半导体鳍上形成一次性栅极叠层。此外，在第一半导体鳍中形成第一源极扩展区域/漏极扩展区域14’，并在第二半导体鳍中形成第二源极扩展区域/漏极扩展区域14B’。在第一一次性栅极结构（23A、27A、29A）的周围形成第一栅极间隔物52A，并在第二一次性栅极结构（23B、27B、29B）的周围形成第二栅极间隔物52B。使用第一一次性栅极结构（23A、27A、29A）和第一栅极间隔物52A作为注入掩膜的部分，在第一半导体鳍中形成第一源极和漏极区域16A’。使用第二一次性栅极结构（23B、27B、29B）和第二栅极间隔物52B作为注入掩膜的部分，在第二半导体鳍中形成第二源极和漏极区域16A’。每个半导体鳍中的半导体材料的未注入部分构成第一主体部分12A’和第二主体部分12B’。可以使用与第一实施例中相同的处理方法，在第一和第二源极和漏极区域（16A’、16B’）上形成各种金属半导体合金部分（46A’、46B’）。

Referring to FIG. 13, a planarization dielectric layer 60 is deposited over the semiconductor fin, the disposable gate structure, and the buried insulator layer 120 using the same processing steps as in the first embodiment, ie,

the processing steps of FIG. 4.

参考图13，使用与第一实施例中相同的处理步骤，即，图4的处理步骤，将平面化电介质层60沉积在半导体鳍、一次性栅极结构和掩埋绝缘体层120之上。

Referring to FIGS. 14 and 15, the same processing steps as in the first embodiment may be performed to form the second exemplary semiconductor structure illustrated in FIGS. 14 and 15. The second exemplary semiconductor structure includes, in addition to each of the first and second field-effect transistors, a fin field-effect transistor having a channel pair located directly on a sidewall portion of the semiconductor fin, The first exemplary semiconductor structure has the same features.

参考图14和15，可以执行与第一实施例中相同的处理步骤，来形成图14和15中示例的第二示例性半导体结构。除了所述第一和第二场效应晶体管中的每一者是具有直接位于半导体鳍的侧壁部分上的沟道对的鳍场效应晶体管之外，第二示例性半导体结构包括与图11的第一示例性半导体结构相同的特征。

Referring to FIG. 16, the photoresist 37 is then patterned to cover the area of the second gate cavity 25B (see FIG. 8) by applying the photoresist 37 over the first exemplary structure of FIG. 8, Without covering the region of the first gate cavity 25A, the third exemplary semiconductor structure according to the third embodiment of the present disclosure is obtained from the first exemplary semiconductor structure of FIG. 8. The physically exposed portion of the second work function material layer 36L may be removed by etching, which etching may be wet etching or dry etching. The photoresist 37 is then removed.

参考图16，通过将光致抗蚀剂37施加到图8的第一示例性结构之上、随后对光致抗蚀剂37进行构图以覆盖第二栅极腔25B的区域（见图8）而不覆盖第一栅极腔25A的区域，从图8的第一示例性半导体结构得到根据本公开的第三实施例的第三示例性半导体结构。可以通过蚀刻来去除第二功函数材料层36L的物理暴露部分，该蚀刻可以是湿法蚀刻或干法蚀刻。随后去除光致抗蚀剂37。

Referring to FIG. 17, a conductive material layer 40L is deposited in the first and second gate cavities (25A, 25B). The conductive material layer 40L may have the same composition and thickness as in the first embodiment, and may be deposited using the same process steps as in the first embodiment.

参考图17，将导电材料层40L沉积在第一和第二栅极腔（25A、25B）中。导电材料层40L可以具有与第一实施例中相同的组成和厚度，并可以采用与第一实施例中相同的处理步骤来沉积。

Referring to FIG. 18, the conductive material layer 40L, the second work function material layer 36L, the first work function material layer 34L, and the gate dielectric layer 32L are planarized, for example, by chemical

mechanical planarization. The same processing steps as in the first embodiment can be used for the planarization.

参考图18，例如通过化学机械平面化来对导电材料层40L、第二功函数材料层36L、第一功函数材料层34L以及栅极电介质层32L进行平面化。与第一实施例中相同的处理步骤可被用于平面化。

Specifically, at the end of the planarization step, the conductive material layer 40L, the second work function material layer 36L, the first work function material layer 34L, and the gate dielectric layer 32L are removed from above the planar dielectric surface 63 of the planarization dielectric layer 60 part. The remaining portion of the gate dielectric layer 32L in the first device region forms the first gate dielectric 32A and the remaining portion of the gate dielectric layer 32L in the second device region forms the second gate dielectric 32B. The remaining portion of the first work function material layer 34L located in the first device region forms the first work function material portion 34 '. The remaining portion of the second work function material layer 36L in the second device region forms a second work function material portion 36 '. The remaining portion of the conductive material layer 40L in the first device region constitutes the first metal portion 40A and the remaining portion of the conductive material layer in the second device region constitutes the second metal portion 40B. The first and second gate dielectrics (32A, 32B), the first and second work function material portions (34, 36A), the work function material portion 36B, and the topmost of the first and second metal portions (40A, 40B) The surface is coplanar with the topmost surface of the planarization dielectric layer 60.

具体地，在平面化步骤结束时，从平面化电介质层60的平面电介质表面63上方去除了导电材料层40L、第二功函数材料层36L、第一功函数材料层34L以及栅极电介质层32L的部分。栅极电介质层32L的位于第一器件区域中的剩余部分形成第一栅极电介质32A，且栅极电介质层32L的位于第二器件区域中的剩余部分形成第二栅极电介质32B。第一功函数材料层34L的位于第一器件区域中的剩余部分形成第一功函数材料部分34'。第二功函数材料层36L的位于第二器件区域中的剩余部分形成第二功函数材料部分36'。导电材料层40L的位于第一器件区域中的剩余部分构成第一金属部分40A，且导电材料层的位于第二器件区域中的剩余部分构成第二金属部分40B。第一和第二栅极电介质（32A、32B）、第一和第二功函数材料部分（34、36A）、功函数材料部分36B以及第一和第二金属部分（40A、40B）的最顶表面与平面化电介质层60的最顶表面共面。

After the first conductive material portion 40A is formed, the first work function material layer, ie, the first work function material portion 34 ', is in contact with the first portion of the gate dielectric layer 32L. After the second conductive material portion 40B is formed, the second work function material layer, ie, the second work function material portion 36 ', is in contact with the second portion of the gate dielectric layer 32L.

在形成第一导电材料部分40A之后，第一功函数材料层，即，第一功函数材料部分34'与栅极电介质层32L的第一部分接触。在形成第二导电材料部分40B之后，第二功函数材料层，即，第二功函数材料部分36'与栅极电介质层32L的第二部分接触。

Referring to FIG. 19, a contact via cavity may be formed, for example, by a combination of photolithographic patterning and anisotropic etching, followed by metal deposition and planarization of an excess portion for removing the metal from above the contact-level dielectric layer 70 to form a contact Grade dielectric layer 70 and various contact via structures (66A, 66B, 68A, 68B).

参考图19，可以例如通过光刻构图和各向异性蚀刻的组合而形成接触过孔腔，然后进行金属沉积和用于从接触级电介质层70上方去除金属的过量部分的平面化，来形成接触级电介质层70和各种接触过孔结构（66A、66B、68A、68B）。

Referring to FIG. 20, the process according to the present disclosure may be obtained from the second exemplary semiconductor structure of FIG. 13 by performing the process steps of FIGS. 5-8 of the first embodiment and the process steps of FIGS. 16-19 of the third embodiment, Fourth Exemplary Semiconductor Structure of Four Embodiments. The fourth exemplary semiconductor structure includes, in addition to each of the first and second field-effect transistors, a fin field-effect transistor having a channel pair directly on a sidewall portion of the semiconductor fin, The third exemplary semiconductor structure has the same features.

参考图20，可以通过执行第一实施例的图5-8的处理步骤和第三实施例的图16-19的处理步骤，来从图13的第二示例性半导体结构得到根据本公开的第四实施例的第四示例性半导体结构。除了所述第一和第二场效应晶体管中的每一者是具有直接位于半导体鳍的侧壁部分上的沟道对的鳍场效应晶体管之外，第四示例性半导体结构包括与图19的第三示例性半导体结构相同的特征。

Although the present disclosure has been described in terms of specific embodiments, it will be apparent to those skilled in the art that various substitutions, modifications, and variations are apparent in view of the foregoing description. Each of the various embodiments of the present disclosure may be implemented alone or in combination with any other embodiment of the present disclosure, unless expressly disclosed otherwise or otherwise impossible to one of ordinary skill in the art. Accordingly, the disclosure is intended to embrace all such alternatives, modifications and variations that fall within the scope and spirit of the disclosure and the following claims.

尽管关于具体实施例描述了本公开，但考虑到上述描述很明显的是，对于本领域技术人员来说，多种替代、修改和变化将是显然的。本公开的各种实施例的每一者可以被单独或者与本公开的任何其他实施例组合来实现，除非另外明确地公开或者据本领域普通技术人员所知是不可能的。因此，本公开旨在包含落在本公开和以下权利要求的范围和精神内的所有这样的替代、修改和变化。

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CLAIMS CN103258823

1.

A semiconductor structure including at least two field effect transistors, the semiconductor structure comprising:

一种包括至少两个场效应晶体管的半导体结构，所述半导体结构包括：

A first field effect transistor including a first gate dielectric and a first gate electrode, wherein the first gate electrode includes a conductive tantalum alloy layer in contact with the first gate dielectric; and

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第一场效应晶体管，其包括第一栅极电介质和第一栅极电极，其中，所述第一栅极电极包括与所述第一栅极电介质接触的导电钽合金层；以及

A second field effect transistor including a second gate dielectric and a second gate electrode, wherein the second gate electrode includes a metal nitride layer in contact with the second gate dielectric.

第二场效应晶体管，其包括第二栅极电介质和第二栅极电极，其中，所述第二栅极电极包括与所述第二栅极电介质接触的金属氮化物层。

2.

The semiconductor structure of claim 1, wherein the first gate electrode comprises a portion of a first conductive material in contact with one of the metal nitride layer and the conductive tantalum alloy layer.

如权利要求1所述的半导体结构，其中，所述第一栅极电极包括与所述金属氮化物层和所述导电钽合金层中的一者接触的第一导电材料部分。

3.

The semiconductor structure of claim 2, wherein the first gate electrode has a first work function and the second gate electrode has a second work function, the first work function being smaller than a middle work of the silicon The gap energy level is closer to the conduction band of silicon, which is closer to the valence band of silicon than the intermediate bandgap level of the silicon.

如权利要求2所述的半导体结构，其中，所述第一栅极电极具有第一功函数，且所述第二栅极电极具有第二功函数，所述第一功函数比硅的中间带隙能级更靠近硅的导带，所述第二功函数比所述硅的中间带隙能级更靠近硅的价带。

4.

The semiconductor structure of claim 2, wherein the second gate electrode includes a second conductive material portion that contacts the other of the metal nitride layer and the conductive tantalum alloy layer And has the same composition as the first conductive material portion.

如权利要求2所述的半导体结构，其中，所述第二栅极电极包括第二导电材料部分，所述第二导电材料部分接触所述金属氮化物层和所述导电钽合金层中的另一者并具有与所述第一导电材料部分相同的组成。

5.

The semiconductor structure of claim 2, wherein the second gate electrode comprises the conductive tantalum alloy layer, and the first gate electrode comprises a semiconductor layer having the same composition and thickness as the conductive tantalum alloy layer Another conductive tantalum alloy layer wherein the other conductive tantalum alloy layer is in contact with the metal nitride layer and the first conductive material portion and the conductive tantalum alloy layer is in contact with the second conductive material portion, The second conductive material portion has the same composition as the first conductive material portion.

如权利要求2所述的半导体结构，其中，所述第二栅极电极包括所述导电钽合金层，且所述第一栅极电极包括具有与所述导电钽合金层相同的组成和厚度的另一导电钽合金层，其中，所述另一导电钽合金层与所述金属氮化物层以及所述第一导电材料部分接触，且所述导电钽合金层与第二导电材料部分接触，所述第二导电材料部分具有与所述第一导电材料部分相同的组成。

6.

The semiconductor structure of claim 2, wherein the second gate electrode includes the metal nitride layer, and the first gate electrode includes a metal layer having a same composition and thickness as the metal nitride layer Another metal nitride layer wherein the other metal nitride layer is in contact with the conductive tantalum alloy layer and the first conductive material portion and the conductive tantalum alloy layer is in contact with the

second conductive material portion, The second conductive material portion has the same composition as the first conductive material portion.

如权利要求2所述的半导体结构，其中，所述第二栅极电极包括所述金属氮化物层，且所述第一栅极电极包括具有与所述金属氮化物层相同的组成和厚度的另一金属氮化物层，其中，所述另一金属氮化物层与所述导电钽合金层以及所述第一导电材料部分接触，且所述导电钽合金层与第二导电材料部分接触，所述第二导电材料部分具有与所述第一导电材料部分相同的组成。

7.

The semiconductor structure of claim 1, wherein the conductive tantalum alloy layer comprises a material selected from the group consisting of an alloy of tantalum and aluminum, an alloy of tantalum and carbon, and an alloy of tantalum, aluminum and carbon.

如权利要求1所述的半导体结构，其中，所述导电钽合金层包括选自钽和铝的合金、钽和碳的合金、以及钽、铝和碳的合金的材料。

8.

The semiconductor structure of claim 1, wherein the conductive tantalum alloy layer comprises an alloy of tantalum and aluminum, wherein tantalum has an atomic percentage of from 10% to 99% in the alloy of tantalum and aluminum, and The atomic percentage of aluminum is from 1% to 90%.

如权利要求1所述的半导体结构，其中，所述导电钽合金层包括钽和铝的合金，其中，在所述钽和铝的合金中，钽的原子百分比为从10%到99%，且铝的原子百分比为从1%到90%。

9.

The semiconductor structure of claim 1, wherein the conductive tantalum alloy layer comprises an alloy of tantalum and carbon, wherein tantalum has an atomic percentage of from 20% to 80% in the alloy of tantalum and carbon, and The atomic percentage of carbon is from 20% to 80%.

如权利要求1所述的半导体结构，其中，所述导电钽合金层包括钽和碳的合金，其中，在所述钽和碳的合金中，钽的原子百分比为从20%到80%，且碳的原子百分比为从20%到80%。

10.

The semiconductor structure of claim 1, wherein the conductive tantalum alloy layer comprises an alloy of tantalum, aluminum and carbon, wherein in the alloy of tantalum, aluminum and carbon, the atomic percentage of tantalum is from 15% to 80%, the atomic percentage of aluminum is from 1% to 60%, and the atomic percentage of carbon is from 15% to 80%.

如权利要求1所述的半导体结构，其中，所述导电钽合金层包括钽、铝和碳的合金，其中，在所述钽、铝和碳的合金中，钽的原子百分比为从15%到80%，铝的原子百分比为从1%到60%，且碳的原子百分比为从15%到80%。

11.

The semiconductor structure of claim 1, wherein the first and second portions of conductive material include at least one of W and Al.

如权利要求1所述的半导体结构，其中，所述第一和第二导电材料部分包括W和Al中的至少一种。

12.

The semiconductor structure of claim 1, wherein the first gate dielectric comprises a first U-shaped gate dielectric portion comprising a first gate dielectric vertical portion and a first A gate dielectric horizontal portion, the second gate dielectric comprises a second U-shaped gate dielectric portion and the second U-shaped gate dielectric portion comprises a second gate dielectric vertical portion and a second gate dielectric horizontal portion.

如权利要求1所述的半导体结构，其中，所述第一栅极电介质包括第一U形栅极电介质部分，所述第一U形栅极电介质部分包括第一栅极电介质垂直部分和第一栅极电介质水平部分，所述第二栅极电介质包括第二U形栅极电介质部分，所述第二U形栅极电介质部分包括第二栅极电介质垂直部分和第二栅极电介质水平部分。

13.

The semiconductor structure of claim 12, wherein the first and second gate dielectrics comprise a dielectric material having a dielectric constant greater than 3.9.

如权利要求12所述的半导体结构，其中，所述第一和第二栅极电介质包括具有大于3.9的介电常数的电介质材料。

14.

The semiconductor structure of claim 1, wherein each of the first and second field effect transistors is a planar field effect transistor having a channel under a topmost surface of the semiconductor substrate.

如权利要求1所述的半导体结构，其中，所述第一和第二场效应晶体管中的每一者是平面场效应晶体管，其具有位于半导体衬底的最顶表面之下的沟道。

15.

The semiconductor structure of claim 1, wherein each of the first and second field effect transistors is a fin field effect transistor having a pair of channels located directly on sidewall portions of the semiconductor fin.

如权利要求1所述的半导体结构，其中，所述第一和第二场效应晶体管中的每一者是鳍场效应晶体管，其具有直接位于半导体鳍的侧壁部分上的沟道对。

16.

A method of forming a semiconductor structure, the method comprising:

一种形成半导体结构的方法，所述方法包括：

Forming a first gate cavity and a second gate cavity over a semiconductor portion, wherein each of the first gate cavity and the second gate cavity is laterally surrounded by a planarization dielectric layer, wherein A top surface of the semiconductor portion is exposed at a bottom of each of the first and second gate cavities;

在半导体部分之上形成第一栅极腔和第二栅极腔，其中，所述第一栅极腔和所述第二栅极腔中的每一者被平面化电介质层侧向包围，其中，在所述第一和第二栅极腔中的每一者的底部处，所述半导体部分的顶表面被暴露；

Forming a gate dielectric layer in the first and second gate cavities;

在所述第一和第二栅极腔中形成栅极电介质层；

Forming a first work function material layer directly on a first portion of the gate dielectric layer located in the first gate cavity and directly over a portion of the gate dielectric layer in the second gate cavity A second work function material layer is formed on the second portion, wherein one of the first and second work function material layers is a conductive tantalum alloy layer, and the other of the first and second work function material layers One is a metal nitride layer; and

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直接在所述栅极电介质层的位于所述第一栅极腔中的第一部分上形成第一功函数材料层，并直接在所述栅极电介质层的位于所述第二栅极腔中的第二部分上形成第二功函数材料层，其中，所述第一和第二功函数材料层中的一者是导电钽合金层，且所述第一和第二功函数材料层中的另一者是金属氮化物层；以及

Filling the first gate cavity and the second gate cavity with a conductive material, wherein forming a first conductive material portion in the first gate cavity and forming a Two conductive material parts.

用导电材料填充所述第一栅极腔和所述第二栅极腔，其中，在所述第一栅极腔中形成第一导电材料部分，且在所述第二栅极腔中形成第二导电材料部分。

17.

The method of claim 16, wherein after forming the first conductive material portion, the first work function material layer is in contact with the first portion of the gate dielectric layer, and after forming the first After the second conductive material portion, the second work function material layer is in contact with the second portion of the gate dielectric layer.

如权利要求16所述的方法，其中，在形成所述第一导电材料部分之后，所述第一功函数材料层与所述栅极电介质层的所述第一部分接触，并且在形成所述第二导电材料部分之后，所述第二功函数材料层与所述栅极电介质层的所述第二部分接触。

18.

The method of claim 16, wherein one of the first and second portions of conductive material is formed directly on the conductive tantalum alloy layer.

如权利要求16所述的方法，其中，直接在所述导电钽合金层上形成所述第一和第二导电材料部分中的一者。

19.

The method of claim 16 wherein one of the first and second portions of conductive material and the gate electrode of the conductive tantalum alloy layer have a first work function and include the first and second The other of the second conductive material portions, and the other gate electrode of the metal nitride layer have a second work function that is closer to the conduction band of silicon than the mid-bandgap energy level of silicon, The second work function is closer to the valence band of silicon than the intermediate band gap energy of the silicon.

如权利要求16所述的方法，其中，包括所述第一和第二导电材料部分中的一者以及所述导电钽合金层的栅极电极具有第一功函数，且包括所述第一和第二导电材料部分中的另一者以及所述金属氮化物层的另一栅极电极具有第二功函数，所述第一功函数比硅的中间带隙能级更靠近硅的导带，所述第二功函数比所述硅的中间带隙能级更靠近硅的价带。

20.

The method of claim 16, wherein one of the first and second conductive material portions is formed directly on the first work function material layer and directly on the second work function material layer Forming the other of the first and second portions of conductive material.

如权利要求16所述的方法，其中，直接在所述第一功函数材料层上形成所述第一和第二导电材料部分中的一者，且直接在所述第二功函数材料层上形成所述第一和第二导电材料部分中的另一者。

21.

The method of claim 16, wherein a portion of the conductive tantalum alloy layer is formed directly on the metal nitride layer, and one of the first and second conductive material portions contacts The portion of the conductive tantalum alloy layer.

如权利要求16所述的方法，其中，所述导电钽合金层的一部分被直接形成在所述金属氮化物层上，且所述第一和第二导电材料部分中的一者在形成时接触所述导电钽合金层的所述一部分。

22.

The method of claim 16, wherein a portion of the metal nitride layer is formed directly on the conductive tantalum alloy layer and one of the first and second conductive material portions is contacted upon formation The portion of the metal nitride layer.

如权利要求16所述的方法，其中，所述金属氮化物层的一部分被直接形成在所述导电钽合金层上，且所述第一和第二导电材料部分中的一者在形成时接触所述金属氮化物层的所述一部分。

23.

The method of claim 16, wherein the conductive tantalum alloy layer comprises an alloy of tantalum and aluminum, wherein in the alloy of tantalum and aluminum, the atomic percentage of tantalum is from 10% to 99%, and the ratio of aluminum Atomic% of from 1% to 90%.

如权利要求16所述的方法，其中，所述导电钽合金层包括钽和铝的合金，其中，在所述钽和铝的合金中，钽的原子百分比为从10%到99%，且铝的原子百分比为从1%到90%。

24.

The method of claim 16, wherein the conductive tantalum alloy layer comprises an alloy of tantalum and carbon, wherein in the alloy of tantalum and carbon, the atomic percentage of tantalum is from 20% to 80%, and the carbon Atomic percent from 20% to 80%.

如权利要求16所述的方法，其中，所述导电钽合金层包括钽和碳的合金，其中，在所述钽和碳的合

金中，钽的原子百分比为从20%到80%，且碳的原子百分比为从20%到80%。

25.

The method of claim 16, wherein the conductive tantalum alloy layer comprises an alloy of tantalum, aluminum and carbon, wherein in the alloy of tantalum, aluminum and carbon, the atomic percentage of tantalum is from 15% to 80 %, The atomic percentage of aluminum is from 1% to 60%, and the atomic percentage of carbon is from 15% to 80%.

如权利要求16所述的方法，其中，所述导电钽合金层包括钽、铝和碳的合金，其中，在所述钽、铝和碳的合金中，钽的原子百分比为从15%到80%，铝的原子百分比为从1%到60%，且碳的原子百分比为从15%到80%。

Espacenet

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Semiconductor structure and formation method thereof

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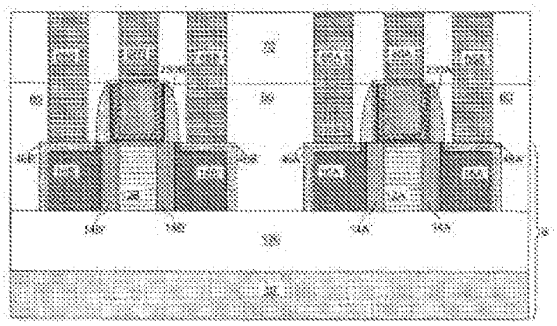
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Abstract of CN103258823 (A)



The invention refers to a semiconductor structure and a formation method thereof. A tantalum alloy layer is employed as a work function metal for field effect transistors. The tantalum alloy layer can be selected from TaC, TaAl, and TaAlC. When used in combination with a metallic nitride layer, the tantalum alloy layer and the metallic nitride layer provides two work function values that differ by 300 mV-500 mV, thereby enabling multiple field effect transistors having different threshold voltages. The tantalum alloy layer can be in contact with a first gate dielectric in a first gate, and the metallic nitride layer can be in contact with a second gate dielectric having a same composition and thickness as the first gate dielectric and located in a second gate.

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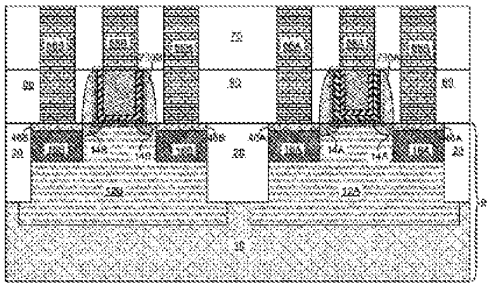
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(54)发明名称

半导体结构及其形成方法

(57)摘要

本发明涉及半导体结构及其形成方法。钽合金层被用作场效应晶体管的功函数金属。该钽合金层可以选自TaC、TaAl和TaAlC。在与金属氮化物层组合使用时，钽合金层和金属氮化物层提供相差300mV~500mV的两个功函数值，从而实现具有不同阈值电压的多个场效应晶体管。钽合金层可以与第一栅极中的第一栅极电介质接触，且金属氮化物层可以与第二栅极电介质接触，该第二栅极电介质具有与第一栅极电介质相同的组成和厚度并位于第二栅极中。



CN 103258823 A

1. 一种包括至少两个场效应晶体管的半导体结构，所述半导体结构包括：

第一场效应晶体管，其包括第一栅极电介质和第一栅极电极，其中，所述第一栅极电极包括与所述第一栅极电介质接触的导电钽合金层；以及

第二场效应晶体管，其包括第二栅极电介质和第二栅极电极，其中，所述第二栅极电极包括与所述第二栅极电介质接触的金属氮化物层。

2. 如权利要求 1 所述的半导体结构，其中，所述第一栅极电极包括与所述金属氮化物层和所述导电钽合金层中的一者接触的第一导电材料部分。

3. 如权利要求 2 所述的半导体结构，其中，所述第一栅极电极具有第一功函数，且所述第二栅极电极具有第二功函数，所述第一功函数比硅的中间带隙能级更靠近硅的导带，所述第二功函数比所述硅的中间带隙能级更靠近硅的价带。

4. 如权利要求 2 所述的半导体结构，其中，所述第二栅极电极包括第二导电材料部分，所述第二导电材料部分接触所述金属氮化物层和所述导电钽合金层中的另一者并具有与所述第一导电材料部分相同的组成。

5. 如权利要求 2 所述的半导体结构，其中，所述第二栅极电极包括所述导电钽合金层，且所述第一栅极电极包括具有与所述导电钽合金层相同的组成和厚度的另一导电钽合金层，其中，所述另一导电钽合金层与所述金属氮化物层以及所述第一导电材料部分接触，且所述导电钽合金层与第二导电材料部分接触，所述第二导电材料部分具有与所述第一导电材料部分相同的组成。

6. 如权利要求 2 所述的半导体结构，其中，所述第二栅极电极包括所述金属氮化物层，且所述第一栅极电极包括具有与所述金属氮化物层相同的组成和厚度的另一金属氮化物层，其中，所述另一金属氮化物层与所述导电钽合金层以及所述第一导电材料部分接触，且所述导电钽合金层与第二导电材料部分接触，所述第二导电材料部分具有与所述第一导电材料部分相同的组成。

7. 如权利要求 1 所述的半导体结构，其中，所述导电钽合金层包括选自钽和铝的合金、钽和碳的合金、以及钽、铝和碳的合金的材料。

8. 如权利要求 1 所述的半导体结构，其中，所述导电钽合金层包括钽和铝的合金，其中，在所述钽和铝的合金中，钽的原子百分比为从 10% 到 99%，且铝的原子百分比为从 1% 到 90%。

9. 如权利要求 1 所述的半导体结构，其中，所述导电钽合金层包括钽和碳的合金，其中，在所述钽和碳的合金中，钽的原子百分比为从 20% 到 80%，且碳的原子百分比为从 20% 到 80%。

10. 如权利要求 1 所述的半导体结构，其中，所述导电钽合金层包括钽、铝和碳的合金，其中，在所述钽、铝和碳的合金中，钽的原子百分比为从 15% 到 80%，铝的原子百分比为从 1% 到 60%，且碳的原子百分比为从 15% 到 80%。

11. 如权利要求 1 所述的半导体结构，其中，所述第一和第二导电材料部分包括 W 和 Al 中的至少一种。

12. 如权利要求 1 所述的半导体结构，其中，所述第一栅极电介质包括第一 U 形栅极电介质部分，所述第一 U 形栅极电介质部分包括第一栅极电介质垂直部分和第一栅极电介质水平部分，所述第二栅极电介质包括第二 U 形栅极电介质部分，所述第二 U 形栅极电介质部

分包括第二栅极电介质垂直部分和第二栅极电介质水平部分。

13. 如权利要求 12 所述的半导体结构，其中，所述第一和第二栅极电介质包括具有大于 3.9 的介电常数的电介质材料。

14. 如权利要求 1 所述的半导体结构，其中，所述第一和第二场效应晶体管中的每一者是平面场效应晶体管，其具有位于半导体衬底的最顶表面之下的沟道。

15. 如权利要求 1 所述的半导体结构，其中，所述第一和第二场效应晶体管中的每一者是鳍场效应晶体管，其具有直接位于半导体鳍的侧壁部分上的沟道对。

16. 一种形成半导体结构的方法，所述方法包括：

在半导体部分之上形成第一栅极腔和第二栅极腔，其中，所述第一栅极腔和所述第二栅极腔中的每一者被平面化电介质层侧向包围，其中，在所述第一和第二栅极腔中的每一者的底部处，所述半导体部分的顶表面被暴露；

在所述第一和第二栅极腔中形成栅极电介质层；

直接在所述栅极电介质层的位于所述第一栅极腔中的第一部分上形成第一功函数材料层，并直接在所述栅极电介质层的位于所述第二栅极腔中的第二部分上形成第二功函数材料层，其中，所述第一和第二功函数材料层中的一者是导电钽合金层，且所述第一和第二功函数材料层中的另一者是金属氮化物层；以及

用导电材料填充所述第一栅极腔和所述第二栅极腔，其中，在所述第一栅极腔中形成第一导电材料部分，且在所述第二栅极腔中形成第二导电材料部分。

17. 如权利要求 16 所述的方法，其中，在形成所述第一导电材料部分之后，所述第一功函数材料层与所述栅极电介质层的所述第一部分接触，并且在形成所述第二导电材料部分之后，所述第二功函数材料层与所述栅极电介质层的所述第二部分接触。

18. 如权利要求 16 所述的方法，其中，直接在所述导电钽合金层上形成所述第一和第二导电材料部分中的一者。

19. 如权利要求 16 所述的方法，其中，包括所述第一和第二导电材料部分中的一者以及所述导电钽合金层的栅极电极具有第一功函数，且包括所述第一和第二导电材料部分中的另一者以及所述金属氮化物层的另一栅极电极具有第二功函数，所述第一功函数比硅的中间带隙能级更靠近硅的导带，所述第二功函数比所述硅的中间带隙能级更靠近硅的价带。

20. 如权利要求 16 所述的方法，其中，直接在所述第一功函数材料层上形成所述第一和第二导电材料部分中的一者，且直接在所述第二功函数材料层上形成所述第一和第二导电材料部分中的另一者。

21. 如权利要求 16 所述的方法，其中，所述导电钽合金层的一部分被直接形成在所述金属氮化物层上，且所述第一和第二导电材料部分中的一者在形成时接触所述导电钽合金层的所述一部分。

22. 如权利要求 16 所述的方法，其中，所述金属氮化物层的一部分被直接形成在所述导电钽合金层上，且所述第一和第二导电材料部分中的一者在形成时接触所述金属氮化物层的所述一部分。

23. 如权利要求 16 所述的方法，其中，所述导电钽合金层包括钽和铝的合金，其中，在所述钽和铝的合金中，钽的原子百分比为从 10% 到 99%，且铝的原子百分比为从 1% 到 90%。

24. 如权利要求 16 所述的方法，其中，所述导电钽合金层包括钽和碳的合金，其中，在所述钽和碳的合金中，钽的原子百分比为从 20% 到 80%，且碳的原子百分比为从 20% 到 80%。

25. 如权利要求 16 所述的方法，其中，所述导电钽合金层包括钽、铝和碳的合金，其中，在所述钽、铝和碳的合金中，钽的原子百分比为从 15% 到 80%，铝的原子百分比为从 1% 到 60%，且碳的原子百分比为从 15% 到 80%。

半导体结构及其形成方法

技术领域

[0001] 本公开一般涉及半导体器件，更具体地，涉及包括钽合金层和金属氮化物层的半导体结构及其制造方法。

背景技术

[0002] CMOS 电路中的 p 型场效应晶体管(PFET)和 n 型场效应晶体管(NFET)的良好运行要求栅极电极具有相差至少 300mV~400mV 的功函数(work function)。为了提供具有不同功函数的多个功函数，在替代栅极集成方案中使用多种功函数金属。但是，这样的功函数金属倾向于无法提供足够低的电阻率，由此要求沉积具有低电阻率的额外的填充金属。因此，典型的替代栅极电极包括不同金属的大约 4-5 个层的叠层。随着半导体器件按比例缩小到 22nm 节点和 14nm 节点，使用不同导电金属层的叠层来填充窄栅极腔变得更具挑战性。

发明内容

[0003] 钽合金层被用作场效应晶体管的功函数金属。钽合金层可以选自 TaC、TaAl 和 TaAlC。在与金属氮化物层组合使用时，钽合金层和金属氮化物层提供相差 300mV~500mV 的两个功函数值，由此使得多个场效应晶体管能够具有不同阈值电压。钽合金层可以与第一栅极中的第一栅极电介质接触，且金属氮化物层可以与第二栅极电介质接触，该第二栅极电介质具有与第一栅极电介质相同的组成和厚度并位于第二栅极中。

[0004] 根据本公开的第一方面，提供了一种包括至少两个场效应晶体管的半导体结构。所述半导体结构包括：第一场效应晶体管，其包括第一栅极电介质和第一栅极电极，其中，所述第一栅极电极包括与所述第一栅极电介质接触的导电钽合金层；以及第二场效应晶体管，其包括第二栅极电介质和第二栅极电极，其中，所述第二栅极电极包括与所述第二栅极电介质接触的金属氮化物层。

[0005] 根据本发明的另一方面，提供了一种形成半导体结构的方法。所述方法包括：在半导体部分之上形成第一栅极腔和第二栅极腔，其中，所述第一栅极腔和所述第二栅极腔中的每一者被平面化电介质层侧向(laterally)包围，其中，在所述第一和第二栅极腔中的每一者的底部处，所述半导体部分的顶表面被暴露；在所述第一和第二栅极腔中形成栅极电介质层；直接在所述栅极电介质层的位于所述第一栅极腔中的第一部分上形成第一功函数材料层，并直接在所述栅极电介质层的位于所述第二栅极腔中的第二部分上形成第二功函数材料层，其中，所述第一和第二功函数材料层中的一者是导电钽合金层，且所述第一和第二功函数材料层中的另一者是金属氮化物层；以及用导电材料填充所述第一栅极腔和所述第二栅极腔，其中，在所述第一栅极腔中形成第一导电材料部分，并在所述第二栅极腔中形成第二导电材料部分。

附图说明

[0006] 图 1 是根据本公开的第一实施例在形成一次性(disposable)栅极级层(level

layer）之后的第一示例性半导体结构的垂直截面图；

[0007] 图 2 是根据本公开的第一实施例在对一次性栅极结构进行构图并形成源极扩展区域 / 漏极扩展区域之后的第一示例性半导体结构的垂直截面图；

[0008] 图 3 是根据本公开的第一实施例在形成间隔物（spacer）和源极区域 / 漏极区域之后的第一示例性半导体结构的垂直截面图；

[0009] 图 4 是根据本公开的第一实施例在平面化电介质层的沉积和平面化之后的第一示例性半导体结构的垂直截面图；

[0010] 图 5 是根据本公开的第一实施例在去除一次性栅极结构之后的第一示例性半导体结构的垂直截面图；

[0011] 图 6 是根据本公开的第一实施例在形成栅极电介质层和第一功函数材料层之后的第一示例性半导体结构的垂直截面图；

[0012] 图 7 是根据本公开的第一实施例在从第二场效应晶体管区域去除第一功函数材料层的暴露部分之后的第一示例性半导体结构的垂直截面图；

[0013] 图 8 是根据本公开的第一实施例在形成第二功函数材料层之后的第一示例性半导体结构的垂直截面图；

[0014] 图 9 是根据本公开的第一实施例在沉积导电材料层之后的第一示例性半导体结构的垂直截面图；

[0015] 图 10 是根据本公开的第一实施例在平面化之后的第一示例性半导体结构的垂直截面图；

[0016] 图 11 是根据本公开的第一实施例在形成接触级电介质层和接触过孔结构（contact via structure）之后的第一示例性半导体结构的垂直截面图；

[0017] 图 12 是根据本公开的第二实施例在形成半导体鳍（fin）、一次性栅极结构、源极扩展区域 / 漏极扩展区域、源极区域 / 漏极区域、源极金属半导体合金部分 / 漏极金属半导体合金部分之后的第二示例性半导体结构的垂直截面图；

[0018] 图 13 是根据本公开的第二实施例在平面化电介质层的沉积和平面化之后的第二示例性半导体结构的垂直截面图；

[0019] 图 14 是根据本公开的第二实施例在形成接触级电介质层和接触过孔结构之后的第二示例性半导体结构的垂直截面图；

[0020] 图 15 是图 14 中的第二示例性半导体结构沿着图 13 中的垂直平面 X-X' 的垂直截面图；

[0021] 图 16 是根据本公开的第三实施例在对第二功函数材料层进行构图之后的第三示例性半导体结构的垂直截面图；

[0022] 图 17 是根据本公开的第三实施例在沉积导电材料层之后的第三示例性半导体结构的垂直截面图；

[0023] 图 18 是根据本公开的第三实施例在平面化之后的第三示例性半导体结构的垂直截面图；

[0024] 图 19 是根据本公开的第三实施例在形成接触级电介质层和接触过孔结构之后的第三示例性半导体结构的垂直截面图；以及

[0025] 图 20 是根据本公开的第四实施例的第四示例性半导体结构的垂直截面图。

具体实施方式

[0026] 如上所述，本公开涉及半导体器件，更具体地，涉及将通过附图来详细地描述的包括钽合金层和金属氮化物层的半导体结构及其制造方法。本文中提到的和在图中示例的相同和相应的要素由相同的参考标号表示。附图未必按比例绘制。

[0027] 本文中使用的“一”、“一个”、“另一个”、“再一个”、“又一个”、“进一步另一个”或者其他文法限定词被用于区分一个要素与另一个要素。这样，在权利要求中用特定的文法限定词来标识的要素可以或可以不对应于说明书中采用相同的文法限定词的要素。

[0028] 本文中使用的“第一”、“第二”、“第三”和其他序数被用于区分一个要素与另一个要素。这样，在权利要求中用特定的序数来标识的要素可以或可以不对应于说明书中采用相同序数的要素。

[0029] 参考图 1，根据本公开的实施例的第一示例性半导体结构包括半导体衬底 8，场效应晶体管的各个部件相继在其上形成。半导体衬底 8 可以是整个地包含体半导体材料的体衬底或者是绝缘体上半导体(SOI)衬底(未示出)，所述 SOI 衬底包含顶部半导体层、位于顶部半导体层下面的掩埋(buried)绝缘体层、以及位于掩埋绝缘体层下面的底部半导体层。

[0030] 可以用 n 型或 p 型的电气掺杂剂以不同的掺杂浓度水平来掺杂半导体衬底 8 中的半导体材料的各个部分。例如，半导体衬底 8 可以包括下伏的(underlying)半导体层 10、在第一器件区域(图 1 中左侧的区域)中形成的第一掺杂阱 12A、以及在第二器件区域(图 1 中右侧的区域)中形成的第二掺杂阱 12B。在一个实施例中，可以用第一导电类型的掺杂剂来掺杂第二掺杂阱 12B，该第一导电类型可以是 n 型或 p 型，并可以用第二导电类型的掺杂剂来掺杂第一掺杂阱 12A，该第二导电类型与第一导电类型相反。如果第一导电类型为 p 型，则第二导电类型为 n 型，且反之亦然。

[0031] 浅沟槽隔离结构 20 被形成为使第二掺杂阱 12B 和第一掺杂阱 12A 中的每一者被侧向分隔。典型地，第二掺杂阱 12B 和第一掺杂阱 12A 中的每一者被浅沟槽隔离结构 20 的邻接(contiguous)部分侧向包围。如果半导体衬底 8 是绝缘体上半导体衬底，第二掺杂阱 12B 和第一掺杂阱 12A 的底表面可以接触掩埋的绝缘体层(未示出)，其连同浅沟槽隔离结构 20 将第二掺杂阱 12B 和第一掺杂阱 12A 中的每一者与半导体衬底 8 的其他半导体部分电隔离。在一个实施例中，浅沟槽隔离结构 20 的最顶表面可以与第二掺杂阱 12B 和第一掺杂阱 12A 的最顶表面基本上共面。

[0032] 一次性栅极级层被沉积在半导体衬底 8 上作为毯覆(blanket)层，即，作为未被构图的连续层。一次性栅极级层可以包括例如一次性栅极电介质层 23L、一次性栅极材料层 27L 和一次性栅极帽盖(cap)电介质层 29L 的垂直叠层。一次性栅极电介质层 23L 可以是例如氧化硅、氮化硅或氧氮化硅的层。一次性栅极电介质层 23L 的厚度可以为从 1nm 到 10nm，但还可以使用更小或更大的厚度。一次性栅极材料层 27L 包括随后对随后将形成的平面化电介质层的电介质材料具有选择性地去除的材料。例如，一次性栅极材料层 27L 可以包括诸如多晶半导体材料或非晶半导体材料的半导体材料。一次性栅极材料层 27L 的厚度可以为从 30nm 到 300nm，但还可以采用更小或更大的厚度。一次性栅极帽盖电介质层 29L 可以包括诸如氧化硅、氮化硅或氧氮化硅的电介质材料。一次性栅极帽盖电介质层 29L 的厚度可以为从 3nm 到 30nm，但还可以采用更小或更大的厚度。尽管以包括一次性栅极电介质层

23L、一次性栅极材料层 27L 和一次性栅极帽盖电介质层 29L 的垂直叠层的一次性栅极级层示例了本公开，但也可以采用任何其他一次性栅极级层，只要可以对随后将形成的平面化电介质层具有选择性地去除该一次性栅极级层中的材料即可。

[0033] 参考图 2，一次性栅极级层（29L、27L、23L）被光刻构图以形成一次性栅极结构。具体地，光致抗蚀剂（未示出）被施加到一次性栅极级层（29L、27L、23L）的最顶表面上，并通过光刻曝光和显影而被光刻构图。光致抗蚀剂中的图形通过蚀刻而被转移（transfer）到一次性栅极级层（29L、27L、23L），该蚀刻可以是各向异性蚀刻，例如反应离子蚀刻。在图形转移之后的一次性栅极级层（29L、27L、23L）的剩余部分构成了一次性栅极结构。

[0034] 一次性栅极叠层可以包括例如在第一器件区域中的第一掺杂阱 12A 之上形成的第一一次性栅极结构以及在第二器件区域中的第二掺杂阱 12B 之上形成的第二一次性栅极结构。第一一次性栅极结构是第一一次性栅极电介质部分 23A、第一一次性栅极材料部分 27A 和第一一次性栅极帽盖部分 29A 的叠层，并且第二一次性栅极结构是第二一次性栅极电介质部分 23B、第二一次性栅极材料部分 27B 和第二一次性栅极帽盖部分 29B 的叠层。第一一次性栅极帽盖部分 29A 和第二一次性栅极帽盖部分 29B 是一次性栅极帽盖电介质层 29L 的剩余部分。第一一次性栅极材料部分 27A 和第二一次性栅极材料部分 27B 是一次性栅极材料层 27L 的剩余部分。第一一次性栅极电介质部分 23A 和第二一次性栅极电介质部分 23B 是一次性栅极电介质层 23L 的剩余部分。

[0035] 可以采用掩蔽离子注入来形成各种源极扩展区域 / 漏极扩展区域。例如，第一导电类型的掺杂剂可被注入到第一掺杂阱 12A 的未被第一一次性栅极结构（23A、27A、29A）覆盖的部分，以形成具有第一导电类型的掺杂的第一源极扩展区域 / 漏极扩展区域 14A。在该注入过程中，可以通过经构图的光致抗蚀剂（未示出）来掩蔽第二掺杂阱 12B，以防止在其中注入额外的第一导电类型的掺杂剂。本文中使用的“源极扩展区域 / 漏极扩展区域”共同地表示源极扩展区域和漏极扩展区域。类似地，第二导电类型的掺杂剂可被注入到第二掺杂阱 12B 的未被第二一次性栅极结构（23B、27B、29B）覆盖的部分，以形成第二源极扩展区域 / 漏极扩展区域 14B。在该注入过程中，可以通过另一经构图的光致抗蚀剂（未示出）来掩蔽第一掺杂阱 12A，以防止在其中注入额外的第二导电类型的掺杂剂。

[0036] 参考图 3，例如，通过保形的（conformal）电介质材料层的沉积和各向异性蚀刻，在一次性栅极结构中的每一者的侧壁上形成栅极间隔物。栅极间隔物可以包括在第一一次性栅极结构（23A、27A、29A）周围形成的第一栅极间隔物 52A 以及在第二一次性栅极结构（23B、27B、29B）周围形成的第二栅极间隔物 52B。

[0037] 通过注入可以是 p 型掺杂剂或 n 型掺杂剂的电气掺杂剂，分别在第一掺杂阱 12A 和第二掺杂阱 12B 中形成第一源极区域 / 漏极区域 16A 和第二源极区域 / 漏极区域 16B。可以采用掩蔽离子注入来形成第一源极区域 / 漏极区域 16A 和第二源极区域 / 漏极区域 16B。或者，可以通过用应力产生（stress-generating）半导体材料（例如硅锗合金或硅碳合金）来替换第一掺杂阱 12A 或第二掺杂阱 12B 的物理暴露部分，来将第一源极区域 / 漏极区域 16A 和第二源极区域 / 漏极区域 16B 形成为源极区域 / 漏极区域。掩埋的应力产生半导体材料可以与第一掺杂阱 12A 的剩余部分或第二掺杂阱 12B 的剩余部分外延对准。

[0038] 参考图 4，可以例如通过金属层（未示出）的沉积和退火，在半导体衬底 8 的顶表面上的暴露半导体材料上形成第一金属半导体合金部分 46A 和第二金属半导体合金部分

46B。对金属层的反应部分具有选择性地去除该金属层的未反应部分。金属层的反应部分构成金属半导体合金部分(46A、46B),如果第一和第二源极和漏极区域(16A、16B)的半导体材料包括硅,则所述金属半导体合金部分可以包括金属硅化物部分。

[0039] 各金属半导体合金部分46A、46B包括:在第一源极区域(16A中的一个)上形成的第一源极侧金属半导体合金部分(46A中的一个)、在第一漏极区域(16A中的另一个)上形成的第一漏极侧金属半导体合金部分(16A中的另一个)、在第二源极区域(16B中的一个)上形成的第二源极侧金属半导体合金部分(46B中的一个)、以及在第二漏极区域(16B中的另一个)上形成的第二漏极侧金属半导体合金部分(16B中的另一个)。

[0040] 可选地,可以在金属半导体合金部分(46A、46B)、第一和第二一次性栅极结构(23A、27A、29A、23B、27B、29B)以及第一和第二栅极间隔物(52A、52B)之上沉积电介质衬里(liner)(未示出)。可选地,可以在第一一次性栅极结构(23A、27A、29A)和第二一次性栅极结构(23B、27B、29B)之上分别形成第一应力产生衬里(未示出)和第二应力产生衬里(未示出)。第一应力产生衬里和第二应力产生衬里可以包括产生对下伏的结构的压缩应力或张伸应力的电介质材料,并且可以是在各种等离子体条件下通过等离子体增强化学气相沉积来沉积的氮化硅层。

[0041] 平面化电介质层60可以被沉积在第一应力产生衬里和/或第二应力产生衬里(如果存在)之上,或者被沉积在金属半导体合金部分(46A、46B)、第一和第二一次性栅极结构(23A、27A、29A、23B、27B、29B)以及第一和第二栅极间隔物(52A、52B)之上(如果不存在应力产生衬里)。优选地,平面化电介质层60是可以被容易地平面化的电介质材料。例如,平面化电介质层60可以是经掺杂的硅酸盐玻璃或未掺杂的硅酸盐玻璃(氧化硅)。

[0042] 在第一和第二一次性栅极结构(23A、27A、29A、23B、27B、29B)的最顶表面之上,即,在第一和第二一次性栅极帽盖部分(29A、29B)的最顶表面上方,对平面化电介质层60和任何额外的电介质材料层(其包括存在的第一应力产生衬里、第二应力产生衬里和电介质衬里中的任一者)进行平面化。例如可以通过化学机械平面化(CPM)来进行平面化。平面化电介质层60的平面最顶表面在这里被称为平面电介质表面63。在平面化之后,一次性栅极帽盖部分(29A、29B)的最顶表面与平面电介质表面63共面。

[0043] 第一源极和漏极扩展区域14A、第一源极和漏极区域16A以及第一掺杂阱12A的组合可被用于随后形成第一场效应晶体管。第二源极和漏极扩展区域14B、第二源极和漏极区域16B以及第二掺杂阱12B的组合可被用于随后形成第二场效应晶体管

[0044] 参考图5,通过至少一次蚀刻,去除第一一次性栅极结构(23A、27A、29A)和第二一次性栅极结构(23B、27B、29B)。例如可以通过可包括各向异性蚀刻、各向同性蚀刻或其组合的至少一次蚀刻,去除第一和第二一次性栅极结构(23A、27A、29A、23B、27B、29B)。所述至少一次蚀刻可以包括干法蚀刻和/或湿法蚀刻。被用于去除第一和第二一次性栅极结构(23A、27A、29A、23B、27B、29B)的所述至少一次蚀刻优选地对平面化电介质层60的电介质材料以及在半导体衬底8之上存在的任何其他电介质材料层具有选择性。

[0045] 在从其中去除了第一一次性栅极结构(23A、27A、29A)的体积(volume)中形成第一栅极腔25A,并在从其中去除了第二一次性栅极结构(23B、27B、29B)的体积中形成第二栅极腔25B。半导体衬底8的半导体表面,即,第一掺杂阱12A的顶表面被暴露在第一栅极腔25A的底部。半导体衬底8的另一半导体表面,即,第二掺杂阱12B的顶表面被暴露在第

二栅极腔 25B 的底部。第一和第二栅极腔(25A、25B)中的每一者被平面化电介质层 60 侧向包围。第一栅极间隔物 52A 侧向包围第一栅极腔 25A,且第二栅极间隔物 52B 侧向包围第二栅极腔 25B。第一栅极间隔物 52A 的内侧壁可以基本垂直,并从第一掺杂阱 12A 的顶表面延伸到平面化电介质层 60 的平面电介质表面 63,即,最顶表面。此外,第二栅极间隔物 52B 的内侧壁可以基本垂直,并从第二掺杂阱 12B 的顶表面延伸到平面化电介质层 60 的平面电介质表面 63。

[0046] 参考图 6,将栅极电介质层 32L 沉积在栅极腔(25A、25B)的底表面和侧壁上以及平面化电介质层 60 的最顶表面上。栅极电介质层 32L 可以是具有大于 3.9 的介电常数的高介电常数(高 k)材料层。栅极电介质层 32L 可以包括介电金属氧化物(其是包含金属和氧的高 k 材料),并在本领域中被已知为高 k 栅极电介质材料。可通过本领域中包括例如化学气相沉积(CVD)、物理气相沉积(PVD)、分子束沉积(MBD)、脉冲激光沉积(PLD)、液态源雾化化学沉积(LSMCD)、原子层沉积(ALD)等的众所周知的方法,来沉积介电金属氧化物。示例性高 k 电介质材料包括 HfO_2、ZrO_2、La_2O_3、Al_2O_3、TiO_2、$SrTiO_3$、$LaAlO_3$、Y_2O_3、HfO_xN_y、ZrO_xN_y、$La_2O_xN_y$、$Al_2O_xN_y$、TiO_xN_y、$SrTiO_xN_y$、$LaAlO_xN_y$、$Y_2O_xN_y$、其硅酸盐及其合金。x 的每个值独立地为从 0.5 到 3,且 y 的每个值独立地为从 0 到 2。在水平部分处测量的栅极电介质层 32L 的厚度可以为从 0.9nm 到 6nm,且优选地从 1.0nm 到 3nm。栅极电介质层 32L 可以具有 2nm 量级或更小的有效氧化物厚度。在一个实施例中,栅极电介质层 32L 是氧化铪(HfO_2)层。

[0047] 沉积包括第一金属材料的第一功函数材料层 34L,该第一金属材料具有第一功函数。第一功函数材料层 34L 可以是 p 型功函数材料层或 n 型功函数材料层。这里所使用的"p 型功函数材料"是指具有在硅的价带能级与硅的中间带隙能级之间的功函数的材料,该中间带隙能级即为与硅的价带能级和导带能级相等分隔的能级。这里所使用的"n 型功函数材料"是指具有在硅的导带能级与硅的中间带隙能级之间的功函数的材料。

[0048] 在一个实施例中,第一功函数材料层 34L 是导电钽合金层。该导电钽合金层可以包括选自钽和铝的合金、钽和碳的合金、以及钽、铝和碳的合金的材料。导电钽合金层的第一实例是钽-铝合金层,其包括钽和铝的合金。在钽和铝的合金中,钽的原子百分比可以为从 10% 到 99%,且铝的原子百分比可以为从 1% 到 90%。钽-铝合金层可以基本由钽和铝组成。

[0049] 导电钽合金层的第二实例是碳化钽层,其包括钽和碳的合金。在钽和碳的合金中,钽的原子百分比可以为从 20% 到 80%,且碳的原子百分比可以为从 20% 到 80%。碳化钽层可以基本由钽和碳组成。

[0050] 导电钽合金层的第三实例是碳化钽铝层,其包括钽、铝和碳的合金。在钽、铝和碳的合金中,钽的原子百分比可以为从 15% 到 80%,铝的原子百分比可以为从 1% 到 60%,且碳的原子百分比可以为从 15% 到 80%。

[0051] 在另一实施例中,第一功函数材料层 34L 是导电金属氮化物层。例如,第一功函数材料层 34L 可以是基本由氮化钛组成的氮化钛层。在氮化钛层中,钛的原子百分比可以为从 30% 到 90%,且氮的原子百分比可以为从 10% 到 70%。

[0052] 第一功函数材料层 34L 例如可以通过原子层沉积(ALD)、物理气相沉积(PVD)或化学气相沉积(CVD)来沉积。第一功函数材料层 34L 可以是或可以不是保形的。换句话说,第一功函数材料层 34L 的垂直部分可以或可以不与第一功函数材料层 34L 的水平部分具有

相同的厚度。第一功函数材料层 34L 的水平部分的在第一和第二栅极腔(25A、25B)的底部处的厚度可以为从 1.0nm 到 10nm,但还可以采用更小或更大的厚度。

[0053] 参考图 7,光致抗蚀剂 39 被施加并被光刻构图,以便光致抗蚀剂 39 覆盖位于第一掺杂阱 12A 之上的区域,而第一功函数材料层 34L 在第二掺杂阱 12B 之上暴露。可以通过蚀刻从第二栅极腔 25B 中去除第一功函数材料层 34L 的暴露部分,该蚀刻可以是湿法蚀刻或干法蚀刻。栅极电介质层 32L 的一部分在第二栅极腔 25B 的底部和侧壁处被物理暴露。例如可以通过灰化(ashing)或湿法蚀刻来去除光致抗蚀剂 39。

[0054] 参考图 8,沉积包含第二金属材料的第二功函数材料层 36L,该第二金属材料具有第二功函数。

[0055] 在一个实施例中,第一功函数材料层 34L 是导电钽合金层,第二功函数材料层 36L 是导电金属氮化物层。例如,第二功函数材料层 36L 可以是基本由氮化钛组成的氮化钛层。在该氮化钛层中,钛的原子百分比可以为从 30% 到 90%,且氮的原子百分比可以为从 10% 到 70%。该金属氮化物层的一部分被直接形成在第一栅极腔 25A 中的导电钽合金层上。

[0056] 在另一实施例中,第一功函数材料层 34L 是导电金属氮化物层,第二功函数材料层 36L 是导电钽合金层。导电钽合金层可以包括选自钽和铝的合金、钽和碳的合金、以及钽、铝和碳的合金的材料。导电钽合金层可以是钽铝合金层、碳化钽层和碳化钽铝层中的任一者,其中每一者可以具有与上述相同的组成。导电钽合金层的一部分被直接形成在第一栅极腔 25A 中的金属氮化物层上。

[0057] 第二功函数材料层 36L 例如可以通过原子层沉积(ALD)、物理气相沉积(PVD)或化学气相沉积(CVD)来沉积。第二功函数材料层 36L 可以是或可以不是保形的。第二功函数材料层 36L 的水平部分的在第一和第二栅极腔(25A、25B)的底部处的厚度可以为从 1.0nm 到 50nm,但还可以采用更小或更大的厚度。

[0058] 由此,直接在栅极电介质层 32L 的位于第一栅极腔 25A 中的第一部分上形成第一功函数材料层 34L,且直接在栅极电介质层 32L 的位于第二栅极腔 25B 中的第二部分上形成第二功函数材料层 36L。第一和第二功函数材料层(34L、36L)中的一者是导电钽合金层,且第一和第二功函数材料层(34L、36L)中的另一者是金属氮化物层。

[0059] 参考图 9,用导电材料层 40L 来填充栅极腔(25A、25B)。直接在钨阻挡层 38L 上形成导电材料层 40L。导电材料层 40L 包括可以通过物理气相沉积或化学气相沉积来沉积的金属。例如,导电材料层 40L 可以是通过物理气相沉积来沉积的铝层或钨层或者铝合金层或钨合金层。在导电材料层 40L 的位于平面化电介质层 60 的顶表面上方的平面区域中测量的导电材料层 40L 的厚度可以为从 100nm 到 500nm,但还可以采用更小或更大的厚度。在一个实施例中,导电材料层 40L 可以包括选自 W 和 Al 的至少一种材料。此外,导电材料层 40L 可以基本上由诸如 W 或 Al 的单种元素金属组成。

[0060] 参考图 10,例如通过化学机械平面化来对导电材料层 40L、第二功函数材料层 36L、第一功函数材料层 34L 和栅极电介质层 32L 进行平面化。具体地,在平面化步骤结束时,从平面化电介质层 60 的平面电介质表面 63 上方去除了导电材料层 40L、第二功函数材料层 36L、第一功函数材料层 34L 和栅极电介质层 32L 的部分。栅极电介质层 32L 的位于第一器件区域中的剩余部分形成第一栅极电介质 32A,且栅极电介质层 32L 的位于第二器件区域中的剩余部分形成第二栅极电介质 32B。第一功函数材料层 34L 的位于第一器件区域

中的剩余部分形成第一功函数材料部分34。第二功函数材料层36L的位于第一器件区域中的剩余部分形成第二功函数材料部分36A。第二功函数材料层36L的位于第二器件区域中的剩余部分形成功函数材料部分36B。导电材料层40L的位于第一器件区域中的剩余部分构成第一金属部分40A，且导电材料层的位于第二器件区域中的剩余部分构成第二金属部分40B。第一和第二栅极电介质(32A、32B)、第一和第二功函数材料部分(34、36A)、功函数材料部分36B以及第一和第二金属部分(40A、40B)的最顶表面与平面化电介质层60的最顶表面共面。

[0061] 由此，之前在图6的步骤中被第一和第二栅极腔(25A、25B)占据的体积中形成替换栅极叠层。该替换栅极叠层包括位于第一器件区域中的第一替换栅极叠层230A以及位于第二器件区域中的第二替换栅极叠层230B。每一个替换栅极叠层(230A、230B)覆盖在场效应晶体管的沟道区域上。第一替换栅极叠层230A和第二替换栅极叠层230B被同时形成。

[0062] 在第一器件区域中形成第一场效应晶体管。第一场效应晶体管包括第一掺杂阱12A、第一源极扩展区域/漏极扩展区域14A、第一源极区域/漏极区域16A、第一金属半导体合金部分46A、第一替换栅极叠层230A和第一栅极间隔物52A。第一替换栅极叠层230A包括第一栅极电介质32A、第一功函数材料部分34、第二功函数材料部分36A和第一金属部分40A。

[0063] 在第二器件区域中形成第二场效应晶体管。第二场效应晶体管包括第二掺杂阱12B、第二源极扩展区域/漏极扩展区域14B、第二源极区域/漏极区域16B、第二金属半导体合金部分46B、第二替换栅极叠层230B和第二栅极间隔物52B。第二替换栅极叠层230B包括第二栅极电介质32B、功函数材料部分36B和第二金属部分40B。第一替换栅极叠层230A中的第二功函数材料部分36A和第二替换栅极叠层230B中的功函数材料部分36B具有相同的材料组成和相同的厚度。

[0064] 第一和第二场效应晶体管中的每一者是平面场效应晶体管，其具有位于半导体衬底的最顶表面下方的沟道。第一和第二场效应晶体管中的一者包括这样的栅极电极：该栅极电极包括导电钽合金层并与栅极电介质接触。第一和第二场效应晶体管中的另一者包括另一栅极电极，该栅极电极包含金属氮化物层并与另一栅极电介质接触。

[0065] 在一个实施例中，第一栅极电极和第二栅极电极中的一者可以具有第一功函数，该第一功函数比硅的中间带隙能级更靠近硅的导带，且第一栅极电极和第二栅极电极中的另一者可以具有第二功函数，该第二功函数比硅的中间带隙能级更靠近硅的价带。

[0066] 第一栅极电极230A包括与第二功函数材料部分36A接触的第一导电材料部分40A，该第二功函数材料部分36A是金属氮化物层和导电钽合金层中的一者。第二栅极电极230B包括与金属氮化物层和导电钽合金层中的另一者接触的第二导电材料部分40B。第二导电材料部分40B可以具有与第一导电材料部分40A相同的组成。

[0067] 在一个实施例中，第二栅极电极230B包括导电钽合金层作为功函数材料部分36B，且第一栅极电极230A包括具有与该导电钽合金层相同的组成和厚度的另一导电钽合金层作为第二功函数材料部分36A。第一栅极电极230A中的导电钽合金层与第一栅极电极230A中的金属氮化物层即第一功函数材料部分34接触，并与第一导电材料部分40A接触。该导电钽合金层与第二导电材料部分40B接触，该第二导电材料部分40B具有与第一导电

材料部分 40A 相同的组成。

[0068] 在另一实施例中，第二栅极电极 230B 包括金属氮化物层为功函数材料部分 36B，且第一栅极电极 230A 包括具有与该金属氮化物层相同的组成和厚度的另一金属氮化物层作为第二功函数材料部分 36A。第一栅极电极 230A 中的金属氮化物层与第一栅极电极 230A 中的导电钽合金层即第一功函数材料部分 34 接触，并与第一导电材料部分 40A 接触。该导电钽合金层与第二导电材料部分 40B 接触，该第二导电材料部分 40B 具有与第一导电材料部分 40A 相同的组成。

[0069] 第一和第二栅极电介质（32A、32B）中的每一者是 U 形栅极电介质，其包括水平栅极电介质部分以及从水平栅极电介质部分的周边区域向上延伸的垂直栅极电介质部分。在第一场效应晶体管中，第一功函数材料部分 34 与第一栅极电介质 32A 的垂直栅极电介质部分的内侧壁接触。在第二场效应晶体管中，功函数材料部分 36B 与第二栅极电介质 32B 的垂直栅极电介质部分的内侧壁接触。每一个 U 形栅极电介质位于半导体衬底 8 上并被掩埋在平面化电介质层 60 中。

[0070] 作为 U 形栅极电介质，每一个栅极电介质（32A、32B）包括水平栅极电介质部分和垂直栅极电介质部分。垂直栅极电介质部分从水平栅极电介质部分连续地延伸到平面化电介质层 60 的最顶表面。

[0071] 如果第二功函数材料部分 36A 和功函数材料部分 36B 包括金属氮化物，则第一和第二导电材料部分（40A、40B）中的每一者在形成时接触金属氮化物层的一部分。如果第二功函数材料部分 36A 和功函数材料部分 36B 包括导电钽合金，则第一和第二导电材料部分（40A、40B）中的每一者在形成时接触导电钽合金层的一部分。

[0072] 参考图 11，在平面化电介质层 60 之上沉积接触级电介质层 70。例如，可以通过光刻图形形成和各向异性蚀刻的组合而形成接触过孔腔，然后进行金属沉积和从接触级电介质层 70 上方去除金属的过量部分的平面化，来形成各种接触过孔结构。各种接触过孔结构可以包括例如第一源极接触过孔结构 / 漏极接触过孔结构（即，至少一个第一源极接触过孔结构和至少一个第一漏极接触过孔结构）66A、第二源极接触过孔结构 / 漏极接触过孔结构（即，至少一个第二源极接触过孔结构和至少一个第二漏极接触过孔结构）66B、第一栅极接触过孔结构 68A 和第二栅极接触过孔结构 68B。每一个源极接触过孔结构（66A、66B）和每一个漏极接触过孔结构（66A、66B）被掩埋在平面化电介质层 60 和接触级电介质材料层 70 中。每一个源极接触过孔结构（66A 和 66B 中的一个）接触源极侧金属半导体合金部分（46A 和 46B 中的一个），且每一个漏极接触过孔结构（66A 和 66B 中的另一个）接触漏极侧金属半导体合金部分（46A 和 46B 中的另一个）。

[0073] 参考图 12，可以例如通过对绝缘体上半导体（SOI）衬底进行构图，来形成第二示例性半导体结构。具体地，提供包括顶部半导体层、掩埋绝缘体层 120、以及处理衬底（handle substrate）10' 的 SOI 衬底。顶部半导体层被构图为形成第一器件区域中的第一半导体鳍和第二器件区域中的第二半导体鳍。

[0074] 使用与第一实施例中相同的方法，在第一和第二半导体鳍上形成一次性栅极叠层。此外，在第一半导体鳍中形成第一源极扩展区域 / 漏极扩展区域 14'，并在第二半导体鳍中形成第二源极扩展区域 / 漏极扩展区域 14B'。在第一一次性栅极结构（23A、27A、29A）的周围形成第一栅极间隔物 52A，并在第二一次性栅极结构（23B、27B、29B）的周围形成第

二栅极间隔物 52B。使用第一一次性栅极结构(23A、27A、29A)和第一栅极间隔物 52A 作为注入掩膜的部分,在第一半导体鳍中形成第一源极和漏极区域 16A'。使用第二一次性栅极结构(23B、27B、29B)和第二栅极间隔物 52B 作为注入掩膜的部分,在第二半导体鳍中形成第二源极和漏极区域 16A'。每个半导体鳍中的半导体材料的未注入部分构成第一主体部分 12A'和第二主体部分 12B'。可以使用与第一实施例中相同的处理方法,在第一和第二源极和漏极区域(16A'、16B')上形成各种金属半导体合金部分(46A'、46B')。

[0075] 参考图 13,使用与第一实施例中相同的处理步骤,即,图 4 的处理步骤,将平面化电介质层 60 沉积在半导体鳍、一次性栅极结构和掩埋绝缘体层 120 之上。

[0076] 参考图 14 和 15,可以执行与第一实施例中相同的处理步骤,来形成图 14 和 15 中示例的第二示例性半导体结构。除了所述第一和第二场效应晶体管中的每一者是具有直接位于半导体鳍的侧壁部分上的沟道对的鳍场效应晶体管之外,第二示例性半导体结构包括与图 11 的第一示例性半导体结构相同的特征。

[0077] 参考图 16,通过将光致抗蚀剂 37 施加到图 8 的第一示例性结构之上、随后对光致抗蚀剂 37 进行构图以覆盖第二栅极腔 25B 的区域(见图 8)而不覆盖第一栅极腔 25A 的区域,从图 8 的第一示例性半导体结构得到根据本公开的第三实施例的第三示例性半导体结构。可以通过蚀刻来去除第二功函数材料层 36L 的物理暴露部分,该蚀刻可以是湿法蚀刻或干法蚀刻。随后去除光致抗蚀剂 37。

[0078] 参考图 17,将导电材料层 40L 沉积在第一和第二栅极腔(25A、25B)中。导电材料层 40L 可以具有与第一实施例中相同的组成和厚度,并可以采用与第一实施例中相同的处理步骤来沉积。

[0079] 参考图 18,例如通过化学机械平面化来对导电材料层 40L、第二功函数材料层 36L、第一功函数材料层 34L 以及栅极电介质层 32L 进行平面化。与第一实施例中相同的处理步骤可被用于平面化。

[0080] 具体地,在平面化步骤结束时,从平面化电介质层 60 的平面电介质表面 63 上方去除了导电材料层 40L、第二功函数材料层 36L、第一功函数材料层 34L 以及栅极电介质层 32L 的部分。栅极电介质层 32L 的位于第一器件区域中的剩余部分形成第一栅极电介质 32A,且栅极电介质层 32L 的位于第二器件区域中的剩余部分形成第二栅极电介质 32B。第一功函数材料层 34L 的位于第一器件区域中的剩余部分形成第一功函数材料部分 34'。第二功函数材料层 36L 的位于第二器件区域中的剩余部分形成第二功函数材料部分 36'。导电材料层 40L 的位于第一器件区域中的剩余部分构成第一金属部分 40A,且导电材料层的位于第二器件区域中的剩余部分构成第二金属部分 40B。第一和第二栅极电介质(32A、32B)、第一和第二功函数材料部分(34、36A)、功函数材料部分 36B 以及第一和第二金属部分(40A、40B)的最顶表面与平面化电介质层 60 的最顶表面共面。

[0081] 在形成第一导电材料部分 40A 之后,第一功函数材料层,即,第一功函数材料部分 34'与栅极电介质层 32L 的第一部分接触。在形成第二导电材料部分 40B 之后,第二功函数材料层,即,第二功函数材料部分 36'与栅极电介质层 32L 的第二部分接触。

[0082] 参考图 19,可以例如通过光刻构图和各向异性蚀刻的组合而形成接触过孔腔,然后进行金属沉积和用于从接触级电介质层 70 上方去除金属的过量部分的平面化,来形成接触级电介质层 70 和各种接触过孔结构(66A、66B、68A、68B)。

[0083] 参考图 20，可以通过执行第一实施例的图 5-8 的处理步骤和第三实施例的图 16-19 的处理步骤，来从图 13 的第二示例性半导体结构得到根据本公开的第四实施例的第四示例性半导体结构。除了所述第一和第二场效应晶体管中的每一者是具有直接位于半导体鳍的侧壁部分上的沟道对的鳍场效应晶体管之外，第四示例性半导体结构包括与图 19 的第三示例性半导体结构相同的特征。

[0084] 尽管关于具体实施例描述了本公开，但考虑到上述描述很明显的是，对于本领域技术人员来说，多种替代、修改和变化将是显然的。本公开的各种实施例的每一者可以被单独或者与本公开的任何其他实施例组合来实现，除非另外明确地公开或者据本领域普通技术人员所知是不可能的。因此，本公开旨在包含落在本公开和以下权利要求的范围和精神内的所有这样的替代、修改和变化。

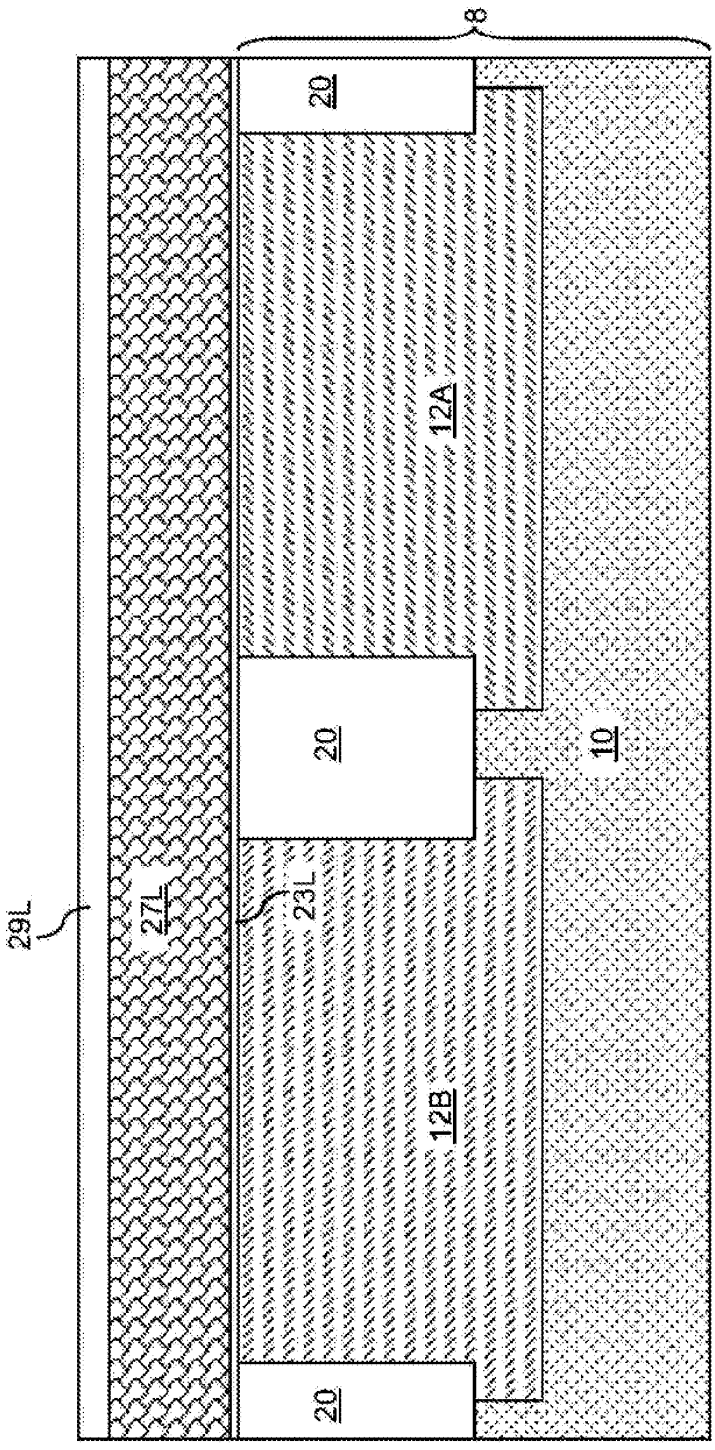


图 1

16

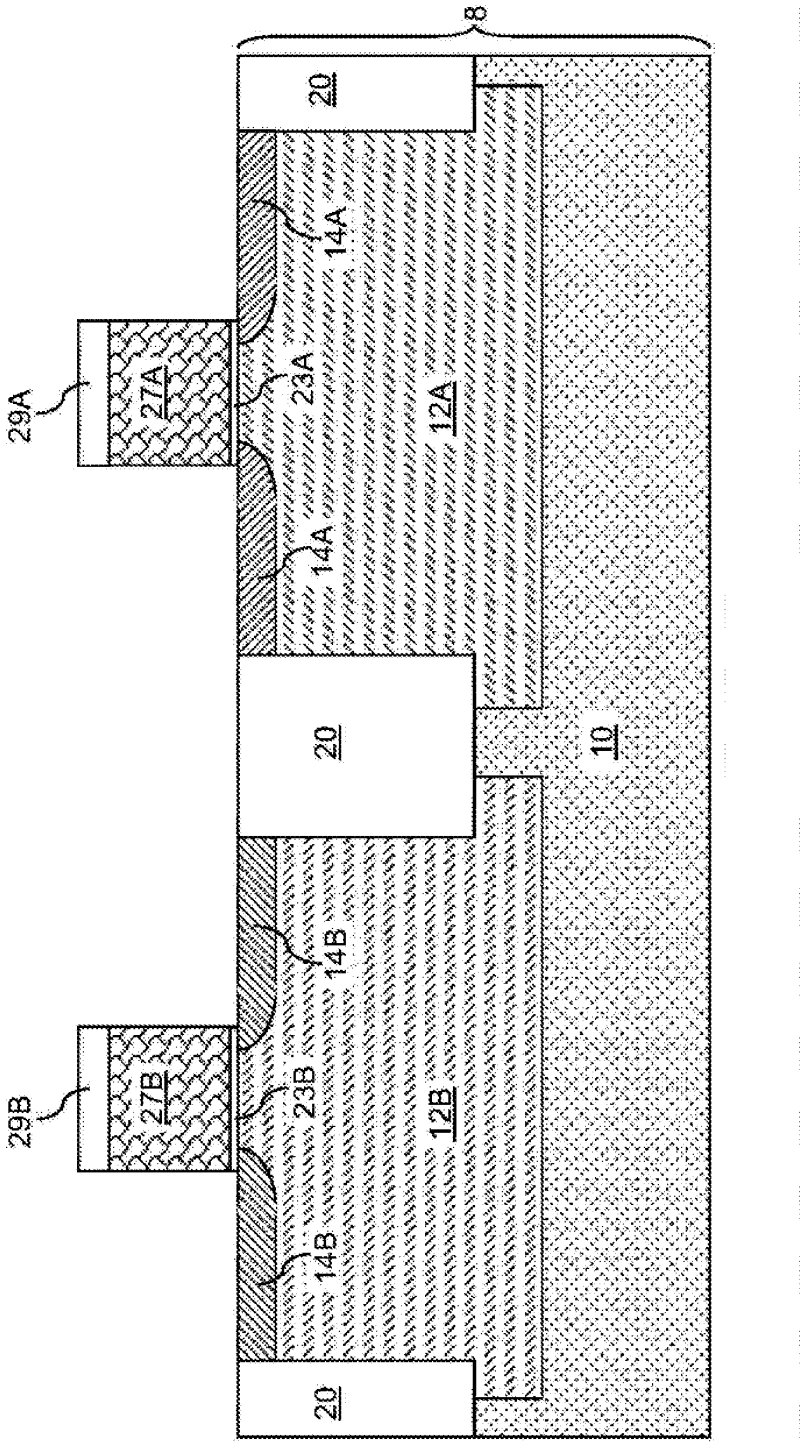


图 2

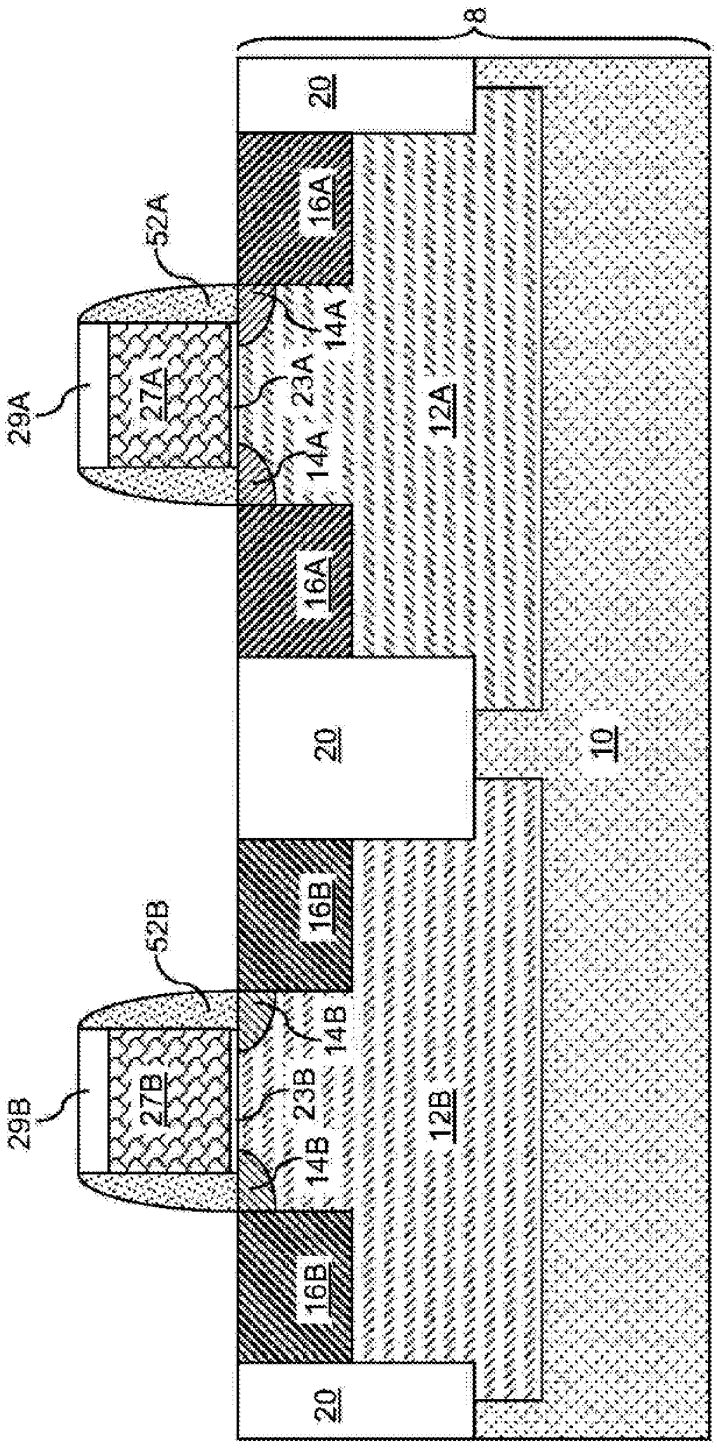

8
20
16A
52A
14A
23A
29A
27A
14A
12A
16A
20
10
16B
52B
14B
23B
29B
27B
14B
12B
16B
20

图 3

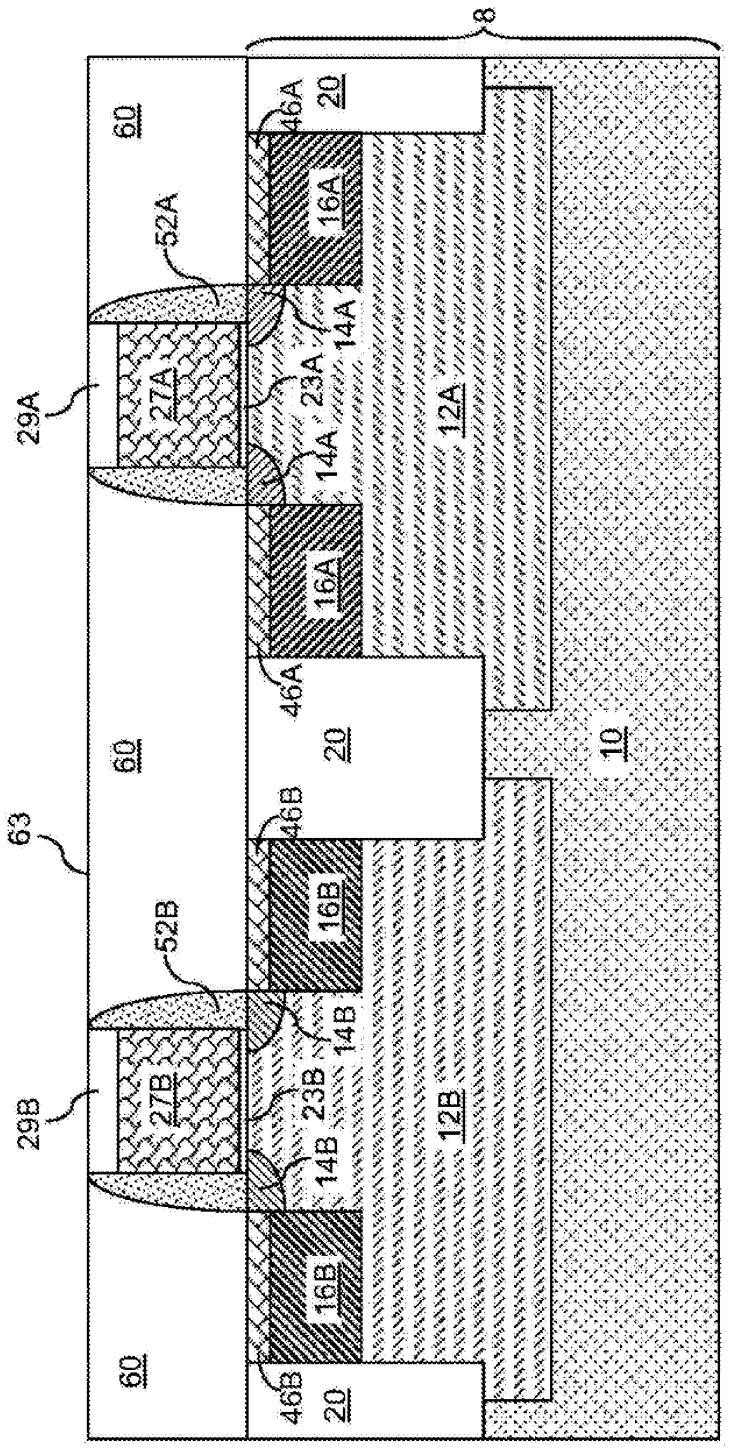

8
60
20
46A
16A
52A
14A
23A
27A
29A
12A
14A
16A
46A
20
10
60
63
46B
16B
52B
14B
23B
27B
29B
12B
14B
16B
60
46B
20

图 4

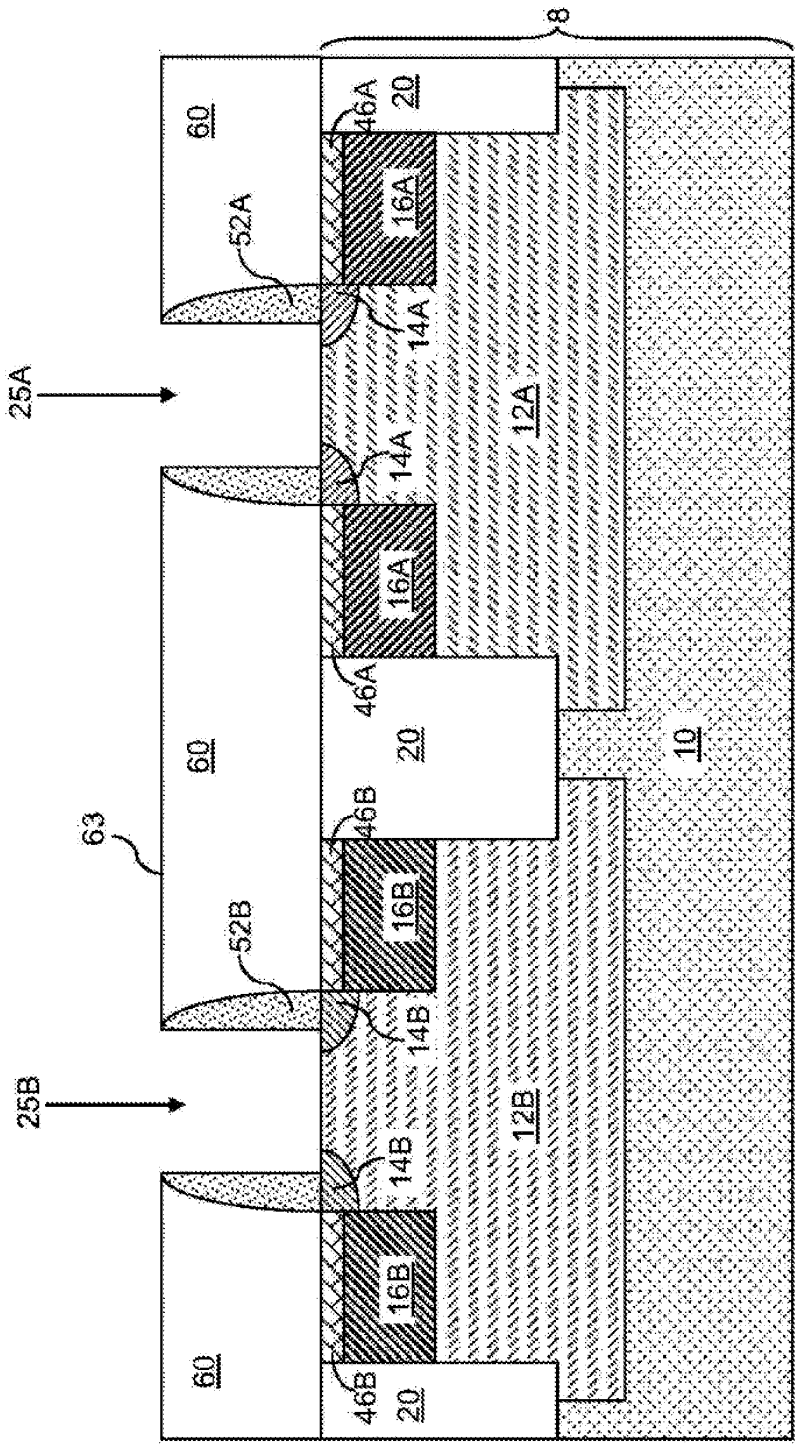

8
60
46A
20
16A
52A
14A
25A
12A
16A
46A
20
10
60
63
46B
16B
52B
14B
25B
12B
14B
16B
60
46B
20

图 5

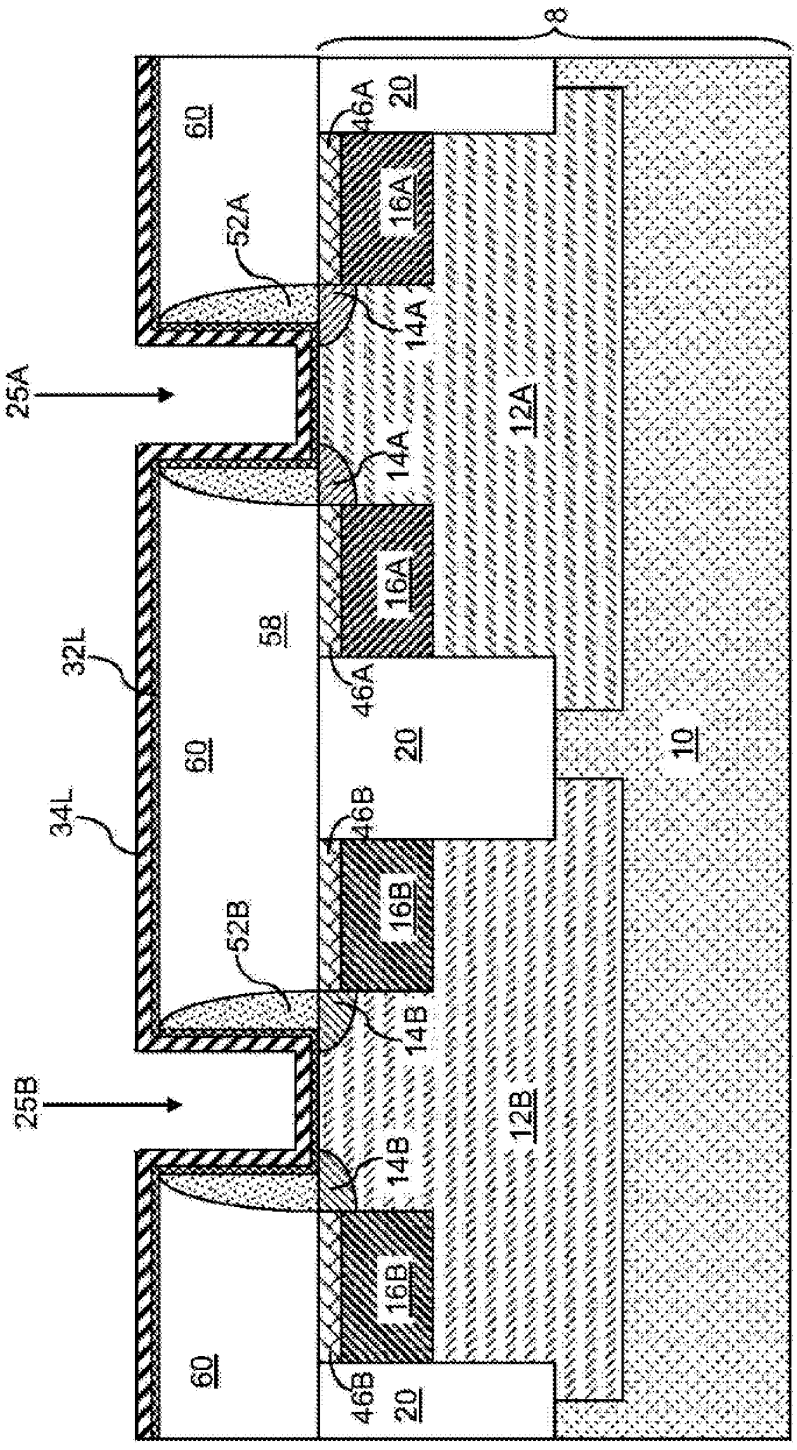

8
60
46A
20
16A
52A
14A
25A
12A
58
32L
60
46A
20
10
34L
46B
16B
52B
14B
25B
12B
14B
16B
60
46B
20

图 6

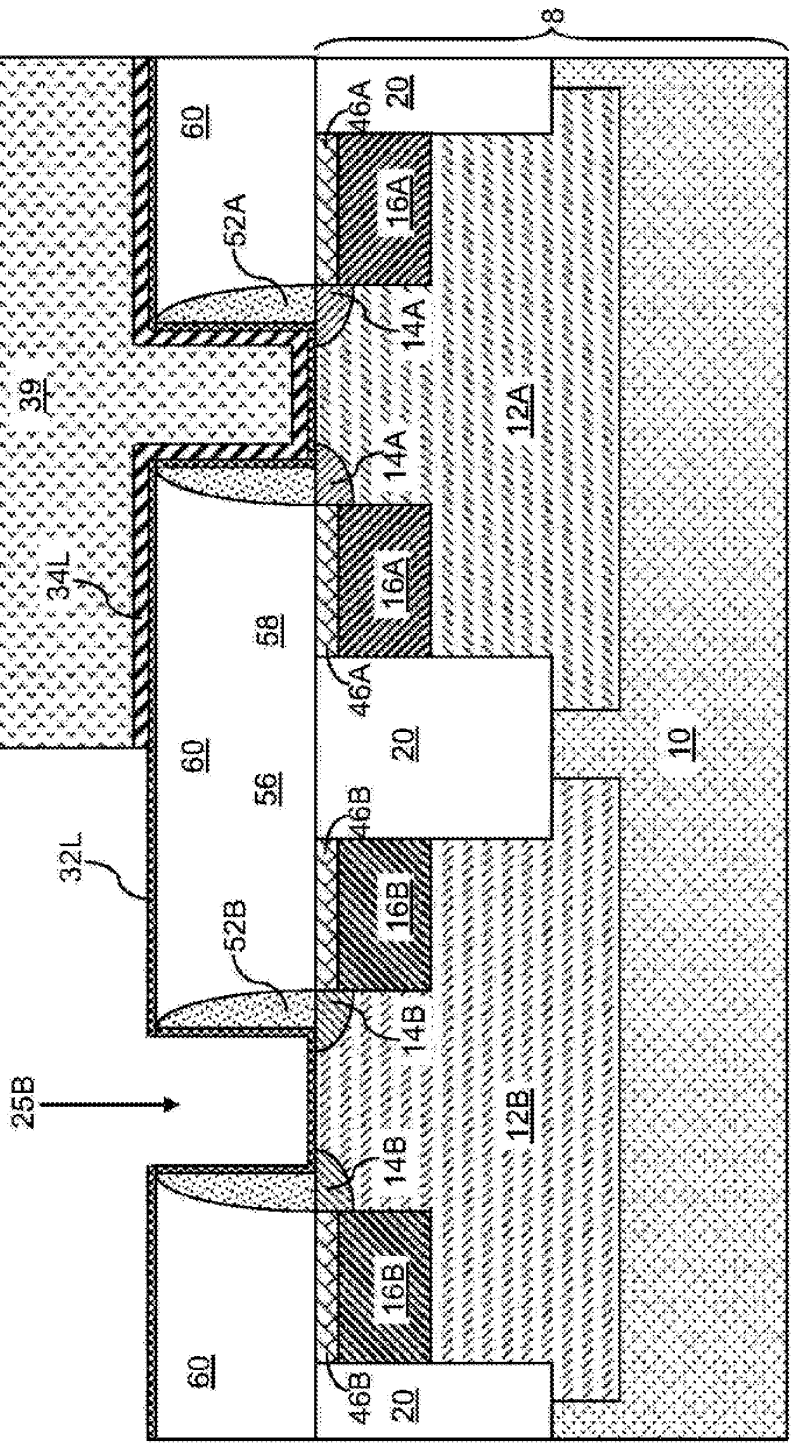


图 7

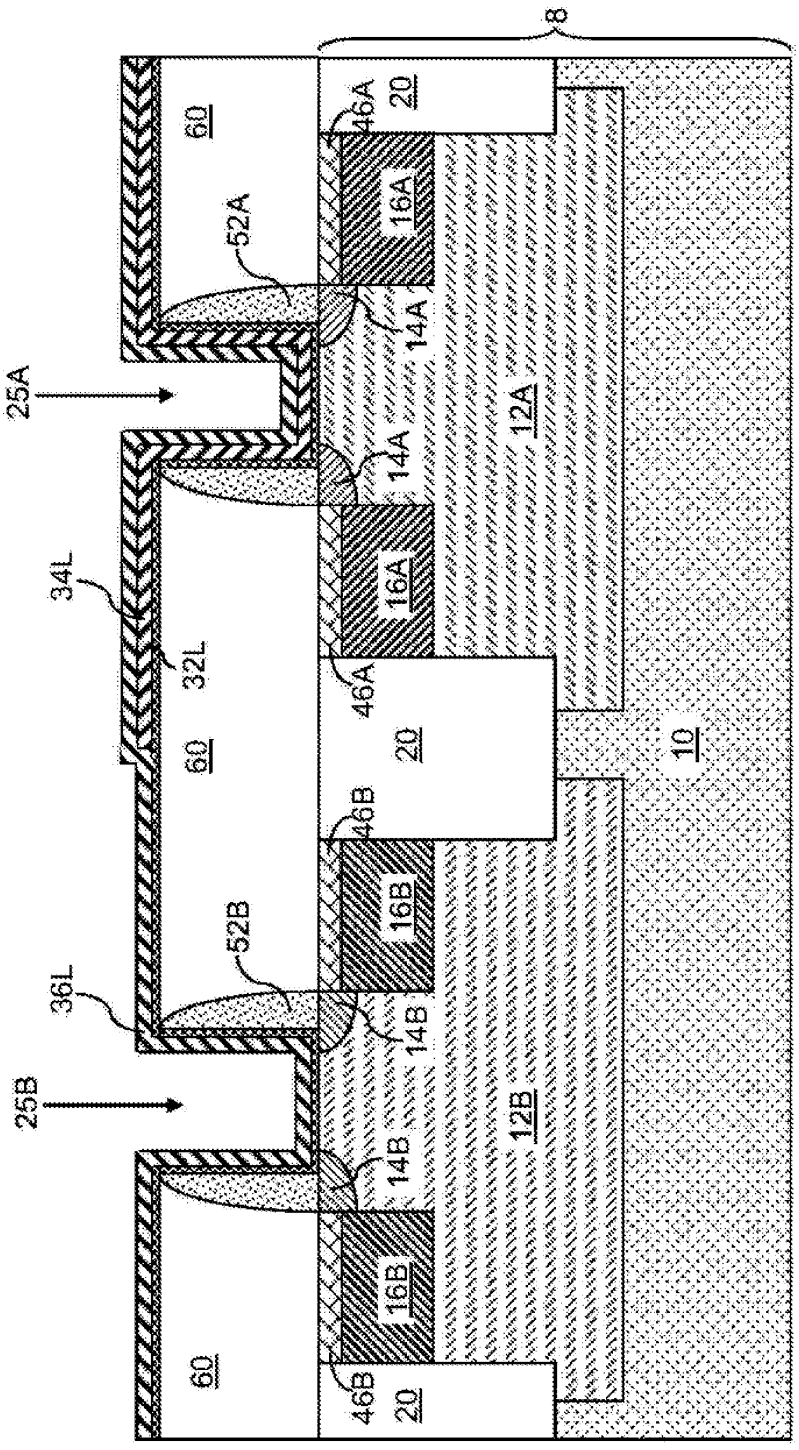

8
60
46A
20
16A
52A
14A
12A
25A
34L
32L
60
46A
20
10
46B
16B
52B
36L
14B
25B
12B
14B
16B
60
46B
20

图 8

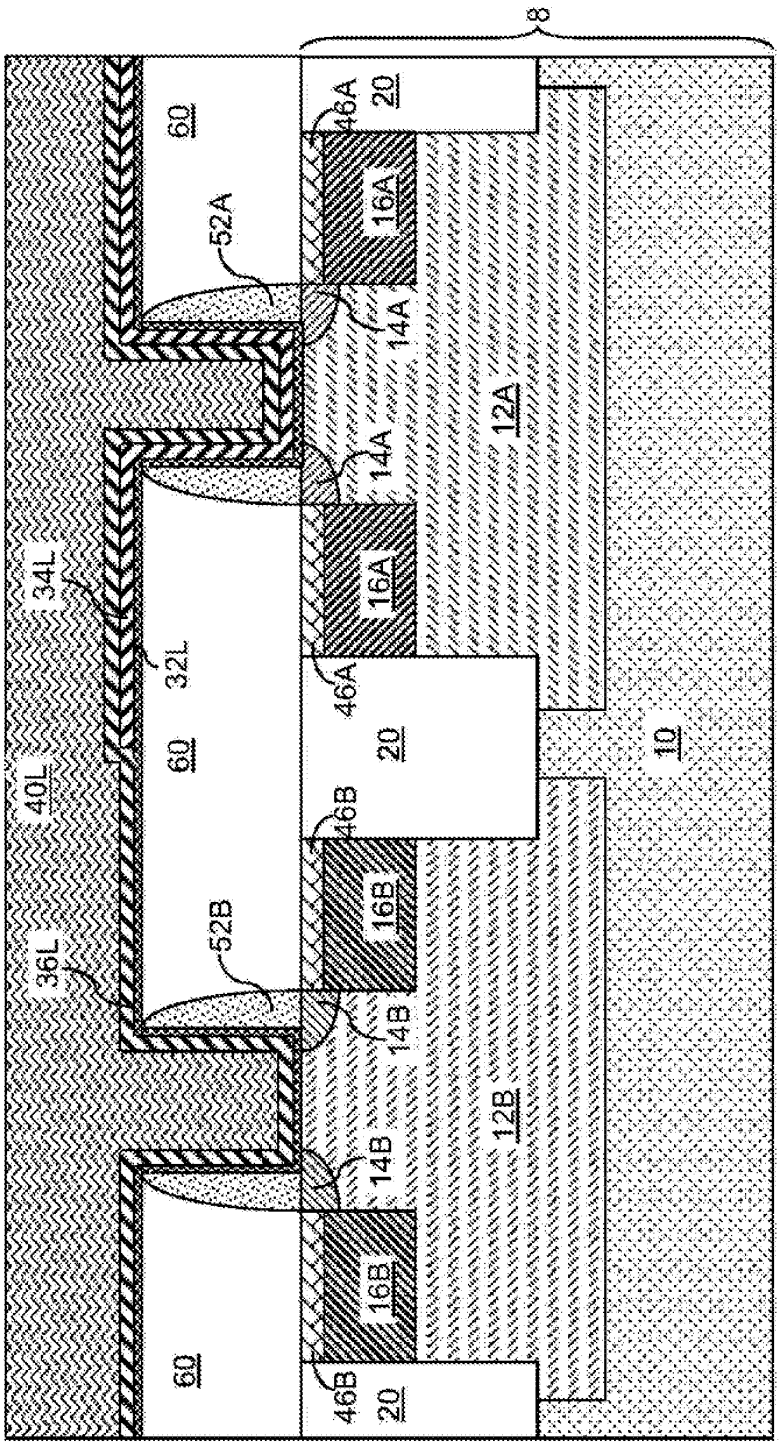


图 9

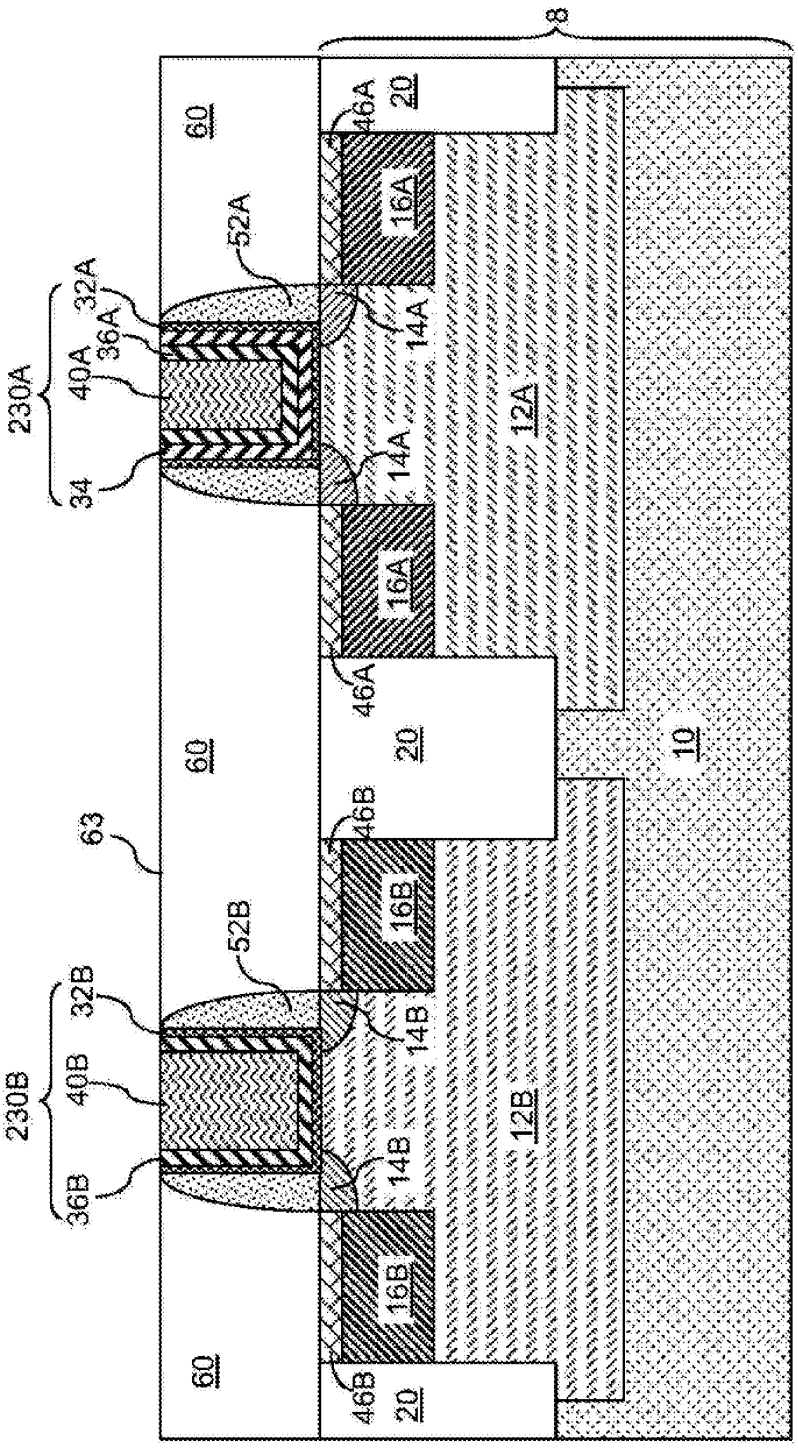

8
60
20
46A
16A
52A
32A
36A
40A
230A
34
14A
12A
10
63
46B
16B
52B
32B
40B
230B
36B
14B
12B

图 10

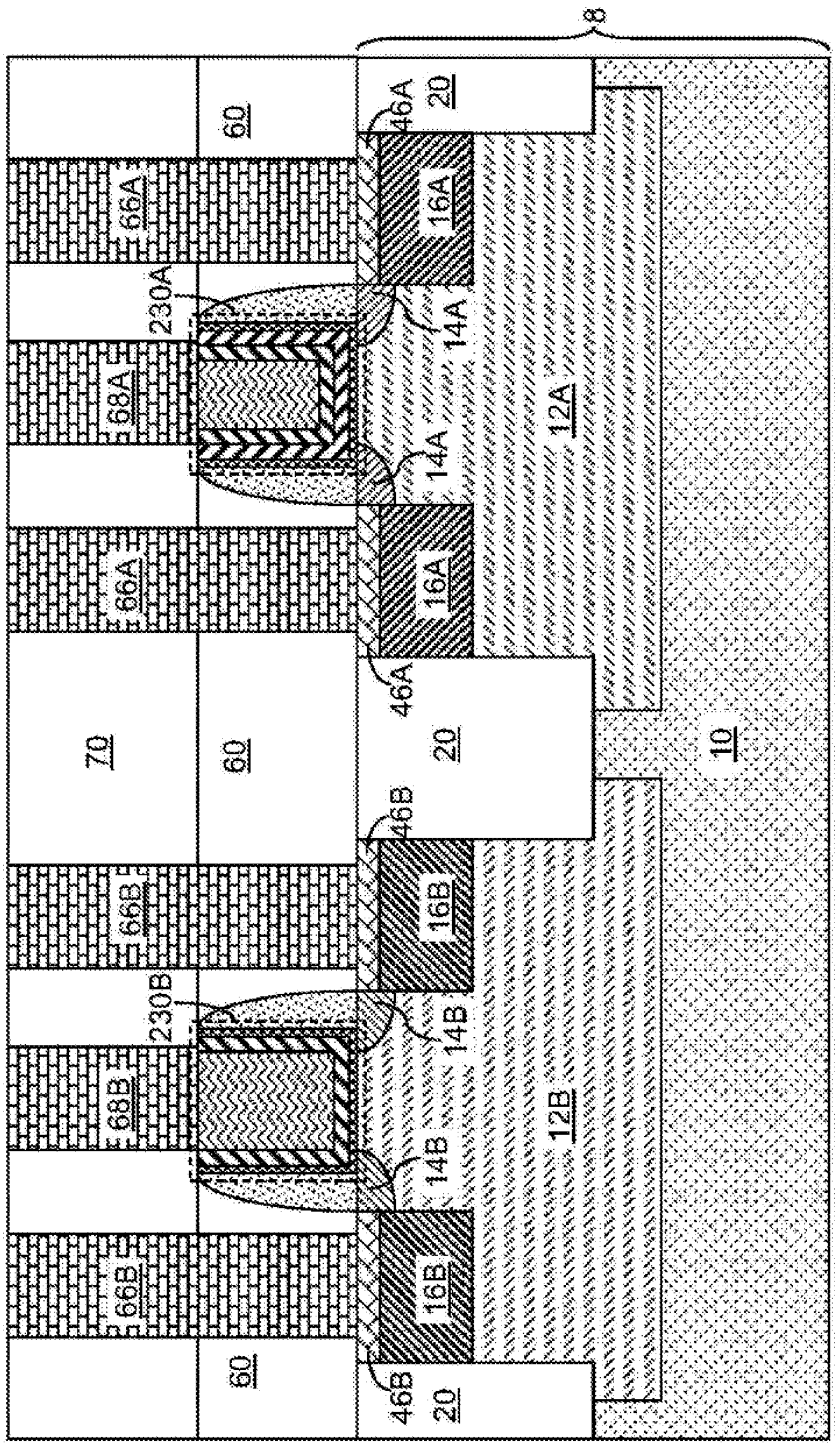

8
60
46A
20
66A
16A
230A
14A
68A
12A
70
10
46B
66B
16B
230B
14B
68B
12B

图 11

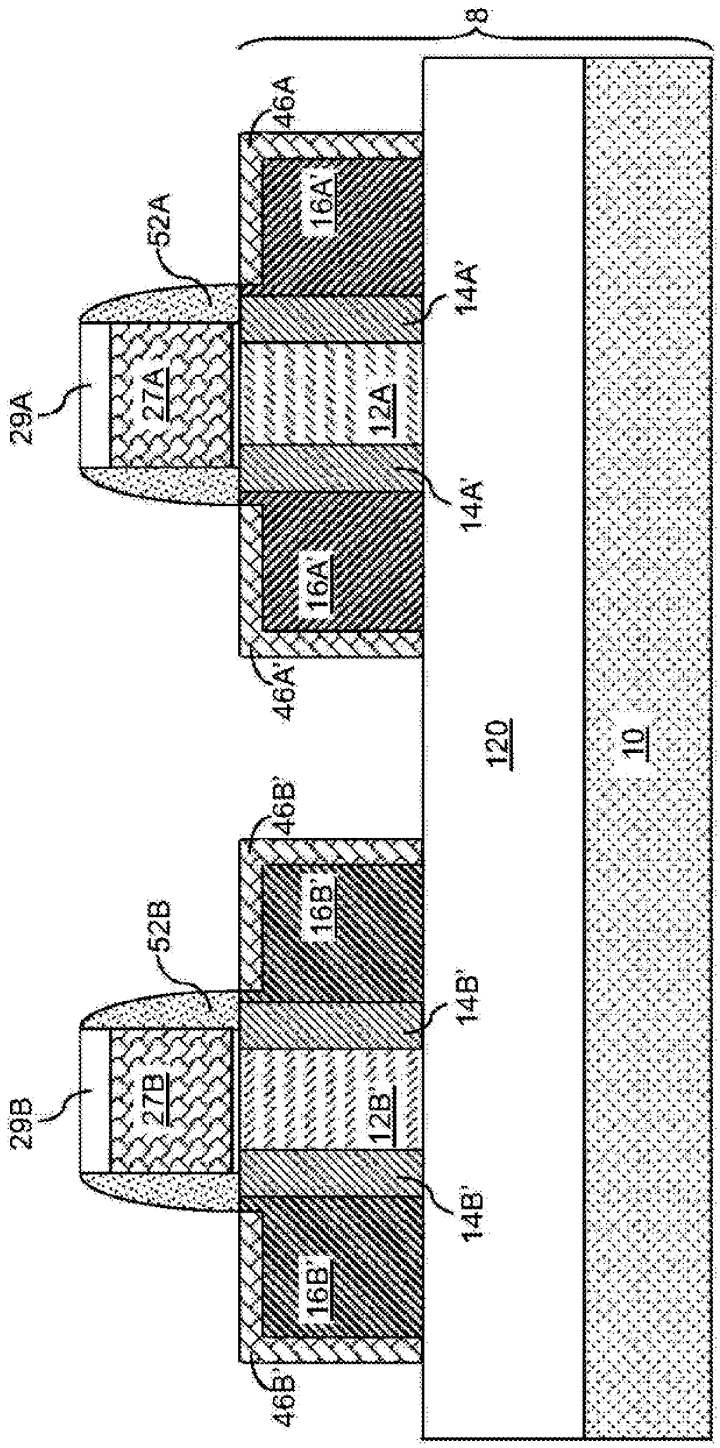

8
46A
16A'
52A
14A'
29A
27A
12A'
14A'
16A'
46A'
120
10
46B'
16B'
52B
14B'
29B
27B
12B'
14B'
16B'
46B'

图 12

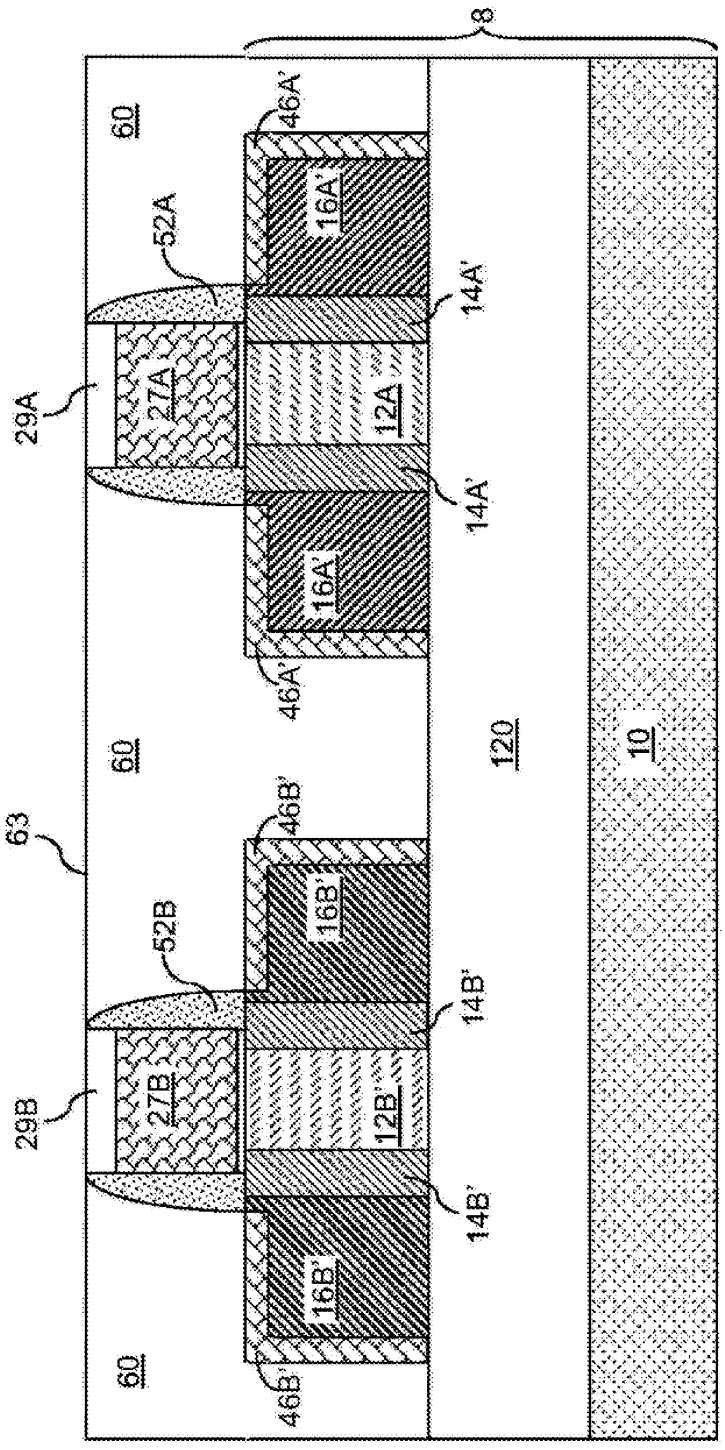

8
60
46A'
16A'
52A
14A'
29A
27A
12A
14A'
16A'
46A'
60
120
10
63
46B'
16B'
52B
14B'
29B
27B
12B'
14B'
16B'
60
46B'

图 13

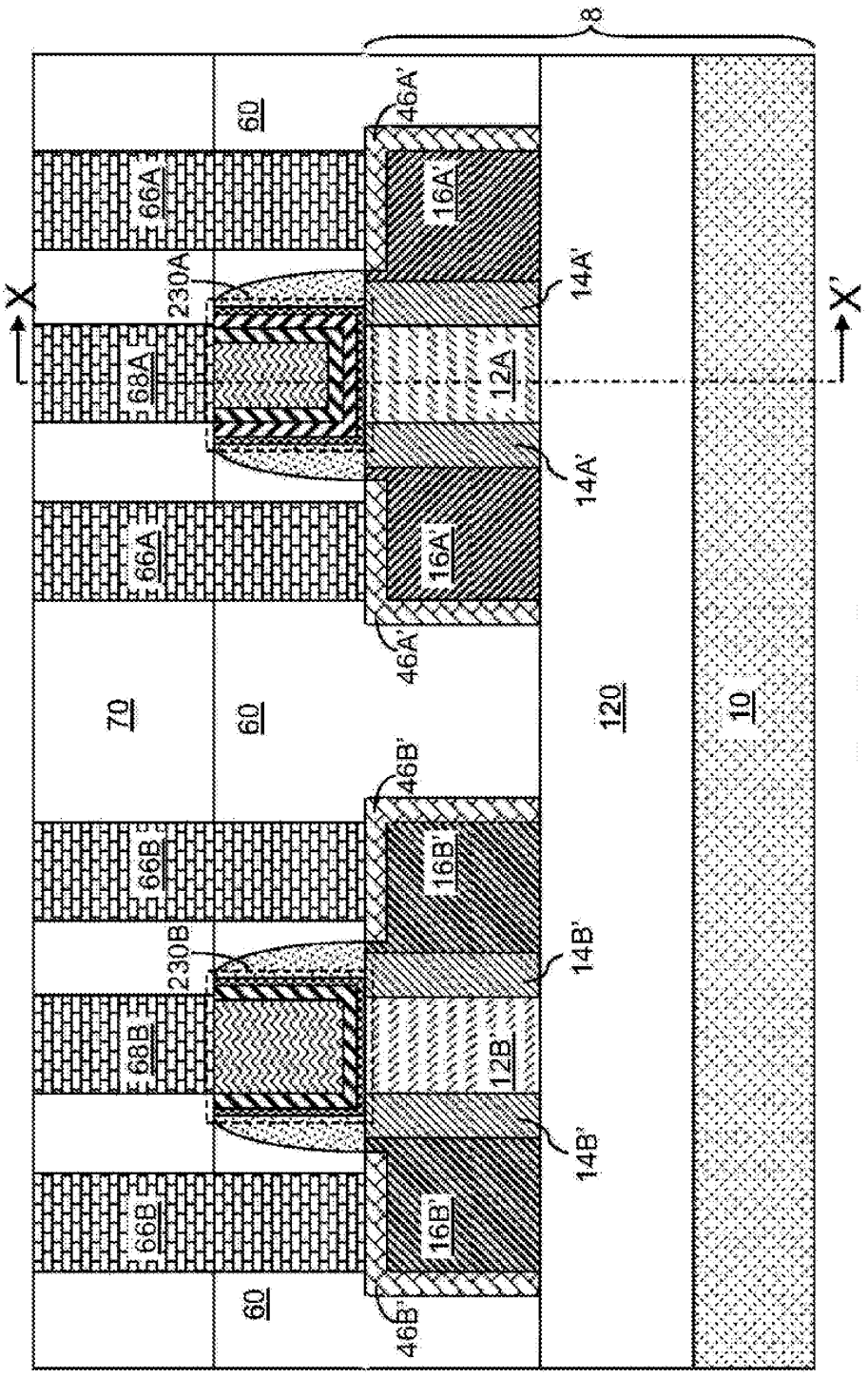

8
60
46A'
16A'
66A
230A
14A'
X
X'
68A
12A
14A'
16A'
66A
46A'
70
60
120
10
46B'
16B'
66B
230B
14B'
68B
12B'
14B'
16B'
66B
60
46B'

图 14

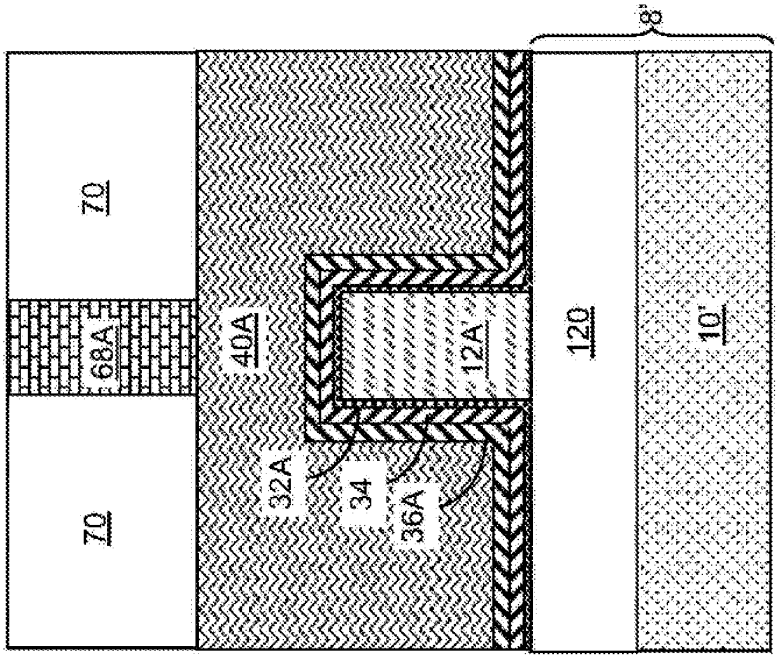


图 15

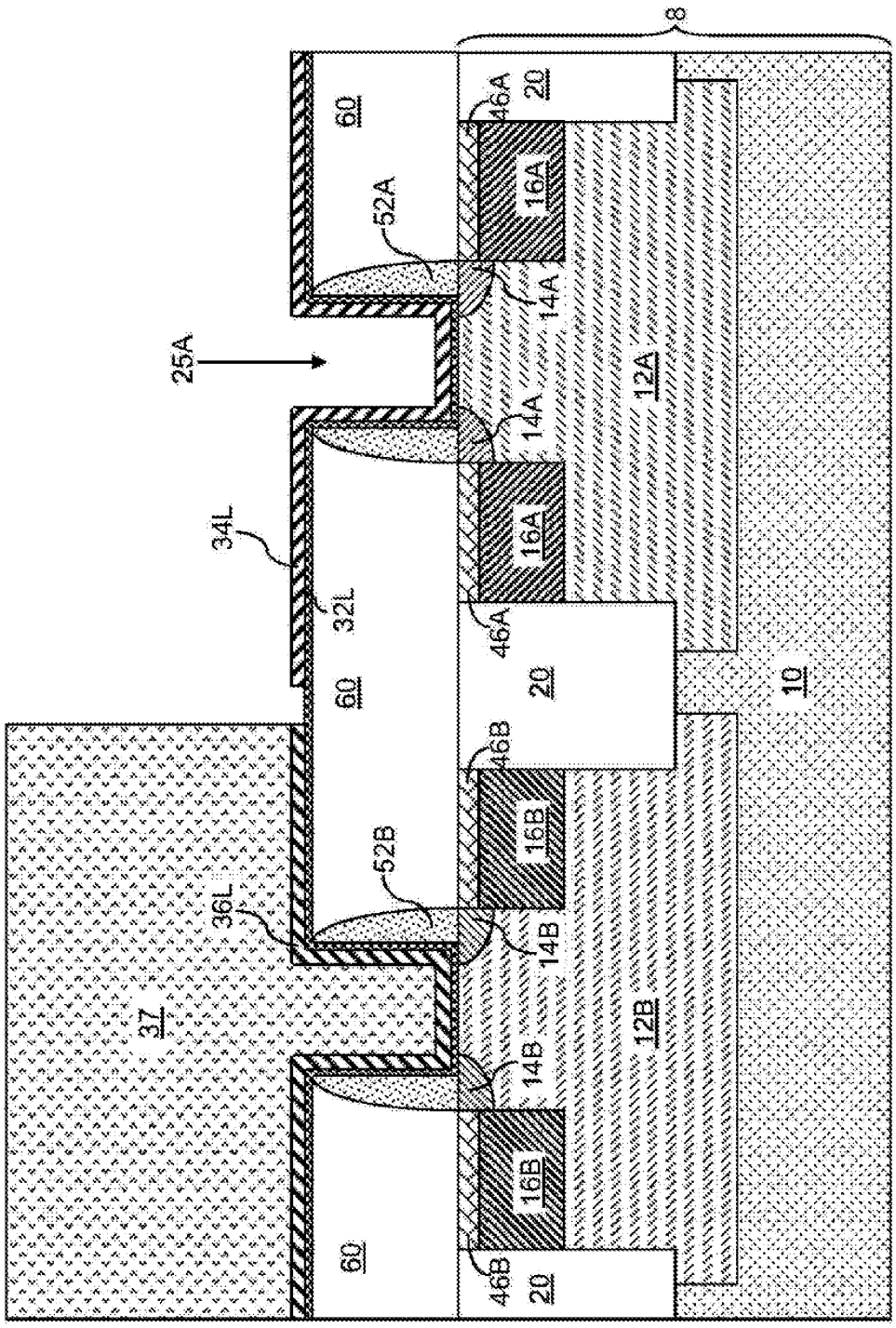

8
60
46A
20
16A
52A
14A
25A
12A
34L
32L
10
46B
16B
52B
36L
37
14B
12B

图 16

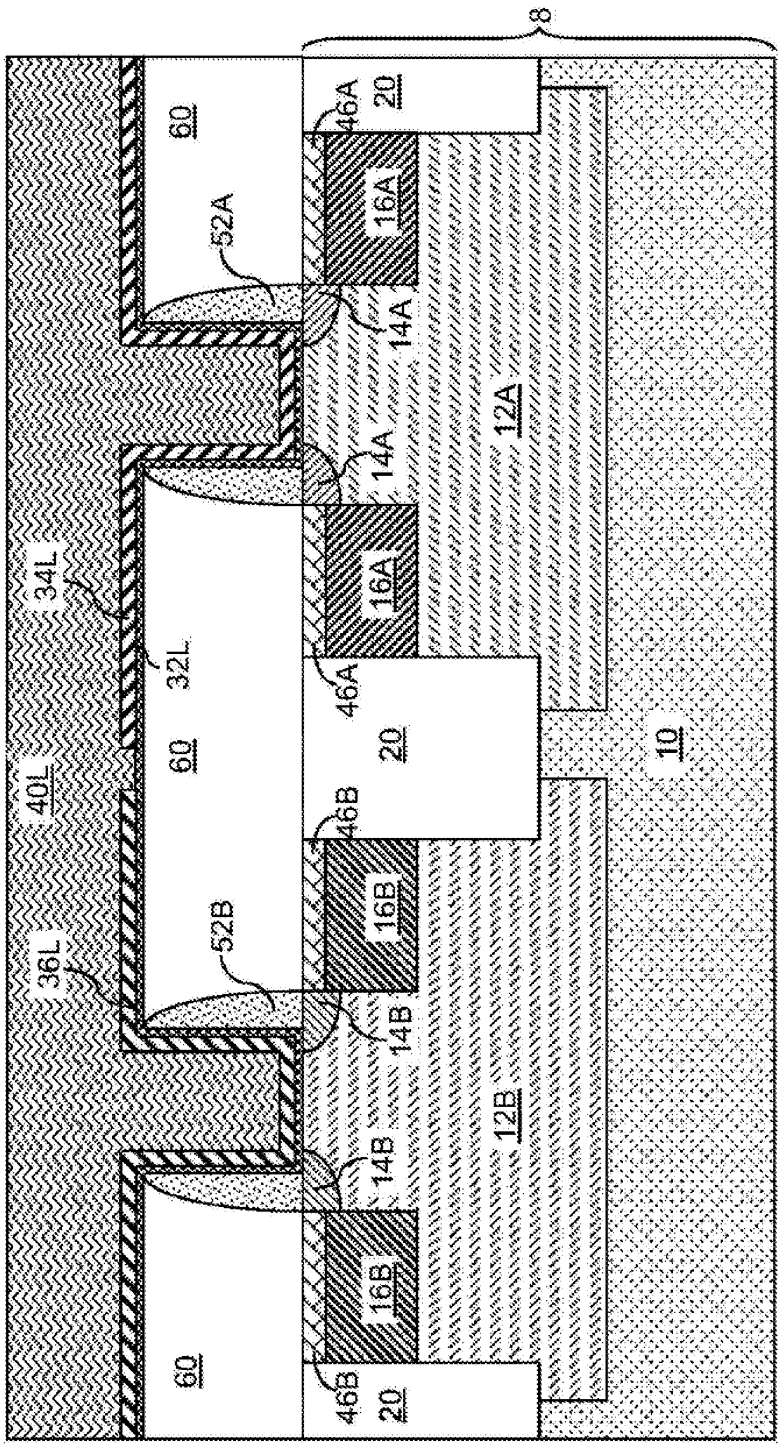


图 17

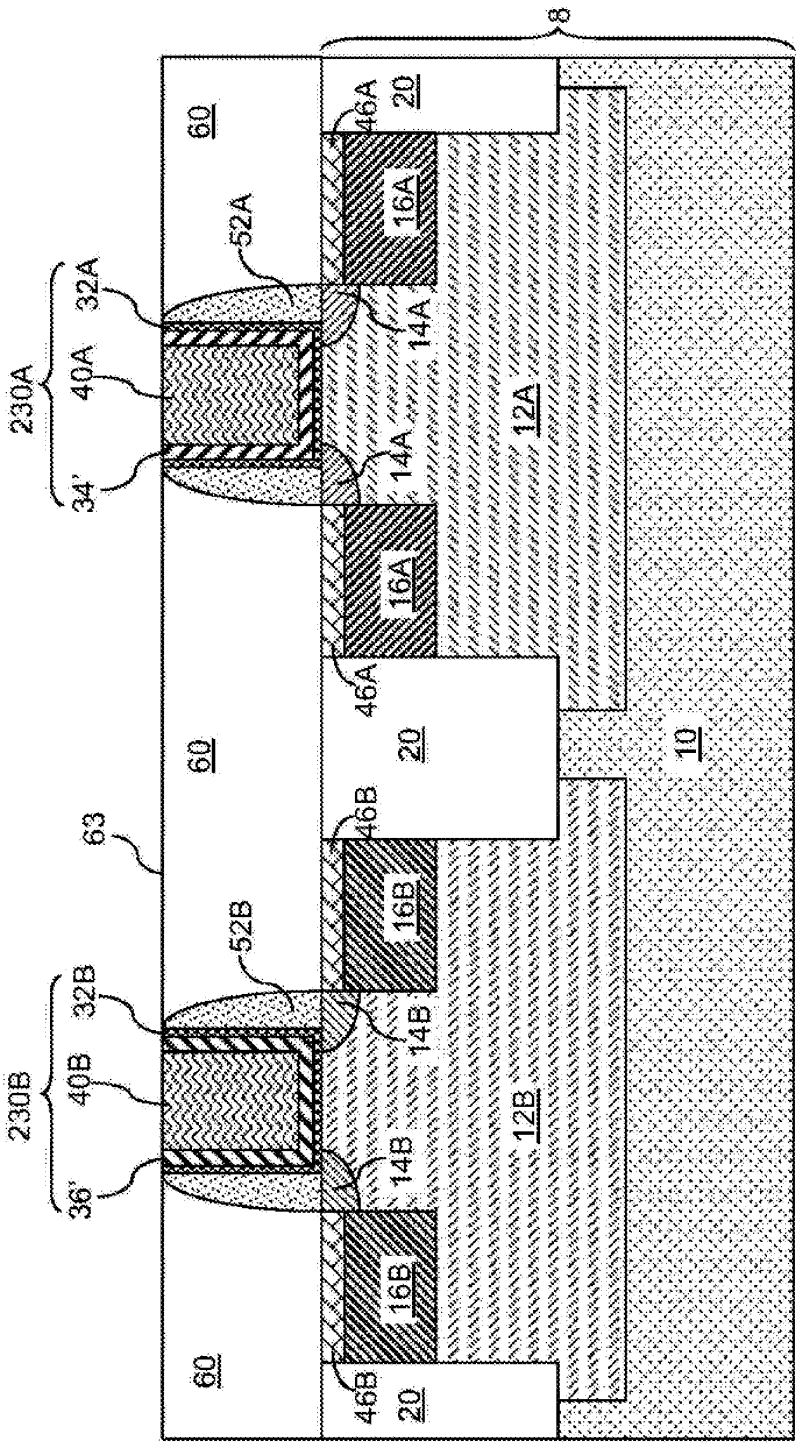

8
60
20
46A
16A
52A
32A
14A
230A
40A
34'
12A
10
63
46B
16B
52B
32B
14B
230B
40B
36'
12B

图 18

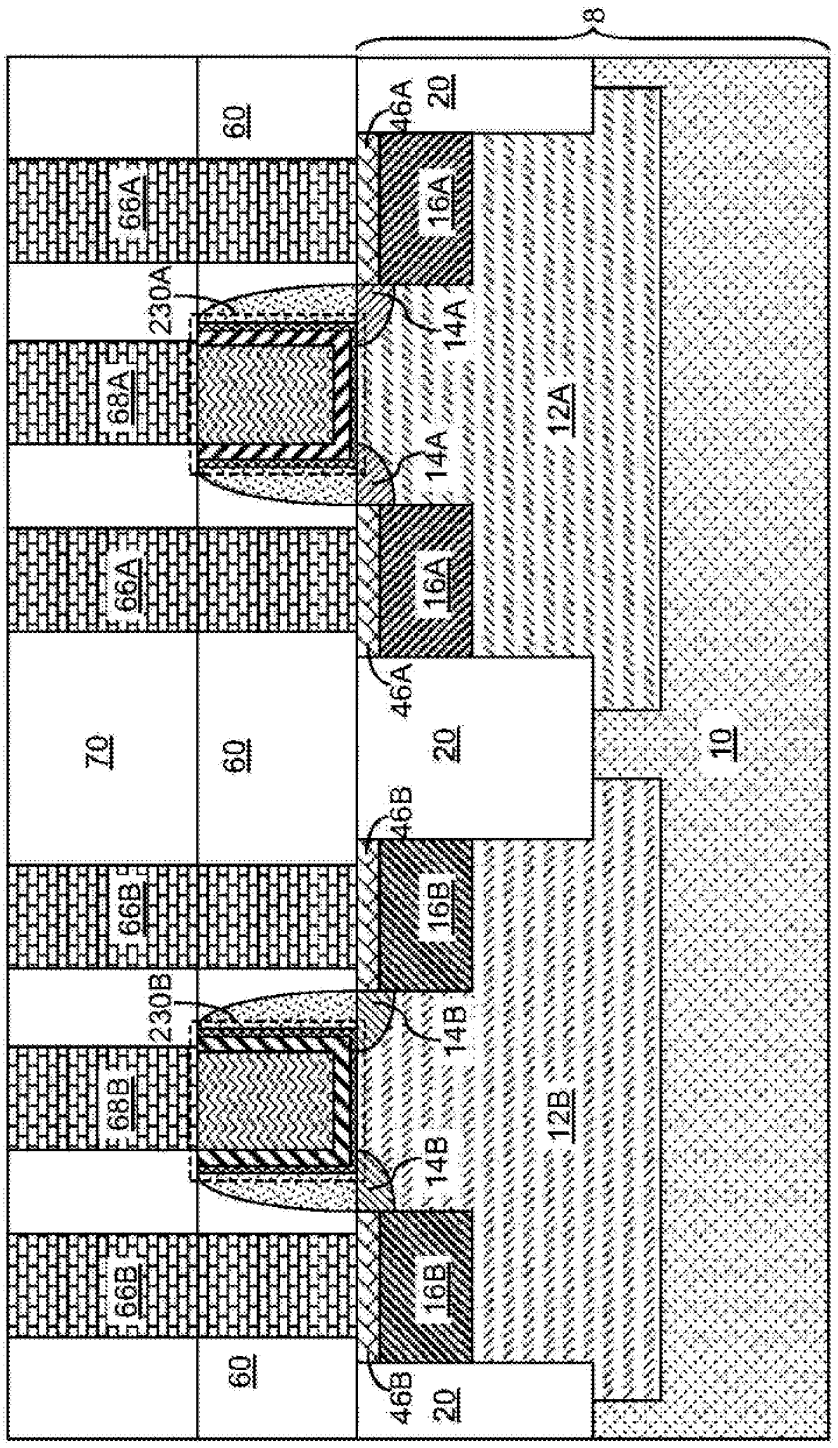

8
60
66A
68A
230A
66A
70
60
66B
68B
230B
66B
60
46A
20
16A
14A
12A
16A
46A
20
46B
16B
14B
12B
16B
46B
20
10

图 19

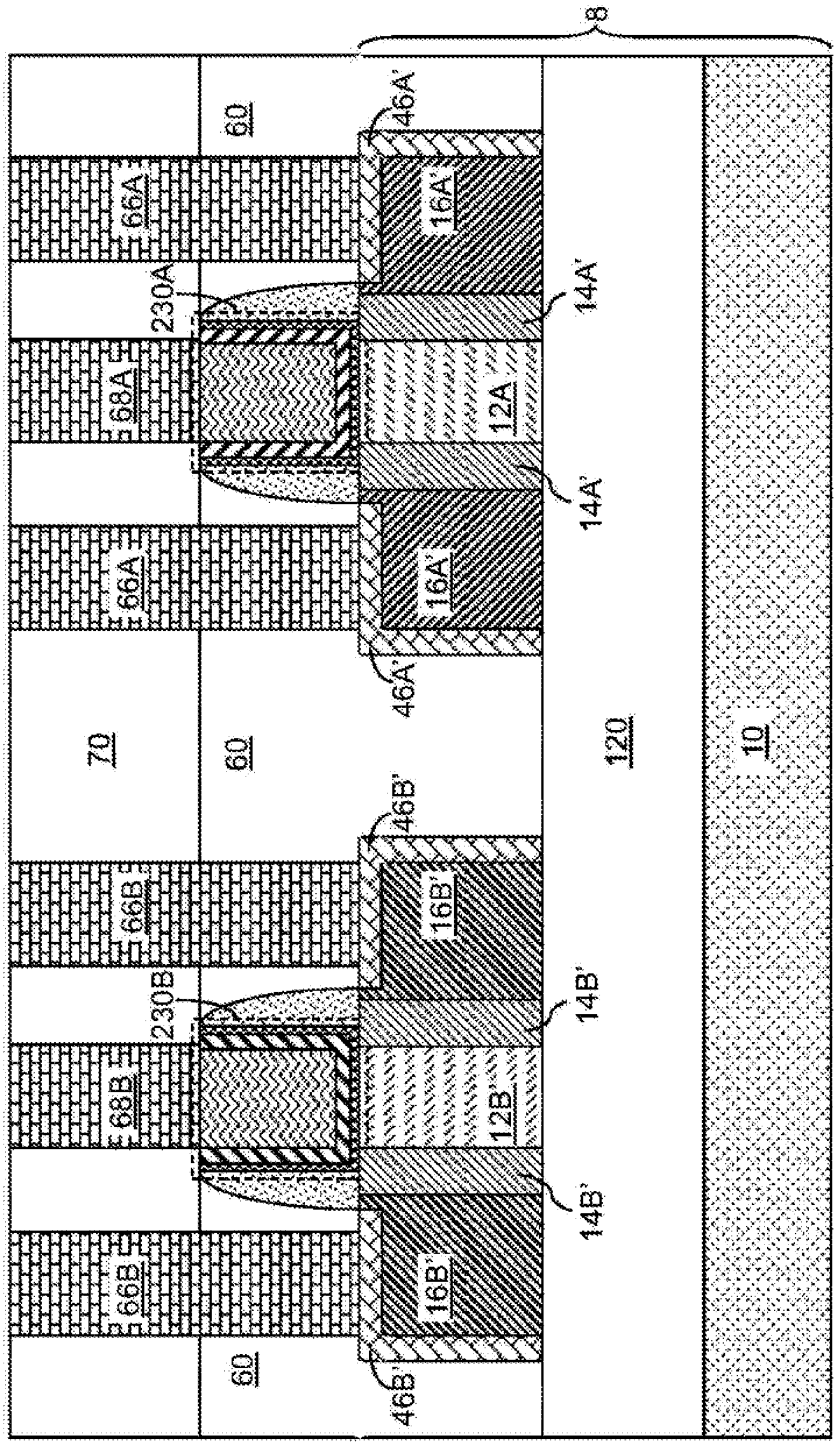

8
60
46A'
16A'
66A
230A
14A'
68A
12A
14A'
66A
16A'
46A'
70
60
120
10
46B'
16B'
66B
230B
14B'
68B
12B'
14B'
66B
16B'
60
46B'

图 20

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Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

[Continued on next page]

(54) Title: METHODS OF INTEGRATING MULTIPLE GATE DIELECTRIC TRANSISTORS ON A TRI-GATE (FINFET) PROCESS

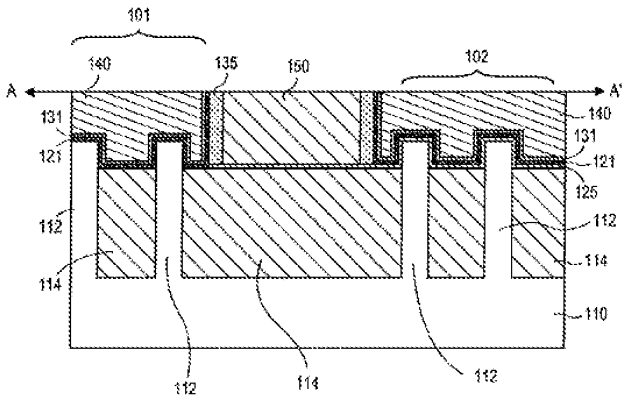


FIG. 1B

(57) Abstract: Two or more types of fin-based transistors having different gate structures and formed on a single integrated circuit are described. The gate structures for each type of transistor are distinguished at least by the thickness or composition of the gate dielectric layer(s) or the composition of the work function metal layer(s) in the gate electrode. Methods are also provided for fabricating an integrated circuit having at least two different types of fin-based transistors, where the transistor types are distinguished by the thickness and composition of the gate dielectric layer(s) and/or the thickness and composition of the work function metal in the gate electrode.

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Published:

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METHODS OF INTEGRATING MULTIPLE GATE DIELECTRIC TRANSISTORS ON A TRI-GATE (FINFET) PROCESS

TECHNICAL FIELD

The present invention relates generally to the manufacture of semiconductor devices, semiconductor logic devices, and transistors. In particular, embodiments of the present invention relate to processes for fabricating a multiple fin-based devices with varied gate structures on the same chip.

BACKGROUND

The desire for ever-smaller integrated circuits (IC) places enormous demands on the techniques and materials used to construct the devices. Components of IC chips include solid-state logic devices (transistors) such as CMOS (complementary metal oxide semiconductor) devices. Recently developed fin-based transistors enable increased performance for a smaller device footprint. Different transistor applications have different structure and performance requirements, for example, high speed logic operations, low power usage, high voltage input output (I/O), and extremely high voltage. Novel processes are required to enable fabrication of multiple types of new fin-based transistors on a single chip.

BRIEF DESCRIPTION OF THE DRAWINGS

Figures 1A-1D illustrate embodiments of dual-gate transistors, wherein each transistor has a different gate stack configuration.

Figures 2A-2B illustrate embodiments of triple-gate transistors, wherein each transistor has a different gate stack configuration.

Figures 3A-3B illustrate embodiments of quad-gate transistors, wherein each transistor has a different gate stack configuration.

Figures 4A-4I illustrate methods for forming a single IC having multiple transistors with different gate stack configurations.

Figures 5A-5I illustrate additional methods for forming a single IC having multiple transistors with different gate stack configurations.

Figures 6A-6G illustrate additional methods for forming a single IC having multiple transistors with different gate stack configurations.

Figures 7A-7E illustrate additional methods for forming a single IC having multiple transistors with different gate stack configurations.

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Figure 8 illustrates a computing device in accordance with one embodiment of the invention.

DETAILED DESCRIPTION

An integrated circuit (IC) structure comprising two or more fin-based field effect transistors, having different types of gate structures, and a method for forming the different types of transistors on a single chip are described. The present invention has been described with respect to specific details in order to provide a thorough understanding of the invention. One of ordinary skill in the art will appreciate that the invention can be practiced without these specific details. In other instances, well known semiconductor processes and equipment have not been described in specific detail in order to not unnecessarily obscure the present invention. Additionally, the various embodiments shown in the figures are illustrative representations and are not necessarily drawn to scale.

Embodiments of the present invention provide an integrated circuit housing a plurality of fin-based transistors having different types of gate structures, and methods for manufacturing these different types of devices on a single circuit. The formation of ICs having a plurality of transistor types can address divergent circuit requirements, such as, for example, high speed logic operation, low power usage, high voltage input output (I/O), and extremely high voltage, which are desirable attributes for components of system-on-a-chip (SOC) integrated circuits. System-on-a-chip devices integrate a wide variety of circuit functions, such as processor cores, analog functions, and mixed signal blocks, onto a single integrated circuit chip. Embodiments of the invention provide ICs with transistors having different types of gate structures, each comprising one or two high k material gate dielectric layers, an oxide (SiO_2) layer, one or two work-function metal layers, a fill metal, and combinations thereof. Transistors with different gate structures are capable of providing performance characteristics that span a wide range of operating speeds, leakage characteristics, and high voltage tolerances. Methods of forming circuits comprising transistors with different gate structures are also disclosed.

Figures 1A-1D illustrate embodiments of fin-based transistors located in an integrated circuit. Each integrated circuit has at least two different transistor types that are distinguished at least by the thickness or composition of the gate dielectric and/or the composition of the work function metal(s) employed in the gate electrode. The transistors may have other distinguishing features. Typically, an integrated circuit having a plurality of different transistor types will have a large number of instances of each type of transistor arranged in various formats (e.g., arrays). For simplicity, one instance of each type of transistor is shown in Figures 1A-1D as an isolated

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transistor, although the transistors illustrated are typically found in various places and arrangements in the integrated circuit chip in which they are located.

Figure 1A illustrates a three-dimensional perspective view of two transistors 101 and 102 formed on the same IC. Figure 1B illustrates a cross-sectional view of transistors 101 and 102 as shown in Figure 1A, taken through the channel regions 116 and gate structures 111A and 111B along line A-A'. Fins 112 extend from semiconductor substrate 110 and, in embodiments, run the full length of substrate 110. In an embodiment, each transistor comprises one or more fins 112 separated by isolation regions 114. In an embodiment, each transistor comprises a gate structure 111 that wraps around the side and top surfaces of a portion of each fin 112, defining a channel region 116. In an embodiment, transistor 101 comprises gate structure 111A, and transistor 102 comprises gate structure 101B, as shown in Figure 1A. Each fin 112 has a pair of source/drain regions 118 disposed on opposite sides of channel region 116, as shown in the embodiment illustrated by Figure 1A. For a PMOS device, the source/drain regions are p-type doped and the channel region is n-type doped. For an NMOS device, the source/drain regions are n-type doped and the channel region is p-type doped. The height of fins 112 above isolation regions 114 ranges from 20 to 100 Å, and the width of fins 112 range from 5 to 20 Å.

Each transistor gate structure 111A and 111B comprises a gate dielectric 113 and a gate electrode 115, as shown in Figure 1A. Each gate dielectric 113 may comprise one or more dielectric layers, for example, a silicon dioxide layer or a high k dielectric layer. The gate dielectric 113 insulates the channel region 116 from the gate electrode 115 to reduce leakage and to set the device threshold voltage. Each gate electrode 115 includes one or more work-function metal layers and may also include a conductive fill metal 140. A work function metal layer manages the barrier height between the dielectric material and the fill metal, minimizing resistance at the metal-semiconductor interface, and setting the work function of the device. The fill metal carries the bulk of the charge that controls the transistor state, and typically is a lower-resistance material than the work function metal(s).

The integrated circuit shown in Figures 1A-D has at least two different types of transistors, 101 and 102 that are distinguished by the composition of the dielectric layers employed in the transistor gate structure. In an embodiment of the invention, the gate structure of transistor 101 comprises a gate dielectric having a high k dielectric layer 121 and a gate electrode having both a work function metal layer 131 and a fill metal 140, as shown in Figure 1B. The type of gate structure in transistor 101 enables use of the transistor for high performance cores.

In an embodiment of the invention, high k dielectric layer 121 conforms to the side and top surfaces of the fins 112 and isolation regions 114 that comprise transistor 101. In general, a high

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k dielectric layer is a dielectric material having a dielectric constant greater than that of silicon dioxide. The dielectric constant of silicon dioxide is 3.9. Exemplary high k dielectric materials that may be used in high-k dielectric layer 121 include hafnium dioxide (HfO_2), hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium dioxide (ZrO_2), zirconium silicon oxide, titanium dioxide (TiO2), tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, and other materials known in the semiconductor art. High k dielectric layer 121 ranges from 10 to 50 Å thick. In an embodiment, high k dielectric layer is 30 Å thick.

Work function metal layer 131 conforms to the surface of high k dielectric layer 121. Exemplary metals that may be used in work function metal layer 131 include titanium nitride, tungsten nitride, tantalum nitride, titanium aluminum, tungsten, silicides and other materials known in the semiconductor art. Work function metal layer 131 ranges from 10 to 50 Å thick. In an embodiment, work function metal layer 131 is 30 Å thick.

Fill metal 140 fills the gate structure opening defined by work function metal layer 131. Fill metal 140 may comprise materials including, for example, metal gate materials, such as, hafnium, zirconium, titanium, titanium nitride, tantalum, aluminum, and combinations thereof. Additional materials include, metal carbides, such as, for example, titanium carbide, zirconium carbide, tantalum carbide, hafnium carbide and aluminum carbide. Further materials that may be used include ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, such as, for example, ruthenium oxide. Other materials are possible.

In an embodiment, the gate structure of transistor 102 has a gate dielectric comprising both a silicon dioxide layer 125 and high k dielectric layer 121, and a gate electrode comprising both work function metal layer 131 and fill metal 140. In an embodiment, silicon dioxide layer 125 is grown from the surfaces of fins 112. In another embodiment, silicon dioxide layer 125 is conformally deposited on fins 112 and isolation region 114. Silicon dioxide layer 125 may be from 5 to 100 Å thick. In an embodiment, silicon dioxide layer 125 is 30 Å thick. In an embodiment, high k dielectric layer 121 covers silicon dioxide layer 125 within the gate structure, and together the two layers form the gate dielectric. In an embodiment, work function metal 131 covers high k dielectric layer 121, and fill metal 140 fills the opening lined by work function metal 131. As compared to the gate structure in transistor 101, the addition of silicon dioxide layer 125 to the gate dielectric enables use of transistor 102 for high voltage, input output (I/O) circuit applications.

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Typically, transistor structures 101 and 102 are at least partially surrounded by a dielectric material 150, as shown in Figure 1B. In some embodiments dielectric material 150 is an interlayer dielectric (ILD) material, such as silicon dioxide or low k dielectric materials. Additional dielectric materials that may be used include carbon doped oxide (CDO), silicon carbide, silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass.

In an embodiment, spacers 135 are located on sidewalls of the gate structure 111. Spacers 135 are formed on the gate structure 111 sidewalls adjacent to the source/drain regions 118, as shown in Figure 1A, in order to isolate the gate structure 111 from epitaxial material grown on fins 112, and also to protect the channel region 116 during heavy doping of the source/drain regions. Spacers 135 may additionally be formed on the ends of each gate structure 111, as shown in Figure 1B. Spacers 135 may be comprised of a suitable dielectric material, such as, for example, silicon nitride, silicon dioxide, silicon oxynitride, or other material known in the semiconductor art.

Another embodiment of the invention comprises at least two different types of fin-based transistors, 101 and 103, where each transistor is distinguished by the composition of the dielectric layers employed in the gate structures, as shown in Figure 1C. In an embodiment of the invention, the gate structure of transistor 101 comprises a gate dielectric having a high k dielectric layer 121 and a gate electrode having both a work function metal layer 131 and a fill metal 140.

The gate structure of transistor 103 comprises a gate dielectric having both a high k dielectric layer 122 and high k dielectric layer 121, and a gate electrode having both work function metal layer 131 and fill metal 140. In an embodiment, high k dielectric layer 122 is formed on the fin surface. In an embodiment, high k dielectric layer 121 covers high k dielectric layer 122. In an embodiment, work function metal layer 131 covers high k dielectric layer 121. In an embodiment, fill metal 140 completes the gate structure by filling in the gate structure opening defined by work function metal layer 131. In an embodiment, high k dielectric layer 122 has a different composition or thickness than high k dielectric layer 121. As compared to the gate structure in transistor 101, the addition of high k dielectric material 122 reduces gate leakage while increasing the threshold voltage, enabling use of transistor 103 for low-power circuits or applications. High k dielectric layer 122 may be any of the materials listed above with respect to high k dielectric layer 121. High k dielectric layer 122 ranges from 10 to 50 Å thick. In an embodiment, high k dielectric layer 122 is 30 Å thick.

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Another embodiment of the invention comprises at least two different types of fin-based transistors, 101 and 104, located on a single integrated circuit, where each type of transistor has a different gate structure, as illustrated by Figure 1D. In an embodiment of the invention, transistors 101 and 104 are distinguished by the composition of the work-function metal(s) employed in each gate electrode. In a specific embodiment, the gate structure of transistor 101 comprises a gate dielectric having a high k dielectric layer 121 and a gate electrode having both a work function metal layer 131 and a fill metal 140.

In an embodiment, the gate structure in transistor 104 comprises a gate dielectric having high k dielectric layer 121 and a gate electrode having a work function metal layer 132, work function metal layer 131 and fill metal 140. In an embodiment, high k dielectric layer 121 covers the fins 112. In an embodiment, work function metal layer 132 covers high k dielectric layer 121. In an embodiment, work function metal layer 131 covers work function metal layer 132. In an embodiment, fill metal 140 fills the gate structure opening defined by work function metal layer 131. In an embodiment, work function metal layer 132 in transistor 104 has a different work function than work function metal layer 131. The addition of work function metal 132, as compared to the gate structure in transistor 101, increases the threshold voltage for transistor 104 and reduces gate leakage, enabling use of transistor 104 for low-power circuits or applications. Work function metal layer 132 may be any of the materials listed above with respect to work function metal layer 131. Work function metal layer 132 may be from 10 to 50 Å thick. In an embodiment, work function metal layer 132 is 30 Å thick.

The embodiments illustrated by Figures 2A-B comprise three or more types of fin-based transistors on a single integrated circuit, where each type of transistor has a different gate structure. Typically, an integrated circuit having a plurality of different types of transistors will have a large number of instances of each type of transistor arranged in various formats (e.g., arrays). For simplicity, one instance of each type of transistor is shown in the figures as an isolated transistor, although the illustrated transistors are typically found in various places and arrangements on the integrated circuit chip in which they are located.

The integrated circuit shown in Figure 2A has at least three different types of transistors, 201, 202, and 203 that are distinguished by the thickness or composition of the dielectric layers employed in the gate structure, according to an embodiment of the invention. In an embodiment, the gate structure in transistor 201 comprises a gate dielectric having high k dielectric layer 221 and a gate electrode having both a work function metal layer 231 and a fill metal 240. Transistor 201 may be used for high performance processor cores. In an embodiment, the gate structure in transistor 202 comprises a gate dielectric having both a silicon dioxide layer 225 on the fin

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surface and high k dielectric layer 221 over silicon dioxide layer 225. In an embodiment, transistor 202 further comprises a gate electrode having work function metal layer 231 and fill metal 240. The addition of silicon dioxide layer 225 reduces leakage and increases the threshold voltage, as compared to transistor 201, enabling use of transistor 202 for high-voltage input output (I/O) circuits or applications. In an embodiment, the gate structure of transistor 203 comprises a gate dielectric having both a high k dielectric layer 222 on fins 212 and high k dielectric layer 221 over high k layer 222. In an embodiment, transistor 202 further comprises a gate electrode having both work function metal layer 231 and fill metal 240. In an embodiment, high k dielectric layer 222 has a different composition than high k dielectric layer 221. In another embodiment, high k dielectric layer 222 has a different thickness than high k dielectric layer 221. The addition of high k dielectric layer 222 to the gate structure reduces leakage, as compared to transistor 201, enabling use of transistor 203 for low-power circuits.

The integrated circuit illustrated in Figure 2B has at least three different types of transistors, 201, 202 and 204, that are distinguished by the composition or thickness of the dielectric layers and/or the composition of the work-function metals employed in the transistor gate structure. In an embodiment, the gate structure in transistor 201 comprises a gate dielectric having high k dielectric layer 221 and a gate electrode having both a work function metal layer 231 and a fill metal 240. Transistor 201 is designed to be used for high performance processor cores. In an embodiment, the gate structure in transistor 202 comprises a gate dielectric having both a silicon dioxide layer 225 on fins 212 and high k dielectric layer 221 on silicon dioxide layer 225. In an embodiment, transistor 202 further comprises both a gate electrode having work function metal layer 231 and fill metal 240. The addition of silicon dioxide layer 225 reduces leakage and increases the threshold voltage, as compared to transistor 201, enabling use of transistor 202 for high-voltage input output (I/O) circuits or applications. In an embodiment, the gate structure of transistor 204 comprises a gate dielectric having high k dielectric layer 221 and a gate electrode having a work function metal layer 232, work function metal layer 231 on work function metal layer 232, and fill metal 240. In an embodiment, work function metal 232 has a different work function than work function metal layer 231. The addition of work function metal layer 232 reduces leakage, as compared to transistor 201, enabling use of transistor 204 for low power circuits or applications.

Circuits comprising at least four types of fin-based transistors, where each type of transistor has a different gate structure, are illustrated in Figures 3A-C, according to embodiments of the invention. The embodiments comprising four types of transistor gate structures, as illustrated in

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Figures 3A-B, are extensions of the three-type transistor embodiments illustrated in Figures 2A-B, and may be fabricated without incurring additional processing steps.

The integrated circuit shown in Figure 3A has at least four different types of transistors, 301, 302, 303 and 305 that are distinguished by the thickness or composition of the dielectric layers employed in the gate structure. In an embodiment, the gate structure in transistor 301 comprises a gate dielectric having a high k dielectric layer 321, and a gate electrode having both a work function metal layer 331 and a fill metal 340. Transistor 301 is designed to be used for high performance processor cores. In an embodiment, the gate structure in transistor 302 comprises a gate dielectric having both a silicon dioxide layer 325 grown on fins 312 and high k dielectric layer 321 over the silicon dioxide layer 325. In an embodiment, transistor 302 further comprises a gate electrode having both work function metal layer 331 and fill metal 340. Transistor 302 is designed to be used for high-voltage input output (I/O) circuits. In an embodiment, the gate structure in transistor 303 comprises a gate dielectric having both a high k dielectric layer 322 on the fin surface and high k dielectric layer 321 over high k dielectric layer 322, and a gate electrode having both work function metal layer 331 and fill metal 340. In an embodiment, the composition of high k dielectric layer 322 is different than that of high k dielectric layer 321. In another embodiment, the thickness of high k dielectric layer 322 is different than that of high k dielectric layer 321. Transistor 303 is designed to be used for low-power circuits.

In an embodiment, the gate structure of transistor 305 comprises a gate dielectric having silicon dioxide layer 325 on the fins, high k dielectric layer 322 over silicon dioxide layer 325, and high k dielectric layer 321 over high k dielectric layer 322. In an embodiment, high k dielectric layer 322 has a different composition than that of high k dielectric layer 321. In another embodiment, high k dielectric layer 322 has a different thickness than that of high k dielectric layer 321. In an embodiment, transistor 305 further comprises a gate electrode having work function metal layer 331 and fill metal 340. As compared to the high-performance gate structure in transistor 301, the additions of silicon dioxide layer 325 and high k dielectric layer 322 increase the threshold voltage of transistor 305, such that transistor 305 may be used for circuits requiring extremely high voltages.

Another embodiment of a circuit having multiple types of transistors is illustrated by Figure 3B. The integrated circuit has at least four types different transistors, 301, 302, 304 and 306, that are distinguished at least by the thickness or composition of the dielectric layers and/or the composition of the work function metals employed in the gate structure. In an embodiment, the gate structure in transistor 301 comprises a gate dielectric having a high k dielectric layer 321

and a gate electrode having both a work function metal layer 331 and a fill metal 340. Transistor 301 is designed to be used for high performance processor cores. In an embodiment, the gate structure in transistor 302 comprises a gate electrode having both a silicon dioxide layer 325 grown on fins 312 and high k dielectric layer 321 over silicon dioxide layer 325. In an embodiment, transistor 302 further comprises a gate electrode having both work function metal layer 331 and fill metal 340. Transistor 302 is designed to be used for high-voltage input output (I/O) circuits. In an embodiment, the gate structure in transistor 304 comprises gate dielectric having a high k dielectric layer 321 and a gate electrode having a work function metal layer 332 layer, work function metal 331 layer over the work function metal layer 332 layer, and fill metal 340. In an embodiment, work function metal layer 332 has a different work function than work function metal 331. Transistor 304 is designed to be used for low-power circuits.

In an embodiment, the gate structure in transistor 306 comprises a gate dielectric having both silicon dioxide layer 325 grown on fins 312 and high k dielectric layer 321 over silicon dioxide layer 325. In an embodiment, transistor 306 further comprises a gate electrode having work function metal layer 332, work function metal layer 331 over work function metal layer 332, and fill metal 340. In an embodiment, work function metal layer 332 has a different work function than work function metal layer 331. As compared to the high-performance gate structure in transistor 301, the additions of silicon dioxide layer 325 and work function metal layer 332 increase the threshold voltage of transistor 306, such that transistor 306 may be used for circuits requiring extremely high voltages.

With respect to the previously described embodiments, it should be noted that it is also possible to vary other device characteristics such as the width of the gate, the width of the channel region, and the types of sources and drains used to achieve specific transistor properties, as is understood by those of skill in the art.

In manufactured devices, layers of materials can deviate in appearance from the simplified illustrations provided herein for clarity, and can be, for example, slightly thicker or thinner in areas. Additionally, what is described here as a "layer" of material may be made up of a plurality of layers of the material that essentially function as one layer.

Figures 4A-I describe an embodiment of a method for the formation of multiple types of fin-based transistor gate structures. The method is useful for forming integrated circuits comprising different types of fin-based transistors on the same chip, wherein the transistors have at least two different gate dielectric structures. An integrated circuit chip typically comprises multiple copies of the same transistor in various locations on the substrate, however, one of each type of transistor is shown in Figures 4A-I for clarity.

A substrate 410 having fins 412 is provided. In an embodiment of the invention, fins 412 are formed from a bulk monocrystalline substrate. Substrate 410 and fins 412 can be formed of any well known semiconductor material, such as but not limited to silicon, germanium, silicon germanium, and III-V combinations including GaAs, InSb, GaP, and GaSb. The lower portions of fins 412 are separated by isolation regions 414 to prevent leakage from the fins, as shown in Figure 4A. In an embodiment, isolation regions 414 comprise a dielectric material such as silicon dioxide. In another embodiment, fins 412 are formed from a semiconductor-on-insulator (SOI) substrate comprising a lower bulk substrate, a middle insulation layer, and a top monocrystalline layer. Fins 412 are formed from the top monocrystalline layer, and the middle insulation layer forms an isolation region. The height of fins 412 extending above isolation regions 414 range from 20 to 100 Å. The width of fins 412 range from 5 to 20 Å.

Next, silicon dioxide layer 425 is formed on the surface of fins 412 extending above isolation regions 414. In an embodiment, silicon dioxide layer 425 will form a portion of the gate dielectric for the transistor formed on gate region 492. In an embodiment, silicon dioxide layer 425 will subsequently be removed from gate region 491 prior to forming additional gate structure components. In a specific embodiment, silicon dioxide layer 425 is grown from the surfaces of fins 412. In another specific embodiment, silicon dioxide layer 425 is blanket deposited by any method that enables conformal deposition on the fins 412 in the gate regions, such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). Silicon dioxide layer 425 may be grown or deposited to a uniform thickness. In an embodiment, silicon dioxide layer 425 is 30 Å thick.

The subsequent etching process to remove silicon dioxide layer 425 from gate region 491 involves two sacrificial layers that protect portions of silicon dioxide layer 425 that will form active components of the device formed in gate region 492. In an embodiment of the invention, an embedded etch stop layer 442 is blanket deposited over the surface of the substrate, and a sacrificial silicon dioxide layer 443 is conformally formed over embedded etch stop layer 442. In an embodiment of the invention, embedded etch stop layer 442 and sacrificial silicon dioxide layer 443 will not form active components of the transistors. Embedded etch stop layer 442 and silicon dioxide layer 443 may each be deposited by any method suitable for forming a conformal layer, such as CVD or ALD. In an embodiment, embedded etch stop layer 442 is a material that is etched at a slower rate as compared to that of silicon dioxide when both are etched by a selected etch chemistry. In an embodiment, embedded etch stop layer 442 is silicon nitride.

Both embedded etch stop layer 442 and silicon dioxide layer 443 are each formed to a uniform thickness. The thicknesses of the embedded etch stop layer 442 and silicon dioxide

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layer 443 are each selected such that a timed etch will remove each layer in approximately the same time. In an embodiment, an HF etching process is used. HF etches silicon dioxide at a faster rate than silicon nitride, and therefore, in an embodiment, sacrificial silicon dioxide layer 443 is thicker than embedded etch stop layer 442. In an embodiment, sacrificial silicon dioxide layer 443 is the same thickness as silicon dioxide layer 425. In an embodiment, embedded etch stop layer 442 is 10 Å thick. In an embodiment, silicon dioxide layer 443 is 30 Å thick.

Next, sacrificial silicon dioxide layer 443 is removed from the surface of gate region 491 using a photolithographic etch process. In an embodiment, a photoresist material is formed over the structure surface. The photoresist is photolithographically patterned so that photoresist 455 covers gate region 492, as shown in Figure 4C, where a gate structure comprising silicon dioxide layer 425 will subsequently be formed. The exposed portion of silicon dioxide layer 443 is then etched from gate structure 491. Silicon dioxide layer 443 may be etched by any suitable etching process, such as a wet etch. The wet etch comprises, for example, HF. The HF etch may have a concentration from 50:1-200:1. In an embodiment, silicon dioxide layer 443 is fully or nearly fully etched from the surface of gate region 491 in 50 seconds.

After the etching of silicon dioxide layer 443, photoresist 455 is removed from the structure surface, as shown in Figure 4D. In general, photoresists are removed by well known processes in the semiconductor industry. Photoresists can be removed, for example, through dry plasma processes. The resist is removed in an oxygen plasma processes, frequently called ashing, designed to remove organic residues. The plasma is generated, for example, by microwave, RF (radio frequency), or UV ozone sources. Alternately, the photoresist can be removed using a solvent or mixture of solvents.

Next, sacrificial gate material 454 is blanket deposited over the structure surface, according to the embodiment illustrated in Figure 4E. Sacrificial gate material 454 is formed to a thickness desired for the gate height. Sacrificial gate material 454 is then patterned and etched to form sacrificial gate structures 456 over gate regions 491 and 492, so that active gate structures may subsequently be formed by a gate replacement process. Deposition, patterning, and etching of sacrificial gate material are well known in the semiconductor art. The sacrificial gate structures 456 are patterned into the same shape and at the same location where the subsequently formed gate electrode and gate dielectric are to be formed. In an embodiment of the present invention, the sacrificial gate electrode material is formed from a material such as silicon nitride or polysilicon. Following the formation of sacrificial gate structures 456, fins 412 may be doped, for example, by tip implantation or halo implantation, as is well-known in the art.

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Next, if desired, dielectric sidewall spacers 435 may be formed on the sidewalls of sacrificial gate structures 456. Sidewall spacers are used to isolate the gate structure from epitaxial semiconductor material that may be grown on the source/drain regions of the fins, as shown in Figure 1A, but spacer material may additionally form on other sidewalls of the gate structure, as shown in Figure 4F. Sidewall spacers 435 can be formed by any well known technique, such as, for example, by blanket depositing a conformal sidewall spacer dielectric over the substrate, and then anisotropically etching to remove the dielectric spacer material from horizontal surfaces while leaving spacer material on vertical surfaces. The spacers 453 may be silicon nitride, silicon oxide, silicon oxynitride, silicon carbide, CDO or a combination thereof. In an embodiment, an overetch is used to remove spacer material from the sidewalls of fins 412 to enable subsequent growth of an epitaxial layer on the fin surface, doping of the source/drain region, and/or formation of source/drain contacts.

Next, a dielectric material 450 is blanket deposited over the substrate. The dielectric material is formed to a thickness sufficient to completely cover the substrate including sacrificial gate structure 456. The dielectric 450 is formed of a material that can be selectively etched with respect to the sacrificial gate material. That is, the dielectric is formed of a material whereby the sacrificial gate structure 456 can be removed without significantly etching away the dielectric 450. After blanket deposition, the dielectric material 450 is planarized, such as by chemical mechanical planarization (CMP), until the top surface is planar with the sacrificial gate structure 456.

The sacrificial gate structure 456 is then etched away to enable formation of the gate structures in gate regions 491 and 492. Sacrificial gate structures 456 may be removed using a wet or dry etch process. The etch process exposes underlying embedded etch stop layer 442 surface on gate region 491 and underlying sacrificial silicon dioxide layer 443 surface on gate region 492, as shown in Figure 4G.

In an embodiment, an additional etch process removes embedded etch stop layer 442 and silicon dioxide layer 425 from gate region 491 and also sacrificial silicon dioxide layer 443 and embedded etch stop layer 442 from gate region 492. In an embodiment, a selective etch is used. In another embodiment, a timed wet etch is used. In an embodiment, the timed wet etch may comprise HF. In a specific embodiment, the HF etches embedded etch stop layer 442 material at a faster rate over the sacrificial silicon dioxide 443 material. The etch process has, in an embodiment, a selectivity of 3:1. The HF etch may have a concentration from 50:1-200:1. Because the thickness of each sacrificial layer has been selected based on the rate at which HF etches the material, both embedded etch stop layer 442 and silicon dioxide layer 425 on gate

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region 491 are etched completely or nearly completely by the HF in the same amount of time that sacrificial silicon dioxide layer 443 and embedded etch stop layer 442 are etched by the HF from gate region 492.

In an embodiment, silicon dioxide layer 425 remains on gate region 492, where it will form part of the gate dielectric. As such, silicon dioxide layer 425 has been formed on gate region 492, without being exposed photoresist, which may contaminate active device layers. This formation of a pristine silicon dioxide layer will improve the performance and reliability of the device over that of devices where active layers are patterned directly using a photolithography process.

Next, a high-k dielectric layer 421 is conformally deposited over the substrate surface to a uniform thickness according to an embodiment of the invention. In an embodiment, high k dielectric material 421 covers the top surface and sidewalls of fins 412 in gate region 491 and conforms to the silicon dioxide layer 425 surface on gate region 492. In an embodiment, high k dielectric layer 421 will form part of the gate dielectric in the gate structures formed in both gate regions 491 and 492. In an embodiment, the high k dielectric material is formed by a conformal process, such as CVD or ALD, to ensure contact with the fin surfaces in gate region 491 and the underlying silicon dioxide layer 425 in gate region 492. High k dielectric layer 421 may be any suitable high k dielectric material, such as described above with respect to high k dielectric layer 121 in Figure 1A. High k dielectric layer 421 may be from 10 to 50 Å thick. In an embodiment, high k dielectric material 421 is 30 Å thick.

Next, a gate electrode is formed in each gate region, over the gate dielectric. The gate electrode may comprise one or more work function metal layers and a fill metal. In an embodiment, work function metal 431 is conformally deposited over the substrate to a uniform thickness. Work function metal 431 sets the work function for the device, and minimizes resistance at the metal-semiconductor interface between the gate dielectric and the gate electrode. Work function metal 431 is formed by a conformal process, such as CVD or ALD to ensure contact with the underlying high k dielectric layer 421 in both gate regions 491 and 492. Work function metal layer 431 may be any suitable work function metal, such as described above with respect to work function metal layer 131 in Figure 1A. Work function metal layer 431 may be from 10 to 50 Å thick. In an embodiment, work function metal layer 431 is 30 Å thick.

A fill metal 440 is then blanket deposited over work function metal 431 to a thickness sufficient to fill the gate structure openings in gate regions 491 and 492. Metal gate 440 may be formed by any suitable process, such as CVD, ALD, or physical vapor deposition (PVD). The

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metal gate material may be any suitable gate electrode material, such as described above with respect to Figure 1A.

The metal gate 440, work function material 431, and high k dielectric layer 421 are then chemically mechanically planarized until the top surface of the dielectric layer 450 is revealed as shown in Figure 4I. Once the gate electrode material and gate dielectric material are polished back or removed from the top dielectric material 450, a gate structure has been formed.

Thus, two transistors 401 and 402 are formed, each with a different gate structure. In an embodiment, Transistor 401 comprises a gate dielectric having a high-k material 421 and a gate electrode having both a work function metal 431 and fill metal 440. Transistor 401 may be used for high-performance processor cores. In an embodiment, transistor 402 comprises a gate dielectric having both a silicon dioxide layer 425 and high k dielectric layer 421 and a gate electrode having work function metal layer 431 and fill metal 440. The addition of silicon dioxide layer 425 to the gate dielectric, as compared to the gate dielectric of transistor 401, enables use of transistor 402 for high voltage input-output (I/O) circuits or applications.

Figures 5A-I illustrate another method for forming integrated circuits comprising two types of transistors that have different gate structures. An integrated circuit chip typically comprises multiple copies of the same transistor in various locations, however, one of each type of transistor is shown in Figures 5A-I for clarity.

A substrate 510 having fins 512 is provided, as shown in Figure 5A. In an embodiment, substrate 510 and fins 512 are monocrystalline silicon. Fins 512 are separated by isolation regions 514, which may comprise a dielectric material such as, for example, silicon dioxide. Methods for forming the structure shown in Figure 5A are known in the art of semiconductor manufacturing.

Next, silicon dioxide layer 525 is formed on the surface of the structure. In an embodiment of the invention, silicon dioxide layer 525 will form part of the gate structure subsequently formed in gate region 592. In a specific embodiment, silicon dioxide layer 525 is grown from the surfaces of fins 512. In another specific embodiment, silicon dioxide layer 525 is deposited by any method that enables conformal deposition on the horizontal and vertical surfaces of the gate region, such as CVD or ALD. In an embodiment, silicon dioxide layer 525 is 30 Å thick.

Sacrificial gate structures are then formed so that active gate structures may subsequently be formed by a gate replacement process, according to an embodiment of the invention. In an embodiment, sacrificial gate material 554 is blanket deposited over silicon dioxide layer 525, as shown in Figure 5B. Sacrificial gate material 554 is formed to a thickness desired for the gate height. Sacrificial gate material 554 is then patterned and etched to form sacrificial gate

structures 556 over gate regions 591 and 592. Deposition, patterning, and etching of sacrificial gate material are well known in the semiconductor art. The sacrificial gate structures 556 are patterned into the same shape and at the same location where the subsequently formed gate electrode and gate dielectric are to be formed. In an embodiment of the present invention, sacrificial gate structure 556 is formed from a material such as silicon nitride or polysilicon. Following the formation of sacrificial gate structures 556, fins 512 may be doped, for example, by tip implantation or halo implantation, as is well-known in the art.

Next, if desired, dielectric sidewall spacers 535 may be formed on the sidewalls of sacrificial gate structures 556. Sidewall spacers are used to isolate the gate structure from epitaxial semiconductor material that may be grown on the source/drain regions of the fins, as shown in Figure 1A, but spacer material may additionally form on other sidewalls of the gate structure, as shown in Figure 5C. Sidewall spacers 535 can be formed by any well known technique, such as, for example, by blanket depositing a conformal sidewall spacer dielectric over the substrate, and then anisotropically etching to remove the dielectric spacer material from horizontal surfaces while leaving spacer material on vertical surfaces. The spacers 553 may be silicon nitride, silicon oxide, silicon oxynitride, silicon carbide, CDO or a combination thereof. In an embodiment, an overetch is used to remove spacer material from the sidewalls of fins 512 to enable subsequent growth of an epitaxial layer on the fin surface, doping of the source/drain region, and/or formation of source/drain contacts.

Next, a dielectric material 550 is blanket deposited over the substrate. The dielectric layer is formed to a thickness sufficient to completely cover the substrate including sacrificial gate structure 556. The dielectric layer 550 is formed of a material that can be selectively etched with respect to the sacrificial gate material. That is, the dielectric material is formed of a material whereby the sacrificial gate structure 556 can be removed without significantly etching away the dielectric layer 550. After blanket depositing the dielectric, the dielectric layer is planarized, for example, by CMP, until the top surface of the dielectric film is planar with the sacrificial gate structure 556.

Next, the sacrificial gate structures 556 are etched away to enable formation of gate structures within gate regions 591 and 592. Sacrificial gate structures 556 may be etched using a wet or dry etch process. Etching sacrificial gate structures 556 exposes silicon dioxide layer 525 within gate regions 591 and 592, as shown in Figure 5D. In an embodiment, the gate dielectric formed in gate region 592 will comprise silicon dioxide layer 525, but the gate structure formed in gate region 592 will not comprise silicon dioxide layer 525. Thus, silicon dioxide layer 525 is subsequently patterned to remove the portion within gate region 591, while protecting the

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portions within gate region 592. In another specific embodiment of the invention, all exposed portions of silicon dioxide layer 525 are etched away from the surface, and a fresh silicon dioxide layer is either grown from the fins or deposited over the substrate, in order to have pristine silicon dioxide with which to form active components of a subsequently formed gate structure.

A hardmask 534 is then blanket deposited over silicon dioxide layer 525, as illustrated in Figure 5E. In an embodiment, hardmask 534 will protect the portion of silicon dioxide layer 525 within gate region 592 from exposure to photoresist during etching of the portion of silicon dioxide layer 525 within gate region 591. Hardmask 534 may comprise, for example, a work function metal resistant to etching by HF, such as, but not limited to titanium nitride, tungsten nitride, and tantalum nitride. In an embodiment, hardmask 534 is formed by ALD. Hardmask 534 is formed to a uniform thickness sufficient to protect underlying materials during the subsequent etching processes, from 10 to 50 Å thick. In an embodiment, hardmask 534 is 30 Å thick.

Next, hardmask 534 is patterned to remove the portion covering silicon dioxide layer 525 within gate region 591, as shown in Figure 5F. In an embodiment, hardmask 534 is patterned by a photolithography process. In an embodiment, a photoresist layer 555 is deposited and patterned such that hardmask 534 on gate region 592 is covered by photoresist. In an embodiment, hardmask 534 is then etched from regions not covered by the photoresist, exposing the underlying silicon dioxide layer 525 on gate region 591. In an embodiment, hardmask 534 is etched using a wet etch process which is highly selective to the underlying oxide, such as peroxide and sulfuric acid.

Next, the photoresist layer 545 is removed, leaving hardmask 534 on gate region 592. In an embodiment, silicon dioxide layer 525 is then etched from gate region 591. By removing photoresist layer 545 prior to etching silicon dioxide layer 525, the etching bath used to etch silicon dioxide layer 525 is not contaminated by the photoresist material. In an embodiment, etching silicon dioxide layer 525 over gate region 591 exposes the surfaces of fins 512 and isolation regions 514 in gate region 591. Any etch selective to the hardmask material over silicon dioxide may be used to etch silicon dioxide layer 525. In an embodiment, silicon dioxide layer 525 is etched using HF. In an embodiment, hardmask 534 is then removed from gate region 592 to expose silicon dioxide layer 525, as shown in Figure 5H. In an embodiment, hardmask 534 is removed by a wet etch process, such as peroxide and sulfuric acid.

The gate structure is then formed by depositing additional gate dielectric layers and gate electrode materials. In an embodiment, a high k dielectric layer 521 is conformally deposited

over the substrate, covering the top surface and sidewalls of the fins in gate region 591 and conforming to the silicon dioxide layer 525 surface on gate region 592. The high k dielectric material is formed by a conformal process, such as CVD or ALD, to ensure contact with the fins in gate region 591 or with underlying first silicon dioxide layer 525 in gate region 592. High k dielectric layer 521 may be any suitable high k dielectric material, such as described above with respect to high k dielectric layer 121 in Figure 1A. High k dielectric layer 521 may be from 10 to 50 Å thick. In an embodiment, high k dielectric material 521 is 30 Å thick.

Next, the gate electrodes are formed. Each gate electrode may comprise one or more work function metal layers and a fill metal. In an embodiment, work function metal 531 is conformally deposited over the substrate. Work function metal 531 is formed by a conformal process, such as CVD or ALD to ensure contact with underlying high k dielectric layer 521. Work function metal layer 531 may be any suitable work function metal, such as described above with respect to work function metal layer 131 in Figure 1A. Work function metal layer 531 may be from 10 to 50 Å thick. In an embodiment, work function metal layer 531 is 30 Å thick.

Next, the fill metal 540 material is blanket deposited over work function metal 531 to a thickness sufficient to fill the gate structure openings within gate regions 591 and 592. Fill metal 540 may be formed by any suitable process, such as CVD, ALD, or PVD. The fill metal material may be any suitable gate electrode material, such as described above with respect to fill metal 140 in Figure 1A.

The fill metal 540, work function material 531, and high k dielectric layer 521 are then chemically mechanically planarized until the top surface of the dielectric layer 550 is revealed as shown in Figure 5I. Once the gate electrode material and gate dielectric material are polished back or removed from the top dielectric material 550, a gate structure has been formed.

Thus, two transistors 501 and 502 are formed, each with a different gate structure. In an embodiment, transistor 501 comprises a gate dielectric having high k dielectric material 521 and a gate electrode having both work function metal 531 and fill metal 540. The gate structure of transistor 501 may be used for high-performance processor cores. In an embodiment, transistor 502 comprises a gate dielectric having a silicon dioxide layer 525 and high k dielectric layer 521 over silicon dioxide layer 525, and a gate electrode having both work function metal 531 and fill metal 540. As compared to transistor 501, the additional silicon dioxide material in the gate dielectric of transistor 502 enables use for high voltage input-output (I/O) circuits.

Figures 6A-G provide an additional embodiment of a method for forming integrated circuits comprising two types of transistors, where each transistor type has a different gate dielectric structure. An integrated circuit chip typically comprises multiple copies of the same

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transistor in various locations, however, one of each type of transistor is shown in Figures 6A-G for clarity.

A structure comprising substrate 610 with fins 612 separated by isolation regions 614 and gate structure openings above the fins defined by a dielectric 650 having spacers 635 is provided. Methods for forming the structure are known in the art of semiconductor manufacturing. The structure may be formed, for example, by first following the process shown in Figures 5A-5D and described above, and then removing the portions of the silicon dioxide layer 625 that cover gate regions 691 and 693, as shown in Figure 6A. In an embodiment, silicon dioxide layer 625 is removed from gate regions 691 and 693 by wet or dry etch.

Next, a high k dielectric layer 622 is blanket deposited over the substrate. High k dielectric material 622 is formed by a conformal process, such as CVD or ALD, to ensure contact with the fins in each gate region. In an embodiment, high k dielectric layer 622 will form part of the gate dielectric for the transistor formed in gate region 693. In an embodiment, high k dielectric layer 622 will be removed from gate region 691. High k dielectric layer 622 may be any suitable high k dielectric material, such as described above with respect to high k dielectric layer 122 in Figure 1B. High k dielectric layer 622 may be from 10 to 50 Å thick. In an embodiment, high k dielectric material 622 is 30 Å thick.

A hardmask 634 is then blanket deposited over high k dielectric layer 622, as illustrated in Figure 6B. In an embodiment, hardmask 634 will protect the portion of high k dielectric layer 622 within gate region 693 from exposure to photoresist during the subsequent etching of high k dielectric layer 622 from gate region 691. Hardmask 634 may comprise, for example, a work function metal resistant to etching by HF, such as, but not limited to titanium nitride, tungsten nitride, and tantalum nitride. In an embodiment, hardmask 634 is formed by ALD. Hardmask 634 is formed to a uniform thickness sufficient to protect underlying materials during the subsequent etching processes, from 10 to 50 Å thick. In an embodiment, hardmask 634 is 30 Å thick.

Next, hardmask 634 is patterned to remove the portion covering high k dielectric layer 622 within gate region 691, as shown in Figure 6C. In an embodiment, hardmask 634 is patterned by a photolithography process. In an embodiment, a photoresist layer 655 is deposited and patterned such that hardmask 634 on gate region 693 is covered by photoresist. Hardmask 634 is then etched to expose high k dielectric layer 622 in gate region 691. In an embodiment, hardmask 634 is etched using a wet etch process that is highly selective to the underlying oxide, such as peroxide and sulfuric acid.

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The photoresist layer 655 is then removed, leaving hardmask 634 on gate region 693. The exposed portion of high k dielectric layer 622 over gate region 691 is then etched to expose the surfaces of fins 612 and isolation regions 614 in gate region 691, as shown in Figure 6D. By removing photoresist layer 655 prior to etching high k dielectric layer 622 on gate region 691, the etching bath used to etch high k dielectric layer 622 is not contaminated by the photoresist material. Any etch selective to the hardmask material over the high k dielectric material may be used to etch high k layer 622. In an embodiment, high k dielectric layer 622 is etched using HF. In an embodiment, hardmask 634 is then removed from gate region 693 to expose the surface of high k dielectric layer 622, as shown in Figure 6E. In an embodiment, hardmask 634 is removed by a wet etch process, such as peroxide and sulfuric acid.

Next, a high k dielectric layer 621 is conformally deposited over the structure. In an embodiment, high k dielectric layer 621 will form part of the gate dielectric for each of the transistors formed in gate regions 691 and 693. In gate region 691, high k dielectric material 621 covers the fins 612 and isolation regions 614 within the gate structure opening, and in gate region 693, high k dielectric layer 621 conforms to high k dielectric layer 622. High k dielectric material 621 is formed by a conformal process, such as CVD or ALD, to ensure contact with underlying materials in the gate region. In an embodiment, high k dielectric layer 621 has a different composition than high k dielectric layer 622. In another embodiment, high k dielectric layer 621 has a different thickness than high k dielectric layer 622. High k dielectric layer 621 comprises a high k dielectric material such as described above with respect to high k dielectric layer 121 in Figure 1A. High k dielectric layer 621 may be from 10 to 50 Å thick. In an embodiment, high k dielectric material 621 is 30 Å thick.

Next, a gate electrode is formed. The gate electrode may comprise one or more work function metal layers and a fill metal. In an embodiment, work function metal layer 631 is deposited over the substrate to a uniform thickness. Work function metal layer 631 is formed by a conformal process, such as CVD or ALD, to ensure contact with underlying high k dielectric layer 621. Work function metal layer 631 may be any suitable work function metal, such as described above with respect to work function metal layer 131 in Figure 1A. Work function metal layer 631 may be from 10 to 50 Å thick. In an embodiment, work function metal layer 631 is 30 Å thick.

Next, the fill metal 640 is blanket deposited over work function metal 631 to a thickness sufficient to fill the gate structure openings over gate regions 691 and 693. Fill metal 640 may be formed by any suitable process, such as CVD, ALD, or PVD. The fill metal may be any

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suitable gate electrode material, such as described above with respect to fill metal 140 in Figure 1A.

The fill metal 640, work function material 631, high k dielectric layer 621 and high k dielectric layer 622 are then chemically mechanically planarized until the top surface of the dielectric layer 650 is revealed as shown in Figure 6G. Once the gate electrode materials and gate dielectric materials are polished back or removed from the top of dielectric material 650, a gate structure has been formed.

Thus, two different transistors 601 and 603 are formed, each with a different gate structure. In an embodiment, transistor 601 comprises a gate dielectric having high k material 621 and a gate electrode having work function metal 631 and fill metal 640. The gate structure of transistor 601 enables use for high-performance processor cores. In an embodiment, transistor 603 comprises a gate dielectric having a high k dielectric layer 622 and high k dielectric layer 621, and a gate electrode having work function metal layer 631 and fill metal 640. The dual high k materials enable use of transistor 603 for low-power circuits or applications.

Figures 7A-E provide an additional embodiment of a method for forming integrated circuits comprising two types of transistors, where each transistor type has a different gate electrode structure. An integrated circuit chip typically comprises multiple copies of the same transistor in various locations, however, one of each type of transistor is shown in Figures 7A-E for clarity.

A structure comprising substrate 710 with fins 712 separated by isolation regions 714 and gate structure openings above the fins, defined by dielectric material 750 and spacers 735 is provided. Methods for forming the structure are known in the art of semiconductor manufacturing. The structure may be formed, for example, by first following the process shown in Figures 5A-5D and described above, and then removing the portions of the silicon dioxide layer 725 that cover gate regions 791 and 794, as shown in Figure 7A.

Next, portions of the gate structures are formed by depositing a gate dielectric layer in gate regions 791 and 794. A high k dielectric layer 721 is blanket deposited on the structure surface, as illustrated in Figure 7B, covering fins 712 and isolation regions 714 within gate regions 791 and 794. The high k dielectric material 721 is formed by a conformal process, such as CVD or ALD, to ensure uniform formation on the surface of fins 712. High k dielectric layer 721 comprises a high k dielectric material such as described above with respect to high k dielectric layer 121 in Figure 1A. High k dielectric layer 721 may be from 10 to 50 Å thick. In an embodiment, high k dielectric material 721 is 30 Å thick.

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Next, work function metal 732 is blanket deposited over the structure, as shown in Figure 7B. In an embodiment, work function metal layer 732 will form part of the gate electrode for the transistor gate structure formed in gate region 794. In an embodiment, work function metal layer 732 will be subsequently removed from gate region 791. In an embodiment, work function metal 732 conforms to the surface of high k dielectric material 721. The work function metal may be deposited by a conformal process, such as CVD or ALD. Work function metal layer 732 may be any suitable work function metal, such as described above with respect to Figure 1A. In an embodiment, work function metal layer 732 is nitridized after deposition to alter the work function of the material. Work function metal layer 732 may be from 10 to 50 Å thick. In an embodiment, work function metal layer 732 is 30 Å thick.

Work function metal layer 732 is then patterned to remove the portion within gate region 791. In an embodiment, work function layer 732 is patterned using photolithography. In an embodiment, photoresist layer 755 is deposited and patterned such that the portion of work function metal layer 732 in gate region 794 is covered by photoresist. In an embodiment, work function metal layer 732 is then etched away from gate region 791 to expose the underlying high k dielectric material 721, as shown in Figure 7C. Work function metal layer 732 may be etched with either a dry etch or a wet etch process.

Next, photoresist 755 is removed and work function metal layer 731 is blanket deposited over the substrate. Work function metal layer 731 is formed by a conformal process, such as CVD or ALD to ensure contact with the underlying high k dielectric layer 721 on gate region 791 and the work function metal layer 732 on gate region 794. Work function metal layer 731 may be any suitable work function metal, such as described above with respect to Figure 1A. In an embodiment, work function metal 731 has a different work function than work function metal layer 732. Work function metal layer 731 may be from 10 to 50 Å thick. In an embodiment, work function metal layer 731 is 30 Å thick.

Next, fill metal 740 is blanket deposited over work function metal 731 to a thickness sufficient to fill the gate structure openings over gate regions 791 and 794. Fill metal 740 may be formed by any suitable process, such as CVD, ALD, or PVD. The fill metal may be any suitable gate electrode material, such as described above with respect to Figure 1A.

Fill metal 740, work function metal 731, work function metal 732, and high k dielectric layer 721 are then chemically mechanically planarized until the top surface of the dielectric 750 is revealed as shown in Figure 7E. Once the gate electrode materials and gate dielectric materials are polished back or removed from the top dielectric material 750, a gate structure has been formed.

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Thus, two different transistors 701 and 704 are formed, each with a different gate structure. In an embodiment, the gate structure of transistor 701 comprises a gate dielectric having high k material 721 and a gate electrode having both work function metal layer 731 and fill metal 740. Transistor 701 may be used for high-performance processor cores. In an embodiment, the gate structure of transistor 704 comprises a gate dielectric having high k material 721 and a gate electrode having work function metal 732, work function metal 731, and fill metal 740. Transistor 704 may be used in low-power circuits or applications.

The above processes, as described with reference to Figures 4A-I, 5A-I, 6A-G, and 7A-E can be used in combination to form integrated circuits with three or more types of transistors, each having a different gate structure.

Figure 8 illustrates a computing device 800 in accordance with one implementation of the invention. The computing device 800 houses a board 802. The board 802 may include a number of components, including but not limited to a processor 804 and at least one communication chip 806. The processor 804 is physically and electrically coupled to the board 802. In some implementations the at least one communication chip 806 is also physically and electrically coupled to the board 802. In further implementations, the communication chip 806 is part of the processor 804.

Depending on its applications, computing device 800 may include other components that may or may not be physically and electrically coupled to the board 802. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

The communication chip 806 enables wireless communications for the transfer of data to and from the computing device 800. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 806 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth,

derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 800 may include a plurality of communication chips 806. For instance, a first communication chip 806 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 806 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 804 of the computing device 800 includes an integrated circuit die packaged within the processor 804. In some implementations of the invention, the integrated circuit die of the processor includes two or more fin-based transistors in accordance with implementations of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

The communication chip 806 also includes an integrated circuit die packaged within the communication chip 806. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes two or more fin-based transistors in accordance with implementations of the invention.

In further implementations, another component housed within the computing device 800 may contain an integrated circuit die that includes two or more fin-based transistors in accordance with implementations of the invention.

In various implementations, the computing device 800 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 800 may be any other electronic device that processes data.

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CLAIMS

What is claimed is:

1. A device comprising,
a substrate having a plurality of semiconductor fins;
a first transistor having a first gate structure that wraps around one or more of the semiconductor fins, wherein the first gate structure comprises a first gate dielectric structure in contact with the semiconductor fins and a first gate electrode structure in contact with the first gate dielectric structure; and
a second transistor having a second gate structure that wraps around one or more of the semiconductor fins.

2. The device of claim 1, wherein the first gate dielectric structure comprises a first high k dielectric layer and wherein the first gate electrode structure comprises a first work function metal layer and a fill metal.

3. The device of claim 2, wherein the second gate structure comprises a second gate dielectric structure and the first gate electrode structure, and wherein the second gate dielectric structure comprises a silicon dioxide layer and the first high k dielectric layer.

4. The device of claim 2, wherein the second gate structure comprises a third gate dielectric structure and the first gate electrode structure, and wherein the third gate dielectric structure comprises a second high k dielectric layer and the first high k dielectric layer.

5. The device of claim 2, wherein the second gate dielectric comprises the first gate dielectric structure and a second gate electrode structure, and wherein the second gate electrode structure comprises the first work function metal layer and a second work function metal layer.

6. The device of claim 2, further comprising a third transistor, wherein the third transistor has a third gate structure comprising the third gate dielectric structure and the first gate electrode structure.

7. The device of claim 2, further comprising a third transistor, wherein the third transistor has a third gate structure comprising the first gate dielectric structure and the second gate

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electrode structure.

8. The device of claim 6, further comprising a fourth transistor, wherein the fourth transistor has a fourth gate structure comprising a fourth gate dielectric structure and the first gate electrode structure, wherein the fourth gate dielectric structure comprises the silicon dioxide layer, the first high k dielectric layer, and the second high k dielectric layer.

9. The device of claim 7, further comprising a fourth transistor, wherein the fourth transistor has a fourth gate structure comprising the second gate dielectric structure and the second gate electrode structure.

10. A method, comprising:

providing a substrate having a plurality of semiconductor fins, each with a channel region disposed therein, wherein a first gate region spans the channel regions of one or more of the semiconductor fins, and wherein a second gate region spans the channel regions of one or more of the semiconductor fins;

growing a first silicon dioxide layer on the semiconductor fins within the first gate region and the second gate region;

blanket depositing an embedded etch stop layer within the first gate region and the second gate regions and over the first silicon dioxide layer;

blanket depositing a second silicon dioxide layer over the embedded etch stop layer;

etching to remove the second silicon dioxide layer from the first gate region using a first etch process; and

etching using a second etch process to remove the embedded etch stop layer and the first silicon dioxide layer from the first gate region and to remove the second silicon dioxide layer and the embedded etch stop layer from the second gate region.

11. The method of claim 10, wherein the second etch process comprises a timed wet etch.

12. The method of claim 11, wherein the timed wet etch comprises HF.

13. The method of claim 10, further comprising:

forming a first dummy gate structure within the first gate region, in contact with the semiconductor fins;

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forming a second dummy gate structure within the second gate region, in contact with the first silicon dioxide layer;

blanket depositing a dielectric layer; and

polishing the dielectric layer to expose the first dummy gate and second dummy gate.

14. The method of claim 10, wherein the embedded etch stop layer is silicon nitride.

15. A method, comprising:

providing a substrate having a plurality of semiconductor fins, each with a channel region disposed therein, wherein a first gate region spans the channel regions of one or more of the semiconductor fins, and wherein a second gate region spans the channel regions of one or more of the semiconductor fins;

blanket depositing a dielectric layer over the fins within the first gate region and the second gate region;

blanket depositing a hardmask layer over the dielectric layer;

patterning the hardmask layer to remove the hardmask layer from the first gate region;

patterning the exposed dielectric layer to remove the dielectric layer from the first gate region;

removing the hardmask layer from the second gate region.

16. The method of claim 15, wherein patterning the hardmask comprises:

forming a photoresist layer over the first gate region and the second gate region;

patterning the photoresist layer to expose the hardmask layer on the first gate region;

etching the exposed portion of the hardmask from the first gate region; and

removing the photoresist layer.

17. The method of claim 15, further comprising

forming a first dummy gate structure within the first gate region, in contact with the semiconductor fins; and

forming a second dummy gate structure within the second gate region, in contact with the first silicon dioxide layer;

blanket depositing a dielectric layer; and

polishing the dielectric layer to expose the first dummy gate and second dummy gate.

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18. The method of claim 17, wherein the dielectric layer is silicon dioxide.

19. The method of claim 15, wherein the first gate region and second gate region have been formed using a replacement gate process.

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20. The method of claim 19, wherein the dielectric layer is a high k dielectric material.

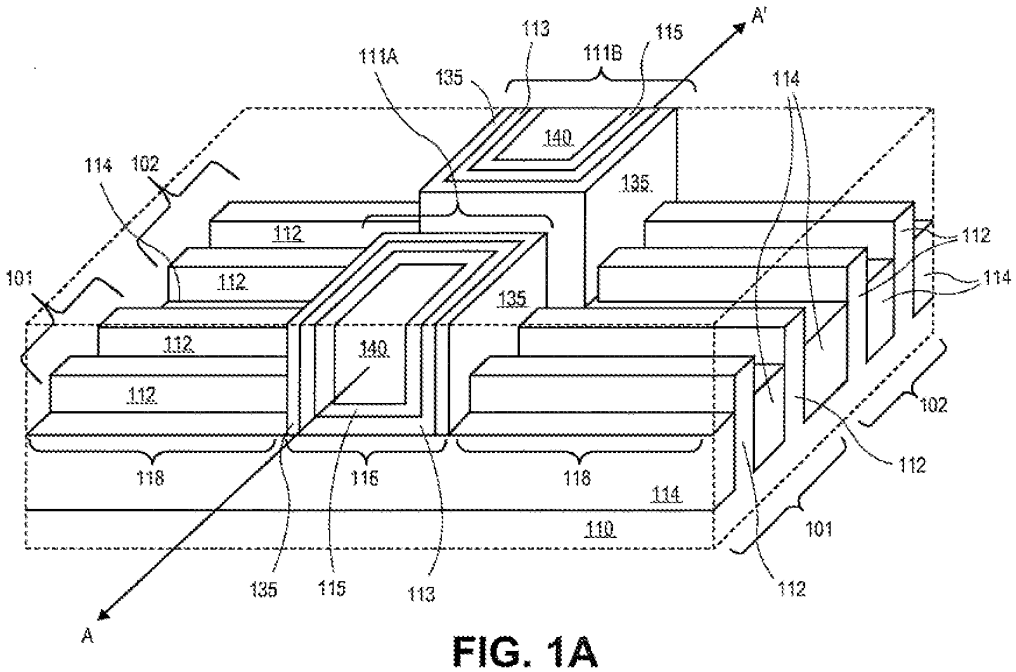

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FIG. 1A

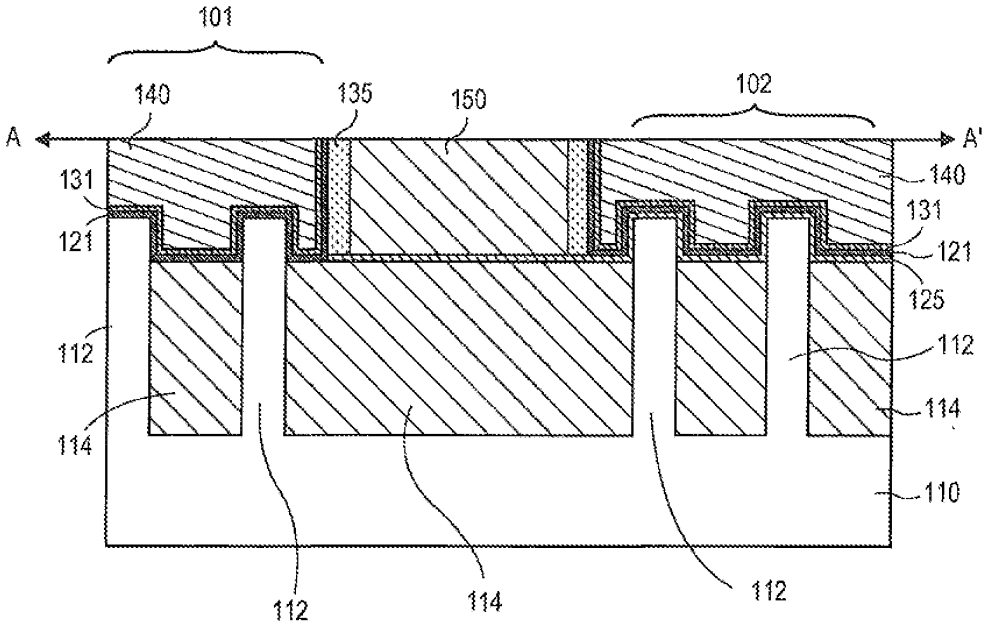

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FIG. 1B

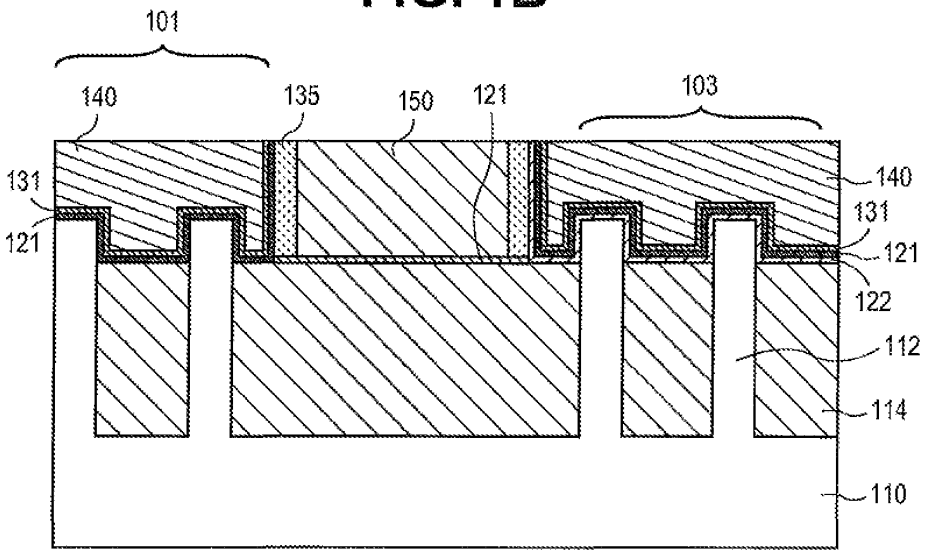

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FIG. 1C

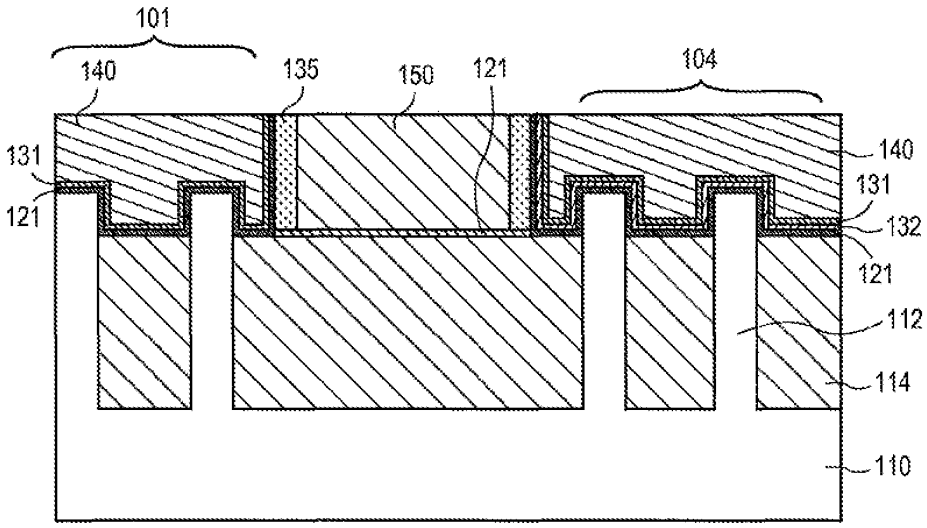


FIG. 1D

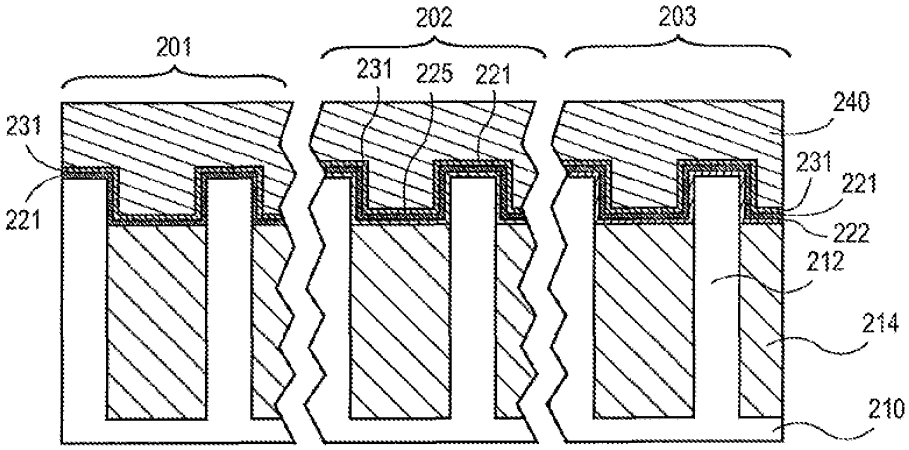

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FIG. 2A

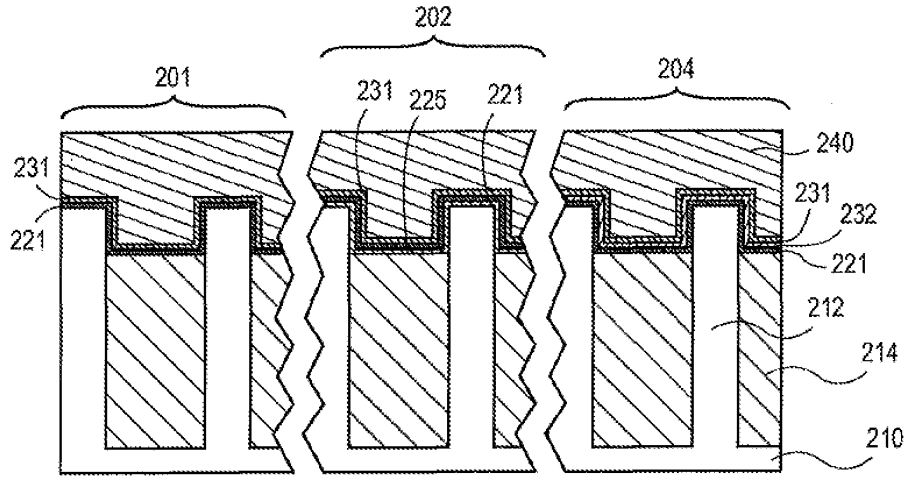

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FIG. 2B

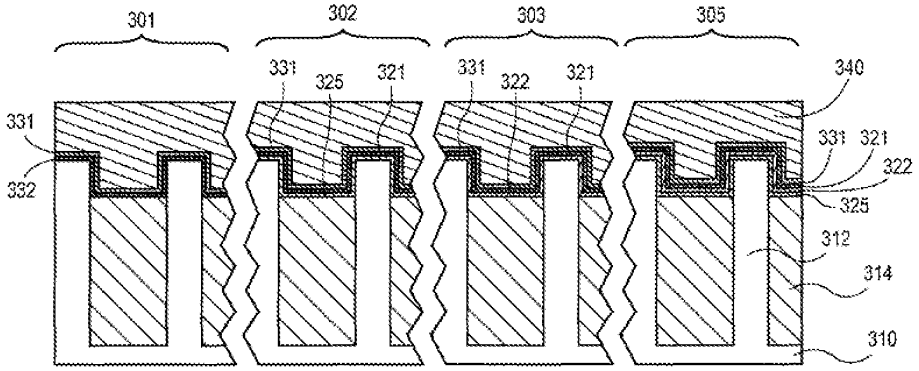

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FIG. 3A

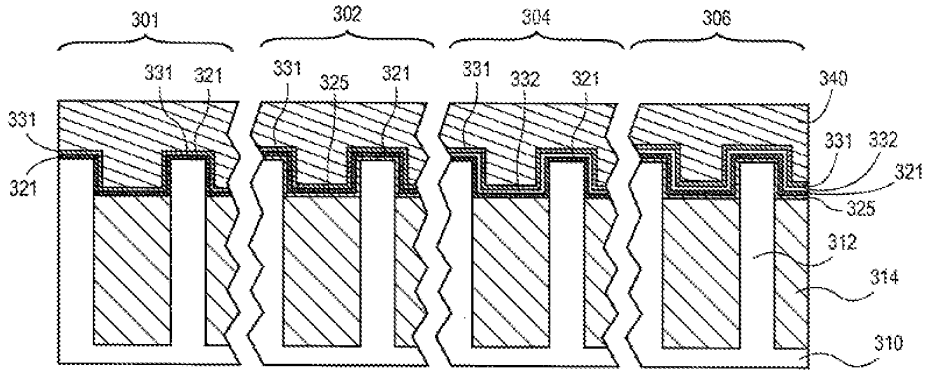

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FIG. 3B

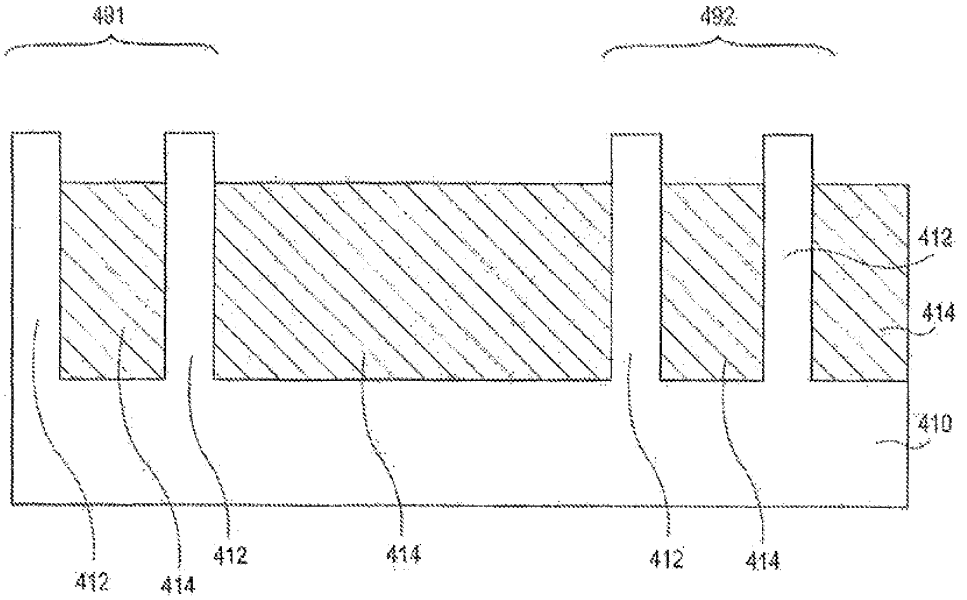

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FIG. 4A

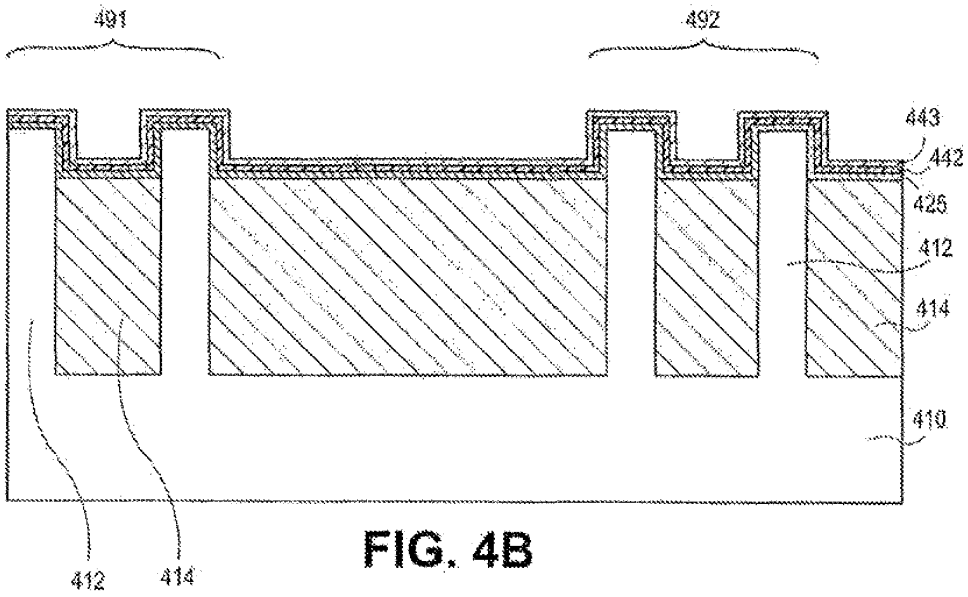

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FIG. 4B

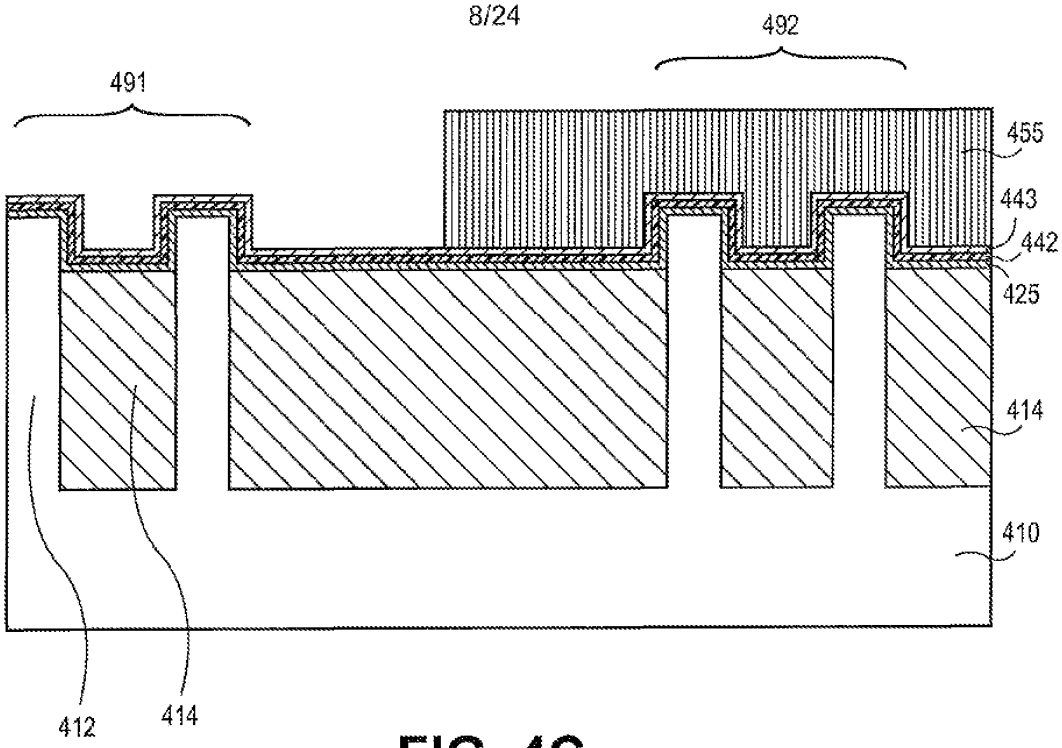

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FIG. 4C

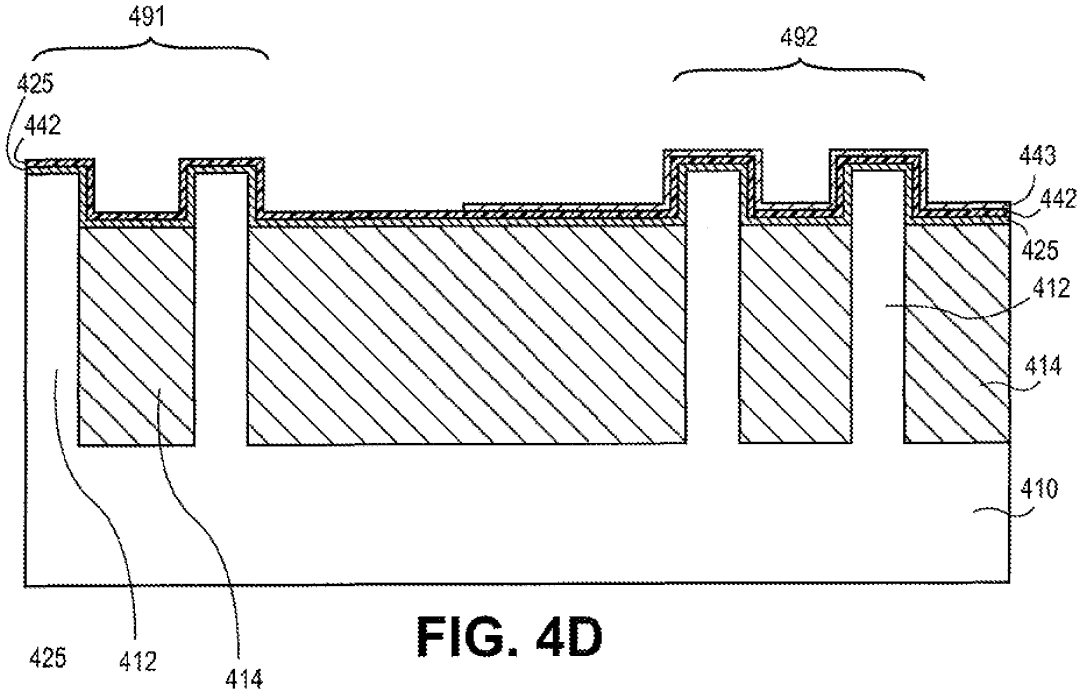

491
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FIG. 4D

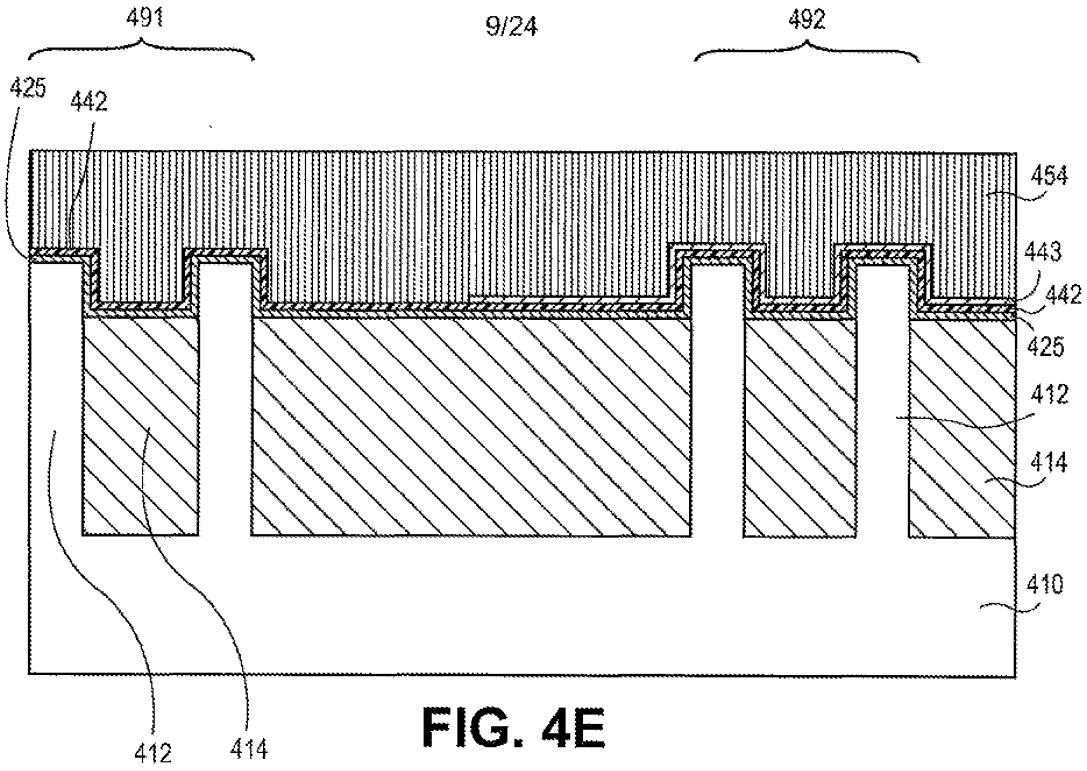

491
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FIG. 4E

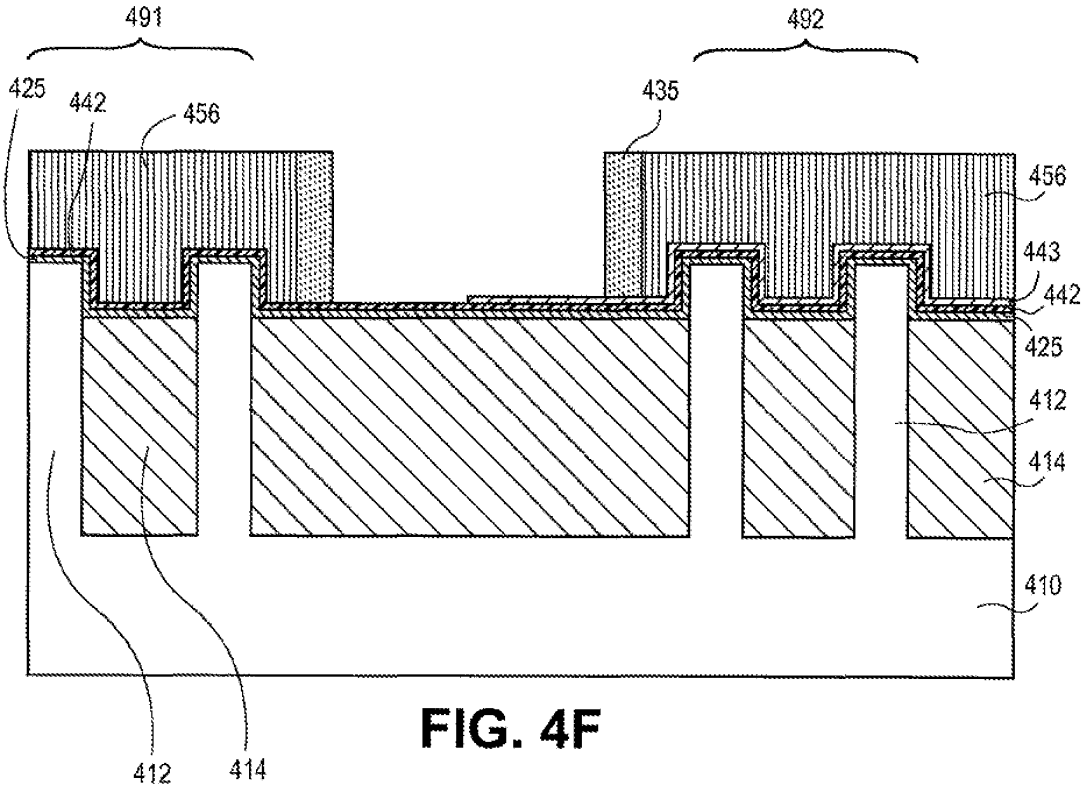

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FIG. 4F

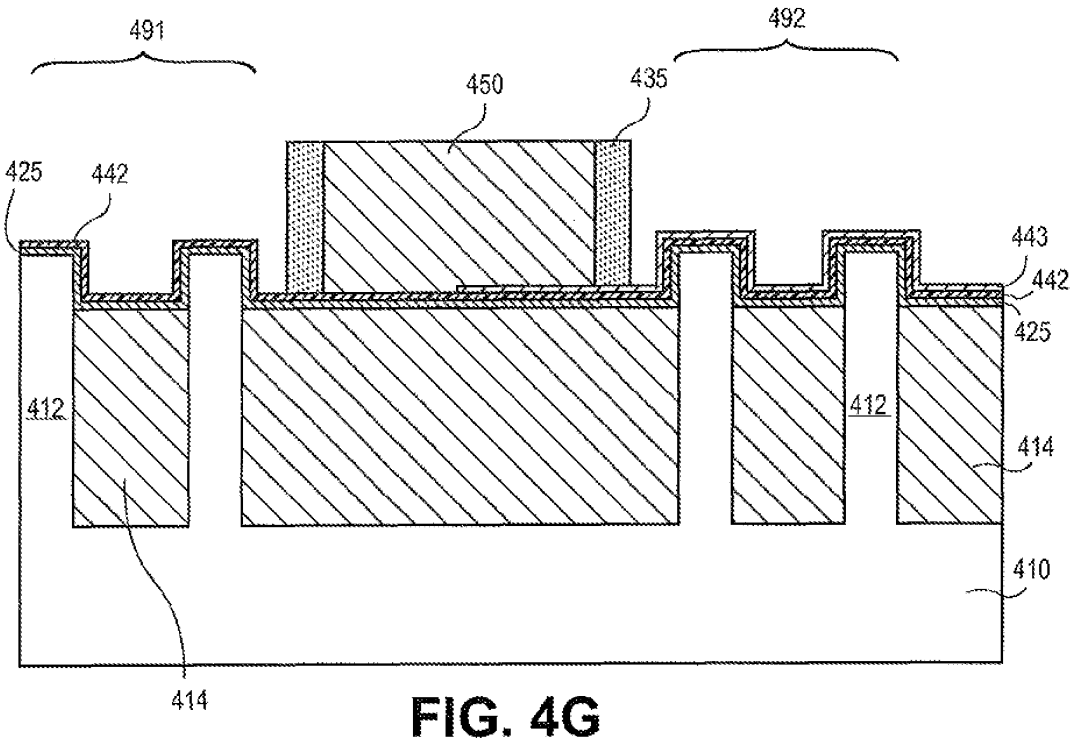

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FIG. 4G

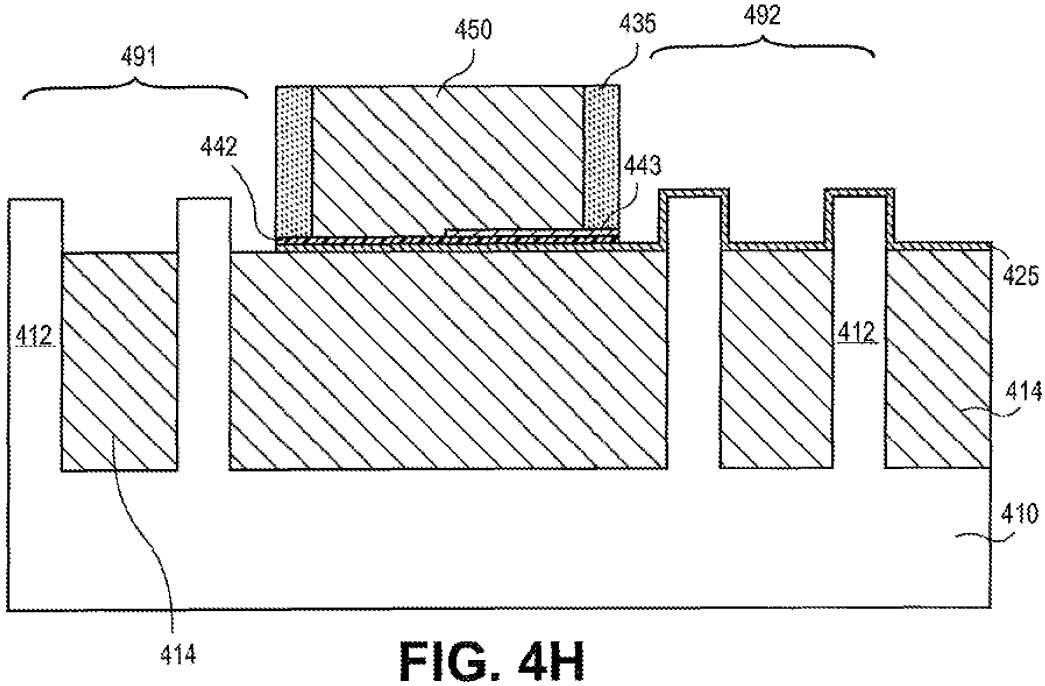

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FIG. 4H

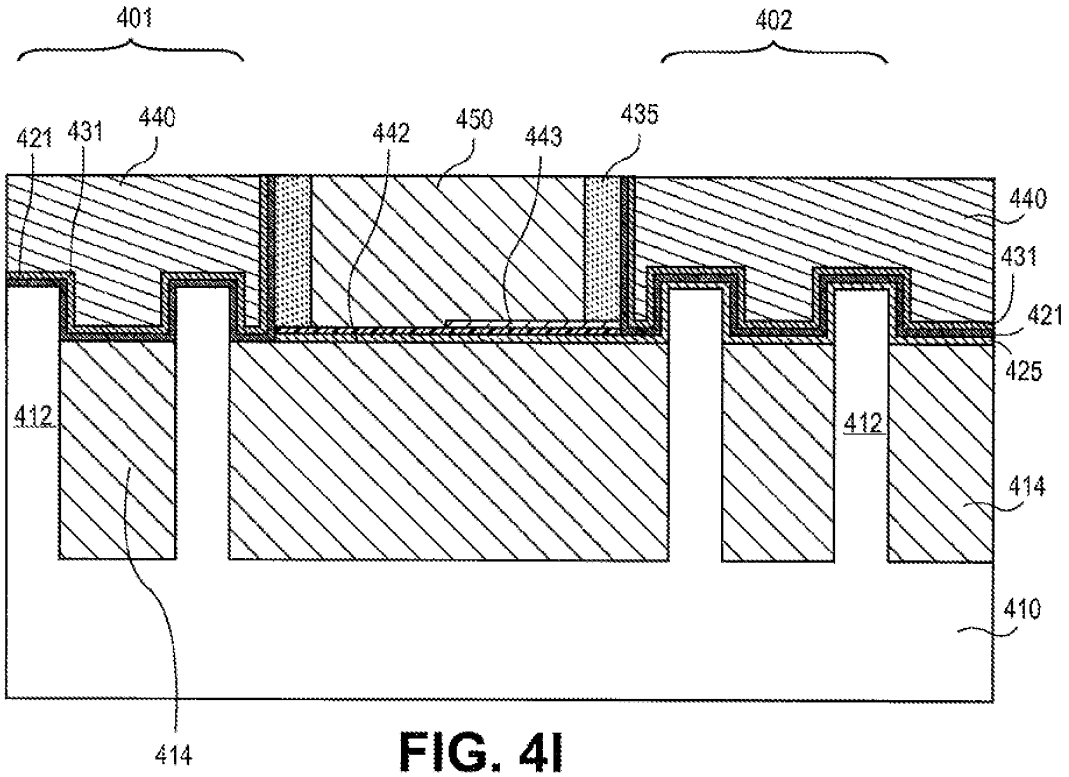

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FIG. 4I

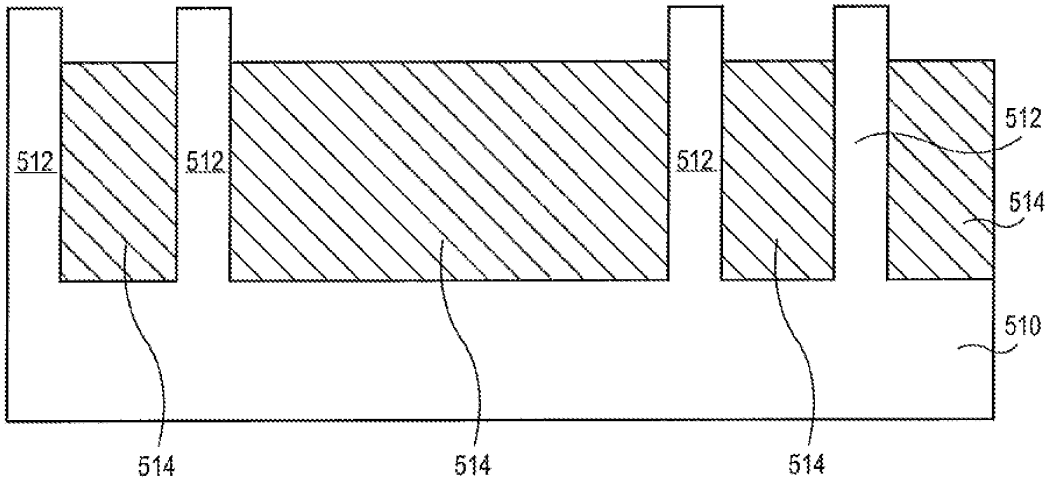

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FIG. 5A

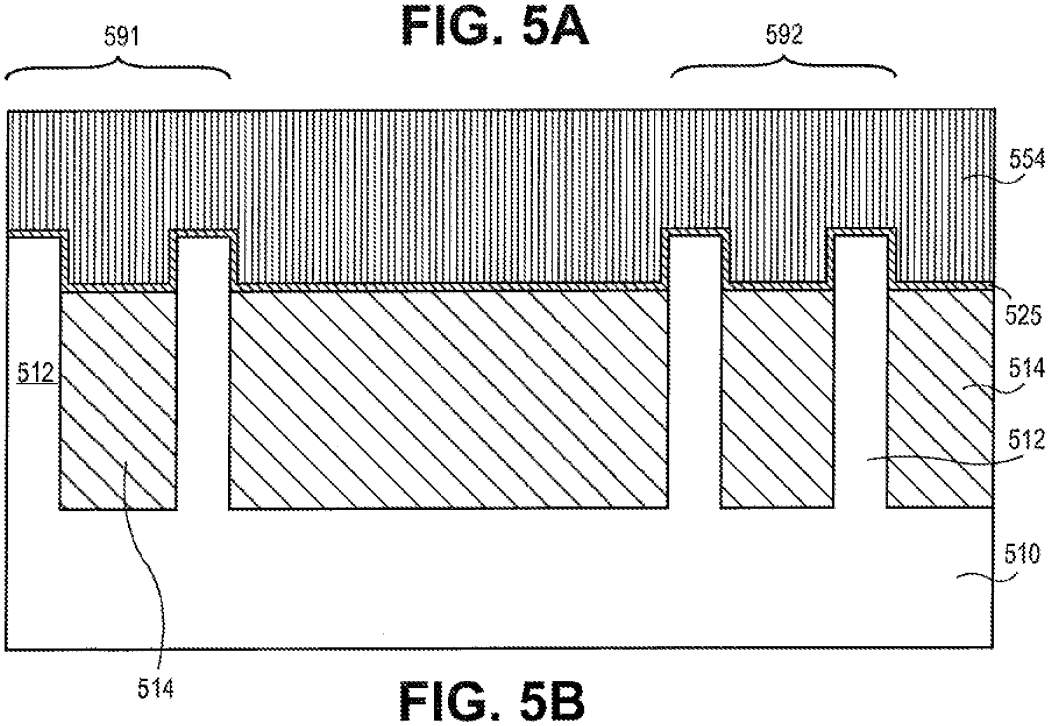

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FIG. 5B

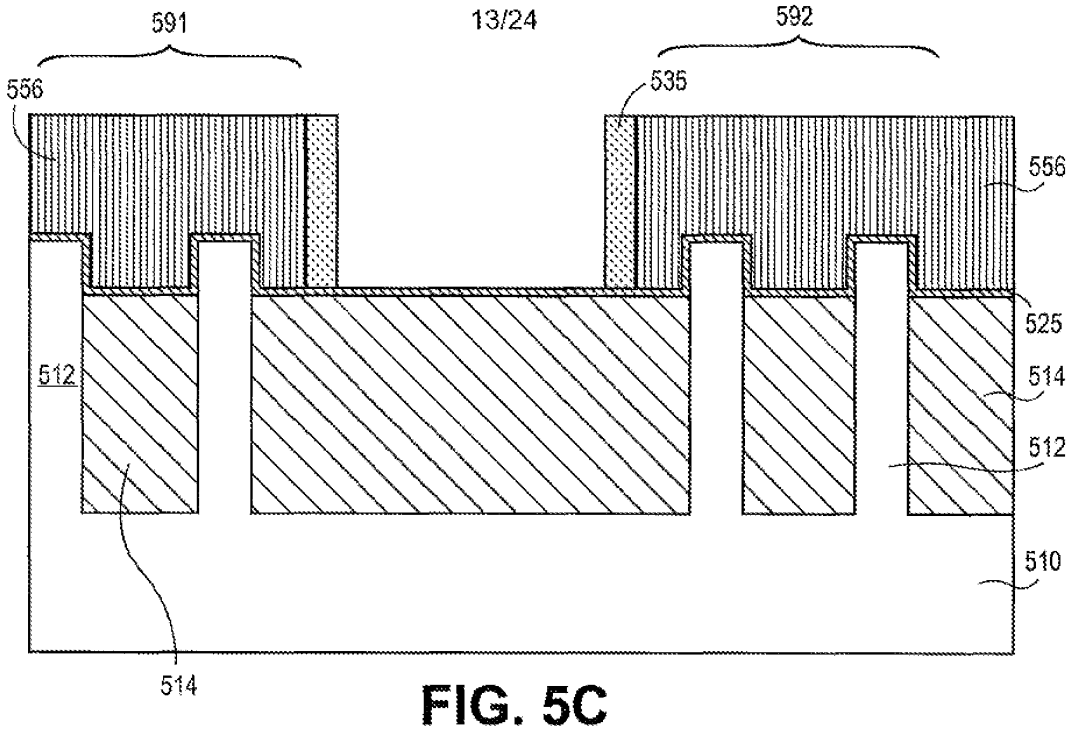

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FIG. 5C

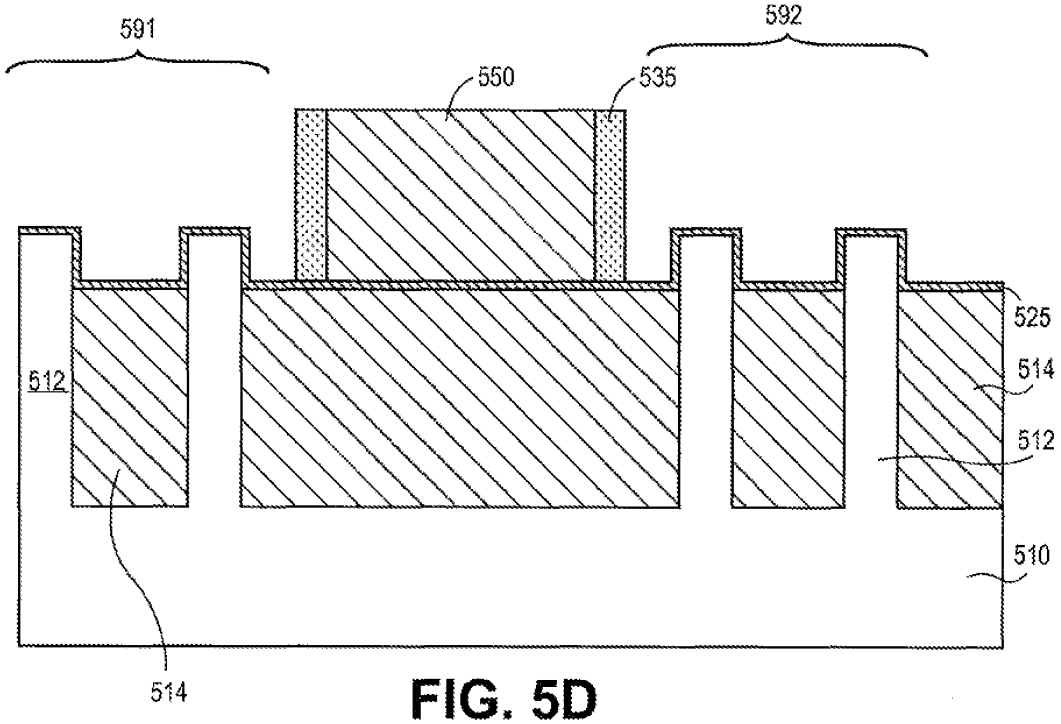

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FIG. 5D

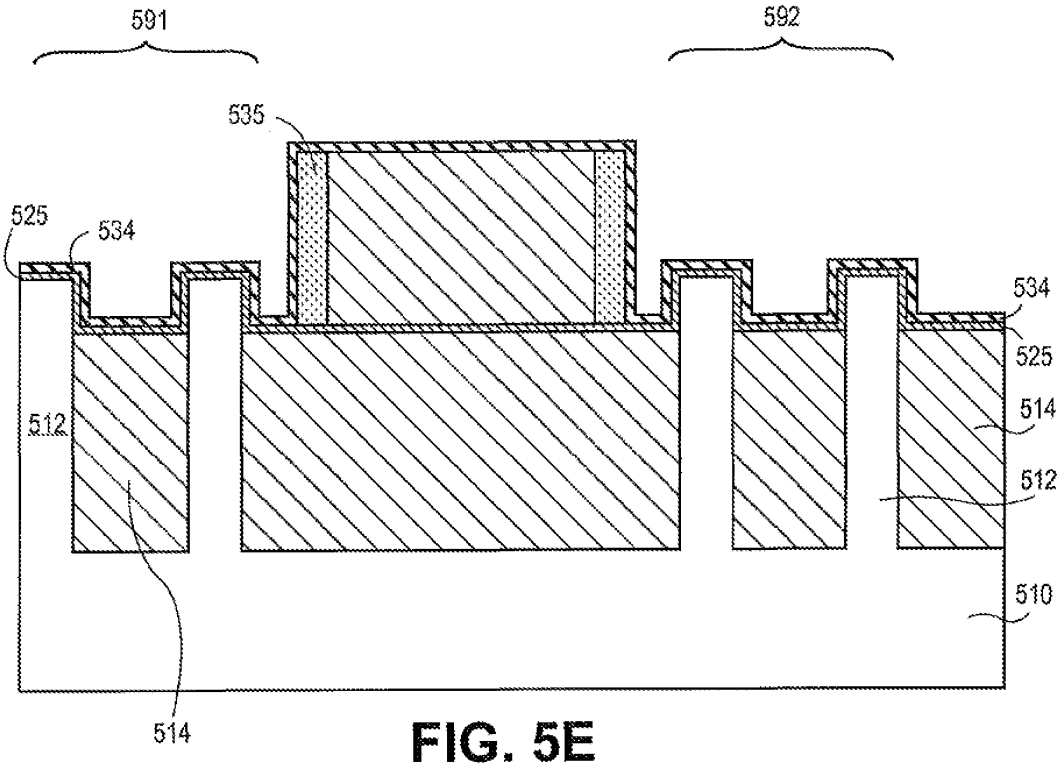

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FIG. 5E

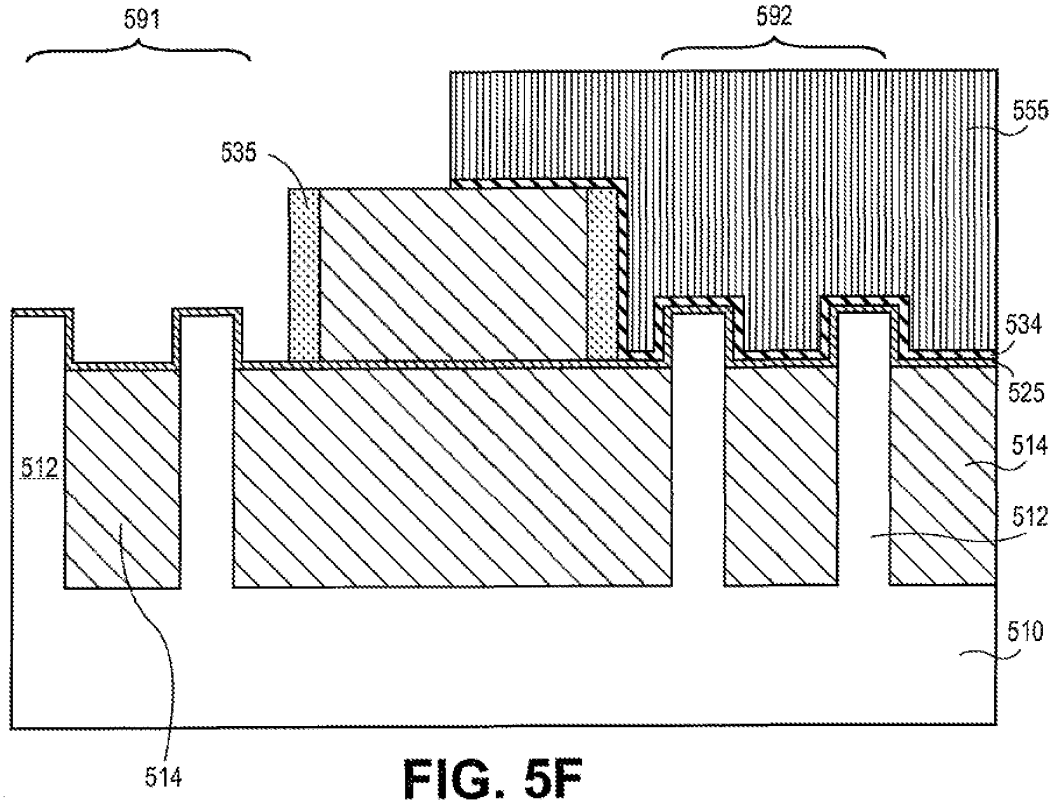

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FIG. 5F

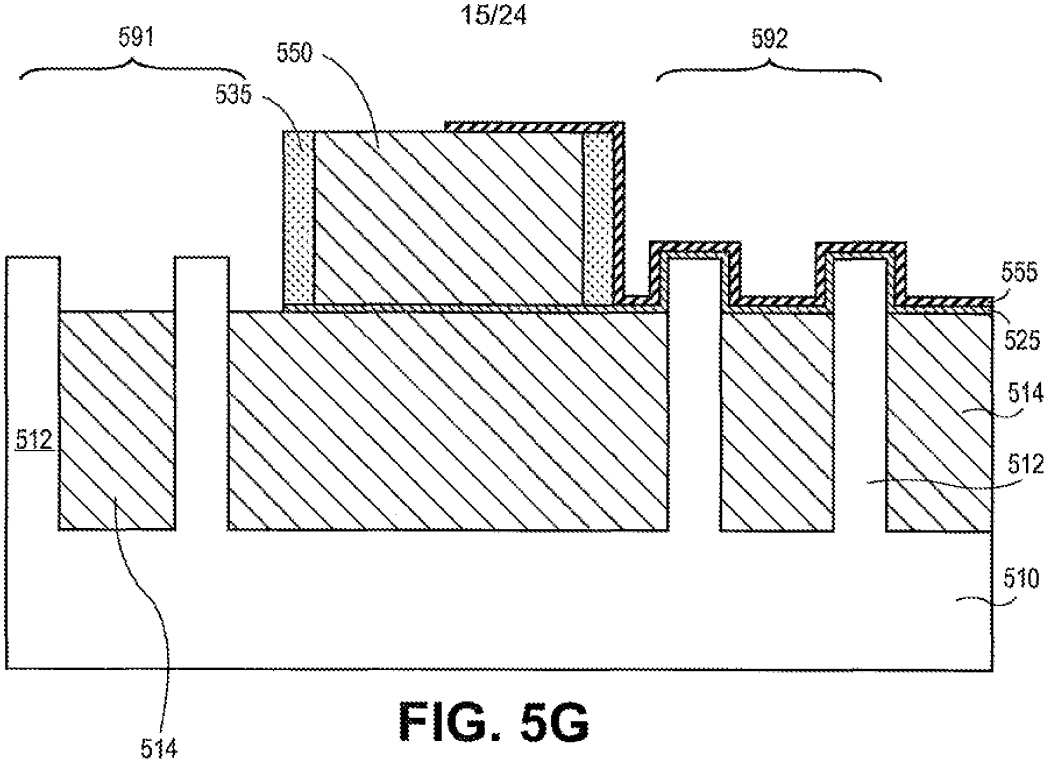

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FIG. 5G

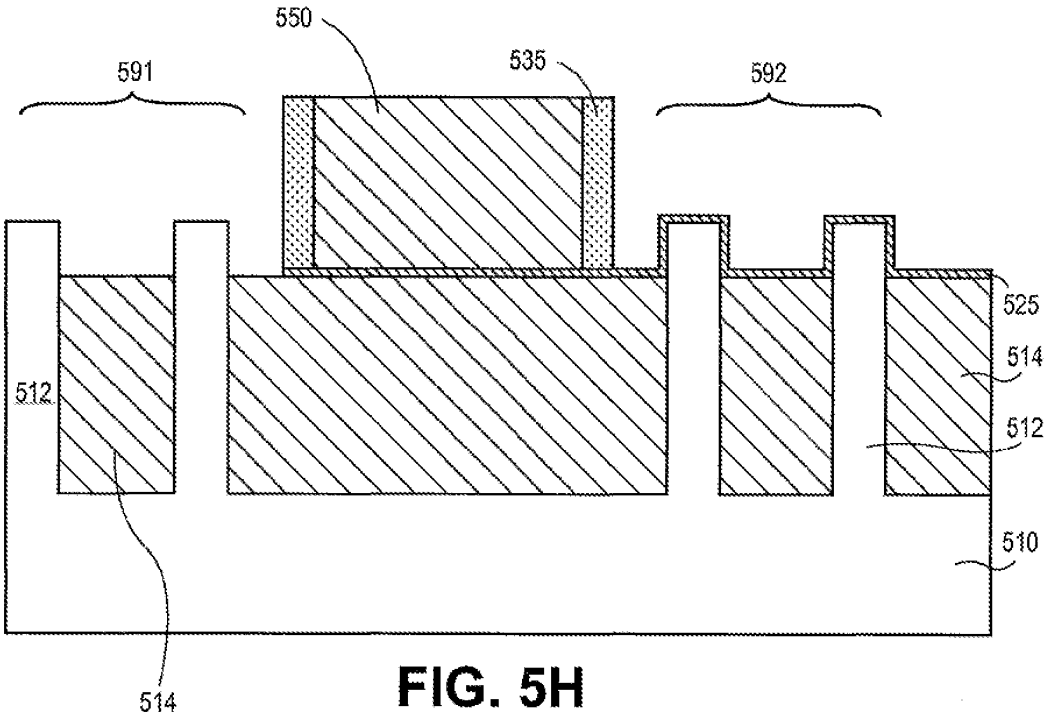

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FIG. 5H

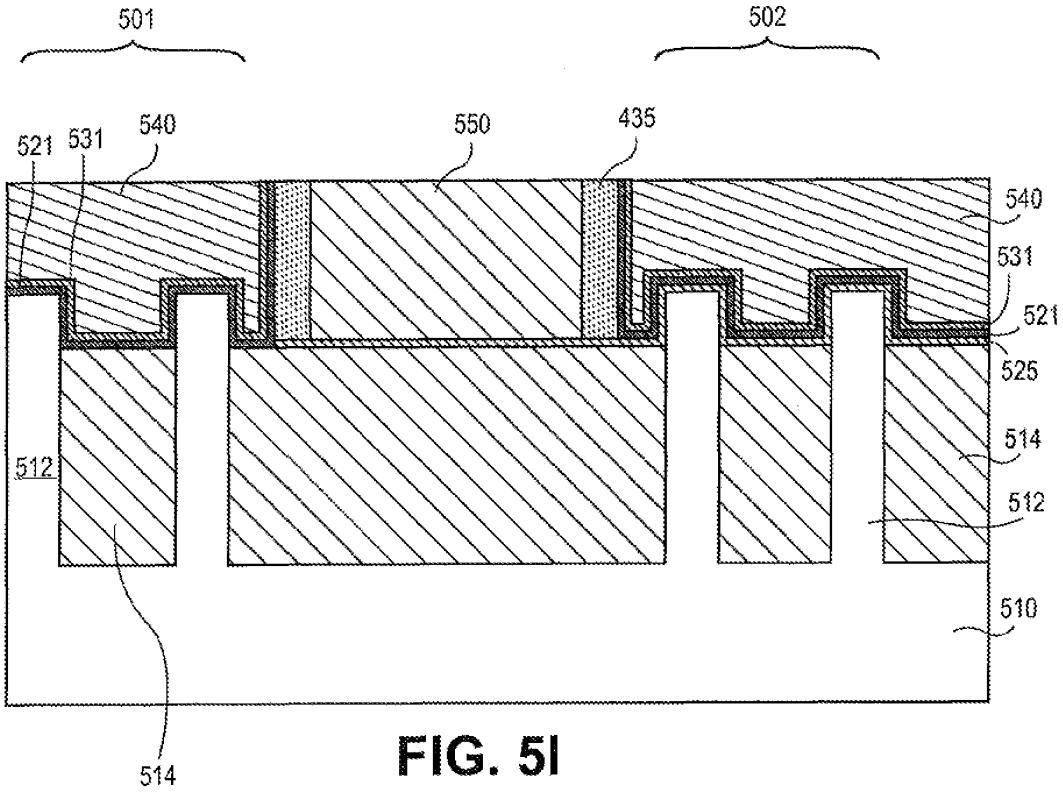


FIG. 5I

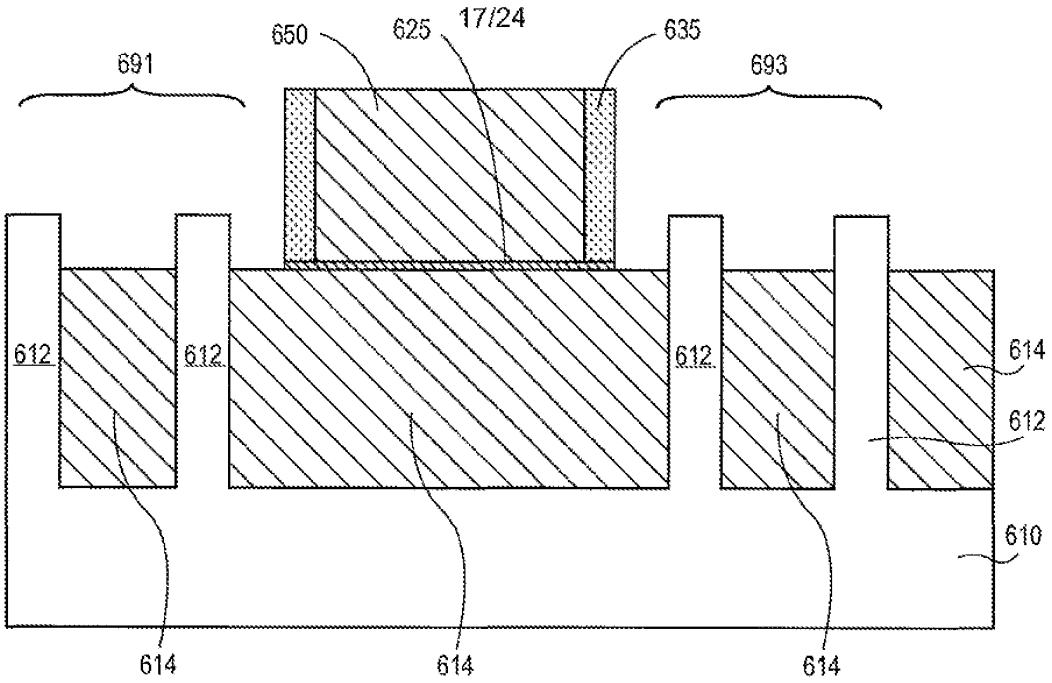

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FIG. 6A

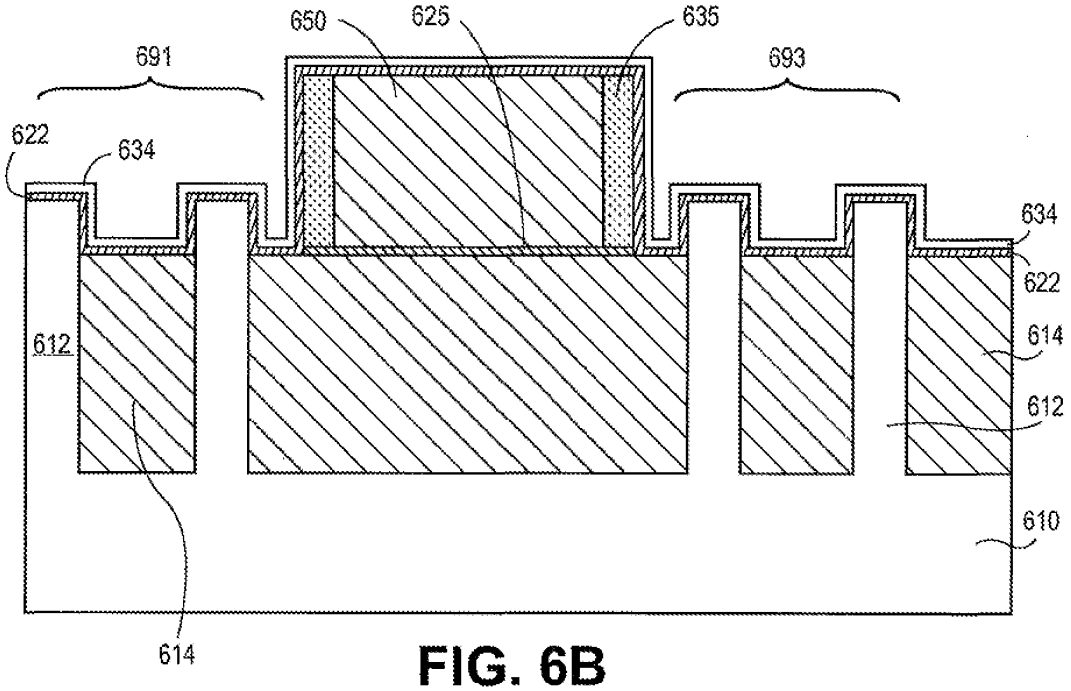

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FIG. 6B

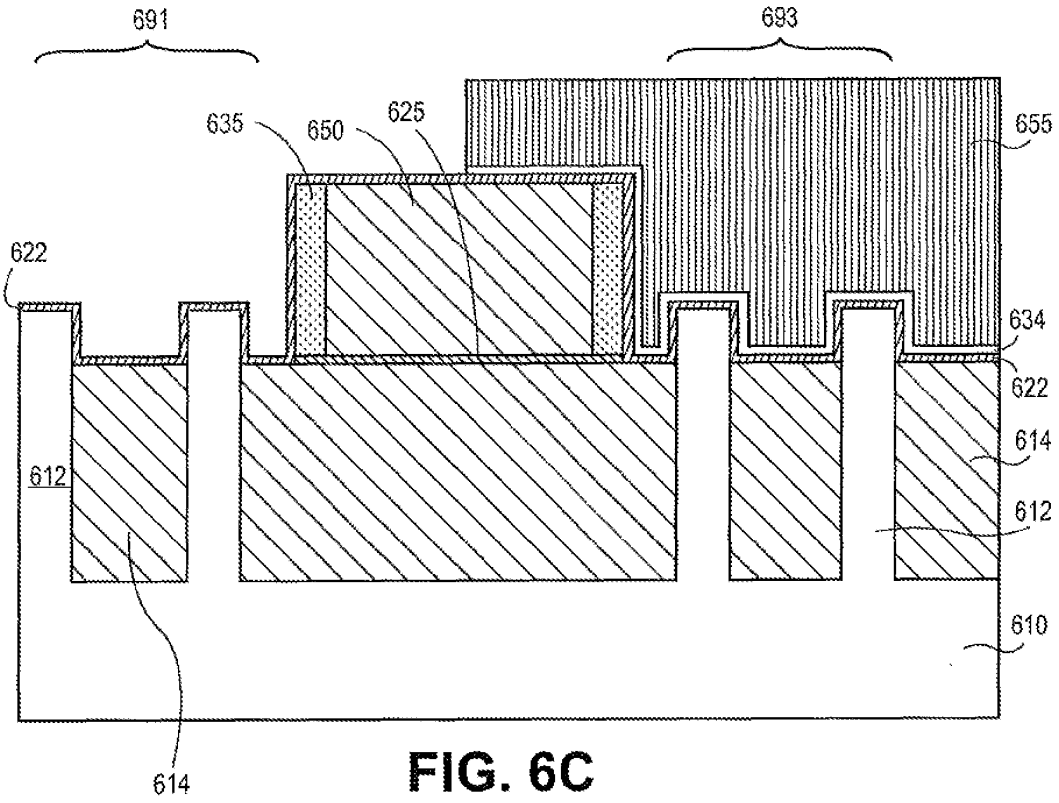


FIG. 6C

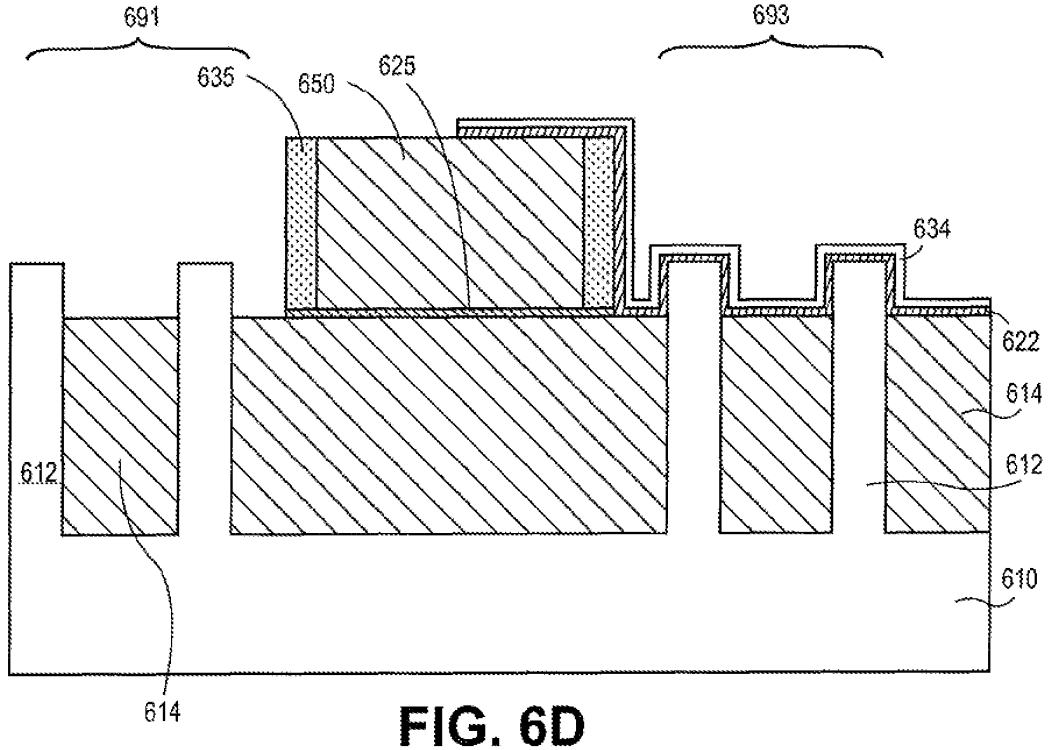


FIG. 6D

BNSDOCID: <WO_____2013101007A1_I_>

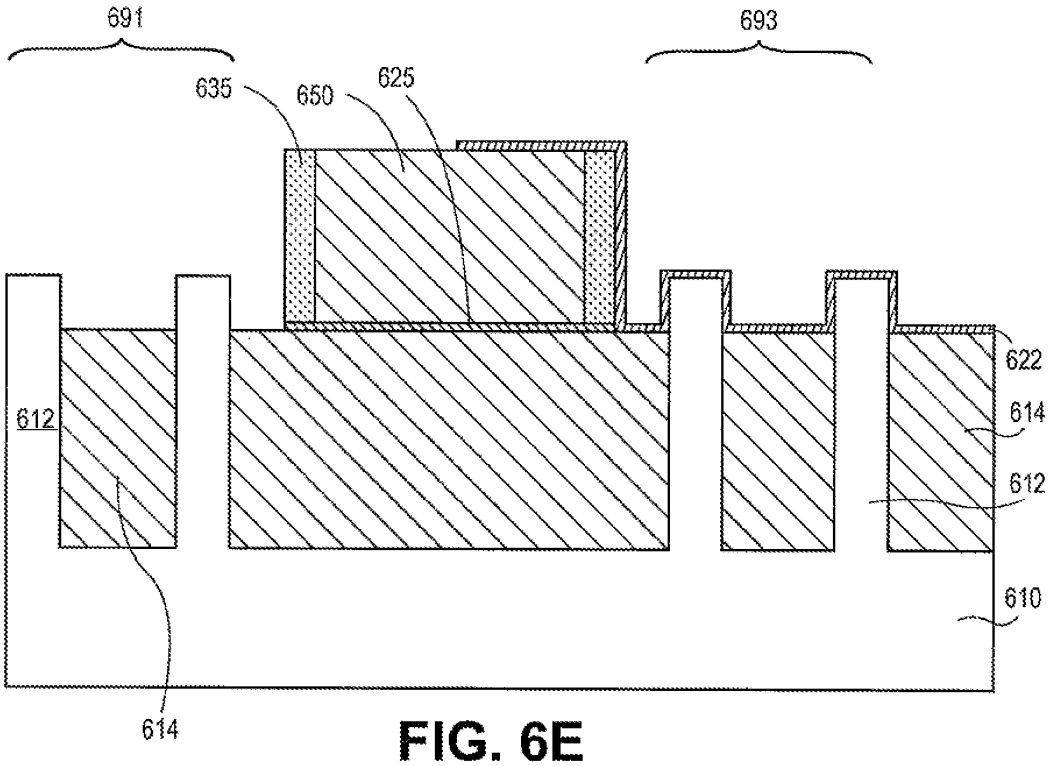

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FIG. 6E

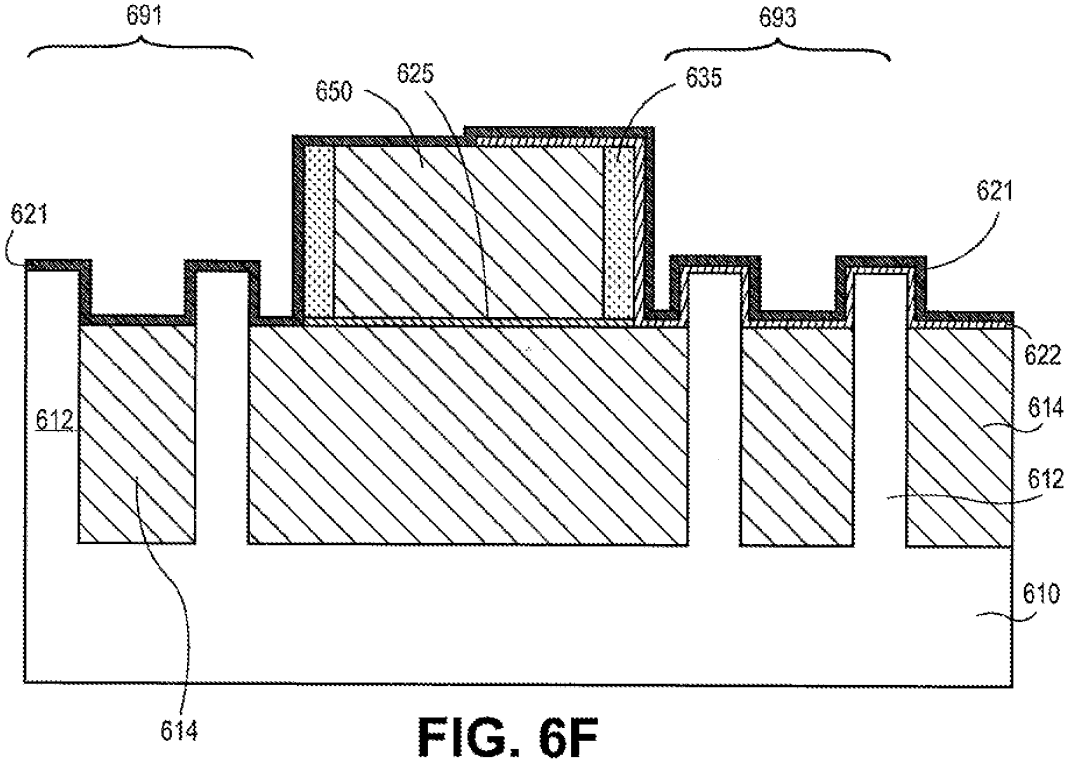

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FIG. 6F

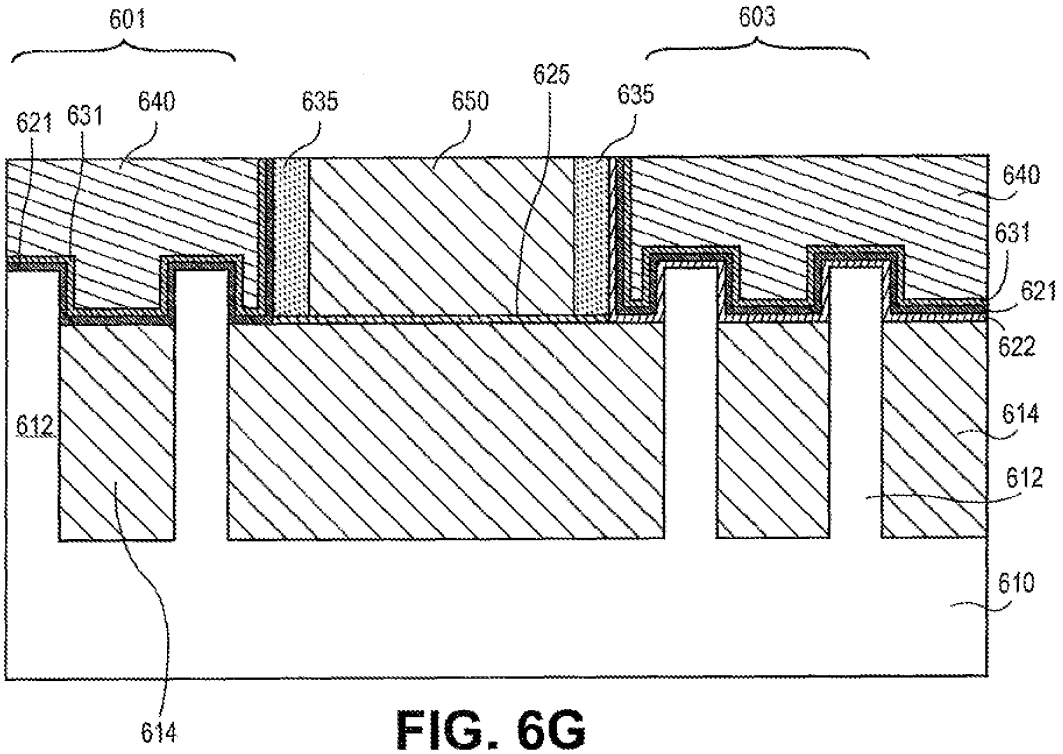

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FIG. 6G

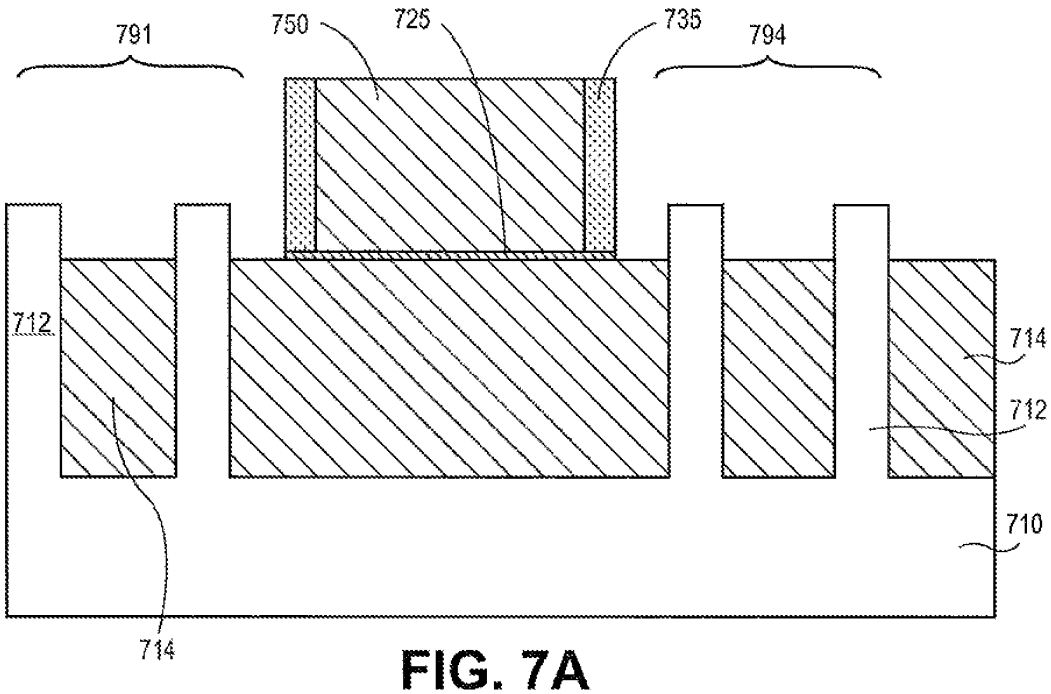

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FIG. 7A

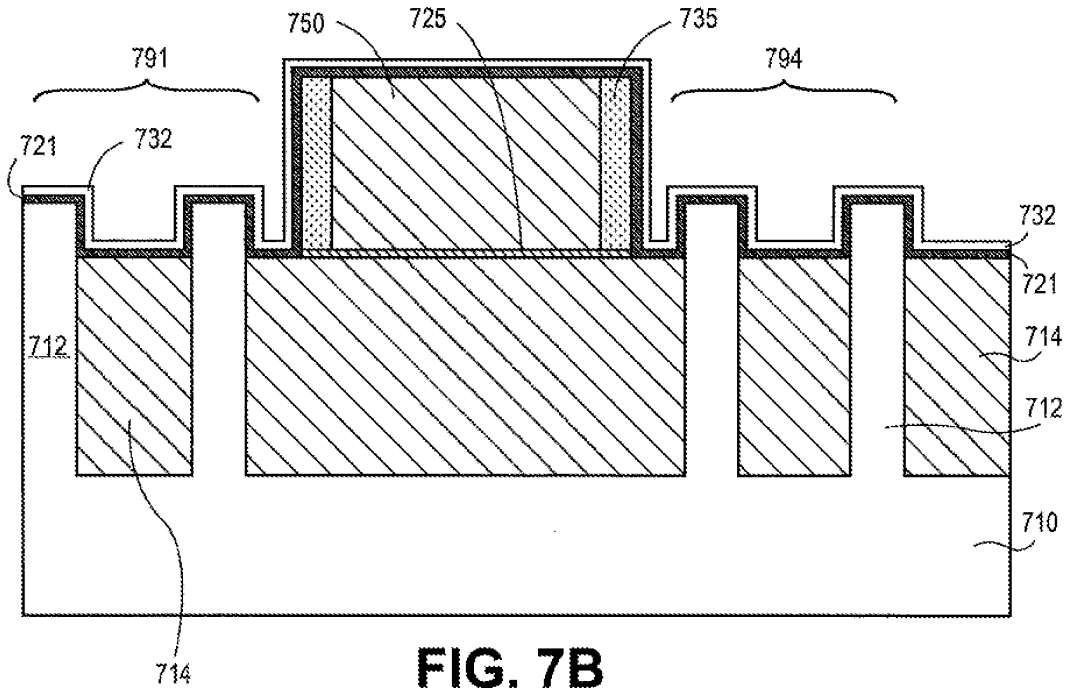

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FIG. 7B

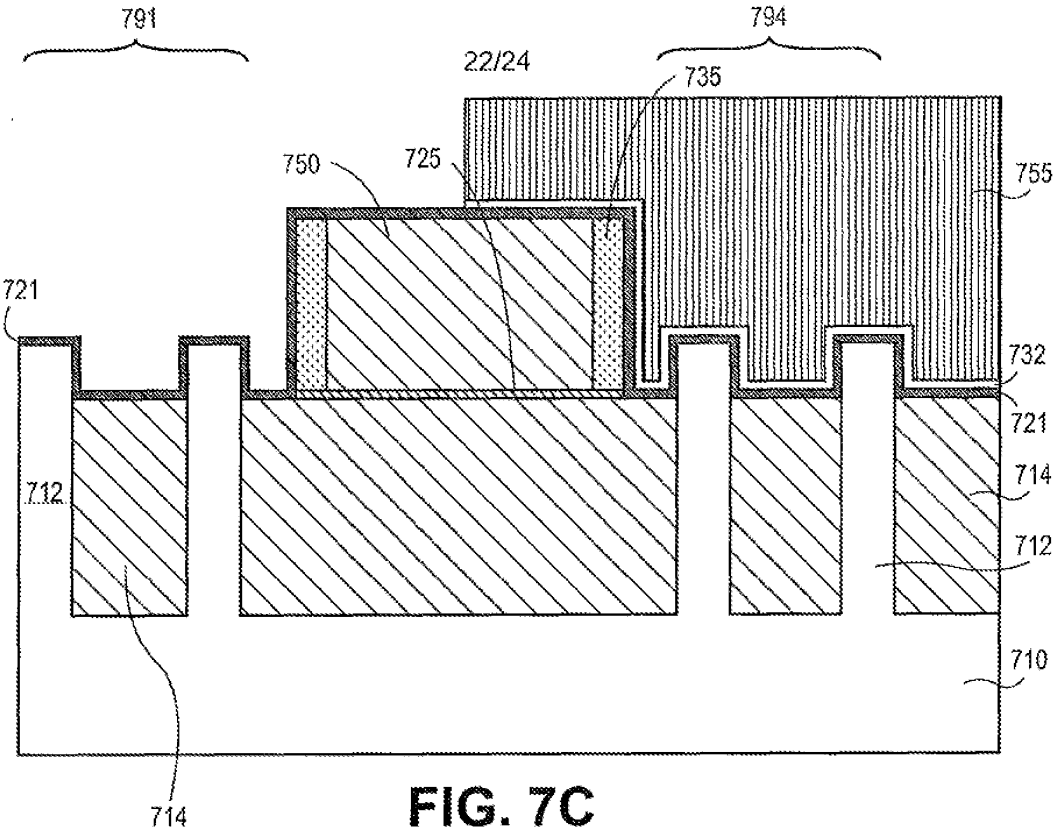

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FIG. 7C

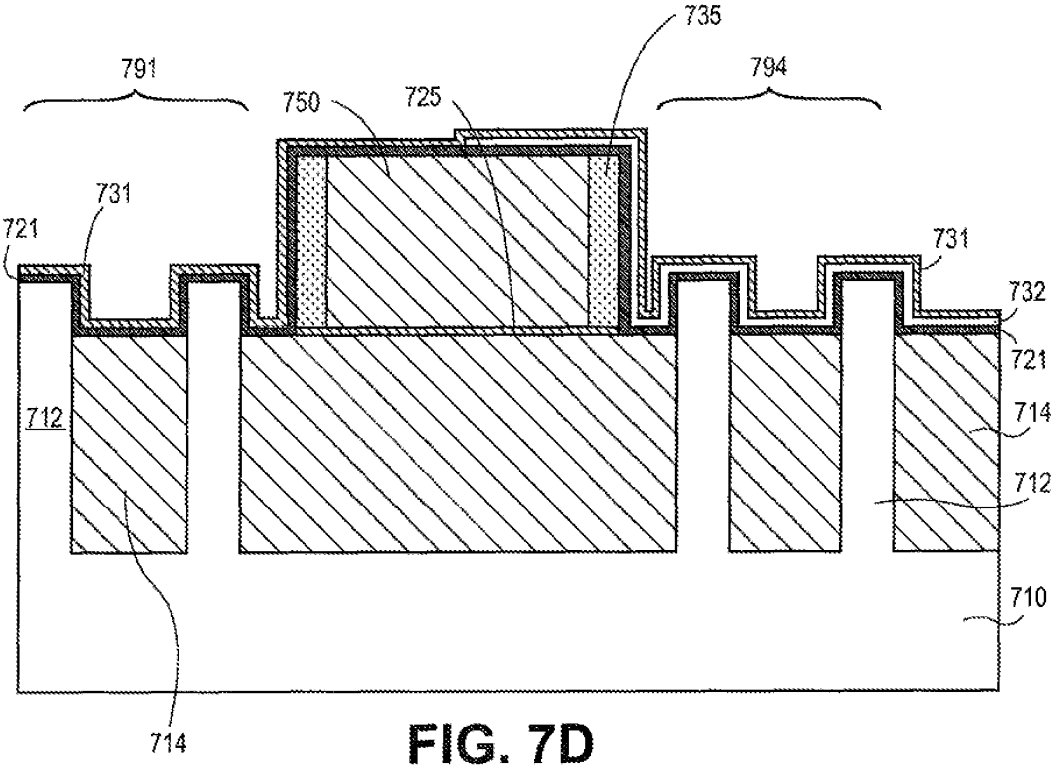

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FIG. 7D

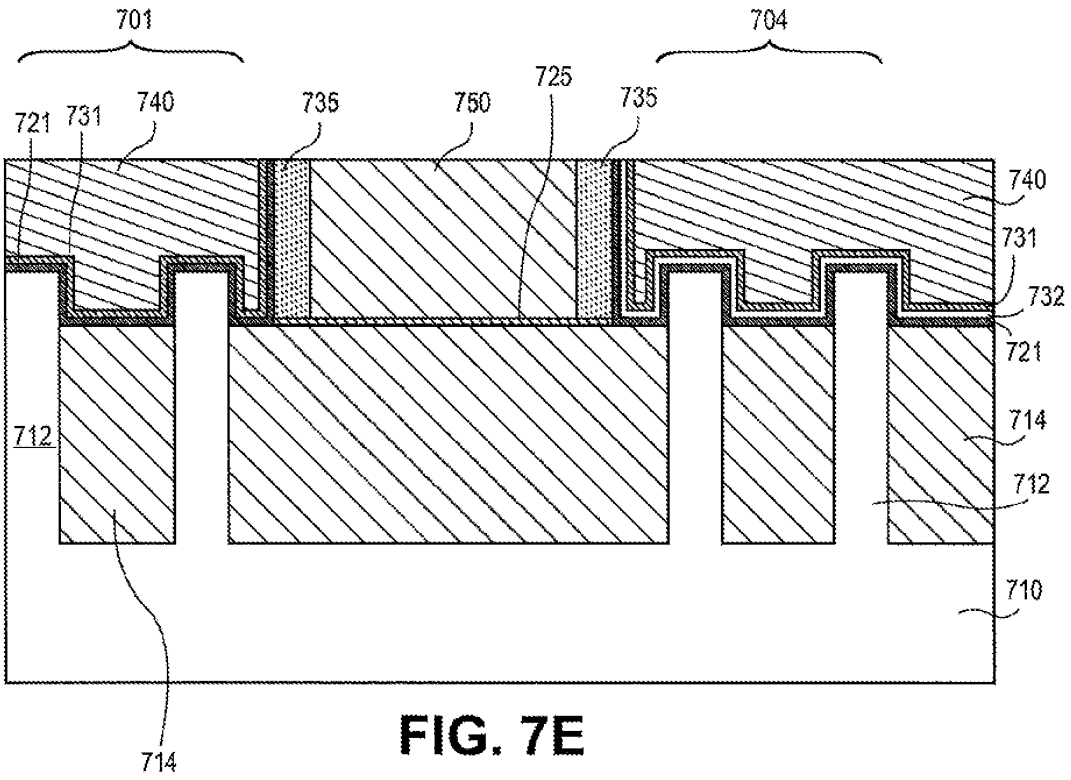

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FIG. 7E

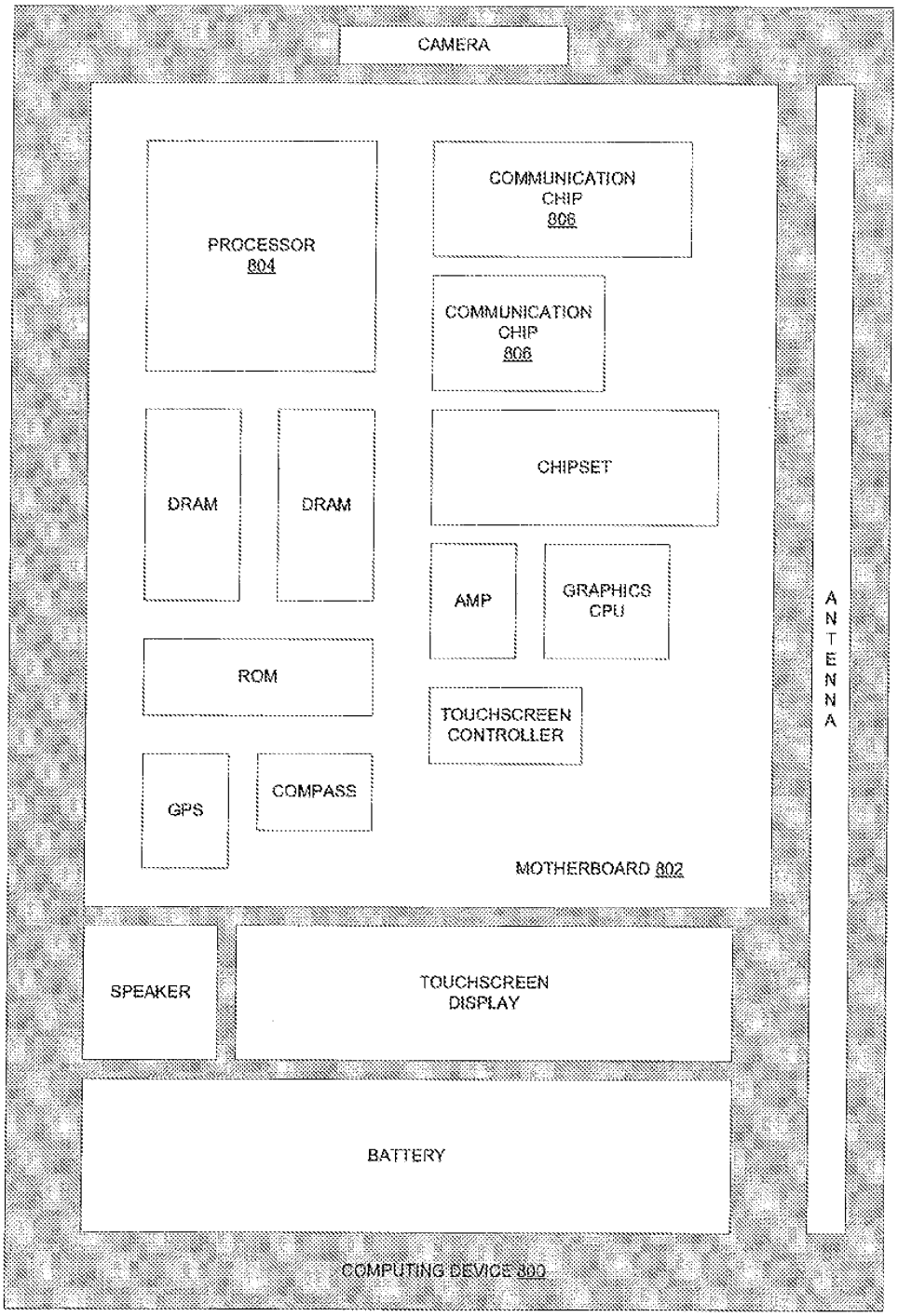

CAMERA
PROCESSOR
804
COMMUNICATION
CHIP
806
COMMUNICATION
CHIP
806
DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD 802
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE 800

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/067681

A. CLASSIFICATION OF SUBJECT MATTER

H01L 27/088(2006.01)i, H01L 27/105(2006.01)i, H01L 29/78(2006.01)i, H01L 21/336(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 27/088; H01L 27/115; H01L 21/336; H01L 29/94; H01L 21/8234; H01L 29/76, H01L 21/8247

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: fin, gate, contact, depose, etch

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2009-0170267 A1 (SHAH UDAY et al.) 02 July 2009 See abstract, paragraphs [0015]-[0017], claims 1,5,6,7,8 and figure 2,5.	1-20
A	KR 10-2011-0071198 A (HANYANG UNIVERSITY INDUSTRY DIGITAL PARK) 29 June 2011 See abstract, pages 5,6,7, claim 1 and figure 1.	1-20
A	US 7361958 B2 (BRASK JUSTIN K. et al.) 22 April 2008 See column 4 line 64 - column 7 line 23 figure 3.	1-20
A	US 7902034 B2 (DOYLE BRIAN S. et al.) 08 March 2011 See column 11 lines 50 - 61, claims 1,3 and figures 4E,4F.	1-20

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 JULY 2012 (17.07.2012)	**18 JULY 2012 (18.07.2012)**

Name and mailing address of the ISA/KR	Authorized officer
Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon Metropolitan City, 302-701, Republic of Korea Facsimile No. 82-42-472-7140	Lee, Sang Don Telephone No. 82-42-481-5665

Form PCT/ISA/210 (second sheet) (July 2009)

BNSDOCID: <WO_____2013101607A1_i_>

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2011/067681

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0170267 A1	02.07.2009	US 7745270 B2	29.06.2010
KR 10-2011-0071198 A	29.06.2011	None	
US 7361958 B2	22.04.2008	US 2006-0071275 A1	06.04.2006
		US 2006-0138552 A1	29.06.2006
		US 2006-0138553 A1	29.06.2006
		US 2008-0090397 A1	17.04.2008
		US 2009-0149012 A1	11.06.2009
		US 7326656 B2	05.02.2008
		US 7528025 B2	05.05.2009
		US 7531437 B2	12.05.2009
US 7902014 B2	08.03.2011	US 2007-0090416 A1	26.04.2007
		US 2007-0111419 A1	17.05.2007
		US 2011-180851 A1	28.07.2011

Electronic Acknowledgement Receipt

EFS ID:	31964996
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1/111548-235422
Receipt Date:	05-MAR-2018
Filing Date:	20-OCT-2017
Time Stamp:	22:41:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US-C1_IDS_03_05_18.pdf	321052 02b676e6d1a0b602acb4e63bf5f3dc411bfa45af	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Foreign Reference	CN103258823_w_English_machine_translation.pdf	20182313 b1a0c52d05f384269187f652fdd5764b377c68ef	no	38
Warnings:					
Information:					
3	Foreign Reference	CN103258823A.pdf	4845709 cd896059a91a3661e54bbb5d8f7ba385f998dc0e	no	37
Warnings:					
Information:					
4	Foreign Reference	WO2013101007.pdf	4702646 89ff7ad78b38aab695477275ca46a6705a797c58	no	55
Warnings:					
Information:					
5	Other Reference-Patent/App/Search documents	P60397EP_EESR_12_04_17.pdf	568471 6ee297051e76496795e53327bded50a3f6193041	no	8
Warnings:					
Information:					
6	Non Patent Literature	P60397TW-D2_OA_09_21_17.pdf	4751323 64e2b8cc28841e3dceba2a2c16a2180e7d20f51f	no	26
Warnings:					
Information:					
		Total Files Size (in bytes):	35371514		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/789,315
Filing Date	October 20, 2017
First Inventor	Milton Clair WEBB, et al.
Art Unit	2822
Examiner Name	POTTER, ROY KARL
Attorney Docket No.	P60397US-C1/111548-235422

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has bee n made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	03-05-2018
Name/Print	Justin K. Brask	Registration Number	61,080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal */Sheri Villarreal/* Date 03-05-18

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1/111548-235422

CONFIRMATION NO. 9752

PUBLICATION NOTICE

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

OC000000097450105

Title:SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Publication No.US-2018-0047808-A1
Publication Date:02/15/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PTO/AIA/01 (06-12)
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

As the below named inventor, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application number 15/789,315 filed on October 20, 2017.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: TAHIR GHANI Date (Optional): 12-20-17

Signature: Ghani

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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LEGAL NAME OF INVENTOR

Inventor: MARK T. BOHR Date (Optional): _____

Signature: Mark T. Bohr

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: MILTON CLAIR WEBB Date (Optional): 12/6/2017

Signature: Milton Clair Webb

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filed on October 20, 2017.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

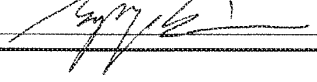
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LEGAL NAME OF INVENTOR

Inventor: SZUYA S. LIAO Date (Optional): 12-30-2017

Signature: 

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Electronic Patent Application Fee Transmittal

Application Number:	15789315
Filing Date:	20-Oct-2017
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Michael A. Bernadicou/Teresa Mattox
Attorney Docket Number:	P60397US-C1/111548-235422

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**140**

Electronic Acknowledgement Receipt	
EFS ID:	31385644
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Michael A. Bernadicou/Teresa Mattox
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P60397US-C1/111548-235422
Receipt Date:	02-JAN-2018
Filing Date:	20-OCT-2017
Time Stamp:	18:29:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$140
RAM confirmation Number	010318INTEFSW00004692500393
Deposit Account	
Authorized User	
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	P60397US_Declaration_1-2-17.pdf	3011578 ad28af8306c3d95ef42c94cb8c2e50378ced39b8	no	4
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30531 9ec0bba6276512887e02cb4c500cd419221a60c3	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3042109		

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/789,315	10/20/2017	2811	2540	P60397US-C1/111548-235422	30	3

CONFIRMATION NO. 9752

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

FILING RECEIPT



Date Mailed: 11/08/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Milton Clair WEBB, Aloha, OR;
Mark BOHR, Aloha, OR;
Tahir GHANI, Portland, OR;
Szuya S. LIAO, Portland, OR;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 15/024,750 03/24/2016
which is a 371 of PCT/US2013/076673 12/19/2013

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

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Permission to Access Search Results: Yes

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/789,315**

Projected Publication Date: 02/15/2018

Non-Publication Request: No

Early Publication Request: No

Title

SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/789,315

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	30 minus 20 =	* 10			OR	x 80 =	800
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2400

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/789,315	10/20/2017	Milton Clair WEBB	P60397US-C1/111548-235422

CONFIRMATION NO. 9752

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

INFORMAL NOTICE

OC000000095198248

Date Mailed: 11/08/2017

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Milton Clair WEBB
  Mark BOHR
  Tahir GHANI
  Szuya S. LIAO

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/llam/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	TDB
	Filing Date	Herewith
	First Named Inventor	Milton Clair WEBB, et al.
	Group Art Unit	
	Examiner Name	TDB
Sheet 1 of 1	Attorney Docket No: P60397US-C1/111548-235422	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**
		US-2007 /0054464	03-08-2007	ZHANG, Guowei	
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Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** — **Country Code/Number/Kind Code (if known)**	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**
		KR-20050082099	08-22-2005	CHOI, Jung A., et al.		
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		JP-2002-530872	09-17-2002	INFINCON TECHNOLOGIES AG		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		International Search Report and Written Opinion from PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) Mailed September 26, 2014, 10 pages.	
		International Preliminary Report on Patentability for PCT Application No. PCT/US2013/076673 (Attorney Docket No. 42P60397PCT) mailed June 30, 2016, 7 pages.	
		Non-Final Office Action and Search Report for Taiwan Patent Application No. 103137443 (Attorney Docket No. P60397TW) mailed June 3, 2016, 3 pgs.'	
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		Non-Final Office Action for U.S. Patent Application No. 15/024,750 (Attorney Docket No. P60397US) mailed February 13, 2017, 6 pgs.	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Filer:	Justin K. Brask/Sheri Villarreal
Attorney Docket Number:	P60397US-C1/111548-235422

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	10	80	800
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	140	140

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2540**

Electronic Acknowledgement Receipt	
EFS ID:	30715775
Application Number:	15789315
International Application Number:	
Confirmation Number:	9752
Title of Invention:	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME
First Named Inventor/Applicant Name:	Milton Clair WEBB
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P60397US-C1/111548-235422
Receipt Date:	20-OCT-2017
Filing Date:	
Time Stamp:	14:49:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$2540
RAM confirmation Number	102317INTEFSW00001229500393
Deposit Account	500393
Authorized User	Sheri Villarreal
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P60397US-C1_APP_10_20_17.pdf	181693 763f63931c56851cb1076ae7ec94a64558dd702a	yes	30
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	23	
	Claims		24	29	
	Abstract		30	30	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	P60397US-C1_FIGS_10_20_17.pdf	2145572 c3289a123ad7da4a9d42be06314f5faf9499494b	no	15
Warnings:					
Information:					
3	Application Data Sheet	P60397US-C1_ADS_10_20_17.pdf	1793383 2a3b736c18370d21391cf5febcef7a41180c0f39	no	9
Warnings:					
Information:					
4		P60397US-C1_IDS_10_20_17.pdf	868715 c85098a024c7e7bc8d11d7eb95f5be013a519644	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	

	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
5	Non Patent Literature	P60397US_OA_02_13_17.pdf	192964 18a680c01613dd06ae4df26709b936915fdad997	no	6
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	38423 ef5fc341bd28d2422991006426554240321 9d78c	no	2
Warnings:					
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME

CLAIM OF PRIORITY

[0001] This application is a continuation of U.S. Patent Application No. 15/024,750, filed March 24, 2016, which is a U.S. National Phase application under 35 U.S.C. § 371 of International Application No. PCT/US13/076673, filed December 19, 2013, entitled "Self-Aligned Gate Edge and Local Interconnect and Method to Fabricate Same" the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0002] Embodiments of the invention are in the field of semiconductor devices and processing and, in particular, self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures.

BACKGROUND

[0003] For the past several decades, the scaling of features in integrated circuits has been a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips. For example, shrinking transistor size allows for the incorporation of an increased number of memory or logic devices on a chip, lending to the fabrication of products with increased capacity. The drive for ever-more capacity, however, is not without issue. The necessity to optimize the performance of each device becomes increasingly significant.

[0004] In the manufacture of integrated circuit devices, multi-gate transistors, such as tri-gate transistors, have become more prevalent as device dimensions continue to scale down. In conventional processes, tri-gate transistors are generally fabricated on either bulk silicon substrates or silicon-on-insulator substrates. In some instances, bulk silicon substrates are preferred due to their lower cost and because they enable a less complicated tri-gate fabrication process.

[0005] Scaling multi-gate transistors has not been without consequence, however. As the dimensions of these fundamental building blocks of microelectronic circuitry are

reduced and as the sheer number of fundamental building blocks fabricated in a given region is increased, the constraints on the lithographic processes used to pattern these building blocks have become overwhelming. In particular, there may be a trade-off between the smallest dimension of a feature patterned in a semiconductor stack (the critical dimension) and the spacing between such features.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 illustrates a plan view of a layout including fin-based semiconductor devices accommodating end-to-end spacing.

[0007] Figures 2A-2D illustrate cross-sectional views of process operations of significance in a conventional finFET or tri-gate process fabrication scheme.

[0008] Figures 3A-3D illustrate cross-sectional views of process operations of significance in a self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with an embodiment of the present invention.

[0009] Figures 4A-4G illustrate cross-sectional views and corresponding top views of process operations in another self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with another embodiment of the present invention.

[0010] Figure 5A illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a pitch division patterned local interconnect (LI), in accordance with one embodiment of the present invention.

[0011] Figure 5B illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a self-aligned local interconnect (SAGELI), in accordance with another embodiment of the present invention.

[0012] Figures 6A-6H illustrate angled, three-dimensional cross-sectional views of various operations in the fabrication of self-aligned gate endcaps, in accordance with an embodiment of the present invention.

[0013] Figures 7A-7D illustrate angled, three-dimensional cross-sectional views of various structural options for providing a foundation for local interconnect fabrication, in accordance with an embodiment of the present invention.

[0014] Figure 8A illustrates a cross-sectional view of a non-planar semiconductor device having self-aligned gate edge isolation, in accordance with an embodiment of the present invention.

[0015] Figure 8B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 8A, in accordance with an embodiment of the present invention.

[0016] Figure 9 illustrates a computing device in accordance with one implementation of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0017] Self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures are described. In the following description, numerous specific details are set forth, such as specific integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as integrated circuit design layouts, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be understood that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale.

[0018] One or more embodiments of the present invention are directed to semiconductor structures or devices having one or more gate edge structures (e.g., as gate isolation regions) of gate electrodes of the semiconductor structures or devices. One or more embodiments are directed to the fabrication of local interconnects for such gate electrode structures. Additionally, methods of fabricating gate edge isolation structures in a self-aligned manner and/or methods of fabricating local interconnects are also described. In one or more embodiments, self-aligned gate edge structures and/or local interconnects are fabricated for logic transistors based on complementary metal oxide semiconductor (CMOS) devices.

[0019] To provide context, scaling of gate endcap and trench contact (TCN) endcap regions are important contributors towards improving transistor layout area and density. Gate and TCN endcap regions refer to gate and TCN overlap of the diffusion

region/fins of semiconductor devices. As an example, Figure 1 illustrates a plan view of a layout 100 including fin-based semiconductor devices accommodating end-to-end spacing. Referring to Figure 1, first 102 and second 104 semiconductor devices are based on semiconductor fins 106 and 108, respectively. Each device 102 and 104 has a gate electrode 110 or 112, respectively. Additionally, each device 102 and 104 has trench contacts (TCNs) 114 and 116, respectively, at source and drain regions of the fins 106 and 108, respectively. The gate electrodes 110 and 112 and the TCNs 114 and 116 each have an end cap region, which is located off of the corresponding fins 106 and 108, respectively.

[0020] Referring again to Figure 1, typically, gate and TCN endcap dimensions must include an allowance for mask registration error to ensure robust transistor operation for worst case mask mis-registration, leaving an end-to-end spacing 118. Thus, another important design rule critical to improving transistor layout density is the spacing between two adjacent endcaps facing each other. However, the parameters of "*2*Endcap + End-to-End Spacing*" are becoming increasingly difficult to scale using lithographic patterning to meet the scaling requirements for new technologies. In particular, the additional endcap length required to allow for mask registration error also increases gate capacitance values due to longer overlap length between TCN and gate electrodes, thereby increasing product dynamic energy consumption and degrading performance. Previous solutions have focused on improving registration budget and patterning or resolution improvements to enable shrinkage of both endcap dimension and endcap-to-endcap spacing.

[0021] In accordance with an embodiment of the present invention, approaches are described which provide for self-aligned gate endcap and TCN overlap of a semiconductor fin without any need to allow for mask registration. In one such embodiment, a disposable spacer is fabricated on the semiconductor fin edges which determines the gate endcap and the contact overlap dimensions. The spacer defined endcap process enables the gate and TCN endcap regions to be self-aligned to the semiconductor fin and, therefore, does not require extra endcap length to account for mask mis-registration. Furthermore, approaches described herein do not require lithographic patterning at previously required stages since the gate and TCN

endcap/overlap dimensions remain fixed, leading to improvement (i.e., reduction) in device to device variability in electrical parameters.

[0022] In order to provide a side-by-side comparison, Figures 2A-2D illustrate cross-sectional views of process operations of significance in a conventional finFET or tri-gate process fabrication scheme, while Figures 3A-3D illustrate cross-sectional views of process operations of significance in a self-aligned gate edge process fabrication scheme for finFET or tri-gate devices, in accordance with an embodiment of the present invention.

[0023] Referring to Figures 2A and 3A, a bulk semiconductor substrate 200 or 300, such as a bulk single crystalline silicon substrate is provided having fins 202 or 302, respectively, etched therein. In an embodiment, the fins are formed directly in the bulk substrate 200 or 300 and, as such, are formed continuous with the bulk substrate 200 or 300. It is to be appreciated that within the substrate 200 or 300, shallow trench isolation structures may be formed between fins. Referring to Figure 3A, a hardmask layer 304, such as a silicon nitride hardmask layer, and a pad oxide layer 306, such as a silicon dioxide layer, remain atop fins 302 following patterning to form the fins 302. By contrast, referring to Figure 2A, such a hardmask layer and pad oxide layer have been removed.

[0024] Referring to Figure 2B, a dummy or permanent gate dielectric layer 210 is formed on the exposed surfaces of the semiconductor fins 202, and a dummy gate layer 212 is formed over the resulting structure. By contrast, referring to Figure 3B, a dummy or permanent gate dielectric layer 310 is formed on the exposed surfaces of the semiconductor fins 302, and dummy spacers 312 are formed adjacent to the resulting structure.

[0025] Referring to Figure 2C, gate endcap cut patterning is performed and isolation regions 214 are formed at the resulting patterned dummy gate ends 216. In the conventional process scheme, a larger gate endcap must be fabricated to allow for gate mask mis-registration, as depicted by the arrowed regions 218. By contrast, referring to Figure 3C, self-aligned isolation regions 314 are formed by providing an isolation layer over the structure of Figure 3B, e.g., by deposition and planarization. In one such embodiment, the self-aligned gate endcap process does not require extra space for mask registration, as compared in Figures 2C and 3C.

[0026] Referring to Figure 2D, the dummy gate electrode 212 of Figure 2C is replaced with permanent gate electrodes. In the case of use of a dummy gate dielectric layer, such a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer in this process. In the specific example shown, a dual metal gate replacement process is performed to provide an N-type gate electrode 220 over a first semiconductor fin 202A and to provide a P-type gate electrode 222 over a second semiconductor fin 202B. The N-type gate electrode 220 and the P-type gate electrode 222 are formed between the gate edge isolations structures 214, but form a P/N junction 224 where they meet. The exact location of the P/N junction 224 may vary, depending on mis-registration, as depicted by the arrowed region 226.

[0027] By contrast, referring to Figure 3D, the hardmask layer 304 and pad oxide layer 306 are removed, and the dummy spacers 314 of Figure 3C are replaced with permanent gate electrodes. In the case of use of a dummy gate dielectric layer, such a dummy gate dielectric layer may also be replaced by a permanent gate dielectric layer in this process. In the specific example shown, a dual metal gate replacement process is performed to provide an N-type gate electrode 320 over a first semiconductor fin 302A and to provide a P-type gate electrode 322 over a second semiconductor fin 302B. The N-type gate electrode 320 and the P-type gate electrode 322 are formed between, and are also separated by, the gate edge isolations structures 314.

[0028] Referring again to Figure 2D, a local interconnect 240 may be fabricated to contact N-type gate electrode 220 and P-type gate electrode 322 to provide a conductive path around the P/N junction 224. Likewise, referring to Figure 3D, a local interconnect 340 may be fabricated to contact N-type gate electrode 320 and P-type gate electrode 322 to provide a conductive path over the intervening isolation structure 314 there between. Referring to both Figures 2D and 3D, a hardmask 242 or 342 may be formed on the local interconnect 240 or 340, respectively.

[0029] In another aspect, a hardmask and pad oxide layer may not be retained atop patterned find throughout a dummy spacer and self-aligned gate edge isolations structure fabrication process. As such, the height of the semiconductor fins relative to the height of the dummy spacers may need to be differentiated in another way. As an example, Figures 4A-4G illustrate cross-sectional views and corresponding top views of process operations in another self-aligned gate edge process fabrication scheme for

finFET or tri-gate devices, in accordance with another embodiment of the present invention.

[0030] Referring to Figure 4A, a bulk semiconductor substrate 400, such as a bulk single crystalline silicon substrate, is provided having fins 402 etched therein. In an embodiment, the fins 402 are formed directly in the bulk substrate 400 and, as such, are formed continuous with the bulk substrate 400. It is to be appreciated that within the substrate 400, shallow trench isolation structures may be formed between fins. In one embodiment, artifacts from patterning the fins 402, such as a hardmask layer and a pad oxide layer, have been removed, as is depicted in Figure 4A.

[0031] Referring to Figure 4B, dummy spacers 404 are formed along the sidewalls of the fins 402. In an embodiment, the dummy spacers 404 are formed by a deposition and etch process that ultimately exposes the top surface of the fins 402. It is to be appreciated that the fins 402 may be passivated, e.g., by deposition or growth of a dummy gate dielectric layer, prior to the formation of the dummy spacers 404. In one embodiment, the fins 402 are silicon fins passivated with a silicon dioxide layer, and the dummy spacers are fabricated from silicon nitride or like material. In another embodiment, however the fins 402 are not passivated at this stage.

[0032] Referring to Figure 4C, isolations structures 406 are formed in the open regions of the structure of Figure 4B. In an embodiment, the isolation regions 406 are formed by deposition and subsequent planarization (e.g., by chemical mechanical polishing) of a dielectric film over the structure of Figure 4B. In a particular embodiment, the isolation structures are composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0033] Referring to Figure 4D, the fins 402 are recessed relative to the height of the isolation structures 406 and relative to the height of the dummy spacers 404. In an embodiment, the recessing is performed by using a selective etch process. In one such embodiment, a passivation layer first formed on fins 402 is removed prior to or during the recessing of the fins 402.

[0034] Referring to Figure 4E, the dummy spacers 404 are removed from the structure of Figure 4D. In an embodiment, the removal is performed by using a selective etch process. In one such embodiment, the isolation structures 406 are composed of

silicon oxide, the fins 402 are composed of silicon, and the selectively removed dummy spacers are composed of silicon nitride.

[0035] Referring to Figure 4F, a gate electrode stack 408 is formed in the locations from which dummy spacers 404 were removed and along the top surfaces of the recessed fins 402. In an embodiment, the gate electrode stack 408 includes a conformal gate dielectric layer 410, such as a high-k gate dielectric layer, and a metal gate electrode 412. The cross-sectional view of Figure 4F is taken along the a-a' axis of the top view of Figure 4F. It is to be understood, however, that the top view is taken somewhat deeper into the structure in order to show the whole fins 402. In actuality, the metal gate material 412 would cover the fins 402 in the top view.

[0036] Referring to Figure 4G, trench contacts 414 are formed adjacent to the gate electrode stacks 408 and along the top surfaces of the recessed fins 402. In an embodiment, the trench contacts 414 are for contacting source and drain regions within the fins 402, and are separated from the gate electrode stacks 408 by dielectric spacers 416. The cross-sectional view of Figure 4G is taken along the b-b' axis of the top view of Figure 4G. It is to be understood, however, that the top view is taken somewhat deeper into the structure in order to show the whole fins 402. In actuality, the trench contacts 414 would cover the fins 402 in the top view.

[0037] In another aspect, referring again to Figure 3D, in an embodiment, one or more of the above approaches requires an additional local interconnect layer (LI) above gate and trench contact (TCN) to connect adjacent gates and TCN electrodes. In one such embodiment, such a local interconnect must overlap gate and TCN, without creating contact to gate (CTG) shorting. As such, fabrication of the local interconnect can require patterning of lines at 1/2 of gate pitch with good CTG short margin, while maintaining robust LI to TCN contact. Hence, the alignment between LI and gate or TCN is another difficult patterning problem. As such, in accordance with an embodiment of the present invention, in order to address the above concern, a fabrication scheme for local interconnect lines which are self-aligned to gate and TCN without any need to allow for mask registration is provided. The approach involves fabrication of a spacer along a taller stack that includes a dummy gate and hardmask and which extends above the self-aligned gate endcap. In one such embodiment, the spacers serve as continuous self-aligned walls separating gate and contact. Two additional dielectric materials with

contrasting etch properties may be used as hardmasks to allow for selectively opening an area for gate-LI (LIG) and TCN-LI (LIT).

[0038] As an example, Figure 5A illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a pitch division patterned local interconnect (LI), in accordance with one embodiment of the present invention. By contrast, Figure 5B illustrates a cross-sectional view of a portion of a semiconductor device having self-aligned gate/trench contact endcap (SAGE) with a self-aligned local interconnect (SAGELI), in accordance with another embodiment of the present invention.

[0039] Referring to Figure 5A, a semiconductor device 500A includes a semiconductor fin 502. A plurality of short self-aligned isolation structures 504 separate alternating gate 506 and trench contact 508 regions. Upper isolation structures 510 separate alternating trench contact local interconnects 512 and gate local interconnects 514. The trench contact local interconnects 512 and gate local interconnects 514 are formed by pitch division patterning to accommodate for mis-registration, as is shown in Figure 5A. It is to be appreciated that dielectric caps may be formed on the trench contact local interconnects 512 and gate local interconnects 514, as is also depicted in Figure 5A.

[0040] Referring to Figure 5B, a semiconductor device 500B includes a semiconductor fin 552. A plurality of tall self-aligned isolation structures 554 separate alternating gate 556 and trench contact 558 regions. The same isolation structures 554 also separate alternating trench contact local interconnects 562 and gate local interconnects 564. The trench contact local interconnects 512 and gate local interconnects 514 are formed without using an additional lithography operation as was need for the case of Figure 5A. It is to be appreciated that dielectric caps may be formed on the trench contact local interconnects 562 and gate local interconnects 564, as is depicted in Figure 5B. It is also to be appreciated that the trench contact local interconnects 512 and gate local interconnects 514 are, in an embodiment, fabricated at different times, the process for forming each taking advantage of the use of plugs/hardmask layers as placeholders prior to replacement with the actual permanent materials of the trench contact local interconnects 512 and gate local interconnects 514. Furthermore, although all locations in Figure 5B are shown as having a gate local

interconnect or trench contact local interconnect, not all locations need be selected for local interconnection. In locations not selected a dielectric plug or hardmask may remain (i.e., it is not selected for removal at certain locations).

[0041] As exemplary approaches, Figures 6A-6H illustrate angled, three-dimensional cross-sectional views of various operations in the fabrication of self-aligned gate endcaps, in accordance with an embodiment of the present invention. Figures 7A-7D illustrate angled, three-dimensional cross-sectional views of various structural options for providing a foundation for local interconnect fabrication, in accordance with an embodiment of the present invention.

[0042] Referring to Figure 6A, a plurality of semiconductor fins 602 is formed by patterning a substrate 600, such as a single crystalline silicon substrate, and the patterning may involve pitch halving or pitch quartering patterning. Furthermore, a passivation layer 604, a dummy gate layer 606 (such as a polycrystalline silicon layer), and a hardmask layer 608 are patterned during the fin 602 patterning.

[0043] Referring to Figure 6B, a shallow trench isolation (STI) layer 610 is formed over the structure of Figure 6A. In an embodiment, the STI layer 610 includes a silicon dioxide layer and is formed by chemical vapor deposition (CVD) and subsequent chemical mechanical planarization (CMP). In one embodiment, the STI structure includes a liner dielectric layer 612, as shown in Figure 6B.

[0044] Referring to Figure 6C, the STI layer 610 of Figure 6B is recessed to form an STI structure 614 (which may include a liner dielectric layer) and a dummy gate dielectric layer 616 is formed on the resulting structure. In one such embodiment, the dummy gate dielectric layer 616 is formed by deposition and is further deposited on the STI structure 614, as depicted. Furthermore, hardmask layer 608 may be removed, as is also depicted.

[0045] Referring to Figure 6D, spacers 618 are formed along the sidewalls of the protruding portions of the structure of Figure 6C. In an embodiment, the spacers 618 are formed by a deposition and subsequent anisotropic etch process. In one such embodiment, the spacers are composed of deposited polycrystalline silicon. Depending on the spacing between certain of the fins 602, some spacers 618 are discrete from all other spacers, while some spacers are continuous with another spacer. As an example, the portion 620A has discrete spacers 618A, while the portion 620B includes a pair of

continuous spacers 618B. Thus, referring collectively to Figures 6A-6D, a finFET "hat" and dummy gate poly are patterned with a standard pitch division fin patterning process and a spacer is created on both sides of the patterned fin-poly pillars.

[0046] Referring to Figure 6E, the gaps between the spacers 618 of Figure 6D are filled with a dielectric material layer 622 to create transistor isolations. In an embodiment, the dielectric material is composed of a silicon nitride material.

[0047] Referring to Figure 6F, the dielectric material layer 622 is planarized (e.g., by CMP) to expose the dummy gate layer 606 and the corresponding spacers 618. In an embodiment, both the dummy gate layer 606 and the corresponding spacers 618 are composed of polycrystalline silicon. The process forms self-aligned end cap isolation walls 624.

[0048] Referring to Figure 6G, a second dummy layer and hardmask stack or a tall hardmask only are/is deposited and patterned using pitch division gate patterning (both cases shown as item 626 in Figure 6G) on the structure of Figure 6H. In an embodiment, in the case that a dummy layer and hardmask stack is used, the dummy layer is composed of polycrystalline silicon.

[0049] Referring to Figure 6H, an anisotropic etch selective to hardmask layer 626, isolation walls 624 and finFET "hat" 616 (e.g., remaining from the dummy gate dielectric layer) is performed to provide a straight profile between patterned lines and resulting endcap isolation cages 628. Although not shown, following gate spacer formation, N-type or P-type source drain formation, and gate electrode replacement (e.g., with high-k/metal gate), a conductive material can be formed in the endcap isolation cages 628 to provide trench contacts. And, in cases where the isolation walls are of sufficient height, self-aligned local interconnect lines may be fabricated, examples of which are described below in association with Figures 7C and 7D.

[0050] To provide an initial comparison, Figure 7A illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700A without self-aligned gate edge isolation. Referring to Figure 7A, a plurality of fins 702A has a dummy gate layer 704A and corresponding hardmask 706A patterned thereon. In the subsequent fabrication of local interconnects, a pitch divisional patterning scheme would have to be employed.

[0051] Figure 7B illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700B having self-aligned gate edge isolation. Referring to Figure 7B, a plurality of fins 702B has a dummy gate layer 704B and corresponding hardmask 706B patterned thereon. Self-aligned gate edge isolation structures 708B are formed between various groupings of the fins 702B. However, the hardmask 706B is relatively short compared with the self-aligned gate edge isolation structures 708B. As such, in the subsequent fabrication of local interconnects, a pitch divisional patterning scheme would have to be employed.

[0052] Figure 7C illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700C having self-aligned gate edge isolation. Referring to Figure 7C, a plurality of fins 702C has a dummy gate layer 704C, corresponding second dummy layer 705C, and corresponding hardmask 706C patterned thereon. Self-aligned gate edge isolation structures 708C are formed between various groupings of the fins 702C. The height of the hardmask 706C together with the second dummy layer 705C is relatively tall compared with the self-aligned gate edge isolation structures 708C. As such, in the subsequent fabrication of local interconnects, a self-aligned local interconnect scheme may be employed.

[0053] Figure 7D illustrates an angled, three-dimensional cross-sectional view of a foundational structure 700D having self-aligned gate edge isolation. Referring to Figure 7D, a plurality of fins 702D has a dummy gate layer 704D and a corresponding tall hardmask 706D patterned thereon. Self-aligned gate edge isolation structures 708D are formed between various groupings of the fins 702D. The height of the tall hardmask 706D is relatively tall compared with the self-aligned gate edge isolation structures 708D. As such, in the subsequent fabrication of local interconnects, a self-aligned local interconnect scheme may be employed.

[0054] More generally, one or more embodiments described herein provide an avenue for area scaling, reducing capacitance, and/or eliminating various critical front end masks, such as gate cut masks. In one such embodiment the width of a minimum transistor can be reduced by up to 30% by implementing one or more of the approaches describe herein. The smaller transistor size reduces the capacitance between the gate and TCN and other parasitic capacitances. No extra mask steps are needed to create the

endcaps, contacts and local interconnect lines so the many masks needed for such features in the standard process are eliminated.

[0055] More specifically, key features of one or more embodiments described above may include one or more of: (1) the gate endcap is the distance from the fin edge to the isolation edge. This distance is defined by the spacer width and is the same size for all transistors. No lithographic patterning is needed to define the endcap so there is no need to allow for mask registration in the endcap. (2) The TCN overlap of the fin is determined by the spacer width and is also not affected by mask registration. (3) The local interconnect lines are self-aligned to the gate and TCN by utilizing the gate patterning lines above the transistor isolation walls to form three distinct hardmasks that can be selectively opened one at a time. Embodiments may be applicable to the 7nm node generation, e.g., to improve transistor layout density and gate capacitance (dynamic energy and performance improvement) and reduce total mask count.

[0056] It is to be appreciated that the structures resulting from the above exemplary processing schemes may be used in a same or similar form for subsequent processing operations to complete device fabrication, such as PMOS and NMOS device fabrication. As an example of a completed device, Figures 8A and 8B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having self-aligned gate edge isolation, in accordance with an embodiment of the present invention, and as building on the structure described in association with Figure 3D.

[0057] Referring to Figure 8A, a semiconductor structure or device 800 includes a non-planar active regions (e.g., a fin structures including protruding fin portion 804 and sub-fin region 805) formed from substrate 802, and within isolation region 806. Gate structures 808 are disposed over the protruding portions 804 of the non-planar active regions as well as over a portion of the isolation region 806. As shown, gate structures 808 include a gate electrode 850 and a gate dielectric layer 852. In one embodiment, although not shown, gate structures 808 may also include a dielectric cap layer. Gate structures 808 are separated by self-aligned gate edge isolation structures 820. A local interconnect 854 coupled adjacent gate structures 808. A gate contact 814, and overlying gate contact via 816 are also seen from this perspective, along with an overlying metal interconnect 860, all of which are disposed in inter-layer dielectric stacks or layers 870.

Also seen from the perspective of Figure 8A, the gate contact 814 is, in one embodiment, disposed over the non-planar active regions. As is also depicted in Figure 8A, an interface 880 exists between a doping profile of protruding fin portions 804 and sub-fin regions 805, although other embodiments do not include such an interface in doping profile between these regions.

[0058] Referring to Figure 8B, the gate structures 808 are shown as disposed over the protruding fin portions 804, as isolated by self-aligned gate edge isolation structures 820. Source and drain regions 804A and 804B of the protruding fin portions 804 are shown in this perspective, although it is to be understood that these regions would be overlapped with trench contact structures. In one embodiment, the source and drain regions 804A and 804B are doped portions of original material of the protruding fin portions 804. In another embodiment, the material of the protruding fin portions 804 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 804A and 804B may extend below the height of dielectric layer 806, i.e., into the sub-fin region 805.

[0059] In an embodiment, the semiconductor structure or device 800 is a non-planar device such as, but not limited to, a finFET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate structures 808 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

[0060] Substrate 802 may be composed of a semiconductor material that can withstand a manufacturing process and in which charge can migrate. In an embodiment, substrate 802 is a bulk substrate composed of a crystalline silicon, silicon/germanium or germanium layer doped with a charge carrier, such as but not limited to phosphorus, arsenic, boron or a combination thereof, to form active region 804. In one embodiment, the concentration of silicon atoms in bulk substrate 802 is greater than 97%. In another embodiment, bulk substrate 802 is composed of an epitaxial layer grown atop a distinct crystalline substrate, e.g. a silicon epitaxial layer grown atop a boron-doped bulk silicon mono-crystalline substrate. Bulk substrate 802 may alternatively be composed of a group III-V material. In an embodiment, bulk substrate 802 is composed of a III-V material such as, but not limited to, gallium nitride, gallium phosphide, gallium arsenide, indium phosphide, indium antimonide, indium gallium arsenide, aluminum gallium arsenide,

indium gallium phosphide, or a combination thereof. In one embodiment, bulk substrate 802 is composed of a III-V material and the charge-carrier dopant impurity atoms are ones such as, but not limited to, carbon, silicon, germanium, oxygen, sulfur, selenium or tellurium.

[0061] Isolation region 806 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of a permanent gate structure from an underlying bulk substrate or isolate active regions formed within an underlying bulk substrate, such as isolating fin active regions. For example, in one embodiment, the isolation region 806 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0062] Self-aligned gate edge isolation structures 820 may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, portions of permanent gate structures from one another. For example, in one embodiment, the isolation region 806 is composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0063] Gate structures 808 may be composed of a gate electrode stack which includes a gate dielectric layer 852 and a gate electrode layer 850. In an embodiment, the gate electrode of the gate electrode stack is composed of a metal gate and the gate dielectric layer is composed of a high-K material. For example, in one embodiment, the gate dielectric layer is composed of a material such as, but not limited to, hafnium oxide, hafnium oxy-nitride, hafnium silicate, lanthanum oxide, zirconium oxide, zirconium silicate, tantalum oxide, barium strontium titanate, barium titanate, strontium titanate, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, lead zinc niobate, or a combination thereof. Furthermore, a portion of gate dielectric layer may include a layer of native oxide formed from the top few layers of the substrate 802. In an embodiment, the gate dielectric layer is composed of a top high-k portion and a lower portion composed of an oxide of a semiconductor material. In one embodiment, the gate dielectric layer is composed of a top portion of hafnium oxide and a bottom portion of silicon dioxide or silicon oxy-nitride.

[0064] In one embodiment, the gate electrode is composed of a metal layer such as, but not limited to, metal nitrides, metal carbides, metal silicides, metal aluminides,

hafnium, zirconium, titanium, tantalum, aluminum, ruthenium, palladium, platinum, cobalt, nickel or conductive metal oxides. In a specific embodiment, the gate electrode is composed of a non-workfunction-setting fill material formed above a metal workfunction-setting layer.

[0065] Spacers associated with the gate electrode stacks may be composed of a material suitable to ultimately electrically isolate, or contribute to the isolation of, a permanent gate structure from adjacent conductive contacts, such as self-aligned contacts. For example, in one embodiment, the spacers are composed of a dielectric material such as, but not limited to, silicon dioxide, silicon oxy-nitride, silicon nitride, or carbon-doped silicon nitride.

[0066] Local interconnect 854, gate contact 814, and overlying gate contact via 816 may be composed of a conductive material. In an embodiment, one or more of the contacts or vias are composed of a metal species. The metal species may be a pure metal, such as tungsten, nickel, or cobalt, or may be an alloy such as a metal-metal alloy or a metal-semiconductor alloy (e.g., such as a silicide material). It is to be appreciated that a hardmask layer may be disposed on the local interconnect 854 in locations where gate contact 814 is not located thereon. Furthermore, the local interconnect 854 may be fabricated by lithographic patterning or, in other embodiments, may be fabricated as a self-aligned interconnect structure, as aligned with taller versions of the Self-aligned gate edge isolation structures 820.

[0067] In an embodiment (although not shown), providing structure 800 involves formation of a contact pattern which is essentially perfectly aligned to an existing gate pattern while eliminating the use of a lithographic step with exceedingly tight registration budget. In one such embodiment, this approach enables the use of intrinsically highly selective wet etching (e.g., versus conventionally implemented dry or plasma etching) to generate contact openings. In an embodiment, a contact pattern is formed by utilizing an existing gate pattern in combination with a contact plug lithography operation. In one such embodiment, the approach enables elimination of the need for an otherwise critical lithography operation to generate a contact pattern, as used in conventional approaches. In an embodiment, a trench contact grid is not separately patterned, but is rather formed between poly (gate) lines. For example, in one such embodiment, a trench contact grid is formed subsequent to gate grating patterning but prior to gate grating cuts.

[0068] Furthermore, the gate structures 808 may be fabricated by a replacement gate process. In such a scheme, dummy gate material such as polysilicon or silicon nitride pillar material, may be removed and replaced with permanent gate electrode material. In one such embodiment, a permanent gate dielectric layer is also formed in this process, as opposed to being carried through from earlier processing. In an embodiment, dummy gates are removed by a dry etch or wet etch process. In one embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a dry etch process including use of SF_6. In another embodiment, dummy gates are composed of polycrystalline silicon or amorphous silicon and are removed with a wet etch process including use of aqueous NH_4OH or tetramethylammonium hydroxide. In one embodiment, dummy gates are composed of silicon nitride and are removed with a wet etch including aqueous phosphoric acid.

[0069] In an embodiment, one or more approaches described herein contemplate essentially a dummy and replacement gate process in combination with a dummy and replacement contact process to arrive at structure 800. In one such embodiment, the replacement contact process is performed after the replacement gate process to allow high temperature anneal of at least a portion of the permanent gate stack. For example, in a specific such embodiment, an anneal of at least a portion of the permanent gate structures, e.g., after a gate dielectric layer is formed, is performed at a temperature greater than approximately 600 degrees Celsius. The anneal is performed prior to formation of the permanent contacts.

[0070] Referring again to Figure 8A, in an embodiment, a semiconductor device has contact structures that contact portions of a gate electrode formed over an active region. In general, prior to (e.g., in addition to) forming a gate contact structure (such as a via) over an active portion of a gate and in a same layer as a trench contact via, one or more embodiments of the present invention include first using a gate aligned trench contact process. Such a process may be implemented to form trench contact structures for semiconductor structure fabrication, e.g., for integrated circuit fabrication. In an embodiment, a trench contact pattern is formed as aligned to an existing gate pattern. By contrast, conventional approaches typically involve an additional lithography process with tight registration of a lithographic contact pattern to an existing gate pattern in

combination with selective contact etches. For example, a conventional process may include patterning of a poly (gate) grid with separate patterning of contact features.

[0071] Figure 9 illustrates a computing device 900 in accordance with one implementation of the invention. The computing device 900 houses a board 902. The board 902 may include a number of components, including but not limited to a processor 904 and at least one communication chip 906. The processor 904 is physically and electrically coupled to the board 902. In some implementations the at least one communication chip 906 is also physically and electrically coupled to the board 902. In further implementations, the communication chip 906 is part of the processor 904.

[0072] Depending on its applications, computing device 900 may include other components that may or may not be physically and electrically coupled to the board 902. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[0073] The communication chip 906 enables wireless communications for the transfer of data to and from the computing device 900. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 906 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 900 may include a plurality of communication chips 906. For instance, a first communication chip 906 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 906 may

be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0074] The processor 904 of the computing device 900 includes an integrated circuit die packaged within the processor 904. In some implementations of the invention, the integrated circuit die of the processor includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention. The term "processor" may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0075] The communication chip 906 also includes an integrated circuit die packaged within the communication chip 906. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0076] In further implementations, another component housed within the computing device 900 may contain an integrated circuit die that includes one or more devices, such as MOS-FET transistors built in accordance with implementations of the invention.

[0077] In various implementations, the computing device 900 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 900 may be any other electronic device that processes data.

[0078] Thus, embodiments of the present invention include self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures.

[0079] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length in a first direction. A gate structure is disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction. A pair of gate edge isolation structures is centered with the semiconductor fin. A first of the pair of gate

edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

[0080] In one embodiment, the semiconductor structure further includes source and drain regions disposed in the semiconductor fin, on either side of the gate structure. A first trench contact is disposed over the source region and a second trench contact disposed over the drain region. Each of the first and second trench contacts has a first end opposite a second end in the second direction. The first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the first trench contact and to the first end of the second trench contact. The second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the first trench contact and to the second end of the second trench contact.

[0081] In one embodiment, the semiconductor structure further includes a second semiconductor fin disposed above the substrate and having a length in the first direction, the second semiconductor fin spaced apart from the first semiconductor fin. A second gate structure is disposed over the second semiconductor fin, the second gate structure having a first end opposite a second end in the second direction. The second of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the second gate structure. A third gate edge isolation structure is disposed directly adjacent to the second end of the second gate structure. The third gate edge isolation structure and the second of the pair of gate edge isolation structures are centered with the second semiconductor fin.

[0082] In one embodiment, the semiconductor structure further includes a local interconnect disposed above and electrically coupling the first and second gate structures.

[0083] In one embodiment, the local interconnect is self-aligned with the pair of and the third gate edge isolation structures.

[0084] In one embodiment, the gate structure is an N-type gate structure, and the second gate structure is a P-type gate structure.

[0085] In one embodiment, the gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0086] In one embodiment, the pair of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0087] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length. Alternating source/drain and channel regions are disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin. The semiconductor structure also includes a plurality of gate edge isolation structures. An adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. A gate local interconnect is disposed above one of the gate structures and between a pair of the plurality of gate edge isolation structures.

[0088] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the gate local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

[0089] In one embodiment, the semiconductor structure further includes a trench contact local interconnect disposed above one of the trench contacts and between a second pair of the plurality of gate edge isolation structures.

[0090] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the second pair of the plurality of gate edge isolation structures.

[0091] In one embodiment, each gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0092] In one embodiment, each of the plurality of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0093] In an embodiment, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length. Alternating source/drain and channel regions are disposed in the length of the semiconductor fin, each source/drain region having an associated trench contact disposed over the semiconductor fin, and each channel region having an associated gate structure disposed over the semiconductor fin.

The semiconductor structure also includes a plurality of gate edge isolation structures. An adjacent trench contact and gate structure are separated by one gate edge isolation structure of the plurality of gate edge isolation structures. A trench contact local interconnect is disposed above one of the trench contacts and between a pair of the plurality of gate edge isolation structures.

[0094] In one embodiment, the semiconductor structure further includes a dielectric cap disposed on the trench contact local interconnect, the dielectric cap disposed between the pair of the plurality of gate edge isolation structures.

[0095] In one embodiment, each gate structure includes a high-k gate dielectric layer and a metal gate electrode.

[0096] In one embodiment, each of the plurality of gate edge isolation structures is composed of a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[0097] In an embodiment, a method of fabricating a semiconductor structure involves forming first and second parallel semiconductor fins above a substrate. The method also involves forming dummy spacers adjacent the sidewalls of each of the first and second semiconductor fins. The dummy spacers of the first semiconductor fin are non-continuous with the dummy spacers of the second semiconductor fin. The method also involves forming an isolation structure between the dummy spacers of the first and second semiconductor fins. The method also involves removing the dummy spacers. The method also involves forming a first replacement gate structure over the first semiconductor fin and a second replacement gate structure over the second semiconductor fin, wherein the first and second gate structures are directly adjacent to, and separated from one another by, the isolation structure.

[0098] In one embodiment, the method also involves forming a first pair of trench contacts over the first semiconductor fin and a second pair of trench contacts over the second semiconductor fin. The first and pairs of trench contacts are directly adjacent to, and separated from one another by, the isolation structure.

[0099] In one embodiment, the method also involves, subsequent to forming an isolation structure and prior to removing the dummy spacers, recessing the first and second semiconductor fins.

[00100] In one embodiment, forming the dummy spacers involves forming and etching a polycrystalline silicon layer.

[00101] In one embodiment, forming the isolation structure involves depositing and planarizing a material such as, but not limited to, silicon oxide, silicon nitride, silicon carbide, or a combination thereof.

[00102] In one embodiment, forming one or both of the first and second replacement gate structures involves forming a high-k gate dielectric layer and a metal gate electrode.

[00103] In one embodiment, the method also involves forming a local interconnect above and electrically coupling the first and second replacement gate structures.

CLAIMS

What is claimed is:

1. An integrated circuit structure, comprising:

a first fin having a longest dimension along a first direction;

a second fin having a longest dimension along the first direction;

a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction;

a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction;

a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure having a length along the first direction greater than a length of the first gate structure and the second gate structure along the first direction; and

a dielectric material laterally adjacent to and in contact with the gate edge isolation structure, and the dielectric material having a composition different than a composition of the gate edge isolation structure.

2. The integrated circuit structure of claim 1, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode, and wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode.

3. The integrated circuit structure of claim 2, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

4. The integrated circuit structure of claim 3, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

5. The integrated circuit structure of claim 2, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

6. The integrated circuit structure of claim 1, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

7. The integrated circuit structure of claim 6, further comprising:

a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

8. The integrated circuit structure of claim 7, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

9. The integrated circuit structure of claim 8, further comprising:

a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

10. The integrated circuit structure of claim 1, wherein the gate edge isolation structure comprises silicon and nitrogen.

11. A method of fabricating and integrated circuit structure, the method comprising:

forming a first fin having a longest dimension along a first direction;

forming a second fin having a longest dimension along the first direction;

forming a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction;

forming a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate

structure having an edge facing an edge of the first gate structure along the second direction;

forming a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure having a length along the first direction greater than a length of the first gate structure and the second gate structure along the first direction; and

forming a dielectric material laterally adjacent to and in contact with the gate edge isolation structure, and the dielectric material having a composition different than a composition of the gate edge isolation structure.

12. The method of claim 11, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode, and wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode.

13. The method of claim 12, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

14. The method of claim 13, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

15. The method of claim 12, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

16. The method of claim 11, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

17. The method of claim 16, further comprising:

forming a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

18. The method of claim 17, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

19. The method of claim 18, further comprising:

forming a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

20. The method of claim 11, wherein the gate edge isolation structure comprises silicon and nitrogen.

21. A method of fabricating an integrated circuit structure, the method comprising:

forming a first fin comprising silicon, the first fin having a longest dimension along a first direction;

forming a second fin comprising silicon, the second fin having a longest dimension along the first direction;

forming an isolation material between the first fin and the second fin;

forming a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

forming a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

forming a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

forming a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

22. The method of claim 21, wherein the gate edge isolation structure comprises silicon and nitrogen.

23. The method of claim 21, wherein the dielectric material is in contact with the gate edge isolation structure.

24. The method of claim 21, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.

25. The method of claim 24, wherein the gate edge isolation structure is in contact with a metal gate electrode layer of the first gate structure and with a metal gate electrode layer of the second gate structure.

26. The method of claim 24, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

27. The method of claim 21, wherein the gate edge isolation structure has a height greater than a height of the first gate structure and greater than a height of the second gate structure.

28. The method of claim 27, further comprising:

forming a local interconnect disposed over a portion of the first gate structure, over a portion of the gate edge isolation structure, and over a portion of the second gate structure.

29. The method of claim 28, wherein the local interconnect electrically couples the first gate structure to the second gate structure.

30. The method of claim 28, further comprising:

forming a gate contact on a portion of the local interconnect over the first gate structure, but not on a portion of the local interconnect over the second gate structure.

ABSTRACT

Self-aligned gate edge and local interconnect structures and methods of fabricating self-aligned gate edge and local interconnect structures are described. In an example, a semiconductor structure includes a semiconductor fin disposed above a substrate and having a length in a first direction. A gate structure is disposed over the semiconductor fin, the gate structure having a first end opposite a second end in a second direction, orthogonal to the first direction. A pair of gate edge isolation structures is centered with the semiconductor fin. A first of the pair of gate edge isolation structures is disposed directly adjacent to the first end of the gate structure, and a second of the pair of gate edge isolation structures is disposed directly adjacent to the second end of the gate structure.

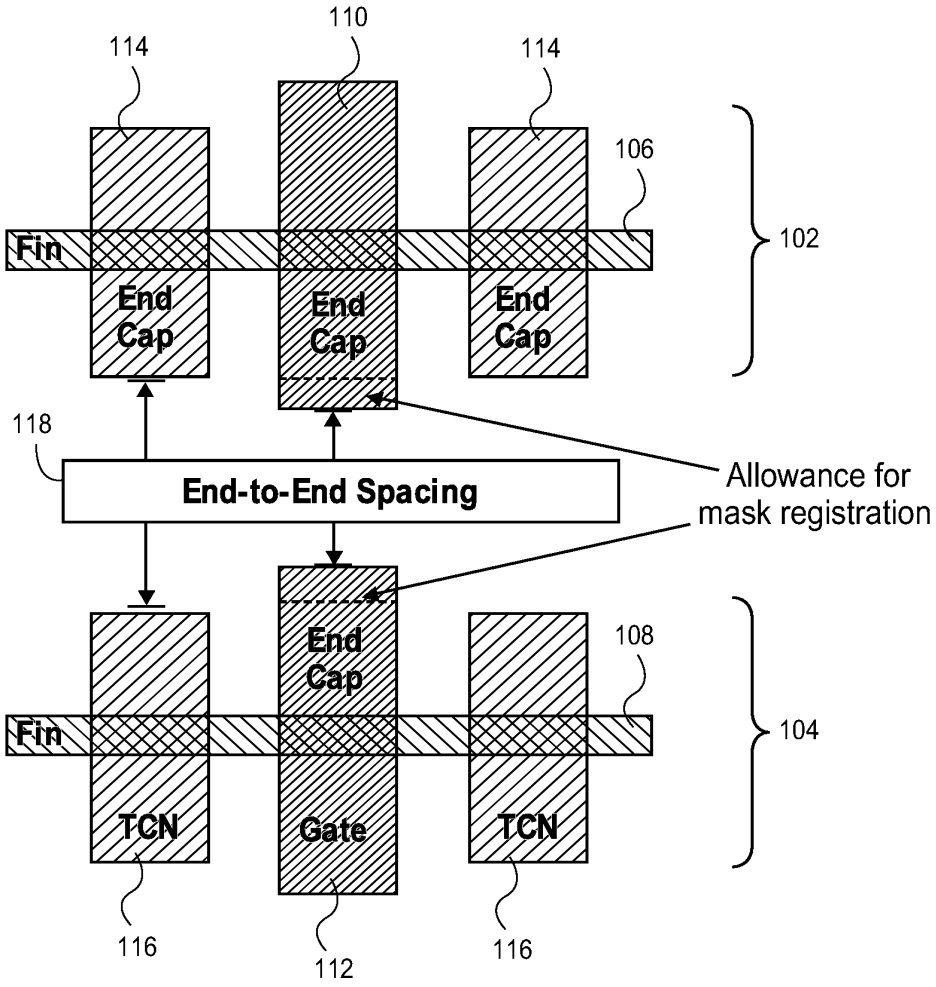

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Fin
End Cap
End Cap
End Cap
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End-to-End Spacing
Allowance for mask registration
End Cap
108
104
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TCN
Gate
TCN
116
112
116

FIG. 1

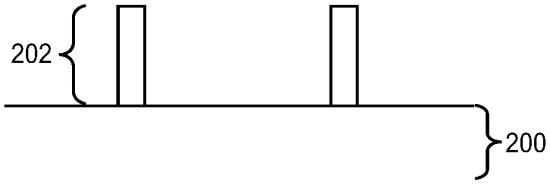


FIG. 2A

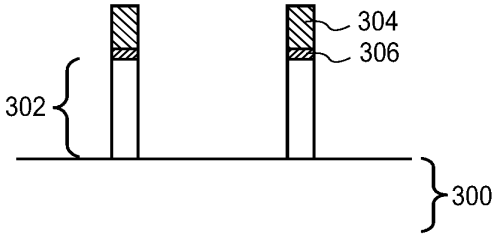


FIG. 3A

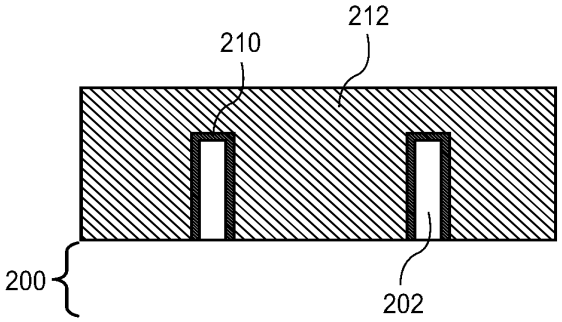


FIG. 2B

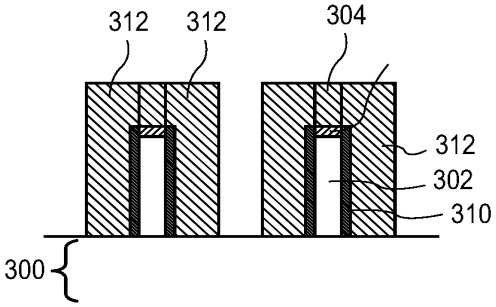


FIG. 3B

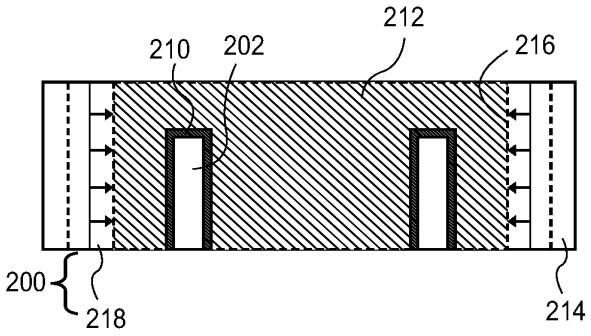


FIG. 2C

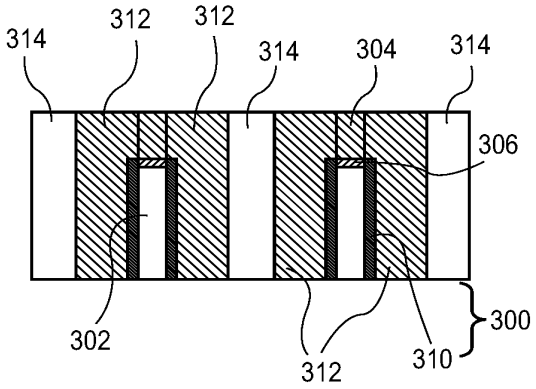


FIG. 3C

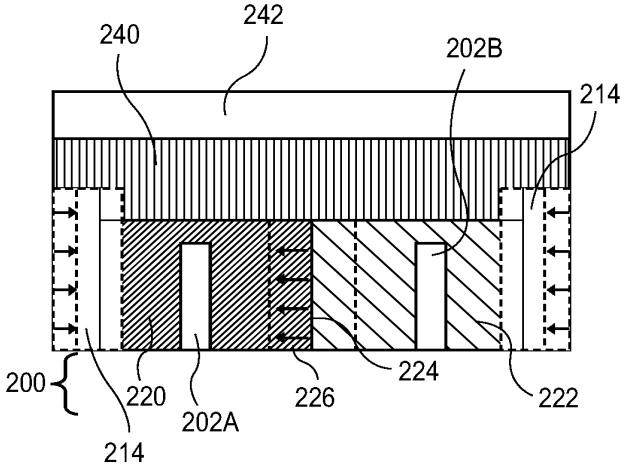


FIG. 2D

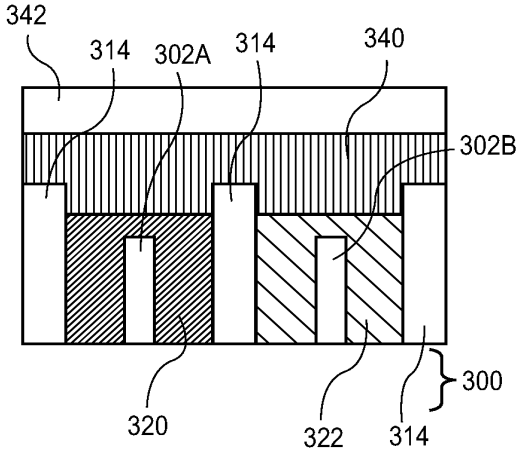


FIG. 3D

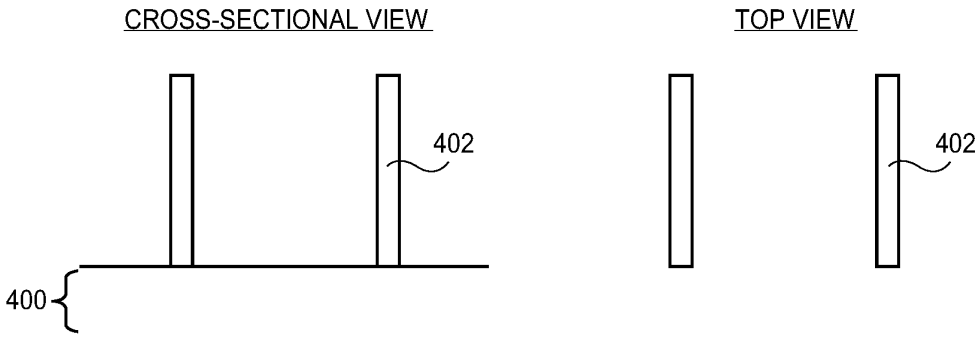


FIG. 4A

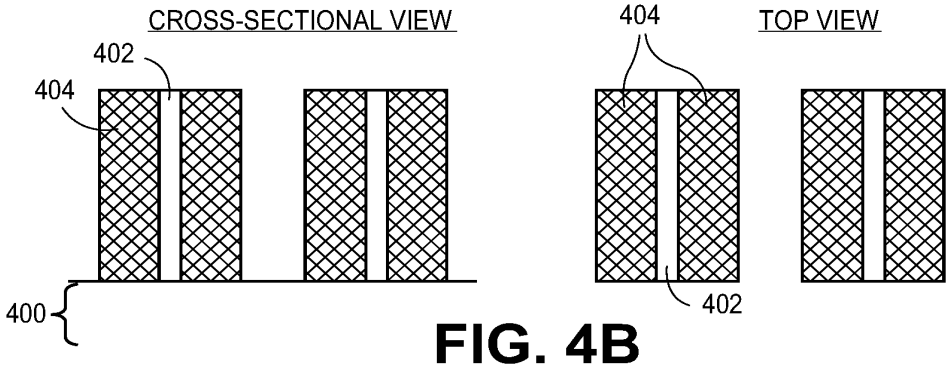


FIG. 4B

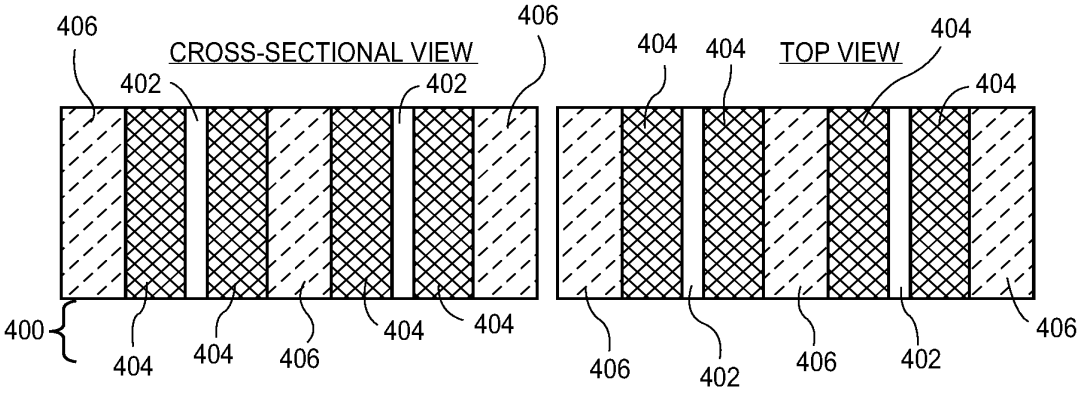


FIG. 4C

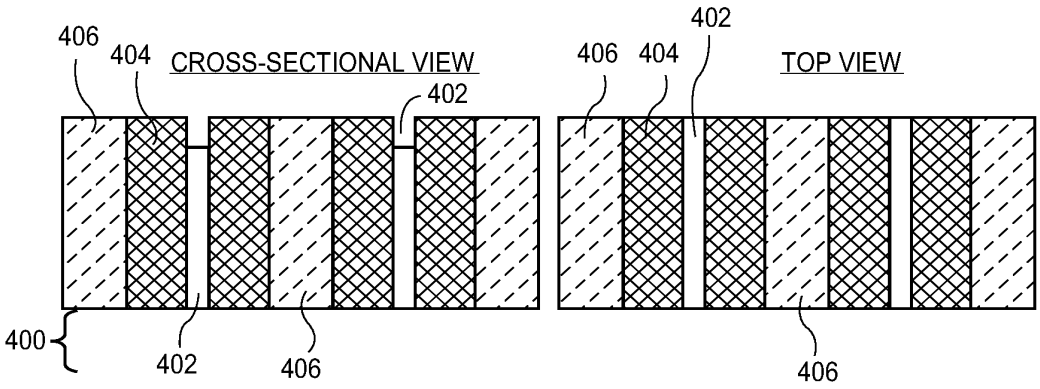


FIG. 4D

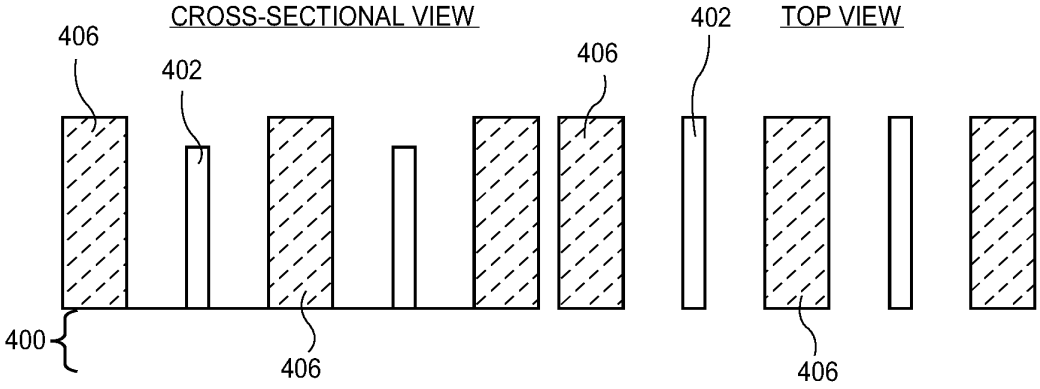


FIG. 4E

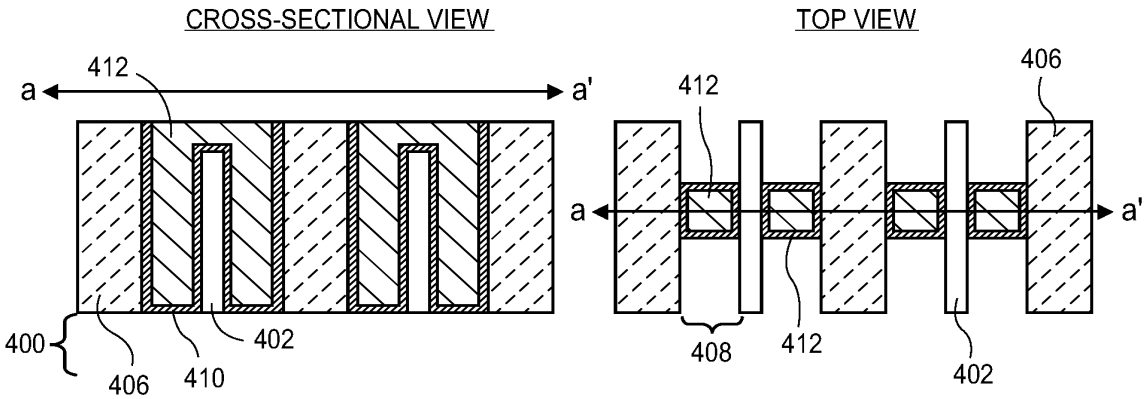


FIG. 4F

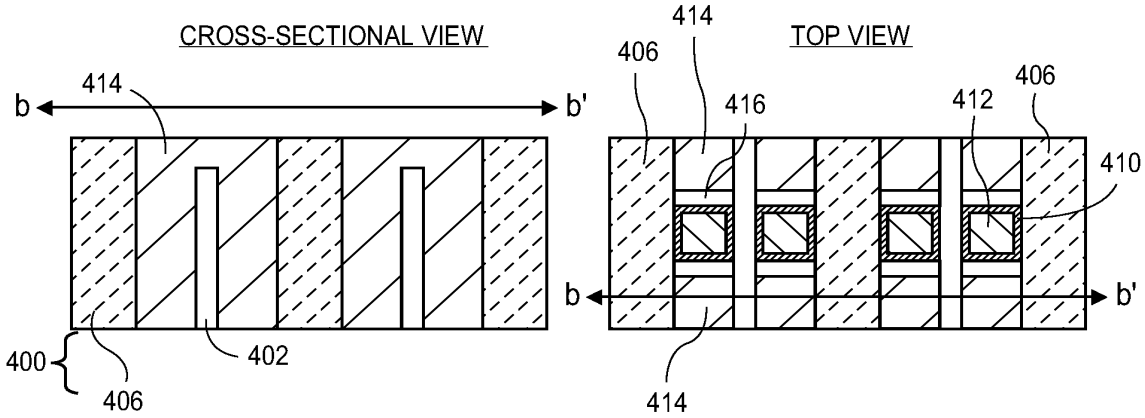


FIG. 4G

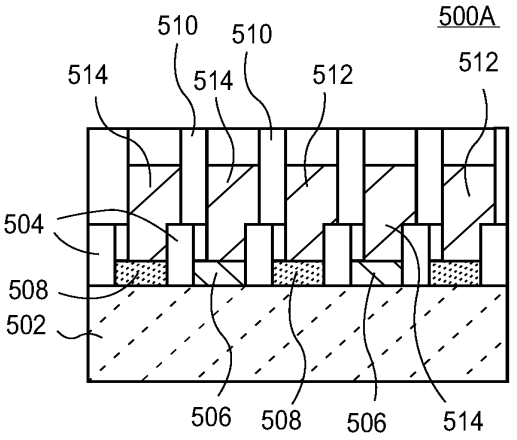


FIG. 5A

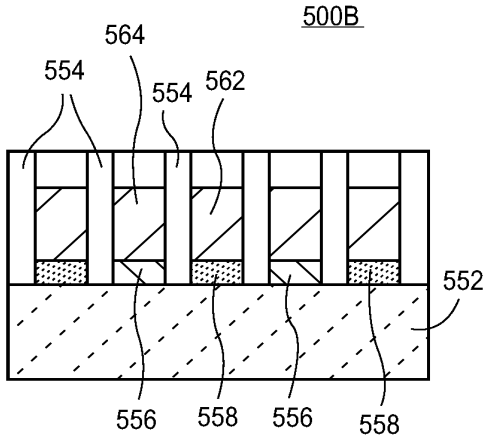


FIG. 5B

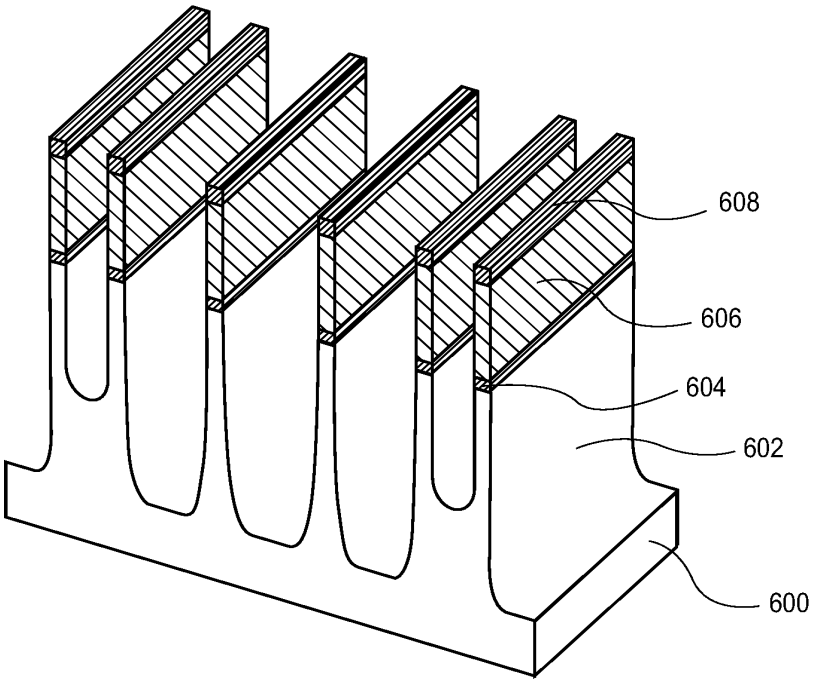


FIG. 6A

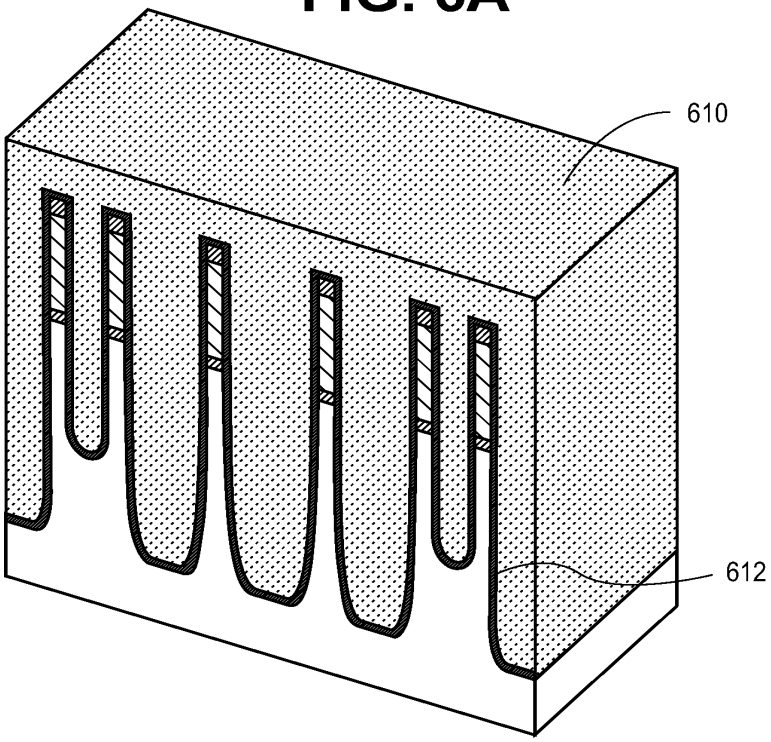


FIG. 6B

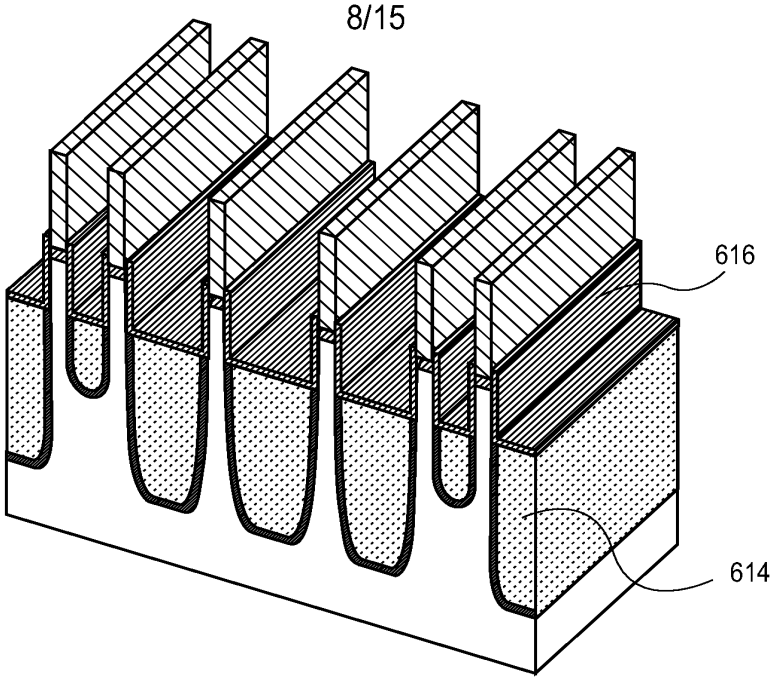


FIG. 6C

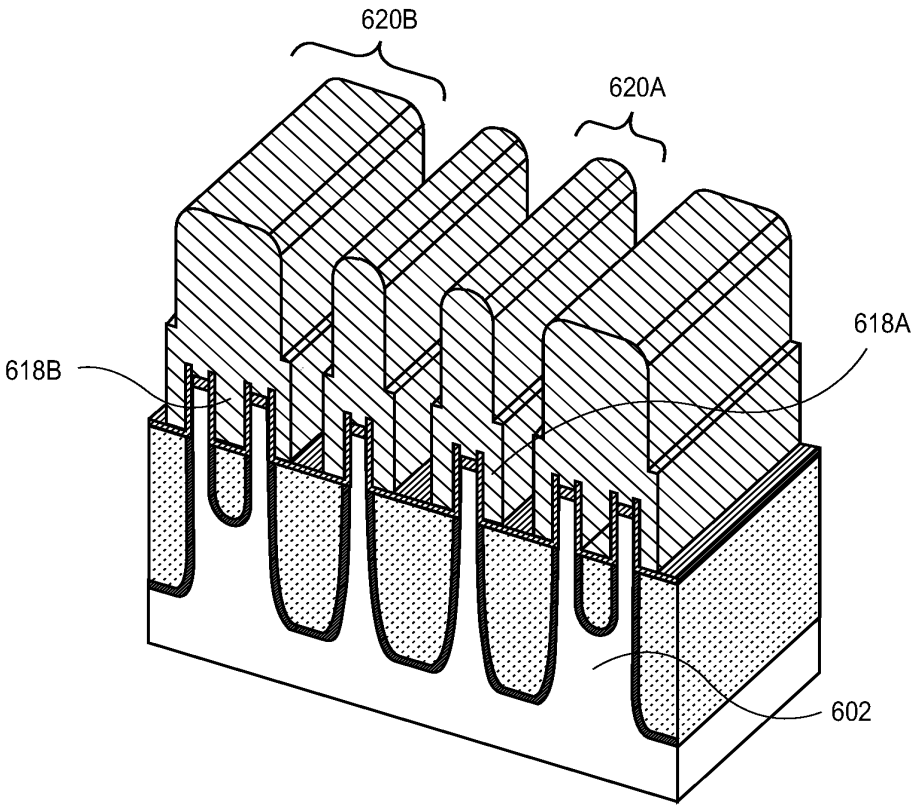


FIG. 6D

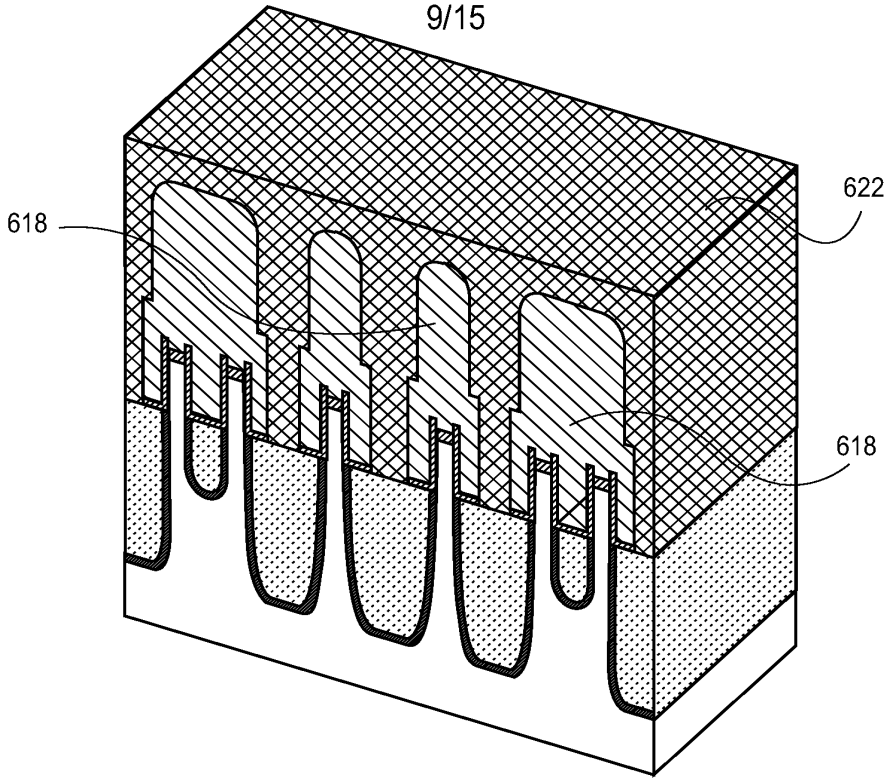


FIG. 6E

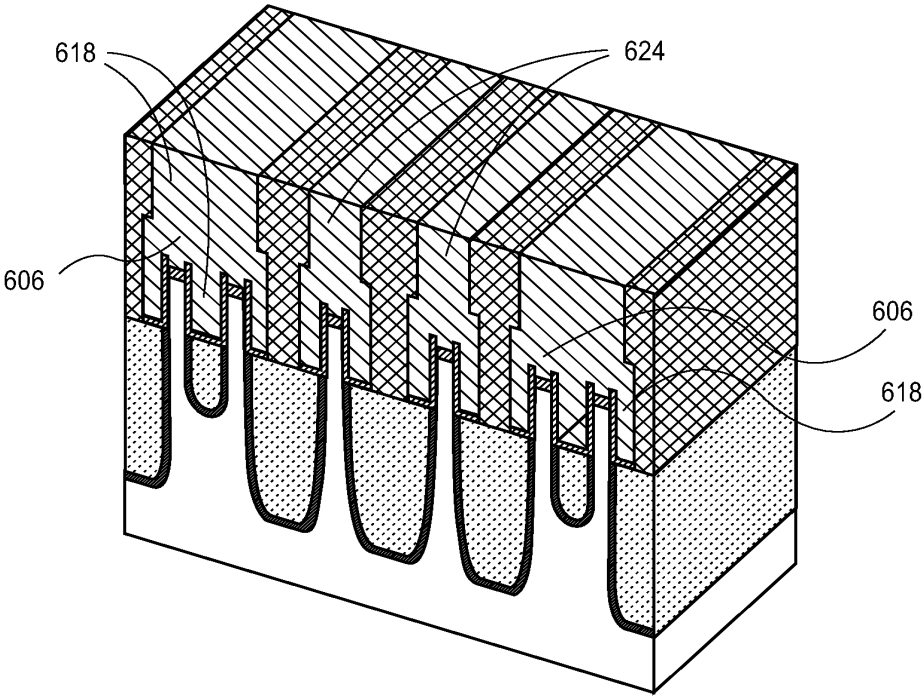


FIG. 6F

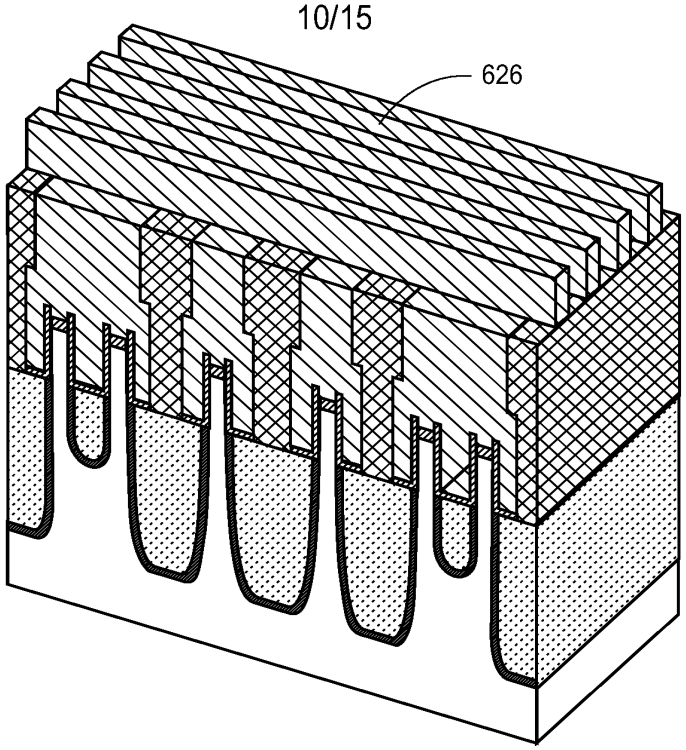


FIG. 6G

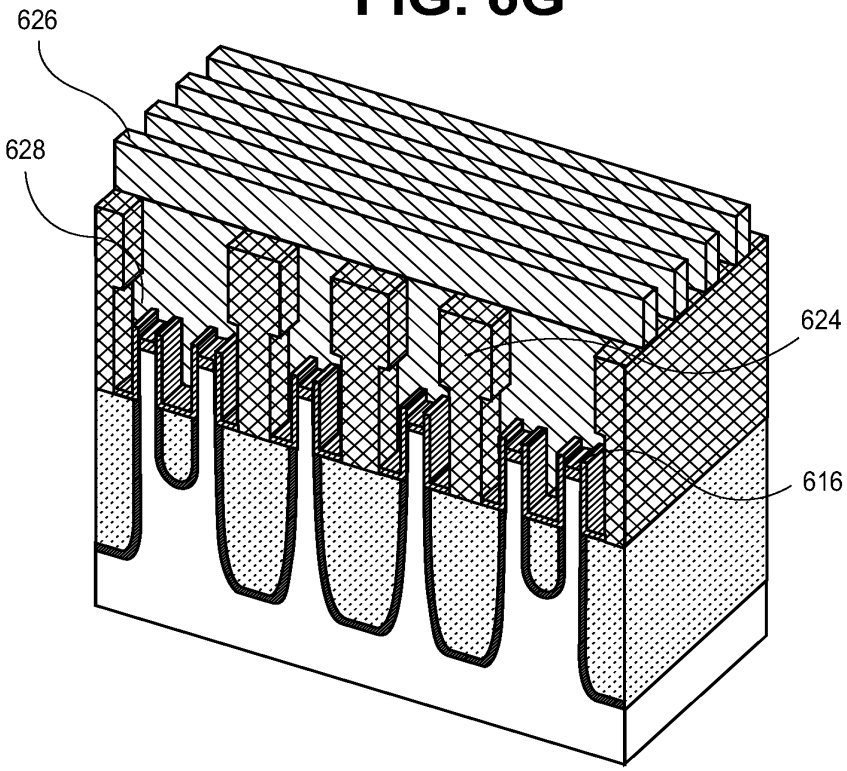


FIG. 6H

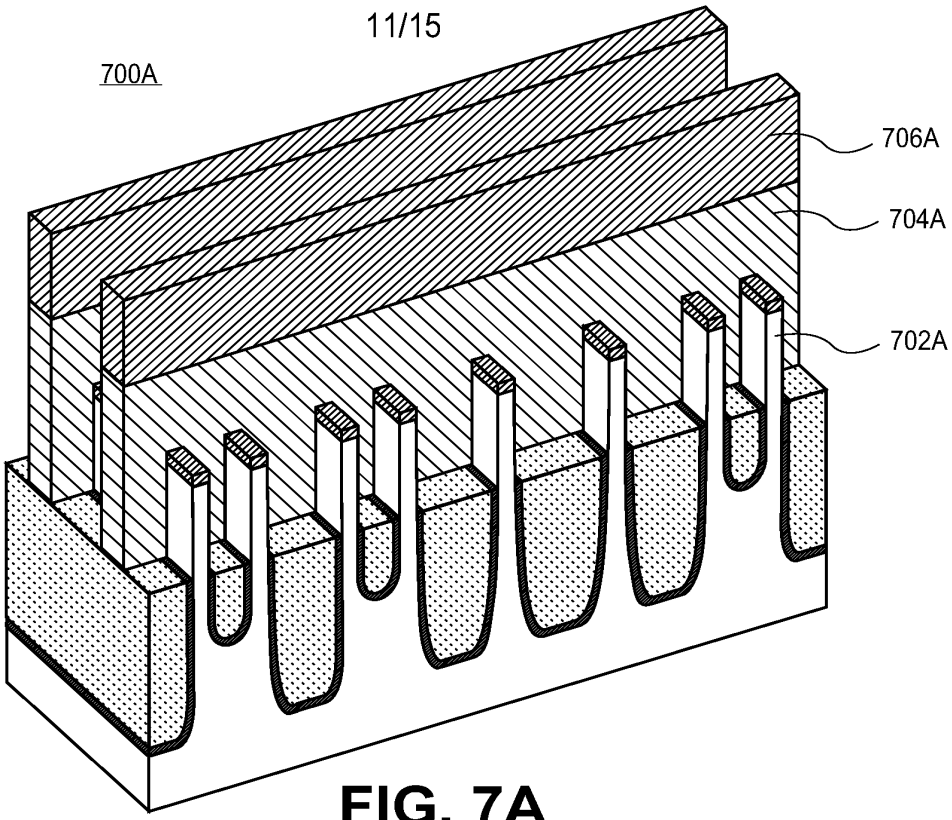


FIG. 7A

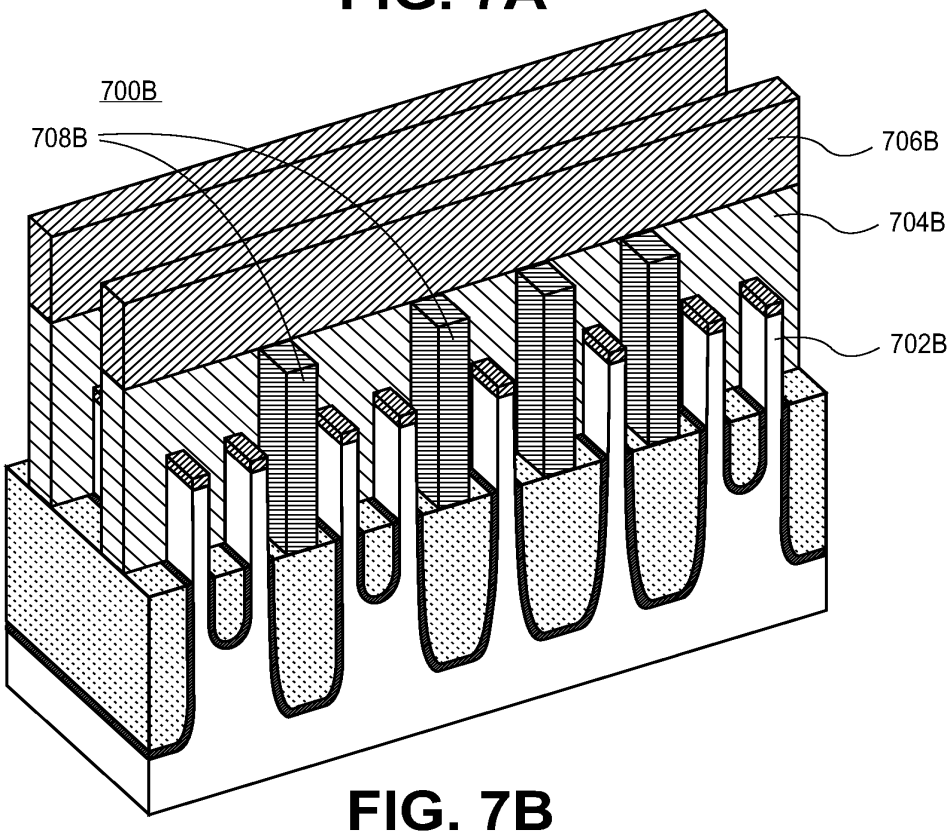


FIG. 7B

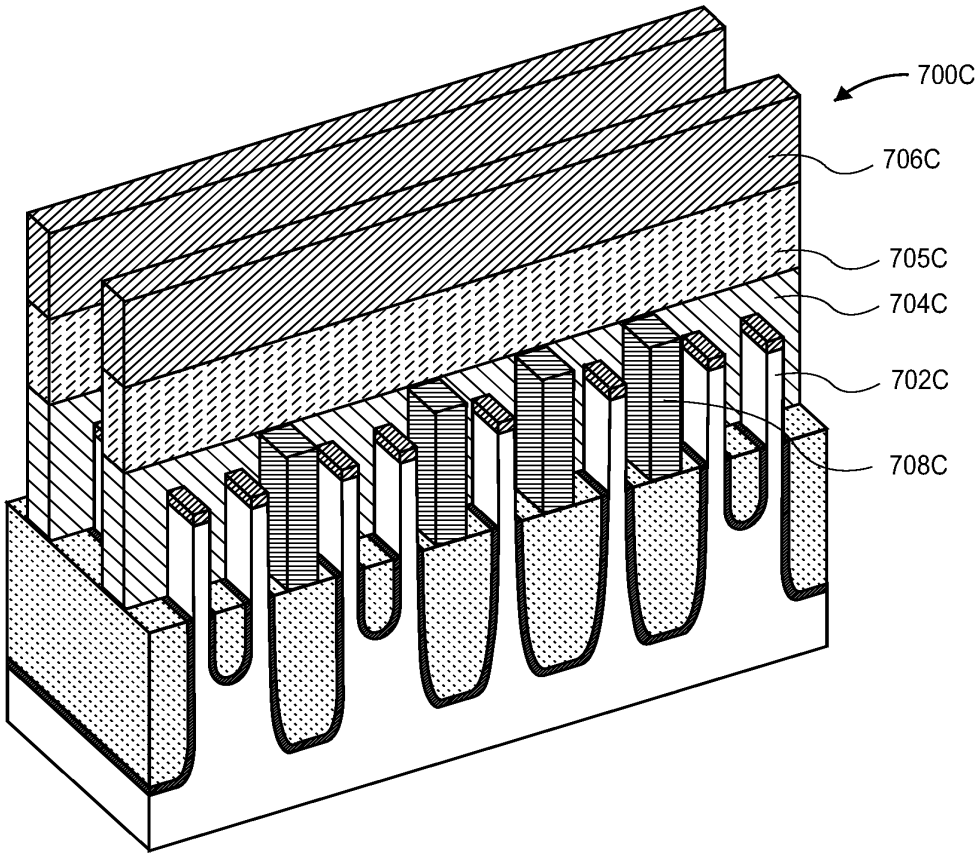


FIG. 7C

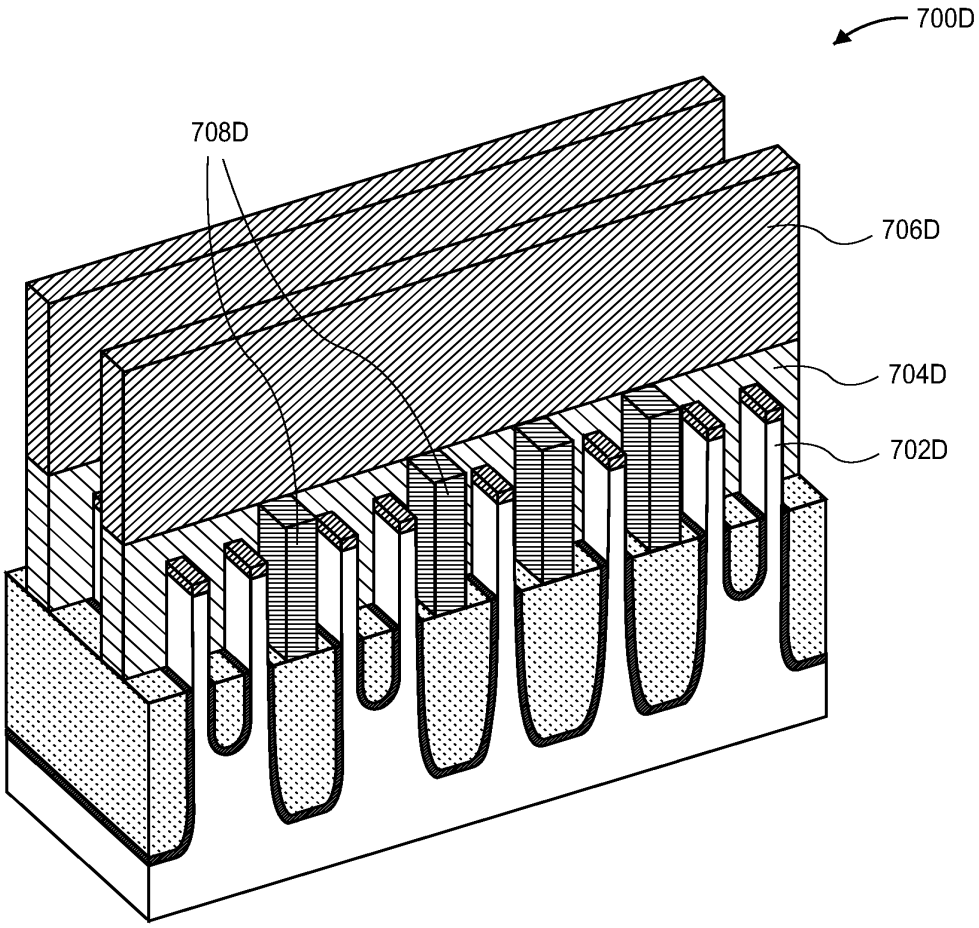


FIG. 7D

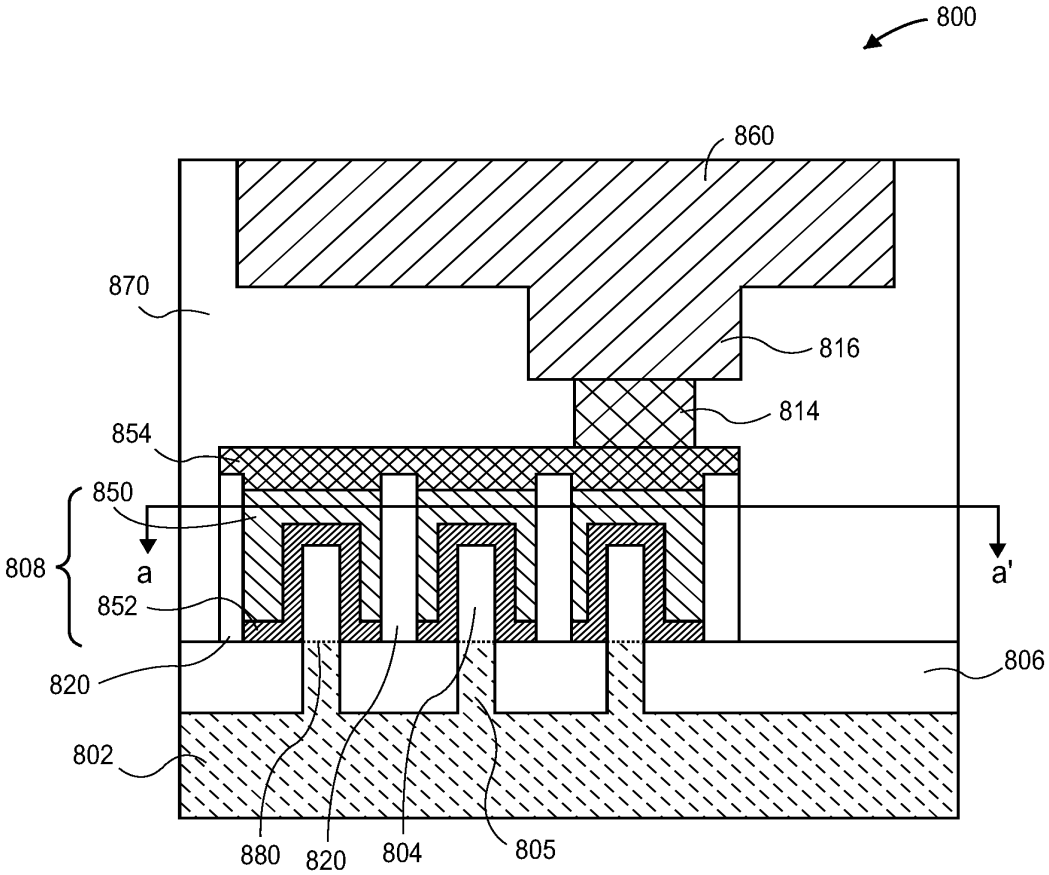

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FIG. 8A

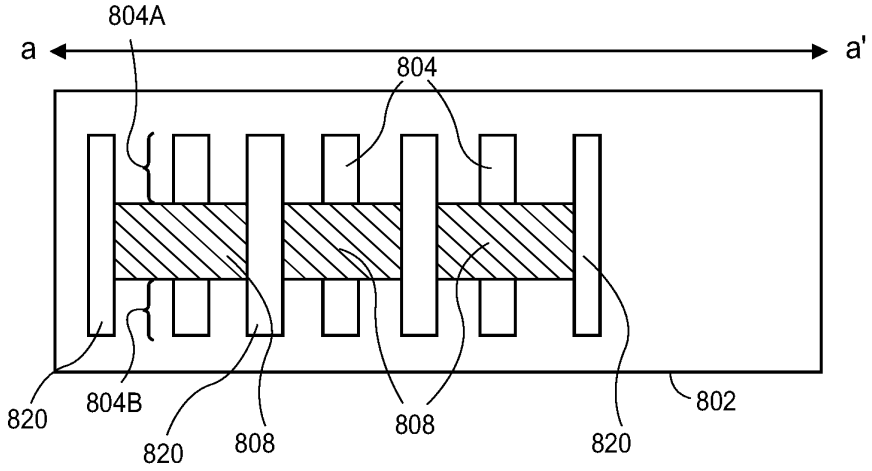

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820
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FIG. 8B

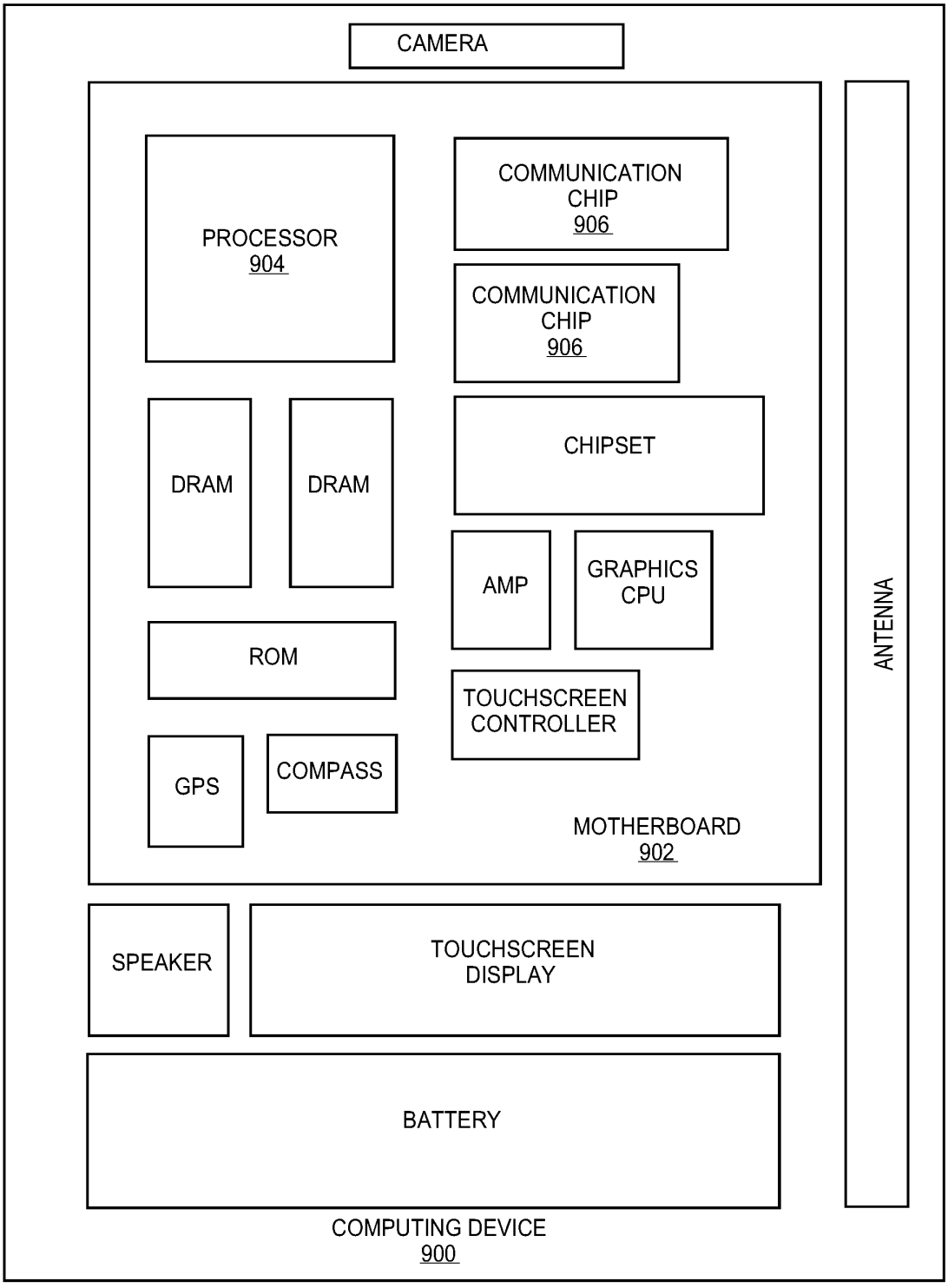

CAMERA
PROCESSOR
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COMMUNICATION
CHIP
906
COMMUNICATION
CHIP
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DRAM
DRAM
CHIPSET
AMP
GRAPHICS
CPU
ROM
TOUCHSCREEN
CONTROLLER
GPS
COMPASS
MOTHERBOARD
902
ANTENNA
SPEAKER
TOUCHSCREEN
DISPLAY
BATTERY
COMPUTING DEVICE
900

FIG. 9

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US-C1/111548-235422
	Application Number	
Title of Invention	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Inventor 2 Remove

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Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
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Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US-C1/111548-235422
	Application Number	
Title of Invention	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME	

City	Portland	State/Province	OR	Country of Residence	US

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Address 2			
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Postal Code	97229	Country	US

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Szuya	S.	LIAO	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

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Address 1	4460 NW Malhuer Avenue		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

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☐ **An Address is being provided for the correspondence Information of this application.**

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Title of the Invention	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME		
Attorney Docket Number	P60397US-C1/111548-235422	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	15	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P60397US-C1/111548-235422
	Application Number	
Title of Invention	SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT AND METHOD TO FABRICATE SAME	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	31817		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15024750	2016-03-24

PTO/AIA/14 (11-15)
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Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
15024750	a 371 of international	PCT/US2013/076673	2013-12-19
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.			Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Intel Corporation		
Mailing Address Information For Applicant:			
Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Justin K. Brask/			Date (YYYY-MM-DD)	2017-10-20
First Name	Justin K.	Last Name	Brask	Registration Number	61080

Additional Signature may be generated within this form by selecting the Add button. Add

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	Not Yet Assigned
Filing Date	Herewith
First Inventor	Milton Clair WEBB et al.
Art Unit	
Attorney Docket No.	P60397US-C1/111548-235422

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the continuation Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 CFR § l.98(d)(l) copies of the references were provided in the prior application, 15/024,750 filed March 24, 2016, which is relied on for priority.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has bee n made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	10-20-2017
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal */Sheri Villarreal/* *Date* 10-20-17

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**