PUBLIC
EXHIBIT 39

SAMSUNG 1052

U.S. Patent No. 9,831,306

Samsung Product (Samsung 5nm node)

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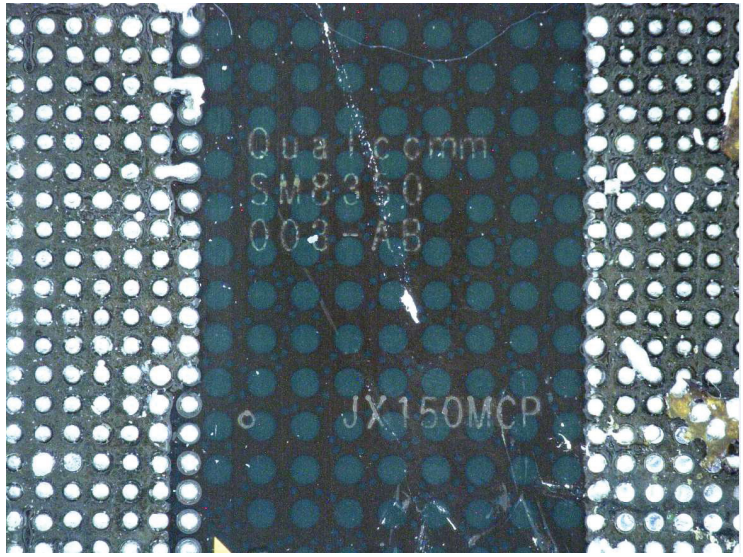
26(pre). An integrated circuit structure, comprising:	The Samsung S21 FE 5G smartphone, (hereinafter, the "Samsung Product") includes an integrated circuit structure. For example, the Samsung Product includes the Qualcomm Snapdragon 888 5G system on chip (hereinafter, the "Qualcomm SoC"). *See* Ex. 23 at 7, Photographs for the first Samsung Representative Article, Samsung Galaxy S21 FE - About Phone.

	  See Ex. 23 at 7, Photographs for the first Samsung Representative Article, Samsung Galaxy S21 FE - SoC Model.  *See* Ex. 23 at 8, Photographs for the first Samsung Representative Article. The Qualcomm SoC is manufactured using Samsung's 5nm technology node.

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Process	Process Node and Technology: 5 nm

See Ex. 91 at 5, Qualcomm Snapdragon 888 5G Mobile Platform, https://www.qualcomm.com/products/snapdragon-888-5g-mobile-platform.

Manufactured on Samsung 5nm / 5LPE

The new Snapdragon 888 is making the transition from 7nm to 5nm, but the new design doesn't merely make a process shift, it's also making a foundry shift. After being with TSMC for the 7nm generations of the Snapdragon 855 and Snapdragon 865, Qualcomm is now switching back to Samsung Foundry and their new 5LPE process node for the new Snapdragon 888.

SoC	Snapdragon 865	Snapdragon 888
…		
Mfc. Process	TSMC 7nm (N7P)	**Samsung** **5nm (5LPE)**

See Ex. 92 at 3, Qualcomm Details The Snapdragon 888 3rd Gen 5G & Cortex-X1 on 5nm, https://www.anandtech.com/show/16271/qualcomm-snapdragon-888-deep-dive.

[redacted]

U.S. Patent No. 9,831,306: Claim 26(pre)

"An integrated circuit structure, comprising:"

	[redacted]

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[redacted]

U.S. Patent No. 9,831,306

Claim 26(a): "a first fin comprising silicon, the first fin having a longest dimension along a first direction;"

26(a). a first fin comprising silicon, the first fin having a longest dimension along a first direction;	The Samsung Product includes a first fin comprising silicon, the first fin having a longest dimension along a first direction. For example, the Qualcomm SoC includes a first fin having a longest dimension along a first direction. [redacted] Further, the first fin comprises silicon.

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[redacted]

U.S. Patent No. 9,831,306: Claim 26(a)

"a first fin comprising silicon, the first fin having a longest dimension along a first direction;"

8	[redacted]

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Claim 26(b): "a second fin comprising silicon, the second fin having a longest dimension along the first direction;"

26(b). a second fin comprising silicon, the second fin having a longest dimension along the first direction;	The Samsung Product includes a second fin comprising silicon, the second fin having a longest dimension along the first direction. For example, the Qualcomm SoC includes a second fin having a longest dimension along the first direction. [redacted] Further, the second fin comprises silicon.

[redacted]

U.S. Patent No. 9,831,306: Claim 26(b)

"a second fin comprising silicon, the second fin having a longest dimension along the first direction;"

	[redacted]

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[redacted]

U.S. Patent No. 9,831,306: Claim 26(c)
"an isolation material between the first fin and the second fin;"

12	[redacted]

U.S. Patent No. 9,831,306

Claim 26(d): "a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;"

26(d). a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;	The Samsung Product includes a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode. For example, the Qualcomm SoC includes a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction. [redacted]

[redacted]

U.S. Patent No. 9,831,306: Claim 26(d)

"a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;"

	[redacted] The first gate structure comprises a first gate dielectric layer and a first gate electrode. For example, the NMOS and PMOS transistors include HfO/SiO gate dielectric. The PMOS transistors further include gate TiAlCI fill and PWF Metal (TiN); the NMOS transistors further include gate fill W/TiN liner and NWF metal (TiAlCCl).

[redacted]

U.S. Patent No. 9,831,306: Claim 26(d)

"a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;"

	[redacted]

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[redacted]

U.S. Patent No. 9,831,306: Claim 26(d)

"a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;"

	[redacted]

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Claim 26(e): "a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;"

26(e). a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;	The Samsung Product includes a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode. For example, the Qualcomm SoC includes a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction. Further, the second gate structure discontinuous with the first gate structure along the second direction. [redacted] [redacted]

[redacted]

U.S. Patent No. 9,831,306: Claim 26(e)

"a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;"

	[redacted] The second gate structure has an edge facing an edge of the first gate structure along the second direction.

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U.S. Patent No. 9,831,306: Claim 26(e)

"a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;"

	[redacted] Further, the second gate structure comprises a second gate dielectric layer and a second gate electrode. For example, the NMOS and PMOS transistors include HfO/SiO gate dielectric. The PMOS transistors further include gate TiAlCI fill and PWF Metal (TiN); the NMOS transistors further include gate fill W/TiN liner and NWF metal (TiAlCCl).

[redacted]

U.S. Patent No. 9,831,306: Claim 26(e)

"a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;"

	[redacted]

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[redacted]

U.S. Patent No. 9,831,306: Claim 26(e)

"a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;"

	[redacted]

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Claim 26(f): "a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and"

26(f). a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and	The Samsung Product includes a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material. For example, the Qualcomm SoC includes a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction. [redacted] Further, the gate edge isolation structure is over the isolation material.

[redacted]

U.S. Patent No. 9,831,306: Claim 26(f)

"a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and"

	[redacted]

U.S. Patent No. 9,831,306

Claim 26(g): "a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure."

26(g). a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.	The Samsung Product includes a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure. For example, the Qualcomm SoC includes a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure. [redacted]

[redacted]

U.S. Patent No. 9,831,306: Claim 26(g)

"a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure."

	[redacted]

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