

PUBLIC EXHIBIT 45

U.S. Patent No. 9,831,306

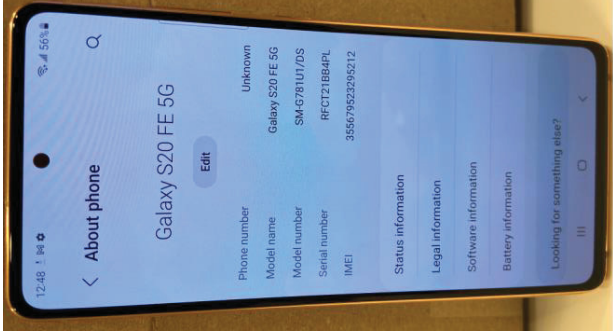
Samsung/TSMC Product (7nm node)

U.S. Patent No. 9,831,306: Claim 26(a)
“An integrated circuit structure, comprising:”

26(pre). An integrated circuit structure, comprising:

The Samsung S20 FE 5G smartphone (hereinafter, the “Samsung/TSMC Product”) includes an integrated circuit structure.

For example, the Samsung/TSMC Product includes the Qualcomm Snapdragon 865 5G system on chip (hereinafter, the “Qualcomm SoC”).

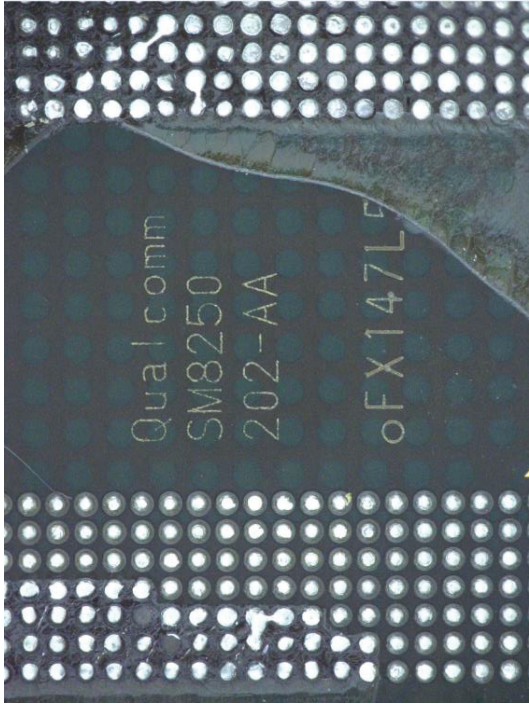


See Ex. 20 at 7, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - About Phone.

U.S. Patent No. 9,831,306: Claim 26(pre)
“An integrated circuit structure, comprising:”



See Ex. 20 at 8, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - SoC Model.



See Ex. 20 at 9, Photographs for the TSMC Representative Article.

The Qualcomm SoC is manufactured using TSMC’s 7nm technology node.

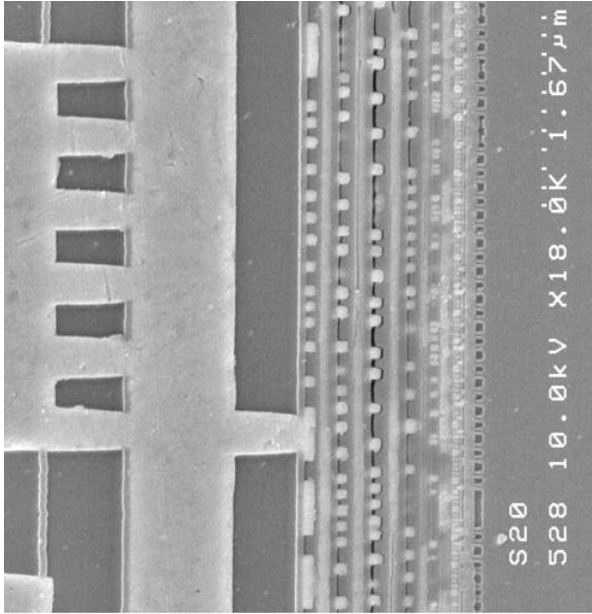
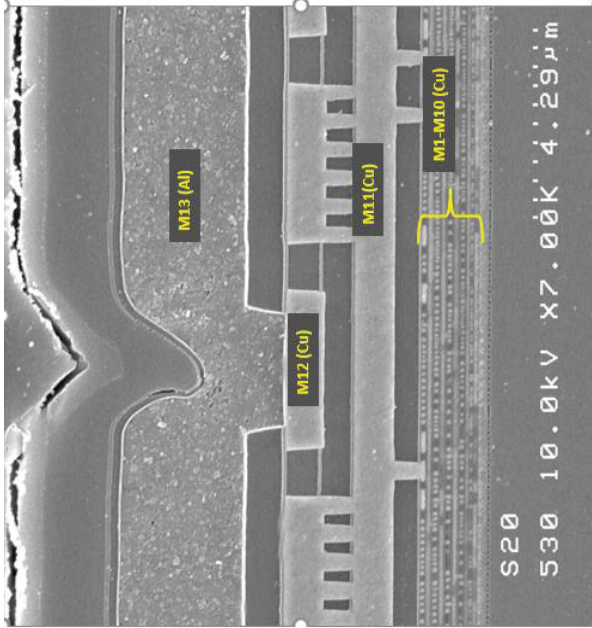
Process **Process Node and Technology: 7 nm**

See Ex. 88 at 8, Qualcomm Snapdragon 865 5G Mobile Platform, <https://www.qualcomm.com/products/snapdragon-865-5g-mobile-platform>.

The Snapdragon 865 Application Processor: TSMC 7nm N7P

With the elephant in the room of the modem configuration being out of the way, we come to the actual Snapdragon 865 application processor.

See Ex. 89 at 4, Qualcomm Announces Snapdragon 865 and 765(G)<https://www.anandtech.com/show/15178/qualcomm-announces-snapdragon-865-and-765-5g-for-all-in-2020-all-the-details>.



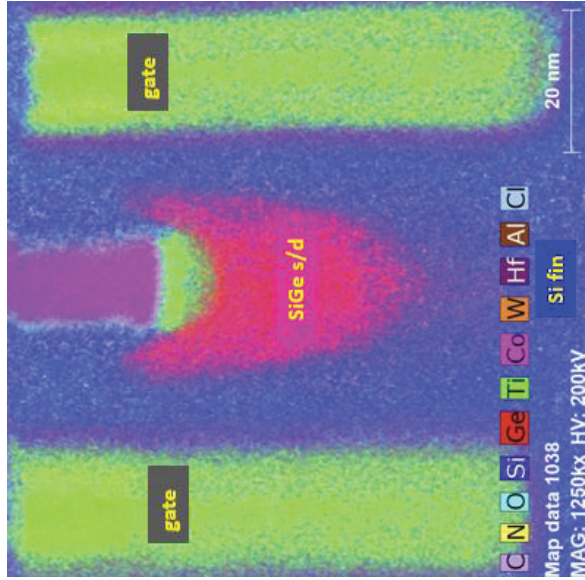
See Ex. 20 at 10 (left) (annotated), 11, Photographs for the TSMC Representative Article.

“a first fin comprising silicon, the first fin having a longest dimension along a first direction,”

26(a). a first fin comprising silicon, the first fin having a longest dimension along a first direction;

The Samsung/TSMC Product includes a first fin comprising silicon, the first fin having a longest dimension along a first direction.

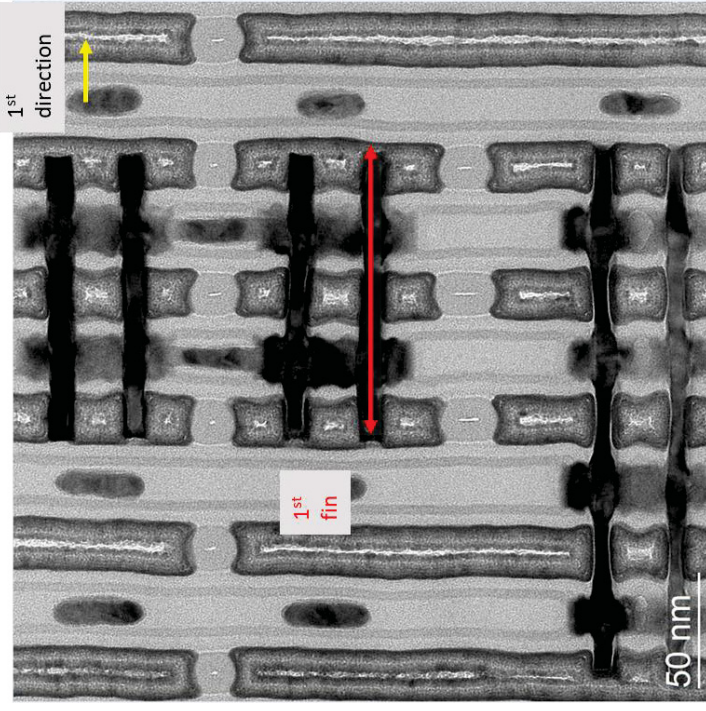
For example, the Qualcomm SoC includes a first fin comprising silicon.



See Ex. 20 at 122, Photographs for the TSMC Representative Article (annotated).

The first fin has a longest dimension along a first direction.

“a first fin comprising silicon, the first fin having a longest dimension along a first direction,”



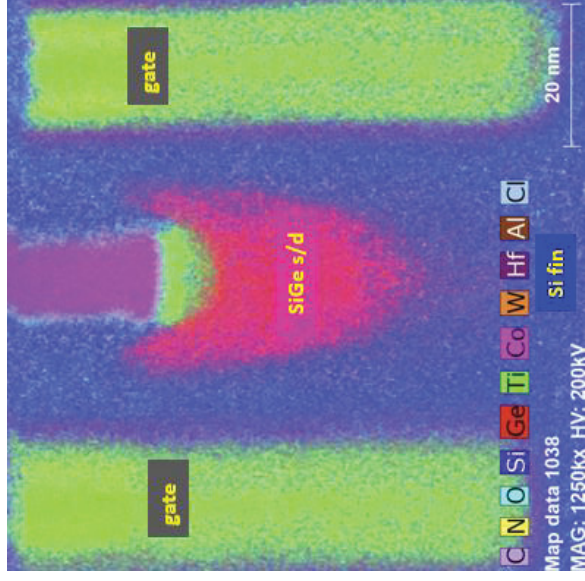
See Ex. 20 at 20, Photographs for the TSMC Representative Article (annotated).

“a second fin comprising silicon, the second fin having a longest dimension along the first direction;”

26(b). a second fin comprising silicon, the second fin having a longest dimension along the first direction;

The Samsung/TSMC Product includes a second fin comprising silicon, the second fin having a longest dimension along the first direction.

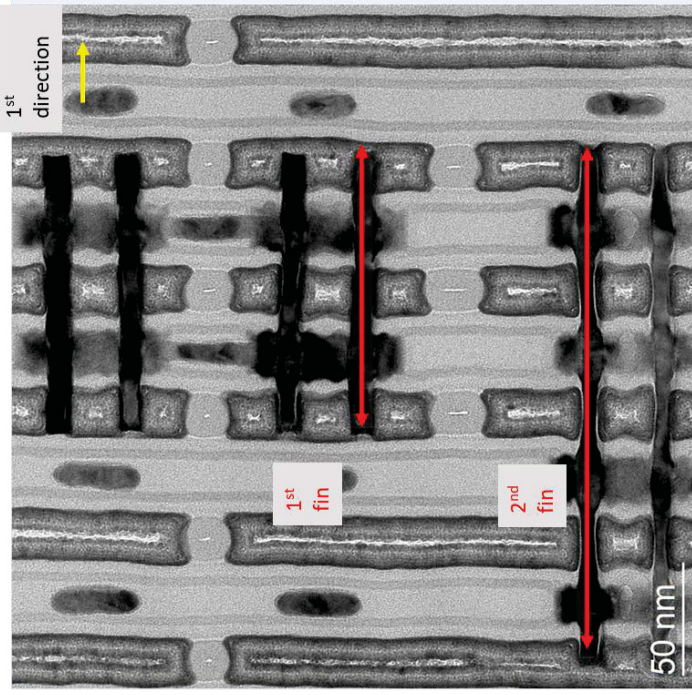
For example, the Qualcomm SoC includes a second silicon fin.



See Ex. 20 at 12, Photographs for the TSMC Representative Article (annotated).

The second silicon fin has a longest dimension along the first direction.

U.S. Patent No. 9,831,306: Claim 26(b)
“a second fin comprising silicon, the second fin having a longest dimension along the first direction;”

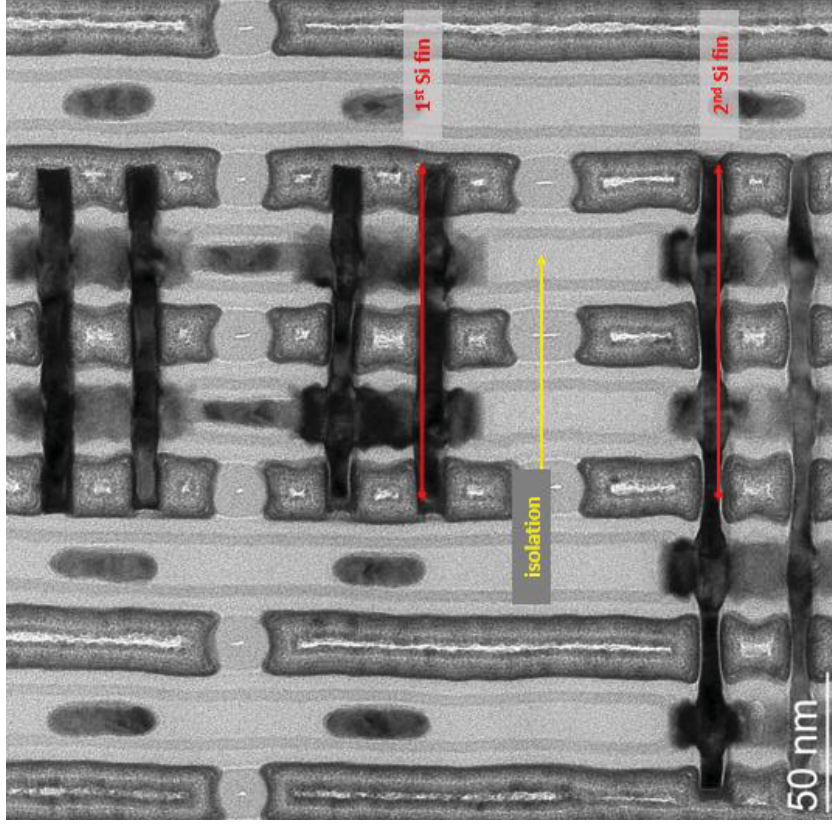


See Ex. 20 at 20, Photographs for the TSMC Representative Article (annotated).

“an isolation material between the first fin and the second fin;”

The Samsung/TSMC Product includes an isolation material between the first fin and the second fin.

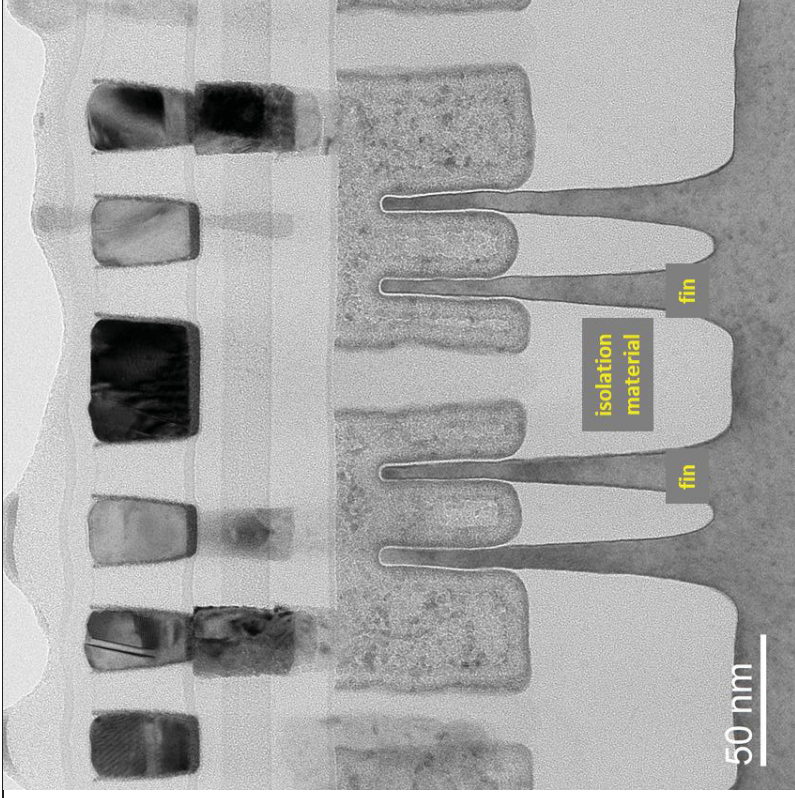
For example, the Qualcomm SoC includes isolation material between the first silicon fin and the second silicon fin.



See Ex. 20 at 20, Photographs for the TSMC Representative Article (annotated).

26(c). an isolation material between the first fin and the second fin;

U.S. Patent No. 9,831,306: Claim 26(c)
“an isolation material between the first fin and the second fin;”



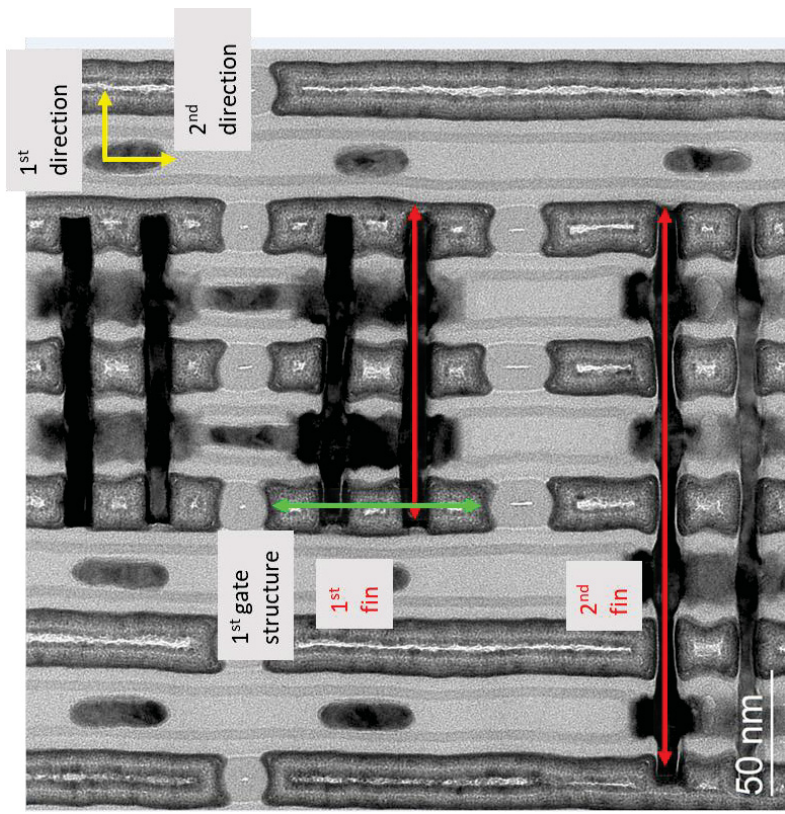
See Ex. 20 at 13, Photographs for the TSMC Representative Article (annotated).

“a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;”

26(d). a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;

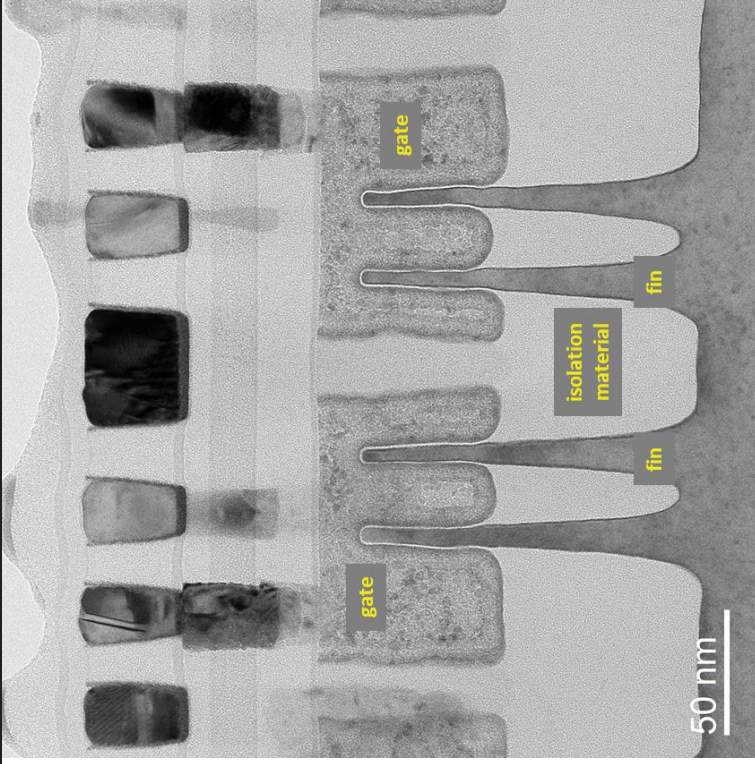
The Samsung/TSMC Product includes a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode.

For example, the Qualcomm SoC includes a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction.



See Ex. 20 at 20, Photographs for the TSMC Representative Article (annotated).

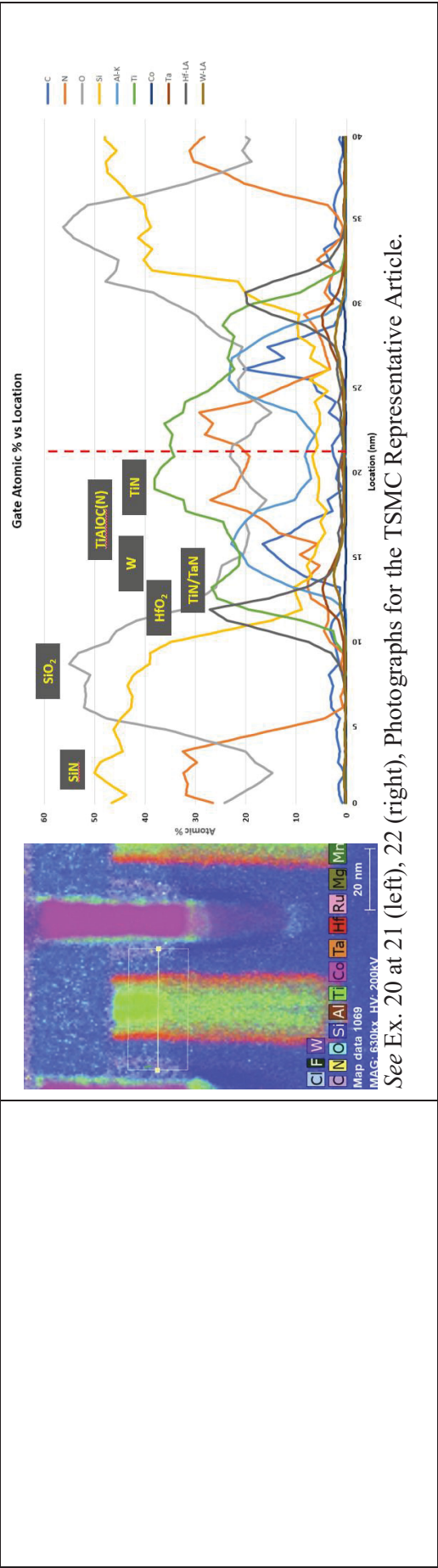
“a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;”



See Ex. 20 at 13, Photographs for the TSMC Representative Article (annotated).

The first gate structure comprises a first gate dielectric layer and a first gate electrode. For example, the transistor includes an HfO_2 gate dielectric with $\text{TiN}/\text{TaN}/\text{W}/\text{TiAlOC}(\text{N})/\text{TiN}$ work function and fill materials as the gate electrode.

“a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;”

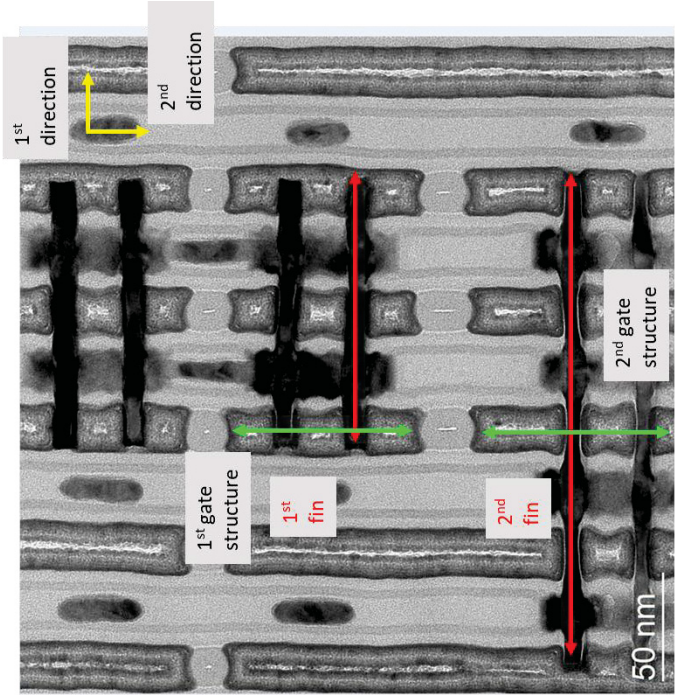


See Ex. 20 at 21 (left), 22 (right), Photographs for the TSMC Representative Article.

“a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;”

The Samsung/TSMC Product includes a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode.

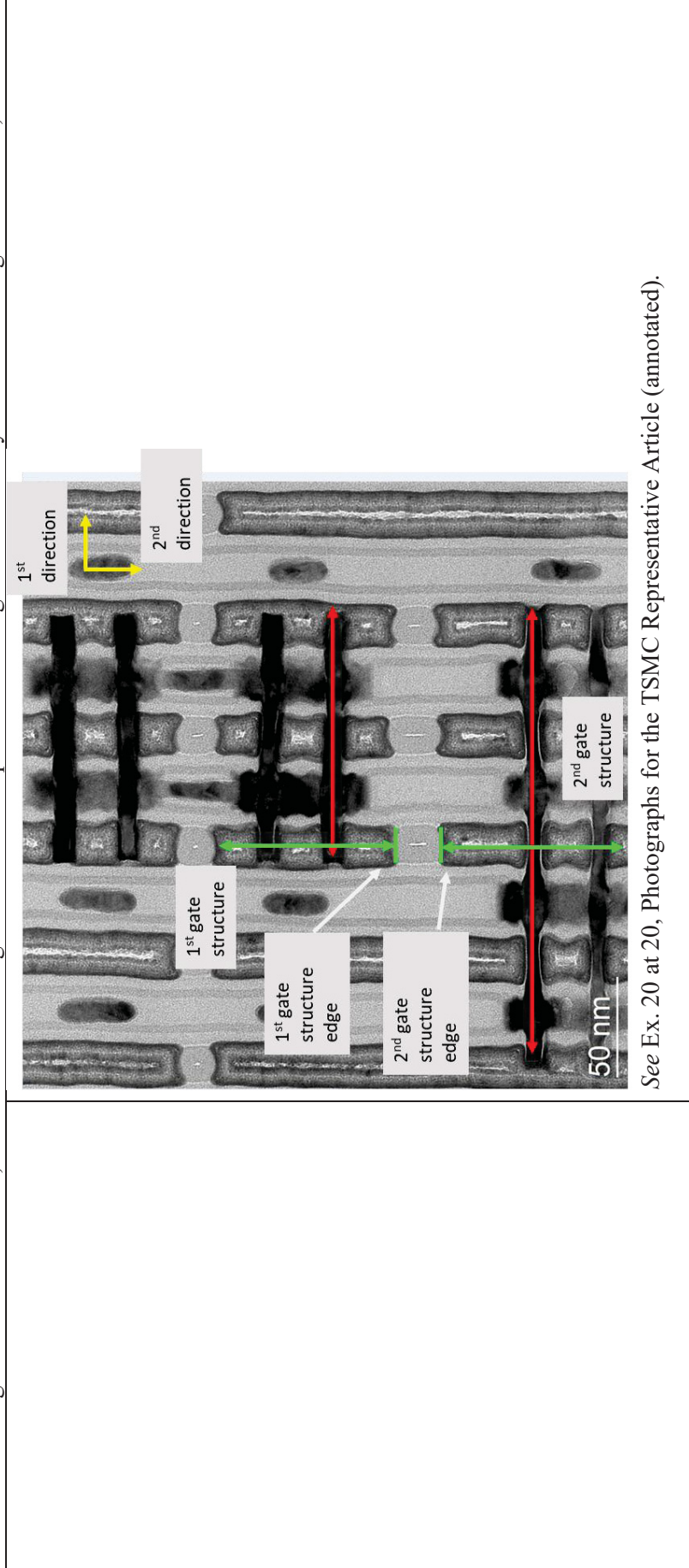
For example, the Qualcomm SoC includes a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction.



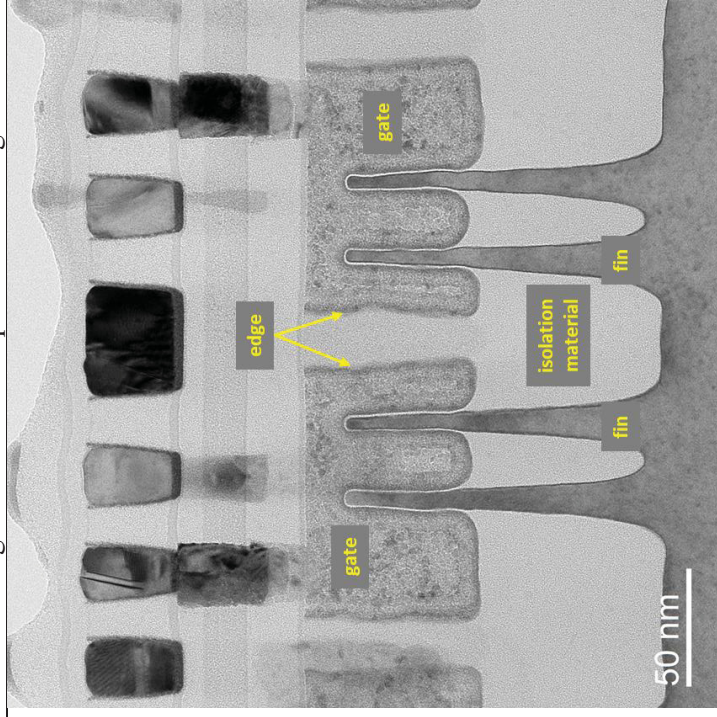
See Ex. 20 at 20, Photographs for the TSMC Representative Article (annotated).

26(e). a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;

“a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;”



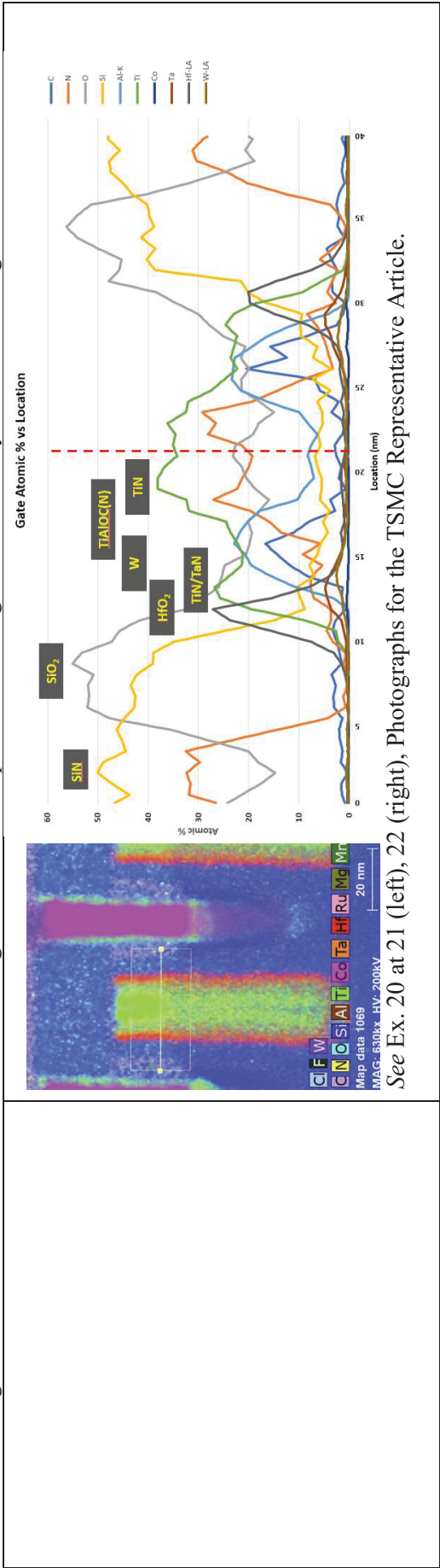
“a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;”



See Ex. 20 at 13, Photographs for the TSMC Representative Article (annotated).

The second gate structure comprises a second gate dielectric layer and a second gate electrode. For example, the transistor includes an HfO_2 gate dielectric with $\text{TiN}/\text{TaN}/\text{W}/\text{TiAlOC}(\text{N})/\text{TiN}$ work function and fill materials as the gate electrode.

“a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;”



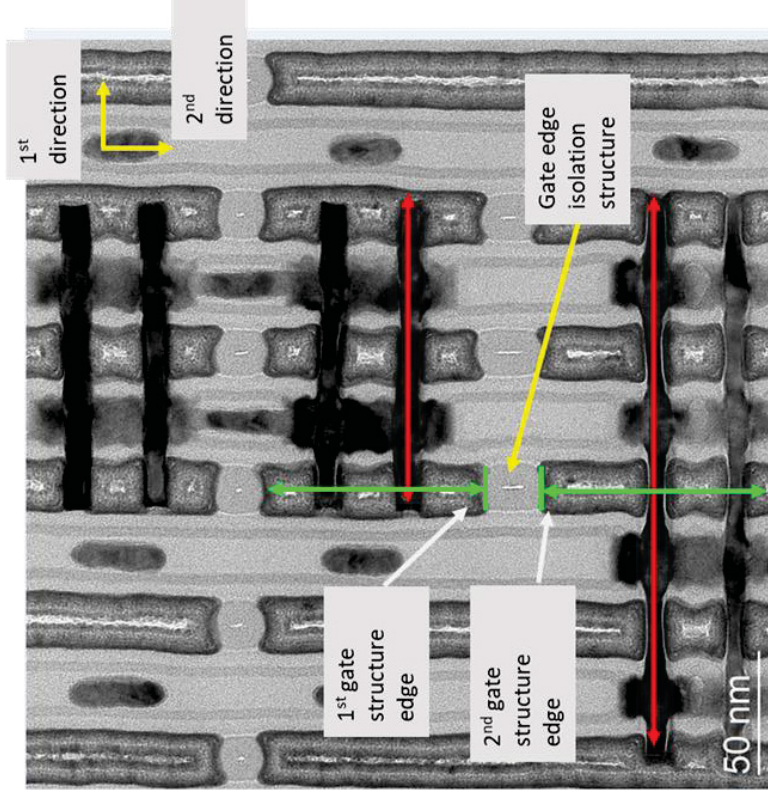
See Ex. 20 at 21 (left), 22 (right), Photographs for the TSMC Representative Article.

“a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and”

26(f). a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and

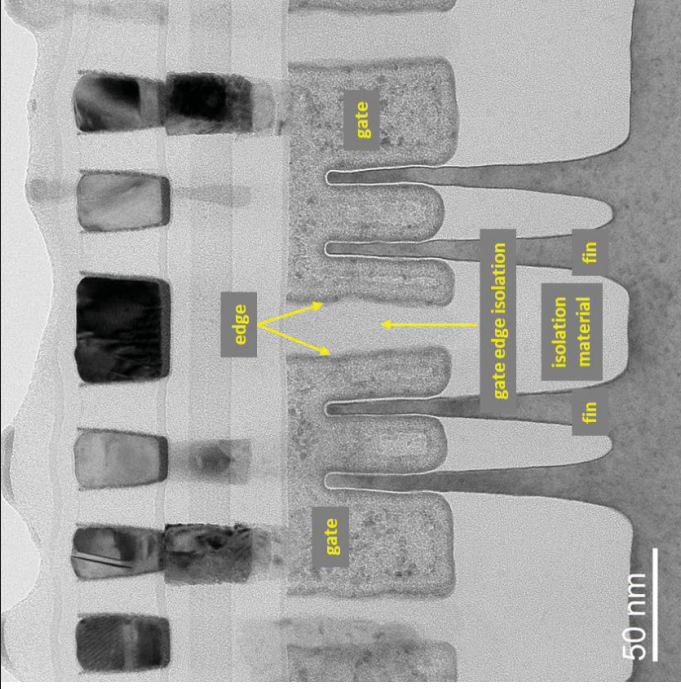
The Samsung/TSMC Product includes a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material.

For example, the Qualcomm SoC includes a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction. The gate edge isolation structure is over the isolation material.



See Ex. 20 at 20, Photographs for the TSMC Representative Article (annotated).

“a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and”



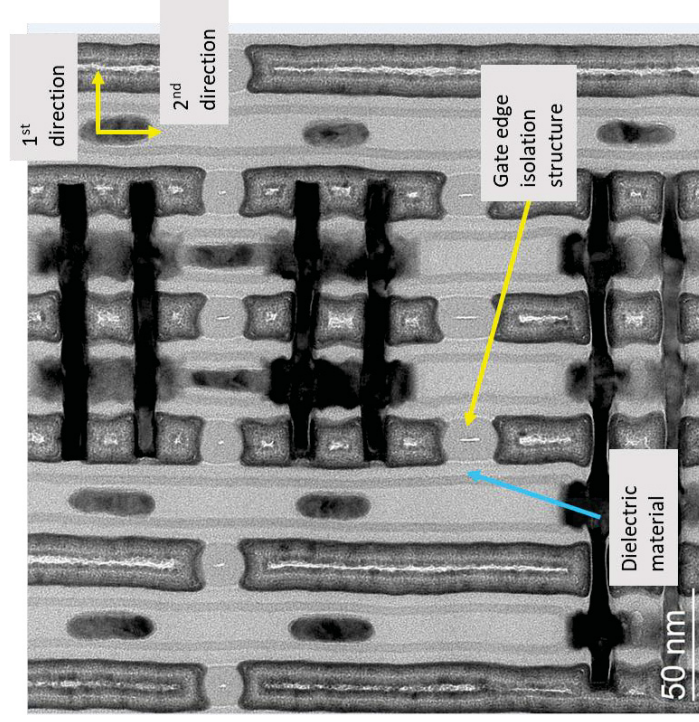
See Ex. 20 at 13, Photographs for the TSMC Representative Article (annotated).

“a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.”

26(g). a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

The Samsung/TSMC Product includes a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.

For example, the Qualcomm SoC includes a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.



See Ex. 20 at 13, Photographs for the TSMC Representative Article (annotated).