

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Milton Clair Webb, et al.
U.S. Patent No.: 10,319,812 Attorney Docket No.: 39843-0152IP2
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Appl. Serial No.: 15/789,315
Filing Date: October 20, 2017
Title: SELF-ALIGNED GATE EDGE AND LOCAL INTERCONNECT
AND METHOD TO FABRICATE SAME

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**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 10,319,812 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

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EXHIBITS

SAMSUNG-1001	U.S. Patent No. 10,319,812 to Webb, et al. (“the ’812 Patent”)
SAMSUNG-1002	Excerpts from the Prosecution History of the ’812 Patent (“the Prosecution History”)
SAMSUNG-1003	Declaration of David Kuan-Yu Liu
SAMSUNG-1004	U.S. Patent Pub. No. 2015/0054078 to Xie (“Xie”)
SAMSUNG-1005	U.S. Patent No. 9,397,217 to Tseng (“Tseng”)
SAMSUNG-1006	U.S. Patent Pub. No. 2012/0086055 to Anderson (“Anderson”)
SAMSUNG-1007	U.S. Patent No. 9,041,125 to Lin (“Lin”)
SAMSUNG-1008	U.S. Patent Pub. No. 2013/0026572 to Kawa (“Kawa”)
SAMSUNG-1009	U.S. Patent Pub. No. 2007/0080380 to Chang (“Chang”)
SAMSUNG-1010	U.S. Patent No. 9,324,790 to Akarvardar (“Akarvardar”)
SAMSUNG-1011	U.S. Patent No. 8,994,116 to Gan (“Gan”)
SAMSUNG-1012	U.S. Patent No. 11,037,923 to Bohr (“Bohr”)
SAMSUNG-1013	U.S. Patent No. 7,898,037 to Chuang (“Chuang”)
SAMSUNG-1014	U.S. Patent No. 9,166,053 to Kuo (“Kuo”)
SAMSUNG-1015	U.S. Patent Pub. No. 2013/0164924 to Shieh (“Shieh”)
SAMSUNG-1016	Reserved
SAMSUNG-1017	U.S. Patent No. 9,196,613 to Basker (“Basker”)
SAMSUNG-1018-1024	Reserved
SAMSUNG-1025	U.S. Patent No. 9,281,378 to Ching (“Ching”)

SAMSUNG-1026	U.S. Patent No. 6,894,357 to Guo (“Guo”)
SAMSUNG-1027	U.S. Patent No. 7,586,159 to Lee (“Lee”)
SAMSUNG-1028	U.S. Patent Pub. No. 2006/0220090 to Metz (“Metz”)
SAMSUNG-1029	U.S. Patent Pub. No. 2015/0200275 to Zhu (“Zhu”)
SAMSUNG-1030	U.S. Patent No. 8,637,931 to Basker (“Basker-931”)
SAMSUNG-1031	U.S. Patent No. 8,697,515 to Yin (“Yin”)
SAMSUNG-1032	Reserved
SAMSUNG-1033	Reserved
SAMSUNG-1034	U.S. Patent No. 7,632,745 to Chen (“Chen”)
SAMSUNG-1035	U.S. Patent No. 9,246,003 to Cheng (“Cheng”)
SAMSUNG-1036	U.S. Patent No. 7,592,675 to Liaw (“Liaw”)
SAMSUNG-1037	U.S. Patent No. 9,214,529 to Chang (“Chang-529”)
SAMSUNG-1038	U.S. Patent Pub. No. 2011/0031552 to Iwamatsu (“Iwamatsu”)
SAMSUNG-1039	U.S. Patent No. 9,461,143 to Pethe (“Pethe”)
SAMSUNG-1040	U.S. Patent No. 8,901,665 to Kelly (“Kelly”)
SAMSUNG-1041	U.S. Patent No. 6,720,619 to Chen (“Chen-619”)
SAMSUNG-1042-1049	Reserved
SAMSUNG-1050	<i>Daedalus Prime LLC v. Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. and Taiwan Semiconductor Manufacturing Company Limited and TSMC North America, Complaint, ITC Inv. No. 337-TA-1336 (ITC) (“ITC Complaint”)</i>
SAMSUNG-1051-1053	Reserved
SAMSUNG-1054	<i>Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al., 2:22-cv-00352, E.D. Tex.</i>

CLAIM LISTING

Limitation	Claim Language
[21pre]	A method of fabricating an integrated circuit structure, the method comprising:
[21a]	forming a first fin comprising silicon, the first fin having a longest dimension along a first direction;
[21b]	forming a second fin comprising silicon, the second fin having a longest dimension along the first direction;
[21c]	forming an isolation material between the first fin and the second fin;
[21d]	forming a first gate structure over the first fin, the first gate structure having a longest dimension along a second direction, the second direction orthogonal to the first direction, wherein the first gate structure comprises a first gate dielectric layer and a first gate electrode;
[21e]	forming a second gate structure over the second fin, the second gate structure having a longest dimension along the second direction, the second gate structure discontinuous with the first gate structure along the second direction, and the second gate structure having an edge facing an edge of the first gate structure along the second direction, wherein the second gate structure comprises a second gate dielectric layer and a second gate electrode;
[21f]	forming a gate edge isolation structure between and in contact with the edge of the first gate structure and the edge of the second gate structure along the second direction, the gate edge isolation structure over the isolation material; and
[21g]	forming a dielectric material laterally adjacent to the first and second gate structures along the first direction, the dielectric material laterally adjacent to the gate edge isolation structure along the first direction, and the dielectric material discrete from the gate edge isolation structure.
[22]	The method of claim 21, wherein the gate edge isolation structure comprises silicon and nitrogen.
[23]	The method of claim 21, wherein the dielectric material is in contact with the gate edge isolation structure.

Limitation	Claim Language
[24]	The method of claim 21, wherein the gate edge isolation structure is in contact with a gate dielectric layer of the first gate structure and with a gate dielectric layer of the second gate structure.
[26]	The method of claim 21, wherein the gate dielectric layer of the first gate structure comprises a high-k dielectric material, and wherein the gate dielectric layer of the second gate structure comprises a high-k dielectric material.

I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner”) petitions for IPR of claims 21-24 and 26 (“Challenged Claims”) of U.S. Patent No. 10,319,812 (“the ’812 Patent”).

II. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’812 Patent is available for IPR. Petitioner is not barred or estopped from requesting this review.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the below grounds.
SAMSUNG-1003, ¶¶1-207.

Ground	Claims	Basis
1	21-24, 26	§103: Chang, Tseng
2	21-24, 26	§103: Akarvardar, Xie
3	21-24, 26	§103: Akarvardar, Xie, Tseng

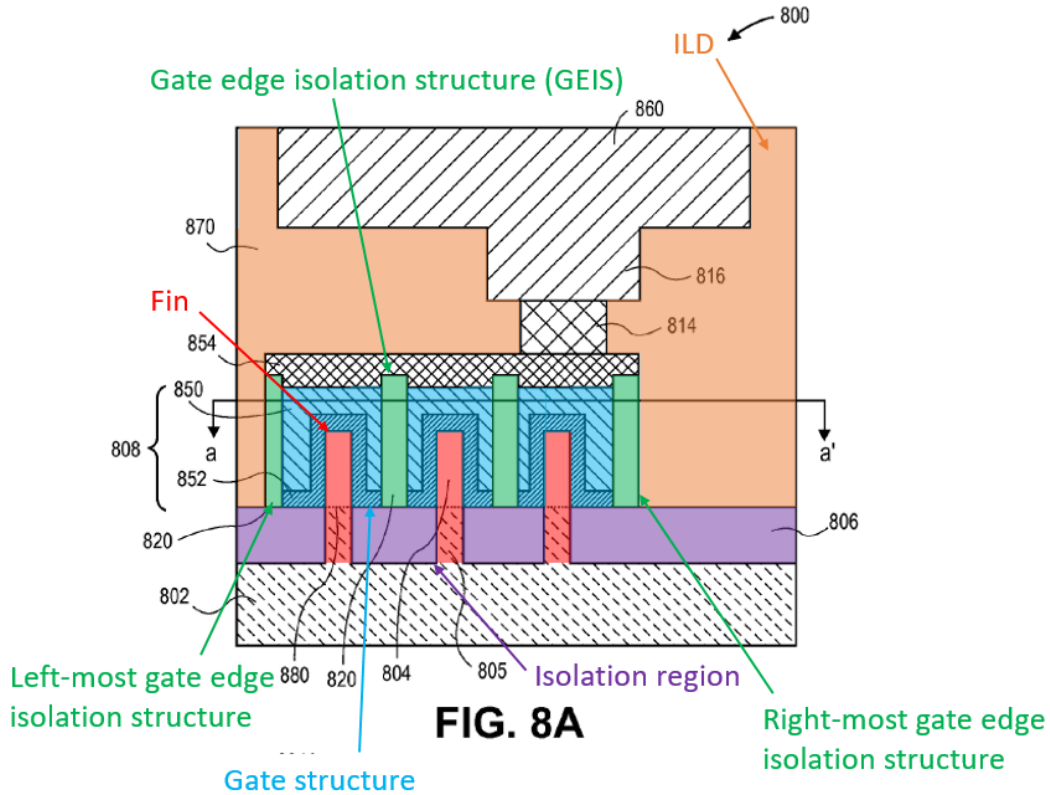
Each reference pre-dates December 19, 2013 (“Critical Date”), which is the earliest filed application from which the ’812 Patent claims priority. Petitioner does not take a position as to whether the ’812 Patent is entitled to the claimed priority date, but has applied references that pre-date the Critical Date and qualify as prior art, as shown below.

Reference	Date	Section
Chang	10/12/2005 (filed), 4/12/2007 (published)	§§102(a)(1), 102(a)(2)
Tseng	12/28/2012 (filed)	§102(a)(2)
Akarvardar	11/19/2013 (filed)	§102(a)(2)
Xie	8/21/2013 (filed)	§102(a)(2)

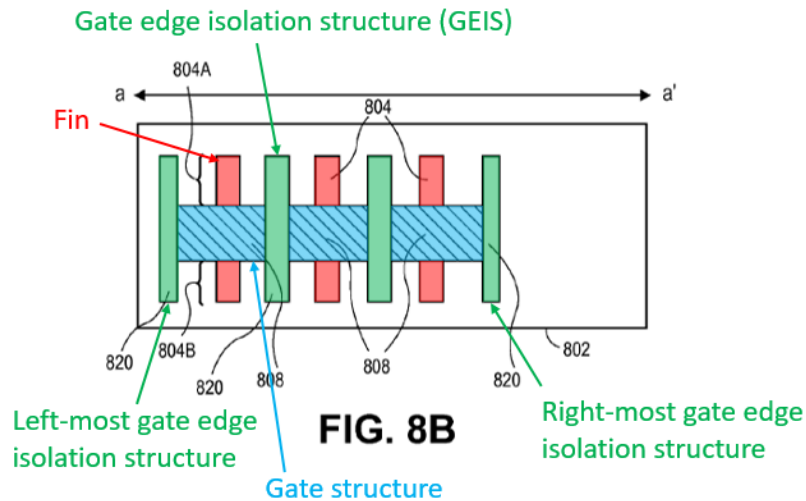
III. SUMMARY OF THE '812 PATENT

A. Brief Description

The '812 Patent describes “[s]elf-aligned gate edge and local interconnect structures.” SAMSUNG-1001, Abstract. An example of such a structure— is shown in cross-section and plan view in FIGS. 8A-8B, *infra. Id.*, 9:27-30; SAMSUNG-1003, ¶21.



Excerpt from '812 Patent, FIG. 8A (annotated)



Excerpt from '812 Patent, FIG. 8B (annotated)

This device includes “non-planar active regions (e.g., a fin structure[]
including protruding fin portion 804 and sub-fin region 805) formed from substrate

802, and within isolation region 806.” SAMSUNG-1001, 9:34-37; *see* claim 21.

The **fin structures** are highlighted in red and the **isolation region** in purple. “**Gate structures** 808,” blue, are “disposed over the **protruding portions** 804 of the non-planar active regions as well as over a portion of the **isolation region** 806.”

SAMSUNG-1001, 9:37-39; *see* claim 21. “Gate structures 808 are separated by self-aligned **gate edge isolation structures** 820,” green. *Id.*, 9:43-44; *see* claim 21.

SAMSUNG-1003, ¶22.

Interconnects and contacts are “disposed in **inter-layer dielectric stacks or layers** 870,” orange. SAMSUNG-1001, 9:45-49. As shown in FIG. 8A, the **inter-layer dielectric (ILD)** covers the **gate structures** and **gate edge isolation structures**, filling the space next to the exposed sidewalls of the right-most and left-most **gate edge isolation structures**.¹ SAMSUNG-1003, ¶23.

¹ FIG. 8B does not label the ILD. However, since FIG. 8B illustrates a top view through the a-a’ cut in FIG. 8A, a POSITA would have understood that the ILD is present at least next to the left-most and right-most gate edge isolation structures of FIG. 8B. SAMSUNG-1003, ¶23.

B. Spatial Relationships of Elements of the Challenged Claims²

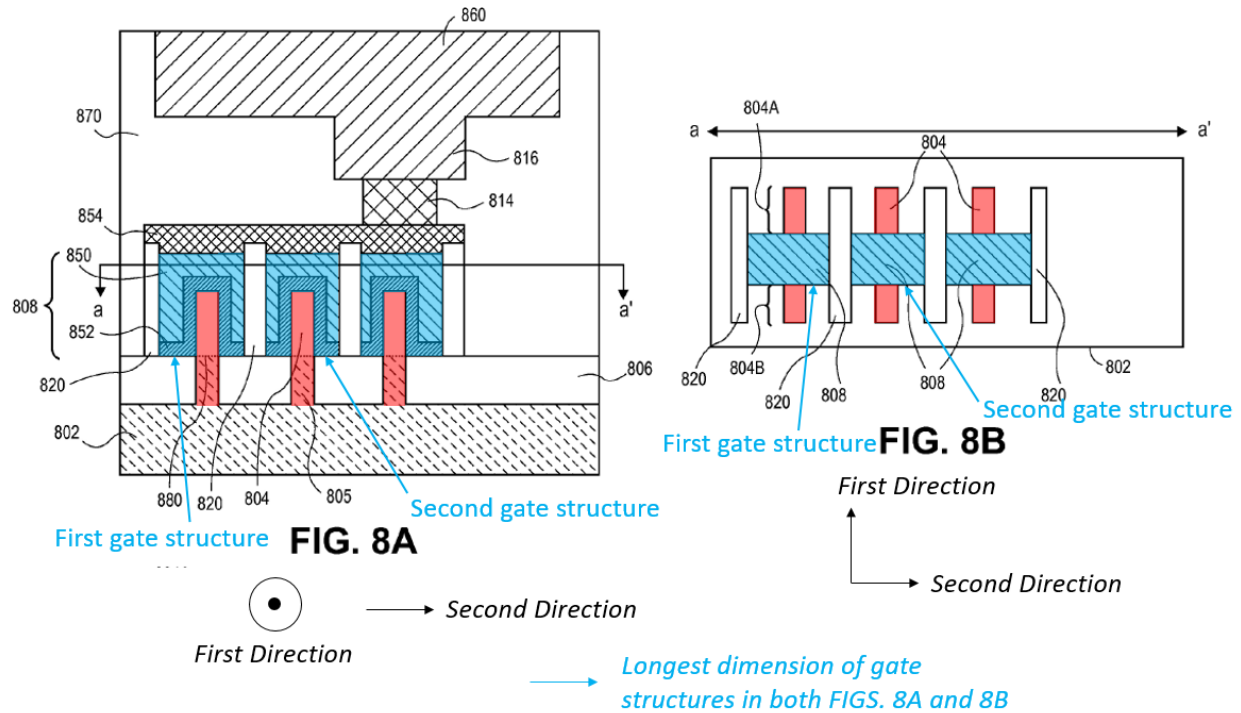
The Challenged Claims recite spatial relationships between features of an integrated circuit structure. The following paragraphs provide an overview of some of these features, with reference to FIGS. 8A and 8B, excerpted *infra*. SAMSUNG-1003, ¶¶24-30.

The Challenged Claims recite that the fins (red) have “a longest dimension *along a first direction*,” illustrated *infra*. SAMSUNG-1001, claim 21. In doing so, the claims indicate the orientation of the fins, thus defining an orientation along the first direction. Based on the figures and read in light of the specification, a POSITA would have understood that the longest dimension of the fins extends from top to bottom in the top view (FIG. 8B), and correspondingly into the page in the cross-sectional view (FIG. 8A): this direction is the first direction. *See id.*, Abstract, 13:47-49, 14:4-8; SAMSUNG-1003, ¶25.

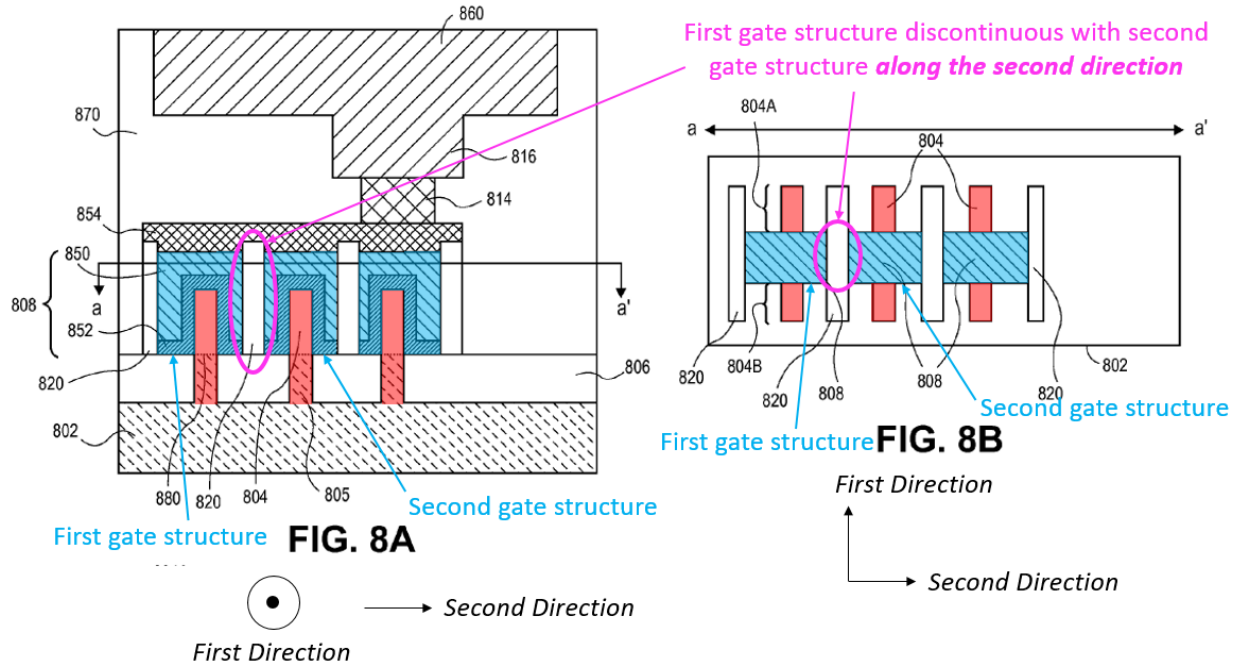
² This discussion is incorporated by reference into any portion of Grounds 1-3 where these terms are referenced.



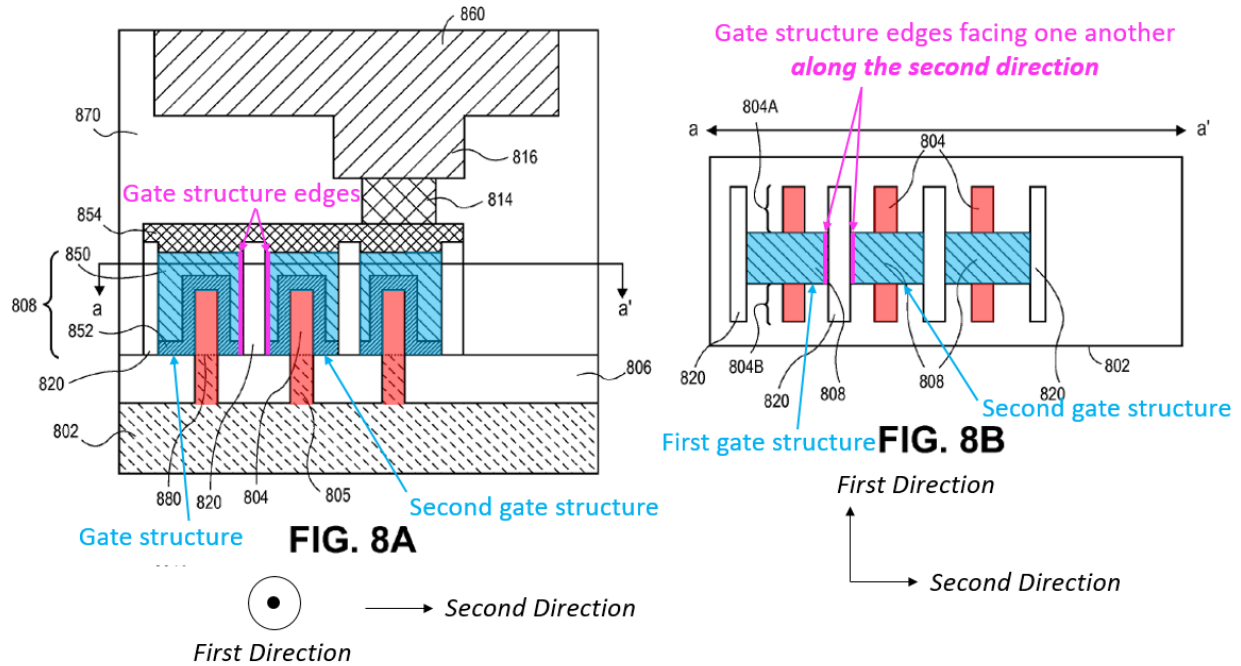
The Challenged Claims also recite that the gate structures have “a longest dimension *along a second direction* ... orthogonal to the first direction,” illustrated *infra*. SAMSUNG-1001, claim 21. The direction orthogonal to the length of the fins is the left-to-right direction in FIGS. 8A and 8B. A POSITA would have understood that this direction is the second direction, *e.g.*, given that the gate structure dimensions that appear to be longest are along this direction. *See id.*, Abstract, 13:49-52, 14:8-10; SAMSUNG-1003, ¶26.



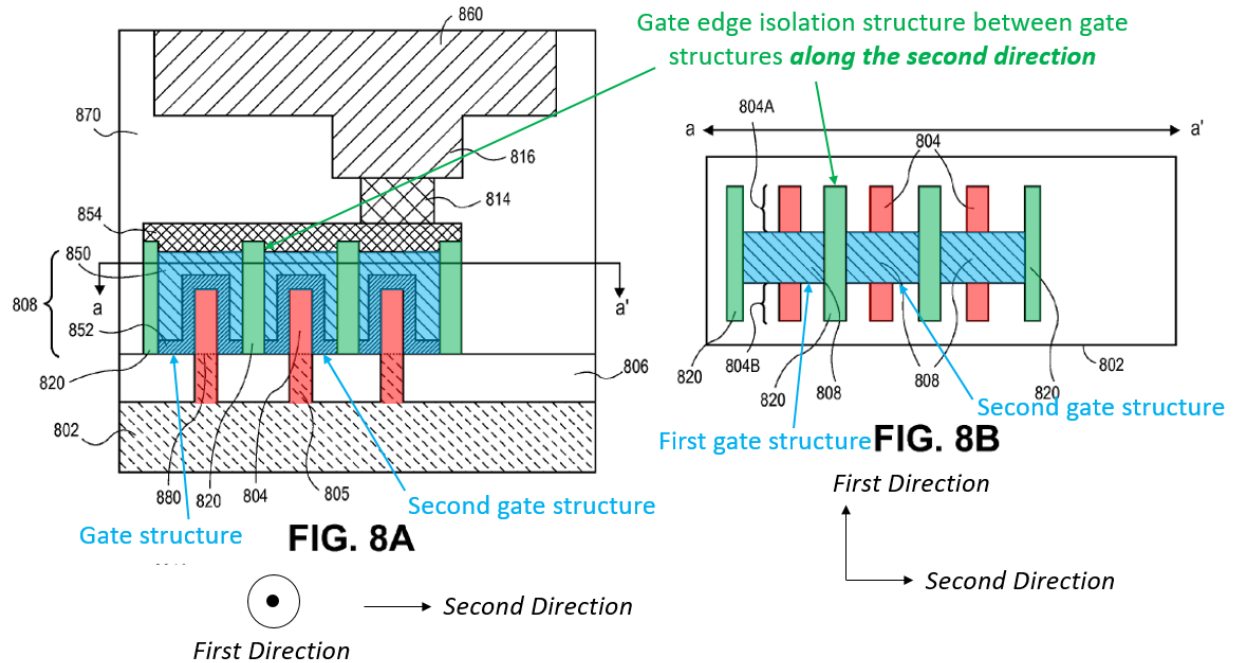
The Challenged Claims recite that a “second gate structure [is] discontinuous with [a] first gate structure *along the second direction*,” illustrated *infra*. SAMSUNG-1001, claim 21. This is revealed when viewing the structure starting from the first gate structure and *moving along the second direction* (left-to-right in both figures): a discontinuity exists (occupied by the gate edge isolation structure, discussed *infra*) before reaching the second gate structure. SAMSUNG-1003, ¶27.



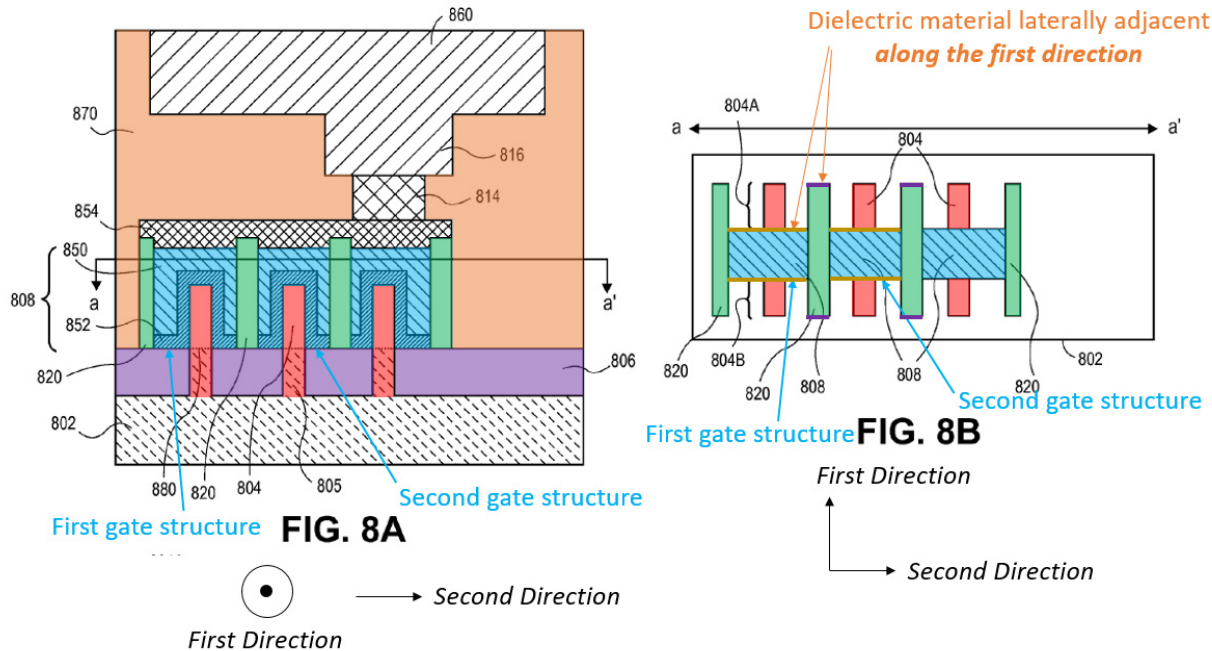
Similarly, the Challenged Claims recite that “an edge” of the second gate structure “fac[es] an edge of the first gate structure *along the second direction*,” illustrated *supra*. SAMSUNG-1001, claim 21. This too would have been understood by a POSITA when viewing the structure starting from the edge of the first gate structure (outlined in pink) and *moving along the second direction* to encounter the edge of the second gate structure (also in pink). SAMSUNG-1003, ¶28.



The gate edge isolation structure of the Challenged Claims is “between and in contact with the edge of the first gate structure and the edge of the second gate structure *along the second direction*,” illustrated *infra*. SAMSUNG-1001, claim 21. Starting from the edge (pink) of the first gate structure (blue) and *moving along the second direction*, one reaches first the gate edge isolation structure (green) and then the edge (pink) of the second gate structure (blue). SAMSUNG-1003, ¶29.



The Challenged Claims also recite that the “dielectric material [is] laterally adjacent to the first and second gate structures *along the first direction*” and “laterally adjacent to the gate edge isolation structure ... *along the first direction.*” SAMSUNG-1001, claim 21. For the purposes of this proceeding and without concession, Petitioner interprets these limitations consistent with the use of the phrase “along the second direction” (discussed *supra*). For instance, a dielectric material would be laterally adjacent to the gate structures (blue) *along the first direction* if it were at the sidewalls of the gate structures (outlined in brown in FIG. 8B, *infra*) and would be laterally adjacent to the gate edge isolation structure (green) *along the first direction* if it were at the short ends of the gate edge isolation structure (outlined in purple in FIG. 8B). SAMSUNG-1003, ¶30.



C. Prosecution History

The '812 Patent issued from U.S. Patent App. No. 15/789,315. A single office action was issued, advancing a double patenting rejection of claims 1-10 and allowing claims 11-30. SAMSUNG-1002, 287-292. The applicant filed a terminal disclaimer and a Notice of Allowance followed, providing no reasons for allowance. *Id.*, 128-132.

D. Level of Ordinary Skill in the Art

A person of ordinary skill in the art relating to the subject matter of the '812 Patent as of the Critical Date (a "POSITA") would have had a Master's degree in electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing. SAMSUNG-1003, ¶¶19-20.

E. Claim Construction

Based on the prior art's description of the claimed elements being similar to that of the '812 Patent specification, no formal claim constructions are necessary in this proceeding because "claim terms need only be construed to the extent necessary to resolve the controversy." *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011).

Furthermore, Petitioner is not conceding that each challenged feature satisfies all statutory requirements such as 35 U.S.C. § 112. As this is an IPR petition, Petitioner is pursuing prior art-based grounds. Petitioner is not waiving any arguments concerning other grounds or claim scope.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. [GROUND 1] – CLAIMS 21-24 AND 26 ARE OBVIOUS OVER CHANG AND TSENG

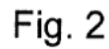
The sections below provide a brief introduction to the Chang-Tseng combination.³

1. Chang describes tri-gate transistors with self-aligned isolation regions and gates

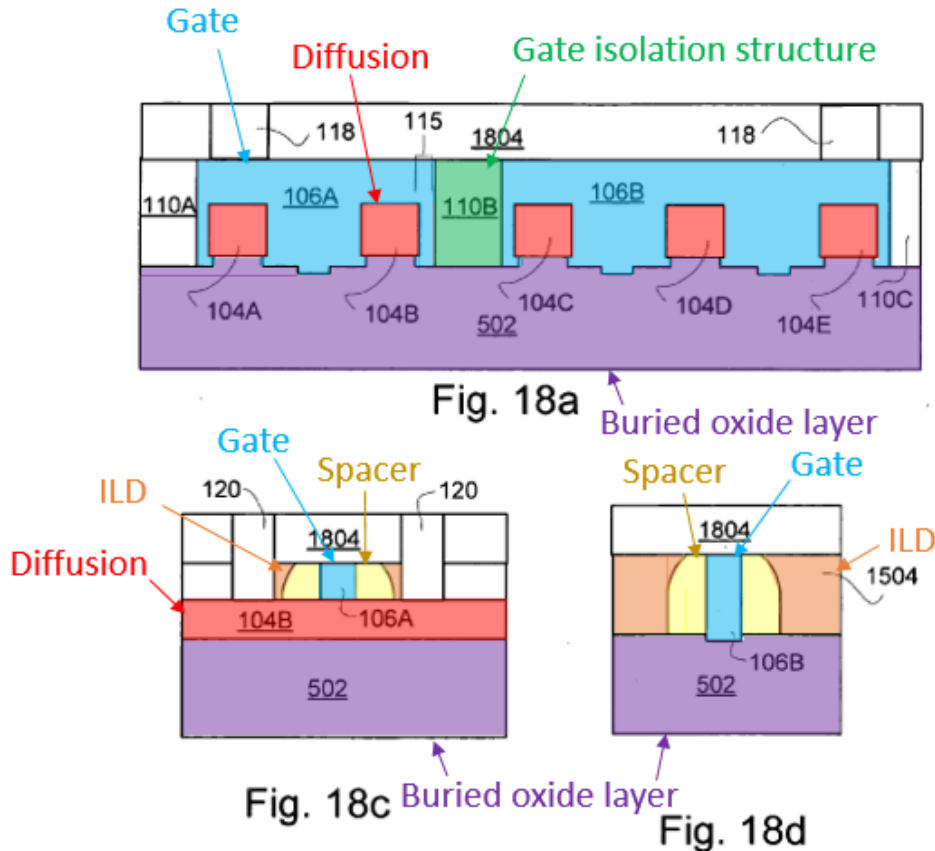
Chang describes "forming self-aligned gates on transistors," *e.g.*, for "a tri-gate transistor." SAMSUNG-1009, [0035], [0046]. FIG. 2, *infra*, is "a top view that illustrates a portion of a circuit 100 that includes transistors with end gaps of

³ Petitioner incorporates this discussion into Ground 1.

also *infra*. See *id.*, [0056]; SAMSUNG-1003, ¶31.



Excerpt from Chang, FIG. 2 top-view (annotated)



Excerpt from Chang, FIGS. 18a, 18c-18d cross-sectional views (annotated)

Chang's diffusions are on "a buried oxide layer 502," purple, of "a silicon-on-insulator (SOI) substrate." SAMSUNG-1009, [0040]; *see* SAMSUNG-1009, [0041], FIGS. 5-6, 10; SAMSUNG-1003, ¶32.

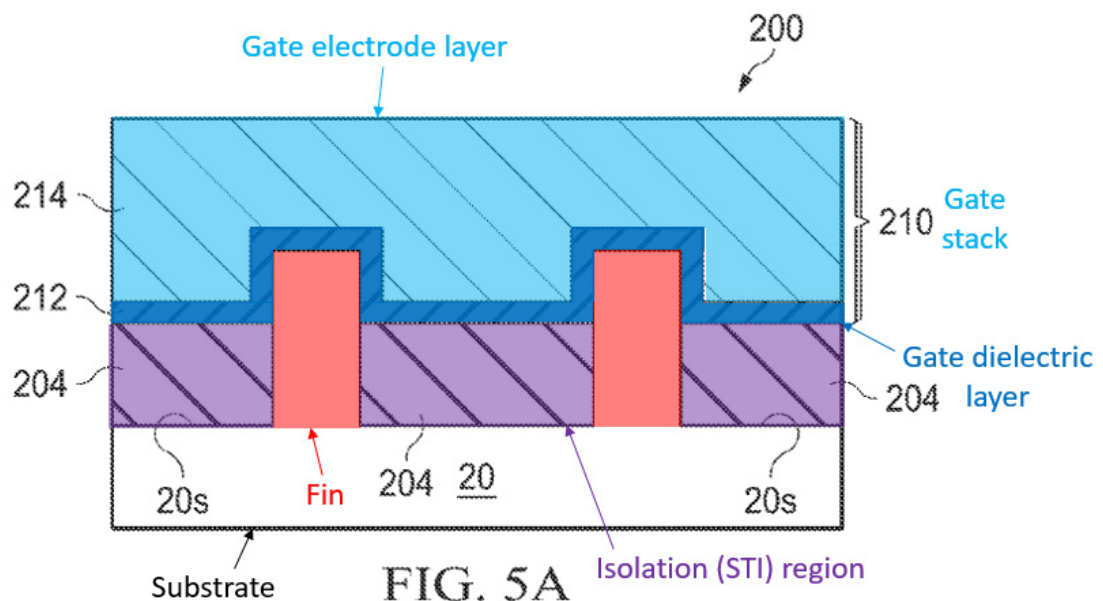
"[G]ate isolation structures 110," green, are "self-aligned to the diffusions 104," and "gates 106," blue, are "self-aligned to the isolation structures 110." SAMSUNG-1009, [0036]; *see* [0043]-[0044]; SAMSUNG-1003, ¶¶33-34. The gate structures can be "made by a replacement gate process" in which "a final

metal gate and gate dielectric replace” a place-holder gate material. SAMSUNG-1009, [0047], [0050]; SAMSUNG-1003, ¶35.

Chang’s circuit includes “spacers 108,” yellow, “on either side of the gates 106” and the isolation structures 110. SAMSUNG-1009, [0037]. A “layer 1504 of interlayer dielectric 1502,” orange, is disposed next to the spacers. *Id.*, [0051]; SAMSUNG-1003, ¶36.

2. Tseng describes FinFET devices having fins isolated by STI regions

Tseng describes a FinFET semiconductor device that includes “a fin structure 202 (comprising a first fin 202a of the substrate and a second fin 202b of the substrate 20),” red in FIG. 5A, *infra*. SAMSUNG-1005, 3:4-9, 3:24-25, 3:60-65; *see* FIG. 2, FIG. 3A; SAMSUNG-1003, ¶37.



Excerpt from Tseng, FIG. 5A (annotated)

Trenches between the fins are “filled with a dielectric material to form the isolation regions 204,” *e.g.*, “shallow trench isolation (STI) regions.” *Id.*, 4:25-32; *see* 3:9-10, FIGS. 2, 5A. A gate stack 210, blue, including a “gate electrode layer 214 and [] gate dielectric layer 212” is “sequentially deposited over the substrate.” *Id.*, 3:4-12, 5:5-13; *see* FIG. 2, 5A. The gate dielectric layer 212, outlined in dark blue, is a “high dielectric constant (high-k) dielectric,” and the gate electrode layer 214, light blue, is a metal. *Id.*, 5:14-42; SAMSUNG-1003, ¶¶38, 195.

3. The Chang-Tseng combination

In the Chang-Tseng combination, a FinFET structure includes elongated diffusions (red in Chang’s FIG. 6, also *infra*) on an SOI substrate. *See* SAMSUNG-1009, [0040]-[0041]. The diffusions are formed by “removing portions of [a] hardmask layer 508, [a] pad oxide layer 506, and [a] semiconductor layer,” such that the diffusions are isolated from each other “by the buried oxide layer 502” of the SOI substrate. SAMSUNG-1009, [0041]; SAMSUNG-1003, ¶40.

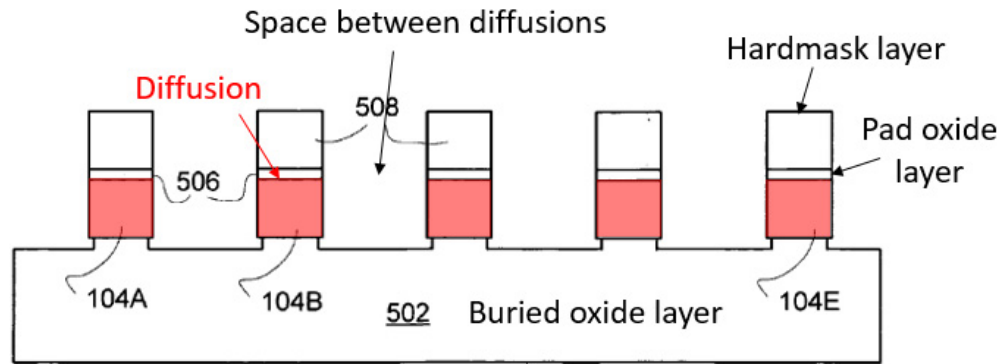


Fig. 6

Excerpt from Chang, FIG. 6 (annotated)

Based on Tseng, the spaces between diffusions (*e.g.*, the spaces shown in Chang's FIG. 6) are "filled with a dielectric material to form isolation regions" such as "shallow trench isolation (STI) regions," purple in the composite figure *infra*. SAMSUNG-1005, 4:25-32; *see* FIGS. 2 and 5A; SAMSUNG-1003, ¶41.

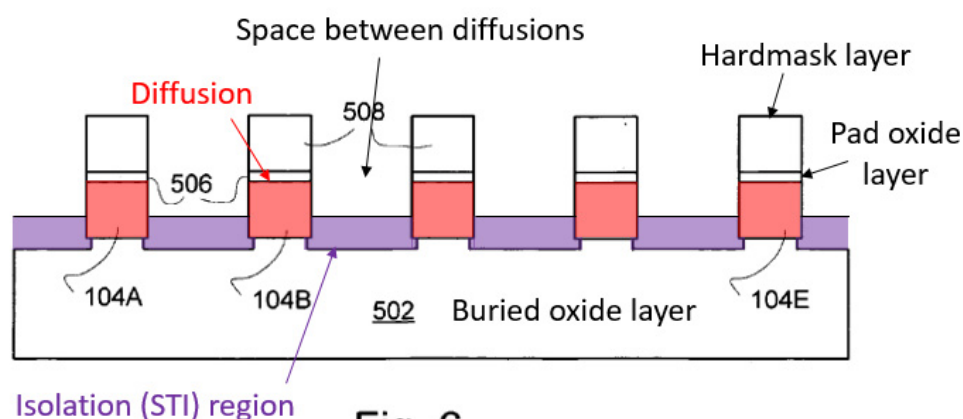


Fig. 6

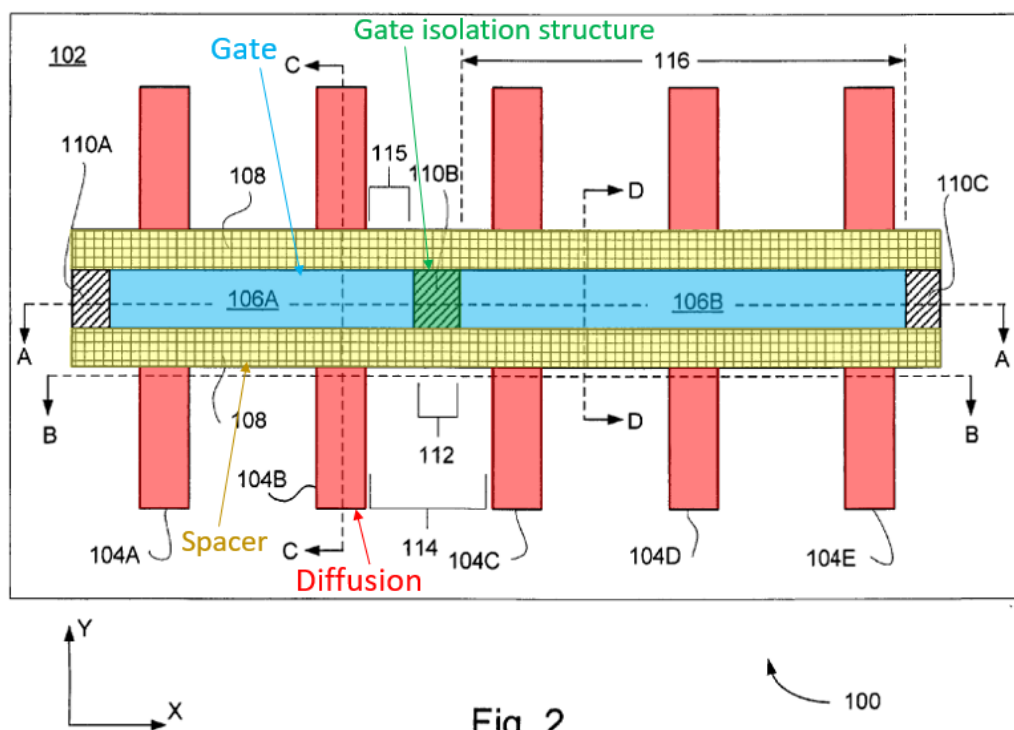
Chang-Tseng composite figure⁴

After formation of the STI regions, “gate isolation structures,” green, are “self-aligned” to the diffusions, *e.g.*, using a self-alignment process described by Chang. SAMSUNG-1009, [0036]; *see* [0042]-[0044], FIGS. 7-8; SAMSUNG-1003, ¶42. To form the isolation structures, a “layer of an insulating material 802” is deposited in the spaces between diffusions, *e.g.*, onto the dielectric material of the STI regions. SAMSUNG-1009, [0042]-[0043], FIGS. 7-8; *see* SAMSUNG-1005, 4:25-32, FIGS. 2 and 5A; SAMSUNG-1003, ¶42. This insulating material is

⁴ This figure, as well as other composite figures herein, is just one example combination that a POSITA would have found obvious, and is provided for illustrative purposes only. Other, similar example configurations also would have been obvious and would render the challenged claims obvious for similar reasons as those discussed herein. SAMSUNG-1003, ¶39.

“used as the insulating isolation structures 110.” SAMSUNG-1009, [0044];

SAMSUNG-1003, ¶42.



Chang-Tseng top-view composite figure

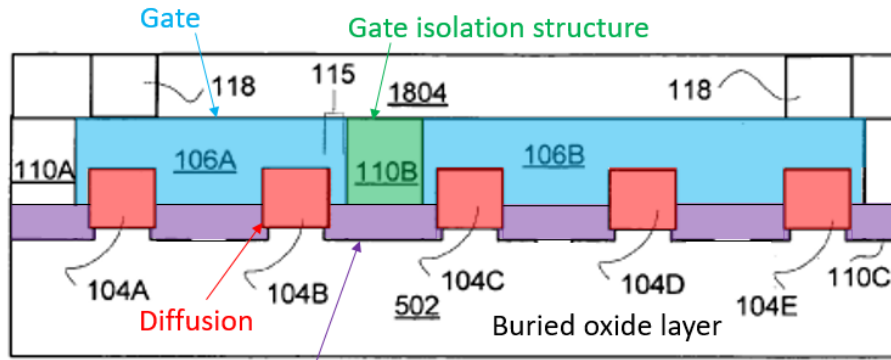


Fig. 18a

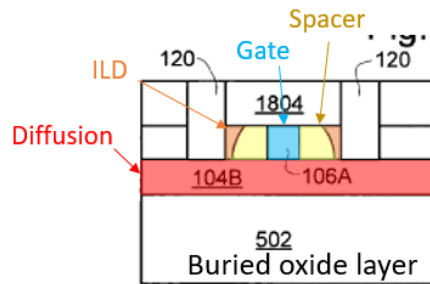


Fig. 18c

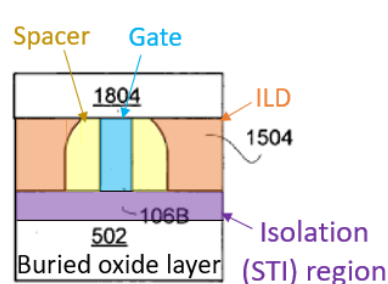


Fig. 18d

Chang-Tseng cross-sectional composite figures

“[G]ates 106,” blue, including a gate dielectric and a metal gate, are formed “self-aligned to the isolation structures 110.” SAMSUNG-1009, [0036]; *see* [0047], [0050], FIG. 11, FIGS. 18a-18d; SAMSUNG-1003, ¶44. Notably, this gate structure is consistent with the structure of Tseng’s gate stack. *See* SAMSUNG-1005, 3:4-12, 5:5-13, FIGS. 2 and 5A; SAMSUNG-1003, ¶43. Spacers 108, yellow, are disposed “on either side of the gates 106,” and a “layer 1504 of interlayer dielectric,” orange, is disposed next to the spacers. SAMSUNG-1009, [0037], [0051]; SAMSUNG-1003, ¶44.

4. Reasons to combine Chang and Tseng

A POSITA would have been motivated to incorporate STI around the base of the Chang-Tseng diffusions for at least the following reasons. SAMSUNG-1003, ¶¶45-49.

First, a POSITA would have been motivated to incorporate STI regions to isolate the fins from one another, thereby improving electrical performance of the device, *e.g.*, by reducing leakage current between neighboring fins. *See* SAMSUNG-1005, 4:25-27; SAMSUNG-1010, 1:43-45; SAMSUNG-1031, 5:16-18; SAMSUNG-1003, ¶46.

Second, a POSITA would have been motivated to integrate STI regions specifically over Chang's buried oxide layer because STI used in conjunction with silicon-on-insulator (SOI) substrates was a conventional approach providing benefits of both SOI and STI. *See* SAMSUNG-1034, 2:24-36 ("The SOI substrate may allow a transistor to operate at a higher switching speed or with a lower power consumption when compared to a bulk semiconductor substrate. ... [S]hallow trench isolation (STI) that extends from a surface of the SOI substrate ... may provide an electrical isolation around a periphery of the transistor primarily in a horizontal (or lateral) direction"); SAMSUNG-1035, 1:22-32 ("FinFET structures may be formed on a semiconductor-on-insulator (SOI) substrate, because of the low source/drain diffusion, low substrate capacitance, and ease of electrical

isolation by shallow trench isolation structures”); SAMSUNG-1041, 3:46-56 (describing a device having SOI and STI isolation that “maintains [] manufacturing simplicity, and benefits from FD-SOI’s and FinFET’s immunity to floating-body effects”), 6:6-46; SAMSUNG-1036, 3:55-59; SAMSUNG-1037, 3:16-18; SAMSUNG-1038, [0074]; SAMSUNG-1003, ¶47.

Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, STI in an integrated circuit device) to a known structure (*e.g.*, a FinFET integrated circuit structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit having STI around the fins). SAMSUNG-1003, ¶48; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007) (a supposed invention that “simply arranges old elements with each performing the same function it had been known to perform” is obvious).

A POSITA would have expected success in incorporating STI regions around the fins because of the compatibility of Tseng’s process for forming the STI regions with the initial steps of Chang’s fabrication process. SAMSUNG-1003, ¶49. Both Chang and Tseng describe initial steps of forming fins, and a POSITA would have expected success in integrating an STI step after these similar fin formation steps, and prior to other steps of Chang’s process. *See* SAMSUNG-1009, [0039], [0041], FIG. 4, FIG. 6; SAMSUNG-1005, 2:11-14, 3:44-4:5, FIG. 2,

FIGS. 3A-3C; SAMSUNG-1003, ¶49. A POSITA also would have expected success given that the use of STI in integrated circuits, such as non-planar integrated circuits (*e.g.*, FinFET-based devices), was well-known. *See* SAMSUNG-1005, 4:25-27; SAMSUNG-1031, 5:16-18; SAMSUNG-1032, 1:50-53; SAMSUNG-1003, ¶49.

5. Analysis

(1) Claim 21

Limitation [21pre]

To the extent the preamble is deemed to be limiting, Chang-Tseng renders it obvious. *See* SAMSUNG-1009, Abstract, [0035], [0036]; SAMSUNG-1003, ¶50.

Limitations [21a] and [21b]

The Chang-Tseng combination includes **first and second fins**, *e.g.*, Chang's *diffusions 104*. SAMSUNG-1003, ¶51; *see* SAMSUNG-1009, [0036] (“a circuit 100 that includes transistors with end caps of gates 106 self-aligned to *diffusions 104*”), [0039], [0041]; claims 1, 5, 10, 14, 15, 18; FIGS. 2-18.

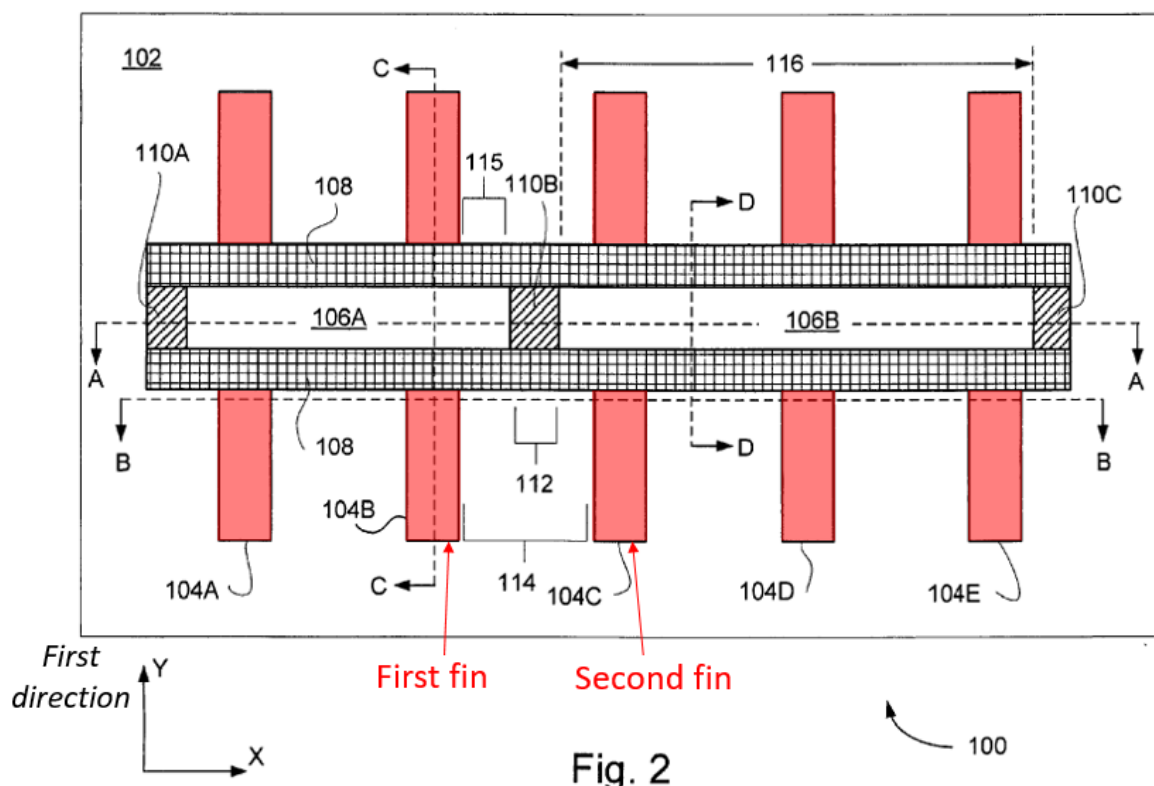


Fig. 2

Chang-Tseng top-view figure

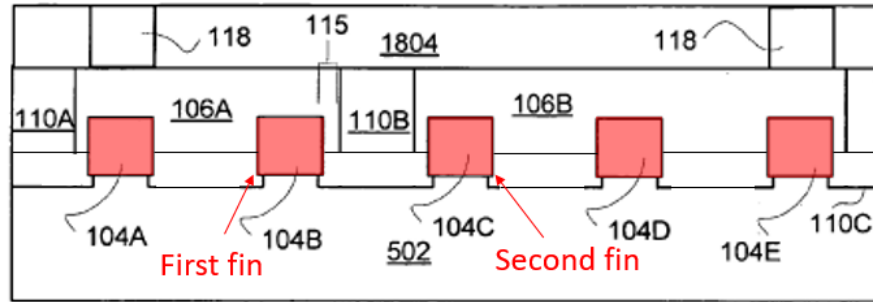


Fig. 18a

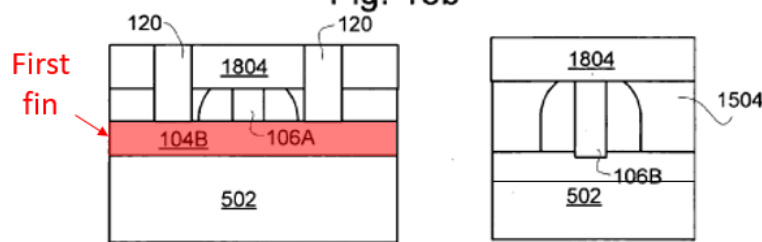


Fig. 18c

First direction

Fig. 18d

First direction

Chang-Tseng cross-sectional figures

In the combination, a POSITA would have understood that Chang's diffusions are **fin**s at least because they are elongated semiconductor structures disposed on the surface of a semiconductor substrate (*see* SAMSUNG-1009, [0041], FIG. 2, FIG. 6) and arranged such that a gate can surround a respective fin

on three sides (*see* SAMSUNG-1009, FIGS. 18a-18d).⁵ SAMSUNG-1003, ¶52; *see* SAMSUNG-1005, 1:17-24 (“A typical FinFET is fabricated with a thin vertical ‘fin’ (or fin structure) extending from a substrate formed by, for example, etching away a portion of a silicon layer of the substrate. ... A gate is provided over three sides (e.g., wrapping) the fin.”); SAMSUNG-1012, 1:24-27; SAMSUNG-1011, 1:21-28; SAMSUNG-1017, 1:28-34. To the extent Patent Owner interprets fins as requiring the elongated semiconductor structure to have flat (*e.g.*, not undercut) sides, Chang discloses that its diffusions have such a geometry: “the etching and/or cleaning process ... undercut the diffusions 104 to some extent, although in some other embodiments such undercutting may be absent.” SAMSUNG-1009, [0041]; SAMSUNG-1003, ¶53.

In the combination, each fin has **a longest dimension along a first direction**, marked in the figures. *See* SAMSUNG-1009, [0036] (“*the diffusions 104 have a major axis in the Y direction*”); SAMSUNG-1003, ¶54. This longest dimension is **along the first direction**: the longest dimension of the fins is

⁵ The ’812 Patent uses “diffusion region” interchangeably with “fin”: “Gate and TCN endcap regions refer to gate and TCN overlap of the *diffusion region/fins* of semiconductor devices.” SAMSUNG-1001, 2:66-3:1; SAMSUNG-1003, ¶52.

traversed *as one moves along the fins in the first direction*, e.g., top to bottom in the top view, into the page in the A-A cross-section. SAMSUNG-1003, ¶54.

Also in the combination, Chang describes **forming the fins**, e.g., the diffusions. *See* SAMSUNG-1009, [0039] (“**Diffusions 104 may be formed** on a substrate 102”), FIG. 4. For instance, Chang’s diffusions are formed by using a patterned photoresist (*see id.*, [0040]) to guide etching of a stack of materials including a “hardmask layer 508, [a] pad oxide layer 506, and *[a] semiconductor layer 504*,” which “may comprise *single crystal silicon*.” SAMSUNG-1009, [0041], FIG. 5, *infra* (outlining the semiconductor layer in pink). The remaining portions of the semiconductor layer following the etch and subsequent removal of the hardmask and pad oxide layers constitute the diffusions. *See id.*, [0041], [0045]-[0046], [0011], FIGS. 6 (*infra*) and 9-10; SAMSUNG-1003, ¶55.

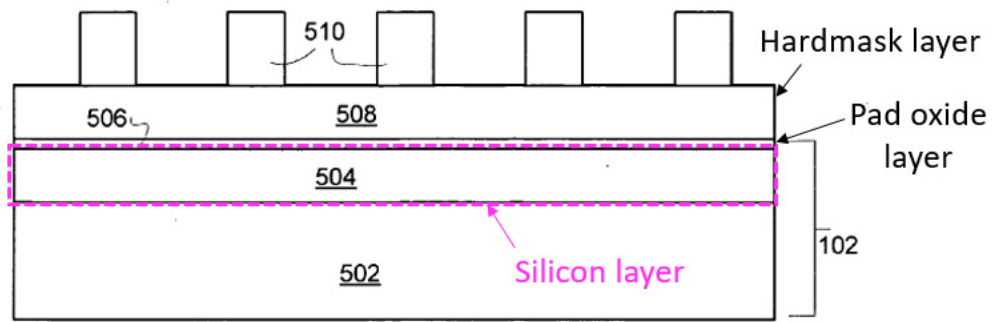


Fig. 5

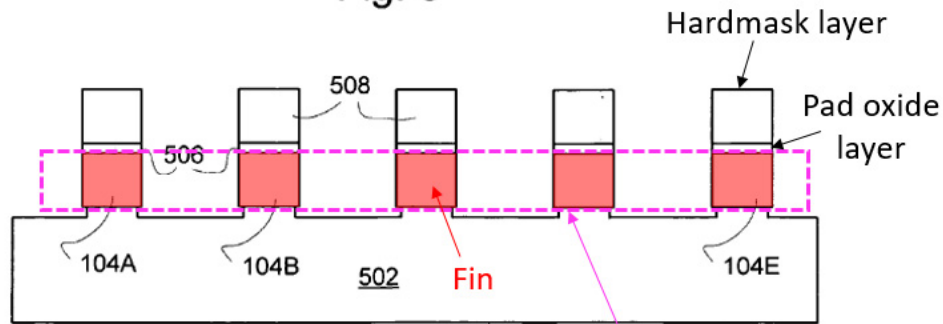


Fig. 6

Excerpts from Chang, FIGS. 5-6 (annotated)

The fins of the combination, *e.g.*, Chang's diffusions, **comprise silicon**, *e.g.*, as evidenced by Chang's fabrication process. As described *supra*, Chang's diffusions are formed of portions of the silicon layer 504 (outlined in pink *supra*), and thus they **include silicon**. See SAMSUNG-1009, [0041], FIGS. 5-6; SAMSUNG-1003, ¶56.

Limitation [21c]

In the Chang-Tseng combination, a “*dielectric material*” is disposed in the spaces between fins “to form isolation regions” such as “*shallow trench isolation*

(STI) regions,” based on Tseng. SAMSUNG-1005, 4:25-32, FIG. 4A;

SAMSUNG-1003, ¶57. The dielectric material of the STI regions, purple in the figure *infra*, is **an isolation material**. SAMSUNG-1003, ¶57; *see* SAMSUNG-1005, 2:15-19, 3:9-10 (“an insulation region 204 between the first fin 202a and second fin 202b”), 4:20-57; claims 1, 10, 12, FIGS. 1-2 and 4-10.

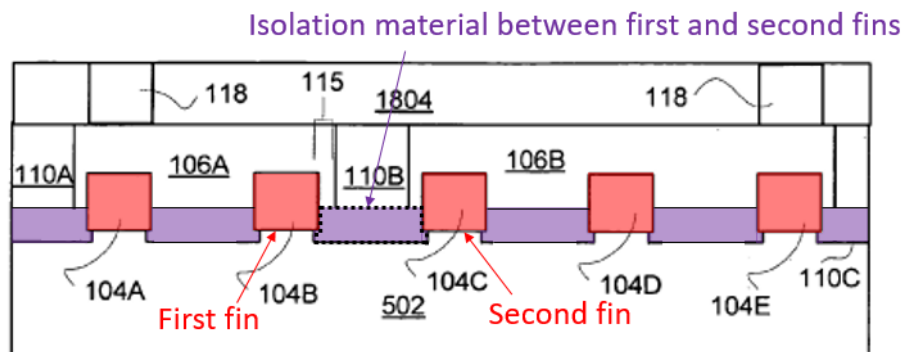


Fig. 18a

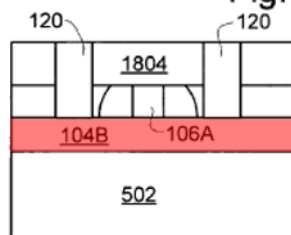


Fig. 18c

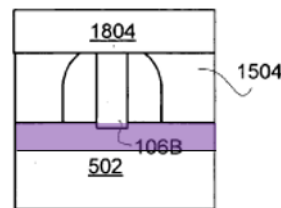


Fig. 18d

Chang-Tseng figures

The isolation material is **formed**, *e.g.*, deposited between the diffusions: the spaces between fins “are filled with a dielectric material to form the isolation regions 204,” *e.g.*, “using a chemical vapor deposition process.” SAMSUNG-1005, 4:25-40; *see* FIG. 4A; SAMSUNG-1003, ¶58. For instance, the dielectric

material is deposited “after formation of the diffusions” onto a structure such as that of Chang’s FIG. 6, as illustrated *infra*. SAMSUNG-1005, [0011]; *see* [0041]; SAMSUNG-1003, ¶58.

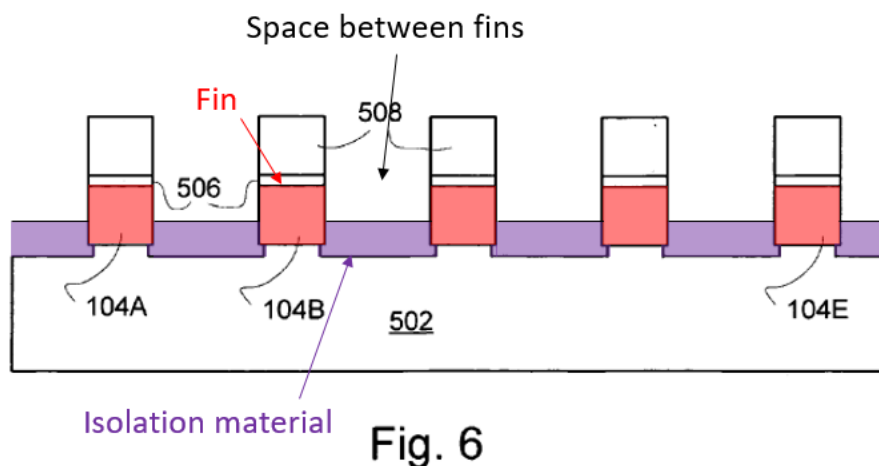


Fig. 6
Chang-Tseng figure

In the combination, the dielectric material of the STI regions is **an isolation material** because it provides electrical isolation between fins: “the trenches 22 are filled with a dielectric material to form the isolation regions 204 to define and *electrically isolate the various fins of the fin structure 202*. In one example, the isolation regions 204 include shallow trench isolation (STI) regions.” SAMSUNG-1005, 4:25-29; *see* SAMSUNG-1010, 1:43-45; SAMSUNG-1031, 5:16-18; SAMSUNG-1034, 2:24-36; SAMSUNG-1035, 1:22-32; SAMSUNG-1003, ¶59.

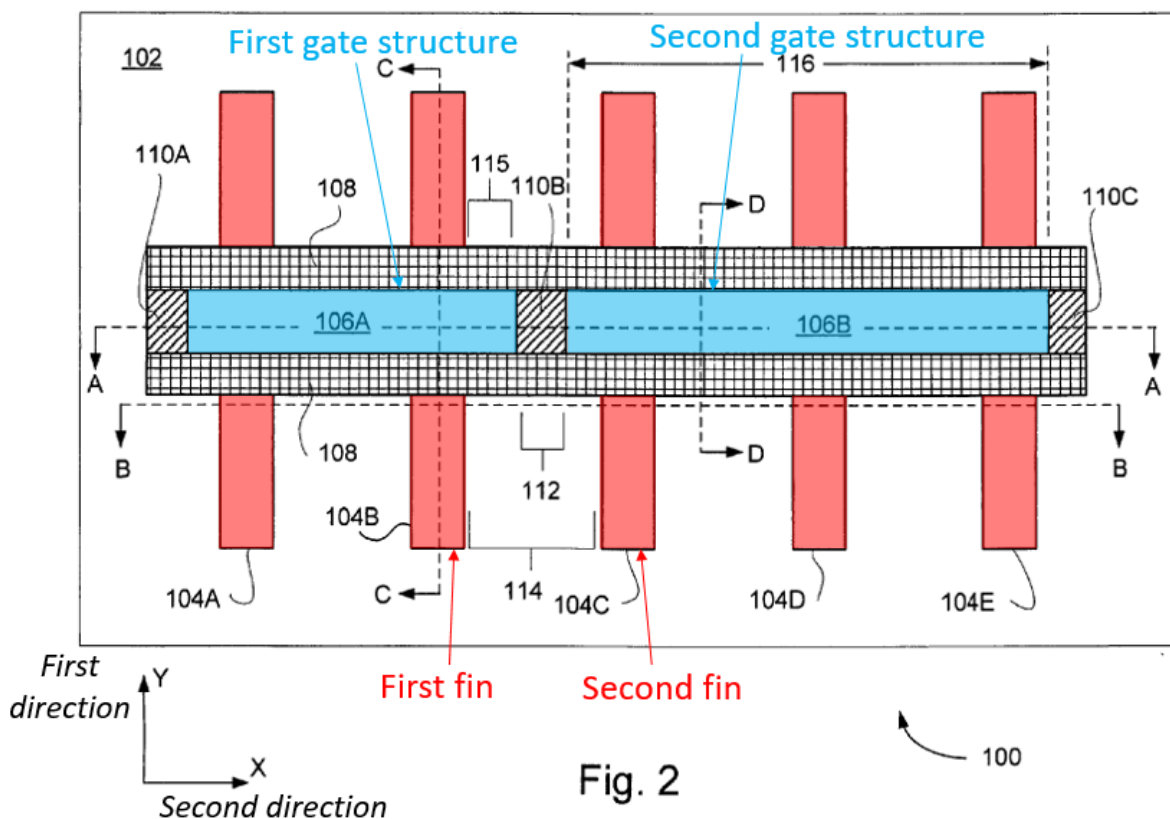
The isolation material (*e.g.*, the dielectric material of Tseng’s STI regions) is **between the fins**: it is in the space separating the fins (*e.g.*, Chang’s diffusions), as shown *supra*. *See* SAMSUNG-1005, 3:9-10 (“an insulation region 204 *between*

the first fin 202a and second fin 202b”), 4:20-24, 2:15-19; claims 1, 10, 12, FIGS.

2, 4-10; SAMSUNG-1003, ¶60.

Limitations [21d] and [21e]

The Chang-Tseng combination includes **first and second gate structures**, e.g., Chang’s gates 106, blue in the figures *infra*. See SAMSUNG-1009, [0036] (“a circuit 100 that includes transistors with end caps of **gates 106** self-aligned to diffusions 100”), [0037], [0039], [0047], [0050], [0056]; claims 1, 10, 15, 18, FIGS. 2-4, FIGS. 18a-d; SAMSUNG-1003, ¶61.



Chang-Tseng figure

disclosure of this orthogonality is not explicit, a POSITA would have understood this to be the case, or otherwise found this to have been obvious, consistent with Chang's disclosure (*see* SAMSUNG-1009, FIGS. 2-3, FIGS. 18a-d) and given that gate structures orthogonal to fins in FinFET devices was well-known. *See, e.g.*, SAMSUNG-1030, Abstract ("The fin structures each comprise a semiconductor layer and extend in a first direction, and the gate stack extends in a second direction that is perpendicular."); SAMSUNG-1008, [0053]; SAMSUNG-1029, [0042]; SAMSUNG-1003, ¶63.

In the combination, Chang describes **forming the first gate structure over the first fin and forming the second gate structure is over the second fin**, as shown *supra*. *See* SAMSUNG-1009, FIG. 2, FIG. 4, FIGS. 18a-18d; SAMSUNG-1003, ¶64. For instance, in Chang's "replacement gate process," "first gate material 1102 around the diffusions" is removed, exposing the diffusions and defining "a volume within which the gates 106 may be formed." SAMSUNG-1009, [0055], FIG. 17a. The gates 106 are then formed in that volume. *See id.*, [0056], FIG. 18a. The gate material deposited into that volume is deposited over the exposed diffusions (*e.g.*, **over the fins**). *See id.*, [0055]-[0056], [0039], FIGS. 17a and 18a; SAMSUNG-1003, ¶64.

Moreover, as illustrated *infra*, **the second gate structure is discontinuous with the first gate structure**. The gate structures (*e.g.*, Chang's gates, blue) are

separated by the isolation structure (green; *see* [21f]). *See* SAMSUNG-1009,

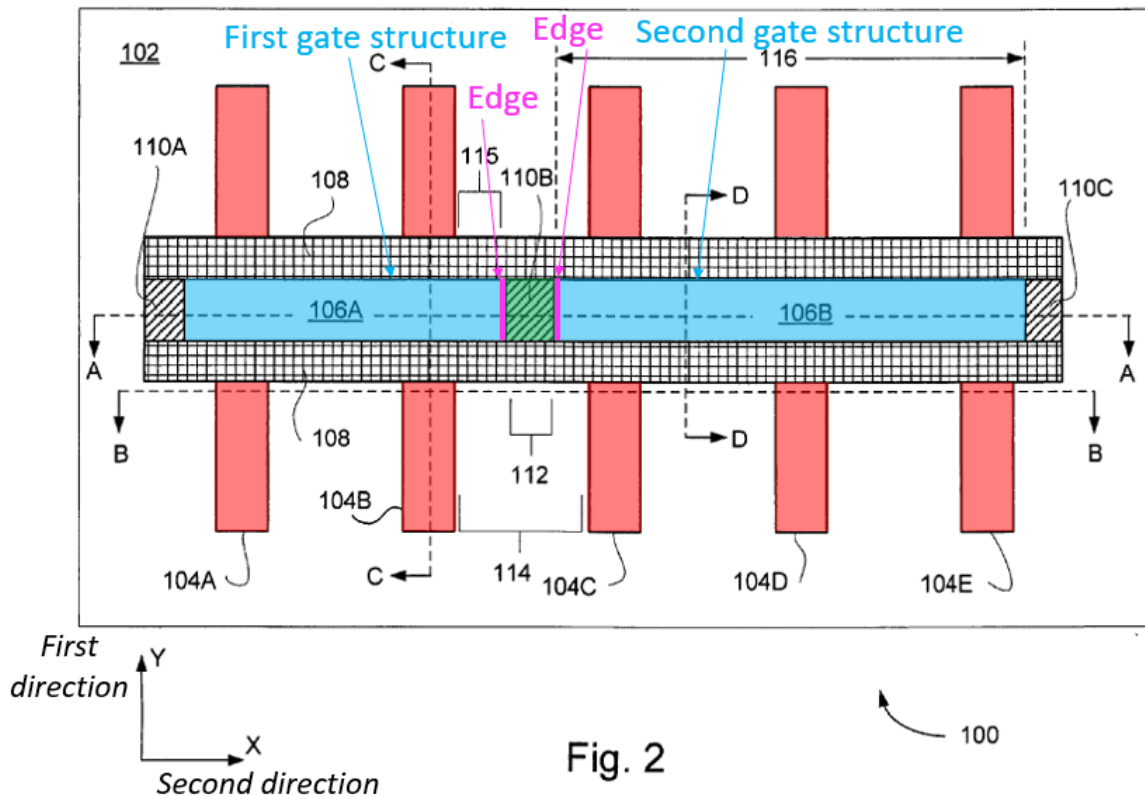
[0036] (“The isolation structures 110 may have a width 112 that determines *the*

distance between adjacent gates 106”), claim 15 (“an insulating isolation structure

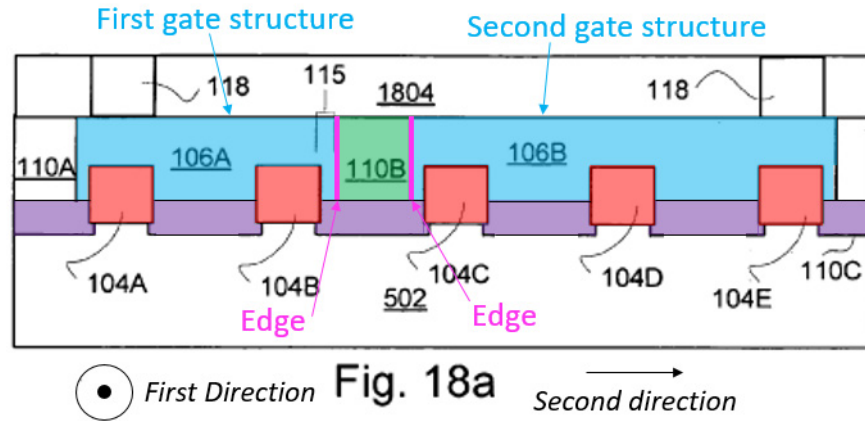
between the first and second gates that *separates* and insulates *the first and second*

gates from each other”), [0044], [0055], claim 1, FIGS. 2-4, FIGS. 18a-18d;

SAMSUNG-1003, ¶65.



Chang-Tseng figure



Chang-Tseng figure

The discontinuity is **along the second direction**: the discontinuity is reached *as one moves in the second direction* from one gate structure to the other (left to right in the FIG. 2 and FIG. 18a views). See SAMSUNG-1009, FIGS. 2-3, FIGS. 18a-18d; SAMSUNG-1003, ¶66.

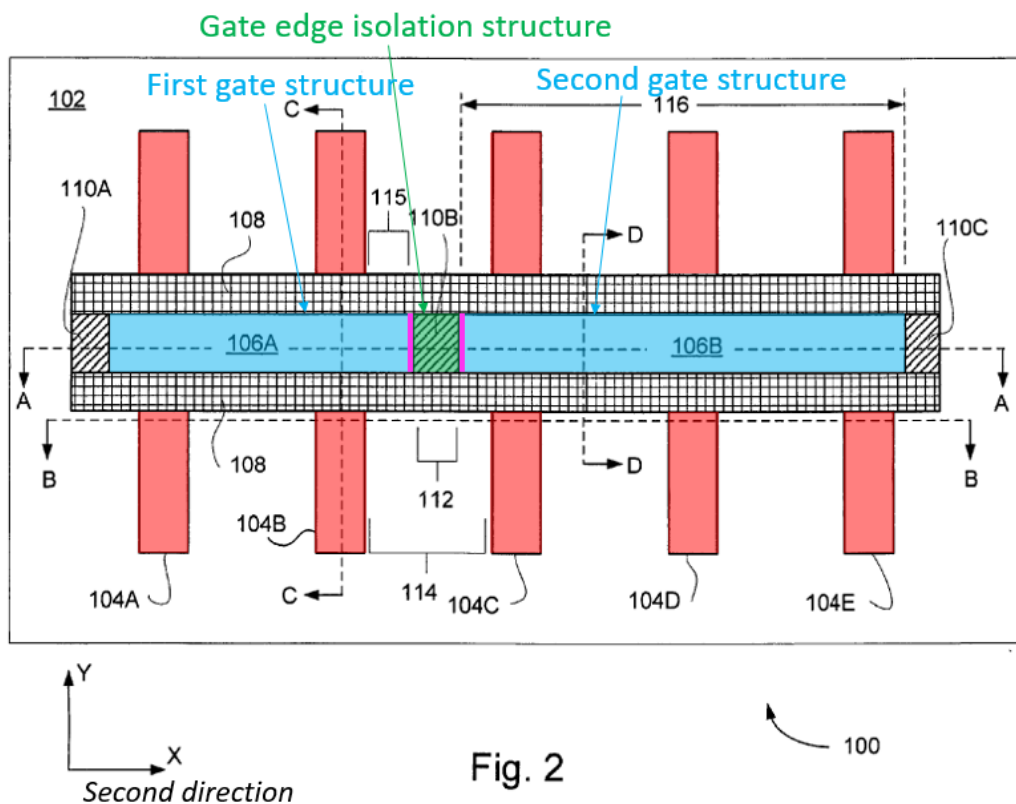
The figures *supra* also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge of the first gate structure** (also outlined in pink), *e.g.*, the edges of the gate structures that contact the isolation structure 110B face one another. See SAMSUNG-1009, [0037], FIGS. 2-3, FIGS. 18a-18d; SAMSUNG-1003, ¶67. The edges face one another **along the second direction**: from the edge of the second gate structure, the edge of the first gate structure is reached *as one moves in the second direction* (left to right in the top and FIG. 18a cross-sectional views). SAMSUNG-1003, ¶67.

In the Chang-Tseng combination, each gate structure includes **a gate dielectric layer and a gate electrode**: “*a final metal gate and gate dielectric*

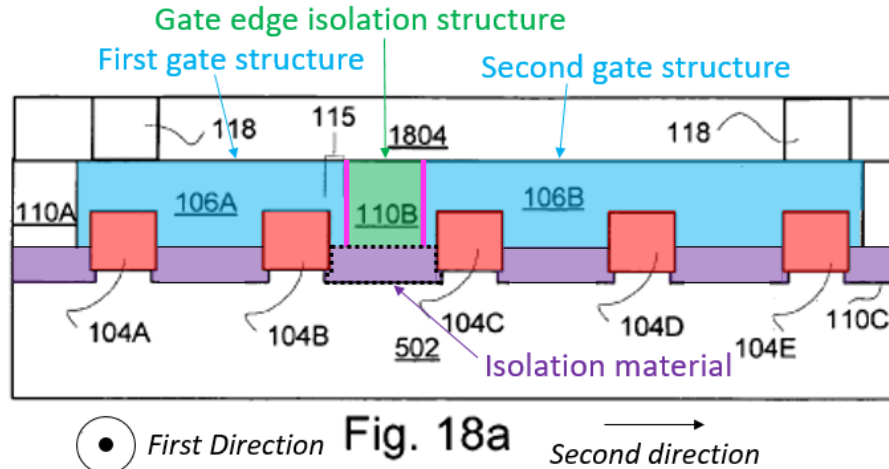
replace the place-holder first gate material 1102.” SAMSUNG-1009, [0047]; *see* [0064], [0066]; SAMSUNG-1003, ¶68.

Limitation [21f]

The Chang-Tseng combination includes a **gate edge isolation structure**, *e.g.*, Chang’s isolation structure 110B, green in the figures *infra*. *See* SAMSUNG-1009, [0039] (“*Insulating isolations structures 110* may be formed 406 between the diffusions”), [0037], [0043]-[0044], FIGS. 2-4, FIGS. 14a-18d; claims 1, 10-12, 15, 18; SAMSUNG-1003, ¶69.



Chang-Tseng figure



Chang-Tseng figure

In the combination, Chang's isolation structure 110B is a **gate edge isolation structure**: it is a self-aligned structure disposed between and in contact with edges of gate structures (discussed *infra*) and isolates those gate structures from one another (*e.g.*, physically and electrically).⁶ SAMSUNG-1003, ¶70.

Notably, Chang's isolation structure is a **self-aligned** structure. See SAMSUNG-1009, [0046] ("The self-alignment may be accomplished by forming gate isolation structures 110 **self-aligned** to the diffusion 104"), Abstract, [0039], [0044]; claims 1, 10, 18; SAMSUNG-1003, ¶71.

Moreover, Chang's isolation structure **physically isolates** the gate structures: the isolation structure is "between the first and second gates" and "**separates ... the**

⁶ For the purposes of this proceeding, Petitioner interprets the phrase "gate edge isolation structure" consistent with the written description of the '812 Patent.

first and second gates from each other.” SAMSUNG-1009, claim 15; *see* [0035]-[0036], [0044], [0055], claim 1, FIGS. 2-4, FIGS. 18a-18d; SAMSUNG-1003, ¶72.

Chang’s isolation structure also *electrically isolates* the gate structures. *See* SAMSUNG-1009, [0035] (“The gates may be self-aligned to *isolation structures insulating gates from each other*”), [0039], Abstract, [0007], claim 15, FIG. 4; SAMSUNG-1003, ¶73.

In the combination, Chang describes **forming the gate edge isolation structure**. Chang describes that “[a] layer of an insulating material 802 may then be deposited to substantially fill the volumes between spacers.” SAMSUNG-1009, [0043], FIG. 8. In the combination, as shown *infra*, that insulating material (green) is deposited over the previously-deposited isolation material (purple; *see* [21c]). SAMSUNG-1003, ¶74. “The layer of insulating material 802 ... may then be planarized,” and “[p]ortions of the insulating material 802 may be used as the insulating isolation structures 110.” *Id.*, [0043]-[0044]; *see* [0039], Abstract, FIG. 4, claims 1, 10-11, 18; SAMSUNG-1003, ¶74.

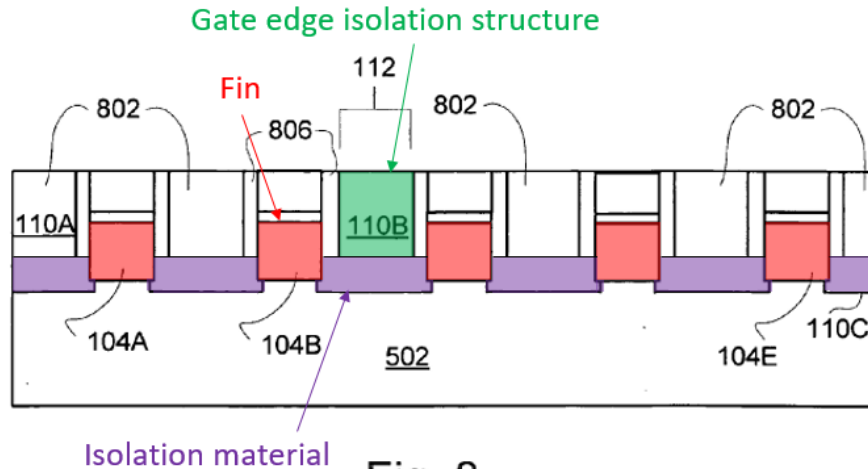


Fig. 8

Chang-Tseng figure

Also in the combination, **the gate edge isolation structure** (e.g., Chang's isolation structure) **between and in contact with the edge of the first gate structure and the edge of the second gate structure**. The figures *supra* illustrate this positioning, with the edges of the gate structures outlined in pink.

SAMSUNG-1003, ¶75.

Specifically, Chang describes that the gate edge isolation structure is **between** the gate structures: “an insulating isolation structure *between the first and second gates* that separates ... the first and second gates from each other.”

SAMSUNG-1009, claim 15; *see* [0035]-[0036], [0044], [0055], claim 1, FIGS. 2-4, FIGS. 18a-18d; SAMSUNG-1003, ¶76.

Additionally, the gate edge isolation structure is **in contact with** the edges of the gate structures, as evidenced by Chang's description of the fabrication process. In Chang's process, the “first gate material 1102” is removed, exposing the edges

of the isolation structure 110B. SAMSUNG-1009, [0055]; *see* FIG. 17a

SAMSUNG-1003, ¶77. The gates are then formed in the space previously occupied by the first gate material 1102, thus contacting the exposed edges of the isolation structure. *See* SAMSUNG-1009, [0056], [0047]; SAMSUNG-1003, ¶77.

The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction: *as one moves in the second direction*** (left to right in the top and FIG. 18a cross-sectional views) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure. SAMSUNG-1003, ¶78.

Furthermore, in the combination, the gate edge isolation structure is **over the isolation material**, as shown in the figures *supra*. SAMSUNG-1003, ¶79. As discussed in §IV.A.3, the isolation material (*e.g.*, Tseng's STI material) is deposited into the spaces between the fins. *See* SAMSUNG-1005, 4:25-32, FIGS. 2 and 5A. A "layer of an insulating material 802," which will become the gate edge isolation structure, then is deposited into the spaces between fins, and onto the previously-deposited isolation material. SAMSUNG-1009, [0042]-[0044], FIGS. 7-8; *see* SAMSUNG-1005, 4:25-32. Thus, the gate edge isolation structure is over the isolation material. SAMSUNG-1003, ¶79.

Limitation [21g]

In the combination, Chang's spacers are a dielectric material

To the extent Patent Owner equates gate spacers to the claimed dielectric material, the Chang-Tseng combination describes **forming a dielectric material**, *e.g.*, Chang's "**spacers 108**," yellow in the figures *infra*, disposed "on either side of the gates 106." SAMSUNG-1009, [0037]; *see* [0049] (describing that Figs. 14a-14c "illustrate[] the circuit 100 **after formation of the spacers 108**"), [0054], [0055], FIGS. 2-3, FIGS. 14a-18d; SAMSUNG-1003, ¶80. The spacers are **dielectric material** at least because they are formed of a dielectric (*e.g.*, insulating) material. *See* SAMSUNG-1009, [0045] ("spacers 108 (which may comprise carbon-doped silicon nitride)"); SAMSUNG-1003, ¶80.

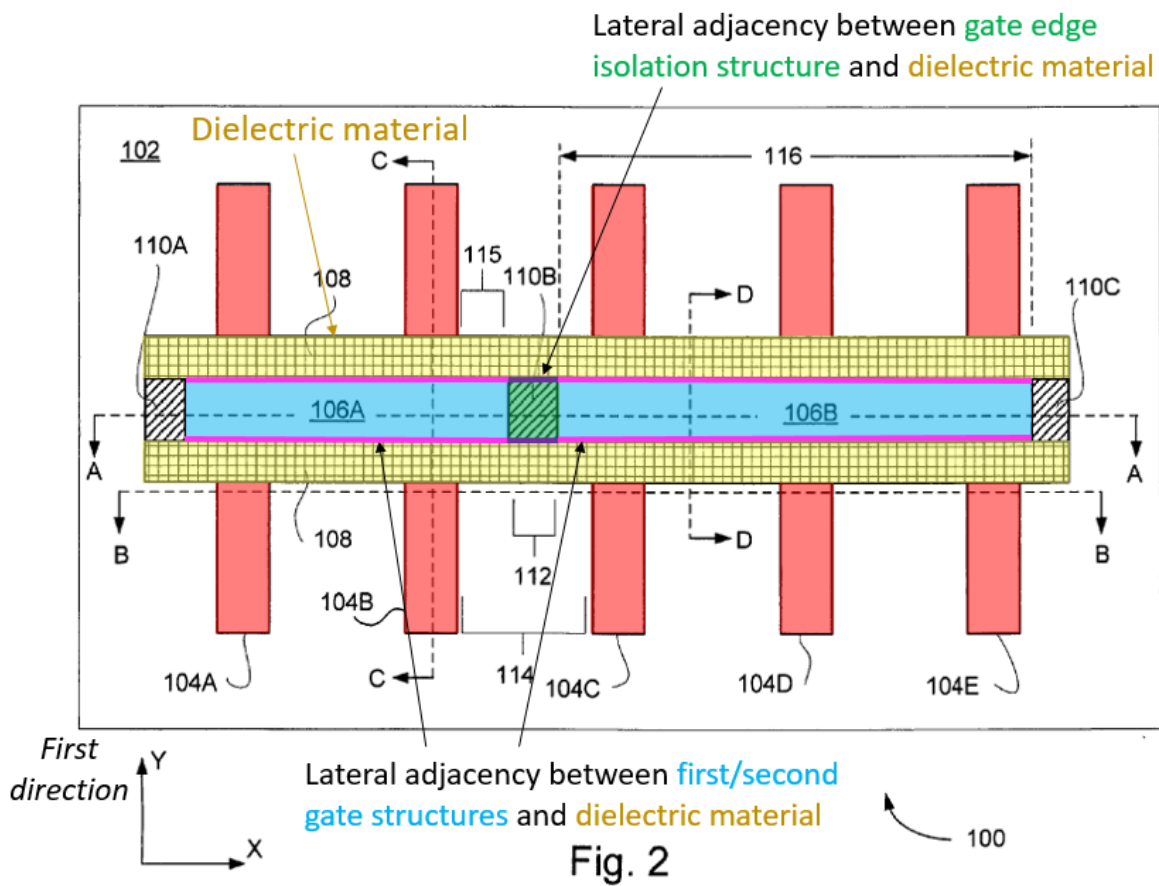
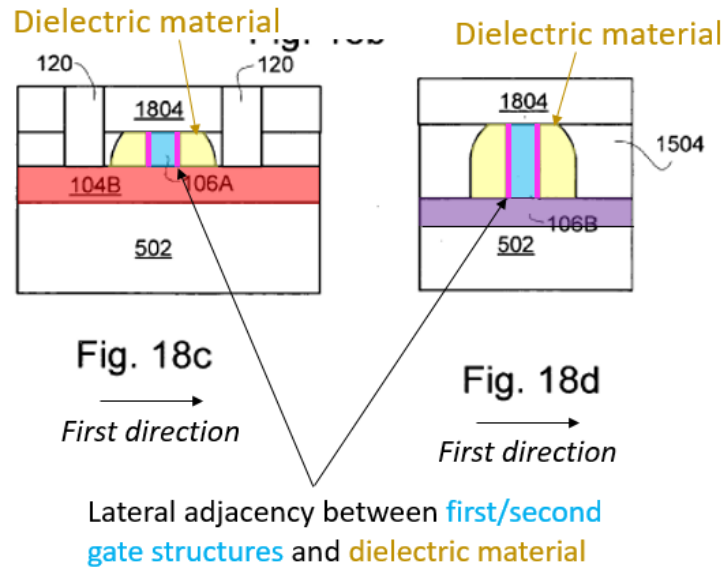


Fig. 2

Chang-Tseng figure



Chang-Tseng figures

The sidewalls of the gate structures, outlined in pink, extend into the page of the top-view figure. As can be seen from the cross-sectional figures, **the dielectric material (yellow) is laterally adjacent to the gate structures** at least at these pink-outlined sidewalls. For instance, the dielectric material (*e.g.*, the spacer) is near (*e.g.*, next to) the sidewalls of the gate structures. SAMSUNG-1003, ¶81.

The sidewalls of the gate edge isolation structure, outlined in purple, extend into the page of the top-view figure, *e.g.*, substantially even with the sidewalls of the gate structures. The spacers are disposed on either side of the gate edge isolation structure at these purple-outlined sidewalls. *See* SAMSUNG-1009, FIGS. 2-3; SAMSUNG-1003, ¶83. The spacers are thus near (*e.g.*, next to) the sidewalls of the gate edge isolation structure, *e.g.*, **the dielectric material (yellow) is**

laterally adjacent to the gate edge isolation structure at least at these purple-outlined sidewalls. SAMSUNG-1003, ¶83.

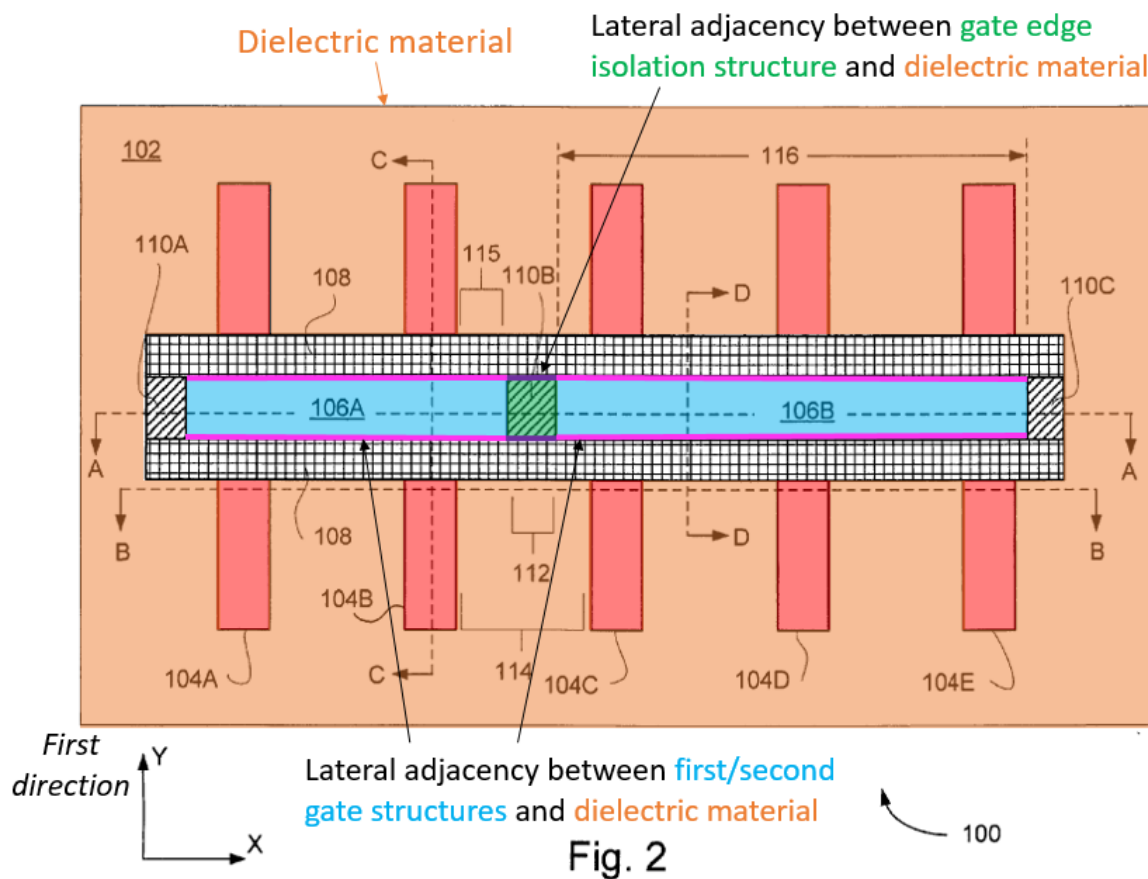
The dielectric material is laterally adjacent to the gate structures and gate edge isolation structure **along the first direction**: viewing the structure starting from either gate structure or from the gate edge isolation structure and ***moving along the first direction*** (*e.g.*, top to bottom in the top-view), one reaches the dielectric material. SAMSUNG-1003, ¶¶82, 84.

In the Chang-Tseng combination, **the dielectric material** (*e.g.*, the spacers) **is discrete from the gate edge isolation structure** (*e.g.*, the isolation structure 110B) at least because ***they are formed in two distinct processing steps***. The gate edge isolation structure is formed prior to deposition of the spacers. *See* SAMSUNG-1009, [0043], [0049], FIG. 8, FIGS. 14a-14c; SAMSUNG-1003, ¶85.

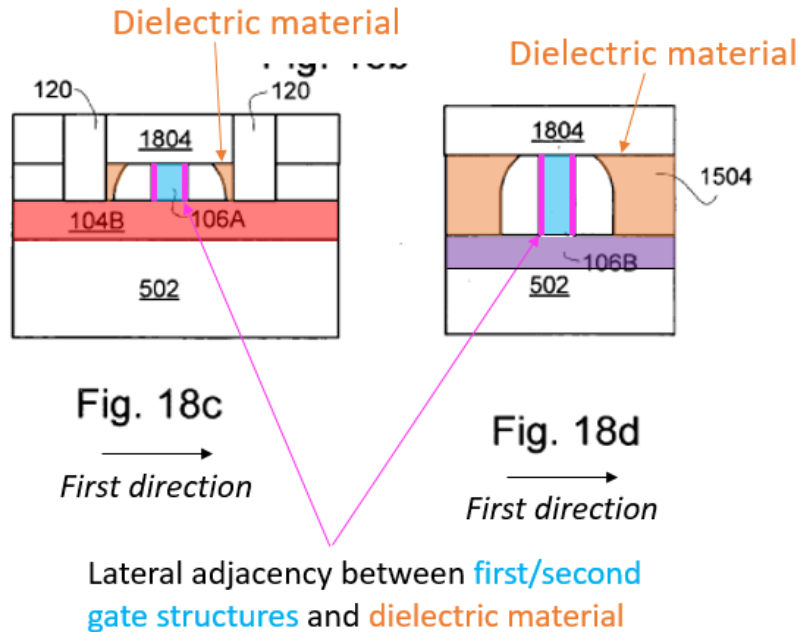
Alternatively or additionally, **the dielectric material is discrete from the gate edge isolation structure** at least because ***they are composed of two different materials***. The dielectric material (*e.g.*, Chang's spacers) are carbon-doped silicon nitride while the gate edge isolation structure (*e.g.*, Chang's isolation structure) is silicon nitride. *See* SAMSUNG-1009, [0054], [0043]-[0044] ("the insulating material 802 may comprise silicon nitride"); SAMSUNG-1003, ¶86.

In the combination, Chang's interlayer dielectric is a dielectric material

Alternatively or additionally, in the Chang-Tseng combination, Chang describes **forming a dielectric material**: “a ***layer 1504 of interlayer dielectric (ILD)***” (e.g., **a dielectric material**, orange in the figures *infra*) is “deposited and planarized so the top of the ILD layer 1504 [is] substantially planar with the top of the remaining insulating material 802 and first gate material 1102.” SAMSUNG-1009, [0051]; *see* FIGS. 15a-18d; SAMSUNG-1003, ¶87. As shown in the top-view figure, the ILD is disposed around the structure that includes the gate structures, gate edge isolation structure, and spacers. *See* SAMSUNG-1009, [0044]), [0051]; SAMSUNG-1003, ¶87.



Chang-Tseng figure



Chang-Tseng figures

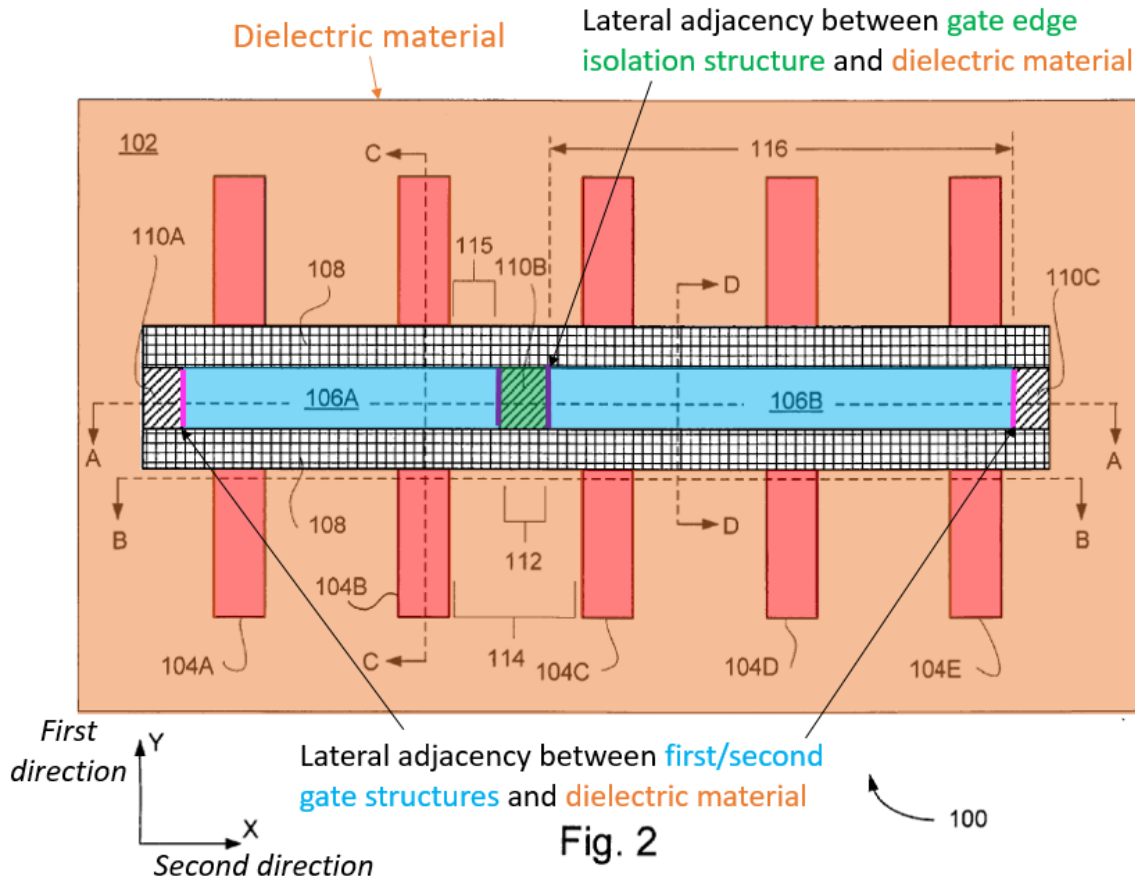
The sidewalls of the gate structures, outlined in pink, extend into the page of the top-view figure. As can be seen from the cross-sectional figures, **the dielectric material** (orange) is **laterally adjacent to the gate structures** at least at these pink-outlined sidewalls. For instance, the dielectric material (*e.g.*, Chang's ILD) contacts the spacers (*see* SAMSUNG-1009, [0037]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate structures, *e.g.*, the dielectric material is near (*e.g.*, next to) the sidewalls of the gate structures. SAMSUNG-1003, ¶88.

The sidewalls of the gate edge isolation structure, outlined in purple, extend into the page of the top-view figure, *e.g.*, substantially even with the sidewalls of the gate structures. As with the sidewalls of the gate structures, **the dielectric**

material (orange) is **laterally adjacent to the gate edge isolation structure** at least at these purple-outlined sidewalls. For instance, the dielectric material (*e.g.*, Chang's ILD) contacts the spacers (*see* SAMSUNG-1009, [0037]) that are disposed on those sidewalls. The dielectric material is thus **laterally adjacent** to the gate edge isolation structure, *e.g.*, the dielectric material is near (*e.g.*, next to) the sidewalls of the gate edge isolation structure. SAMSUNG-1003, ¶90.

The dielectric material is laterally adjacent to the gate structures and gate edge isolation structure **along the first direction**: viewing the structure starting from the either gate structure or from the gate edge isolation structure and ***moving along the first direction*** (top to bottom in the top view), one reaches the dielectric material. SAMSUNG-1003, ¶¶89, 91.

Alternatively or additionally, the dielectric material is laterally adjacent to the gate structures and gate edge isolation structure at the pink-outlined and purple-outlined locations, respectively, in the alternative top-view figure *infra*. SAMSUNG-1003, ¶¶92-93. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material is laterally adjacent to the gate structures and gate edge isolation structure along the first direction. SAMSUNG-1003, ¶¶92-93.



Chang-Tseng figure (alternative)

In the Chang-Tseng combination, **the dielectric material** (e.g., Chang's ILD) **is discrete from the gate edge isolation structure** (e.g., Chang's isolation structure) at least because *they are formed in two distinct processing steps*. The gate edge isolation structure is formed prior to deposition of the ILD. See SAMSUNG-1009, [0043]-[0044], [0051], FIG. 8, FIGS. 15a-15d; SAMSUNG-1003, ¶94.

(2) Claim 22

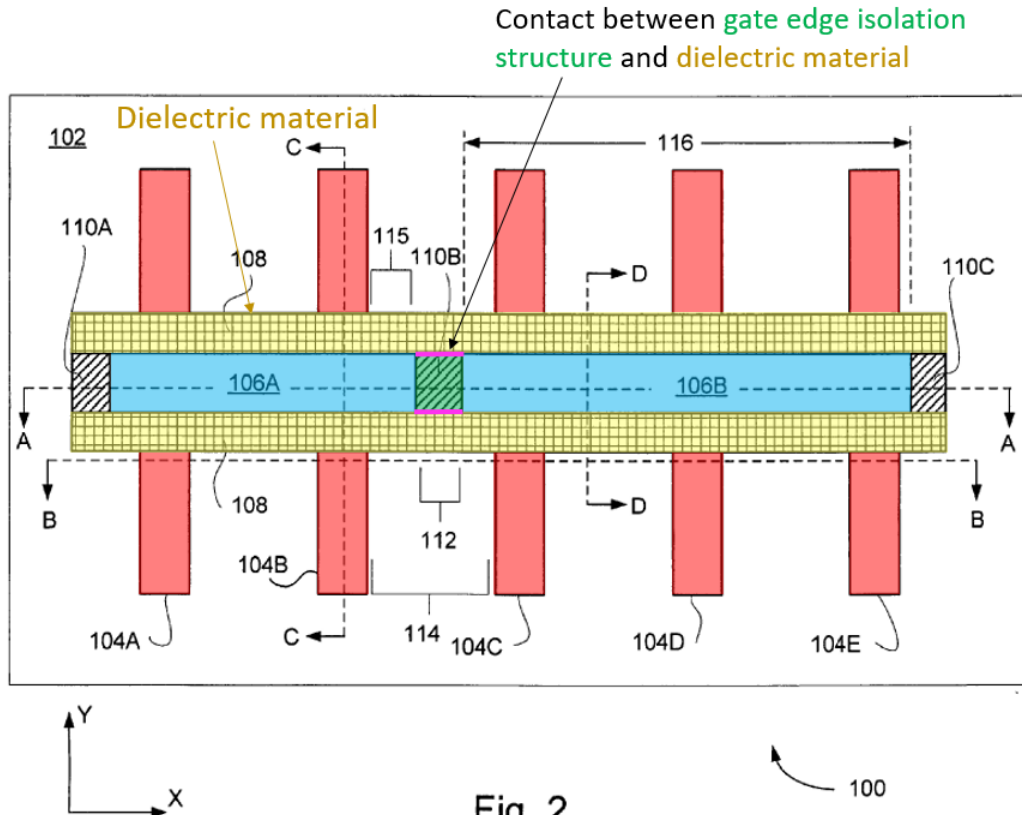
Limitation [22]

In the combination, Chang describes that the gate edge isolation structure **comprises silicon and nitrogen**. Chang's "insulating material 802 may comprise silicon nitride," where "[p]ortions of the insulating material 802 may be used as the insulating isolation structures 110." SAMSUNG-1009, [0043]-[0044]; SAMSUNG-1003, ¶95.

(3) Claim 23

Limitation [23]

In the combination, Chang's spacers (the dielectric material; *see* [21g]) are **in contact with the gate edge isolation structure** (at least on the pink-highlighted sidewalls of the gate edge isolation structure, as shown *infra*. SAMSUNG-1003, ¶96.



Chang-Tseng figure

Chang's fabrication process reveals the contact between the gate edge isolation structure and the dielectric material (*e.g.*, Chang's spacers). Chang describes that "[a] layer of an insulating material 802 may then be deposited to substantially fill the volume between spacers 806," *i.e.*, the spacers contact the insulating material 802, which later becomes the isolation structures (*e.g.*, the gate edge isolation structure). SAMSUNG-1009, [0043]-[0044]; *see* FIG. 8; SAMSUNG-1003, ¶97.

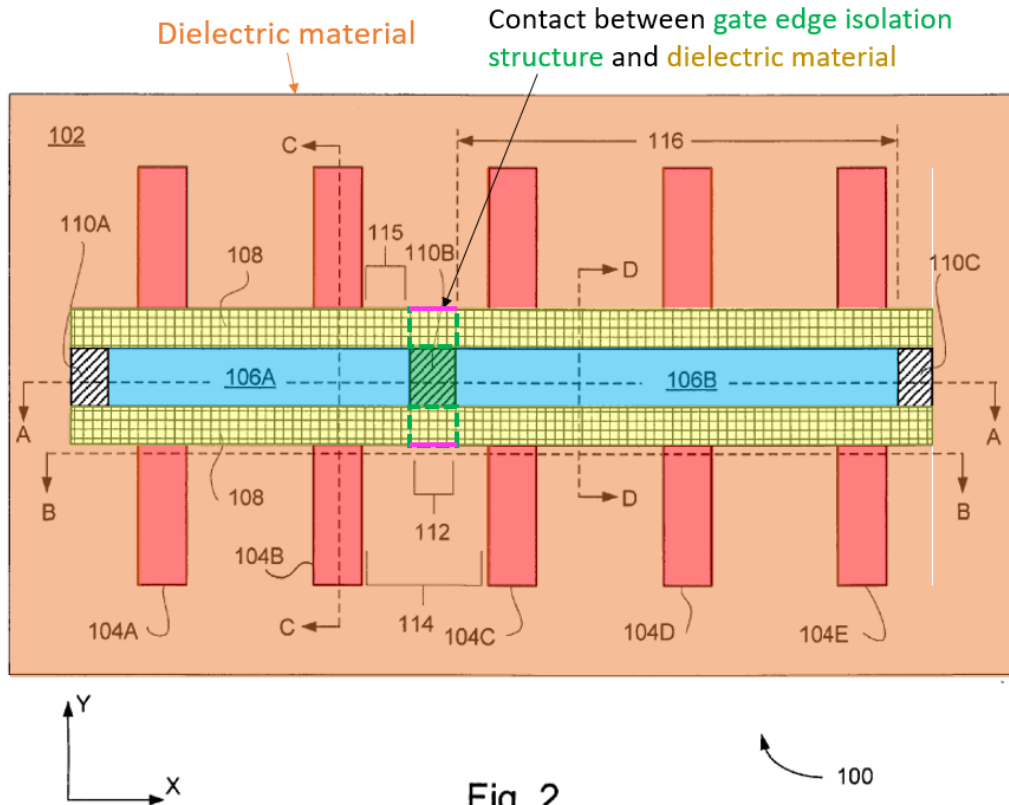
Alternatively or additionally, the portion of the spacer outlined in dashed lines in the figure *infra* is aligned with the gate edge isolation structure. To the

extent that this portion of the spacer, , can be considered part of the gate edge

isolation structure, the dielectric material (orange) is in contact with the gate edge

isolation structure at least at the outer edges of the spacers, outlined in pink.

SAMSUNG-1003, ¶98.



Chang-Tseng figure

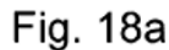
(4) Claim 24

Limitation [24]⁷

In the Chang-Tseng combination, **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures.** In Chang's replacement gate process (*see* SAMSUNG-1009, [0047], [0050], [0056]-[0057], FIGS. 17-18), the sacrificial "first gate material 1102" is removed defining "a volume within which the gates 106 may be formed" and exposing the edges of the isolation structure 110B. SAMSUNG-1009, [0055], FIG. 17a; SAMSUNG-1003, ¶¶99-100. The gates are then formed in the defined volume, thus contacting the exposed edges of the isolation structure. *See* SAMSUNG-1009, [0055]-[0056], [0047]; SAMSUNG-1003, ¶¶99-100. A POSITA would have understood that formation of these gates can involve depositing first the gate dielectric layer and then the gate electrode into that defined volume. *See* SAMSUNG-1025, 4:39-5:56, FIG. 8A; SAMSUNG-1005, 8:62-9:4; SAMSUNG-1015, [0045]-[0047];

⁷ As best understood, Petitioner interprets the "gate dielectric layer of the first gate structure" and the "gate dielectric layer of the second gate structure" of claim 24 as being equivalent to the "first gate dielectric layer" and "second gate dielectric layer," respectively, of claim 21.

As illustrated in the figure *infra*, depositing the gate dielectric layer (dark blue) into this defined volume coats the gate dielectric layer onto exposed surfaces, including exposed edges of the isolation structure (green), *i.e.*, **the gate edge isolation structure** (*e.g.*, the isolation structure) **is in contact with the gate dielectric layer**. See SAMSUNG-1025, 4:39-5:56; SAMSUNG-1040, 6:33-38, FIGS. 7A-7B (showing the gate dielectric layer 704 coating onto exposed sidewalls of an opening formed by removing a dummy gate structure); SAMSUNG-1036, [0023], FIG. 1F; SAMSUNG-1003, ¶101.



Chang-Tseng figure

(5) Claim 26

In the combination, the gate dielectric layers of the gate structures **include a high-k dielectric material**. SAMSUNG-1003, ¶102.

Tseng's FinFET includes "a gate stack 210" including a "gate electrode layer 214 and [a] gate dielectric layer 212." SAMSUNG-1005, 5:5-10; *see* FIG. 9A. The gate dielectric layer can be a "high dielectric constant (high-k) dielectric," and the gate electrode is a metal. SAMSUNG-1005, 5:12-46. Tseng's gate stack can be fabricated "using a gate-last process performed by first forming a dummy gate stack." *Id.*, 8:59-62; SAMSUNG-1003, ¶103.

In the Chang-Tseng combination, the gate dielectric layer of the gate structures (*see* SAMSUNG-1009, [0047]) is implemented as a "***high dielectric constant (high-k) dielectric***" and the gate electrode is implemented as a metal gate electrode, as taught by Tseng. SAMSUNG-1005, 5:12-46, 8:67-9:4, FIG. 5A; SAMSUNG-1003, ¶104.

A POSITA would have been motivated to implement the gate dielectric layer of the combination's gate structures as a high-k gate dielectric layer for at least the following reasons. SAMSUNG-1003, ¶¶105-110.

First, a POSITA would have been motivated to pursue the use of a high-k gate dielectric layer (*e.g.*, along with a metal gate electrode) to obtain performance advantages afforded by these materials, *e.g.*, decreased threshold voltage, reduced fringe capacitance, and suppressed leakage current. *See* SAMSUNG-1011, 1:32-35; SAMSUNG-1026, Abstract; SAMSUNG-1027, 1:38-46; SAMSUNG-1028, Abstract; SAMSUNG-1003, ¶106. Moreover, the use of a high-k gate dielectric

layer provides finer control over the channel potential, enabling more effective on/off control to be achieved, thus facilitating higher speed performance. *See* SAMSUNG-1028, Abstract; SAMSUNG-1003, ¶106.

Second, gate structures having high-k gate dielectric layers and metal gate electrodes were standard elements of FinFET transistors, such as the FinFET structure of the Chang-Tseng combination. *See, e.g.*, SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1011, 3:59-4:10; *see* SAMSUNG-1001, 3:49-4:49. The implementation of the gate dielectric layer and gate electrode layer as a high-k gate dielectric layer and a metal gate electrode, respectively, is thus merely a comprehensive implementation of a structure already described by the Chang-Tseng combination. SAMSUNG-1003, ¶107.

Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, high-k gate dielectric layers and metal gate electrodes) to a known structure (*e.g.*, the gate insulation layer and bulk conductive metal layer of the gate structure of the Chang-Tseng FinFET device) to yield predictable results (*e.g.*, a gate structure having a high-k gate dielectric layer and a metal gate electrode). SAMSUNG-1003, ¶108; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success in pursuing this implementation given that high-k gate dielectric layers and metal gate electrodes are well-known

elements of FinFET gate structures. *See* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025, 4:39-5:3, FIG. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-48; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0046]-[0047]; SAMSUNG-1003, ¶109. A POSITA also would have expected success because these materials are consistent with Chang’s description of the composition of its gate structures when fabricated using a subtractive process. *See* SAMSUNG-1009, [0064] (“The gate dielectric may comprise ... a layer of high-k dielectric material ... The first gate material 2202 may comprise Au, TiN, or another suitable material”); SAMSUNG-1003, ¶110.

B. [GROUND 2] – CLAIMS 21-24 AND 26 ARE OBVIOUS OVER AKARVARDAR AND XIE

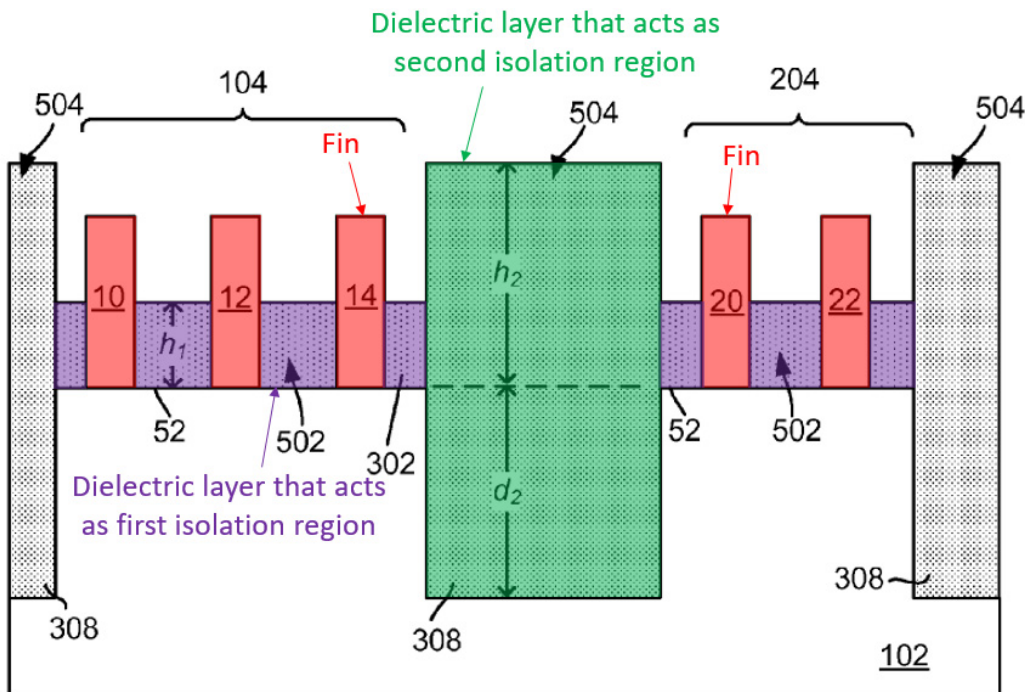
The sections below provide a brief introduction to Akarvardar and its combination with Xie.⁸

1. Akarvardar describes self-aligned isolation regions in FinFET devices

Akarvardar describes “bulk FinFET devices” including “multiple self-aligned isolation regions.” SAMSUNG-1010, 3:46-58; *see* 1:6-9. Akarvardar’s device includes a “first group of fins 104 [that] may include fins 10, 12, and 14” and a “second group of fins 204 [that] may include fins 20 and 22” (red in FIG. 9,

⁸ Petitioner incorporates this discussion into Ground 2.

infra). *Id.*, 4:28-30, FIGS. 1-9. A “first dielectric layer 302” is disposed between fins and acts as “first isolation region[s] 502,” purple, that “electrically separate[s] each individual fin of the first and second group of fins.” *Id.*, 5:65-6:3, 7:36-38, 7:63-65, FIGS. 2-9. A “second dielectric layer 308” acts as a “second isolation region 504,” green, that extends into the substrate and “electrically separate[s] the first group of fins 104 from the second group of fins 204.” *Id.*, 7:8-38, 7:64-65, FIGS. 8-9; *see* 6:47-66. “A height and a depth of the second isolation region may be greater than a height and a depth of the first isolation region.” *Id.*, 8:16-19; SAMSUNG-1003, ¶111.



Excerpt from Akarvardar, FIG. 9 (annotated)

Akarvardar's fabrication process involves multiple etch steps to form the second isolation region 504. As shown in FIGS. 5-6, *infra*, in a first etch step, a "dummy material 304" is "removed from the recess 42" that is "between [the] two groups of fins and above the first dielectric layer 302," thus exposing "a portion of the first dielectric layer 302 positioned between ... the first group of fins 104 and the second group of fins 204." SAMSUNG-1010, 5:23-24, 6:33-41. This exposed portion of the first dielectric layer is removed in a second etch step, "expos[ing] the bulk semiconductor substrate." *Id.*, 6:39-46. In a third etch step, "[t]he etch process [] continue[s] to etch the bulk semiconductor substrate 102 to form an extended recess 44." *Id.*, 6:47-51, FIG. 7, *infra*. The result of these multiple etch steps is a self-aligned recess 44 that "may subsequently be used to form a second isolation region" by depositing "a second dielectric layer 308" therein. *Id.*, 6:52-67, FIG. 8, *infra*; SAMSUNG-1003, ¶112.

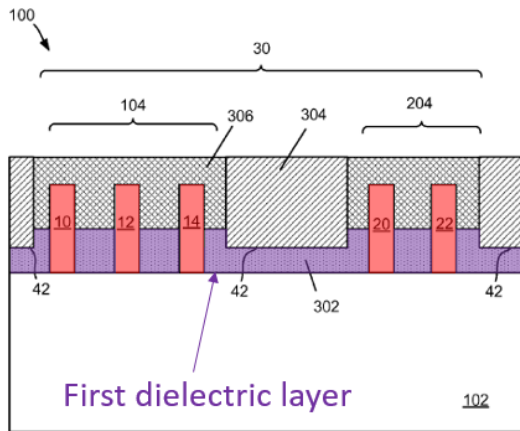


FIG. 5

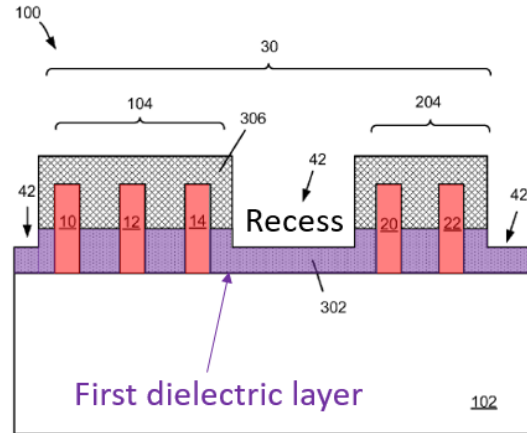


FIG. 6

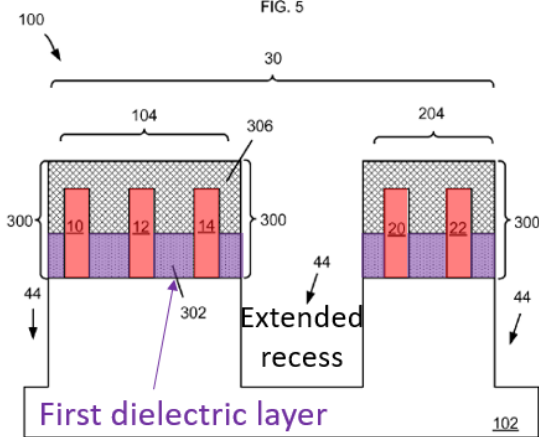


FIG. 7

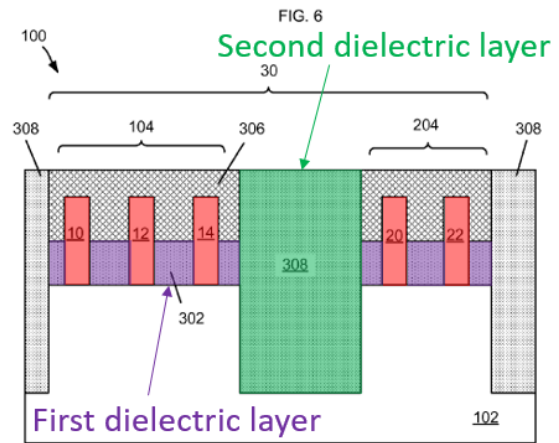


FIG. 8

Excerpts from Akarvardar, FIGS. 5-8 (annotated)

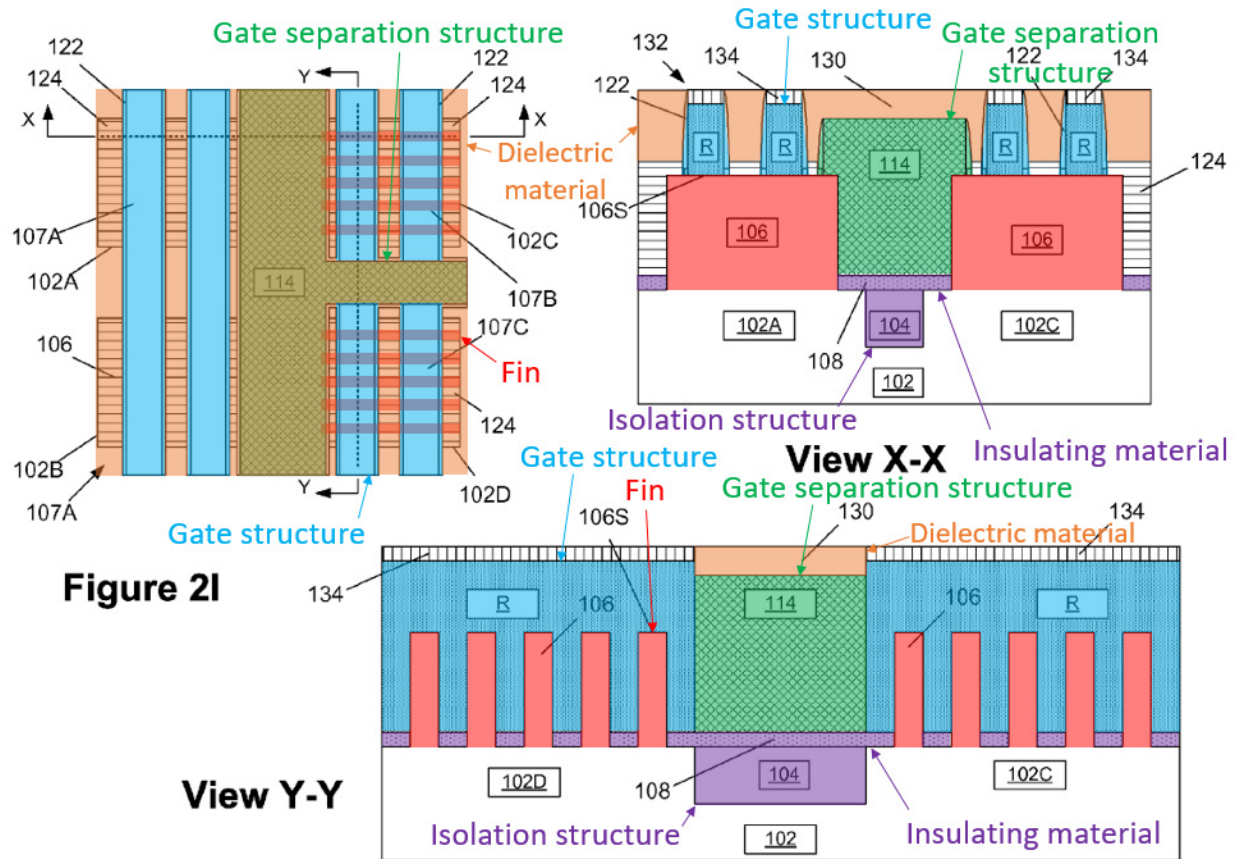
The second dielectric layer 308 deposited in the recess forms the second isolation region 504, which is “self-aligned to the first group of fins 104 and the second group of fins 204.” SAMSUNG-1010, 7:57-59; *see* 7:8-10, FIG. 9. This configuration provides “enhanced device isolation and additional protection” to “subsequently formed FinFET device[s].” *Id.*, 8:9-22. For instance, “the first group of fins 104 may be part of a subsequently formed p-FET device and the second group of fins 204 may be part of a subsequently formed n-FET device” that

are electrically isolated from one another by the second isolation region 504. *Id.*, 7:65-8:2; SAMSUNG-1003, ¶113.

2. Xie describes FinFET devices having gate separation structures

Xie describes “methods ... for forming gate structures for FinFET devices and resulting devices.” SAMSUNG-1004, [0027]. One such FinFET structure, illustrated FIG. 2I, *infra*, includes a substrate having “active regions 102A-D” defined by “isolation structures 104,” purple. SAMSUNG-1004, [0028]. “[A] plurality of fins 106,” some of which are highlighted in red, are formed in the substrate.⁹ *Id.* An insulating material 108, purple, “remains in the bottom of the trenches” between the fins “to locally isolate the fins 106 from one another.” *Id.*, [0028]; SAMSUNG-1003, ¶114.

⁹ The fins 106 are obscured by the epi semiconductor layer 124 in the top view. SAMSUNG-1004, [0035]. The exposed fins can be seen, *e.g.*, in FIG. 2A. SAMSUNG-1003, ¶115.



Excerpt from Xie, FIG. 2I (annotated)

Gate structures, blue, are disposed over the fins. *See* SAMSUNG-1004, [0016]-[0018], [0038]. Each gate structure is “a stack of material layers” “formed using either gate-first or gate-last techniques.” *Id.*, [0017], [0030]; *see* claims 4-5; SAMSUNG-1003, ¶116.

A “gate separation structure 114,” green, is “positioned between the first and second spaced-apart gate structures” and over the insulating material 108. SAMSUNG-1004, [0017], [0032]. A “layer of insulating material 130,” orange, is

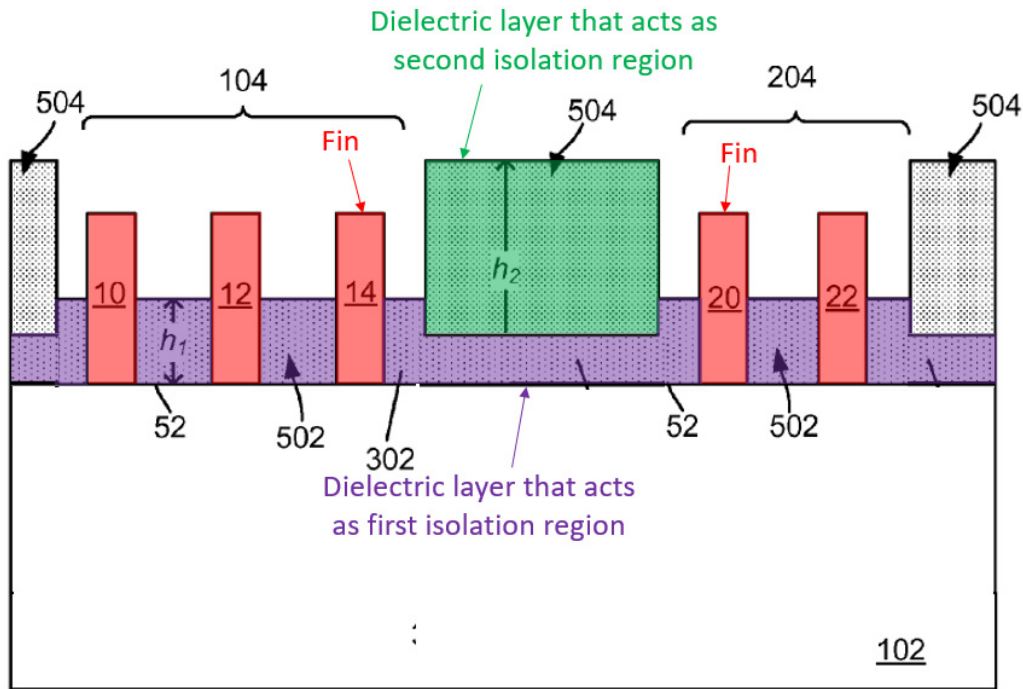
“blanket-deposited” onto the structure. SAMSUNG-1004, [0036]; *see* FIG. 2I; SAMSUNG-1003, ¶117.

3. The Akarvardar-Xie combination

The self-aligned isolation region in the Akarvardar-Xie combination

In the Akarvardar-Xie combination, illustrated *infra*, fins (red) are “formed from a bulk semiconductor substrate,” as taught by Akarvardar. SAMSUNG-1010, 3:61-63, FIGS. 1-9. A “first isolation region 502” (purple) is made from a “first dielectric layer 302” disposed in the space around the base of the fins, and “electrically separate[s] the fins 30 from one another.” *Id.*, 7:35-37, 7:63-65, FIGS. 2-9; SAMSUNG-1003, ¶118.

A self-aligned “second isolation region” (green) is made from a “second dielectric layer 308” that is disposed “between ... the first group of fins 104 and the second group of fins 204” and “electrically separate[s]” the two groups of fins. SAMSUNG-1010, 6:39-41, 6:64-65, 7:8-10, 7:64-65; SAMSUNG-1003, ¶119. Based on Xie, this second isolation region is disposed on the first dielectric layer 302, *e.g.*, it does not extend into the substrate. *See* SAMSUNG-1004, [0031]-[0032], [0039]-[0041], FIGS. 2C-2I (showing a fabrication process in which the gate separation structure is formed on insulating material 108); SAMSUNG-1003, ¶119.



Akarvardar-Xie cross-sectional composite figure

In the combination, this configuration is implemented using a simplified version of Akarvardar's fabrication process to achieve the structural design taught by Xie. SAMSUNG-1003, ¶120. As described by Akarvardar, a recess 42 is opened by removing dummy material 304 from the recess, exposing a "portion of the first dielectric layer 302 positioned between ... the first group of fins 104 and the second group of fins 204" at the bottom of the recess. *See* SAMSUNG-1010, 5:23-24, 6:33-41, FIGS. 5-6; SAMSUNG-1003, ¶120. Akarvardar's second dielectric layer 308 then is deposited into that recess, *e.g.*, onto the exposed portion of the first dielectric layer 302. *See* SAMSUNG-1010, 6:64-66; *see* SAMSUNG-1004, [0032], FIGS. 2C-2D (illustrating formation of the gate separation structure

114 in an opening 112, with insulating material 108 exposed at the bottom of the opening); SAMSUNG-1003, ¶120. Akarvardar's further etch steps to remove the portion of the first dielectric layer and to etch a recess into the substrate (*see* SAMSUNG-1010, 6:39-51) are eliminated. SAMSUNG-1003, ¶120.

As discussed further below, a POSITA would have recognized several benefits of eliminating etch steps from Akarvardar's manufacturing (*e.g.*, improved manufacturing efficiency/cost) to achieve the known structure for gate separation described by Xie. SAMSUNG-1003, ¶¶125-133. Indeed, as Dr. Liu explains, a POSITA would have viewed etch depth (and corresponding isolation structure depth) as a matter of obvious design choice that a POSITA would have considered in evaluating Akarvardar's process in view of Xie's structural design. *Id.* Because Xie describes a known design where the isolation structure between gates does not extend into the substrate and is, instead, located on a dielectric layer on top of the substrate, and because Akarvardar describes a process that would enable formation of Xie's structure (*e.g.*, by depositing Akarvardar's self-aligned isolating dielectric at the step illustrated by Akarvardar's FIG. 6), a POSITA would have found it obvious to simplify Akarvardar's process to achieve the known structure taught by Xie, as discussed and illustrated above. *Id.*

A cross-sectional diagram of a semiconductor device. The diagram shows a substrate with a purple dielectric layer (labeled 302) acting as a first isolation region. On top of this is a blue gate structure (labeled 104 and 204) with a height h_1 . Within the gate structure, there is a green dielectric layer (labeled 504) acting as a second isolation region, with a height h_2 . Red fins (labeled 10, 12, 14, 20, 22) are embedded in the substrate. The top surface is covered by an orange insulating material (labeled 504). The diagram is labeled with 'x direction' and 'y direction' (indicated by a circle with a dot). The number 102 is in the bottom right corner.

66

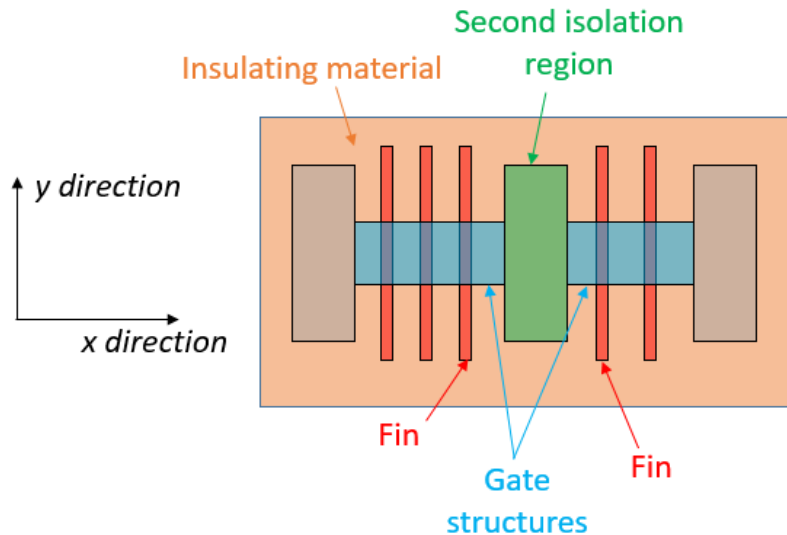
Based on Xie, the gate structures are “spaced-apart gate structures,” with the modified second isolation region (green) disposed between the edges of the two gate structures. *See* SAMSUNG-1004, [0017]; SAMSUNG-1003, ¶122. The second isolation region electrically separates the two gates, consistent with its role in Akarvardar’s structure. *See* SAMSUNG-1010, 8:1-4 (“p-FET and n-FET devices may be electrically separated by the second isolation region”), 7:66-8:4; SAMSUNG-1003, ¶122.

A “layer of insulating material 130,” orange, is “blanket-deposited” onto the gate structures and the modified second isolation region, as taught by Xie. SAMSUNG-1004, [0036]; SAMSUNG-1003, ¶123.

The composite figure *infra* is a schematic top view of elements of the Akarvardar-Xie structure.¹⁰ In the combination, the fins extend in the y-direction, and the gates extend orthogonal to the length of the fins (the x-direction). *See* SAMSUNG-1010, FIG. 9; SAMSUNG-1004, [0027], Fig. 2I; SAMSUNG-1003,

¹⁰ The top view composite figure is for illustration only and is not to scale. For instance, the extent of the long axis of the fins, the extent of the second isolation region 504, and the width of the gate structures in the y-direction are not necessarily as illustrated. SAMSUNG-1003, ¶124.

¶124. The insulating material is disposed over the top of illustrated structure. See SAMSUNG-1004, [0036]; SAMSUNG-1003, ¶124.



Akarvardar-Xie top-view composite figure

4. Reasons to combine Akarvardar and Xie

A POSITA would have been motivated to implement the Akarvardar-Xie combination for at least the following reasons. SAMSUNG-1003, ¶¶125-142.

Arrangement of Akarvardar's second isolation region on the first dielectric layer

In the combination, the configuration of Akarvardar's second isolation region 504 is modified based on Xie such that the second isolation region is disposed on the first dielectric layer 302. SAMSUNG-1003, ¶¶118-120. A POSITA would have been motivated to pursue this implementation for at least the following reasons. *Id.*, ¶¶126-133.

First, the number of process steps involved in forming a second isolation region on Akarvardar's dielectric layer is reduced as compared to Akarvardar's unmodified fabrication process. SAMSUNG-1003, ¶127. Akarvardar describes three etch steps to form the second isolation region: a first etch to remove dummy material (*see* SAMSUNG-1010, 5:23-24, FIGS. 5-6); a second etch to remove a portion of the first dielectric layer (*see id.*, 6:39-46, FIGS. 6-7); and a third etch to form an extended recess in the substrate (*see id.*, 6:47-51, FIG. 7). SAMSUNG-1003, ¶127. The modified second isolation region of the combination is formed using only the first etch to remove the dummy material. *Id.* A POSITA would have recognized the advantages of this processing change, *e.g.*, efficiency and time and cost savings, and would have been motivated to pursue this implementation to achieve these advantages. *Id.*

Second, a POSITA would have recognized that the self-alignment of Akarvardar's second isolation region would be maintained in the combination. *See* SAMSUNG-1010, 3:51-56, 7:57-58, 8:9-22; claims 2, 10; SAMSUNG-1003, ¶128. A POSITA, recognizing the advantages of self-aligned isolation structures, would have been motivated to pursue an approach in which these advantages are maintained even with a simpler fabrication process. *See* SAMSUNG-1010, 8:23-28 (describing that with a self-aligned second isolation region, "the use of additional masks to define the isolation regions may not be required hence

reducing bulk FinFET manufacturing costs”); SAMSUNG-1009, [0056]; SAMSUNG-1003, ¶128. To the extent there is a reduction in the electrical isolation capability of the modified second isolation region because it no longer extends into the underlying substrate, a POSITA nevertheless would recognize that some isolation benefit is still obtained, and would weigh the advantages of the simplified fabrication process against the potential reduction in isolation capability. *Id.*; see *Winner Int’l Royalty Corp. v. Wang*, 202 F.3d 1340, 1349 n.8 (Fed. Cir. 2000) (“The fact that the motivating benefit comes at the expense of another benefit...should not nullify its use as a basis to modify the disclosure of one reference with the teachings of another.”); *In re Urbanski*, 809 F.3d 1237, 1244 (Fed. Cir. 2016); *Medichem, S.A. v. Rolabo, S.L.*, 437 F.3d 1157, 1165 (Fed. Cir. 2006) (holding that “[a] given course of action often has simultaneous advantages and disadvantages, and this does not necessarily obviate motivation to combine.”).

Third, a POSITA would have been motivated to pursue this modification to Akarvardar’s structure because Xie discloses a generally similar structure with an isolation structure that does not extend into the substrate. See SAMSUNG-1004, FIG. 2I, [0028]-[0032]; SAMSUNG-1003, ¶129. Akarvardar’s process that would enable the fabrication of the structure described by Xie. A POSITA would have been motivated to consider the parameters of Xie’s design, *e.g.*, the depth and height of Xie’s isolation structure, as design considerations when implementing

Akarvardar's process, *e.g.*, to simplify Akarvardar's fabrication process.

SAMSUNG-1003, ¶129.

Fourth, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, gate isolation structures that do not extend into the underlying substrate) to a known structure (*e.g.*, a FinFET integrated circuit structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit having a gate isolation structure disposed on a layer of dielectric material on the substrate). SAMSUNG-1003, ¶130; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because the Akarvardar-Xie isolation region would retain, at least to some extent, the electrical isolation benefits provided by Akarvardar's unmodified second isolation region. *See* SAMSUNG-1010, 8:16-20; SAMSUNG-1003, ¶131. Xie demonstrates that isolation regions between gates provide electrical isolation even when the isolation regions do not extend into the substrate. *See* SAMSUNG-1004, [0032], [0035]; SAMSUNG-1003, ¶131. Akarvardar also describes that its second isolation region provides "additional protection during subsequent processing steps, including CMP." SAMSUNG-1010, 8:16-22. Because the height of the second isolation region is not modified in the combination, a POSITA would have expected the

second isolation region in the combination to retain these physical protection advantages. SAMSUNG-1003, ¶131.

Additionally, a POSITA would have expected success because Akarvardar indicates that the etching of the first dielectric layer and substrate to form the extended recess are optional: “a portion of the first dielectric layer 302 positioned between two groups of fins ... *may be removed*,” and “[t]he etch process *may continue to etch the bulk semiconductor substrate* 102 to form an extended recess.” SAMSUNG-1010, 6:39-51; SAMSUNG-1003, ¶132. Indeed, the structure of the Akarvardar-Xie combination is generally of a similar configuration to the interim Akarvardar structure of Akarvardar’s FIG. 4. SAMSUNG-1003, ¶132.

A POSITA also would have expected success given that FinFET devices having gate isolation structures that do not extend into the underlying substrate were well-known. *See* SAMSUNG-1004, [0032], FIG. 2I; SAMSUNG-1009, [0056], FIG. 18a; SAMSUNG-1012, Abstract; SAMSUNG-1003, ¶133.

Incorporation of gate structures

A POSITA would have been motivated to incorporate gate structures into the Akarvardar-Xie integrated circuit structure for at least the following reasons. SAMSUNG-1003, ¶¶134-137.

First, a POSITA would have been motivated to pursue this implementation to follow Akarvardar's direction to use its structure with "subsequently formed FinFET device[s]." SAMSUNG-1010, 8:19; SAMSUNG-1003, ¶135. Indeed, a POSITA would have recognized gate structures as standard features of FinFET devices. *See* SAMSUNG-1009, [0036]; SAMSUNG-1005, 3:4-12, 5:5-42; SAMSUNG-1004, [0016]-[0018], [0038]; SAMSUNG-1006, [0038]-[0039]; SAMSUNG-1007, 4:65-5:9; SAMSUNG-1003, ¶135.

Second, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, gate structures in an integrated circuit device) to a known structure (*e.g.*, a FinFET integrated circuit structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit having gate structures). SAMSUNG-1003, ¶136; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because gate structures are part of the "subsequently formed FinFET device[s]" to be made from Akarvardar's structures. SAMSUNG-1010, 8:19-22; *see* 7:64-8:4; SAMSUNG-1003, ¶137. Indeed, Akarvardar explicitly contemplates the formation of "gate structures." SAMSUNG-1010, 8:21. A POSITA also would have expected success given that the use of gate structures in FinFET-based devices, was well-known. *See* SAMSUNG-1009, [0036]; SAMSUNG-1005, 3:4-12, 5:5-42; SAMSUNG-1004,

[0016]-[0018], [0038]; SAMSUNG-1006, [0038]-[0039]; SAMSUNG-1007, 4:65-5:9; SAMSUNG-1003, ¶137.

Incorporation of an interlayer dielectric

A POSITA would have been motivated to incorporate an interlayer dielectric (ILD) into the Akarvardar-Xie integrated circuit structure for at least the following reasons. SAMSUNG-1003, ¶¶138-142.

First, a POSITA would have been motivated to incorporate an ILD to provide electrical isolation between the “subsequently formed FinFET device[s]” and overlying interconnect structures. SAMSUNG-1010, 7:65-8:2, 8:19-22; *see* SAMSUNG-1008, [0068]; SAMSUNG-1017, 6:42-44; SAMSUNG-1039, 9:5-8; SAMSUNG-1003, ¶139. The presence of an ILD would enable the FinFET devices envisioned by Akarvardar to be connected to upper-level wiring. *See* SAMSUNG-1010, 7:65-8:2, 8:19-22; SAMSUNG-1008, [0068]; SAMSUNG-1003, ¶139.

Second, a POSITA would have been motivated to incorporate an ILD because the use of ILDs above transistor-level structures was a standard element of integrated circuits. *See* SAMSUNG-1004, [0036], FIG. 2I; SAMSUNG-1009, [0051], FIGS. 15A-18D; SAMSUNG-1007, 5:15-17, FIGS. 5A-5C; SAMSUNG-1008, [0068], FIG. 5; SAMSUNG-1017, 6:42-44, FIG. 5; SAMSUNG-1039, 9:1-8, FIG. 3F; SAMSUNG-1003, ¶140.

Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, ILD in an integrated circuit device) to a known structure (*e.g.*, a FinFET integrated circuit structure) to yield predictable results (*e.g.*, a FinFET-based integrated circuit having an ILD). SAMSUNG-1003, ¶141; *see KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because an ILD is compatible with the further device structure and processing described by Akarvardar. *See* SAMSUNG-1010, 8:19-22 (“subsequent processing steps, including CMP of gate structures and epi isolation”); SAMSUNG-1003, ¶142. A POSITA also would have expected success given that the use of ILDs in FinFET-based devices was well-known. *See* SAMSUNG-1004, [0036], FIG. 2I; SAMSUNG-1009, [0051], FIGS. 15A-18D; SAMSUNG-1007, 5:15-17, FIGS. 5A-5C; SAMSUNG-1008, [0068], FIG. 5; SAMSUNG-1017, 6:42-44, FIG. 5; SAMSUNG-1039, 9:5-8, FIG. 3F; SAMSUNG-1003, ¶142.

5. The Akarvardar-Xie gate structures each includes a gate dielectric layer and a gate electrode

Based on Xie, the gate structures in the Akarvardar-Xie combination include “a stack of material layers” including “a high-k ... gate insulation layer,” “one or more metal layers,” and “a bulk conductive metal layer.” SAMSUNG-1004, [0038], claim 1; *see* claim 5, [0015]-[0016], [0040]; SAMSUNG-1003, ¶143. To

the extent Xie does not explicitly disclose gate structures each having a gate dielectric layer and a gate electrode, a POSITA would have found this configuration obvious, as discussed in the following paragraphs. SAMSUNG-1003, ¶143.

It was well-known for a gate structure in a FinFET device to include a gate dielectric layer (*e.g.*, a high-k gate dielectric layer) and a gate electrode (*e.g.*, a metal gate electrode). *See, e.g.*, SAMSUNG-1005, 8:67-9:4, 5:5-46, FIGS. 2 and 5A; SAMSUNG-1025, 4:39-5:3, Fig. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-48; SAMSUNG-1013, 3:45-46; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0041], [0046]-[0047]; SAMSUNG-1003, ¶144.

In view of the state of the art and given the composition of Xie's gate structures (*see* SAMSUNG-1004, [0038], [0015]-[0016], [0040], claims 1 and 5), a POSITA would have understood or found obvious that the "stack of material layers" of the Akarvardar-Xie gate structures includes a gate dielectric layer (*e.g.*, Xie's high-k gate insulation layer) and a gate electrode (*e.g.*, Xie's bulk conductive metal layer). SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶145.

A POSITA would have been motivated to implement Xie's "high-k ... gate insulation layer" and "bulk conductive metal layer" as a high-k gate dielectric layer

and metal gate electrode in the combination, respectively, for at least the following reasons. SAMSUNG-1003, ¶¶146-150.

First, gate structures having high-k gate dielectric layers and metal gate electrodes were standard elements of FinFET transistors. *See, e.g.*, SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1011, 3:59-4:10; *see* SAMSUNG-1001, 3:49-4:49; SAMSUNG-1003, ¶147. The implementation of Xie's gate insulation layer and bulk conductive material layer as a gate dielectric layer and gate electrode, respectively, is thus merely a comprehensive implementation of a structure already described by Xie. SAMSUNG-1003, ¶147.

Second, a POSITA would have been motivated to use a high-k gate dielectric layer and a metal gate electrode to obtain performance advantages afforded by these materials, *e.g.*, decreased threshold voltage, reduced fringe capacitance, and suppressed leakage current. *See* SAMSUNG-1011, 1:32-35; SAMSUNG-1026, Abstract; SAMSUNG-1027, 1:38-46; SAMSUNG-1028, Abstract; SAMSUNG-1003, ¶148. Moreover, the use of a high-k gate dielectric layer provides finer control over the channel potential, enabling more effective on/off control to be achieved, thus facilitating higher speed performance. *See* SAMSUNG-1028, Abstract; SAMSUNG-1003, ¶148.

Third, a POSITA would have been prompted to pursue this implementation because doing so is merely the application of known techniques (*e.g.*, high-k gate

dielectric layers and metal gate electrodes) to a known structure (*e.g.*, a FinFET gate structure) to yield predictable results (*e.g.*, a gate structure having a high-k gate dielectric layer and a metal gate electrode). SAMSUNG-1003, ¶149; *see KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have expected success because high-k gate dielectric layers and metal gate electrodes are consistent with the composition of Xie's gate structures. *See* SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶150. A POSITA also would have expected success because these materials are well-known elements of FinFET gate structures. *See* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025, 4:39-5:3, FIG. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-54; SAMSUNG-1013, 3:45-46; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0041], [0046]-[0047]; SAMSUNG-1003, ¶150.

6. Analysis

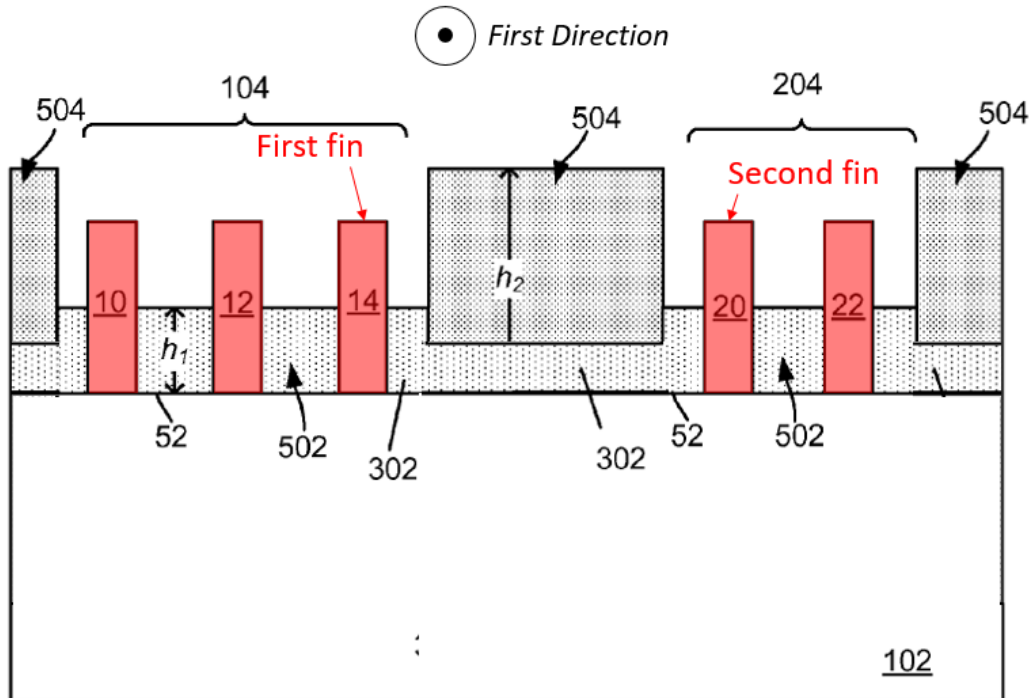
(1) Claim 21

Limitation [21pre]

To the extent the preamble is deemed to be limiting, the Akarvardar-Xie combination renders it obvious. Akarvardar indicates that its structure is for use with "FinFET device[s]." SAMSUNG-1010, 8:19; *see* 1:6-9, FIGS. 1-9; SAMSUNG-1004, FIGS. 2A-2I; SAMSUNG-1003, ¶151.

Limitations [21a] and [21b]

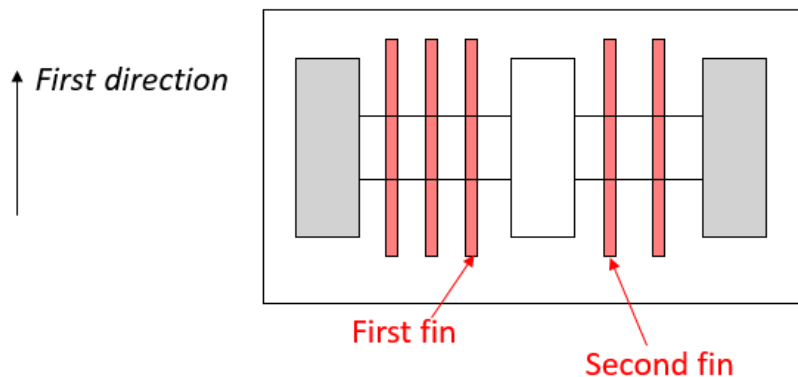
The Akarvardar-Xie combination includes **first and second fins**, *e.g.*, Akarvardar's fins 14, 20, red in the figures *infra*. See SAMSUNG-1010, 4:23-31 ("The fins 30 may include a first group of fins 104 and a second group of fins 204. ... the first group of fins 104 may include 10, 12, 14 and the second group of fins 204 may include fins 20 and 22"), 2:15-18, 2:39-44, 3:61-63, 4:32-46, FIGS. 1-9; SAMSUNG-1003, ¶152.



Akarvardar-Xie cross-sectional figure

In the combination, each fin has **a longest dimension along a first direction**, into the page in the cross-sectional view *supra* and top to bottom in the top view *infra*. To the extent that Akarvardar does not explicitly state this, a

POSITA would have understood this to be the case given that it was well-known for fins in FinFET devices to be elongated in one direction. *See, e.g.*, SAMSUNG-1004, [0027], FIG. 2A; SAMSUNG-1006, [0036], FIG. 11; SAMSUNG-1007, 2:14-25, FIGS. 1A-1C; SAMSUNG-1005, 3:4-15, FIG. 2; SAMSUNG-1003, ¶153. This longest dimension is **along the first direction**: the longest dimension of the fins is traversed *as one moves along the fins in the first direction*. SAMSUNG-1003, ¶153.



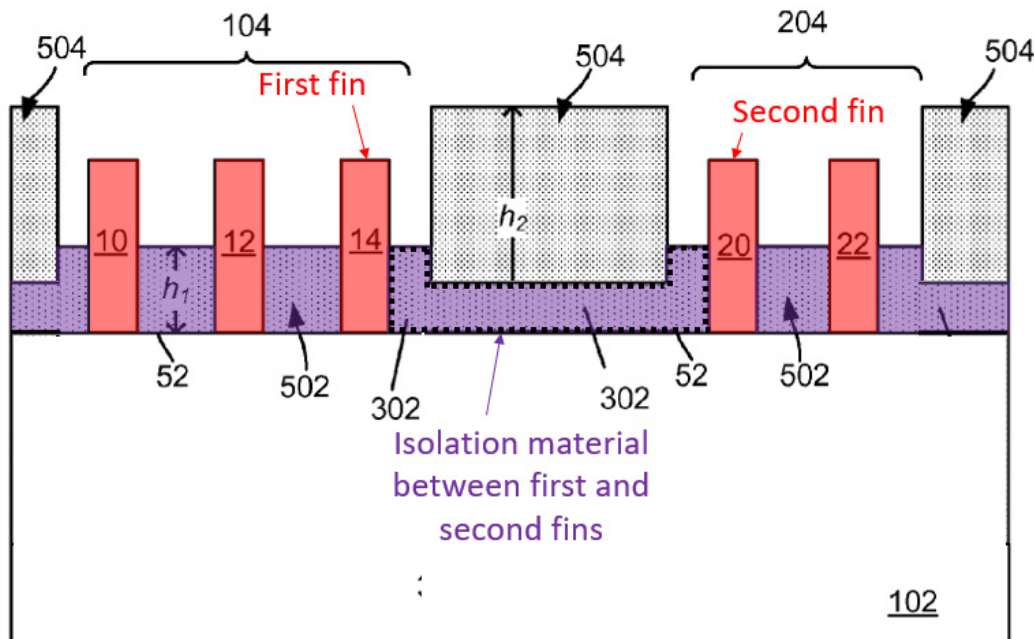
Akarvardar-Xie top-view figure

Also in the combination, Akarvardar describes **forming the fins**. *See* SAMSUNG-1010, 4:4-7 (“The fins 30 may be patterned and formed from the bulk semiconductor substrate 102 by any suitable method”), 2:15-18 (“forming a first group of fins and a second group of fins in a bulk semiconductor substrate”), 2:39-44, FIG. 1; SAMSUNG-1003, ¶154.

Moreover, in the combination, **the fins comprise silicon**. Akarvardar describes that the fins are formed from “*a bulk silicon substrate.*” SAMSUNG-1010, 3:62-65; *see* 3:64-4:8, FIG. 1; SAMSUNG-1003, ¶155.

Limitation [21c]

The Akarvardar-Xie combination includes **an isolation material**, *e.g.*, Akarvardar’s “*first dielectric layer 302.*” purple in the figure *infra*. SAMSUNG-1010, 7:36-38; *see* 4:59-67 (“a first dielectric layer 302 may be deposited on the semiconductor structure”), 2:18-27, 2:2-5, 5:65-6:3, 7:63-65, FIGS. 2-9; SAMSUNG-1003, ¶156.



Akarvardar-Xie figure

In the combination, the dielectric material 302 is **an isolation material** because it provides electrical isolation between fins: “the semiconductor structure

100 may include a first isolation region 502 made from the first dielectric layer 302,” where “[t]he first isolation region 502 may *electrically separate the fins 30 from one another.*” SAMSUNG-1010, 7:35-37, 63-64; *see* 8:9-14 (“The first isolation region may be located between each individual fin of a determined group of fins to electrically isolate each fin from one another”), 2:2-4; SAMSUNG-1003, ¶157.

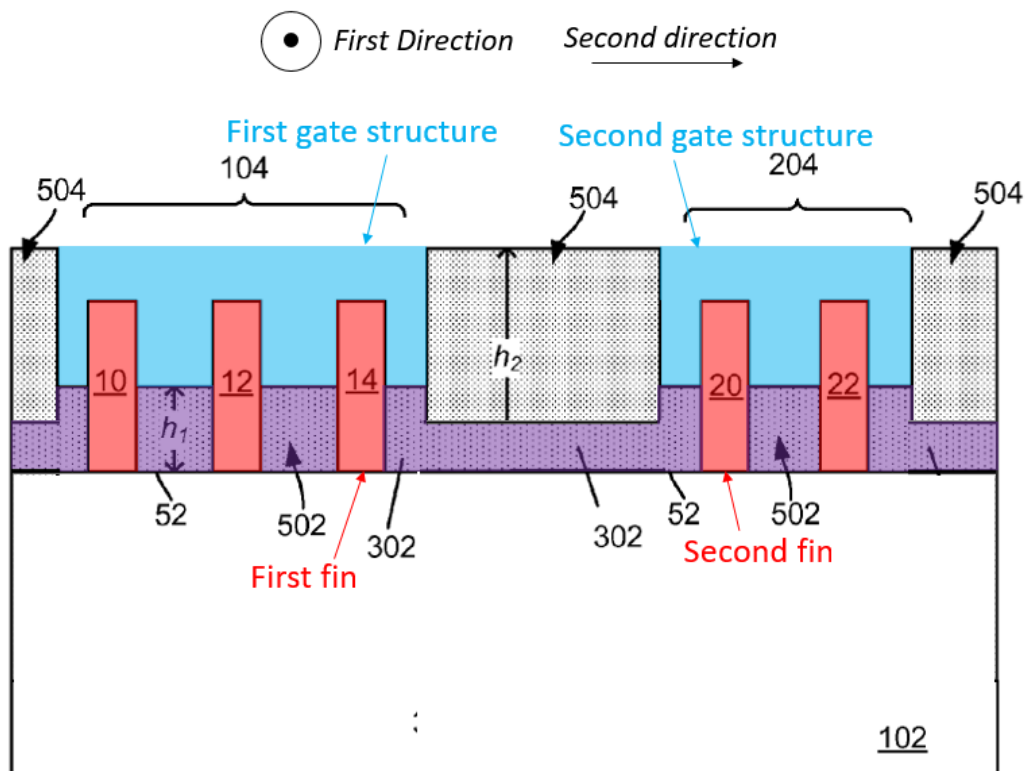
Specifically, Akarvardar describes depositing the first dielectric layer 302 between the fins, and then removing a portion of the first dielectric layer 302 to expose upper portions of the fins. *See* SAMSUNG-1010, 5:18-20 (“the first dielectric layer 302 may be conformally deposited between two groups of fins, such as the first and second group of fins 104, 204”), 5:4-14, 5:47-61, 8:10-14, FIGS. 2-6; SAMSUNG-1003, ¶158. Although Akarvardar describes later removing the portion of the first dielectric layer between the fins (*see* SAMSUNG-1010, 6:39-41), in the Akarvardar-Xie combination, this portion of the first dielectric layer (outlined in dashed lines *supra*) is not removed, based on Xie. *See* §IV.B.3. SAMSUNG-1003, ¶158.

The isolation material (*e.g.*, the outlined portion of the first dielectric layer) is “positioned between ... the first group of fins 104 and the second group of fins” (SAMSUNG-1010, 6:39-41), *i.e.*, **between the first fin and the second fin** (*e.g.*, in the space separating the fins. SAMSUNG-1003, ¶158.

Limitations [21d] and [21e]

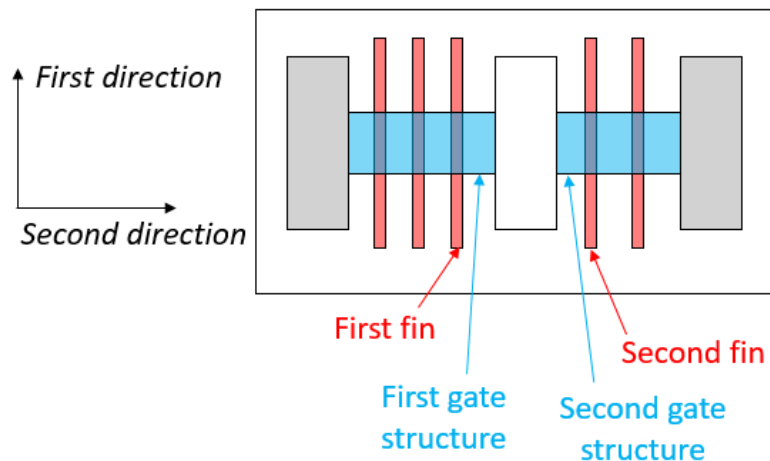
The Akarvardar-Xie combination includes first and second gate structures

The Akarvardar-Xie combination includes **first and second gate structures**, e.g., based on Xie’s “**final gate structures**,” blue in the figures *infra*. SAMSUNG-1004, [0030]; SAMSUNG-1003, ¶159. Based on Xie, the gate structures are disposed on opposing sides of the modified second isolation region 504 of the combination. See SAMSUNG-1004, [0017] (“**first and second spaced-apart gate structures**”), [0002], [0013]-[0016], [0027], [0040]-[0041], FIG. 2I, FIGS. 2K-2O; claims 1, 5, 9, 11, 16; SAMSUNG-1003, ¶159.



Akarvardar-Xie figure

Based on Xie, the gate structures have **a longest dimension along a second direction**: the longest dimension of the gate structures is traversed *as one moves along the gate structures in the second direction* (left to right in the cross-sectional and top views). See SAMSUNG-1004, FIG. 2I; SAMSUNG-1003, ¶160.

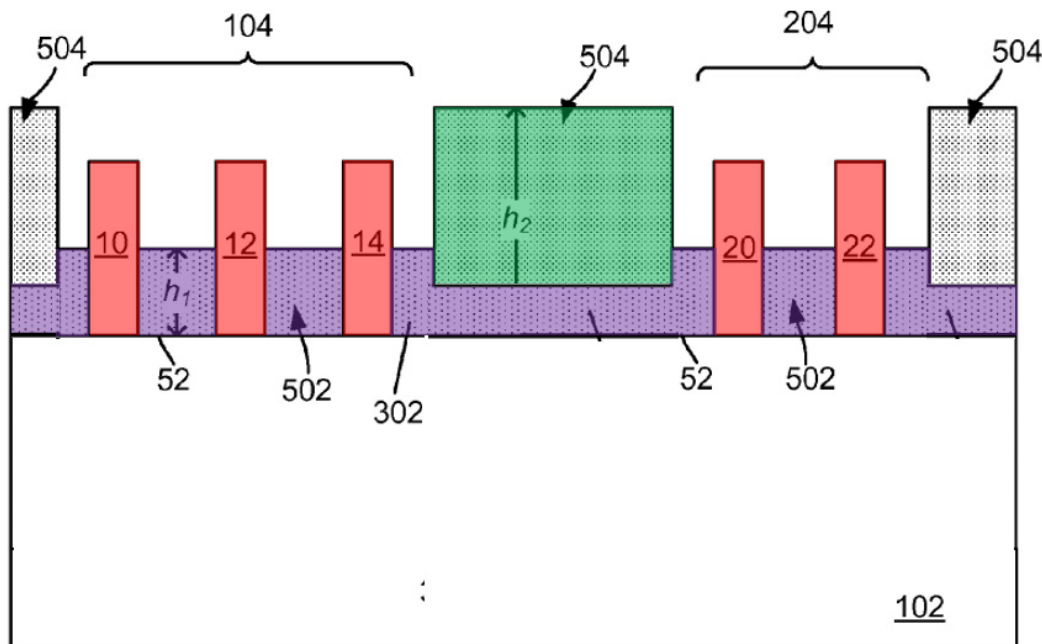


Akarvardar-Xie figure

In the combination, **the second direction is orthogonal to the first direction**, *e.g.*, the gate structures extend in a direction orthogonal to the fins, as shown in the figures *supra*. See SAMSUNG-1004, FIG. 2I, SAMSUNG-1010, FIG. 9; SAMSUNG-1003, ¶161. To the extent that this orthogonality is not explicitly stated, a POSITA would have understood this to be the case, or otherwise found this to be obvious, consistent with Xie's FIG. 2I and given that gate structures orthogonal to fins in FinFET devices was well-known. See, *e.g.*, SAMSUNG-1008, [0053]; SAMSUNG-1029, [0042]; SAMSUNG-1030, Abstract; SAMSUNG-1003, ¶161.

The Akarvardar-Xie gate structures are formed in the recited configuration

In the combination, the **first gate structure is formed over the first fin** and **the second gate structure is formed over the second fin**, as shown in the figure *supra*. Based on Xie, gate structures are formed onto the structure illustrated *infra*. See SAMSUNG-1010, 7:65-8:2, 8:19-22; SAMSUNG-1003, ¶162.

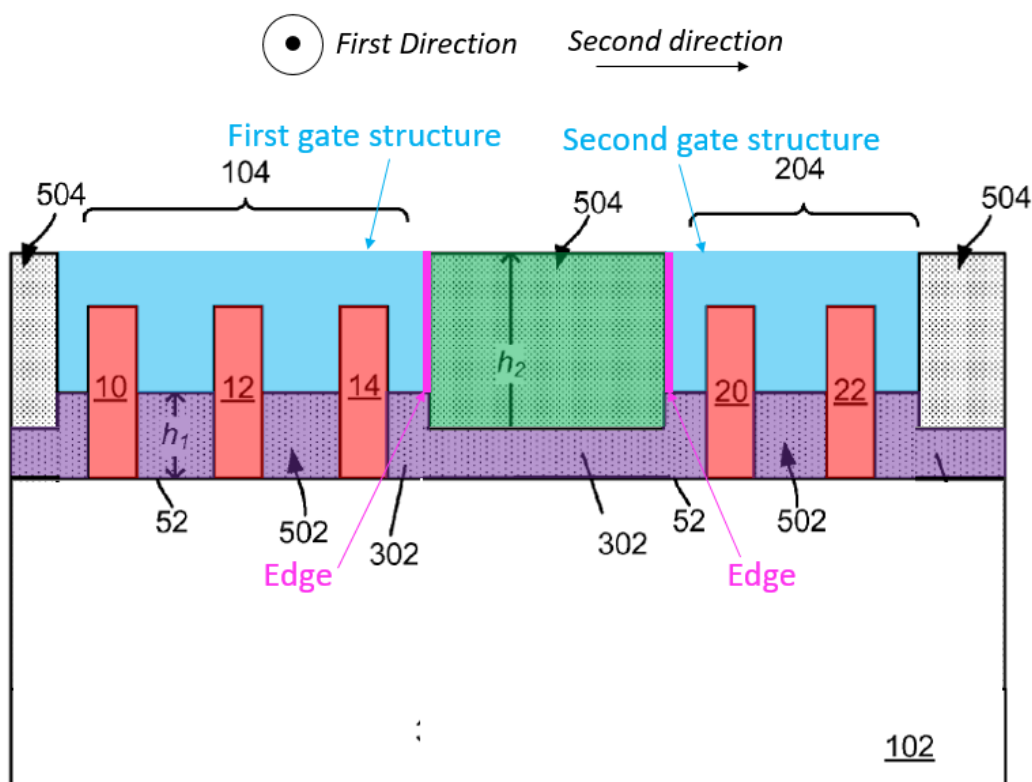


Akarvardar-Xie figure

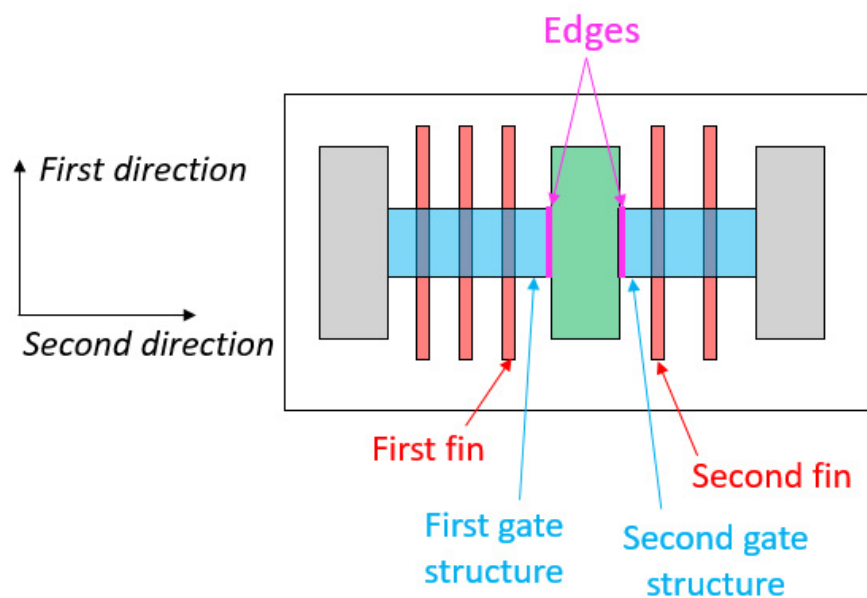
In this structure, the fins are exposed because a previously-deposited protective layer has been removed: “the protective material 306 may be removed selective to the first and second group of fins 104, 204.” SAMSUNG-1010, 7:20-27, FIGS. 8-9. The gate structures are deposited onto these exposed fins and thus are **over** the respective fins, *e.g.*, consistent with Xie. See SAMSUNG-1004, [0016] (“forming a stack of material layers to form *a plurality of gate structures*

above a plurality of spaced-apart active regions defined in a semiconductor substrate, wherein *each of the active regions have at least one fin* formed thereabove”), [0040] (“the stack of materials 140S that will comprise the gate structure 140 (be it a final gate structure or a sacrificial gate structure) are blanket-deposited across all of the active regions”), [0015]-[0018], [0041], FIG. 2I, FIGS. 2K-2O; claims 9, 11, 16; SAMSUNG-1003, ¶162.

Moreover, in the Akarvardar-Xie combination, **the second gate structure is discontinuous with the first gate structure**, as illustrated in the figures *infra*. Consistent with Xie, the gate structures (blue) are **discontinuous** because they are separated by Akarvardar’s modified second isolation region 504 (green; *see* [21f]). *See* SAMSUNG-1004, [0017] (“first and second *spaced-apart gate structures* ..., and a gate separation structure positioned between the first and second spaced-apart gate structures”), [0031]-[0032], [0040]-[0041], [0015]-[0016], [0018], FIG. 2I, FIGS. 2K-2O, claims 1, 9, 11, 16; SAMSUNG-1003, ¶163.



Akarvardar-Xie figure



Akarvardar-Xie figure

The discontinuity is **along the second direction**: the discontinuity is reached *as one moves in the second direction* from one gate structure to the other (left to right in the cross-sectional and top views). See SAMSUNG-1010, FIG. 9; SAMSUNG-1004, FIG. 2I; SAMSUNG-1003, ¶164.

The figures *supra* also illustrate that **the second gate structure has an edge** (outlined in pink) **that faces an edge of the first gate structure** (also outlined in pink), *e.g.*, the edges of the gate structures that contacts modified second isolation region face one another. This arrangement, too, is consistent with Xie. Xie explains that “each of the gate structures has an end surface” (*e.g.*, **an edge**), where “first and second opposing surfaces of the gate separation structure” “abut the end surfaces of first and second spaced-apart gate structures, respectively.” SAMSUNG-1004, [0016]; *see* [0032] (in FIG. 2D, “**the ends 110X** of what will become the sacrificial gate structures 107 abut the horizontal portions 114H of the gate separation structure 114”), [0035], [0040]-[0041], FIG. 2I, FIGS. 2C-2E, FIGS. 2K-2O, claims 1, 11, and 16; SAMSUNG-1003, ¶165.

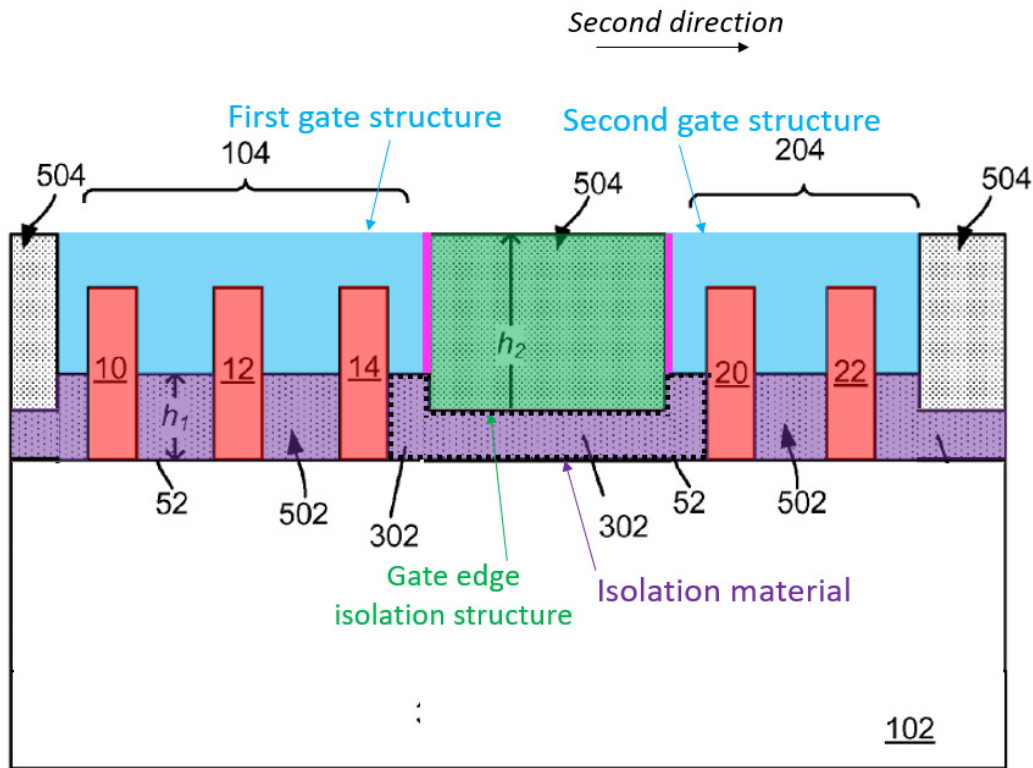
The edges (*e.g.*, end surfaces) of the gate structures face one another **along the second direction**: from the edge of the second gate structure, the edge of the first gate structure is reached *as one moves in the second direction* (left to right in the cross-sectional and top views). SAMSUNG-1003, ¶166.

The Akarvardar-Xie gate structures each includes a gate dielectric layer and a gate electrode

In the combination, the gate structures include “a high-k (k value greater than 10) gate insulation layer,” “one or more metal layers,” and “a bulk conductive metal layer.” SAMSUNG-1004, [0038]; *see* [0030]. As discussed *supra* in §IV.B.5, a POSITA would have understood or found obvious to implement the “gate insulation layer” and “bulk conductive metal layer” (*id.*, [0038]) of Xie’s gate structures as **a gate dielectric layer** and **a gate electrode**, respectively. *See* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1025, 4:39-5:3, FIG. 9A; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1012, 4:46-54; SAMSUNG-1013, 3:45-46; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0041], [0046]-[0047]; SAMSUNG-1003, ¶167.

Limitation [21f]

The Akarvardar-Xie combination includes **a gate edge isolation structure**, green in the figure *infra*, *e.g.*, Akarvardar’s ***second isolation region 504***, modified based on Xie such that it is disposed on the first dielectric layer 302 (*e.g.*, the isolation material, purple) and does not extend into the substrate. *See* SAMSUNG-1010, 6:39-41, 6:64-65, 7:8-10, 7:64-65, FIG. 9; SAMSUNG-1004, [0031]-[0032], [0039]-[0041], FIGS. 2C-2I; §IV.B.3, SAMSUNG-1003, ¶168.



Akarvardar-Xie figure

As discussed in §IV.B.3, in the combination, **the gate edge isolation structure is formed** using a process based on Akarvardar's fabrication process. SAMSUNG-1003, ¶169. A recess is opened in a structure such as that of Akarvardar's FIG. 5, and Akarvardar's second dielectric layer 308 is deposited into that recess, *e.g.*, onto the exposed portion of the first dielectric layer 302, thereby forming the gate edge isolation structure. *See* SAMSUNG-1010, 5:23-24, 6:33-41, 6:64-66, FIGS. 5-6; *see* SAMSUNG-1004, [0032], FIGS. 2C-2D; SAMSUNG-1003, ¶169.

In the combination, Akarvardar's modified second isolation region 504 is a **gate edge isolation structure**: it is a self-aligned structure that is disposed between and in contact with edges of gate structures (discussed *infra*) and isolates those gate structures from one another (*e.g.*, physically and electrically). SAMSUNG-1003, ¶170.

Notably, Akarvardar's modified second isolation region is a ***self-aligned*** structure: "the second isolation region 508 may be formed self-aligned to the first group of fins 104 and the second group of fins 204." SAMSUNG-1010, 7:57-59; *see* 1:6-9, 8:25-28, 1:64-66, 3:51-58, 8:9-11, claim 2; SAMSUNG-1003, ¶171.

Moreover, Akarvardar's modified second isolation region ***physically isolates*** the gate structures such that they are not in physical contact. *See* SAMSUNG-1010, 8:14-16 ("The second isolation region may be located ***between*** two adjacent groups of fins"), 6:59-61, 6:18-20, claims 1 and 5, FIGS. 8-9; SAMSUNG-1003, ¶172.

The modified second isolation region also ***electrically isolates*** the gate structures. Akarvardar describes that "the second isolation region 504 may ***electrically separate*** the first group of fins 104 from the second group of fins 204." SAMSUNG-1010, 7:64-67. More specifically, Akarvardar describes that when the groups of fins are part of subsequently formed FET devices, such "***devices may be electrically separated*** by the second isolation region 504." *Id.*, 7:67-8:4. In the

combination, when gate structures are disposed over the fins to form FET devices (see [21d]-[21e]), these devices (e.g., devices including the gate structures) are thus electrically separated by Akarvardar's modified second isolation region.

SAMSUNG-1003, ¶173.

In the combination, **the gate edge isolation structure** (e.g., Akarvardar's modified second isolation region) **is between and in contact with the edge of the first gate structure and the edge of the second gate structure.** The figures *supra* illustrate this positioning, with the edges of the gate structures outlined in pink. SAMSUNG-1003, ¶174.

Specifically, in the combination, the gate edge isolation structure is **between** the gate structures, as illustrated in the figures. Based on Xie, Akarvardar's modified second isolation region is "*positioned between the first and second spaced-apart gate structures.*" SAMSUNG-1004, [0017]; *see* [0031]-[0032], [0040], [0015]-[0016], [0018], [0041], FIG. 2I, FIGS. 2K-2O, claims 1, 9, 11, 16; SAMSUNG-1010, FIG. 9; SAMSUNG-1003, ¶175. This positioning of the gate edge isolation structure between the gate structures enables Akarvardar's modified second isolation region "electrically separate[]" "p-FET and n-FET devices" formed over the groups of fins. SAMSUNG-1010, 7:66-8:4; SAMSUNG-1003, ¶175.

Additionally, in the combination, the gate edge isolation structure is **in contact with** the edges of the gate structures, as evidenced by the fabrication process for the combination structure. In the combination, the modified second isolation region is formed by depositing “a second dielectric layer 308” into a recess between groups of fins. SAMSUNG-1010, 6:58-65; *see* FIGS. 6-8. A “protective material 306 [is] removed selective to ... the first and second dielectric layers 302, 308,” thus exposing the sidewalls of the second dielectric layer 308, *e.g.*, exposing the sidewalls of the modified second isolation region. SAMSUNG-1003, ¶176. When the gate structures are then deposited on opposite sides of that modified second isolation region, the edges of the gate structures (outlined in pink in the figures *supra*) are **in contact with** those exposed edges of the modified second isolation region (*e.g.*, of the gate edge isolation structure). SAMSUNG-1003, ¶176.

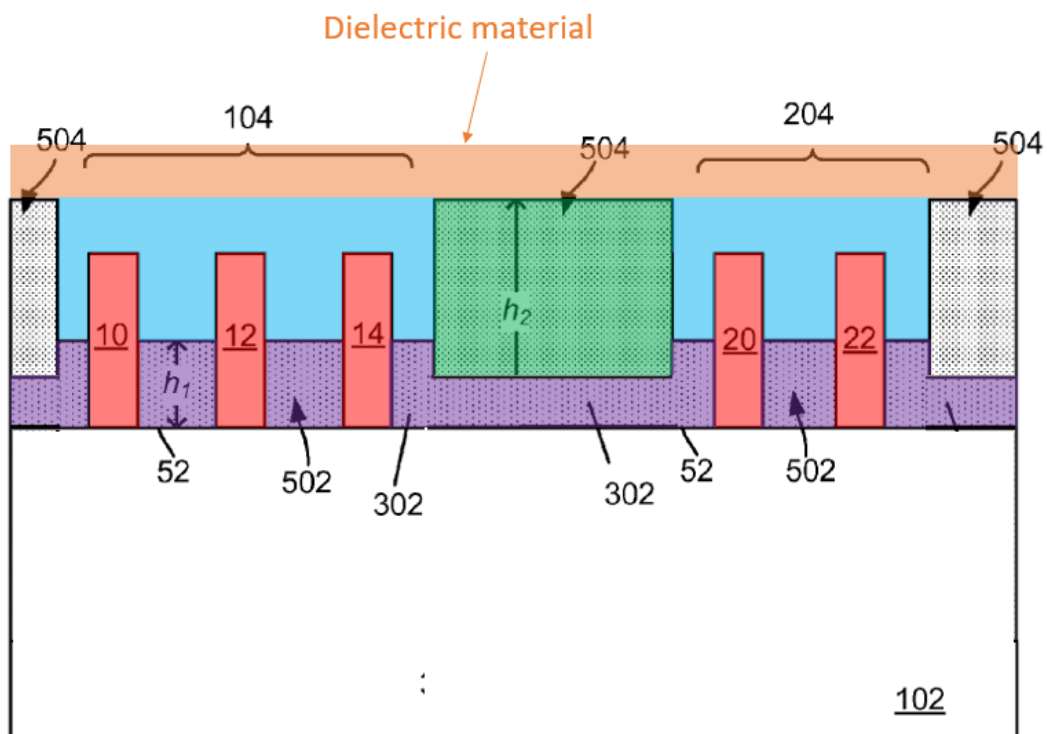
The gate edge isolation structure is between and in contact with the edges of the gate structures **along the second direction: *as one moves in the second direction*** (left to right in the cross-sectional view) starting from the edge of the first gate structure, one reaches first the gate edge isolation structure and then the edge of the second gate structure. SAMSUNG-1003, ¶177.

Furthermore, in the combination, the gate edge isolation structure is **over the isolation material**, as shown in the figures *supra*. As discussed in §IV.B.3, in the

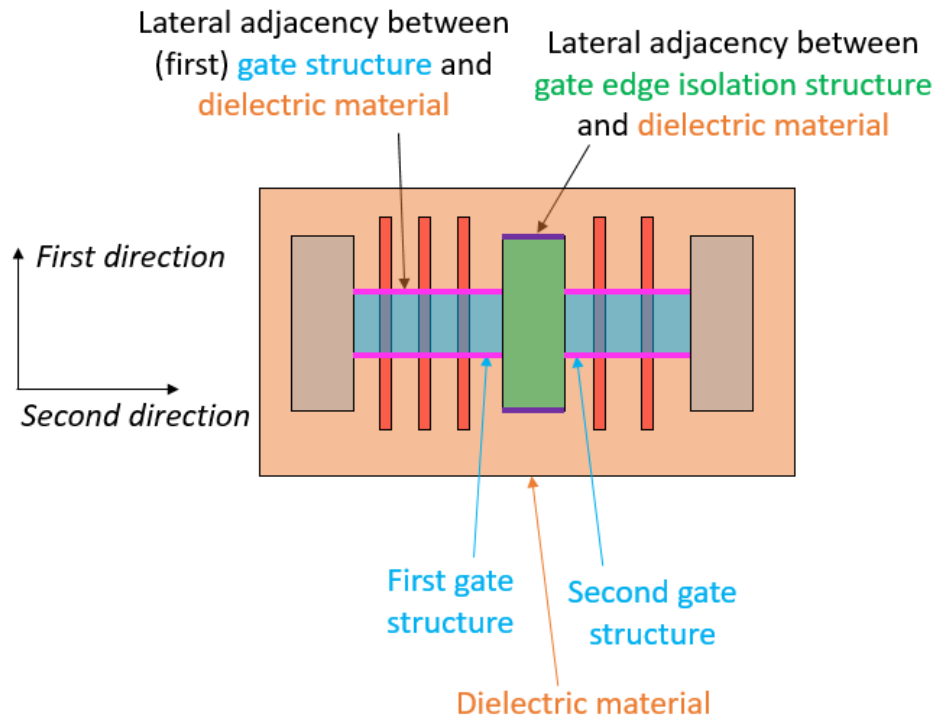
Akarvardar-Xie combination, the modified second isolation region 504 is disposed directly on the first dielectric layer 302 (*e.g.*, the isolation material, purple), consistent with Xie's teachings of a gate edge isolation structure over isolation material. *See* SAMSUNG-1004, [0031]-[0032], [0039]-[0041] (describing forming a gate separation structure 114 in an opening 112 (*see* FIG. 2C), where insulating material 108 is disposed at the bottom of the opening), FIGS. 2C-2I; SAMSUNG-1003, ¶178.

Limitation [21g]

In the Akarvardar-Xie combination, Xie describes **forming a dielectric material**: “a layer of *insulating material 130*, *e.g.*, silicon dioxide” (*e.g.*, a **dielectric material**, orange in the figures *infra*) is “blanket-deposited above the epi semiconductor material.” SAMSUNG-1004, [0036], FIG. 2I; SAMSUNG-1003, ¶179. In the combination, the dielectric material (*e.g.*, Xie's insulating material) is deposited onto the gate structures and the gate edge isolation structure. *Id.* When seen in top view, the dielectric material extends into the page next to the sidewalls of the gates and next to at least the end walls of the gate edge isolation structure. *Id.*



Akarvardar-Xie figure



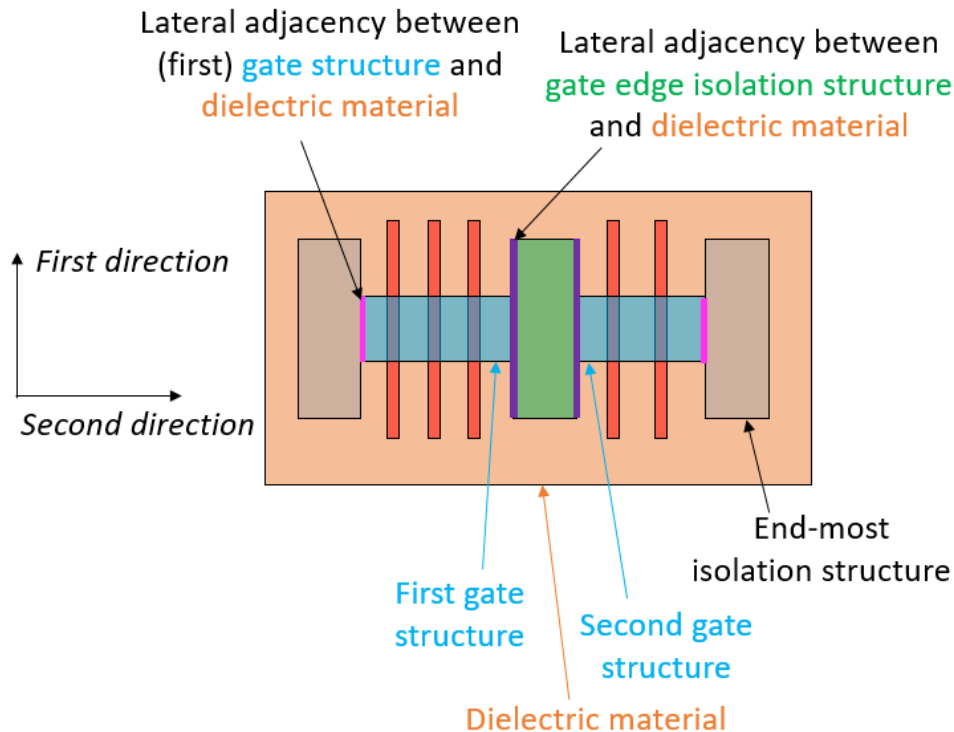
Akarvardar-Xie figure

The sidewalls of the gate structures are outlined in pink. These sidewalls extend into the page of the top-view figure, and the dielectric material is disposed next to these sidewalls, *i.e.*, the **dielectric material** (orange) is **laterally adjacent to each gate structure** at least at these pink-outlined sidewalls. SAMSUNG-1003, ¶180.

The ends of the gate edge isolation structure are outlined in purple. These ends extend into the page of the top-view figure, and the dielectric material is disposed next to these ends, *i.e.*, the **dielectric material** (orange) is **laterally adjacent to the gate edge isolation structure** at least at these purple-outlined ends. SAMSUNG-1003, ¶182.

The dielectric material is laterally adjacent to the gate structures and to the gate edge isolation structure **along the first direction**: viewing the structure starting from either gate structure or from the gate edge isolation structure and ***moving along the first direction*** (top to bottom in the top view), one reaches the dielectric material. SAMSUNG-1003, ¶¶181, 183.

Alternatively or additionally, the dielectric material is laterally adjacent to the gate structures and gate edge isolation structure at the pink-outlined and purple-outlined locations, respectively, in the alternative figure *infra*. SAMSUNG-1003, ¶¶184-185. To the extent this spatial relationship is considered to be laterally adjacent **along the first direction**, the dielectric material is laterally adjacent to the first and second gate structures along the first direction. *Id.*



Akarvardar-Xie figure (alternative)

In the combination, **the dielectric material** (e.g., Xie's insulating material 130) **is discrete from the gate edge isolation structure** (e.g., Akarvardar's modified second isolation region 504) at least because *they are formed in two distinct processing steps*. The modified second isolation region is formed in a self-alignment process (see SAMSUNG-1010, 5:52-65, 7:8-11, 7:57-59) while the insulating material is deposited over the second isolation region (see SAMSUNG-1004, [0031]-[0032], [0039]-[0041], FIGS. 2C-2I). SAMSUNG-1003, ¶186.

Alternatively or additionally, **the dielectric material is discrete from the gate edge isolation structure** at least because *they are formed of different materials*. The gate edge isolation structure (e.g., Akarvardar's modified second

isolation region) “may include oxides, nitrides, and oxynitrides of silicon,” while the dielectric material (*e.g.*, Xie’s insulating material) is “silicon dioxide.” SAMSUNG-1010, 6:64-7:9; SAMSUNG-1004, [0036]; SAMSUNG-1003, ¶187.

(2) Claim 22

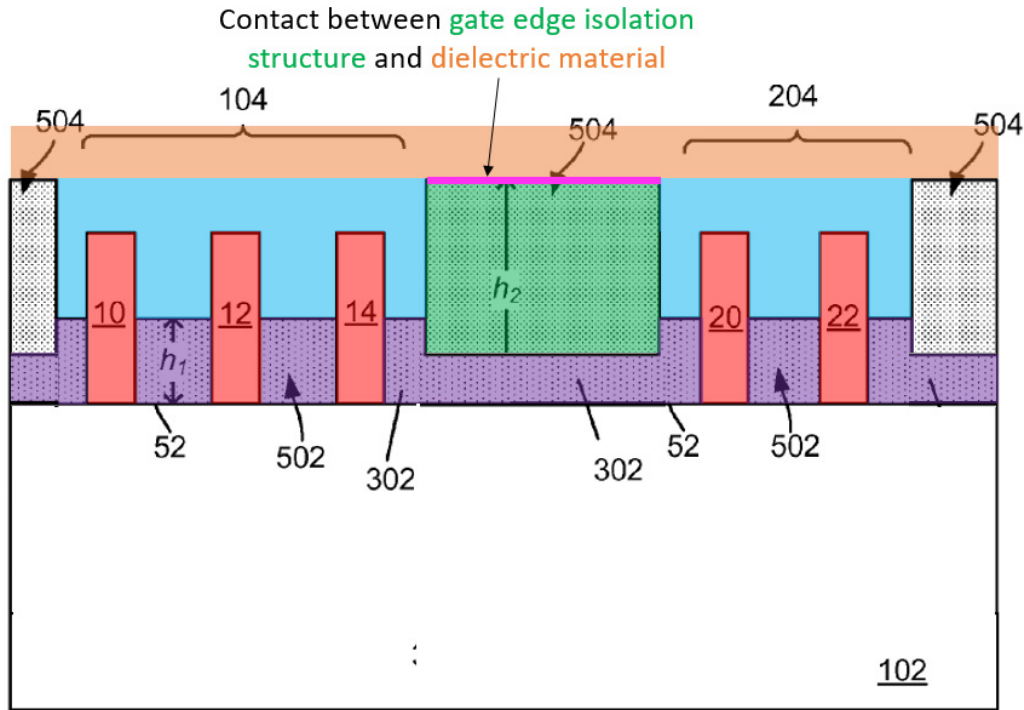
Limitation [22]

In the combination, Akarvardar describes that the gate edge isolation structure (*e.g.*, based on Akarvardar’s second isolation region 504) includes **silicon and nitrogen**: “a second dielectric layer 208 ... may include oxides, ***nitrides, and oxynitrides of silicon***,” where “[t]he second dielectric layer 308 may form a second isolation region 504.” SAMSUNG-1010, 6:64-7:9; SAMSUNG-1003, ¶188.

(3) Claim 23

Limitation [23]

In the combination, the dielectric material (*e.g.*, Xie’s insulating material) is “blanket-deposited” onto the gate structures and gate edge isolation structure. SAMSUNG-1004, [0036]; SAMSUNG-1003, ¶189. Thus, **the dielectric material is in contact with the gate edge isolation structure** at least on the top surface of the gate edge isolation structure, outlined in pink in the figure *infra*. SAMSUNG-1003, ¶189.



Akarvardar-Xie figure

(4) Claim 24

Limitation [24]

In the combination, the gate structures are deposited after formation of the gate edge isolation structure, and thus the gate material is in contact with the exposed sidewalls of the gate edge isolation structure. *See* SAMSUNG-1010, 7:65-8:2; SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶190.

A POSITA would have understood that formation of a gate structure involves depositing first the gate dielectric layer and then the gate electrode into the space over the fins and bounded by the gate edge isolation structure. *See* SAMSUNG-1025, 4:39-5:56, FIG. 8A; SAMSUNG-1005, 8:62-9:4; SAMSUNG-

1015, [0045]-[0047]; SAMSUNG-1012, 11:4-14; SAMSUNG-1014, 7:8-42; ;

SAMSUNG-1003, ¶¶191-192. As illustrated *infra*, depositing the gate dielectric

layer (dark blue) coats the gate dielectric layer onto exposed surfaces, including

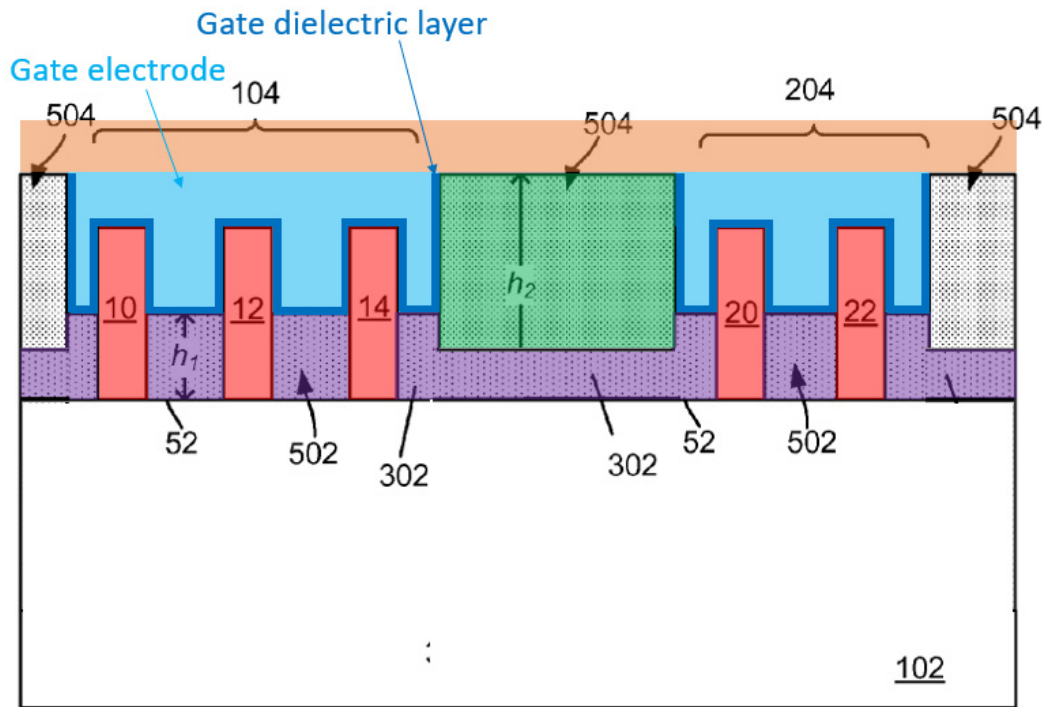
onto exposed edges of the gate edge isolation structure (green). See SAMSUNG-

1025, 4:39-5:56; SAMSUNG-1040, 6:33-38, FIGS. 7A-7B; SAMSUNG-1036,

[0023], FIG. 1F; SAMSUNG-1003, ¶¶191-192. Thus, **the gate edge isolation**

structure is in contact with the gate dielectric layer of each gate structure.

SAMSUNG-1003, ¶¶191-192.



Akarvardar-Xie figure

(5) Claim 26

Limitation [26]

In the Akarvardar-Xie combination, a POSITA would have understood or found obvious that Xie's gate structures each includes a gate dielectric layer (*e.g.*, **a high-k gate dielectric layer**) and a gate electrode (*e.g.*, a metal gate electrode). *See* SAMSUNG-1004, [0038]; SAMSUNG-1005, 5:5-46; SAMSUNG-1025, 4:39-5:3; SAMSUNG-1006, [0029]; SAMSUNG-1011, 3:59-4:10; SAMSUNG-1014, 7:8-22; SAMSUNG-1015, [0047]; SAMSUNG-1003, ¶193. For instance, a POSITA would have understood or found obvious for Xie's "high-k ... gate insulation layer" to be a gate dielectric layer that includes **a high-k dielectric material**. SAMSUNG-1004, [0038]; SAMSUNG-1003, ¶193.

C. [GROUND 3] – CLAIMS 21-24 AND 26 ARE OBVIOUS OVER AKARVARDAR, XIE, AND TSENG

The sections below provide a brief introduction to Tseng and the Akarvardar-Xie-Tseng combination.¹¹

Ground 3 is substantively identical to, and incorporates the analysis of, Ground 2 in all but the following respects. While Ground 2 demonstrates that the Element [21d] and [21e] features are obvious in view of Akarvardar and Xie, Ground 3 relies on the even more explicit disclosure of Tseng to reach these

¹¹ Petitioner incorporates this discussion into Ground 3.

features, as well as to reach dependent claims 24 and 26. Integration of Tseng does not disturb the mapping of the Akarvardar-Xie combination to other claim elements. To avoid repetition, and because the analysis of all other claim elements is identical, only the pertinent portions of Elements [21d]-[21e] and claims 24 and 26 are addressed in §IV.C. The unaddressed claim 21 elements, and claims 22-23, are obvious over the Akarvardar-Xie-Tseng combination at least as demonstrated for Ground 2. SAMSUNG-1003, ¶194.

1. The Akarvardar-Xie-Tseng combination

In the Akarvardar-Xie-Tseng combination, the gate structures (*e.g.*, Xie's replacement gate structures; *see* SAMSUNG-1004, [0030], [0038]) include gate dielectric layers and gate electrodes based on Tseng. *See* SAMSUNG-1005, 5:5-46; SAMSUNG-1003, ¶¶195-196. For instance, in the combination, Xie's "high-k ... gate insulation layer" and "bulk conductive metal layer" are implemented as a high-k gate dielectric layer and a metal gate electrode layer, respectively.

SAMSUNG-1004, [0038]; *see* SAMSUNG-1005, 5:5-46, 8:67-9:4, FIG. 5A; SAMSUNG-1003, ¶¶195-196.

A POSITA would have been motivated to pursue this implementation, and would have expected success in doing so, at least as discussed in §IV.B.5. SAMSUNG-1003, ¶197. Moreover, a POSITA would have expected success specifically in the Akarvardar-Xie-Tseng combination given that Akarvardar, Xie,

and Tseng all relate to FinFET fabrication processes. *See* SAMSUNG-1010, 7:11-14, 8:1-8, 8:23-28; SAMSUNG-1004, [0030]; SAMSUNG-1005, 8:59-62; SAMSUNG-1003, ¶197.

2. Analysis

(1) Claim 21

Limitations [21d] and [21e]

Akarvardar-Xie-Tseng renders obvious gate structures having the recited features, *e.g.*, in view of Xie's final gate structures. *See* [21d]-[21e] of Ground 2. SAMSUNG-1003, ¶198.

In the Akarvardar-Xie-Tseng combination, the gate structures include respective **gate dielectric layers** and respective **gate electrodes**, *e.g.*, based on Tseng's description of gate structures with gate dielectric layers and gate electrodes. *See* SAMSUNG-1005, 5:5-46, 3:4-12, FIGS. 2, 5A; SAMSUNG-1003, ¶199.

(2) Claim 24

Limitation [24]

When the Akarvardar-Xie-Tseng gate structures are fabricated by a replacement gate process (*see* SAMSUNG-1004, [0030]), **the gate edge isolation structure is in contact with a gate dielectric layer of each of the gate structures**. *See* [24] of Ground 1. SAMSUNG-1003, ¶200.

(3) Claim 26

Limitation [26]

The Akarvardar-Xie-Tseng gate dielectric layers include **a high-k dielectric material**. For instance, in the combination, Xie’s “high-k ... gate insulation layer” is implemented as a **gate dielectric layer** that includes **a high-k dielectric material** based on Tseng. SAMSUNG-1004, [0038]; *see* SAMSUNG-1005, 5:5-46; SAMSUNG-1003, ¶201.

V. PTAB DISCRETION SHOULD NOT PRECLUDE INSTITUTION

A. The Fintiv Factors Favor Institution—§314(a)

The ’812 Patent is the subject of complaints filed by Patent Owner in both district court and ITC on September 12, 2022. The district court case is currently stayed pending resolution of the ITC matter, and thus only the ITC matter is proceeding at this time. Pursuant to the Interim Procedure For Discretionary Denials In AIA Post-Grant Proceedings (June 21, 2022), the “PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” Accordingly, the *Fintiv* factors do not provide a reason to discretionarily deny institution based on the co-pending ITC proceeding.

B. The *Advanced Bionics* Test Favors Institution—§ 325(d)

This Petition presents new prior art and arguments against the Challenged Claims for which the file history contains no indication that the Office ever previously considered in connection with the ’812 Patent. Indeed, none of Tseng,

Akarvardar, or Xie—three of the four prior art references relied upon in this Petition—were previously cited or applied in a rejection during prosecution of the '812 Patent.

While Chang, which is used in Ground 1, is listed on the face of the '812 Patent, it is merely one of many references that were cited to the Examiner and, more critically, was not applied or discussed by the Examiner in any capacity during prosecution. *See generally* SAMSUNG-1002. Simply citing a reference on an information disclosure statement, with nothing more, does not favor denial of institution. *See Navistar, Inc. v. Fatigue Fracture Tech., LLC*, IPR2018-00853, Paper 13 at 16-17 (PTAB Sept. 12, 2018) (“[T]he fact that [references] were of record, but not applied in any rejection by the Examiner . . . provides little impetus for us to exercise our discretion to deny institution under §325(d).”).

VI. CONCLUSION AND FEES

The Challenged Claims are unpatentable. Petitioner authorizes charge of fees to Deposit Account 06-1050.

VII. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung”) are the real parties-in-interest.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

The '812 Patent is the subject of a civil action, *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352, E.D. Tex., filed September 12, 2022 (SAMSUNG-1054) and *Semiconductor Devices, Mobile Devices Containing The Same, and Components Thereof*; 337-TA-1336 (ITC) filed September 12, 2022 (SAMSUNG-1050). This Petition is being filed concurrently with another petition for IPR of the '812 Patent (IPR2023-00534).¹² Petitioner previously challenged related U.S. Patents in IPR2023-00403 and IPR2023-00404. Petitioner is not aware of any other disclaimers, reexamination certificates, or IPR petitions addressing the '812 Patent.

¹² Pursuant to the Trial Practice Guide, both petitions for IPR of the '812 Patent are being filed with a paper providing a succinct explanation of the differences between the petitions, why the issues addressed by the differences are material, and why the Board should exercise its discretion to institute both petitions.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

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D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR39843-0152IP2@fr.com

(referencing No. 39843-0152IP2 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, jjm@fr.com, in@fr.com and devries@fr.com).

Respectfully submitted,

Dated January 30, 2023

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CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,914 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated January 30, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on January 30, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, to the Patent Owner by serving the correspondence address of record as follows:

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