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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1

CONFIRMATION NO. 5347

POWER OF ATTORNEY NOTICE

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

OC00000129327234

Date Mailed: 10/26/2021

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/15/2021.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ggasgedom/

SAMSUNG 1002

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	D480-012035

CONFIRMATION NO. 5347

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

POA ACCEPTANCE LETTER

OC000000129327255

Date Mailed: 10/26/2021

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/15/2021.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ggasgedom/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/416,445
Filing Date	May 20, 2019
First Named Inventor	Glenn A. Glass
Title	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
Art Unit	2826
Examiner Name	Fazli Erdem
Attorney Docket Number	D480-012035

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	October 15, 2021
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
16/416,445	May 20, 2019

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 00164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/lisa hopkinson/	Date (Optional)	October 12, 2021
Name	Lisa Hopkinson		
Title	Administrator of Patents		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	44042649
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	15-OCT-2021
Filing Date:	20-MAY-2019
Time Stamp:	19:32:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2021-10-15_POA_D480-012035.pdf	1251579 e0de264adef4264ee1a1b4e5d26d3460aed5b102	no	2

Warnings:

Information:	
Total Files Size (in bytes):	1251579

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	06/30/2020	10700178	P38507USC2-C1	5347

31817 7590 06/10/2020

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

GLENN A. GLASS, Portland, OR;
INTEL CORPORATION, Santa Clara, CA;
ANAND S. MURTHY, Portland, OR;
TAHIR GHANI, Portland, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/416,445
	Filing Date	May 20, 2019
	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2826
	Examiner Name	N/A
Sheet 1 of 3	Attorney Docket No: P38507USC2-C1	

Change(s) applied to document, /L.H./ 4/27/2020

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-5,312,766	05-17-1994	Sheldon Aronowitz et al.	
		US-5,296,387	03-22-1994	Sheldon Aronowitz et al.	
		US-5,296,386	03-22-1994	Sheldon Aronowitz et al.	
		US-7,821,044	10-26-2010	Mark T. Bohr et al.	
		US-8,575,652	11-05-2013	Yoshiki Kamata	
		US-7,221,006	05-22-2007	Marius Orlowski et al.	
		US-7,732,285	06-08-2010	~~Intel Corporation~~ Sell et al.	
		US-7,880,228	02-01-2011	~~Toshiba Corp.~~ Yasutake	
		US-7,683,362	03-23-2010	~~Fujitsu Ltd.~~ Ohta et al.	
		US-7,667,227	02-23-2010	~~Fujitsu Ltd.~~ Shimamune et al.	
		US-20030057416	03-27-2003	Matthew Currie	
		US-20050130454	06-16-2005	Anand Murthy et al.	
		US-20050184354	08-25-2005	Chu et al.	
		US-20060156080	07-13-2006	John P. Tellkamp et al	
		US-20060237746	10-26-2006	Marius Orlowski et al.	
		US-20060255330	11-16-2006	Chen et al.	
		US-20070187767	08-16-2007	Yasutake, Nobuaki	
		US-20070238236	10-11-2007	Ted Cook Jr. et al.	
		US-20070275548	11-29-2007	Lavoie et al.	
		US-20080135878	06-12-2008	Kim et al.	
		US-20080179752	07-31-2008	Takashi Yamauchi et al.	
		US-20080197412	08-21-2008	Zhang et al.	
		US-20080242037	10-02-2008	Bernhard Sell et al.	
		US-20090224369	09-10-2009	Harold Samuel Gamble et al.	
		US-20100148217	06-17-2010	Danielle Simonelli	
		US-20110062498	03-17-2011	Frank Yang et al.	
		US-20110068407	03-24-2011	Chih Chieh Yeh et al.	
		US-20120007051	01-12-2012	Sarunya Bangsaruntip et al.	
		US-20120037998	02-16-2012	Bedell et al.	
		US-20130240989	09-19-2013	Glenn Glass et al.	
		US-20140070377	03-13-2014	Yu et al.	

EXAMINER	/FAZLI ERDEM/	DATE CONSIDERED	09/25/2019

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.E/

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1	5347

31817 7590 05/28/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
05/28/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

Corrected ***Notice of Allowability***	**Application No.** 16/416,445	**Applicant(s)** GLASS et al.	
	Examiner FAZLI ERDEM	**Art Unit** 2826	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to IDS filed on 5/12/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 10-29 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 5/12/2020.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/416,445
	Filing Date	May 20, 2019
	First Named Inventor	Glass, et al.
	Group Art Unit	2826
	Examiner Name	Erdem, Fazli
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/F.E/		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed March 24, 2020, 12 pgs	
/F.E/		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed April 24, 2020, 3 pgs	

EXAMINER /FAZLI ERDEM/ **DATE CONSIDERED** 05/25/2020

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
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"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 000197

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	16/416,445

Completed by (check one):

☐ Applicant/Inventor — /Michael A. Bernadicou/ (Signature)

☑ Attorney or Agent of record 35934 (Reg. No.) — Michael A. Bernadicou (Typed or printed name)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) — 503-222-9981 (Requester's telephone number)

☐ Assignee recorded at Reel _____ Frame_____ — 5/26/2020 (Date)

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ * Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	16416445
Filing Date:	20-May-2019
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Attorney Docket Number:	P38507USC2-C1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt	
EFS ID:	39532997
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	26-MAY-2020
Filing Date:	20-MAY-2019
Time Stamp:	20:23:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20205PK24020882
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P38507USC2-C1_Issue_Fee_05-26-20.pdf	93771 2131f3b83339ab3fb25c6d1844a0a0d8818 24a3b	no	1
Warnings:					
Information:					
2	Maintenance Fee Address Change	P38507USC2-C1_Maintenance_Fees.pdf	312408 df8c464ea8be65bd51b9753f5843a8e1b0d 8a7b2	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30386 3459e3c9fac43486b194efc29386ae789510 298d	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	436565		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 03/02/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Lisa Puccinelli	(Typed or printed name)
/Lisa Puccinelli/	(Signature)
May 26, 2020	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1	5347

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/02/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwabe, Williamson & Wyatt, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Intel Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-0393

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Michael A. Bernadicou/ Date May 26, 2020

Typed or printed name Michael A. Bernadicou Registration No. 35934

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/416,445
	Filing Date	May 20, 2019
	First Named Inventor	Glass, et al.
	Group Art Unit	2826
	Examiner Name	Erdem, Fazli
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed March 24, 2020, 12 pgs	
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed April 24, 2020, 3 pgs	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal	
Application Number:	16416445
Filing Date:	20-May-2019
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Attorney Docket Number:	P38507USC2-C1
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	39421942
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	12-MAY-2020
Filing Date:	20-MAY-2019
Time Stamp:	20:33:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	E20205BK34243962
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38507USC2-C1_IDS_05-12-20.pdf	328369 55c4eb02bab8c95c2df000c49b03765505d1cf41	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	P38507CN-D-OA_03-24-20.pdf	430544 a2b172ebf1feab0f1b95a5803c945d9fa0c9777f	no	12
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	P38507CN-D-OA_04-24-20.pdf	98832 bca236e60354118fe00b14560a2c253fbb7db819	no	3
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30530 3cfc425303a83a6b40654ebcb252ddfa1622b489	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	888275		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	16/416,445
Filing Date	May 20, 2019
First Inventor	Glass, et al
Art Unit	2826
Examiner Name	Erdem, Fazli
Attorney Docket No.	P38507USC2-C1 Conf. No. 5347

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted after Allowance but prior to payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☒ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	05-12-2020
Name/Print	Michael A. Bernadicou	Registration Number	35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 05-12-2020

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1248	209	germanide same contact.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 08:54
S1249	68	germanide same contact same source.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 08:56
S1250	28	germanide same contact same source.clm. and germanium near concentration	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 08:58
S1251	21	germanide same contact same source.clm. and germanium near concentration near10 higher	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 10:57
S1252	21	germanide same contact same source.clm. and germanium near concentration near10 (greater or higher)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 10:57
S1253	21	germanide same contact same source.clm. and germanium near concentration near10 (excess or greater or higher)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:00
S1254	46	germanide same contact same source and germanium near concentration near10 (excess or greater or higher) and fin near10 (facet or faceted or etch or etching or etched or recess or recessing or recessed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:01
S1255	44	germanide same contact same source	US-PGPUB;	OR	ON	2020/02/20

		and germanium near concentration near10 (excess or greater or higher) and fin near10 (facet or faceted or etch or etching or etched or recess or recessing or recessed) and contact near resistance	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			11:02
S1256	26	germanide same contact same source and germanium near concentration near10 (excess or greater or higher) and fin near10 (facet or faceted or etch or etching or etched or recess or recessing or recessed) and contact near resistance and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:05
S1257	12728	glass.in. or "murthy.in" or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:16
S1258	22362	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:16
S1259	204869	intel.as. or intel.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:17
S1260	176509	257/190.ccls. or H01L29/45.cpc. or H01L21/28.cpc. or H01L21/28518.cpc. or H01L21/28525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc. or H01L29/0847.cpc. or H01L9/165.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:19
S1261	396160	S1258 or S1259 or S1260	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:20
S1262	6103	S1261 and (ge or germanium) near10 concentration	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2020/02/20 11:20

			IBM_TDB			
S1263	299	S1262 and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:20
S1264	178	S1263 and contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:20
S1265	96	S1264 and (fin near5 (etch or etching or etched or recess or recessing or recessed))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:21
S1266	18	S1265 and (source or drain) same contact same (ge or germanium) same germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:21
S1267	1	S1265 and (source or drain) same contact same (ge or germanium) same germanide and 16/416,445	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:23
S1268	179574	257/190.ccls. or H01L29/45.cpc. or H01L21/28.cpc. or H01L21/28518.cpc. or H01L21/28525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc. or H01L29/0847.cpc. or H01L29/165.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:24
S1269	399082	S1258 or S1259 or S1268	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:24
S1270	35	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin	US-PGPUB; USPAT; USOCR;	OR	ON	2020/02/20 11:24

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S1271	21	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin near2 (recess or recessing or recessed or etch or etching or etched or facet or faceted)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:26
S1272	21	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:26
S1273	21	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin near10 surface	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:27
S1274	0	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin near10 surface near10 (facet or faceted)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:28
S1275	0	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin near10 surface with (facet or faceted)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:28
S1276	1	S1269 and (source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (facet or faceted)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:28
S1277	1	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (facet or faceted)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:29
S1278	1	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (facet or faceted) and	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:29

		germanide.ti,ab,clm.				
S1279	1	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (facet or faceted) and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:29
S1280	1	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface near10 (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:30
S1281	0	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin near10 surface near10 (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:30
S1282	1	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface near10 (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:30
S1283	1	(source or drain) same contact same (ge or germanium) same germanide same source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:30
S1284	10	(source or drain) same contact same (ge or germanium) same germanide and source same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:31
S1285	10	(source or drain) same contact same (ge or germanium) same germanide and (source or drain) same fin near10 (etch or etching or etched) near10 (recess or recessing or recessed or facet or faceted) and fin with surface with (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2020/02/20 11:31

3/16/2020 1:05:44 PM
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EAST Search History

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1286	7053	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT	OR	ON	2020/02/20 11:32
S1287	61469	intel.as. or intel.aanm.	US-PGPUB; USPAT	OR	ON	2020/02/20 11:32
S1288	75650	257/190.ccls. or H01L29/45.cpc. or H01L21/28.cpc. or H01L21/28518.cpc. or H01L21/28525.cpc. or H01L21/76.cpc. or H01L21/76805.cpc. or H01L21/76843.cpc. or H01L21/76864.cpc. or H01L21/76895.cpc. or H01L29/0847.cpc. or H01L29/165.cpc. or H01L29/66.cpc. or H01L29/66545.cpc. or H01L29/66636.cpc. or H01L29/66795.cpc. or H01L29/78.cpc. or H01L29/7833.cpc. or H01L29/7848.cpc. or H01L29/785.cpc. or H01L29/7851.cpc.	US-PGPUB; USPAT	OR	ON	2020/02/20 11:33
S1289	141692	S1286 or S1287 or S1288	US-PGPUB; USPAT	OR	ON	2020/02/20 11:33
S1290	580	S1289 and (germanide same (source or drain))	US-PGPUB; USPAT	OR	ON	2020/02/20 11:33
S1291	192	S1289 and (germanide same (source or drain)) and fin near10 (source or drain)	US-PGPUB; USPAT	OR	ON	2020/02/20 11:33
S1292	83	S1289 and (germanide same (source or drain)) and fin near10 (source or drain) and (ge or germanium) near10 concentration	US-PGPUB; USPAT	OR	ON	2020/02/20 11:34
S1293	63	S1292 and contact near resistance	US-PGPUB; USPAT	OR	ON	2020/02/20 11:58
S1294	44	S1293 and fin near10 (etch or etching or etched)	US-PGPUB; USPAT	OR	ON	2020/02/20 11:58

3/16/2020 1:06:41 PM
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

31817 7590 03/02/2020

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
ERDEM, FAZLI	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/02/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1	5347

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/02/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 03/02/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1	5347

TITLE OF INVENTION: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	06/02/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
ERDEM, FAZLI	2826	257-190000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1	5347

31817 7590 03/02/2020

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
ERDEM, FAZLI	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/02/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/416,445	Applicant(s) GLASS et al.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Response filed on 12/30/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 10-29 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 1/23/2020.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Response to Arguments

2. Applicant's arguments, filed on 12/30/2019, with respect to 35 USC 112 rejection on claims 10-29 (particularly see arguments on pages 8 and 9 of the remarks filed on 12/30/2019) have been fully considered and are persuasive. The 35 USC 112 rejeciton issued on 9/30/20190 has been withdrawn.

Allowable Subject Matter

3. Claims 10-29 are allowed.

4. The following is an examiner's statement of reasons for allowance:

5. Regarding Claim 10, prior art failed to disclose or fairly suggest an integrated circuit structure, comprising, along with other recited claim limitations, first and second germanide layers and graded germanium concentration in excess of 50% where a first source drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface. Claims 11-14 depend from claim 10 and hence are allowed for the same reason therein.

6. Regarding Claim 15, prior art failed to disclose or fairly suggest an integrated circuit structure, comprising, along with other recited claim limitations, first and second germanide layers and graded germanium concentration in excess of 50% where a first source drain region in the fin proximate a first side of the gate electrode, the first source

or drain region comprising two or more facets and a top surface. Claims 16-19 depend from claim 15 and hence are allowed for the same reason therein.

7. Regarding Claim 20, prior art failed to disclose or fairly suggest an integrated circuit structure, comprising, along with other recited claim limitations, first and second germanide layers and graded germanium concentration in excess of 50% where a first source drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface. Claims 21-29 depend from claim 20 and hence are allowed for the same reason therein.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F, 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
2/20/2020

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L29/45	2/20/2020	FE
H01L21/28518	2/20/2020	FE
H01L29/785	2/20/2020	FE

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
257	190	2/20/2020	FE

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

Search Notes		
Search Notes	**Date**	**Examiner**
Inventors are searched	9/25/2019	FE
Assignee is searched	9/25/2019	FE
Searched H01L29/45 limited with text	9/25/2019	FE
EAST Search History is attached	9/25/2019	FE
Inventors are searched	2/20/2020	FE
Assignee is searched	2/20/2020	FE
Searched 257/190 limited with text	2/20/2020	FE
Searched H01L29/45 limited with text	2/20/2020	FE
Searched H01L21/28, 28518 limited with text	2/20/2020	FE
Searched H01L29/66, 78, 785,. 7851 limited with text	2/20/2020	FE
Interference search is conducted	2/20/2020	FE
Updated EAST Search History is attached	2/20/2020	FE

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
H01L21	28, 28518	2/20/2020	FE
H01L29	66, 78, 785, 7851	2/20/2020	FE
H01L29	45	2/20/2020	FE

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

CPC						
Symbol					**Type**	**Version**
H01L	/	29	/	45	F	2013-01-01
H01L	/	29	/	66795	I	2013-01-01
H01L	/	29	/	7848	I	2013-01-01
H01L	/	29	/	785	I	2013-01-01
H01L	/	29	/	66636	I	2013-01-01
H01L	/	29	/	7833	I	2013-01-01
H01L	/	29	/	0847	I	2013-01-01
H01L	/	29	/	165	I	2013-01-01
H01L	/	21	/	28525	I	2013-01-01
H01L	/	21	/	28518	I	2013-01-01
H01L	/	29	/	66545	I	2013-01-01
H01L	/	21	/	76805	I	2013-01-01
H01L	/	21	/	76843	I	2013-01-01
H01L	/	21	/	76864	I	2013-01-01
H01L	/	21	/	76895	I	2013-01-01
H01L	/	29	/	7851	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826	20 February 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	6

U.S. Patent and Trademark Office — Part of Paper No.: 20200220

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	29	/	45

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
257	190

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826 (Primary Examiner)	20 February 2020 (Date)	O.G. Print Claim(s) 10	O.G. Print Figure 6

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	10	10	19	19	28										
2	11	11	20	20	29										
3	12	12	21												
4	13	13	22												
5	14	14	23												
6	15	15	24												
7	16	16	25												
8	17	17	26												
9	18	18	27												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	20	
/FAZLI ERDEM/ Primary Examiner, Art Unit 2826	20 February 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	10	6

U.S. Patent and Trademark Office — Part of Paper No.: 20200220

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/416,445
	Filing Date	May 20, 2019
	First Named Inventor	Glass, et al.
	Group Art Unit	2826
	Examiner Name	Erdem, Fazli
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
/F.E/		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed November 29, 2019, 6 pgs	
/F.E/		Office Action for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed December 12, 2019, 2 pgs.	
/F.E/		Notice of Allowance for European Patent Application No. 19188924.5 (Attorney Docket No. P38507EP-D1) mailed October 23, 2019, 2 pgs.	
/F.E/		STANTON P. ASHBURN ET AL: FORMATION OF C54 TITANIUM GERMANOSILICIDE USING RAPID THERMAL PROCESSING AND APPLICATION TO RAISED, ULTRASHALLOW JUNCTIONS", MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS,vol. 320, 1 January 1993, pages 311-316, XP055631293	

EXAMINER /FAZLI ERDEM/ **DATE CONSIDERED** 02/20/2020

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 5347

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
16/416,445	05/20/2019 RULE	257	2826	P38507USC2-C1

APPLICANTS

INTEL CORPORATION, Santa Clara, CA;

INVENTORS

GLENN A. GLASS, Portland, OR;
ANAND S. MURTHY, Portland, OR;
TAHIR GHANI, Portland, OR;

**** CONTINUING DATA ***************************

This application is a CON of 15/339,308 10/31/2016 PAT 10297670
which is a CON of 14/673,143 03/30/2015 PAT 9484432
which is a CON of 13/990,224 05/29/2013 PAT 8994104
which is a 371 of PCT/US2011/054198 09/30/2011
which is a CIP of 12/975,278 12/21/2010 PAT 8901537

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

05/28/2019

Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ❑ No Verified and Acknowledged /FAZLI ERDEM/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		OR	11	20	3

ADDRESS

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204
UNITED STATES

TITLE

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

FILING FEE RECEIVED		
1880	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

BIB (Rev. 05/07).

Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/416,445
	Filing Date	May 20, 2019
	First Named Inventor	Glass, et al.
	Group Art Unit	2826
	Examiner Name	Erdem, Fazli
Sheet 1 of 1	Attorney Docket No: P38507USC2-C1	

US PATENT DOCUMENTS					
Examiner Initial *	**Cite No [1]**	**USP Document Number**	**Publication or Issue Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	**Cite No [1]**	**Foreign Patent Document** Country Code/Number/Kind Code (if known)	**Publication Date MM-DD-YYYY**	**Name of Patentee or Applicant of cited Document**	**Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear**	**T[2]**

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		Office Action for Chinese Patent Application No. 201610313170.4 (Attorney Docket No. P38507CN-D) mailed November 29, 2019, 6 pgs	
		Office Action for European Patent Application No. 11852027.9 (Attorney Docket No. P38507EP) mailed December 12, 2019, 2 pgs.	
		Notice of Allowance for European Patent Application No. 19188924.5 (Attorney Docket No. P38507EP-D1) mailed October 23, 2019, 2 pgs.	
		STANTON P. ASHBURN ET AL: FORMATION OF C54 TITANIUM GERMANOSILICIDE USING RAPID THERMAL PROCESSING AND APPLICATION TO RAISED, ULTRASHALLOW JUNCTIONS", MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS,vol. 320, 1 January 1993, pages 311-316, XP055631293	

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	38384422
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	23-JAN-2020
Filing Date:	20-MAY-2019
Time Stamp:	19:57:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38507USC2-C1_IDS_01-23-20.pdf	201247 766df65fbba0d9cb7879b138bc948418727 8f690	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Non Patent Literature	NPL_Stanton.pdf	860304 43115dd03b07def88aa7846e249549f1180be46d	no	6
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	Ref_P38507CN-D_OA_11-29-19.pdf	804245 abab5319dfdebe68d4c89eb02bed11c63edd1c04	no	6
Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	Ref_P38507EP_Decision_to_Grant_12-05-19.pdf	240656 34821a70a8fb5c9c9d5579bbc6a1747fb3f675ef	no	2
Warnings:					
Information:					
5	Other Reference-Patent/App/Search documents	Ref_P38507EP-D1_OA_10-23-19.pdf	861480 55388ec9a47b4f217920e24ea1ca89d64bfa8673	no	9
Warnings:					
Information:					
		Total Files Size (in bytes):	2967932		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application No.	16/416,445
	Filing Date	May 20, 2019
	First Inventor	Glass, et al.
	Art Unit	2826
	Examiner Name	Erdem, Fazli
	Attorney Docket No.	P38507USC2-C1 Conf. No. 5347

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action or Notice of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	01-23-2020
Name/Print	Michael A. Bernadicou	Registration Number	35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 01-23-20

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Glen A. GLASS	Examiner: Erdem, Fazli
Application No.: 16/416,445	Art Unit: 2826
Filed: May 20, 2019	Confirmation No.: 5347
For: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

This is in response to the Office Action mailed September 30, 2019. Applicant respectfully requests the Examiner to enter the following response and consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. – 9. (Canceled)

10. (Previously Presented) An integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin;

a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

11. (Previously Presented) The integrated circuit structure of claim 10, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

12. (Previously Presented) The integrated circuit structure of claim 10, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

13. (Previously Presented) The integrated circuit structure of claim 10, wherein the fin comprises a strained channel between the first and second source or drain regions.

14. (Previously Presented) The integrated circuit structure of claim 10, wherein the first and second source or drain regions are P-type.

15. (Previously Presented) An integrated circuit structure, comprising:

a body comprising silicon;

a gate electrode over the body;

a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the body proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

16. (Previously Presented) The integrated circuit structure of claim 15, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

17. (Previously Presented) The integrated circuit structure of claim 15, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

18. (Previously Presented) The integrated circuit structure of claim 15, wherein the body comprises a strained channel between the first and second source or drain regions.

19. (Previously Presented) The integrated circuit structure of claim 15, wherein the first and second source or drain regions are P-type.

20. (Previously Presented) A computing device, comprising:

a board; and

a component coupled to the board, the component including an integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin;

a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

21. (Previously Presented) The computing device of claim 20, further comprising:

a memory coupled to the board.

22. (Previously Presented) The computing device of claim 20, further comprising:

a communication chip coupled to the board.

23. (Previously Presented) The computing device of claim 20, further comprising:

a camera coupled to the board.

24. (Previously Presented) The computing device of claim 20, further comprising:

a global positioning system coupled to the board.

25. (Previously Presented) The computing device of claim 20, further comprising:

a battery coupled to the board.

26. (Previously Presented) The computing device of claim 20, further comprising:

an antenna coupled to the board.

27. (Previously Presented) The computing device of claim 20, wherein the component is a packaged integrated circuit die.

28. (Previously Presented) The computing device of claim 20, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

29. (Previously Presented) The computing device of claim 20, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

REMARKS

Claim Rejection – 35 U.S.C. § 112

Claims 10-29 are rejected under 35 U.S.C. § 112(a) and 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement.

With respect to the claims limitations, "*the first source or drain region comprising two or more facets*," the Examiner indicates "*Examiner does not understand where the "facets" are located with respect to the source/drain regions.*" (*See* Office Action, Page 3, Section 5.) In response, Applicant provides below an annotated version of Figure 6 of Applicant's specification. In the annotated version of Figure 6, two exemplary but non-limiting locations for facets for a first source or drain region are indicated. It is to be appreciated that reciprocal exemplary but non-limiting locations for facets for a second source or drain region would similarly be located on the opposite side of gate electrode 640.

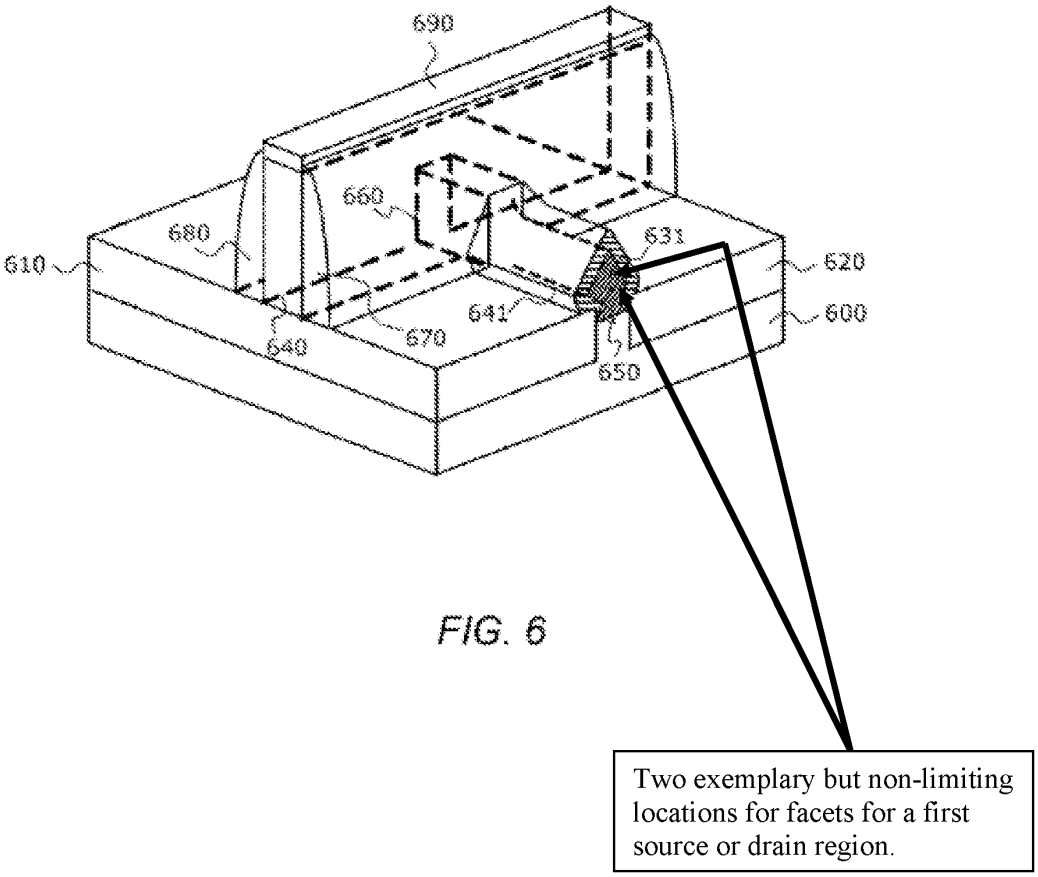


FIG. 6

Annotated Figure 6 of Applicant's specification.

Thus, contrary to the Examiner's statements in the Office Action, Applicant's original specification as filed provides clear support for the claim limitations "*the first source or drain region comprising two or more facets*," and "*the second source or drain region comprising two or more facets*." Accordingly, Applicant respectfully requests that the Examiner remove the rejection of the claims.

REMARKS

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 50-0393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

December 30, 2019
Date

/Michael A. Bernadicou/
Michael A. Bernadicou
Reg. No. 35,934

1211 SW 5th, Ste. 1900
Portland, OR 97204
Telephone: (503) 222-9981
Facsimile: (503) 796-2900

Electronic Acknowledgement Receipt	
EFS ID:	38168918
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	30-DEC-2019
Filing Date:	20-MAY-2019
Time Stamp:	20:31:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Intel_P38507USC2-C1_ROA_12_30_19.pdf	135856 e4ca67fc431f791f3579bf4b0faa0e6e0caf6c54	yes	10

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	10
Warnings:			
Information:			
	Total Files Size (in bytes):	135856	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/416,445	Filing Date 05/20/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	12/30/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/JACKIE A WHITE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1

CONFIRMATION NO. 5347

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

PUBLICATION NOTICE

OC000000112484951

Title:CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Publication No.US-2019-0341464-A1
Publication Date:11/07/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1	5347

31817 7590 09/30/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

NOTIFICATION DATE	DELIVERY MODE
09/30/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

Office Action Summary	Application No. 16/416,445	Applicant(s) GLASS et al.	
	Examiner FAZLI ERDEM	Art Unit 2826	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 7/31/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 10-29 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 10-29 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 5/20/2019 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 8/2/2019.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> (a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 10-29 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for pre-AIA the inventor(s), at the time the application was filed, had possession of the claimed invention.

4. Examiner does not consider the limitation “drain region comprising two or more facets” or “source region comprising two or more facets” as claimed in independent claims 10, 15 and 20, to not have enough description disclosure in specification and drawings as originally filed.

5. The closest place in specification that refers to "facet" is paragraph 0029 and it is with respect to Fig. 6. Examiner does not understand where the "facets" are located with respect to the source/drain regions.

6. Paragraph 0045 also mentions "recessed source interface 650" which might be related to "facets"

7. Examiner is requesting explanation of where the facets are located in the specification and in Fig. 6

8. Examiner is readily available for an interview for further clarification.

9. Examiner is recommending inclusion trigate structure as mentioned paragraphs 0043, 0044 and 0046 with respect to Fig 6, for allowable subject matter. Should the applicant decide to include this trigate limitation, applicant is urged to review commonly owned Glass et al. (9,349,810)'s claim section (claim 14, tri-gate structure) to not to cause an interference issue.

Examiner is making following pertinent prior art references record.

Glass et al. (9,349,810) (Claim 14, Fig. 6)

Adam et al. (2009/0302348) (faceted/recessed/undercut fin/channel area under gate as shown in Figs. 6, 11 and 12)

Currie et al. (2003/0057416) (boron/germanium concentration gradient, Fig. 2)

Chu et al. (2009/0206307) (germanide contacts, Figs 1K, 1L)

Yasutake (2007/0187767) (germanide contacts Figs. 1, 9 and 10)

Sugiyama et al. (6,607,948) (contact resistance lowering configuration

Sell et al. (2008/0242037) (source/drain region extensions/facets/recess/undercut, as shown in Figs. 1C, 3F and 3I)

Orlowski (2006/0237746)(germanium source/drain regions, see Fig. 2)

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to FAZLI ERDEM whose telephone number is (571)272-1914. The examiner can normally be reached on M-F, 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Davienne Monbleau can be reached on 571-272-1945. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/FAZLI ERDEM/
Primary Examiner, Art Unit 2826
9/25/2019

Notice of References Cited	Application/Control No. 16/416,445	Applicant(s)/Patent Under Reexamination GLASS et al.	
	Examiner FAZLI ERDEM	Art Unit 2826	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20080242037-A1	10-2008	Sell; Bernhard	H01L21/30608	438/299
*	B	US-6607948-B1	08-2003	Sugiyama; Naoharu	H01L21/02381	438/151
*	C	US-20070187767-A1	08-2007	Yasutake; Nobuaki	H01L21/28518	257/368
*	D	US-20090206370-A1	08-2009	CHU; JACK O.	H01L29/45	257/197
*	E	US-20030057416-A1	03-2003	Currie, Matthew	H01L29/105	257/19
*	F	US-20090302348-A1	12-2009	Adam; Thomas N.	H01L21/26513	257/190
*	G	US-9349810-B2	05-2016	Glass; Glenn A.	H01L29/165	1/1
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	**Art Unit**
	FAZLI ERDEM	2826

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant						☐ CPA		☐ T.D.		☐ R.1.47
CLAIM		**DATE**								
Final	Original	09/25/2019								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
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	21	✓								
	22	✓								
	23	✓								
	24	✓								
	25	✓								
	26	✓								
	27	✓								
	28	✓								
	29	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	16/416,445	GLASS et al.
	Examiner	Art Unit
	FAZLI ERDEM	2826

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventors are searched	9/25/2019	FE
Assignee is searched	9/25/2019	FE
Searched H01L29/45 limited with text	9/25/2019	FE
EAST Search History is attached	9/25/2019	FE

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	70	finfet same germanide same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:09
L2	53	finfet same germanide same contact near2 (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:10
L3	22	finfet same germanide same contact near2 (source or drain) same contact near2 resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:10
L4	9	finfet same germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:11
L5	0	finfet same germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:11
L6	22	finfet and germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:12
L7	3	finfet and germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm. and fin.clm. and (titanium or ti).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:12
L8	37	(finfet or fin).clm. and (germanide same	US-PGPUB;	OR	ON	2019/09/25

		boron same germanium)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:15
L9	35	(finfet or fin).clm. and (germanide same boron same germanium same source same drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:15
L10	18	(fin).clm. and (germanide same boron same germanium same source same drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:16
L11	14	(fin).clm. and (germanide same boron same germanium same source same drain same contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:17
L12	0	(fin same finfet same facet) and (germanide same boron same germanium same source same drain same contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:18
L13	18	(fin same finfet same facet same contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:19
L14	0	(fin same finfet same facet same contact near resistance) and (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:20
L15	13	(fin same finfet same facet and contact near resistance) and (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:20
L16	301	(fin same finfet and contact near resistance) and (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/09/25 12:29

			IBM_TDB			
L17	207	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:29
L18	100	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium))) and contact.ab. and contact.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:30
L19	90	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium))) and contact.ab. and contact.clm. and (ge or germanium or germanide).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:30
L20	38	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium))) and contact.ab. and contact.clm. and (ge or germanium or germanide).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:31
L35	305	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 12:32

		20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-				

		20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$ or US-20190109234-$ or US-20150035017-$ or US-20140162442-$ or US-20190097012-$ or US-20180033882-$ or US-20150069531-$ or US-20110193141-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$ or US-10269646-$ or US-9214556-$).did. or (KR-20030057416-$				

		or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$ or WO-2015032274-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$ or US-20090302348-$).did.				
L37	67	l35 and (undercut or under-cut or under near cut)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:33
L38	35	l35 and (undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:33
L39	30	l35 and (undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched) and contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:35
L40	20	l35 and (undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched) and contact near resistance near10 (germanium or germanide or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:35
L41	20	(undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:36
L42	22	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:37
L43	20	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/09/25 12:38

		germanide or ge) and (germanium or ge or germanide).clm.	DERWENT; IBM_TDB			
L44	18	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact near10 (germanium or ge or germanide).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:38
L45	2	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact near10 (germanium or ge or germanide) near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:38
L46	17	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact with (germanium or ge or germanide) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:39
L47	8	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact with (germanium or ge or germanide) with (ti or titanium) and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:40
L48	11724	"glass.in" or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:46
L49	21824	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L50	198625	intel.as. or intel.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L51	12198	257/190.ccls. or H01L29/45.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47

L52	230560	l49 or l50 or l51	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L53	2458	l52 and finfet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L54	636	l53 and fin same (recess or recessing or recessed or facet)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L55	193	l54 and (contact same (germanium or germanide or ge) same source same drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L56	93	l55 and (ge or germanium or germanide) same (contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L57	54	l56 and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L58	32	l57 and (ge or germanium) near10 concentration same source same drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:49
L59	32	l58 and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:49
L60	30	l59 and (germanide or ge or germanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/09/25 12:50

			DERWENT; IBM_TDB			
L61	30	l60 and (source or drain) near10 (germanium or ge or germanide) same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:50
L62	11	l61 and (graded or gradient).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:51
L63	2	l62 and contact same (titanium or ti).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:51
L64	14	contact near resistance near10 (ge or germanium or germanide).ti,ab,clm. and (ge or germanium) near10 (titanium or ti) and fin.clm. and contact.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:53
L65	0	l64 and (ge or germanium) near10 (ti or titanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:54
L66	14	l64 and (ge or germanium) near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:54
L67	11	l64 and (germanide) near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:56
L82	313	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 12:56

		$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-				

		$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$ or US-20190109234-$ or US-20150035017-$ or US-20140162442-$ or US-20190097012-$ or US-20180033882-$ or US-20150069531-$ or US-20110193141-$ or US-20160293760-$ or US-20160027781-$ or US-20170345933-$ or US-20180261696-$ or US-20180145174-$ or US-20190165124-$ or US-20190207015-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-				

		9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$ or US-10269646-$ or US-9214556-$ or US-10147817-$).did. or (KR-20030057416-$ or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$ or WO-2015032274-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$ or US-20090302348-$).did.				
L84	78	l82 and germanide with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:57
L85	49	l82 and germanide with (ti or titanium) same (si or silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:58
L86	26	l82 and germanide with (ti or titanium) same (si or silicon) same (contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/09/25 12:58

			IBM_TDB			
L87	14	l82 and germanide with (ti or titanium) same (si or silicon) same (contact near resistance) and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:59
L88	14	l82 and germanide same (ti or titanium) same (si or silicon) same (contact near resistance) and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:59

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L15	293	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 09:49

		$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-					

		9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$).did. or (KR-20030057416-$ or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$).did.				
L17	41	l15 and facet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 09:50
L18	35	l15 and (fin near10 (facet or faceted))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 09:57
L19	22	l15 and (fin near10 (facet or faceted)) same (undercut or under-cut or under near cut)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/09/25 09:58

			EPO; JPO; DERWENT; IBM_TDB			
L20	22	l15 and (fin near10 (facet or faceted)) same (undercut or under-cut or under near cut) same (etch or etching or etched)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 09:58
L21	4	"6373746".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:02
L22	15	"09667610"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:03
L23	40	"7177196"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:03
L24	3	"7177196".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:03
L25	22	l15 and (fin near10 (facet or faceted)) same (undercut or under-cut or under near cut) same (etch or etching or etched) and germanide	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:04
L26	37	(fin or finfet).clm. and germanide.clm. and (source or drain) near5 contact near5 resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:06
L27	24	(fin or finfet).clm. and germanide same (source or drain) near5 contact near5 resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:07
L28	6	(fin or finfet) same germanide same (source or drain) near5 contact near5	US-PGPUB; USPAT;	OR	ON	2019/09/25 10:07

		resistance	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
L29	63	(fin or finfet).clm. and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:09
L30	25	(fin or finfet) same germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:12
L31	85	(fin or finfet) same germanide same source same drain same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:13
L32	32	(fin or finfet) same germanide same source same drain same contact same (titanium or ti)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:17
L33	32	(fin or finfet) same germanide same source same drain same contact same (titanium or ti) and (fin or finfet).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:18
L34	16	(fin or finfet) same germanide same source same drain same contact same (titanium or ti) and (fin or finfet).clm. and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:18
L35	13	(fin or finfet) same germanide same source same drain same contact same (titanium or ti) and (fin or finfet).clm. and germanide.clm. and (germanium or ge) near10 concentration.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:21
L36	5	(fin or finfet) same germanide same source same drain same contact same (titanium or ti) and (fin or finfet).clm. and germanide.clm. and (germanium or ge) near10 concentration.clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:22

L51	296	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 10:23

		or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$ or US-20190109234-$ or US-20150035017-$ or US-20140162442-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-				

		5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$).did. or (KR-20030057416-$ or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$).did.				
L53	96	l51 and (etch or etching or etched) near10 fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:24
L54	57	l51 and (etch or etching or etched) near10 fin near10 (recess or recessing or recessed)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:26
L55	24	l51 and (etch or etching or etched) near10 fin near10 (recess or recessing or recessed) and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:26
L56	28	contact adj resistance and (etch or etching or etched) near10 fin near10 (recess or recessing or recessed) and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/09/25 10:26

			IBM_TDB			
L57	13	contact adj resistance and (etch or etching or etched) near10 fin near10 (recess or recessing or recessed) and germanide.clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:27
L58	2	"20090302348".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:30
L59	2	"20090302348".pn. and "34"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:33
L74	298	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 10:34

		or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-					

		20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$ or US-20190109234-$ or US-20150035017-$ or US-20140162442-$ or US-20190097012-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$).did. or (KR-20030057416-$ or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$ or US-20090302348-$).did.				
L76	5	contact near10 germanide.clm. and (tri-gate or tri near gate or trigate).clm.	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/09/25 10:37

			EPO; JPO; DERWENT; IBM_TDB			
L77	2	contact near10 germanide.clm. and (tri-gate or tri near gate or trigate).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:37
L78	0	contact near10 germanide same (tri-gate or tri near gate or trigate) same fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:41
L79	0	contact near10 germanide same (tri-gate or tri near gate or trigate) same fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:44
L80	0	germanide same (tri-gate or tri near gate or trigate) same fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:44
L81	4101	(tri-gate or tri near gate or trigate) same fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:45
L82	59	l51 and (tri-gate or tri near gate or trigate) same fin	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 10:45
L97	298	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 10:52

		or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-					

		20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$ or US-20190109234-$ or US-20150035017-$ or US-20140162442-$ or US-20190097012-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-					

		7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$).did. or (KR-20030057416-$ or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$ or US-20090302348-$).did.				

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	70	finfet same germanide same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:09
L2	53	finfet same germanide same contact near2 (source or drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:10
L3	22	finfet same germanide same contact near2 (source or drain) same contact near2 resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:10
L4	9	finfet same germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:11
L5	0	finfet same germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:11
L6	22	finfet and germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:12
L7	3	finfet and germanide same contact near2 (source or drain) same contact near2 resistance and (germanium or ge).clm. and fin.clm. and (titanium or ti).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:12
L8	37	(finfet or fin).clm. and (germanide same	US-PGPUB;	OR	ON	2019/09/25

		boron same germanium)	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			12:15
L9	35	(finfet or fin).clm. and (germanide same boron same germanium same source same drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:15
L10	18	(fin).clm. and (germanide same boron same germanium same source same drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:16
L11	14	(fin).clm. and (germanide same boron same germanium same source same drain same contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:17
L12	0	(fin same finfet same facet) and (germanide same boron same germanium same source same drain same contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:18
L13	18	(fin same finfet same facet same contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:19
L14	0	(fin same finfet same facet same contact near resistance) and (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:20
L15	13	(fin same finfet same facet and contact near resistance) and (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:20
L16	301	(fin same finfet and contact near resistance) and (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/09/25 12:29

			IBM_TDB			
L17	207	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:29
L18	100	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium))) and contact.ab. and contact.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:30
L19	90	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium))) and contact.ab. and contact.clm. and (ge or germanium or germanide).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:30
L20	38	(fin same finfet and contact near resistance) and contact same (germanide or ((germanium or ge) near10 (ti or titanium))) and contact.ab. and contact.clm. and (ge or germanium or germanide).clm. and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:31
L35	305	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 12:32

		20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-				

		20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$ or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$ or US-20190109234-$ or US-20150035017-$ or US-20140162442-$ or US-20190097012-$ or US-20180033882-$ or US-20150069531-$ or US-20110193141-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$ or US-10269646-$ or US-9214556-$).did. or (KR-20030057416-$				

		or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$ or WO-2015032274-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$ or US-20090302348-$).did.				
L37	67	l35 and (undercut or under-cut or under near cut)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:33
L38	35	l35 and (undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:33
L39	30	l35 and (undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched) and contact near resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:35
L40	20	l35 and (undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched) and contact near resistance near10 (germanium or germanide or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:35
L41	20	(undercut or under-cut or under near cut) near10 (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:36
L42	22	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:37
L43	20	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/09/25 12:38

		germanide or ge) and (germanium or ge or germanide).clm.	DERWENT; IBM_TDB			
L44	18	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact near10 (germanium or ge or germanide).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:38
L45	2	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact near10 (germanium or ge or germanide) near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:38
L46	17	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact with (germanium or ge or germanide) with (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:39
L47	8	(undercut or under-cut or under near cut) same (fin or channel) same (etch or etching or etched) same (recess or recessing or recessed) and contact near resistance near10 (germanium or germanide or ge) and contact with (germanium or ge or germanide) with (ti or titanium) and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:40
L48	11724	"glass.in" or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:46
L49	21824	glass.in. or murthy.in. or ghani.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L50	198625	intel.as. or intel.aanm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L51	12198	257/190.ccls. or H01L29/45.cpc.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47

L52	230560	l49 or l50 or l51	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L53	2458	l52 and finfet	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:47
L54	636	l53 and fin same (recess or recessing or recessed or facet)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L55	193	l54 and (contact same (germanium or germanide or ge) same source same drain)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L56	93	l55 and (ge or germanium or germanide) same (contact near resistance)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L57	54	l56 and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:48
L58	32	l57 and (ge or germanium) near10 concentration same source same drain	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:49
L59	32	l58 and fin.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:49
L60	30	l59 and (germanide or ge or germanium).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/09/25 12:50

			DERWENT; IBM_TDB			
L61	30	l60 and (source or drain) near10 (germanium or ge or germanide) same contact	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:50
L62	11	l61 and (graded or gradient).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:51
L63	2	l62 and contact same (titanium or ti).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 12:51

9/ 25/ 2019 12:52:56 PM
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	"16416445"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:38
L2	0	"16/416445"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:38
L3	69	germanide near10 silicon near10 germanium near10 titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:39
L4	2	germanide near10 silicon near10 germanium near10 titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:40
L5	8	germanide with silicon with germanium with titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:42
L6	0	germanide with silicon with germanium with "titanium." same (source or drain) near2 region	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:42
L7	16	germanide with silicon with germanium with titanium same (source or drain) near2 region	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:42
L8	72	germanide same silicon same germanium	US-PGPUB;	OR	ON	2019/09/25

		same titanium same (source or drain) near2 region	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			07:43
L9	19	contact near resistance same germanide same silicon same germanium same titanium same (source or drain) near2 region	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:45
L10	17	contact near resistance.ti,ab,clm. and germanide same (source or drain) near2 region.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:48
L11	25	12/975278	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:49
L12	76	("20020197806" | "20030057416" | "20050130454" | "20050145944" | "20050184354" | "20060060859" | "20060138398" | "20060148151" | "20060156080" | "20060172511" | "20060255330" | "20060289856" | "20070004123" | "20070053381" | "20070187767" | "20070275548" | "20080054347" | "20080135878" | "20080197412" | "20080230805" | "20080242037" | "20090075029" | "20090302348" | "20100109044" | "20100148217" | "20100244154" | "20110147828" | "20120037998" | "20130240989" | "20130248999" | "20130264639" | "20140070377" | "5281552" | "5296386" | "5296387" | "5312766" | "6235568" | "6541343" | "6605498" | "6621131" | "6653700" | "6797556" | "6812086" | "6861318" | "6885084" | "6887762" | "6933589" | "6949482" | "6952040" | "6972228" | "7060576" | "7129139" | "7138320" | "7138697" | "7226842" | "7244668" | "7274055" | "7338873" | "7358547" | "7391087" | "7402872" | "7427775" | "7436035" | "7491643" | "7492017" | "7494858" | "7518196" | "7544997" | "7662689" | "7663192" | "7678631" | "7682887" | "7682916" | "7732285" | "7880228" | "8354694").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2019/09/25 07:50
L13	16	l12 and germanide	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/09/25 07:50

			EPO; JPO; DERWENT; IBM_TDB			
L14	1987	(germanium or ge) near10 (source or drain) near10 region.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:52
L15	52	(germanium or ge) near10 (source or drain) near10 region.clm. and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:52
L16	0	(germanium or ge) near10 (source or drain) near10 region.clm. and germanide.clm. and germaniun near10 graded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:53
L17	20	(germanium or ge) near10 (source or drain) near10 region.clm. and germanide.clm. and germanium near10 graded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:53
L18	102	("20020197806" | "20030057416" | "20050130454" | "20050145944" | "20050184354" | "20060060859" | "20060065914" | "20060138398" | "20060148151" | "20060156080" | "20060172511" | "20060199622" | "20060237746" | "20060255330" | "20060289856" | "20070004123" | "20070053381" | "20070075378" | "20070187767" | "20070235802" | "20070275548" | "20080054347" | "20080135878" | "20080179752" | "20080197412" | "20080230805" | "20080242037" | "20090075029" | "20090302348" | "20100109044" | "20100123198" | "20100148217" | "20100197092" | "20100244154" | "20110068407" | "20110147828" | "20110183486" | "20120037998" | "20120153387" | "20130240989" | "20130248999" | "20130264639" | "20140070377" | "20140231914" | "20150060945" | "20150206942" | "20150333180" | "5089872" | "5216271" | "5281552" | "5296386" | "5296387" | "5312766" | "6235568" | "6274894" | "6541343" | "6605498" | "6607948" | "6621131" | "6653700" | "6797556" | "6812086" | "6861318" | "6885084" | "6887762" | "6933589" | "6949482" | "6952040" | "6972228" | "7060576" |	US-PGPUB; USPAT; USOCR	OR	ON	2019/09/25 07:54

		"7129139" | "7135724" | "7138320" | "7138697" | "7226842" | "7244668" | "7274055" | "7338873" | "7358547" | "7391087" | "7402872" | "7427775" | "7436035" | "7491643" | "7492017" | "7494858" | "7518196" | "7544997" | "7662689" | "7663192" | "7678631" | "7682887" | "7682916" | "7732285" | "7880228" | "8039902" | "8354694" | "8598003" | "8901537" | "8994104" | "9117791" | "9349810").PN.				
L19	11	pre-contact near metallization	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:56
L20	6	pre-contact near metallization and germanide.ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:57
L21	0	pre-contact near metallization and germanide.ti,ab,clm. and titanium.ti,ab,clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:57
L22	0	pre-contact near metallization and germanide.ti,ab,clm. and titaniu	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:58
L23	6	pre-contact near metallization and germanide.ti,ab,clm. and titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:58
L24	6	pre-contact near metallization and germanide.ti,ab,clm. and germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:58
L25	179	germanide.clm. and titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 07:59
L26	62	germanide.clm. and titanium.clm. and	US-PGPUB;	OR	ON	2019/09/25

		contact adj resistance	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			07:59
L27	11	(source or drain) same contact same germanide.clm. and titanium.clm. and contact adj resistance	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:00
L28	7	(source or drain) same contact same germanide.clm. and contact same titanium.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:01
L29	163	(source or drain) same contact same germanide same titanium	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:01
L30	45	(source or drain) same contact same germanide same titanium same trench	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:02
L31	22	(source or drain) same contact same germanide same titanium same trench and glass.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:03
L32	21	(source or drain) same contact same germanide same titanium same trench same resistance and glass.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:04
L33	10	(source or drain) same contact same germanide same titanium same trench same resistance and glass.in.	USPAT	OR	ON	2019/09/25 08:05
L34	6	(source or drain) same contact same germanide same titanium same trench same resistance and glass.in. and germanide.clm.	USPAT	OR	ON	2019/09/25 08:07
L35	20	(glass or murthy or thani).in. and (intel.as. or intel.aanm.) and germanide.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2019/09/25 08:10

			IBM_TDB			
L36	3	"20130240989"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:11
L37	3	"6653700".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:11
L38	0	(glass or murthy or thani).in. and (intel.as. or intel.aanm.) and germanide.clm. and gradient.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:13
L39	6	(glass or murthy or thani).in. and (intel.as. or intel.aanm.) and germanide.clm. and gradient	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:13
L40	5	"20030057416"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:15
L41	3	"20080242037"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:15
L42	20	(glass or murthy or thani).in. and (intel.as. or intel.aanm.) and germanide.clm. and graded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:19
L43	14	(glass or murthy or thani).in. and (intel.as. or intel.aanm.) and germanide.clm. and graded.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:19
L44	13	"6607648"	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2019/09/25 08:23

			EPO; JPO; DERWENT; IBM_TDB			
L45	160	"6607948"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:24
L46	5	"6607948".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:24
L61	293	(US-20120153387-$ or US-20170012124-$ or US-20150206942-$ or US-20130248999-$ or US-20140001520-$ or US-20170047419-$ or US-20130240989-$ or US-20150060945-$ or US-20150333180-$ or US-20160322359-$ or US-20070187767-$ or US-20160190233-$ or US-20130277752-$ or US-20090224369-$ or US-20150311204-$ or US-20160118384-$ or US-20160372547-$ or US-20100244154-$ or US-20130034931-$ or US-20090194846-$ or US-20020042197-$ or US-20030057416-$ or US-20040266116-$ or US-20040262594-$ or US-20080242037-$ or US-20150372142-$).did. or (US-20150364561-$ or US-20150155359-$ or US-20100320606-$ or US-20090224368-$ or US-20080197412-$ or US-20170077244-$ or US-20090206370-$ or US-20160358826-$ or US-20060156080-$ or US-20170117277-$ or US-20080135878-$ or US-20080124878-$ or US-20130207166-$ or US-20160104673-$ or US-20170221724-$ or US-20090224256-$ or US-20130264639-$ or US-20090189189-$ or US-20160336446-$ or US-20050130454-$ or US-20070262296-$ or US-20140159159-$ or US-20130187171-$ or US-20170352597-$ or US-20080217658-$ or US-20170213889-$ or US-20130320449-$).did. or (US-20130320450-$ or US-20060166492-$ or US-20150108546-$ or US-20160163815-$ or US-20130264613-$ or US-20080119025-$ or US-20120119268-$ or US-20170373147-$ or US-20160111537-$ or US-20160211338-$ or US-20090090934-$ or US-20150008490-$ or US-20160064563-$ or US-20160020305-$ or US-20130154016-$ or US-20150236016-$ or US-20140264492-$ or US-20180190653-$ or US-20160254383-$ or US-20160240681-$ or US-20160240534-$ or US-20160155668-$ or US-20160148936-$ or US-20160087063-$ or US-20160087062-$ or US-20160086946-$ or US-20160056290-$).did. or (US-	US-PGPUB; USPAT; FPRS; JPO; DERWENT	OR	ON	2019/09/25 08:26

		20150380558-$ or US-20150318354-$ or US-20140363943-$ or US-20150295084-$ or US-20150279840-$ or US-20150069473-$ or US-20140306290-$ or US-20140103429-$ or US-20130313524-$ or US-20130270652-$ or US-20130241004-$ or US-20130200454-$ or US-20120068273-$ or US-20100148217-$ or US-20120001197-$ or US-20110089493-$ or US-20110062443-$ or US-20100078728-$ or US-20040063286-$ or US-20070196973-$ or US-20050266645-$ or US-20050116218-$ or US-20050045965-$ or US-20040198003-$ or US-20180174913-$ or US-20180145184-$ or US-20180108727-$).did. or (US-20180096885-$ or US-20180090582-$ or US-20180076203-$ or US-20180068904-$ or US-20170194434-$ or US-20170186748-$ or US-20170179301-$ or US-20170154990-$ or US-20170141235-$ or US-20170141199-$ or US-20170117291-$ or US-20170104101-$ or US-20170053918-$ or US-20160380056-$ or US-20160359022-$ or US-20160358940-$ or US-20150295089-$ or US-20160322479-$ or US-20180053763-$ or US-20180047824-$ or US-20180005904-$ or US-20170243868-$ or US-20170005173-$ or US-20150129891-$ or US-20170229342-$ or US-20130285155-$ or US-20090142899-$).did. or (US-20080242012-$ or US-20090035911-$ or US-20180076326-$ or US-20160087078-$ or US-20160005825-$ or US-20140167164-$ or US-20080265417-$ or US-20080116532-$ or US-20080029836-$ or US-20160027918-$ or US-20160293717-$ or US-20090273034-$ or US-20170352759-$ or US-20030006484-$ or US-20040251473-$ or US-20070122954-$ or US-20030124761-$ or US-20120161249-$ or US-20080311710-$ or US-20070164388-$ or US-20050237602-$ or US-20190259861-$ or US-20180315647-$ or US-20180315618-$ or US-20190035916-$ or US-20180248011-$ or US-20140027823-$).did. or (US-20190259835-$ or US-20190165135-$ or US-20190165156-$ or US-20140070377-$ or US-20120037998-$ or US-20110147828-$ or US-20100109044-$ or US-20070275548-$ or US-20140231914-$ or US-20110183486-$ or US-20110068407-$ or US-20100197092-$ or US-20100123198-$ or US-20090302348-$ or US-20090075029-$ or US-20080230805-$ or US-20080179752-$ or US-20080054347-$ or US-20070235802-$ or US-20070075378-$ or US-20070053381-$ or US-20070004123-$ or US-20060289856-$ or US-20060255330-$ or US-20060237746-$ or US-20060199622-$ or US-20060172511-$).did. or (US-20060148151-$ or US-20060138398-$ or US-20060065914-$ or US-20060060859-$					

		or US-20050184354-$ or US-20050145944-$ or US-20020197806-$ or US-20180068857-$ or US-20180083114-$ or US-20190259756-$ or US-20190259755-$ or US-20190067280-$ or US-20130189839-$).did. or (US-9484432-$ or US-8994104-$ or US-8901537-$ or US-9117791-$ or US-9349810-$ or US-9059024-$ or US-9224735-$ or US-9437691-$ or US-7880228-$ or US-5144410-$ or US-7732285-$ or US-5296387-$ or US-9397214-$ or US-9627384-$ or US-9722023-$ or US-9449885-$ or US-5656859-$ or US-7821044-$ or US-8575652-$ or US-9859424-$ or US-5516724-$ or US-9768077-$ or US-5214298-$ or US-4611388-$ or US-7238580-$ or US-8299455-$).did. or (US-9679961-$ or US-9966440-$ or US-9553031-$ or US-9978868-$ or US-9966471-$ or US-9905646-$ or US-9825036-$ or US-9793400-$ or US-9711417-$ or US-9698060-$ or US-9391171-$ or US-9379108-$ or US-9209261-$ or US-9917060-$ or US-9484255-$ or US-5710450-$ or US-6239029-$ or US-9754940-$ or US-9722082-$ or US-5644166-$ or US-6828602-$ or US-6939772-$ or US-10276400-$ or US-5725573-$ or US-10304927-$ or US-10297670-$ or US-7491643-$).did. or (US-6887762-$ or US-7682887-$ or US-7678631-$ or US-7663192-$ or US-9837357-$ or US-9059316-$ or US-9059096-$ or US-10236217-$ or US-9934977-$ or US-10056379-$ or US-10170308-$ or US-6653700-$).did. or (KR-20030057416-$ or WO-2012087403-$ or CN-103270598-$ or EP-2656393-$ or KR-20130111595-$ or EP-2656393-$ or KR-101489611-$ or JP-5644166-$ or KR-100976119-$ or KR-20090056763-$).did. or (JP-2013207231-$).did. or (US-9117791-$ or WO-2009101449-$ or WO-03025984-$ or US-20080242037-$ or US-20070187767-$ or US-5281552-$ or US-20070007590-$ or US-20150108546-$ or US-20120119297-$ or US-20120153387-$ or US-20160322359-$ or JP-2011225936-$ or US-20070122954-$ or EP-867701-$ or US-20090218640-$).did.				
L63	51	l61 and germanide near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:26
L64	51	l61 and germanide near10 (ti or titanium)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2019/09/25 08:26

			DERWENT; IBM_TDB			
L65	1	l61 and germanide near10 (ti or titanium).clm. and (graded or gradient).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:28
L66	1	l61 and germanide same (ti or titanium).clm. and (graded or gradient).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:28
L67	0	l61 and germanide same (ti or titanium).clm. and (graded or gradient).clm. and boron.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:28
L68	2	l61 and germanide same (ti or titanium).clm. and boron.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:29
L69	0	l61 and germanide same (ti or titanium) same boron.clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:29
L70	27	l61 and germanide same (ti or titanium) same boron	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:29
L71	25	"2008242037"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:31
L72	0	"20082042037"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:32
L73	2	"2008242037".pn.	US-PGPUB; USPAT; USOCR;	OR	ON	2019/09/25 08:32

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
L74	25	"2008242037"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:33
L75	3	"20080242037"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:33
L76	39	"2007187767"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:34
L77	2	"2007187767".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:34
L78	2	"20070187767".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:35
L79	3	"20030057416".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:36
L80	11	pre-contact near metallization	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:36
L81	2	"20060156080"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/09/25 08:37

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	16/416,445
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	First Named Inventor	Glenn A. GLASS, et al.
	Group Art Unit	2826
	Examiner Name	N/A
Sheet 1 of 3	Attorney Docket No: P38507USC2-C1	

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		US-20130240989	09-19-2013	Glenn Glass et al.	
		US-20140070377	03-13-2014	Yu et al.	

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		WO 2010-068530	06-17-2010	Intel Corporation		
		JP-2007-214481	08-23-2007	Toshiba Corp		
		CN-101622690	01-06-2010	Intel Corporation		
		JPH-07-169958	07-04-1995	NEC Corp		
		JPH-05-183160	07-23-1993	Toshiba Corp		
		JP-2007-318132	12-06-2007	IBM		
		JP-2007-036205	02-08-2007	Fujitsu Ltd.		
		JP-2006-186240	07-13-2006	Fujitsu Ltd.		
		JP-2012-510720	05-10-2012	Intel Corporation		

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Espacenet

Bibliographic data: CN101622690 (A) — 2010-01-06

Semiconductor device having self-aligned epitaxial source and drain extensions

Inventor(s): BERNHARD SELL; TAHIR GHANI; ANAND MURTHY; HARRY GOMEZ ± (SELL BERNHARD, ; GHANI TAHIR, ; MURTHY ANAND, ; GOMEZ HARRY)

Applicant(s): INTEL CORP ± (INTEL CORP)

Classification: **- international:*H01L21/20***
- cooperative: **H01L21/30608**; **H01L21/3065**; **H01L29/66545**; **H01L29/66628**; **H01L29/66636**; **H01L29/7848**; H01L21/26513; H01L29/165; H01L29/495; H01L29/4966; H01L29/517

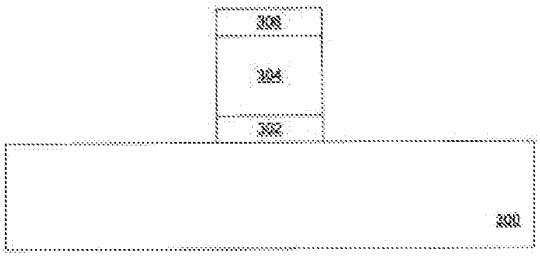
Application number: CN20088006389 20080326

Priority number (s): US20070729189 20070328

Also published as: DE112008000638 (B4) DE112008000638 (T5) JP2010520651 (A) JP5198478 (B2) KR101237664 (B1) KR20090125149 (A) US2008242037 (A1) US7732285 (B2) WO2008121659 (A1) less

Abstract of CN101622690 (A)

A method of forming a transistor with self-aligned source and drain extensions in close proximity to a gate dielectric layer of the transistor comprises forming a gate stack on a substrate, implanting a dopant into regions of the substrate adjacent to the gate stack, wherein the dopant increases the etch rate of the substrate and defines the location of the source and drain extensions, forming a pair of spacers on laterally opposite sides of the gate stack that are disposed atop the doped regions of the substrate, etching the doped regions of the substrate and portions of the substrate subjacent to the doped regions, wherein an etch rate of the doped regions is higher than an etch rate of the portions of the substrate subjacent to the doped regions, and depositing a silicon-based material in the etched portions of the substrate.



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DESCRIPTION CN101622690

A method of forming a transistor having a self-aligned source and drain extension that is in close proximity to a gate dielectric layer of a transistor includes: forming a gate stack on a substrate; implanting dopants into the substrate and In a region adjacent to the gate stack, wherein the dopant increases the etch rate of the substrate and defines the locations of the source and drain extensions; forming a pair of isolation layers on laterally opposite sides of the gate stack, The isolation layer is on top of the doped region of the substrate; the doped region of the etched substrate and the portion of the substrate under the doped region, wherein the doped region has an etch rate higher than the substrate is at the doping An etch rate of a portion below the impurity region; and depositing a silicon-based material in the etched portion of the substrate.

一种形成具有与晶体管的栅极电介质层非常接近的自对准源极和漏极延伸部分的晶体管的方法包括：在衬底上形成栅极叠置体；将掺杂剂注入到衬底与栅极叠置体相邻的区域中，其中掺杂剂增加衬底的蚀刻速率并限定源极和漏极延伸部分的位置；在栅极叠置体的横向相对侧上形成一对隔离层，所述隔离层位于衬底的掺杂区域的顶部上；蚀刻衬底的掺杂区域以及衬底位于掺杂区域下方的部分，其中所述掺杂区域的蚀刻速率高于衬底位于所述掺杂区域下方的部分的蚀刻速率；以及在衬底的蚀刻部分中沉积基于硅的材料。

Semiconductor device with self-aligned epitaxial source and drain extensions

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具有自对准外延源极和漏极延伸部分的半导体器件

Background technique

背景技术

Improvements in the performance of circuit devices on a substrate, such as integrated circuit (IC) transistors, resistors, capacitors, etc. on a semiconductor substrate, are often the primary considerations during the design, manufacture, and operation of these devices. For example, during the design and fabrication or formation of metal oxide semiconductor (MOS) transistor semiconductor devices such as those used in complementary metal oxide semiconductors (CMOS), it is often desirable to increase electrons in the N-type MOS device (NMOS) channel region. The motion and increase the motion of positively charged holes in the channel region of the P-type MOS device (PMOS).

衬底上的电路器件(例如半导体衬底上的集成电路(IC)晶体管、电阻器、电容器等)性能的提高通常是设计、制造和操作这些器件期间考虑的主要因素。例如，在设计与制造或形成诸如在互补金属氧化物半导体(CMOS)中使用的金属氧化物半导体(MOS)晶体管半导体器件期间，常常希望增大电子在N型MOS器件(NMOS)沟道区中的运动，并增大带正电荷的空穴在P型MOS器件(PMOS)沟道区中的运动。

One way to reduce the total resistance of a MOS device is to dope the region between the source/drain region and the channel region (referred to as the tip region of the MOS device). For example, dopants can be implanted in the source/drain regions and can be annealed to diffuse dopants into the channel region.

减小MOS器件总电阻的一种方法是对源极/漏极区和沟道区之间的区域(被称为MOS器件的尖端区域(tip region))进行掺杂。例如，可以在源极/漏极区中注入掺杂剂，并可以进行退火以使掺杂剂向沟道区扩散。

Because of the implantation and diffusion methods, the ability to control dopant concentration and position is limited. In addition, the dimensions of other parts of the MOS device, such as the thickness of its offset spacer, can also have a large impact on the position of the tip region. All of this in turn affects the ability of the tip region to maximize dopant concentration and access the channel region. Therefore, there is a need for improved methods or structures to overcome the limitations of conventional tip regions.

因为使用了注入和扩散方法，所以限制了控制掺杂剂浓度和位置的能力。此外，MOS器件其他部分的尺寸，例如其偏移隔离层(offset spacer)的厚度，也能够对尖端区域的位置产生很大的影响。所有这些又影响到尖端区域使掺杂剂浓度最大化并接近沟道区的能力。因此，需要改进的方法或结构来克服常规尖端区域的局限。

DRAWINGS

附图说明

Figure 1A shows a conventional MOS device including source and drain tip regions;

图1A示出了包括源极和漏极尖端区域的常规MOS器件；

Figure 1B shows a MOS device including source and drain epitaxial extensions;

图1B示出了包括源极和漏极外延延伸部分的MOS器件；

Figure 1C shows how the thickness of the isolation layer affects the etching of the epitaxial extension of the MOS device;

图1C示出了隔离层厚度是如何影响MOS器件的外延延伸部分的蚀刻 的；

Figure 1D is a graph showing the dependence of UC to UC distance on the thickness of the isolation layer;

图1D是示出UC到UC距离对隔离层厚度的依赖关系的曲线图；

2 is a method of forming source and drain epitaxial extensions in accordance with an embodiment of the present invention. ;

图2是根据本发明的实施方式形成源极和漏极外延延伸部分的方法。 ；

Figures 3A through 3I illustrate structures formed when the method of Figure 2 is performed;

图3A到3I示出了在执行图2的方法时形成的结构；

4 is a graph showing how the UC to UC distance of a MOS device formed in accordance with an embodiment of the present invention is less dependent on the thickness of the isolation layer.

图4是示出根据本发明的实施方式形成的MOS器件的UC到UC距离 如何较少地依赖于隔离层厚度的曲线图。

Detailed ways

具体实施方式

Described herein are systems and methods for forming epitaxial source and drain extensions in a MOS device. In the following description, various aspects of the exemplary embodiments will be described in terms of what is generally employed by those skilled in the art in However, it will be apparent to those skilled in the art that the present invention may be practiced using only some of the described aspects. For the purposes of explanation, specific quantities, materials, and constructions are set forth in order to provide a thorough understanding of the exemplary embodiments. However, it will be apparent to those skilled in the art that the present invention may be practiced without the specific details. In other instances, well-known features are omitted or simplified in order to avoid obscuring the exemplary embodiments.

这里所述的是在MOS器件中形成外延源极和漏极延伸部分的系统和 方法。 在以下描述中，将利用本领域技术人员为向其他本领域技术人员传 达其工作内容而通常采用的术语来描述示例性实施方式的各方面。 然而， 本领域的技术人员将会明了，可以仅利用一些所述方面来实施本发明。 出 于解释的目的，对具体的数量、材料和构造进行了阐述，以便对示例性实 施方式有透彻的理解。 然而，本领域的技术人员将会明了，可以在没有这 些具体细节的情况下实施本发明。 在其他情况下，省略或简化了公知特征， 以免使示例性实施方式不清楚。

The various operations are described as a plurality of discrete operations and, conversely, are described in a manner that is most helpful in understanding the invention. However, the order of the description should not be construed as implying that the operations are necessarily related to the order. In particular, it is not necessary to perform these operations in the order presented.

将把各个操作描述为多个分立的操作，反过来讲，也是以最有助于理 解本发明的方式来描述的，然而，不应将描述的顺序视为暗指这些操作必 定与顺序有关。 具体而言，不必按照所呈现的顺序来执行这些操作。

As a background art, conventional metal oxide semiconductor (MOS) transistors include source and drain "tip regions" which are designed to reduce the total resistance of the transistor while improving short channel effects. These tip regions are portions of the substrate that are implanted with dopants such as boron or carbon using implantation and diffusion techniques. A source tip region is formed in a region between the source region and the channel region. Similarly, the drain tip region is formed in a region between the drain region and the channel region. The tip region is minimally diffused below the gate dielectric layer of the transistor.

作为背景技术，常规金属氧化物半导体(MOS)晶体管包括源极和漏 极“尖端区域”，设计所述尖端区域以降低晶体管的总电阻，同时改善短沟 道效应。 这些尖端区域是衬底中利用注入和扩散技术注入了诸如硼或碳的 掺杂剂的部分。 源极尖端区域形成在源极区和沟道区之间的区域中。 类似 地，漏极尖端区域形成在漏极区和沟道区之间的区域中。 尖端区域最小限 度地在晶体管的栅极电介质

层下方扩散。

FIG. 1A shows a conventional MOS transistor 100A formed on a substrate 102. The source region 110 and the drain region 112 are typically formed by implanting a dopant such as boron into the substrate or by etching the substrate and then epitaxially depositing silicon or silicon germanium material. A gate stack 122 is formed on top of the channel region 120 of the transistor 100A. The gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104. A pair of isolation layers 108 are formed adjacent to the gate stack 122.

图1A示出了形成在衬底102上的常规MOS晶体管100A。通常通过将诸如硼的掺杂剂注入到衬底中或通过蚀刻衬底，然后外延沉积硅或硅锗材料来形成源极区110和漏极区112。栅极叠置体122形成在晶体管100A的沟道区120的顶部。栅极叠置体122包括栅极电介质层106和栅电极104。形成一对隔离层108使其与栅极叠置体122相邻。

As is known in the art, the isolation layer 108 typically produces a distance of between about 10 and 20 nanometers (nm) between the edge of the gate dielectric layer 106 and the edge of each of the source and drain regions 110/112. It is within this interval that the source tip region 110A and the drain tip region 112A are formed. The tip region 110A/112A overlaps the isolation layer 108 and may overlap or under the gate dielectric layer 106 by a distance of less than 10 nm.

如本领域所公知的，隔离层108一般在栅极电介质层106的边缘与源极和漏极区110/112中的每一个的边缘之间产生大约10到20纳米(nm)的距离。就是在这一间隔之内形成源极尖端区域110A和漏极尖端区域112A。尖端区域110A/112A与隔离层108重叠，并且可以与栅极电介质层106重叠或在其下方扩散少于10nm的距离。

The source tip region 110A and the drain tip region 112A are typically fabricated using implantation and diffusion techniques. First, a dopant is implanted into the source region 110 and the drain region 112. Doping agents which may be used include, but are not limited to, boron, arsenic, antimony, phosphorus, indium, or antimony. The doping amount may be in the range of 1 × 10 < 14 > to 1 × 10 < 16 > atoms / cm < 3 >. Transistor 100A is then annealed to diffuse dopants into channel region 120. The dopant can also be implanted further into those regions between the gate dielectric layer 106 and the source/drain regions 110/112 using a tilted ion implantation technique.

通常利用注入和扩散技术制造源极尖端区域110A和漏极尖端区域112A。首先，将掺杂剂注入到源极区110和漏极区112中。可以使用的掺杂剂包括但不限于硼、砷、锑、磷、铟、或锑。掺杂剂量可以在1×10<14>到1×10<16>原子/cm<3>的范围内。然后对晶体管100A进行退火，以使掺杂剂向沟道区120扩散。也可以使用倾斜离子注入技术进一步将掺杂剂注入到栅极电介质层106和源极/漏极区110/112之间的那些区域中。

Unfortunately, as will be appreciated by those skilled in the art, the shape of the tip region 110A/112A, the distance the dopant penetrates under the spacer layer 108, and the concentration gradient of the tip region 110A/112A all depend on the dopant. Diffusion properties in the substrate material. For example, the concentration of the tip region will be higher near the source/drain regions 110/112 and lower near the channel region 120. Although highly desirable, it is almost impossible to make the dopant concentration very high near the channel region 120 without driving the dopant into the channel region 120. Furthermore, the source and drain regions 110/112 cannot be moved closer to the channel region 120 because dopants may be driven into the channel region 120 again. This limits the extent to which the source and drain regions 110/112 are formed in close proximity to the channel region 120, thereby limiting the extent to which the gate length can be reduced.

令人遗憾的是，如本领域技术人员将认识到的，尖端区域110A/112A 的形状、掺杂剂在隔离层108下方渗透的距离以及尖端区域110A/112A的 浓度梯度全部取决于掺杂剂在衬底材料中的扩散特性。 例如，尖端区域的 浓度在靠近源极/漏极区110/112之处将较为高，而在靠近沟道区120之处 将为低。 尽管非常希望，但是在不将掺杂剂驱动到沟道区120中的情况下 几乎不可能使掺杂剂浓度在靠近沟道区120之处非常高。 此外，源极和漏 极区110/112不能被移动得更靠近沟道区120，因为可能再次将掺杂剂驱动 到沟道区120中。 这限制了将源极和漏极区110/112形成为与沟道区120所 能靠近的程度，由此限制了可以将栅极长度缩小到什么程度。

Figure 1B shows an improved MOS transistor 100B formed on a substrate 102 using source and drain "extensions". Rather than implanting and diffusing dopants under isolation layer 108 to form the tip regions, MOS transistor 100B uses undercut etching to allow source regions 110 and drain regions 112 to extend to isolation layer 108 and gate dielectric layer 106. Below. The portion of the source/drain regions 110/112 extending below the isolation layer 108 is referred to as a source extension portion 110B and a drain extension portion 112B. The source and drain extensions 110B/112B replace the less desirable tip regions 110A/112A shown in Figure 1A.

图1B示出了利用源极和漏极“延伸部分”形成在衬底102上的改进的 MOS晶体管100B。 并非是在隔离层108下方注入和扩散掺杂剂以形成尖端 区域，MOS晶体管100B而是使用底切蚀刻，以允许源极区110和漏极区 112延伸到隔离层108和栅极电介质层106的下方。 在此将源极/漏极区 110/112延伸到隔离层108下方的部分称为源极延伸部分110B和漏极延伸 部分112B。 源极和漏极延伸部分110B/112B取代了图1A所示的较不理想 的尖端区域110A/112A。

The source/drain regions 110/112 and the source/drain extensions 110B/112B are formed by etching the substrate, including undercutting the isolation layer, and then epitaxially depositing a silicon or silicon germanium material. The source and drain extensions 110B/112B are thus formed in the same process steps as the source and drain regions 110/112, which reduces the total number of process steps. The source and drain extensions 110B/112B also provide other advantages with respect to the source/drain tip regions 110A/112A. For example, unlike conventional tip regions, the lattice structure of source/drain extensions 110B/112B causes strain

in channel region 120, which increases electron mobility and thus reduces resistance in the channel.

通过蚀刻衬底，包括对隔离层进行底切，然后外延沉积硅或硅锗材料 来形成源极/漏极区110/112和源极/漏极延伸部分110B/112B。 因此在与源 极和漏极区110/112相同的工艺步骤中形成了源极和漏极延伸部分 110B/112B，这减少了工艺步骤的总数。 源极和漏极延伸部分110B/112B相 对于源极/漏极尖端区域110A/112A还提供了其他优点。 例如，与常规尖端 区域不同，源极/漏极延伸部分110B/112B的晶格结构在沟道区120中引起 应变，其增加了电子迁移率并因此减小了沟道中的电阻。

Another advantage is that the interface between the source/drain extensions 110B/112B and the substrate material 102 forming the channel region 120 is abrupt. On one side of the interface is an epitaxially deposited doped silicon material, and on the other side of the interface is a substrate material constituting the channel region 120. This configuration enables the epitaxial source/drain extensions 110B/112B to bring the heavily doped silicon material very close to the channel region 120. The dopants in the epitaxial source/drain extensions 110B/112B are substantially or completely retained in the extension without tending to diffuse into the channel region 120.

另一个优点是源极/漏极延伸部分110B/112B和形成沟道区120的衬底 材料102之间的界面是陡峭的(abrupt)。 在界面的一侧是外延沉积的掺杂 硅材料，在界面的另一侧是构成沟道区120的衬底材料。这种结构使得外 延源极/漏极延伸部分110B/112B能够使重掺杂硅材料非常靠近沟道区120。 外延源极/漏极延伸部分110B/112B中的掺杂剂基本或完全保持在延伸部分 中，而不趋向于扩散到沟道区120中。

Unfortunately, conventional methods of forming source and drain extensions 110B/112B have some disadvantages. A disadvantage is shown in Figures 1B and 1C. As shown, conventional undercut etching techniques result in a sub-bore region forming a bullet-shaped profile. In other words, more substrate material is etched at a lesser distance below the gate dielectric layer 106 than at a substrate material that is directly etched adjacent the gate dielectric layer 106. Thus, the source extension portion 110B and the drain extension portion 112B also each have a bullet-shaped profile, which produces a less than optimal strain in the channel region 120. In addition, there are many variations in the resulting final source and drain extensions 110B/112B due to many variations in conventional undercut etch techniques.

令人遗憾的是，形成源极和漏极延伸部分110B/112B的常规方法有一 些缺点。 在图1B和1C中示出了一种缺点。 如图所示，常规的底切蚀刻技 术导致底切区域形成了子弹形轮廓。 换言之，在栅极电介质层106下方少 许距离处被蚀刻的衬底材料多于在直接与栅极电介质层106相邻处被蚀刻 的衬底材料。 这样一来，源极延伸部分110B和漏极延伸部分112B也各自 具有子弹形轮廓，这在沟道区120中产生了并非最理想的应变。 此外，因 为在常规底切蚀刻技术中有很多变化，因此在所形成的最终源极和漏极延 伸部分110B/112B中往往有很多变化。

Another disadvantage of conventional methods of forming source and drain extensions 110B/112B relates to the

effect of isolation layer thickness on undercut etching, as shown in Figures 1B and 1C. Beginning with FIG. 1B, the illustrated MOS transistor 100B has an offset isolation layer 108 having a first thickness x1. A substrate etch is performed to undercut the isolation layer 108 and a portion of the gate dielectric layer 106 to form source and drain extensions 110B/112B. The undercut tangent (UC to UC) distance 114 separates the source extension portion 110B from the drain extension portion 112B.

形成源极和漏极延伸部分110B/112B的常规方法的另一缺点涉及隔离层厚度对底切蚀刻的影响，如图1B和1C所示。从图1B开始，所示的MOS晶体管100B具有偏移隔离层108，其具有第一厚度x1。进行衬底蚀刻，以对隔离层108和栅极电介质层106的一部分进行底切，从而能够形成源极和漏极延伸部分110B/112B。底切到底切(UC到UC)距离114将源极延伸部分110B与漏极延伸部分112B分隔开。

Turning to FIG. 1C, MOS transistor 100C is shown having an offset isolation layer 108 having a thickness of x2. Here, the thickness x2 is much larger than the thickness x1 of the isolation layer 108 in FIG. 1B. As a result, the thicker isolation layer 108 pushes the undercut etch while the substrate is being etched, and the source/drain extensions 110B/112B are formed further away from the channel region 120 of the transistor 100C. Therefore, the substrate etching undercuts a small surface area under the MOS transistor 100C. Therefore, the UC to UC distance 116 of the MOS transistor 100C is much larger than the UC to UC distance 114 of the MOS transistor 100B. Unfortunately, changing the UC to UC distance in this way causes a large drive current change to the MOS transistor.

转到图1C，所示的MOS晶体管100C具有厚度为x2的偏移隔离层108。这里，厚度x2比图1B中的隔离层108的厚度x1大得多。结果，在进行衬底蚀刻时，较厚的隔离层108推出底切蚀刻，并且使源极/漏极延伸部分110B/112B形成得更加远离晶体管100C的沟道区120。因此，衬底蚀刻底切了较少的MOS晶体管100C下方的表面区域。因此，MOS晶体管100C的UC到UC距离116比MOS晶体管100B的UC到UC距离114大得多。令人遗憾的是，通过这种方式改变UC到UC距离给MOS晶体管造成大的驱动电流变化。

FIG. 1D is a graph showing how the thickness of the spacer affects the UC to UC distance in a device formed by a known method. The graph provides data represented by line 118, showing that as the thickness of the isolation layer increases, the UC to UC distance also increases, resulting in large drive current variations. Typically, the UC to UC distance is increased by about 2 nm for each nanometer (nm) increase in the thickness of the isolation layer. Thus, forming the source/drain extensions using conventional methods allows the thickness of the offset isolation layer to have a large effect on the performance of the MOS device.

图1D为示出了在利用公知方法形成的器件中隔离层厚度如何影响UC到UC距离的曲线图。该曲线图提供了由线118表示的数据，示出了随着隔离层厚度的增加，UC到UC距离也增加，导致大的驱动电流变化。典型地，隔离层厚度每增加一纳米(nm)，UC到UC距离增加大约2nm。这样一来，使用常规方法形成源极/漏极延伸部分允许偏移隔离层的厚度对MOS器件的性能有巨大影响。

In order to address the above problems, embodiments of the present invention provide methods of forming novel, self-aligned and epitaxially deposited source and drain extensions. The epitaxial source and drain extensions of the present invention place the highly doped silicon material very close to the channel region of the MOS transistor. And because the source and drain extensions are self-aligned, they are much less affected by the thickness of the offset isolation layer than conventional processes.

为了解决上述这些问题，本发明的实施方式提供了形成新颖的、自对准和外延沉积的源极和漏极延伸部分的方法。本发明的外延源极和漏极延伸部分将高掺杂硅材料设置得非常靠近MOS晶体管的沟道区。并且因为源极和漏极延伸部分是自对准的，所以相对于常规工艺而言，它们受偏移隔离层厚度的影响要小得多。

2 is a method 200 of constructing a MOS transistor having self-aligned epitaxial source and drain extensions. 3A through 3E illustrate structures formed when the method 200 of FIG. 2 is performed.

图2是构建具有自对准外延源极和漏极延伸部分的MOS晶体管的方法200。图3A到3E示出了在执行图2的方法200时形成的结构。

The method 200 begins with a semiconductor substrate on which a MOS device such as a MOS transistor can be formed (process 202 of FIG. 2). The semiconductor substrate can be formed using bulk silicon or a silicon-on-insulator underlayer structure. In other embodiments, other materials may be used to form the semiconductor substrate. Other materials may or may not be combined with silicon, including but not limited to germanium, antimony telluride, lead telluride, indium arsenide, indium phosphide, Gallium arsenide or gallium antimonide. Although some examples of materials that can form a substrate are described herein, any material that can serve as a basis for making a semiconductor device is within the spirit and scope of the present invention.

方法200以半导体衬底开始，在所述半导体衬底上可以形成诸如MOS晶体管的MOS器件(图2的工艺202)。可以利用体硅或绝缘体上硅底层结构形成半导体衬底。在其他实施方式中，可以利用其他材料形成半导体衬底，其他材料可以与硅结合或可以不与硅结合，包括但不限于锗、锑化铟、碲化铅、砷化铟、磷化铟、砷化镓或锑化镓。虽然这里描述了可以形成衬底的一些材料范例，但是可以充当可制造半导体器件的基础的任何材料都落在本发明的精神和范围内。

A gate stack (204) is formed on the semiconductor substrate. In some embodiments of the invention, the gate stack can be formed by depositing and then patterning the gate dielectric layer and the gate electrode layer. For example, in one embodiment, the gate dielectric layer can be blanketed using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Deposited onto a semiconductor substrate. Other deposition techniques can also be used, for example, the gate dielectric layer can be thermally grown. Next, a gate electrode material can be

deposited on the gate dielectric layer using a similar deposition technique such as ALD, CVD or PVD. In some embodiments, the gate electrode material is a polysilicon or metal layer. In some embodiments, the gate electrode material is a sacrificial material that can later be removed to perform a replacement metal gate process. A conventional patterning process can then be performed to etch away portions of the gate electrode layer and the gate dielectric layer to form a gate stack.

在半导体衬底上形成栅极叠置体(204)。在本发明的一些实施方式中，可以通过沉积然后对栅极电介质层和栅电极层进行构图来形成栅极叠置 体。例如，在一种实施方式中，可以利用诸如化学气相沉积(CVD)、原子 层沉积(ALD)、旋涂沉积(SOD)或物理气相沉积(PVD)的常规沉积工 艺将栅极电介质层均厚沉积到半导体衬底上。也可以使用其他沉积技术，例如，可以热生长栅极电介质层。接下来，可以利用诸如ALD、CVD或 PVD的类似沉积技术在栅极电介质层上沉积栅电极材料。在一些实施方式 中，栅电极材料为多晶硅或金属层。在一些实施方式中，栅电极材料为后 来可以去除以进行替换金属栅极工艺的牺牲材料。然后可以执行常规的构 图工艺，以蚀刻掉部分栅电极层和栅极电介质层，从而形成栅极叠置体。

The gate dielectric material can be formed from a material such as silicon dioxide or a high-k dielectric material. Examples of high-k gate dielectric materials that may be used include, but are not limited to, hafnium oxide, hafnium silicon oxide, hafnium oxide, hafnium aluminum oxide, zirconium oxide, zirconium oxide silicon, hafnium oxide, titanium oxide, niobium oxide, niobium oxide , bismuth oxide titanium oxide, cerium oxide, aluminum oxide, lead oxide bismuth and lead zinc citrate. In some embodiments, the high-k gate dielectric layer can have a thickness of about 5 angstroms to about

可以由诸如二氧化硅或高k电介质材料的材料形成栅极电介质材料。可以使用的高k栅极电介质材料的范例包括但不限于氧化铪、氧化铪硅、 氧化镧、氧化镧铝、氧化锆、氧化锆硅、氧化钽、氧化钛、氧化钡锶钛、 氧化钡钛、氧化锶钛、氧化钇、氧化铝、氧化铅钪钽和铌酸铅锌。在一些 实施方式中，高k栅极电介质层的厚度可以在大约5埃 到大约

between. In other embodiments, additional processing, such as an annealing process, can be performed on the high-k gate dielectric layer to improve the quality of the high-k material.

之间。在其他实施方式中，可以对高k栅极电介质层进行额外的处理，例 如退火工艺，以改善高k材料的质量。

FIG. 3A shows a substrate 300 on which a gate stack is formed. In the embodiments described herein, the gate stack can include a high-k gate dielectric layer 302 and a sacrificial gate electrode 304. In other embodiments, the gate stack can include a silicon dioxide gate dielectric layer and a polysilicon gate electrode. The gate stack can

also include a gate hard mask layer 306 that can provide certain advantages or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. In an embodiment of the invention, the hard mask layer 306 can be formed using a material conventionally used as a hard mask, such as a conventional dielectric material.

图3A示出了其上形成栅极叠置体的衬底300。在这里所述的实施方式 中，栅极叠置体可以包括高k栅极电介质层302和牺牲栅电极304。在其他 实施方式中，栅极叠置体可以包括二氧化硅栅极电介质层和多晶硅栅电极。栅极叠置体还可以包括栅极硬掩模层306，其在处理期间可以提供某些优点或用处，例如保护栅电极304不受随后的离子注入工艺的影响。在本发明 的实施方式中，可以利用常规用作硬掩模的材料，例如常规电介质材料来 形成该硬掩模层306。

After forming the gate stack, an ion implantation process is performed to highly dope the portion of the substrate adjacent to the gate stack (206). According to an embodiment of the present invention, a dopant used in an ion implantation process in which the dopant is to be implanted is selected based on its ability to increase the etching rate of the substrate material. The particular dopant selected for the ion implantation process can vary depending on the substrate material and the etchant used in the subsequent etching process. Since most substrates contain large silicon, germanium or antimonide compositions, dopants that increase the etch rate of silicon, germanium or indium antimonide are often selected.

在形成栅极叠置体之后，执行离子注入工艺以对与栅极叠置体相邻的 衬底部分进行高掺杂(206)。根据本发明的实施方式，基于其增加衬底材 料的蚀刻速率的能力来选择在离子注入工艺中使用的掺杂剂，在所述衬底 材料中要注入所述掺杂剂。为离子注入工艺选择的特定掺杂剂可以根据衬 底材料和在随后的蚀刻工艺中使用的蚀刻剂而变化。由于大部分衬底包含 大的硅、锗或锑化铟成分，所以常常选择可以增加硅、锗或锑化铟的蚀刻 速率的掺杂剂。

In embodiments of the invention, specific dopants that may be selected to increase the etch rate of the substrate include, but are not limited to, carbon, phosphorus, and arsenic. For example, the implantation energy between 5 and 15 kilo-electron volts (keV) may be utilized to use carbon at a dose ranging from 1 x 10 < 14 > to 1 x 10 < 16 > atoms/cm < 3 >. Phosphorus may be used at a dose ranging from 1 x 10 < 14 > to 5 x 10 < 15 > atoms/cm < 3 > with an implantation energy between 1 and 5 keV. The implantation energy between 2 and 5 keV can be utilized to use arsenic at a dose ranging from 1 x 10 < 14 > to 5 x 10 < 15 > atoms/cm < 3 >.

在本发明的实施方式中，可以选择的用来增加衬底的蚀刻速率的特定 掺杂剂包括但不限于碳、磷和砷。例如，可以利用5到15千电子伏(keV) 之间的注入能量，以在1×10<14>到1×10<16>原子/cm<3>范围内的剂量使用碳。可以利用1到5keV之间的注入能量，以1×10<14>到5×10<15>原子/cm<3>范围内 的剂量使用磷。可以利用2到5keV之间的注入能量，以在1×10<14>到5× 10<15>原子/cm<3>范围内的剂量使用砷。

In an embodiment of the invention, ion implantation occurs substantially in a vertical direction (i.e., a direction perpendicular to the substrate). In some embodiments, at least a portion of the ion implantation can occur in a tilting direction to implant ions below the gate stack. As described above, if the gate electrode contains metal, a dielectric hard mask can be formed on the gate stack to prevent doping of the metal gate electrode.

在本发明的实施方式中，离子注入基本发生在垂直方向(即垂直于衬 底的方向)上。 在一些实施方式中，离子注入的至少一部分可以发生在倾 斜方向上，以将离子注入到栅极叠置体的下方。 如上所述，如果栅电极包 含金属，那么可以在栅极叠置体上形成电介质硬掩模，以防止对金属栅电 极的掺杂。

Next, an anneal is performed to further drive the dopant into the substrate and reduce any damage experienced by the substrate during the ion implantation process (207). The implantation and subsequent annealing can drive the ions to a substrate depth between 2 nm and 20 nm. Annealing can be carried out at temperatures between 700 ° C and 1100 ° C for up to one minute, for example for five seconds.

接下来，执行退火，以进一步将掺杂剂驱动到衬底中，并减小离子注 入工艺期间衬底所受到的任何损害(207)。 注入和随后的退火可以将离子 驱动到2nm到20nm之间的衬底深度。 退火可以在700° C到1100° C之间的 温度下持续最高达一分钟的时间，例如持续五秒的时间。

FIG. 3B shows the substrate 300 after the ion implantation and diffusion process. As shown, the ion implantation process produces two doped regions 308 adjacent to the gate dielectric layer 302. When exposed to a suitable etchant, the etch rate of doped region 308 will be higher than the etch rate of the surrounding substrate material. One of the doped regions 308 will serve as part of the source region of the MOS transistor being formed, including the self-aligned epitaxial source extension. Another doped region 308 will serve as part of the drain region of the MOS transistor, including a self-aligned epitaxial drain extension. In the illustrated embodiment, a portion of the doped region 308 is located below the gate dielectric layer 302. In various embodiments of the invention, the dimensions of the doped regions 308, including their depth, may vary depending on the requirements of the MOS transistor being formed.

图3B示出了离子注入和扩散工艺之后的衬底300。 如图所示，离子注 入工艺产生了两个与栅极电介质层302相邻的掺杂区308。 当暴露于适当的 蚀刻剂时，掺杂区308的蚀刻速率将高于周围衬底材料的蚀刻速率。 掺杂 区308之一将用作正形成的MOS晶体管的源极区的一部分，包括自对准外 延源极延伸部分。 另一个掺杂区308将用作MOS晶体管的漏极区的一部分， 包括自对准外延漏极延伸部分。 在所示的实施方式中，掺杂区308的一部 分位于栅极电介质层302的下方。 在本发明的各实施方式中，掺杂区308 的尺寸，包括它们的深度，可以根据正形成MOS晶体管的要求而变化。

Next, an isolation layer (208) is formed on either side of the gate stack. The spacer layer can be formed using conventional materials including, but not limited to, silicon oxide or silicon nitride. The width of the isolation

layer can be selected based on the design requirements of the MOS transistor being formed. According to an embodiment of the invention, the width of the isolation layer is not constrained by the design caused by the formation of the epitaxial source and drain extensions. FIG. 3C shows substrate 300 with isolation layer 310 formed on either side of gate electrode layer 304 and gate dielectric layer 302.

接下来，在栅极叠置体的任一侧上形成隔离层(208)。可以使用常规 材料，包括但不限于氧化硅或氮化硅来形成隔离层。可以基于正形成的MOS 晶体管的设计要求选择隔离层的宽度。根据本发明的实施方式，隔离层的 宽度不受形成外延源极和漏极延伸部分所造成的设计约束。图3C示出了衬底300，在栅电极层304和栅极电介质层302的任一侧上形成隔离层310。

After the isolation layer is formed on the substrate, a dry etching process may be performed to etch the doped regions and etch a portion of the substrate to form a cavity in which the source/drain regions and the source/drain extension portions may be formed (210). The etched cavity is adjacent to the gate stack. The etched cavity can be formed to a depth of between 50 nm and 1500 nm which is deeper than the doped region. Therefore, the etching process will remove the substrate material underlying the doped regions.

在衬底上形成隔离层之后，可以执行干法蚀刻工艺以蚀刻掺杂区并蚀 刻部分衬底，以形成可以在其中形成源极/漏极区和源极/漏极延伸部分的空 腔(210)。所蚀刻的空腔与栅极叠置体相邻。可以将所蚀刻的空腔形成到 50nm到1500nm之间的深度，该深度比掺杂区深。因此，蚀刻工艺将去除 位于掺杂区下方的衬底材料。

The dry etch process uses an etchant formulation that is complementary to the dopant used in the ion implantation process to increase the etch rate of the doped regions. This allows the etching process to remove the doped regions at a faster rate than other portions of the substrate. Thus, with an appropriate increase in the etch rate, the etch process can remove all of the material from the doped region substrate when the cavity is etched. This includes the doped regions undercutting the isolation layer and portions of the gate dielectric layer to define a self-aligned extension of the transistor. Increasing the etch rate of the doped regions allows the etched source and drain extension portions of the cavity to undercut the isolation layer and the gate dielectric layer, while the UC to UC distance is substantially independent of variations such as isolation layer thickness, dry etch process And the influence of other process change factors.

干法蚀刻工艺使用与离子注入工艺中使用的掺杂剂互补的蚀刻剂配 方，以提高掺杂区的蚀刻速率。这使得蚀刻工艺能够以快于衬底的其他部 分的速率去除掺杂区。这样一来，利用蚀刻速率的适当增加，蚀刻工艺能 够到完成空腔的蚀刻时从掺杂区基板去除所有的材料。这包括掺杂区底切 隔离层和栅极电介质层的部分，从而限定晶体管的自对准延伸架构。增加 掺杂区的蚀刻速率使得所蚀刻的源极和漏极延伸部分空腔能够底切隔离层 和栅极电介质层，而UC到UC距离基本不受诸如隔离层厚度、干法蚀刻工 艺的变化和其他工艺变化的因素的影响。

According to an embodiment of the present invention, the dry etching process may use chlorinated chemistry occurring in a plasma reaction chamber. In one embodiment, the etchant formulation can be comprised of a combination of NF3 and Cl2, with argon or helium used as a buffer gas or carrier gas. The flow rate of the active etchant species can vary from 50 to 200 standard cubic centimeters per minute (SCCM), while the carrier gas flow rate can vary from 150 to 400 SCCM. A high energy plasma can be used with a low RF bias of less than 100 W at powers ranging from 700 W to 1100 W. The reaction chamber pressure can range from about 1 Pascal (Pa) to about 2 Pa.

根据本发明的实施方式，干法蚀刻工艺可以使用发生在等离子体反应室中的氯化化学(chlorinated chemistry)。在一种实施方式中，蚀刻剂配方可以由NF3和Cl2的组合构成，其中将氩或氦用作缓冲气体或载气。活性蚀刻剂物质的流速可以在50到200标准立方厘米每分钟(SCCM)之间变化，而载气的流速可以在150到400SCCM之间变化。可以在700W到1100W范围内的功率下，以小于100W的低RF偏置，使用高能量等离子体。反应室压力可以在大约1帕斯卡(Pa)到大约2Pa的范围内。

In another embodiment, the etchant chemistry can be comprised of a combination of HBr and Cl2. The flow rate of the etchant species can vary from 40 SCCM to 100 SCCM. A high energy plasma can be used with a low RF bias of less than 100 W at powers ranging from about 600 W to about 1000 W. The reaction chamber pressure can range from about 0.3 Pa to about 0.8 Pa. In another embodiment, the etchant chemistry can be comprised of a combination of SE6 and Cl2. The flow rate of SF6 can vary from 3 SCCM to 10 SCCM, and the flow rate of Cl2 can vary from 20 SCCM to 60 SCCM. High energy plasma can be used at powers ranging from about 400 W to about 900 W without RF bias or with RF bias of less than 50 W. In this embodiment, a low flow rate of SF6 and reaction chamber pressure can be maintained to reduce the removal rate and maximize control. For example, the reaction chamber pressure can range from about 0.1 Pa to about 0.5 Pa. In another embodiment, the etchant chemistry can be composed of a combination of Ar and Cl2. Here, the flow rate of the etchant substance may vary from 40 SCCM to 80 SCCM. A medium energy plasma can be used at high RF biases between about 100 W and 200 W at powers ranging from about 400 W to about 800 W. The reaction chamber pressure can range from about 1 Pa to about 2 Pa.

在另一实施方式中，蚀刻剂化学物质可以由HBr和Cl2的组合构成。蚀刻剂物质的流速可以在40SCCM到100SCCM之间变化。可以在大约600W到大约1000W范围内的功率下，以小于100W的低RF偏置，使用高能量等离子体。反应室压力可以在大约0.3Pa到大约0.8Pa的范围内。在另一实施方式中，蚀刻剂化学物质可以由SE6和Cl2的组合构成。SF6的流速可以在3SCCM到10SCCM之间变化，Cl2的流速可以在20SCCM到60 SCCM之间变化。可以在大约400W到大约900W范围内的功率下，在没有RF偏置的情况下或以小于50W的RF偏置，使用高能量等离子体。在这种实施方式中，可以保持低的SF6的流速和反应室压力，以降低去除速率并使控制最大化。例如，反应室压力可以在大约0.1Pa到大约0.5Pa的范围内。在另一实施方式中，蚀刻剂化学物质可以由Ar和Cl2的组合构成。这里，蚀刻剂物质的流速可以在40SCCM到80SCCM之间变化。可以在从大约400W到大约800W范围内的功率下，以大约100W到200W之间的高RF偏置，使用中等能量等离子体。反应室压力可以在大约1Pa到大约2Pa的范围内。

FIG. 3D shows the substrate 300 after the dry etching process has been performed. As shown, a source region cavity 312 and a drain region cavity 314 are formed. Further, the source extension portion cavity 312A and the drain extension portion cavity 314A have been formed by etching the doping region 308. The thickness of the isolation layer 310 has the least effect on the etched source extension cavity 312A and the drain extension cavity 314A due to the dopant and etchant formulation that increases the etch rate of the doped region 308.

图3D示出了已经执行干法蚀刻工艺之后的衬底300。如图所示，形成了源极区空腔312和漏极区空腔314。此外，已经通过蚀刻掺杂区308形成源极延伸部分空腔312A和漏极延伸部分空腔314A。由于使用了增加掺杂区308的蚀刻速率的掺杂剂和蚀刻剂配方，隔离层310的厚度对蚀刻源极延伸部分空腔312A和漏极延伸部分空腔314A的影响最小。

After the dry etching process is completed, a wet etching process may be applied to clean and further etch the source region cavity 312, the source extension portion cavity 312A, the drain region cavity 314, and the drain extension portion cavity 314A (212). Conventional wet etching chemistries known in the art for cleaning silicon and oxide materials can be used. For example, a wet etch chemistry capable of removing silicon along the crystal face can be used.

在完成干法蚀刻工艺之后，可以应用湿法蚀刻工艺，以清洁和进一步蚀刻源极区空腔312、源极延伸部分空腔312A、漏极区空腔314以及漏极延伸部分空腔314A(212)。可以使用现有技术中公知的用于清洁硅和氧化物材料的常规湿法蚀刻化学物质。例如，可以使用能够沿晶面去除硅的湿法蚀刻化学物质。

Wet etching is used for at least two purposes. First, wet etching removes contaminants such as carbon, fluorine, chlorofluorocarbons, and oxides such as silicon oxide to provide a clean surface on which subsequent processing can be performed. Second, wet etching removes thin portions of the substrate along the <111> and <001> crystal faces to provide a smooth surface on which high quality epitaxial deposition can occur. The thin portion of the etched substrate can be up to 5 nm thick and can also remove residual contaminants. As shown in Fig. 3E, the wet etching causes the edges of the source region cavity 312, the source extension portion 312A, the drain region cavity 314, and the drain extension portion 314A to follow the <111> and <001> crystal faces. It should also be noted that the source and drain extensions 312A and 314A do not have a bullet-shaped profile that occurs during conventional processing.

湿法蚀刻至少用于两个目的。首先，湿法蚀刻去除诸如碳、氟、含氯氟烃的污染物以及诸如氧化硅的氧化物，以提供可以在其上执行后续处理的清洁表面。其次，湿法蚀刻沿着<111>和<001>晶面去除衬底的薄部分，以提供可以在其上发生高质量外延沉积的光滑表面。所蚀刻掉的衬底的薄部分可最高达5nm厚，并且还可以去除残余污染物。如图3E所示，湿法蚀刻使得源极区空腔312、源极延伸部分312A、漏极区空腔314和漏极延伸部分314A的边缘沿着<111>和<001>晶面。还应当指

出，源极和漏极延伸 部分312A和314A不具有在常规处理中发生的子弹形轮廓。

The remainder of the process for forming MOS transistors is similar to conventional MOS processing techniques. For example, after the etch process, the source and drain region cavities, including the source and drain extensions (214), may be filled with a silicon alloy using a selective epitaxial deposition process. Thus, the epitaxial deposition forms source and drain regions and source and drain extensions in a single process. In some embodiments, the silicon alloy can be in-situ doped silicon germanium, in-situ doped silicon carbide, or in-situ doped silicon. In alternative embodiments, other silicon alloys can be used. For example, optional silicon alloy materials that may be used include, but are not limited to, nickel silicide, titanium silicide, cobalt silicide, and may be doped with one or more of boron and/or aluminum. In some embodiments, deposition can be performed using a CVD process.

用于形成MOS晶体管的工艺的其余部分类似于常规的MOS处理技术。 例如，在蚀刻工艺之后，可以利用选择性外延沉积工艺用硅合金填充源极 和漏极区空腔，包括源极和漏极延伸部分(214)。 因此，该外延沉积在一 个工艺中形成源极和漏极区以及源极和漏极延伸部分。 在一些实施方式中， 硅合金可以是原位掺杂的硅锗、原位掺杂的碳化硅或原位掺杂的硅。 在可 选实施方式中，可以使用其他的硅合金。 例如，可以使用的可选硅合金材 料包括，但不限于硅化镍、硅化钛、硅化钴，并且可能掺杂有硼和/或铝的 一种或多种。 在一些实施方式中，可以使用CVD工艺进行沉积。

In an embodiment, the lattice spacing of the silicon alloy material deposited in the source and drain region cavities is different from the lattice spacing of the substrate material. The difference in lattice spacing induces tensile or compressive stress in the channel region of the MOS transistor, which is enhanced by the deposition of silicon alloy in the source and drain extensions. As is known to those skilled in the art, the decision whether to cause tensile or compressive stress will depend on whether an NMOS or PMOS transistor is formed.

在实施方式中，沉积在源极和漏极区空腔中的硅合金材料的晶格间距 与衬底材料的晶格间距不同。晶格间距的差异在MOS晶体管的沟道区中引 起拉伸或压缩应力，由于在源极和漏极延伸部分中沉积硅合金而增强了所 述应力。 如本领域技术人员所知，决定是引起拉伸应力还是压缩应力将取 决于是形成NMOS还是PMOS晶体管。

According to an embodiment of the present invention, for NMOS transistors, source and drain region cavities may be filled with carbon doped silicon. Carbon doped silicon can be deposited in an epitaxial and selective manner. In other embodiments, carbon doped silicon may also be doped in situ with phosphorus. The carbon concentration may range from 0.5 atomic percent to 3.0 atomic percent. The phosphorus concentration may be in the range of 5 × 10 < 19 > / cm 3 to 5 × 10 < 20 > / cm < 3 >. The thickness of carbon-doped silicon can be to

根据本发明的实施方式，对于NMOS晶体管而言，可以利用掺碳硅 (carbon doped silicon)填充源

极和漏极区空腔。可以以外延和选择性的方式沉积掺碳硅。在其他实施方式中，还可以用磷对掺碳硅进行原位掺杂。碳浓度可以在0.5原子百分比到3.0原子百分比的范围内。磷浓度可以在5×10<19>/cm3到5×10<20>/cm<3>的范围内。掺碳硅的厚度可以在 到

In the range. Silicon doped with carbon and phosphorus can be expressed as (C,P)ySi(1-y).

的范围内。掺碳和磷的硅可以表示为(C，P)ySi(1-y)。

Highly doped (C, P) in a low pressure chemical vapor deposition (LPCVD) reaction chamber using up to 60 deposition cycles and etching sequences based on silane (SiH4), PH3, CH3SiH3 and chlorine (Cl2) chemistries ySi (1-y) deposition of source and drain regions. The reaction chamber temperature can be between 500 ° C and 625 ° C and the reaction chamber pressure can be below 20 Pa. To achieve selectivity, epitaxy, and high dopant concentration, the process parameters described in the following paragraphs can be used.

可以在低压化学气相沉积(LPCVD)反应室中，利用多达60个沉积周期和基于硅烷(SiH4)、PH3、CH3SiH3和氯气(Cl2)化学物质的蚀刻次序，进行高掺杂(C，P)ySi(1-y)源极和漏极区的沉积。反应室温度可以在500°C到625°C之间，反应室压力可以低于20Pa。为了实现选择性、外延和高掺杂剂浓度，可以使用以下段落中所描述的工艺参数。

For the deposition stage, the co-reactant may include SiH4 at a flow rate between 100 and 400 standard cubic centimeters per minute (SCCM), CH3SiH3 at a flow rate between 25 and 150 SCCM, PH3 at a flow rate between 1 and 25 SCCM, and H2 with a flow rate between 500 and 4000 SCCM. Each cycle of the deposition phase can last up to 4 minutes.

对于沉积阶段而言，共反应剂可以包括流速在100到400标准立方厘米每分钟(SCCM)之间的SiH4、流速在25到150SCCM之间的CH3SiH3、流速在1到25SCCM之间的PH3、以及流速在500到4000SCCM之间的H2。沉积阶段的每个周期可以持续最高达4分钟。

The deposition stage can be followed by a first cleaning stage. The first purge may include nitrogen gas at a flow rate between 500 SCCM and 2 standard liters per minute (SLM) and N2Cl2 at a flow rate between 5 and 50 SCCM. Each cycle of the first cleaning phase can last up to 10 seconds.

沉积阶段之后可以是第一清洗阶段。第一清洗可以包括流速在500 SCCM到2标准升每分钟(SLM)之间的氮气以及流速在5到50SCCM之间的N2Cl2。第一清洗阶段的每个周期可以持续最高达10秒。

The etching phase can be after the cleaning phase. For the etching stage, the co-reactant may include Cl2 having a flow rate between 5 and 25 SCCM. Each cycle of the etch phase can last up to 30 seconds.

蚀刻阶段可以在清洗阶段之后。对于蚀刻阶段而言，共反应剂可以包括流速在5到25SCCM之间的Cl2。蚀刻阶段的每个周期可以持续最高达30秒。

The etching stage can be followed by a second cleaning stage. The second purge can include nitrogen at a flow rate between 50 SCCM and 2 SLM and N2Cl2 at a flow rate between 5 and 35 SCCM. Each cycle of the second cleaning phase can last up to 10 seconds.

蚀刻阶段之后可以是第二清洗阶段。该第二清洗可以包括流速在50 SCCM扫2SLM之间的氮气以及流速在5到35SCCM之间的N2Cl2。第二清洗阶段的每个周期可以持续最高达10秒。

The second cleaning stage can be followed by a third cleaning stage. The third purge can include hydrogen (H2) at a flow rate between 5 and 25 SLM. Each cycle of the third cleaning phase can last up to 2 minutes.

第二清洗阶段之后可以是第三清洗阶段。第三清洗可以包括流速在5 到25SLM之间的氢气(H2)。第三清洗阶段的每个周期可以持续最高达2 分钟。

In accordance with embodiments of the present invention, for PMOS transistors, source and drain region cavities may be filled with silicon germanium. Silicon germanium can be epitaxially deposited. The cerium concentration may range from 10 atomic percent to 50 atomic percent. In other embodiments, silicon germanium may also be ortho doped with boron. The boron concentration may be in the range of 2 × 10 < 19 > / cm < 3 > to 7 × 10 < 20 > / cm < 3 >. The thickness of the silicon germanium can range from to .

根据本发明的实施方式，对于PMOS晶体管而言，可以利用硅锗填充源极和漏极区空腔。硅锗可以是外延沉积的。锗浓度可以在10原子百分比到50原子百分比的范围内。在其他实施方式中，还可以用硼对硅锗进行原位掺杂。硼浓度可以在2×10<19>/cm<3>到7×10<20>/cm<3>的范围内。硅锗的厚度可以在 到 的范围内。

The deposition of doped silicon germanium can be carried out in a CVD reaction chamber, an LPCVD reaction chamber or ultra high vacuum CVD (UHVCVD). The reaction chamber temperature can be between 600 ° C and 800 ° C and the reaction chamber pressure can be between 1 and 760 Torr. The carrier gas may be composed of hydrogen or helium in a flow rate between 10 and 50 SLM.

可以在CVD反应室、LPCVD反应室或超高真空CVD(UHVCVD)中进行被掺杂的硅锗的沉积。反应室温度可以在600°C和800°C之间，反应室压力可以在1到760托之间。载气可以由流速在10到50SLM之间的范围内的氢气或氮气构成。

The deposition may be carried out using a silicon source precursor gas such as dichlorosilane (DCS or SiH2Cl2), silane (SiH4) or disilane (Si2H6). For example, DCS can be used at flow rates ranging from 15 to 100 SCCM. Deposition can also use a ruthenium precursor gas, such as GeH4 diluted in H2 (e.g., GeH4 can be diluted to 1-5%). For example, diluted GeH4 can be used at a concentration of 1% and a flow rate ranging between 50 and 300 SCCM. For in situ doping of boron, diluted B2H6 can be used (for example, B2H6 can be diluted to 1-5% in H2). For example, diluted B2H6 can be used at a concentration of 3% and a flow rate between 10 and 100 SCCM. In some embodiments, an etchant can be added to increase the selectivity of the deposition. For example, HCl or Cl2 can be added at a flow rate ranging from 50 to 300 SCCM.

可以利用诸如二氯甲硅烷(DCS或SiH2Cl2)、硅烷(SiH4)或乙硅烷(Si2H6)的硅源前体气体进行沉积。例如，可以在范围在15到100SCCM之间的流量下使用DCS。沉积还可以使用锗源前体气体，例如在H2中稀释的GeH4(例如可以将GeH4稀释为1-5%)。例如，可以以1%的浓度和范围在50到300SCCM之间的流速使用稀释的GeH4。对于硼的原位掺杂，可以使用稀释的B2H6(例如可以在H2中将B2H6稀释为1-5%)。例如，可以以3%的浓度和范围在10到100SCCM之间的流速使用稀释的B2H6。在一些实施方式中，可以添加蚀刻剂以提高沉积的选择性。例如，可以以范围在50到300SCCM之间的流速添加HCl或Cl2。

3F shows MOS transistor 316 in which source cavity 312 has been filled with a silicon alloy to form source region 318, which has been filled with a silicon alloy to form drain region 320. The extension portion is also filled to form the epitaxial source extension portion 318A and the epitaxial drain extension portion 320A. As shown in FIG. 3F, the self-aligned epitaxial source and drain of the present invention are different from conventional source and drain tip regions formed by implantation and diffusion techniques and thus having no sharp boundary between the tip region and the channel region. The extension has a steep boundary. In other words, the interface between the epitaxial source/drain extension and the channel region is clear and unambiguous. On one side of the interface is an epitaxially deposited doped silicon material, and on the other side of the interface is a substrate material that constitutes the channel region. The dopant in the epitaxial source/drain extension is substantially or completely retained within the extension and does not tend to diffuse into the channel region, thereby allowing the epitaxial source and drain extensions to be heavy relative to conventional techniques. The doped silicon material is very close to the channel region (ie, the source/drain extensions 318A/320A can undercut the gate dielectric layer 302 over 10 nm). As will be appreciated by those skilled in the art, this in turn enables the gate length to be reduced without having to shorten the channel region.

图3F示出了MOS晶体管316，其中已经用硅合金填充了源极空腔312以形成源极区318，已经用硅合金填充了漏极空腔314以形成漏极区320。也填充了延伸部分以形成外延源极延伸部分318A和外延漏极延伸部分320A。如图3F所示，与通过注入和扩散技术形成且因此在尖端区域和沟道区之间没有

清晰边界的常规源极和漏极尖端区域不同，本发明的自对准外 延源极和漏极延伸部分具有陡峭的边界。换言之，外延源极/漏极延伸部分 和沟道区之间的界面是清晰而明确的。在界面的一侧是外延沉积的掺杂硅 材料，在界面的另一侧是构成沟道区的衬底材料。外延源极/漏极延伸部分 中的掺杂剂基本或完全保持在延伸部分内，并不趋向于扩散到沟道区中，从而允许外延源极和漏极延伸部分能够相对于常规技术使重掺杂硅材料非 常接近沟道区(即源极/漏极延伸部分318A/320A可以底切栅极电介质层302 超过10nm)。如本领域技术人员将要认识到的，这又使得栅极长度能够被 缩小，而不必缩短沟道区。

Forming the epitaxial source and drain extensions closer to the channel region also imparts greater hydrostatic stress to the channel. This stress increases the strain in the channel, thereby increasing the mobility in the channel and increasing the drive current. It is also possible to further amplify the stress by increasing the doping of the epitaxial source and drain extensions, which is easily controlled during epitaxial deposition of the silicon alloy. This is an improvement over conventional diffusion processes where the tip region generally does not cause strain on the channel region.

较靠近沟道区形成外延源极和漏极延伸部分还给沟道带来更大的流体 静应力。该应力增大了沟道内的应变，从而提高了沟道中的迁移率并增大 了驱动电流。还可以通过提高外延源极和漏极延伸部分的掺杂来进一步放 大该应力，在硅合金的外延沉积期间这很容易控制。与尖端区域一般不在 沟道区上引起应变的常规扩散工艺相比，这是一种改进。

As will be appreciated by those skilled in the art, MOS transistor 316 can also undergo further MOS processing, such as a replacement gate oxide process, a replacement metal gate process, an anneal or a salicidation process, which can be further modified. Transistor 316 and/or provides the necessary electrical interconnections. For example, after epitaxial deposition of the source/drain regions and the source/drain extensions, an interlayer dielectric (ILD) can be deposited over transistor 316 and planarized (216). The well-known material that can be applied to the dielectric layer of the integrated circuit structure, such as a low-k dielectric material, can be used to form the ILD. Such dielectric materials include, but are not limited to, oxides such as silicon dioxide (SiO_2) and carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorinated cyclobutane or polytetrafluoroethylene, fluorine Silicate glass (FSG) and organosilicates such as silsesquioxane, siloxane or organosilicate glass. The dielectric layer can include microvias or other holes to further reduce its dielectric constant. FIG. 3G shows the ILD layer 322 that has been deposited over the MOS transistor 316.

如本领域技术人员将要认识到的，MOS晶体管316还可以经受进一步 的MOS处理，例如替换栅极氧化物工艺、替换金属栅极工艺、退火或硅化 工艺(salicidation process)，所述处理可以进一步改变晶体管316和/或提供 必要的电互连。例如，在外延沉积源极/漏极区和源极/漏极延伸部分之后， 可以在晶体管316上方沉积层间电介质(ILD)并进行平面化(216)。可以使用公知的可应用于集成电路结构的电介质层的材料，例如低k电介质材 料来形成ILD。这种电介质材料包括但不限于诸如二氧化硅(SiO_2)和碳掺 杂氧化物(CDO)的氧化物、氮化硅、诸如过氟化环丁烷或聚四氟乙烯的 有机聚合物、氟硅酸盐玻璃(FSG)以及诸如硅倍半氧烷(silsesquioxane)、 硅氧烷或有机硅酸盐玻璃的有机硅酸盐。

电介质层可以包括微孔或其他孔 穴以进一步减小其介电常数。 图3G示出了已经沉积在MOS晶体管316上 方的ILD层322。

Next, in an embodiment of the present invention using a replacement metal gate process, the gate stack (ie, high-k gate dielectric layer 302, sacrificial gate electrode 304, and hard mask layer 306) may be removed using an etch process (218)). Methods for removing these layers are well known in the art. In an alternative embodiment, only the sacrificial gate 304 is removed. Figure 3H shows the trench opening formed when the gate stack is etched away.

接下来，在本发明使用替换金属栅极工艺的实施方式中，可以利用蚀 刻工艺去除栅极叠置体(即高k栅极电介质层302、牺牲栅电极304和硬掩 模层306) (218)。 用于去除这些层的方法在现有技术中是公知的。 在可选 实施方式中，仅去除牺牲栅极304。 图3H示出了在蚀刻掉栅极叠置体时形 成的沟槽开口。

If the gate dielectric layer is removed, a new gate dielectric layer can be deposited into the trench opening (220). The high k dielectric material described above, such as yttrium oxide, can be used herein. The same deposition process can also be used. The replacement of the gate dielectric layer can be utilized to address any damage that may be caused to the original gate dielectric layer during the application of the dry and wet etch processes. A metal gate electrode layer (222) can then be deposited over the gate dielectric layer. A conventional metal deposition process can be used to form a metal gate electrode layer such as CVD, ALD, PVD, electroless plating or electroplating. Figure 3I shows a high-k gate dielectric layer 324 and a metal gate electrode 326 that have been deposited into the trench openings.

如果去除了栅极电介质层，可以将新的栅极电介质层沉积到沟槽开口 中(220)。 这里可以使用上述高k电介质材料，例如氧化铪。 也可以使用 相同的沉积工艺。 可以利用栅极电介质层的替换来解决在应用干法和湿法 蚀刻工艺期间可能对原始栅极电介质层造成的任何损害。 然后可以在栅极 电介质层之上沉积金属栅电极层(222)。 可以使用常规的金属沉积工艺来 形成金属栅电极层，例如CVD、ALD、PVD、无电镀或电镀。 图3I示出了 已经沉积到沟槽开口中的高k栅极电介质层324和金属栅电极326。

The metal gate electrode layer may be composed of a P-type work function metal or an N-type work function metal depending on whether the transistor is a PMOS or an NMOS transistor. In some embodiments, PMOS transistors are formed, and materials that can be used to form the P-type work function metal layer include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides such as ruthenium oxide. The P-type metal layer will enable the formation of a PMOS gate electrode with a success function between about 4.9 eV and about 5.2 eV. Alternatively, in some embodiments, NMOS transistors are formed, and materials that can be used to form the N-type work function metal layer include, but are not limited to, hafnium, zirconium, titanium, hafnium, aluminum, and alloys thereof, such as metal carbides including these

elements. , namely tantalum carbide, zirconium carbide, titanium carbide, tantalum carbide and aluminum carbide. The N-type metal layer will enable the formation of an NMOS gate electrode with a success function between about 3.9 eV and about 4.2 eV. In some embodiments, two or more metal gate electrode layers can be deposited. For example, a work function metal can be deposited followed by a metal gate electrode fill metal such as aluminum metal.

根据晶体管是PMOS还是NMOS晶体管，金属栅电极层可以由P型功 函数金属或N型功函数金属构成 。 在一些实施方式中，形成PMOS晶体管，并且可用于形成P型功函数金属层的材料包括但不限于 钌、钯、铂、钴、 镍和导电金属氧化物，例如氧化钌。 P型金属层将使得能够形成功函数在大 约4.9eV到大约5.2eV之间的PMOS栅电极。 或者，在一些实施方式中， 形成NMOS晶体管，并且可用于形成N型功函数金属层的材料包括但不限 于铪、锆、钛、钽、铝及它们的合金，例如包括这些元素的金属碳化物， 即碳化铪、碳化锆、碳化钛、碳化钽和碳化铝。 N型金属层将使得能够形 成功函数在大约3.9eV到大约4.2eV之间的NMOS栅电极。 在一些实施方 式中，可以沉积两个或更多的金属栅电极层。 例如，可以沉积功函数金属， 随后是诸如铝金属的金属栅电极填充金属。

Thus, self-aligned epitaxial source and drain extensions have been disclosed which are reduced by the combination of an increase in the doped silicon volume (e.g., boron doped silicon germanium volume) and a decrease in silicon volume. The total resistance of the MOS transistor increases the channel strain. The epitaxial source and drain extensions do not have a bullet-shaped profile, forming a sharp boundary between the channel region and the source and drain regions, and having a more easily controlled doping concentration for a more optimized source-drain Extreme profile. Moreover, embodiments of the present invention are capable of etching the source and drain extensions substantially independent of the thickness of the isolation layer by selecting an appropriate combination of dopant and etchant formulations. Therefore, the self-aligned process improves performance while minimizing process variations.

因此，已经公开了自对准外延源极和漏极延伸部分，所述延伸部分由 于掺杂硅体积(例如硼掺杂的硅锗体积)的增大与硅体积减小的结合，而 减小了MOS晶体管的总电阻，并增大了沟道应变。 外延源极和漏极延伸部 分不具有子弹形轮廓，在沟道区与源极和漏极区之间形成陡峭的边界，并 具有更容易控制的掺杂浓度，获得更加优化的源极-漏极轮廓。 此外，通过 选择掺杂剂和蚀刻剂配方的适当组合，本发明的实施方式能够蚀刻源极和 漏极延伸部分而基本不受隔离层厚度的影响。 因此，该自对准工艺提高了 性能，同时使工艺变化最小化。

4 is a graph showing an improvement that can be achieved by the self-alignment method disclosed herein. Line 400 represents data collected for a MOS device constructed using embodiments of the present invention. As shown, the UC to UC distance is much less affected by the thickness of the isolation layer than the device formed using conventional methods, and the data for the device formed by conventional methods is represented by line 118.

图4为示出了可通过本文所公开的自对准方法实现的改进的曲线图。 线400表示针对利用本发明实施

方式构建的MOS器件采集的数据。如图所示，与利用常规方法形成的器件相比，UC到UC距离受隔离层厚度的影响要小得多，针对常规方法形成的器件的数据由线118表示。

The above description of the illustrated embodiments of the invention, including the description of the invention, is not intended to be While the invention has been described with respect to the specific embodiments and examples of the present invention, various equivalent modifications are possible within the scope of the invention.

以上对本发明所示实施方式的描述，包括在摘要中描述的内容，并不旨在是穷举性的或将本发明限于所公开的精确形式。尽管在本文中为了说明的目的描述了本发明的具体实施方式和例子，但如本领域的技术人员将认识到的，在本发明的范围内各种等价的修改都是可能的。

These modifications can be made to the invention in light of the above detailed description. The use of the terms in the following claims should not be construed as limiting the invention to the particular embodiments disclosed. Rather, the scope of the invention is to be determined by the appended claims and the appended claims

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可以依据以上详细描述对本发明进行这些修改。在所附权利要求书中使用的术语不应被视为将本发明限于在说明书和权利要求中所公开的具体实施方式。相反，本发明的范围完全由所附权利要求书决定，应根据权利要求解释的确立原则来解释所附权利要求书。

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CLAIMS CN101622690

1、

A method comprising:

一种方法，其包括：

Forming a gate stack on the substrate;

在衬底上形成栅极叠置体；

A dopant is implanted into a region of the substrate adjacent the gate stack, wherein the dopant increases an etch rate of the substrate;

将掺杂剂注入到所述衬底与所述栅极叠置体相邻的区域中，其中所述 掺杂剂增加所述衬底的蚀刻速率；

Forming a pair of isolation layers on laterally opposite sides of the gate stack, the isolation layer being on top of a doped region of the substrate;

在所述栅极叠置体的横向相对侧上形成一对隔离层，所述隔离层位于 所述衬底的掺杂区域的顶部上；

Etching the doped region of the substrate and the region of the substrate below the doped region, wherein an etch rate of the doped region is higher than a region of the substrate below the doped region Etching rate;

蚀刻所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的 区域，其中所述掺杂区域的蚀刻速率高于所述衬底位于所述掺杂区域下方 的区域的蚀刻速率；以及

A silicon-containing material is deposited in the etched regions of the substrate to form source and drain regions and source and drain extensions.

在所述衬底的蚀刻区域中沉积含硅材料，以形成源极区和漏极区以及 源极延伸部分和漏极延伸部分。

2、

The method of claim 1 further comprising annealing the substrate after implanting the dopant, wherein the annealing occurs at a temperature between about 700 ° C and about 1100 ° C for the highest Up to five seconds.

根据权利要求1所述的方法，还包括在注入所述掺杂剂之后对所述 衬底进行退火，其中所述退火发生在大约700° C到大约1100° C之间的温度 下，持续最高达五秒的时间。

3、

The method of claim 1 further comprising applying a wet etch to said etched regions of said substrate to remove portions of said lining along <111> and <001> crystal faces prior to depositing said silicon-containing material bottom.

根据权利要求1所述的方法，还包括对所述衬底的所述蚀刻区域施 加湿法蚀刻，以在沉积所述含硅材料之前沿<111>和<001>晶面去除部分所 述衬底。

4、

The method of claim 1 wherein implanting said dopant comprises utilizing an implantation energy between about 5 keV and about 15 keV at about 1 x 10 < 14 > to about 1 x 10 < 16 > atoms / cm < 3 > A dose between them injects carbon into the substrate.

根据权利要求1所述的方法，其中注入所述掺杂剂包括利用大约 5keV到大约15keV之间的注入能量以大约1×10<14>到大约1×10<16>原子/cm<3> 之间的剂量将碳注入到所述衬底中。

5、

The method of claim 1 wherein implanting the dopant comprises utilizing an implant energy between about 1

keV and about 5 keV at about 1 x 10 < 14 > to about 5 x 10 < 15 > atoms / cm < 3 > A dose between them injects phosphorus into the substrate.

根据权利要求1所述的方法，其中注入所述掺杂剂包括利用大约 1keV到大约5keV之间的注入能量以大约1×10<14>到大约5×10<15>原子/cm<3> 之间的剂量将磷注入到所述衬底中。

6、

The method of claim 1 wherein implanting said dopant comprises utilizing an implantation energy between about 2 keV and about 5 keV at about 1 x 10 < 14 > and about 5 x 10 < 15 > atoms / cm < 3 > The dose between the injected arsenic.

根据权利要求1所述的方法，其中注入所述掺杂剂包括利用大约 2keV到大约5keV之间的注入能量以大约1×10<14>和大约5×10<15>原子/cm<3> 之间的剂量注入砷。

7、

The method of claim 1 wherein said etching is a dry etching process, the process comprising:

根据权利要求1所述的方法，其中所述蚀刻为干法蚀刻工艺，该工 艺包括：

Applying NF3 and Cl2 to the doped region of the substrate and the region of the substrate below the doped region;

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区 域施加NF3和Cl2；以及

The plasma is applied at a power of between about 700 W and about 1100 W.

在大约700W到大约1100W之间的功率下施加等离子体。

8、

The method of claim 1 wherein said etching is a dry etching process, the process comprising:

根据权利要求1所述的方法，其中所述蚀刻为干法蚀刻工艺，该工 艺包括：

Applying HBr and Cl2 to the doped region of the substrate and the region of the substrate below the doped region;

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加HBr和Cl2；以及

The plasma is applied at a power of between about 600 W and about 1000 W.

在大约600W到大约1000W之间的功率下施加等离子体。

9、

The method of claim 1 wherein said etching is a dry etching process, the process comprising:

根据权利要求1所述的方法，其中所述蚀刻为干法蚀刻工艺，该工艺包括：

Applying SF6 and Cl2 to the doped region of the substrate and the region of the substrate below the doped region;

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加SF6和Cl2；以及

The plasma is applied at a power of between about 400 W and about 900 W.

在大约400W到大约900W之间的功率下施加等离子体。

10、

The method of claim 1 wherein said etching is a dry etching process, the process comprising:

根据权利要求1所述的方法，其中所述蚀刻为干法蚀刻工艺，该工艺包括：

Applying Ar and Cl2 to the doped region of the substrate and the region of the substrate below the doped region;

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加Ar和Cl2；以及

The plasma is applied at a power of between about 400 W and about 800 W.

在大约400W到大约800W之间的功率下施加等离子体。

11、

The method of claim 1 wherein said silicon-containing material comprises carbon doped silicon.

根据权利要求1所述的方法，其中所述含硅材料包括掺碳硅。

12、

The method of claim 1 wherein said silicon-containing material comprises silicon doped with carbon and phosphorus.

根据权利要求1所述的方法，其中所述含硅材料包括用碳和磷掺 杂的硅。

13、

The method of claim 1 wherein said silicon-containing material comprises silicon germanium doped with boron.

根据权利要求1所述的方法，其中所述含硅材料包括用硼掺杂的 硅锗。

14、

The method of claim 1 wherein said gate stack comprises:

根据权利要求1所述的方法，其中所述栅极叠置体包括：

a high-k gate dielectric layer;

高k栅极电介质层；

a sacrificial layer formed on the high-k gate dielectric layer;

形成在所述高k栅极电介质层上的牺牲层；以及

A hard mask layer formed on the sacrificial layer.

形成在所述牺牲层上的硬掩模层。

15、
The method of claim 14 further comprising:

根据权利要求14所述的方法，还包括：

Depositing an ILD layer after depositing the silicon-containing material;

在沉积所述含硅材料之后沉积ILD层；

Removing the hard mask layer and the sacrificial layer to form a trench between the isolation layers;

去除所述硬掩模层和所述牺牲层以在所述隔离层之间形成沟槽；以及

A metal gate electrode is deposited into the trench.

将金属栅电极沉积到所述沟槽中。

16、
The method of claim 14 further comprising:

根据权利要求14所述的方法，还包括：

Depositing an ILD layer after depositing the silicon-containing material;

在沉积所述含硅材料之后沉积ILD层；

Removing the hard mask layer, the sacrificial layer, and the high-k gate dielectric layer to form a trench between the isolation layers;

去除所述硬掩模层、所述牺牲层和所述高k栅极电介质层以在所述隔 离层之间形成沟槽；

Depositing a new high-k gate dielectric layer into the trench;

将新的高k栅极电介质层沉积到所述沟槽中；以及

A metal gate electrode is deposited into the trench.

将金属栅电极沉积到所述沟槽中。

17、

The method of claim 1 wherein the interface between the source extension portion and the substrate is steep, and wherein the interface between the drain extension portion and the substrate is steep.

根据权利要求1所述的方法，其中所述源极延伸部分和所述衬底之间的界面是陡峭的，并且其中所述漏极延伸部分和所述衬底之间的界面是陡峭的。

18、

The method of claim 1 wherein said dopant is implanted in a region of said substrate where said source and drain extensions are to be formed.

根据权利要求1所述的方法，其中在所述衬底中要形成所述源极和漏极延伸部分的区域中注入所述掺杂剂。

19、

The method of claim 1 wherein the thickness of said pair of isolation layers has a minimal effect on the locations of said source extensions and said drain extensions.

根据权利要求1所述的方法，其中所述一对隔离层的厚度对所述源极延伸部分和所述漏极延伸部分的位置造成最低程度的影响。

20、

The method of claim 1 wherein said source extension portion and said drain extension portion overlap said gate stack of a transistor.

根据权利要求1所述的方法，其中所述源极延伸部分和所述漏极延伸部分与晶体管的所述栅极叠置体重叠。

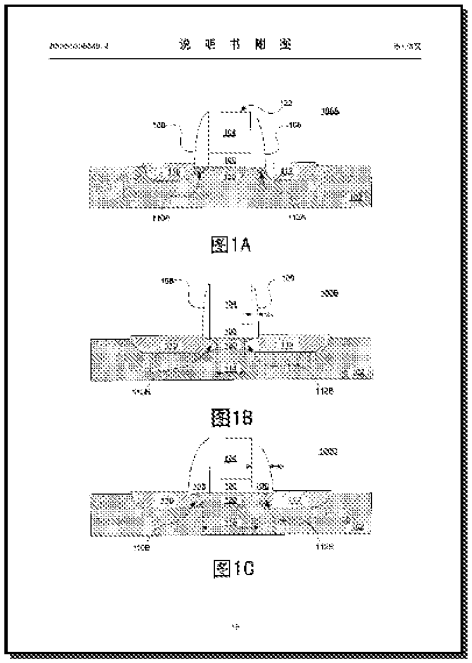


图1A

图1B

图1C

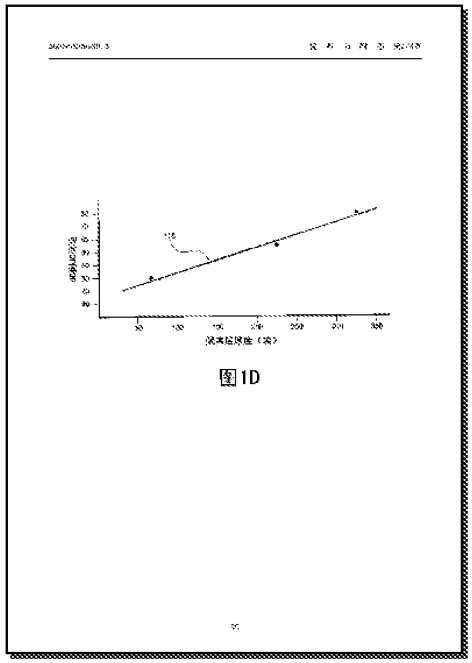


图1D

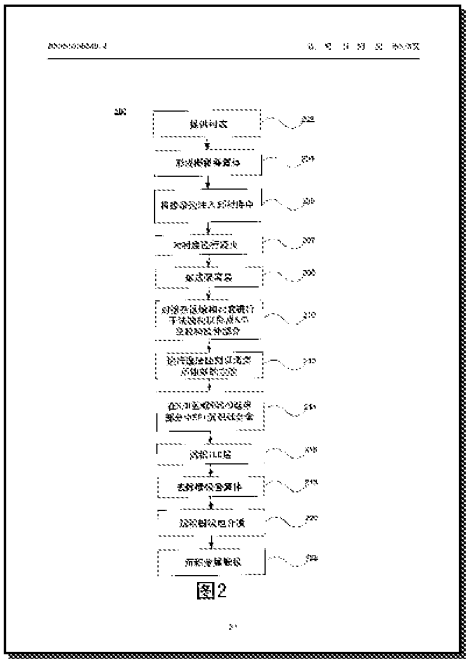


图2

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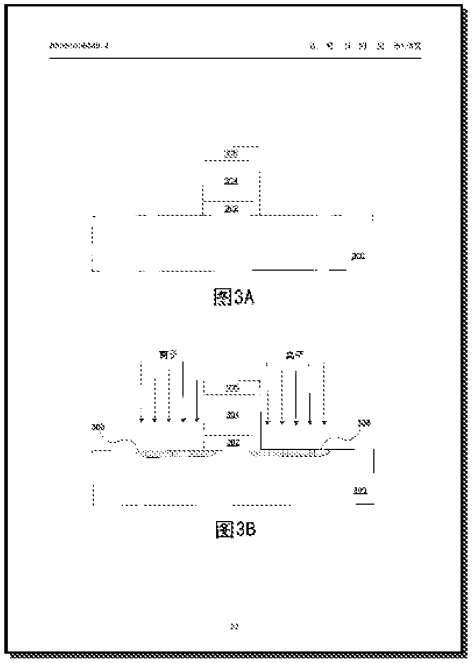


图3A

图3B

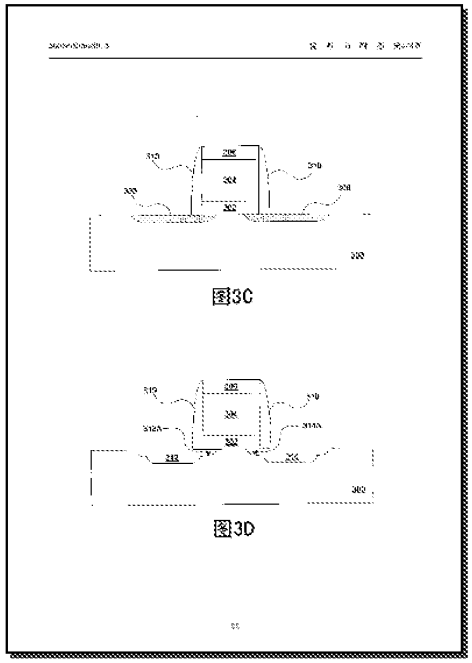


图3C

图3D

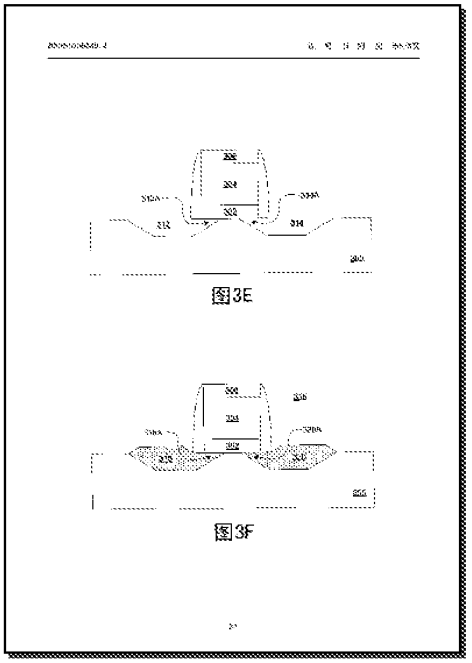


图3E

图3F

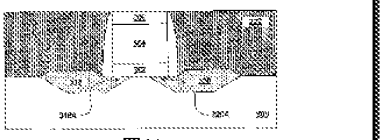


图3G

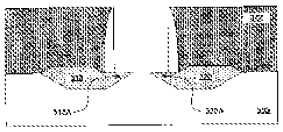


图3H

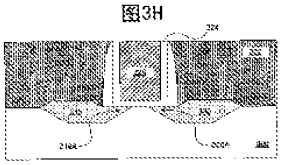


图3I

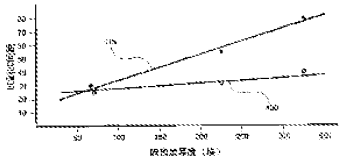


图4

Drawing pages of CN101622690 A

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H01L 21/20 (2006.01)

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[71] 申请人 英特尔公司
地址 美国加利福尼亚
[72] 发明人 B·塞尔 T·加尼 A·默西 H·戈麦斯

[74] 专利代理机构 永新专利商标代理有限公司
代理人 邬少俊 王 英

权利要求书 4 页 说明书 13 页 附图 8 页

[54] 发明名称

具有自对准外延源极和漏极延伸部分的半导体器件

[57] 摘要

一种形成具有与晶体管的栅极电介质层非常接近的自对准源极和漏极延伸部分的晶体管的方法包括：在衬底上形成栅极叠置体；将掺杂剂注入到衬底与栅极叠置体相邻的区域中，其中掺杂剂增加衬底的蚀刻速率并限定源极和漏极延伸部分的位置；在栅极叠置体的横向相对侧上形成一对隔离层，所述隔离层位于衬底的掺杂区域的顶部上；蚀刻衬底的掺杂区域以及衬底位于掺杂区域下方的部分，其中所述掺杂区域的蚀刻速率高于衬底位于所述掺杂区域下方的部分的蚀刻速率；以及在衬底的蚀刻部分中沉积基于硅的材料。

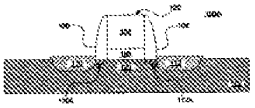


图1A

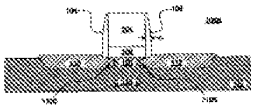


图1B

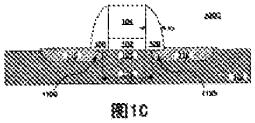


图1C

1、一种方法，其包括：

在衬底上形成栅极叠置体；

将掺杂剂注入到所述衬底与所述栅极叠置体相邻的区域中，其中所述掺杂剂增加所述衬底的蚀刻速率；

在所述栅极叠置体的横向相对侧上形成一对隔离层，所述隔离层位于所述衬底的掺杂区域的顶部上；

蚀刻所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域，其中所述掺杂区域的蚀刻速率高于所述衬底位于所述掺杂区域下方的区域的蚀刻速率；以及

在所述衬底的蚀刻区域中沉积含硅材料，以形成源极区和漏极区以及源极延伸部分和漏极延伸部分。

2、根据权利要求 1 所述的方法，还包括在注入所述掺杂剂之后对所述衬底进行退火，其中所述退火发生在大约 700℃到大约 1100℃之间的温度下，持续最高达五秒的时间。

3、根据权利要求 1 所述的方法，还包括对所述衬底的所述蚀刻区域施加湿法蚀刻，以在沉积所述含硅材料之前沿<111>和<001>晶面去除部分所述衬底。

4、根据权利要求 1 所述的方法，其中注入所述掺杂剂包括利用大约 5keV 到大约 15keV 之间的注入能量以大约 1×10^{14} 到大约 1×10^{16} 原子/cm^3 之间的剂量将碳注入到所述衬底中。

5、根据权利要求 1 所述的方法，其中注入所述掺杂剂包括利用大约 1keV 到大约 5keV 之间的注入能量以大约 1×10^{14} 到大约 5×10^{15} 原子/cm^3 之间的剂量将磷注入到所述衬底中。

6、根据权利要求 1 所述的方法，其中注入所述掺杂剂包括利用大约 2keV 到大约 5keV 之间的注入能量以大约 1×10^{14} 和大约 5×10^{15} 原子/cm^3 之间的剂量注入砷。

7、根据权利要求 1 所述的方法，其中所述蚀刻为干法蚀刻工艺，该工艺包括：

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加 NF_3 和 Cl_2；以及

在大约 700W 到大约 1100W 之间的功率下施加等离子体。

8、根据权利要求 1 所述的方法，其中所述蚀刻为干法蚀刻工艺，该工艺包括：

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加 HBr 和 Cl_2；以及

在大约 600W 到大约 1000W 之间的功率下施加等离子体。

9、根据权利要求 1 所述的方法，其中所述蚀刻为干法蚀刻工艺，该工艺包括：

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加 SF_6 和 Cl_2；以及

在大约 400W 到大约 900W 之间的功率下施加等离子体。

10、根据权利要求 1 所述的方法，其中所述蚀刻为干法蚀刻工艺，该工艺包括：

向所述衬底的所述掺杂区域以及所述衬底位于所述掺杂区域下方的区域施加 Ar 和 Cl_2；以及

在大约 400W 到大约 800W 之间的功率下施加等离子体。

11、根据权利要求 1 所述的方法，其中所述含硅材料包括掺碳硅。

12、根据权利要求 1 所述的方法，其中所述含硅材料包括用碳和磷掺杂的硅。

13、根据权利要求 1 所述的方法，其中所述含硅材料包括用硼掺杂的硅锗。

14、根据权利要求 1 所述的方法，其中所述栅极叠置体包括：

高 k 栅极电介质层；

形成在所述高 k 栅极电介质层上的牺牲层；以及

形成在所述牺牲层上的硬掩模层。

15、根据权利要求 14 所述的方法，还包括：

在沉积所述含硅材料之后沉积 ILD 层；

去除所述硬掩模层和所述牺牲层以在所述隔离层之间形成沟槽；以及

将金属栅电极沉积到所述沟槽中。

16、根据权利要求 14 所述的方法，还包括：

在沉积所述含硅材料之后沉积 ILD 层；

去除所述硬掩模层、所述牺牲层和所述高 k 栅极电介质层以在所述隔离层之间形成沟槽；

将新的高 k 栅极电介质层沉积到所述沟槽中；以及

将金属栅电极沉积到所述沟槽中。

17、根据权利要求 1 所述的方法，其中所述源极延伸部分和所述衬底之间的界面是陡峭的，并且其中所述漏极延伸部分和所述衬底之间的界面是陡峭的。

18、根据权利要求 1 所述的方法，其中在所述衬底中要形成所述源极和漏极延伸部分的区域中注入所述掺杂剂。

19、根据权利要求 1 所述的方法，其中所述一对隔离层的厚度对所述源极延伸部分和所述漏极延伸部分的位置造成最低程度的影响。

20、根据权利要求 1 所述的方法，其中所述源极延伸部分和所述漏极延伸部分与晶体管的所述栅极叠置体重叠。

具有自对准外延源极和漏极延伸部分的半导体器件

背景技术

衬底上的电路器件（例如半导体衬底上的集成电路（IC）晶体管、电阻器、电容器等）性能的提高通常是设计、制造和操作这些器件期间考虑的主要因素。例如，在设计与制造或形成诸如在互补金属氧化物半导体（CMOS）中使用的金属氧化物半导体（MOS）晶体管半导体器件期间，常常希望增大电子在N型MOS器件（NMOS）沟道区中的运动，并增大带正电荷的空穴在P型MOS器件（PMOS）沟道区中的运动。

减小MOS器件总电阻的一种方法是对源极/漏极区和沟道区之间的区域（被称为MOS器件的尖端区域（tip region））进行掺杂。例如，可以在源极/漏极区中注入掺杂剂，并可以进行退火以使掺杂剂向沟道区扩散。

因为使用了注入和扩散方法，所以限制了控制掺杂剂浓度和位置的能力。此外，MOS器件其他部分的尺寸，例如其偏移隔离层（offset spacer）的厚度，也能够对尖端区域的位置产生很大的影响。所有这些又影响到尖端区域使掺杂剂浓度最大化并接近沟道区的能力。因此，需要改进的方法或结构来克服常规尖端区域的局限。

附图说明

图1A示出了包括源极和漏极尖端区域的常规MOS器件；

图1B示出了包括源极和漏极外延延伸部分的MOS器件；

图1C示出了隔离层厚度是如何影响MOS器件的外延延伸部分的蚀刻的；

图1D是示出UC到UC距离对隔离层厚度的依赖关系的曲线图；

图2是根据本发明的实施方式形成源极和漏极外延延伸部分的方法。；

图3A到3I示出了在执行图2的方法时形成的结构；

图4是示出根据本发明的实施方式形成的MOS器件的UC到UC距离如何较少地依赖于隔离层厚度的曲线图。

具体实施方式

这里所述的是在 MOS 器件中形成外延源极和漏极延伸部分的系统和方法。在以下描述中，将利用本领域技术人员为向其他本领域技术人员传达其工作内容而通常采用的术语来描述示例性实施方式的各方面。然而，本领域的技术人员将会明了，可以仅利用一些所述方面来实施本发明。出于解释的目的，对具体的数量、材料和构造进行了阐述，以便对示例性实施方式有透彻的理解。然而，本领域的技术人员将会明了，可以在没有这些具体细节的情况下实施本发明。在其他情况下，省略或简化了公知特征，以免使示例性实施方式不清楚。

将把各个操作描述为多个分立的操作，反过来讲，也是以最有助于理解本发明的方式来描述的，然而，不应将描述的顺序视为暗指这些操作必定与顺序有关。具体而言，不必按照所呈现的顺序来执行这些操作。

作为背景技术，常规金属氧化物半导体（MOS）晶体管包括源极和漏极“尖端区域”，设计所述尖端区域以降低晶体管的总电阻，同时改善短沟道效应。这些尖端区域是衬底中利用注入和扩散技术注入了诸如硼或碳的掺杂剂的部分。源极尖端区域形成在源极区和沟道区之间的区域中。类似地，漏极尖端区域形成在漏极区和沟道区之间的区域中。尖端区域最小限度地在晶体管的栅极电介质层下方扩散。

图 1A 示出了形成在衬底 102 上的常规 MOS 晶体管 100A。通常通过将诸如硼的掺杂剂注入到衬底中或通过蚀刻衬底，然后外延沉积硅或硅锗材料来形成源极区 110 和漏极区 112。栅极叠置体 122 形成在晶体管 100A 的沟道区 120 的顶部。栅极叠置体 122 包括栅极电介质层 106 和栅电极 104。形成一对隔离层 108 使其与栅极叠置体 122 相邻。

如本领域所公知的，隔离层 108 一般在栅极电介质层 106 的边缘与源极和漏极区 110/112 中的每一个的边缘之间产生大约 10 到 20 纳米（nm）的距离。就是在这一间隔之内形成源极尖端区域 110A 和漏极尖端区域 112A。尖端区域 110A/112A 与隔离层 108 重叠，并且可以与栅极电介质层 106 重叠或在其下方扩散少于 10nm 的距离。

通常利用注入和扩散技术制造源极尖端区域 110A 和漏极尖端区域 112A。首先，将掺杂剂注入到源极区 110 和漏极区 112 中。可以使用的掺

杂剂包括但不限于硼、砷、锗、磷、铟、或锑。掺杂剂量可以在 1×10^{14} 到 1×10^{16} 原子/cm^3 的范围内。然后对晶体管 100A 进行退火，以使掺杂剂向沟道区 120 扩散。也可以使用倾斜离子注入技术进一步将掺杂剂注入到栅极电介质层 106 和源极/漏极区 110/112 之间的那些区域中。

令人遗憾的是，如本领域技术人员将认识到的，尖端区域 110A/112A 的形状、掺杂剂在隔离层 108 下方渗透的距离以及尖端区域 110A/112A 的浓度梯度全部取决于掺杂剂在衬底材料中的扩散特性。例如，尖端区域的浓度在靠近源极/漏极区 110/112 之处将较为高，而在靠近沟道区 120 之处将为低。尽管非常希望，但是在不将掺杂剂驱动到沟道区 120 中的情况下几乎不可能使掺杂剂浓度在靠近沟道区 120 之处非常高。此外，源极和漏极区 110/112 不能被移动得更靠近沟道区 120，因为可能再次将掺杂剂驱动到沟道区 120 中。这限制了将源极和漏极区 110/112 形成为与沟道区 120 所能靠近的程度，由此限制了可以将栅极长度缩小到什么程度。

图 1B 示出了利用源极和漏极“延伸部分”形成在衬底 102 上的改进的 MOS 晶体管 100B。并非是在隔离层 108 下方注入和扩散掺杂剂以形成尖端区域，MOS 晶体管 100B 而是使用底切蚀刻，以允许源极区 110 和漏极区 112 延伸到隔离层 108 和栅极电介质层 106 的下方。在此将源极/漏极区 110/112 延伸到隔离层 108 下方的部分称为源极延伸部分 110B 和漏极延伸部分 112B。源极和漏极延伸部分 110B/112B 取代了图 1A 所示的较不理想的尖端区域 110A/112A。

通过蚀刻衬底，包括对隔离层进行底切，然后外延沉积硅或硅锗材料来形成源极/漏极区 110/112 和源极/漏极延伸部分 110B/112B。因此在与源极和漏极区 110/112 相同的工艺步骤中形成了源极和漏极延伸部分 110B/112B，这减少了工艺步骤的总数。源极和漏极延伸部分 110B/112B 相对于源极/漏极尖端区域 110A/112A 还提供了其他优点。例如，与常规尖端区域不同，源极/漏极延伸部分 110B/112B 的晶格结构在沟道区 120 中引起应变，其增加了电子迁移率并因此减小了沟道中的电阻。

另一个优点是源极/漏极延伸部分 110B/112B 和形成沟道区 120 的衬底材料 102 之间的界面是陡峭的（abrupt）。在界面的一侧是外延沉积的掺杂硅材料，在界面的另一侧是构成沟道区 120 的衬底材料。这种结构使得外

延源极/漏极延伸部分 110B/112B 能够使重掺杂硅材料非常靠近沟道区 120。外延源极/漏极延伸部分 110B/112B 中的掺杂剂基本或完全保持在延伸部分中，而不趋向于扩散到沟道区 120 中。

令人遗憾的是，形成源极和漏极延伸部分 110B/112B 的常规方法有一些缺点。在图 1B 和 1C 中示出了一种缺点。如图所示，常规的底切蚀刻技术导致底切区域形成了子弹形轮廓。换言之，在栅极电介质层 106 下方少许距离处被蚀刻的衬底材料多于在直接与栅极电介质层 106 相邻处被蚀刻的衬底材料。这样一来，源极延伸部分 110B 和漏极延伸部分 112B 也各自具有子弹形轮廓，这在沟道区 120 中产生了并非最理想的应变。此外，因为在常规底切蚀刻技术中有很多变化，因此在所形成的最终源极和漏极延伸部分 110B/112B 中往往有很多变化。

形成源极和漏极延伸部分 110B/112B 的常规方法的另一缺点涉及隔离层厚度对底切蚀刻的影响，如图 1B 和 1C 所示。从图 1B 开始，所示的 MOS 晶体管 100B 具有偏移隔离层 108，其具有第一厚度 x_1。进行衬底蚀刻，以对隔离层 108 和栅极电介质层 106 的一部分进行底切，从而能够形成源极和漏极延伸部分 110B/112B。底切到底切（UC 到 UC）距离 114 将源极延伸部分 110B 与漏极延伸部分 112B 分隔开。

转到图 1C，所示的 MOS 晶体管 100C 具有厚度为 x_2 的偏移隔离层 108。这里，厚度 x_2 比图 1B 中的隔离层 108 的厚度 x_1 大得多。结果，在进行衬底蚀刻时，较厚的隔离层 108 推出底切蚀刻，并且使源极/漏极延伸部分 110B/112B 形成得更加远离晶体管 100C 的沟道区 120。因此，衬底蚀刻底切了较少的 MOS 晶体管 100C 下方的表面区域。因此，MOS 晶体管 100C 的 UC 到 UC 距离 116 比 MOS 晶体管 100B 的 UC 到 UC 距离 114 大得多。令人遗憾的是，通过这种方式改变 UC 到 UC 距离给 MOS 晶体管造成大的驱动电流变化。

图 1D 为示出了在利用公知方法形成的器件中隔离层厚度如何影响 UC 到 UC 距离的曲线图。该曲线图提供了由线 118 表示的数据，示出了随着隔离层厚度的增加，UC 到 UC 距离也增加，导致大的驱动电流变化。典型地，隔离层厚度每增加一纳米（nm），UC 到 UC 距离增加大约 2nm。这样一来，使用常规方法形成源极/漏极延伸部分允许偏移隔离层的厚度对 MOS 器件

的性能有巨大影响。

为了解决上述这些问题，本发明的实施方式提供了形成新颖的、自对准和外延沉积的源极和漏极延伸部分的方法。本发明的外延源极和漏极延伸部分将高掺杂硅材料设置得非常靠近MOS晶体管的沟道区。并且因为源极和漏极延伸部分是自对准的，所以相对于常规工艺而言，它们受偏移隔离层厚度的影响要小得多。

图2是构建具有自对准外延源极和漏极延伸部分的MOS晶体管的方法200。图3A到3E示出了在执行图2的方法200时形成的结构。

方法200以半导体衬底开始，在所述半导体衬底上可以形成诸如MOS晶体管的MOS器件（图2的工艺202）。可以利用体硅或绝缘体上硅底层结构形成半导体衬底。在其他实施方式中，可以利用其他材料形成半导体衬底，其他材料可以与硅结合或可以不与硅结合，包括但不限于锗、锑化铟、碲化铅、砷化铟、磷化铟、砷化镓或锑化镓。虽然这里描述了可以形成衬底的一些材料范例，但是可以充当可制造半导体器件的基础的任何材料都落在本发明的精神和范围内。

在半导体衬底上形成栅极叠置体（204）。在本发明的一些实施方式中，可以通过沉积然后对栅极电介质层和栅电极层进行构图来形成栅极叠置体。例如，在一种实施方式中，可以利用诸如化学气相沉积（CVD）、原子层沉积（ALD）、旋涂沉积（SOD）或物理气相沉积（PVD）的常规沉积工艺将栅极电介质层均厚沉积到半导体衬底上。也可以使用其他沉积技术，例如，可以热生长栅极电介质层。接下来，可以利用诸如ALD、CVD或PVD的类似沉积技术在栅极电介质层上沉积栅电极材料。在一些实施方式中，栅电极材料为多晶硅或金属层。在一些实施方式中，栅电极材料为后来可以去除以进行替换金属栅极工艺的牺牲材料。然后可以执行常规的构图工艺，以蚀刻掉部分栅电极层和栅极电介质层，从而形成栅极叠置体。

可以由诸如二氧化硅或高k电介质材料的材料形成栅极电介质材料。可以使用的高k栅极电介质材料的范例包括但不限于氧化铪、氧化铪硅、氧化镧、氧化镧铝、氧化锆、氧化锆硅、氧化钽、氧化钛、氧化钡锶钛、氧化钡钛、氧化锶钛、氧化钇、氧化铝、氧化铅钪钽和铌酸铅锌。在一些实施方式中，高k栅极电介质层的厚度可以在大约5埃（Å）到大约50Å

之间。在其他实施方式中，可以对高 k 栅极电介质层进行额外的处理，例如退火工艺，以改善高 k 材料的质量。

图 3A 示出了其上形成栅极叠置体的衬底 300。在这里所述的实施方式中，栅极叠置体可以包括高 k 栅极电介质层 302 和牺牲栅电极 304。在其他实施方式中，栅极叠置体可以包括二氧化硅栅极电介质层和多晶硅栅电极。栅极叠置体还可以包括栅极硬掩模层 306，其在处理期间可以提供某些优点或用处，例如保护栅电极 304 不受随后的离子注入工艺的影响。在本发明的实施方式中，可以利用常规用作硬掩模的材料，例如常规电介质材料来形成该硬掩模层 306。

在形成栅极叠置体之后，执行离子注入工艺以对与栅极叠置体相邻的衬底部分进行高掺杂（206）。根据本发明的实施方式，基于其增加衬底材料的蚀刻速率的能力来选择在离子注入工艺中使用的掺杂剂，在所述衬底材料中要注入所述掺杂剂。为离子注入工艺选择的特定掺杂剂可以根据衬底材料和在随后的蚀刻工艺中使用的蚀刻剂而变化。由于大部分衬底包含大的硅、锗或锑化铟成分，所以常常选择可以增加硅、锗或锑化铟的蚀刻速率的掺杂剂。

在本发明的实施方式中，可以选择的用来增加衬底的蚀刻速率的特定掺杂剂包括但不限于碳、磷和砷。例如，可以利用 5 到 15 千电子伏（keV）之间的注入能量，以在 1×10^{14} 到 1×10^{16} 原子/cm^3 范围内的剂量使用碳。可以利用 1 到 5keV 之间的注入能量，以 1×10^{14} 到 5×10^{15} 原子/cm^3 范围内的剂量使用磷。可以利用 2 到 5keV 之间的注入能量，以在 1×10^{14} 到 5×10^{15} 原子/cm^3 范围内的剂量使用砷。

在本发明的实施方式中，离子注入基本发生在垂直方向（即垂直于衬底的方向）上。在一些实施方式中，离子注入的至少一部分可以发生在倾斜方向上，以将离子注入到栅极叠置体的下方。如上所述，如果栅电极包含金属，那么可以在栅极叠置体上形成电介质硬掩模，以防止对金属栅电极的掺杂。

接下来，执行退火，以进一步将掺杂剂驱动到衬底中，并减小离子注入工艺期间衬底所受到的任何损害（207）。注入和随后的退火可以将离子驱动到 2nm 到 20nm 之间的衬底深度。退火可以在 700℃ 到 1100℃之间的

温度下持续最高达一分钟的时间，例如持续五秒的时间。

图 3B 示出了离子注入和扩散工艺之后的衬底 300。如图所示，离子注入工艺产生了两个与栅极电介质层 302 相邻的掺杂区 308。当暴露于适当的蚀刻剂时，掺杂区 308 的蚀刻速率将高于周围衬底材料的蚀刻速率。掺杂区 308 之一将用作正形成的 MOS 晶体管的源极区的一部分，包括自对准外延源极延伸部分。另一个掺杂区 308 将用作 MOS 晶体管的漏极区的一部分，包括自对准外延漏极延伸部分。在所示的实施方式中，掺杂区 308 的一部分位于栅极电介质层 302 的下方。在本发明的各实施方式中，掺杂区 308 的尺寸，包括它们的深度，可以根据正形成 MOS 晶体管的要求而变化。

接下来，在栅极叠置体的任一侧上形成隔离层（208）。可以使用常规材料，包括但不限于氧化硅或氮化硅来形成隔离层。可以基于正形成的 MOS 晶体管的设计要求选择隔离层的宽度。根据本发明的实施方式，隔离层的宽度不受形成外延源极和漏极延伸部分所造成的设计约束。图 3C 示出了衬底 300，在栅电极层 304 和栅极电介质层 302 的任一侧上形成隔离层 310。

在衬底上形成隔离层之后，可以执行干法蚀刻工艺以蚀刻掺杂区并蚀刻部分衬底，以形成可以在其中形成源极/漏极区和源极/漏极延伸部分的空腔（210）。所蚀刻的空腔与栅极叠置体相邻。可以将所蚀刻的空腔形成到 50nm 到 1500nm 之间的深度，该深度比掺杂区深。因此，蚀刻工艺将去除位于掺杂区下方的衬底材料。

干法蚀刻工艺使用与离子注入工艺中使用的掺杂剂互补的蚀刻剂配方，以提高掺杂区的蚀刻速率。这使得蚀刻工艺能够以快于衬底的其他部分的速率去除掺杂区。这样一来，利用蚀刻速率的适当增加，蚀刻工艺能够到完成空腔的蚀刻时从掺杂区基板去除所有的材料。这包括掺杂区底切隔离层和栅极电介质层的部分，从而限定晶体管的自对准延伸架构。增加掺杂区的蚀刻速率使得所蚀刻的源极和漏极延伸部分空腔能够底切隔离层和栅极电介质层，而 UC 到 UC 距离基本不受诸如隔离层厚度、干法蚀刻工艺的变化和其他工艺变化的因素的影响。

根据本发明的实施方式，干法蚀刻工艺可以使用发生在等离子体反应室中的氯化化学（chlorinated chemistry）。在一种实施方式中，蚀刻剂配方可以由 NF_3 和 Cl_2 的组合构成，其中将氩或氦用作缓冲气体或载气。活性蚀

刻剂物质的流速可以在 50 到 200 标准立方厘米每分钟（SCCM）之间变化，而载气的流速可以在 150 到 400 SCCM 之间变化。可以在 700W 到 1100W 范围内的功率下，以小于 100W 的低 RF 偏置，使用高能量等离子体。反应室压力可以在大约 1 帕斯卡（Pa）到大约 2Pa 的范围内。

在另一实施方式中，蚀刻剂化学物质可以由 HBr 和 Cl_2 的组合构成。蚀刻剂物质的流速可以在 40 SCCM 到 100 SCCM 之间变化。可以在大约 600W 到大约 1000W 范围内的功率下，以小于 100W 的低 RF 偏置，使用高能量等离子体。反应室压力可以在大约 0.3Pa 到大约 0.8Pa 的范围内。在另一实施方式中，蚀刻剂化学物质可以由 SF_6 和 Cl_2 的组合构成。SF_6 的流速可以在 3 SCCM 到 10 SCCM 之间变化，Cl_2 的流速可以在 20 SCCM 到 60 SCCM 之间变化。可以在大约 400W 到大约 900W 范围内的功率下，在没有 RF 偏置的情况下或以小于 50W 的 RF 偏置，使用高能量等离子体。在这种实施方式中，可以保持低的 SF_6 的流速和反应室压力，以降低去除速率并使控制最大化。例如，反应室压力可以在大约 0.1Pa 到大约 0.5Pa 的范围内。在另一实施方式中，蚀刻剂化学物质可以由 Ar 和 Cl_2 的组合构成。这里，蚀刻剂物质的流速可以在 40 SCCM 到 80 SCCM 之间变化。可以在从大约 400W 到大约 800W 范围内的功率下，以大约 100W 到 200W 之间的高 RF 偏置，使用中等能量等离子体。反应室压力可以在大约 1Pa 到大约 2Pa 的范围内。

图 3D 示出了已经执行干法蚀刻工艺之后的衬底 300。如图所示，形成了源极区空腔 312 和漏极区空腔 314。此外，已经通过蚀刻掺杂区 308 形成源极延伸部分空腔 312A 和漏极延伸部分空腔 314A。由于使用了增加掺杂区 308 的蚀刻速率的掺杂剂和蚀刻剂配方，隔离层 310 的厚度对蚀刻源极延伸部分空腔 312A 和漏极延伸部分空腔 314A 的影响最小。

在完成干法蚀刻工艺之后，可以应用湿法蚀刻工艺，以清洁和进一步蚀刻源极区空腔 312、源极延伸部分空腔 312A、漏极区空腔 314 以及漏极延伸部分空腔 314A（212）。可以使用现有技术中公知的用于清洁硅和氧化物材料的常规湿法蚀刻化学物质。例如，可以使用能够沿晶面去除硅的湿法蚀刻化学物质。

湿法蚀刻至少用于两个目的。首先，湿法蚀刻去除诸如碳、氟、含氯

氟烃的污染物以及诸如氧化硅的氧化物，以提供可以在其上执行后续处理的清洁表面。其次，湿法蚀刻沿着<111>和<001>晶面去除衬底的薄部分，以提供可以在其上发生高质量外延沉积的光滑表面。所蚀刻掉的衬底的薄部分可最高达 5nm 厚，并且还可以去除残余污染物。如图 3E 所示，湿法蚀刻使得源极区空腔 312、源极延伸部分 312A、漏极区空腔 314 和漏极延伸部分 314A 的边缘沿着<111>和<001>晶面。还应当指出，源极和漏极延伸部分 312A 和 314A 不具有在常规处理中发生的子弹形轮廓。

用于形成MOS晶体管的工艺的其余部分类似于常规的MOS处理技术。例如，在蚀刻工艺之后，可以利用选择性外延沉积工艺用硅合金填充源极和漏极区空腔，包括源极和漏极延伸部分（214）。因此，该外延沉积在一个工艺中形成源极和漏极区以及源极和漏极延伸部分。在一些实施方式中，硅合金可以是原位掺杂的硅锗、原位掺杂的碳化硅或原位掺杂的硅。在可选实施方式中，可以使用其他的硅合金。例如，可以使用的可选硅合金材料包括，但不限于硅化镍、硅化钛、硅化钴，并且可能掺杂有硼和/或铝的一种或多种。在一些实施方式中，可以使用 CVD 工艺进行沉积。

在实施方式中，沉积在源极和漏极区空腔中的硅合金材料的晶格间距与衬底材料的晶格间距不同。晶格间距的差异在 MOS 晶体管的沟道区中引起拉伸或压缩应力，由于在源极和漏极延伸部分中沉积硅合金而增强了所述应力。如本领域技术人员所知，决定是引起拉伸应力还是压缩应力将取决于是形成 NMOS 还是 PMOS 晶体管。

根据本发明的实施方式，对于 NMOS 晶体管而言，可以利用掺碳硅（carbon doped silicon）填充源极和漏极区空腔。可以以外延和选择性的方式沉积掺碳硅。在其他实施方式中，还可以用磷对掺碳硅进行原位掺杂。碳浓度可以在 0.5 原子百分比到 3.0 原子百分比的范围内。磷浓度可以在 5×10^{19}/cm3 到 $5\times10^{20}/cm^3$ 的范围内。掺碳硅的厚度可以在 400Å 到 1200Å 的范围内。掺碳和磷的硅可以表示为 $(C,P)_ySi_{(1-y)}$。

可以在低压化学气相沉积（LPCVD）反应室中，利用多达 60 个沉积周期和基于硅烷（SiH_4）、PH_3、CH_3SiH_3 和氯气（Cl_2）化学物质的蚀刻次序，进行高掺杂$(C,P)_ySi_{(1-y)}$源极和漏极区的沉积。反应室温度可以在500℃到625℃之间，反应室压力可以低于 20Pa。为了实现选择性、外延和高掺杂剂浓

度，可以使用以下段落中所描述的工艺参数。

对于沉积阶段而言，共反应剂可以包括流速在 100 到 400 标准立方厘米每分钟（SCCM）之间的 SiH_4、流速在 25 到 150 SCCM 之间的 CH_3SiH_3、流速在 1 到 25 SCCM 之间的 PH_3、以及流速在 500 到 4000 SCCM 之间的 H_2。沉积阶段的每个周期可以持续最高达 4 分钟。

沉积阶段之后可以是第一清洗阶段。第一清洗可以包括流速在 500 SCCM 到 2 标准升每分钟（SLM）之间的氮气以及流速在 5 到 50 SCCM 之间的 N_2Cl_2。第一清洗阶段的每个周期可以持续最高达 10 秒。

蚀刻阶段可以在清洗阶段之后。对于蚀刻阶段而言，共反应剂可以包括流速在 5 到 25 SCCM 之间的 Cl_2。蚀刻阶段的每个周期可以持续最高达 30 秒。

蚀刻阶段之后可以是第二清洗阶段。该第二清洗可以包括流速在 50 SCCM 扫 2 SLM 之间的氮气以及流速在 5 到 35 SCCM 之间的 N_2Cl_2。第二清洗阶段的每个周期可以持续最高达 10 秒。

第二清洗阶段之后可以是第三清洗阶段。第三清洗可以包括流速在 5 到 25 SLM 之间的氢气（H_2）。第三清洗阶段的每个周期可以持续最高达 2 分钟。

根据本发明的实施方式，对于 PMOS 晶体管而言，可以利用硅锗填充源极和漏极区空腔。硅锗可以是外延沉积的。锗浓度可以在 10 原子百分比到 50 原子百分比的范围内。在其他实施方式中，还可以用硼对硅锗进行原位掺杂。硼浓度可以在 $2\times10^{19}/cm^3$ 到 $7\times10^{20}/cm^3$ 的范围内。硅锗的厚度可以在 40Å 到 1500Å 的范围内。

可以在 CVD 反应室、LPCVD 反应室或超高真空 CVD（UHVCVD）中进行被掺杂的硅锗的沉积。反应室温度可以在 600℃和 800℃之间，反应室压力可以在 1 到 760 托之间。载气可以由流速在 10 到 50 SLM 之间的范围内的氢气或氮气构成。

可以利用诸如二氯甲硅烷（DCS 或 SiH_2Cl_2）、硅烷（SiH_4）或乙硅烷（Si_2H_6）的硅源前体气体进行沉积。例如，可以在范围在 15 到 100 SCCM 之间的流量下使用 DCS。沉积还可以使用锗源前体气体，例如在 H_2 中稀释的 GeH_4（例如可以将 GeH_4 稀释为 1-5%）。例如，可以以 1%的浓度和范围

在 50 到 300 SCCM 之间的流速使用稀释的 GeH_4。对于硼的原位掺杂，可以使用稀释的 B_2H_6（例如可以在 H_2 中将 B_2H_6 稀释为 1-5%）。例如，可以以 3%的浓度和范围在 10 到 100 SCCM 之间的流速使用稀释的 B_2H_6。在一些实施方式中，可以添加蚀刻剂以提高沉积的选择性。例如，可以以范围在 50 到 300 SCCM 之间的流速添加 HCl 或 Cl_2。

图 3F 示出了 MOS 晶体管 316，其中已经用硅合金填充了源极空腔 312 以形成源极区 318，已经用硅合金填充了漏极空腔 314 以形成漏极区 320。也填充了延伸部分以形成外延源极延伸部分 318A 和外延漏极延伸部分 320A。如图 3F 所示，与通过注入和扩散技术形成且因此在尖端区域和沟道区之间没有清晰边界的常规源极和漏极尖端区域不同，本发明的自对准外延源极和漏极延伸部分具有陡峭的边界。换言之，外延源极/漏极延伸部分和沟道区之间的界面是清晰而明确的。在界面的一侧是外延沉积的掺杂硅材料，在界面的另一侧是构成沟道区的衬底材料。外延源极/漏极延伸部分中的掺杂剂基本或完全保持在延伸部分内，并不趋向于扩散到沟道区中，从而允许外延源极和漏极延伸部分能够相对于常规技术使重掺杂硅材料非常接近沟道区（即源极/漏极延伸部分 318A/320A 可以底切栅极电介质层 302 超过 10nm）。如本领域技术人员将要认识到的，这又使得栅极长度能够被缩小，而不必缩短沟道区。

较靠近沟道区形成外延源极和漏极延伸部分还给沟道带来更大的流体静应力。该应力增大了沟道内的应变，从而提高了沟道中的迁移率并增大了驱动电流。还可以通过提高外延源极和漏极延伸部分的掺杂来进一步放大该应力，在硅合金的外延沉积期间这很容易控制。与尖端区域一般不在沟道区上引起应变的常规扩散工艺相比，这是一种改进。

如本领域技术人员将要认识到的，MOS 晶体管 316 还可以经受进一步的 MOS 处理，例如替换栅极氧化物工艺、替换金属栅极工艺、退火或硅化工艺（salicidation process），所述处理可以进一步改变晶体管 316 和/或提供必要的电互连。例如，在外延沉积源极/漏极区和源极/漏极延伸部分之后，可以在晶体管 316 上方沉积层间电介质（ILD）并进行平面化（216）。可以使用公知的可应用于集成电路结构的电介质层的材料，例如低 k 电介质材料来形成 ILD。这种电介质材料包括但不限于诸如二氧化硅（SiO_2）和碳掺

杂氧化物（CDO）的氧化物、氮化硅、诸如过氟化环丁烷或聚四氟乙烯的有机聚合物、氟硅酸盐玻璃（FSG）以及诸如硅倍半氧烷（silsesquioxane）、硅氧烷或有机硅酸盐玻璃的有机硅酸盐。电介质层可以包括微孔或其他孔穴以进一步减小其介电常数。图 3G 示出了已经沉积在 MOS 晶体管 316 上方的 ILD 层 322。

接下来，在本发明使用替换金属栅极工艺的实施方式中，可以利用蚀刻工艺去除栅极叠置体（即高 k 栅极电介质层 302、牺牲栅电极 304 和硬掩模层 306）（218）。用于去除这些层的方法在现有技术中是公知的。在可选实施方式中，仅去除牺牲栅极 304。图 3H 示出了在蚀刻掉栅极叠置体时形成的沟槽开口。

如果去除了栅极电介质层，可以将新的栅极电介质层沉积到沟槽开口中（220）。这里可以使用上述高 k 电介质材料，例如氧化铪。也可以使用相同的沉积工艺。可以利用栅极电介质层的替换来解决在应用干法和湿法蚀刻工艺期间可能对原始栅极电介质层造成的任何损害。然后可以在栅极电介质层之上沉积金属栅电极层（222）。可以使用常规的金属沉积工艺来形成金属栅电极层，例如 CVD、ALD、PVD、无电镀或电镀。图 3I 示出了已经沉积到沟槽开口中的高 k 栅极电介质层 324 和金属栅电极 326。

根据晶体管是 PMOS 还是 NMOS 晶体管，金属栅电极层可以由 P 型功函数金属或 N 型功函数金属构成。在一些实施方式中，形成 PMOS 晶体管，并且可用于形成 P 型功函数金属层的材料包括但不限于钌、钯、铂、钴、镍和导电金属氧化物，例如氧化钌。P 型金属层将使得能够形成功函数在大约 4.9eV 到大约 5.2eV 之间的 PMOS 栅电极。或者，在一些实施方式中，形成 NMOS 晶体管，并且可用于形成 N 型功函数金属层的材料包括但不限于铪、锆、钛、钽、铝及它们的合金，例如包括这些元素的金属碳化物，即碳化铪、碳化锆、碳化钛、碳化钽和碳化铝。N 型金属层将使得能够形成功函数在大约 3.9eV 到大约 4.2eV 之间的 NMOS 栅电极。在一些实施方式中，可以沉积两个或更多的金属栅电极层。例如，可以沉积功函数金属，随后是诸如铝金属的金属栅电极填充金属。

因此，已经公开了自对准外延源极和漏极延伸部分，所述延伸部分由于掺杂硅体积（例如硼掺杂的硅锗体积）的增大与硅体积减小的结合，而

减小了 MOS 晶体管的总电阻，并增大了沟道应变。外延源极和漏极延伸部分不具有子弹形轮廓，在沟道区与源极和漏极区之间形成陡峭的边界，并具有更容易控制的掺杂浓度，获得更加优化的源极-漏极轮廓。此外，通过选择掺杂剂和蚀刻剂配方的适当组合，本发明的实施方式能够蚀刻源极和漏极延伸部分而基本不受隔离层厚度的影响。因此，该自对准工艺提高了性能，同时使工艺变化最小化。

图 4 为示出了可通过本文所公开的自对准方法实现的改进的曲线图。线 400 表示针对利用本发明实施方式构建的 MOS 器件采集的数据。如图所示，与利用常规方法形成的器件相比，UC 到 UC 距离受隔离层厚度的影响要小得多，针对常规方法形成的器件的数据由线 118 表示。

以上对本发明所示实施方式的描述，包括在摘要中描述的内容，并不旨在是穷举性的或将本发明限于所公开的精确形式。尽管在本文中为了说明的目的描述了本发明的具体实施方式和例子，但如本领域的技术人员将认识到的，在本发明的范围内各种等价的修改都是可能的。

可以依据以上详细描述对本发明进行这些修改。在所附权利要求书中使用的术语不应被视为将本发明限于在说明书和权利要求中所公开的具体实施方式。相反，本发明的范围完全由所附权利要求书决定，应根据权利要求解释的确立原则来解释所附权利要求书。

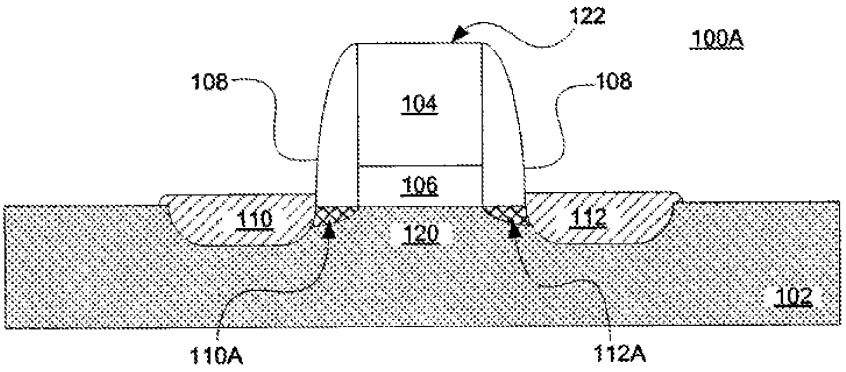

122
100A
108
108
104
106
110
120
112
102
110A
112A

图1A

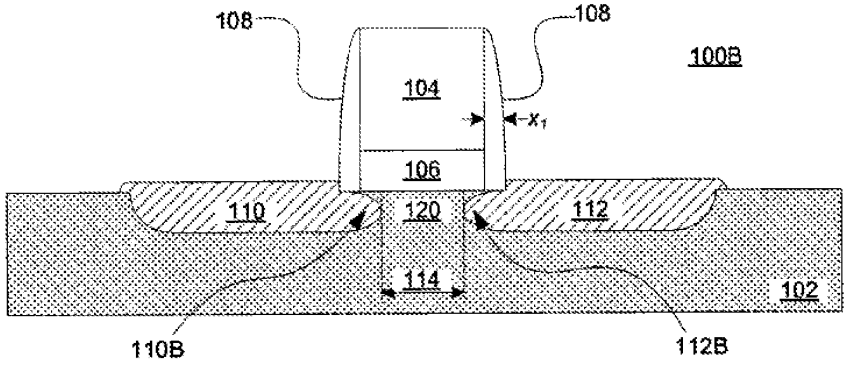

108
108
100B
104
x_1
106
110
120
112
114
102
110B
112B

图1B

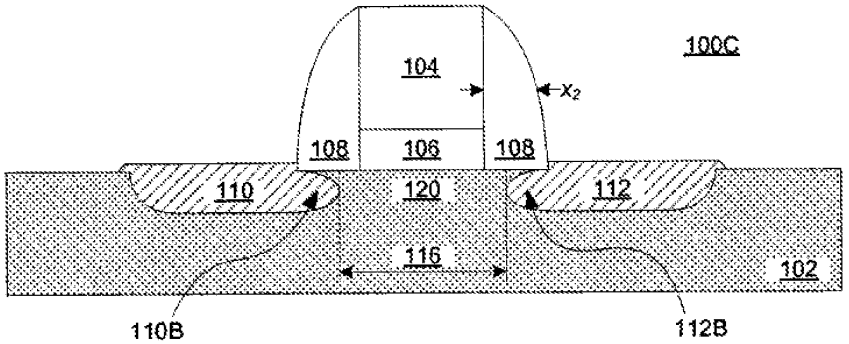

100C
104
x_2
108
106
108
110
120
112
116
102
110B
112B

图1C

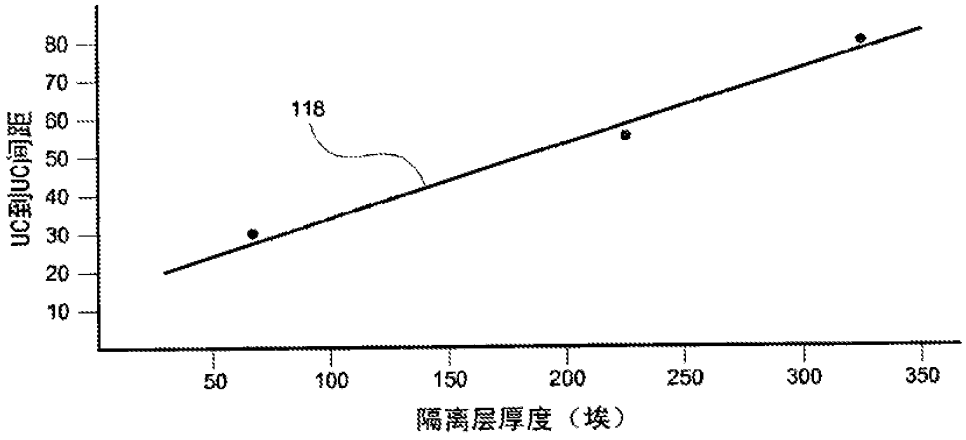


图1D

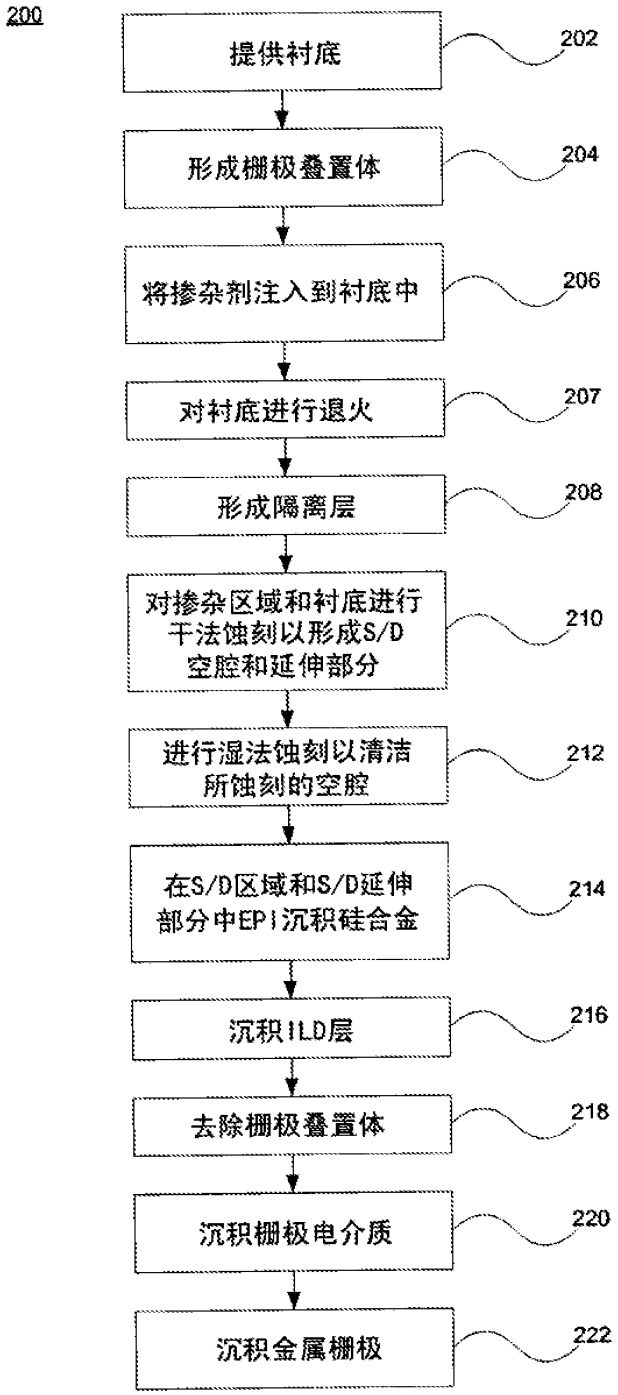

200
提供衬底
202
形成栅极叠置体
204
将掺杂剂注入到衬底中
206
对衬底进行退火
207
形成隔离层
208
对掺杂区域和衬底进行干法蚀刻以形成S/D空腔和延伸部分
210
进行湿法蚀刻以清洁所蚀刻的空腔
212
在S/D区域和S/D延伸部分中EPI沉积硅合金
214
沉积ILD层
216
去除栅极叠置体
218
沉积栅极电介质
220
沉积金属栅极
222

图2

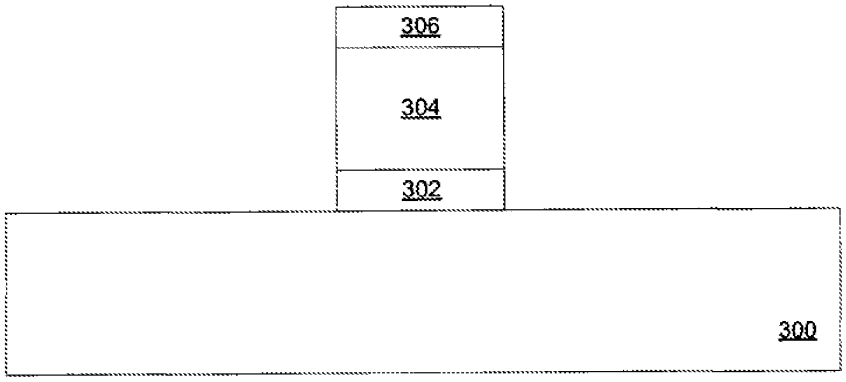


图3A

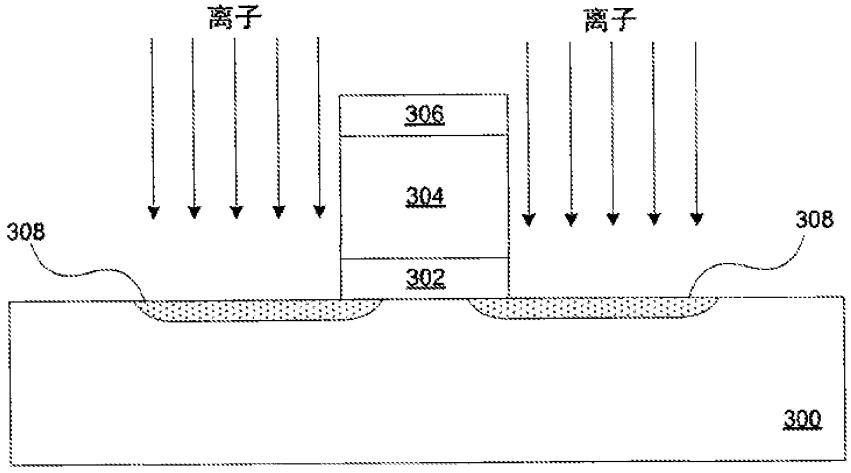


图3B

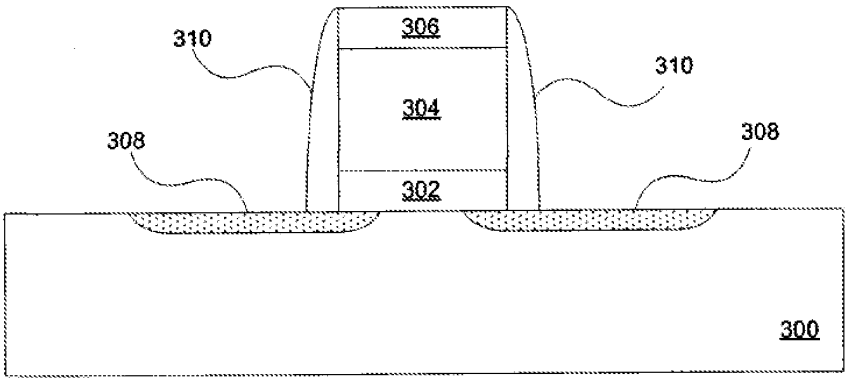

310
306
310
304
308
308
302
300

图3C

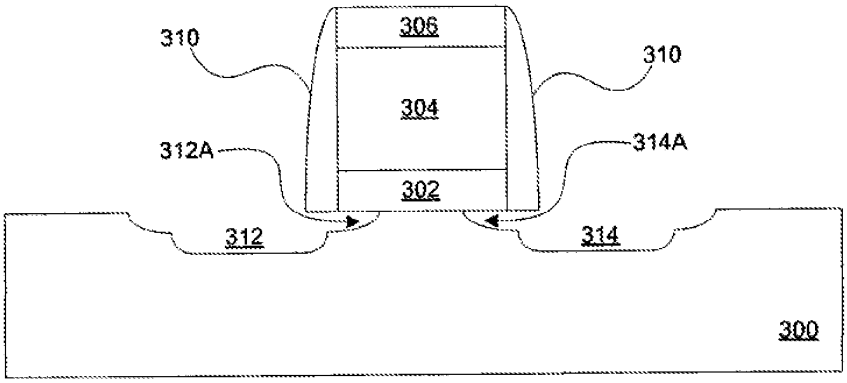

310
306
310
304
312A
314A
302
312
314
300

图3D

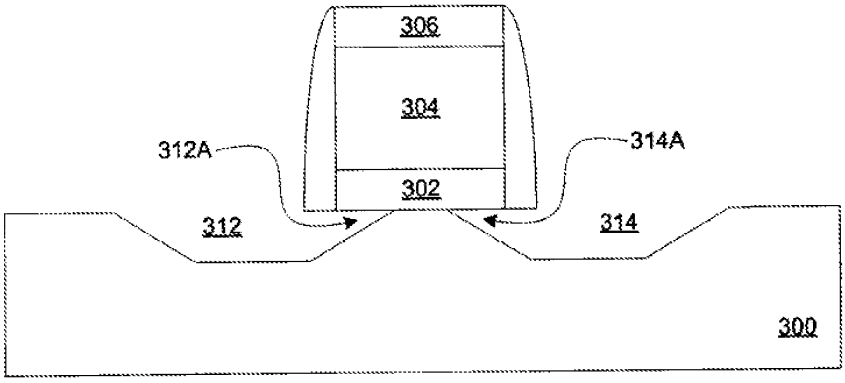

306
304
312A
314A
302
312
314
300

图3E

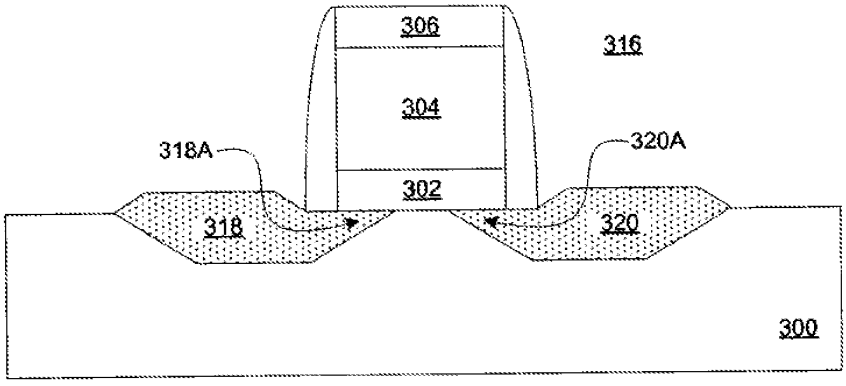

306
316
304
318A
320A
302
318
320
300

图3F

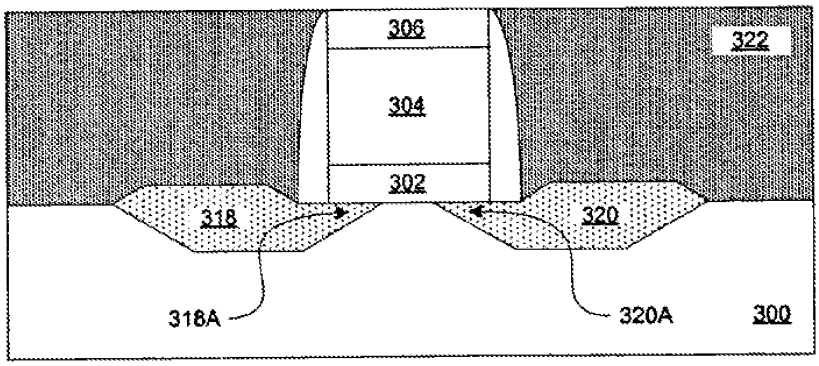

306
304
302
322
318
320
318A
320A
300

图3G

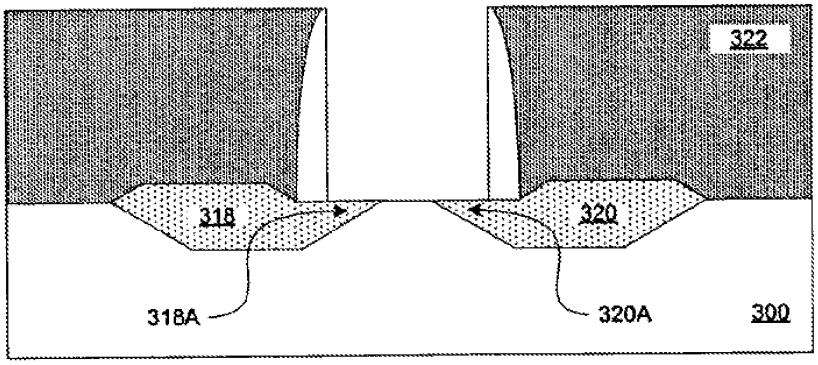

322
318
320
318A
320A
300

图3H

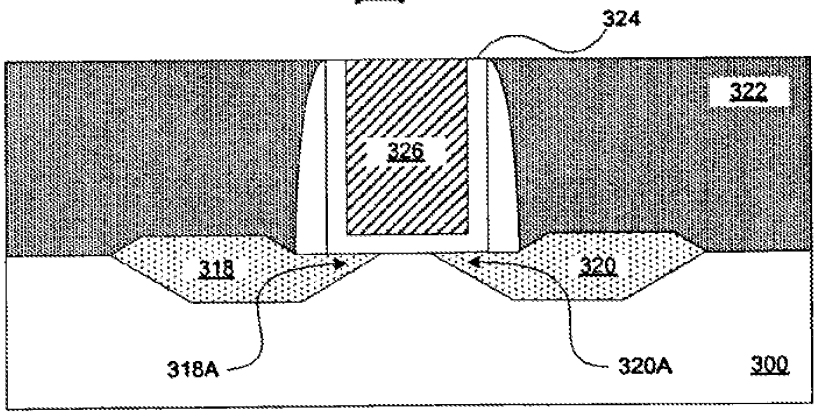

324
322
326
318
320
318A
320A
300

图3I

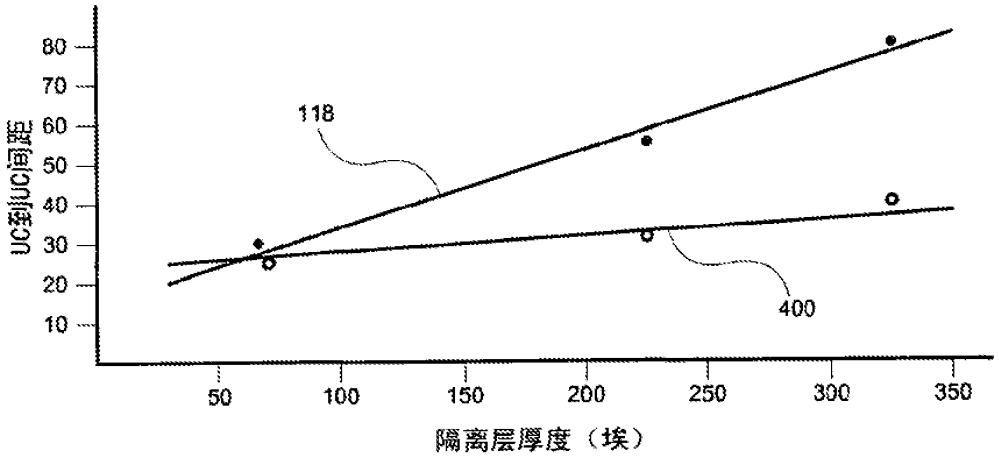

80
70
60
50
40
30
20
10
UC到UC间距
118
400
50
100
150
200
250
300
350
隔离层厚度（埃）

图4

Espacenet

Bibliographic data: JPH05183160 (A) — 1993-07-23

SEMICONDUCTOR DEVICE AND FABRICATION THEREOF

Inventor(s): NISHIYAMA AKIRA; USHIKU YUKIHIRO ± (NISHIYAMA AKIRA, ; USHIKU YUKIHIRO)

Applicant(s): TOSHIBA CORP ± (TOSHIBA CORP)

Classification: **- international:*H01L21/28; H01L29/43; H01L29/78;***
(IPC1-7): H01L29/46; H01L29/784
- cooperative:

Application number: JP19910345630 19911226

Priority number (s): JP19910345630 19911226

Abstract of JPH05183160 (A)

PURPOSE:To provide a semiconductor device wherein contact resistance is not increased even though the device is made finer. CONSTITUTION:There are provided on a silicon substrate 1 a gate electrode 4 formed through a gate oxide film 3, a source-drain diffusion layer 6 formed on the surface of the silicon substrate 1 oppositely to the gate electrode 4, a source-drain electrode 9 formed on the source-drain diffusion layer 6, and a Si-Ge mixed crystal layer 8 displaced between the source-drain electrode 9 and the source-drain diffusion layer 6.

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DESCRIPTION JPH05183160

[0001]
BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a semiconductor device capable of reducing contact resistance and a method of manufacturing the same.

【産業上の利用分野】本発明は、コンタクト抵抗の低減化を図り得る半導体装置及びその製造方法に関する。

[0002]
2. Description of the Related Art In recent years, large-scale integrated circuits (LSI) formed by integrating a large number of transistors, resistors and the like to achieve an electric circuit and integrating them on one chip are formed in important parts of computers and communication devices. It is used extensively. Therefore, the performance of the entire device is closely linked to the performance of the single LSI.

【従来の技術】近年、コンピューターや通信機器の重要部分には、多数のトランジスタや抵抗等を電気回路を達成するようにむすびつけ、１チップ上に集積化して形成した大規模集積回路（ＬＳＩ）が多用されている。このため、機器全体の性能は、ＬＳＩ単体の性能と大きく結び付いている。

[0003]
The performance improvement of a single LSI can be realized by increasing the degree of integration, that is, by miniaturizing the element. As the miniaturization of elements progresses, the diameter of the contact hole connecting the wiring material and each element becomes smaller, and the contact area between the wiring material and the element becomes smaller. As a

result, the resistance in the contact hole, so-called contact resistance, increases with the miniaturization of the device. For this reason, the contact resistance acts as a parasitic resistance, the current supplied to the device decreases, and an operation delay occurs.

ＬＳＩ単体の性能向上は、集積度を高めること、つまり、素子の微細化により実現できる。素子の微細化が進と、配線材と各素子とを結ぶコンタクトホールの径が小さくなり、配線材と素子との接触面積が小さくなる。この結果、コンタクトホールにおける抵抗、いわゆる、コンタクト抵抗は、素子の微細化とともに増大する。このため、コンタクト抵抗が寄生抵抗として働き、素子に供給される電流が少なくなり、動作遅延が生じる。

[0004]

Therefore, in an electric field transistor (FET), as shown in FIG. 14, a method of forming silicide 93 on the surface of source / drain diffusion layer 92 has been studied. In this method, after forming the source / drain diffusion layer 92, an insulating film 93 is formed on the sidewall of the polysilicon gate electrode 91, and subsequently, a metal film made of titanium or the like is deposited on the entire surface of the silicon substrate 90. The metal film is heat-treated to form the polysilicon gate electrode 91 and the drain / source diffusion layer 92 into silicide, and thereafter, the unreacted metal film is removed by etching.

そこで、電界トランジスタ（ＦＥＴ）においては、図１４に示すように、ソース・ドレイン拡散層９２の表面にシリサイド９３を形成する方法が検討されている。この方法は、ソース・ドレイン拡散層９２を形成した後に、ポリシリコンゲート電極９１の側壁に絶縁膜９３を形成し、続いて、シリコン基板９０の全面に、チタン等からなる金属膜を堆積し、この金属膜に熱処理を施してポリシリコンゲート電極９１、ドレイン・ソース拡散層９２をシリサイド化し、この後、未反応の金属膜をエッチング除去するというものである。

[0005]

By using such a method, the effective contact area between the source / drain diffusion layer 92 and the source / drain electrode 95 is the same as the area of the source / drain diffusion layer 92 even if the diameter of the contact hole is reduced. It is possible to prevent an increase in contact resistance.

このような方法を用いることで、コンタクトホールの径が小さくなっても、ソース・ドレイン拡散層９２とソース・ドレイン電極９５との実効的な接触面積を、ソース・ドレイン拡散層９２の面積と同じにでき、コンタクト抵抗の増大を防止できる。

[0006]

However, as miniaturization advances further in the future, the area of the source / drain

diffusion layer 92 is expected to decrease to about 1.0 μm 2. As a result, even if the contact area is the same as the area of the source / drain 92, The contact resistance value is high, causing problems such as operation delay.

しかしながら、今後さらに微細化が進んでいくと、ソース・ドレイン拡散層９２の面積が１．０μｍ2 程度まで小さくなると予想され、この結果、接触面積がソース・ドレイン９２の面積と同じであっても、コンタクト抵抗の値は高いものとなり、動作遅延等の問題が生じる。

In particular, the contact resistance between the p @ + diffusion layer and the silicide is higher than that between the n @ + diffusion layer and the silicide, and it is necessary to lower the resistance of this portion.

特に、ｐ＋拡散層とシリサイドとの間のコンタクト抵抗は、ｎ＋拡散層とシリサイドとの間のそれに比べ高く、この部分を低抵抗化する必要がある。

[0007]

As described above, if the device is further miniaturized in the future, the area of the source / drain diffusion layer becomes very small even in the FET using silicide, so the source / drain There is a problem that the contact area between the electrode and the source / drain diffusion layer is reduced, thereby increasing the contact resistance and causing problems such as operation delay.

【発明が解決しようとする課題】上述の如く、今後さらに素子の微細化が進むと、シリサイドを用いたＦＥＴであっても、ソース・ドレイン拡散層の面積が非常に小さくなるので、ソース・ドレイン電極とソース・ドレイン拡散層との接触面積が小さくなり、これにより、コンタクト抵抗が増大し、動作遅延等の問題が生じるという問題があった。

[0008]

The present invention has been made in consideration of the above circumstances, and an object of the present invention is to provide a semiconductor device which does not cause an increase in contact resistance even if the miniaturization of the device is further advanced, and a method of manufacturing the same. is there.

本発明は、上記事情を考慮してなされたもので、その目的とするところは、今後さらに素子の微細化が進んでも、コンタクト抵抗の増大を招かない半導体装置及びその製造方法を提供することにある。

[0009]
SUMMARY OF THE INVENTION In order to achieve the above object, a semiconductor device according to the present invention comprises a silicon substrate and a source / drain diffusion layer formed on a silicon substrate, a silicon A mixed crystal layer comprising an element is provided, and as the predetermined element, a difference between an energy level at a valence band edge of the mixed crystal layer and a Fermi level of the source / drain electrode is the source / drain diffusion. It is characterized in that an element smaller than the difference between the energy level at the valence band edge of the layer and the Fermi level of the source / drain electrode is selected.

【課題を解決するための手段】上記の目的を達成するために、本発明の半導体装置は、シリコン基板に形成されたソース・ドレイン拡散層とソース・ドレイン電極との間に、シリコンと所定の元素とからなる混晶層が設けられ、前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする。

[0010]
Further, in the method of manufacturing a semiconductor device according to the present invention, after forming source / drain diffusion layers on a silicon substrate, a mixed crystal layer consisting of silicon and a predetermined element is formed on the source / drain diffusion layers using a CVD method. And the step of forming, as the predetermined element, the difference between the energy level at the valence band edge of the mixed crystal layer and the Fermi level of the source / drain electrode is the valence electron of the source / drain diffusion layer It is characterized in that an element smaller than the difference between the energy level at the band edge and the Fermi level of the source / drain electrode is selected.

また、本発明の半導体装置の製造方法は、シリコン基板にソース・ドレイン拡散層を形成した後、ＣＶＤ法を用いてシリコンと所定の元素とからなる混晶層を前記ソース・ドレイン拡散層上に形成する工程を有し、前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする。

Alternatively, instead of using the CVD method, the mixed crystal layer may be formed by implanting ions of a predetermined element satisfying the above-described conditions into the source / drain diffusion layer.

また、ＣＶＤ法を用いる代わりに、ソース・ドレイン拡散層に上述した条件を満たす所定の元素

のイオンを打込むことで、混晶層を形成しても良い。

[0011]
The contact resistance between the source / drain electrode and the source / drain diffusion layer decreases as the difference between the Fermi level of the source / drain electrode and the energy level of the valence band of the source / drain diffusion layer decreases.

【作用】ソース・ドレイン電極とソース・ドレイン拡散層とのコンタクト抵抗は、ソース・ドレイン電極のフェルミ準位とソース・ドレイン拡散層の価電子帯のエネルギー準位との差が小さいほど小さくなる。

[0012]
In the semiconductor device according to the present invention, the source / drain electrode is connected to the source / drain diffusion layer through the mixed crystal layer consisting of silicon and a predetermined element, and the energy of the valence band edge of the mixed crystal layer as the predetermined element An element in which the difference between the energy level and the Fermi level of the source / drain electrode is smaller than the difference between the energy level of the valence band edge of the source / drain diffusion layer and the Fermi level of the source / drain electrode It is used.

本発明の半導体装置では、ソース・ドレイン電極をシリコンと所定の元素からなる混晶層を介してソース・ドレイン拡散層と接続し、所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を用いている。

[0013]
That is, by connecting the source / drain diffusion layer and the source / drain electrode via the mixed crystal layer, the difference between the Fermi level of the source / drain electrode and the energy level of the valence band of the source / drain diffusion layer Is effectively reduced.

即ち、混晶層を介してソース・ドレイン拡散層とソース・ドレイン電極とを接続することで、ソース・ドレイン電極のフェルミ準位とソース・ドレイン拡散層の価電子帯のエネルギー準位との差を実効的に小さくしている。

[0014]
Therefore, even if the contact area between the source / drain electrode and the source / drain

diffusion layer is reduced due to the miniaturization of the device, the increase in the contact resistance due to this can be prevented by the decrease in the contact resistance by the mixed crystal layer.

したがって、素子の微細化により、ソース・ドレイン電極とソース・ドレイン拡散層との接触面積が小さくなっても、これによるコンタクト抵抗の増大は、上記混晶層によるコンタクト抵抗の減少により防止できる。

[0015]

In the method of manufacturing the semiconductor device, the mixed crystal layer is formed on the source / drain diffusion layer using the CVD method.

また、半導体装置の製造方法では、ＣＶＤ法を用いてソース・ドレイン拡散層上に混晶層を形成している。

Therefore, the mixed crystal layer can be formed without damaging the silicon substrate.

したがって、シリコン基板にダメージを与えること無く混晶層を形成できる。

[0016]

Embodiments of the present invention will be described below with reference to the drawings.

【実施例】以下、図面を参照しながら実施例を説明する。

1 and 2 are cross-sectional views of manufacturing processes of a MOS transistor according to a first embodiment of the present invention.

図１，図２は、本発明の第１の実施例に係わるＭＯＳトランジスタの製造工程断面図である。

[0017]

First, as shown in FIG. 1A, an element isolation oxide film 2 is formed on an n-type Si substrate 1.

まず、図１（ａ）に示す如く、ｎ型のＳｉ基板１上に、素子分離用酸化膜２を形成する。

Then, a gate oxide film 3 having a thickness of 8 nm is formed in the element formation region surrounded by the oxide film 2 using a thermal oxidation method, and subsequently, a polycrystalline silicon film to be a gate electrode 4 having a thickness of 300 nm on the entire surface. Deposit.

次いでこの酸化膜２で囲まれた素子形成領域に、熱酸化法を用いて厚さ８ｎｍのゲート酸化膜３を形成し、続いて、全面に厚さ３００ｎｍのゲート電極４となる多結晶シリコン膜を堆積する。

Then, the polycrystalline silicon film is patterned by photolithography to form the gate electrode 4.

そして、フォトリソグラフィ技術を用いて上記多結晶シリコン膜をパターニングしてゲート電極４を形成する。

[0018]

Next, as shown in FIG. 1B, a SiO2 film to be the sidewall gate insulating film 5 is deposited on the entire surface, and then the entire surface of the SiO2 film is etched back to form the sidewall gate insulating film 5 on the sidewalls of the gate electrode 4. Form.

次に図１（ｂ）に示す如く、全面に側壁ゲート絶縁膜５となるＳｉＯ２膜を堆積した後、このＳｉＯ２膜の全面をエッチバックして、ゲート電極４の側壁に側壁ゲート絶縁膜５を形成する。

Next, BF2 is implanted under conditions of an acceleration voltage of 40 keV and a dose of 5.times.10@15 cm @ -2, followed by heat treatment at 850 DEG C. for 30 minutes in a nitrogen atmosphere to form the p @ + -type source / drain diffusion layer 6 Do.

次いで加速電圧４０ｋｅＶ，ドーズ量５×１０15ｃｍ-2の条件でＢＦ２を注入し、続いて、窒素雰囲気中で８５０°Ｃ，３０分の熱処理を行なってｐ+型のソース・ドレイン拡散層６を形成する。

[0019]

Next, as shown in FIG. 2A, a SiO2 film 7 having a thickness of 800 nm is deposited on the entire surface by the CVD method, and then the source / drain diffusion layer 6 and the source / drain electrode 9 formed in a later step are formed. Form a contact hole for making contact.

次に図２（ａ）に示す如く、ＣＶＤ法を用いて、全面に厚さ８００ｎｍのＳｉＯ２膜７を堆積し

た後、ソース・ドレイン拡散層６と後工程で形成するソース・ドレイン電極９とのコンタクトを取るためのコンタクトホールを形成する。

Then, Ge + ion implantation is performed under the conditions of an acceleration voltage of 20 keV and a dose of 3 × 10 16 cm 2. Thereafter, heat treatment is performed in an Ar atmosphere at 600 ° C. for one hour to bond Ge and Si implanted into the Si substrate 1 at the lower portion of the contact hole. By such an ion implantation step and a heat treatment step, the Si-Ge mixed crystal layer 8 to be Si 0.8 Ge 0.2 can be formed on the surface of the Si substrate 1 at the lower part of the contact hole.

次いで加速電圧２０ｋｅＶ，ドーズ量３×１０16ｃｍ2の条件でＧｅ+のイオン注入を行なう。この後、Ａｒ雰囲気中で６００°Ｃ，１時間の熱処理を行ない、コンタクトホール低部のＳｉ基板１に注入されたＧｅとＳｉとを結合させる。このようなイオン注入工程，熱処理工程により、コンタクトホール低部のＳｉ基板１の表面で、Ｓｉ0.8 Ｇｅ0.2 となるＳｉ－Ｇｅ混晶層８を形成できる。

[0020]

Next, as shown in FIG. 2B, in order to sufficiently increase the impurity activation ratio of the Si—Ge mixed crystal layer 8 and the source / drain diffusion layer 6 therebelow, 1000 ° C. Perform heat treatment for seconds. Then, an 800 nm thick Al alloy film is deposited on the entire surface as an electrode material. Finally, the Al alloy film is patterned to form source / drain electrodes 9 to complete a MOS transistor.

次に図２（ｂ）に示す如く、Ｓｉ－Ｇｅ混晶層８及びその下のソース・ドレイン拡散層６の不純物活性化率を十分に高くするために、Ａｒ雰囲気中で１０００°Ｃ，１０秒の熱処理を行なう。次いで、電極材料として厚さ８００ｎｍのＡｌ合金膜を全面に堆積する。最後に、このＡｌ合金膜をパターニングしてソース・ドレイン電極９を形成してＭＯＳトランジスタが完成する。

[0021]

FIG. 3 is an energy band diagram of the source / drain diffusion layer 6, the Si—Ge mixed crystal layer 8 and the source / drain electrode 9 in the contact hole of the MOS transistor obtained by the above method, and FIG. It is that of the obtained MOS transistor, that is, a MOS transistor in which no Si—Ge mixed crystal layer is provided between the source / drain diffusion layer and the source / drain electrode. In the figure, ϕ B is the energy level difference between the Fermi level of the source / drain electrode and the energy level of the valence band edge of the mixed crystal layer or the source / drain diffusion layer in contact with the source / drain electrode. It is.

図３は、上記方法で得られたＭＯＳトランジスタのコンタクトホールにおけるソース・ドレイン拡散層６，Ｓｉ－Ｇｅ混晶層８，ソース・ドレイン電極９のエネルギーバンド図であり、図４は、従来方法で得られたＭＯＳトランジスタ、つまり、ソース・ドレイン拡散層とソース・ドレイン電極との間にＳｉ－Ｇｅ混晶層が設けられてないＭＯＳトランジスタのそれである。なお、図中、φＢは、ソース・ドレイン電極のフェルミ準位と、このソース・ドレイン電極と接触した混晶層又はソース・ドレイン拡散層の価電子帯端のエネルギー準位とのエネルギー準位差である。

[0022]
From these figures, it can be seen that the energy level difference .phi.B of the MOS transistor of this embodiment is smaller than that of the prior art. This is because, in the MOS transistor of this embodiment, the energy level of the minimum level of the valence band is shifted to the high level side under the influence of the Si—Ge mixed crystal layer 8. As described above, the ratio of Si to Ge in the Si—Ge mixed crystal layer 8 at the interface between the Si—Ge mixed crystal layer 8 and the source / drain electrode 9 is 4: 1. On the other hand, the contact resistance Rc between the semiconductor having a high impurity concentration and the metal is expressed by the following equation using the energy level difference .phi.B. Rc = .alpha.exp (A.phi.B / 1/2 Nd) where .alpha. Is a proportional coefficient, Nd is the interface density of holes, and A is a constant. From the above equation, it can be seen that the contact resistance Rc becomes smaller as the energy level difference .phi.B becomes smaller.

これらの図から、本実施例のＭＯＳトランジスタのエネルギー準位差φＢの方が、従来のそれより小さいことが分かる。これは、本実施例のＭＯＳトランジスタでは、Ｓｉ－Ｇｅ混晶層８の影響により、価電子帯の最小準位のエネルギレベルが高準位側にシフトしたからである。なお、上述したように、Ｓｉ－Ｇｅ混晶層８とソース・ドレイン電極９との界面における、Ｓｉ－Ｇｅ混晶層８のＳｉとＧｅとの比は４：１である。一方、不純物濃度が高い半導体と金属とのコンタクト抵抗Ｒｃは、エネルギー準位差φＢを用いて次式のように表わせられる。Ｒｃ＝αｅｘｐ（Ａφ Ｂ／1/2 Ｎｄ）ここで、αは比例係数，Ｎｄはホールの界面濃度，Ａは定数である。上式から、エネルギー準位差φＢが小さいほど、コンタクト抵抗Ｒｃが小さくなることが分かる。

[0023]
Therefore, since the contact resistance can be made smaller in the MOS transistor of this embodiment than in the conventional one, even if the area of the source / drain diffusion layer becomes smaller due to miniaturization, an operation delay due to the increase in contact resistance occurs. Absent.

したがって、本実施例のＭＯＳトランジスタの方が、従来のそれより、コンタクト抵抗を小さくできるので、微細化により、ソース・ドレイン拡散層の面積が小さくなっても、コンタクト抵抗の増大による動作遅延は生じない。

[0024]
Further, in the present embodiment, since the Si-Ge mixed crystal layer 8 is formed using the ion implantation method, the Ge concentration becomes higher closer to the substrate surface, and as a result, the Si-Ge mixed crystal layer 8 and the source / drain The energy level of the conduction band of the electrode changes smoothly as shown in FIG.

また、本実施例では、イオン注入法を用いてＳｉ－Ｇｅ混晶層８を形成するので、基板表面に近いほどＧｅ濃度が高くなり、この結果、Ｓｉ－Ｇｅ混晶層８及びソース・ドレイン電極の伝導帯のエネルギー準位は、図３に示したように滑らかに変化する。

[0025]
Thus, according to this embodiment, since the energy level difference .phi.B can be reduced, an increase in contact resistance can be prevented, and a MOS transistor can be obtained which does not cause an operation delay even if miniaturization is performed.

かくして本実施例によれば、エネルギー準位差φＢを小さくできるので、コンタクト抵抗の増大を防止でき、もって、微細化を行なっても動作遅延の起きないＭＯＳトランジスタを得ることができる。

In the present embodiment, the contact holes are not completely closed, but may be completely closed by a metal such as W.

なお、本実施例では、コンタクトホールを完全に塞いでいないが、W等の金属で完全に塞いでも良い。

[0026]
FIG. 6 is a cross-sectional view of a MOS transistor according to a second embodiment of the present invention.

図６は、本発明の第２の実施例に係わるＭＯＳトランジスタの断面図である。

The MOS transistor of this embodiment is different from that of the previous embodiment in that a Si-Ge mixed crystal layer is formed by using a CVD method.

本実施例のＭＯＳトランジスタが先の実施例のそれと異なる点は、ＣＶＤ法を用いて

Ｓｉ－Ｇｅ混晶層を形成したことにある。

[0027]
That is, after the gate oxide film 13, the gate electrode 14 and the sidewall gate insulating film 15 are formed in the element formation region of the silicon substrate 11 surrounded by the element isolation oxide film 12 by the same method as the previous embodiment. Ion implantation of BF2 is performed under the conditions of an acceleration voltage of 40 keV and a dose of 5.times.10@15 cm @ -2 to form a p-type source / drain diffusion layer 16. As shown in FIG. Next, a SiO2 film 17 is deposited on the entire surface, and a contact hole is opened in the SiO2 film 17.

即ち、先の実施例と同様な方法で、素子分離用酸化膜１２で囲まれたシリコン基板１１の素子形成領域に、ゲート酸化膜１３，ゲート電極１４，側壁ゲート絶縁膜１５を形成した後、加速電圧４０ｋｅＶ，ドーズ量５×１０15ｃｍ-2の条件でＢＦ２のイオン注入を行なってｐ型のソース・ドレイン拡散層１６を形成する。次に全面にＳｉＯ２膜１７を堆積した後、このＳｉＯ２膜１７にコンタクトホールを開口する。

[0028]
Next, the Si--Ge mixed crystal layer 18 is buried in the contact holes to a predetermined height by a selective CVD method using a mixed gas of SiH4, GeH4 and H2. Specifically, first, the total pressure of the mixed gas is set to 27 Pa (SiH 4 partial pressure: 6.5 Pa), the substrate temperature is set to 550 ° C., and the Si—Ge mixed crystal layer 18 is formed. Then, the GeH4 partial pressure is gradually raised to a final value of 1.3 Pa. During this time, the H2 partial pressure is decreased so that the SiH4 partial pressure and the total pressure become constant at 6.5 Pa and 27 Pa, respectively. After forming the Si-Ge mixed crystal layer 18 by the CVD method under such conditions, for example, ion implantation of 200 keV, 1.times.10@15 cm @ -2 and 30 keV, 3.times.10@15 cm @ -2 of B is performed, followed by the impurity. Is subjected to activation annealing at 1000 ° C. for about 10 seconds using Ar. Finally, source / drain electrodes 19 made of an Al alloy are formed to complete the MOS transistor.

次にＳｉＨ4とＧｅＨ4とＨ2との混合ガスを使用した選択ＣＶＤ法により、コンタクトホール内にＳｉ－Ｇｅ混晶層１８を所定の高さまで埋める。具体的には、最初、混合ガスの全圧力を２７Ｐａ（ＳｉＨ4分圧：６．５Ｐａ），基板温度を５５０°Cに設定してＳｉ－Ｇｅ混晶層１８を形成する。そして、徐々にＧｅＨ4分圧を高くし、最終的には１．３Ｐａとする。この間、ＳｉＨ4分圧，全圧力が、それぞれ６．５Ｐａ，２７Ｐａと一定になるように、Ｈ2分圧を減少させる。このような条件でＣＶＤ法によりＳｉ－Ｇｅ混晶層１８を形成した後、例えば、Ｂの２００ｋｅＶ，１×１０15ｃｍ-2と３０ｋｅＶ，３×１０15ｃｍ-2のイオン注入を行ない、続いて、この不純物にＡｒを用いた１０００°Ｃ，約１０秒の活性化アニールを施する。最後に、Ａｌ合金からなるソース・ドレイン電極１９を形成してＭＯＳトランジスタが完成する。

[0029]
If the GeH 4 partial pressure to the SiH 4 partial pressure is always constant, a Si—Ge mixed crystal layer in which the ratio of Si to Ge is constant at 4: 1 can be formed. In this case, a band structure as shown in FIG. That is, at the boundary between the Si—Ge mixed crystal layer 18 and the Si substrate 1, a band structure in which the conduction band is discontinuous is obtained.

なお、ＳｉＨ4分圧に対するＧｅＨ4分圧を常に一定にすれば、ＳｉとＧｅとの比が４：１と一定のＳｉ－Ｇｅ混晶層を形成でき、この場合、図５に示すようなバンド構造、つまり、Ｓｉ－Ｇｅ混晶層１８とＳｉ基板１との境界で伝導バンドが不連続なバンド構造が得られる。

[0030]
Even in the MOS transistor obtained by the method described above, the source / drain electrode 19 is connected to the source / drain diffusion layer 16 through the Si—Ge mixed crystal layer 18, so the conduction band edge and the valence band edge Regardless of discontinuities and continuity, the energy level difference ϕB decreases and the contact resistance decreases.

以上述べた方法で得られたＭＯＳトランジスタでも、ソース・ドレイン電極１９がＳｉ－Ｇｅ混晶層１８を介してソース・ドレイン拡散層１６に接続しているので、伝導帯端，価電子帯端の不連続，連続に関わらず、エネルギー準位差ϕBが小さくなり、コンタクト抵抗が小さくなる。

Therefore, even if the elements are miniaturized, the operating speed can be kept high. Further, since the Si-Ge mixed crystal layer 18 is formed by using the CVD method, there is no possibility of damaging the Si substrate 11 as in the case of ion implantation.

したがって、素子の微細化を行なっても、動作速度を速く保つことができる。また、ＣＶＤ法を用いてＳｉ－Ｇｅ混晶層１８を形成しているので、イオン注入の場合のようにＳｉ基板１１にダメージが与える恐れはない。

[0031]
In the present embodiment, the contact holes are not completely filled with the Si-Ge mixed crystal layer 18, but as shown in FIG. 7, the same applies even if the contact holes are completely filled with the Si-Ge mixed crystal layer 18. An effect is obtained.

なお、本実施例では、コンタクトホールをＳｉ－Ｇｅ混晶層１８で完全に埋めなかったが、図７に示すように、コンタクトホールをＳｉ－Ｇｅ混晶層１８で完全に埋めても同様な効果が得ら

れる。

[0032]
Also, instead of depositing the Si-Ge mixed crystal layer 18 in the contact holes to a predetermined height by selective CVD, after depositing Si-Ge on the entire surface, the entire surface is etched back to perform Si in the contact holes. The Ge mixed crystal layer 18 may be formed.

また、選択ＣＶＤ法により、コンタクトホール内にＳｉ－Ｇｅ混晶層１８を所定の高さまで堆積する代わりに、全面にＳｉ－Ｇｅに堆積した後、全面エッチバックを行なうことでコンタクトホール内にＳｉ－Ｇｅ混晶層１８を形成しても良い。

FIG. 8 is a cross-sectional view of the manufacturing process of the MOS transistor according to the third embodiment of the present invention.

図８は、本発明の第３の実施例に係わるＭＯＳトランジスタの製造工程断面図である。

[0033]
First, using the same method as in the first embodiment, as shown in FIG. 8A, a gate oxide film 23 and a gate electrode are formed on the element formation region of the silicon substrate 21 surrounded by the element isolation oxide film 22. A sidewall gate insulating film 25 and p-type source / drain diffusion layers 26 are formed.

先ず、第１の実施例と同様な方法を用いて、図８（ａ）に示す如く、素子分離用酸化膜２２で囲まれたシリコン基板２１の素子形成領域に、ゲート酸化膜２３，ゲート電極２４，側壁ゲート絶縁膜２５，ｐ型のソース・ドレイン拡散層２６を形成する。

[0034]
Next, as shown in FIG. 8B, Ge + ions are implanted under the conditions of an acceleration voltage of 20 keV and a dose of 3 × 10 16 cm −2 to introduce Ge on the surfaces of the gate electrode 24 and the source / drain diffusion layer 26.

次に図８（ｂ）に示す如く、Ｇｅ＋イオンを加速電圧２０ｋｅＶ，ドーズ量３×１０16ｃｍ-2の条件で打込み、ゲート電極２４，ソース・ドレイン拡散層２６の表面にＧｅを導入する。

Next, Ge and Si are bonded to each other using a heat treatment at 600 ° C. for one hour in an

Ar atmosphere to form a Si—Ge mixed crystal layer 28. Thereafter, heat treatment at 1000 ° C. for 10 seconds is performed in an Ar atmosphere to increase the activation ratio of the impurities in the Si—Ge mixed crystal layer 28 and the source / drain diffusion layer 26 thereunder and the gate electrode 24. .

次いでＡｒ雰囲気中で、６００°Ｃ，１時間の熱処理を用いてＧｅとＳｉとを結合させ、Ｓｉ－Ｇｅ混晶層２８を形成する。この後、Ｓｉ－Ｇｅ混晶層２８及びその下のソース・ドレイン拡散層２６並びにゲート電極２４中の不純物の活性化率を上げるために、１０００°Ｃ，１０秒の熱処理をＡｒ雰囲気中で行なう。

[0035]

Next, as shown in FIG. 8C, after depositing a SiO2 film 27 with a thickness of 800 nm on the entire surface by CVD, contact holes are opened in the SiO2 film 27. Then, as shown in FIG. Finally, an Al alloy film having a thickness of 800 nm is deposited on the entire surface, and this is patterned to form source / drain electrodes 29. Thus, the MOS transistor is completed.

次に図８（ｃ）に示す如く、ＣＶＤ法を用いて、全面に厚さ８００ｎｍのＳｉＯ２膜２７を堆積した後、このＳｉＯ２膜２７にコンタクトホールを開口する。最後に、全面に厚さ８００ｎｍのＡｌ合金膜を堆積した後、これをパターニングしてソース・ドレイン電極２９を形成してＭＯＳトランジスタが完成する。

[0036]

Even in the method described above, since the source / drain electrode 29 and the source / drain diffusion layer 26 are connected via the Si-Ge mixed crystal layer 28, the energy level difference φB becomes small, and as a result, miniaturization Even if it does, since the parasitic resistance by contact resistance can be kept low, an operation delay does not occur. In the present embodiment, the contact holes are not completely closed, but may be filled with a metal such as W to be completely closed.

以上述べた方法でも、Ｓｉ－Ｇｅ混晶層２８を介してソース・ドレイン電極２９とソース・ドレイン拡散層２６とが接続しているので、エネルギー準位差φBが小さくなり、この結果、微細化を行なっても、コンタクト抵抗による寄生抵抗を低く保つことができるので動作遅延は生じない。なお、本実施例では、コンタクトホールが完全に塞がれていないが、Ｗ等の金属を充填して完全に塞がれた構造としても良い。

[0037]

FIG. 9 is a cross-sectional view of the MOS transistor according to the fourth embodiment of the present invention. The MOS transistor of this embodiment is different from that of the third

embodiment in that a Si-Ge mixed crystal layer is formed by using the CVD method.

図９は、本発明の第４の実施例に係わるＭＯＳトランジスタの断面図である。本実施例のＭＯＳトランジスタが第３の実施例のそれと異なる点は、ＣＶＤ法用いてＳｉ－Ｇｅ混晶層を形成したことにある。

[0038]

That is, after the gate oxide film 33, the gate electrode 34, the sidewall gate insulating film 35, and the p-type source / drain diffusion layer 36 are formed in the element formation region of the silicon substrate 31 surrounded by the element isolation oxide film 32; A Si—Ge mixed crystal layer 38 is selectively formed on the source / drain diffusion layer 36 to a thickness of, for example, 50 nm using a selective CVD method. Thereafter, the same steps of depositing the SiO 2 film 37 as in the previous embodiment, opening the contact holes, and forming the source / drain electrodes 39 are performed to complete the MOS transistor. The impurity is introduced into the Si-Ge mixed crystal layer 38 on the source / drain diffusion layer 36 by, for example, implanting B ions under conditions of an acceleration voltage of 40 keV and a dose of about 1 × 10 16 cm −2. The activation annealing may be performed at 10 ° C. for 10 seconds.

即ち、素子分離用酸化膜３２で囲まれたシリコン基板３１の素子形成領域に、ゲート酸化膜３３，ゲート電極３４，側壁ゲート絶縁膜３５，ｐ型のソース・ドレイン拡散層３６を形成した後、選択ＣＶＤ法を用いてソース・ドレイン拡散層３６上にＳｉ－Ｇｅ混晶層３８を例えば５０ｎｍの厚さに選択的に形成する。この後、先の実施例と同様なＳｉＯ2膜３７の堆積工程、コンタクトホールの開口工程、ソース・ドレイン電極３９の形成工程を経てＭＯＳトランジスタが完成する。なお、ソース・ドレイン拡散層３６上のＳｉ－Ｇｅ混晶層３８への不純物導入は、例えば、加速電圧４０ｋｅＶ，ドーズ量１×１０16ｃｍ-2程度の条件でＢのイオン注入を行なった後、１０００°Ｃ，１０秒の活性化アニールを行なえば良い。

[0039]

Even with the MOS transistor obtained by such a method, the same effect as that of the previous embodiment can be obtained. Also in the case of the present embodiment, the contact hole may be closed with a metal such as W. FIG. 10 is a cross-sectional view of the MOS transistor according to the fifth embodiment of the present invention.

このような方法で得られたＭＯＳトランジスタでも先の実施例と同様な効果が得られる。なお、本実施例の場合も、Ｗ等の金属でコンタクトホールを塞いでも良い。図１０は、本発明の第５の実施例に係わるＭＯＳトランジスタの断面図である。

[0040]

This will be described according to the manufacturing process. First, the gate oxide film 43, the gate electrode 44, and the sidewall gate insulating film 45 are formed in the device formation region of the silicon substrate 41 divided by the device isolation oxide film 42.

これを製造工程に従い説明すると、まず、素子分離用酸化膜４２で区分されたシリコン基板４１の素子形成領域に、ゲート酸化膜４３，ゲート電極４４，側壁ゲート絶縁膜４５を形成する。

[0041]

Next, ion implantation of B is performed to form a p-type source / drain diffusion layer 46, and then ion implantation of Ge is performed to form a Si—Ge mixed crystal layer 48.

次にＢのイオン注入を行なってｐ型のソース・ドレイン拡散層４６を形成し、引き続き、Ｇｅのイオン注入を行なってＳｉ－Ｇｅ混晶層４８を形成する。

Thereafter, in order to activate B in the source / drain diffusion layer 46, a heat treatment at 1000 ° C. for 10 seconds is performed in an Ar atmosphere as in the third embodiment.

この後、ソース・ドレイン拡散層４６のＢの活性化のために、第３の実施例と同様に１０００°Ｃ，１０秒の熱処理をＡｒ雰囲気中で行なう。

[0042]

Next, titanium silicide (TiSi2) 40 is selectively formed on the source / drain diffusion layer 46 by selective CVD method using a mixed gas of SiH4 and TiCl4 and setting the substrate temperature to 750.degree.

次にＳｉＨ４とＴｉＣｌ４との混合ガスを使用し、基板温度を７５０°Ｃに設定した選択ＣＶＤ法により、ソース・ドレイン拡散層４６上にチタンシリサイド（ＴｉＳｉ２）４０を選択的に形成する。

[0043]

Next, a SiO2 film 47 is deposited on the entire surface by the CVD method, and a contact hole is opened in the SiO2 film 47.

次にＣＶＤ法を用いてＳｉＯ２膜４７を全面に堆積した後、このＳｉＯ２膜４７にコンタクトホールを開口しする。

Finally, an Al alloy film is deposited on the entire surface and patterned to form source / drain electrodes 49, thereby completing the MOS transistor.

最後に、Ａｌ合金膜を全面に堆積し、これをパターニングしてソース・ドレイン電極４９を形成してＭＯＳトランジスタが完成する。

[0044]

According to the method described above, since the TiSi2 film 40 is provided between the Si-Ge mixed crystal layer 48 and the source / drain electrode 49, the contact resistance can be further reduced.

以上述べた方法によれば、Ｓｉ－Ｇｅ混晶層４８とソース・ドレイン電極４９との間にＴｉＳｉ２膜４０を設けたので、コンタクト抵抗をよりいっそう小さくできる。

[0045]

In this embodiment, the Si-Ge mixed crystal layer 48 is formed by using Ge ion implantation, but as shown in FIG. 11, the Si-Ge mixed crystal layer 48a is formed by using the selective CVD method. It is good.

なお、本実施例では、Ｇｅのイオン注入法を用いてＳｉ－Ｇｅ混晶層４８を形成したが、図１１に示すように、選択ＣＶＤ法を用いてＳｉ－Ｇｅ混晶層４８ａを形成しても良い。

In addition, the contact hole may be completely closed with a metal such as W. FIG. 12 is a cross-sectional view of the manufacturing process of the MOS transistor according to the sixth embodiment of the present invention.

また、Ｗなどの金属でコンタクトホールを完全に塞いでも良い。図１２は、本発明の第６の実施例に係わるＭＯＳトランジスタの製造工程断面図である。

[0046]

First, as shown in FIG. 12A, a SiO 2 film 52 for element isolation is formed on an n-type Si substrate 51. Next, Ge ions are implanted into the Si substrate 51 under the conditions of an acceleration voltage of 100 keV and a dose of 3 × 10 16 cm −2, followed by annealing at 600 ° C. for one hour in an Ar atmosphere. As a result, the Si-Ge mixed crystal layer 58 is formed in the vicinity of the substrate surface, and the Si layer 50 is formed thereon. Then, the Si layer 50 is thermally oxidized to form a gate oxide film 53 having a thickness of 8 nm, and a

polycrystalline silicon film to be a gate electrode 56 is deposited on the entire surface, and subsequently patterned using photolithography. The gate electrode 56 is formed. Thereafter, an SiO 2 film is deposited on the entire surface, and this is etched back to form a sidewall gate insulating film 55.

まず、図１２（ａ）に示す如く、ｎ型のＳｉ基板５１上に素子分離用ＳｉＯ2膜５２を形成する。次いでＧｅイオンを加速電圧１００ｋｅＶ，ドーズ量３×１０16ｃｍ-2の条件でＳｉ基板５１に打込み、続いて、Ａｒ雰囲気中で６００°Ｃ，１時間のアニールを行なう。この結果、基板表面付近にＳｉ－Ｇｅ混晶層５８が形成され、その上にＳｉ層５０が形成される。次いでこのＳｉ層５０を熱酸化して厚さ８ｎｍのゲート酸化膜５３を形成した後、全面にゲート電極５６となる多結晶シリコン膜を堆積し、続いて、これをフォトリソグラフィを用いてパターニングしてゲート電極５６を形成する。この後、ＳｉＯ２膜を全面に堆積し、これにエッチバックを施して側壁ゲート絶縁膜５５を形成する。

[0047]
Next, as shown in FIG. 12 (b), BF2 ions are implanted under the conditions of an acceleration voltage of 40 keV and a dose of 5.times.10@15 cm @ -2, followed by annealing at 850 DEG C. for 30 minutes in a nitrogen atmosphere. Source / drain diffusion layer 56 is formed.

次に図１２（ｂ）に示す如く、ＢＦ２イオンを加速電圧４０ｋｅＶ，ドーズ量５×１０15ｃｍ-2の条件で打ち込んだ後、窒素雰囲気中で８５０°Ｃ，３０分のアニールを行ない、ｐ型のソース・ドレイン拡散層５６を形成する。

[0048]
Next, as shown in FIG. 12C, after depositing a SiO2 film 57 having a thickness of 800 nm on the entire surface by using the CVD method, the SiO2 film 57 and the Si layer 50 thereunder are sequentially etched to obtain Si-Ge. A contact hole is formed to expose mixed crystal layer 58.

次に図１２（ｃ）に示す如く、ＣＶＤ法を用いて、全面に厚さ８００ｎｍのＳｉＯ２膜５７を堆積した後、ＳｉＯ２膜５７，その下のＳｉ層５０に順次エッチングを施し、Ｓｉ－Ｇｅ混晶層５８が露出するようにコンタクトホールを形成する。

Finally, an Al alloy film is deposited on the entire surface and patterned to form source / drain electrodes 59, thereby completing the MOS transistor.

最後に、全面にＡｌ合金膜を堆積し、これをパターニングしてソース・ドレイン電極５９を形成してＭＯＳトランジスタが完成する。

[0049]
Even in the method described above, the energy level difference ϕ B is reduced by the Si—Ge mixed crystal layer 58 as in the MOS transistor described above, so that the contact resistance can be reduced.

以上述べた方法でも、先に説明したＭＯＳトランジスタと同様にＳｉ－Ｇｅ混晶層５８によりエネルギー準位差φＢが小さくなるので、コンタクト抵抗の低減が図れる。

[0050]
Note that the Si—Ge mixed crystal layer 58 can be formed by using the selective CVD method instead of ion implantation.

なお、イオン注入の代わりに選択ＣＶＤ法を用いてもＳｉ－Ｇｅ混晶層５８を形成できる。

That is, after the SiO 2 film 52 for element isolation is formed, a Si—Ge mixed crystal layer 58 is deposited on the surface of the Si substrate 51 in the element formation region using the selective CVD method. The Si layer 50 may be deposited on the Si—Ge mixed crystal layer 58 by using. Also, the contact hole may be filled with a metal such as W.

即ち、素子分離用ＳｉＯ2膜５２を形成した後、選択ＣＶＤ法を用いて、素子形成領域のＳｉ基板５１の表面に、Ｓｉ－Ｇｅ混晶層５８を堆積し、この後、再び選択ＣＶＤ法を用いて、Ｓｉ－Ｇｅ混晶層５８上にＳｉ層５０を堆積すれば良い。また、コンタクトホールをW等の金属で埋込んでも良い。

[0051]
FIG. 13 is a cross-sectional view of the MOS transistor according to the seventh embodiment of the present invention. The portions corresponding to the MOS transistors in FIG. 12 are assigned the same reference numerals as in FIG. 12, and detailed descriptions thereof will be omitted. The MOS transistor of this embodiment is different from that of the sixth embodiment in that a silicide is formed on the Si-Ge mixed crystal layer 58.

図１３は、本発明の第７の実施例に係わるＭＯＳトランジスタの断面図である。なお、図１２のＭＯＳトランジスタと対応する部分には図１２と同一符号を付してあり、詳細な説明は省略する。本実施例のＭＯＳトランジスタが第６の実施例のそれと異なる点は、Ｓｉ－Ｇｅ混晶層５８上にシリサイドを形成したことにある。

[0052]
That is, after the source / drain diffusion layer 56 is formed, a Ti film is deposited on the entire surface, followed by annealing at 700 ° C. for 30 seconds in a nitrogen atmosphere. As a result, all of the Si layer 50 in contact with the Ti film is changed to the TiSi2 film 60. After this, the unreacted Ti film and TiN film are removed. The subsequent steps are the same as in the previous embodiment. By the above-described steps, the MOS transistor having the structure left on the TiSi2 film 60 on the gate electrode 54 and the source / drain diffusion layer 56 is obtained.

即ち、ソース・ドレイン拡散層５６を形成した後、全面にＴｉ膜を堆積し、続いて、窒素雰囲気中で７００°Ｃ，３０秒間のアニールを行なう。この結果、Ｔｉ膜と接触していたＳｉ層５０は全てＴｉＳｉ２膜６０に変わる。この後、未反応のＴｉ膜や、ＴｉＮ膜を除去する。この後の工程は先の実施例と同様である。以上の工程により、ゲート電極５４，ソース・ドレイン拡散層５６上にＴｉＳｉ2膜６０に残った構造のＭＯＳトランジスタが得られる。

[0053]
In the MOS transistor thus obtained, since the TiSi2 film 50 is formed between the Si-Ge mixed crystal layer 58 and the source / drain electrode 59, the contact resistance is further reduced. The contact holes may be completely filled with a metal such as W.

このようにして得られたＭＯＳトランジスタでは、Ｓｉ－Ｇｅ混晶層５８とソース・ドレイン電極５９との間にＴｉＳｉ２膜５０が形成されているので、コンタクト抵抗をよりいっそう小さくなる。なお、コンタクトホールがW等の金属で完全に埋込んで良い。

[0054]
The present invention is not limited to the embodiments described above. For example, in the MOS transistor of FIG. 7, the contact hole is completely filled with the Si-Ge mixed crystal layer by the whole surface deposition of Si-Ge and the etch back, but even if the contact hole is buried by the selective CVD method good. Although TiSi2 is used as the silicide in the fifth and seventh embodiments, other silicides may be used.

なお、本発明は上述した実施例に限定されるものではない。例えば、図７のＭＯＳトランジスタでは、Ｓｉ－Ｇｅの全面堆積と、エッチバックとにより、コンタクトホールをＳｉ－Ｇｅ混晶層で完全に埋めたが、選択ＣＶＤ法によりコンタクトホールの埋込みを行なっても良い。また、第５，第７の実施例では，シリサイドとしてＴｉＳｉ２を用いたが他のシリサイドを用いても良い。

[0055]

In the above embodiment, the p-channel MOS transistor is described, but the present invention is similarly applied to an n-channel MOS transistor, a MIS transistor using silicon other than the MOS transistor, and a CMOS transistor as well. it can.

また、上記実施例では、ｐチャネルのＭＯＳトランジスタの場合について説明したが、本発明は、ｎチャネルのＭＯＳトランジスタや，ＭＯＳトランジスタ以外のシリコンを用いたＭＩＳトランジスタ、更に、ＣＭＯＳトランジスタにも同様に適用できる。

[0056]

Although the mixed crystal layer of Si-Ge is used in the above embodiment, a mixed crystal layer of Si and another element, for example, a mixed crystal layer of Si and a Group IV element other than Ge may be used. .

また、上記実施例では、Ｓｉ－Ｇｅの混晶層を用いたが、Ｓｉと他の元素との混晶層、例えば、ＳｉとＧｅ以外のＩＶ族元素との混晶層を用いても良い。

The point is that the energy level difference ϕB should be small. In addition, various modifications can be made without departing from the scope of the present invention.

要はエネルギー準位差ϕＢが小さくなれば良い。その他、本発明の要旨を逸脱しない範囲で、種々変形して実施できる。

[0057]

As described above in detail, according to the present invention, even if the miniaturization of the device progresses and the contact area between the source / drain electrode and the source / drain diffusion layer becomes smaller, the increase in contact resistance is prevented. A semiconductor device that can be obtained can be obtained.

【発明の効果】以上詳述したように本発明によれば、素子の微細化が進み、ソース・ドレイン電極とソース・ドレイン拡散層との接触面積が小さくなっても、コンタクト抵抗の増大を防止し得る半導体装置を得ることができる。

[0058]

Brief description of the drawings

図面の簡単な説明

[0059]
1 is a cross-sectional view of a manufacturing step of the MOS transistor according to the first embodiment of the present invention.

図１本発明の第１の実施例に係わるＭＯＳトランジスタの製造工程断面図。

[0060]
FIG. 2 is a cross-sectional view of a manufacturing step of the MOS transistor according to the first embodiment of the present invention.

図２本発明の第１の実施例に係わるＭＯＳトランジスタの製造工程断面図。

[0061]
3 is an energy band diagram of the contact hole portion of the MOS transistor of FIG.

図３図２のＭＯＳトランジスタのコンタクトホール部のエネルギーバンド図。

[0062]
4 is an energy band diagram of the contact hole portion of the conventional MOS transistor.

図４従来法のＭＯＳトランジスタのコンタクトホール部のエネルギーバンド図。

[0063]
5 is an energy band diagram of the contact hole portion of the MOS transistor of FIG.

図５図６のＭＯＳトランジスタのコンタクトホール部のエネルギーバンド図。

[0064]
6 is a cross-sectional view of a MOS transistor according to a second embodiment of the present invention.

図６本発明の第２の実施例に係わるＭＯＳトランジスタの断面図。

[0065]

7 is a cross-sectional view of the MOS transistor in which the contact hole is filled with the Si—Ge mixed crystal layer.

図７コンタクトホールがＳｉ－Ｇｅ混晶層で埋められたＭＯＳトランジスタの断面図。

[0066]

8 is a cross-sectional view of a manufacturing step of the MOS transistor according to the third embodiment of the present invention. FIG.

図８本発明の第３の実施例に係わるＭＯＳトランジスタの製造工程断面図。

[0067]

9 is a cross-sectional view of a MOS transistor according to a fourth embodiment of the present invention.

図９本発明の第４の実施例に係わるＭＯＳトランジスタの断面図。

[0068]

10 is a cross-sectional view of a MOS transistor according to a fifth embodiment of the present invention.

図１０本発明の第５の実施例に係わるＭＯＳトランジスタの断面図。

[0069]

11 is a cross-sectional view of a MOS transistor in the case of forming a Si-Ge mixed crystal layer using a selective CVD method.

図１１選択ＣＶＤ法を用いてＳｉ－Ｇｅ混晶層を形成した場合のＭＯＳトランジスタの断面図。

[0070]

FIG. 12 is a cross-sectional view of a manufacturing step of the MOS transistor according to the sixth embodiment of the present invention.

図１２本発明の第６の実施例に係わるＭＯＳトランジスタの製造工程断面図。

[0071]
13 is a cross-sectional view of a MOS transistor according to a seventh embodiment of the present invention.

図１３本発明の第７の実施例に係わるＭＯＳトランジスタの断面図。

[0072]
14 is a cross-sectional view of a conventional MOS transistor.

図１４従来のＭＯＳトランジスタの断面図。

[0073]
Explanation of sign

符号の説明

[0074]
1, 11, 21, 31, 41, 51 ... Si substrate 2, 12, 22, 32, 42, 52 ... Oxide film for element separation 3, 13, 23, 33, 43, 53 ... Gate oxide film 4, 14, 24, 34, 44, 45 ... gate electrodes 5, 15, 25, 35, 45, 55 ... sidewall gate insulating films 6, 16, 26, 36, 46, 56 ... source / drain diffusion layers 7, 17, 27, 37 , 47, 57 ... SiO 2 films 8, 18, 28, 38, 48, 58 ... Si-Ge mixed crystal layers 9, 19, 29, 39, 49, 59 ... source / drain electrodes 40, 60 ... titanium silicide (TiSi2) 50 ... Si layer

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１，１１，２１，３１，４１，５１…Ｓｉ基板２，１２，２２，３２，４２，５２…素子分離用酸化膜３，１３，２３，３３，４３，５３…ゲート酸化膜
４，１４，２４，３４，４４，５４…ゲート電極５，１５，２５，３５，４５，５５…側壁ゲート絶縁膜６，１６，２６，３６，４６，５６…ソース・ドレイン拡散層
７，１７，２７，３７，４７，５７…ＳｉＯ2膜
８，１８，２８，３８，４８，５８…Ｓｉ－Ｇｅ混晶層９，１９，２９，３９，４９，５９…ソース・ドレイン電極４０，６０…チタンシリサイド（ＴｉＳｉ2）５０…Ｓｉ層

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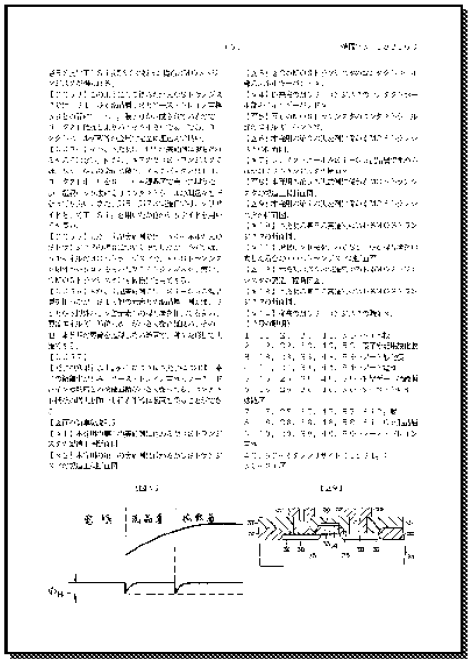
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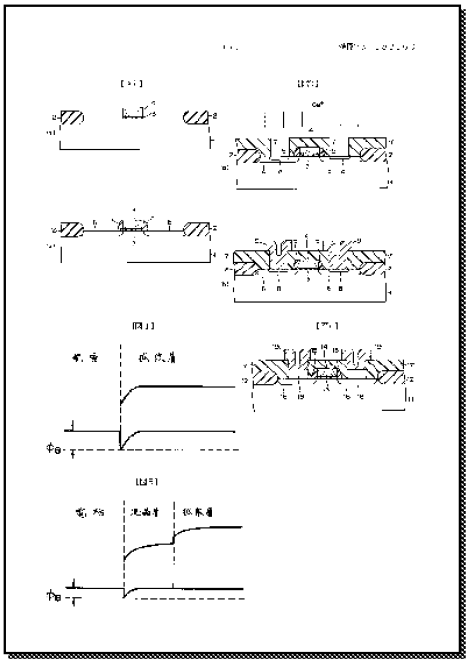
1.
A source / drain diffusion layer formed on the surface of a silicon substrate, a source / drain electrode formed on the source / drain diffusion layer, and a portion between the source / drain electrode and the source / drain diffusion layer A mixed crystal layer made of silicon and a predetermined element, and as the predetermined element, the energy level at the valence band edge of the mixed crystal layer and the Fermi level of the source / drain electrode A semiconductor device characterized in that an element whose difference is smaller than a difference between an energy level of a valence band edge of the source / drain diffusion layer and a Fermi level of the source / drain electrode is selected.

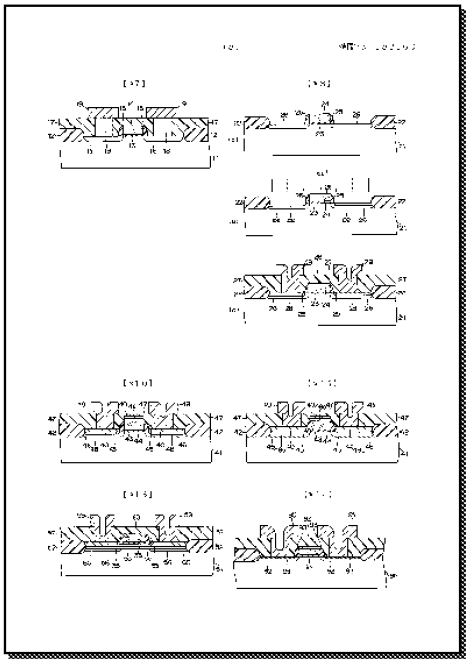
シリコン基板の表面に形成されたソース・ドレイン拡散層と、このソース・ドレイン拡散層上に形成されたソース・ドレイン電極と、このソース・ドレイン電極と前記ソース・ドレイン拡散層との間に設けられたシリコンと所定の元素とからなる混晶層とを具備してなり、前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする半導体装置。

2.
Forming a source / drain diffusion layer on the surface of a silicon substrate; forming a mixed crystal layer consisting of silicon and a predetermined element on the source / drain diffusion layer using a CVD method; and the mixed crystal layer And forming a source / drain electrode thereon, wherein, as the predetermined element, the difference between the energy level at the valence band edge of the mixed crystal layer and the Fermi level of the source / drain electrode is A method of manufacturing a semiconductor device, comprising selecting an element smaller than the difference between the energy level at the valence band edge of the source / drain diffusion layer and the Fermi level of the source / drain electrode.

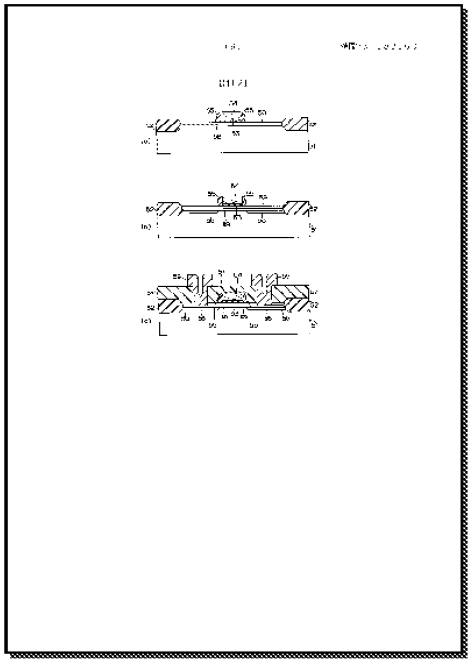
シリコン基板の表面にソース・ドレイン拡散層を形成する工程と、ＣＶＤ法を用いて前記ソース・ドレイン拡散層上にシリコンと所定の元素とからなる混晶層を形成する工程と、この混晶層上にソース・ドレイン電極を形成する工程とを具備してなり、前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする半導体装置の製造方法。







Drawing pages of JPH05183160 A



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(71)出願人　000003078
株式会社東芝
神奈川県川崎市幸区堀川町72番地

(72)発明者　西山　彰
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝総合研究所内

(72)発明者　牛久　幸広
神奈川県川崎市幸区小向東芝町１番地　株式会社東芝総合研究所内

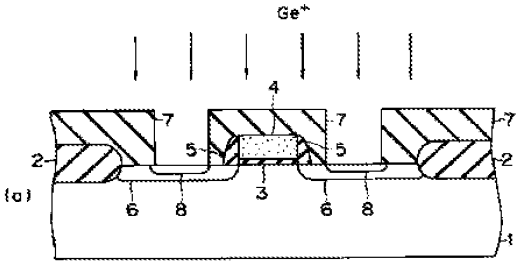
(74)代理人　弁理士　鈴江　武彦

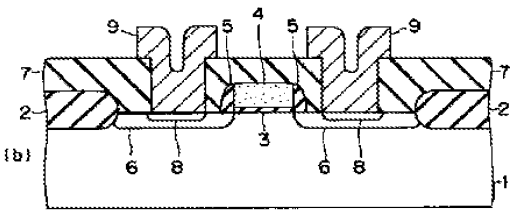
(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】

【目的】本発明は、素子の微細化が進んでも、コンタクト抵抗の増大を招かない半導体装置を提供することを目的とする。

【構成】シリコン基板１上に、ゲート酸化膜３を介して形成されたゲート電極４と、このゲート電極４に対向してシリコン基板１の表面に形成されたソース・ドレイン拡散層６と、このソース・ドレイン拡散層６上に形成されたソース・ドレイン電極９と、このソース・ドレイン電極９とソース・ドレイン拡散層６との間に設けられたＳｉ－Ｇｅ混晶層８とを備えていることを特徴とする。





【特許請求の範囲】
【請求項１】シリコン基板の表面に形成されたソース・ドレイン拡散層と、
このソース・ドレイン拡散層上に形成されたソース・ドレイン電極と、
このソース・ドレイン電極と前記ソース・ドレイン拡散層との間に設けられたシリコンと所定の元素とからなる混晶層とを具備してなり、
前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする半導体装置。
【請求項２】シリコン基板の表面にソース・ドレイン拡散層を形成する工程と、
ＣＶＤ法を用いて前記ソース・ドレイン拡散層上にシリコンと所定の元素とからなる混晶層を形成する工程と、この混晶層上にソース・ドレイン電極を形成する工程とを具備してなり、
前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は、コンタクト抵抗の低減化を図り得る半導体装置及びその製造方法に関する。
【０００２】
【従来の技術】近年、コンピューターや通信機器の重要部分には、多数のトランジスタや抵抗等を電気回路を達成するようにむすびつけ、１チップ上に集積化して形成した大規模集積回路（ＬＳＩ）が多用されている。このため、機器全体の性能は、ＬＳＩ単体の性能と大きく結び付いている。
【０００３】ＬＳＩ単体の性能向上は、集積度を高めること、つまり、素子の微細化により実現できる。素子の微細化が進と、配線材と各素子とを結ぶコンタクトホールの径が小さくなり、配線材と素子との接触面積が小さくなる。この結果、コンタクトホールにおける抵抗、いわゆる、コンタクト抵抗は、素子の微細化とともに増大する。このため、コンタクト抵抗が寄生抵抗として働き、素子に供給される電流が少なくなり、動作遅延が生じる。
【０００４】そこで、電界トランジスタ（ＦＥＴ）においては、図１４に示すように、ソース・ドレイン拡散層９２の表面にシリサイド９３を形成する方法が検討されている。この方法は、ソース・ドレイン拡散層９２を形成した後に、ポリシリコンゲート電極９１の側壁に絶縁膜９３を形成し、続いて、シリコン基板９０の全面に、チタン等からなる金属膜を堆積し、この金属膜に熱処理を施してポリシリコンゲート電極９１、ドレイン・ソース拡散層９２をシリサイド化し、この後、未反応の金属膜をエッチング除去するというものである。
【０００５】このような方法を用いることで、コンタクトホールの径が小さくなっても、ソース・ドレイン拡散層９２とソース・ドレイン電極９５との実効的な接触面積を、ソース・ドレイン拡散層９２の面積と同じにでき、コンタクト抵抗の増大を防止できる。
【０００６】しかしながら、今後さらに微細化が進んでいくと、ソース・ドレイン拡散層９２の面積が１．０μm^2程度まで小さくなると予想され、この結果、接触面積がソース・ドレイン９２の面積と同じであっても、コンタクト抵抗の値は高いものとなり、動作遅延等の問題が生じる。特に、p^+拡散層とシリサイドとの間のコンタクト抵抗は、n^+拡散層とシリサイドとの間のそれに比べ高く、この部分を低抵抗化する必要がある。
【０００７】
【発明が解決しようとする課題】上述の如く、今後さらに素子の微細化が進むと、シリサイドを用いたＦＥＴであっても、ソース・ドレイン拡散層の面積が非常に小さくなるので、ソース・ドレイン電極とソース・ドレイン拡散層との接触面積が小さくなり、これにより、コンタクト抵抗が増大し、動作遅延等の問題が生じるという問題があった。
【０００８】本発明は、上記事情を考慮してなされたもので、その目的とするところは、今後さらに素子の微細化が進んでも、コンタクト抵抗の増大を招かない半導体装置及びその製造方法を提供することにある。
【０００９】
【課題を解決するための手段】上記の目的を達成するために、本発明の半導体装置は、シリコン基板に形成されたソース・ドレイン拡散層とソース・ドレイン電極との間に、シリコンと所定の元素とからなる混晶層が設けられ、前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を選んだことを特徴とする。
【００１０】また、本発明の半導体装置の製造方法は、シリコン基板にソース・ドレイン拡散層を形成した後、ＣＶＤ法を用いてシリコンと所定の元素とからなる混晶層を前記ソース・ドレイン拡散層上に形成する工程を有し、前記所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェ

ルミ準位との差より小さくなる元素を選んだことを特徴とする。また、ＣＶＤ法を用いる代わりに、ソース・ドレイン拡散層に上述した条件を満たす所定の元素のイオンを打込むことで、混晶層を形成しても良い。

【００１１】

【作用】ソース・ドレイン電極とソース・ドレイン拡散層とのコンタクト抵抗は、ソース・ドレイン電極のフェルミ準位とソース・ドレイン拡散層の価電子帯のエネルギー準位との差が小さいほど小さくなる。

【００１２】本発明の半導体装置では、ソース・ドレイン電極をシリコンと所定の元素からなる混晶層を介してソース・ドレイン拡散層と接続し、所定の元素として、前記混晶層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差が、前記ソース・ドレイン拡散層の価電子帯端のエネルギー準位と前記ソース・ドレイン電極のフェルミ準位との差より小さくなる元素を用いている。

【００１３】即ち、混晶層を介してソース・ドレイン拡散層とソース・ドレイン電極とを接続することで、ソース・ドレイン電極のフェルミ準位とソース・ドレイン拡散層の価電子帯のエネルギー準位との差を実効的に小さくしている。

【００１４】したがって、素子の微細化により、ソース・ドレイン電極とソース・ドレイン拡散層との接触面積が小さくなっても、これによるコンタクト抵抗の増大は、上記混晶層によるコンタクト抵抗の減少により防止できる。

【００１５】また、半導体装置の製造方法では、ＣＶＤ法を用いてソース・ドレイン拡散層上に混晶層を形成している。したがって、シリコン基板にダメージを与えること無く混晶層を形成できる。

【００１６】

【実施例】以下、図面を参照しながら実施例を説明する。図１，図２は、本発明の第１の実施例に係わるＭＯＳトランジスタの製造工程断面図である。

【００１７】まず、図１（ａ）に示す如く、ｎ型のＳｉ基板１上に、素子分離用酸化膜２を形成する。次いでこの酸化膜２で囲まれた素子形成領域に、熱酸化法を用いて厚さ８ｎｍのゲート酸化膜３を形成し、続いて、全面に厚さ３００ｎｍのゲート電極４となる多結晶シリコン膜を堆積する。そして、フォトリソグラフィ技術を用いて上記多結晶シリコン膜をパターニングしてゲート電極４を形成する。

【００１８】次に図１（ｂ）に示す如く、全面に側壁ゲート絶縁膜５となるSiO_2膜を堆積した後、このSiO_2膜の全面をエッチバックして、ゲート電極４の側壁に側壁ゲート絶縁膜５を形成する。次いで加速電圧４０ｋｅＶ，ドーズ量$5\times10^{15}cm^{-2}$の条件でBF_2を注入し、続いて、窒素雰囲気中で８５０℃，３０分の熱処理を行なってp^+型のソース・ドレイン拡散層６を形成する。

【００１９】次に図２（ａ）に示す如く、ＣＶＤ法を用いて、全面に厚さ８００ｎｍのSiO_2膜７を堆積した後、ソース・ドレイン拡散層６と後工程で形成するソース・ドレイン電極９とのコンタクトを取るためのコンタクトホールを形成する。次いで加速電圧２０ｋｅＶ，ドーズ量$3\times10^{15}cm^{-2}$の条件でGe^+のイオン注入を行なう。この後、Ａｒ雰囲気中で６００℃，１時間の熱処理を行ない、コンタクトホール低部のＳｉ基板１に注入されたＧｅとＳｉとを結合させる。このようなイオン注入工程，熱処理工程により、コンタクトホール低部のＳｉ基板１の表面で、$Si_{0.8}Ge_{0.2}$となるＳｉ－Ｇｅ混晶層８を形成できる。

【００２０】次に図２（ｂ）に示す如く、Ｓｉ－Ｇｅ混晶層８及びその下のソース・ドレイン拡散層６の不純物活性化率を十分に高くするために、Ａｒ雰囲気中で１０００℃，１０秒の熱処理を行なう。次いで、電極材料として厚さ８００ｎｍのＡｌ合金膜を全面に堆積する。最後に、このＡｌ合金膜をパターニングしてソース・ドレイン電極９を形成してＭＯＳトランジスタが完成する。

【００２１】図３は、上記方法で得られたＭＯＳトランジスタのコンタクトホールにおけるソース・ドレイン拡散層６，Ｓｉ－Ｇｅ混晶層８，ソース・ドレイン電極９のエネルギーバンド図であり、図４は、従来方法で得られたＭＯＳトランジスタ、つまり、ソース・ドレイン拡散層とソース・ドレイン電極との間にＳｉ－Ｇｅ混晶層が設けられてないＭＯＳトランジスタのそれである。なお、図中、ϕ_Bは、ソース・ドレイン電極のフェルミ準位と、このソース・ドレイン電極と接触した混晶層又はソース・ドレイン拡散層の価電子帯端のエネルギー準位とのエネルギー準位差である。

【００２２】これらの図から、本実施例のＭＯＳトランジスタのエネルギー準位差ϕ_Bの方が、従来のそれより小さいことが分かる。これは、本実施例のＭＯＳトランジスタでは、Ｓｉ－Ｇｅ混晶層８の影響により、価電子帯の最小準位のエネルギレベルが高準位側にシフトしたからである。なお、上述したように、Ｓｉ－Ｇｅ混晶層８とソース・ドレイン電極９との界面における、Ｓｉ－Ｇｅ混晶層８のＳｉとＧｅとの比は４：１である。一方、不純物濃度が高い半導体と金属とのコンタクト抵抗R_cは、エネルギー準位差ϕ_Bを用いて次式のように表わせられる。

$R_c=\alpha\exp(A\phi_B/N_d^{1/2})$

ここで、αは比例係数，N_dはホールの界面濃度，Ａは定数である。上式から、エネルギー準位差ϕ_Bが小さいほど、コンタクト抵抗R_cが小さくなることが分かる。

【００２３】したがって、本実施例のＭＯＳトランジスタの方が、従来のそれより、コンタクト抵抗を小さくできるので、微細化により、ソース・ドレイン拡散層の面積が小さくなっても、コンタクト抵抗の増大による動作

遅延は生じない。

【0024】また、本実施例では、イオン注入法を用いてSi－Ge混晶層8を形成するので、基板表面に近いほどGe濃度が高くなり、この結果、Si－Ge混晶層8及びソース・ドレイン電極の伝導帯のエネルギー準位は、図3に示したように滑らかに変化する。

【0025】かくして本実施例によれば、エネルギー準位差ϕ_Bを小さくできるので、コンタクト抵抗の増大を防止でき、もって、微細化を行なっても動作遅延の起きないMOSトランジスタを得ることができる。なお、本実施例では、コンタクトホールを完全に塞いでいないが、W等の金属で完全に塞いでも良い。

【0026】図6は、本発明の第2の実施例に係わるMOSトランジスタの断面図である。本実施例のMOSトランジスタが先の実施例のそれと異なる点は、CVD法を用いてSi－Ge混晶層を形成したことにある。

【0027】即ち、先の実施例と同様な方法で、素子分離用酸化膜12で囲まれたシリコン基板11の素子形成領域に、ゲート酸化膜13，ゲート電極14，側壁ゲート絶縁膜15を形成した後、加速電圧40keV，ドーズ量$5\times10^{15}cm^{-2}$の条件でBF_2のイオン注入を行なってp型のソース・ドレイン拡散層16を形成する。次に全面にSiO_2膜17を堆積した後、このSiO_2膜17にコンタクトホールを開口する。

【0028】次にSiH_4とGeH_4とH_2との混合ガスを使用した選択CVD法により、コンタクトホール内にSi－Ge混晶層18を所定の高さまで埋める。具体的には、最初、混合ガスの全圧力を27Pa（SiH_4分圧：6．5Pa），基板温度を550℃に設定してSi－Ge混晶層18を形成する。そして、徐々にGeH_4分圧を高くし、最終的には1．3Paとする。この間、SiH_4分圧，全圧力が、それぞれ6．5Pa，27Paと一定になるように、H_2分圧を減少させる。このような条件でCVD法によりSi－Ge混晶層18を形成した後、例えば、Bの200keV，$1\times10^{15}cm^{-2}$と30keV，$3\times10^{15}cm^{-2}$のイオン注入を行ない、続いて、この不純物にArを用いた1000℃，約10秒の活性化アニールを施す。最後に、Al合金からなるソース・ドレイン電極19を形成してMOSトランジスタが完成する。

【0029】なお、SiH_4分圧に対するGeH_4分圧を常に一定にすれば、SiとGeとの比が4：1と一定のSi－Ge混晶層を形成でき、この場合、図5に示すようなバンド構造、つまり、Si－Ge混晶層18とSi基板1との境界で伝導バンドが不連続なバンド構造が得られる。

【0030】以上述べた方法で得られたMOSトランジスタでも、ソース・ドレイン電極19がSi－Ge混晶層18を介してソース・ドレイン拡散層16に接続しているので、伝導帯端，価電子帯端の不連続，連続に関わらず、エネルギー準位差ϕ_Bが小さくなり、コンタクト抵抗が小さくなる。したがって、素子の微細化を行なっても、動作速度を速く保つことができる。また、CVD法を用いてSi－Ge混晶層18を形成しているので、イオン注入の場合のようにSi基板11にダメージが与える恐れはない。

【0031】なお、本実施例では、コンタクトホールをSi－Ge混晶層18で完全に埋めなかったが、図7に示すように、コンタクトホールをSi－Ge混晶層18で完全に埋めても同様な効果が得られる。

【0032】また、選択CVD法により、コンタクトホール内にSi－Ge混晶層18を所定の高さまで堆積する代わりに、全面にSi－Geに堆積した後、全面エッチバックを行なうことでコンタクトホール内にSi－Ge混晶層18を形成しても良い。図8は、本発明の第3の実施例に係わるMOSトランジスタの製造工程断面図である。

【0033】先ず、第1の実施例と同様な方法を用いて、図8（a）に示す如く、素子分離用酸化膜22で囲まれたシリコン基板21の素子形成領域に、ゲート酸化膜23，ゲート電極24，側壁ゲート絶縁膜25，p型のソース・ドレイン拡散層26を形成する。

【0034】次に図8（b）に示す如く、Ge^+イオンを加速電圧20keV，ドーズ量$3\times10^{16}cm^{-2}$の条件で打込み、ゲート電極24，ソース・ドレイン拡散層26の表面にGeを導入する。次いでAr雰囲気中で、600℃，1時間の熱処理を用いてGeとSiとを結合させ、Si－Ge混晶層28を形成する。この後、Si－Ge混晶層28及びその下のソース・ドレイン拡散層26並びにゲート電極24中の不純物の活性化率を上げるために、1000℃，10秒の熱処理をAr雰囲気中で行なう。

【0035】次に図8（c）に示す如く、CVD法を用いて、全面に厚さ800nmのSiO_2膜27を堆積した後、このSiO_2膜27にコンタクトホールを開口する。最後に、全面に厚さ800nmのAl合金膜を堆積した後、これをパターニングしてソース・ドレイン電極29を形成してMOSトランジスタが完成する。

【0036】以上述べた方法でも、Si－Ge混晶層28を介してソース・ドレイン電極29とソース・ドレイン拡散層26とが接続しているので、エネルギー準位差ϕ_Bが小さくなり、この結果、微細化を行なっても、コンタクト抵抗による寄生抵抗を低く保つことができるので動作遅延は生じない。なお、本実施例では、コンタクトホールが完全に塞がれていないが、W等の金属を充填して完全に塞がれた構造としても良い。

【0037】図9は、本発明の第4の実施例に係わるMOSトランジスタの断面図である。本実施例のMOSトランジスタが第3の実施例のそれと異なる点は、CVD法用いてSi－Ge混晶層を形成したことにある。

【００３８】即ち、素子分離用酸化膜３２で囲まれたシリコン基板３１の素子形成領域に、ゲート酸化膜３３，ゲート電極３４，側壁ゲート絶縁膜３５，p型のソース・ドレイン拡散層３６を形成した後、選択ＣＶＤ法を用いてソース・ドレイン拡散層３６上にＳｉ－Ｇｅ混晶層３８を例えば５０ｎｍの厚さに選択的に形成する。この後、先の実施例と同様なSiO_2膜３７の堆積工程、コンタクトホールの開口工程、ソース・ドレイン電極３９の形成工程を経てＭＯＳトランジスタが完成する。なお、ソース・ドレイン拡散層３６上のＳｉ－Ｇｅ混晶層３８への不純物導入は、例えば、加速電圧４０ｋｅＶ，ドーズ量$1\times10^{15}cm^{-2}$程度の条件でＢのイオン注入を行なった後、１０００℃，１０秒の活性化アニールを行なえば良い。

【００３９】このような方法で得られたＭＯＳトランジスタでも先の実施例と同様な効果が得られる。なお、本実施例の場合も、Ｗ等の金属でコンタクトホールを塞いでも良い。図１０は、本発明の第５の実施例に係わるＭＯＳトランジスタの断面図である。

【００４０】これを製造工程に従い説明すると、まず、素子分離用酸化膜４２で区分されたシリコン基板４１の素子形成領域に、ゲート酸化膜４３，ゲート電極４４，側壁ゲート絶縁膜４５を形成する。

【００４１】次にＢのイオン注入を行なってｐ型のソース・ドレイン拡散層４６を形成し、引き続き、Ｇｅのイオン注入を行なってＳｉ－Ｇｅ混晶層４８を形成する。この後、ソース・ドレイン拡散層４６のＢの活性化のために、第３の実施例と同様に１０００℃，１０秒の熱処理をＡｒ雰囲気中で行なう。

【００４２】次にSiH_4とＴｉＣｌ４との混合ガスを使用し、基板温度を７５０℃に設定した選択ＣＶＤ法により、ソース・ドレイン拡散層４６上にチタンシリサイド（$TiSi_2$）４０を選択的に形成する。

【００４３】次にＣＶＤ法を用いてSiO_2膜４７を全面に堆積した後、このSiO_2膜４７にコンタクトホールを開口する。最後に、Ａｌ合金膜を全面に堆積し、これをパターニングしてソース・ドレイン電極４９を形成してＭＯＳトランジスタが完成する。

【００４４】以上述べた方法によれば、Ｓｉ－Ｇｅ混晶層４８とソース・ドレイン電極４９との間に$TiSi_2$膜４０を設けたので、コンタクト抵抗をよりいっそう小さくできる。

【００４５】なお、本実施例では、Ｇｅのイオン注入法を用いてＳｉ－Ｇｅ混晶層４８を形成したが、図１１に示すように、選択ＣＶＤ法を用いてＳｉ－Ｇｅ混晶層４８ａを形成しても良い。また、Ｗなどの金属でコンタクトホールを完全に塞いでも良い。図１２は、本発明の第６の実施例に係わるＭＯＳトランジスタの製造工程断面図である。

【００４６】まず、図１２（ａ）に示す如く、ｎ型のＳｉ基板５１上に素子分離用SiO_2膜５２を形成する。次いでＧｅイオンを加速電圧１００ｋｅＶ，ドーズ量$3\times10^{15}cm^{-2}$の条件でＳｉ基板５１に打込み、続いて、Ａｒ雰囲気中で６００℃，１時間のアニールを行なう。この結果、基板表面付近にＳｉ－Ｇｅ混晶層５８が形成され、その上にＳｉ層５０が形成される。次いでこのＳｉ層５０を熱酸化して厚さ８ｎｍのゲート酸化膜５３を形成した後、全面にゲート電極５６となる多結晶シリコン膜を堆積し、続いて、これをフォトリソグラフィを用いてパターニングしてゲート電極５６を形成する。この後、SiO_2膜を全面に堆積し、これにエッチバックを施して側壁ゲート絶縁膜５５を形成する。

【００４７】次に図１２（ｂ）に示す如く、BF_2イオンを加速電圧４０ｋｅＶ，ドーズ量$5\times10^{15}cm^{-2}$の条件で打ち込んだ後、窒素雰囲気中で８５０℃，３０分のアニールを行ない、ｐ型のソース・ドレイン拡散層５６を形成する。

【００４８】次に図１２（ｃ）に示す如く、ＣＶＤ法を用いて、全面に厚さ８００ｎｍのSiO_2膜５７を堆積した後、SiO_2膜５７，その下のＳｉ層５０に順次エッチングを施し、Ｓｉ－Ｇｅ混晶層５８が露出するようにコンタクトホールを形成する。最後に、全面にＡｌ合金膜を堆積し、これをパターニングしてソース・ドレイン電極５９を形成してＭＯＳトランジスタが完成する。

【００４９】以上述べた方法でも、先に説明したＭＯＳトランジスタと同様にＳｉ－Ｇｅ混晶層５８によりエネルギー準位差ϕ_Eが小さくなるので、コンタクト抵抗の低減が図れる。

【００５０】なお、イオン注入の代わりに選択ＣＶＤ法を用いてもＳｉ－Ｇｅ混晶層５８を形成できる。即ち、素子分離用SiO_2膜５２を形成した後、選択ＣＶＤ法を用いて、素子形成領域のＳｉ基板５１の表面に、Ｓｉ－Ｇｅ混晶層５８を堆積し、この後、再び選択ＣＶＤ法を用いて、Ｓｉ－Ｇｅ混晶層５８上にＳｉ層５０を堆積すれば良い。また、コンタクトホールをＷ等の金属で埋込んでも良い。

【００５１】図１３は、本発明の第７の実施例に係わるＭＯＳトランジスタの断面図である。なお、図１２のＭＯＳトランジスタと対応する部分には図１２と同一符号を付してあり、詳細な説明は省略する。本実施例のＭＯＳトランジスタが第６の実施例のそれと異なる点は、Ｓｉ－Ｇｅ混晶層５８上にシリサイドを形成したことにある。

【００５２】即ち、ソース・ドレイン拡散層５６を形成した後、全面にＴｉ膜を堆積し、続いて、窒素雰囲気中で７００℃，３０秒間のアニールを行なう。この結果、Ｔｉ膜と接触していたＳｉ層５０は全て$TiSi_2$膜６０に変わる。この後、未反応のＴｉ膜や、ＴｉＮ膜を除去する。この後の工程は先の実施例と同様である。以上の工程により、ゲート電極５４，ソース・ドレイン拡散

層５６上に$TiSi_2$膜６０に残った構造のＭＯＳトランジスタが得られる。

【００５３】このようにして得られたＭＯＳトランジスタでは、Ｓｉ－Ｇｅ混晶層５８とソース・ドレイン電極５９との間に$TiSi_2$膜５０が形成されているので、コンタクト抵抗をよりいっそう小さくなる。なお、コンタクトホールがW等の金属で完全に埋込んで良い。

【００５４】なお、本発明は上述した実施例に限定されるものではない。例えば、図７のＭＯＳトランジスタでは、Ｓｉ－Ｇｅの全面堆積と、エッチバックとにより、コンタクトホールをＳｉ－Ｇｅ混晶層で完全に埋めたが、選択ＣＶＤ法によりコンタクトホールの埋込みを行なっても良い。また、第５，第７の実施例では，シリサイドとして$TiSi_2$を用いたが他のシリサイドを用いても良い。

【００５５】また、上記実施例では、ｐチャネルのＭＯＳトランジスタの場合について説明したが、本発明は、ｎチャネルのＭＯＳトランジスタや，ＭＯＳトランジスタ以外のシリコンを用いたＭＩＳトランジスタ、更に、ＣＭＯＳトランジスタにも同様に適用できる。

【００５６】また、上記実施例では、Ｓｉ－Ｇｅの混晶層を用いたが、Ｓｉと他の元素との混晶層、例えば、ＳｉとＧｅ以外のＩＶ族元素との混晶層を用いても良い。要はエネルギー準位差ϕ_Bが小さくなれば良い。その他、本発明の要旨を逸脱しない範囲で、種々変形して実施できる。

【００５７】

【発明の効果】以上詳述したように本発明によれば、素子の微細化が進み、ソース・ドレイン電極とソース・ドレイン拡散層との接触面積が小さくなっても、コンタクト抵抗の増大を防止し得る半導体装置を得ることができる。

【図面の簡単な説明】

【図１】本発明の第１の実施例に係わるＭＯＳトランジスタの製造工程断面図。

【図２】本発明の第１の実施例に係わるＭＯＳトランジスタの製造工程断面図。

【図３】図２のＭＯＳトランジスタのコンタクトホール部のエネルギーバンド図。

【図４】従来法のＭＯＳトランジスタのコンタクトホール部のエネルギーバンド図。

【図５】図６のＭＯＳトランジスタのコンタクトホール部のエネルギーバンド図。

【図６】本発明の第２の実施例に係わるＭＯＳトランジスタの断面図。

【図７】コンタクトホールがＳｉ－Ｇｅ混晶層で埋められたＭＯＳトランジスタの断面図。

【図８】本発明の第３の実施例に係わるＭＯＳトランジスタの製造工程断面図。

【図９】本発明の第４の実施例に係わるＭＯＳトランジスタの断面図。

【図１０】本発明の第５の実施例に係わるＭＯＳトランジスタの断面図。

【図１１】選択ＣＶＤ法を用いてＳｉ－Ｇｅ混晶層を形成した場合のＭＯＳトランジスタの断面図。

【図１２】本発明の第６の実施例に係わるＭＯＳトランジスタの製造工程断面図。

【図１３】本発明の第７の実施例に係わるＭＯＳトランジスタの断面図。

【図１４】従来のＭＯＳトランジスタの断面図。

【符号の説明】

１，１１，２１，３１，４１，５１…Ｓｉ基板

２，１２，２２，３２，４２，５２…素子分離用酸化膜

３，１３，２３，３３，４３，５３…ゲート酸化膜

４，１４，２４，３４，４４，５４…ゲート電極

５，１５，２５，３５，４５，５５…側壁ゲート絶縁膜

６，１６，２６，３６，４６，５６…ソース・ドレイン拡散層

７，１７，２７，３７，４７，５７…SiO_2膜

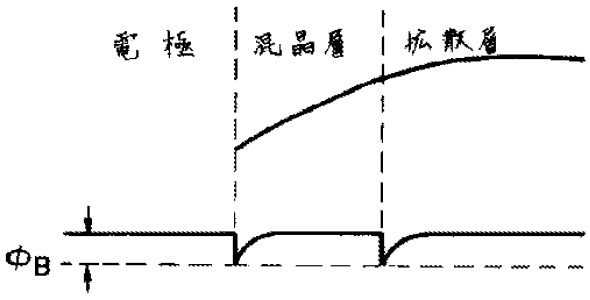
８，１８，２８，３８，４８，５８…Ｓｉ－Ｇｅ混晶層

９，１９，２９，３９，４９，５９…ソース・ドレイン電極

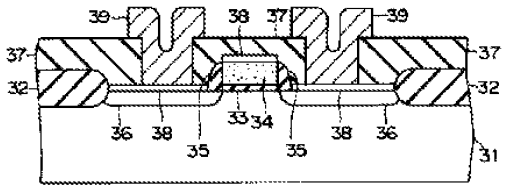
４０，６０…チタンシリサイド（$TiSi_2$）

５０…Ｓｉ層

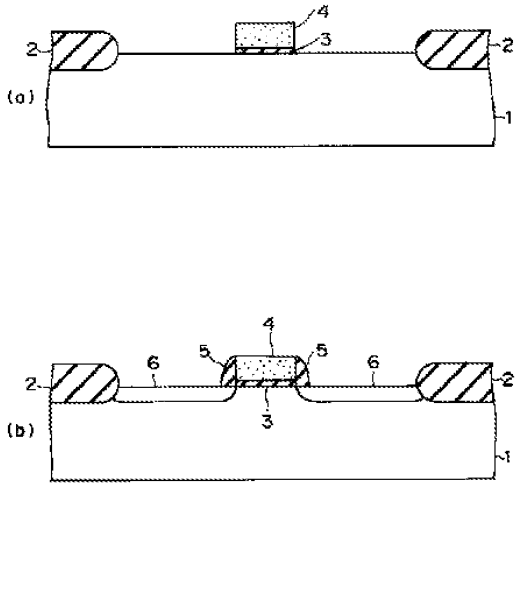
【図３】



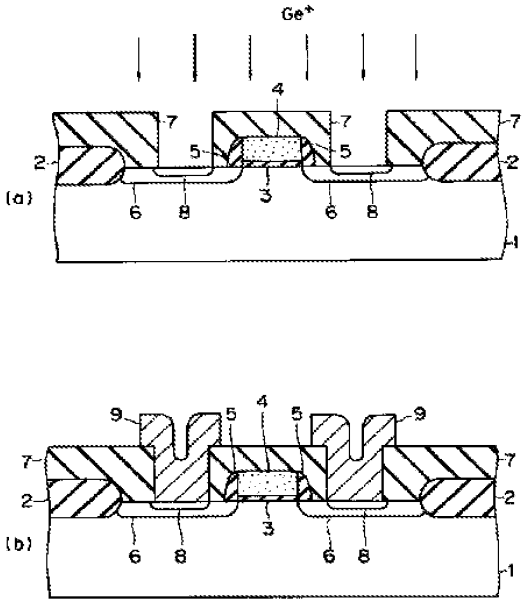
【図９】



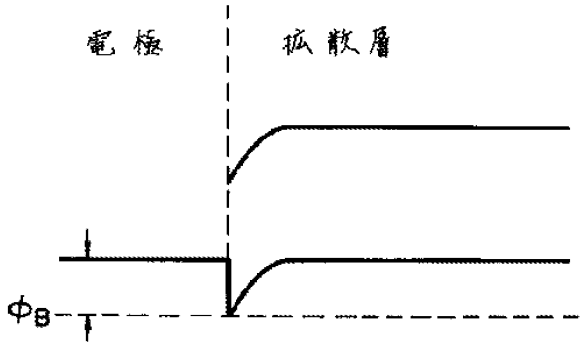
【図1】


(a)
(b)
1
2
3
4
5
6

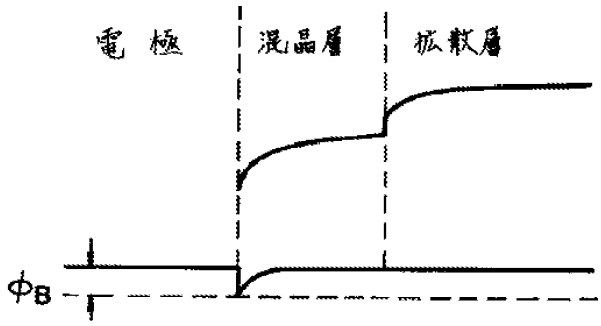
【図2】


Ge+
(a)
(b)
1
2
3
4
5
6
7
8
9

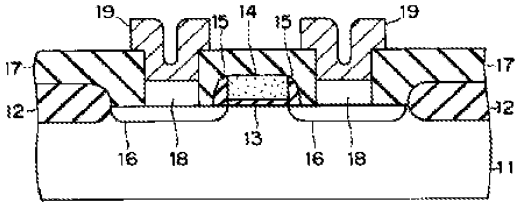
【図4】


電極
拡散層
ΦB

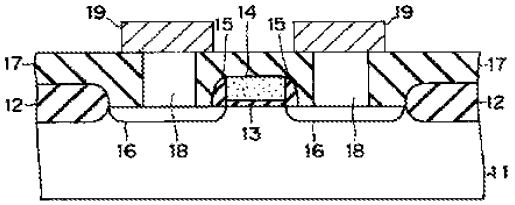
【図5】


電極
混晶層
拡散層
ΦB

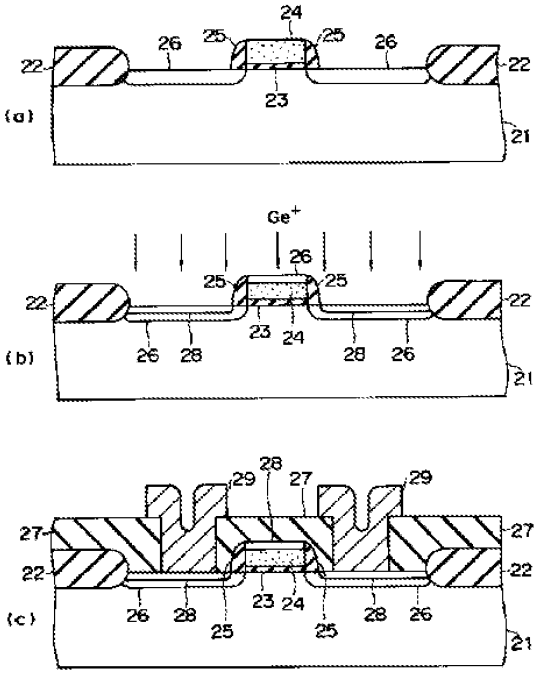
【図6】


11
12
13
14
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17
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19

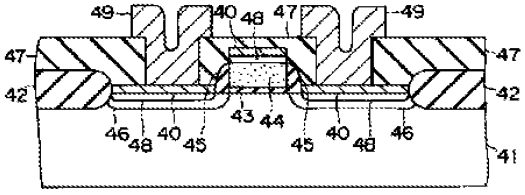
【図7】



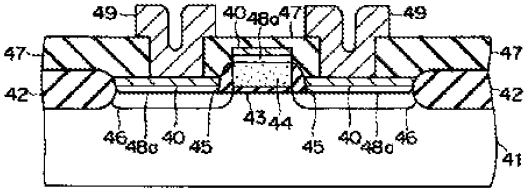
【図8】



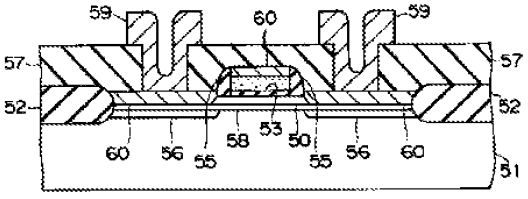
【図10】



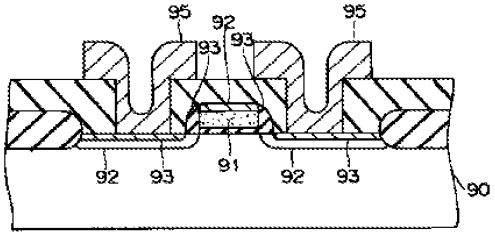
【図11】



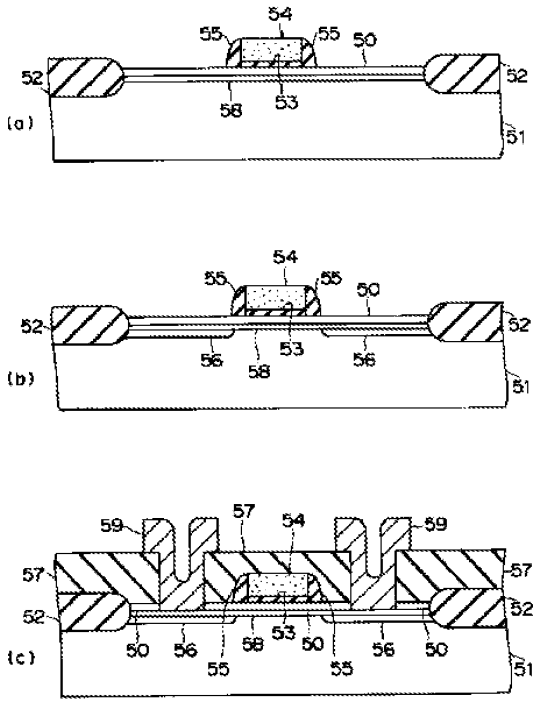
【図13】



【図14】



【図12】



Espacenet

Bibliographic data: JPH07169958 (A) — 1995-07-04

SEMICONDUCTOR DEVICE AND ITS MANUFACTURE

Inventor(s): ANDO TAKESHI ± (ANDO TAKESHI)

Applicant(s): NEC CORP ± (NEC CORP)

Classification: **- international:** ***H01L29/78;*** (IPC1-7): H01L29/78
- cooperative:

Application number: JP19930317009 19931216

Priority number(s): JP19930317009 19931216

Abstract of JPH07169958 (A)

PURPOSE:To enable a shallow junction of a source and a drain region having low diffusion layer resistance and low contact resistance to be increased in controllability. CONSTITUTION:Germanium layers or silicon-germanium layers are selectively formed on the surface of a P-type silicon substrate sandwiching a gate electrode 3 between them through a selective chemical vapor growth method, and then N-type impurity ions are implanted to form a source region 10 and a drain region 10.

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DESCRIPTION JPH07169958

[0001]
The present invention relates to a semiconductor device and a method of manufacturing the same, and more particularly to an insulated gate field effect transistor (hereinafter referred to as a MOSFET) and a method of manufacturing the same.

【産業上の利用分野】本発明は半導体装置およびその製造方法に関わり、特に絶縁ゲート電界効果トランジスタ（以下、ＭＯＳＦＥＴと称す）およびその製造方法に関する。

[0002]
2. Description of the Related Art When germanium is used as the source and drain of a MOSFET, a stable low resistance source and drain can be obtained since the resistivity of germanium is about one half of that of silicon. In addition, since the band gap of germanium is smaller than that of silicon, the Schottky barrier is also small, so that the source / drain contact has a low resistance.

【従来の技術】ＭＯＳＦＥＴのソース、ドレインにゲルマニウムを用いると、ゲルマニウムの抵抗率がシリコンの約１／２であるから安定した低抵抗のソース、ドレインが得られる。また、ゲルマニウムのバンドギャップがシリコンより小さいためショットキーバリヤも小さく、したがってソース、ドレインのコンタクトが低抵抗となる。

[0003]
The prior art disclosed in Japanese Patent Application Laid-Open No. 63-13379 using germanium for the source and drain of the MOSFET will be described.

ＭＯＳＦＥＴのソース、ドレインにゲルマニウムを用いた特開昭６３－１３３７９号公報に開示

されている従来技術を説明する。

[0004]
This prior art becomes the MOSFET of FIG. 5 (d) through the steps of FIGS. 5 (a) -5 (c).

この従来技術は図５（ａ）―図５（ｃ）の工程を経て図５（ｄ）のＭＯＳＦＥＴとなる。

[0005]
First, as shown in FIG. 5A, the gate electrode 3 of polycrystalline silicon is formed on the flat surface 21 of the p-type silicon substrate 1 via the gate oxide film 2, and silicon oxide is formed on the gate electrode 3. The film 4 is formed, and the side wall 5 of the silicon oxide film is formed on the side surface of the gate electrode 3.

まず図５（ａ）に示すように、ｐ型シリコン基板１の平坦な表面２１上にゲート酸化膜２を介して多結晶シリコンのゲート電極３を形成し、ゲート電極３の上部にはシリコン酸化膜４を、ゲート電極３の側面にはシリコン酸化膜の側壁５を形成する。

Next, as shown in FIG. 5 (b), the silicon substrate in the source and drain formation regions is etched to form a recess 22, and then, as shown in FIG. 5 (c), the n-type germanium layer 16 is The layer 16 is grown by the growth method to form the source and drain 16.

次に図５（ｂ）に示すように、ソースおよびドレイン形成領域のシリコン基板をエッチングして凹部２２を形成後、図５（ｃ）に示すように、ｎ型ゲルマニウム層１６を選択化学気相成長法により成長させ、この層１６によりソースおよびドレイン１６を形成する。

Further, as shown in FIG. 5D, after covering the surface with the interlayer insulating film 11 and opening the contact holes 12, the aluminum wiring 13 is connected to the source and drain 16 composed of the n-type germanium layer to form the MOSFET Complete. Here, the reason why the source and drain are made of germanium instead of silicon is to lower the diffusion layer resistance by utilizing the difference in resistivity as described above, and to lower the contact resistance by utilizing the difference in band gap.

更に図５（ｄ）に示すように、表面を層間絶縁膜１１で被い、コンタクト孔１２を開孔した後、アルミニウム配線１３をｎ型ゲルマニウム層から成るソースおよびドレイン１６に接続してＭＯＳＦＥＴが完成する。ここでソース・ドレインをシリコンではなくゲルマニウムによって形成したのは、上記したように抵抗率の差を利用して拡散層抵抗を下げ、バンドギャップの差を利用してコンタクト抵抗を下げるためである。

[0006]
In this conventional MOSFET, since the germanium layer is grown after etching the silicon substrate to form the source and drain regions, it is difficult to control the etching end point. There is a problem that the junction depth of the drain region tends to vary. In addition, in the n-channel MOSFET, the n-type germanium layer must be grown by selective chemical vapor deposition to form the source and drain regions, so that a CMOS in which the n-channel MOSFET and the p-channel MOSFET are mixed on the same chip There is a problem that it is not suitable as a manufacturing method.

【発明が解決しようとする課題】この従来のＭＯＳＦＥＴでは、ソースおよびドレイン領域を形成するためにシリコン基板をエッチングした後、ゲルマニウム層を成長させるため、エッチング終了点の制御が困難であり、ソースおよびドレイン領域の接合の深さがばらつき易いという問題がある。またｎチャネルＭＯＳＦＥＴにおいてはｎ型ゲルマニウム層を選択化学気相成長法により成長させてソースおよびドレイン領域を形成しなげればならないため、同一チップ上にｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴが混在するＣＭＯＳの製造方法としては適さないという問題がある。

[0007]
SUMMARY OF THE INVENTION A feature of the present invention is a first surface area as well as second and third surface areas spaced apart from the first surface area and flat with the first surface area. A silicon substrate having a surface region of the first conductive region, a gate electrode formed on the first surface region of the first conductivity type with a gate insulating film interposed therebetween, and an insulating film on the side, and the second and third surface regions. In the semiconductor device, the source and drain regions of the second conductivity type of the semiconductor layer made of germanium or germanium and liquid crystal of silicon formed respectively are formed. A metal wire such as an aluminum wire is connected to the upper surface of the semiconductor layer. Here, the semiconductor layer is formed of a stack of germanium or a mixed crystal of germanium and silicon different in composition ratio, and the composition ratio of germanium can be made higher in the upper layer than in the lower layer. Alternatively, the semiconductor layer is made of a mixed crystal of germanium and silicon in which the composition ratio changes, and the composition ratio of germanium can be made higher in the upper part than in the lower part. Further, a silicon layer of a second conductivity type is formed on each of the second and third surface regions of the silicon substrate under the semiconductor layer, and each of the source and drain regions is composed of the silicon layer and the semiconductor layer. It can be done.

【課題を解決するための手段】本発明の特徴は、第１の表面領域ならびに該第１の表面領域を間にはさんで位置しかつ該第１の表面領域と平坦な第２および第３の表面領域を有するシリコン基

板と、第一導電型の前記第１の表面領域上にゲート絶縁膜を介して形成され側面に絶縁膜を有するゲート電極と、前記第２および第３の表面領域上にそれぞれ形成されたゲルマニウムまたはゲルマニウムとシリコンの液晶から成る半導体層の第二導電型のソースおよびドレイン領域とを備える半導体装置にある。この半導体層の上面にはアルミニウム配線等の金属配線が接続される。ここで、前記半導体層が組成比の異なるゲルマニウムまたはゲルマニウムとシリコンの混晶の積層から成り、下層よりも上層の方がゲルマニウムの組成比を高くすることができる。あるいは、前記半導体層が組成比が変化するゲルマニウムとシリコンの混晶から成り、下部よりも上部の方がゲルマニウムの組成比を高くすることができる。また、前記半導体層下の前記シリコン基板の前記第２および第３の表面領域にそれぞれ第二導電型のシリコン層が形成され、前記ソースおよびドレイン領域のそれぞれは該シリコン層と前記半導体層により構成されることができる。

[0008]
Another feature of the present invention is that the semiconductor layer is formed on the second and third surface regions by selective chemical vapor deposition, and then the second conductivity type impurity is ion implanted. A method of manufacturing a semiconductor device is to obtain the semiconductor device by forming the source and drain regions of a conductive type.

本発明の他の特徴は、前記第２および第３の表面領域上に前記半導体層を選択化学気相成長法により形成し、しかる後、第二導電型の不純物をイオン注入することにより第二導電型の前記ソースおよびドレイン領域を形成することで上記半導体装置を得る半導体装置の製造方法にある。

[0009]
The present invention will now be described with reference to the drawings.

【実施例】次に本発明について図面を参照して説明する。

[0010]
FIG. 1 is a plan view (a) showing a MOSFET according to a first embodiment of the present invention and a cross-sectional view (b) of a B-B 'portion of (a).

図１は本発明の第１の実施例のＭＯＳＦＥＴを示す平面図（ａ）および（ａ）のＢ－Ｂ′部の断面図（ｂ）である。

In the plan view (a), the interlayer insulating film is omitted.

なお平面図（ａ）において層間絶縁膜は図示を省略してある。

[0011]
The first and second surface regions 31 and 31 are interposed between the flat main surface 21 of the p-type silicon substrate 1 and the first and second surface regions 31 and 32 are flat and flat. It has surface area 32,33.

ｐ型シリコン基板１の平坦な主表面２１に第１の表面領域３１とこの第１の表面領域３１を間にはさんで位置しかつ第１の表面領域３１と平坦な第２および第３の表面領域３２，３３を有している。

The gate electrode 3 is formed on the p-type first surface region 31 via the gate oxide film 2, the upper surface of the gate electrode 3 is covered with the silicon oxide film 4, and the side wall is covered with the silicon oxide film 5. Source and drain regions 10 together with silicon layers 6 and 6 formed on the second and third surface regions below the n-type germania layers 7, 7 respectively formed on the second and third surface regions 32, 33 , 10 are configured. The aluminum wires 13 are connected to the n-type germanium layers 7 as source and drain electrode wires through the contact holes 12 formed in the interlayer insulating film 11.

ｐ型の第１の表面領域３１上にゲート酸化膜２を介してゲート電極３が形成され、ゲート電極３の上面をシリコン酸化膜４が被覆し側壁をシリコン酸化膜５が被覆している。第２および第３の表面領域３２，３３上にそれぞれｎ型ゲルマニム層７，７が生成されその下の第２および第３の表面領域に形成されたシリコン層６，６とともにソースおよびドレイン領域１０，１０を構成している。そして層間絶縁膜１１に形成されたコンタクト孔１２を通してアルミニウム配線１３，１３がソース電極配線およびドレイン電極配線としてｎ型ゲルマニウム層７，７に接続されている。

[0012]
Next, the manufacturing method of the first embodiment will be described with reference to FIG.

次に図２を参照して第１の実施例の製造方法を説明する。

[0013]
First, as shown in FIG. 2A, polycrystalline silicon having a thickness of 200 nm is formed on the first surface region 31 of the flat surface 21 of the p-type silicon substrate 1 through the gate oxide film 2 having a thickness of 5 to 10 nm. The gate electrode 3 is formed, the silicon oxide film 4 having a thickness of 50 nm is formed on the gate electrode 3, and the side wall 5 of the silicon oxide film having a width of 50 to 100 nm is formed on the side surface of the gate

electrode 3.

まず、図２（ａ）に示すように、ｐ型シリコン基板１の平坦な表面２１の第１の表面領域３１に厚さ５～１０ｎｍのゲート酸化膜２を介して厚さ２００ｎｍの多結晶シリコンのゲート電極３を形成し、ゲート電極３の上部には厚さ５０ｎｍのシリコン酸化膜４を、ゲート電極３の側面には幅５０～１００ｎｍのシリコン酸化膜の側壁５を形成する。

[0014]
Next, as shown in FIG. 2 (b), the 50 to 100 nm thick non-doped germanium layer 14 is selected on the second and third surface regions 32, 33 of the silicon substrate to be the source and drain forming regions. Grow by phase growth method.

次に図２（ｂ）に示すように、ソースおよびドレイン形成領域となるシリコン基板の第２および第３の表面領域３２，３３上に厚さ５０～１００ｎｍのノンドープのゲルマニウム層１４を選択化学気相成長法により成長させる。

[0015]
Next, as shown in FIG. 2C, n-type impurities are ion-implanted to form a source and drain 10 comprising n-type silicon layers 6, 6 and n-type germanium layers 7, 7.

次に図２（ｃ）に示すように、ｎ型不純物をイオン注入してｎ型シリコン層６，６とｎ型ゲルマニウム層７，７から成るソースおよびドレイン１０を形成する。

[0016]
Next, as shown in FIG. 2D, the surface is covered with an interlayer insulating film 11 and the contact holes 12 are opened, and then the aluminum wires 13 and 13 are used as n-type germanium layers 7 of the source and drain 10, 10, Then, the MOSFET shown in FIG. 1 is completed.

次に図２（ｄ）に示すように、表面を層間絶縁膜１１で被い、コンタクト孔１２を開孔した後、アルミニウム配線１３，１３をソースおよびドレイン１０，１０のｎ型ゲルマニウム層７，７の上面に接続し、図１に示す構造のＭＯＳＦＥＴが完成する。

Although the diffusion layer resistance and the contact resistance are slightly high, it is also possible to grow a silicon germanium layer instead of the germanium layer 7.

なお拡散層抵抗及びコンタクト抵抗はやや高くなるが、ゲルマニウム層７の代りにシリコンゲル

マニウム層を成長させても差し支えない。

[0017]
FIG. 3 is a cross-sectional view showing a MOSFET according to a second embodiment of the present invention. The difference from the first embodiment is that the source and drain regions 10, 10 are n-type silicon layers 6, 6 and n-type silicon germanium. The mixed crystal layers 8 and 8 and the n-type germanium layers 7 and 7 stacked thereover.

図３は本発明の第２の実施例のＭＯＳＦＥＴを示す断面図であり、第１の実施例との相違点はソースおよびドレイン領域１０，１０がｎ型シリコン層６，６とｎ型シリコンゲルマニウムの混晶の層８，８およびその上に積層されたｎ型ゲルマニウム層７，７から構成されていることである。

[0018]
Further, FIG. 4 is a cross-sectional view of a MOSFET showing a third embodiment of the present invention, and the source and drain regions 10 have a composition ratio of germanium in the upper part than the n-type silicon layers 6, 6 and the lower part. It is composed of layers 9 and 9 of mixed crystals of high n-type silicon germanium.

また、図４は本発明の第３の実施例を示すＭＯＳＦＥＴの断面図であり、ソースおよびドレイン領域１０，１０はｎ型シリコン層６，６と下部よりも上部の方がゲルマニウムの組成比が高いｎ型シリコンゲルマニウムの混晶の層９，９から構成されている。

[0019]
Although it is desirable that the source and drain regions be formed of germanium in order to lower the diffusion layer resistance and the contact resistance, when the germanium layer is directly grown on the surface of the silicon substrate, the lattice constant difference between silicon and germanium As a result, crystal defects may occur to deteriorate the characteristics of the MOSFET.

拡散層抵抗及びコンタクト抵抗を下げるためにはソースおよびドレイン領域はゲルマニウムで形成されることが望ましいが、一方でシリコン基板の表面にゲルマニウム層を直接成長させた場合、シリコンとゲルマニウムの格子定数の相違から結晶欠陥が発生しＭＯＳＦＥＴの特性を悪化させる可能性がある。

In order to avoid this problem, in the second and third embodiments, a silicon germanium layer having a lattice constant between silicon and germanium is formed as a buffer layer on the

surface of the silicon substrate to prevent the occurrence of crystal defects. It is

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この問題を避けるために、第２、第３の実施例ではシリコン基板の表面にシリコンとゲルマニウムの中間の格子定数を有するシリコンゲルマニウム層をバッファ層として形成し、結晶欠陥の発生を防止しているのである。

[0020]

According to the present invention, the MOSFET according to the present invention is formed of germanium or a mixed crystal of germanium and silicon formed with a predetermined thickness on the surface of the first conductivity type silicon substrate with the gate electrode interposed therebetween. Source and drain regions of the second conductivity type including a semiconductor layer are provided.

【発明の効果】本発明のＭＯＳＦＥＴは、ゲート電極をはさんで第一導電型のシリコン基板表面上に所定の厚さを持って形成されたゲルマニウムまたはゲルマニウムとシリコンの混晶から構成されている半導体層を含む第二導電型のソースおよびドレイン領域を備えている。

[0021]

The semiconductor layer is formed by selective chemical vapor deposition, and the source and drain regions are formed by ion implantation of impurities of the second conductivity type thereafter.

また上記半導体層は選択化学気相成長法によって形成され、その後で第二導電型の不純物をイオン注入することによって、上記ソースおよびドレイン領域が形成されている。

Therefore, a shallow junction can be formed with good controllability as compared with the conventional example, and it is also suitable as a CMOS manufacturing method.

したがって従来例に比較して浅い接合を制御性良く形成することができ、しかもＣＭＯＳの製造方法としても適したものとなっている。

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CLAIMS JPH07169958

1.
A silicon substrate having a first surface area and a first and second surface area spaced apart from the first surface area and flat with the first and second surface areas; A gate electrode formed on a first surface region through a gate insulating film and having an insulating film on the side surface, and germanium or a mixed crystal of germanium and silicon formed on the second and third surface regions, respectively A semiconductor device comprising: source and drain regions of a second conductivity type of a semiconductor layer.

第１の表面領域ならびに該第１の表面領域を間にはさんで位置しかつ該第１の表面領域と平坦な第２および第３の表面領域を有するシリコン基板と、第一導電型の前記第１の表面領域上にゲート絶縁膜を介して形成され側面に絶縁膜を有するゲート電極と、前記第２および第３の表面領域上にそれぞれ形成されたゲルマニウムまたはゲルマニウムとシリコンの混晶から成る半導体層の第二導電型のソースおよびドレイン領域とを備えることを特徴とする半導体装置。

2.
2. The semiconductor device according to claim 1, wherein the semiconductor layer is formed of a stack of germanium or mixed crystals of germanium and silicon having different composition ratios, and the upper layer has a higher composition ratio of germanium than the lower layer.

前記半導体層が組成比の異なるゲルマニウムまたはゲルマニウムとシリコンの混晶の積層から成り、下層よりも上層の方がゲルマニウムの組成比が高いことを特徴とする請求項１に記載の半導体装置。

3.
2. The semiconductor device according to claim 1, wherein the semiconductor layer is made of a

mixed crystal of germanium and silicon whose composition ratio changes, and the composition ratio of germanium is higher in the upper part than in the lower part.

前記半導体層が組成比が変化するゲルマニウムとシリコンの混晶から成り、下部よりも上部の方がゲルマニウムの組成比が高いことを特徴とする請求項１に記載の半導体装置。

4.

A silicon layer of a second conductivity type is formed on each of the second and third surface regions of the silicon substrate under the semiconductor layer, and each of the source and drain regions is composed of the silicon layer and the semiconductor layer The semiconductor device according to claim 1 or 2 characterized in that:

前記半導体層下の前記シリコン基板の前記第２および第３の表面領域にそれぞれ第二導電型のシリコン層が形成され、前記ソースおよびドレイン領域のそれぞれは該シリコン層と前記半導体層により構成されていることを特徴とする請求項１請求項２もしくは請求項３に記載の半導体装置。

5.

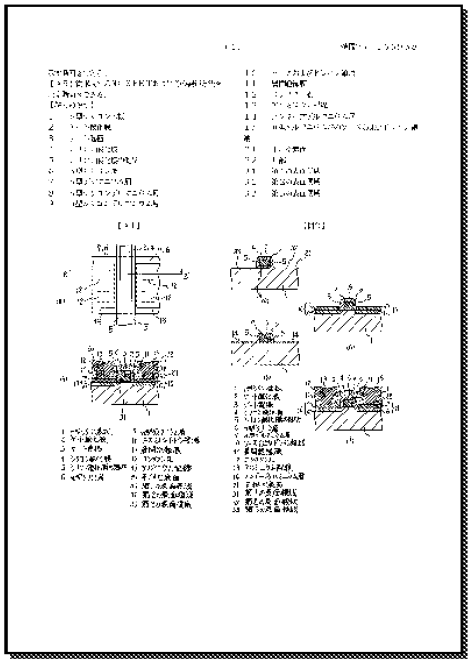
The semiconductor device according to claim 1, wherein a metal wiring is connected to an upper surface of the semiconductor layer.

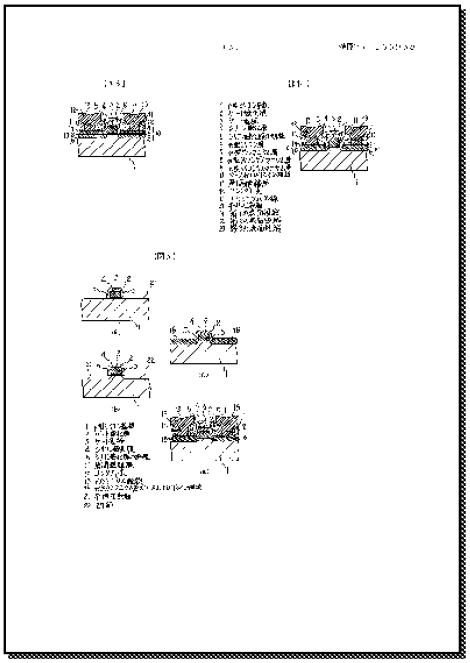
前記半導体層の上面に金属配線が接続されていることを特徴とする請求項１に記載の半導体装置。

6.

The semiconductor layer is formed on the second and third surface regions by a selective chemical vapor deposition method, and then the second conductivity type source and drain regions are formed by ion implantation of impurities of the second conductivity type. A method of manufacturing a semiconductor device according to any one of claims 1 to 5, wherein:

前記第２および第３の表面領域上に前記半導体層を選択化学気相成長法により形成し、しかる後、第二導電型の不純物をイオン注入することにより第二導電型の前記ソースおよびドレイン領域を形成することを特徴とする請求項１乃至請求項５にいずれかに記載の半導体装置の製造方法。





Drawing pages of JPH07169958 A

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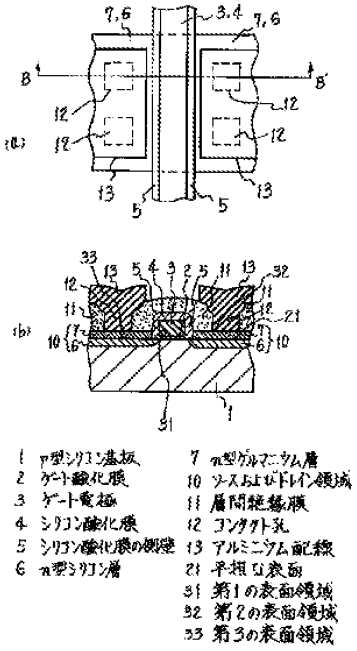
(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号

(72)発明者　安藤　岳
東京都港区芝五丁目７番１号　日本電気株式会社内

(74)代理人　弁理士　京本　直樹　（外２名）

(54)【発明の名称】　半導体装置およびその製造方法

(57)【要約】
【目的】低拡散層抵抗、低コンタクト抵抗のソースおよびドレイン領域の浅い接合を、制御性良く形成する。
【構成】ゲート電極３をはさんだｐ型シリコン基板１の表面上にゲルマニウム層またはシリコンゲルマニウム層を選択化学気相成長法によって形成し、その後でｎ型不純物をイオン注入することによって、ソースおよびドレイン領域１０を形成する。



【特許請求の範囲】
【請求項1】　第1の表面領域ならびに該第1の表面領域を間にはさんで位置しかつ該第1の表面領域と平坦な第2および第3の表面領域を有するシリコン基板と、第一導電型の前記第1の表面領域上にゲート絶縁膜を介して形成され側面に絶縁膜を有するゲート電極と、前記第2および第3の表面領域上にそれぞれ形成されたゲルマニウムまたはゲルマニウムとシリコンの混晶から成る半導体層の第二導電型のソースおよびドレイン領域とを備えることを特徴とする半導体装置。
【請求項2】　前記半導体層が組成比の異なるゲルマニウムまたはゲルマニウムとシリコンの混晶の積層から成り、下層よりも上層の方がゲルマニウムの組成比が高いことを特徴とする請求項1に記載の半導体装置。
【請求項3】　前記半導体層が組成比が変化するゲルマニウムとシリコンの混晶から成り、下部よりも上部の方がゲルマニウムの組成比が高いことを特徴とする請求項1に記載の半導体装置。
【請求項4】　前記半導体層下の前記シリコン基板の前記第2および第3の表面領域にそれぞれ第二導電型のシリコン層が形成され、前記ソースおよびドレイン領域のそれぞれは該シリコン層と前記半導体層により構成されていることを特徴とする請求項1請求項2もしくは請求項3に記載の半導体装置。
【請求項5】　前記半導体層の上面に金属配線が接続されていることを特徴とする請求項1に記載の半導体装置。
【請求項6】　前記第2および第3の表面領域上に前記半導体層を選択化学気相成長法により形成し、しかる後、第二導電型の不純物をイオン注入することにより第二導電型の前記ソースおよびドレイン領域を形成することを特徴とする請求項1乃至請求項5にいずれかに記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【産業上の利用分野】本発明は半導体装置およびその製造方法に関わり、特に絶縁ゲート電界効果トランジスタ（以下、ＭＯＳＦＥＴと称す）およびその製造方法に関する。
【０００２】
【従来の技術】ＭＯＳＦＥＴのソース、ドレインにゲルマニウムを用いると、ゲルマニウムの抵抗率がシリコンの約１／２であるから安定した低抵抗のソース、ドレインが得られる。また、ゲルマニウムのバンドギャップがシリコンより小さいためショットキーバリヤも小さく、したがってソース、ドレインのコンタクトが低抵抗となる。
【０００３】ＭＯＳＦＥＴのソース、ドレインにゲルマニウムを用いた特開昭６３－１３３７９号公報に開示されている従来技術を説明する。
【０００４】この従来技術は図５（ａ）－図５（ｃ）の工程を経て図５（ｄ）のＭＯＳＦＥＴとなる。
【０００５】まず図５（ａ）に示すように、ｐ型シリコン基板１の平坦な表面２１上にゲート酸化膜２を介して多結晶シリコンのゲート電極３を形成し、ゲート電極３の上部にはシリコン酸化膜４を、ゲート電極３の側面にはシリコン酸化膜の側壁５を形成する。次に図５（ｂ）に示すように、ソースおよびドレイン形成領域のシリコン基板をエッチングして凹部２２を形成後、図５（ｃ）に示すように、ｎ型ゲルマニウム層１６を選択化学気相成長法により成長させ、この層１６によりソースおよびドレイン１６を形成する。更に図５（ｄ）に示すように、表面を層間絶縁膜１１で被い、コンタクト孔１２を開孔した後、アルミニウム配線１３をｎ型ゲルマニウム層から成るソースおよびドレイン１６に接続してＭＯＳＦＥＴが完成する。ここでソース・ドレインをシリコンではなくゲルマニウムによって形成したのは、上記したように抵抗率の差を利用して拡散層抵抗を下げ、バンドギャップの差を利用してコンタクト抵抗を下げるためである。
【０００６】
【発明が解決しようとする課題】この従来のＭＯＳＦＥＴでは、ソースおよびドレイン領域を形成するためにシリコン基板をエッチングした後、ゲルマニウム層を成長させるため、エッチング終了点の制御が困難であり、ソースおよびドレイン領域の接合の深さがばらつき易いという問題がある。またｎチャネルＭＯＳＦＥＴにおいてはｎ型ゲルマニウム層を選択化学気相成長法により成長させてソースおよびドレイン領域を形成しなければならないため、同一チップ上にｎチャネルＭＯＳＦＥＴとｐチャネルＭＯＳＦＥＴが混在するＣＭＯＳの製造方法としては適さないという問題がある。
【０００７】
【課題を解決するための手段】本発明の特徴は、第1の表面領域ならびに該第1の表面領域を間にはさんで位置しかつ該第1の表面領域と平坦な第2および第3の表面領域を有するシリコン基板と、第一導電型の前記第1の表面領域上にゲート絶縁膜を介して形成され側面に絶縁膜を有するゲート電極と、前記第2および第3の表面領域上にそれぞれ形成されたゲルマニウムまたはゲルマニウムとシリコンの液晶から成る半導体層の第二導電型のソースおよびドレイン領域とを備える半導体装置にある。この半導体層の上面にはアルミニウム配線等の金属配線が接続される。ここで、前記半導体層が組成比の異なるゲルマニウムまたはゲルマニウムとシリコンの混晶の積層から成り、下層よりも上層の方がゲルマニウムの組成比を高くすることができる。あるいは、前記半導体層が組成比が変化するゲルマニウムとシリコンの混晶から成り、下部よりも上部の方がゲルマニウムの組成比を高くすることができる。また、前記半導体層下の前記シ

リコン基板の前記第２および第３の表面領域にそれぞれ第二導電型のシリコン層が形成され、前記ソースおよびドレイン領域のそれぞれは該シリコン層と前記半導体層により構成されることができる。

【０００８】本発明の他の特徴は、前記第２および第３の表面領域上に前記半導体層を選択化学気相成長法により形成し、しかる後、第二導電型の不純物をイオン注入することにより第二導電型の前記ソースおよびドレイン領域を形成することで上記半導体装置を得る半導体装置の製造方法にある。

【０００９】

【実施例】次に本発明について図面を参照して説明する。

【００１０】図１は本発明の第１の実施例のＭＯＳＦＥＴを示す平面図（ａ）および（ａ）のＢ－Ｂ′部の断面図（ｂ）である。なお平面図（ａ）において層間絶縁膜は図示を省略してある。

【００１１】ｐ型シリコン基板１の平坦な主表面２１に第１の表面領域３１とこの第１の表面領域３１を間にはさんで位置しかつ第１の表面領域３１と平坦な第２および第３の表面領域３２、３３を有している。ｐ型の第１の表面領域３１上にゲート酸化膜２を介してゲート電極３が形成され、ゲート電極３の上面をシリコン酸化膜４が被覆し側壁をシリコン酸化膜５が被覆している。第２および第３の表面領域３２，３３上にそれぞれｎ型ゲルマニム層７，７が生成されその下の第２および第３の表面領域に形成されたシリコン層６，６とともにソースおよびドレイン領域１０，１０を構成している。そして層間絶縁膜１１に形成されたコンタクト孔１２を通してアルミニウム配線１３，１３がソース電極配線およびドレイン電極配線としてｎ型ゲルマニウム層７，７に接続されている。

【００１２】次に図２を参照して第１の実施例の製造方法を説明する。

【００１３】まず、図２（ａ）に示すように、ｐ型シリコン基板１の平坦な表面２１の第１の表面領域３１に厚さ５～１０ｎｍのゲート酸化膜２を介して厚さ２００ｎｍの多結晶シリコンのゲート電極３を形成し、ゲート電極３の上部には厚さ５０ｎｍのシリコン酸化膜４を、ゲート電極３の側面には幅５０～１００ｎｍのシリコン酸化膜の側壁５を形成する。

【００１４】次に図２（ｂ）に示すように、ソースおよびドレイン形成領域となるシリコン基板の第２および第３の表面領域３２，３３上に厚さ５０～１００ｎｍのノンドープのゲルマニウム層１４を選択化学気相成長法により成長させる。

【００１５】次に図２（ｃ）に示すように、ｎ型不純物をイオン注入してｎ型シリコン層６，６とｎ型ゲルマニウム層７，７から成るソースおよびドレイン１０を形成する。

【００１６】次に図２（ｄ）に示すように、表面を層間絶縁膜１１で被い、コンタクト孔１２を開孔した後、アルミニウム配線１３，１３をソースおよびドレイン１０，１０のｎ型ゲルマニウム層７，７の上面に接続し、図１に示す構造のＭＯＳＦＥＴが完成する。なお拡散層抵抗及びコンタクト抵抗はやや高くなるが、ゲルマニウム層７の代りにシリコンゲルマニウム層を成長させても差し支えない。

【００１７】図３は本発明の第２の実施例のＭＯＳＦＥＴを示す断面図であり、第１の実施例との相違点はソースおよびドレイン領域１０，１０がｎ型シリコン層６，６とｎ型シリコンゲルマニウムの混晶の層８，８およびその上に積層されたｎ型ゲルマニウム層７，７から構成されていることである。

【００１８】また、図４は本発明の第３の実施例を示すＭＯＳＦＥＴの断面図であり、ソースおよびドレイン領域１０，１０はｎ型シリコン層６，６と下部よりも上部の方がゲルマニウムの組成比が高いｎ型シリコンゲルマニウムの混晶の層９，９から構成されている。

【００１９】拡散層抵抗及びコンタクト抵抗を下げるためにはソースおよびドレイン領域はゲルマニウムで形成されることが望ましいが、一方でシリコン基板の表面にゲルマニウム層を直接成長させた場合、シリコンとゲルマニウムの格子定数の相違から結晶欠陥が発生しＭＯＳＦＥＴの特性を悪化させる可能性がある。この問題を避けるために、第２、第３の実施例ではシリコン基板の表面にシリコンとゲルマニウムの中間の格子定数を有するシリコンゲルマニウム層をバッファ層として形成し、結晶欠陥の発生を防止しているのである。

【００２０】

【発明の効果】本発明のＭＯＳＦＥＴは、ゲート電極をはさんで第一導電型のシリコン基板表面上に所定の厚さを持って形成されたゲルマニウムまたはゲルマニウムとシリコンの混晶から構成されている半導体層を含む第二導電型のソースおよびドレイン領域を備えている。

【００２１】また上記半導体層は選択化学気相成長法によって形成され、その後で第二導電型の不純物をイオン注入することによって、上記ソースおよびドレイン領域が形成されている。したがって従来例に比較して浅い接合を制御性良く形成することができ、しかもＣＭＯＳの製造方法としても適したものとなっている。

【図面の簡単な説明】

【図１】本発明の第１の実施例におけるＭＯＳＦＥＴを示す平面図（ａ）および（ａ）のＢ－Ｂ′部の断面図（ｂ）である。

【図２】本発明の第１の実施例におけるＭＯＳＦＥＴの製造方法を工程順に示した断面図である。

【図３】本発明の第２の実施例におけるＭＯＳＦＥＴを示す断面図である。

【図４】本発明の第３の実施例におけるＭＯＳＦＥＴを

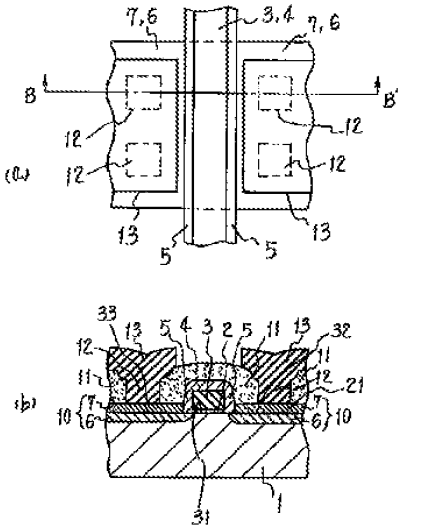
示す断面図である。

【図5】従来技術のＭＯＳＦＥＴおよびその製造方法を示す断面図である。

【符号の説明】

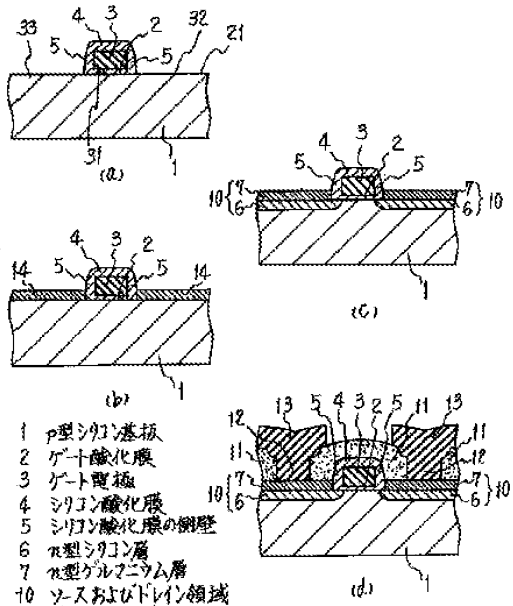
1　p型シリコン基板
2　ゲート酸化膜
3　ゲート電極
4　シリコン酸化膜
5　シリコン酸化膜の側壁
6　n型シリコン層
7　n型ゲルマニウム層
8　n型シリコンゲルマニウム層
9　n型シリコンゲルマニウム層
10　ソースおよびドレイン領域
11　層間絶縁膜
12　コンタクト孔
13　アルミニウム配線
14　ノンドープゲルマニウム層
15　n型ゲルマニウム層のソースおよびドレイン領域
21　平坦な表面
22　凹部
31　第1の表面領域
32　第2の表面領域
33　第3の表面領域

【図1】



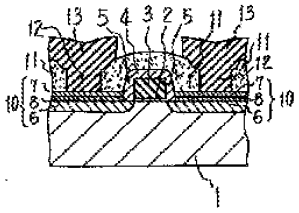
1　p型シリコン基板
2　ゲート酸化膜
3　ゲート電極
4　シリコン酸化膜
5　シリコン酸化膜の側壁
6　n型シリコン層
7　n型ゲルマニウム層
10　ソースおよびドレイン領域
11　層間絶縁膜
12　コンタクト孔
13　アルミニウム配線
21　平坦な表面
31　第1の表面領域
32　第2の表面領域
33　第3の表面領域

【図2】

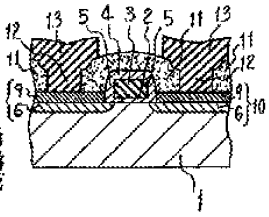


1　p型シリコン基板
2　ゲート酸化膜
3　ゲート電極
4　シリコン酸化膜
5　シリコン酸化膜の側壁
6　n型シリコン層
7　n型ゲルマニウム層
10　ソースおよびドレイン領域
11　層間絶縁膜
12　コンタクト孔
13　アルミニウム配線
14　ノンドープゲルマニウム層
21　平坦な表面
31　第1の表面領域
32　第2の表面領域
33　第3の表面領域

【図3】

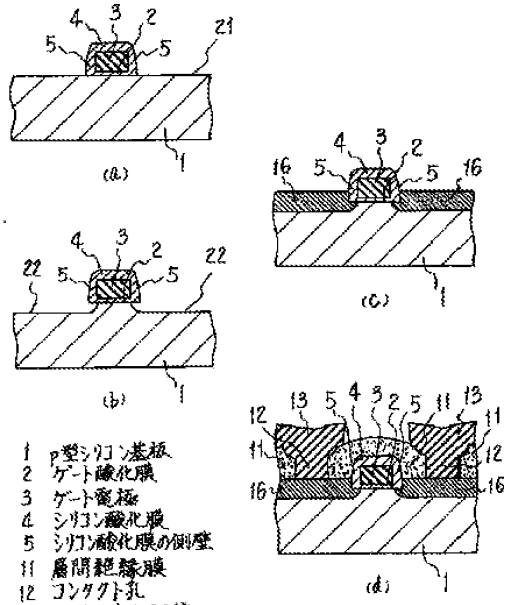


【図4】



1 P型シリコン基板
2 ゲート酸化膜
3 ゲート電極
4 シリコン酸化膜
5 シリコン酸化膜の側壁
6 n型シリコン層
7 n型ゲルマニウム層
8 n型シリコンゲルマニウム層
9 n型シリコンゲルマニウム層
10 ソースおよびドレイン領域
11 層間絶縁膜
12 コンタクト孔
13 アルミニウム配線
21 平坦な表面
31 第1の表面領域
32 第2の表面領域
33 第3の表面領域

【図5】



1 P型シリコン基板
2 ゲート酸化膜
3 ゲート電極
4 シリコン酸化膜
5 シリコン酸化膜の側壁
11 層間絶縁膜
12 コンタクト孔
13 アルミニウム配線
16 n型ゲルマニウム層のソースおよびドレイン領域
21 平坦な表面
22 凹部

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First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
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Information:					
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Warnings:					
Information:					
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Warnings:					
Information:					
5	Non Patent Literature	P38507CN_Grant_w_English_translation_02_26_16.pdf	337460 ec50253aef7030d33b3d1165758a12e0b33c5d20	no	4
Warnings:					
Information:					
6	Non Patent Literature	P38507CN_OA1_no_translation_05_05_15.pdf	536678 f25838a77eb07e9af79e27c35f83cc078b911760	no	6
Warnings:					
Information:					
7	Non Patent Literature	P38507CN_OA2_no_translation_10_20_15.pdf	229650 60d9e29da3d9286755c2d70eba19e02b453c146c	no	3
Warnings:					

Information:					
8	Non Patent Literature	P38507CN-D_OA1_no_translation_05_04_18.pdf	575789 088571743b837219d61b61460eef265a048f8980	no	6
Warnings:					
Information:					
9	Non Patent Literature	P38507CN-D_OA2_no_Translation_12_03_18.pdf	525337 de44283c8e092d7f84e4c5b98c7fc44cb6f65e19	no	5
Warnings:					
Information:					
10	Non Patent Literature	P38507CN-D_OA3_no_translation_04_10_19.pdf	476509 f3dcfa72b7e5d91ee8ab5593059dc625320f0d37	no	4
Warnings:					
Information:					
11	Non Patent Literature	P38507JP_NOA_no_translation_02_10_15.pdf	517378 34f5066878322b8cc52783889d34fe99ba6ecf26	no	3
Warnings:					
Information:					
12	Non Patent Literature	P38507KR_NOA_no_translation_11_13_14.pdf	603063 4d9ec6000de670f5ec83bb50586182e9a0232fb1	no	3
Warnings:					
Information:					
			Total Files Size (in bytes):	42023169	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	16/416,445
Filing Date	May 20, 2019
First Inventor	Glenn A. GLASS, et al.
Art Unit	2826
Examiner Name	N/A
Attorney Docket No.	P38507USC2-C1

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 CFR § I.98(d)(l) copies of the references were provided in prior applications 13/990,224 filed September 30, 2011, 14/673,143 filed March 30, 2015, 15/339,308 filed October 31, 2016 which are relied on for priority.

It is respectfully requested that the examiner consider information which has been previously submitted to the Patent Office in the parent application and any prior related applications.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☐ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	08-02-2019
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal */Sheri Villarreal/* *Date* 08-02-2019

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/416,445	05/20/2019	2811	1880	P38507USC2-C1	9	3

CONFIRMATION NO. 5347

UPDATED FILING RECEIPT

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204



Date Mailed: 08/01/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

GLENN A. GLASS, Portland, OR;
ANAND S. MURTHY, Portland, OR;
TAHIR GHANI, Portland, OR;

Applicant(s)

INTEL CORPORATION, Santa Clara, CA;

Assignment For Published Patent Application

INTEL CORPORATION, Santa Clara, CA

Power of Attorney: The patent practitioners associated with Customer Number 31817

Domestic Priority data as claimed by applicant

This application is a CON of 15/339,308 10/31/2016 PAT 10297670
which is a CON of 14/673,143 03/30/2015 PAT 9484432
which is a CON of 13/990,224 05/29/2013 PAT 8994104
which is a 371 of PCT/US2011/054198 09/30/2011
which is a CIP of 12/975,278 12/21/2010 PAT 8901537

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/28/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/416,445**

Projected Publication Date: 11/07/2019

Non-Publication Request: No

Early Publication Request: No

Title

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/416,445

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	9 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Glass et al.	Examiner: Not yet assigned
Application No.: 16/416,445	Art Unit: 2826
Filed: May 20, 2019	Confirmation No.: 5347
For: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Examiner:

This Preliminary Amendment is being filed in the above matter before the mailing of a first Office Action from the United States Patent and Trademark Office. Applicants respectfully request the Examiner to enter this Amendment and consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendment to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. – 9. (Canceled)

10. (New) An integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin;

a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

11. (New) The integrated circuit structure of claim 10, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

12. (New) The integrated circuit structure of claim 10, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

13. (New) The integrated circuit structure of claim 10, wherein the fin comprises a strained channel between the first and second source or drain regions.

14. (New) The integrated circuit structure of claim 10, wherein the first and second source or drain regions are P-type.

15. (New) An integrated circuit structure, comprising:

a body comprising silicon;

a gate electrode over the body;

a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the body proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

16. (New) The integrated circuit structure of claim 15, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

17. (New) The integrated circuit structure of claim 15, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

18. (New) The integrated circuit structure of claim 15, wherein the body comprises a strained channel between the first and second source or drain regions.

19. (New) The integrated circuit structure of claim 15, wherein the first and second source or drain regions are P-type.

20. (New) A computing device, comprising:

a board; and

a component coupled to the board, the component including an integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin;

a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

21. (New) The computing device of claim 20, further comprising:

a memory coupled to the board.

22. (New) The computing device of claim 20, further comprising:

a communication chip coupled to the board.

23. (New) The computing device of claim 20, further comprising:

a camera coupled to the board.

24. (New) The computing device of claim 20, further comprising:

a global positioning system coupled to the board.

25. (New) The computing device of claim 20, further comprising:

a battery coupled to the board.

26. (New) The computing device of claim 20, further comprising:

an antenna coupled to the board.

27. (New) The computing device of claim 20, wherein the component is a packaged integrated circuit die.

28. (New) The computing device of claim 20, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

29. (New) The computing device of claim 20, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

REMARKS

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 50-0393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

July 31, 2019
Date

/Justin K. Brask/
Justin K. Brask
Reg. No. 61080

1211 SW 5th, Ste. 1900
Portland, OR 97204
Telephone: (503) 222-9981
Facsimile: (503) 796-2900

Electronic Acknowledgement Receipt	
EFS ID:	36748675
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	31-JUL-2019
Filing Date:	20-MAY-2019
Time Stamp:	20:42:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38507USC2-C1_PrelimAmd_07-31-19.pdf	91803 61240dd1c8a1d58c275abd87ba2c891900bc9045	yes	8

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	7
	Applicant Arguments/Remarks Made in an Amendment	8	8
Warnings:			
Information:			
	Total Files Size (in bytes):	91803	

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 16/416,445	Filing Date 05/20/2019	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	07/31/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/DIANE FLOYD/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
GLENN A. GLASS	Examiner: N/A
Application No.: 16/416,445	Art Unit: 2811
Filed: May 20, 2019	Confirmation No.: 5347
For: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION,

Dear Examiner:

This is in response to the Notice to File Missing Parts of Nonprovisional Application mailed May 29, 2019 and June 20, 2019, please find enclosed:

- Payment in the amount of $160.00 for the surcharge of 37 CFR §1.16(f);

- statutory basic filing fee in the amount of $1720.00

If any additional fee is required, please charge deposit account No. 50-0393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, P.C.

July 29, 2019
Date

/Justin K. Brask/
Justin K. Brask
Reg. No. 61,080

1211 SW 5th Ave., Ste. 1900
Portland, OR 97204
Telephone: (503) 222-9981
Facsimile: (503) 796-2900

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1

CONFIRMATION NO. 5347

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

FORMALITIES LETTER

OC000000109042736

Date Mailed: 06/20/2019

NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on to the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION (Notice) mailed 05/29/2019 and it has been entered into the application. The reply, however, is not a complete reply for the reason(s) listed below. A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application. Replies should be mailed to: Mail Stop Missing Parts, Commissioner for Patents, P.O.Box 1450, Alexandria VA 22313-1450.

The period for reply continues to run from the date of the Notice mailed 05/29/2019. Applicant must submit all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the appropriate extension fee under the provisions of 37 CFR 1.136(a).

Applicant's reply to the Notice mailed on 05/29/2019 was received in the U.S. Patent and Trademark Office on , after the expiration of the two month period for reply set forth in the Notice. The application will become abandoned unless applicant obtains an extension of the period for reply, as above. The petition must be accompanied by the appropriate fee as set forth in 37 CFR 1.17 (see the current fees below). The date on which the reply, the petition, and the fee have been filed is the date of the reply and also the date for purposes of determining the period of extension and the corresponding amount of the fee due. The expiration of the time period is determined by the amount of the fee paid. Applicant is advised that extensions may not be granted under 37 CFR 1.136(a) for more than FIVE MONTHS beyond the time period set in the Notice.

Items Required to Avoid Abandonment:

The required items noted below SHOULD be filed along with any items required above.

- The statutory basic filing fee is missing.
- The application search fee was not received.
- The application examination fee was not received.
- Surcharge as set forth in 37 CFR 1.16(f) was not received.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of the Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Mail date of Notice:	05/29/2019
Last date that extension may be obtained: (Note: The petition and fee must be received by this date, or include a proper certificate of mailing under 37 CFR 1.8 with a date on or before this date, and extend the time to include this date.)	12/29/2019

Length of Extension of Time	Fee under 37 CFR 1.17(a) effective March 19, 2013		
(response due on or before)	Undiscounted	Small Entity	Micro Entity
One Month (08/29/2019)	$200	$100	$50
Two Months (09/29/2019)	$600	$300	$150
Three Months (10/29/2019)	$1400	$700	$350
Four Months (11/29/2019)	$2200	$1100	$550
Five Months (12/29/2019)	$3000	$1500	$750

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tbaile/

Electronic Patent Application Fee Transmittal

Application Number:	16416445
Filing Date:	20-May-2019
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Filer:	Justin K. Brask/Sheri Villarreal
Attorney Docket Number:	P38507USC2-C1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1880**

Electronic Acknowledgement Receipt	
EFS ID:	36714820
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	29-JUL-2019
Filing Date:	20-MAY-2019
Time Stamp:	15:13:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1880
RAM confirmation Number	E20197SF14288859
Deposit Account	500393
Authorized User	Sheri Villarreal
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	P38507USC2-C1_RTMP_07_29_19.pdf	73931 c51327094d2cc10421635e0dcdeb2eba6809cbbe	no	1
Warnings:					
Information:					
2	Applicant Response to Pre-Exam Formalities Notice	P38507USC2-C1_NTFMP_06_20_19.pdf	159106 5434691c8d161182d096a463a88d81d45132e1e2	no	3
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	37102 b789b9e7f33db600b4f37c9f519aff725062047e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	270139		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/416,445

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	9 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1

CONFIRMATION NO. 5347

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

FORMALITIES LETTER

OC000000109042736

Date Mailed: 06/20/2019

NOTICE OF INCOMPLETE REPLY (NONPROVISIONAL)

Filing Date Granted

The U.S. Patent and Trademark Office has received your reply on to the NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION (Notice) mailed 05/29/2019 and it has been entered into the application. The reply, however, is not a complete reply for the reason(s) listed below. A complete reply must be timely filed to prevent ABANDONMENT of the above-identified application. Replies should be mailed to: Mail Stop Missing Parts, Commissioner for Patents, P.O.Box 1450, Alexandria VA 22313-1450.

The period for reply continues to run from the date of the Notice mailed 05/29/2019. Applicant must submit all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the appropriate extension fee under the provisions of 37 CFR 1.136(a).

Applicant's reply to the Notice mailed on 05/29/2019 was received in the U.S. Patent and Trademark Office on , after the expiration of the two month period for reply set forth in the Notice. The application will become abandoned unless applicant obtains an extension of the period for reply, as above. The petition must be accompanied by the appropriate fee as set forth in 37 CFR 1.17 (see the current fees below). The date on which the reply, the petition, and the fee have been filed is the date of the reply and also the date for purposes of determining the period of extension and the corresponding amount of the fee due. The expiration of the time period is determined by the amount of the fee paid. Applicant is advised that extensions may not be granted under 37 CFR 1.136(a) for more than FIVE MONTHS beyond the time period set in the Notice.

Items Required to Avoid Abandonment:

The required items noted below SHOULD be filed along with any items required above.

- The statutory basic filing fee is missing.
- The application search fee was not received.
- The application examination fee was not received.
- Surcharge as set forth in 37 CFR 1.16(f) was not received.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of the Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Mail date of Notice:	05/29/2019
Last date that extension may be obtained: (Note: The petition and fee must be received by this date, or include a proper certificate of mailing under 37 CFR 1.8 with a date on or before this date, and extend the time to include this date.)	12/29/2019

Length of Extension of Time	Fee under 37 CFR 1.17(a) effective March 19, 2013		
(response due on or before)	Undiscounted	Small Entity	Micro Entity
One Month (08/29/2019)	$200	$100	$50
Two Months (09/29/2019)	$600	$300	$150
Three Months (10/29/2019)	$1400	$700	$350
Four Months (11/29/2019)	$2200	$1100	$550
Five Months (12/29/2019)	$3000	$1500	$750

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/thaile/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1

CONFIRMATION NO. 5347

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

POA ACCEPTANCE LETTER

OC000000109042917

Date Mailed: 06/20/2019

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/17/2019.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/thaile/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/416,445
Filing Date	May 20, 2019
First Named Inventor	GLENN A. GLASS
Title	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
Art Unit	2811
Examiner Name	N/A
Attorney Docket Number	P38507USC2-C1/111548

SIGNATURE of Applicant or Patent Practitioner

Signature	/Justin K. Brask/	Date (Optional)	
Name	Justin K. Brask	Registration Number	61080
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 01/31/2016. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
16/416,445	May 20, 2019

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 31817

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

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OR

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OR

☐	Firm or Individual Name				
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	
Name	Lisa Hopkinson		
Title	Administrator of Patents		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Electronic Acknowledgement Receipt	
EFS ID:	36322147
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	99256
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	17-JUN-2019
Filing Date:	20-MAY-2019
Time Stamp:	20:06:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	P38507USC2-C1_Transmittal_06_17_19.pdf	247182 97a93930c389d82334457706d8db6ed8b3cc5ec8	no	2

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	P38507USC2-C1_Stmt_373c_06_17_19.pdf	118130 0b1649fc92e9ec02724a30c8c807accee59598dd	no	3
Warnings:					
Information:					
3	Power of Attorney	P38507USC2-C1_POA_82A_06_17_19.pdf	155699 3e80cfc55f55090251d39913f893a2c5085c7398	no	1
Warnings:					
Information:					
4	Power of Attorney	P38507USC2-C1_POA_82B_06_17_19.pdf	791669 5e782650e8550c45a585af6b3a623e4e95e58863	no	1
Warnings:					
Information:					
		Total Files Size (in bytes):	1312680		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: TRAN.LET

Document Description: Transmittal Letter

PTO/SB/21 (07-09)
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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	16/416,445
Filing Date	May 20, 2019
First Named Inventor	GLENN A. GLASS
Art Unit	2811
Examiner Name	
Total Number of Pages in This Submission: 7	Attorney Docket Number: P38507USC2-C1/111548

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):
  Statement 373C, POA's

Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Schwabe, Williamson & Wyatt P.C.		
Signature	/Justin K. Brask/		
Printed name	Justin K. Brask		
Date	June 17, 2019	Reg. No.	61,080

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	/Sheri Villarreal/		
Typed or printed name	Sheri Villarreal	Date	June 17, 2019

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Intel Corporation

Application No./Patent No.: 16/416,445 Filed/Issue Date: May 20, 2019

Titled: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Intel Corporation, a corporation

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 027086, Frame 0004, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Justin K. Brask/	June 17, 2019
Signature	Date
Justin K. Brask	61080
Printed or Typed Name	Title or Registration Number

[Page 2 of 2]

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
16/416,445	05/20/2019	2811	0.00	P38507USC2-C1	9	3

CONFIRMATION NO. 5347

99256
Finch & Maloney PLLC
50 Commercial Street
Gateway One, Suite 300
Manchester, NH 03101

FILING RECEIPT

OC000000108301961

Date Mailed: 05/29/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

GLENN A. GLASS, Portland, OR;
ANAND S. MURTHY, Portland, OR;
TAHIR GHANI, Portland, OR;

Applicant(s)

INTEL CORPORATION, Santa Clara, CA;

Assignment For Published Patent Application

INTEL CORPORATION, Santa Clara, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 15/339,308 10/31/2016 PAT 10297670
which is a CON of 14/673,143 03/30/2015 PAT 9484432
which is a CON of 13/990,224 05/29/2013 PAT 8994104
which is a 371 of PCT/US2011/054198 09/30/2011
which is a CIP of 12/975,278 12/21/2010 PAT 8901537

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/28/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/416,445**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/416,445	05/20/2019	GLENN A. GLASS	P38507USC2-C1

CONFIRMATION NO. 5347

99256
Finch & Maloney PLLC
50 Commercial Street
Gateway One, Suite 300
Manchester, NH 03101

FORMALITIES LETTER

OC000000108501962

Date Mailed: 05/29/2019

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **300** basic filing fee.
- $ **160** surcharge.
- $ **660** search fee.
- $ **760** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1880** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tqlam/

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 16/416,445

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	9 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	GLENN	A.	GLASS	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	5009 NW 124th Avenue
Address 2	

City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	ANAND	S.	MURTHY	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	10934 NW Lucerne Court
Address 2	

City	Portland	State/Province	OR
Postal Code	97229	Country	US

Inventor 3 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	TAHIR		GHANI	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

City	Portland	State/Province	OR	Country of Residence	US

Mailing Address of Inventor:

Address 1	14191 NW Stonebridge Drive		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	99256		
Email Address	docketing@finchmaloney.com	Add Email	Remove Email

Application Information:

Title of the Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION		
Attorney Docket Number	P38507USC2-C1	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	11	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	99256		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending				Remove
Application Number	Continuity Type		Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of		15339308		2016-10-31
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15339308	Continuation of	14673143	2015-03-30	9484432	2016-11-01
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14673143	Continuation of	13990224	2013-05-29	8994104	2015-03-31
Prior Application Status	Expired				Remove
Application Number	Continuity Type		Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)
13990224	a 371 of international		PCT/US2011/054198		2011-09-30
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
PCT/US2011/0541	Continuation in part of	12975278	2010-12-21	8901537	2014-12-02

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	INTEL CORPORATION		
Mailing Address Information For Applicant:			
Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country	US	Postal Code	95054
Phone Number		Fax Number	
Email Address	docketing@finchmaloney.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	INTEL CORPORATION

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country i	US	Postal Code	95054
Phone Number		Fax Number	
Email Address	docketing@finchmaloney.com		

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Paul A. Smith/			Date (YYYY-MM-DD)	2019-05-20
First Name	Paul A.	Last Name	Smith	Registration Number	64,121

Additional Signature may be generated within this form by selecting the Add button. Add

PTO/AIA/14 (02-18)
Approved for use through 11/30/2020. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P38507USC2-C1
	Application Number	
Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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Title of Invention	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

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This declaration is directed to: ■ The attached application, or

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I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: GLENN A. GLASS Date (Optional): 5-22-13

Signature: Glenn A. Glass

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LEGAL NAME OF INVENTOR

Inventor: ANAND S. MURTHY Date (Optional): 5/23/13

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LEGAL NAME OF INVENTOR

Inventor: TAHIR GHANI Date (Optional): 5-23-13

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CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inventors:
Glenn A. Glass
Anand S. Murthy
Tahir Ghani

RELATED APPLICATIONS

[0001] This patent application is a continuation of U.S. Application No. 15/339,308, filed October 31, 2016, which is a continuation of U.S. Application No. 14/673,143, filed March 30, 2015, which is a continuation of 13/990,224, filed May 29, 2013, now U.S. Patent No. 8,994,104, which is a U.S. National Phase application under 35 U.S.C. § 371 of International Application No. PCT/US2011/054198, filed September 30, 2011, which is a continuation-in-part of U.S. Application No. 12/975,278 filed December 21, 2010, now U.S. Patent No. 8,901,537, each of which are incorporated herein by reference in their entireties.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0006] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention.

[0007] Figures 3A to 3I illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

[0008] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention.

[0009] Figures 5A to 5F illustrate structures that are formed when carrying out the method of Figure 4, in accordance with various embodiment of the present invention.

[0010] Figure 6 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

[0011] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap.

[0012] Figure 8 illustrates a computing system implemented with one or more transistor structures in accordance with an example embodiment of the present invention.

[0013] As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines, right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

[0014] Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

General Overview

[0015] As previously explained, increased drive current in the transistors can be achieved by reducing device resistance. Contact resistance is one component of a device's overall resistance. A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV. Thus, and in accordance with an example embodiment of the present invention, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value and contact resistance.

[0016] In one specific example embodiment, contacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV and a corresponding reduction in contact resistance of about 3X (relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer between the source/drain regions and contact metal). A transmission electron microscopy (TEM) cross section or secondary ion mass spectrometry (SIMS) profile can be used to show the germanium concentration throughout the vertical stack of the film structure, as profiles of

epitaxial alloys of silicon and SiGe can readily be distinguished from germanium concentration profiles.

[0017] Thus, transistor structures configured in accordance with embodiments of the present invention provide an improvement over conventional structures with respect to lower contact resistance. Some such embodiments effectively marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.

[0018] Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., such as double-gate and trigate transistor structures), as well as strained and unstrained channel structures. Any number of such structural features and material systems can be used in conjunction with a germanium overlayer as described herein. The transistor structure may include p-type source/drain regions, n-type source/drain regions, or both n-type and p-type source/drain regions. In some example embodiments, the transistor structure includes dopant-implanted source/drain regions or epitaxial (or poly) replacement source/drain regions of silicon, SiGe alloys, or nominally pure germanium films (e.g., such as those with less than 10% silicon) in a MOS structure. In any such implementations, an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions, in accordance with an embodiment of the present invention. A contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts. As will be appreciated, the contact may be implemented as a stack including one or more of a silicide layer, an adhesion layer, and/or a metal pad layer. The boron doped germanium overlayer can be formed directly over other parts of the transistor structure as well, such as the poly gate and/or grounding tap regions, if so desired.

[0019] As is known, a MOS transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. Some embodiments of the present invention are configured with such conventionally formed tip

regions. In other example embodiments, fabrication techniques are employed to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. This can be accomplished, for instance, by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions to form a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer in the source/drain and respective tip regions. The germanium and boron concentrations can vary, but in some example embodiments, the germanium concentration is in the range of 20 atomic % to 100 atomic %, and the boron concentration is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). Note that the boron doped germanium layer may be provided in the tip regions, but in other embodiments is just provided over the source/drain regions (and not in the tip regions).

[0020] In still other example embodiments, an optional thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the underlying substrate with the source/drain layer (e.g., silicon or SiGe). Likewise, a thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the source/drain layer and the boron doped germanium cap. In still other embodiments, the boron doped germanium overlayer or source/drain layer themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the relative suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height.

Architecture and Methodology

[0021] Figure 1A illustrates a MOS device 100A formed on a substrate 102 and configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention. In particular, boron doped germanium layer 117 is provided between the source layer 110 and contact metals 125, and boron doped germanium layer 119 is provided between the drain layer 112 and contact metals 127. The source region 110 and the drain region 112 can be formed using any number of conventional

techniques. In this example embodiment, for instance, the source region 110 and the drain region 112 are formed by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).

[0022] A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104, and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A can be formed. In this example embodiment, the tip regions 110A/112A are formed via a typical implantation-diffusion based process, and overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of, for instance, less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the source/drain regions 110/112. Such implantation-diffusion-based tip formation processes generally do not induce a strain on the channel region.

[0023] In any case, and as will be appreciated in light of this disclosure, whether a transistor structure has a strained or unstrained channel, or source-drain tip regions or no source-drain tip regions, is not particularly relevant to various embodiments of the present invention, and such embodiments are not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types can benefit from employing a boron doped germanium overlayer as described herein. The techniques provided herein are compatible, for instance, with conventional dopant implanted silicon, raised source/drain, strained SiGe (or other suitable materials), and any deposited epitaxial tip (sometimes referred to as source-drain extensions) that extend below the gate electrode dielectric or are spaced away from the vertical line defined by the gate electrode dielectric.

[0024] The germanium overlayer 117/119 is generally provided after formation of the source/drain regions 110/112 and prior to formation of the contacts 125/127. The thickness of

this overlayer 117/119 can vary from one embodiment to the next, but in one example embodiment is in the range of 50 to 250 Angstroms (Å). The boron concentration of overlayer 117/119 can also vary, but in one example embodiment is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., in excess of 2E20 cm^{-3}). The overlayer 117/119 can be selectively deposited over the source/drain 110/112 regions (and/or other regions as desired, such as the poly gate or grounding tap regions). Any number of suitable deposition techniques can be used to provide the overlayer 117/119 (e.g., chemical vapor deposition, molecular beam epitaxy, etc). In accordance with one example embodiment, the contact metals 125 and 127 each comprise a stack a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad, and although any number of contact metal configurations can be used as will be appreciated in light of this disclosure. Standard deposition techniques can be used in providing the contact metals 125/127.

[0025] Figure 1B illustrates an example MOS device 100B formed on a substrate 102 and configured with a boron doped germanium layer 117/119 between the source/drain layer 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. This example configuration includes source and drain epitaxial tips (generally referred to herein as epi-tips). In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are generally referred to as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A. In accordance with one embodiment, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective epitaxial deposition to provide, for instance, an in situ doped silicon, germanium, or SiGe to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown in Figure 1B, although non-raised configurations can be used as well. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0026] Figure 1C illustrates a MOS device 100C formed on a substrate 102 and configured with boron doped germanium layers 117/119 between the respective source/drain layers 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. The source region 110 and the drain region 112 in this example embodiment are formed by implanting dopants such as boron into the substrate. The gate stack 122 is formed over a channel region 120 of the transistor 100C and is this example case does not include sidewalls 108. Nor does this example transistor structure include an undercut or tip regions like the embodiments shown in Figures 1A and 1B. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0027] Numerous other variations and features can be implemented for transistor structures configured in accordance with an embodiment of the present invention. For example, a graded buffer may be used in one or more locations of the structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped SiGe fill in the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the source/drain material. In one such embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium concentration graded from a base level compatible with the underlying substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). The boron concentration within this buffer can be either fixed (e.g., at a high level) or graded, for instance, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}). Note that 'compatibility' as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The

thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Å, such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be further appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

[0028] Alternatively, rather than using a thin buffer between the substrate 102 and the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, the source/drain material itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, boron doped SiGe source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}).

[0029] In other embodiments, a buffer can be provided between the source/drain material and the boron doped germanium overlayer 117/119. In one such embodiment, the source/drain material is a boron doped SiGe layer having a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to the desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, or 3E20 cm^{-3}). Alternatively, rather than using a buffer between the source/drain material and the boron doped germanium overlayer 117/119, the overlayer 117/119 itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped overlayer 117/119 can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate and/or source/drain regions (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %). The boron concentration within this overlayer 117/119 layer can be fixed at a desired high level or can

range, for example, from a base concentration at or otherwise compatible with the underlying substrate and/or source/drain regions up to the desired high level (e.g., in excess of 2E20 cm^{-3}).

[0030] Thus, a low contact resistance architecture for numerous transistor devices is provided. The devices may be formed in part using any number of conventional processes such as, for example, by gate oxide, poly gate electrode, thin spacer, and an isotropic undercut etch in the source/drain regions (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective epitaxial deposition can be used to provide in situ doped silicon or alternatively, a fully strained silicon germanium layer to form source/drain regions with or without tips. Optional buffers may be used as previously explained. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the conventional gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

[0031] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention. Figures 3A through 3I illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments.

[0032] As can be seen, the method begins with forming 202 a gate stack on a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate

stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other suitable gate electrode materials can be used as well. The gate electrode material, which is may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A. As can be seen, Figure 3A illustrates a substrate 300 upon which a gate stack is formed. In this example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode 304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask

materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials. Figure 3A further illustrates spacers 310 formed on either side of the stack. The spacers 310 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers 310 may generally be chosen based on design requirements for the transistor being formed. In accordance with some embodiments, however, the width of the spacers 310 is not subject to design constraints imposed by the formation of the source and drain epi-tips, given sufficiently high boron doped germanium content in the source/drain tip regions, as described herein (boron won't diffuse into channel).

[0033] With further reference to Figure 2, after the gate stack is formed, the method continues with defining 204 the source/drain regions of the transistor structure. As previously explained, the source/drain regions can be implemented with any number of suitable processes and configurations. For example, the source/drain regions may be implanted, etched and epi filled, raised, silicon or SiGe alloy, p-type and/or n-type, and have a planar or fin shaped diffusion region. In the example embodiment shown in Figure 3A, substrate 300 has been etched to provide cavities 312/314 as well as respective tip areas 312A/314A which undercuts the gate dielectric 302. Figure 3B illustrates the substrate 300 after cavities 312/314 and tip areas 312A/314A have been filled to provide the source/drain regions 318/320 and tip regions 318A/320A. In accordance with some example embodiments, the source and drain region cavities 312/314 along with their respective tip areas 312A/314A are filled with in situ doped silicon or SiGe, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A). Any number of source/drain layer configurations can be used here, with respect to materials (e.g., silicon, SiGe, III-V materials), dopant (e.g., boron in excess of 2E21 cm^{-3}, or other suitable dopant/concentration), and dimension (e.g., thickness of source/drain layer may range, for instance, from 50 to 500 nm so as to provide a flush or raised source/drain region).

[0034] As previously explained, some such embodiments may include with a thin buffer between the source/drain layer and the substrate or the source/drain and boron doped germanium overlayer. For instance, and as can further be seen in the example embodiment shown in Figure 3B, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the source/drain materials. In some embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration

compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The boron concentration can be appropriately graded as well. Numerous buffer schemes will be apparent in light of this disclosure.

[0035] With further reference to Figure 2, after the source/drain regions are defined, the method continues with depositing 206 boron doped germanium on the source/drain regions of the transistor structure. Figure 3C shows the boron doped germanium layer 317/319. In some example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, …, or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %). The boron concentration in some such embodiments can be in excess of 1E20 cm^{-3}, such as higher than 2E20 cm^{-3} or 2E21 cm^{-3}, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of 1E20 cm^{-3} or 2E20 cm^{-3} or 3E20 cm^{-3}, …, 2E21 cm^{-3}). In embodiments where the germanium concentration of the underlying source/drain regions 318/320 is fixed or otherwise relatively low, a graded buffer may be used to better interface source/drain regions 318/320 with the boron doped germanium layer 317/319, as previously explained. The thickness of the boron doped germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 Å, in accordance with some specific example embodiments, although alternative embodiments may have other layer thicknesses, as will be apparent in light of this disclosure.

[0036] In some embodiments, a CVD process or other suitable deposition technique may be used for the depositing 206 or otherwise forming the boron doped germanium layer 317/319. For example, the depositing 206 may be carried out in a CVD, or rapid thermal CVD (RT-CVD), or low pressure CVD (LP-CVD), or ultra-high vacuum CVD (UHV-CVD), or gas source molecular beam epitaxy (GS-MBE) tool using germanium and boron containing precursors such as germane (GeH_4) or digermane (Ge_2H_6) and diborane (B_2H_6) or boron difluoride (BF_2). In some such embodiments, there may be a carrier gas such as, for instance, hydrogen, nitrogen, or a noble gas (e.g., precursor is diluted at 1-5% concentration of carrier gas). There may also be an etchant gas such as, for example, halogen-based gas such as hydrogen chloride (HCl), chlorine

(Cl), or, hydrogen bromide (HBr). The basic deposition of germanium and also boron doped germanium is possible over a wide range of conditions using deposition temperature in the range, for example, of 300°C to 800°C (e.g., 300-500°C) and reactor pressure, for instance, in the range 1 Torr to 760 Torr. Germanium is naturally selective in that it deposits on silicon or silicon-germanium alloy, and does not deposit on other materials such as silicon dioxide and silicon nitride. Since this natural selectivity is not entirely perfect, a small flow of etchant can be used to increase the selectivity of the deposition, as previously noted. Each of the carrier and etchants can have a flow in the range of 10 and 300 SCCM (typically, no more than 100 SCCM of flow is required, but some embodiments may require higher flow rates). In one specific example embodiment, the deposition 206 is carried out using GeH_4 that is diluted in hydrogen at a 1% concentration and at a flow rate that ranges between 100 and 1000 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 3% concentration and at a flow rate that ranges between 100 and 600 SCCM. In some such specific example cases, an etching agent of HCl or Cl_2 is added at a flow rate that ranges, for example, between 10 and 100 SCCM, to increase the selectivity of the deposition.

[0037] As will be appreciated in light of this disclosure, the selectivity at which the boron doped germanium layer 317/319 is deposited can vary as desired. In some cases, for instance, the boron doped germanium layer 317/319 is deposited only on the source/drain regions 318/320 or a portion of the source/drain regions 318/320 (rather than across the entire structure). Any number of masking/patterning techniques can be used to selectively deposit layer 317/319. Moreover, other embodiments may benefit from layer 317/319 covering, for example, poly gate regions or grounding tap regions. As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 90 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of 2E20 cm^{-3}) can be used to realize significantly lower contact resistance in the source and drain regions (and other areas where low contact resistance is desirable, such as ground tap regions), in accordance with some example embodiments. Further, and as previously explained, since boron diffusion is sufficiently suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite any high boron concentration proximate the channel (if applicable). Barrier height lowering is also enabled from the higher concentration of germanium at the contact

surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

[0038] With further reference to Figure 2, after the boron doped germanium layer 317/319 is provided, the method continues with depositing 208 a dielectric over layer 317/319. Figure 3D shows dielectric 322 as being flush with the hard mask 306 of the gate stack, but it need not be. The dielectric can be configured in a number of ways. In some embodiments, dielectric 322 is implemented with silicon dioxide (SiO_2) or other low-k dielectric materials. In other embodiments, dielectric 322 is implemented with a silicon nitride (SiN) liner followed by one or more layers of SiO_2, or any combination of nitride, oxide, oxynitride, carbide, oxycarbide, or other suitable dielectric materials). The dielectric 322, which may be referred to as an interlayer dielectric (ILD), may be planarized as commonly done. Other example dielectric materials include, for instance, carbon doped oxide (CDO), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant.

[0039] Next, in some embodiments of the present invention where a replacement metal gate (RMG) process is used and as best shown in Figure 3E, the method may further include removing the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 and hard mask layer 306 are removed. Figure 3E illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing a new gate dielectric layer into the trench opening (designated as 324 in Figure 3F). Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material. As further shown in Figure 3F, the method may further continue with depositing the metal gate electrode layer 326 into the trench and over the gate dielectric layer 324. Conventional metal deposition processes may be used to form the metal gate

electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a P-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited in the gate trench followed by a suitable metal gate electrode fill metal such as aluminum or silver.

[0040] With further reference to Figure 2, after dielectric layer 322 is provided over layer 317/319 (and any desired RMG process), the method continues with etching 210 to form the source/drain contact trenches. Any suitable dry and/or wet etch processes can be used. Figure 3G shows the source/drain contact trenches after etching is complete, in accordance with one example embodiment. The method then continues with depositing 212 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 214 the source/drain contact plugs. Figure 3H shows the contact metals 325/327, which in some embodiments includes the silicide/germanide, although other embodiments may include additional layers (e.g., adhesion layer). Figure 3I shows the contact plug metal 329/331, which in some embodiments includes aluminum, although any suitably conductive contact metal or alloy can be used for the contact plug 329/331, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. The germanide/metalization 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants to form a low resistance germanide. The boron doped germanium layer 317/319 allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit R_{ext} values of about 140 Ohm*um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS devices (e.g., about a 2x improvement or better, such as a R_{ext} of about 70 Ohm*um), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with

boron doped germanium cap 317/319 in accordance with an embodiment of the present, with a boron concentration in excess of 1E20 cm^{-3} and a germanium concentration in excess of 90 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain regions 318/320 and the contact metals 325/327, can exhibit R_{ext} values of less than 100 Ohm*um, and in some cases less than 90 Ohm*um, and in some cases less than 80 Ohm*um, and in some cases less than 75 Ohm*um, or lower.

[0041] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention. Figures 5A through 5F illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments. In general, this method is similar to the method described with reference to Figures 2 and 3A-H, except that the deposition of the boron doped germanium layer 317/319 on the source/drain regions is carried out after the dielectric 322 is deposited and etched to form the contact trench. Thus, the method includes depositing 406 the dielectric 322 directly over the source/drain regions 318/320, and then continues with etching 408 to form the source/drain contact trench and then selectively deposting 410 the boron doped germanium layer 317/319 into the trench (and directly onto the source/drain regions 318/320), as best shown in Figures 5C through 5E. Deposting 410 can be carried out using any suitable deposition process, such as selective epitaxy. Once layer 317/319 is provided, the contact metals 325/327 can be provided on top of the layer 317/319, as shown in Figure 5F. This alternate methodology provides the same benefit of improved contact resistance, but is more selective in where the boron doped germanium is deposited. Other such selective deposition processes will be apparent in light of this disclosure, using any suitable combination of masking/patterning and selective deposition techniques.

[0042] As will be further appreciated, the previous relevant discussion with respect to similar parts of the method is equally applicable here. In particular, forming 402 a gate stack and defining 404 the source/drain regions of the transistor structure can be carried as previously discussed with reference to the forming 202 and defining 204 previously discussed with reference to Figure 2. Likewise, depositing 412 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 414 the source/drain contact plugs can be carried as previously discussed with reference to the forming 212 and defining 214 previously discussed with reference to Figure 2.

FinFET Configuration

[0043] As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

[0044] Figure 6 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620. A gate electrode 640 is formed over 3 surfaces of the fin 660 to form 3 gates. A hard mask 690 is formed on top of the gate electrode 640. Gate spacers 670, 680 are formed at opposite sidewalls of the gate electrode 640.

[0045] A source region comprises the epitaxial region 631 formed on a recessed source interface 650 and on one fin 660 sidewall, and a drain region comprises the epitaxial region 631 formed on a recessed source interface 650 and on the opposing fin 660 sidewall (not shown). A cap layer 641 is deposited over the epitaxial regions 631. Note that the boron cap layer 641 may be provided in the recessed (tip) regions, but in other embodiments is just provided over the source/drain regions (and not in the recessed regions). In one embodiment, the isolation regions 610, 620 are shallow trench isolation (STI) regions formed using conventional techniques, such as etching the substrate 600 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 610, 620 can be made from any suitable dielectric/insulative material, such as SiO_2. The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 600 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

[0046] As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the FinFET transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 631 and cap layer 641 can be implemented, for instance, using an in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641), with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer may be used to transition from a base level germanium/boron concentration compatible with the epitaxial region 631 to the boron doped germanium cap 641. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 631 and/or the cap 641, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 660.

[0047] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap. The transistor structures associated with the high resistance numbers in excess of 0.18 are all implemented with standard SiGe alloy raised PMOS source/drain regions with contact metal deposited directly thereon. The transistor structures associated with the resistance numbers of 0.107 and lower are all similarly implemented but with the addition a boron doped germanium cap between the source/drain regions and contact metal, in accordance with various embodiments of the present invention. Table 1 shows the raw data quantiles resulting from testing of the example structures with and without a boron doped germanium cap as described herein.

Ge Cap	Min	10%	25%	Median	75%	90%	Max
Yes	0.032	0.032	0.033	0.040	0.078	0.105	0.107
No	0.183	0.183	0.192	0.239	0.250	0.265	0.265

Table 1

As can be seen, this example lot actually shows an improvement (reduction) in contact resistance of about a three to six times (3X to 6X) over conventional transistor structures. The units are Ohms per arbitrary area.

[0048] Other improvements enabled by using a boron doped germanium cap in accordance with an embodiment of the present invention will be apparent in light of this disclosure. In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2x R_{ext} improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

Example System

[0049] Figure 8 illustrates a computing device 1000 configured in accordance with one embodiment of the invention. As can be seen, the computing device 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of device 1000, etc. Depending on its applications, computing device 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing device 1000 may include one or more transistor structures as described herein. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

[0050] The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0051] The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes an onboard non-volatile memory or cache, and/or is otherwise communicatively coupled to off-chip memory that is implemented with one or more transistor structures as described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0052] The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more devices implemented with one or more transistor structures as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or

communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

[0053] In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the device 1000 may be any other electronic device that processes data or employs transistors.

[0054] Numerous embodiments will be apparent in light of this disclosure, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region, and a gate electrode above the channel region. A gate dielectric layer is provided between the gate electrode and the channel region, and source and drain regions are provided in the substrate and adjacent to the channel region. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions. This boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. In one such example, the device is one of a planar or FinFET transistor. In another example case, the device comprises a PMOS transistor. In another example case, the device further includes an interlayer dielectric. In another example case, the device further includes a graded buffer between the substrate and the source and drain regions and/or a graded buffer between the source and drain regions and the boron doped germanium layer. In one such case, the graded buffer between the source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %. In one such specific example case, the high concentration reflects pure germanium. In another example case, the graded buffer between the source and drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and

drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %. In another example case, the source and drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another example case, the source and drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}. Another embodiment provides an electronic device that includes a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as variously defined in in this paragraph. In one such case, the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices. In another such case, the device is a computing device (e.g., mobile telephone or smartphone, laptop, tablet computer, etc).

[0055] Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region, and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. The

device is one of a planar or FinFET transistor. In one such example case, the device further includes a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %. In another example case, the source and drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In another example case, the source and drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms. Another embodiment provides a computing device (e.g., desktop or portable computer, etc) that includes a printed circuit board having a communication chip and/or a processor, wherein at least one of the communication chip and/or processor comprises one or more transistor devices as variously defined in this paragraph.

[0056] Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region. The method continues with providing source and drain regions in the substrate and adjacent to the channel region, and providing a boron doped germanium layer on at least a portion of the source and drain regions. The boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron

concentration in excess of 1E20 cm^{-3}. The method continues with providing metal-germanide source and drain contacts on the boron doped germanium layer. In some example such cases, the method further includes providing a graded buffer between the substrate and the source and drain regions, and/or providing a graded buffer between the source and drain regions and the boron doped germanium layer. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron (which may be used with or without graded buffers). This method may be employed, for example, in the fabrication of any electronic devices such as a computing device.

[0057] The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. An integrated circuit including at least one transistor device, the integrated circuit comprising:

a fin including a first region;

a second region and a third region, the first region being between the second region and the third region;

a gate electrode above the first region, the first region between two portions of the gate electrode, the gate electrode including one or more metals;

a gate dielectric between the gate electrode and the first region;

a first spacer structure and a second spacer structure adjacent opposite sidewalls of the gate electrode, the first and second spacer structures including one or more dielectrics;

a first cap structure on and above at least a portion of the second region, the first cap structure comprising a germanium concentration in excess of 50 atomic %, wherein the first cap structure does not extend under the gate dielectric;

a second cap structure on and above at least a portion of the third region, the second cap structure comprising a germanium concentration in excess of 50 atomic %, wherein the second cap structure does not extend under the gate dielectric;

a first contact structure on and above the first cap structure, the first contact structure including one or more metals, the first contact structure further including germanium; and

a second contact structure on and above the second cap structure, the second contact structure including one or more metals, the second contact structure further including germanium.

2. The integrated circuit of claim 1, wherein the second and third regions comprise at least one of silicon and germanium.

3. The integrated circuit of claim 1, further comprising a substrate comprising silicon, wherein and the fin is part of the substrate, and the first and second regions comprise silicon and germanium.

4. The integrated circuit of claim 1, wherein the second and third regions at least one of:

extend above a topmost portion of the fin;

include a tip region that extends under a corresponding one of the spacer structures; or

include a tip region that extends under the gate dielectric.

5. An integrated circuit including at least one transistor device, the integrated circuit comprising:

a fin including a first region;

a source region and a drain region at least one of on or in the fin, such that the first region is between the source and drain regions, the source and drain regions including semiconductor material and p-type dopant;

a gate electrode at least above the first region;

a gate dielectric between the gate electrode and the first region;

a first gate spacer and a second gate spacer adjacent opposite sidewalls of the gate electrode, the first and second gate spacers including dielectric material;

a first cap structure on and above at least a portion of the source region, the first cap structure not present under the gate dielectric, the first cap structure comprising a germanium concentration in excess of 50 atomic %, wherein there is no overlap between the first cap structure and the gate dielectric;

a second cap structure on and above at least a portion of the drain region, the second cap structure not present under the gate dielectric, the second cap structure comprising a germanium concentration in excess of 50 atomic %,

wherein there is no overlap between the second cap structure and the gate dielectric;

a first contact on and above the first cap structure, the first contact including metal-germanide; and

a second contact on and above the second cap structure, the second contact including metal-germanide.

6. The integrated circuit of claim 5, wherein the source and drain regions comprise at least one of silicon and germanium.

7. The integrated circuit of claim 5, further comprising a substrate, wherein the substrate is single crystal silicon and the fin is part of the substrate, and the source and drain regions comprise silicon and germanium and are within a faceted recess.

8. The integrated circuit of claim 5, wherein the source and drain regions at least one of:

extend above a topmost portion of the fin;

include a tip region that extends under a corresponding one of the gate spacers; or

include a tip region that extends under the gate dielectric.

9. An integrated circuit including at least one transistor device, the integrated circuit comprising:

a fin including a first region;

a source region and a drain region at least one of on or in the fin, such that the first region is between the source and drain regions, the source and drain regions including semiconductor material and p-type dopant;

a gate electrode at least above the first region;

a gate dielectric between the gate electrode and the first region;

a first gate spacer and a second gate spacer adjacent opposite sidewalls of the gate electrode, the first and second gate spacers including dielectric material;

a first cap structure on and above at least a portion of the source region, the first cap structure not present under the gate dielectric, the first cap structure

comprising a germanium concentration in excess of 50 atomic %, wherein there is no overlap between the first cap structure and the gate dielectric; and

a second cap structure on and above at least a portion of the drain region, the second cap structure not present under the gate dielectric, the second cap structure comprising a germanium concentration in excess of 50 atomic %, wherein there is no overlap between the second cap structure and the gate dielectric.

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

ABSTRACT OF THE DISCLOSURE

Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

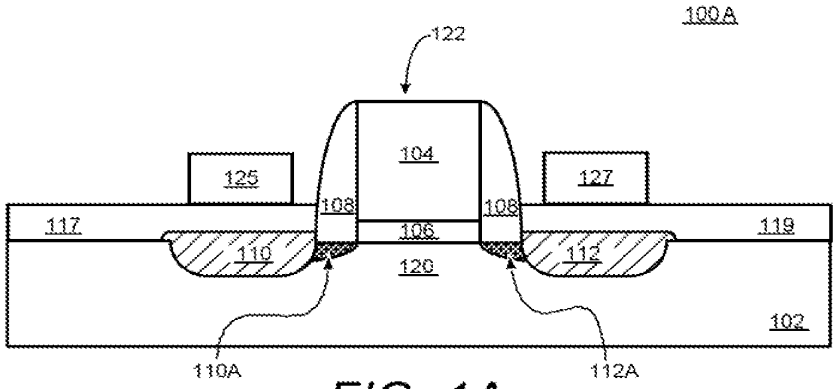


FIG. 1A

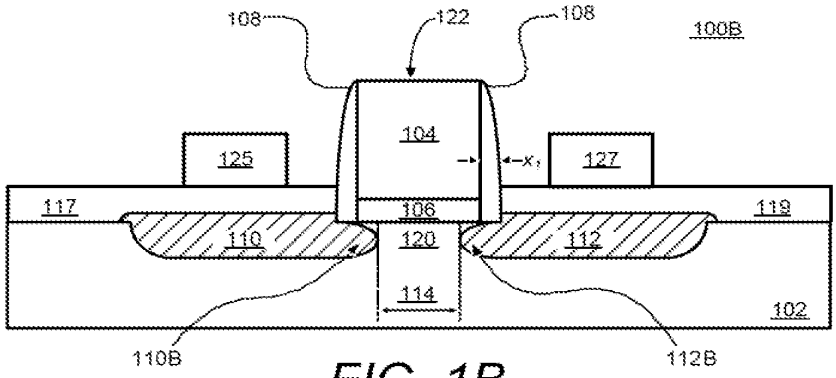


FIG. 1B

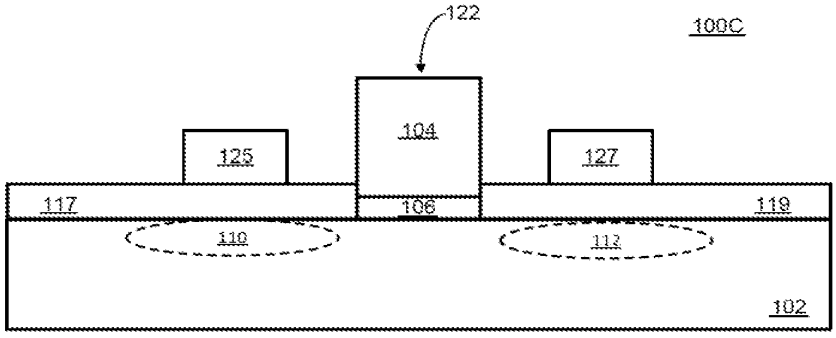


FIG. 1C

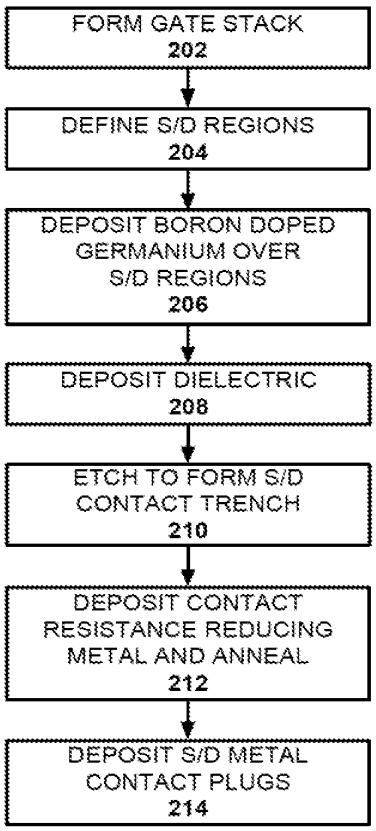

FORM GATE STACK
202
DEFINE S/D REGIONS
204
DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
206
DEPOSIT DIELECTRIC
208
ETCH TO FORM S/D CONTACT TRENCH
210
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
212
DEPOSIT S/D METAL CONTACT PLUGS
214

FIG. 2

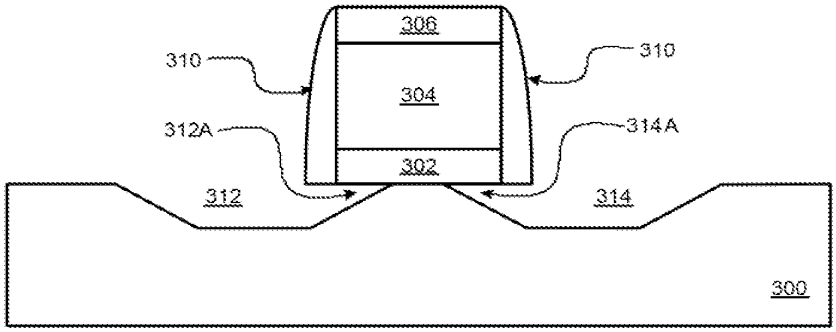


FIG. 3A

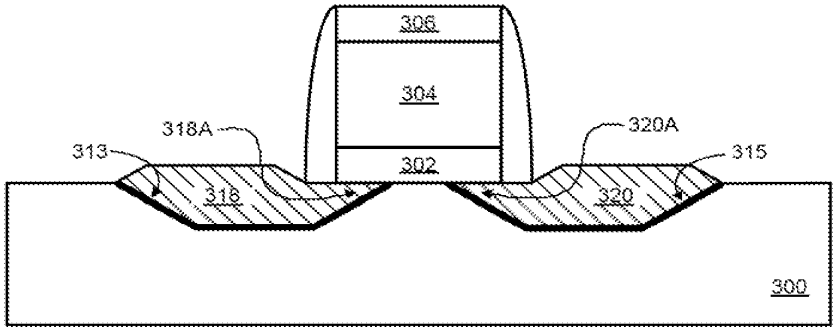


FIG. 3B

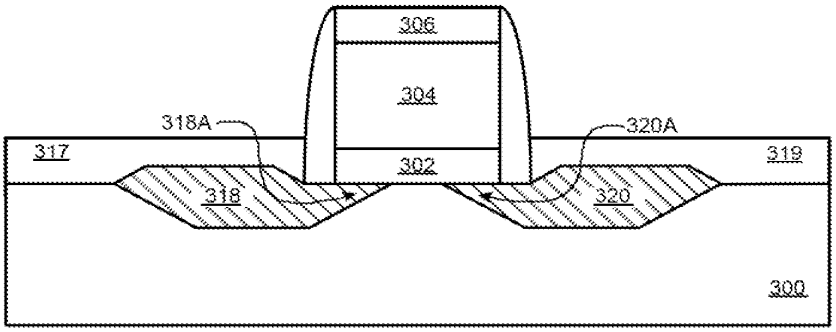


FIG. 3C

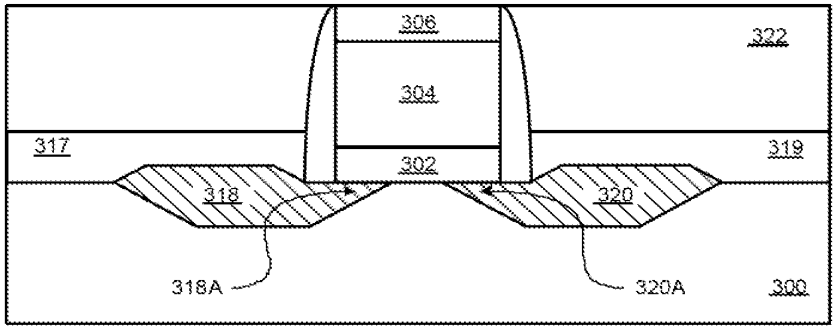


FIG. 3D

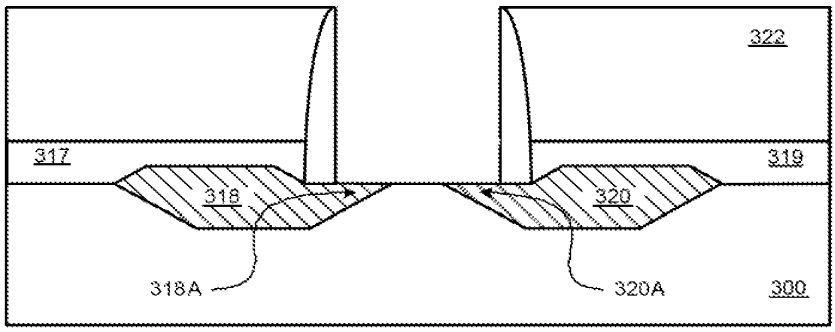


FIG. 3E

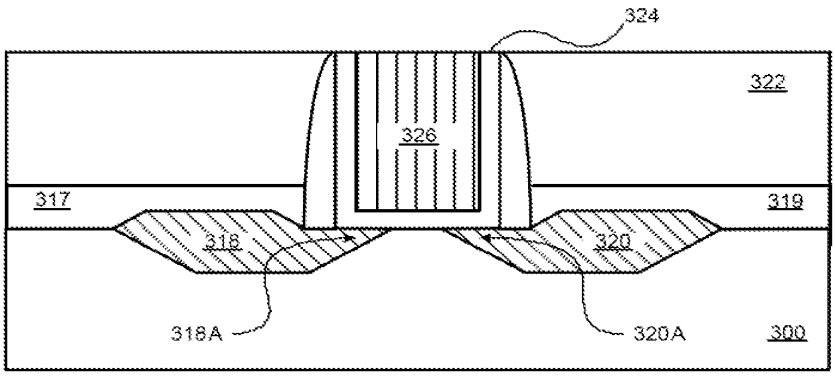


FIG. 3F

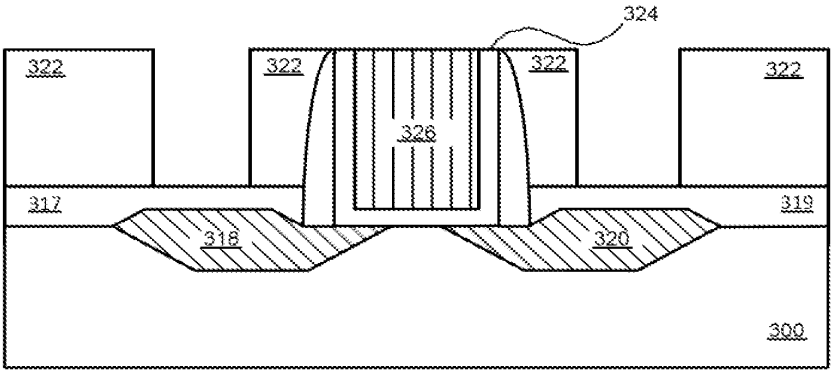


FIG. 3G

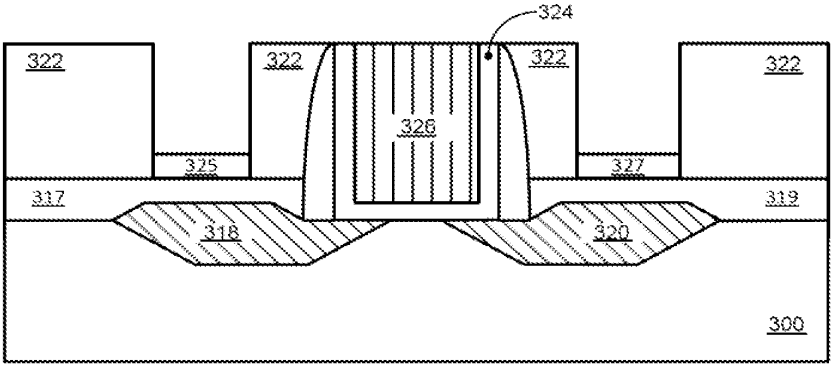


FIG. 3H

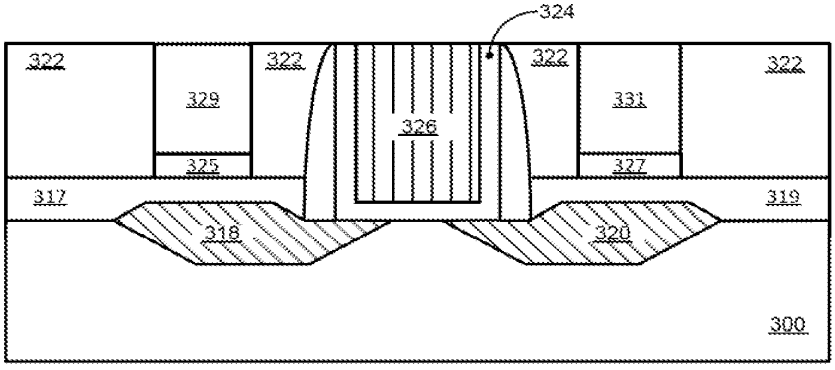


FIG. 3I

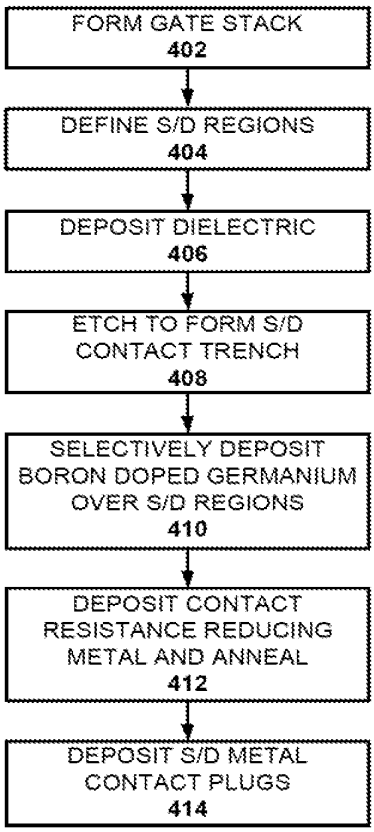

FORM GATE STACK
402
DEFINE S/D REGIONS
404
DEPOSIT DIELECTRIC
406
ETCH TO FORM S/D CONTACT TRENCH
408
SELECTIVELY DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
410
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
412
DEPOSIT S/D METAL CONTACT PLUGS
414

FIG. 4

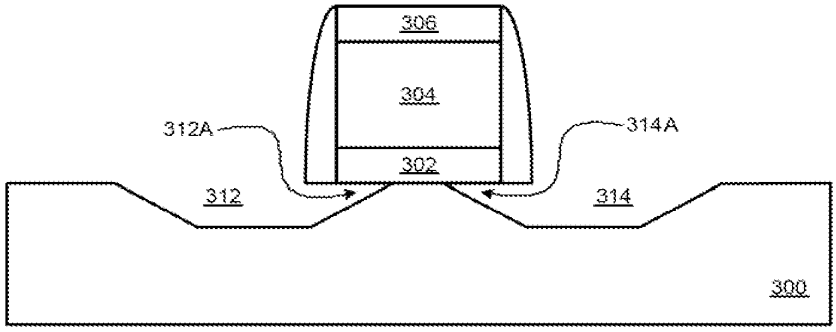


FIG. 5A

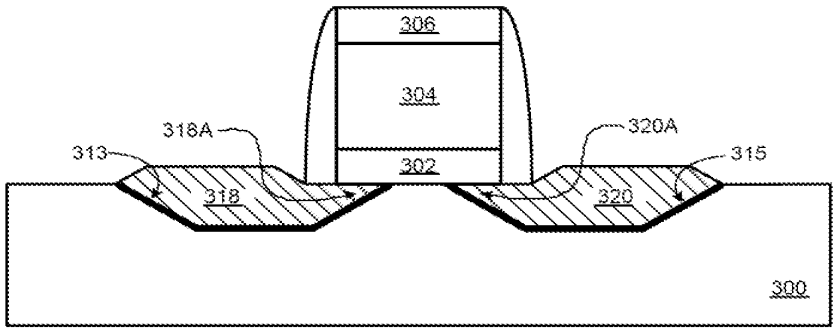


FIG. 5B

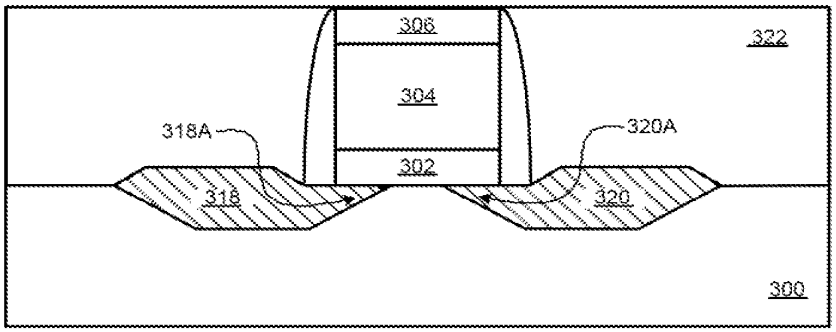


FIG. 5C

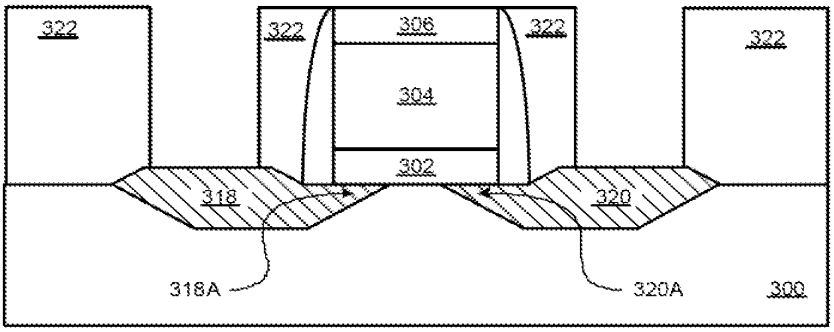


FIG. 5D

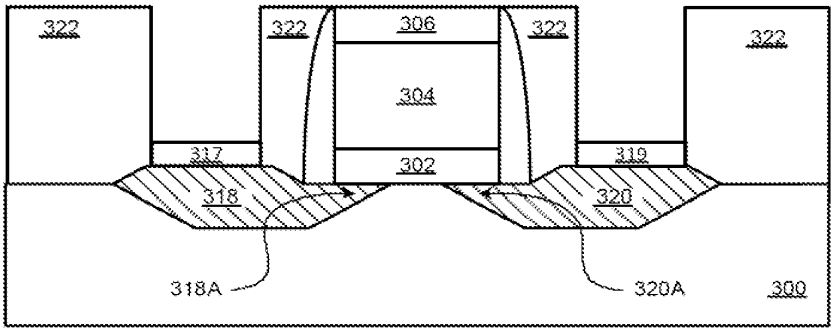


FIG. 5E

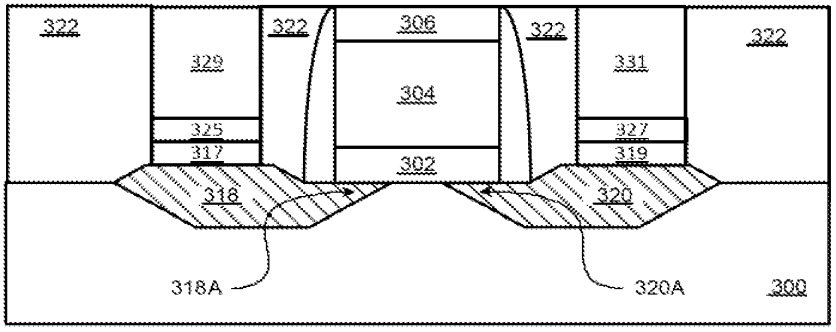


FIG. 5F

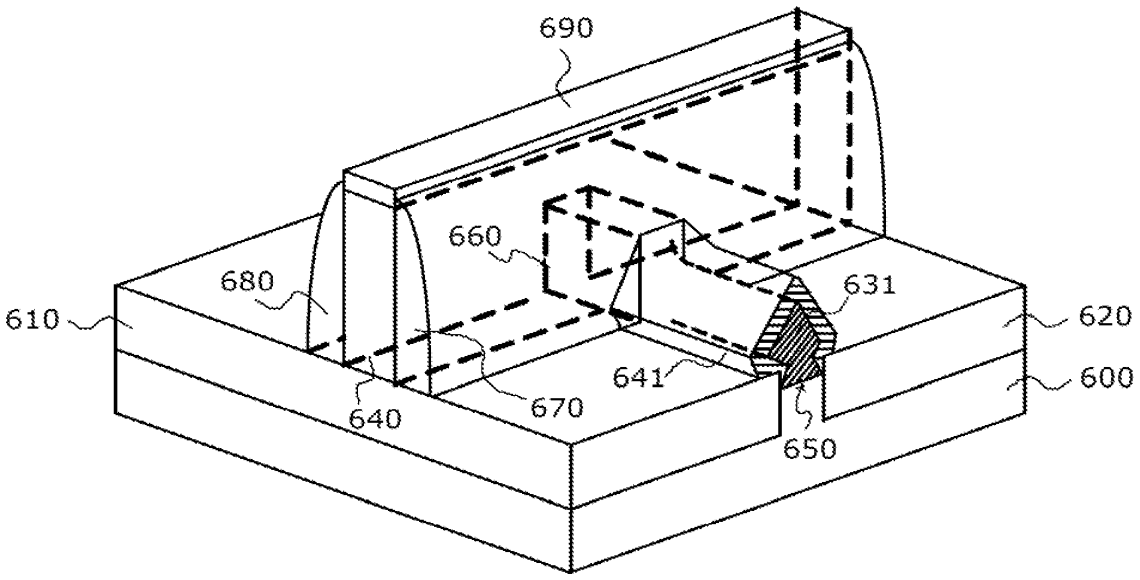


FIG. 6

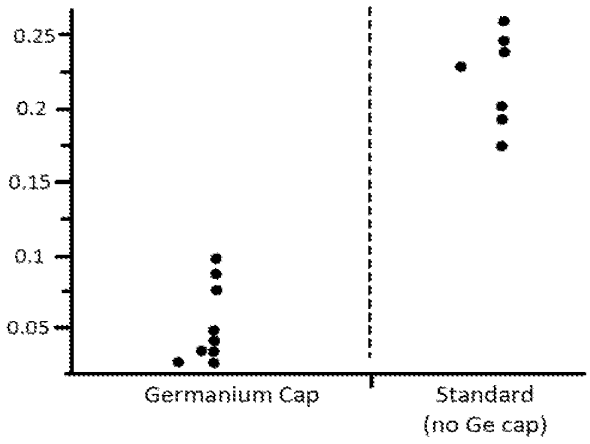


FIG. 7

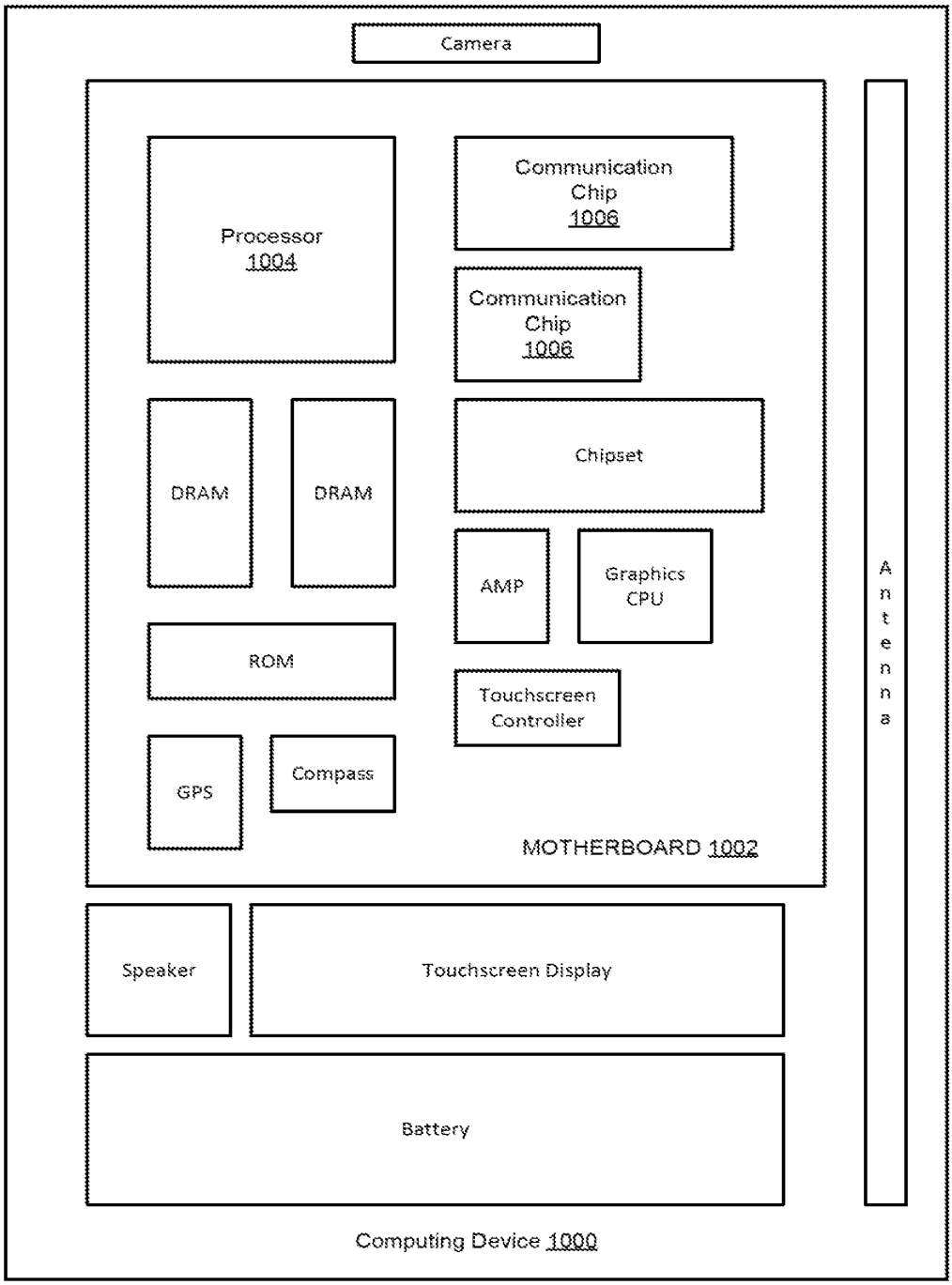

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 8

Electronic Acknowledgement Receipt

EFS ID:	36054382
Application Number:	16416445
International Application Number:	
Confirmation Number:	5347
Title of Invention:	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
First Named Inventor/Applicant Name:	GLENN A. GLASS
Customer Number:	99256
Filer:	Paul A. Smith/Lisa Underhilll
Filer Authorized By:	Paul A. Smith
Attorney Docket Number:	P38507USC2-C1
Receipt Date:	20-MAY-2019
Filing Date:	
Time Stamp:	11:50:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	P38507USC2-C1-ADS.pdf	1256610 280fb7226bda7172a008230d5a609bd95986e83e	no	9

Warnings:

Information:					
2	Oath or Declaration filed	P38507USC2-C1_Fully_Executed_Declaration_.pdf	1463377 3083c1275816f91b3af0129724023cef3ba8cdd2	no	3
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Information:					
3		P38507USC2C1_Patent_App_.pdf	254159 88b6e2f8e30da87e21ea6b56525b4da43943e254	yes	30
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4	Drawings-only black and white line drawings	P38507USC2-C1_Drawings.pdf	834128 e2c65a5e494bbefe039bf9df528a28ae0a079b17	no	11
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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.