

PUBLIC EXHIBIT 48

U.S. Patent No. 11,251,281

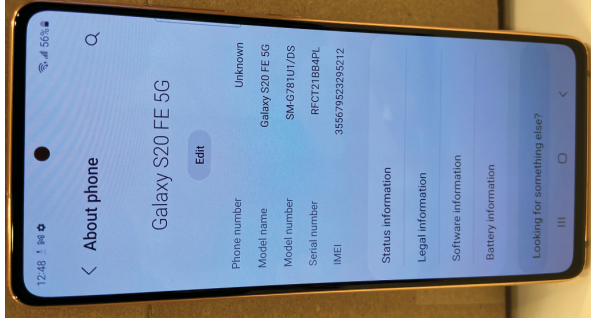
Samsung/TSMC Product (7nm node)

Claim 1(pre): “An integrated circuit structure, comprising:”

1(pre). An integrated circuit structure, comprising:

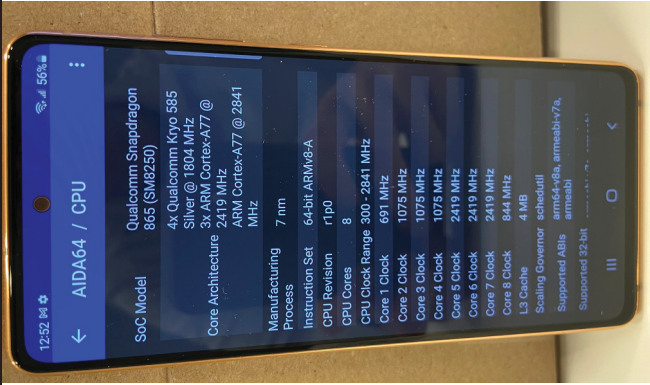
The Samsung S20 FE 5G smartphone (hereinafter, the “Samsung/TSMC Product”) includes an integrated circuit structure.

For example, the Samsung/TSMC Product includes the Qualcomm Snapdragon 865 5G system on chip (hereinafter, the “Qualcomm SoC”).

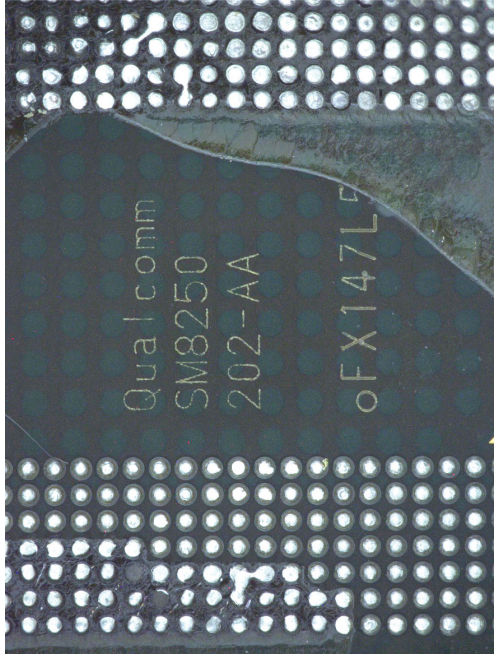


See Ex. 20 at 7, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - About Phone.

U.S. Patent No. 11,251,281: Claim 1(pre)
“An integrated circuit structure, comprising:”



See Ex. 20 at 8, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - SoC Model.



See Ex. 20 at 9, Photographs for the TSMC Representative Article.

The Qualcomm SoC is manufactured using TSMC's 7nm technology node.

U.S. Patent No. 11,251,281: Claim 1(pre)
“An integrated circuit structure, comprising:”

Process

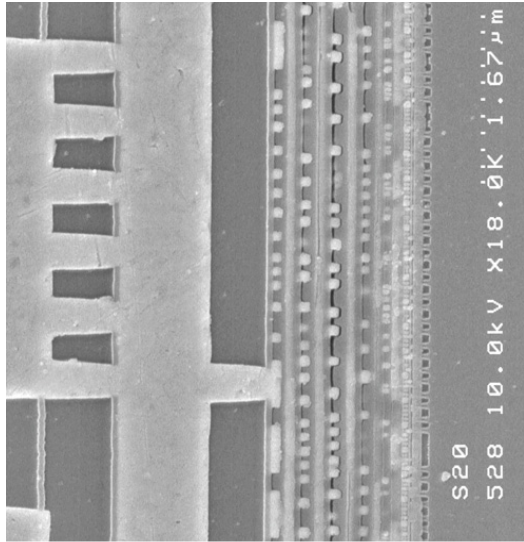
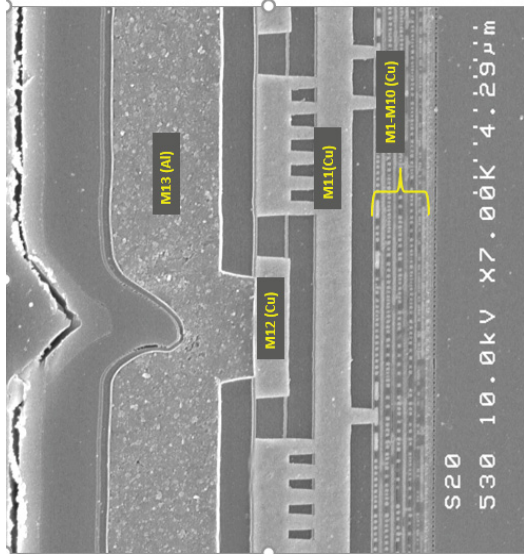
Process Node and Technology: 7 nm

See Ex. 88 at 8, Qualcomm Snapdragon 865 5G Mobile Platform,
<https://www.qualcomm.com/products/snapdragon-865-5g-mobile-platform>.

The Snapdragon 865 Application Processor: TSMC 7nm N7P

With the elephant in the room of the modem configuration being out of the way, we come to the actual Snapdragon 865 application processor.

See Ex. 89 at 4, Qualcomm Announces Snapdragon 865 and 765(G),
<https://www.anandtech.com/show/15178/qualcomm-announces-snapdragon-865-and-765-5g-for-all-in-2020-all-the-details>.



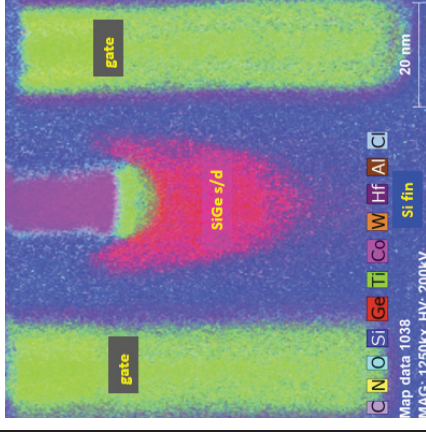
See Ex. 20 at 10 (left) (annotated), 11, Photographs for the TSMC Representative Article.

Claim 1(a) “a fin comprising silicon;”

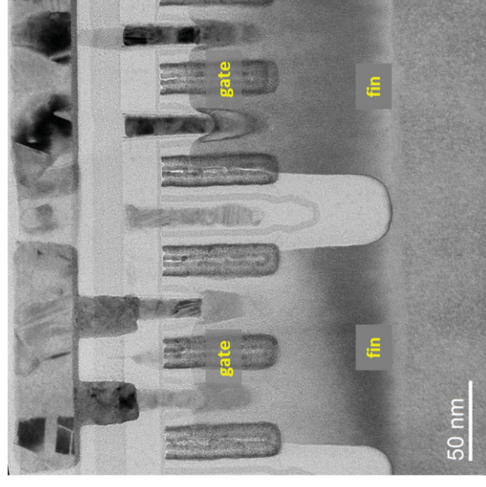
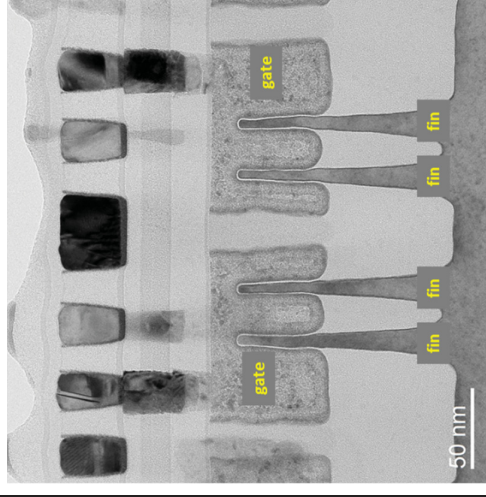
1(a). a fin comprising silicon;

The Samsung/TSMC Product includes a fin comprising silicon.

For example, the Qualcomm SoC includes multiple PMOS transistors that include a silicon fin.



See Ex. 20 at 12, Photographs for the TSMC Representative Article (annotated).

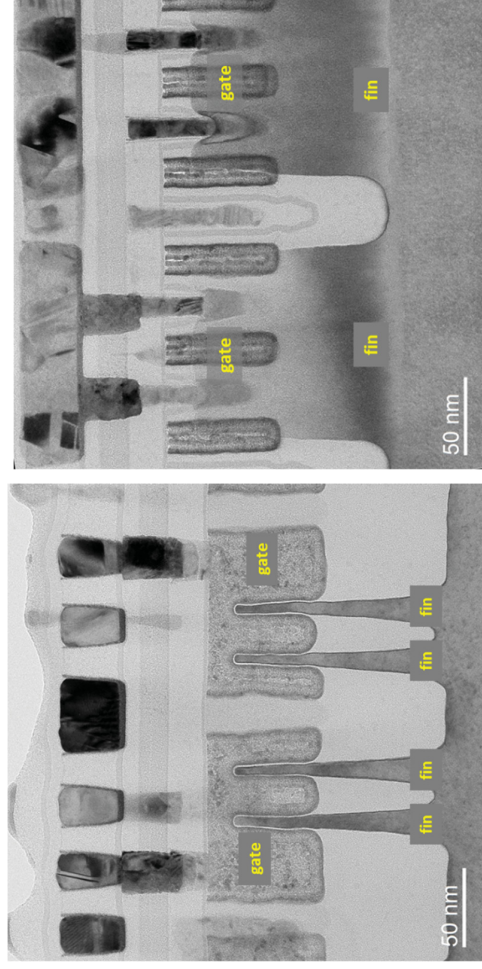


See Ex. 20 at 13 (left) (annotated), 14 (right) (annotated), Photographs for the TSMC Representative Article.

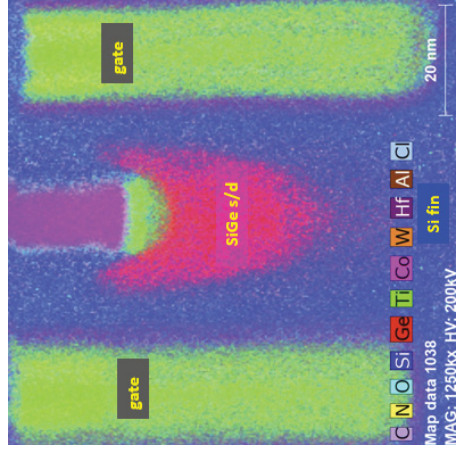
Claim 1(b): “a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side; a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

the gate electrode having a first side, and the gate electrode having a second side opposite the first side; and the gate electrode having a second side opposite the first side.”

For example, the Qualcomm SoC includes a gate electrode over the fin.



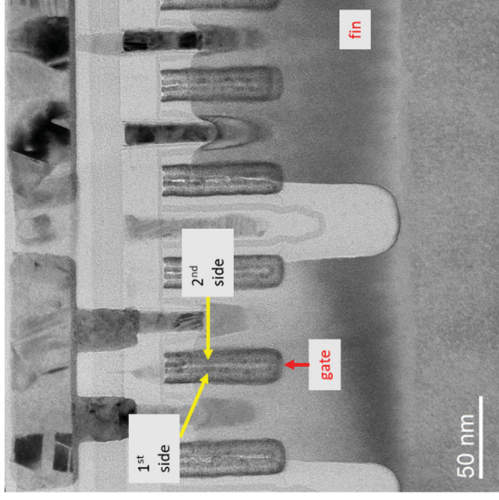
See Ex. 20 at 13 (left) (annotated), 14 (right) (annotated), Photographs for the TSMC Representative Article.



See Ex. 20 at 12, Photographs for the TSMC Representative Article (annotated).

Further the gate electrode has a first side and a second side, the second side being opposite the first side.

“a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;”

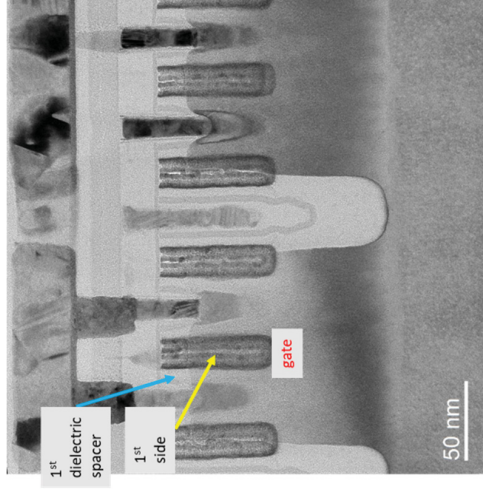


See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).

Claim 1(c): “a first dielectric spacer along the first side of the gate electrode;”

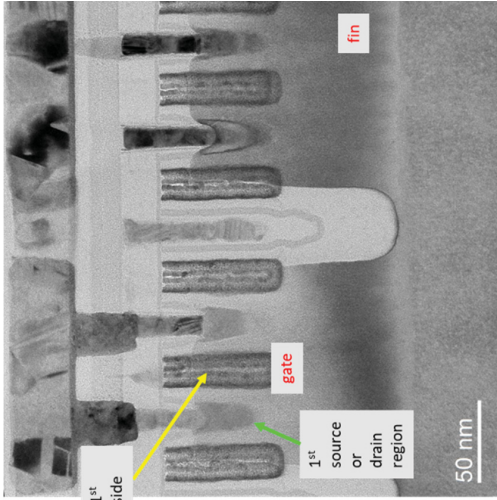
1(c). a first dielectric spacer along the first side of the gate electrode;

The Samsung/TSMC Product includes a first dielectric spacer along the first side of the gate electrode. For example, the Qualcomm SoC has a first dielectric spacer is along the first side of the gate electrode.

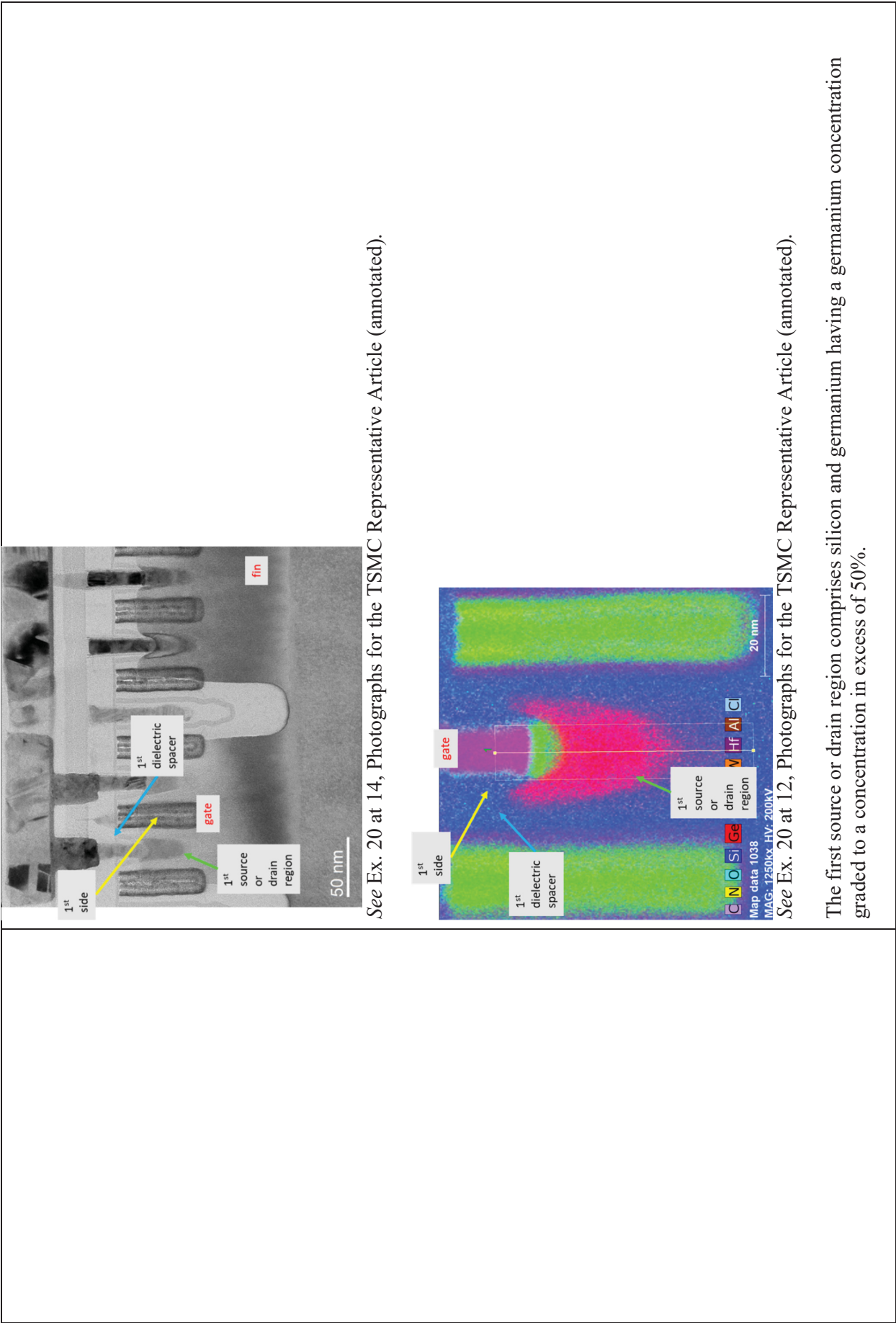


See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).

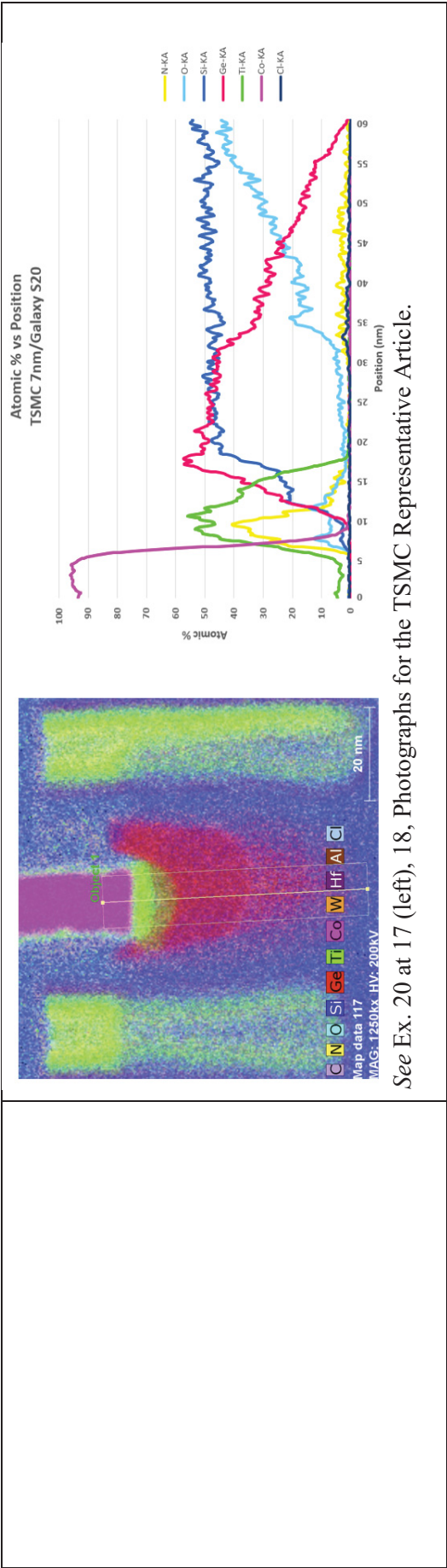
Claim 1(d): “a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%,”

1(d). a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;	The Samsung/TSMC Product includes a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%. For example, the Qualcomm SoC includes a first source or drain region in the fin proximate a first side of the gate electrode. For example, the Qualcomm SoC includes a source/drain region in the fin proximate to a first side of the gate electrode.  See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated). Further, for example, a portion of the first source or drain region is beneath the first dielectric spacer.
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“a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;”



“a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;”

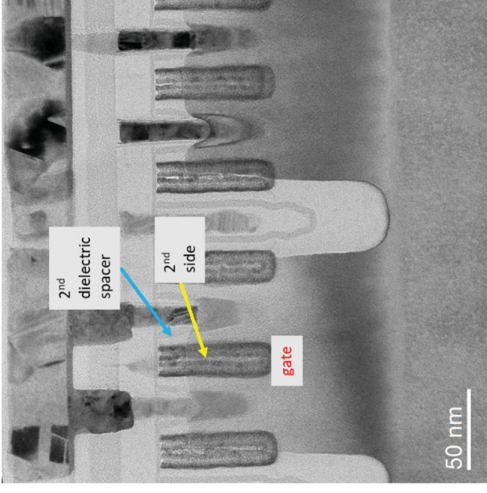


See Ex. 20 at 17 (left), 18, Photographs for the TSMC Representative Article.

Claim 1(e): "a second dielectric spacer along the second side of the gate electrode;

Claim 1(e): "a second dielectric spacer along the second side of the gate electrode;"

The Samsung/TSMC Product includes a second dielectric spacer along the second side of the gate electrode. For example, the Qualcomm SoC has a second dielectric spacer is along the second side of the gate electrode.



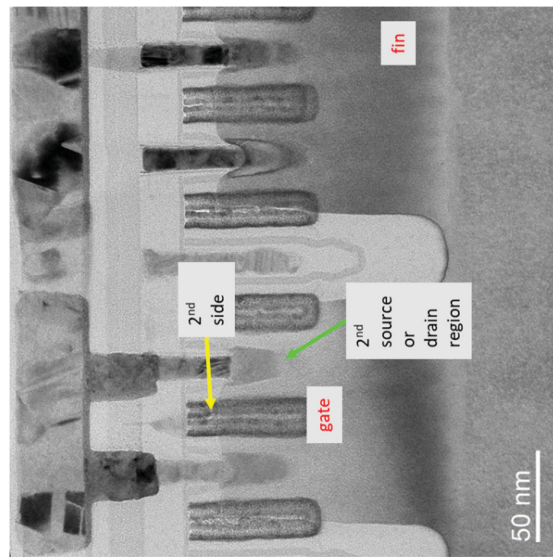
See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).

Claim 1(f): “a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%,”

1(f). a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

The Samsung/TSMC Product includes a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.

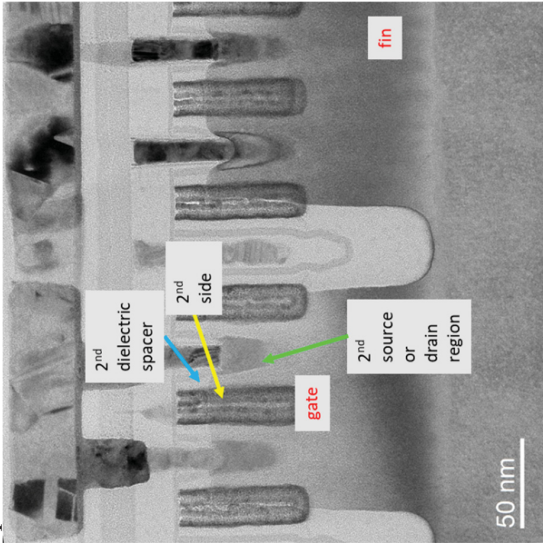
For example, the Qualcomm SoC includes a second source or drain region in the fin proximate a second side of the gate electrode. For example, the Qualcomm SoC includes a source/drain region in the fin proximate to a second side of the gate electrode.



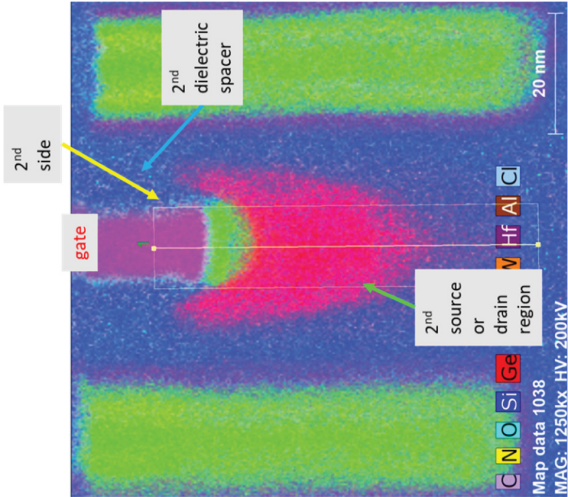
See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).

U.S. Patent No. 10,700,178: Claim 1(f)
 “a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%,”

Further, for example, a portion of the second source or drain region is beneath the second dielectric spacer.



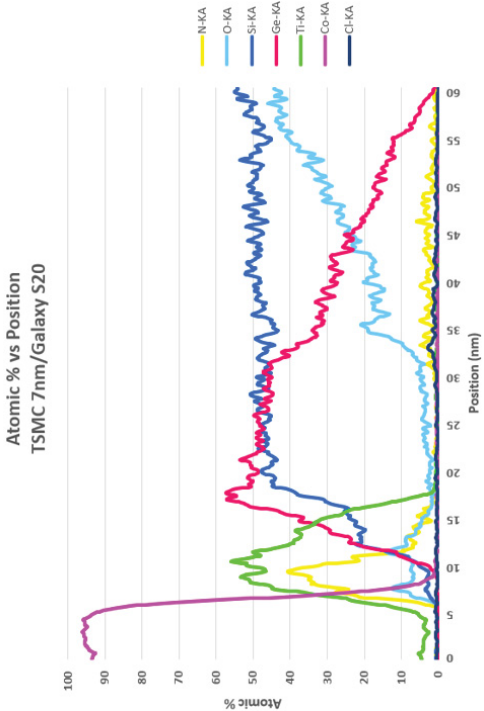
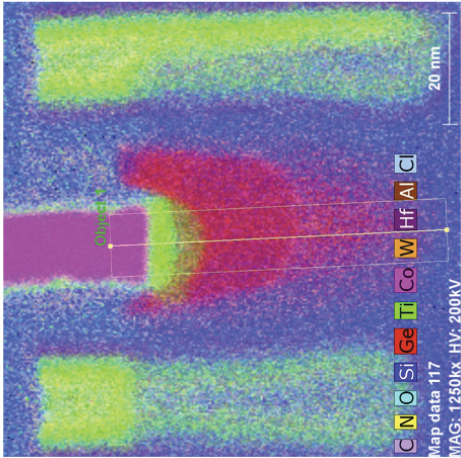
See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).



“a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%,”

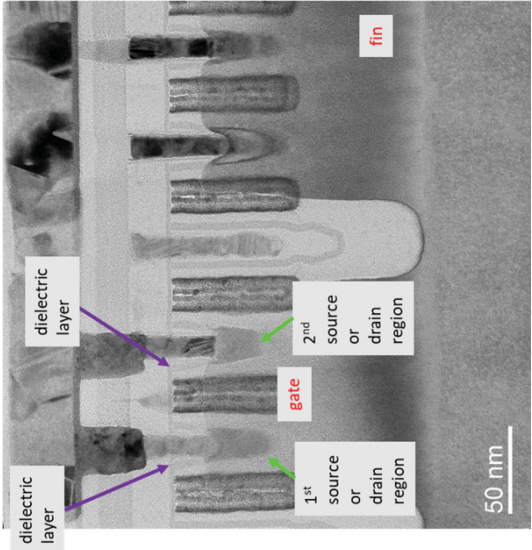
See Ex. 20 at 12, Photographs for the TSMC Representative Article (annotated).

The second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%.

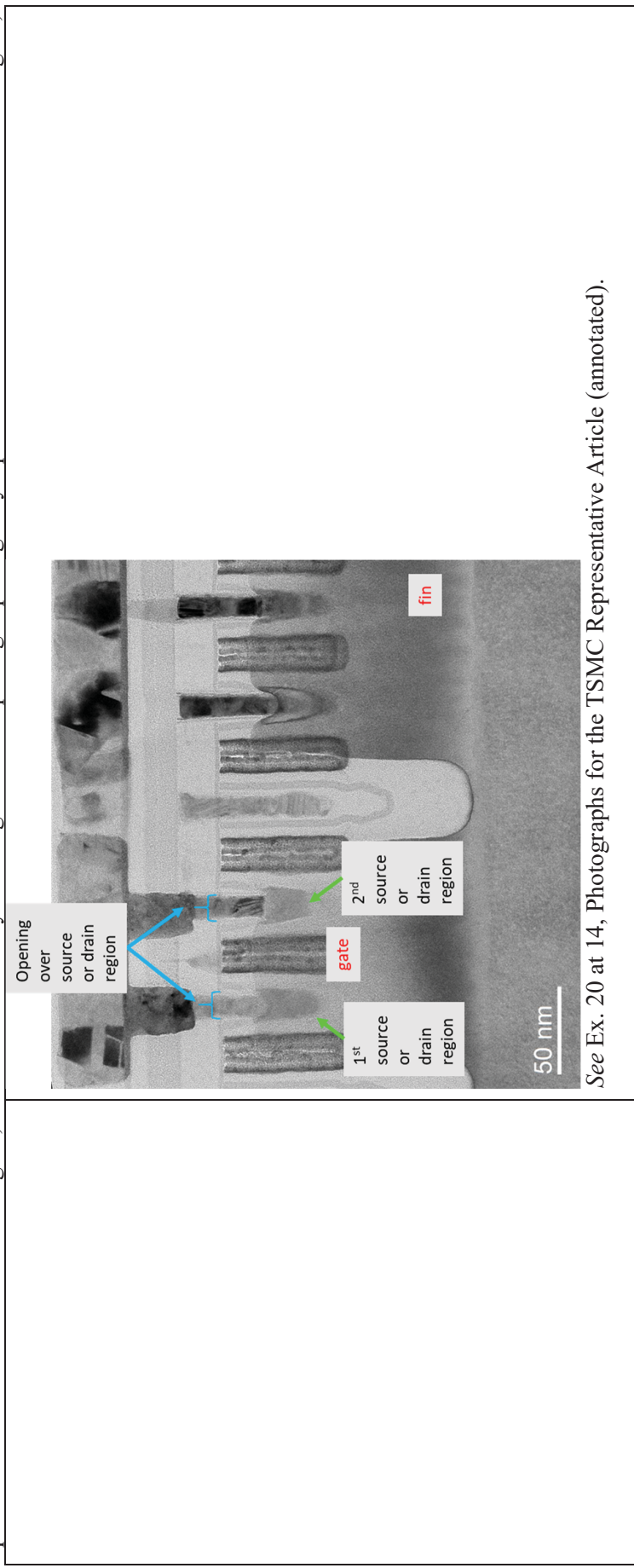


See Ex. 20 at 17 (left), 18 (right), Photographs for the TSMC Representative Article.

Claim 1(g): “a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;”

1(g). a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;	The Samsung/TSMC Product includes a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region. For example, the Qualcomm SoC includes a dielectric layer over the first source or drain region and over the second source or drain region.  See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated). Further, portions of the dielectric layer is removed exposing the first and second source or drain regions.
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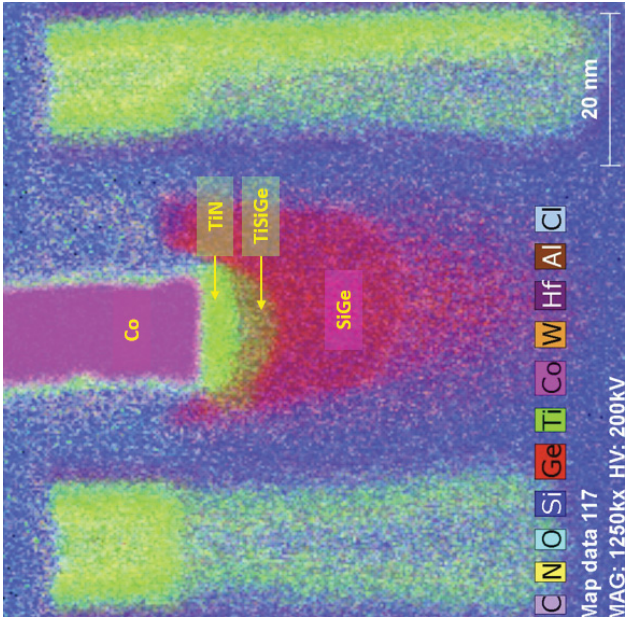
“a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;”



Claim 1(h): “a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;”

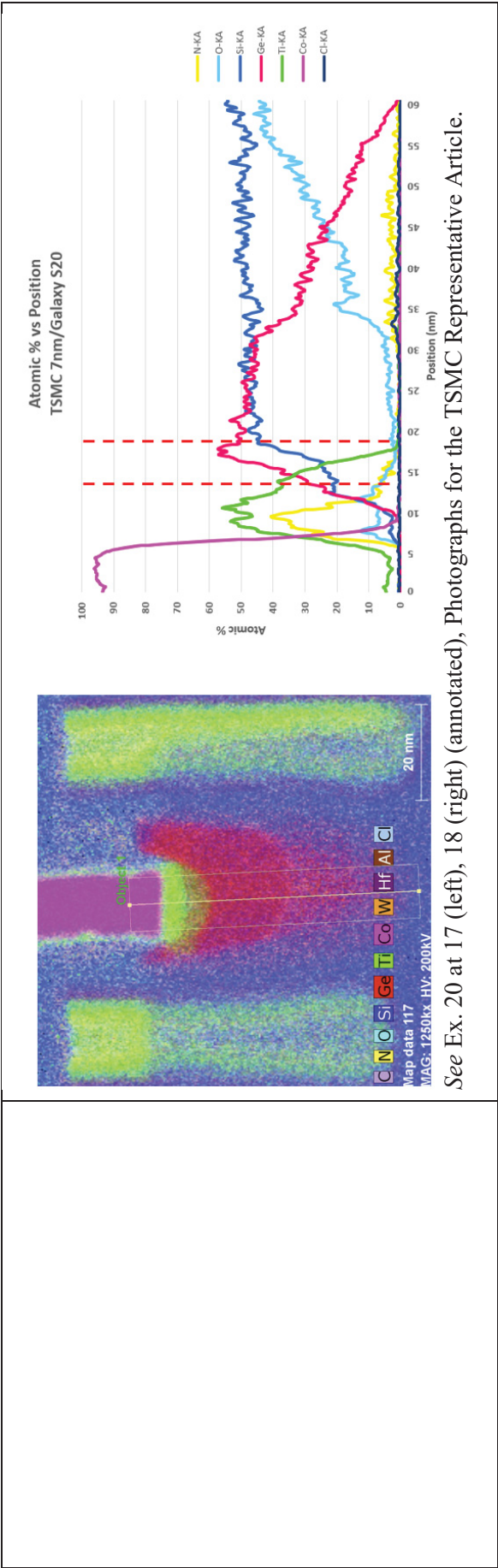
The Samsung/TSMC Product includes a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium.

For example, the Qualcomm SoC includes a germanide layer comprising silicon, germanium and titanium over the top surface of the first source/drain region.



See Ex. 20 at 19, Photographs for the TSMC Representative Article (annotated).

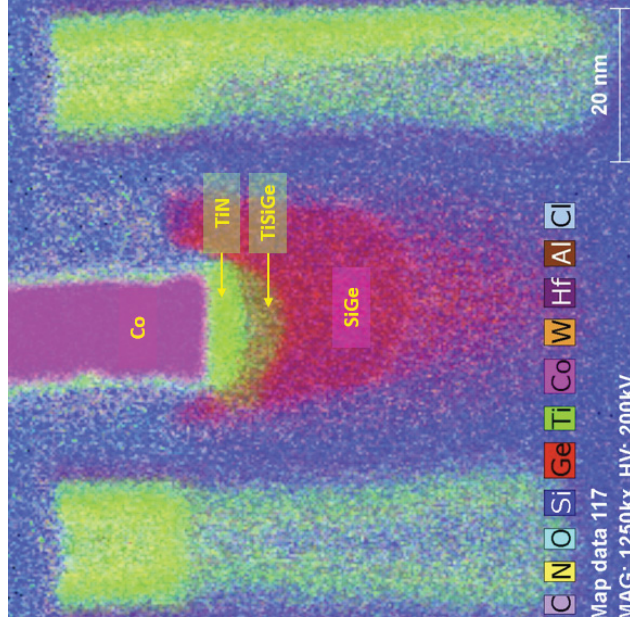
U.S. Patent No. 11,251,281: Claim 1(h)
“a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;”



Claim 1(i): “a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;”

The Samsung/TSMC Product includes a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

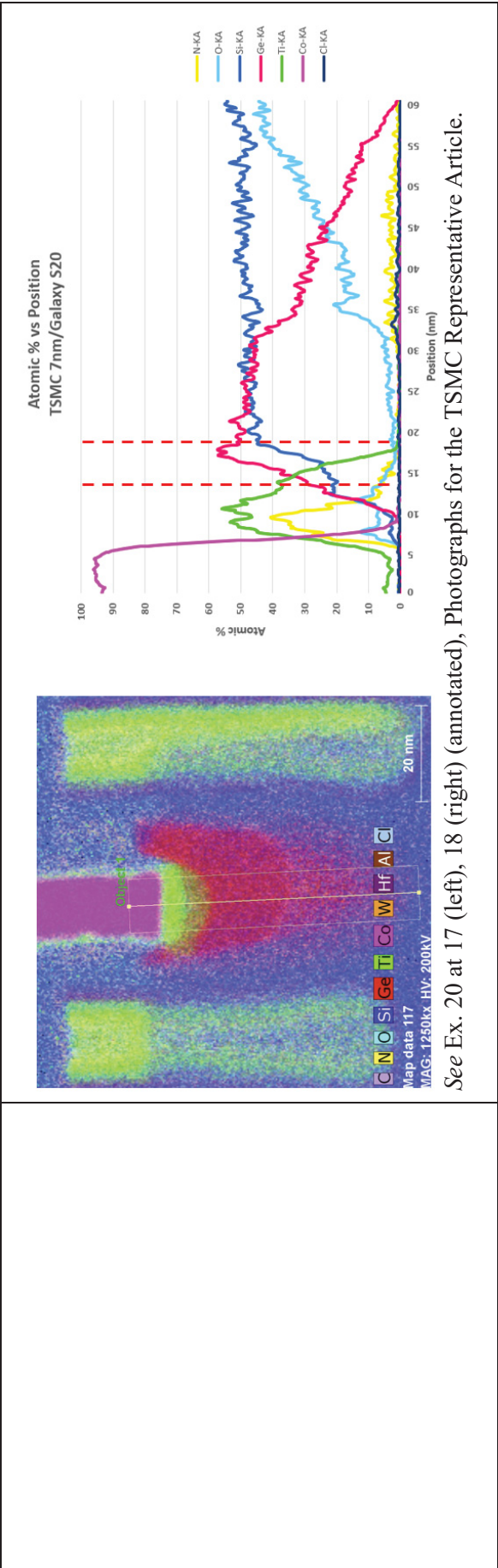
For example, the Qualcomm SoC includes a germanide layer comprising silicon, germanium and titanium over the top surface of the second source/drain region.



See Ex. 20 at 19, Photographs for the TSMC Representative Article (annotated).

1(i). a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;

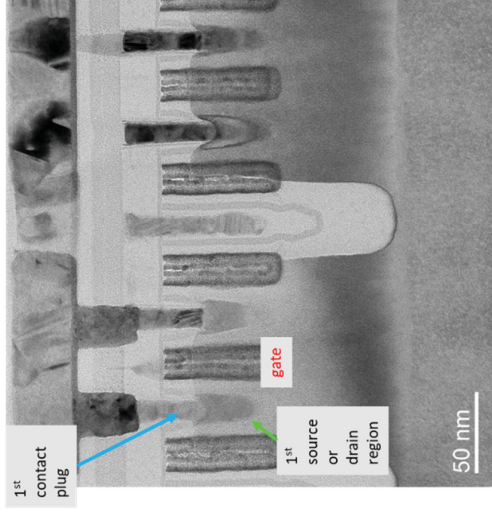
U.S. Patent No. 11,251,281: Claim 1(i)
“a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;”



Claim 1(j): “a first contact plug in the first opening and on the first germanide layer; and”

1(j). a first contact plug in the first opening and on the first germanide layer; and on the first germanide layer;

For example, the Qualcomm SoC has a first contact plug in the first opening and on the first germanide layer over a portion of the first source or drain region.



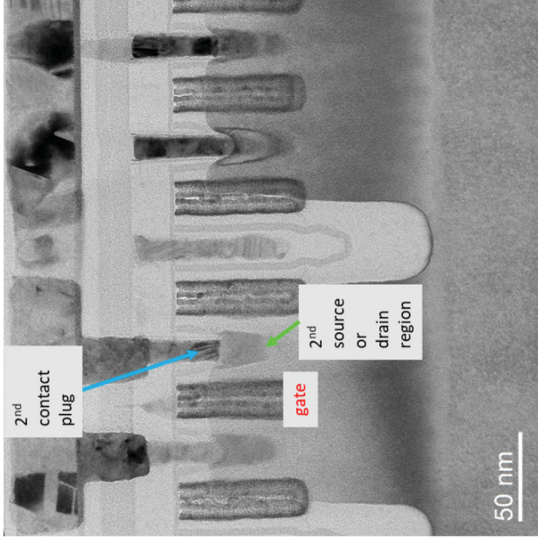
See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).

“a first contact plug in the first opening and on the first germanide layer; and
Claim 1(k): “a second contact plug in the second opening and on the second germanide layer.”

1(k). a second contact plug in the second opening and on the second germanide layer.

The Samsung/TSMC Product includes a second contact plug in the second opening and on the second germanide layer.

For example, the Qualcomm SoC has a second contact plug in the second opening and on the first germanide layer over a portion of the first source or drain region.



See Ex. 20 at 14, Photographs for the TSMC Representative Article (annotated).

U.S. Patent No. 11,251,281: Claim 1(j)
“a first contact plug in the first opening and on the first germanide layer; and

Claim 12(pre): “A computing device, comprising:”

12(pre). A computing device, comprising:

The Samsung Product includes a computing device.

See supra Claim 1(pre).

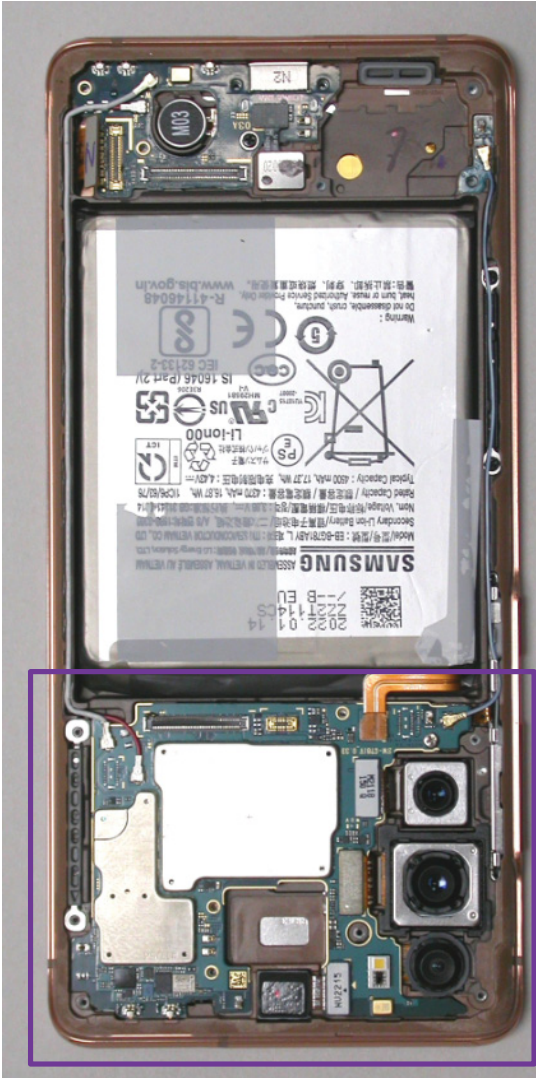
U.S. Patent No. 11,251,281: Claim 1(j)
“a first contact plug in the first opening and on the first germanide layer; and

Claim 12(a): “a board; and”
12(a). a board; and

The Samsung Product includes a board.

See *supra* Claim 1(pre).

Further, for example, upon information and belief, the Samsung Product includes a circuit board.



See Ex. 20 at 23, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - About Phone (annotated).

“a first contact plug in the first opening and on the first germanide layer; and
Claim 12(b): “a component coupled to the board, the component including an integrated circuit structure, comprising:”

12(b). a component coupled to the board,
the component including an integrated
circuit structure, comprising:

The Samsung Product includes a component coupled to the board, the component including an integrated circuit structure.

See *supra* Claim 1(pre).

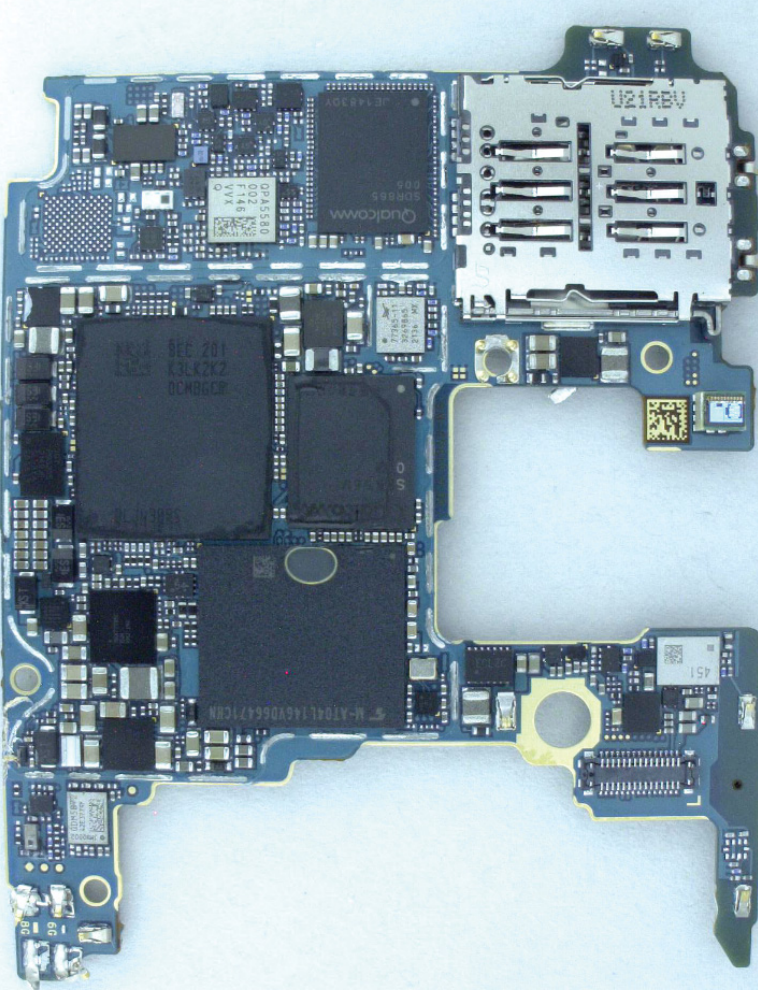
Further, for example, upon information and belief, the Samsung Product includes an SoC coupled to the circuit board.



See Ex. 20 at 23, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - About Phone (annotated).

Upon information and belief, the SoC is layered underneath the Samsung memory.

U.S. Patent No. 11,251,281: Claim 1(j)
“a first contact plug in the first opening and on the first germanide layer; and



See Ex. 20 at 24, Photographs for the TSMC Representative Article, Samsung Galaxy S20 FE - About Phone (annotated).

U.S. Patent No. 11,251,281: Claim 1(j)
“a first contact plug in the first opening and on the first germanide layer; and
Claim 12(c): “a fin comprising silicon;”

12(c). a fin comprising silicon;	The Samsung Product includes a fin comprising silicon. <i>See supra</i> Claim 1(a).
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“a first contact plug in the first opening and on the first germanide layer; and

Claim 12(d): “a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;”

12(d). a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

The Samsung Product includes a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side.

See supra Claim 1(b).

“a first contact plug in the first opening and on the first germanide layer; and
Claim 12(e): “a first dielectric spacer along the first side of the gate electrode;”

12(e). a first dielectric spacer along the first
side of the gate electrode;

The Samsung Product includes a first dielectric spacer along the first side of the gate electrode;

See supra Claim 1(c).

“a first contact plug in the first opening and on the first germanide layer; and

Claim 12(f): “a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%,”

12(f). a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;	The Samsung Product includes a first source or drain region in the fin proximate the first side of the gate electrode, a portion of the first source or drain region beneath the first dielectric spacer, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%. <i>See supra</i> Claim 1(d).
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“a first contact plug in the first opening and on the first germanide layer; and
Claim 12(g): “a second dielectric spacer along the second side of the gate electrode;”

12(g). a second dielectric spacer along the
second side of the gate electrode;

The Samsung Product includes a second dielectric spacer along the second side of the gate electrode.

See supra Claim 1(e).

“a first contact plug in the first opening and on the first germanide layer; and

Claim 12(h): “a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%,”

12(h). a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;	The Samsung Product includes a second source or drain region in the fin proximate the second side of the gate electrode, a portion of the second source or drain region beneath the second dielectric spacer, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%. <i>See supra</i> Claim 1(f).
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“a first contact plug in the first opening and on the first germanide layer; and

Claim 12(i): “a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region,”

12(i). a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;	The Samsung Product includes a dielectric layer over the first source or drain region and over the second source or drain region, the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region. <i>See supra</i> Claim 1(g).
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“a first contact plug in the first opening and on the first germanide layer; and
Claim 12(j): “a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;”

12(j). a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;	The Samsung Product includes a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium. <i>See supra</i> Claim 1(h).
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Claim 12(k): “a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;”

12(k). a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;	The Samsung Product includes a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium; <i>See supra</i> Claim 1(i).
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“a first contact plug in the first opening and on the first germanide layer; and
Claim 12(l): “a first contact plug in the first opening and on the first germanide layer; and”

12(l). a first contact plug in the first opening and on the first germanide layer; and	The Samsung Product includes a first contact plug in the first opening and on the first germanide layer; and and <i>See supra</i> Claim 1(j).
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Claim 12(m): “a second contact plug in the second opening and on the second germanide layer.”

12(m). a second contact plug in the second opening and on the second germanide layer.	The Samsung Product includes a second contact plug in the second opening and on the second germanide layer. <i>See supra</i> Claim 1(k).
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