

Epitaxial growth of Ge and SiGe on Si substrates

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Abstract

Epitaxial silicon-germanium layers have already for some time been used in Si-based high performance devices. More recently integration of Ge layers in Si-based structures has been considered due to its superior carrier mobilities compared to silicon. The most feasible method for integrating SiGe and Ge layers into Si-based structures is through epitaxial growth. Among the epitaxial growth systems molecular-beam epitaxy (MBE) and ultra-high vacuum chemical-vapor deposition (UHV-CVD) are widely used, in particular in research environments, due to their flexibility with respect to controlling growth parameters. The emphasis of this review will be on structures grown by these two techniques. Due to the 4.2% lattice misfit between Si and Ge, SiGe and Ge layers on Si substrates are usually grown on a buffer layer to accommodate the strain, thus producing SiGe or Ge top layers of reduced defect densities. Top layers with or without strain can then be produced by adjusting the composition of the buffer relative to that of the top layer. A high quality top layer of low defect density is the required product, and different buffer-layer concepts on Si are discussed.

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1. Introduction

Epitaxial silicon-germanium layers have already for some time been used in Si-based high performance devices such as heterojunction-bipolar transistors [1]. More recently integration of pure Ge layers in Si-based structures has been considered. Three possible applications of Ge in the Si-based technology have been the driving force behind the efforts to integrate Ge with Si: As photodetector in Si-based optical devices [2], as templates for lattice-matched III–V growth [3], and most recently as high mobility channel in Si-based field-effect transistors [4].

Because of the lattice mismatch of 4.2% between Si and Ge only very thin layers of Ge can be grown

defect free on (001)-oriented Si substrates; such layers are biaxially strained with an in-plane lattice constant equal to that of the Si substrate. The growth takes place in a dislocation free way only below a certain critical thickness which is ~ 10 Å for Ge on Si [5]. For layer thicknesses above the critical thickness, dislocations will nucleate with misfit segments parallel to and near the interface, and with threading segments running through the layer to the surface. When a fully relaxed Ge layer is grown directly on top of a (001)-oriented Si substrate, the resulting density of threading dislocations might be as high as 10^9 cm^{-2} . Such a layer is useless for most applications, the dislocation density being several orders of magnitude too high. As a rule of thumb LeGoues [6] states that the acceptable number of dislocations is as high as 10^7 disl/cm^2 for majority-carrier devices and below 10^4 disl/cm^2 for minority-carrier devices.

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So the challenge has been to develop growth procedures which could produce Ge layers of high crystalline quality. Common to all of the growth procedures of relaxed Ge on Si discussed in the following are processing steps which confine the misfit dislocations, which are needed to relax the stress, to a buffer layer or layers between the Si substrate and the Ge-top layer, and which reduce the concentration of threading dislocations in the Ge-top layer.

Although in manufacturing, the definition of quality covers several criteria [4], the concentration of threading dislocations in the Ge layers will be used here to compare the different growth procedures. The focus will be on the growth of pure Ge layers on Si (001) wafers as this is the most demanding process and, in most cases, the same procedures can be used to grow relaxed $\text{Si}_{1-x}\text{Ge}_x$ layers.

Many different concepts have been proposed for attaining relaxed Ge layers on (001)-Si substrates. In the following, four of these will be discussed and compared, namely the compositional grading technique, the low-temperature buffer technique, the two-step ultrahigh vacuum chemical-vapor deposition (UHV-CVD) technique, and the surfactant-mediated growth technique. As it will appear there is not always sharp separations between these concepts.

2. Growth procedures

2.1. The compositional-grading technique

Growth of strain-relaxed layers of lattice-mismatched III–V compounds have, since the seventies, exploited the phenomenon that the concentration of threading dislocations can be reduced significantly by grading the composition [7]. A layer, grown on top of a compositionally graded buffer, of a composition equal to the final concentration in the graded buffer layer, was found to be strain free and to have a significantly reduced dislocation density. The high density of misfit dislocations, needed to relieve the strain, was buried in the compositionally graded buffer layer. This growth procedure was successfully taken over by the SiGe community in particular advocated by the groups of Fitzgerald first at Bell Labs and later at MIT [8]; thus, between the (001)-Si substrate and the strain-relaxed SiGe top layer a compositionally graded buffer layer is included. For properly chosen growth procedures,

the effect is a reduction in the number of threading dislocations in the top layer of a factor of $\sim 10^3$. The mechanism behind this reduction is a combination of several effects: prevention of dislocation nucleation at the multiple low-mismatch interfaces in the compositionally graded region, increased dislocation-glide, and annihilation of threading dislocations with antiparallel Burgers vectors [9].

The observed increase in threading dislocation density from about $5 \times 10^4 \text{ cm}^{-2}$ in a relaxed $\text{Si}_{0.90}\text{Ge}_{0.10}$ structure on a graded buffer to the rather high density of $\sim 10^7 \text{ cm}^{-2}$ in a pure Ge layer, as demonstrated by Fitzgerald and Samavedam [9], is not in agreement with predictions of standard dislocation theory [9]; only an increase of a factor of 10 is expected. The increase of more than two orders of magnitude has been explained as being due to blocking of the motion of threading dislocations in the structure [9]. A blocking will result in a smaller average misfit dislocation density, and, consequently, to achieve the same amount of relaxation, additional dislocations will be nucleated, leading to a higher threading dislocation density. Evidence for blocking events is revealed in the pile-ups of dislocations as demonstrated in TEM investigations and from the rough, faceted surface morphology of the structures [10]. The observed surface cross-hatch pattern has been shown to be a result of, among other things, the pile-ups in the buffer layer, leading to displacements in the top layer and to regions of preferential growth [9,10]. The roughness of these layers can be serious, having root mean square (RMS) values of about 50 nm for a 100% Ge layer. This phenomenon has led Currie et al. [11] to interrupt the linear compositional grading procedure towards 100% Ge at a 50% Ge composition and perform a chemical mechanical polishing step at this composition (Fig. 1). This polishing step liberates dislocations trapped in pile-ups and obviates the necessity to nucleate new dislocations during the resumed growth towards 100% Ge (Fig. 2). They found a reduction in the threading dislocation density to $2.1 \times 10^6 \text{ cm}^{-2}$ as a result of the inclusion of such a polishing step at 50% Ge. In addition, the surface roughness was reduced about a factor of two to a RMS roughness of 24 nm as determined by atomic force microscopy (AFM).

2.2. The low-temperature buffer technique

There are two major disadvantages of the compositional grading procedure as described

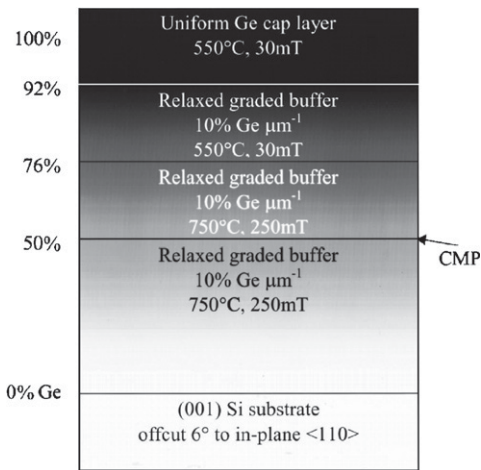


Fig. 1. Schematic of the structure and growth conditions for the compositional grading technique with a chemical-mechanical polishing (CMP) step. The Ge concentrations are indicated on the left. Reprinted with permission from M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, and E.A. Fitzgerald, Appl. Phys. Lett. 72 (1998) 1718. Copyright 1998, the American Institute of Physics.

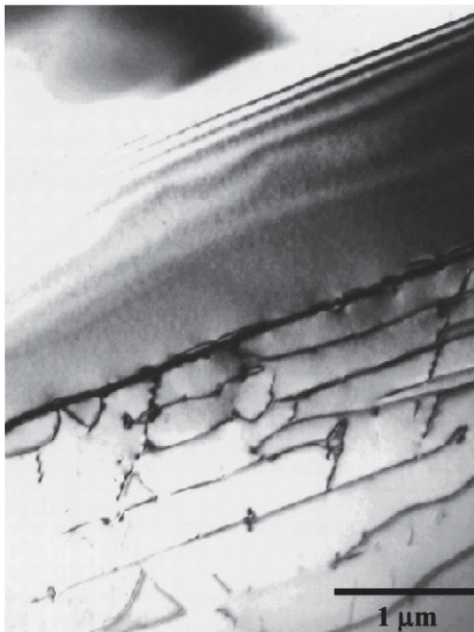


Fig. 2. Cross-sectional TEM image of the upper graded region and uniform Ge cap layer of the sample whose structure is sketch in Fig. 1. Reprinted with permission from M.T. Currie, S.B. Samavedam, T.A. Langdo, C.W. Leitz, and E.A. Fitzgerald, Appl. Phys. Lett. 72 (1998) 1718. Copyright 1998, the American Institute of Physics.

above, namely that the graded buffer layers are thick, and the rather large surface roughness. With typical growth rates the production of a composi-

tionally graded buffer to 100% Ge using a linear compositional grading will last a couple of hours. Furthermore, as discussed by Yang et al. [12], in applications which require the use of the Si substrate, or strained $\text{Si}_{1-x}\text{Ge}_x$ layers as well as strained Si layers, the step heights needed to define these layers would preclude state-of-the-art lithography due to depth-focus limitations. These disadvantages have caused a very active research in order to find new approaches to produce alternative buffers of smaller thicknesses.

The stepwise incorporation of thin $\text{Si}_{1-x}\text{Ge}_x$ layers, grown at relatively low temperature, into the buffer layer between the Si substrate and the uniform $\text{Si}_{1-x}\text{Ge}_x$ layer has recently been demonstrated to be a very successful route towards structures with thin buffer layers and low threading dislocation densities [13–15]. Fig. 3 shows cross-section TEM images of structures of three different final compositions [15]. A group from the Chinese Academy of Sciences in Beijing has in particular developed this technique. In the case of the 90% Ge structure, the uniform top layer is 5000 Å thick; the buffer layer between the Si substrate and the uniform top layer is in total only 1.15 μm, and it consists of two 5000 Å thick high-temperature layers (550 °C) and three 500 Å thick low-temperature layers (450 °C). Despite the thin buffer layer, the threading dislocation density is only $2\text{--}3 \times 10^6 \text{ cm}^{-2}$, thus similar to that reported by Currie et al. [11] which was for a 10 μm thick linearly graded layer including an intermediate polishing. The surface roughness is very low, only about 6 nm compared to the 24 nm found by Currie et al. [11]. The mechanism responsible for the reduction in the threading dislocation density has been explained as a combination of several effects [16]: The low-temperature stage creates many centres for nucleation of misfit dislocations and decrease the probability of strain-driven 3D growth; the high-temperature stage increases the velocity of the threading-dislocation motion and improves the conditions for threading-dislocation annihilation.

2.3. The two-step UHV-CVD technique

This technique, which has been developed by the group of Kimerling at MIT, is merely a variation of the low-temperature buffer technique. Luan et al. [17] grew first a 30 nm Ge layer at 350 °C to avoid 3D growth followed by a 1 μm thick Ge layer at a high-temperature of 600 °C. The threading

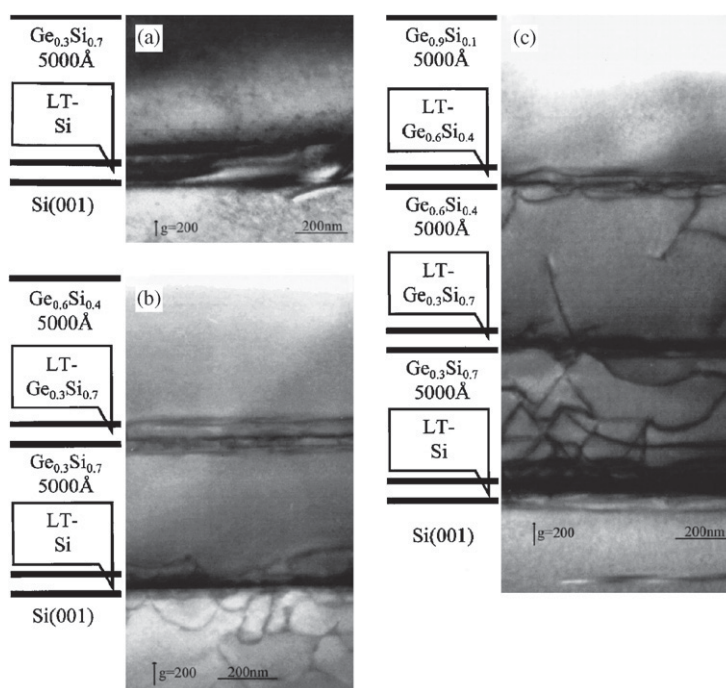


Fig. 3. Layer structures and bright field cross-section TEM images of structures grown by the low-temperature buffer technique. The low-temperature (LT) layers were grown at 400 °C and the 5000 Å SiGe layers at 550 °C. Reprinted with permission from C.S. Peng, Z.Y. Zhao, H. Chen, J.H. Li, Y.K. Li, L.W. Guo, D.Y. Dai, Q. Huang, J.M. Zhou, Y.H. Zhang, T.T. Sheng, and C.H. Tung, Appl. Phys. Lett. 72 (1998) 3161. Copyright 1998, the American Institute of Physics.

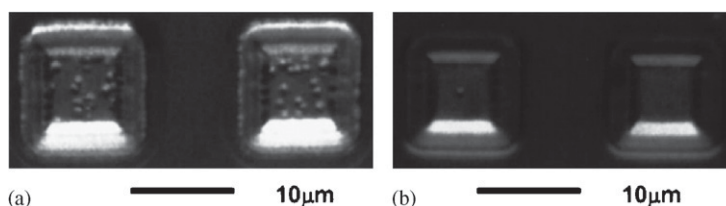


Fig. 4. Results from etch-pit density (EPD) counting of Ge selectively grown on patterned SiO₂/Si wafers by two-step UHV-CVD technique. The width of the mesa sidewalls is 10 μm: (a) is a sample grown using the two-step UHV/CVD process followed by 10 min annealing at 900 °C. The average EPD for the sample is $4.3 \pm 0.2 \times 10^7 \text{ cm}^{-2}$; (b) is a sample grown using the two-step UHV/CVD process followed by 10 annealing cycles between $T_H = 900 \text{ °C}$ and $T_L = 100 \text{ °C}$. The average EPD in this sample is $2.3 \pm 0.2 \times 10^6 \text{ cm}^{-2}$. Reprinted with permission from H.-C. Luan, D.R. Lim, K.K. Lee, K.M. Chen, J.G. Sandland, K. Wada, and L.C. Kimerling, Appl. Phys. Lett. 75 (1999) 2909. Copyright 1998, the American Institute of Physics.

dislocation density at this stage was typically $\sim 1 \times 10^9 \text{ cm}^{-2}$. The growth was then followed by cyclic thermal annealing, and the best result was obtained with 10 cycles between a high-temperature treatment (900 °C/10 min) and a low-temperature treatment (780 °C/10 min) which reduced the threading dislocation density to $2.3 \times 10^7 \text{ cm}^{-2}$. Selective area growth experiments were also performed in square windows made in oxide layers of 1 μm thickness; the square windows had sides ranging from 10 to 100 μm. Fig. 4 shows optical-microscopy pictures after an etch to enhance the

dislocation pits. It is seen that the sample which has been through a cycle annealing (Fig. 4(b)) has no dislocations within the mesa. The dependence of the threading-dislocation density in small Ge mesas as a function of mesa sidewall width was studied and it was found that the average threading-dislocation density decreased with decreasing side-wall width and reached a value of $2.3 \times 10^6 \text{ cm}^{-2}$ for $10 \mu\text{m} \times 10 \mu\text{m}$ mesas. This behaviour was explained as thermal-stress induced dislocation glide to the mesa sidewalls which act as dislocation sinks.

Table 1

Compilation of characteristic growth parameters and results of the different growth techniques discussed

Method	Si _{1-x} Ge _x (%)	Buffer-layer thickness (μm)	Ge layer thickness (μm)	Number of threading dislocations (cm ⁻²)	Surface roughness - RMS (nm)	Ref.
Compositional-graded buffer	100	23	1.5	1.1×10^7	36	Currie et al. [11]
Comp.-graded buffer with chemical-mechanical polishing	100	11	1.5	2.1×10^6	24	Currie et al. [11]
Low-temperature buffer	90	1.7	0.5	3×10^6	6	Peng et al. [15]
Two-step UHV-CVD with cyclic thermal annealing	100	0.03	1	2.3×10^7	No inf.	Luan et al. [17]
Two-step growth—low temp./high temp.	96	0.02	2.5	4×10^6	No inf.	Peng et al. [18]
Surfactant-mediated growth	100	No buffer	1	$\sim 2 \times 10^7$	No inf.	Wietler et al. [19]

A variant of this method, in which the high-temperature growth step and the subsequent high-temperature annealing have been united to one growth step at very high-temperature (900 °C), has been presented by Peng et al. [18]. They find a threading-dislocation density of $4 \times 10^6 \text{ cm}^{-2}$.

2.4. The surfactant-mediated growth

The use of a surfactant for Ge growth on Si (001) stabilizes layer-by-layer growth instead of 3D growth. This means that by the use of a surfactant a higher growth temperature can be chosen. This has recently been demonstrated by a group from University of Hannover [19]. They used Sb as a surfactant, and deposited a monolayer of Sb prior to evaporation of Ge and they maintained a large Sb-flux during the subsequent Ge epitaxy which was done at the comparatively high substrate temperature of 670 °C. They measured a dislocation density of $\sim 2 \times 10^7 \text{ cm}^{-2}$ penetrating the Ge surface. The relative low dislocation density is explained as the result of an abrupt strain-relief via the formation of a regular array of 90° misfit dislocations at the interface during the initial growth. The nucleation of misfit compensating 90° dislocations with the Burgers vector in the (001) plane is favored by the high Sb coverage at ~ 700 °C. The use of Sb as surfactant leads to the incorporation of high concentrations of Sb giving rise to a high n-type background doping level. Under the above conditions n-type doping levels of $3\text{--}4 \times 10^{16} \text{ cm}^{-3}$ were measured.

3. Discussion and conclusion

Characteristic results obtained with the growth methods discussed above are collected in Table 1. None of the methods produces Ge layers with threading-dislocation concentration below $1 \times 10^6 \text{ cm}^{-2}$, however, two of the methods, the compositional-graded buffer method with chemical-mechanical polishing and the low-temperature buffer method, produce layers with dislocation concentrations close to this value. It should be noted that the low-temperature buffer method gives a small surface roughness (RMS ≈ 6 nm) as compared to that of the compositional-graded buffer method with chemical-mechanical polishing (RMS ≈ 24 nm) and that the thickness of the buffer layer of the low-temperature buffer method is only 1.7 μm as compared to 11 μm of the compositional-graded buffer method with chemical-mechanical polishing. If smaller dislocation concentrations are needed then selective area growths is an option in which selected areas free of dislocations can be produced.

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