

Silicides for S/D Contacts

Silicide has been the preferred material for contact to the source/drain (S/D) regions of silicon field effect transistor (FET) devices for many years. The main advantage silicide contacts offer over nonsilicided contacts is a higher device performance owing to lower parasitic resistance. Also, self-aligned silicide processes are inexpensive to implement and relatively robust. A silicide layer reduces the resistance of a S/D contact in two ways. First, the low sheet resistance of the silicide layer shunts the heavily doped diffusion region of the S/D to reduce its in-plane resistance, and second, the silicide reaction leads to intimate and more reliable metal–semiconductor (MS) contact and improves the conduction in the vertical direction. In terms of performance, the most important properties of a silicide material are its electrical resistivity and its Schottky barrier height, a list of which for silicide materials commonly used in silicon devices is given in Table 1. There are, of course, other integration issues that more critically determine the overall effectiveness and compatibility of a silicide process. As the dimensions of ULSI devices shrink to below 0.2 μm , several challenges begin to surface for silicided contacts. One issue is simply with the formation of the desired silicide phase, which, in very narrow silicon regions or on highly doped silicon, has been known to be problematic for some silicides. But a more difficult challenge is to make low-leakage contacts to very shallow junctions ($< 50\text{nm}$), while maintaining a low sheet/contact resistance. Important for junction considerations and also listed in Table 1 is the material consumption in silicide reactions.

The strategy for silicide contacts is often inseparable from the scheme for shallow junction formation (see *Front-end Dopant Profile Engineering*). Traditionally the silicidation process is applied to the S/D area with a junction and an extension already in place, as shown

Table 1

Properties of common silicides: electrical resistivities at 298 K, Schottky barrier height to *n*-type silicon, and amounts of metal and silicon consumed in order to form a 100 nm thick silicide layer.

Silicide	Resistivity at 298 K ($\mu\Omega\text{ cm}$)	<i>n</i> -type SBH (eV)	Reaction consumption (nm)	
			Metal	Silicon
CoSi ₂	16	0.64	28.5	103.6
C49 TiSi ₂	55	0.55	39.3	89.1
C54 TiSi ₂	14	0.55	41.6	94.3
PtSi	30	0.87	50.6	67.0
NiSi	15	0.68	49.8	91.0
NiSi ₂	45	0.66	27.7	101.2
MoSi ₂	38	0.55	38.8	99.3
TaSi ₂	38	0.59	41.8	92.2
WSi ₂	30	0.65	39.0	98.6

in Fig. 1(a), so an important constraint of the silicide growth is to maintain the junction integrity. Not only should the physical extent of the silicide layer, with all the fluctuation in its thickness, be well contained within the diffusion region, but the silicidation process should not significantly modify the intended junction depth/width or cause leakage. It is clear then that an ideal silicide for the S/D is one which (i) consumes a minimum amount of silicon, (ii) has low sheet resistance, (iii) forms easily and uniformly, independent of geometry, (iv) is thermally stable, (v) has favorable dopant interaction, and (vi) does not stress, or inject impurities or other point defects into the silicon. Generally speaking, the morphology of a silicide layer, although ultimately governed by surface and interface energies, is largely the result of growth kinetics. To induce uniform growth of silicide globally across a wafer, or for consistent formation from wafer to wafer, attention must be paid to the uniformity of all processes leading up to and including the silicidation process (deposition uniformity, temperature uniformity, etc.). On a local scale, layer uniformity is more easily achieved under conditions of high nucleation densities (see *Salicides*) and minimized lateral diffusion. The latter can sometimes be accomplished by placing a “cap” over the silicide to reduce surface diffusion, which offers the most convenient path for lateral diffusion. The nucleation density of silicide is determined not only by thermodynamic driving forces but also by kinetic factors. The silicidation behavior on heavily doped silicon can be quite different from that on lightly doped silicon. Dopant incorporation in the silicide crystal can lead to an increase in silicide resistivity.

Segregation of dopants at the silicide interface can lead to higher doping concentration for silicon, which is beneficial. However, the formation of stable compounds between a dopant and either the metal or the silicon can lead to a depletion of dopants near the silicon interface, which is undesirable for the contact resistance. Early dopant diffusion experiments suggested that silicide reaction induced the injection of self point defects with concentrations orders of magnitude higher than the equilibrium concentration in silicon. Furthermore, it was suggested that the type of injected point defects depended on whether the silicon or the metal was the diffusing species in the silicide reaction. Later, more careful studies, however, saw only small increases in the self-vacancy concentration during silicide reactions, independent of the diffusing species. Well-annealed silicide layers are usually in tension owing to larger thermal expansion coefficients than silicon. Increased junction leakage has often been attributed to the stress that silicide layers exert on the silicon junction, although a definite relationship between the two has yet to be established. Generally speaking, the level of stress due to silicide layers is far less than that caused by dielectric isolation, and is a concern only in extreme cases (e.g., $> 1\text{ GPa}$).

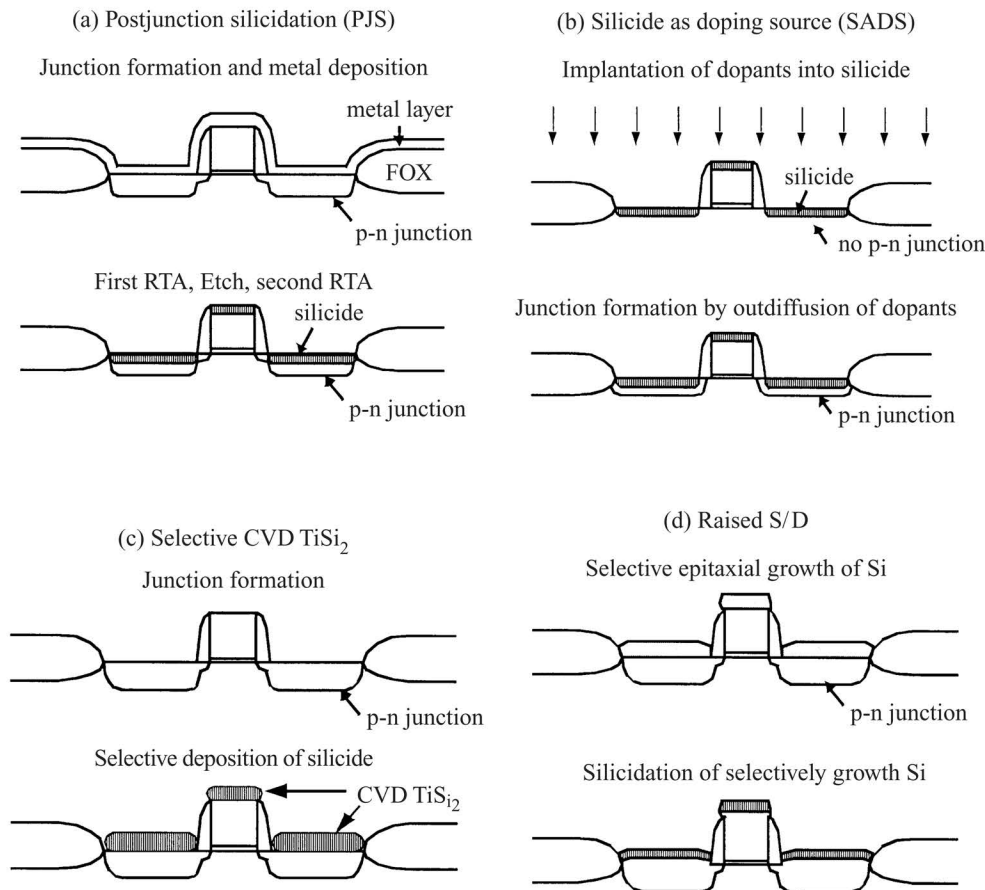


Figure 1

Schemes for silicided junctions. (a) Postjunction silicidation, (b) silicide as doping source, (c) selective deposition of silicide, and (d) silicidation of selectively grown silicon (or SiGe).

As the junction depths of ULSI devices are scaled down to much less than 100nm, new junction technologies are required. The procedures for the formation of low-resistance silicide contacts can be integrated with the procedures for shallow junction formation to offer more flexibility and capability. Silicide layers can be used as a buffer in an implantation through metal (ITM) scheme. Another scheme that has often been discussed is the silicide as doping source (SADS) technique for shallow junction formation (Liu *et al.* 1988) (see *Solid Source Diffusion for Shallow Junctions*). In this technique, as shown in Fig. 1(b), a silicide (or salicide) layer is first formed in the source and drain region. A low-energy ion implantation of dopants then follows with the range of the implanted dopants to be confined entirely within the silicide layer. A subsequent high-temperature anneal then drives the dopants out of the silicide and into surrounding silicon, thus forming the *p-n* junction. Since the junction contour by the SADS method is conformal to the silicide interface under the condition of bulk-dominated diffusion, there are some expectations that “weak points” of the junction owing to silicide interface roughness can be eliminated. The

SADS technique also promotes the formation of ultrashallow junctions by eliminating transient-enhanced diffusion (TED) of dopants in silicon, associated with implantation-induced point defects. Obviously, the dopants in the silicide should be very mobile for this technique to work, and the silicide layer has to remain stable during out-diffusion anneals. Various raised S/D structures have been investigated and they are the only techniques that allow as low a sheet resistance as desired, without jeopardizing junction depth or junction integrity (Fig. 1(d)). Selectively deposited silicide (Fig. 1(c)) is a major candidate for raised S/D, but this technology still faces challenges.

1. TiSi_2 Contacts

Titanium silicide is favored as a contact material to silicon. When applied as part of the front-end process, titanium silicide is usually formed in a self-aligned fashion, with a final anneal of $\sim 800\text{--}900^\circ\text{C}$ for the low resistivity C54 TiSi_2 phase. Titanium has also been used as a contact material of choice later in the process

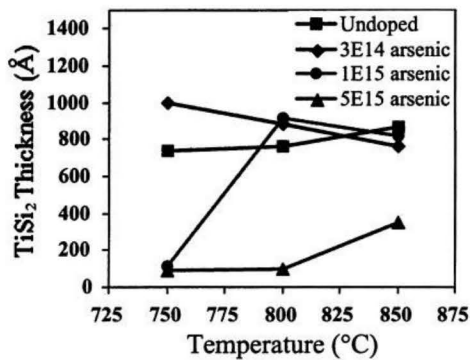


Figure 2

Dependence of CVD TiSi_2 deposition on the arsenic doping level of silicon. At high arsenic doping levels, not only is the deposition rate reduced as shown, but the silicon consumption also increases (courtesy of M. Ozturk).

flow, when windows are opened in dielectric layers to expose heavily doped silicon regions. In the later scheme, the titanium layer is often capped with a TiN layer. The popularity of titanium-based contacts is due, to some degree, to its low resistivity and high chemical reactivity. Because the titanium silicide reaction can proceed right through residual and native oxide on the silicon surface, intimate and reliable contacts are easily made. Compared with other silicides such as CoSi_2 , low-leakage junctions are relatively easy to form in titanium silicide contacts. Another advantage of titanium silicide is its interface Fermi level position, which is near midgap of silicon, allowing low contact resistance to be achieved on both *n*- and *p*-type silicon. Unfortunately, there are known stable compounds between titanium and common dopants boron and arsenic. So titanium silicide scavenges these dopants from the silicon interface during high-temperature anneals, which can lead to a decrease of the interface doping level and an increase in contact resistance. It is clear that, because of these dopant reactions, TiSi_2 does not support diffusion of dopants (boron in particular) and that it is not a good candidate for a doping source (SADS) (Jiang *et al.* 1992). Furthermore, prolonged annealing of TiSi_2 contacts at high temperatures should be avoided to maintain the low contact resistance. The formation of the C54 TiSi_2 phase is known to be extremely difficult for very thin and/or narrow silicide layers. Since contacts to modern ULSI devices will progressively become even smaller in both their lateral and vertical dimensions, very severe challenges will face TiSi_2 contacts in the future. The latest trend is to use refractory metals (tantalum, molybdenum, etc.) to enhance the C54 TiSi_2 reaction (Mann *et al.* 1995). There is no reported effect of these impurities on the junction integrity of TiSi_2 contacts.

2. Selective TiSi_2 Contacts

A very attractive raised S/D scheme is LPCVD TiSi_2 in the temperature range 700–850 °C, using SiH_4 (or DCS)/ TiCl_4/H_2 gas sources. The actual chemistry involved in the deposition of TiSi_2 is quite complicated, as shown by detailed analyses. Even though CVD TiSi_2 has been proposed as a selective deposition process, it is actually possible to consume more silicon by the CVD process than in a PVD process, for the same silicide layer thickness, if the process is not properly controlled. This is because silicon is not only consumed in the silicide reaction but can also be lost to the gas phase during the decomposition of TiCl_4 . However, with high $\text{SiH}_4/\text{TiCl}_4$ flow rate ratios, it is possible to achieve silicide deposition with little silicon consumption (Maury *et al.* 1997). In a rapid thermal (RTCVD) process, silicon is first selectively deposited which is followed by the deposition of titanium and the consumption of silicon. This process needs to be timed precisely to stop the titanium deposition before the silicide reaction proceeds beyond the original silicon surface. Immediately after the CVD growth, the titanium silicide is usually found in the low-resistance C54 TiSi_2 phase, prompting the notion that this phase is directly formed at elevated growth temperature. Studies, however, have shown that the initial isolated silicide grains deposited are in the C49- TiSi_2 phase, which is transformed to the C54 TiSi_2 phase only after the silicide layer thickness increases to ≥ 40 nm where silicide grains coalesce and become a continuous layer. It is likely that grain boundaries are also important for the transformation to the C54 TiSi_2 phase during CVD, just as in the case of the PVD silicide process. There is no nucleation problem on narrow silicon lines when the CVD TiSi_2 thickness is large. For thin-film deposition (< 30 nm), surface preparation is very important to ensure a homogeneous nucleation of titanium silicide, which then facilitates the C49 TiSi_2 to C54 TiSi_2 phase transformation.

The selectivity of the TiSi_2 CVD process on SiO_2/Si pattern is very good below 800 °C. It is not expected to have good selectivity on $\text{Si}_3\text{N}_4/\text{Si}$ pattern, because of the poor selectivity of epitaxial silicon. The deposition rate of TiSi_2 is known to be affected by the ratio of $\text{SiO}_2:\text{Si}$ area. This mask loading phenomenon is slightly alleviated by the addition of HCl to the process and by optimizing the gas pressure (Maury *et al.* 1997), even though full control of mask-related problems for large diameter wafer size still needs to be demonstrated. Another problem selective TiSi_2 faces is the substrate consumption problem on heavily doped *n*-type silicon (Fang *et al.* 1999). Surface arsenic hinders the deposition process of silicon, which leads to significant consumption of the substrate silicon in the titanium deposition process, as shown in Fig. 2. Presilicidation selective deposition of a silicon buffer layer does not remove this problem entirely because of

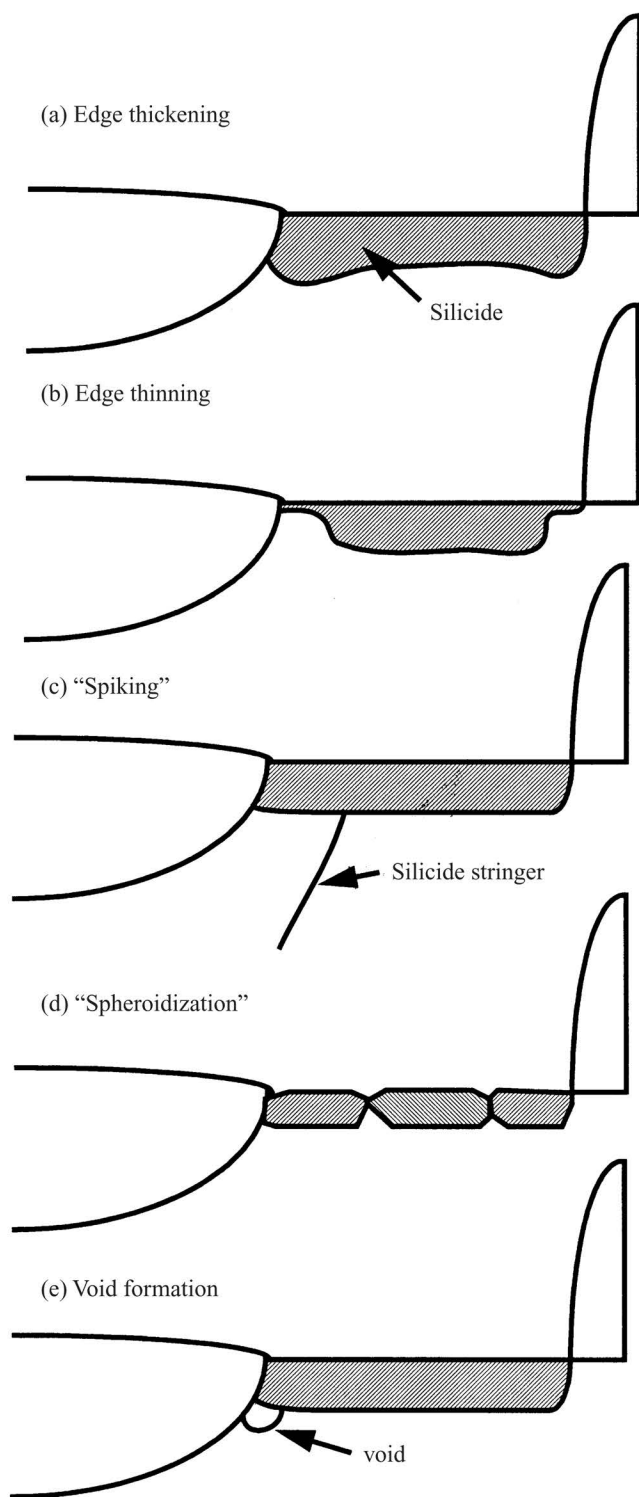


Figure 3
Reported problems with CoSi_2 formation in S/D area of a MOSFET device: (a) edge thickening owing to cobalt diffusion; (b) edge thinning owing to contamination; (c) silicide spikes for CoSi RTA at $\sim 450^\circ\text{C}$; (d) grain boundary grooving; (e) void formation.

the surface segregation of arsenic during growth. It has been reported that a brief etch of the surface by chlorine gas or a hydrogen prebake can reduce the silicon consumption problem on arsenic-doped silicon. With optimized parameters, selectively grown TiSi_2 is capable of excellent resistance with low junction leakage. But with the doping and mask-related issues not entirely resolved, it remains to be seen whether selectively deposited TiSi_2 can find applications in mainstream IC fabrication. It should be pointed out that for special applications on SOI devices, an optimized CVD TiSi_2 process, with hydrogen prebake, has been shown to lead to excellent low-resistance contacts.

3. CoSi_2 Contacts

3.1 CoSi_2 Salicide Contacts

Cobalt silicide is clearly the silicide contact material of choice for sub-150 nm silicon ULSI devices, because of the ease with which CoSi_2 can be formed on narrow silicon lines. As a matter of fact, the sheet resistance of CoSi_2 layer often shows a reverse fine-line effect, i.e., sheet resistance decreases as the linewidth decreases (Inoue *et al.* 1995). This effect is due to cobalt diffusion from atop the dielectric, thus increasing the silicide thickness near the edges of the S/D, as shown schematically in Fig. 3(a). While desirable from the point of view of sheet resistance, the enhancement of silicide thickness near the edges may be problematic for junction integrity. Modified sidewall profiles and limited reaction have been shown to eliminate this problem. Sometimes the opposite problem occurs: the thickness of fully reacted CoSi_2 layer is thinner near the edges of a SiO_2 pattern. This apparent peel-back of CoSi_2 from the edges, shown schematically in Fig. 3(b), is likely to be due to the incomplete cleaning of the silicon surface, the release of contamination from SiO_2 during annealing, and/or stress-related effects. Cobalt silicide reaction is known to be sensitive to surface cleanliness and ambient contamination. The use of a titanium cap has been demonstrated to eliminate this problem, as titanium scavenges the surface oxide and arrests the oxygen and water vapor evolved during annealing (Maex *et al.* 1998). Capping by titanium or TiN is known to significantly improve the uniformity of CoSi_2 layers (Berti and Bolkhovsky 1992). A proper management of possible by-products between the titanium cap and the cobalt silicide should be taken to avoid possible deleterious effect of the titanium on CoSi_2 junction characteristics. Large junction leakage has also been reported for partial cobalt silicide interfaces which have been annealed to $450\text{--}500^\circ\text{C}$. Detailed analysis shows that long strings of a metallic phase (likely to be CoSi_2) are sometimes found to sprout out from CoSi/Si interfaces and extend deep into the silicon beyond the $p\text{--}n$ junction,

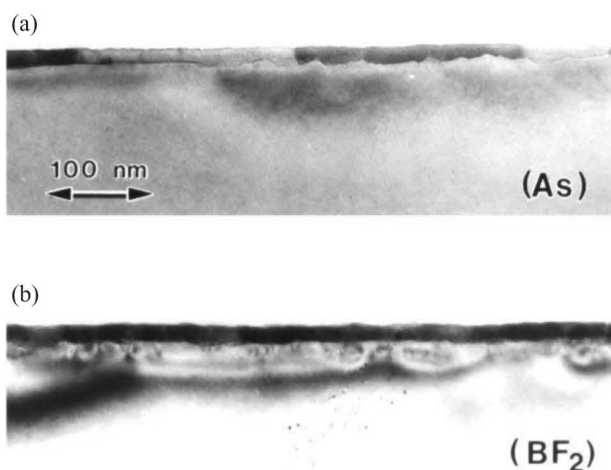


Figure 4

Cross-sectional TEM images of ~ 22 nm thick CoSi_2 layers grown by HTS on Si(100) and annealed at 600°C . (a) On arsenic-implanted silicon, several epitaxial orientations are present, and (b) on BF_2 -implanted silicon, the film has predominantly (100) orientation.

causing severe leakage problems (Goto *et al.* 1995). By increasing the first RTA temperature to above 550°C , this “spiking” problem, as illustrated in Fig. 3(c), can be essentially eliminated. Because of grain boundary grooving, the morphology of CoSi_2 layers grown on single crystals is not very uniform. During high-temperature anneals, the grain structure coarsens and goes through what has been called a “spheroidization” process to a lumpy structure (Probst *et al.* 1991), as shown in Fig. 3(d). Leakage in CoSi_2 junctions has often been attributed to the nonuniformity of CoSi_2 layer. It has also been reported that high-temperature sputtering (Inoue *et al.* 1997), discussed below, is beneficial to the junction integrity of CoSi_2 contacts.

Dopants are known to slow down cobalt silicide reactions: phosphorus and arsenic retard both the CoSi and the CoSi_2 reactions, while boron hinders the formation of CoSi_2 . Since the solubility of dopants is low in CoSi_2 , they diffuse out of the silicide during reaction and either redistribute in silicon or are lost at the surface. CoSi_2 has been regarded as a good candidate for SADS applications (Probst *et al.* 1991). Even though there are stable compounds between cobalt and common dopants in the phase diagrams, these compounds have not been observed in the presence of silicon. CoSi_2 has a rather open lattice structure and, therefore, is expected to accommodate rapid dopant diffusion via mechanisms other than substitutional diffusion. This turns out to be true only for boron, which is found to have a significant diffusivity in CoSi_2 lattice at moderate temperatures. Implanted boron redistributes quickly in CoSi_2 layer and diffuses into silicon and forms good p^+-n junctions. Arsenic has no detectable mobility in CoSi_2 although it diffuses along grain boundaries and can

still be used to dope silicon to the solubility limit (Probst *et al.* 1991). Because of possible lateral inhomogeneity of grain boundary diffusion, the quality of junctions formed by arsenic diffusion from polycrystalline CoSi_2 is thus suspect. A high implantation dose is required for arsenic SADS to compensate for dopant loss during the high-temperature anneal (Jiang *et al.* 1992).

3.2 Epitaxial CoSi_2 Contacts

Because of a favorable lattice matching condition, CoSi_2 can be grown epitaxially on silicon (Tung and Inoue 1997). Some of the noted features of epitaxial silicide layers, such that very thin layers can be fabricated which are very uniform and thermally stable, make epitaxial silicides a potential solution to the problems facing future silicided shallow junctions. High-quality epitaxial silicide layers used to be fabricated exclusively with UHV and other nonorthodox methods (Tung and Inoue 1997). Beginning in the mid 1990s, however, a few epitaxial silicide techniques have emerged which are compatible with the conventional processing environment of ULSI devices (Tung and Inoue 1997).

(a) *High-temperature sputtering (HTS)*. Sputtering and *in situ* annealing of ultrathin cobalt films at elevated temperatures, $\sim 400^\circ\text{C}$, have been found to lead to an improvement in the electrical characteristics of CoSi_2 films subsequently annealed (Inoue *et al.* 1995). Analyses reveal that CoSi_2 films grown by the HTS technique have predominantly epitaxial

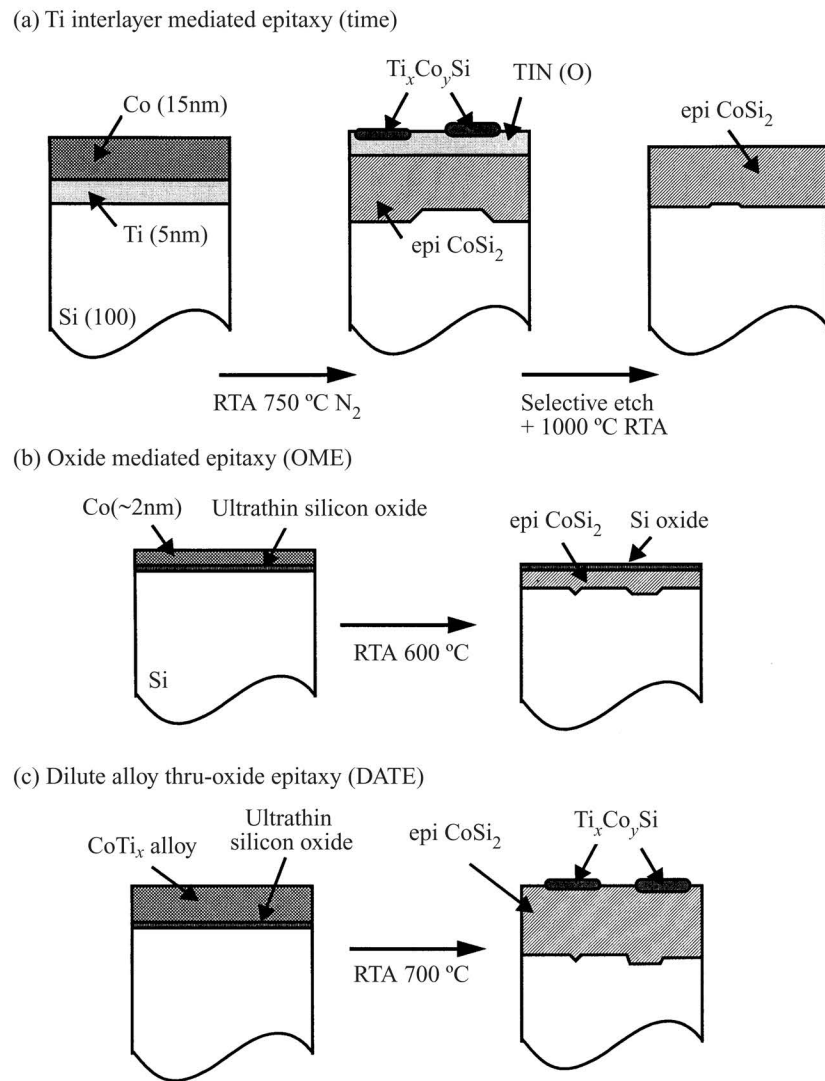


Figure 5

Schematics of epitaxial CoSi_2 techniques: (a) titanium interlayer-mediated epitaxy; (b) oxide-mediated epitaxy; (c) dilute alloy through-oxide epitaxy.

orientations on heavily doped Si(100) (Inoue *et al.* 1997). The majority of CoSi_2 layers has the regular (100) epitaxial orientation on BF_2 -implanted Si(100), as shown in Fig. 4(b). On arsenic-implanted Si(100), HTS processing leads to a complete coverage by oriented CoSi_2 , but with two epitaxial orientations. In addition to the regular (100) orientation, the majority of CoSi_2 films grown on Si(As) is found to have the (221) orientation, as shown in Fig. 4(a). This orientation is equivalent to type-B orientation on an inclined {111} interface. Only slight modifications to a routine cobalt silicide process are involved in the HTS technique, making it very attractive for device processing. The HTS process, however, is not well poised for SADS application, because CoSi_2 layers grown by HTS on lightly doped silicon contain only a small fraction of epitaxial grains.

(b) *Titanium interlayer-mediated epitaxy (TIME)*. If a titanium layer (2–10nm) is first deposited on silicon before the cobalt deposition (10–20nm), a subsequent anneal leads to the growth of an epitaxial layer of CoSi_2 (Dass *et al.* 1991). After the reaction, titanium is found near the surface in the forms of TiN and other titanium-containing phases. The main role played by the titanium interlayer (or tantalum, zirconium, and other interlayers) is to slow down the supply of cobalt for silicide reaction. Epitaxial CoSi_2 layers grown by TIME are often nonuniform in thickness. Improvements in the quality of TIME layers have been demonstrated by using a titanium cap, and by removing the surface $\text{Ti}_x\text{Co}_y\text{Si}_z$ layer (Hsia *et al.* 1991) prior to high-temperature annealing. The entire TIME process is illustrated in Fig. 5(a). An obvious advantage of the TIME technique is its

compatibility with the standard silicon fabrication environment. However, the TIME process has some problems, one of which is the growth of multi-oriented CoSi_2 on heavily arsenic-doped silicon. Another, more serious, problem of the TIME process is the formation of voids near the edges of CoSi_2 layers grown on silicon surfaces with an oxide pattern (Byun *et al.* 1996), as shown schematically in Fig. 3(e).

(c) *Oxide-mediated epitaxy.* The oxide mediated epitaxy (OME) technique (Tung 1996) uses a thin SiO_x layer, grown on silicon substrates in an aqueous bath containing H_2O_2 , to promote the epitaxial growth of CoSi_2 . When $\sim 1.5\text{--}3\text{ nm}$ of cobalt is deposited at room temperature on thin SiO_x -covered $\text{Si}(100)$ and annealed at $\sim 600^\circ\text{C}$, a (100)-oriented CoSi_2 layer is grown. Ultrathin $\text{CoSi}_2/\text{Si}(100)$ interfaces grown by OME are continuous and single crystalline, but they are characterized by microfaceting. OME growth is not significantly affected by substrate doping, and essentially the same OME procedures can be applied to grow epitaxial CoSi_2 layers on any silicon surface (Tung 1996). The OME process is shown schematically in Fig. 5(b). OME-grown, ultrathin CoSi_2 layers can be used as template layers for the growth of thicker CoSi_2 layers. The degree of interfacial microfaceting is generally reduced when OME layers are made thicker by template growth. It is further reduced significantly after prolonged high-temperature anneals. The OME technique is capable of generating high-quality single-crystal CoSi_2 layers on patterned narrow silicon lines without the formation of voids. Single-crystal OME layers have also been grown on the nonplanar surfaces of selectively deposited silicon. Ultrashallow junctions have been demonstrated by the out-diffusion of dopants from OME-grown CoSi_2 layers (Herner *et al.* 1998). Various modifications to the OME technique, aimed at simplifying the OME procedures under conventional processing environments, have shown promise. The use of titanium caps (Kim *et al.* 1999) and $\text{Ti}_x\text{Co}_{1-x}$ ($x \sim 0.1$) alloy (Iinuma *et al.* 1998), shown schematically in Fig. 5(c), have been found effective in increasing the thickness of OME CoSi_2 layers that can be grown in one deposition sequence. The advantage of a two-step OME processes (with one vacuum operation) has been pointed out (Tung and Ohmi 2000).

4. Conclusions

As the dimensions of ULSI devices continue to shrink, it becomes more critical for devices to have adequate contacts. Because of many factors including the low cost of ownership and the maturity of the technology,

silicides will remain the preferred contact material for many generations of high-performance devices. Beyond the 60nm generation, however, the present junction extension scheme may have problems performing adequately. Some sort of raised S/D technique, involving the use of silicide or metal, will be likely to be necessary.

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