

SILICIDE-TO-SILICON
SPECIFIC CONTACT RESISTANCE
CHARACTERIZATION
TEST STRUCTURES AND MODELS

Natalie Stavitski

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SPECIFIC CONTACT RESISTANCE
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DISSERTATION

to obtain
the doctor's degree at the University of Twente,
on the authority of the rector magnificus,
prof.dr. H. Brinksma
on account of the decision of the graduation committee,
to be publically defended
on Thursday 3rd of December 2009 at 15.00

by

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born on 15 March 1979
in Kemerovo (Soviet Union)

This dissertation is approved by
the promoter
prof. dr. ir. R. A. M. Wolters
and the assistant promoter
dr. A. Y. Kovalgin

*To my mother Tatiana,
my husband-to-be Mark
and our lovely son Daniel*

v

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1 INTRODUCTION

This chapter provides the relevant theoretical background for further reading. Silicide-silicon contacts and their technological importance are discussed. The motivation of this research is presented. The principle of metal-semiconductor contact formation based on generally-accepted conduction mechanisms is illustrated. The specific contact resistance, which is the important parameter for contact characterisation, is defined. Main methods to measure contact resistance and extract specific contact resistance are presented. Main techniques to characterize one of the important parameters for contact resistance study, i.e., dopant concentration, are shown. Finally, the outline of this thesis is given.

1.1 MOTIVATION OF THIS WORK

1.1.1 LOW RESISTANCE CONTACTS FOR MOS DEVICES

The performance of Metal-Oxide-Semiconductor (MOS) circuits depends strongly on transistor drive current [1]. The drive current of the transistor is determined by the total device impedance, which includes the channel resistance and the parasitic resistances associated with dopant diffusion areas and contacts (Fig. 1.1).

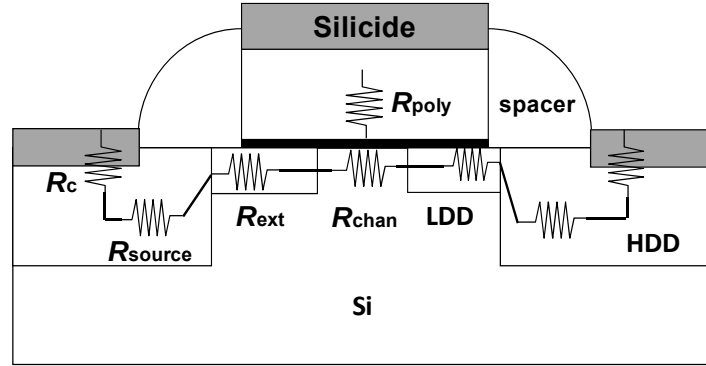


Fig.1.1. Schematic of a MOS device cross-section, showing the parasitic resistances.

Scaling of MOS devices has been a key driving force in Integrated Circuits (IC) industry due to high speed and low power requirements [2]. As device dimensions shrink with each new technology generation, contact resistance scales as a power of the reciprocal dimensions [3]. The contact and metallization processes have to scale accordingly and therefore become increasingly of technological importance [3]-[5]. The field of low resistance contacts to semiconductors comprises two main areas: (i) material science aspects for choosing the appropriate materials and related processing, and (ii) the electrical characterization, which includes a proper definition of contact resistance and its measurement techniques.

1.1.2 SILICIDES ARE THE MATERIALS OF CHOICE

Silicides attracted attention in silicon IC technology because of their low resistivity [6]. Moreover, silicide-silicon contacts show stable electric

characteristics and, compared to metal-silicon contacts, they are stable at higher temperature [7]. The vast majority of the silicides exhibit metallic conductivity [8] and then the silicide-silicon junction behaves as a metal-semiconductor contact. The applications of silicides in silicon technology have been given by Murarka [9] and up to date they are continuing to be the focus of many researches.

Silicide-silicon Schottky barrier diodes were first described by Sze and Lepselter [10]. These diodes found the first application of silicides in integrated circuits. Another application is the so-called poly-silicon shunt: The line resistance of poly-silicon (local) interconnect can be lowered considerably by adding a WSi_2 layer on top of a poly-silicon line [11]. This is also known as the poly-silicon/tungsten silicide (polycide) process. In an existing poly-silicon based process a WSi_2 layer is deposited over the poly-Si layer by Chemical Vapor Deposition (CVD) from WF_6 and SiH_4 . This stack can be patterned in the existing (poly-silicon) etching process. Making use of the low resistivity ($100 \mu\Omega\cdot\text{cm}$) and the high temperature stability of the poly-silicon/ WSi_2 stack ($>1000^\circ\text{C}$) all subsequent high temperature steps such as dopant activation and dielectric processing can be done without compromise.

In order to lower the resistance of gate, source and drain of a MOS transistor, silicides can be formed on these areas [1], [6], [8]. The process consists of the deposition of a metal over the structure (Fig. 1.2) followed by a Rapid Thermal Anneal (RTA) to form the metal-silicon compound. It will be formed only in the areas where the metal is in direct contact with silicon. Hence, it is self-aligned. Therefore, this process is called the Self-Aligned Silicide (SALICIDE) process [1]. After silicide formation the remaining metal over the dielectric areas (spacers and isolation areas) is etched away selectively (Fig. 1.2). The SALICIDE process can be achieved by a one- or two-step RTA. Depending on the choice of metal and annealing conditions, a high- or low- resistivity phase of silicide can be formed after the first RTA. The second RTA is then required to transform the high-resistivity phase into the required low-resistivity phase [9].

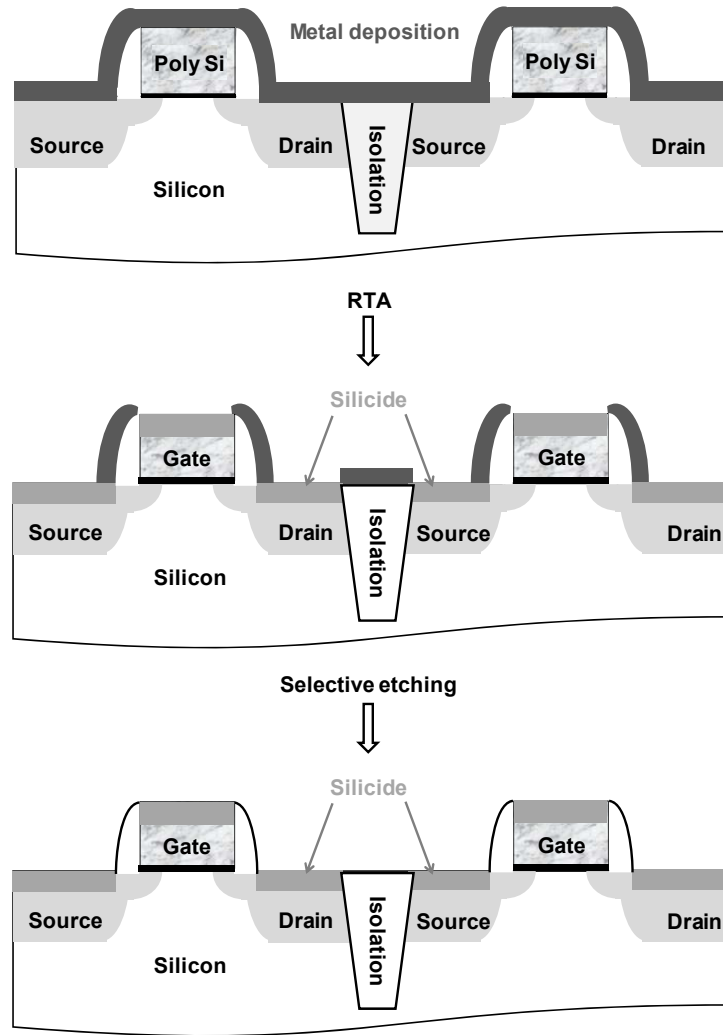


Fig. 1.2. Illustration of SALICIDE process.

The first SALICIDE process in CMOS production was introduced using titanium silicide (TiSi_2) with a maximum formation temperature of 800 – 900 °C [12]. As poly-Si line width decreased with technology node, the thermal stability of this silicide on narrow lines became insufficient. Agglomeration of the silicide and high line resistance occurred [13], [14]. The application of cobalt silicide (CoSi_2) showed an improved stability for poly-silicon line widths down to 40 nm [15], but further downscaling was

limited by a steep increase in the resistance of the silicided lines. For sub-90 nm technology nodes, nickel silicide (NiSi) is the silicide of choice [16]. NiSi can be easily formed on narrow lines without an increase of its resistance [17].

Needless to say that silicide formation by direct metallurgical reaction consumes silicon from the underlying silicon structure (gate, junction). Thus it is important to know how much silicide is formed at the cost of how much silicon (see Table 1.1). This determines where the actual silicide-silicon interface will be located. For a given dopant profile this will in turn determine what the dopant concentration at that interface will be. Apart from the dopant level, the silicide-to-silicon Schottky barrier height (Φ_b) also determines the electrical characteristics of silicide-to-silicon junctions, i.e. the contact resistance. The important properties in this respect of commonly used silicides are summarized in Table 1.1.

Table 1.1. The main properties of commonly used silicides [9].

Silicide	Formation temperature (°C)	Resistivity ($\mu\Omega\cdot\text{cm}$)	Silicon consumed ($\text{\AA}$) per $\text{\AA}$ of metal	Resulting silicide thickness ($\text{\AA}$) per $\text{\AA}$ of metal	Φ_b on n-type (eV)
TiSi ₂	800-900	13-16	2.27	2.51	0.6
CoSi ₂	600-700	18-20	3.64	3.52	0.64
PtSi	300-600	28-35	1.32	1.97	0.87
NiSi	400-600	14-20	1.83	2.34	0.7

1.1.3 THE PURPOSE OF THIS WORK

It is expected that the contact resistance between silicide and source/drain region will dominate the total series resistance (Fig. 1.1) [1], [3]. This has serious consequences for current drive and device speed. The silicide must provide low contact resistance to the doped silicon regions. The reduction of this contact resistance and the corresponding specific contact resistance is an important issue not to compromise the device performance. Thus the ability to accurately measure the silicide-to-silicon contact resistance is essential to contact process development. The main purpose of

this work is to develop and examine various types of test structures and the corresponding models for silicide-to-silicon specific contact resistance characterization.

1.2 SILICIDE-TO-SILICON CONTACTS

Silicide-to-silicon contacts behave as metal-semiconductor contacts, therefore the general theory of metal-semiconductor junctions is applicable.

1.2.1 THE SCHOTTKY BARRIER FORMATION

Metal-semiconductor junctions are essential to any electronic system containing semiconductors. They have been a topic of research for many decades [6], [18], [19]. Metal-semiconductor junctions were first described by Braun in 1874. The first generally accepted theory was developed in 1930s by Schottky and in his honor it is frequently referred as Schottky model [20]. The energy band diagrams, as the basis of the Schottky model, are shown in Fig 1.3.

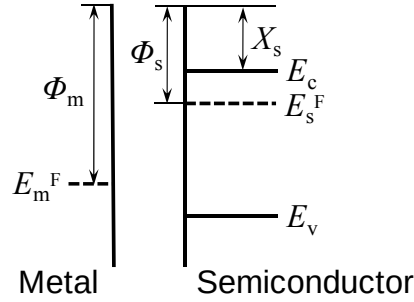
When a metal makes contact with a semiconductor, a barrier (referred to as Schottky barrier) will be formed at the metal-semiconductor interface. To understand how this barrier is formed, we first have to define a few important parameters (see Fig. 1.3). The work function of a metal (Φ_m) is the minimum amount of energy required to raise an electron from the Fermi level (E_m^F) to the vacuum level. Similar, the work function of a semiconductor (Φ_s) is the difference in energy between the Fermi level (E_s^F) and the vacuum level. A work function Φ_i is an energy related to the potential ϕ_i as $\phi_i = \Phi_i/q$, where q is the electron charge. Another important parameter for a semiconductor is the electron affinity X_s , which is the difference in energy between an electron at vacuum level and an electron at the bottom of the conduction band.

Let us consider the case for an n-type semiconductor with a work function less than that of the metal. The energy band diagram when the metal and semiconductor are both electrically neutral and separated from each other is presented in Fig. 1.3a. If the metal and semiconductor make

intimate contact, electrons pass from the semiconductor into the metal and the two Fermi levels are forced to coincide (Fig. 1.3b), which means that the thermal equilibrium is achieved. The resulting potential difference across this region is simply the difference between ϕ_m and ϕ_s . This is called the built-in potential (V_{bi}) of the junction. The basic metal-semiconductor rectifying contact (i.e., metal-semiconductor contact with asymmetric current-voltage characteristics) with Schottky barrier ($q\phi_b$) and built-in potential (qV_{bi}) heights is shown in Fig 1.3b.

Similar considerations can be used to describe metal to p-type semiconductor contacts [18, 20].

(a)



(b)

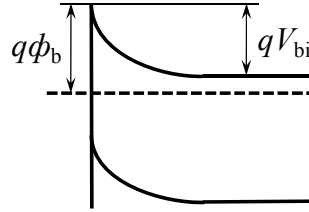


Fig. 1.3. Formation of a barrier between a metal and an n-type semiconductor ($\Phi_m > \Phi_s$), when they are neutral and separated (a) and in intimate contact (b).

1.2.2 CONDUCTION MECHANISMS

There are three main conduction mechanisms to describe the current transport in metal-semiconductor junctions [18]-[20]. For lightly-doped semiconductors the current flows as a result of dominating *thermionic emission*, when electrons are thermally excited over the barrier, see Fig. 1.4a. For heavily-doped semiconductors the tunneling current becomes the dominant transport process, known as *field emission* (Fig. 1.4c). For an intermediate dopant concentration level *thermionic-field emission* dominates with carriers thermally excited to the energy level where tunneling can take place (Fig. 1.4b).

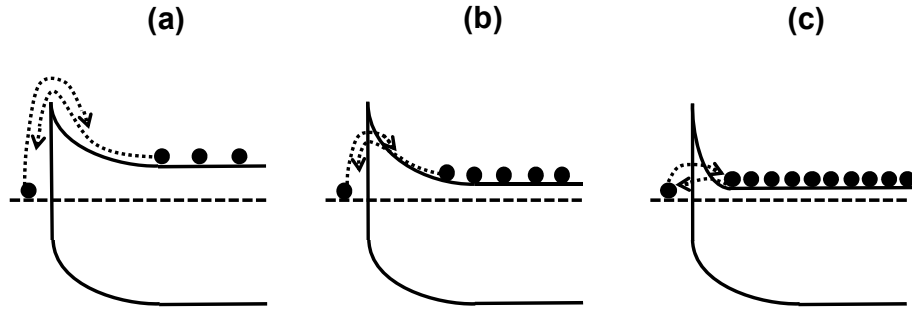


Fig. 1.4. Main conduction mechanisms through metal-semiconductor junctions.

We will first consider the transport of electrons over a potential barrier mainly due to *thermionic emission*. The thermionic emission theory established by Bethe [20] is derived under the assumptions that $q\phi_b$ is much larger than kT (see Eq. 1.1 for parameters definition). Further, a thermal equilibrium is established and the existence of the thermionic current does not affect this equilibrium. Because of these assumptions the current flow depends solely on the barrier height. Electrical current from the semiconductor to the metal is due to electrons with energies high enough to overcome the potential barrier. The current density (J) of such metal-semiconductor contact, dominated by thermionic emission, is given by

$$J = \left[A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \right] \left[\exp\left(\frac{qV}{kT}\right) - 1 \right], \quad (1.1)$$

where T is the temperature, k is the Boltzmann's constant, V is the applied voltage and A^* is the Richardson constant:

$$A^* = 4\pi q k^2 m^* / h^3, \quad (1.2)$$

where m^* is the effective electron mass and h is the Planck constant.

The other conduction mechanism is tunneling through the barrier, which can be described by *the field emission* theory [20]. From the quantum-mechanical considerations, the probability of a triangular barrier to be penetrated by an electron with energy ΔE less than the height of the barrier, is expressed by

$$P = \exp \left\{ -\frac{2}{3} (\Delta E)^{3/2} / E_{00} (qV_{bi})^{1/2} \right\}, \quad (1.3)$$

where E_{00} is a parameter which plays an important role in the tunneling theory and is given by

$$E_{00} = \frac{q\hbar}{2} \left[\frac{N_d}{m^* \varepsilon_s} \right]^{1/2}, \quad (1.4)$$

where ε_s is the permittivity of a semiconductor, $\hbar$ is the reduced Planck constant (i.e., $\hbar = h/2\pi$) and N_d is the dopant concentration.

The tunneling current can be described by the following expression:

$$J_t \propto \exp \left(\frac{-q\phi_b}{E_{00}} \right). \quad (1.5)$$

This equation demonstrates that the tunneling current increases exponentially with $1/\sqrt{N_d}$.

The *thermionic-field emission* is basically a combination of the thermionic and field emission mechanisms and therefore will not be considered separately.

The kT/E_{00} ratio indicates which mechanism dominates [20]. As a rough guide, thermionic emission is expected if $kT \gg E_{00}$. Field emission takes place for $kT \ll E_{00}$ and thermionic-field emission – if $kT \approx E_{00}$.

1.2.3 OHMIC CONTACT AND SPECIFIC CONTACT RESISTANCE

Electrical connections must be made between any semiconductor device or an integrated circuit, and the outside world. These connections are made via *ohmic contacts*. An ohmic contact is a low resistance junction providing similar conduction in both current directions between the metal and the semiconductor [6]. Ideally, the current (I) through the ohmic contact is a linear function of applied voltage (V). From the application point of view, the I - V characteristic of the contact itself does not necessarily have to be linear, provided its resistance is very small compared with the resistance of the device [18]. For this reason an ohmic contact is also often defined as a metal-semiconductor contact that has a negligible (contact) resistance relative to the bulk resistance of semiconductor [19].

A figure of merit of ohmic contacts is the specific contact resistance, ρ_c , expressed in $\Omega \cdot \text{cm}^2$. The classic definition of the ρ_c is the reciprocal of the derivative of current density with respect to the voltage at zero bias [19]:

$$\rho_c = \left(\frac{\partial J}{\partial V} \right)_{V=0}^{-1}. \quad (1.6)$$

The specific contact resistance can not be measured directly in contrast to contact resistance, R_c (Ω). The ρ_c can be calculated from the corresponding R_c as

$$\rho_c = R_c A, \quad (1.7)$$

where A (cm^2) is the *effective contact size*. The ρ_c is a very useful characteristic of ohmic contacts because of its independence of contact area size and it is a convenient parameter while comparing contacts of different sizes.

For metal-semiconductor contacts with lower doping concentrations, the thermionic emission dominates. The current density is given as in Eq. 1.1. Therefore, using Eq. 1.6 and neglecting the small voltage dependence on barrier height,

$$\rho_c = \frac{k}{qA^*T} \exp\left(\frac{q\phi_b}{kT}\right). \quad (1.8)$$

This equation shows that low barrier height should be used to obtain low ρ_c values. It also demonstrates a strong temperature dependence of the ρ_c for a given barrier height.

For contacts with higher dopant concentrations, the tunneling process will dominate. The tunneling current is given in Eq. 1.5 and the corresponding ρ_c can be derived as

$$\rho_c \propto \exp\left(\frac{q\phi_b}{E_{00}}\right) = \exp\left[\frac{2\sqrt{\epsilon_s m^*}}{\hbar} \left(\frac{\phi_b}{\sqrt{N_d}}\right)\right]. \quad (1.9)$$

Equation 1.9 shows that, in the tunneling regime, the ρ_c exponentially depends on the ratio $\phi_b / \sqrt{N_d}$.

In general, for metal-semiconductor junctions at room temperature, the choice of the metal (ϕ_b) and the dopant level in the semiconductor (N_d) will determine the value of ρ_c .

1.3 METHODS TO OBTAIN ρ_c

Electrical measurements can not provide ρ_c directly. The measurements normally result in measured contact/structure resistance, from which the ρ_c is extracted, using additional theoretical considerations [18].

There are methods that are used to roughly estimate the contact resistance. Such methods, e.g., *two-terminal resistor structures* [21] are not meant for the ρ_c extraction. The latter allows to measure interconnects or vias using the so-called *contact string or contact chain structures*, incorporating many contacts (up to 10^4) of one type [18], [21]. The total

measured resistance is divided by the number of sections to obtain the so-called resistance per section, i.e., the value that gives an indication of the contact process quality. The two-terminal contact string is used mainly as a process monitor. It gives neither detailed contact resistance information nor the ρ_c value.

The focus of this work is to study the fundamental contact properties, such as ρ_c . In the following sub-sections, the discussion is limited to commonly used measurement techniques that are relevant for further reading and understanding. In addition, a more detailed evaluation of the current flow and current distribution is essential to reliably extract ρ_c . It requires making dedicated test structures. Such test structures and the corresponding measurement/extraction methods are described in details in sub-sections 1.3.1 – 1.3.3.

1.3.1 SHOCKLEY METHOD

In 1964 Shockley proposed a method to obtain ρ_c using a ladder structure [22]. This method is based on measuring the potential difference between progressing pairs of contacts (Fig. 1.5) and plotting this as a function of the pair distance (Fig. 1.6).

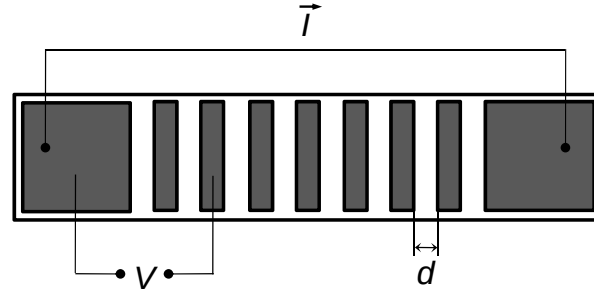


Fig. 1.5. Top view of the Shockley's ladder structure, showing the contacts on silicon.

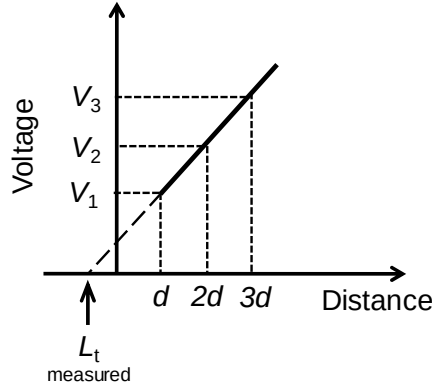


Fig. 1.6. L_t extraction from the Shockley method [22].

The resulting function, when extrapolated to zero potential difference, enables determination of a parameter known as the *transfer length* (L_t). From the known L_t , ρ_c can be calculated according to Eq. 1.10 [22], [23]:

$$L_t = \sqrt{\rho_c / R_{sh}}, \quad (1.10)$$

where R_{sh} is the *sheet resistance* of the underlying silicon. The general physical meaning of L_t is a distance over which most of the current transfers from one material into the other.

This method is also known as the *Transfer Length Method*. This method is abbreviated as TLM in literature [18], but since the other existing method (see section 1.3.2) has unfortunately the same abbreviation, we will refer (in the following sections and chapters) to the former as to the *Shockley method*, to avoid confusion.

Later on, the ladder test structures were improved by making unequally-spaced contacts, with the voltage measured between adjacent contacts [18], [23]. Such a structure is preferred because the current flow is not perturbed by other contact(s) in between (Fig. 1.7).

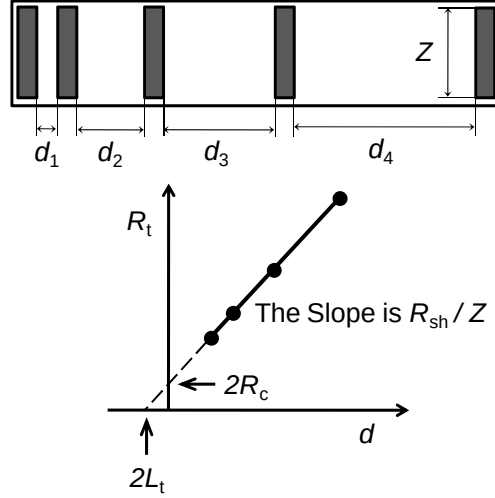


Fig. 1.7. Test structure for Shockley method with various spacings and a plot for L_t , R_c and R_{sh} extraction [18].

The total resistance (R_t) is measured for various contact spacings and plotted versus contact spacing (d). It was shown that for contact length $L \geq 1.5 L_t$ the total resistance between any two contacts is

$$R_t = \frac{R_{sh}d}{Z} + 2R_c \approx \frac{R_{sh}}{Z}(d + 2L_t), \quad (1.11)$$

where Z is the contact width (see Fig. 1.7).

From the plot in Fig 1.7, using Eq. 1.11, three parameters can be extracted: (i) the intercept with the x-axis, at $R_t = 0$, similar to Fig. 1.4 gives $2L_t$, (ii) the intercept at $d = 0$ results in $2R_c$ (*contact resistance*). From the slope of the R_t vs. d , that equals R_{sh}/Z , R_{sh} can be obtained (Fig. 1.7). From Eq. 1.10, the ρ_c value can then be calculated.

To summarize, the Shockley method gives a complete characterization of the contact by providing the sheet resistance, the contact resistance and the ρ_c . This method is commonly used, but the intercept at $R_t = 0$ giving L_t is sometimes not very distinct, which complicates the procedure and can lead to incorrect ρ_c values.

The same principle can be applied to circular structures and it is known in literature as Circular Transfer Length Method (CTLTM) [18].

1.3.2 TRANSMISSION LINE MODEL BY SCOTT

In this sub-section the focus is on the extraction of ρ_c for silicide-to-HDD (Highly Doped Drain) silicon contacts, which is of a great importance for CMOS technology (see section 1.1).

The theoretical expression of the contact resistance contribution to the series source (R_{cs}) and drain (R_{cd}) resistance is expressed in [24] as

$$(R_c)_{\text{Transistor}} = R_{cs} + R_{cd} = \frac{2\sqrt{\rho_c R_{sh}}}{W \tanh(L/L_c)}, \quad (1.12)$$

where ρ_c is the specific contact resistance from the silicide to silicon. The HDD area under the silicide is characterized by R_{sh} , the sheet resistance of silicon, W is the transistor width and L is the length of the silicide contact. L_c is the transfer length as defined in Eq. 1.10. We use another symbol instead of L_t to emphasize that L_c is not obtained using the Shockley method.

The current tends to stay in the silicide as long as possible before moving into the silicon over a distance corresponding to the transfer length L_c . Two limiting cases for the contact resistance could be distinguished.

For $L \gg L_c$, Eq. 1.12 is reduced to

$$R_{cs} + R_{cd} = \frac{2\sqrt{\rho_c R_s}}{W} = R_0. \quad (1.13)$$

Eq. 1.13 corresponds to the ideal case when the contact contribution of the source and drain to the series resistance is independent of the silicided contact length (L).

For $L \ll L_c$, Eq. 1.12 is reduced to

$$R_{cs} + R_{cd} = \frac{2\rho_c}{LW}. \quad (1.14)$$

Eq. 1.14 denotes the case when the contact resistance depends on the contact area. The extraction of the contact resistance contribution to the series source and drain resistance cannot be done using transistor

measurements; therefore appropriate test structures are necessary for contact resistance evaluation.

The Transmission Line Model (TLM) is a useful tool to describe the behavior of the silicide-to-silicon contact resistance. TLM structures have been studied extensively by many researchers [18]. Scott modified the general TLM structures to a structure dedicated for silicide-to-silicon contacts [24, 25]. In the further discussion it will be referred as the “TLM Scott method” or for simplicity just TLM.

The TLM structure consists of a number of silicon fragments. The first fragment is called a reference fragment, not interrupted by silicide segments. Other fragments consist of alternating silicided and unsilicided segments formed by using a silicide-blocking mask (Fig. 1.8).

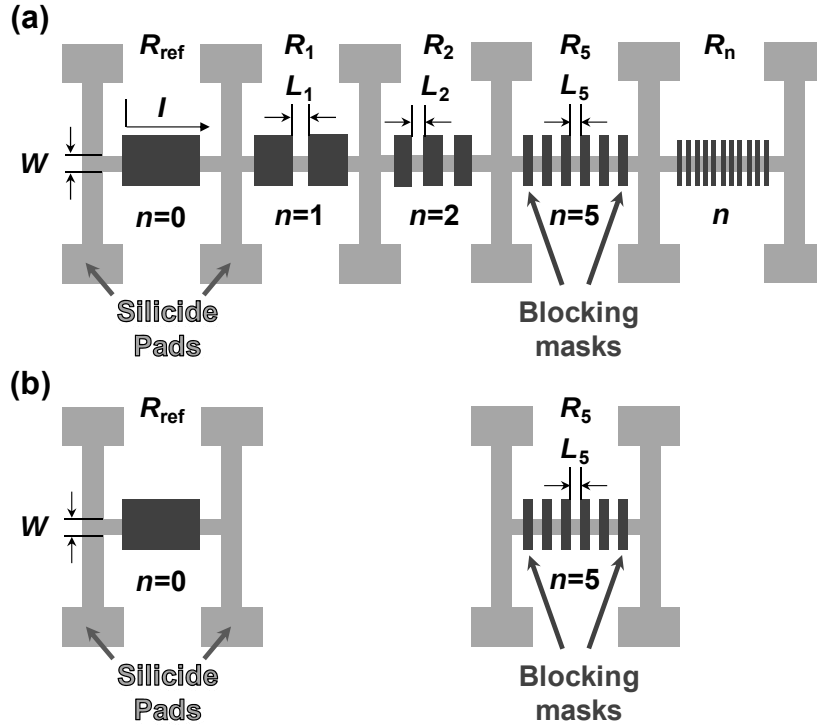


Fig. 1.8. Example of a TLM layout structure (top view). (a) TLM structure, when all fragments are connected. (b) TLM structure, when fragments are separated (only two among many fragments are shown).

The measurement technique involves forcing the current through the reference fragment and through the other fragments interrupted by one, two or n silicided segments and measuring the voltage drop across each fragment. As the fragments have been designed to have equal silicided and non-silicided segments lengths, the difference between the reference resistance and the other resistances is attributed to the contact resistance contribution. Thus, the contact resistance of each structure measured experimentally is expressed as

$$R_c W = \left(\frac{R_n - R_{\text{ref}}}{n} \right) W, \quad (1.15)$$

where R_n is the resistance of the fragment interrupted by n silicided segments, R_{ref} is the resistance of the reference fragment and W is the structure/silicide width.

The theoretical expression of the silicide-to-silicon contact resistance for the test structure as stated by Scott is given as

$$R_c = \frac{2\sqrt{\rho_c R_{\text{sh}}} \tanh(L / 2L_c)}{W}, \quad (1.16)$$

where R_{sh} is the sheet resistance under the silicide, W is the structure/silicide width and L is the length of the silicided segment. L_c is the transfer length, as defined in Eq. 1.10.

The ρ_c is defined as

$$\rho_c = \frac{L_c R_0 W}{2}. \quad (1.17)$$

Once more, two cases for the contact resistance can be expressed, for $L \gg L_c$ Eq. 1.16 reduces to

$$R_c = \frac{2\sqrt{\rho_c R_{\text{sh}}}}{W} = R_0. \quad (1.18)$$

The case expressed by Eq. 1.18 corresponds to low contact resistance, thus all the current flows through the silicide. The value of R_0 obtained with the TLM structure using the long silicided segments is equal to the limit achieved for a transistor with a long silicided contact (Eq. 1.13).

For $L \ll L_c$ Eq. 1.16 reduces to

$$R_c = \frac{L}{W} R_{sh}. \quad (1.19)$$

Eq. 1.19 shows the case when only a fraction of the current will flow in the silicided segment of the TLM. In the transistor all the current has to enter the silicide, resulting in lower drive current when $L \ll L_c$. Whilst plotting $R_c W$ as a function of silicide length L , the $R_c W$ saturates for $L \gg L_c$ to the maximum value of $R_0 W$. From this, R_0 can be extracted.

The TLM contact resistance given by Eq. 1.16 can be expressed as

$$\frac{R_0 + R_c}{R_0 - R_c} = \exp\left(\frac{L}{L_c}\right). \quad (1.20)$$

Plotting $\ln((R_0 + R_c)/(R_0 - R_c))$ as a function of L allows to extract the L_c . Using the extracted L_c and R_0 values, the $R_c W$ product can be plotted as a function of L to verify the theoretical curve (Eq. 1.16). Finally, the specific contact resistance ρ_c can be calculated (Eq. 1.17).

1.3.3 CROSS-BRIDGE KELVIN RESISTOR

Cross-Bridge Kelvin Resistor (CBKR) structures are widely used to characterize metal-semiconductor contacts [6], [18]. The measurement is simple and not time-consuming, ρ_c is believed to be easily extracted from the measured Kelvin resistance and therefore these structures are often adapted within a parametric test. A standard general four-terminal CBKR test structure is shown in Fig. 1.9.

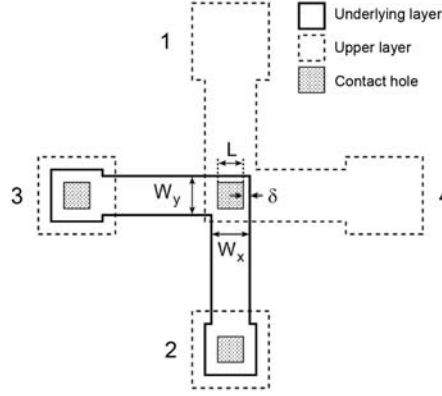


Fig. 1.9. Four-terminal CBKR structure (top view) with geometry parameters definition.

The measurement principle consists of forcing the current (I) between pads 1 and 2 and measuring the voltage drop (V_{34}) between pads 3 and 4. The actually measured Kelvin resistance R_k can then be found as

$$R_k = \frac{V_{34}}{I}. \quad (1.21)$$

In the 1D-Model approach [26], the ρ_c can be calculated directly from the contact area A and R_k , assuming that the resistance due to the voltage drop across the actual contact (R_c) equals R_k :

$$\rho_c = R_c A = R_k A. \quad (1.22)$$

The 1D-Model does not account for the current flowing in the overlap region (δ) between the contact edge and the underlying layer sidewall. In the ideal case with $\delta = 0$ (Fig. 1.10a), the voltage drop is $V_{34} = IR_c$. For $\delta > 0$ (Fig. 1.10b), the lateral current flow gives an additional voltage drop that is included in V_{34} , leading to higher R_k .

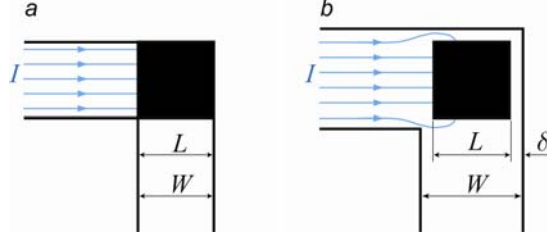


Fig. 1.10. Schematic of a current flow in a four-terminal CBKR test structure. (a) Ideal case with current flow in the contact only ($\delta = 0$). (b) Real case with current flowing through the contact and the overlap region ($\delta > 0$).

In that case the so-called 2D-Model should be applied [26]. This analytical model was proposed by Schreyer and Saraswat to correct for the current crowding effect [26], [27]. The measured R_k is then a sum of the R_c and the resistance R_{geom} , due to the current flow around the contact in the overlap region (Eq. 1.23). The ρ_c can further be extracted from Eq. 1.24, where R_{sh} is the sheet resistance of the underlying layer. The contact geometry parameters are defined in Fig. 1.7.

$$R_k = R_c + R_{\text{geom}}, \quad (1.23)$$

$$R_k = \frac{\rho_c}{A} + \frac{4R_{\text{sh}}\delta^2}{3W_x W_y} \left[1 + \frac{\delta}{2(W_x - \delta)} \right]. \quad (1.24)$$

In addition to the aforementioned models, there is also a 3D-approximation, which takes into account the thickness of semiconductor (for the case of metal-semiconductor contacts), however no analytical model exists and a simulator is required [28, 29].

1.4 DOPANT CONCENTRATION PROFILING

As mentioned in the discussion on the metal-semiconductor junctions, the dopant level in the semiconductor determines the actual contact resistance to a large extent. Therefore, the basic principles of dopant concentration measurement techniques, which were used in this work, are further discussed.

1.4.1 SECONDARY ION MASS SPECTROMETRY

Secondary Ion Mass Spectrometry (SIMS) is one of the most powerful techniques for dopant concentration profiling [11, 18]. The technique is element specific and is capable of detecting all relevant elements as well as isotopes and molecular species.

The basis of SIMS is destructive removal of material from the sample by sputtering and the analysis of the ejected material by a mass analyzer. A primary ion beam bombards the sample and secondary atoms/ions from the sample are ejected. The mass-to-charge ratio of these ions is analyzed.

Depth profiling is commonly done by *dynamic* SIMS, e.g., the intensity of one peak for one particular mass-to-charge is recorded as a function of time as the sample is sputtered at a high sputter rate. It is the major strength of SIMS to provide quantitative depth profile. Plots of secondary ion yield of selected mass versus sputtering time can be converted to dopant concentration versus depth (see Fig. 1.11). It is normally done by using the ion implanted standards with similar composition, which are very accurate (implant dose accuracy of $\sim 5\%$).

SIMS analysis is the most sensitive among the beam techniques. The detection limits for some elements can be $10^{14} - 10^{15} \text{ cm}^{-3}$, proving very little

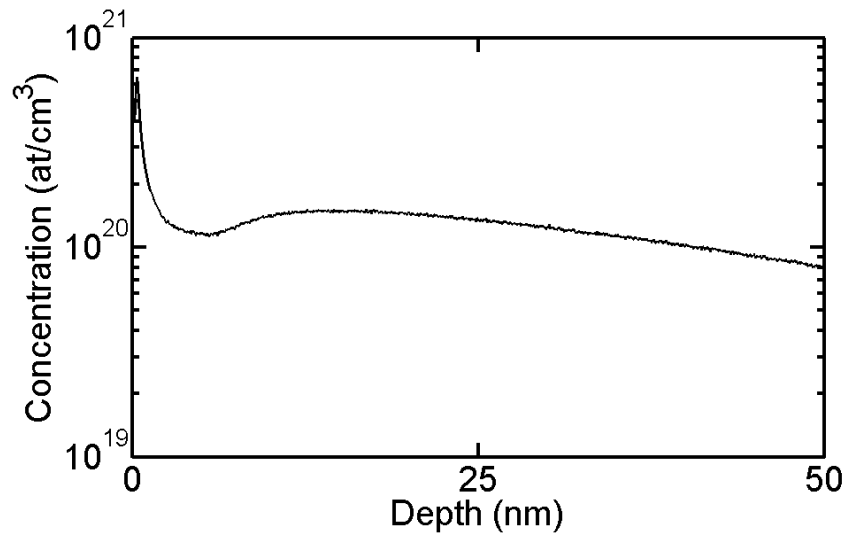


Fig. 1.11. An example of a SIMS dopant concentration profile (from the results of this work).

background interference signal. Lateral resolution can be as small as $0.5\ \mu\text{m}$ with the depth resolution of 1 to 5 nm [18].

SIMS determines the *total* impurity/dopant concentration.

1.4.2 SPREADING RESISTANCE PROFILING

The Spreading Resistance Probe (SRP) technique is mainly used nowadays for resistivity and dopant concentration depth profiling [11], [18].

The instrument consists of carefully aligned probes that are stepped along the beveled semiconductor surface and the resistance is measured at each location. The sample is prepared by mounting it on a bevel block with melted wax. The bevel block is inserted into a well-fitting cylinder, and the sample is lapped using a polishing compound [18], [30]. The sample is then positioned in the measurement apparatus with the bevel edge perpendicular to the probe stepping direction. The bevel angle is usually measured using a well-calibrated profilometer.

The conversion of SRP data to a dopant concentration profile (Fig. 1.12) is a complicated task that involves data smoothing to reduce measurement noise, a deconvolution algorithm, and a correct model for the contact [30].

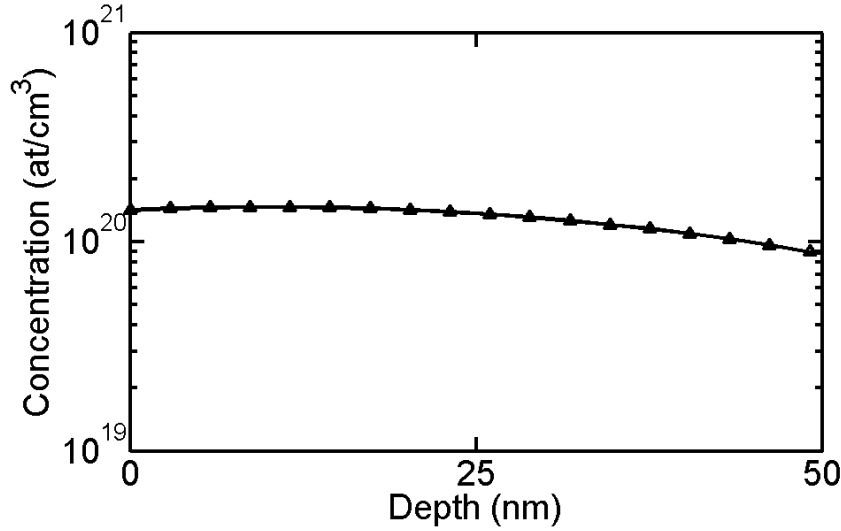


Fig. 1.12. An example of a SRP dopant concentration profile (from the results of this work).

The spreading resistance profiling technique is a comparative technique. Calibration curves are generated for a particular set of probes at a particular time using samples of known resistivity.

SRP analysis determines the *electrically active*, not the total dopant concentration.

1.5 OUTLINE OF THIS THESIS

*"If you can't explain it simply,
you don't understand it well enough"*
by Albert Einstein

The thesis consists of six chapters.

The relevant theoretical background for further reading and the motivation of this research have been discussed in CHAPTER 1.

CHAPTER 2 demonstrates the importance of using optimized TLM structures to measure silicide-to-silicon contact resistance. NiSi and PtSi have been chosen as the silicides and the TLM structures for various dopant levels of n- and p-type silicon have been evaluated. The measurement limitations and accuracy of the ρ_c extraction from the optimized TLM structures are discussed.

CHAPTER 3 provides a novel database for NiSi-to-silicon contact resistance for a broad range of doping levels, using PtSi as a reference. The origin of the low ρ_c values obtained has been investigated. The presence of doping segregation has been examined using SRP and SIMS depth profiling techniques. The Ni ion implantation experiments were performed to clarify the role of the impact of the silicide-silicon interface.

CHAPTER 4 presents the experimental confirmation of the minimum of the ρ_c value, which could be accurately extracted using CBKR structures. For this purpose, low resistivity metal-to-metal CBKR structures have been fabricated and evaluated. In addition, a model is presented to account for the actual current flow and a method for reliable ρ_c extraction is created.

CHAPTER 5 discusses the application of CBKR structures to study silicide-to-silicon ρ_c . The experiments have been performed for four different silicides, i.e., NiSi, PtSi, TiSi₂ and CoSi₂. The silicides were

processed using SALICIDE and co-sputtering techniques to obtain different contact geometry.

Finally, this thesis is summarized in CHAPTER 6.

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2

TLM STRUCTURES EVALUATION

The purpose of this chapter is to demonstrate the importance of using optimized TLM structures to measure silicide-to-silicon contact resistance. We have chosen NiSi and PtSi as the silicides and evaluated the structures for various dopant levels of n- and p-type silicon. The measurement limitations and accuracy of the ρ_c extraction from the optimized TLM structures are discussed.

In the first section of this chapter we demonstrate preliminary results on the PtSi-to-silicon ρ_c that was extracted from *non-optimized* TLM structures. Based on this, the necessity to further optimize the design of these structures is demonstrated. The optimization of TLM structures in terms of silicide lengths and the number of segments is detailed in the second section. The optimized structures to measure silicide-to-silicon contact resistance with NiSi and PtSi as silicides were processed for various dopant levels of n- and p-type silicon. The process flow information can be found in the third section. The evaluation of the structures in terms of material and electrical analysis is described in section 2.4. The necessity of applying TEM analyses to examine geometries and uniform silicide formation is demonstrated. The measurement limitations in terms of the lowest dopant concentration and accuracy of the ρ_c extraction from the optimized TLM structures are discussed. The structures were evaluated at different temperatures and the results were in agreement with the theory. The optimized structures provided a higher accuracy for the ρ_c extraction.

This chapter is based on the following publications:

N. Stavitski, M. J. H. van Dal, R. A. M. Wolters, A. Y. Kovalgin, and J. Schmitz, "Specific contact resistance measurements of Metal-Semiconductor Junctions," in *Proc. IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Austin, TX, pp. 13-17, Mar. 2006.

N. Stavitski, M. J. H. van Dal, A. Lauwers, C. Vrancken, A. Y. Kovalgin, and R. A. M. Wolters, "Evaluation of transmission line model structures for silicide-to-silicon specific contact resistance extraction," *IEEE Trans. Electron Devices*, vol. 55, pp. 1170-1176, May. 2008.

2.1 MOTIVATION

2.1.1 BACKGROUND

The SALICIDE process is commonly used to reduce the source, drain and gate resistances in submicron MOS devices (section 1.1.1, section 1.1.2, [1], [4]). NiSi is being used as the silicide of choice for CMOS devices in the 90-nm technology node and beyond (section 1.1.2, [5]). NiSi has several advantages over TiSi_2 and CoSi_2 . These advantages include low sheet resistance on narrow lines and low silicon consumption (section 1.1.2, [6]-[11]). The latter is important for the formation of contacts to ultra shallow source/drain junctions.

For the contact process, the ρ_c is a crucial parameter. A well-defined method for extraction of its value is required (section 1.1.3). Several methods for contact resistance measurement such as CBKR (section 1.3.3, [12], [13]), CTLM [14], Shockley method (section 1.3.1, [15]) and Two-terminal resistor structures [15] were introduced in the past.

In recent years, there is a trend towards using TLM structures as they can easier be embedded in the standard self-aligned silicide CMOS process. The advantage of the TLM structure over the CBKR structure is that in TLM structures the silicide segments and the contacts pads are made in one single silicide process step. An attractive method for direct contact resistance measurement of silicide to silicon contacts and the extraction of the specific contact resistance was proposed by Scott (section 1.3.2, [16]). This method was extensively evaluated for TiSi_2 , demonstrating its advantages including the relative simple processing of the test structures [16]. However, until now very little attention has been paid to the evaluation of these structures for NiSi and the other important silicides, such as PtSi, used in the fabrication of Schottky barrier devices [17]. Furthermore, issues such as short contact (silicide) lengths, n- or p- type Si and a wide range of dopant concentrations were not yet addressed.

2.1.2 PRELIMINARY EXPERIMENTS

The first phase of the TLM structures characterization was dedicated to examine the existing mask-set design, developed at the Interuniversity Microelectronics Center (IMEC) in Leuven.

For the TLM contact resistance study (100) p-type Si wafers were used as starting material on which active areas were defined by Shallow Trench Isolation (STI). Channels were defined by I-line lithography and dopant concentrations were achieved by low-dose well implantations B (180 keV) and P (380 keV) for the p-well and n-well, respectively. Highly Doped Drain (HDD) implantations were carried out for corresponding wells: As (20 keV) for n-HDD and B (2keV) for p-HDD and followed by spike annealing at 1100 °C. For the TLM, a silicide blocking layer ($\text{SiO}_2/\text{Si}_3\text{N}_4$) was deposited and patterned using I-line lithography. The segment lengths range from 0.05 to 3 μm and have a width of 8 μm . The smaller segments (0.25 μm to 50 nm) were defined with e-beam lithography. Finally a 13-nm Pt layer was deposited and silicide was formed by anneal (500 °C for 30 sec). The unreacted metal was selectively removed by wet etching.

The PtSi-to-silicon specific contact resistance was extracted using the Scott method as explained in section 1.3.2. The fit with the Scott method is shown in Fig. 2.1. The calculated values of specific contact resistance of PtSi-to-silicon are $5.3 \times 10^{-8} \Omega \cdot \text{cm}^2$ (to n-HDD) and $9.3 \times 10^{-8} \Omega \cdot \text{cm}^2$ (to p-HDD).

The measured R_{ref} and R_n values (section 1.3.2) have been given considerable examination. These values revealed a small difference, causing a significant relative error during R_c calculation (Eq. 1.15). Another problem was a non-homogeneous distribution of the measured data on the fitting curve, i.e., $R_c W$ vs. L (see Fig. 2.1), which is determined by the silicide length L . Moreover, the latter was complicated due to a short circuit, caused by a mistake in design (see Table 2.1). These data points were measured after several efforts have been put in applying Focused Ion Beam (FIB) technique and manually repairing the short circuit to allow the measurement. Furthermore, a visual inspection of the silicides by Scanning Electron

Microscopy (SEM) revealed length mismatch, as a result of using two lithography techniques, i.e., I-line and E-beam (see Table 2.1).

Summarizing, the examination of the existing design revealed several problems: (i) a significant relative error during R_c calculation, (ii) a non-homogeneous distribution of the measured data on the fitting curve, i.e., $R_c W$ vs. L , (iii) a short circuit, caused by a mistake in design, (iv) length mismatch, as a result of using two lithography techniques. Moreover, the continuous need to lower the contact resistance [18] would require an increase in amount of silicide segments (n) (section 1.3.2) to prevent the relative error during R_c calculation (Eq. 1.15).

For these reasons, a set of optimized TLM test structures was designed and realized with NiSi and PtSi contacts to silicon. Electrical characterization and evaluation of these structures were performed for various dopant concentrations of n- and p-type Si, and at different measurement temperatures.

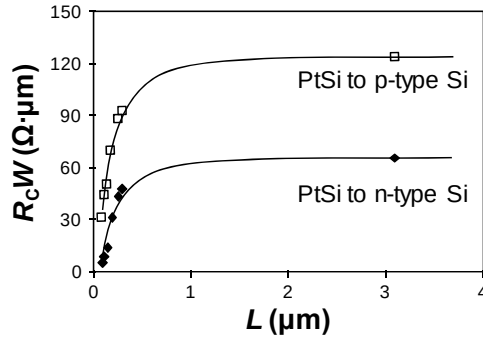


Fig. 2.1. Contact resistance values for PtSi measured (dots) vs. calculated (lines) using the Scott method.

2.2 TEST STRUCTURES OPTIMIZATION

In the following sections silicide-to-silicon contact resistance is investigated using a set of *optimized* test structures. Each TLM structure consists of fragments with silicided segments of varying lengths, and the reference fragment, not interrupted by silicide segments (Fig. 1.8). For the optimized TLM structures, the separated-fragment configuration was chosen (Fig. 1.8b). The purpose was to optimize the measurements and minimize

possible mask design errors, existed for the old configuration (Fig. 1.8a). Further the optimization is done in terms of the silicides lengths and the number of segments.

One known accuracy problem of this method, while measuring low values of contact resistance, is a relatively small difference between R_{ref} and R_n (Eq. 1.15), that might result in a low $(R_n - R_{\text{ref}})$ value, and hence, an increased calculation error. This error might be reduced by increasing the number of silicide segments per each fragment of TLM structure, which would cause higher R_n values, reducing the relative error during the R_c calculation. To optimize the TLM structures, we increased the number of silicide segments per fragment from $n = 1, 2, 6, 12 \dots 60$ for the *non-optimized* structures to $n = 5, 10, 15, 30 \dots 150$. The design is chosen such that the total amount of metal for silicide formation is the same for each fragment.

Yet another factor that affects the accuracy of ρ_c extraction is a non-uniform distribution of the points on the $R_c W(L)$ graph (Eq. 1.16). Based on our previous experience, we adjusted the lengths of the silicide segments (L) to improve this uniformity (see Table 2.1). In addition, our optimized TLM structures had two different silicide widths (W). The values of R_c should be related to the corresponding silicide width (Eq. 1.15) according to

$$R_{c1}W_1 = R_{c2}W_2. \quad (2.1)$$

So by varying W , the measurements results can be verified and more statistical data can be provided to make a better fit.

Another complication of the data analysis is that the actual silicide lengths always deviate from the blocking mask dimensions. In previous experiments, two different techniques, i.e., I-line and e-beam lithography, were used for defining the feature dimensions. The present optimized structures were realized by using only DUV lithography, to minimize the size mismatch caused by two different techniques. A comparison of both mask designs is presented in Table 2.1.

Table 2.1. OLD vs. NEW mask comparison for TLM structures.

	OLD MASK				NEW MASK			
Structure	n	L silicide (μm)	Litho		n	L silicide (μm)	Litho	
R_{ref}	0	-	I-line		0	-	DUV	
R_n	1	3	I-line		5	3	DUV	
R_n	2	1.5	I-line	Short	10	1.5	DUV	No short
R_n	No	No	I-line		15	1	DUV	
R_n	6	0.5	I-line	Short	30	0.5	DUV	No short
R_n	12	0.25	E-beam		60	0.25	DUV	
R_n	15	0.2	E-beam		75	0.2	DUV	
R_n	20	0.15	E-beam		100	0.15	DUV	
R_n	30	0.1	E-beam		150	0.1	DUV	
R_n	40	0.075	E-beam		No	No	-	
R_n	60	0.050	E-beam		No	No	-	

Summarizing the above considerations, each optimized TLM structure consisted of a reference fragment without silicide segments and a number of fragments, where each fragment comprised n silicided segments of length L . The number of segments n was 5, 10, 15, 30, 60, 75, 100 and 150. The optimized TLM structures comprised of areas with silicide lengths (L) ranging from 0.1 to 3 μm and two different silicide widths (W) of 2 and 8 μm .

2.3 FABRICATION OF OPTIMIZED TEST STRUCTURES

The (100) p-type silicon wafers were used as a starting material to fabricate the optimized TLM structures. The process flow for the TLM test structures fabrication is summarized in Fig 2.2. The active areas were defined by Shallow Trench Isolation and the implanted regions were defined by I-line lithography. Dopant concentrations were achieved by low-dose well implantations of B (180 keV) and P (420 keV) for the p-well and n-well, respectively. As and B implantations, followed by spike annealing at

1100 °C, were carried out for n-HDD and p-HDD areas, respectively. The doses and energies were adjusted to cover the $10^{17} - 10^{20} \text{ cm}^{-3}$ dopant concentration range.

In order to verify the actual concentrations, the same implantation recipes were applied to blanket wafers, and the total dopant concentration and the concentration of electrically active impurities were determined by SIMS (section 1.4.1) and SRP (section 1.4.2) technique, respectively. The relevant active concentrations used in this work were taken at the certain depth, according to the amount silicon consumed during the silicide formation.

Deep junctions were chosen in order to enable an accurate measurement of the dopant profiles and therefore to minimize errors during the extraction of the specific contact resistance. Moreover, the sheet resistance of deeper junctions is less sensitive to changes due to silicon consumption during silicide formation and to variations of the doping profile in the area of silicide-silicon junction.

For the TLM structures, a silicide blocking layer ($\text{SiO}_2/\text{Si}_3\text{N}_4$), representing the standard Si protection in the SALICIDE process, was deposited and patterned on the n-HDD and p-HDD areas using DUV lithography. Finally, a 10-nm thick Ni layer or a 13-nm thick Pt layer was deposited, and the silicide was formed by either two-step annealing (300 °C for 43 s followed by 470 °C for 43 s) for NiSi or one-step annealing (500 °C for 30 s) for PtSi. In both cases, the unreacted metal was selectively removed by wet etching.

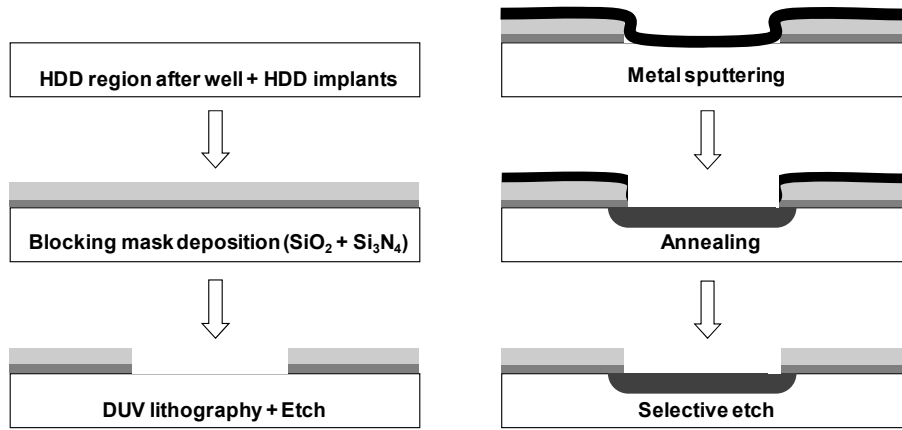


Fig. 2.2. The process flow to fabricate the optimized TLM test structures.

The aforementioned experiments were carried out in the clean room (P-Line) at IMEC, Leuven, Belgium.

2.4 RESULTS AND DISCUSSION

2.4.1 TEM ANALYSIS

The actual silicide lengths and the shape of the silicide-silicon interface for NiSi and PtSi were verified by Transmission Electron Microscopy (TEM) analysis using a FEI Tecnai F30ST TEM operated at 300 kV. The samples were prepared by a combination of mechanical polishing and FIB200 technique. A low-temperature PECVD silicon nitride layer and a sputtered Pt layer were deposited prior to the sample preparation for a better image contrast and to avoid charging.

From the TEM analysis, both NiSi and PtSi revealed good quality in terms of uniform silicide formation within the segments (Fig. 2.3a). The silicide segment lengths were always larger than the corresponding blocking mask dimensions, due to the lateral growth of the silicide (Fig. 2.3b). This growth (ΔL) varied from 0.025 to 0.035 μm for NiSi and from 0.035 to 0.05 μm for PtSi, on each side of the segment. The actual silicide length was independent of dopant type and concentration. For the smallest segments, the lateral growth of PtSi became comparable with the designed spacing between the silicides. In some cases this led to a short circuit or a complete

merge of the silicide segments (Fig. 2.3c). As a result, these fragments showed a much lower R_c and were therefore taken out of the analysis. Although this problem did not compromise the data analysis, in the next generation of TLM structures with similar dimensions, for silicides with a relatively large lateral growth, spacing between the smallest segments should be at least twice the expected lateral growth ($2\Delta L$). For example, if the smallest spacing is $0.1\text{ }\mu\text{m}$ with an expected ΔL_{max} of $0.05\text{ }\mu\text{m}$, the contribution to the total growth is the same ($2 \times \Delta L_{\text{max}} = 0.1\text{ }\mu\text{m}$). To yield valid fragments, the spacing should then be preferably twice total growth, i.e., $2 \times 2\Delta L_{\text{max}} = 0.2\text{ }\mu\text{m}$. An additional method to reduce this effect could be the reduction of the silicide segment width W (Fig. 1.8). In our case, the amount of such abnormal fragments for PtSi for $W = 2\text{ }\mu\text{m}$ was much smaller than that for $W = 8\text{ }\mu\text{m}$, obviously reducing the probability of the merge effects.

PtSi segments were equally thick, independent of segment length or dopant type (Fig. 2.3a). However, in the case of NiSi segments, homogeneous thickness distribution was confirmed for the p-HDD area only, while for the n-HDD area the silicide segments thickness deviations of 20% – 30% were observed (Fig. 2.3d).

It should be noted that it was not possible to perform a valid fit of the measured data by the Scott method without knowing the exact silicide lengths for the small segments. This underlines the importance of the profile verification by TEM.

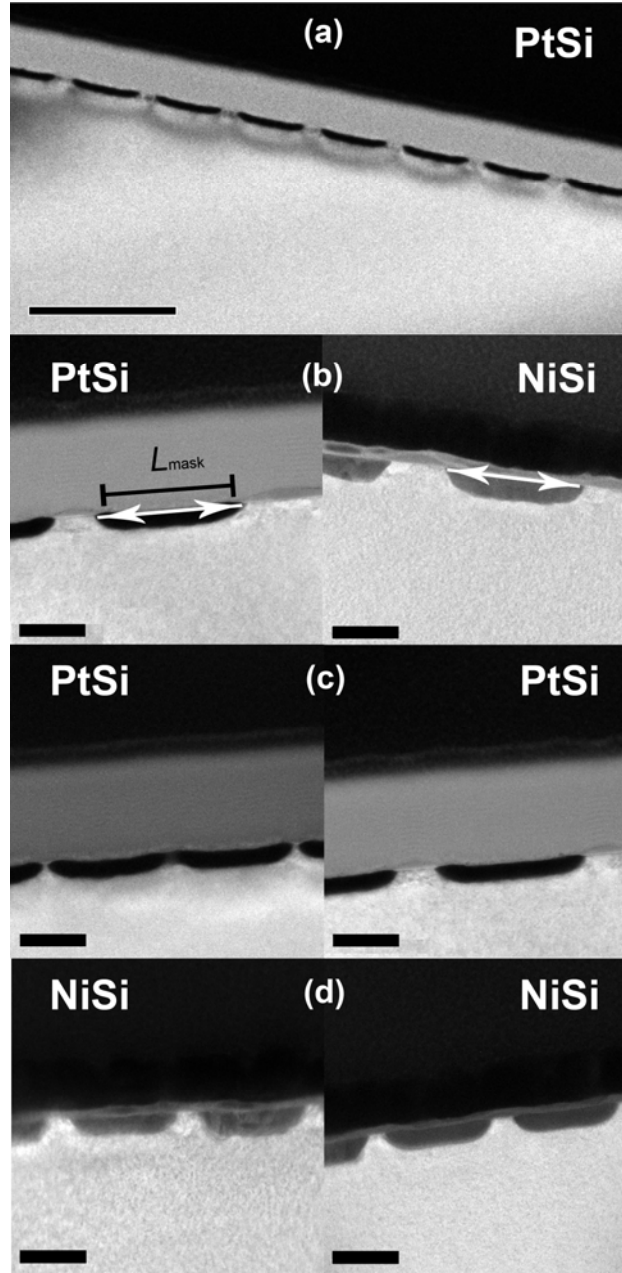


Fig. 2.3. (a) TEM cross-section of PtSi on n-HDD for $n = 100$. (b) The arrows represent PtSi and NiSi (p-HDD, $L_{\text{mask}} = 0.2 \mu\text{m}$) actual silicide length and show the lateral expansion. The arrows depict the location where the length was measured. (c) PtSi merged segments for $n = 150$ (left) and non-merged segments for $n = 100$ (right). (d) NiSi segments for $n = 150$, non-equally thick on n-HDD (left) and equally thick on p-HDD (right). The scale bar equals $0.5 \mu\text{m}$ (a) and $0.1 \mu\text{m}$ (b, c and d).

2.4.2 VERIFICATION FOR DIFFERENT SILICIDE WIDTHS

As mentioned in section 2.2, by varying W , the measurement results can be verified accordingly to Eq. 2.1 and therefore more statistical data can be provided to make a better fit. The measurements of each TLM fragment (with a given n and L) resulted in two sets of I - V curves, for $W = 2 \mu\text{m}$ and $W = 8 \mu\text{m}$. In Fig. 2.4, the I - V curves for identical fragments, measured at 18 different locations on the wafer, are presented.

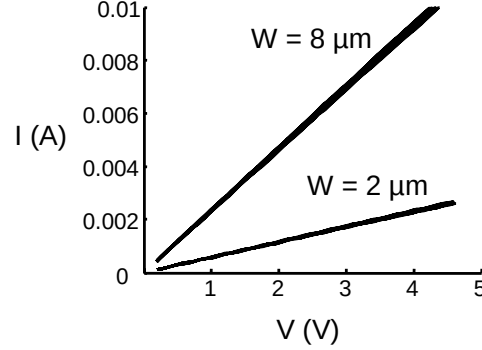


Fig. 2.4. Two sets of I - V curves for NiSi on a p-HDD ($N_a = 1.4 \cdot 10^{20} \text{ cm}^{-3}$) fragment with $n = 30$; each set corresponds to a given silicide width, i.e. $W = 2 \mu\text{m}$ and $W = 8 \mu\text{m}$.

The resistance values (i.e., R_{ref} and R_n) of all the fragments were extracted from such I - V curves, and the R_c values were calculated (Eq. 1.15). The $R_c W$ product (i.e., the R_c values normalized to the silicide width) versus the silicide length was plotted for both W (see Figs. 2.5 and 2.6) to verify the validity of Eq. 2.1 and to extract the specific contact resistance. The $R_c W$ values obtained for the two different silicide widths matched very well for both silicides and for different dopant types, indicating their validity (Figs. 2.5 and 2.6).

2.4.3 FITTING WITH THE SCOTT METHOD

The fits of the $R_c W$ products versus L for the NiSi and PtSi contacts to the n-HDD and p-HDD areas were analyzed for different dopant levels (Figs. 2.5 and 2.6).

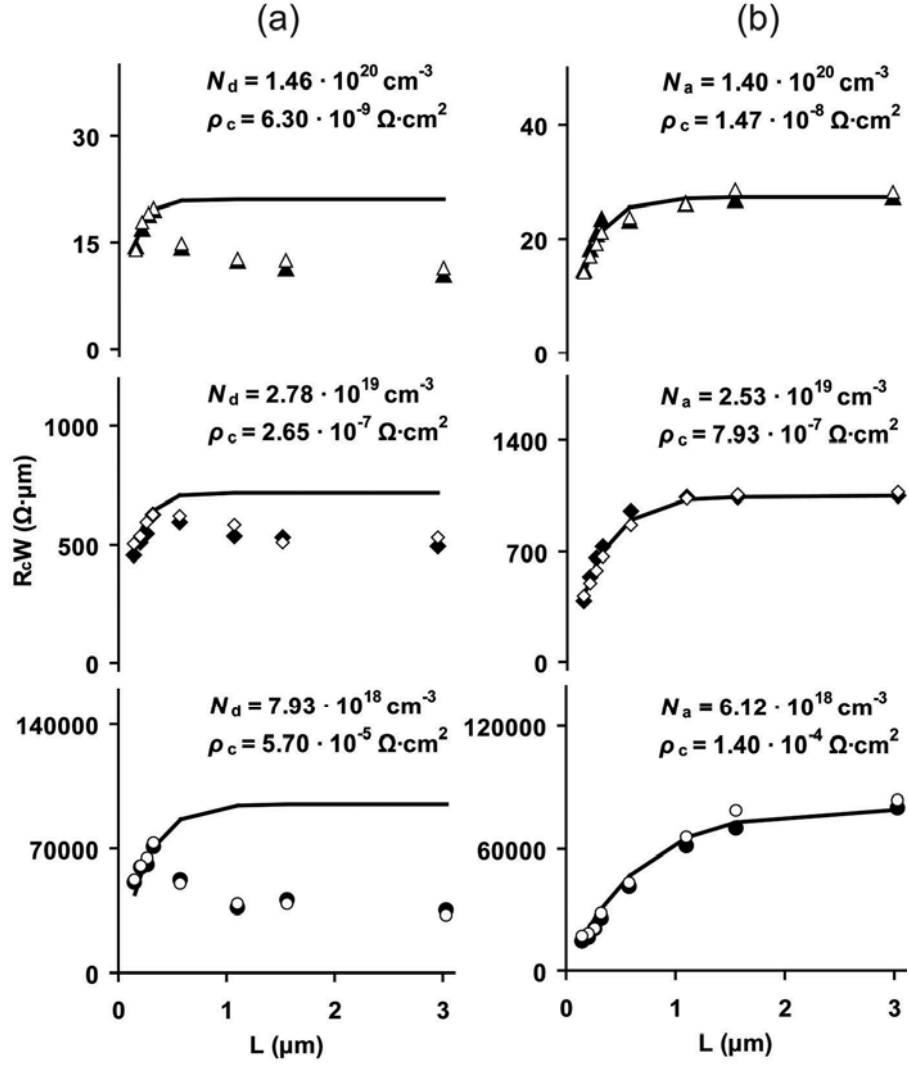


Fig. 2.5. Contact resistance values for NiSi contacts to n-HDD (a) and p-HDD (b) areas for different dopant levels (N_a and N_d). Solid symbols represent measured data for silicide width $W = 2 \mu\text{m}$, open symbols for $W = 8 \mu\text{m}$. Each symbol type corresponds to certain dopant level. Lines are fits, obtained by the Scott method, from which ρ_c is extracted.

Based on this analysis, two Scott regimes, i.e. for L comparable with L_c (Eq. 1.17) and for $L \gg L_c$ (Eq. 1.18) were observed. For PtSi to p-HDD contacts (Fig. 2.6b), the R_cW was constant for $L > 1 \mu\text{m}$ according to Eq. 1.18, while for $L < 1 \mu\text{m}$, the R_cW was L dependent (Eq. 1.19). The L_c for

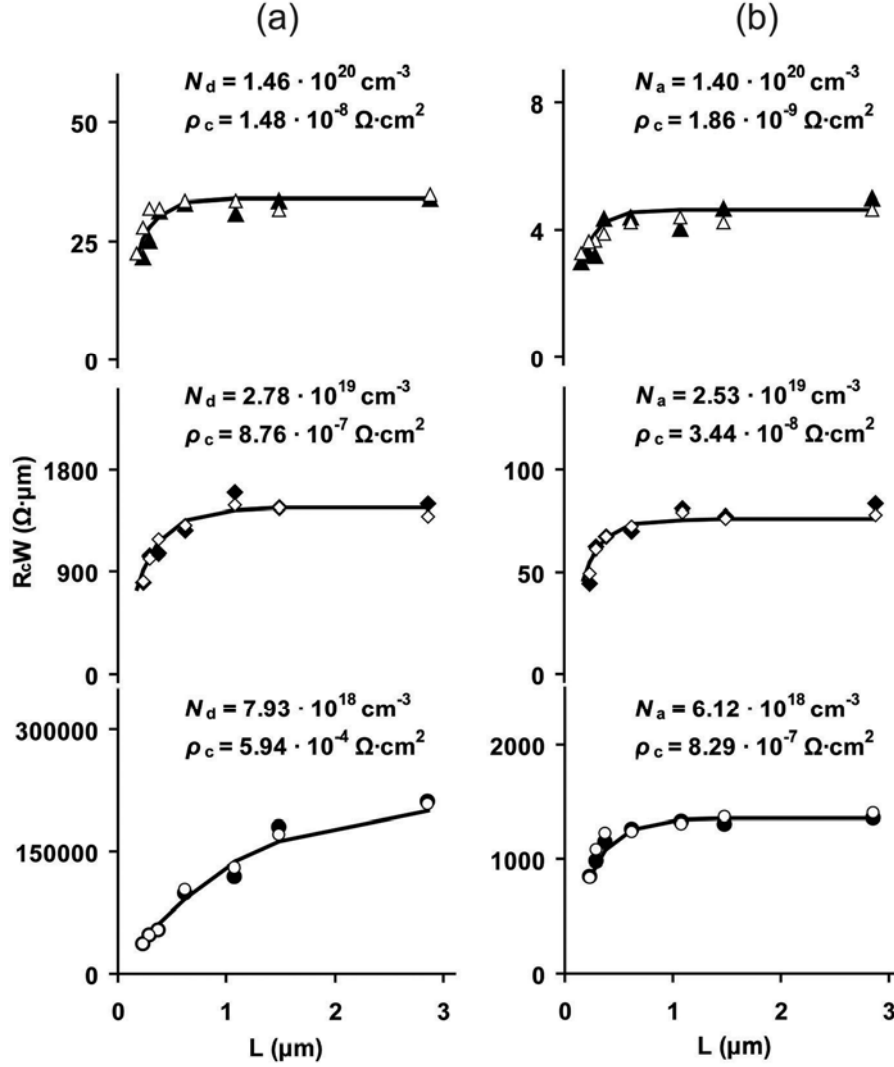


Fig. 2.6. Contact resistance values for PtSi contacts to n-HDD (a) and p-HDD (b) areas for different dopant levels (N_a and N_d). Solid symbols represent measured data for silicide width $W = 2 \mu\text{m}$, open symbols for $W = 8 \mu\text{m}$. Each symbol type corresponds to a given doping level. Lines are fits, obtained by the Scott method, from which ρ_c is extracted.

PtSi ranged from 0.08 μm to 0.122 μm , depending on the p-HDD dopant level.

The R_cW values and the corresponding extracted ρ_c increased with decreasing the dopant concentration, as depicted in Figs. 2.5 and 2.6, in accordance with the tunnelling mechanism (section 1.2.3, Eq. 1.9).

The $R_c W$ values for NiSi to p-HDD contacts agreed very well with the fit, obtained by Scott method (Fig. 2.5b), while in the case of NiSi to n-HDD contacts the theoretical fit and the measured $R_c W$ product coincided only for $L < 0.5$. Starting from $L = 0.5 \mu\text{m}$ a disagreement appeared, and a deviation from the model was observed (Fig. 2.5a). The results for PtSi to n-HDD and p-HDD were both in agreement with the theoretical fit (Fig. 2.6). In these cases the distribution of the measurement points on the theoretical fit is much more uniform, compared to our previous results (Fig. 2.1), providing a better fit and a higher accuracy.

2.4.4 DEVIATING $R_c W$ VALUES OF NiSi-TO-n-HDD CONTACTS

A number of factors can be considered to explain the deviation of the $R_c W$ product of NiSi-to-n-HDD contacts from the Scott fit (see Fig. 2.5a):

- (i) the HDD dopant type,
- (ii) the barrier height between silicide and Si,
- (iii) dopant/metal influence on silicide formation at the Ni-Si interface.

(i) As PtSi to n-HDD contacts revealed good agreement with the model, the possibility of processing problems, related to the n-HDD, must be excluded. Edge effects due to the patterning and cleaning process of the blocking mask and layout errors can be excluded as well because both the n-HDD and p-HDD areas were processed on the same wafers with the same DUV mask.

(ii) The Schottky barrier between NiSi and n-HDD can not cause this deviation either, since for PtSi to n-HDD a higher Schottky barrier is expected (see Table 1.1) and in this case the deviation was not observed (Fig. 2.6a). The fact that this deviation for NiSi to n-HDD contacts was observed at all studied dopant concentrations (Fig. 2.5a) indicated that the contact resistance value itself should not play a role in this case. Moreover, as expected from theory (section 1.2.3) and proven experimentally in this work, increasing the barrier height for a given dopant concentration (or alternatively lowering the doping level for a given barrier height) would lead to a higher specific contact resistance. In terms of the Scott method, this would mean a higher saturation value for R_0 (Eq. 1.18), but certainly not the

deviation from the theoretical fit, shown in Fig. 2.5a.

(iii) The most probable explanation of this deviation is the difficulty of silicide formation caused by the presence of As as stated by Davari [19]. The Scott method is based on the assumption that all the segments are identical in terms of silicide thickness. As shown in Fig. 2.3d, a difference in NiSi thickness between NiSi segments on the same fragment was observed, only for the NiSi formation on n-HDD. From segment to segment, the NiSi thickness was not the same for $L = 0.1 \mu\text{m}$ (see Fig. 2.3d). Here and for other small silicide lengths, the corresponding “electrical” silicide thickness would then be averaged over the large number of segments. The obstruction of silicide formation on n-type Si, caused by the presence of As [19], could lead to a distribution of areas with enhanced and retarded silicide formation (Ni diffusion) on a $0.1 \mu\text{m}$ length scale. In this case, for larger L ($> \sim 0.5 \mu\text{m}$) there is a larger effective area and hence, a higher probability for silicide formation. This would lead to the formation of a thicker NiSi and, consequently, to a lower sheet silicide resistance for the larger segments. Then, comparison of the fragments with the short and large L would result in a lower $R_c W$, as shown in Fig. 2.5a. This effect was enhanced in our experiments by the low sheet resistance of the NiSi ($7\text{-}8 \Omega/\square$) compared to PtSi ($25\text{-}26 \Omega/\square$). The deviation from the theoretical fit was not observed for NiSi to p-HDD and PtSi to n-/p-HDD contacts, since these silicide segments were grown uniformly.

A uniform formation of a silicide is a prerequisite for the reliable application of the TLM structures by the Scott method. Fortunately, for process development this effect may serve as an indication of improper silicide growth in submicron structures.

2.4.5 NON-LINEARITY OF THE I-V CURVES FOR LOW DOPANT LEVELS

The measurements were performed in the entire dopant range of $10^{17} - 10^{20} \text{ cm}^{-3}$. For the high dopant concentrations ($\sim > 1 \cdot 10^{19} \text{ cm}^{-3}$), the I - V curves were perfectly linear (with the linear fit coefficients $R^2 = 1$), as the

contacts exhibited ohmic behavior (see Fig. 2.4). In the mid-dopant range ($\sim < 1 \cdot 10^{19} \text{ cm}^{-3}$), however, the I - V curves were not perfectly linear ($R^2 < 1$). The observed non-linearity was in agreement with the difference in the

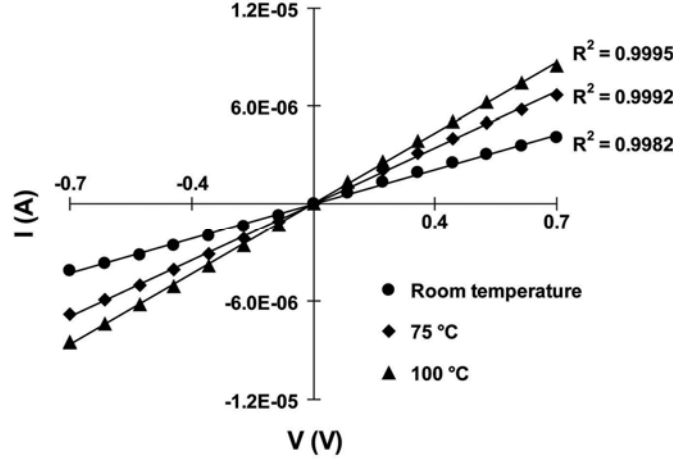


Fig. 2.7. I - V curves for NiSi on a p-HDD ($N_a = 7.9 \cdot 10^{18} \text{ cm}^{-3}$) fragment with $n = 30$ silicide segments and a silicide width of $W = 8 \mu\text{m}$.

barrier height between the NiSi or PtSi and p- or n-type Si (see Table 1.1). For the PtSi to n-HDD contacts, the non-linearity was observed for dopant concentrations (N_d) less than $1 \cdot 10^{19} \text{ cm}^{-3}$, whereas for the PtSi to p-HDD contacts, the non-linearity was observed for $N_a < 5 \cdot 10^{18} \text{ cm}^{-3}$. The I - V curves were measured at 75 and 100 °C for the wafers falling in the mid-dopant range. The R^2 values were calculated for the I - V curves of all measured TLM fragments, showing an improved linearity as the temperature increased (Fig. 2.7).

2.4.6 $R_c W$ VALUES AT DIFFERENT TEMPERATURES

For the mid-range dopant concentrations in the order of 10^{18} cm^{-3} , the R_c values were obtained from the I - V curves at room- and higher temperatures, making it possible to apply the Scott method. The fitting of the $R_c W$ values with the Scott method had successfully been done for all temperatures. As the temperature increased, the R_c values decreased. A good agreement for the two silicide widths was again demonstrated (Fig. 2.8). The extracted ρ_c

decreased with increasing temperature (Fig. 2.8) as expected from the Eq.1.18 (section 1.2.3).

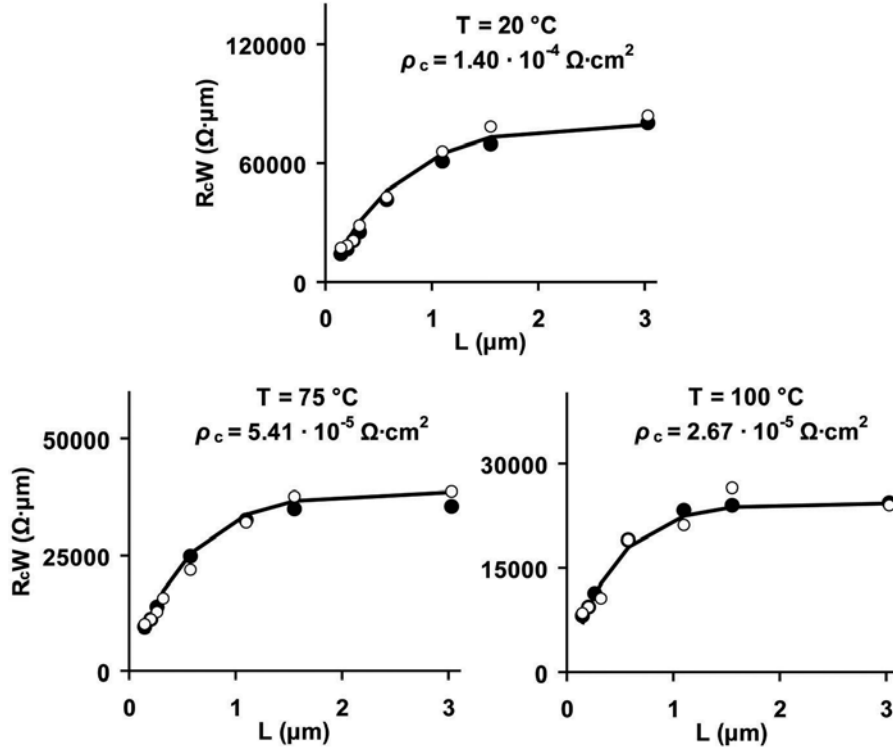


Fig. 2.8. Contact resistance values for PtSi to p-HDD contacts at room temperature, 75 °C and 100 °C with a dopant concentration $N_a = 7.9 \cdot 10^{18} \text{ cm}^{-3}$. Solid symbols represent measured data for $W = 2 \mu\text{m}$, open symbols are for $W = 8 \mu\text{m}$. The lines are the fits obtained by Scott method.

2.4.7 MEASUREMENT LIMITS IN TERMS OF DOPANT CONCENTRATION

For the wafers with the low doping levels, R_c values could not be used to extract the ρ_c because the R_n resistances obtained for different TLM fragments were identical to R_{ref} (Eq. 1.15). This result indicated that the current did not enter the silicide segments because of the Schottky barrier and flowed through the HDD areas only. Ultimately this resulted in the same resistance value for the TLM fragments with n silicide segments and R_{ref} , obtained from the fragment without silicide. Therefore, the lowest dopant limits for obtaining the ρ_c from the TLM structures can be determined.

Obviously, these limits are related to the corresponding Schottky barriers between silicide and silicon (Table 1.1). The limits are $4\text{--}5\cdot 10^{18}\text{ cm}^{-3}$ and $2\text{--}3\cdot 10^{18}\text{ cm}^{-3}$ for NiSi grown on n-HDD and p-HDD silicon area, respectively. For PtSi to n-HDD contacts this is $7\text{--}8\cdot 10^{18}\text{ cm}^{-3}$. As expected due to the lower Schottky barrier between PtSi and p-HDD silicon (Table 1.1), in this case the limit is also lower, i.e., $1\text{--}2\cdot 10^{18}\text{ cm}^{-3}$.

2.5 CONCLUSIONS

Optimized TLM test structures were fabricated and characterized. The structures were designed to provide a better fit and a higher accuracy using the Scott method, and to verify the measurement data. The TLM structures were evaluated for NiSi- and PtSi-to-silicon contacts in a broad range of dopant concentration. The ρ_c extraction method and the measurement drawbacks were discussed in terms of the necessity of applying a TEM analyses and uniform silicide formation. The TLM structures were evaluated at different temperatures. The observed decrease of the ρ_c values with increasing temperature was in agreement with theory. The lowest dopant concentrations of p- and n-type silicon, enabling measuring NiSi- and PtSi-to-silicon contact resistance, were determined.

Our work provided an important reference for the further use of TLM structures, also applicable to other silicides. It contributed to the development of test structures and outlined the requirements to characterize NiSi- and PtSi-to-silicon contacts by TLM method.

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3

LOW ρ_c OF NiSi AND PtSi TO Si

The first purpose of this chapter is to provide a novel database for NiSi-to-silicon specific contact resistance in a broad range of doping levels, using PtSi as a reference. The obtained ρ_c is extracted from direct contact resistance measurements using standard silicide formation process. These values are low, compared to results reported by others from similar experiments.

The second purpose of this chapter is to investigate the origin of the low ρ_c values. In other works values in this low range were achieved using dopant segregation technique. We tested this hypothesis using SRP technique and observed an absence of substantial active dopant segregation within the normal thermal budget for silicidation. In addition, SIMS depth profiling showed no dopant segregation either. The Ni ion implantation experiments (to induce interface damage) were performed to clarify the role of the impact of the interface. It is demonstrated that low contact resistance for a given active dopant level can be obtained without any active dopant segregation, given a silicide formation process flow resulting in a good silicide-silicon interface.

In the first section of this chapter the optimized TLM structures (see chapter 2) are processed for a broad range of n- and p-type silicon dopant levels, with NiSi and PtSi as the silicides. The results of SRP and SIMS analyses, to verify the dopant concentration, can be found in the second section. In the third section of this chapter the additional experiments using Ni ion implantation (to induce interface damage) are performed to clarify the impact of the interface.

This chapter is based on the following publications:

N. Stavitski, M. J. H. van Dal, A. Lauwers, C. Vrancken, A. Y. Kovalgin, and R. A. M. Wolters, "Systematic TLM measurements of NiSi and PtSi specific contact resistance to n- and p-type Si in a broad doping range," *IEEE Electron Device Lett.*, vol. 29, pp. 378-381, Apr. 2008.

N. Stavitski, A. Y. Kovalgin, R. Brennan, R. A. M. Wolters, "Low Specific Contact Resistance of NiSi and PtSi to Si: Impact of Interface," submitted to *Electrochem. Solid State Lett.*

3.1 THE ρ_c OF NiSi AND PtSi TO Si IN A BROAD DOPING RANGE

3.1.1 MOTIVATION

The contact resistance of silicide-semiconductor junctions has been extensively studied using various methods and structures, although the results show considerable scatter [1]. Some values for NiSi can be found in the literature [2]-[5], but no solid database for NiSi-silicon contact resistance exists, especially for a broad range of dopant levels. Most of the researchers used CBKR structures to study ρ_c , while in modern IC technology one would tend to use TLM structures as they could easier be embedded in the standard self-aligned silicide CMOS process (section 1.1.2, [6]). The advantage of the TLM structure over CBKR is that in TLM structures the silicide segments and the contacts pads are made in one single SALICIDE process step (section 1.1.2). This allows to define critical dimensions and makes in-line process control possible. Furthermore, the extraction of the specific contact resistance, determined either by CBKR or TLM structures, resulted in different values (orders of magnitude difference) for a given dopant level [1]. The purpose of section 3.1 is to compare the results obtained from our optimized TLM structures (section 2.2) with the data known from literature for thorough studied PtSi, and provide novel systematic measurement data for NiSi.

3.1.2 EXPERIMENTAL APPROACH

The contact resistance is determined mainly by the thermionic emission current transport mechanism for contacts with lower dopant concentrations (section 1.2.3, [7]). For contacts with higher dopant levels, the tunneling process dominates. Hence ρ_c depends strongly on dopant concentration and varies exponentially with $(\phi_b / \sqrt{N_d})$ (section 1.2.3, [7]). To verify the consistency of the extracted contact resistance, it was decided to evaluate contacts of NiSi and PtSi to a wide range of dopant levels ($10^{18} - 10^{21} \text{ cm}^{-3}$) of p- and n- type Si.

The ρ_c is also temperature dependent and this dependence is different for high and medium-low dopant concentrations (section 1.2.3). For this reason, in order to validate our results, NiSi-to-silicon contact resistance was measured at three different temperatures for high, medium and low silicon dopant concentration levels.

Deep junctions were chosen in order to enable an accurate measurement of the dopant profiles and therefore to minimize errors during the extraction of the specific contact resistance. Moreover, for deeper junctions, the relative (to the junction depth) silicon consumption is lower. This also improves the validity of our measurements, resulting in a smaller relative change of the dopant profile (and, therefore, the sheet resistance). This can be expected when silicon is consumed, since the sheet resistance of the semiconductor immediately beneath the contact tremendously affect the contact resistance.

NiSi and PtSi silicides are chosen because of their technological importance. NiSi is widely used in advanced CMOS (section 1.1.2, [8]). It has a resistivity comparable to that of commonly used TiSi_2 and CoSi_2 . NiSi can be formed at low temperatures and less silicon is consumed (Table 1.1) (section 1.1.2, [9]-[11]). In addition, NiSi has no agglomeration problems on narrow lines [12]-[14]. On the other hand, PtSi has been studied thoroughly [1], [15]-[17], providing a good reference. The silicide-to-silicon contact resistance was investigated using a set of optimized test structures with silicided segments of varying lengths (section 2.2), based on the Scott method for TLM structures (section 1.3.2, [6]).

Summarising, the validity of our results is based on:

- (i) systematic measurements and statistical data analysis (i.e., the represented data were averaged over 18 dies for each dopant type and concentration);
- (ii) validation at different temperatures for several dopant levels;
- (iii) experimental verification of the actual active doping concentrations and doping profiles by SIMS and SRP techniques;

- (iv) verification of the actual silicide lengths for different silicide segments by TEM analysis;
- (v) optimizing the TLM structures in terms of the silicide lengths and the number of segments.

3.1.3 RESULTS

NiSi and PtSi TLM structures were processed as described in section 2.3. In order to verify the actual dopant concentrations, the same implantation recipes were applied to blanket wafers, and the total dopant concentration and the concentration of electrically active impurities were determined by SIMS and SRP technique, respectively. The results agreed very well with the expectations based on the implantation energies and doses used. The concentration profiles for the blanket wafers are presented in Fig. 3.1.

Resistance values R_{ref} and R_n of all the fragments were measured, as explained in section 1.3.2. Fitting of the obtained $R_c W$ values with the Scott method (section 1.3.2, section 2.4) was carried out to extract the ρ_c . The ρ_c values, plotted as a function of the dopant levels (N_d and N_a) for n- and p-HDD, are presented in Fig. 3.2. The dopant levels were taken from the SRP profiles at ~ 20 nm depth, as they represented the relevant electrically active concentrations of HDD areas after the silicide had been formed.

The contact resistance of NiSi-to-silicon was measured at room temperature, 75 °C and 100 °C. The ρ_c values, plotted as a function of the temperature for high and medium-low dopant concentrations of n- and p-HDD are presented in Fig. 3.3.

3.1.4 DISCUSSION

Except for the highest concentrations (10^{21} cm^{-3} for B and $10^{20} - 10^{21} \text{ cm}^{-3}$ for As), all the dopants were activated showing a good match between the results obtained by SIMS and SRP methods (Fig. 3.1). The first 10 nm of the SIMS curves can not be compared with the results obtained by SRP, because of the known SIMS accuracy problem for the upper layer. However,

this fact does not compromise the interpretation of the results, since the upper silicon layer is consumed during the silicide formation.

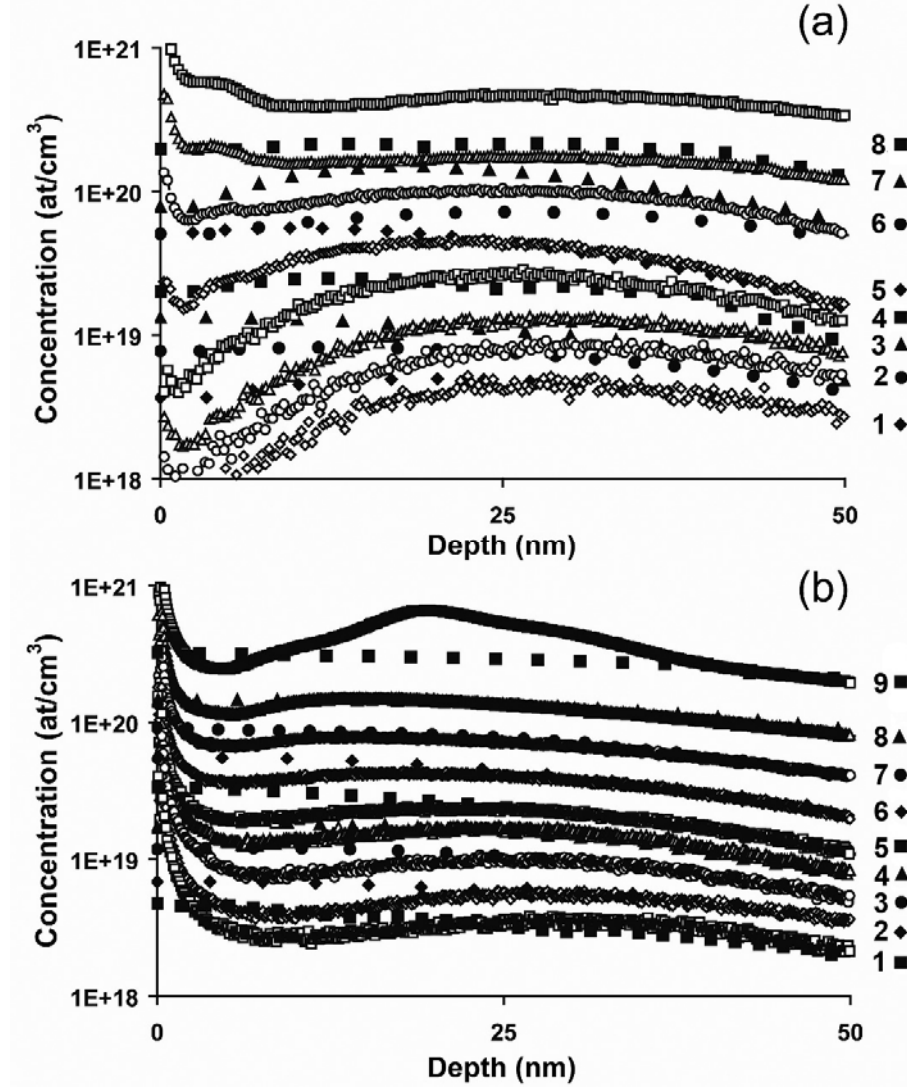


Fig. 3.1. As (a) and B (b) concentration profiles of n-HDD (a) and p-HDD (b) areas obtained by SIMS (open symbols) and SRP (solid symbols). Each symbol type corresponds to a given profile. Active dopant concentrations ($\times 10^{19}$, cm^{-3}) used for ρ_c extraction:
for (a): 0.5 (1), 0.79 (2), 1.2 (3), 2.1 (4), 4.7 (5), 7.1 (6), 15 (7), 19 (8);
for (b): 0.31 (1), 0.61 (2), 1.0 (3), 1.7 (4), 2.5 (5), 4.6 (6), 8.3 (7), 14 (8), 30 (9).

It was found that ρ_c decreased with increasing As or B concentration, as expected from Eq. 1.9 (section 1.2.3, [7]). For lower As concentrations, PtSi to n-type silicon contact resistance was slightly higher than that of NiSi to n-type silicon (Fig 3.2a). It is known, that at high dopant levels the effective barrier height for given metal-semiconductor contacts can be lower [7].

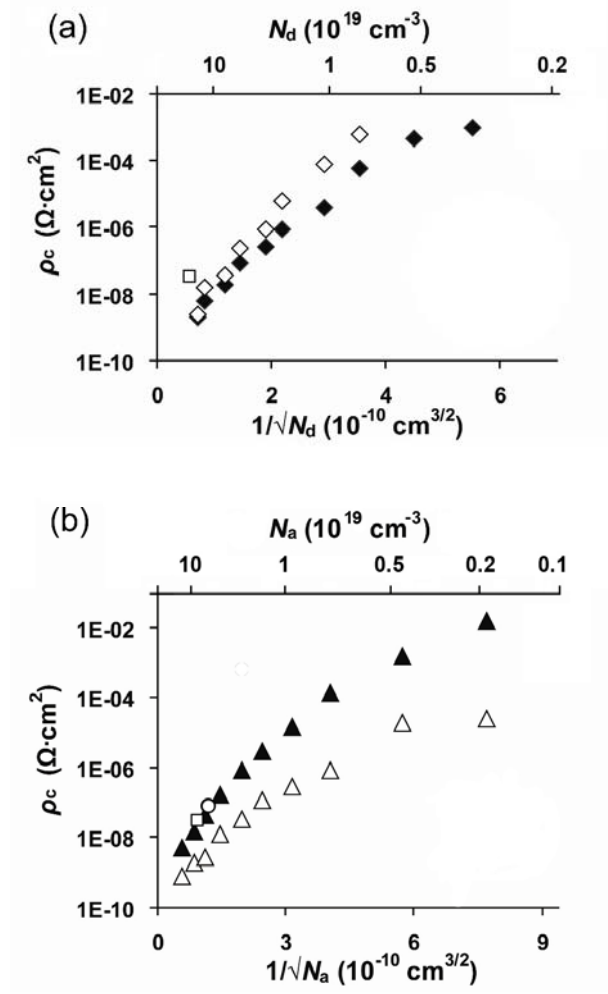


Fig. 3.2. (a) Specific contact resistances to n-HDD as a function of the dopant level: (a) NiSi from this work ($\blacklozenge$), PtSi from this work ($\diamond$), PtSi from [15] ($\square$); (b) Specific contact resistances to p-HDD as a function of the doping level: NiSi from this work ($\blacktriangle$), PtSi from this work ($\triangle$), PtSi from [15] ($\square$), PtSi from [16] ($\circ$).

The similar values of specific contact resistance to silicon for PtSi and NiSi at high dopant levels, shown in Fig. 3.2, are due to a convergence of the effective barrier height for these silicides. PtSi contacts to p-type silicon exhibited the lowest contact resistance at lower dopant concentration in agreement with the lower Schottky barrier (Table 1.1).

The ρ_c values of PtSi-to-n-type, known from literature, range from $3 \cdot 10^{-4}$ to $4 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ for dopant concentrations between $5 \cdot 10^{18}$ and $3 \cdot 10^{20} \text{ cm}^{-3}$ [1]. For low concentrations ($3 \cdot 10^{19} \text{ cm}^{-3}$ and below), our results are in agreement with the results previously obtained using other methods. For concentrations of 10^{20} cm^{-3} and higher, a disagreement appears. For example, Cohen et al. determined a ρ_c of $3.7 \cdot 5 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ at an As concentration of $3 \cdot 10^{20} \text{ cm}^{-3}$ [15], whereas in our work a value of $1.5 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ is found at an As concentration of $1.9 \cdot 10^{20} \text{ cm}^{-3}$ (Fig 3.2a). The difference can be explained by the fact that most of the measurements presented in the literature have been performed using SIMS analysis for determining the dopant concentration. The active concentrations for the highest doses might be lower, as shown in this section. This could crucially affect the contact resistance value. From our results for PtSi to n-type silicon, a change of two orders of magnitude in the dopant range of $1.9 \cdot 10^{20}$ to $4.7 \cdot 10^{19} \text{ cm}^{-3}$ was observed.

The ρ_c results of PtSi-to-p-type silicon are a similar case. For a low concentration of $\sim 10^{18} \text{ cm}^{-3}$, our results fall in the expected range [1]. For higher concentrations, in particular 10^{19} cm^{-3} and beyond, the difference becomes larger. Reported values are $4 \cdot 10^{-8}$ and $7.4 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ for B concentrations of $1.2 \cdot 10^{20}$ and $7 \cdot 10^{19} \text{ cm}^{-3}$, respectively [15], [16]. In this work, much lower ρ_c values of $1.9 \cdot 10^{-9}$ and $2.8 \cdot 10^{-9} \Omega \cdot \text{cm}^2$ have been determined for similar B concentration, i.e. $1.4 \cdot 10^{20}$ and $8.2 \cdot 10^{19} \text{ cm}^{-3}$ (Fig 3.2b). In addition to the fact that the exact concentrations of the active As/B were not always verified, a possible explanation of the difference is the known accuracy problems during the data extraction using CBKR structures in the range of $\sim 10^{-8} \Omega \cdot \text{cm}^2$ and below [18]. In this case, the current crowding effect may lead to significant errors (orders of magnitude) [1],

[19]. Yet another factor that complicates the data comparison is that in various studies different processing and measurement techniques were used.

Measurement of temperature dependence of the contact resistance provided an additional validation of our results (Fig. 3.3). It was observed that the NiSi-to-silicon specific contact resistance for medium-low dopant concentrations was strongly temperature dependent, i.e., abruptly decreasing with increasing the temperature, in agreement with the thermionic emission mechanism (section 1.2.3). For the high dopant concentration in silicon, there was a slight temperature dependence (Fig. 3.3), since in this case the tunneling mechanism prevails (section 1.2.3).

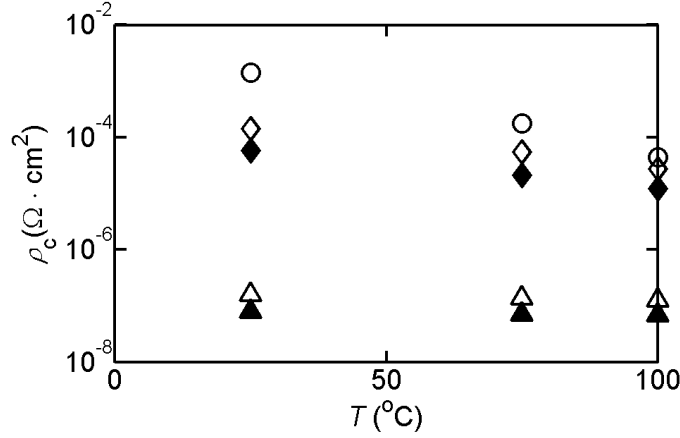


Fig. 3.3. Specific contact resistances of NiSi-to-p-HDD (open symbols) and to n-HDD (solid symbols) as a function of the measurement temperature for different silicon dopant concentrations: high (▲/△), medium (◆/◇) and medium-low (○).

3.1.5 CONCLUSION

Using systematic measurements on optimized TLM structures to determine PtSi-to-silicon ρ_c , the disagreements with the literature values have been explained in terms of active dopant concentrations and CBKR method measurement limitations. Based on our study of PtSi-to-silicon ρ_c , the ρ_c values obtained for NiSi-to-silicon were validated. Temperature dependence of the contact resistance of NiSi-to-silicon served as an additional confirmation and was in agreement with the theory. The NiSi data were obtained from the structures fabricated by a CMOS technology, using standard SALICIDE recipe. These very low ρ_c values further favor the use of

NiSi in modern CMOS processes. An extra advantage is the similar values obtained on both n- and p-type silicon. Finally, we created a unique database for NiSi-to-silicon ρ_c for a wide range of doping levels, which is important for the development of the modern contact technology.

3.2 ACTIVE DOPANT SEGREGATION

3.2.1 MOTIVATION

As a reduction of contact resistance of silicide-silicon junctions became a focus in recent years (section 1.1.1, [20], [21]), several techniques have been proposed to reduce the contact resistance, which is determined by the Schottky barrier height and the concentration of active dopants at the silicide/silicon interface (section 1.2.3). Ni-alloy silicides [22] were demonstrated, improvements were reported using Al [23] and Sb [24] segregation, and silicon-carbon source/drains [25] were suggested. NiSi-to-silicon contacts were reported to be improved through dopant segregation [26], and good results were obtained with Pt-incorporated NiSi [27]. Other approaches such as dual-silicides are less attractive due to the process complexity.

In section 3.1, the achievement of low specific contact resistance of NiSi and PtSi to silicon doped in the range of $10^{18} - 10^{21} \text{ cm}^{-3}$ is reported. Namely, the obtained values for a given dopant concentration are relatively low for both n- and p-type Si, compared to the values published elsewhere [1]. In the other works values in this low range were achieved using dopant segregation technique.

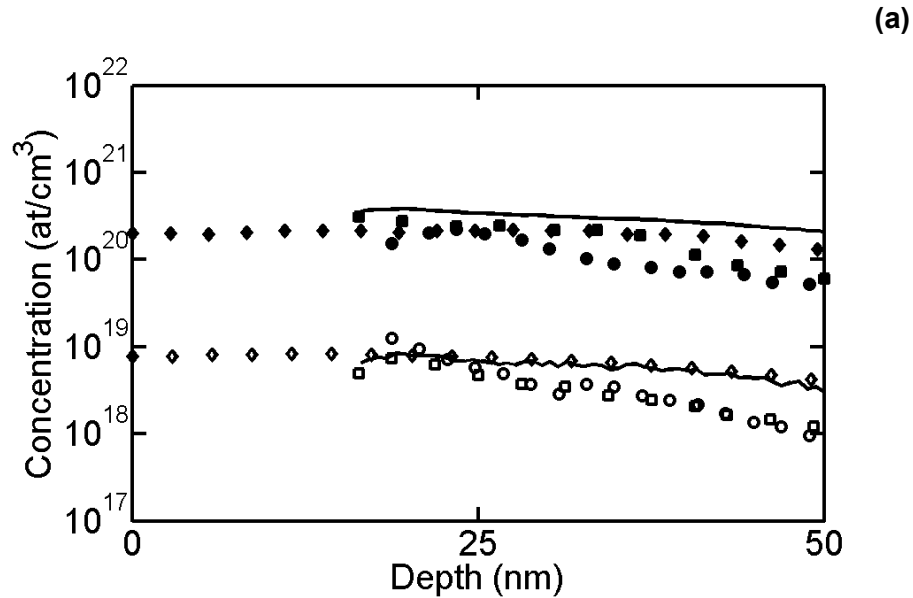
In this section we investigate the role of the active dopant segregation using the SRP method. In other words, we clarify whether the low contact resistance in our process originates from active dopant segregation. Moreover, we verify the dopant concentration profile as such using SIMS depth profiling.

3.2.2 EXPERIMENTAL APPROACH

For the active dopant segregation study, two different dopant levels were chosen – the high and the middle-low range of concentrations, i.e. $1.5\text{--}3\cdot 10^{20}\text{ cm}^{-3}$ and $6\text{--}8\cdot 10^{18}\text{ cm}^{-3}$. In order to examine the influence of silicide growth on the active dopant segregation at the silicide-silicon interface, NiSi and PtSi were grown on blanket wafers, by using exact the same deposition and annealing recipes as for the TLM structures (section 2.3). The active concentrations with the silicide present were determined by SRP for both n- and p-HDD areas. SIMS analysis was performed for the aforementioned NiSi samples to obtain dopant concentration profiles.

3.2.3 RESULTS AND DISCUSSION

The active dopant concentration profiles for As and B were derived from the SRP measurements. The As profiles for blanket n-HDD and for blanket with NiSi and PtSi are shown in Fig. 3.4a. The results of B-profiling for blanket p-HDD wafers and blanket wafers with the silicides are shown in Fig. 3.4b.



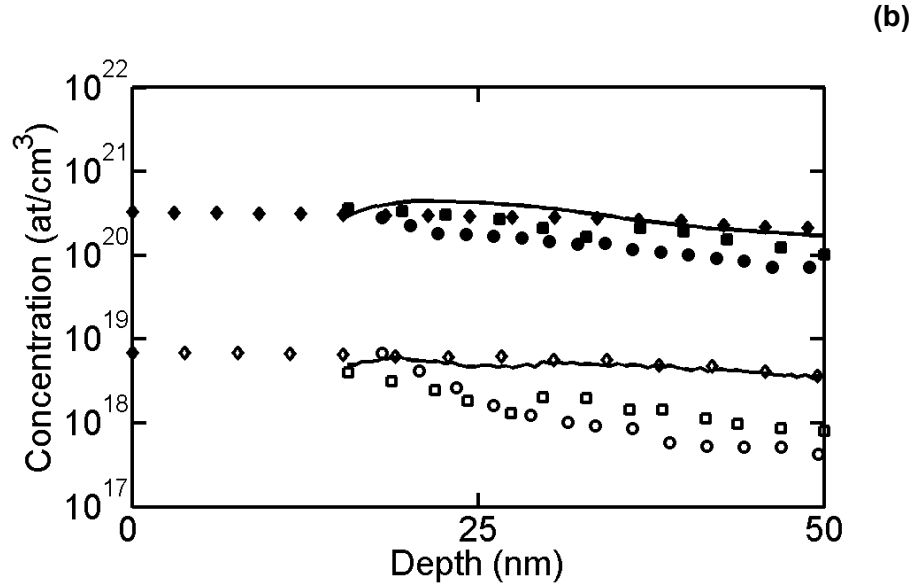


Fig. 3.4. As (a) and B (b) concentration profiles obtained by SRP for high (solid symbols) and medium/low (open symbols) dopant levels of HDD area. Each symbol type corresponds to a given sample: blanket wafers (▲ and △), blanket wafers with NiSi (■ and □), blanket wafers with PtSi (● and ○). Solid lines are concentration profiles obtained by SIMS for blanket wafers with NiSi. Zero depth marks the silicon's upper interface of the blanket lot.

The SRP profiles of the samples with NiSi and PtSi are shifted in depth, depending on the amount of silicon consumed. The active concentration profiles of the blanket lot and of the samples with NiSi and PtSi for both high and low-medium dopant levels are similar. No peak of the dopant concentration is observed for both n- and p-HDD areas. This means that the silicide formation did not affect the active dopant concentration at the silicide-silicon interface. In other words, no active dopant segregation is present on the nanometer scale.

Earlier works [26], [28], [29] reported an increase of total dopant concentration at the silicide-silicon interface, measured by SIMS. We verified the dopant concentration profiles for NiSi on n- and p-HDD areas using SIMS depth profiling. The results are shown in Figs. 3.4a and 3.4b, respectively. These results are in a good agreement with the SRP data and confirm no dopant segregation.

The absence of dopant segregation can be explained by the relatively

thin (20-25 nm) silicides and the related low amount of dopant in the reacted (consumed) Si. In other works, 70-80 nm thick silicides were normally used, creating dopant segregation [28], [29]. We have intentionally chosen a standard silicide formation process with typical silicide thickness used in modern CMOS technology.

3.2.4 CONCLUSION

In order to understand the occurrence of the low ρ_c values of NiSi and PtSi to silicon, the aspect of active dopant segregation was investigated. Using SRP analysis, we found no substantial enhancement of electrically active dopants at the silicide-silicon interface. The dopant concentration profiles obtained using SIMS analysis showed no segregation either. Dopant segregation is therefore not the explanation for the low contact resistances obtained.

3.3 IMPACT OF INTERFACE

3.3.1 MOTIVATION

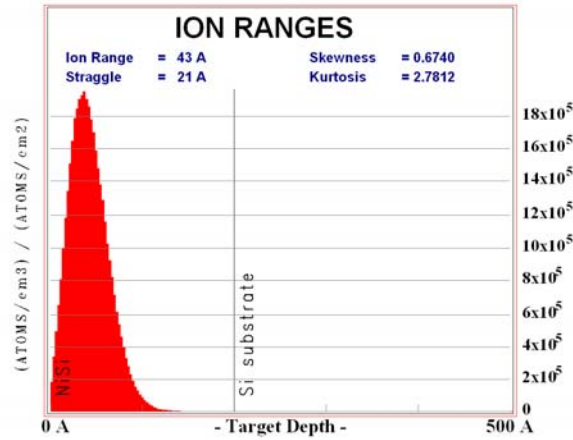
Given the low ρ_c values (section 3.1) and the absence of dopant segregation (section 3.2), the silicide-silicon interface should be of high quality. In this section we perform the experiments to highlight the impact of the interface. For that purpose, the interface is intentionally damaged using Ni implantation into realized NiSi TLM structures. The implantation effect on specific contact resistance is further quantified.

3.3.2 EXPERIMENTAL APPROACH

For implantation, Ni was chosen in order not to significantly deviate from initial composition (i.e. NiSi). Two silicon dopant concentrations were chosen for this experiment. First, a p-HDD of $3 \cdot 10^{18} \text{ cm}^{-3}$ was chosen because a larger effect is expected for this lower dopant concentration. Second, a p-HDD of $6 \cdot 10^{18} \text{ cm}^{-3}$ was chosen to refer to the SRP analysis for the medium dopant level (section 3.2.2).

Ni was implanted using a low energy (5 keV) implantation with three different doses: $2 \times$, $5 \times$ and $10 \times 10^{15} \text{ cm}^{-2}$. Based on our simulations for a minimum thickness of NiSi of 18 nm (i.e. $20 \pm 2 \text{ nm}$), the 5 keV implanted Ni profile (for the highest Ni dose) is very well positioned within the NiSi layer (Fig. 3.5a) and within the $\text{SiO}_2/\text{Si}_3\text{N}_4$ blocking mask layer (Fig. 3.5b).

(a)



(b)

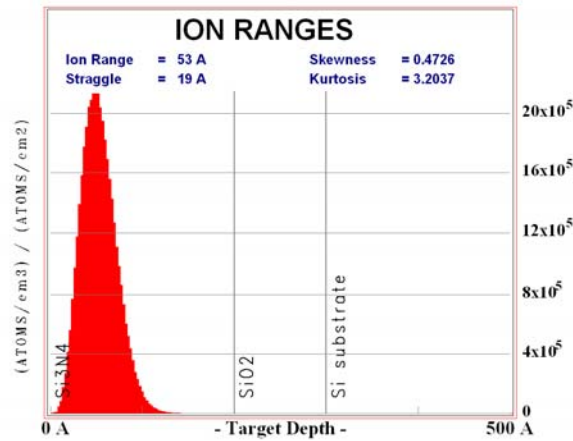


Fig. 3.5. Ni implantation profiles obtained by SRIM simulator. (a) Ni is implanted into NiSi. (b) Ni is implanted into the $\text{SiO}_2/\text{Si}_3\text{N}_4$ blocking mask layer. Both Ni profiles are well positioned within either NiSi or Si_3N_4 layer.

The samples were annealed at 470 °C for 43 s (as used for the NiSi formation). The specific contact resistance was extracted from TLM measurements (section 1.3.2) before and after annealing.

3.3.3 RESULTS AND DISCUSSION

The ρ_c values after the implantation (before and after annealing) as a function of Ni dose are presented in Figs. 3.6 and 3.7. Unimplanted samples were used as a reference.

The as-implanted samples exhibit much higher ρ_c than the unimplanted reference. This effect is stronger when a higher dose is implanted. After the annealing procedure ρ_c decreases, but remains significantly higher than that of the unimplanted reference. The contact resistance before and after annealing increases with increasing Ni implantation dose for both silicon dopant concentrations (Figs. 3.6 and 3.7).

The implantation can damage both the silicide and silicide-silicon interface. The silicide damage can result in an increase of its sheet resistance. After annealing, the sheet resistance of NiSi was exactly the same as that for the unimplanted samples, meaning that the damage caused to the

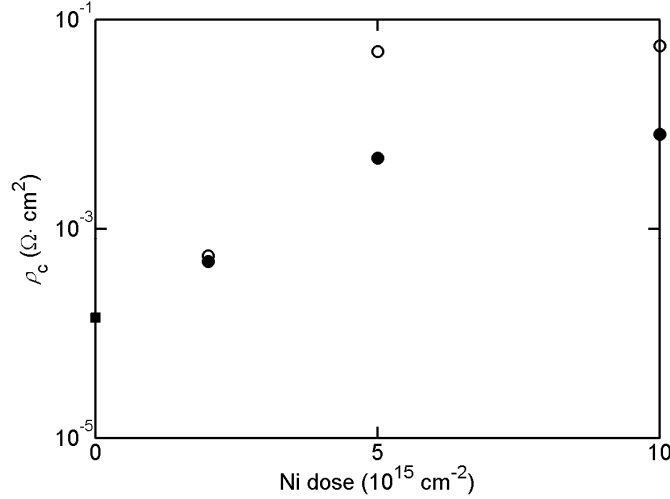


Fig. 3.6. Specific contact resistance of NiSi-to-p-HDD with the dopant level of $6 \cdot 10^{18} \text{ cm}^{-3}$ as a function of the Ni implantation dose before (○) and after (●) the annealing process, using an un-implanted sample (■) as a reference.

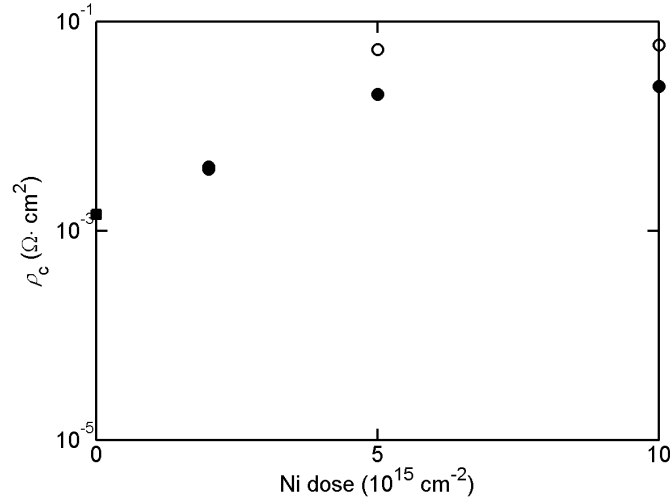


Fig. 3.7. Specific contact resistance of NiSi-to-p-HDD with the doping level of $3 \cdot 10^{18} \text{ cm}^{-3}$ as a function of the Ni implantation dose before (○) and after (●) the annealing process, using an un-implanted sample (■) as a reference.

NiSi was fully annihilated. Moreover, this would not affect the extraction of the ρ_c as such. On the other hand, the damage at the silicide-silicon interface was only partially recovered. As a result the ρ_c values decreased after annealing, but remained significantly higher than the reference values.

It is important to note that the ρ_c values for the silicon dopant concentration of $3 \cdot 10^{18} \text{ cm}^{-3}$ (Fig. 3.7) were higher than those of $6 \cdot 10^{18} \text{ cm}^{-3}$ (Fig. 3.6) for the unimplanted samples, as expected from the theory (section 1.2.3, [30]). These values remained consistently higher for the Ni-implanted samples before and after annealing.

The same implantation experiments were performed for NiSi-to-n-HDD contacts. The ρ_c values revealed the same trend for as-implanted and annealed samples. The results were consistent for both dopant levels of silicon.

3.3.4 CONCLUSION

In section 3.2 we concluded that active dopant segregation was not the explanation for the low ρ_c values obtained. To achieve such low values, the silicide-silicon interface should be of a high quality. The NiSi-silicon

interface was purposely damaged by Ni implantation into realized TLM structures. The increasing implantation doses led to a higher contact resistance, which could only be partially annealed out at the silicidation temperature.

Our results confirm that low ρ_c values for a certain active dopant level can be obtained, given a silicide formation process flow resulting in a good silicide-silicon interface.

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4

THE EXTRACTION OF ρ_c USING METAL-TO-METAL CBKR STRUCTURES

The parasitic factors that strongly influence the measurement accuracy of CBKR structures have been extensively discussed during last few decades. The minimum value of ρ_c , that can be accurately extracted, has been estimated. The purpose of this chapter is to confirm this minimum experimentally for low resistivity metal-to-metal contacts. A model is presented to account for the actual current flow and a method for a reliable ρ_c extraction is proposed. For ideal metal-to-metal contacts, the contact resistance is determined by the dimensions of the two-metal stack in the area of contact and sheet resistances of the metals used.

The first section of this chapter starts with the motivation, the test structure description is provided in the second section, followed by the experimental in section 4.3. The fourth section contains the evaluation of measured data versus test structure geometry parameters, i.e., contact shapes and dimensions. The fifth section is about the extraction of ρ_c using the analytical model by Schreyer and Saraswat. In section 4.6 our approach to extract ρ_c is presented, including the full derivation of the model to account for the actual current flow and its application to our measurement data. A comparison of this model with a standard simulator is shown as well. The minimum value that can be measured using CBKR structures is discussed in section 4.7. The temperature dependence of the measurement data is presented in section 4.8. Finally, in section 4.9 conclusions are drawn.

This chapter is based on the following publications:

N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, A. Y. Kovalgin, R. A. M. Wolters, "A study of cross-bridge kelvin resistor structures for reliable measurement of low contact resistances," in *Proc. IEEE International Conference on Microelectronic Test Structures (ICMTS)*, Edinburgh, Scotland, pp. 199-204, Mar. 2008.

N. Stavitski, J. H. Klootwijk, H. W. van Zeijl, A. Y. Kovalgin, R. A. M. Wolters, "Cross-Bridge Kelvin Resistor Structures for Reliable Measurement of Low Contact Resistances and Contact Interface Characterization," *IEEE Trans. Semiconductor Manufacturing*, vol. 22, no. 1, pp. 146-152, Feb. 2009.

4.1 MOTIVATION

Beside TLM structures, CBKR structures (section 1.3.3) are widely used test structures to characterize metal-semiconductor contacts in the planar devices of VLSI technology [1], [2]. On the other hand, CBKR was found to be very sensitive to lateral current crowding around the contact when the contact window is smaller than the underlying layer (Fig. 1.7). Several simulations and correction methods were introduced in order to account for this current crowding effect [3]-[6]. However in the low resistance range, the extracted values for silicide-to-silicon ρ_c , obtained using CBKR structures, were still orders of magnitude different from the results obtained using other methods [2]. An explanation of this phenomenon is the accuracy problems during the data extraction using CBKR structures in the range of $\rho_c \sim 10^{-8} \Omega \cdot \text{cm}^2$ and below [7]. In this case, the lateral current flow around the contacts gives rise to an even higher additional resistance ([8], [9], section 1.3.3). This effect becomes more pronounced for a lower ρ_c and a higher sheet resistance (R_{sh}) of the underlying layer (Eq. 1.24). Simulations show that for $\rho_c < 10^{-7} \Omega \cdot \text{cm}^2$ the extracted ρ_c can differ by one or two orders of magnitude from the actual value [6]. Moreover, the trend in the modern technology of high-density integrated circuits is toward lower ρ_c and higher R_{sh} values, due to the shallower junctions. This will further complicate the interpretation of CBKR measurement results.

Our research is therefore concerned with finding the minimum contact resistance, which can be obtained experimentally using CBKR test structures, and developing a correction model to account for the actual current flow. In addition, this method should allow to characterize metal-to-metal contact interfaces, crucial for contact manufacturing. For that purpose, CBKR structures of different geometries, i.e., dimensions and shapes of the contact area were designed and manufactured. These structures were evaluated for metal-to-metal contacts without a physical interfacial layer, to assure the case of very low contact resistances, and for metal-to-metal

contacts with an interface present, to demonstrate the ability of the interface characterization.

4.2 TEST STRUCTURES DESCRIPTION

The metal-to-metal CBKR structures were designed to cover a wide range of contact sizes, i.e., length L for square contacts and diameter D for round contacts, and overlap size δ (Fig. 1.7). The chip layout and an example of the square and round CBKR structure are presented in Fig. 4.1.

Some of the structures were designed with two δ , different for the lower and upper metal layers: δ_L and δ_U , respectively. To exclude the uncertainty in the definition of δ in the case of round contacts, the metal tap width (V_{TAP} , Fig. 4.1b) was varied as well. The details are summarized in Table 4.1.

Table 4.1. Important geometry parameters of our CBKR structures.

Geometry	L (D) μm	δ μm	δ_U μm	δ_L μm	V_{TAP} μm
Square	1	0.2 – 5	n/a	n/a	n/a
Square	2	0.2 – 5	n/a	n/a	n/a
Square	4.4	0.2 – 5	n/a	n/a	n/a
Square	8.9	0.2 – 5	n/a	n/a	n/a
Square	17.7	0.2 – 5	n/a	n/a	n/a
Square	8.9	n/a	0.2 – 5	0.2 – 5	n/a
Round	5	0.5 – 10	n/a	n/a	1 – 2
Round	10	0.5 – 10	n/a	n/a	1 – 2
Round	20	0.5 – 10	n/a	n/a	1 – 2
Round	10	n/a	1 – 5	1 – 5	2
Round	20	n/a	1 – 5	1 – 5	2

4.3 EXPERIMENTAL

4.3.1 TEST STRUCTURES FABRICATION

The (100) p-type Si wafers with a 1 μm -thick thermal oxide were used to fabricate the test structures for this study. First, a 0.675 or 1.4 μm - thick Al layer was sputtered and patterned using I-line lithography and plasma

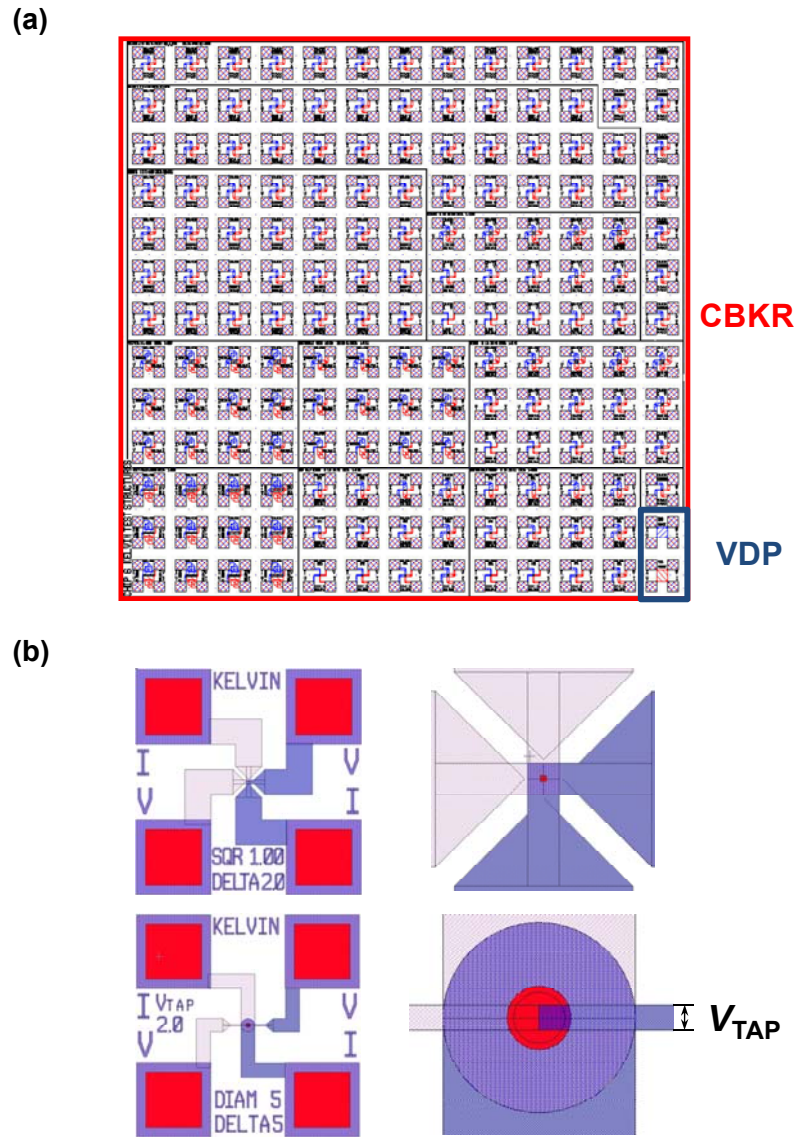


Fig. 4.1 (a) The chip layout, including CBKR and VDP structures. (b) An example of the newly-designed square and round CBKR structures. The complete structure including the bond pads is on the left- and a blow up of the actual contact is on the right-hand side.

etching. Then, a 0.8 μm -thick layer of SiO_2 was deposited by PECVD and the contact holes were opened. Prior to the second Al deposition, the contacts were either in-situ RF-precleaned to create a non-interface metal-to-metal contacts or this preclean procedure was omitted to obtain the contacts with interface present. The second Al layer of 0.675 or 1.41 μm was sputtered and patterned as the upper metallization layer, including the bond pads. Finally, the structures received 20-min annealing at 400 $^\circ\text{C}$ in a N_2/H_2 (10%) mixture. The schematic cross-section of the structure is shown in Fig. 4.2.

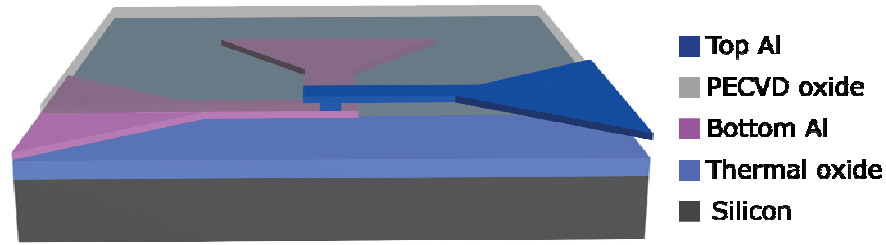


Fig. 4.2. A schematic cross-section of the CBKR structure.

4.3.2 MEASUREMENT DESCRIPTION

The CBKR structures were measured as explained in section 1.3.3, resulting in R_k values (Eq. 1.3.1).

The sheet resistances of both the lower and upper metal layers were measured using Van-der-Pauw (VDP) structures [2], located on the same chip (Fig. 4.1a). The obtained values of 0.054 and 0.027 $\Omega/\square$ for the 0.675 μm -thick and 1.4 μm -thick metals, respectively, were in agreement with the corresponding metal thicknesses.

Five dies per wafer were measured (CBKR and VDP). The obtained values were such, that the measurement error bars were within the symbol size.

4.4 MEASUREMENT RESULTS AND DISCUSSION

4.4.1 R_k FOR SQUARE CONTACTS WITH $\delta_u = \delta_L$

The R_k data as a function of contact size $A = L^2$ and the overlap size δ are given in Figs. 4.3 and 4.4, respectively. It can clearly be seen that R_k increases with increasing δ and decreases with increasing contact size. This is in agreement with the theory (Eq. 1.24), demonstrating, that for $\delta > 0$, the

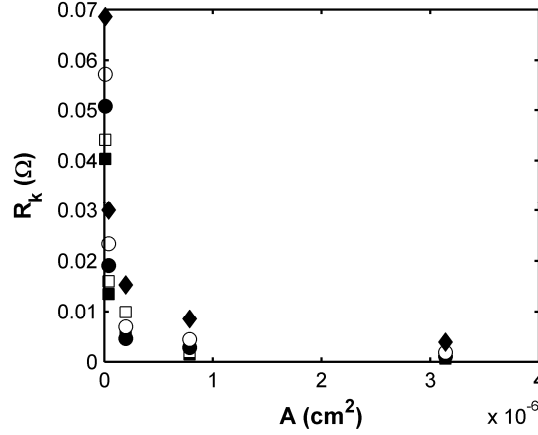


Fig. 4.3. Measured Kelvin resistance vs. contact size for given symmetric overlap area sizes for square contacts: $\delta = 0.2 \mu\text{m}$ (■), $\delta = 0.5 \mu\text{m}$ (□), $\delta = 1 \mu\text{m}$ (●), $\delta = 2 \mu\text{m}$ (○), $\delta = 5 \mu\text{m}$ (◆).

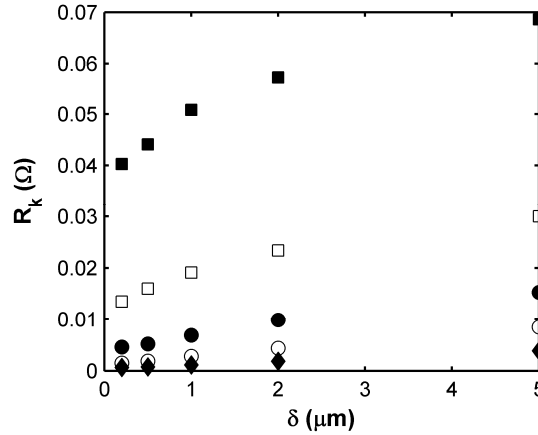


Fig. 4.4. Measured Kelvin resistance vs. symmetric overlap size for given square contact sizes: $L = 1 \mu\text{m}$ (■), $L = 2 \mu\text{m}$ (□), $L = 4.4 \mu\text{m}$ (●), $L = 8.9 \mu\text{m}$ (○), $L = 17.7 \mu\text{m}$ (◆).

lateral current flow gives rise to an additional voltage drop that is included in V_{34} , leading to a higher R_k value.

4.4.2 R_k FOR SQUARE CONTACTS WITH $\delta_U \neq \delta_L$

For the non-symmetric overlaps for upper and lower metals, the R_k values were dependent on the direction of the forced current I , as expected. This is in contrast to the other structures with symmetric δ for lower and upper metals, where R_k was not current direction dependent (Fig. 4.5).

It is noteworthy that Eq. 1.24 is derived for extracting specific *metal-to-silicon* contact resistance, when only R_{sh} and δ of the diffusion layer are considered, since R_{sh} of the metal is much lower than that of even highly doped silicon. While measuring contact resistance between two materials with similar R_{sh} , δ and R_{sh} of both layers must be taken into account.

Therefore, the R_k dependences on δ_L and δ_U were studied separately (Figs. 4.6a and 4.6b). It was demonstrated that R_k values increased with increasing δ_L or δ_U .

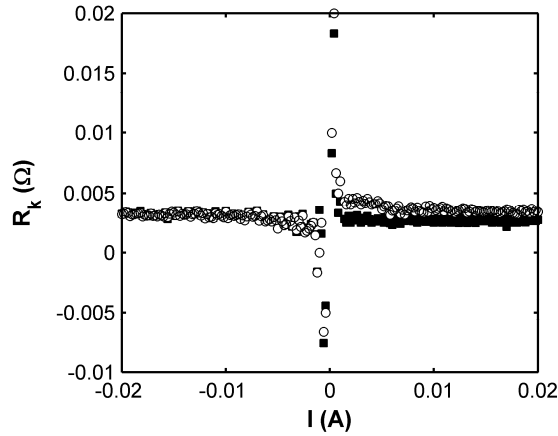
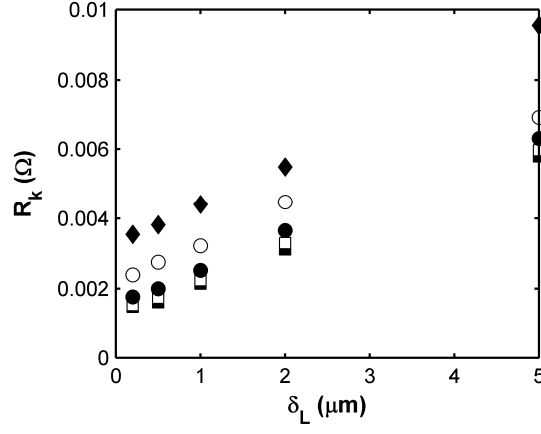


Fig. 4.5. Measured Kelvin resistance vs. forced current for symmetric (■) (i.e., $\delta_L = \delta_U$) and non-symmetric (i.e., $\delta_L \neq \delta_U$) (○) overlaps of square contacts.

(a)



(b)

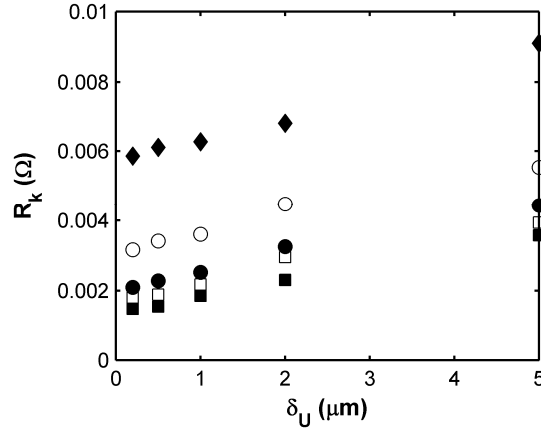


Fig. 4.6. Dependence of measured Kelvin resistance on overlap size δ_L (a) varying δ_U of 0.2 μm ($\blacksquare$), 0.5 μm ($\square$), 1 μm ($\bullet$), 2 μm ($\circ$), 5 μm ($\blacklozenge$) and on overlap size δ_U ; (b) varying δ_L of 0.2 μm ($\blacksquare$), 0.5 μm ($\square$), 1 μm ($\bullet$), 2 μm ($\circ$), 5 μm ($\blacklozenge$) for given square contact size ($L = 8.9$ μm).

4.4.3 R_k FOR ROUND CONTACTS

For round structures, the R_k data for different metal tap widths (V_{TAP}) as a function of contact size (A) and overlap size (δ) are given in Figs. 4.7 and 4.8, respectively.

Similar to the square contacts, the R_k increased with increasing δ and decreased with increasing A , in agreement with the theory (Eq. 1.24). The R_k

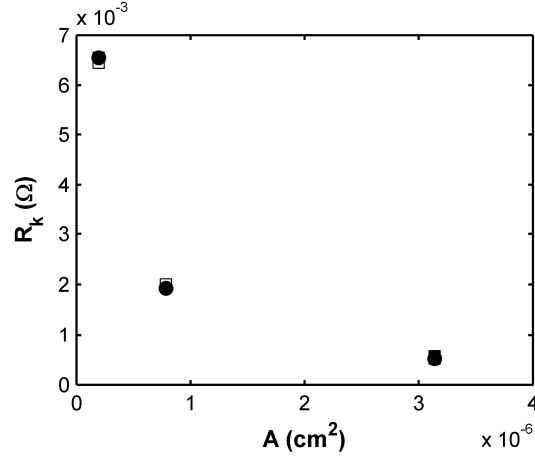


Fig. 4.7. Measured Kelvin resistance vs. contact size for given symmetric overlap area sizes for round contacts and various $V_{TAP} = 2 \mu\text{m}$ (■), $V_{TAP} = 1.5 \mu\text{m}$ (□), $V_{TAP} = 1 \mu\text{m}$ (●).

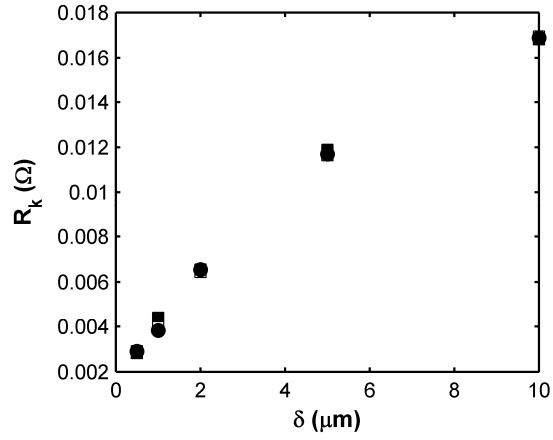


Fig. 4.8. Measured Kelvin resistance vs. symmetric overlap size for given round contact sizes and various $V_{TAP} = 2 \mu\text{m}$ (■), $V_{TAP} = 1.5 \mu\text{m}$ (□), $V_{TAP} = 1 \mu\text{m}$ (●).

was not dependent on V_{TAP} (Figs. 4.7 and 4.8), proving validity of the measurements and supporting a correct definition of overlap size for round contacts. The R_k behavior for the non-symmetric overlaps was studied by varying δ_L and δ_U separately and revealed the same behavior as for the square contacts.

4.5 ρ_c EXTRACTION USING 1D- AND 2D-MODEL

The ρ_c values were extracted using both the 1D- and 2D-approximations (section 1.3.3) for a variety of different contact and overlap sizes.

The ρ_c values for square contacts with symmetric overlaps can be found in Figs. 4.9 and 4.10. The ρ_c values obtained using the 1D-approach (Fig. 9) were strongly dependent on the contact and overlap size. This supported the significance of applying the 2D-Model instead of the simple 1D-approximation, as discussed earlier in section 1.3.3.

The ρ_c values, extracted using the 2D-Model for the smallest contact sizes, were hardly dependent on the overlap dimensions and revealed similar values for different contact sizes. As the contact size increased, a clear dependence of ρ_c values on δ appeared (Fig. 4.10), showing a difference between the geometrical factor, calculated from Eq. 1.24 and the actual geometrical factor, which led to a dependence on δ .

For structures with non-symmetrical overlaps, the ρ_c values were extracted by varying δ_L and δ_U separately, using R_{sh} (Eq. 1.24) of the corresponding metal layers. An example for δ_L can be found in Fig. 4.11, where the current direction was from the lower to upper metal. The dependence of ρ_c values on δ_L for given δ_U (Fig. 4.11) was similar to the dependence of ρ_c values on δ for symmetrical overlaps, shown in Figs. 4.9 and 4.10. If the current direction is changed, the ρ_c extracted using δ_U (instead of δ_L) revealed the same values. In summary, it was found that ρ_c is determined by δ_L , if current enters from the lower metal and by δ_U if the current enters from the upper metal.

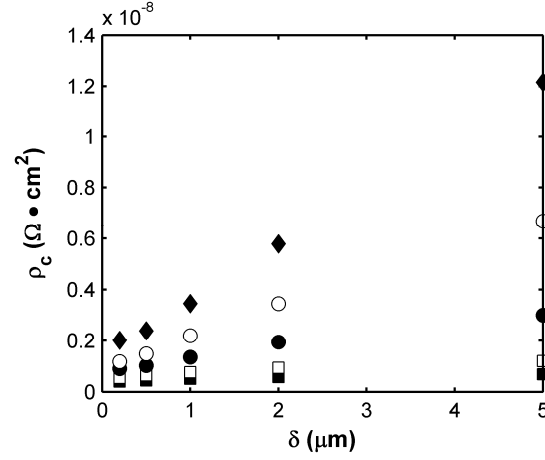


Fig. 4.9. Specific contact resistance obtained using 1D-approach vs. overlap size for given square contact sizes: $L = 1 \mu\text{m}$ (■), $L = 2 \mu\text{m}$ (□), $L = 4.4 \mu\text{m}$ (●), $L = 8.9 \mu\text{m}$ (○), $L = 17.7 \mu\text{m}$ (◆).

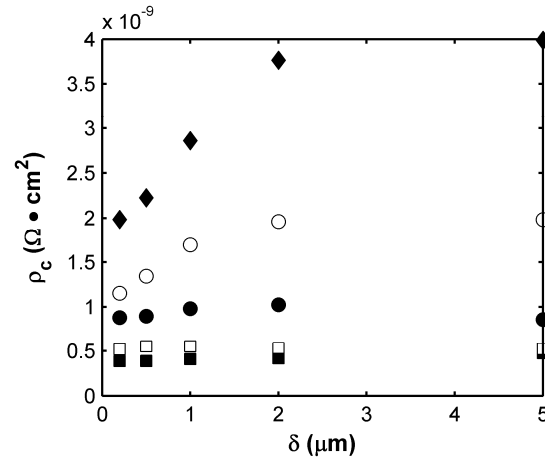


Fig. 4.10. Specific contact resistance obtained using 2D-approach vs. overlap size for given square contact sizes: $L = 1 \mu\text{m}$ (■), $L = 2 \mu\text{m}$ (□), $L = 4.4 \mu\text{m}$ (●), $L = 8.9 \mu\text{m}$ (○), $L = 17.7 \mu\text{m}$ (◆).

For a given contact size, the ρ_c values obtained using the 1D-approach were also strongly dependent on the overlap size, in contrast to the values, extracted using the 2D-Model (Fig. 4.11). The latter was also observed for the round contacts with various V_{TAPS} (Fig. 4.12).

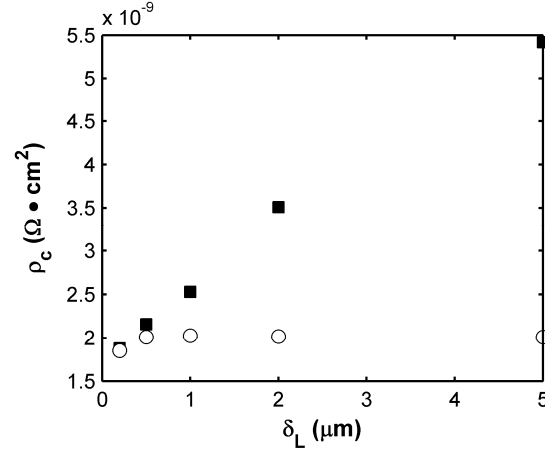


Fig. 4.11. Specific contact resistance obtained using 1D- (■) and 2D-(○) approach vs. δ_L for given $\delta_U = 2 \mu\text{m}$ and square contact size ($L = 8.9 \mu\text{m}$).

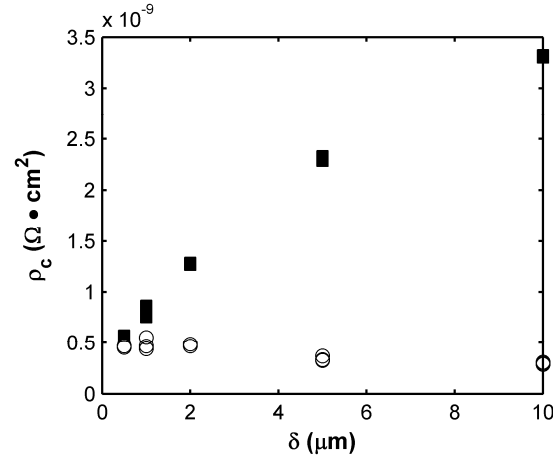


Fig. 4.12. Specific contact resistance obtained using 1D- (■) and 2D-(○) approach vs. overlap size for given round contact size ($D = 5 \mu\text{m}$).

4.6 ρ_c EXTRACTION BY OUR APPROACH

A more accurate approach to extract the ρ_c values is the extrapolation of the measured dependence R_k versus δ to $\delta = 0$, and the calculation of ρ_c from Eq. 1.22, using the R_k value at $\delta = 0$ as the R_c . In this way the model simplifications for deriving Eq. 1.24 can be ignored. However, for larger contacts, the results were still dependent on the contact size. An explanation of this observation is that the current, which contributes to V_{34} , can flow

across a smaller area compared to the actual contact area A . As the contact size becomes larger, this effect enhances, causing significant differences while extracting ρ_c . At first approximation, if a current enters the second material above/below the contact, the current value at every point of the contact is substantially high and can not be neglected. Particularly for relatively large-area and low-resistivity metal-to-metal contacts this is the case. For the larger contacts, the entire contact area was not used; this resulted in the observed dependence of ρ_c on contact area size. However, this dependence could not occur due to the definition of ρ_c (section 1.2.3).

We developed a model to visualize the current transition between the conducting layers through the contact. The model provides a correction for the actual (i.e., non-zero current) contact size. In the following sub-sections we describe the model in detail.

4.6.1 DEFINITION OF GENERAL PARAMETERS

Assuming $\delta = 0$, the contact geometry description can be simplified because $W_x = L$ in this case (see Fig. 1.7). W_y can be defined as W , to generalize the model for non-square contacts. In our currently fabricated structures the upper and lower metal layers have sheet resistances R_{shU} and R_{shL} and thicknesses t_U and t_L . The subscripts U and L correspond to the upper and lower metal, respectively.

4.6.2 MODEL DESCRIPTION

The algorithm to extract the ρ_c is presented in Fig. 4.13. As input data, the following parameters are used: $R_k, I, L, W, R_{shU}, R_{shL}, t_U, t_L$.

The initial approximation for ρ_c, ρ_C^I , is chosen as the value calculated by extrapolating R_k to $\delta = 0$. This assumes the entire contact area to participate in current flow. Then Block I is processed.

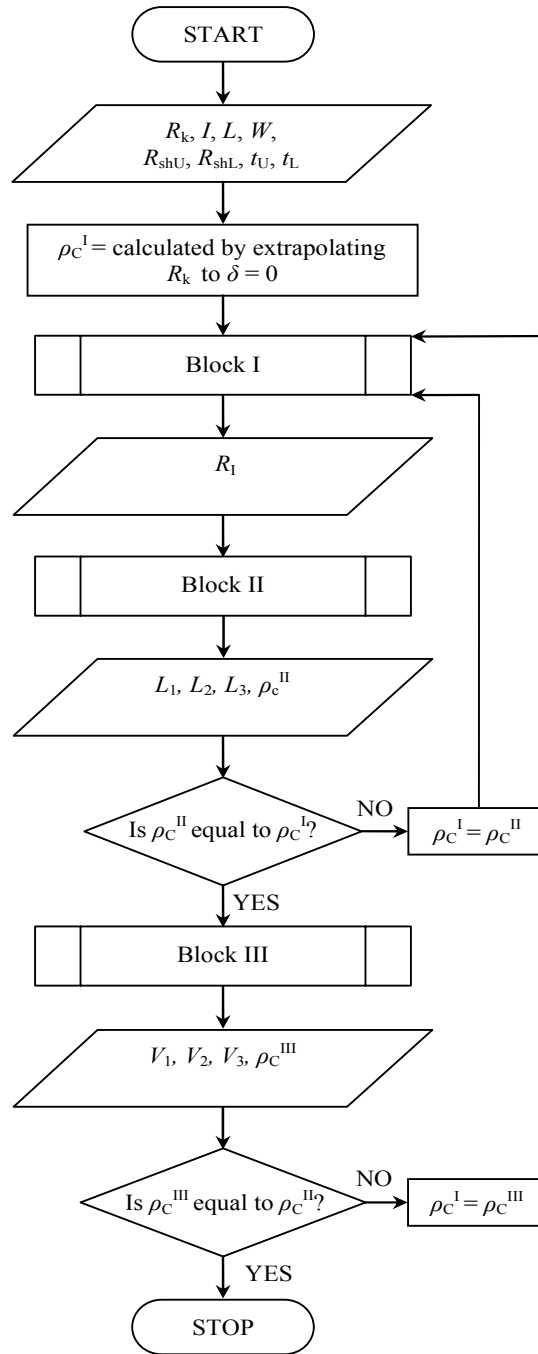


Fig. 4.13. The model flow chart.

BLOCK I

We describe our test structures as two horizontal resistive layers, vertically separated by a resistive contact (Figs. 4.14a and 4.14b). For the given test structures, potential distributions along the contact can be described by the following pair of coupled differential equations [10]:

$$\frac{\partial^2 V_L(x)}{\partial x^2} = \frac{R_{shL}}{\rho_C^I + \rho_G} (V_L(x) - V_U(x)) \quad (4.1)$$

$$\frac{\partial^2 V_U(x)}{\partial x^2} = \frac{R_{shU}}{\rho_C^I + \rho_G} (V_U(x) - V_L(x)), \quad (4.2)$$

where $V_U(x)$ and $V_L(x)$ are the potential distributions in the upper and lower metal layers, respectively, x is the coordinate along the contact length L , and $(\rho_C^I + \rho_G)$ corresponds to the specific contact resistance caused by the properties (ρ_C^I) and the resistance related to the geometry (ρ_G) of the contact. The latter is given in Eq. 4.5. The superscript I refers to the first-level correction of actual ρ_C provided by this Block. To solve Equations 4.1 and 4.2 and to obtain the voltage difference distribution along the contact ($V_{34}(x) = V_U(x) - V_L(x)$, see Eq. 1.21), the following boundary conditions must be applied:

$$\begin{aligned} V_L(x_0) &= V \\ \frac{\partial V_L(x_0)}{\partial x} &= 0 \\ V_U(x_0 + L) &= 0 \\ \frac{\partial V_U(x_0 + L)}{\partial x} &= 0, \end{aligned} \quad (4.3)$$

where x_0 is the initial contact coordinate (i.e., first point where current can enter the upper layer, see Fig. 3a) and $(x_0 + L)$ is the last contact coordinate (i.e., last point where current can enter the upper layer). V is the voltage in the lower metal layer at x_0 . It is assumed that, in the upper layer, the voltage

is zero at $(x_0 + L)$. Furthermore, vertical distribution of V_U and V_L in the corresponding layers is homogeneous for all x -values. The partial derivatives equal zero at x_0 and $(x_0 + L)$ for the lower and upper layer, respectively. This expresses the model simplification that, for $x \leq x_0$ and $x \geq (x_0 + L)$, the resistances of the corresponding lower and upper metal layers are neglected. In other words, $V_L(x) = V$ for $x \leq x_0$ in the lower metal and $V_U(x) = 0$ for $x \geq (x_0 + L)$ in the upper metal. Only the contact area is therefore considered and the potential changes from V to 0 within the contact length. Thus, the voltage drop across L in the current-flow direction equals V . As V is needed for the boundary conditions (see Eq. 4.3), it can be obtained provided known I and resistance in the direction of the current (R_I) as the fitting parameter:

$$V = IR_I. \quad (4.4)$$

The ρ_G , needed to solve Eq. 4.1 and 4.2, can be calculated from the thicknesses of the upper and lower metal layers and their sheet resistances (Fig. 4.14a):

$$\rho_G = R_{shL} t_L^2 + R_{shU} t_U^2. \quad (4.5)$$

Applying the boundary conditions (Eq. 4.3) to Eqs. 4.1 and 4.2 and using R_k as a first approximation for R_I , the voltage distributions $V_U(x)$ and $V_L(x)$ can be obtained. Further, $V_{34}(x)$ is calculated as $(V_U(x) - V_L(x))$. Based on this, $R_{kcalculated}$ can be obtained:

$$R_{kcalculated} = \frac{V_{34calculated}}{I} = \frac{\frac{1}{L} \int_{x_0}^{x_0+L} V_{34}(x) dx}{I}. \quad (4.6)$$

The R_I is continuously used as a fitting parameter within this Block until $R_{kcalculated} = R_k$.

Block I finally results in the $V_{34}(x)$ distribution, which is used as an input for Block II.

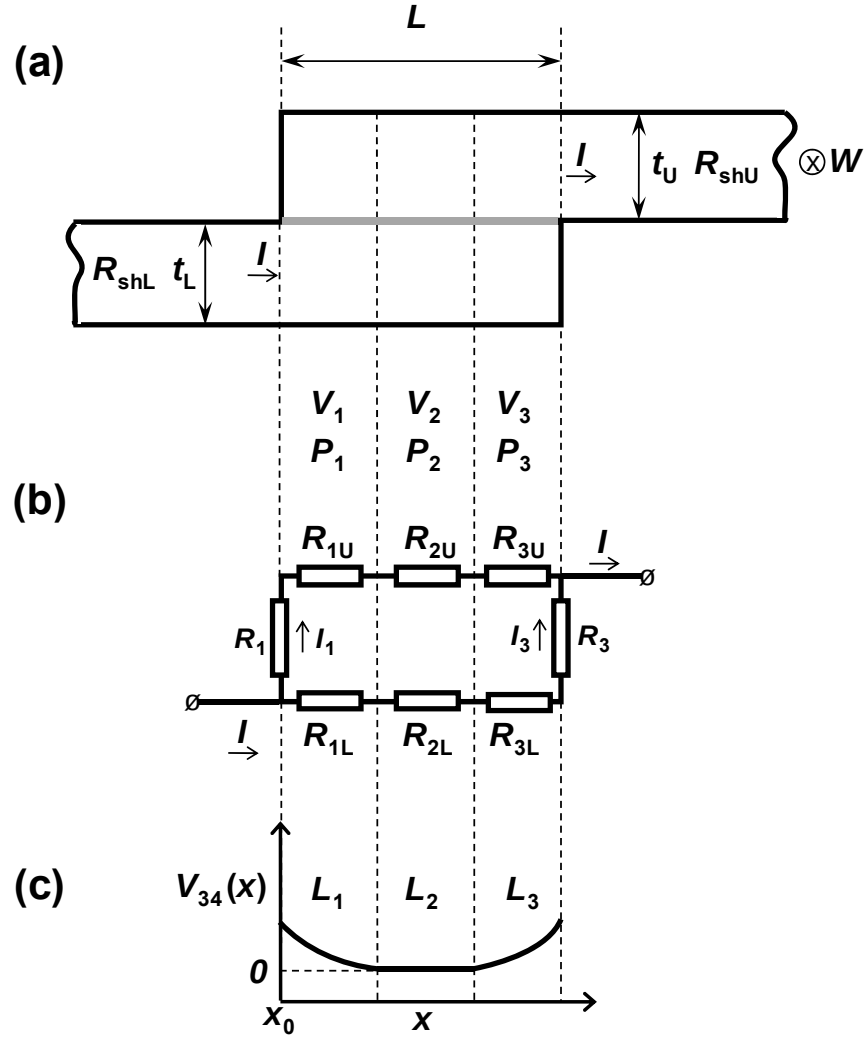


Fig. 4.14. Schematic representation of the two metal layer stack: (a) - cross-section, (b) - corresponding resistor network, and (c) - voltage distribution along the contact coordinate x . The discussed in Block II current-flow sub-areas are shown as L_1, L_2 and L_3 .

BLOCK II

This block is aimed to analyze the current distribution across the contact. If the current value within a given contact area is below the threshold, this area is assumed not to contribute to the contact resistance. In other words, this area can be excluded from the contact area while calculating the ρ_c , which reduces the actual contact size. The local current

value at a given x is determined by the earlier calculated $V_{34}(x)$ and $(\rho_C^I + \rho_G)$.

It is important, for a better understanding, to make first some general remarks and consider two extreme cases. First we assume that, in the lower metal, the current approaches the contact at x_0 from the left-hand side (Fig. 4.14a). For $x_0 > x$ both metals are infinitely long, parallel to each other and have the same sheet resistance. Their (intimate) contact is also infinitely long in this case. Simple analysis reveals that 50 % of the current will transfer to the upper layer and 50 % of the current will remain flowing in the lower layer. Thus, for an infinitely long contact, there will be no current exchange between the lower and upper layers if x exceeds certain transfer length x_{tr} . Now we will attribute a finite length to the lower metal but still keep it sufficiently longer compared to the mentioned x_{tr} . In this case, the lower 50 % of the current must finally be injected into the upper layer. This current transfer between the layers is expected to start at $x = (L - x_{tr})$ and finish at $x = L$.

The above considerations demonstrate that three regions of the current distribution through the contact can be expected (see Fig. 4.14c), depending on the contact length. To describe this mathematically, the contact length L is divided into 3 sub-areas: L_1 , L_2 and L_3 (see Eq. 4.7). L_1 is the first part where the current transfers from the lower into the upper layer, L_2 is the middle part without any current exchange, and L_3 is the third part where the remaining current injects from the lower into the upper layer. For L_1 and L_3 holds $V_{34}(x) \neq 0$. For L_2 , $V_{34}(x)$ equals 0. If L is shorter than $2x_{tr}$, L_2 is equal to zero.

$$L = L_1 + L_2 + L_3. \quad (4.7)$$

After analyzing the dependence $V_{34}(x)$ versus x one can easily extract L_1 , L_2 and L_3 (see Fig. 4.14c). Then, the second-level correction for ρ_c (i.e. ρ_c^{II} , which is now corrected for the actual current flow area) can be obtained:

$$\rho_C^{II} = R_k W(L_1 + L_3) - \rho_G. \quad (4.8)$$

If the calculated sum $(L_1 + L_3)$ reflects the real situation, the obtained ρ_c^{II} must be equal to the ρ_c^{I} . If the latter condition is not satisfied, the algorithm continues to Block III to obtain the third-level correction for ρ_c , i.e. ρ_c^{III} . When $\rho_c^{\text{I}} = \rho_c^{\text{II}} = \rho_c^{\text{III}}$, the iterations stop (see Fig. 4.13).

BLOCK III

The two-metal contact in Fig. 4.14a can schematically be depicted as a resistor network (Fig. 4.14b). The corresponding resistances and currents are expressed below:

$$\begin{aligned}
 R_1 &= \frac{\rho_1}{L_1 W} \\
 R_3 &= \frac{\rho_3}{L_3 W} \\
 R_{iU} &= \frac{R_{\text{sh}U} L_i}{W} \\
 R_{iL} &= \frac{R_{\text{sh}L} L_i}{W} \\
 I_1 &= \frac{V_1}{R_1} = \frac{V_1}{\rho_1} L_1 W \\
 I_3 &= \frac{V_3}{R_3} = \frac{V_3}{\rho_3} L_3 W,
 \end{aligned} \tag{4.9}$$

where ρ_1 and ρ_3 are the specific contact resistances between the upper and lower metal layers in areas L_1 and L_3 , respectively; i is 1, 2 or 3 and indicates the corresponding area, and the subscripts U or L refer to the upper or lower layer, respectively. V_i is a part of $V_{34}(x)$, averaged within the corresponding L_i (Fig. 4.14c).

For each L_i region, the dissipated power P_i can be obtained as:

$$\begin{aligned}
 P_1 &= I_1^2 R_1 + (I - I_1)^2 R_{1L} + I_1^2 R_{1U} \\
 P_2 &= I_1^2 R_{2U} + (I - I_1)^2 R_{2L} \\
 P_3 &= I_3^2 R_3 + I_3^2 R_{3L} + (I_1 + I_3)^2 R_{3U}.
 \end{aligned} \tag{4.10}$$

The total dissipated power, using the energy conservation law, is given by

$$P_{\text{total}} = P_1 + P_2 + P_3 = I^2 R_1. \quad (4.11)$$

For $\rho_1 = \rho_3 = \rho_{\text{CG}}$ ($\rho_{\text{CG}} = \rho_{\text{C}}^{\text{III}} + \rho_{\text{G}}$), substituting Eq. 4.9 into Eq. 4.10 and Eq. 4.10 into Eq. 4.11 reveals

$$\begin{aligned} a \rho_{\text{CG}}^2 + b \rho_{\text{CG}} + c &= 0, \\ a &= I^2 \left[\frac{R_{\text{shL}}}{W} (L_1 + L_2) - R_1 \right] \\ b &= V_1^2 L_1 W - 2IV_1 R_{\text{shL}} L_1 (L_1 + L_2) + V_3^2 L_3 W \\ c &= V_1^2 L_1^2 W \left[(R_{\text{shL}} + R_{\text{shU}}) (L_1 + L_2) + R_{\text{shU}} L_3 \right] + \\ &\quad + V_3^2 L_3^2 W \left[V_3 L_3 (R_{\text{shL}} + R_{\text{shU}}) + 2V_1 L_1 R_{\text{shU}} \right]. \end{aligned} \quad (4.12)$$

Solving Eq. 4.12, one can calculate the ρ_{CG} provided known V_i ($i=1, 2, 3$). To obtain the V_i values, one should integrate $V_{34}(x)$ over the relevant range of x , i.e. using the corresponding L_i values from Block II:

$$\begin{aligned} V_1 &= \frac{1}{L_1} \int_{x_0}^{L_1} V_{34}(x) dx \\ V_2 &= \frac{1}{L_2} \int_{L_1}^{L_1+L_2} V_{34}(x) dx \\ V_3 &= \frac{1}{L_3} \int_{L_1+L_2}^{L_1+L_2+L_3} V_{34}(x) dx \end{aligned} \quad (4.13)$$

Substituting ρ_{CG} in Eq. 4.12 by $(\rho_{\text{C}}^{\text{III}} + \rho_{\text{G}})$ reveals the following equation for $\rho_{\text{C}}^{\text{III}}$:

$$\begin{aligned} A_1 (\rho_{\text{C}}^{\text{III}})^2 + B_1 \rho_{\text{C}}^{\text{III}} + C_1 &= 0 \\ A_1 &= a \\ B_1 &= 2a \rho_{\text{G}} + b \\ C_1 &= c + \rho_{\text{G}} b + a \rho_{\text{G}}^2. \end{aligned} \quad (4.14)$$

For a sufficient number of iterations (Block I $\rightarrow$ Block II $\rightarrow$ Block III $\rightarrow$ Block I $\rightarrow \dots$), $\rho_C^{\text{III}} = \rho_C^{\text{II}} = \rho_C^{\text{I}}$. This criterion is used to stop the iterations. If, however, $\rho_C^{\text{III}} \neq \rho_C^{\text{II}}$, the next iteration loop begins with ρ_C^{III} as the starting value for ρ_C^{I} in Block I (see Fig. 4.13).

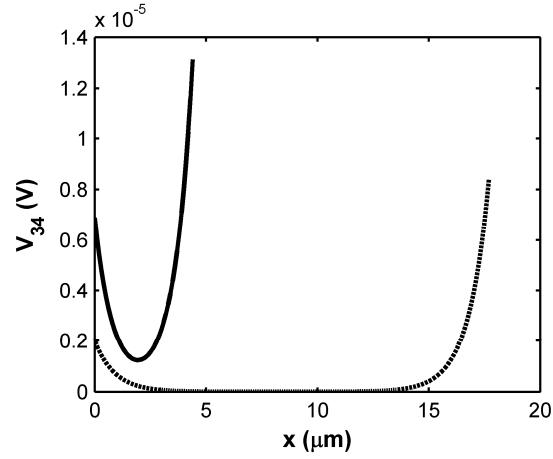
In the model derivations we separate between the specific contact resistance caused by the properties (ρ_C^{I} , ρ_C^{II} and ρ_C^{III}) and the resistance related to the geometry (ρ_G) of the contact. When discussing the real contacts, ρ_G is always a part of the measured contact resistance, therefore we will further use ρ_C as *effective specific contact resistance*, the one that includes ρ_G .

4.6.3 MODEL APPLICATION

Applying the described model (Fig. 4.13) to our measured R_k values, $V_{34}(x) = V_U(x) - V_L(x)$ (i.e., voltage difference distribution along the contact) can be calculated. It is important to note that the $V_{34}(x)$ dependence will indicate the actual current flow areas because the current can only flow from the lower metal layer into the upper metal layer if $V_{34}(x) \neq 0$. It was shown that for the small contacts, the current flow area was identical to that of the physical contact area, while for the larger contacts the current flow area was much smaller than the designed contact area (Fig. 4.15a). The demonstrated approach allowed to estimate the actual current-flow area size A_{cor} ($A_{\text{cor}} < A$). This resulted in a more accurate extraction of ρ_c .

The voltage distribution along the contact was non-symmetrical (Fig. 4.15a) due to the fact that the two metals had different thicknesses and, hence, different sheet resistances. Verification structures with similar upper and lower metal thicknesses show symmetrical voltage distribution, providing validity of our model. A direct comparison of these distributions for the certain contact length is presented in Fig. 4.15b.

(a)



(b)

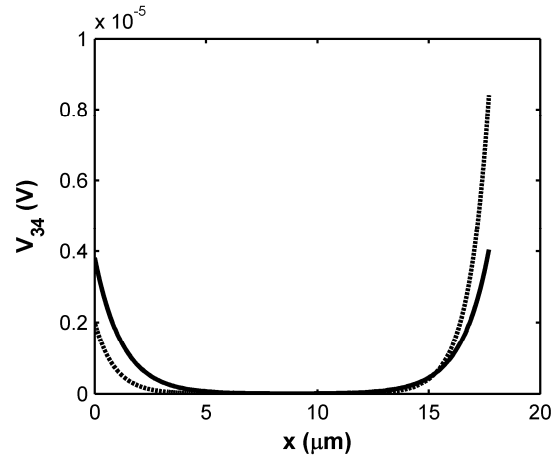


Fig. 4.15. Voltage difference distribution $V_{34}(x) = V_U(x) - V_L(x)$ along the contact coordinate x (a) for the contact length of $4.43 \mu\text{m}$ (solid line) and $17.72 \mu\text{m}$ (dotted line) and differently-thick aluminum as a metal; b) for aluminum with the same thickness (i.e. $R_{shU} = R_{shL} = 0.043 \Omega/\square$, (solid line)) and different thicknesses (i.e. $R_{shU} = 0.054 \Omega/\square$ and $R_{shL} = 0.027 \Omega/\square$, (dotted line)).

These voltage distributions were obtained during processing Block II of the model, resulting in actual current flow area. The ρ_c values were then extracted, as explained in section 4.6.2. The extracted ρ_c values were $(6.31 \pm 0.66) \cdot 10^{-10} \Omega \cdot \text{cm}^2$ (Fig. 4.16, (O)) and they were independent of the contact area, in accordance with the definition of ρ_c (section 1.2.3).

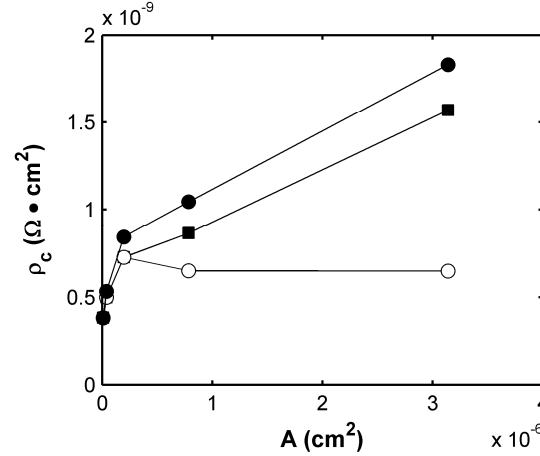


Fig. 4.16. Specific contact resistance vs. contact size obtained using Schreyer and Saraswat model and then extrapolated to $\delta = 0$ (●), the extrapolation of R_k to $\delta = 0$ (■) and our approach, i.e., the current-flow area correction (○).

A comparison of the ρ_c extraction by our approach and other methods is presented in Fig. 4.16. It can be clearly observed, that only our approach results in similar ρ_c values for various contact sizes. This obviously points to the importance of knowing the actual current flow distribution and the area.

4.6.4 COMPARISON WITH A STANDARD SIMULATOR

The total current density distribution was also simulated using ATLAS code (Silvaco Int.). The contact geometry used for the simulations is as shown in Fig. 4.14a. Instead of metal layers, highly doped polysilicon layers (with the resistivity closed to that of metal) were used to prevent convergence problems of the simulator. Silicon oxide was used as an isolation layer. The standard output of the simulation program is the total current density (J) distribution within the structure.

To compare the simulation results with the results obtained using our approach, a cutline along the contact length can be drawn (Fig. 4.17). Visualized 1D J -distribution along the contact must reflect the voltage difference distribution, obtained by our model. The shape of the curve, obtained using the standard simulator is very similar to our results (Fig. 4.17). The curve is symmetrical, since both layers have approximately the same thickness.

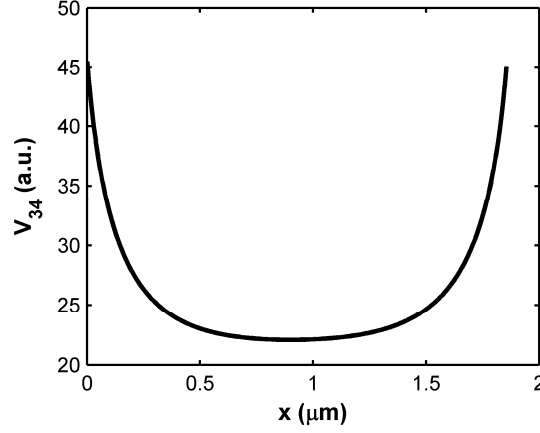


Fig. 4.17. Voltage difference distribution $V_{34}(x)$ along the contact coordinate x , obtained using ATLAS simulator.

The absolute values can not be compared due to the assumptions used to create the structure in ATLAS and therefore V_{34} is plotted in arbitrary units (a. u.).

4.7 THE MINIMUM VALUE OF ρ_c

The R_k values for structures, processed without the RF pre-clean procedure prior to the deposition of the upper metal, were measured as well. A comparison with the results, obtained for structures with RF pre-clean is given in Fig. 4.18. Higher R_k values were measured for the structures without pre-clean (for all contact sizes), indicating presence of a contact interface.

In Eq. 4.5 contribution to the specific resistance, related to geometry of the contact is given. Using the same principle, the resistance of a two metal stack can be calculated. The latter matched very well with the measured R_k values for the structures, processed with the RF pre-clean (i.e., having “ideal” contacts). This means that the minimum value of ρ_c , to be accurately extracted from given CBKR structures, can be determined. It further provides a method for contact interface characterization.

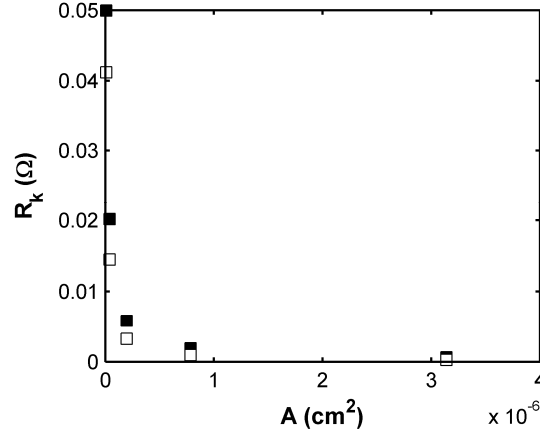


Fig. 4.18. Measured R_k values for the wafers with (□) and without (■) RF pre-clean procedure prior to the upper metal deposition (metals are 1.4 μm thick).

4.8 TEMPERATURE DEPENDENCE

In section 4.7 we observed that the measured R_k values for the “ideal” contacts were determined by the metal stack, i.e., geometry and the sheet resistance. Since sheet resistance is temperature dependent [2] and increases with increasing the temperature, R_k measurement at elevated temperatures can provide a good verification.

The wafers were measured at 200 °C and the obtained R_k values were compared with the results at room temperature. An example of such a comparison can be found in Fig. 4.19. The measured at 200 °C R_k values were higher than those at room temperature, for various contact sizes as expected.

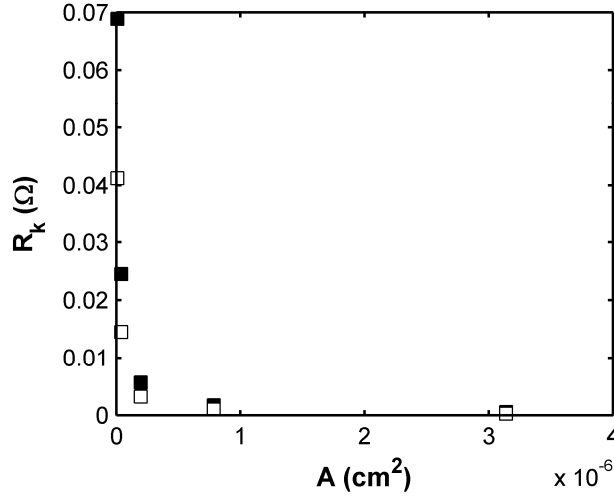


Fig. 4.19. Measured R_k values at the room temperature ($\square$) and at 200 °C ($\blacksquare$) (metals are 1.4 μm thick).

4.9 CONCLUSIONS

Design and fabrication of various metal-to-metal CBKR structures have been performed. The structures included a large variety of contact geometries, i.e., various shapes and sizes for contact holes and overlap regions.

The obtained behavior of Kelvin resistance, R_k , was in agreement with the analytical model proposed by Schreyer and Saraswat. This demonstrated the necessity to account for 2D current flow effects around the contact area while measuring low contact resistance values. However, as the calculated ρ_c values were still dependent on the contact size, we developed a new correction method to account for the actual current-flow areas through the contact. The approach allowed to obtain a voltage difference distribution along the contact length and led to a physically-correct extraction of the ρ_c . The comparison of our approach with the standard simulator revealed similar shapes of the voltage difference distribution. An extra advantage of our model is that it is an analytical model that uses the measured data as an input to extract the ρ_c .

The measured R_k values for the structures processed with RF pre-clean

procedure corresponded to the two-metal stack resistance, calculated from the given dimensions of the contact size and sheet resistances of the metals used. The measurements were verified at room temperature and at 200 °C. The measured R_k values for the wafers processed without RF pre-clean procedure were higher, indicating presence of the contact interface. This can be used to improve contact process characterization in contact manufacturing. Finally, the minimum value, to be accurately extracted from the CBKR structures, was determined.

In this work the aluminum-aluminum contacts have been analyzed. For the present technology nodes using copper metallization, the properties of e.g. the Cu - Ta(N) - Cu contact structures can be described accordingly.

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5

SILICIDE-TO-SILICON CBKR STRUCTURES

The purpose of this chapter is to apply the evaluated CBKR structures (chapter 4) to characterize silicide-to-silicon contacts with NiSi, PtSi, CoSi₂ and TiSi₂ as silicides. The structures were processed for two different silicide geometries, i.e., for the silicide contact embedded into the silicon (built-in geometry) or for the silicide contact placed on top of the silicon (planar geometry). The results obtained for both geometries were compared and examined for different test structure parameters. The measured values for built-in and planar geometry were in the same range. The results show, that the contact resistance was not sensitive to the silicon consumption during built-in silicide formation. The behavior of the measured Kelvin resistance R_k on geometry demonstrated the necessity of 3D-modeling, and an analytical approach was not applicable. To understand this behavior, the total current density was numerically simulated by simplifying the 3D contact configuration to a 2D-modeling structure. The modeling provided a qualitative explanation of the R_k behavior. Based on this, an estimation of a silicide-to-silicon ρ_c was made. First approximation of the ρ_c showed good agreement with the ρ_c , obtained using TLM structures (see chapter 3).

The first section of this chapter starts with the motivation, followed by the experimental approach in the second section. The third section presents test structures fabrication, i.e., the experimental process flow. The R_k values as a function of test structure geometry parameters, i.e., shapes and dimensions, are discussed in section 5.4 for various silicides. The modeling of the current distribution and the estimation of a silicide-to-silicon ρ_c can be found in section 5.5. Finally, in section 5.6 the conclusions are drawn.

5.1 MOTIVATION

It is well known from literature [1]-[3] and it has also been demonstrated in this work (section 4.6) that the actual current flow distribution is of great importance for contact resistance analysis. Various contact geometries can behave quite differently because the *effective* contact area might differ from the *actual* contact area (section 4.6.3). For this reason, it was decided to study the silicide-to-silicon contact resistance for two different silicide geometries:

- (i) silicide embedded into silicon,
- (ii) silicide on top of silicon.

The test structures chosen for this study are CBKR structures. These structures have been already evaluated for metal-to-metal contacts in chapter 4 and will be evaluated in this chapter for the application for different silicide-to-silicon contacts.

5.2 EXPERIMENTAL APPROACH

The same CBKR structures, presented and discussed in chapter 4, were used to fabricate silicide-to-silicon contacts with NiSi, PtSi, CoSi₂ and TiSi₂ as silicides. NiSi and PtSi were chosen as a reference to TLM structures (chapter 3). CoSi₂ and TiSi₂ were chosen as well-known silicides in the literature (section 1.1.3, [4]-[7]).

As stated in chapter 1, most of the silicides in modern process technology are made using a SALICIDE process (section 1.1.2, [8]-[10]). This process results in silicides, that are *built-in* into the silicon (Fig. 1.2).

There are more methods to form silicides. One of these methods is sputter deposition. Sputtering is basically a deposition process where atoms or molecules are ejected from a target by high-energy particle bombardment (usually Ar ions) and the ejected atoms or molecules are condensed on a substrate as a thin film [11], [12]. In the case of sputtering a silicide from a metal and a silicon target, the correct sputtering rates of the metal and silicon

must be carefully determined and applied to ensure proper deposition of the silicide film.

Sputter deposition of silicides comes in various forms [9]. For instance, sputtering from two targets using multi-pass sputtering systems achieves the appropriate mixture of metal and silicon in a layered, atomically mixed structure. Sintering then completes the chemical reaction between the metal and silicon to form the silicide. Sputtering from a composite target (MSi_x) can also be done. It allows a better, but fixed compositional control, and it is vulnerable to contamination issues associated with composite targets.

In this work, the co-sputtering method was chosen as a second method to form silicides. The structures obtained by co-sputtering are planar structures. The geometries of the silicides, formed using two different processes, are illustrated in Fig. 5.1. We will further refer to the silicides, formed in the SALICIDE as to *built-in silicides* and to the silicides, formed using co-sputtering technique as to *planar silicides*.

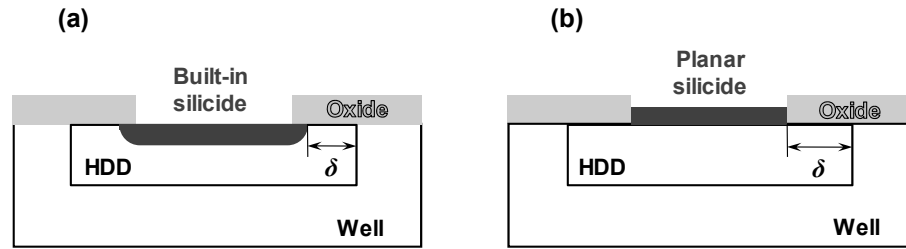


Fig. 5.1. Schematic cross-section of planar (a) and built-in (b) silicide geometries.

The CBKR structures used to study the silicide-to-silicon contacts were discussed in detail in chapter 4. The important geometry characteristics, i.e., overlap size δ (Fig. 5.1) and contact size L are summarized in Table 5.1.

Table 5.1. Important geometry parameters of our silicide-to-silicon CBKR structures

Built-in silicide	Planar silicide	δ (see Fig.5.1) μm	L μm
NiSi	NiSi	0.2, 0.5, 1, 2, 5	1, 2, 4.4
PtSi	PtSi	0.2, 0.5, 1, 2, 5	1, 2, 4.4
CoSi_2	CoSi_2	0.2, 0.5, 1, 2, 5	1, 2, 4.4
TiSi_2	TiSi_2	0.2, 0.5, 1, 2, 5	1, 2, 4.4

5.3 TEST STRUCTURES FABRICATION

As a starting material, (100)-oriented p-type silicon wafers were used. First, a thin scatter oxide layer was grown by dry oxidation. Then, two dopant implantations were carried out:

- (i) Half-blanket, low-dose well implantation of either P ($8 \cdot 10^{12} \text{ cm}^{-2}$ dose at 420 keV) for n-well or B ($1 \cdot 10^{13} \text{ cm}^{-2}$ dose at 180 keV) for p-well, followed by RTP annealing (1000 °C for 20 s in N₂);
- (ii) Lithographically defined HDD implantation of either B ($3 \cdot 10^{15} \text{ cm}^{-2}$ at 5keV) in n-well or As ($3 \cdot 10^{15} \text{ cm}^{-2}$ at 30keV) in p-well, followed by spike annealing (1100 °C at 133 ppm of O₂).

To define the contact areas, 70 nm of silicon oxide was deposited by Low-Pressure Chemical Vapor Deposition (LPCVD) and patterned using I-line lithography and a combination of dry and wet etching.

To form built-in silicides, the corresponding metal layers were deposited followed by one- (for PtSi) or two-step (for NiSi, CoSi₂ and TiSi₂) annealing procedures (RTP1 and RTP2). The thicknesses of the sputtered Ni and Pt layers and the corresponding annealing recipes were similar to the recipes used to fabricate TLM structures (section 2.3). The non-reacted metal on the oxide area was selectively removed by wet etching. The fabrication of built-in silicides is summarized in Table 5.2.

Table 5.2. The recipes of the fabrication of the built-in silicides.

Silicide	Metal thickness nm	RTP1	Selective etch	RTP2
NiSi	10	300°C, 43 s in N ₂	SRM* 10 min	470°C, 43 s in N ₂
PtSi	13	500°C, 30 s in O ₂	AR** 5 min	no
CoSi ₂	15	500°C, 30 s in N ₂	SPM 5 min	700°C, 30s in N ₂
TiSi ₂	20	670°C, 30 s in N ₂	APM*** 10 min	900°C, 30s in N ₂

*SPM – **Sulfuric acid hydrogen Peroxide Mixture** (H₂SO₄ and H₂O₂)

AR – **Aqua Regia, i.e., hydrochloric and nitric acid mixture (HCl and HNO₃)

***APM – **Ammonium hydroxide hydrogen Peroxide Mixture** (NH₄OH and H₂O₂)

Standard back-end processing was applied to finalize the test structures, i.e., deposition and patterning of TiW (100 nm) and Al (500nm) layers.

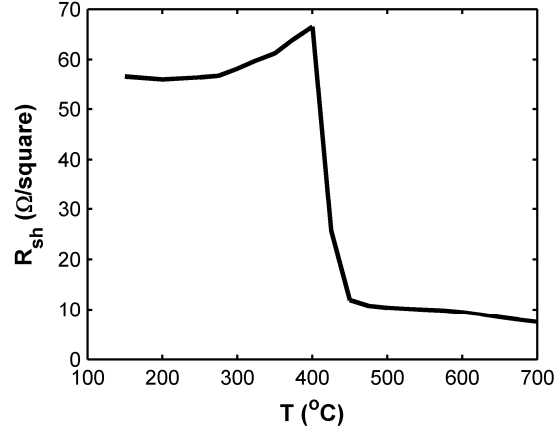
For the planar devices, the silicides were co-sputtered using Leybold Emerald (for NiSi and TiSi₂) and Perkin-Elmer 4400 (for PtSi and CoSi₂) deposition systems, **to obtain purposely the slightly silicon deficient silicides**. The composition was characterized for all four silicides using the Rutherford Backscattering Spectrometry (RBS) technique [1], **from where the thickness of silicides was determined**. From the deposition recipes (Table 5.3), one can see that the deposition process results in atomic scale mixture. For example for PtSi deposition, each rotation results in a metal-and-silicon thickness of 0.42 nm (120 rotations/50 nm PtSi thickness), i.e., approximately the thickness of two atomic layers. The sputtering time (see Table 5.3) for planar silicides was chosen to enable the silicide thickness of 50 nm.

Table 5.3. Deposition recipes for co-sputtered (planar) silicides.

Silicide	Ar flow SCCM	Ar pressure Torr	Deposition power W	Target voltage V	Rotation speed RPM	Deposition time
Ni:Si=1:1	80	9.5×10^{-3}	500	610 (Ni) 280 (Si)	8	21'12''
Pt:Si=1:1	60	5.2×10^{-3}	400	500 (Pt) 1360 (Si)	4	30'
Co:Si=1:2	60	5.2×10^{-3}	500	550 (Co) 1400 (Si)	4	28'
Ti:Si=1:2	80	9.5×10^{-3}	1000	170 (Ti) 480 (Si)	8	9'30''

The silicides were further annealed and patterned. The annealing recipes for planar silicides were identical to the second annealing step of the built-in silicides. The quality of the planar silicides was verified by sheet resistance measurements. Examples of R_{sh} dependence on temperature for NiSi and CoSi₂ can be found in Figs. 5.2a and 5.2b, respectively. The corresponding RTP temperatures for NiSi and CoSi₂ were 470 °C and 700 °C, respectively.

(a)



(b)

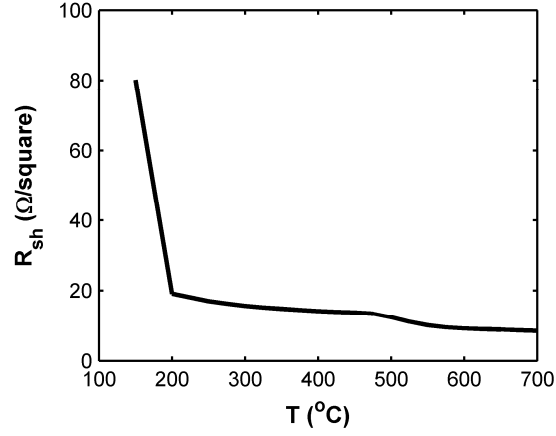


Fig. 5.2. Sheet resistance measurements as a function of annealing temperature for planar NiSi (a) and planar CoSi₂ (b). The RTP temperatures were 470 °C (for NiSi) and 700 °C (for CoSi₂).

5.4 MEASUREMENT RESULTS AND DISCUSSION

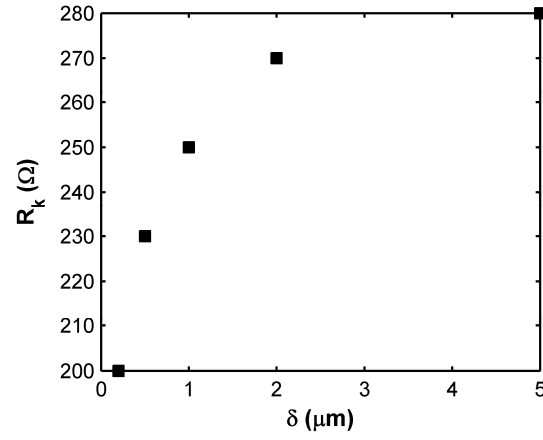
The silicide-to-silicon CBKR structures were measured as explained in section 1.3.3, resulting in R_k values (Eq. 1.21).

The R_k data for the planar TiSi₂-to-p-HDD contacts as a function of the overlap size δ (see Fig. 1.9) before and after annealing are given in Figs. 5.3a and 5.3b, respectively.

It can be seen that R_k values prior to RTP2 annealing were much higher than those after annealing. This clearly indicates that the silicide-silicon interface before annealing is not yet defined and it serves as a measure of the valid annealing process.

The R_k values of the planar structures ($L = 1 \mu\text{m}$) before annealing increase with increasing δ (Fig. 5.3a). This *classic behavior* was predicted by Schreyer and Saraswat (section 1.3.3) and it was observed in this work for

(a)



(b)

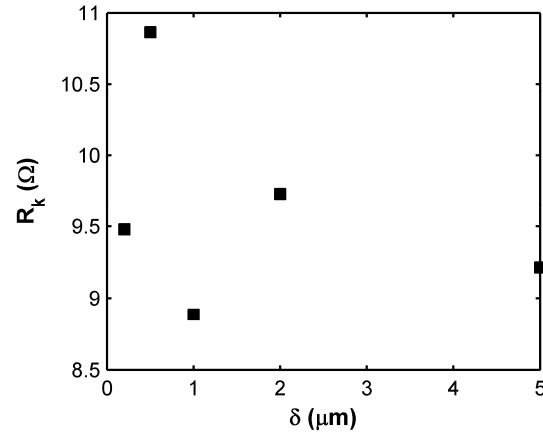
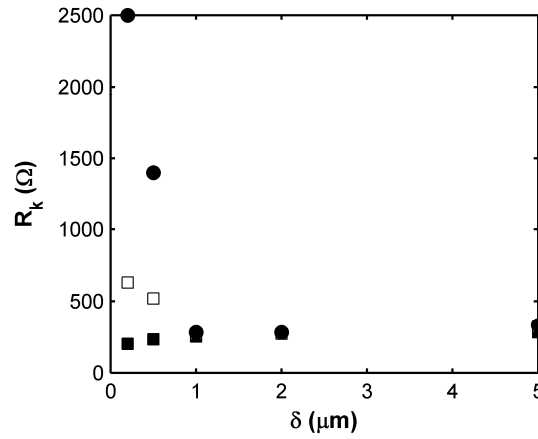


Fig. 5.3. Measured Kelvin resistance vs. overlap size for given contact area size ($L = 1 \mu\text{m}$) for planar TiSi_2 -to-p-HDD contacts before (a) and after (b) annealing.

metal-to-metal contacts (section 4.4). This is in agreement with the *classic* theory (Eq. 1.24), demonstrating, that for $\delta > 0$, the lateral current flow gives rise to an additional voltage drop that is included in V_{34} , leading to a higher R_k value.

The R_k values decreased after annealing and yielded no classic behavior (Fig. 5.3b). Moreover, for the unannealed structures with the contact size larger than $L = 1 \mu\text{m}$, i.e., for $L = 2 \mu\text{m}$ and $L = 4.4 \mu\text{m}$, this classic behavior was not observed either (Fig. 5.4a).

(a)



(b)

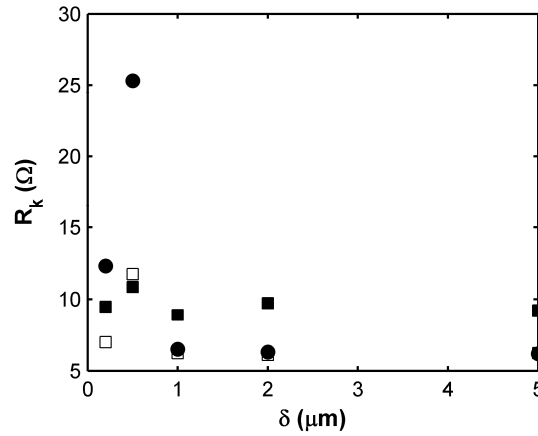


Fig. 5.4. Measured Kelvin resistance vs. overlap size for planar TiSi_2 -to-pHDD contacts before (a) and after (b) annealing for various contact sizes: $L = 1 \mu\text{m}$ (■), $L = 2 \mu\text{m}$ (□), $L = 4.4 \mu\text{m}$ (●).

The annealed planar TiSi_2 -to-p-HDD structures exhibited the following R_k dependence on the overlap size: the R_k values increased for small δ (0.2 and 0.5 μm) and then decreased and remained approximately constant for large δ (1, 2 and 5 μm). The larger the contact size, the higher the R_k value in the *transition zone*, i.e., between $\delta = 0.5 - 1 \mu\text{m}$.

The R_k data for built-in TiSi_2 -to-p-HDD contacts as a function of δ are given in Fig. 5.5. The R_k values were in the same range as for the annealed planar TiSi_2 -to-p-HDD contacts and a similar dependence on δ occurred.

The aforementioned measurements were also performed for TiSi_2 -to-n-HDD contacts. The same trends, observed for all TiSi_2 -to-p-HDD contacts, were also observed in this case. An example of the R_k dependence on δ for built-in TiSi_2 -to-n-HDD contacts is given in Fig. 5.6. The R_k values for TiSi_2 to both n- and p-HDD contacts were approximately in the same range. A comparison of the absolute values would not be appropriate for n- and p-type HDD areas. According to the Schottky barrier height, the contact resistance of TiSi_2 -to-n-HDD must be lower than that to p-HDD (Table 1.1), but this holds for the same active dopant concentration only.

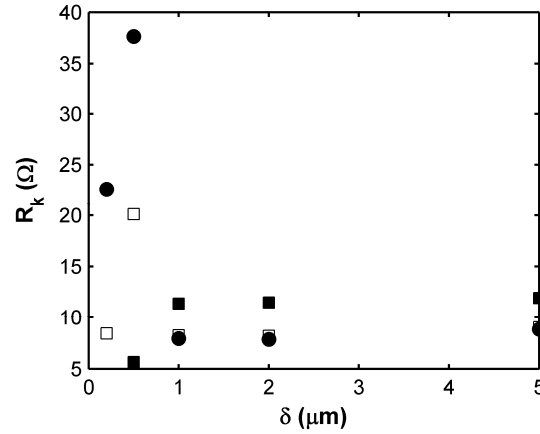


Fig. 5.5. Measured Kelvin resistance vs. overlap size for built-in TiSi_2 -to-p-HDD contacts for various contact sizes: $L = 1 \mu\text{m}$ (■), $L = 2 \mu\text{m}$ (□), $L = 4.4 \mu\text{m}$ (●).

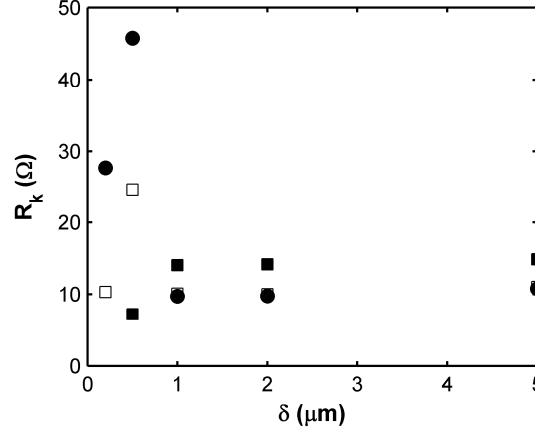
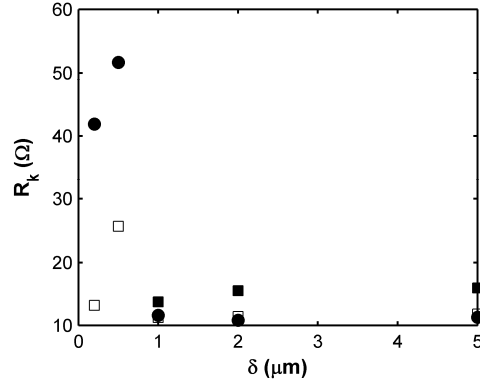


Fig. 5.6. Measured Kelvin resistance vs. overlap size for built-in TiSi_2 -to-n-HDD contacts for various contact sizes: $L = 1 \mu\text{m}$ (■), $L = 2 \mu\text{m}$ (□), $L = 4.4 \mu\text{m}$ (●).

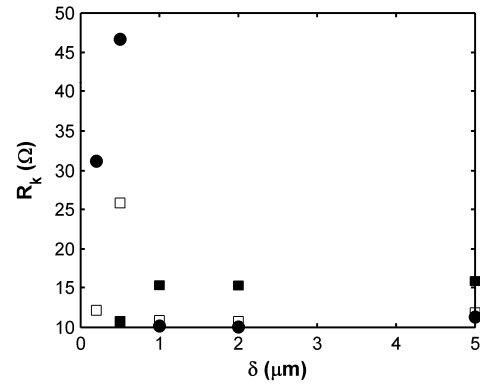
It is known from literature [13] and it is demonstrated in this work (chapter 3) that, for high dopant concentration, the active dopant concentration is the main factor that determines the specific contact resistance. Therefore, it is crucial to know the exact active dopant concentration of both p- and n-HDD areas, to be able to compare the corresponding contact resistances. Both HDD areas were similarly-high doped to obtain similar high dopant concentrations. However, as shown in chapter 3, for high dopant concentrations the *active* dopant concentration can be lower than the total concentration.

The same analysis was performed for the other planar and built-in NiSi , PtSi and CoSi_2 formed on both p- and n-HDD regions. The R_k dependence on overlap size was similar to that of TiSi_2 . The same trends occurred with the increasing of the contact size. The results for all the silicides were consistent for both the planar and built-in geometries, and for n- and p-HDD areas. The several examples can be found in Figs. 5.7a, 5.7b and 5.7c.

(a)



(b)



(c)

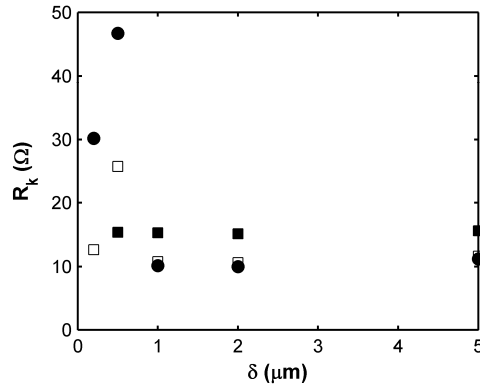


Fig. 5.7. Measured Kelvin resistance vs. overlap size for built-in PtSi (a), CoSi₂ (b) and NiSi (c) to-n-HDD contacts for various contact sizes: $L = 1$ μm (■), $L = 2$ μm (□), $L = 4.4$ μm (●).

5.5 MODELING

The obtained behavior of measured Kelvin resistance (i.e., no gradual increase of R_k versus δ) does not allow to extrapolate R_k to $\delta = 0$ and apply the developed approach for metal-to-metal contacts from chapter 4. In the case of silicide-to-silicon contacts with a low contact resistance it is not possible to eliminate one parameter, i.e., δ and develop an analytical model to correct only for the actual contact size. Clearly, in this case both δ and L have to be considered simultaneously.

To understand the R_k behaviour, the total current density distribution was simulated using ATLAS code (Silvaco Int.), by simplifying the 3D- to a 2D-contact configuration. The 2D-contact model used for the simulations is shown in Fig. 5.8. Instead of the silicide and HDD region, highly doped polysilicon layers (with corresponding resistivity close to that of silicide or HDD) were used to prevent convergence problems of the simulator. Silicon oxide was used as an isolation layer. To simulate different contact resistances, an additional layer was introduced between the silicide and HDD region, defined as silicon in the simulator. To change the contact resistance, the resistivity of this layer was properly adjusted. The layer could additionally be removed to reflect the case of very low contact resistance.

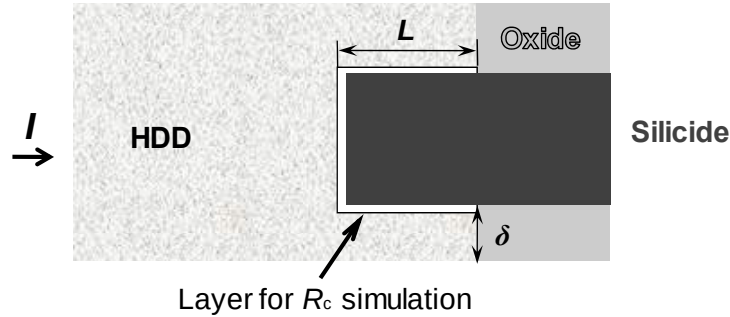
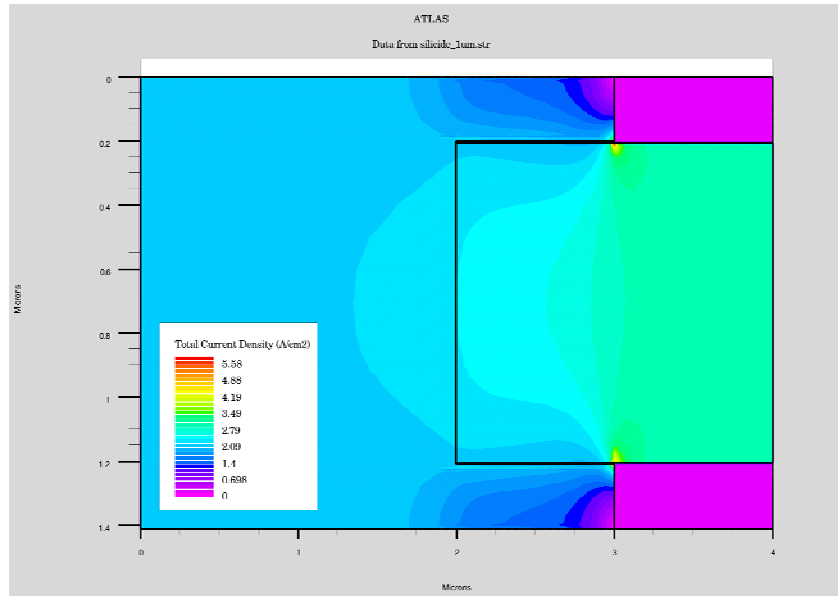


Fig. 5.8. The contact model used for simulations, i.e., simplifying 3D-contact into 2D-contact.

In section 5.4, the R_k dependencies on δ were demonstrated. It was shown that R_k (i) increased for small δ and (ii) remained approximately constant for large δ (Figs. 5.4b-5.7).

(a)



(b)

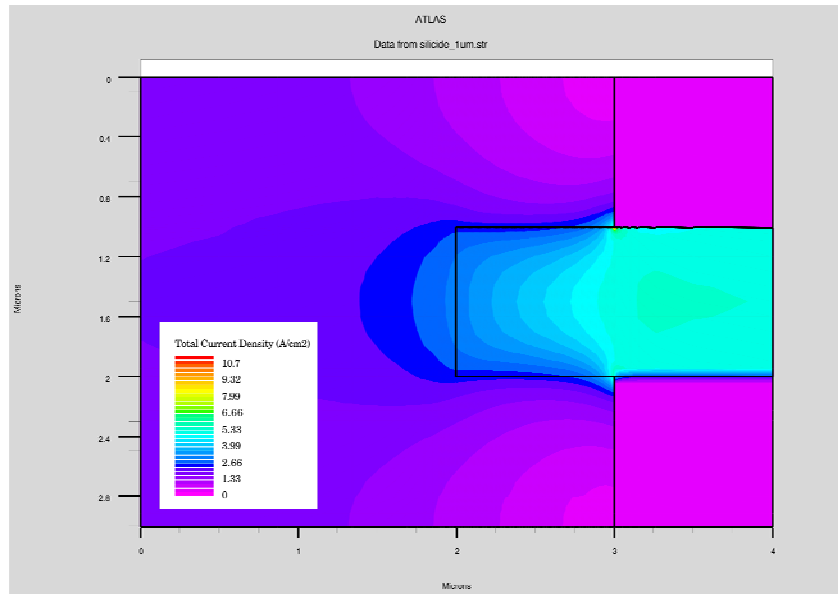


Fig. 5.9. The total current density distribution in silicide-to-silicon contacts, obtained using ATLAS simulator: (a) the case for small overlap size $\delta = 0.2 \mu\text{m}$; (b) the case for large overlap size $\delta = 1 \mu\text{m}$.

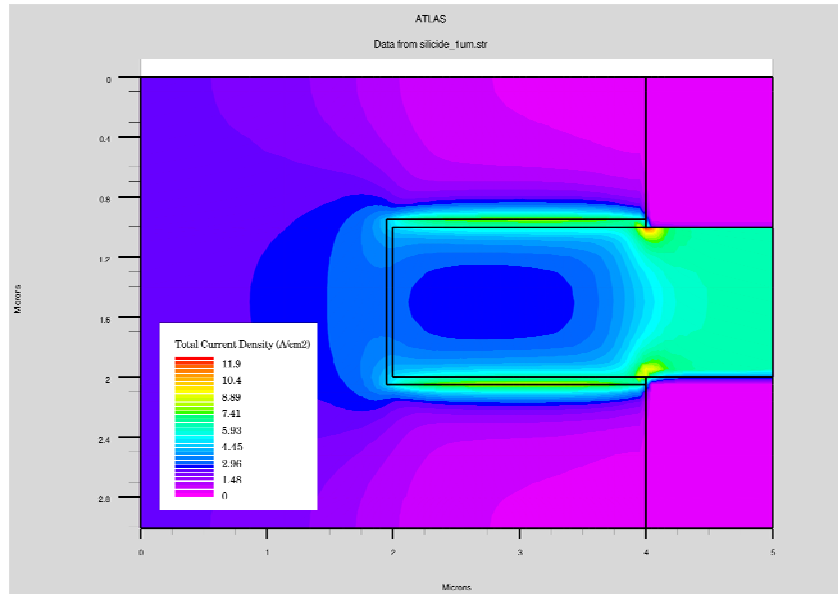
The simulations were performed to imitate these two cases. The current density distribution was simulated for the fixed contact size ($L = 1 \mu\text{m}$) and two different overlap sizes, i.e. $\delta = 0.2 \mu\text{m}$ (Fig. 5.9a) and $\delta = 1 \mu\text{m}$ (Fig. 5.9b) for the case of low contact resistance.

It can be clearly seen that for the small δ , almost the entire overlap area is involved in the current density distribution. For the larger δ , this is not the case – a significant part of the overlap area shows a zero or close to zero current density. From the measurements (Figs. 5.4b-5.7), the R_k values remained approximately the same for large δ . An explanation to this effect is that, for a given contact size, the current crowding occurs across certain δ , depending on the contact resistance and the sheet resistance of the HDD area. As δ increases, the lateral current flow gives rise to an additional voltage drop that is included in V_{34} , leading to a higher R_k value. If the δ -limit is reached, with further increase of the physical δ the actual δ -area involved in the current flow remains unchanged, leading to constant R_k values.

Another effect, observed in section 5.4 is the different R_k behavior for high and low contact resistances, as demonstrated in Figs. 5.4a and 5.4b. To reflect this situation, the current density distribution was simulated for the chosen contact and overlap sizes considering either a high (Fig. 5.10a) or low (Fig. 5.10b) contact resistance. The simulation results revealed a completely different current distribution along the contact for these two cases. For the higher contact resistance, the current density was distributed homogeneously along the contact length. This is in contrast to the case of the low contact resistance. This again highlights the importance of knowing the *actual* contact size. Another important observation is that, although the physical δ is defined being the same for the two cases, the actual δ -area involved in the current flow is different.

Figure 5.10 demonstrates the complexity of the current density distribution. In fact, three parameters determine the R_k behavior: δ , L and silicide-to-silicon contact resistance (for a given sheet resistance of silicon).

(a)



(b)

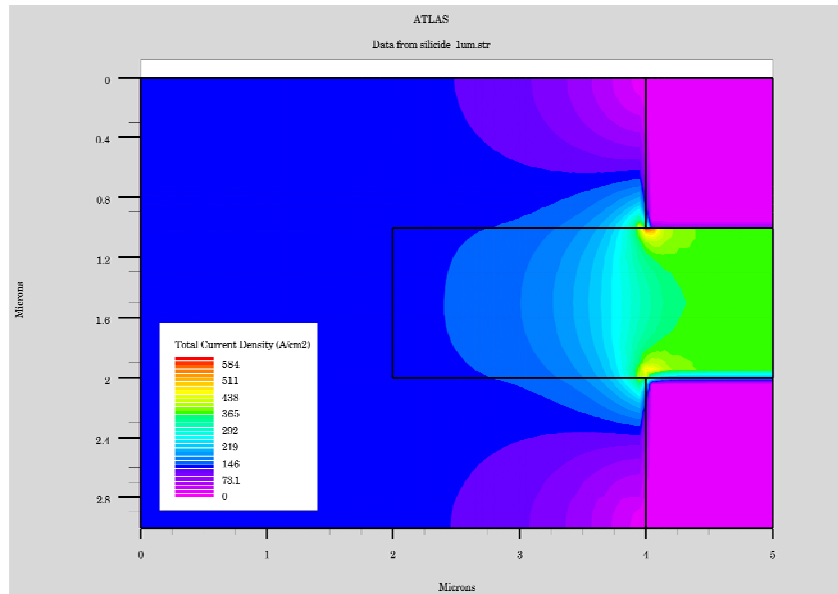


Fig. 5.10. The total current density distribution in silicide-to-silicon contacts, obtained using ATLAS simulator: (a) case of a high contact resistance; (b) case of a very low contact resistance.

These parameters can not be analysed separately: they all play an important role for R_k , and hence, make the contact characterization more complicated.

The real situation is even more complex, since the ATLAS simulations were performed for the simplified 2D-contact geometry, and not for the real 3D-contact configuration.

Although the accurate extraction of the silicide-to-silicon ρ_c can not be performed, a first estimation of this value can be done. Based on simulations, the probability of the actual current flow to be distributed over the entire contact and overlap is higher for the smallest CBKR structures. Assuming that the actual current flow area for the smallest contact size ($L = 1 \mu\text{m}$) is the same as the physical contact size, and the current also flows across the whole overlap size (for $\delta = 0.2$ or $0.5 \mu\text{m}$), the ρ_c values can be calculated. These values range from $\sim 6 \cdot 10^{-8}$ to $\sim 8 \cdot 10^{-8} \Omega \cdot \text{cm}^2$ for silicide-to-silicon contacts with NiSi, PtSi, CoSi₂ and TiSi₂ as silicides. This approximation of ρ_c shows a good agreement with the ρ_c , obtained using TLM structures.

5.6 CONCLUSIONS

CBKR structures were applied to characterize silicide-to-silicon contacts with NiSi, PtSi, CoSi₂ and TiSi₂ as silicides. The structures were processed for two different silicide geometries, i.e., silicide contact embedded into the silicon (built-in geometry) and silicide contact on top of the silicon (planar geometry). The results obtained for both geometries were compared and examined for different test structure parameters.

The measured R_k values for the built-in and planar geometry were in the same range. The results show, that the contact resistance was not sensitive to the silicon consumption during built-in silicide formation.

The obtained behavior of Kelvin resistance R_k demonstrated the necessity of numerical 3D-modeling, since an analytical approach was not applicable. To understand this behavior, the total current density was simulated by simplifying the 3D- to a 2D-contact configuration. The simulation results underlined the complexity of the current distribution, expressed by three parameters that determine the R_k behavior: δ , L and

silicide-to-silicon contact resistance (for a given sheet resistance of silicon). These parameters have to be taken into account simultaneously while studying R_k , which significantly complicates the contact characterization. This is in contrast to the metal-to-metal contacts from chapter 4, where R_k behavior allowed to first extrapolate the R_k values to $\delta = 0$, and afterwards correct it for the actual current flow size.

The modeling provided a qualitative explanation of the R_k behavior. Based on this, an estimation of a silicide-to-silicon ρ_c was made. First approximation of the ρ_c for these CBKR structures showed good agreement with the ρ_c , obtained using TLM structures.

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6

SUMMARY AND CONCLUSIONS

The purpose of this chapter is to highlight the motivation for this research, to shortly overview the performed experiments as well as to summarize the main achievements and the important conclusions of this work.

The performance of Si integrated circuits depends on the transistor drive current. The drive current of a MOS transistor is determined by the total device resistance, which consists of the channel resistance and the parasitic resistances associated with dopant diffusion areas and contacts. It is expected that the contact resistance between silicide and source/drain regions will significantly contribute to the total series resistance. The reduction of this contact resistance and the corresponding specific contact resistance is an important issue. Thus the ability to accurately obtain the specific silicide-to-silicon contact resistance is essential for contact processing. It therefore requires dedicated test structures and a reliable extraction method of this specific contact resistance.

The main purpose of this thesis is to develop and examine various types of test structures and the corresponding models for silicide-to-silicon specific contact resistance characterization.

The first test structure discussed in this thesis is the TLM structure. The importance of using optimized TLM structures to measure the silicide-to-silicon contact resistance has been motivated. Optimized, in terms of the number of silicide segments and their lengths, the TLM test structures were fabricated and characterized. These structures were designed to provide a better fit and a higher accuracy using the Scott method. The TLM structures were evaluated for NiSi- and PtSi-to-silicon contacts, because of the technological importance of these silicides. The ρ_c extraction method and the measurement drawbacks were discussed in terms of uniform silicide formation and the results of TEM analyses. The TLM structures were evaluated at different temperatures. The observed decrease of the ρ_c values with increasing temperature was in agreement with theory. The lowest dopant concentration of p- and n-type silicon was determined, where NiSi- and PtSi-to-silicon specific contact resistance could be extracted.

This work provided an important reference for the further use of TLM structures, also applicable to other silicides. It contributed to the development of test structures and outlined the requirements to characterize NiSi- and PtSi-to-silicon contacts by the TLM method.

Further, the optimized TLM structures were processed for a broad range of n- and p- type silicon dopant levels. NiSi and PtSi were used as silicides in order to compare the data known from literature for thoroughly studied PtSi, and provide novel systematic measurement data for NiSi. Using systematic measurements on optimized TLM structures to determine PtSi-to-silicon ρ_c , the disagreements with the literature values have been explained in terms of active dopant concentrations and different measurement limitations of various test structures. Based on our study of PtSi-to-silicon ρ_c , the ρ_c values obtained for NiSi-to-silicon were validated. Temperature dependence of the contact resistance of NiSi-to-silicon served as an additional confirmation and it was in agreement with theory. The NiSi data were obtained from the structures fabricated by CMOS technology, using a standard SALICIDE recipe. These very low ρ_c values further favor the use of NiSi in modern CMOS processes.

Summarizing, a unique database for NiSi-to-silicon ρ_c was created for a wide range of doping levels, which is important for the development of modern contact technology.

The obtained ρ_c values of NiSi and PtSi to silicon were low, compared to published results reported by others. For this reason the origin of the low ρ_c values was investigated.

In other works values in this low range were achieved using dopant segregation techniques. This hypothesis was tested using SRP analysis and the absence of substantial active dopant segregation was observed. In addition, SIMS depth profiling showed no dopant segregation either. Dopant segregation is therefore not the explanation for the low contact resistances obtained.

To achieve such low values, the silicide-silicon interface should be of a high quality. The NiSi-silicon interface was purposely damaged by Ni implantation into realized TLM structures. The increasing implantation doses led to a higher contact resistance, which could only be partially annealed out at a subsequent anneal.

The results confirm that low ρ_c values for a certain active dopant level can be obtained, given a silicide formation process flow resulting in a good silicide-silicon interface.

Another test structure discussed in this thesis is the CBKR structure. The parasitic factors that strongly influence the measurement accuracy of CBKR structures have been extensively discussed during last few decades. The minimum ρ_c value, to be accurately extracted, has been estimated. The purpose of the experiments in this thesis was to confirm this minimum value experimentally for low resistivity metal-to-metal contacts. Design and fabrication of various metal-to-metal CBKR structures have been performed. The structures included a large variety of contact geometries, i.e., various shapes and sizes of contact holes and overlap regions.

The obtained behavior of the measured Kelvin resistance, R_k , was in agreement with the analytical model proposed by Schreyer and Saraswat. This demonstrated the necessity to account for 2D current flow effects around the contact area while measuring low contact resistance values. However, as the calculated ρ_c values were still dependent on the contact size, a new correction method to account for the actual current-flow areas through the contact was developed. The approach allowed to obtain a voltage difference distribution along the contact length and led to a physically-correct extraction of the ρ_c . The comparison of our approach with the standard simulator revealed a similar shape of the voltage difference distribution. An extra advantage of our model is that it is an analytical model that uses the measured data as an input to extract the ρ_c .

The measured R_k values for the structures processed with an RF pre-clean procedure corresponded to the resistance of the two-metal stack. These values could be calculated from the given dimensions of the contact size and sheet resistances of the metals used. The measurements were verified at room temperature and at 200 °C. The measured R_k values for the wafers processed without RF pre-clean procedure were higher, pointing at the presence of a contact interface. This indication can be used to improve contact process characterization in contact manufacturing.

Finally, the model, which led to a physically-correct extraction of the ρ_c , was created. The minimum value to be accurately obtained from the CBKR structures was determined.

These CBKR structures were further applied to characterize silicide-to-silicon contacts with NiSi, PtSi, CoSi₂ and TiSi₂ as silicides. The structures were processed for two different silicide geometries, i.e., for silicide contacts embedded into the silicon (built-in geometry) and for silicide contacts placed on top of the silicon (planar geometry). The results obtained for both geometries were compared and examined for different test structure configurations.

The measured R_k values for the built-in and planar geometry were in the same range. The results show, that the contact resistance was not sensitive to the silicon consumption during built-in silicide formation.

The obtained behavior of the measured Kelvin resistance R_k demonstrated the necessity of numerical 3D-modeling, since an analytical approach could not be applied. To understand this behavior, the total current density was simulated by simplifying the 3D- to a 2D-contact configuration. The simulation results underlined the complexity of the current distribution, expressed by three parameters that determine the R_k behavior: δ , L and silicide-to-silicon contact resistance. These parameters have to be taken into account simultaneously while analyzing R_k , which significantly complicates characterization of the specific contact resistance. The modeling provided a qualitative explanation of the R_k behavior. Based on this, an estimation of ρ_c for the silicide-to-silicon contacts was made.

First approximation of the ρ_c for these CBKR structures showed good agreement with the ρ_c , obtained using the TLM structures. Hence systematic characterization of test structures resulted in a reliable and consistent determination of the specific contact resistance of silicide-to-silicon contacts.

SAMENVATTING

Dit proefschrift behandelt de karakterisering van de specifieke contactweerstand van (metaal)silicides met silicium. Hiervoor worden teststructuren gebruikt die in dit proefschrift worden toegelicht. Uit de meetgegevens van die structuren kan de specifieke contactweerstand worden bepaald. De verschillende teststructuren worden vergeleken, hun beperkingen worden beschreven en de gemeten waarden worden gestaafd met modellen.

De kwaliteit en prestaties van geïntegreerde schakelingen in silicium zijn sterk afhankelijk van het stroomvoerend vermogen van die schakelingen. De stroom in een basiselement van de schakeling, een MOS transistor, wordt op zijn beurt bepaald door de totale weerstand van deze transistor. Die weerstand is de som van verschillende weerstanden:

- de kanaalweerstand;

- de parasitaire weerstanden, die gerelateerd zijn aan de “source/drain” diffusiegebieden;

- de weerstand van de metaal-halfgeleider contacten.

In het bijzonder de contactweerstand tussen het (metaal)silicide en de “source/drain” gebieden draagt sterk bij aan de totale weerstand van de transistor. Het verkrijgen van kennis over de vorming van de contactweerstand en de bepaling van de gerelateerde specifieke contactweerstand zijn de belangrijke aandachtspunten in dit onderzoek. Speciaal ontwikkelde teststructuren voor het meten van de contactweerstand en een betrouwbare extractiemethode om de specifieke contactweerstand te bepalen zijn hiervoor essentieel. *Het hoofddoel van dit onderzoek is om speciale teststructuren te ontwikkelen om daaruit de specifieke contactweerstand (ρ_c) betrouwbaar af te kunnen leiden.*

De eerste teststructuur die onder de loep wordt genomen is de zogenaamde Transmissielijn Model (TLM) structuur. Hiermee zijn de contactweerstand voor NiSi- en PtSi-silicium gemeten. Deze structuur is, in ons geval, geoptimaliseerd om de waarde van ρ_c met een hoge nauwkeurigheid te kunnen bepalen. Zowel de extractie methode van ρ_c als de beperkingen worden behandeld aan de hand van het geometrische ontwerp,

een uniforme silicide vorming en de resultaten van de Transmissie Electronen Microscoop (TEM) analyse. Tevens is de laagste doping concentratie van p- en n-type silicium bepaald waarbij de specifieke contactweerstand voor NiSi- en PtSi-silicium contacten nog betrouwbaar bepaald kan worden. *Het verkregen begrip vormt een belangrijke basis voor verder gebruik van deze TLM structuur. Deze is overigens ook bruikbaar voor andere silicides.*

Vervolgens zijn geoptimaliseerde TLM structuren gefabriceerd met verschillende doping niveaus van p- en n-type silicium. NiSi en PtSi zijn gebruikt als contactmateriaal. Deze silicides zijn gekozen vanwege hun technologisch belang. Bovendien kunnen de meetgegevens van PtSi direct vergeleken worden met uitgebreide gegevens uit de literatuur. Door systematisch de ρ_c te bepalen van geoptimaliseerde TLM structuren zijn voor PtSi contacten discrepanties met waarden uit de literatuur verklaard. Hierbij spelen actieve doping concentraties en de meetbeperkingen van verschillende teststructuren een rol. De gevonden waarden van ρ_c voor NiSi-silicium contacten zijn systematisch geanalyseerd, gebaseerd op dezelfde teststructuren die gebruikt zijn voor onze studie naar de ρ_c voor PtSi. *Er is hiermee een uniek gegevensbestand opgebouwd voor ρ_c voor NiSi-silicium contacten voor een grote variatie in de doping concentratie, dat van belang is voor de ontwikkeling van moderne contact technologieën.*

De verkregen waarden van ρ_c voor NiSi en PtSi contacten naar silicium zijn laag vergeleken met gegevens uit de literatuur. Het is bekend dat, voor een gegeven doping niveau, lagere waarden bereikt kunnen worden door doping segregatie aan het silicide-silicium grensvlak. Dit is, in ons geval, getoetst met behulp van “Spreading Resistance Probe (SRP)” en “Secondary Ion Mass Spectrometry (SIMS)” analyses. Hieruit is echter geen substantiële doping segregatie gevonden, waardoor dit niet kan worden aangevoerd als de reden voor de lage gemeten contactweerstand. Een belangrijke voorwaarde om lage ρ_c waarden te krijgen is een silicide-silicium grensvlak met een hoge kwaliteit. Dit is aangetoond door het NiSi-silicium grensvlak in gefabriceerde TLM structuren bewust te beschadigen door een Ni

implantatie met als gevolg een verhoogde contactweerstand. Deze wordt slechts gedeeltelijk ongedaan gemaakt door de structuur te verhitten. *Deze resultaten bevestigen dat lage ρ_c waarden voor een gegeven doping niveau verkregen kunnen worden, wanneer het silicide-silicium grensvlak van goede kwaliteit is.*

De tweede teststructuur die in dit proefschrift wordt beschouwd is de “Cross Bridge Kelvin Resistor (CBKR)” structuur. De parasitaire factoren die van invloed zijn op de nauwkeurigheid van de bepaling van ρ_c zijn veelvuldig besproken in de literatuur. Ook is de minimale waarde van ρ_c , die nog nauwkeurig bepaald kan worden, een punt van discussie. Structuren met een grote variatie in contactgeometrie zijn ontworpen. De variaties bestaan uit onder andere verschillen in de vorm en grootte van de contact gaten en de overlapgebieden. De structuren zijn gerealiseerd in verschillende metaal-metaal contacten met een lage weerstand. De gemeten Kelvin weerstanden R_k zijn in overeenstemming met het analytische model van Schreyer en Saraswat, dat rekening houdt met 2D stroomdistributie effecten rondom het contact. De berekende waarden van ρ_c blijken af te hangen van de contactgrootte. Hiervoor is een nieuwe correctie methode ontwikkeld, die een voltageverdeling langs de lengte van het contact bepaalt. Hiermee is een fysisch correcte extractie van ρ_c mogelijk. Onze analytische beschrijving is geverifieerd met de resultaten van een standaard simulator. De gemeten R_k weerstandswaarden voor zuivere metaal-metaal structuren komen overeen met de weerstand van de dubbele metaal stapeling. Deze waarde legt de minimale waarde van ρ_c vast. De gemeten R_k waarden van structuren die op voorhand gemaakt zijn met een minder zuiver metaal-metaal contact zijn hoger. Dit duidt op de aanwezigheid van een contact interface. *Uiteindelijk is er een model ontwikkeld, dat leidt tot een fysisch correcte extractie van ρ_c . De minimale waarde van ρ_c , die nog nauwkeurig bepaald kan worden uit CBKR structuren, is vastgesteld.*

De CBKR structuren zijn verder toegepast om silicide-silicium contacten te karakteriseren met NiSi, PtSi, CoSi₂ en TiSi₂ als silicides. De structuren zijn ontwikkeld.

Voor twee verschillende silicide geometrieën: de silicide contacten bevinden zich in het silicium (ingebouwde geometrie) of op het silicium (vlakke geometrie).

De gemeten R_k waarden voor de ingebouwde en vlakke geometrie liggen in hetzelfde bereik. Dit toont aan dat de contactweerstand in dit geval niet beïnvloed wordt door de afname van silicium bij de vorming van de ingebouwde geometrie.

Aangezien een analytische beschrijving niet kan worden toegepast om de gemeten Kelvin weerstandswaarden te verklaren, is het nodig om een numeriek 3D model te gebruiken. Hiervoor is de totale stroomdichtheid gesimuleerd door de 3D contactstructuur te vereenvoudigen naar een 2D structuur. De simulatieresultaten tonen de complexiteit van de stroomverdeling aan. Er zijn drie parameters die de R_k bepalen, namelijk het overlapgebied, de grootte van het contact en de silicide-silicium contactweerstand. Bij het karakteriseren van R_k moeten deze parameters tegelijkertijd meegenomen worden. Het uitvoeren van de simulaties met behulp van het model geeft een kwalitatieve verklaring voor de gemeten R_k waarden en er kan een redelijke schatting gemaakt worden van de waarde van ρ_c . *In eerste benadering is de waarde van ρ_c voor deze CBKR structuren in goede overeenstemming met de waarden van ρ_c die verkregen zijn voor de TLM structuren. Al met al laat de systematische karakterisering van de teststructuren zien dat er betrouwbare en consistente waarden voor de specifieke silicide-silicium contactweerstand verkregen kunnen worden.*

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Almost everybody looks forward to writing this part of his/her thesis, for several reasons. Firstly, if you have gotten this far, your dissertation has been already approved by the committee and you have more confidence that you are soon going to get your title. Secondly, you finally have an official opportunity to express your gratitude to your colleagues, friends, and family. Finally, you know that this part of your dissertation will be read by every person who will ever get a copy in his/her possession.

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As every foreigner knows, the first months are spent dealing with paper work, settling in and arranging a lot of bureaucratic stuff. This would have been very difficult if not for the group's secretary, Annemiek Janssen. She arranged everything for me. Thank you for this, Annemiek, and for the other administrative help during these years.

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I must admit that half a year went by so fast, I would rather say too fast...and the moment had come to return to the Netherlands.

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Before the reader gets an impression that I quit traveling and spent these three years only in Twente, I must stop and tell you about the projects and collaborations I was involved in.

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ABOUT THE AUTHOR

Natalie Stavitski received her B.Sc. degree in Chemistry from the Hebrew University of Jerusalem and her M.Sc. degree in Chemistry Science, from the Weizmann Institute of Science, Rehovot, Israel, in 2000 and 2003, respectively. She conducted her master assignment at the Department of Materials and Interfaces, Faculty of Chemistry. Her master thesis is entitled “Substrate-free Crystallization of Thin Films: Pyroelectric Hexagonal BaTiO₃”.

From 2002 to 2005 she was a member of the engineering staff with the Intel Corporation, Jerusalem, Israel, where she worked in the area of photolithography processes. Her primary focus was on improving and optimizing microfabrication processes and corresponding equipment.

She decided to pursue a Ph.D. degree to acquire technical knowledge in the field of electrical engineering. In April 2005 she joined the Chair of Semiconductor Components, Faculty of Electrical Engineering, Mathematics and Computer science, in the University of Twente, Enschede, the Netherlands. The main purpose of her research was to develop and examine various types of test structures and the corresponding models for silicide-to-silicon specific contact resistance characterization.

Within the framework of her research project, Natalie successfully completed two internships: at Philips Research within IMEC, Leuven, Belgium and at NXP Semiconductors Research, Eindhoven, the Netherlands, in 2006 and 2009, respectively.

The results of her work were published in well-respected international scientific journals and presented at (inter)national conferences. During her Master and Ph.D. studies Natalie performed numerous educational tasks, and supervised and assisted several students.

This dissertation is the summary of her Ph.D. research.