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Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	10848399	
Application number	EP19188924.5	
Date of receipt	12 April 2022	
Filing Office	European Patent Office, The Hague	
Procedural phase	All procedures	
Your reference	M/KIE-150-EP/A1	
Documents submitted	package-data.xml epf1038.pdf (1 p.) CLMS-1.pdf\KIE-150-EPA1_claims_clean.pdf (2 p.)	ep-sfd-request.xml EXRE3-1.pdf\KIE-150-EPA1_Response to Office Action.pdf (5 p.) CLMS-HWA-1.pdf\KIE-150-EPA1_claims_m-up.pdf (2 p.)
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/European Patent Office/

NEW CLAIMS
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1. ~~An integrated circuit structure~~ A FinFET transistor, comprising:

a substrate (600);

isolation regions (610, 620) on the substrate (600),

a semiconductor fin (660) ~~comprising silicon~~extending from the substrate (600) through the isolation regions (610, 620);

a gate electrode (640) over the fin (660);

a first source or drain region in the fin (660) proximate a first side of the gate electrode (640), the first source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650) recessed with respect to the upper surfaces of the isolation regions (610, 620), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on one fin sidewall, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded from a base level compatible with the substrate (600) to a concentration in excess of 50 atomic %; **(para. [0054] cf. 1-3 OA)**

a first boron doped germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) between the epitaxial region (631) and the respective isolation region (610, 620) of the first source or drain region, the first boron doped germanium cap layer ~~comprising germanium and titanium and~~ having a germanium concentration in excess of 95 atomic %;

a second source or drain region in the fin (660) proximate a second side of the gate electrode (640) opposite the first side, the second source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650) recessed with respect to the upper surfaces of the isolation regions (610, 620), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded from a base level compatible with the substrate (600) to a concentration in excess of 50 atomic %; and

a second boron doped ~~germanide~~ germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) between the epitaxial region (631) and the respective isolation region (610, 620) of the second source or drain region, the second boron doped germanium cap layer ~~comprising germanium and titanium and~~ having a germanium concentration in excess of 95 atomic %.

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20 cm^{-3}.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20cm^{-3}.

NEW CLAIMS

CLEAN

1. A FinFET transistor, comprising:

a substrate (600);

isolation regions (610, 620) on the substrate (600),

a semiconductor fin (660) extending from the substrate (600) through the isolation regions (610, 620);

a gate electrode (640) over the fin (660);

a first source or drain region in the fin (660) proximate a first side of the gate electrode (640), the first source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650) recessed with respect to the upper surfaces of the isolation regions (610, 620), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on one fin sidewall, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded from a base level compatible with the substrate (600) to a concentration in excess of 50 atomic %;

a first boron doped germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) between the epitaxial region (631) and the respective isolation region (610, 620) of the first source or drain region, the first boron doped germanium cap layer having a germanium concentration in excess of 95 atomic %;

a second source or drain region in the fin (660) proximate a second side of

the gate electrode (640) opposite the first side, the second source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650) recessed with respect to the upper surfaces of the isolation regions (610, 620), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded from a base level compatible with the substrate (600) to a concentration in excess of 50 atomic %; and

a second boron doped germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) between the epitaxial region (631) and the respective isolation region (610, 620) of the second source or drain region, the second boron doped germanium cap layer having a germanium concentration in excess of 95 atomic %.

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20 cm^{-3}.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20cm^{-3}.

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Letter accompanying subsequently filed items

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The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number:	EP19188924.5
Applicant's or representative's reference	M/KIE-150-EP/A1

	Description of document	Original file name	Assigned file name
1	Reply to examination report	KIE-150-EPA1_Response to Office Action.pdf	EXRE3-1.pdf
2	Amended claims (clean copy)	KIE-150-EPA1_claims_clean.pdf	CLMS-1.pdf
3	Amended claims with annotations	KIE-150-EPA1_claims_m-up.pdf	CLMS-HWA-1.pdf

Annotations

Authorisation of Association No. 19 (Melita Kapun; 12.04.2022)
1. Remark (Annotate)
Association No. 19 is authorised to represent in this case.

Signatures

Place:	**Munich**
Date:	**12 April 2022**
Signed by:	**/Andrew Parker/**
Representative name:	**Andrew Parker**
Capacity:	**Representative**
Function of person signing:	**Representative**

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ANSPRECHPARTNER | CONTACT	IHR ZEICHEN | YOUR REF.	UNSER ZEICHEN | OUR REF.	DATUM | DATE
Dr. Andrew Parker	19188924.5	M/KIE-150-EP/A1	April 12, 2022 PA/cd/kk

European Patent Application No. 19188924.5
CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
Intel Corporation

Dear Madam/Sir,

In response to the Official Communication of October 14, 2021.

We request that examination be continued on the basis of the following documents:

- claims 1-3 as enclosed;
- description pages 1, 1a as filed on June 16, 2020;
- description pages 2-29 as originally filed; as well as
- drawing sheets 1/11-11/11 as originally filed.

The Examiner will note that the Applicant has chosen to file an amended set of claims 1-3 that is based on claims 1-3 as filed on November 6, 2020, and as discussed herein below. These claims replace the claims presently on file. A marked-up copy of the claims is enclosed for the Examiner's convenience.

Support for the amendments can be found in parentheses in the marked-up claims and as discussed below.

Remarks:

1. The Examiner has raised a number of objections on the basis that the claims are not unambiguously supported by the parent disclosure. The Applicant has, as the Examiner will note, included a number of additional aspects to the claims in order to overcome the objections in this file.

2. The fin is described as a semiconductor fin which extends from the substrate, which can be seen in paragraph [0044] of the originally filed application, this teaching has been adopted. Regarding the objections in 1.2: in the Applicant's view, the bilayer structure is properly defined in the claim already. The first and second source or drain regions are properly defined as comprising an epitaxial region (631) which is itself comprised of silicon and germanium. The cap layer is also described as being deposited on the epitaxial region, and this is a boron doped germanium cap layer. The Applicant is a little unsure why the Examiner thinks these features are not included in the claim, and believes that this objection is misplaced.

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3. The Applicant also does not see the clarity in including that the epitaxial region is implemented using an in situ doped silicon or silicon germanium. Firstly, the section of the description highlighted by the Examiner already indicates that this is an optional feature, and secondly it seems to be a process step in order to form the silicon germanium structure. The Applicant is concerned that this could raise clarity issues as being a product-by-process feature, wherein in fact it is merely the presence of the doped silicon germanium region which should be included in the claim.

4. Turning to the objection 1.3, the Examiner has highlighted the two different embodiments shown in paragraphs [0054] and [0055]. Given that the Examiner actually highlights that these two relate to separate embodiments, it is surprising that paragraph [0055] is being discussed. The Applicant notes that paragraph [0054] fully supports the concentrations claimed for the first and second source or drain regions and the boron doped germanium cap layers. Given that the Examiner also indicates that the discussion in paragraph [0055] is a separate embodiment, it is unclear why the fully supporting embodiment of paragraph [0054] should be combined with

paragraph [0055] in the Office Action. The Applicant believes that no modification needs to be made at this stage, the description at paragraph [0054] as highlighted by the Examiner fully supports the claimed concentration ranges and no modification appears necessary.

5. The objection under 1.4 appears to relate to clarity. It seems that the Examiner has concerns with how the claimed structure of the recess source or drain interface with the epitaxial region therein and the first boron doped germanium cap layer being provided in the recessed source or drain interface, should be understood. This also seems to have led to issues with regard to the overlap with the cited art. The Applicant expressly incorporates the substrate as well as isolation regions formed on the substrate into the claim. Incorporating the isolation regions clearly defines the nature of the recessed source or drain interface, this being recessed with respect to the upper surfaces of the isolation region. This is perfectly clear from the description in Fig. 6, and further clarifies the understanding of the recessed tip region according to paragraph [0045] of the application as filed. This added feature also properly clarifies the structure being claimed, whilst also greatly assisting in further distinguishing over the cited art.

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6. The Applicant deletes the reference to titanium in the claims. The discussion of adding titanium into the FinFET structure according to Fig. 6 is limited. The titanium according to the planar devices will be added once the cap layer has been formed, and an anneal step will be undertaken. The disclosure according to the FinFET in Fig. 6 does not, however, properly introduce the use of the metal, in particular titanium. Given that the presence of titanium is not necessary for distinguishing over the cited art, as the Applicant discusses below, removal of titanium is beneficial as this avoids possible objections as to undisclosed features, whilst also maintaining the inventive subject matter in the claim.

7. As has been discussed in the Office Action from the Examiner, and in previous Communications, the claims distinguish over document D1 at least in relation to the provision of the cap layers. It is clear that Fig. 14 of D1 shows a layered electrode which will be positioned according to Fig. 12 at Section 1210. It is to be noted that the layered electrode from Fig. 14 in D1 is not present in a recessed source or drain interface which is recessed with respect to the upper surfaces of the isolation regions, as required by the claims. The recess which the Examiner refers to, is that on the

spacer layer around the gate electrode. This physical recess also assists in properly defining the tip regions for the cap layers as also claimed. As was previously discussed with the Examiner, the additional features included in claim 1 which distinguish over document D1 are related to improving the resistance characteristics of a FinFET. It is further noted that a combination of documents D1 and D3 will at no point introduce the tip structures as now claimed between the epitaxial silicon germanium layer and the isolation region. The tips extending between this gap improve the resistance connections further, and are a structure which cannot be obtained by combining documents D1 and D3.

8. Document D3 does suggest increasing further the concentration of the germanium in the equivalent of the epitaxial region. There is no disclosure in document D3 suggesting the use of adding a boron doped germanium layer: the section referred to by the Examiner at paragraph [0090], is an indication that the germanium concentration should be increased possibly even to 100 atomic %. Consequently, adding the teachings from document D3 into D1 would simply lead to increasing the germanium content even further. Although the disclosure in paragraph [0039] of D1 suggests the use of boron doping, this is again to be used in the graded silicon germanium epitaxial layer. There is no suggestion of using a separate boron doped germanium cap layer as described, and consequently a combination of documents D1 and D3 does not suggest this feature of claim 1.

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9. The Applicant also notes, in reference to FIG. 6, that the epitaxial layer 631 is of a germanium-silicon composition which has a different lattice constant than the underlying substrate (which is typically doped silicon only). This lattice mismatch induces strain in the epitaxial layer 631, which also strains the regions immediately surrounding this lattice mismatched region. The specific intent of using such a lattice mismatched material is to induce strain in the channel between the source and drain. If the induced channel strain is properly oriented, such strain enhances the mobility of the carriers (electrons or holes) in the channel region. Such mobility enhancement improves the transistors' maximum speed of operation – a very important parameter of such devices.

10. The cap layer 641 is a very heavily boron doped layer. Using such a heavily doped layer results in a reduction in contact resistance of a subsequently deposited metal or metal alloy. This layer need not be strained or even epitaxially deposited, as

its purpose is simply to reduce the contact resistance of the subsequently deposited contact. The contact resistance can be further reduced by grading the germanium concentration of the epitaxial layer 631 from a lower level at the bottom to a high level at the top.

11. Support for the above is provided in the specification as originally filed, especially in the paragraphs that reference FIGS. 6 and 7. See, for example, paragraphs [0035-0038].

12. The Applicant is well aware that the description is not yet in line with the new claims. The description will, of course, be adapted in the appropriate manner once an allowable version of the claims has been found. It is requested that at present, in the interests of expediency, revision of the description is postponed in order to avoid the unnecessary recasting of pages.

In the circumstances, the Examiner is asked to reconsider the outstanding objections and to acknowledge the patentability of the new claims in principle. The Applicant is, of course, readily prepared to make further clarifications to the application documents, if necessary.

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Should the Examiner care to raise further questions or comments, we would be delighted for the Examiner to contact the undersigning attorney directly to discuss the application and/or to arrange for a **personal consultation by telephone**. If the Examiner considers it appropriate, we would also be happy to receive a positive proposal of amendments in this file, so as to expedite the Examination Proceedings.

13. Oral Proceedings are requested in this application as a matter of precaution only.

Yours faithfully,

Dr. Andrew Parker
European Patent Attorney

Enclosure
- New claims 1 to 3 clean and marked-up

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Questions about this communication?
Contact Customer Services at www.epo.org/contact

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Date 01.03.2022

Reference	Application No./Patent No.
J100788EPA	19188924.5 - 1212 / 3582265
Applicant/Proprietor: INTEL Corporation	

Extension of time limit pursuant to Rule 132(2) EPC

Examination procedure

With reference to your request, the time limit for replying to the communication pursuant to Article 94(3) EPC dated 14.10.21 has been extended

by 2 months

to a total of 6 months

from the date of notification of the above-mentioned communication.

Please note: To the extent that your request exceeded the above extension, your request has been refused.

Note
The granting of extensions to time limits is governed by the Implementing Regulations to the EPC and the Guidelines for Examination in the EPO, E-VIII, 1.6. A request for extension, which would result in the total period set exceeding six months, must be reasoned and supported by evidence.

If no reply to the communication is received in due time, the European patent application will be deemed to be withdrawn (Art. 94(4) EPC).

Important information in case of a PACE request
If a PACE request has been validly filed for the application, the applicant is herewith informed that with the grant of the request for extension of time limit the application is removed from the PACE programme. A second PACE request for that application during the same stage of the procedure will not be processed (see OJ EPO 2015, A93, point 4).

For the Examining Division



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Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	10697703	
Application number	EP19188924.5	
Date of receipt	24 February 2022	
Filing Office	European Patent Office, The Hague	
Procedural phase	All procedures	
Your reference	M/KIE-150-EP/A1	
Documents submitted	package-data.xml epf1038.pdf (1 p.)	ep-sfd-request.xml
Submitted by	CN=secure.epoline.org	
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Letter accompanying subsequently filed items

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The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number:	EP19188924.5
Applicant's or representative's reference	M/KIE-150-EP/A1
Name of represented party	INTEL Corporation

Annotations

Extension of time request (Pamela Gellrich; 24.02.2022)
1. Remark (Annotate)
Dear Madam/Sir,

Further to the Communication pursuant to Art. 94(3) EPC dated October 14, 2021, we request an extension of two months in order to deal with the objections raised by the Examiner. The necessary information could not yet be obtained from our client. Accordingly, we request that this extension of time be granted.

Yours faithfully,

Signatures

Place:	**Munich**
Date:	**24 February 2022**
Signed by:	**/Andrew Parker/**
Representative name:	**Andrew Parker**
Capacity:	**Representative**
Function of person signing:	**Representative**

The examination is being carried out on the **following application documents**

Description, Pages

2-29	as originally filed	
1, 1a	filed in electronic form on	16-06-2020

Claims, Numbers

1-3	filed in electronic form on	06-11-2020

Drawings, Sheets

1/11-11/11	as originally filed

The following document is cited by the Examiner. A copy of the document is annexed to the communication and the numbering will be adhered to in the rest of the procedure.

D3 US 2007/187767 A1 (YASUTAKE NOBUAKI [JP]) 16 August 2007 (2007-08-16)

1 Articles 76, 123(2) and 84 EPC

1.1 Present claim 1 relates to an "integrated circuit structure"; however, a structure is defined as a mere arrangement between parts (in the present case "a semiconductor fin", etc.), whereas from the earlier application as filed it is evident that the elements constituting said structure are in a well precise electronic relation, i.e. they are parts of a FinFET transistor (see e.g. fig. 6). This is also evident from the definition of "gate", "source" and "drain" in the remaining subject-matter of present claim 1, and therefore the requirements of Art. 76 EPC are not met.

1.2 Present claim 1 refers to a "fin comprising silicon". There is no basis for this in the application as filed, contrary to Art. 123(2) EPC. Fig. 6 and para [44] mention "a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600", but there is no direct and unambiguous disclosure of a "fin comprising silicon"; according to para [33], "the source and drain region cavities 312/314 along with their respective tip areas 312A/314A are filled with in situ doped silicon or SiGe, thereby forming

source region 318 (along with epi-tip 3 18A) and drain region 320", but this embodiment actually refers to a planar device (cf. figs. 3A-3C). According to [46], which also refers to fig. 6, "the **bilayer structure of the epitaxial region 631 and cap layer 641** can be implemented, for instance, using an **in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641)**", emphasis added, and the fin structure should therefore be restricted to the above features in **bold**. These features are essential (Art. 84 EPC) in that they are inextricably linked to the graded buffer layer (cf. para [46]: "with an optional germanium and/or boron graded buffer between the two bilayers") defined for the fin structure of present claim 1.

1.3 As far as the germanium concentrations of the first source/drain region (cf. claim 1: "in excess of 50 atomic %") and germanium cap layer (cf. claim 1: "in excess of 95 atomic %") are concerned, the embodiment of fig. 6, the only one directly relating to a FinFET device, specific values are given by:

para [54], reading: "In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %"; however,

para [55] reads: "The device further includes a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and **a boron concentration in excess of 2E20 cm-3**. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. The device is one of a planar or FinFET transistor. In one such example case, the device further includes a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a **boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm-3**".

It is noted that the above represent two different embodiments. In any case, essential features (Art. 84 EPC, marked in **bold**) appear to be missing from present claim 1.

1.4 As far as the (cf. claim 1) "germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface" is concerned, it is noted that [45] reads:
"A cap layer 641 is deposited over the epitaxial regions 631. Note that the boron cap layer 641 may be provided in the recessed (tip) regions, but in other embodiments is just provided over the source/drain regions";
Thus, the application refers to the tip regions, i.e. the S/D extensions that are used to reduce short channel effects, SCE, see also para [19]: "source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE)", and (also [19]):
"selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions to form a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer in the source/drain and respective tip regions". It is however unclear to the skilled person (Art. 84 EPC) how this can be applied to the FinFET structure shown in fig. 6 of the earlier application.

Independently of the above unclarity, the applicant's arguments on page 2 of his letter of 06-11-2020 that "D1 does also not disclose that any boron doped germanium cap layers are provided in the alleged recessed source/drain interfaces of the source/drain regions", cannot be followed, because e.g. document D1 (see D1, fig. 5 and [40]) discloses filling "the source region cavity 310 [...] with a graded high-germanium content silicon-germanium stack 1400 [...] to form a source region 510 and the drain region cavity 320 [...] with a graded high-germanium content silicon-germanium stack 1400, also further described in FIG. 14, to form a drain region 520. The **extensions** have been filled with the graded high-germanium content silicon-germanium stack 1400 to form an **epitaxial source extension** 530 and an **epitaxial drain extension** 540", emphasis added.

1.5 As to the presence of titanium in claim 1, it is noted that para [39] reads:
"**contact plug** 329/331 , such as silver, nickel-platinum or nickel- aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes";

1.6 For these features, no other direct and unambiguous link could be established with the other embodiments/disclosures of the earlier/parent application as filed contrary to Art. 76 EPC.

2 Independently of the above, and for the sake of reasoning it is noted that D1 discloses:

2.1 An integrated circuit structure (see D1, para [01]), comprising:
a semiconductor fin (see D1, fig. 6) comprising silicon (see e.g. para [45]);
a gate electrode (item 810, fig. 8) over the fin;
a first source or drain region (items 1210, fig. 12) in the fin proximate a first side of the gate electrode, the first source or drain region comprising an epitaxial region (see fig. 5 and para 40]: "the source region cavity 310 has been filled with a graded high-germanium content silicon-germanium stack 1400, further described in FIG. 14, to form a source region 510 and the drain region cavity 320 has been filled with a graded high-germanium content silicon-germanium stack 1400, also further described in FIG. 14, to form a drain region 520. The extensions have been filled with the graded high-germanium content silicon-germanium stack 1400 to form an epitaxial source extension 530 and an epitaxial drain extension 540") and a recessed source or drain interface (cf. figs. 3, 5 and 11), wherein the epitaxial region is formed on the recessed source or drain interface and on one fin sidewall (see figs. 11 and 12), wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded (see [40], "graded high-germanium content silicon-germanium stack") ~~to a concentration in excess of 50 atomic %~~;
~~a first boron doped germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) of the first source or drain region, the first boron doped germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %~~;
a second source or drain region in the fin (see references for the "first source or drain region" above) proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising an epitaxial region and a recessed source or drain interface, wherein the epitaxial region is formed on the recessed source or drain interface and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded (see [40]) ~~to a concentration in excess of 50 atomic %~~; ~~and~~
~~a second boron doped germanide cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) of the second source or drain region, the second boron doped germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %.~~

2.2 The subject-matter of claim 1 differs from this known integrated circuit structure in that:
i) in the first source or drain region and in the second source or drain region the

germanium concentration is graded to a concentration in excess of 50 atomic %; and
ii) a first (respectively: a second) boron doped germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) of the first (respectively: the second) source or drain region, the first (respectively: the second) boron doped germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %.

2.3 The problem to be solved by the present invention (see also application as filed, [14]) may be regarded as reducing the contact resistance.

2.4 The solution proposed in claim 1 of the present application cannot be considered to involve an inventive step (Articles 52(1) and 56 EPC).

2.5 The technical problem underlying the present application is also present in document D1 (see e.g. D1, [24]: "use of a strained high germanium compound film including a graded transition layer in the source/drain (S/D) regions of a pMOS device can provide the combined effect of contact resistance reduction and mobility enhancement resulting from the strained configuration") and therefore it would certainly be faced by the skilled person starting from the closest prior art D1.

2.6 The skilled person would then turn to document D3, also dealing with the same technical problem, see e.g. D3, para [05], [06] and [24]) and would solve this problem by introducing a higher Ge content in the SiGe source/drain graded regions (see e.g. D3, para [90]: "rising to approximately 100 at %"). Subsequent Ti deposition to form a titanium germanide top layer is also envisaged by D3, see D3, [36], "Further, as a **metallic material of the metal film**, it is possible to use a high-melting point metal, **e.g.**, nickel (Ni), cobalt (Co), **titanium (Ti)**, iridium (Ir), platinum (Pt), or palladium (Pd). Thereafter, an unreacted metal film other than the silicide layer 112 and the germanide layer 113 is removed", emphasis added. See also D3, [50].

2.7 It is incidentally noted that the combination of documents D1 and D3 also discloses boron doping at very high concentrations (see e.g. D1, [39]: "germanium silicon alloy may be further doped in situ with boron. The boron concentration may range from 2×10<19>/cm<3 >to 7×10<20>/cm<3>"); see also D3, [95].

3 At least some of the objections raised above are such that there appears to be no possibility of overcoming them by amendment. Refusal of the application under Article 97(2) EPC is therefore to be expected.

4 Should the applicant, nevertheless, wish to file new claims, in order to comply with the requirements of Rule 137(4) EPC, the applicant should clearly identify - **based on the earlier/parent application as filed** - the amendments made, irrespective of whether they concern amendments by addition, replacement or deletion, and indicate the passages of the application as filed on which these amendments are based (see Guidelines H III, 2.1).

If the applicant considers it appropriate, these indications could be submitted in handwritten form on a copy of the relevant parts of the application as filed or in documents with tracked changes.

4.1 When filing amended claims the applicant should at the same time bring the description into conformity with the amended claims. Care should be taken during revision, especially of the introductory portion and of any statements of problem or advantage, not to add subject-matter which extends beyond the content of the application as originally filed (Article 123(2) EPC).

4.2 The description should be amended where appropriate to fulfil the following requirements:

- The technical field of the invention (Rule 42(1)(a) EPC; Guidelines F-II. 4.2) must correspond to the amended set of claims.
- Document D1-D3 should be cited by the description, Rule 42(1)(b) EPC.
- The summary of the invention (Rule 42(1)(c) EPC; Guidelines F-II.4.5) must correspond to the amended set of claims. Where appropriate, statements such as “The invention is set out in the appended set of claims“ or “The invention is as defined in claim X“ may be used instead of repeating the claims verbatim.
- Embodiments which are no longer covered by the claims must be deleted, unless they can reasonably be considered to be useful for highlighting specific aspects of the amended subject-matter. If this is the case, they must be clearly marked as not being part of the present invention (T 1808/06 and Guidelines F-IV, 4.3)
    - Any combinations of features which do not fall under the scope of the amended independent claims must be clearly marked as not being part of the present invention.
    - Statements such as “The following examples/aspects/embodiments X, Y, Z are not according to the invention and are present for illustration purposes only” may be used at the start of the description or in the list of figures.

- The technical features of the independent claims may not be presented as optional in the description. Where they precede a feature of an independent claim, terms such as “for example“, “may“, “can”, “exemplary“, “optionally“, “preferably“ and the like must be removed.
- “Claim-like” clauses must be deleted. Claim-like clauses are clauses present in the description (see present pages 26-29, "Further Exemplary Embodiments") which use claim language such as “according to the preceding clause“ or “characterised in that“ (Guidelines F-IV, 4.4). Claim-like clauses include examples, embodiments or aspects which are presented as claim-like clauses. The simple conversion of these clauses into separate optional features will not be admitted either.

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Meissner Bolte Patentanwälte
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Application No.	Ref.	Date
19 188 924.5 - 1212	J100788EPA	14.10.2021
Applicant: INTEL Corporation		

Communication pursuant to Article 94(3) EPC

The examination of the above-identified application has revealed that it does not meet the requirements of the European Patent Convention for the reasons enclosed herewith. If the deficiencies indicated are not rectified the application may be refused pursuant to Article 97(2) EPC.

You are invited to file your observations and insofar as the deficiencies are such as to be rectifiable, to correct the indicated deficiencies within a period

of 4 months

from the notification of this communication, this period being computed in accordance with Rules 126(2) and 131(2) and (4) EPC. One set of amendments to the description, claims and drawings is to be filed within the said period on separate sheets (R. 50(1) EPC).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

Failure to comply with this invitation in due time will result in the application being deemed to be withdrawn (Art. 94(4) EPC).

Registered letter
EPO Form 2001 11.16TRI

Nesso, Stefano
Primary Examiner
For the Examining Division

Enclosure(s): 7 page/s reasons (Form 2906)
US-20070187767-A1

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European Patent Office
80298 MUNICH
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Questions about this communication ?
Contact Customer Services at www.epo.org/contact

Parker, Andrew James
Meissner Bolte Patentanwälte
Rechtsanwälte Partnerschaft mbB
Widenmayerstraße 47
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ALLEMAGNE

Date
08.06.21

Reference	Application No./Patent No.
M/KIE-150-EP/A1	19188924.5 - 1212 / 3582265
Applicant/Proprietor	
INTEL Corporation	

Communication of amended entries concerning the representative (R. 143(1)(h) EPC)

As requested, for the above-mentioned European patent application / European patent the entries concerning the representative have been amended as follows:

Parker, Andrew James
Meissner Bolte Patentanwälte
Rechtsanwälte Partnerschaft mbB
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DE

The amendment will be recorded in the Register of European Patents.

Important note for EPO deposit account holders

If you would like to have fee refunds credited to a deposit account held with the EPO, you should ensure that you provide clear and up-to-date refund instructions to this effect, using one of the permitted electronic means of filing (see Arrangements for deposit accounts).

For the Examining Division

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Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	9853665	
Application number	EP19188924.5	
Date of receipt	01 June 2021	
Receiving Office	European Patent Office, The Hague	
Your reference	J100788EPA	
Applicant	All applicants as on file	
Documents submitted	package-data.xml epf1038.pdf (1 p.)	ep-sfd-request.xml CDAPPR-CHOR-1.pdf\J100788EPA et al Withdraw Representation Letter to EPO.pdf (1 p.)
Submitted by	CN=Felix Rummler 25782	
Method of submission	Online	
Date and time receipt generated	01 June 2021, 17:21 (CEST)	
Message Digest	7B:E6:28:1A:0B:95:25:7B:3C:F2:31:63:EE:D1:84:6E:81:BE:DA:AB	

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Letter accompanying subsequently filed items

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The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number	19188924.5
Applicant's or representative's reference	J100788EPA

	Description of document	Original file name	Assigned file name
1	Request for change of representative	J100788EPA et al Withdraw Representation Letter to EPO.pdf	CDAPPR-CHOR-1.pdf

	Payment	
1	Method of payment	Not specified

Signatures

Place:

Date: **01 June 2021**

Signed by: **Felix Rummler 25782**

Representative name: **Felix Rummler**

Capacity: **(Representative)**

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Please reply to: London office

Our Cases: J100788EPA, J100789EPA, J100797EPA,
J100790EPB;

31 May 2021

European Patent Office
D-80298 Munich
GERMANY

European Patent Application No. 19188924.5
European Patent Application No. 17193291.6
European Patent Application No. 19191370.6
European Patent Application No. 20177754.7
Intel Corporation

We resign from representation of the applicant for the applications listed above.

We understand that the new representative will be:

Meissner Bolte Patentanwälte Rechtsanwälte Partnerschaft mbB
Dr. Pier Luigi de Anna
Widenmayerstr. 47
80538 München

Please direct all further correspondence to the new representative.

Yours faithfully,

/Felix Rummler/
Authorised Representative
Maucher Jenkins

MEISSNER BOLTE

Meissner Bolte P.O. Box 860624 81633 München, Germany

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EPO - Munich
101
21. Mai 2021

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ANSPRECHPARTNER I CONTACT	IHR ZEICHEN I YOUR REF.	UNSER ZEICHEN I OUR REF.	DATUM I DATE
Dr. Andrew Parker		M/KIE-VARIA	May 17, 2021 PA/ef

European Patent Applications
Assuming Representation for Intel Corporation

Dear Madam/Sir,

We herewith assume representation of the following applications:

Application Number	Filing Date	Our Reference Number
19188924.5	September 30, 2011	M/KIE-150-EP/A1
17193291.6	September 30, 2011	M/KIE-151-EP/A1
13899890.1	December 19, 2013	M/KIE-152-PC/EP
14887192.4	March 27, 2014	M/KIE-153-PC/EP
19191370.6	December 7, 2011	M/KIE-154-EP/A1
20177754.7	December 20, 2011	M/KIE-155-EP/A1

MEISSNER BOLTE

Please direct all further correspondence regarding these cases to:

Meissner Bolte Patentanwälte Rechtsanwälte Partnerschaft mbB
Dr. Andrew Parker
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80538 München
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Yours faithfully,

Dr. Andrew Parker
European Patent Attorney

MB

Europäisches Patentamt
European Patent Office
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Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	9187069
Application number	EP19188924.5
Date of receipt	06 November 2020
Receiving Office	European Patent Office, The Hague
Your reference	J100788EPA
Applicant	All applicants as on file

Documents submitted	package-data.xml epf1038.pdf (1 p.) CLMS-1.pdf\P38507EP-D1 J100788EPA amended claims (clean).pdf (2 p.)	ep-sfd-request.xml EXRE3-1.pdf\P38507EP-D1 J100788EPA EPO ROA 94(3).pdf (3 p.) CLMS-HWA-1.pdf\P38507EP-D1 J100788EPA amended claims (marked).pdf (2 p.)

Submitted by	CN=Britta Fischer 64823
Method of submission	Online
Date and time receipt generated	06 November 2020, 09:04 (CET)
Message Digest	3E:71:74:E9:AE:4D:ED:3C:C7:3D:B4:66:A4:2E:1A:98:6C:A7:17:19

/European Patent Office/

Claims

1. An integrated circuit structure, comprising:

a semiconductor fin (660) comprising silicon;

a gate electrode (640) over the fin (660);

a first source or drain region in the fin (660) proximate a first side of the gate electrode (640), the first source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on one fin sidewall, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50 atomic %;

a first boron doped ~~germanide~~ germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) ~~over the top surface~~ and provided in the recessed source or drain interface (650)[1] of the first source or drain region, the first boron doped ~~germanide~~ germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %[2];

a second source or drain region in the fin (660) proximate a second side of the gate electrode (640) opposite the first side, the second source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50 atomic %; and

a second boron doped germanide cap layer (325; 327; 641) deposited on the epitaxial region (631) ~~over the top surface~~ and provided in the recessed source or drain interface (650)[3] of the second source or drain region, the second boron doped ~~germanide~~ germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %[4].

[1] See paragraphs 45-46 as originally filed
[2] Page 22, penultimate sentence, as originally filed
[3] See paragraphs 45-46 as originally filed
[4] Page 22, penultimate sentence, as originally filed

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20 cm^{-3}.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20 cm^{-3}.

Claims

1. An integrated circuit structure, comprising:

a semiconductor fin (660) comprising silicon;

a gate electrode (640) over the fin (660);

a first source or drain region in the fin (660) proximate a first side of the gate electrode (640), the first source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on one fin sidewall, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50 atomic %;

a first boron doped germanium cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) of the first source or drain region, the first boron doped germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %;

a second source or drain region in the fin (660) proximate a second side of the gate electrode (640) opposite the first side, the second source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50 atomic %; and

a second boron doped germanide cap layer (325; 327; 641) deposited on the epitaxial region (631) and provided in the recessed source or drain interface (650) of the second source or drain region, the second boron doped germanium cap layer comprising germanium and titanium and having a germanium concentration in excess of 95 atomic %.

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20 cm^{-3}.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20 cm^{-3}.

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Letter accompanying subsequently filed items

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The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number	19188924.5
Applicant's or representative's reference	J100788EPA

	Description of document	Original file name	Assigned file name
1	Reply to examination report	P38507EP-D1 J100788EPA EPO ROA 94(3).pdf	EXRE3-1.pdf
2	Amended claims (clean copy)	P38507EP-D1 J100788EPA amended claims (clean).pdf	CLMS-1.pdf
3	Amended claims with annotations	P38507EP-D1 J100788EPA amended claims (marked).pdf	CLMS-HWA-1.pdf

	Payment	
1	Method of payment	Not specified

Signatures

Place:	**Munich**
Date:	**06 November 2020**
Signed by:	**Britta Fischer 64823**
Representative name:	**Britta Fischer**
Capacity:	**(Representative)**

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Our Case: J100788EPA

Please reply to: London office

5 November 2020

European Patent Office
D-80298 Munich
GERMANY

European Patent Application No. 19188924.5
Intel Corporation
Contact Resistance Reduction Employing Germanium Overlayer Pre-Contact Metalization

We refer to the official communication dated 14 July 2020 and file herewith a new set of claims to replace the claims currently on file. To assist the Examiner in understanding our amendments, we also enclose an annotated copy of the previous claims showing our amendments underlined and struck through.

Any subject-matter removed by the amendments is not to be regarded as irrevocably abandoned. The removal of any subject-matter is without prejudice to later reinstatement or dividing out of that subject-matter.

Amendments
The claims have been amended to overcome the objections raised in sections 1 and 2 of the above-identified communication. A clear basis for the amendments is indicated in the footnotes of the enclosed annotated claims. All amendments are considered to be self-explanatory from the annotated set of claims.

Article 76(1) EPC
Following items 1.1-1.3 of the above-identified communication the feature of the boron doped germanium layer "*having a germanium concentration in excess of 95 atomic %*" has been introduced into claim 1 based on originally filed description page 22, penultimate sentence.

Inventive step
The last paragraph on page 2 of the communication states

> *"Concerning point 3), figures 11 and 12 of D1 clearly show the removal of a portion of body 620 (see D1, fig. 11; of course this applies to both sides, source and drain) and subsequent formation of epitaxial source/drain regions (see fig. 12, item 1210) on both sides of the gate,*

i.e. on the recessed source or drain interface and on one/on the opposing fin sidewall, as defined by present claim 1."

Referring to Figure 11 of D1 reproduced below, it is assumed that the arrow/line associated with reference sign 1110 points to the alleged recessed source or drain interface of D1.

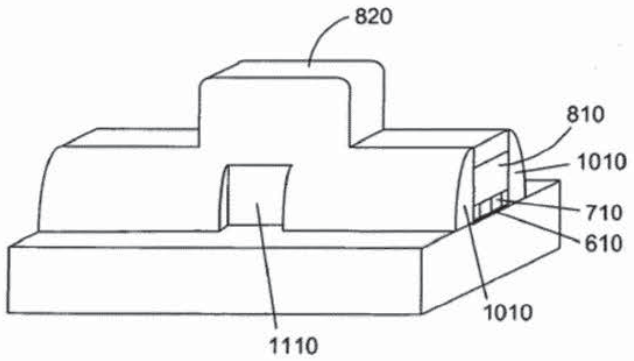


FIG. 11

Amended claim 1 now specifies (emphasis added)

a first boron doped germanium cap layer deposited on the epitaxial region and provided in the recessed source or drain interface of the first source or drain region; and
a second boron doped germanium cap layer deposited on the epitaxial region and provided in the recessed source or drain interface of the second source or drain region.

See Figure 6 and para. 44-46 of the present application for the corresponding embodiment.

D1 does not disclose any boron doped germanium cap layers deposited on the epitaxially formed source/drain regions 1210 (cf. Figure 12 of D1). This is not in dispute (cf. items 3.2-3.3 of the European search opinion and item 2.3 of the above-identified communication).

Consequently D1 does also not disclose that any boron doped germanium cap layers are provided in the alleged recessed source/drain interfaces of the source/drain regions, i.e. in the recess towards which the arrow associated with reference sign 1110 in Figure 11 points. Reference sign 1110 denotes a multi-channel gate region.

In D1 in the next manufacturing step the recess, i.e., the multi-channel gate-regions 1110, shown in Figure 11 is entirely covered by the epitaxially formed source/drain regions 1210, see reproduced Figure 12 below. I.e., the epitaxially formed source/drain regions 1210 are formed on the multi-gate channel regions 1110 (cf. para. 51 of D1). If follows that the recess shown in Figure 11 does not and cannot constitute an interface for contacting the source/drain regions 1210 within an integrated circuit structure.

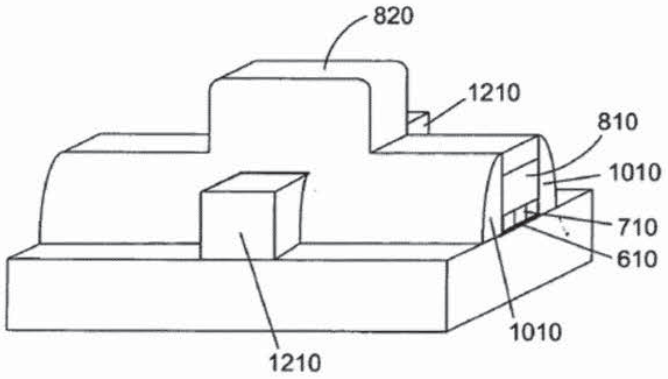


FIG. 12

Thus, even if the skilled person would apply the teaching of D2 to the embodiment shown in Figure 12 of D1, the skilled person would not arrive at the claimed solution. In the Applicant's opinion it makes technically no sense to provide a "*self-aligned germanosilicide or silicide formation*" (as disclosed in D2) between the source/drain regions 1210 and the multi-gate channel region 1110 of D1.

The subject-matter of amended claim 1 is therefore inventive with respect to the cited prior art.

For the sake of completeness it is noted that the problem-solution-approach applied in Applicant's letter of 16 June 2020 similarly applies with respect to claim 1 as presently amended.

Conclusion
All the objections raised by the Examiner have been addressed, and this application should now be in condition for grant.

We request Oral Proceedings – to be held by videoconference – in the event that the Examining Division intends to refuse the application. It is stressed, however, that the request for Oral Proceedings is not a desired option and the Applicant would prefer to continue proceedings in writing.

Yours faithfully

/Dr. Britta Fischer/
Authorised Representative
Maucher Jenkins

The examination is being carried out on the **following application documents**

Description, Pages

2-29	as originally filed	
1, 1a	filed in electronic form on	16-06-2020

Claims, Numbers

1-3	filed in electronic form on	16-06-2020

Drawings, Sheets

1/11-11/11	as originally filed

1 Article 76(1) EPC

1.1 Concerning the objection under Art. 76(1) EPC raised in the official communication (ESOP) dated 23-10-2019, § 1.4, in his letter dated 16-06-2020, on page 2, the applicant mentions that para [54] of the parent application as filed provides a basis for the divisional application. However, the passage cited by the applicant, on page 22 reads (in its entirety):
"In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic % **and the boron doped germanium layer** has a germanium concentration in excess of 95 atomic %" (emphasis added).

1.2 It is noted that the application (see e.g. parent, para [15], last sentence) discloses as essential the presence of boron (cf. "boron doped germanium layer") in order to "significantly reduce the band misalignment and contact resistance".

1.3 Therefore, the feature of the of the boron doped germanium layer - missing in present claim 1 - extends the divisional application beyond the content of the parent application as filed, contrary to Art. 76(1) EPC.

2 Inventive step

2.1 The objections as to the lack of inventive step (Art. 56 EPC) already raised in the previous communication dated 23-10-2019, § 3.1, are maintained and can be applied to the subject-matter of present claim 1, mutatis mutandis.

2.2 In his letter of 16-06-2020, the applicant argues that:
1) "Contrary to item 3.3 of the Opinion, D1 does deal with the provision at electrical interconnections (cf. par. 43, Figure 5). Paragraph 43 of D1 gives a concrete example: For instance, after the epitaxial deposition of the source/ drain regions and the source/drain extension, an interlayer dielectric (ILD) may be deposited and planarized over the device [...] FIG. 5 illustrates an /LD layer 550 that has been deposited over the planar MOS device 100"; that
2) "the provision of such a dielectric layer teaches away from providing a germanide layer as defined in claim 1. Paragraph 43 would not incite a skilled person to revert to the teaching of D2"; and moreover
3) "D1 does not disclose that the first and second S/D regions comprise 'an epitaxial region and a recessed source or drain interface, wherein the epitaxial region is formed on the recessed source or drain interface and on one/on the opposing fin sidewall' as defined in new claim 1".

2.3 Concerning point 1) supra, D1 merely explains what kind of ILD could be used, without giving details as to the metal interconnection to the transistor device, which is instead proposed by document D2;
The arguments of point 2) are not followed: claim 1 defines the germanide layer as formed "over the top surface of the first [respectively second] source or drain region, the first germanide layer comprising germanium and titanium"; document D1 mentions (cf. para [43]) that "after the epitaxial deposition of the source/drain regions and the source/drain extension, an interlayer dielectric (ILD) may be deposited and planarized over the device"; it is noted that for the finFET transistor, the epitaxial source/drain regions correspond to items 1210 in fig. 12 (see also D1, para [51]). As to D2 (see page 312, EXPERIMENTAL, third sentence from below), it discloses: "Self-aligned germanosilicide or silicide formation was then performed on the device wafers followed by low temperature oxide deposition and contact hole formation" and therefore no teaching would be reverted;
Concerning point 3), figures 11 and 12 of D1 clearly show the removal of a portion of body 620 (see D1, fig. 11; of course this applies to both sides, source and drain) and subsequent formation of epitaxial source/drain regions (see fig. 12, item 1210) on both sides of the gate, i.e. on the recessed source or drain interface and on one/on the opposing fin sidewall, as defined by present claim 1.

2.4 The subject-matter of present claim 1 is therefore not regarded as inventive (Art. 56 EPC).

3 Dependent claims 2 and 3 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, meet the requirements of the EPC with respect to inventive step, see ESOP, § 4 and sub-paragraphs, mutatis mutandis.

4 At least some of the objections raised above are such that there appears to be no possibility of overcoming them by amendment. Refusal of the application under Article 97(2) EPC is therefore to be expected.

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Application No.	Ref.	Date
19 188 924.5 - 1212	J100788EPA	14.07.2020
Applicant: INTEL Corporation		

Communication pursuant to Article 94(3) EPC

The examination of the above-identified application has revealed that it does not meet the requirements of the European Patent Convention for the reasons enclosed herewith. If the deficiencies indicated are not rectified the application may be refused pursuant to Article 97(2) EPC.

You are invited to file your observations and insofar as the deficiencies are such as to be rectifiable, to correct the indicated deficiencies within a period

of 4 months

from the notification of this communication, this period being computed in accordance with Rules 126(2) and 131(2) and (4) EPC. One set of amendments to the description, claims and drawings is to be filed within the said period on separate sheets (R. 50(1) EPC).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

In case you withdraw the application within the above-mentioned period, the examination fee will be refunded at a rate of 50% (Art. 11 (b) RFees).

Failure to comply with this invitation in due time will result in the application being deemed to be withdrawn (Art. 94(4) EPC).

Registered letter
EPO Form 2001 11.16TRI

Nesso, Stefano
Primary Examiner
For the Examining Division

Enclosure(s): 3 page/s reasons (Form 2906)

Application No.: 19188924.5

Substantive examination has started on 06.07.20 (see Notice from the European Patent Office dated 29.01.2013, OJ EPO 2013, 153).

For the Examining Division

Europäisches Patentamt
European Patent Office
Office européen des brevets

Acknowledgement of receipt

We hereby acknowledge receipt of the following subsequently filed document(s):

Submission number	8730092
Application number	EP19188924.5
Date of receipt	16 June 2020
Receiving Office	European Patent Office, The Hague
Your reference	J100788EPA
Applicant	All applicants as on file

Documents submitted		
	package-data.xml	ep-sfd-request.xml
	epf1038.pdf (2 p.)	TIMEEXTREQ-1.pdf\J100788EPA P38507EP-D1 ROA RULE 69 - EPO.pdf (3 p.)
	CLMS-1.pdf\J100788EPA P38507EP-D1 amended claims (clean).pdf (1 p.)	CLMS-HWA-1.pdf\J100788EPA P38507EP-D1 amended claims (annotated).pdf (1 p.)
	DESC-1.pdf\J100788EPA P38507EP-D1 amended description (clean).pdf (2 p.)	DESC-HWA-1.pdf\J100788EPA P38507EP-D1 amended description (annotated).pdf (2 p.)

Submitted by	CN=Felix Rummler 25782
Method of submission	Online
Date and time receipt generated	16 June 2020, 16:11 (CEST)
Message Digest	90:7E:F7:79:16:D4:9C:86:7D:7E:32:BF:B7:BC:58:DB:E9:32:08:FE

Correction by the EPO of errors in debit instructions filed by eOLF
Errors in debit instructions filed by eOLF that are caused by the editing of Form 1038E entries or the continued use of outdated

software (all forms) may be corrected automatically by the EPO, leaving the payment date unchanged (see decision T 152/82, OJ EPO 1984, 301 and point 6.3 ff ADA, Supplement to OJ EPO 10/2007).

/European Patent Office/

Claims

1. An integrated circuit structure, comprising:

a semiconductor fin (660) comprising silicon;

a gate electrode (640) over the fin (660);

a first source or drain region in the fin (660) proximate a first side of the gate electrode (640), the first source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on one fin sidewall, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer (325; 327) over the top surface of the first source or drain region, the first germanide layer comprising germanium and titanium;

a second source or drain region in the fin (660) proximate a second side of the gate electrode (640) opposite the first side, the second source or drain region comprising an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer (325; 327) over the top surface of the second source or drain region, the second germanide layer comprising germanium and titanium.

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

Claims

1. An integrated circuit structure, comprising:

a semiconductor fin (660) comprising silicon;

a gate electrode (640) over the fin (660);

a first source or drain region in the fin (660) proximate a first side of the gate electrode (640), the first source or drain region comprising ~~two or more facets and a top surface~~an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on one fin sidewall, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer (325; 327) over the top surface of the first source or drain region, the first germanide layer comprising ~~silicon,~~ germanium and titanium;

a second source or drain region in the fin (660) proximate a second side of the gate electrode (640) opposite the first side, the second source or drain region comprising ~~two or more facets and a top surface~~an epitaxial region (631) and a recessed source or drain interface (650), wherein the epitaxial region (631) is formed on the recessed source or drain interface (650) and on the opposing fin sidewall, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer (325; 327) over the top surface of the second source or drain region, the second germanide layer comprising ~~silicon,~~ germanium and titanium.

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

RELATED APPLICATION

[0001] This application is a continuation-in-part of U.S. Application No. 12/975,278 filed December 21, 2010.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

US 2010/148217 A1 describes an apparatus and methods for providing a graded high germanium compound region for strained semiconductor devices.

"Self-Aligned Formation of C54 Titanium Germanosilicide Using Rapid Thermal Processing and Application to Raised, Ultrashallow Junctions" by Stanton P. Ashburn et al., Materials Research Society Symposium Proceedings, US, (19930101), vol. 320, doi:10.1557/PROC-320-311, ISSN 0272-9172, pages 311 - 316, XP055631293, presents results on solid state reactions between Ti and $Si_{1-x}Ge_x$ alloys selectively deposited onto Si (100) substrates using rapid thermal annealing for contact applications. As the Ge concentration within the reacting alloy decreases the lateral grain size for the C54 structures increases. A self-aligned germanosilicide process is identified and used to fabricate raised, ultrashallow junctions with $Ti(SiGe)_2$ (germanosilicide) contacts. Forward and reverse bias characterization of the junctions indicate that leakage current induced during silicidation can be eliminated using raised junctions with germanosilicide contacts.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

RELATED APPLICATION

[0001] This application is a continuation-in-part of U.S. Application No. 12/975,278 filed December 21, 2010.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

US 2010/148217 A1 describes an apparatus and methods for providing a graded high germanium compound region for strained semiconductor devices.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

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Our Case: J100788EPA

Please reply to: London office

16 June 2020

European Patent Office
D-80298 Munich
GERMANY

Dear Sirs,

European Patent Application No. 19188924.5
Intel Corporation
Contact Resistance Reduction Employing Germanium Overlayer Pre-Contact Metalization

We refer to the official communication pursuant to Rule 69 EPC dated 2 January 2020.

We hereby request examination. The examination and designation fees are paid together with this letter.

Referring to the opinion accompanying the European search report ("Opinion"), we file herewith a new set of claims and new description pages 1-1a which are to replace the corresponding pages of this application currently on file. To assist the Examiner in understanding our amendments, we also enclose an annotated copy of the corresponding previous pages showing our amendments underlined and struck through.

Any subject-matter removed by the amendments is not to be regarded as irrevocably abandoned. The removal of any subject-matter is without prejudice to later reinstatement or dividing out of that subject-matter.

Amendments

New claim 1 corresponds to previous claim 1 with the following amendments:

- The feature "a fin comprising silicon" has been replaced by "a semiconductor fin comprising silicon" supported by paragraph 44, 2nd sentence, on page 18 of the parent application EP 11 852 027.9.
- In the paragraph starting with "a first source or drain region..." the expression "two or more facets and a top surface" has been replaced by the expression "an epitaxial region and a recessed source or drain interface, wherein the epitaxial region is formed on the recessed source or drain interface and on one fin sidewall" disclosed in paragraph 45, 1st sentence, on page 18 of the parent application EP 11 852 027.9. The paragraph starting with "a second source or drain region..." has been correspondingly amended.

- In the antepenultimate and the last paragraphs the term "silicon" has been removed. Please see, e.g., paragraph 40, ll. 7-16, on page 16 of the parent application EP 11 852 027.9.

New claims 2 and 3 correspond to previous claims 2 and 3.

Reference numerals have been inserted in the claims.

The independent claims have not been drafted in the two-part form because it is believed that this would result in unnecessarily involved claims. However, prior art document D1 and D2 have been identified in the background section of the description.

Article 76(1) EPC
Following item 1.2 of the Opinion the Applicant has replaced the expression "a fin comprising silicon" in claim 1 by the expression "a semiconductor fin comprising silicon" supported by paragraph 44, 2nd sentence, on page 18 of the parent application EP 11 852 027.9.

Following item 1.3 of the Opinion the Applicant has replaced the expression "two or more facets and a top surface" in claim 1 in the paragraphs relating to the first and second S/D regions by "an epitaxial region and a recessed source or drain interface, wherein the epitaxial region is formed on the recessed source or drain interface and on one fin sidewall" and "an epitaxial region and a recessed source or drain interface, wherein the epitaxial region is formed on the recessed source or drain interface and on the opposing fin sidewall", respectively. This amendment is disclosed in paragraph 45, 1st sentence, on page 18 of the parent application EP 11 852 027.9.

Regarding item 1.4 of the Opinion the Applicant refers to paragraph 54, penultimate sentence, on page 22 (ll. 26-30) of the parent application EP 11 852 027.9 literally stating: "In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %,...". See also page 24, ll. 2-4, (paragraph 55) of the parent application EP 11 852 027.9.

Hence, the feature according to which the first and second S/D regions comprise "silicon and germanium having a germanium concentration graded to a concentration in excess of 50%" is disclosed in the parent application. The Applicant respectfully notes that he did not find the passage cited in item 1.4 of the Opinion in the application documents of the parent application EP 11 852 027.9.

Clarity
Following item 2.2 of the Opinion the term "silicon" has been removed from the antepenultimate and the last paragraphs of claim 1. It is now clear that the germanide layer is a binary compound comprising germanium and titanium.

Inventive step
In item 3.2 of the Opinion the following distinguishing features were already been identified with respect to D1 (US 2010/148217 A1):

- "*a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising germanium and titanium*", and
- "*a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising germanium and titanium*".

Contrary to item 3.3 of the Opinion, D1 does deal with the provision at electrical interconnections (cf. par. 43, Figure 5). Paragraph 43 of D1 gives a concrete example:

> "*For instance, after the epitaxial deposition of the source/drain regions and the source/drain extension, an interlayer dielectric (ILD) may be deposited and planarized over the device. The ILD may be formed using materials known for the applicability in dielectric layers for integrated circuit structures, such as low-k dielectric materials. Such dielectric materials include, but are not limited to, oxides such as silicon dioxide (SiO2) and carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The dielectric layer may include pores or other voids to further reduce its dielectric constant. FIG. 5 illustrates an ILD layer 550 that has been deposited over the planar MOS device 100.*"

However, the provision of such a dielectric layer teaches away from providing a germanide layer as defined in claim 1. Paragraph 43 would not incite a skilled person to revert to the teaching of D2.

Apart from that, D1 does not disclose that the first and second S/D regions comprise "*an epitaxial region and a recessed source or drain interface, wherein the epitaxial region is formed on the recessed source or drain interface and on one/on the opposing fin sidewall*" as defined in new claim 1. Following Figure 12 and paragraph 51 of D1 there are no recessed source or drain interfaces provided on which the epitaxial regions are formed.

This distinguishing feature has the technical effect of even further reducing contact resistance, which is already reduced by the provision of the germanide layers.

Thus, starting from D1 and bearing in mind the above-identified distinguishing features the skilled person faces the objective technical problem of providing an integrated circuit structure with much lower contact resistance.

Neither D1 nor D2 disclose or suggest S/D regions with recessed S/D interfaces with epitaxial regions being formed on the recessed S/D interfaces and on fin sidewalls. Neither D1 nor D2 give any other hint towards the claimed solution.

The subject-matter of new claim 1 is thus inventive with respect to the cited prior art.

Conclusion

All the objections raised by the Examiner have been addressed, and this application should now be in condition for grant.

We request Oral Proceedings – to be held by videoconference – in the event that the Examining Division intends to refuse the application. It is stressed, however, that the request for Oral Proceedings is not a desired option and the Applicant would prefer to continue proceedings in writing.

Yours faithfully

/Felix Rummler/
Authorised Representative
Maucher Jenkins

Europäisches Patentamt
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Office européen des brevets

Letter accompanying subsequently filed items

Representative:

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The document(s) listed below is (are) subsequently filed documents pertaining to the following application:

Application number	19188924.5
Applicant's or representative's reference	J100788EPA

	Description of document	Original file name	Assigned file name
1	Request for extension of time limit during search procedure	J100788EPA P38507EP-D1 ROA RULE 69 - EPO.pdf	TIMEEXTREQ-1.pdf
2	Amended claims (clean copy)	J100788EPA P38507EP-D1 amended claims (clean).pdf	CLMS-1.pdf
3	Amended claims with annotations	J100788EPA P38507EP-D1 amended claims (annotated).pdf	CLMS-HWA-1.pdf
4	Amended description (clean copy)	J100788EPA P38507EP-D1 amended description (clean).pdf	DESC-1.pdf
5	Amended description with annotations	J100788EPA P38507EP-D1 amended description (annotated).pdf	DESC-HWA-1.pdf

	Fees	Factor applied	Fee schedule	Amount to be paid
15-1	005e Designation fee - For all contracting States designated for applications filed on/after 01.04.2009	1	610.00	610.00
15-2	006 Examination fee - For applications filed on/after 01.07.2005	1	1 700.00	1 700.00
	Total:		**EUR**	**2 310.00**

	Payment	
1	Method of payment	Debit from deposit account
	Currency:	EUR
	The European Patent Office is hereby authorised, to debit from the deposit account with the EPO any fees and costs indicated on the fees page.	
	Deposit account number:	28050072
	Account holder:	Maucher Jenkins
2	Refund/Reimburserment	

	Reimbursement (if any) to be made to EPO deposit account:	28050072
	Account holder:	Maucher Jenkins

Signatures

Place:	
Date:	**16 June 2020**
Signed by:	**Felix Rummler 25782**
Representative name:	**Felix Rummler**
Capacity:	**(Representative)**

Europäisches Patentamt
European Patent Office
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Questions about this communication ?
Contact Customer Services at www.epo.org/contact

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Date
02.01.20

Reference	Application No./Patent No.
J100788EPA	19188924.5 - 1212 / 3582265
Applicant/Proprietor	
INTEL Corporation	

Communication pursuant to Rule 69 EPC - reminder concerning payment of the designation fee (Art. 79(2) EPC) and of the examination fee (Art. 94(1) EPC) - and invitation pursuant to Rule 70a(1) EPC

The date on which the European Patent Bulletin mentions the publication of the European search report for the above-mentioned European patent application is: 18.12.19.

Your attention is drawn to Article 79(2) and Rule 39(1) EPC as well as Article 94(1), Rule 70(1) and Rule 70a(1) EPC, according to which within **six months** of the above-mentioned publication date of the search report

- the designation fee must be paid,
- the request for examination must be filed and the examination fee must be paid,
- comments on the objections raised in the opinion accompanying the European search report and/or any amendments to the description, claims and drawings correcting any deficiencies noted in the opinion must be filed (R. 70a(1), 137(2) EPC; Guidelines for Examination in the EPO, B-XI, 8).

1. Payment of the designation fee and of the examination fee

The current amount of the flat-rate designation fee is: EUR 585,00

The current amount of the examination fee is: EUR 1635,00

If the written request for examination is filed in an admissible non-EPO language in accordance with Article 14(4) EPC, a reduction of the examination fee according to Rule 6(3) EPC applies.

For European patent applications filed on or after 01.04.2014, the reduction applies only if the applicant(s) has (have) declared to be an entity or a natural person within the meaning of Rule 6(4) EPC (Decision of the Administrative Council of 13 December 2013, OJ EPO 2014, A4).

If the designation fee and the examination fee are not paid within the period laid down in Rule 39(1) and Rule 70(1) EPC, the application **will be deemed to be withdrawn** (R. 39(2) and Art. 94(2) EPC).

Any extension or validation fees are also payable within the above-mentioned period.

Registered letter
EPO Form 1081 12.17 (NFS/RTB/ESOP01=N)

2. Comments on the opinion accompanying the European search report and filing of amendments

Should the reply to the invitation pursuant to Rule 70a(1) EPC be filed in an admissible non-EPO language, a translation is to be submitted within one month of its filing (R. 6(2) EPC).

If filing amendments, you must identify them and indicate the basis for them in the application as filed. Failure to meet either requirement may lead to a communication from the Examining Division requesting that you correct this deficiency (R. 137(4) EPC).

Should you not comply with this invitation within the time limit, the application **will be deemed to be withdrawn** in accordance with Rule 70a(3) EPC.

Making payments
For payments made via deposit account, please note that as from 1 December 2017 debit orders will only be carried out if filed in an electronically processable format (xml), using an accepted means of filing as laid down in the Arrangements for deposit accounts (ADA), published in the Supplementary publication in the Official Journal.

All relevant information related to the modes of payment of fees to the EPO can be retrieved from the EPO website at "**Making Payments**".

Information concerning fee amounts
Procedural fees are usually adjusted every two years, on even years, with effect from 1 April. Therefore, before making a payment, parties should verify the amounts actually due on the date of payment using the applicable version of the Schedule of fees and expenses, published as a Supplement to the Official Journal of the EPO, available on the EPO website (**www.epo.org**) at **www.epo.org/schedule-of-fees**. The "Schedule of fees" table allows the viewing, downloading and searching of individual fee amounts, both current and previous.

Receiving Section



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Questions about this communication ?
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Date
20.11.19

Reference	Application No./Patent No.
J100788EPA	19188924.5 - 1212 / 3582265
Applicant/Proprietor	
INTEL Corporation	

Notification of European publication number and information on the application of Article 67(3) EPC

You are hereby informed that the technical preparations for the publication of the above-mentioned European patent application have been completed.

The application will be published on 18.12.19 with the European search report.
The publication number is: 3582265.
The publication will be mentioned in European Patent Bulletin number 2019/51.
(**http://bulletin.european-patent-office.org**).

Provisional protection under Article 67(1) and (2) EPC in the individual contracting states becomes effective when the conditions referred to in Article 67(3) EPC have been fulfilled. Provisional protection in the individual extension and validation states is governed by the national laws of the countries concerned. For more details, see Chapter III of the EPO brochure "National Law relating to the EPC" (**www.epo.org/law-practice/legal-texts/national-law.html**), which also contains information about the extension and validation system. Further information can also be found in the Official Journal of the European Patent Office.

The title of the invention in the three official languages of the European Patent Office is worded as follows:

KONTAKTWIDERSTANDSREDUKTION MIT GERMANIUM-ÜBERSCHICHT-VORKONTAKT-METALLISIERUNG
CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
RÉDUCTION DE LA RÉSISTANCE DE CONTACT EMPLOYANT UNE MÉTALLISATION DE PRÉ-CONTACT DE SURCOUCHE DE GERMANIUM

In all future communications to the EPO, please quote the application number as indicated above, i.e. including the final four figures (which identify the Directorate responsible for the subsequent procedure).

Remark
The publication can be downloaded, free of charge, from the EPO publication server **https://data.epo.org/publication-server/** or can be ordered from the Vienna sub-office upon payment of a fee (see Decision of the President of the EPO dated 12 July 2007 concerning the form of publication of European patent applications, European search reports and European patent specifications, Special edition No. 3, OJ EPO 2007, 97).

Note concerning renewal fees
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Date
06.11.19

Reference	Application No./Patent No.
J100788EPA	19188924.5 - 1212
Applicant/Proprietor	
INTEL Corporation	

Refund of fees

The following fee has been paid in respect of application No. 19188924.5:

Fee	Reference	Voucher No.	Date	Currency	Amount
Search fee	002	01062216	29.07.19	EUR	1 300,00

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Communication

The extended European search report is enclosed.

The extended European search report includes, pursuant to Rule 62 EPC, the European search report (R. 61 EPC) or the partial European search report/ declaration of no search (R. 63 EPC) and the European search opinion.

Copies of documents cited in the European search report are attached.

☑ 0 additional set(s) of copies of such documents is (are) enclosed as well.

The following have been approved:

☑ Abstract ☑ Title

☐ The Abstract was modified and the definitive text is attached to this communication.

The following figure(s) will be published together with the abstract: 5F

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Should you wish to further prosecute this application in the examination phase, your attention is drawn to the provisions of Rule 70a EPC. An invitation to respond to the extended European search report will be issued once the date of publication of the European search report has been mentioned in the European Patent Bulletin (R. 69(1), R. 70(2) EPC).

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The examination is being carried out on the **following application documents**

Description, Pages

1-29 as originally filed

Claims, Numbers

1-3 as originally filed

Drawings, Sheets

1/11-11/11 as originally filed

Reference is made to the following documents; the numbering will be adhered to in the rest of the procedure.

D1 US 2010/148217 A1 (SIMONELLI DANIELLE [US] ET AL) 17 June 2010 (2010-06-17)

D2 STANTON P. ASHBURN ET AL: "SELF-ALIGNED FORMATION OF C54 TITANIUM GERMANOSILICIDE USING RAPID THERMAL PROCESSING AND APPLICATION TO RAISED, ULTRASHALLOW JUNCTIONS", MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, vol. 320, 1 January 1993 (1993-01-01), pages 311-316, XP055631293, US
ISSN: 0272-9172, DOI: 10.1557/PROC-320-311

1 Article 76(1) EPC

1.1 Even though the present application has been filed as a divisional application in the sense of Article 76 EPC of the earlier European patent applications

Nos. 11 852 027, 17 193 291 and 11 850 136,

the present application contains subject-matter that extends beyond the content of the earlier applications filed, and therefore the requirements of Art. 76(1) EPC are not met, for the reasons shown below.

1.2 According to present claim 1, the integrated circuit structure comprises "a fin comprising silicon";
however, e.g. EP11 852 027 (see fig. 6 and [44]) actually refers to "tri-gate device includ[ing] a substrate 600 having a **semiconductor** body or fin 660", emphasis added.

1.3 According to claim 1, the first and the second S/D regions comprise "two or more facets and a top surface";
There is no basis in the parent application either for the "two or more facets" or for "a top surface".

1.4 According to claim 1, the first and the second S/D regions comprise "silicon and germanium having a germanium concentration graded to a concentration in excess of 50%";
Basis seems to be page 23, lines 10-13 of parent application EP11 852 027; however, said passage is inextricably linked to other features, because the complete sentence reads:
" In another example case, the p-type and n-type source drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between at least one of the p-type and n-type source drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the at least one of the p-type and n-type source/drain regions to a high concentration in excess of 1E20 cm^{-3}";

By leaving out some of the above technical features, the inevitable intermediate generalisation offends against Art. 76(1) EPC.

2 Article 84 EPC

2.1 The application does not meet the requirements of Article 84 EPC, because claim 1 is not clear.

2.2 The term a "germanide comprising silicon, germanium and titanium" used twice in claim 1 (for the first and the second "source/drain regions) is unclear in that, while on the one hand a germanide is defined as a binary compound, i.e. as a compound containing Ge and another component, typically a metal, on the other hand the claim defines the germanium as comprising "silicon germanium and titanium", thus leaving the reader in doubt as to the meaning of the technical feature to which it refers, thereby rendering the definition of the subject-matter of said claim unclear (Article 84 EPC).

3 For the sake of reasoning - and independently of the above objections - the subject-matter of claim 1 has been examined.

3.1 Document D1 is considered to be the prior art closest to the subject-matter of claim 1 and discloses:
An integrated circuit structure (see para [01], "semiconductor integrated circuit manufacturing"), comprising:
a fin comprising silicon (see fig. 6 and para [45], "multi-gate body 620 may comprise silicon");
a gate electrode (item 810, fig. 8, "multi-gate electrode") over the fin;
a first source or drain region (fig. 12, "source/drain regions 1210"**)** in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets (sides of the fin) and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded (see para [53]: "strained semiconductor device comprising a graded high-germanium content") to a concentration in excess of 50% (see figs. 14, 15 and para [58], indicating a range from 40% to 55%);
a second source or drain region (fig. 12, "source/drain regions 1210"**)** in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets (sides of the fin) and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded (see para [53]: "strained semiconductor device comprising a graded high-germanium content") to a concentration in excess of 50% (see figs. 14, 15 and para [58], indicating a range from 40% to 55%).

3.2 The subject-matter of claim 1 therefore differs from this known integrated circuit structure in that it also comprises:
a first/second germanide layer over the top surface of the first/second source or drain region, the germanide layer comprising silicon, germanium and titanium;

3.3 Even if document D1 deals with semiconductor integrated circuit manufacturing, see e.g. para [01], this document D1 does not indicate any specific way of contacting the source/drain regions and connecting the disclosed device within an integrated circuit structure.

3.4 Document D2 (see abstract) presents results of reactions between Ti and SiGe for contact applications. Therefore, would apply the teaching of D2 to the method known from D1, thus falling within the terms of present claim 1.

3.5 The subject-matter of claim 1 is therefore not inventive (Art. 56 EPC).

4 Dependent claims 2 and 3 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, meet the requirements of the EPC with respect to inventive step:

4.1 claim 2: see D1, para [39]: "The boron concentration may range from $2\times10^{19}/cm^3$ to $7\times10^{20}/cm^3$"

4.2 claim 3: see D1, para [57]: "The transition layer 1420 is further formed epitaxially by decrementing a gas mixture flow of DCS, HCl, and GeH_4 from a higher flow to a lower flow during the formation of the transitional layer 1420. If doping the transition layer 1420, the diborane flow is increased while forming the transitional layer 1420"; the **increase** in diborane flow means that the boron concentration will be **graded**.

5 At least some of the objections raised above are such that there appears to be no possibility of overcoming them by amendment. Refusal of the application under Article 97(2) EPC is therefore to be expected.

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EUROPEAN SEARCH REPORT

Application Number
EP 19 18 8924

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
Y	US 2010/148217 A1 (SIMONELLI DANIELLE [US] ET AL) 17 June 2010 (2010-06-17) * paragraph [0001] - paragraph [0003] * * paragraph [0024] * * paragraph [0034] - paragraph [0051]; figures 6-12 * * paragraph [0053] - paragraph [0058]; figures 14, 15 * -----	1-3	INV. H01L29/78 H01L21/336 H01L21/285 H01L29/45 H01L29/49 H01L29/66 H01L29/167 H01L29/165
Y	STANTON P. ASHBURN ET AL: "SELF-ALIGNED FORMATION OF C54 TITANIUM GERMANOSILICIDE USING RAPID THERMAL PROCESSING AND APPLICATION TO RAISED, ULTRASHALLOW JUNCTIONS", MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, vol. 320, 1 January 1993 (1993-01-01), pages 311-316, XP055631293, US ISSN: 0272-9172, DOI: 10.1557/PROC-320-311 * abstract * * page 311 - page 312 * -----	1-3	

TECHNICAL FIELDS SEARCHED (IPC)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	14 October 2019	Nesso, Stefano

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 19 18 8924

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14-10-2019

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2010148217 A1	17-06-2010	CN 102171794 A	31-08-2011
		EP 2356670 A2	17-08-2011
		JP 2012510720 A	10-05-2012
		KR 20110050713 A	16-05-2011
		TW 201036044 A	01-10-2010
		US 2010148217 A1	17-06-2010
		US 2012032265 A1	09-02-2012
		WO 2010068530 A2	17-06-2010

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Information on Search Strategy - Pilot phase (see OJ 2015, A86)
The type of information contained in this sheet may change during the pilot for improving the usefulness of this new service.

Application Number
EP 19 18 8924

TITLE: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

APPLICANT: INTEL Corporation

IPC CLASSIFICATION: H01L29/78, H01L21/336, H01L21/285, H01L29/45, H01L29/49, H01L29/66, H01L29/167, H01L29/165

EXAMINER: Nesso, Stefano

CONSULTED DATABASES: NPL, WPI, EPODOC, XFULL

CLASSIFICATION SYMBOLS DEFINING EXTENT OF THE SEARCH:

IPC:

CPC: H01L29/66628, H01L29/66636, H01L29/785, H01L29/165, H01L29/66795

FI/F-TERMS:

KEYWORDS OR OTHER ELEMENTS FEATURING THE INVENTION:
FinFET titanium germanosilicide source drain contacts top Ge concentration high 100%

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Date
20.09.19

Reference	Application No./Patent No.
	19188924.5 - 1212
Applicant/Proprietor	
INTEL Corporation	

Designation as inventor - communication under Rule 19(3) EPC

You have been designated as inventor in the above-mentioned European patent application. Below you will find the data contained in the designation of inventor and further data mentioned in Rule 143(1) EPC:

DATE OF FILING	: 30.09.11
PRIORITY	: US/21.12.10/ USA 97527810
TITLE	: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
DESIGNATED STATES	: AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR

INVENTOR (PUBLISHED = 1, NOT PUBLISHED = 0):

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1/GHANI, Tahir/15523 NW Andalusian Way/Portland, OR Oregon 97229/US

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Abstract

Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

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Acknowledgement of receipt

We hereby acknowledge receipt of your request for grant of a European patent as follows:

Submission number	7715914
Application number	EP19188924.5
File No. to be used for priority declarations	EP19188924
Date of receipt	29 July 2019
Your reference	J100788EPA
Applicant	Intel Corporation
Country	US
Title	CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION
Documents submitted	package-data.xml application-body.xml SPECEPO-1.pdf\J100788EPA Spec to be filed.pdf (31 p.) OTHER-1.pdf\ADDREPS - All.pdf (1 p.) ep-request.xml ep-request.pdf (5 p.) SPECEPO-2.pdf\J100788EPA Figures to be filed.pdf (11 p.) f1002-1.pdf (1 p.)
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/European Patent Office/

Claims

1. An integrated circuit structure, comprising:

a fin comprising silicon;

a gate electrode over the fin;

a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;

a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and

a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

Inventors:
Glenn A. Glass
Anand S. Murthy
Tahir Ghani

RELATED APPLICATION

[0001] This application is a continuation-in-part of U.S. Application No. 12/975,278 filed December 21, 2010.

BACKGROUND

[0002] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext}. Decreased R_{ext} enables higher current from an equal transistor design.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention.

[0004] Figure 1B illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0005] Figure 1C illustrates a MOS device configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with another embodiment of the present invention.

[0006] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention.

[0007] Figures 3A to 3I illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

[0008] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention.

[0009] Figures 5A to 5F illustrate structures that are formed when carrying out the method of Figure 4, in accordance with various embodiment of the present invention.

[0010] Figure 6 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

[0011] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap.

[0012] Figure 8 illustrates a computing system implemented with one or more transistor structures in accordance with an example embodiment of the present invention.

[0013] As will be appreciated, the figures are not necessarily drawn to scale or intended to limit the claimed invention to the specific configurations shown. For instance, while some figures generally indicate straight lines, right angles, and smooth surfaces, an actual implementation of a transistor structure may have less than perfect straight lines, right angles, and some features may have surface topology or otherwise be non-smooth, given real world limitations of the processing equipment and techniques used. In short, the figures are provided merely to show example structures.

DETAILED DESCRIPTION

[0014] Techniques are disclosed for forming transistor devices having reduced parasitic contact resistance relative to conventional devices. The techniques can be implemented, for example, using a standard contact stack such as a series of metals on silicon or silicon germanium (SiGe) source/drain regions. In accordance with one example such embodiment, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance. Numerous transistor configurations and

suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. The techniques are particularly well-suited for implementing p-type devices, but can be used for n-type devices if so desired.

General Overview

[0015] As previously explained, increased drive current in the transistors can be achieved by reducing device resistance. Contact resistance is one component of a device's overall resistance. A standard transistor contact stack typically includes, for example, a silicon or SiGe source/drain layer, a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad. In such configurations, the contact resistance is effectively limited by the silicon or SiGe valence band alignment to the pinning level in the metal. Typically, using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV. Thus, and in accordance with an example embodiment of the present invention, an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce the band misalignment value and contact resistance.

[0016] In one specific example embodiment, contacts configured with the intermediate boron doped germanium layer exhibit a reduction in the band misalignment value to less than 0.2 eV and a corresponding reduction in contact resistance of about 3X (relative to a conventional contact stack similarly configured, but without the intermediate boron doped germanium layer between the source/drain regions and contact metal). A transmission electron microscopy (TEM) cross section or secondary ion mass spectrometry (SIMS) profile can be used to show the germanium concentration throughout the vertical stack of the film structure, as profiles of epitaxial alloys of silicon and SiGe can readily be distinguished from germanium concentration profiles.

[0017] Thus, transistor structures configured in accordance with embodiments of the present invention provide an improvement over conventional structures with respect to lower contact resistance. Some such embodiments effectively marry superior contact properties of germanium with superior semiconductor transistor properties of Si and SiGe to provide next generation low resistance contacts.

[0018] Numerous transistor configurations and suitable fabrication processes will be apparent in light of this disclosure, including both planar and non-planar transistor structures (e.g., such as double-gate and trigate transistor structures), as well as strained and unstrained channel structures. Any number of such structural features and material systems can be used in conjunction with a germanium overlayer as described herein. The transistor structure may include p-type source/drain regions, n-type source/drain regions, or both n-type and p-type source/drain regions. In some example embodiments, the transistor structure includes dopant-implanted source/drain regions or epitaxial (or poly) replacement source/drain regions of silicon, SiGe alloys, or nominally pure germanium films (e.g., such as those with less than 10% silicon) in a MOS structure. In any such implementations, an overlayer or cap of boron doped germanium can be formed directly over the source/drain regions, in accordance with an embodiment of the present invention. A contact metal (or series of metals) can then be deposited and a subsequent reaction (annealing) can be carried out to form metal germanide source and drain contacts. As will be appreciated, the contact may be implemented as a stack including one or more of a silicide layer, an adhesion layer, and/or a metal pad layer. The boron doped germanium overlayer can be formed directly over other parts of the transistor structure as well, such as the poly gate and/or grounding tap regions, if so desired.

[0019] As is known, a MOS transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. Some embodiments of the present invention are configured with such conventionally formed tip regions. In other example embodiments, fabrication techniques are employed to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. This can be accomplished, for instance, by selective epitaxial deposition in the source and drain regions as well as their corresponding tip regions to form a bilayer construction of boron doped silicon or SiGe (for the source/drain regions) capped with an overlayer of a boron doped germanium layer in the source/drain and respective tip regions. The germanium and boron concentrations can vary, but in some example embodiments, the germanium concentration is in

the range of 20 atomic % to 100 atomic %, and the boron concentration is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). Note that the boron doped germanium layer may be provided in the tip regions, but in other embodiments is just provided over the source/drain regions (and not in the tip regions).

[0020] In still other example embodiments, an optional thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the underlying substrate with the source/drain layer (e.g., silicon or SiGe). Likewise, a thin buffer with graded germanium concentration and/or boron concentration can be used as an interfacial layer between the source/drain layer and the boron doped germanium cap. In still other embodiments, the boron doped germanium overlayer or source/drain layer themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the relative suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height.

Architecture and Methodology

[0021] Figure 1A illustrates a MOS device 100A formed on a substrate 102 and configured with a boron doped germanium layer between the source/drain layer and contact metals, in accordance with an embodiment of the present invention. In particular, boron doped germanium layer 117 is provided between the source layer 110 and contact metals 125, and boron doped germanium layer 119 is provided between the drain layer 112 and contact metals 127. The source region 110 and the drain region 112 can be formed using any number of conventional techniques. In this example embodiment, for instance, the source region 110 and the drain region 112 are formed by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (e.g., with a germanium concentration in the range of, for instance, 10 to 70 atomic %).

[0022] A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104,

and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A can be formed. In this example embodiment, the tip regions 110A/112A are formed via a typical implantation-diffusion based process, and overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of, for instance, less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the source/drain regions 110/112. Such implantation-diffusion-based tip formation processes generally do not induce a strain on the channel region.

[0023] In any case, and as will be appreciated in light of this disclosure, whether a transistor structure has a strained or unstrained channel, or source-drain tip regions or no source-drain tip regions, is not particularly relevant to various embodiments of the present invention, and such embodiments are not intended to be limited to any particular such structural features. Rather, any number of transistor structures and types can benefit from employing a boron doped germanium overlayer as described herein. The techniques provided herein are compatible, for instance, with conventional dopant implanted silicon, raised source/drain, strained SiGe (or other suitable materials), and any deposited epitaxial tip (sometimes referred to as source-drain extensions) that extend below the gate electrode dielectric or are spaced away from the vertical line defined by the gate electrode dielectric.

[0024] The germanium overlayer 117/119 is generally provided after formation of the source/drain regions 110/112 and prior to formation of the contacts 125/127. The thickness of this overlayer 117/119 can vary from one embodiment to the next, but in one example embodiment is in the range of 50 to 250 Angstroms (Å). The boron concentration of overlayer 117/119 can also vary, but in one example embodiment is in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., in excess of 2E20 cm^{-3}). The overlayer 117/119 can be selectively deposited over the source/drain 110/112 regions (and/or other regions as desired, such as the poly gate or grounding tap regions). Any number of suitable deposition techniques can be used to provide the overlayer

117/119 (e.g., chemical vapor deposition, molecular beam epitaxy, etc). In accordance with one example embodiment, the contact metals 125 and 127 each comprise a stack a nickel silicide layer, a titanium nitride adhesion layer, and a tungsten contact/pad, and although any number of contact metal configurations can be used as will be appreciated in light of this disclosure. Standard deposition techniques can be used in providing the contact metals 125/127.

[0025] Figure 1B illustrates an example MOS device 100B formed on a substrate 102 and configured with a boron doped germanium layer 117/119 between the source/drain layer 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. This example configuration includes source and drain epitaxial tips (generally referred to herein as epi-tips). In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are generally referred to as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A. In accordance with one embodiment, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective epitaxial deposition to provide, for instance, an in situ doped silicon, germanium, or SiGe to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown in Figure 1B, although non-raised configurations can be used as well. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0026] Figure 1C illustrates a MOS device 100C formed on a substrate 102 and configured with boron doped germanium layers 117/119 between the respective source/drain layers 110/112 and contact metals 125/127, in accordance with another embodiment of the present invention. The source region 110 and the drain region 112 in this example embodiment are formed by implanting dopants such as boron into the substrate. The gate stack 122 is formed over a channel region 120 of the transistor 100C and is this example case does not include sidewalls 108. Nor does this example transistor structure include an undercut or tip regions like the embodiments

shown in Figures 1A and 1B. The germanium overlayer 117/119 and the contact metals 125/127 can be implemented, for instance, as previously described with respect to Figure 1A.

[0027] Numerous other variations and features can be implemented for transistor structures configured in accordance with an embodiment of the present invention. For example, a graded buffer may be used in one or more locations of the structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped SiGe fill in the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the source/drain material. In one such embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium concentration graded from a base level compatible with the underlying substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). The boron concentration within this buffer can be either fixed (e.g., at a high level) or graded, for instance, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}). Note that 'compatibility' as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Å, such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be further appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

[0028] Alternatively, rather than using a thin buffer between the substrate 102 and the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, the source/drain material itself can be graded in a similar fashion. For example, and in accordance with one example

embodiment, boron doped SiGe source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 2E20 cm^{-3}).

[0029] In other embodiments, a buffer can be provided between the source/drain material and the boron doped germanium overlayer 117/119. In one such embodiment, the source/drain material is a boron doped SiGe layer having a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to the desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, or 3E20 cm^{-3}). Alternatively, rather than using a buffer between the source/drain material and the boron doped germanium overlayer 117/119, the overlayer 117/119 itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped overlayer 117/119 can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate and/or source/drain regions (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %). The boron concentration within this overlayer 117/119 layer can be fixed at a desired high level or can range, for example, from a base concentration at or otherwise compatible with the underlying substrate and/or source/drain regions up to the desired high level (e.g., in excess of 2E20 cm^{-3}).

[0030] Thus, a low contact resistance architecture for numerous transistor devices is provided. The devices may be formed in part using any number of conventional processes such as, for example, by gate oxide, poly gate electrode, thin spacer, and an isotropic undercut etch in the source/drain regions (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective

epitaxial deposition can be used to provide in situ doped silicon or alternatively, a fully strained silicon germanium layer to form source/drain regions with or without tips. Optional buffers may be used as previously explained. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the conventional gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

[0031] Figure 2 is a method for forming a transistor structure with low contact resistance in accordance with an embodiment of the present invention. Figures 3A through 3I illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments.

[0032] As can be seen, the method begins with forming 202 a gate stack on a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials.

Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other suitable gate electrode materials can be used as well. The gate electrode material, which is may be a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A. As can be seen, Figure 3A illustrates a substrate 300 upon which a gate stack is formed. In this example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode 304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials. Figure 3A further illustrates spacers 310 formed on either side of the stack. The spacers 310 may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers 310 may generally be chosen based on design requirements for the transistor being formed. In accordance with some embodiments, however, the width of the spacers 310 is not subject to design constraints imposed

by the formation of the source and drain epi-tips, given sufficiently high boron doped germanium content in the source/drain tip regions, as described herein (boron won't diffuse into channel).

[0033] With further reference to Figure 2, after the gate stack is formed, the method continues with defining 204 the source/drain regions of the transistor structure. As previously explained, the source/drain regions can be implemented with any number of suitable processes and configurations. For example, the source/drain regions may be implanted, etched and epi filled, raised, silicon or SiGe alloy, p-type and/or n-type, and have a planar or fin shaped diffusion region. In the example embodiment shown in Figure 3A, substrate 300 has been etched to provide cavities 312/314 as well as respective tip areas 312A/314A which undercuts the gate dielectric 302. Figure 3B illustrates the substrate 300 after cavities 312/314 and tip areas 312A/314A have been filled to provide the source/drain regions 318/320 and tip regions 318A/320A. In accordance with some example embodiments, the source and drain region cavities 312/314 along with their respective tip areas 312A/314A are filled with in situ doped silicon or SiGe, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A). Any number of source/drain layer configurations can be used here, with respect to materials (e.g., silicon, SiGe, III-V materials), dopant (e.g., boron in excess of 2E21 cm^{-3}, or other suitable dopant/concentration), and dimension (e.g., thickness of source/drain layer may range, for instance, from 50 to 500 nm so as to provide a flush or raised source/drain region).

[0034] As previously explained, some such embodiments may include with a thin buffer between the source/drain layer and the substrate or the source/drain and boron doped germanium overlayer. For instance, and as can further be seen in the example embodiment shown in Figure 3B, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the source/drain materials. In some embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The boron concentration can be appropriately graded as well. Numerous buffer schemes will be apparent in light of this disclosure.

[0035] With further reference to Figure 2, after the source/drain regions are defined, the method continues with depositing 206 boron doped germanium on the source/drain regions of the transistor structure. Figure 3C shows the boron doped germanium layer 317/319. In some

example embodiments, the boron doped germanium layer 317/319, which may be epitaxially deposited in one or more layers, has a germanium concentration in excess of 90 atomic %, although other suitable concentration levels can be used as will be appreciated in light of this disclosure (e.g., in excess of 91 atomic %, or 92 atomic %, ..., or 98 atomic %, or 99 atomic %, or truly pure germanium). As previously explained, this germanium concentration may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 90 atomic %). The boron concentration in some such embodiments can be in excess of 1E20 cm^{-3}, such as higher than 2E20 cm^{-3} or 2E21 cm^{-3}, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of 1E20 cm^{-3} or 2E20 cm^{-3} or 3E20 cm^{-3}, ..., 2E21 cm^{-3}). In embodiments where the germanium concentration of the underlying source/drain regions 318/320 is fixed or otherwise relatively low, a graded buffer may be used to better interface source/drain regions 318/320 with the boron doped germanium layer 317/319, as previously explained. The thickness of the boron doped germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 Å, in accordance with some specific example embodiments, although alternative embodiments may have other layer thicknesses, as will be apparent in light of this disclosure.

[0036] In some embodiments, a CVD process or other suitable deposition technique may be used for the depositing 206 or otherwise forming the boron doped germanium layer 317/319. For example, the depositing 206 may be carried out in a CVD, or rapid thermal CVD (RT-CVD), or low pressure CVD (LP-CVD), or ultra-high vacuum CVD (UHV-CVD), or gas source molecular beam epitaxy (GS-MBE) tool using germanium and boron containing precursors such as germane (GeH_4) or digermane (Ge_2H_6) and diborane (B_2H_6) or boron difluoride (BF_2). In some such embodiments, there may be a carrier gas such as, for instance, hydrogen, nitrogen, or a noble gas (e.g., precursor is diluted at 1-5% concentration of carrier gas). There may also be an etchant gas such as, for example, halogen-based gas such as hydrogen chloride (HCl), chlorine (Cl), or, hydrogen bromide (HBr). The basic deposition of germanium and also boron doped germanium is possible over a wide range of conditions using deposition temperature in the range, for example, of 300°C to 800°C (e.g., 300-500°C) and reactor pressure, for instance, in the range 1 Torr to 760 Torr. Germanium is naturally selective in that it deposits on silicon or silicon-germanium alloy, and does not deposit on other materials such as silicon dioxide and silicon nitride. Since this natural selectivity is not entirely perfect, a small flow of etchant can be used

to increase the selectivity of the deposition, as previously noted. Each of the carrier and etchants can have a flow in the range of 10 and 300 SCCM (typically, no more than 100 SCCM of flow is required, but some embodiments may require higher flow rates). In one specific example embodiment, the deposition 206 is carried out using GeH_4 that is diluted in hydrogen at a 1% concentration and at a flow rate that ranges between 100 and 1000 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 3% concentration and at a flow rate that ranges between 100 and 600 SCCM. In some such specific example cases, an etching agent of HCl or Cl_2 is added at a flow rate that ranges, for example, between 10 and 100 SCCM, to increase the selectivity of the deposition.

[0037] As will be appreciated in light of this disclosure, the selectivity at which the boron doped germanium layer 317/319 is deposited can vary as desired. In some cases, for instance, the boron doped germanium layer 317/319 is deposited only on the source/drain regions 318/320 or a portion of the source/drain regions 318/320 (rather than across the entire structure). Any number of masking/patterning techniques can be used to selectively deposit layer 317/319. Moreover, other embodiments may benefit from layer 317/319 covering, for example, poly gate regions or grounding tap regions. As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 90 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of 2E20 cm^{-3}) can be used to realize significantly lower contact resistance in the source and drain regions (and other areas where low contact resistance is desirable, such as ground tap regions), in accordance with some example embodiments. Further, and as previously explained, since boron diffusion is sufficiently suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite any high boron concentration proximate the channel (if applicable). Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

[0038] With further reference to Figure 2, after the boron doped germanium layer 317/319 is provided, the method continues with depositing 208 a dielectric over layer 317/319. Figure 3D shows dielectric 322 as being flush with the hard mask 306 of the gate stack, but it need not be. The dielectric can be configured in a number of ways. In some embodiments, dielectric 322 is implemented with silicon dioxide (SiO_2) or other low-k dielectric materials. In other

embodiments, dielectric 322 is implemented with a silicon nitride (SiN) liner followed by one or more layers of SiO_2, or any combination of nitride, oxide, oxynitride, carbide, oxycarbide, or other suitable dielectric materials). The dielectric 322, which may be referred to as an interlayer dielectric (ILD), may be planarized as commonly done. Other example dielectric materials include, for instance, carbon doped oxide (CDO), organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant.

[0039] Next, in some embodiments of the present invention where a replacement metal gate (RMG) process is used and as best shown in Figure 3E, the method may further include removing the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 and hard mask layer 306 are removed. Figure 3E illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing a new gate dielectric layer into the trench opening (designated as 324 in Figure 3F). Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material. As further shown in Figure 3F, the method may further continue with depositing the metal gate electrode layer 326 into the trench and over the gate dielectric layer 324. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a P-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited in the gate trench followed by a suitable metal gate electrode fill metal such as aluminum or silver.

[0040] With further reference to Figure 2, after dielectric layer 322 is provided over layer 317/319 (and any desired RMG process), the method continues with etching 210 to form the source/drain contact trenches. Any suitable dry and/or wet etch processes can be used. Figure 3G shows the source/drain contact trenches after etching is complete, in accordance with one example embodiment. The method then continues with depositing 212 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 214 the source/drain contact plugs. Figure 3H shows the contact metals 325/327, which in some embodiments includes the silicide/germanide, although other embodiments may include additional layers (e.g., adhesion layer). Figure 3I shows the contact plug metal 329/331, which in some embodiments includes aluminum, although any suitably conductive contact metal or alloy can be used for the contact plug 329/331, such as silver, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium, using conventional deposition processes. The germanide/metalization 212 of the source and drain contacts can be carried out, for instance, by silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants to form a low resistance germanide. The boron doped germanium layer 317/319 allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including R_{ext}) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit R_{ext} values of about 140 Ohm*um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in R_{ext} in PMOS devices (e.g., about a 2x improvement or better, such as a R_{ext} of about 70 Ohm*um), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with boron doped germanium cap 317/319 in accordance with an embodiment of the present, with a boron concentration in excess of 1E20 cm^{-3} and a germanium concentration in excess of 90 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain regions 318/320 and the contact metals 325/327, can exhibit R_{ext} values of less than 100 Ohm*um, and in some cases less than 90 Ohm*um, and in some cases less than 80 Ohm*um, and in some cases less than 75 Ohm*um, or lower.

[0041] Figure 4 is a method for forming a transistor structure with low contact resistance in accordance with another embodiment of the present invention. Figures 5A through 5F illustrate example structures that are formed as the method is carried out, and in accordance with some embodiments. In general, this method is similar to the method described with reference to Figures 2 and 3A-H, except that the deposition of the boron doped germanium layer 317/319 on the source/drain regions is carried out after the dielectric 322 is deposited and etched to form the contact trench. Thus, the method includes depositing 406 the dielectric 322 directly over the source/drain regions 318/320, and then continues with etching 408 to form the source/drain contact trench and then selectively depositing 410 the boron doped germanium layer 317/319 into the trench (and directly onto the source/drain regions 318/320), as best shown in Figures 5C through 5E. Depositing 410 can be carried out using any suitable deposition process, such as selective epitaxy. Once layer 317/319 is provided, the contact metals 325/327 can be provided on top of the layer 317/319, as shown in Figure 5F. This alternate methodology provides the same benefit of improved contact resistance, but is more selective in where the boron doped germanium is deposited. Other such selective deposition processes will be apparent in light of this disclosure, using any suitable combination of masking/patterning and selective deposition techniques.

[0042] As will be further appreciated, the previous relevant discussion with respect to similar parts of the method is equally applicable here. In particular, forming 402 a gate stack and defining 404 the source/drain regions of the transistor structure can be carried as previously discussed with reference to the forming 202 and defining 204 previously discussed with reference to Figure 2. Likewise, depositing 412 contact resistance reducing metal and annealing to form silicide/germanide, and then depositing 414 the source/drain contact plugs can be carried as previously discussed with reference to the forming 212 and defining 214 previously discussed with reference to Figure 2.

FinFET Configuration

[0043] As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate

surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

[0044] Figure 6 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 600 having a semiconductor body or fin 660 (represented by dashed lines) extending from the substrate 600 through isolation regions 610, 620. A gate electrode 640 is formed over 3 surfaces of the fin 660 to form 3 gates. A hard mask 690 is formed on top of the gate electrode 640. Gate spacers 670, 680 are formed at opposite sidewalls of the gate electrode 640.

[0045] A source region comprises the epitaxial region 631 formed on a recessed source interface 650 and on one fin 660 sidewall, and a drain region comprises the epitaxial region 631 formed on a recessed source interface 650 and on the opposing fin 660 sidewall (not shown). A cap layer 641 is deposited over the epitaxial regions 631. Note that the boron cap layer 641 may be provided in the recessed (tip) regions, but in other embodiments is just provided over the source/drain regions (and not in the recessed regions). In one embodiment, the isolation regions 610, 620 are shallow trench isolation (STI) regions formed using conventional techniques, such as etching the substrate 600 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 610, 620 can be made from any suitable dielectric/insulative material, such as SiO_2. The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 600 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

[0046] As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the FinFET transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 631 and cap layer 641 can be implemented, for instance, using an in situ doped silicon or SiGe (for 631) capped with a boron doped germanium (for 641), with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer

may be used to transition from a base level germanium/boron concentration compatible with the epitaxial region 631 to the boron doped germanium cap 641. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 631 and/or the cap 641, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 660.

[0047] Figure 7 shows a plot of a split lot showing contact resistance for transistor structures configured with in accordance with embodiments of the present invention and standard transistor structures configured with no cap. The transistor structures associated with the high resistance numbers in excess of 0.18 are all implemented with standard SiGe alloy raised PMOS source/drain regions with contact metal deposited directly thereon. The transistor structures associated with the resistance numbers of 0.107 and lower are all similarly implemented but with the addition a boron doped germanium cap between the source/drain regions and contact metal, in accordance with various embodiments of the present invention. Table 1 shows the raw data quantiles resulting from testing of the example structures with and without a boron doped germanium cap as described herein.

Ge Cap	Min	10%	25%	Median	75%	90%	Max
Yes	0.032	0.032	0.033	0.040	0.078	0.105	0.107
No	0.183	0.183	0.192	0.239	0.250	0.265	0.265

Table 1

As can be seen, this example lot actually shows an improvement (reduction) in contact resistance of about a three to six times (3X to 6X) over conventional transistor structures. The units are Ohms per arbitrary area.

[0048] Other improvements enabled by using a boron doped germanium cap in accordance with an embodiment of the present invention will be apparent in light of this disclosure. In particular, the resulting germanide materials and Schottky barrier height improvement enables more than a 2x R_{ext} improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position

of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

Example System

[0049] Figure 8 illustrates a computing device 1000 configured in accordance with one embodiment of the invention. As can be seen, the computing device 1000 houses a motherboard 1002. The motherboard 1002 may include a number of components, including but not limited to a processor 1004 and at least one communication chip 1006, each of which can be physically and electrically coupled to the motherboard 1002, or otherwise integrated therein. As will be appreciated, the motherboard 1002 may be, for example, any printed circuit board, whether a main board or a daughterboard mounted on a main board or the only board of device 1000, etc. Depending on its applications, computing device 1000 may include one or more other components that may or may not be physically and electrically coupled to the motherboard 1002. These other components may include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth). Any of the components included in computing device 1000 may include one or more transistor structures as described herein. In some embodiments, multiple functions can be integrated into one or more chips (e.g., for instance, note that the communication chip 1006 can be part of or otherwise integrated into the processor 1004).

[0050] The communication chip 1006 enables wireless communications for the transfer of data to and from the computing device 1000. The term "wireless" and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 1006 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE

802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 1000 may include a plurality of communication chips 1006. For instance, a first communication chip 1006 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0051] The processor 1004 of the computing device 1000 includes an integrated circuit die packaged within the processor 1004. In some embodiments of the present invention, the integrated circuit die of the processor includes an onboard non-volatile memory or cache, and/or is otherwise communicatively coupled to off-chip memory that is implemented with one or more transistor structures as described herein. The term "processor" may refer to any device or portion of a device that processes, for instance, electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0052] The communication chip 1006 may also include an integrated circuit die packaged within the communication chip 1006. In accordance with some such example embodiments, the integrated circuit die of the communication chip includes one or more devices implemented with one or more transistor structures as described herein. As will be appreciated in light of this disclosure, note that multi-standard wireless capability may be integrated directly into the processor 1004 (e.g., where functionality of any chips 1006 is integrated into processor 1004, rather than having separate communication chips). Further note that processor 1004 may be a chip set having such wireless capability. In short, any number of processor 1004 and/or communication chips 1006 can be used. Likewise, any one chip or chip set can have multiple functions integrated therein.

[0053] In various implementations, the computing device 1000 may be a laptop, a netbook, a notebook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder.

In further implementations, the device 1000 may be any other electronic device that processes data or employs transistors.

[0054] Numerous embodiments will be apparent in light of this disclosure, and features described herein can be combined in any number of configurations. One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region, and a gate electrode above the channel region. A gate dielectric layer is provided between the gate electrode and the channel region, and source and drain regions are provided in the substrate and adjacent to the channel region. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions. This boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. In one such example, the device is one of a planar or FinFET transistor. In another example case, the device comprises a PMOS transistor. In another example case, the device further includes an interlayer dielectric. In another example case, the device further includes a graded buffer between the substrate and the source and drain regions and/or a graded buffer between the source and drain regions and the boron doped germanium layer. In one such case, the graded buffer between the source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %. In one such specific example case, the high concentration reflects pure germanium. In another example case, the graded buffer between the source and drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %. In another example case, the source and drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another

example case, the source and drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}. In another example case, the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}. Another embodiment provides an electronic device that includes a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as variously defined in in this paragraph. In one such case, the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices. In another such case, the device is a computing device (e.g., mobile telephone or smartphone, laptop, tablet computer, etc).

[0055] Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region, and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers. The device further includes a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}. The device further includes metal-germanide source and drain contacts on the boron doped germanium layer. The device is one of a planar or FinFET transistor. In one such example case, the device further includes a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}. In another example

case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron. In another example case, the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %. In another example case, the source and drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In another example case, the source and drain regions comprise silicon germanium having a fixed germanium concentration, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms. Another embodiment provides a computing device (e.g., desktop or portable computer, etc) that includes a printed circuit board having a communication chip and/or a processor, wherein at least one of the communication chip and/or processor comprises one or more transistor devices as variously defined in this paragraph.

[0056] Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region. The method continues with providing source and drain regions in the substrate and adjacent to the channel region, and providing a boron doped germanium layer on at least a portion of the source and drain regions. The boron doped germanium layer comprises a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1E20 cm^{-3}. The method continues with providing metal-germanide source and drain contacts on the boron doped germanium layer. In some example such cases, the method further includes providing a graded buffer between the substrate and the source and drain regions, and/or providing a graded buffer between the source and drain regions and the boron doped germanium layer. In another example case, the boron doped germanium layer has a graded concentration of at least one of germanium and boron (which may be used with or

without graded buffers). This method may be employed, for example, in the fabrication of any electronic devices such as a computing device.

[0057] The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

Further Exemplary Embodiments

Example 1. A transistor device, comprising: a substrate having a channel region; a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region; source and drain regions in the substrate and adjacent to the channel region; a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1 E20 cm^{-3}; and metal-germanide source and drain contacts on the boron doped germanium layer.

Example 2. The device of example 1 wherein the device is one of a planar or FinFET transistor.

Example 3. The device of examples 1 or 2 wherein the device comprises a PMOS transistor.

Example 4. The device of any of the preceding examples further comprising an interlayer dielectric.

Example 5. The device of the preceding examples, further comprising at least one of: a graded buffer between the substrate and the source and drain regions; and a graded buffer between the source and drain regions and the boron doped germanium layer.

Example 6. The device of example 5 wherein the graded buffer between the source and drain regions and the boron doped germanium layer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %.

Example 7. The device of example 6 wherein the high concentration reflects pure germanium.

Example 8. The device of examples 5, 6, or 7 wherein the graded buffer between the source and drain regions and the boron doped germanium layer has a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1E20 cm^{-3}.

Example 9. The device of any of the preceding examples wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

Example 10. The device of any of the preceding examples wherein the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 95 atomic %.

Example 11. The device of any of the preceding examples wherein the source and drain regions comprise boron doped silicon germanium having a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1 E20 cm^{-3}.

Example 12. The device of any of examples 1 through 4 wherein the source and drain regions comprise silicon or silicon germanium, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 1 E20 cm- 3.

Example 13. The device of any of the preceding examples wherein the boron doped germanium layer comprises a germanium concentration in excess of 98 atomic %, and a boron concentration in excess of 2E20 cm^{-3}.

Example 14. An electronic device comprising: a printed circuit board having one or more integrated circuits, wherein at least one of the one or more integrated circuits comprises one or more transistor devices as defined in any of the preceding examples.

Example 15. The electronic device of example 14 wherein the one or more integrated circuits includes at least one of a communication chip and/or a processor, and at least one of the communication chip and/or processor comprises the one or more transistor devices.

Example 16. The electronic device of examples 14 or 15 wherein the device is a computing device.

Example 17. A transistor device, comprising: a substrate having a channel region; a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers; a boron doped germanium layer on at least a portion of the source and drain regions, and comprising a germanium concentration in excess of 95 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and metal-germanide source and drain contacts on the boron doped germanium layer; wherein the device is one of a planar or FinFET transistor.

Example 18. The device of example 17, the device further comprising: a buffer between the source and drain regions and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}.

Example 19. The device of example 17 wherein the boron doped germanium layer has a graded concentration of at least one of germanium and boron.

Example 20. The device of example 17 wherein the source and drain regions comprise silicon germanium having a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium layer has a germanium concentration in excess of 98 atomic %.

Example 21. The device of example 20 wherein the source and drain regions have a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

Example 22. The device of example 17 wherein the source and drain regions comprise silicon germanium having a fixed gemianium concentration, and the device further comprises a buffer between the source and drain regions and the boron doped germanium layer, the buffer having a gemianium concentration that is graded from a base level concentration compatible with the

source and drain regions to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the source and drain regions to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

Example 23. A method for forming a transistor device, comprising: providing a substrate having a channel region; providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region; and providing source and drain regions in the substrate and adjacent to the channel region; providing a boron doped germanium layer on at least a portion of the source and drain regions, the boron doped germanium layer comprising a germanium concentration in excess of 90 atomic % and a boron concentration in excess of 1 E20 cm^{-3}; and providing metal-germanide source and drain contacts on the boron doped germanium layer.

Form 1002 - 1: Public inventor(s)

Designation of inventor

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Application No:

Public

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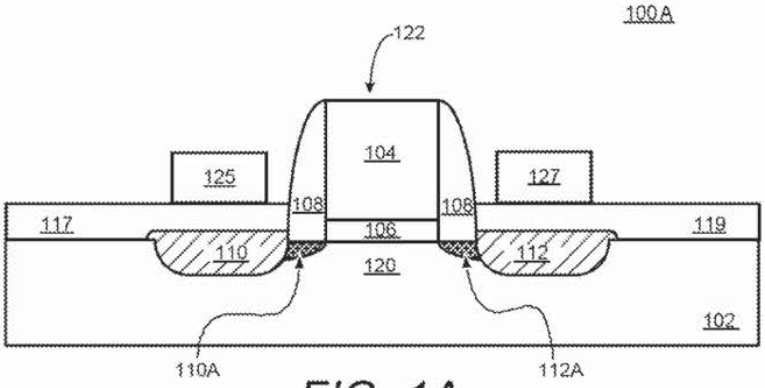


FIG. 1A

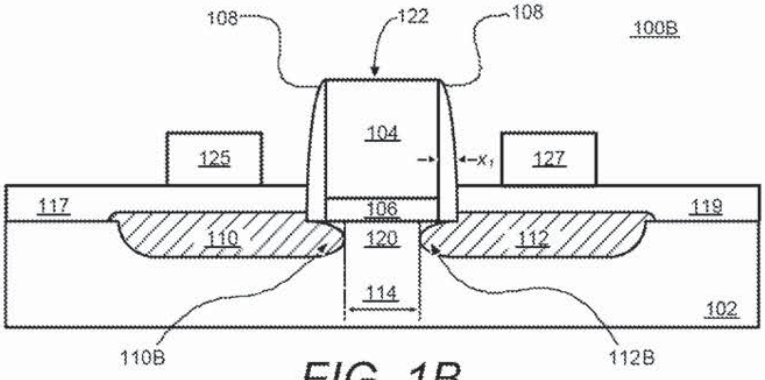


FIG. 1B

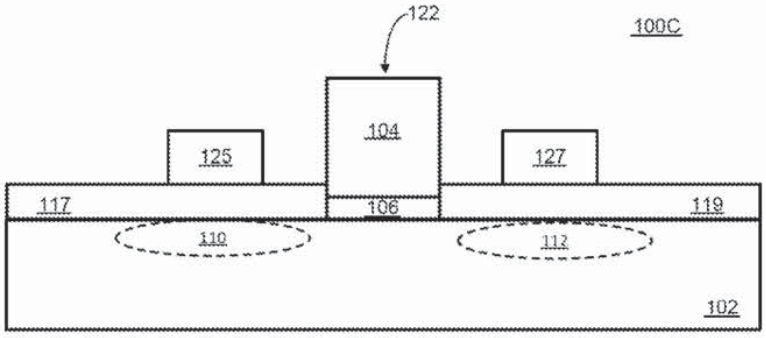


FIG. 1C

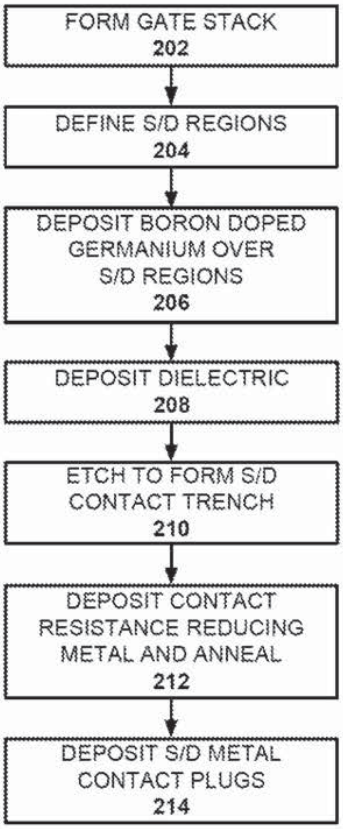

FORM GATE STACK
202
DEFINE S/D REGIONS
204
DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
206
DEPOSIT DIELECTRIC
208
ETCH TO FORM S/D CONTACT TRENCH
210
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
212
DEPOSIT S/D METAL CONTACT PLUGS
214

FIG. 2

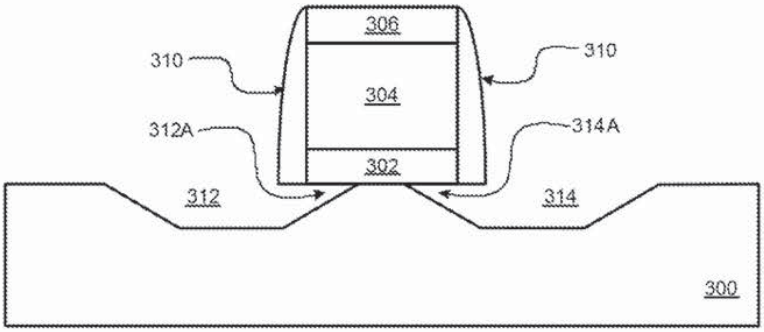


FIG. 3A

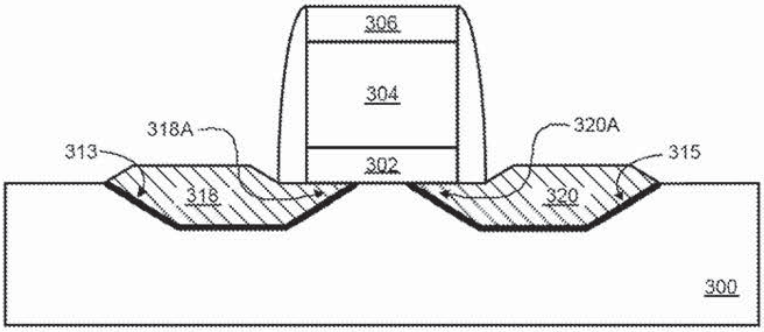


FIG. 3B

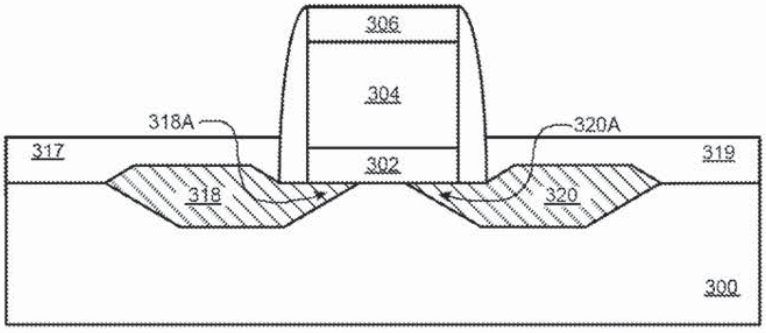


FIG. 3C

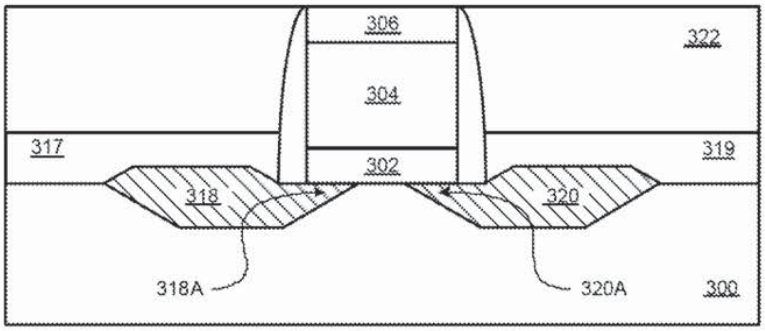


FIG. 3D

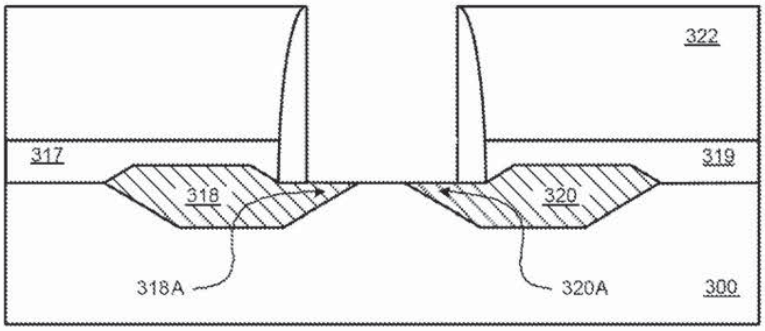


FIG. 3E

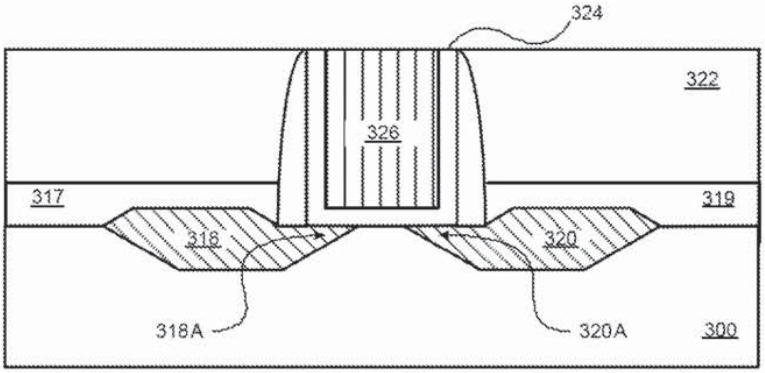


FIG. 3F

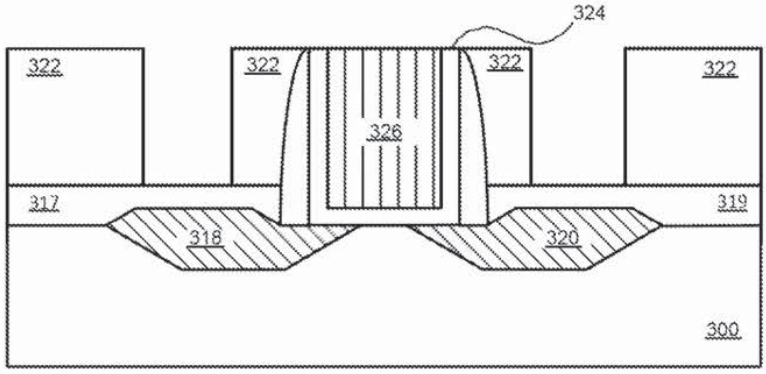


FIG. 3G

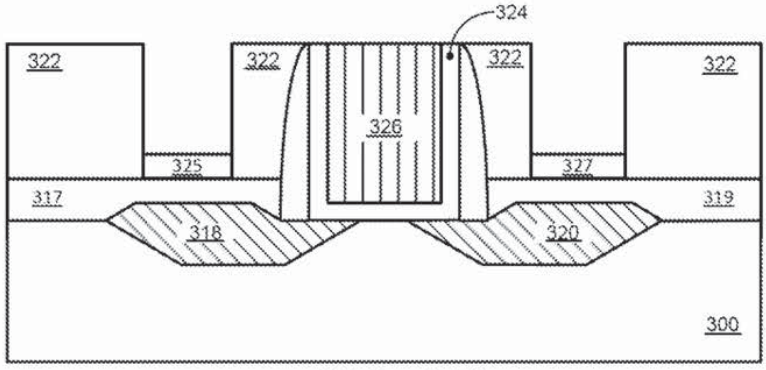


FIG. 3H

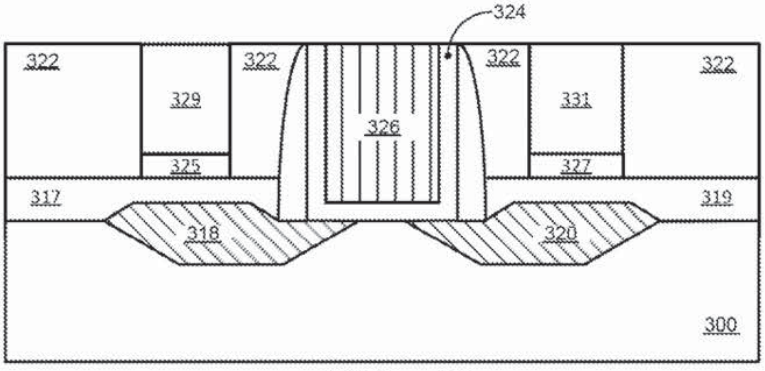


FIG. 3I

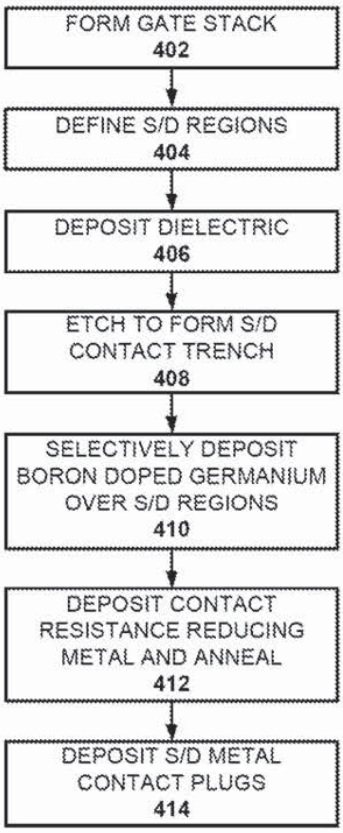

FORM GATE STACK
402
DEFINE S/D REGIONS
404
DEPOSIT DIELECTRIC
406
ETCH TO FORM S/D CONTACT TRENCH
408
SELECTIVELY DEPOSIT BORON DOPED GERMANIUM OVER S/D REGIONS
410
DEPOSIT CONTACT RESISTANCE REDUCING METAL AND ANNEAL
412
DEPOSIT S/D METAL CONTACT PLUGS
414

FIG. 4

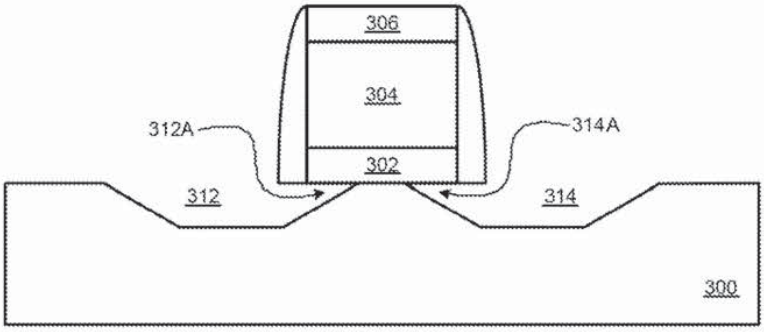


FIG. 5A

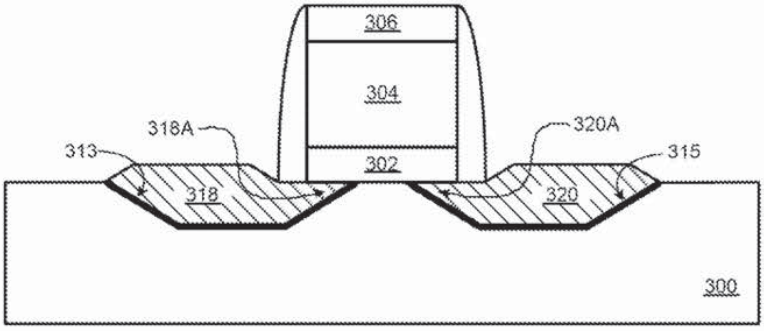


FIG. 5B

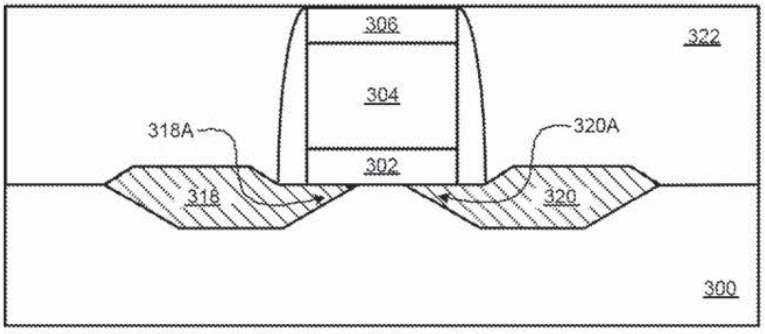


FIG. 5C

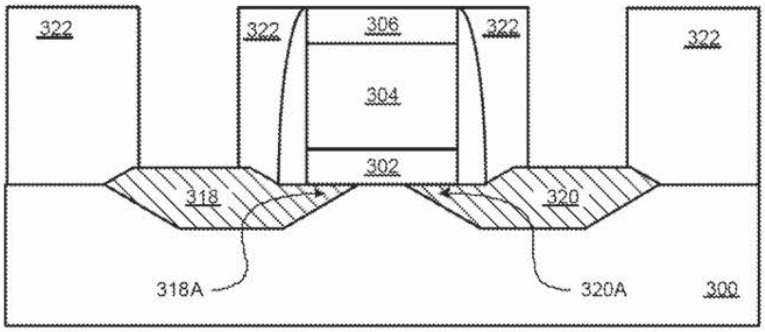


FIG. 5D

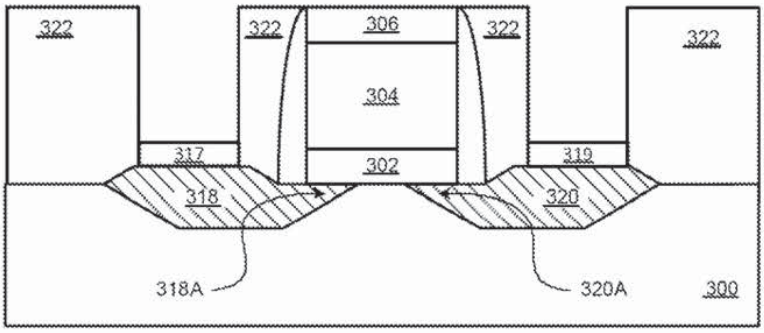


FIG. 5E

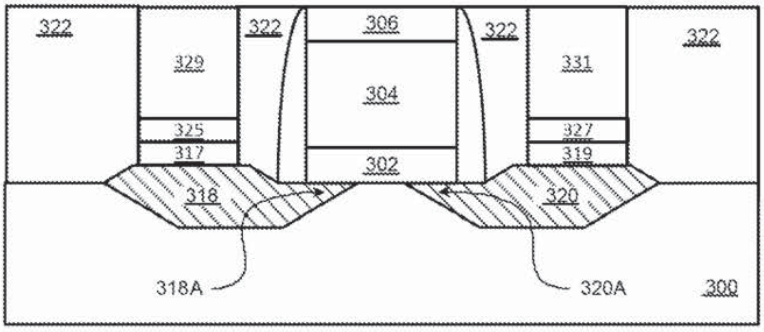


FIG. 5F

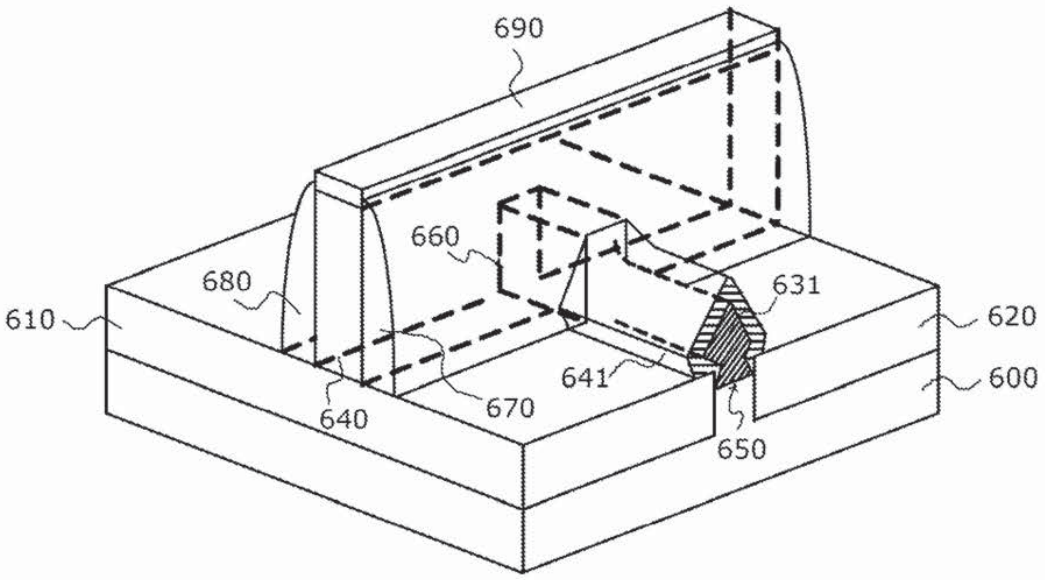


FIG. 6

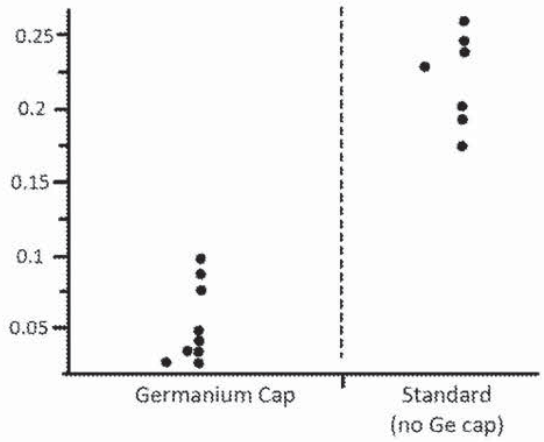


FIG. 7

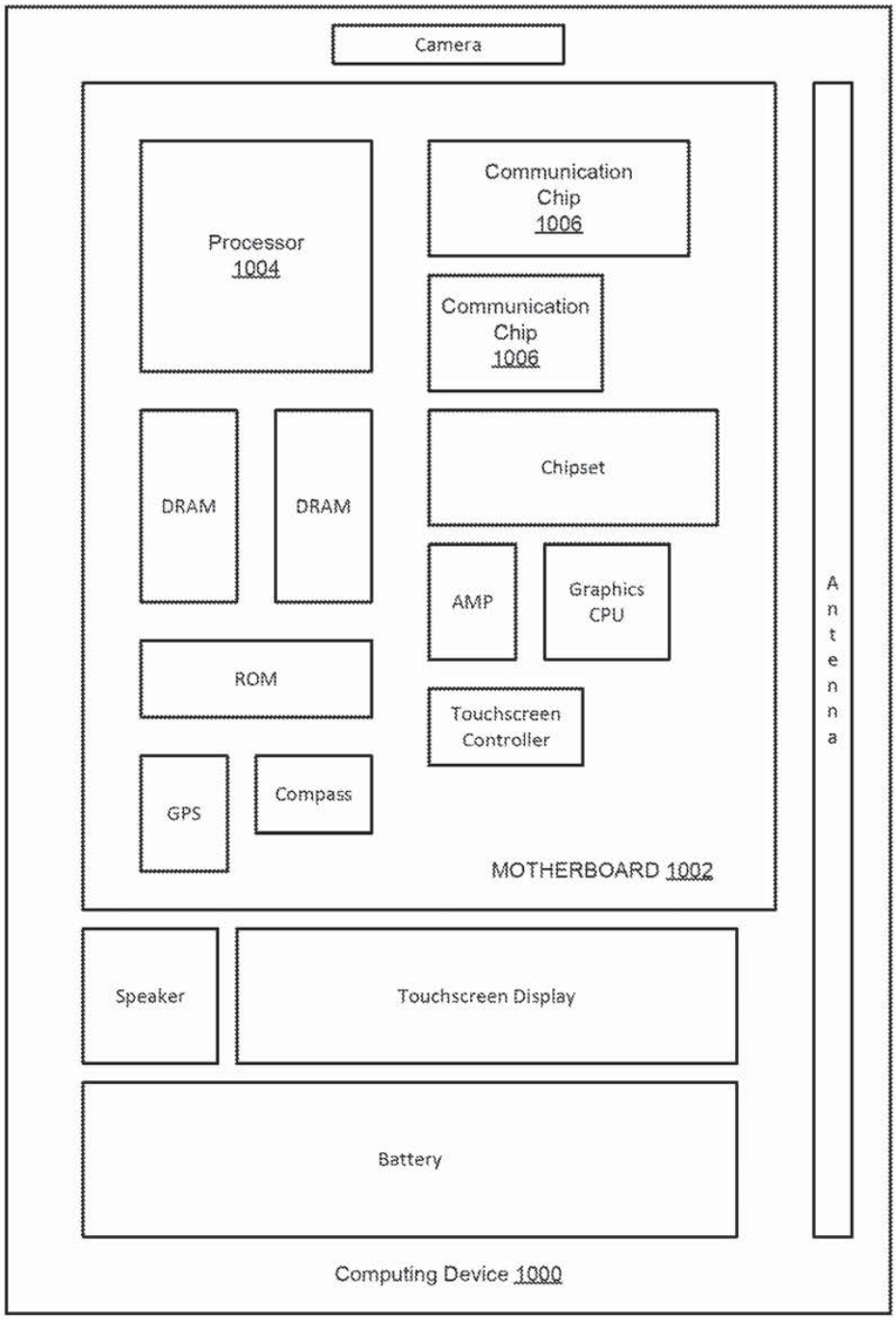

Camera
Processor
1004
Communication
Chip
1006
Communication
Chip
1006
DRAM
DRAM
Chipset
AMP
Graphics
CPU
ROM
Touchscreen
Controller
GPS
Compass
MOTHERBOARD 1002
Antenna
Speaker
Touchscreen Display
Battery
Computing Device 1000

Fig. 8

Europäisches Patentamt
European Patent Office
Office européen des brevets

Request for grant of a European patent

For official use only		
1 Application number:	MKEY	**MKEY - EP19188924.5**
2 Date of receipt (Rule 35(2) EPC):	DREC	**DREC - 29 Jul 2019**
3 Date of receipt at EPO (Rule 35(4) EPC):	RENA	
4 Date of filing:		

5 Grant of European patent, and examination of the application under Article 94, are hereby requested. ☒

5.1 The applicant waives his right to be asked whether he wishes to proceed further with the application (Rule 70(2)) ☐

Procedural language: en

Filing Language: en

6 Applicant's or representative's reference: J100788EPA

Filing Office: EP

Applicant 1

7-1 Name: Intel Corporation

8-1 Address:
2200 Mission College Boulevard
Santa Clara CA California 95054
United States of America

10-1 State of residence or of principal place of business: United States of America

14.1 The/Each applicant hereby declares that he is an entity or a natural person under Rule 6(4) EPC. ☐

Representative 1

15-1 Name: Rummler, Mr. Felix

Company: Maucher Jenkins

16-1 Address of place of business:
26 Caxton Street
London SW1H 0RJ
United Kingdom

17-1 Telephone: +44 (0)20 7931 7141

17-1 Fax: +44 (0)20 7222 4660

17-1 E-mail: info@maucherjenkins.com

Inventor(s)

23 Designation of inventor attached ☒

24 **Title of invention**

Title of invention: CONTACT RESISTANCE REDUCTION EMPLOYING GERMANIUM OVERLAYER PRE-CONTACT METALIZATION

25 **Declaration of priority (Rule 52) and search results under Rule 141(1)**

A declaration of priority is hereby made for the following applications

	State	Filing date	Kind	Application number:	Search results under Rule 141(1) are attached
Priority 01	US	21.12.2010	ap	12/975278	☐

25.2 Re-establishment of rights

Re-establishment of rights under Article 122 EPC in respect of the priority period is herewith requested for the following priority/priorities

25.3 The EPO is requested to retrieve a certified copy of the following previous application(s) (priority document(s)) via the WIPO Digital Access Service (DAS) using the indicated access code(s):

	Request	Application number:	Access Code
Priority 01	☐	12/975278	

25.4 This application is a complete translation of the previous application ☐

25.5 It is not intended to file a (further) declaration of priority ☐

26 **Reference to a previously filed application**

27 **Divisional application** ☒

Application number of earlier application: EP11852027.9

Date of Filing (Art. 80/Rule 40 EPC): 30 September 2011

27.1 This divisional application is of the following generation: ☒ 1 ☐ 2 ☐ 3 ☐ 4 ☐ 5 or subsequent

28 **Article 61(1)(b) application** ☐

29 Claims

Number of claims: 3

29.1 ☒ as attached

29.2 ☐ as in the previously filed application (see Section 26.2)

29.3 ☐ The claims will be filed later

30 Figures

It is proposed that the abstract be published together with figure No. 5F

31 Designation of contracting states

All the contracting states party to the EPC and valid for the parent application at the time of filing of this divisional application are deemed to be designated (see Article 76(2)).

32 Different applicants for different contracting states

33 Extension/Validation

This application is deemed to be a request to extend the effects of the European patent application and the European patent granted in respect of it to all non-contracting states to the EPC with which extension or validation agreements are in force on the date on which the application is filed. However, the request is deemed withdrawn if the extension fee or the validation fee, whichever is applicable, is not paid within the prescribed time limit.

33.1 It is intended to pay the extension fee(s) for the following state(s):

33.2 It is intended to pay the validation fee(s) for the following state(s):

34 Biological material

38 Nucleotide and amino acid sequences

38.1 The description contains a sequence listing. ☐

38.2a The sequence listing is attached in computer-readable format in accordance with WIPO Standard ST.25 (Rule 30(1)). ☐

38.2b The sequence listing is attached in PDF format ☐

Further indications

39 Additional copies of the documents cited in the European search report are requested

Number of additional sets of copies:

40 Refund of the search fee under Article 9(2) of the Rules relating to Fees is requested ☒

Application number or publication number of earlier search report: 11852027.9

42 Payment

Method of payment: Debit from deposit account

The European Patent Office is hereby authorised, to debit from the deposit account with the EPO any fees and costs indicated on the fees section below.

Currency: EUR

Deposit account number: 28050072

Account holder: Maucher Jenkins

43 Refunds

Fees	Factor applied	Fee schedule	Amount to be paid
001 Filing fee - EP direct - online	1	120.00	120.00
002 Fee for a European search - Applications filed on/after 01.07.2005	1	1 300.00	1 300.00
015 Claims fee - For the 16th to the 50th claim	0	235.00	0.00
015e Claims fee - For the 51st and each subsequent claim	0	585.00	0.00
033 Renewal fee for the 3rd year	1	470.00	470.00
034 Renewal fee for the 4th year	1	585.00	585.00
035 Renewal fee for the 5th year	1	820.00	820.00
036 Renewal fee for the 6th year	1	1 050.00	1 050.00
037 Renewal fee for the 7th year	1	1 165.00	1 165.00
038 Renewal fee for the 8th year	1	1 280.00	1 280.00
039 Renewal fee for the 9th year	1	1 395.00	1 395.00
501 Additional filing fee for the 36th and each subsequent page	7	15.00	105.00
Total:		EUR	8 290.00

44-A Forms

		Details:	System file name:
A-1	Request		as ep-request.pdf
A-2	1. Designation of inventor	1. Inventor	as f1002-1.pdf

44-B Technical documents

		Original file name:	System file name:
B-1	Specification	J100788EPA Spec to be filed.pdf Description; 3 claims; abstract	SPECEPO-1.pdf

B-2	Specification	J100788EPA Figures to be filed.pdf 23 figure(s)	SPECEPO-2.pdf

44-C Other documents		Original file name:	System file name:
C-1	Additional Representatives	ADDREPS - All.pdf	OTHER-1.pdf

45 General authorisation:

46 Signature(s)

Place:

Date: 29 July 2019

Signed by: Felix Rummler 25782

Representative name: Felix Rummler

Capacity: (Representative)

WIPO
WORLD
INTELLECTUAL PROPERTY
ORGANIZATION

DOCUMENT MADE AVAILABLE UNDER THE PATENT COOPERATION TREATY (PCT)

International application number:		**PCT/US2011/054198**
International filing date:		**30 September 2011 (30.09.2011)**
Document type:		**Certified copy of priority document**
Document details:	Country/Office:	**US**
	Number:	**12/975,278**
	Filing date:	**21 December 2010 (21.12.2010)**
Date of receipt at the International Bureau:		**15 October 2011 (15.10.2011)**

Remark: Priority document submitted or transmitted to the International Bureau in compliance with Rule 17.1(a),(b) or (b-*bis*)

34, chemin des Colombettes
1211 Geneva 20, Switzerland
www.wipo.int

425102

THE UNITED STATES OF AMERICA

TO ALL TO WHOM THESE PRESENTS SHALL COME:

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

October 13, 2011

THIS IS TO CERTIFY THAT ANNEXED HERETO IS A TRUE COPY FROM THE RECORDS OF THE UNITED STATES PATENT AND TRADEMARK OFFICE OF THOSE PAPERS OF THE BELOW IDENTIFIED PATENT APPLICATION THAT MET THE REQUIREMENTS TO BE GRANTED A FILING DATE.

APPLICATION NUMBER: *12/975,278*
FILING DATE: *December 21, 2010*
RELATED PCT APPLICATION NUMBER: *PCT/US11/54198*

THE COUNTRY CODE AND NUMBER OF YOUR PRIORITY APPLICATION, TO BE USED FOR FILING ABROAD UNDER THE PARIS CONVENTION, IS *US12/975,278*

Certified by

David J. Kappos

Under Secretary of Commerce
for Intellectual Property
and Director of the United States
Patent and Trademark Office

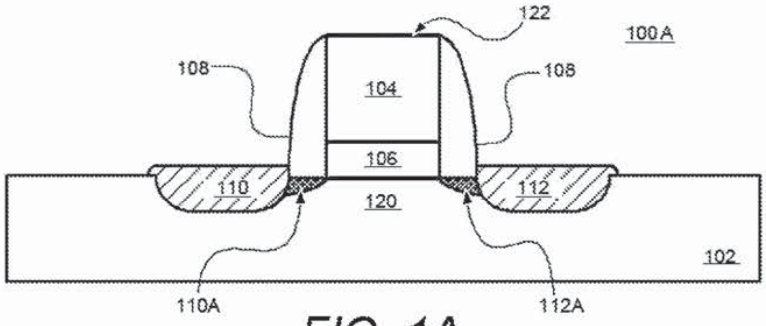


FIG. 1A

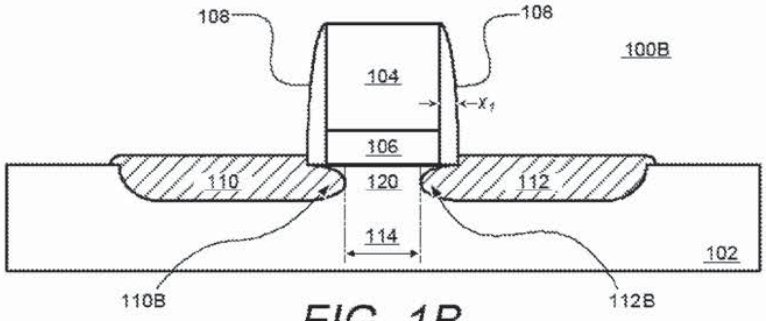


FIG. 1B

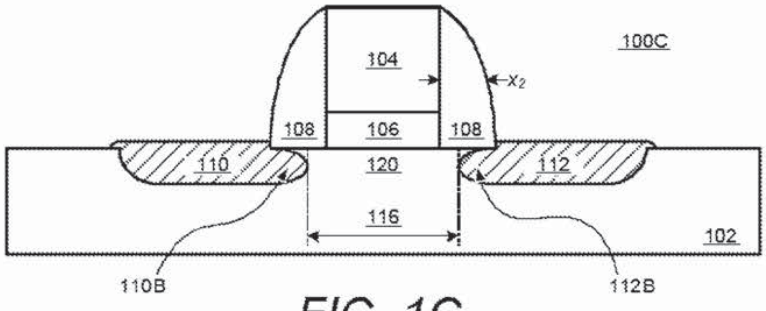


FIG. 1C

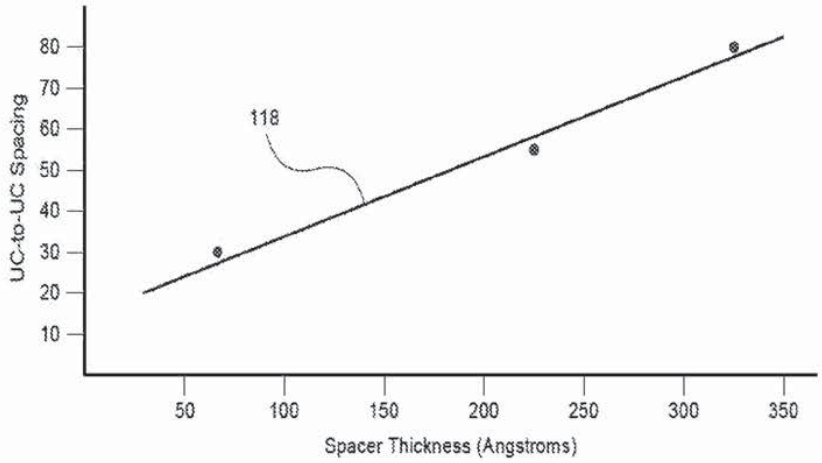

UC-to-UC Spacing
80
70
60
50
40
30
20
10
118
50
100
150
200
250
300
350
Spacer Thickness (Angstroms)

FIG. 1D

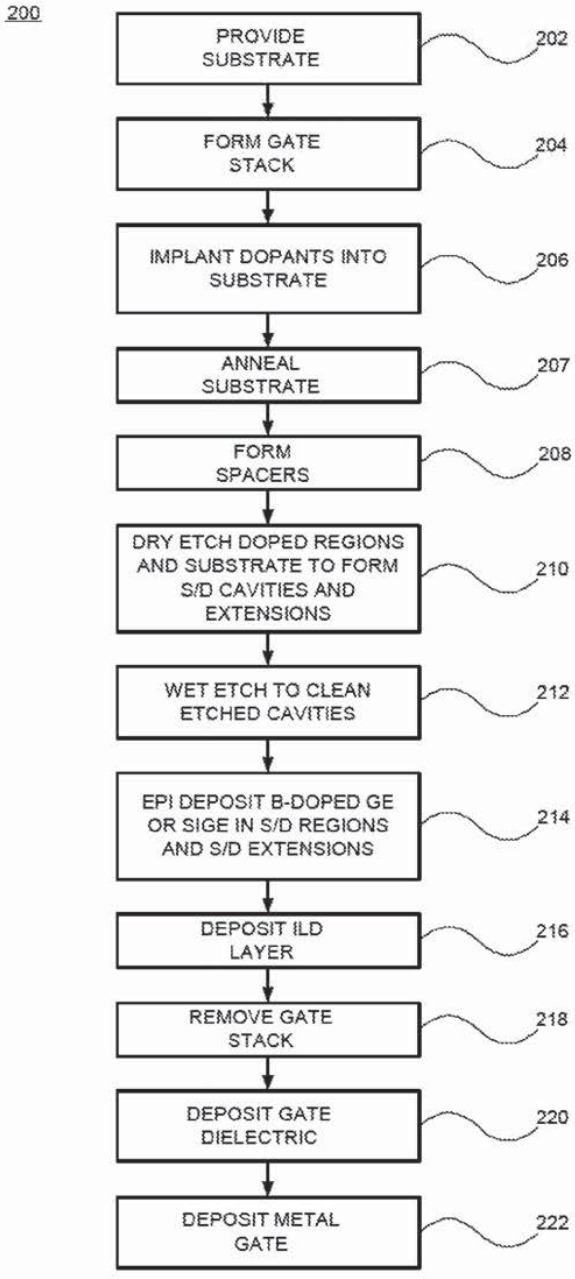

200
PROVIDE SUBSTRATE
202
FORM GATE STACK
204
IMPLANT DOPANTS INTO SUBSTRATE
206
ANNEAL SUBSTRATE
207
FORM SPACERS
208
DRY ETCH DOPED REGIONS AND SUBSTRATE TO FORM S/D CAVITIES AND EXTENSIONS
210
WET ETCH TO CLEAN ETCHED CAVITIES
212
EPI DEPOSIT B-DOPED GE OR SIGE IN S/D REGIONS AND S/D EXTENSIONS
214
DEPOSIT ILD LAYER
216
REMOVE GATE STACK
218
DEPOSIT GATE DIELECTRIC
220
DEPOSIT METAL GATE
222

FIG. 2

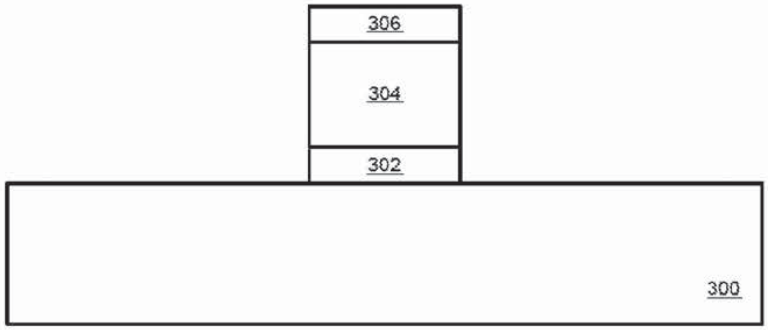


FIG. 3A

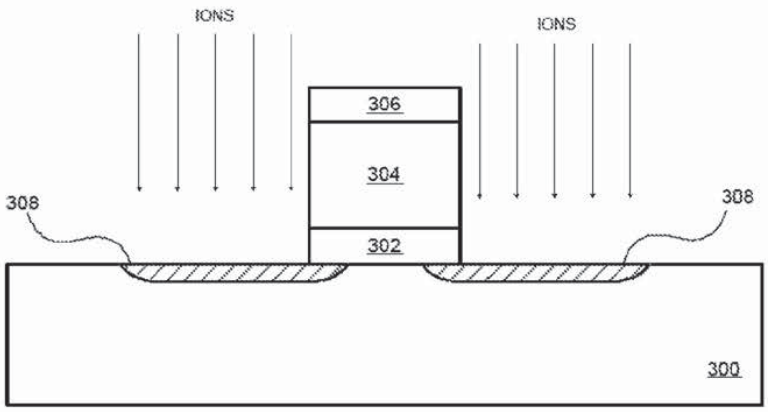


FIG. 3B

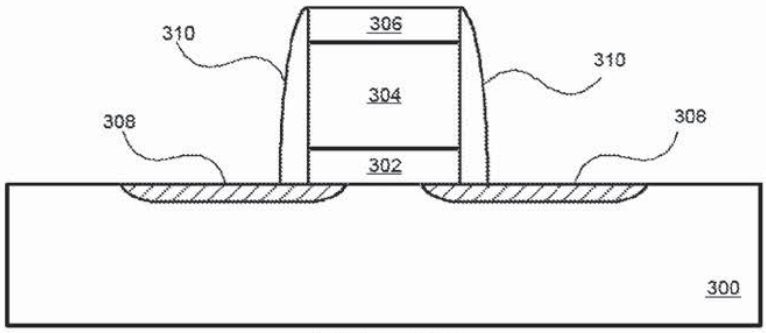

310
306
310
304
308
308
302
300

FIG. 3C

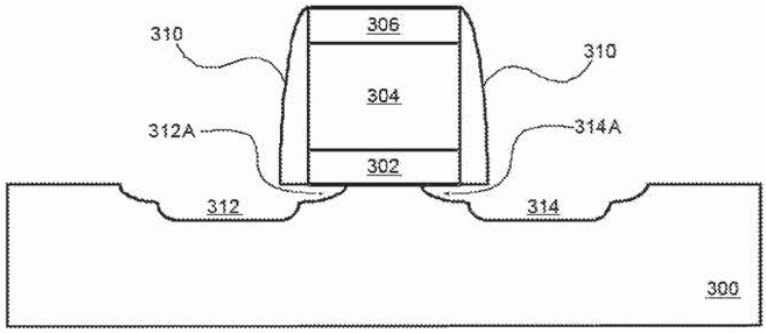

310
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310
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312A
314A
302
312
314
300

FIG. 3D

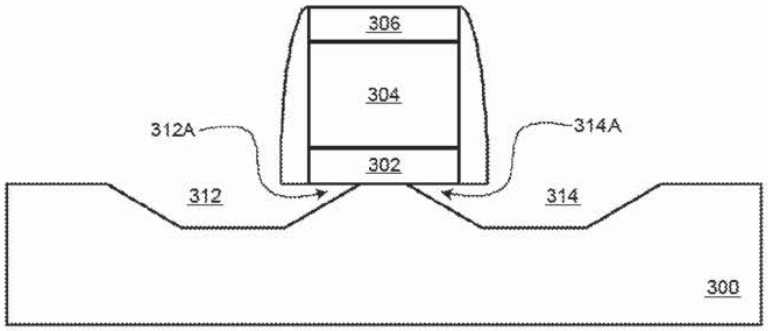


FIG. 3E

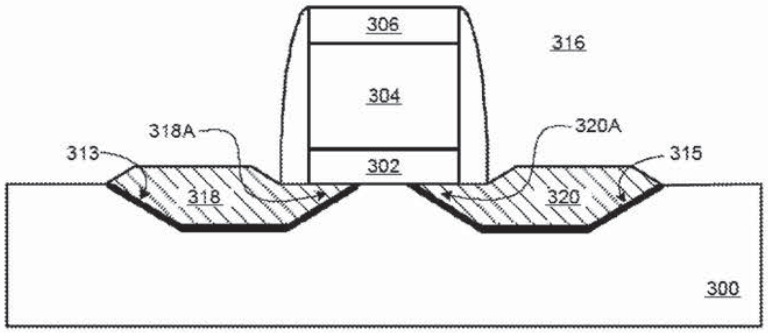


FIG. 3F

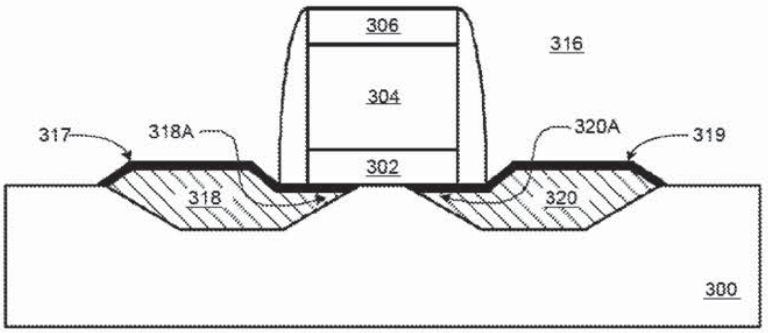


FIG. 3G

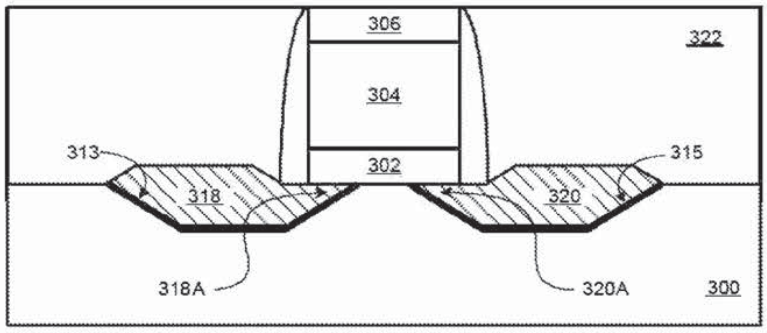


FIG. 3H

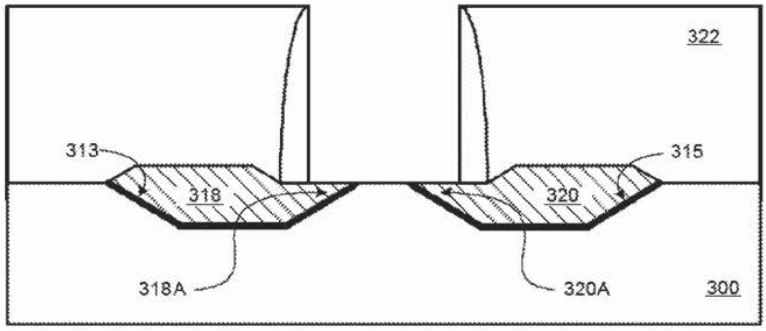


FIG. 3I

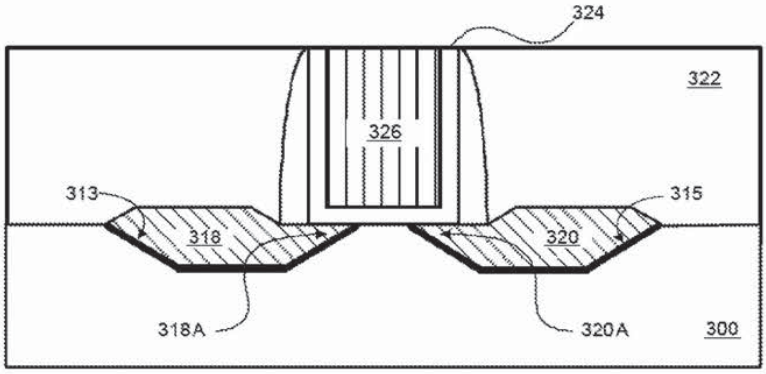


FIG. 3J

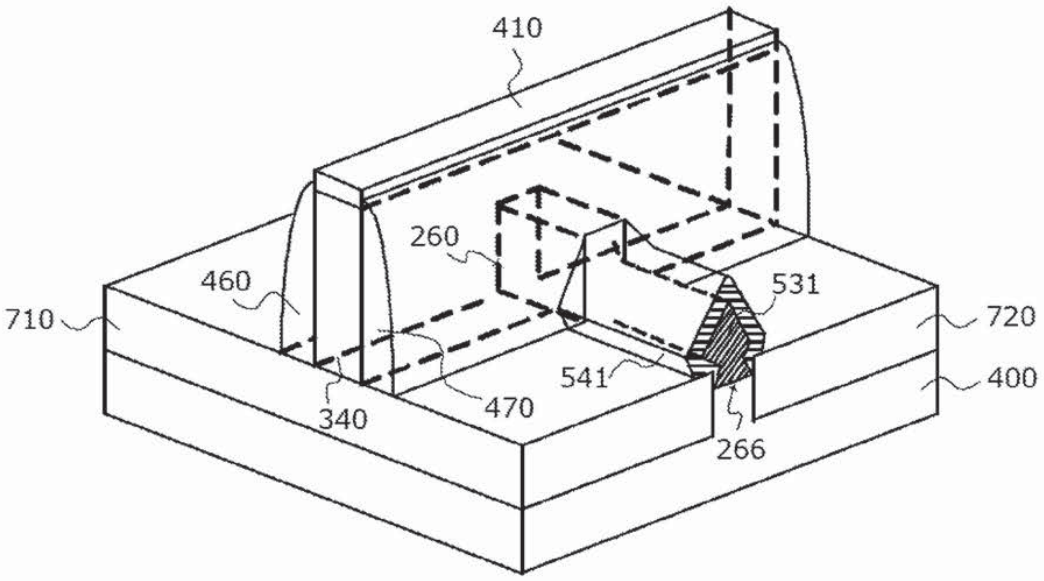


FIG. 4

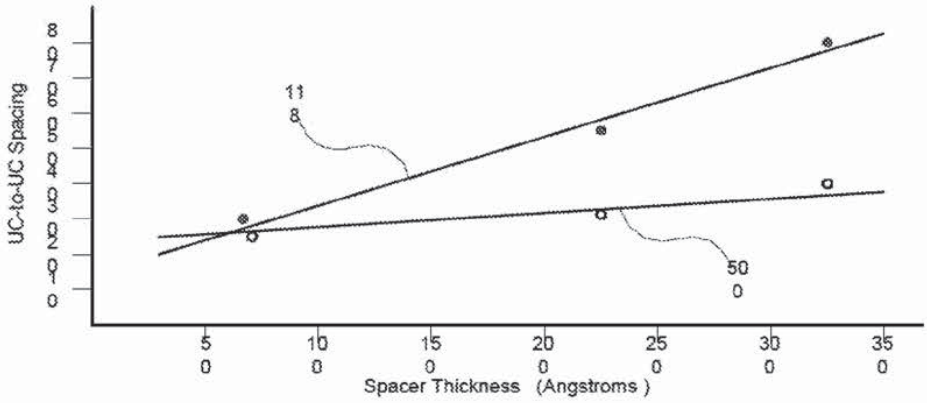

UC-to-UC Spacing
11
8
50
0
5
0
10
0
15
0
20
0
25
0
30
0
35
0
Spacer Thickness (Angstroms)

FIG. 5

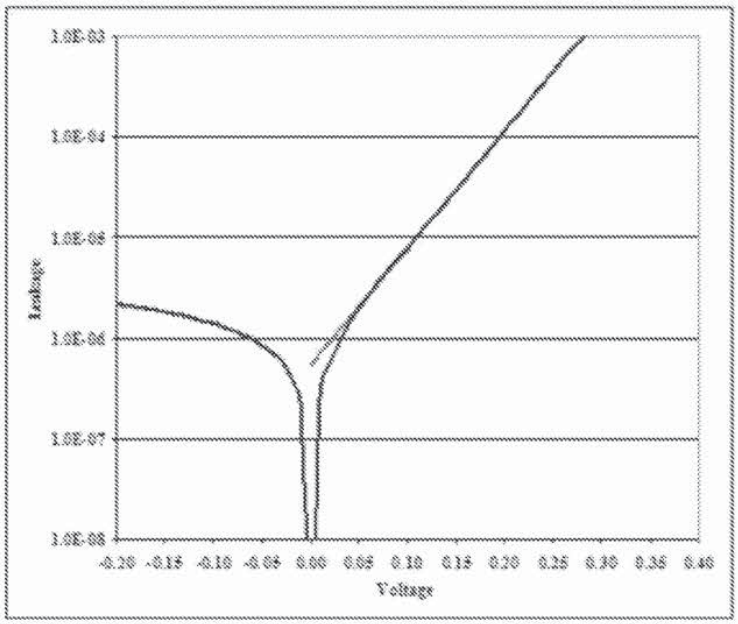

1.0E-03
1.0E-04
1.0E-05
1.0E-06
1.0E-07
1.0E-08
Leakage
-0.20 -0.15 -0.10 -0.05 0.00 0.05 0.10 0.15 0.20 0.25 0.30 0.35 0.40
Voltage

FIG. 6A

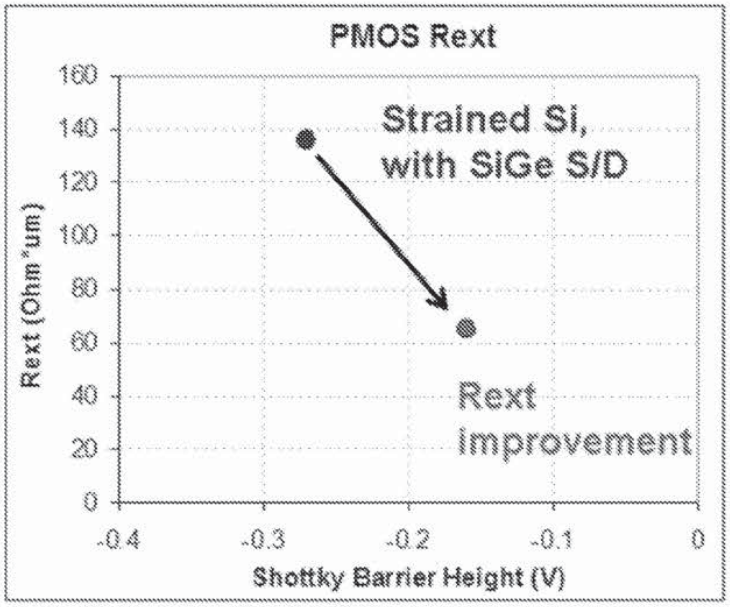

PMOS Rext
160
140
120
100
80
60
40
20
0
Rext (Ohm*um)
Strained Si,
with SiGe S/D
Rext
improvement
-0.4
-0.3
-0.2
-0.1
0
Shottky Barrier Height (V)

FIG. 6B

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P34115
	Application Number	
Title of Invention	TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
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Applicant Information:

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	Application Number	
Title of Invention	TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM	

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	Jack	T.		Kavalieros	
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Citizenship under 37 CFR 1.41(b)	US				

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P34115
	Application Number	
Title of Invention	TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM	

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Postal Code	97007	Country	US

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Email Address	nmaloney@finchmaloney.com	Add Email	Remove Email

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Application Information:

Title of the Invention	TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM		
Attorney Docket Number	P34115	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

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Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P34115
	Application Number	
Title of Invention	TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM	

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Application Number	Country[i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			(•) Yes ( ) No

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Assignee 1

If the Assignee is an Organization check here. ☐

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City		**State/Province**	
Country[i]		Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Neil F. Maloney/			Date (YYYY-MM-DD)	2010-12-21
First Name	Neil F.	Last Name	Maloney	Registration Number	42833

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TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM

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BACKGROUND

[0001] Increased performance of circuit devices including transistors, diodes, resistors, capacitors, and other passive and active electronic devices formed on a semiconductor substrate is typically a major factor considered during design, manufacture, and operation of those devices. For example, during design and manufacture or forming of, metal oxide semiconductor (MOS) transistor semiconductor devices, such as those used in a complementary metal oxide semiconductor (CMOS), it is often desired to increase movement of electrons in N-type MOS device (NMOS) channel regions and to increase movement of positive charged holes in P-type MOS device (PMOS) channel regions. Such increased drive current in the transistors can be achieved by reducing device resistance.

[0002] One method of reducing the overall resistance of a MOS device is to dope the area between the source/drain regions and the channel region, known as the tip regions (or sometimes as source/drain extensions) of a MOS device. For instance, a dopant may be implanted in the source/drain regions and a subsequent anneal may be carried out to diffuse the dopant towards the channel region. Because an implant and diffusion method is used, the ability to control the dopant concentration and location is limited. Furthermore, the size of other parts of a MOS device, such as the thickness of its offset spacers, can also have a great impact on the location of the tip regions. All of this, in turn, affects the ability of the tip regions to maximize dopant concentration and come into close proximity of the channel region. Accordingly, improved methods or structures are needed to overcome the limitations of conventional tip regions.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1A illustrates a conventional MOS device that includes source and drain tip regions formed using implantation and diffusion.

[0004] Figure 1B illustrates a MOS device that includes source and drain epitaxial tips configured in accordance with an embodiment of the present invention.

[0005] Figure 1C illustrates how spacer thickness can impact etching of epitaxial tips of a MOS device.

[0006] Figure 1D is a graph illustrating the dependence of UC-to-UC distance on spacer thickness.

[0007] Figure 2 is a method of forming source and drain epitaxial tips in accordance with an embodiment of the present invention.

[0008] Figures 3A to 3J illustrate structures that are formed when carrying out the method of Figure 2, in accordance with various embodiment of the present invention.

[0009] Figure 4 shows a perspective view of a FinFET transistor architecture, configured in accordance with one embodiment of the present invention.

[0010] Figure 5 is a graph illustrating how the UC-to-UC distance of a MOS device formed in accordance with an embodiment of the present invention is less dependent on spacer thickness.

[0011] Figure 6A illustrates Schottky barrier nickel germanide (NiGe) diode measurements, confirming that the NiGe workfunction is about 85 mV of the valance band edge, in accordance with some embodiments of the present invention.

[0012] Figure 6B plots simulation data that shows that such germanide materials provide a significant Rext improvement over that in conventional silicon germanium source/drain PMOS devices, in accordance with some embodiments of the present invention.

DETAILED DESCRIPTION

[0013] Techniques are disclosed for forming transistor devices having source and drain regions with high concentrations of boron doped germanium. The techniques can be used, for example, to extend self-aligned epitaxial tip (SET) transistors to achieve very near to the theoretical limit of uniaxial strain. In some embodiments, this is accomplished by use of an in situ boron doped germanium provided by selective epitaxial deposition in the source and drain regions as well as

their corresponding tip regions. In other embodiments, selective epitaxial deposition is used to form a bilayer construction of boron doped silicon germanium capped with a heavily boron doped germanium layer in the source/drain and respective tip regions. In such cases, the germanium concentration can be, for example, in the range of 20 atomic % to 100 atomic %, and the boron concentration can be, for instance, in the range of 1E20 cm^{-3} to 2E21 cm^{-3} (e.g., germanium concentration in excess of 50 atomic % and boron concentration in excess of 2E20 cm^{-3}). An optional thin buffer with graded germanium and/or boron concentration can be used as an interfacial layer to the underlying substrate material or materials with the layer of boron doped germanium. Likewise, in a bilayer configuration, a thin buffer with graded germanium and/or boron concentration can be used as an interfacial layer to the silicon germanium layer with the boron doped germanium cap. In still other embodiments, the boron doped germanium or silicon germanium layers themselves can have a graded germanium and/or boron concentration in a similar fashion as to the optional buffers. In any such case, since boron diffusion is suppressed in germanium (the higher the concentration, the greater the suppression), a high concentration of boron can be doped in the germanium, which in turn results in lower parasitic resistance and without degrading tip abruptness. In addition, the contact resistance is reduced from lowering of Schottky-barrier height. The techniques can be embodied, for instance, in planar or non-planar FinFET transistor devices.

General Overview

[0014] As is known, a metal oxide semiconductor (MOS) transistor may include source and drain tip regions that are designed to decrease the overall resistance of the transistor while improving short channel effects (SCE). Conventionally, these tip regions are portions of the substrate where a dopant such as boron or carbon is implanted using an implant and diffusion technique. The source tip region is formed in the area between the source region and the channel region. Likewise, the drain tip region is formed in the area between the drain region and the channel region. The tip regions resulting from such conventional processing minimally underdiffuse the gate dielectric layer of the transistor.

[0015] In more detail, Figure 1A illustrates a conventional MOS transistor 100A formed on a substrate 102. The source region 110 and the drain region 112 are typically formed by either implanting dopants such as boron into the substrate or by etching the substrate and then epitaxially depositing a silicon or silicon germanium material (with a germanium concentration

in the range of 10 to 40 atomic %). A gate stack 122 is formed over a channel region 120 of the transistor 100A. As can further be seen, the gate stack 122 includes a gate dielectric layer 106 and a gate electrode 104, and spacers 108 are formed adjacent to the gate stack 122. In some example cases, and depending on the technology node, the spacers 108 create a distance of about 10 to 20 nanometers (nm) between the edges of the gate dielectric layer 106 and the edges of each of the source and drain regions 110/112. It is within this space that a source tip region 110A and a drain tip region 112A are formed. As can be seen, the implantation-diffusion based tip regions 110A/112A overlap the spacers 108 and may also overlap or underdiffuse the gate dielectric layer 106 by a distance of less than 10 nm. In forming the implantation-diffusion based tip regions 110A/112A, a dopant such as boron or carbon is implanted into the source region 110 and the drain region 112. The transistor 100A is then annealed to cause the dopant to diffuse towards the channel region 120. Angled ion implantation techniques may also be used to further implant dopants into those areas between the gate dielectric layer 106 and the source/drain regions 110/112. Unfortunately, factors such as the shape of the tip regions 110A/112A, the distance the dopants penetrate below the spacers 108, and the concentration gradient of the tip regions 110A/112A are dependent on the diffusion properties of the dopant in the substrate material. For instance, the concentration of the tip regions will be high proximate to the source/drain region 110/112 and low proximate to the channel region 120. Although highly desired, it is nearly impossible to make the dopant concentration proximate to the channel region 120 very high without driving the dopant into the channel region 120. Furthermore, the source and drain regions 110/112 cannot be moved closer to the channel region 120 because the dopant may again be driven into the channel region 120. This limits how close the source and drain regions 110/112 can be formed to the channel region 120, thereby constraining gate length scaling.

[0016] Figure 1B illustrates an example MOS device 100B that includes source and drain epitaxial tips (generally referred to herein as epi-tips) configured in accordance with an embodiment of the present invention. In more detail, the MOS transistor 100B uses an undercut etch to allow the source region 110 and the drain region 112 to extend below the spacers 108, and in some cases, below the gate dielectric layer 106. The portions of the source/drain regions 110/112 that extend below the spacers 108 (and possibly the gate dielectric layer 106) are referred to herein as the source epi-tip 110B and the drain epi-tip 112B, respectively. The source

and drain epi-tips 110B/112B replace the implantation/diffusion based tip regions 110A/112A described with regard to Figure 1A.

[0017] In accordance with an embodiment of the present invention, the source/drain regions 110/112 and the source/drain epi-tips 110B/112B can be formed, for example, by etching the substrate 102, which includes undercutting the spacers 108 (and possibly the gate dielectric layer 106), and then using selective epitaxial deposition to provide an in situ boron doped germanium, or boron doped silicon germanium (SiGe) capped with heavily boron doped germanium, to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, as shown in Figure 1B. Note the epitaxial fill may be raised relative to the surface of substrate 102, as further shown in Figure 1B.

[0018] In accordance with some embodiments of the present invention, a graded buffer may be used in more or more locations of the structure, depending on factors such as the substrate composition and extent to which misfit dislocation is to be inhibited between disparate layers of the device structure. For instance, the substrate 102 can be a silicon substrate, or a silicon film of a silicon on insulator (SOI) substrate, or a multi-layered substrate comprising silicon, silicon germanium, germanium, and/or III-V compound semiconductors. Thus, and by way of example, in an embodiment having a silicon or silicon germanium substrate 102 and an in situ boron doped germanium is used to fill the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the underlying substrate 102 and the upper boron doped germanium. In such an embodiment, the buffer can be a graded boron doped (or intrinsic) silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying silicon substrate or silicon germanium substrate up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In one specific such embodiment, the germanium concentration ranges from 40 atomic % or less to in excess of 98 atomic %. The boron concentration within this buffer can be fixed, for example, at a high level or grade, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}, or 5E20 cm^{-3}). Note that compatibility as used herein does not necessitate an overlap in concentration levels (for instance, the germanium concentration of underlying substrate can be 0 to 20 atomic % and initial germanium concentration of the buffer can be 30 to 40 atomic %). In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a

relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level. The thickness of the buffer can vary depending on factors such as the range of concentrations being buffered, but in some embodiments is in the range of 30 to 120 Angstroms (Å), such as 50 to 100 Å (e.g., 60 Å or 65 Å). As will be appreciated in light of this disclosure, such a graded buffer beneficially lowers the Schottky-barrier height.

[0019] Alternatively, rather than using a thin buffer between the underlying substrate 102 and the upper boron doped germanium, the boron doped boron doped germanium layer itself can be graded in a similar fashion. For example, and in accordance with one example embodiment, the boron doped germanium layer can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic %. In some such embodiments, the boron concentration within this boron doped germanium layer can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}).

[0020] In other embodiments having a silicon or silicon germanium substrate 102 and a bi-layer structure of an in situ boron doped SiGe and boron doped germanium cap filling the source/drain regions 110/112 and the source/drain epi-tips 110B/112B, a buffer can be provided between the boron doped SiGe layer and the upper boron doped germanium cap. In one such embodiment, the boron doped SiGe layer has a fixed concentration of germanium (e.g., in the range of 30 to 70 atomic %) and the buffer can be a thin SiGe layer (e.g., 30 to 120 Å, such as 50 to 100 Å) having a germanium concentration graded from a base level concentration compatible with the underlying boron doped SiGe layer up to 100 atomic % (or near 100 atomic %, such as in excess of 90 atomic % or 95 atomic % or 98 atomic %). In some such cases, the boron concentration within this buffer can be fixed, for example, at a high level or can range, for example, from a base concentration at or otherwise compatible with the underlying SiGe layer up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}, 2E20 cm^{-3}, 3E20 cm^{-3}, 4E20 cm^{-3}, or 5E20 cm^{-3}).

[0021] Alternatively, rather than using a thin buffer between the two layers of the bilayer structure, the boron doped SiGe layer itself can be graded in a similar fashion. For example, and

in accordance with one example embodiment, the boron doped SiGe layer can be configured with a germanium concentration graded from a base level concentration compatible with the underlying substrate (e.g., in the range of 30 to 70 atomic %) up to 100 atomic % (or near 100 atomic %, as previously explained). The boron concentration within this boron doped SiGe layer can be fixed, for example, at a high level or can range, for example, from a base concentration at or otherwise compatible with the underlying substrate up to a desired high concentration (e.g., in excess of 1E20 cm^{-3}).

[0022] Thus, a SET architecture for planar and non-planar FinFET transistor devices is provided. The devices may be formed in part using conventional processes such as, for example, by dummy gate oxide, thin spacer, and an isotropic undercut etch (or an ammonia etch to form faceted fin recess in monocrystalline substrate, or other suitable etch to form fin recess). In accordance with some embodiments, selective epitaxial deposition can then be used to provide in situ boron doped germanium or alternatively, a fully strained boron doped silicon germanium layer capped with heavily boron doped pure germanium, to form both tips and source/drain regions. Optional buffers may be used as previously explained. With such embodiments, no P-type source and drain (PSD) implants or high temp diffusion-based anneals are required, since boron is fully active as deposited. Any suitable high-k replacement metal gate (RMG) process flow can also be used, where a high-k dielectric replaces the dummy gate oxide. Silicidation with, for example, nickel, nickel-platinum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. As previously explained, such embodiments extend SET transistor device architecture to achieve (near) theoretical limit of uniaxial strain. The techniques provided herein can be applied, for example, to benefit any technology nodes (e.g., 90nm, 65nm, 45nm, 32nm, 22nm, 14nm, and 10nm transistors, and lower), and the claimed invention is not intended to be limited to any particular such nodes or range of device geometries. Other advantages will be apparent in light of this disclosure.

[0023] For instance, note that the source and drain epi-tips 110B/112B configured in accordance with an embodiment of the present invention can be formed in the same process as the source and drain regions 110/112, which reduces process time. In addition, unlike conventional implantation/diffusion based tip regions, the lattice parameter of the source/drain epi-tips 110B/112B configured in accordance with an embodiment of the present invention

induces a strain in the channel region 120 that increases hole mobility and therefore decreases resistance in the channel. Another advantage of a SET architecture configured in accordance with some embodiments of the present invention is that the interface between the source/drain epi-tips 110B and 112B and the substrate material 102 that forms the channel region 120 is abrupt. For instance, on one side of the interface is the epitaxially deposited boron doped germanium (B:Ge) material (e.g., with B concentration in excess of 2E20 cm^{-3} or 5E20 cm^{-3}) and on the other side of the interface is the substrate material that makes up the channel region 120 (e.g., silicon germanium, or other suitable substrate material). This structure enables the epitaxial source/drain epi-tips 110B/112B to bring the heavily boron doped high concentration germanium material in very close proximity to the channel region 120. The boron in the epitaxial source/drain epi-tips 110B/112B remains substantially or completely within the epi-tips and does not tend to diffuse into the channel region 120.

[0024] Conventional methods that can be used in forming the source and drain epi-tips 110B/112B can have issues that should be considered. In particular, and with reference to Figures 1B and 1C, conventional undercut etching techniques may result in the formation of a bulleted profile for the undercut region. In such cases, more of the substrate material is etched a slight distance below the gate dielectric layer 106 than is etched directly adjacent to the gate dielectric layer 106. As such, the source epi-tip 110B and the drain epi-tip 112B each conform to that bulleted profile, which may produce a less than optimal strain in the channel region 120. Furthermore, variance in conventional undercut etching techniques can translate into a variance in the resulting source and drain epi-tips 110B/112B that are formed. Another issue with conventional methods of forming source and drain epi-tips 110B/112B concerns the effect that spacer thickness has on the undercut etch, as shown in Figures 1B and 1C. With reference to Figure 1B, the MOS transistor 100B is shown having offset spacers 108 of a first thickness x_1. A substrate etch has been performed that undercuts the spacers 108 and a portion of the gate dielectric layer 106 to enable the formation of source and drain epi-tips 110B/112B. An undercut-to-undercut (UC-to-UC) distance 114 separates source epi-tip 110B from drain epi-tip 112B. With reference to Figure 1C, a MOS transistor 100C is shown with offset spacers 108 having a thickness x_2. Here, the thickness x_2 is much greater than the thickness x_1 of the spacers 108 in Figure 1B. As a result, when the substrate etch is performed, the thicker spacers 108 push out the undercut etch and cause the source/drain epi-tips 110B/112B to be formed further away

from the channel region 120 of the transistor 100C. The substrate etch therefore undercuts less of the surface area beneath the MOS transistor 100C. Accordingly, a UC-to-UC distance 116 for the MOS transistor 100C is much larger than the UC-to-UC distance 114 for the MOS transistor 100B. Altering the UC-to-UC distance in this manner yields large drive current variations for MOS transistors. Figure 1D is a graph illustrating how spacer thickness affects the UC-to-UC distance in devices formed using known methods. The graph provides data, represented by line 118, showing that as spacer thickness increases, the UC-to-UC distance also increases, leading to large drive current variations. Typically, for every nanometer of spacer thickness increase, the UC-to-UC distance increases by around 2 nm. In this sense, forming source/drain epi-tips using conventional methods at least in some cases permits the thickness of the offset spacers to have a significant impact on the performance of the MOS device. As will be appreciated in light of this disclosure, some embodiments of the present invention provide methods of forming self-aligned and epitaxially deposited source and drain tips that address such issues.

Architecture and Methodology

[0025] Figure 2 is a method 200 of building a MOS transistor with self-aligned source and drain epi-tips, in accordance with an embodiment of the present invention. Figures 3A through 3J illustrate example structures that are formed as the method 200 is carried out, and in accordance with some embodiments.

[0026] As can be seen, the method 200 begins with providing 202 a semiconductor substrate upon which a MOS device, such as a PMOS transistor, may be formed. The semiconductor substrate may be implemented, for example, with a bulk silicon or a silicon-on-insulator configuration. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, such as germanium, silicon germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, or gallium antimonide. In a more general sense, any material that may serve as a foundation upon which a semiconductor device may be built can be used in accordance with embodiments of the present invention.

[0027] The method 200 continues with forming 204 a gate stack on the semiconductor substrate. The gate stack can be formed as conventionally done or using any suitable custom techniques. In some embodiments of the present invention, the gate stack may be formed by depositing and then patterning a gate dielectric layer and a gate electrode layer. For instance, in

one example case, a gate dielectric layer may be blanket deposited onto the semiconductor substrate using conventional deposition processes such as chemical vapor deposition (CVD), atomic layer deposition (ALD), spin-on deposition (SOD), or physical vapor deposition (PVD). Alternate deposition techniques may be used as well, for instance, the gate dielectric layer may be thermally grown. The gate dielectric material may be formed, for example, from materials such as silicon dioxide or high-k dielectric materials. Examples of high-k gate dielectric materials include, for instance, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some specific example embodiments, the high-k gate dielectric layer may be between around 5 Å to around 200 Å thick (e.g., 20 Å to 50 Å). In general, the thickness of the gate dielectric layer should be sufficient to electrically isolate the gate electrode from the neighboring source and drain contacts. In further embodiments, additional processing may be performed on the high-k gate dielectric layer, such as an annealing process to improve the quality of the high-k material. Next, a gate electrode material may be deposited on the gate dielectric layer using similar deposition techniques such as ALD, CVD, or PVD. In some such specific embodiments, the gate electrode material is polysilicon or a metal layer, although other suitable gate electrode materials can be used as well. The gate electrode material, which is typically a sacrificial material that is later removed for a replacement metal gate (RMG) process, has a thickness in the range of 50Å to 500Å (e.g., 100Å), in some example embodiments. A conventional patterning process may then be carried out to etch away portions of the gate electrode layer and the gate dielectric layer to form the gate stack, as shown in Figure 3A.

[0028] Figure 3A illustrates a substrate 300 upon which a gate stack is formed. As can be seen with this example embodiment, the gate stack includes a gate dielectric layer 302 (which may be high-k gate dielectric material) and a sacrificial gate electrode 304. In one specific example case, the gate stack includes a silicon dioxide gate dielectric layer 302 and a polysilicon gate electrode 304. The gate stack may also include a gate hard mask layer 306 that provides certain benefits or uses during processing, such as protecting the gate electrode 304 from subsequent ion implantation processes. The hard mask layer 306 may be formed using typical hard mask

materials, such as such as silicon dioxide, silicon nitride, and/or other conventional dielectric materials.

[0029] With further reference to Figure 2, after the gate stack is formed, the method 200 continues with an ion implantation process to highly dope portions of the substrate adjacent to the gate stack, by implanting 206 dopants into the substrate. The dopant used in the ion implantation process can be chosen, for example, based on its ability to increase the etch rate of the substrate material in which it is implanted, and the specific dopant selected for the ion implantation process may vary based on the substrate material(s) and the etchant used in a subsequent etching process. Specific dopants that may be selected to increase the etch rate of the substrate include, for example, carbon, phosphorous, and arsenic. For instance, carbon may be used at a dosage that ranges from 1×10^{14} to 1×10^{16} atoms/cm^3 using an implantation energy that falls between 5 and 15 kilo-electron volts (keV). Phosphorous may be used at a dosage that ranges from 1×10^{14} to 5×10^{15} atoms/cm^3 using an implantation energy that falls between 1 and 5 keV. Arsenic may be used at a dosage that ranges from 1×10^{14} to 5×10^{15} atoms/cm^3 using an implantation energy that falls between 2 and 5 keV. Other suitable dopants and dosage schemes will be apparent in light of this disclosure. In some embodiments, the ion implantation substantially occurs in a vertical direction (i.e., a direction perpendicular to substrate); while in other embodiments at least a portion of the ion implantation process occurs in an angled direction to implant ions below the gate stack. Note that the hard mask 306 can be used to prevent doping of the gate electrode 304 material.

[0030] Next, the method 200 continues with annealing 207 the substrate to drive the dopants further into the substrate and to reduce any damage sustained by the substrate during the ion implantation process. In some embodiments, the implanting 206 and subsequent annealing 207 may drive the ions to a substrate depth that falls, for example, between 2 nm and 20 nm. The annealing 207 may be carried out at a temperature that falls, for example, between 700°C and 1100°C for a time duration of up sixty seconds or less (e.g., five seconds). As will be appreciated, the annealing temperature and duration can vary from one embodiment to the next, depending on factors such as the diffusion rate, substrate material, dopant used, and desired end dopant concentration.

[0031] Figure 3B illustrates the substrate 300 after the ion implantation and diffusion process. As shown in this example embodiment, the ion implantation process creates two doped regions

308 adjacent to the gate dielectric layer 302, for the MOS transistor being formed. When exposed to an appropriate etchant, the doped regions 308 will have an etch rate that is higher than the etch rate of the surrounding substrate material. One of the doped regions 308 will serve as a portion of a source region, including its self-aligned epi-tip. The other doped region 308 will serve as a portion of a drain region, including its self-aligned epi-tip. In the example embodiment shown, portions of the doped regions 308 are sited below the gate dielectric layer 302. Note that the size of the doped regions 308, including their depth, may vary based on the requirements of the MOS transistor being formed.

[0032] Next, the method 200 continues with forming 208 spacers on either side of the gate stack. The spacers may be formed, for example, using conventional materials such as silicon oxide, silicon nitride, or other suitable spacer materials. The width of the spacers may generally be chosen based on design requirements for the MOS transistor being formed. In accordance with some embodiments, however, the width of the spacers is not subject to design constraints imposed by the formation of the source and drain epi-tips. Figure 3C illustrates the substrate 300 with spacers 310 formed on either side of the gate electrode layer 304 and the gate dielectric layer 302, in accordance with an example embodiment.

[0033] With further reference to Figure 2, the method 200 continues with dry etching 210 the doped regions of the substrate to form cavities in which source/drain regions including their respective epi-tips may be formed. As best seen with reference to Figure 3D, the etched cavities are generally adjacent to the gate stack, and the epi-tip areas are effectively extensions of the source/drain cavity regions. In some example embodiments, the etched cavities may be formed to a depth that falls between 50 nm and 1500 nm, which can be deeper than the doped regions. In a more general sense, the etch depth can be set as needed, based on desired MOS device performance. In some embodiments, the dry etch process can use an etchant recipe that complements the dopant used in the ion implantation process to increase the etch rate of the doped regions, thereby enabling the etching process to remove substrate material from the doped regions at a faster rate than the remainder of the substrate 300. In some embodiments, this includes portions of the doped regions that undercut the spacers 310 and the gate dielectric layer 302, thereby defining the self-aligned tip architecture of the transistor. Increasing the etch rate of the doped regions enables the etched source and drain tip cavities to undercut the spacers 310 and the gate dielectric layer 302 without the UC-to-UC distance being substantially impacted by

factors such as the thickness of the spacers, variations in the dry etch process, and other process variations.

[0034] In accordance with some embodiments, the dry etch process may use a chlorinated chemistry that takes place in a plasma reactor. In some specific such embodiments, the etchant recipe may include a combination of NF_3 and Cl_2 with argon or helium used as a buffer or carrier gas. In accordance with some such embodiments, the flow rate for the active etchant species may vary, for example, between 50 and 200 standard cubic centimeters per minute (SCCM) while the flow rate of the carrier gas may vary, for example, between 150 and 400 SCCM. A high energy plasma may be employed at a power that ranges, for instance, from 700W to 1100W with a low RF bias of less than 100W, in accordance with some such embodiments. The reactor pressure may range from around 1 pascal (Pa) to around 2 Pa, in accordance with some such embodiments. In another specific example embodiment, the etchant chemistry may include a combination of HBr and Cl_2. In some such embodiments, the flow rate for the etchant species may vary, for example, between 40 SCCM and 100 SCCM. A high energy plasma may be employed at a power that ranges from around 600W to around 1000W with a low RF bias of less than 100W, and the reactor pressure may range from around 0.3 Pa to around 0.8 Pa, in accordance with some such embodiments. In yet another example embodiment, the etchant chemistry may include a combination of Ar and Cl_2. In some such embodiments, the flow rate for the etchant species may vary, for example, between 40 SCCM and 80 SCCM. A medium energy plasma may be employed at a power that ranges from around 400W to around 800W with a high RF bias of between around 100W and 200W, and the reactor pressure may range from around 1 Pa to around 2 Pa, in accordance with some such embodiments. The dry etch process times for each of these example embodiments may be, for example, up to 60 seconds per substrate, but can vary depending factors such as desired etch depth and etchant. Such etch process parameters may vary, as will be appreciated.

[0035] Figure 3D illustrates the substrate 300 after the dry etch process has been carried out, in accordance with some embodiments of the present invention. As shown, a source region cavity 312 and a drain region cavity 314 are formed. In addition, a source tip cavity 312A and a drain tip cavity 314A have been formed as extensions of cavities 312 and 314, respectively, by the etching 210 of the doped regions as previously discussed. Note that the thickness of the spacers 310 has minimal impact on the etching of the source tip cavity 312A and the drain tip cavity

314A due to the use of dopants and etchant recipes that increase the etch rate of the doped regions during etching 210.

[0036] After the dry etch process has completed, and with further reference to Figure 2, the method of this example embodiment continues with wet etching 212 to clean and further etch the source region cavity 312 and its source epi-tip cavity 312A, as well as the drain region cavity 314 and its drain epi-tip cavity 314A. The wet etching 212, which can be carried out using conventional or custom wet etch chemistries, can be used to remove contaminants such as carbon, fluorine, chlorofluorocarbons, and oxides such as silicon oxide to provide a clean surface upon which subsequent processes may be carried out. In addition, and assuming a monocrystalline silicon substrate, the wet etching 212 may also be used to remove a thin portion of the substrate along the <111> and <001> crystallographic planes to provide a smooth surface upon which a high quality epitaxial deposition may occur. In some example cases, the thin portion of the substrate that is etched away may be, for example, up to 5 nm thick and may also remove residual contaminants. As best shown in Figure 3E, the wet etching 212 causes edges of the source region cavity 312 and its epi-tip region 312A, as well as the drain region cavity 314 its epi-tip region 314A to follow the <111> and <001> crystallographic planes. Further note that the source and drain epi-tip regions 312A and 314A do not have the bulleted profile that occurs in conventional processing.

[0037] After the wet etch process has completed, and with further reference to Figure 2, the method 200 continues with epitaxially depositing 214 in the source/drain and respective tip cavities either an in situ boron doped germanium (with an intervening thin buffer in some cases), or boron doped silicon germanium capped with a heavily boron doped germanium layer. This epitaxial deposition fills the source and drain cavities including their respective epi-tip regions in one process, in accordance with some embodiments. A CVD process or other suitable deposition technique may be used for the depositing 214. For example, the depositing 214 may be carried out in a CVD reactor, an LPCVD reactor, or an ultra high vacuum CVD (UHVCVD). In some example cases, the reactor temperature may fall, for instance, between 600°C and 800°C and the reactor pressure may fall, for instance, between 1 and 760 Torr. The carrier gas may include, for example, hydrogen or helium at a suitable flow rate, such as between 10 and 50 SLM. In some specific embodiments, the deposition may be carried out using a germanium source precursor gas such as GeH_4 that is diluted in H_2 (e.g., the GeH_4 may be diluted at 1-5%). For instance, the

diluted GeH_4 may be used at a 1% concentration and at a flow rate that ranges between 50 and 300 SCCM. For an in situ doping of boron, diluted B_2H_6 may be used (e.g., the B_2H_6 may be diluted in H_2 at 1-5%). For instance, the diluted B_2H_6 may be used at a 3% concentration and at a flow rate that ranges between 10 and 100 SCCM. In some example cases, an etching agent may be added to increase the selectivity of the deposition. For instance, HCl or Cl_2 may be added at a flow rate that ranges, for example, between 50 and 300 SCCM.

[0038] In accordance with some example embodiments of the present invention, and as best shown in Figure 3F, the source and drain region cavities 312/314 along with their respective tip regions 312A/314A are filled with in situ boron doped germanium, thereby forming source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A) of a MOS transistor 316 in substrate 300. In some such embodiments, the boron doped germanium has a boron concentration in excess of 5E20 cm^{-3}, such as 2E21 cm^{-3} or higher. The thickness of the boron doped germanium deposited layer may range, for example, from 50 to 500 nm (e.g., 120 nm), in accordance with some specific embodiments, although other layer thicknesses will be apparent in light of this disclosure. As previously explained, some such embodiments may include with a thin buffer between the pure germanium layer and the substrate. For instance, and as can further be seen in the example embodiment shown in Figure 3F, a source buffer 313 and a drain buffer 315 are deposited prior to depositing the in situ boron doped germanium. In some such embodiments, the buffers 313 and 315 can be a graded boron doped silicon germanium layer with the germanium composition graded from a base level concentration compatible with the underlying substrate 300 material up to 100 atomic % (or near to 100 atomic % as previously described). The thickness of the buffers 313 and 315 will vary depending on factors such as the concentration range over which the buffer transitions and the make-up of the underlying substrate 300. In one example embodiment having a silicon germanium substrate, the buffer thickness ranges from 2 nm to 10 nm, although other suitable thicknesses can be used also. In one specific such embodiment, the boron concentration within the buffers 313 and 315 can range, for example, from a base concentration compatible with the underlying silicon germanium substrate up to a desired concentration (e.g., in excess of 1E20 cm^{-3} and up to 2E21 cm^{-3}), with two specific embodiments being in excess of 2E20 cm^{-3} or in excess of 5E20 cm^{-3}. In a more general sense, the boron concentration can be adjusted as necessary to provide the desired degree of conductivity, as will be appreciated in light of this disclosure.

[0039] In accordance with other example embodiments of the present invention, and as best shown in Figure 3G, the source and drain region cavities 312/314 along with their respective tip regions 312A/314A are filled with in situ boron doped silicon germanium to form source region 318 (along with epi-tip 318A) and drain region 320 (along with drain epi-tip 320A) of MOS transistor 316 in substrate 300. The boron doped silicon germanium fill is then capped with a heavily boron doped germanium layer, to provide source cap 317 and drain cap 319. In some such bilayer construction embodiments, the boron doped silicon germanium fill, which may be epitaxially deposited in one or more layers, has a germanium concentration in the range of 30 to 70 atomic %, or higher. As previously explained, this germanium concentration of the SiGe fill may be fixed or graded so as to increase from a base level (near substrate 300) to a high level (e.g., in excess of 50 atomic %, near the pure germanium cap 317/319). The boron concentration in some such embodiments can be in excess of 1E20 cm^{-3}, such as higher than 5E20 cm^{-3} or 2E21 cm^{-3}, and may also be graded so as to increase from a base level near substrate 300 to a high level (e.g., in excess of 1E20 cm^{-3} or 2E20 cm^{-3} or 3E20 cm^{-3}, etc, near cap 317/319). In embodiments where the germanium concentration of the boron doped SiGe layer is fixed, a thin graded buffer may be used to better interface the boron doped SiGe layer with the boron doped Ge cap, as previously explained. The thickness of the boron doped SiGe deposited layer (or collection of layers) 318/320 may range, for example, from 50 to 250 nm (e.g., 60 nm), and the pure germanium cap 317/319 may have a thickness in the range, for example, of 50 to 250 nm (e.g., 50 nm), in accordance with some specific embodiments, although alternative embodiments may have other layer and cap thicknesses, as will be apparent in light of this disclosure. In some embodiments, note that cavities may be created underneath the spacers during cyclical deposition-etch processing, and those cavities can be backfilled by an epitaxial cap layer as well (which can have, for example, the same composition as the boron doped germanium cap 317/319).

[0040] As will further be appreciated in light of this disclosure, the combination of high germanium concentration (e.g., in excess of 50 atomic % and up to pure germanium) and high boron concentration (e.g., in excess of 1E20 cm^{-3}), such as discussed with respect to embodiments shown in Figures 3F and 3G, can be used to realize significantly higher conductance in the source and drain regions as well as their respective tip regions in PMOS SET transistor devices. Further, and as previously explained, since boron diffusion is sufficiently

suppressed by pure germanium, no adverse SCE degradation is realized with subsequent thermal anneals despite high boron in the deposited stressor film. Barrier height lowering is also enabled from the higher concentration of germanium at the contact surface. In some example embodiments, a germanium concentration in excess of 95 atomic % and up to pure germanium (100 atomic %) can be used to achieve such benefits.

[0041] As further shown in Figures 3F and 3G, unlike conventional source and drain tip regions that are formed through implant and diffusion techniques and therefore have no clear boundary between the tip regions and the channel region, the self-aligned source and drain epi-tips of the MOS transistor 316 have an abrupt boundary. In other words, the interface between the source/drain epi-tips and the channel region is clear and well-defined. On one side of the interface is the heavily boron doped germanium layer (layer 318/320 of Figure 3F or cap 317/319 of Figure 3G) and on the other side of the interface is the substrate 300 material that makes up the channel region. The boron in the source/drain epi-tips 318A/320A remains substantially or completely within the epi-tips and does not tend to diffuse into the channel region, thereby enabling the heavily boron doped germanium material in very close proximity to the channel region relative to conventional techniques. For instance, in some specific embodiments, the source/drain epi-tips 318A/320A may undercut the gate dielectric layer 302 by more than 10 nm. This in turn enables the gate length to be scaled down without having to shorten the channel region.

[0042] Forming the source and drain epi-tips in relatively close proximity to the channel region also imparts a larger hydrostatic stress on the channel. This stress increases the strain within the channel, thereby increasing mobility in the channel and increasing drive current. This stress can be further amplified by increasing the germanium concentration of the source and drain epi-tips. This is an improvement over diffusion-based processes where the tip regions generally do not induce a strain on the channel region.

[0043] Once the source and drain regions are filled in accordance with an embodiment of the present invention, various conventional MOS processing can be carried out to complete fabrication of MOS transistor 316, such as replacement gate oxide processes, replacement metal gate processes, annealing, and salicidation processes, that may further modify the transistor 316 and/or provide the necessary electrical interconnections. For instance, after the epitaxial deposition of the source/drain regions along with their respective tips, and with further reference

to Figure 2, the method 200 may continue with depositing 216 an interlayer dielectric (ILD) over the transistor 316, and then planarizing the ILD layer as commonly done. The ILD layer may be formed using materials known for the applicability in dielectric layers for integrated circuit structures, such as low-k dielectric materials. Such dielectric materials include, for example, oxides such as silicon dioxide (SiO_2) and carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. In some example configurations, the ILD layer may include pores or other voids to further reduce its dielectric constant. Figure 3H illustrates an example ILD layer 322 that has been deposited and then planarized down to the hard mask 306.

[0044] Next, in some embodiments of the present invention where a replacement metal gate process is used, the method 200 continues with removing 218 the gate stack (including the high-k gate dielectric layer 302, the sacrificial gate electrode 304, and the hard mask layer 306) using an etching process as conventionally done. In alternate implementations, only the sacrificial gate 304 is removed. Figure 3I illustrates the trench opening that is formed when the gate stack is etched away, in accordance with one such embodiment. If the gate dielectric layer is removed, the method may continue with depositing 220 a new gate dielectric layer into the trench opening. Any suitable high-k dielectric materials such as those previously described may be used here, such as hafnium oxide. The same deposition processes may also be used. Replacement of the gate dielectric layer may be used, for example, to address any damage that may have occurred to the original gate dielectric layer during application of the dry and wet etch processes, and/or to replace a low-k or sacrificial dielectric material with a high-k or otherwise desired gate dielectric material.

[0045] The method 200 may then continue with depositing 222 the metal gate electrode layer into the trench and over the gate dielectric layer. Conventional metal deposition processes may be used to form the metal gate electrode layer, such as CVD, ALD, PVD, electroless plating, or electroplating. The metal gate electrode layer may include, for example, a P-type workfunction metal, such as ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. In some example configurations, two or more metal gate electrode layers may be deposited. For instance, a workfunction metal may be deposited followed by a suitable metal gate electrode fill metal such as aluminum. Figure 3J illustrates an example high-k gate

dielectric layer 324 and a metal gate electrode 326 that have been deposited into the trench opening, in accordance with one embodiment.

[0046] Metalization of the source and drain contacts can be carried out using a silicidation process (generally, deposition of contact metal and subsequent annealing). For instance, silicidation with nickel, aluminum, nickel-platinum or nickel-aluminum or other alloys of nickel and aluminum, or titanium with or without germanium pre-amorphization implants can be used to form a low resistance germanide. The boron doped germanium epi layer allows for metal-germanide formation (e.g., nickel-germanium). The germanide allows for significantly lower Schottky-barrier height and improved contact resistance (including Rext) over that in conventional metal-silicide systems. For instance, conventional transistors typically use a source/drain SiGe epi process, with germanium concentration in the range of 30-40 atomic %. Such conventional systems exhibit Rext values of about 140 Ohm*um, limited by epi/silicide interfacial resistance, which is high and may impede future gate pitch scaling. Some embodiments of the present invention allow for a significant improvement in Rext in PMOS devices (e.g., about a 2x improvement, or a Rext of about 70 Ohm*um), which can better support PMOS device scaling. Thus, transistors having a source/drain configured with heavily boron doped germanium in accordance with an embodiment of the present, with a boron concentration in excess of 1E20 cm^{-3} and a germanium concentration in excess of 50 atomic % and up to or otherwise near pure germanium (100 atomic %) at the interface between the source/drain epi-tips and the channel region, can exhibit Rext values of less than 100 Ohm*um, and in some cases less than 90 Ohm*um, and in some cases less than 80 Ohm*um, and in some cases less than 75 Ohm*um, or lower.

[0047] Accordingly, self-aligned source and drain epi-tips have been disclosed that reduce the overall resistance of the MOS transistor and increase channel strain due to increased boron doped germanium volume (e.g., boron doped germanium or boron doped silicon germanium volume with a germanium cap). In some such embodiments, the source and drain epi-tips do not have a bulleted profile, form an abrupt boundary between the channel region and the source and drain regions, and/or have a doping concentration that is more readily controlled, yielding a more optimized source-drain profile. Furthermore, by selecting an appropriate combination of a dopant and an etchant recipe in accordance with some embodiments, the source and drain epi-tips can be etched without being substantially impacted by the spacer thickness. This self-

aligned process can therefore be used to increase performance while minimizing process variation, where desirable to do so.

FinFET Configuration

[0048] As is known, FinFET is a transistor built around a thin strip of semiconductor material (generally referred to as the fin). The transistor includes the standard field effect transistor (FET) nodes, including a gate, a gate dielectric, a source region, and a drain region. The conductive channel of the device resides on the outer sides of the fin beneath the gate dielectric. Specifically, current runs along both sidewalls of the fin (sides perpendicular to the substrate surface) as well as along the top of the fin (side parallel to the substrate surface). Because the conductive channel of such configurations essentially resides along the three different outer, planar regions of the fin, such a FinFET design is sometimes referred to as a tri-gate FinFET. Other types of FinFET configurations are also available, such as so-called double-gate FinFETs, in which the conductive channel principally resides only along the two sidewalls of the fin (and not along the top of the fin).

[0049] Figure 4 shows a perspective view of an example tri-gate architecture, configured in accordance with one embodiment of the present invention. As can be seen, the tri-gate device includes a substrate 400 having a semiconductor body or fin 260 (represented by dashed lines) extending from the substrate 400 through isolation regions 710, 720. A gate electrode 340 is formed over 3 surfaces of the fin 260 to form 3 gates. A hard mask 410 is formed on top of the gate electrode 340. Gate spacers 460, 470 are formed at opposite sidewalls of the gate electrode 340. A source region comprises the epitaxial region 531 formed on a recessed source interface 266 and on one fin 260 sidewall, and a drain region comprises the epitaxial region 531 formed on a recessed source interface 266 and on the opposing fin 260 sidewall (not shown). A cap layer 541 is deposited over the epitaxial regions 531. In one embodiment, the isolation regions 710, 720 are shallow trench isolation (STI) regions formed by common techniques, such as etching the substrate 200 to form trenches, and then depositing oxide material onto the trenches to form the STI regions. The isolation regions 710, 720 can be made from any well known insulative material, such as SiO_2. The previous discussion with respect to the substrate 102 is equally applicable here (e.g., substrate 400 may be a silicon substrate, or SOI substrate, or a multi-layered substrate).

[0050] As will be appreciated in light of this disclosure, conventional processes and forming techniques can be used to fabricate the tri-gate transistor structure. However, and in accordance with one example embodiment of the present invention, the bilayer structure of the epitaxial region 531 and cap layer 541 can be implemented using an in situ boron doped silicon germanium capped with a heavily boron doped germanium, with an optional germanium and/or boron graded buffer between the two bilayers. As previously explained, such a buffer may be used to transition from a base level germanium/boron concentration compatible with the boron doped SiGe deposited for epitaxial region 531 in the recessed source interface 266 to the heavily boron doped germanium cap 541. Alternatively, germanium and/or boron concentration grading can be implemented directly in the epitaxial region 531, rather than in an intervening graded buffer arrangement. As will further be appreciated, note that an alternative to the tri-gate configuration is a double-gate architecture, which includes a dielectric/isolation layer on top of the fin 260.

[0051] Figure 5 is a graph illustrating an improvement made available by using self-aligned source and drain epi-tips configured in accordance with one example embodiment of the present invention. Line 500 represents data collected for MOS devices built using techniques provided herein. As shown, the UC-to-UC distance is much less impacted by spacer thickness than devices formed using conventional processes, the data for which is again represented by line 118. Figures 6A and 6B further demonstrate improvements enabled by using self-aligned source and drain epi-tips configured in accordance with one example embodiment of the present invention. In particular, Figure 6A illustrates Schottky barrier NiGe diode measurements (leakage v. voltage), confirming that the nickel-germanium workfunction is very p-type (roughly 85 mV above the Ge valance band). Figure 6B plots simulation data that shows that such germanide materials and Schottky barrier height improvement enables more than a 2x Rext improvement over that in conventional SiGe source/drain PMOS devices, in accordance with some example embodiments of the present invention. As is known, the Schottky barrier height is the rectifying barrier for electrical conduction across a semiconductor-metal junction. The magnitude of the Schottky barrier height reflects a mismatch in the energy position of the metal's Fermi level and the majority carrier band edge of the semiconductor across the semiconductor-metal interface. For a p-type semiconductor-metal interface, the Schottky barrier height is the difference between the metal Fermi level and the valence band maximum of the semiconductor.

[0052] Thus, and as will be appreciated in light of this disclosure, various embodiments of the present invention provided herein can be used to address several transistor scaling issues, such as providing for higher channel mobility with pitch and power supply (Vcc) scaling, providing reduced source/drain and contact resistance, providing for improved channel abruptness, providing reduced barrier height between salicide and source/drain to minimize overall parasitic resistance, particularly in planar and non-planar architectures. Numerous embodiments will be apparent in light of this disclosure.

[0053] One example embodiment of the present invention provides a transistor device. The device includes a substrate having a channel region. The device further includes a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}. In one such case, the device is one of a planar or FinFET PMOS transistor. In another such case, the device may include metal-germanide source and drain contacts. In another such case, the device may include an interlayer dielectric over the source and drain regions. In another such case, the device may include a buffer between the substrate and the boron doped germanium layer. In one such specific case, the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %. In another such specific case, the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another particular embodiment, the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon. In one such specific case, the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %. In another such specific case, the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration

compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In another such specific case, the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}. In another particular case, the transistor has a Rext value of less than 100 Ohm*um (such as Rext = 70 Ohm*um, +/-10%). As will be appreciated, the boron concentration can be set higher based on factors such as desired conductivity, and in some such example cases is in excess of 2E20 cm^{-3} or 3E20 cm^{-3} or 4E20 cm^{-3} or 5E20 cm^{-3} 2E21 cm^{-3}.

[0054] Another embodiment of the present invention provides a transistor device. In this example case, the device includes a substrate having a channel region and a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The device further includes source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 2E20 cm^{-3}. The device further includes metal-germanide source and drain contacts. In some such cases, the device may further include a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In other example cases, the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon. In some such specific cases, the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a

germanium concentration in excess of 95 atomic %. In some such specific embodiments, the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}. In other specific cases, the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a thin buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

[0055] Another embodiment of the present invention provides a method for forming a transistor device. The method includes providing a substrate having a channel region, and providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode. The method continues with forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}. In some such embodiments, the method further includes providing a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}. In other embodiments, the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon. In one such case, the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %. In another such case, the boron doped silicon germanium portion has a fixed

germanium concentration, and the method further includes providing a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm-3. In some such cases, the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

[0056] The foregoing description of example embodiments of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many modifications and variations are possible in light of this disclosure. For instance, while some embodiments of the present invention utilize in situ boron doping of germanium, other embodiments may use an intrinsic germanium that after its deposition is subsequently subjected to boron implantation and annealing processes to provide the desired boron doping concentration. Moreover, some embodiments may include source and drain regions fabricated as described herein (e.g., having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}), but still use conventional processing (e.g., implantation and annealing) to form the tips of the source and drain regions. In such embodiments, the tips may have a lower germanium and/or boron concentration than the main source/drain region, which may be acceptable in some applications. In still other embodiments, only tips of the source and drain regions may be configured with the high germanium and boron concentrations and the main portions of the source and drain regions may have conventional or otherwise lower germanium/boron concentrations. It is intended that the scope of the invention be limited not by this detailed description, but rather by the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}.

2. The device of claim 1 wherein the device is one of a planar or FinFET PMOS transistor.

3. The device of claim 1 further comprising metal-germanide source and drain contacts.

4. The device of claim 1 further comprising an interlayer dielectric over the source and drain regions.

5. The device of claim 1, the device further comprising:

a buffer between the substrate and the boron doped germanium layer.

6. The device of claim 5 wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %.

7. The device of claim 6 wherein the high concentration reflects pure germanium.

8. The device of claim 5 wherein the buffer has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

9. The device of claim 1 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

10. The device of claim 9 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

11. The device of claim 9 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

12. The device of claim 9 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}.

13. The device of claim 9 wherein the transistor has a Rext value of less than 100 Ohm*um.

14. A transistor device, comprising:

a substrate having a channel region;

a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode;

source and drain regions formed in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 2E20 cm^{-3}; and

metal-germanide source and drain contacts.

15. The device of claim 14, the device further comprising:

a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

16. The device of claim 14 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

17. The device of claim 16 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

18. The device of claim 17 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 2E20 cm^{-3}.

19. The device of claim 16 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the device further comprises a thin buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 2E20 cm^{-3}, the buffer having a thickness of less than 100 Angstroms.

20. A method for forming a transistor device, comprising:

providing a substrate having a channel region;

providing a gate electrode above the channel region, wherein a gate dielectric layer is provided between the gate electrode and the channel region and spacers are provided on sides of the gate electrode; and

forming source and drain regions in the substrate and adjacent to the channel region, each of the source and drain regions including a tip region that extends under the gate dielectric layer and/or a corresponding one of the spacers, wherein the source and drain regions comprise a boron doped germanium layer having a germanium concentration in excess of 50 atomic % and a boron concentration in excess of 1E20 cm^{-3}.

21. The method of claim 20, further comprising:

providing a buffer between the substrate and the boron doped germanium layer, wherein the buffer has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 95 atomic %, and a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

22. The method of claim 20 wherein the boron doped germanium layer has a bilayer construction comprising a boron doped silicon germanium portion and a boron doped germanium cap thereon.

23. The method of claim 22 wherein the boron doped silicon germanium portion has a germanium concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 50 atomic %, and the boron doped germanium cap has a germanium concentration in excess of 95 atomic %.

24. The method of claim 22 wherein the boron doped silicon germanium portion has a fixed germanium concentration, and the method further comprises providing a buffer between the boron doped silicon germanium portion and the boron doped germanium cap, the buffer having a germanium concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 50 atomic %, and a boron concentration that is graded from a base level concentration compatible with the boron doped silicon germanium portion to a high concentration in excess of 1E20 cm^{-3}.

25. The method of claim 24 wherein the boron doped silicon germanium portion has a boron concentration that is graded from a base level concentration compatible with the substrate to a high concentration in excess of 1E20 cm^{-3}.

TRANSISTORS WITH HIGH CONCENTRATION OF BORON DOPED GERMANIUM

ABSTRACT OF THE DISCLOSURE

Techniques are disclosed for forming transistor devices having source and drain regions with high concentrations of boron doped germanium. In some embodiments, an in situ boron doped germanium, or alternatively, boron doped silicon germanium capped with a heavily boron doped germanium layer, are provided using selective epitaxial deposition in the source and drain regions and their corresponding tip regions. In some such cases, germanium concentration can be, for example, in excess of 50 atomic % and up to 100 atomic %, and the boron concentration can be, for instance, in excess of 1E20 cm^{-3}. A buffer providing graded germanium and/or boron concentrations can be used to better interface disparate layers. The concentration of boron doped in the germanium at the epi-metal interface effectively lowers parasitic resistance without degrading tip abruptness. The techniques can be embodied, for instance, in planar or non-planar transistor devices.

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2	Application Data Sheet	P34115_ADS_12-21-10-.pdf	554711 ec9cf08add4ab2f2c2c2387a7e9dea331f550da1	no	6
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