

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG CORP.
("Samsung"),
Petitioner

v.

DAEDALUS PRIME LLC
("Daedalus"),
Patent Owner

Case IPR2023-00536
Patent No. 10,700,178

DECLARATION OF E. FRED SCHUBERT, Ph.D.

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I, E. Fred Schubert, Ph.D. of Troy, New York, declare that:

I. Introduction

1. My name is E. Fred Schubert, and I have been retained by counsel for Petitioner Samsung Corp. (“Samsung” or “Petitioner”) as an expert witness to provide assistance regarding U.S. Patent No. 10,700,178 (“the ’178 Patent”). Specifically, I have been asked to consider the validity of claims 1-20 of the ’178 Patent (the “Challenged Claims”) in view of prior art and obviousness considerations from the perspective of a person of ordinary skill in the art at the time of the invention (“POSITA”) as it relates to the ’178 Patent.

2. I am being compensated for my time at my standard consulting rate. I am also being reimbursed for expenses that I incur during the course of this work. My compensation is not contingent upon the results of my study, the substance of my opinions, or the outcome of any proceeding involving the challenged claims. I have no financial interest in the outcome of this matter or on the pending litigation between Petitioner and Patent Owner.

3. My analysis here is based on my years of education, research and experience, as well as my investigation and study of relevant materials, including those cited herein.

4. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may

also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

5. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. Qualifications

6. I have more than 25 years of experience in the field of electrical engineering and applied physics including semiconductor materials, processing, and devices. I am currently an active tenured full Professor in the Department for Electrical, Computer, and Systems Engineering at the Rensselaer Polytechnic Institute (RPI) located in Troy, New York.

7. I received a Master's Degree in Electrical Engineering from the University of Stuttgart, Germany, in 1981. I received a Ph.D. degree in Electrical Engineering from the University of Stuttgart, Germany, in 1986.

8. Subsequent to my education, starting in 1985, I worked in industry at AT&T Bell Laboratories in Holmdel and Murray Hill, New Jersey, for ten years.

9. In 1995, I joined academia. My first position was at Boston University (Boston, MA), where I worked as a full professor for seven years.

10. In 2002, I joined RPI as a distinguished professor, the Wellfleet Senior Constellation Professor and Head of the Future Chips Constellation with appointments in the Department for Electrical, Computer, and Systems Engineering and the Department for Physics, Applied Physics and Astronomy. I am the founding Director of the Smart Lighting Engineering Research Center that was funded by the U.S. National Science Foundation at a volume of \$40 million for over 10 years.

11. I am named as co-inventor in more than 35 U.S. patents and have co-authored more than 300 publications. I authored the books “*Doping in III-V Semiconductors*” (1993), “*Delta Doping of Semiconductors*” (1996), “*Physical Foundations of Solid-State Devices*” (2015) and the first, second and third editions of “*Light-Emitting Diodes*” (2003, 2006 and 2018); the latter book is known as a standard textbook in the field of LEDs, and the book has been translated into Russian, Japanese and Korean. My publications have been well recognized by the technical community as illustrated by the more than 40,000 citations that my publications have received.

12. I received several awards for my technical contributions. They include: Senior Member IEEE (1993); Literature Prize of Verein Deutscher Elektrotechniker for the book “*Doping in III-V Semiconductors*” (1994); Fellow SPIE (1999); Alexander von Humboldt Senior Research Award (1999); Fellow IEEE (1999); Fellow OSA (2000); Boston University Provost Innovation Award (2000); Discover

Magazine Award for Technological Innovation (2000); R&D 100 Award for RCLED (2001); Fellow APS (2001); RPI Trustees Award for Faculty Achievement (2002 and 2008); honorary membership in Eta Kappa Nu (2004); 25 Most Innovative Micro- and Nano-Products of the Year Award of R&D Magazine (2007); and Scientific American 50 Award (2007).

13. My general expertise is in the field of electrical engineering and applied physics including semiconductor materials, processing, and devices. My specific expertise is in the field of semiconductor devices, semiconductor integrated circuits, semiconductor processing, ohmic contacts, Schottky contacts, and optoelectronic devices such as detectors and light-emitting diodes (LEDs). My work has included the design, growth, fabrication, and testing of semiconductor devices as well as the employment of these devices in a variety of applications. I have made contributions, including pioneering contributions, to the following technical fields that are relevant to the present matter: Delta-doping of semiconductors, monolayer doping of semiconductors, integrated circuit fabrication processes, thin-film deposition processes, Schottky contacts, ohmic contacts, epitaxial growth, strained-layer semiconductor growth, polarization-enhanced ohmic contacts, delta-doped ohmic contacts, non-alloyed ohmic contacts, fabrication technologies of ohmic contacts, and the theory of semiconductor devices and contacts.

14. The '178 Patent generally relates to MOSFET devices “having reduced parasitic contact resistance relative to conventional devices,” and the techniques disclosed in the '178 Patent can “can be implemented, for example, using a standard contact stack such as a series of metals on, for example, silicon (Si) or silicon germanium (SiGe) source/drain regions.” EX1001, Abstract. Furthermore, “an intermediate boron doped germanium layer is provided between the source/drain and contact metals to significantly reduce contact resistance.” *Id.* Configurations include “both planar and non-planar transistor structures (e.g., FinFETs), as well as strained and unstrained channel structures. Graded buffering can be used to reduce misfit dislocation.” *Id.*

15. I have extensive experience related to semiconductor devices, both with silicon-based semiconductors and group III-V semiconductors.

16. My publications on the topic of ohmic contacts to semiconductors include:

- E. F. Schubert, J. E. Cunningham, W. T. Tsang, and T. H. Chiu “Delta-doped ohmic contacts to n-GaAs” Applied Physics Letters 49, 292 (1986) and Applied Physics Letters 49, 984 (1986).
- Y.-L. Li, E. F. Schubert, J. W. Graff, A. Osinsky, and W. F. Schaff “Low-resistance ohmic contacts to p-type GaN” Applied Physics Letters 76, 2728 (May 2000).

- T. Gessmann, Y.-L. Li, E. L. Waldron, J. W. Graff, and E. F. Schubert “Ohmic contacts to p-type GaN mediated by polarization fields in thin InGaN capping layers” *Applied Physics Letters* 80, 986 (Feb. 2002).
 - T. Gessmann, Y.-L. Li, E. L. Waldron, and E. F. Schubert “Novel type of ohmic contacts to p-doped GaN using polarization fields in thin InGaN capping layers” *J. of Electronic Materials* 31, 416 (May 2002).
 - T. Gessmann, J. W. Graff, Y.-L. Li, E. L. Waldron, and E. F. Schubert “Ohmic contact technology in III-V nitrides using polarization effects in cap layers” *Proceedings of the Lester Eastman conference on high-speed devices* (Sept. 2002).
 - T. Gessmann, J. W. Graff, Y.-L. Li, E. L. Waldron, and E. F. Schubert “Ohmic contacts to III-V nitrides using polarization effects of cap layers” *Journal of Applied Physics* 92, 3740 (October 2002).
 - Seung Cheol Han, Jae-Kwan Kim, Jun Young Kim, Dong Min Lee, Jae-Sik Yoon, Jong-Kyu Kim, E. F. Schubert, and Ji-Myon Lee “Ohmic contacts to N-face p-type GaN using Ni/Au for the fabrication of polarization inverted light-emitting diodes” *Journal of Nanoscience and Nanotechnology* 13, 5715 (Aug. 2013).
17. My publications related to the doping of semiconductors include:
- E. F. Schubert (author) “Doping in III-V Semiconductors,” Hardback and paperback book, 628 pages (Cambridge University Press, Cambridge, UK, 1993).
 - E. F. Schubert (editor) “Delta Doping in Semiconductors,” Hardback and paperback book, 616 pages (Cambridge University Press, Cambridge, UK, 1996).

- H.-J. Gossmann and E. F. Schubert “Delta doping in silicon” CRC Critical Reviews in Solid State and Materials Sciences 18, 1 (1993).
 - E. F. Schubert “Delta doping of III–V compound semiconductors: Fundamentals and device applications” Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, Volume 8, page 2980 (1990).
18. My publications related to the theory of semiconductor devices include:
- E. F. Schubert (Dissertation” “Modern Schottky gate field-effect transistors based on III-V semiconductors” (University of Stuttgart, Germany, 1986).
 - E. F. Schubert “Physical Foundations of Solid-State Devices” (Book, Google Books, Mountain View CA, 2015 and 2022).
19. I am an inventor on U.S. patents that are directed to ohmic contacts for semiconductors. These patents include:
- J. E. Cunningham, E. F. Schubert, and W. T. Tsang, “Delta doped ohmic metal to semiconductor contacts” U.S. Patent No. 4,772,934, issued on September 20, 1988.
 - J. E. Cunningham, E. F. Schubert, and W. T. Tsang, “Field-effect transistor having a delta-doped ohmic contact” U.S. Patent No. 4,780,748, issued on October 25, 1988.
20. I have researched, worked, and consulted on a wide variety of technology relevant to silicon integrated circuits. This includes transistors (planar MOSFETs, FinFETs, and GAA FETs), thin-film deposition technologies (PVD, CVD, ALD, and MBE); stressors (SiGe and III-V compounds), etching technologies (wet etching, dry etching, anisotropic wet chemical etching, and crystallographic

etching), low-k materials, high-k materials, and the scaling of the geometric dimensions of MOSFET devices.

21. Further, at my home institution, Rensselaer Polytechnic Institute (RPI), I regularly teach on the subject of silicon integrated circuit technology, including the theory of transistors, strained semiconductors, and ohmic contacts. In my research laboratories, we routinely measure the properties of ohmic contacts, including the specific contact resistance and the transfer length. We also assess structural aspects of semiconductor devices, including ohmic contacts, by assessment techniques such as SIMS (secondary ion mass spectrometry), AES (auger electron spectroscopy), SEM (scanning electron microscopy), EDXS (energy dispersive x-ray spectroscopy), and ellipsometry.

22. A detailed record of my professional qualifications, including a list of publications, awards, and professional activities, is attached as Appendix A to this report and summarized below.

III. Level of Ordinary Skill in the Art

23. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a POSITA at the time of the alleged invention, which I understand is asserted to be December 21, 2010—the filing date of a parent patent application. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of

education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

24. Taking these factors into consideration, on or before December 21, 2010, a POSITA relating to the technology of the '178 Patent would have had a Master's degree in electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing. Additional education could substitute for professional experience, or significant experience in the field could substitute for formal education.

25. Before December 21, 2010, my level of skill in the art was at least that of a POSITA. I am qualified to provide opinions concerning what a POSITA would have known and understood at that time, and my analysis and conclusions herein are from the perspective of a POSITA as of that date.

IV. Materials Considered and Relied Upon

26. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein as well as those identified in this declaration, including the '178 Patent, the prosecution history of the '178 Patent, and

prior art references cited herein. These materials comprise patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions.

27. I have also relied on my education, training, research, knowledge, and personal and professional experience in the relevant technologies and systems that were already in use prior to, and within the timeframe of the earliest priority date of the claimed subject matter in the '178 Patent, which is December 21, 2010.

- **EX1001** U.S. Patent No. 10,700,178 to Glass (“the ’178 Patent”)
- **EX1002** File History of the ’178 Patent
- **EX1005** Certified English Translation of Japanese Patent Application Publication No. 2010-171337 (“Tezuka”)
- **EX1006** U.S. Patent App. Pub. No. 2010/0276761 (“Tung”)
- **EX1007** U.S. Patent App. Pub. No. 2011/0073952 (“Kwok”)
- **EX1008** U.S. Patent App. Pub. No. 2010/0148217 (“Simonelli”)
- **EX1009** U.S. Patent App. Pub. No. 2012/0139015 (“Yu”)
- **EX1010** U.S. Patent App. Pub. No. 2009/0325607 (“Conway”)
- **EX1013** Excerpts of the File History of EP Patent App. No. 19188924
- **EX1016** Findlay Shearer, *Power Management in Mobile Devices - A View of Energy Conservation - Part IV*, EE Times, May 5, 2008, available at <https://www.eetimes.com/power-management-in-mobile-devices-a-view-of-energy-conservation-part-iv/>
- **EX1017** U.S. Patent App. Pub. No. 2011/0147842 (“Cappellani”)

- **EX1018** U.S. Patent No. 7,288,443 (“Zhu”)
- **EX1019** U.S. Patent No. 2007/0235802 (“Chong”)
- **EX1020** U.S. Patent App. Pub. No. 2005/0184316 (“Kim I”)
- **EX1021** U.S. Patent App. Pub. No. 2007/0082451 (“Samoilov”)
- **EX1022** A. Nishida et al., *Elimination of Misfit Dislocations in $\text{Si}_{1-x}\text{Ge}_x/\text{Si}$ Heterostructures by Limited-area Molecular-beam Epitaxial Growth*, J. Appl. Phys 71 at 5913-5917 (1992) (“Nishida”)
- **EX1023** E.A. Fitzgerald, *The Effect of Substrate Growth Area on Misfit and Threading Dislocation Densities in Mismatched Heterostructures*, J. Vac. Sci. Tech. B7 at 782-788 (1989) (“Fitzgerald”)
- **EX1024** Arne Larsen, *Epitaxial Growth of Ge and SiGe on Si Substrates*, Materials Science in Semiconductor Processing 9 at 454-459 (2006) (“Larsen”)
- **EX1025** Schubert, *Room Temperature Properties of Si, Ge, GaAs, and GaN* (“Schubert Materials Datasheet”)
- **EX1026** Elsevier, *Encyclopedia of Materials: Science and Technology* at pp. 8479-8486 (2001) (“Elsevier”)
- **EX1027** Kim et al., *Increased Critical Thickness for High Ge-Content Strained SiGe-on-Si Using Selective Epitaxial Growth*, American Institute of Physics, Applied Physics Letter 97, 262106 (2010) (“Kim II”)
- **EX1028** Semiconductor Doping Technology, *available at* <https://www.iue.tuwien.ac.at/phd/wittmann/node7.html>
- **EX1029** Natalie Stavitski, *Silicide-to-Silicon Specific Contact Resistance Characterization: Test Structures and Models* (2009) (“Stavitski”)
- **EX1030** EP Application No. 1 575 082 A2 (“Demeurisse”)
- **EX1031** U.S. Patent No. 5,296,386 (“Aronowitz”)

- **EX1032** U.S. Patent App. Pub. No. 2006/0286755 (“Brask”)
- **EX1033** U.S. Patent App. Pub. No. 2011/0024804 (“Chang”)
- **EX1035** Mirabella et al., *Mechanisms of Boron Diffusion in Silicon and Germanium*, Journal of Applied Physics 113, 031101 (2013) (“Mirabella”)
- **EX1036** U.S. Patent App. Pub. No. 2006/0071275 (“Brask”)
- **EX1037** Brown et al., *Lattice stability and point defect energetics of TiSi_2 and TiGe_2 allotropes from first-principles calculations*, Journal of Applied Physics 129, 085104 (2021) (“Brown”)

V. Legal Standards

28. I am not a lawyer and do not provide any legal opinions, but I have been advised that certain legal standards are to be applied by technical experts in forming opinions regarding meaning and validity of patent claims. I have applied the legal standards described below, which were provided to me by counsel for the Petitioner.

29. It is my understanding that assessing the validity of a U.S. patent based on a prior art analysis involves two steps. First, one must construe the terms of the patent claims to understand what meaning one of ordinary skill in the art would have given the terms. Second, after the claim terms have been construed, one may then assess validity by comparing a patent claim to the “prior art.” I understand that the teaching of the prior art is viewed through the eyes of a POSITA at the time the invention was made. My analysis as to what constitutes a relevant POSITA (in the present context) is set forth above.

A. Legal Standards for Prior Art

30. I understand that a patent or other publication must first qualify as prior art before it can be used to invalidate a patent claim. For purposes of this declaration, counsel for Petitioner has instructed me to assume that each prior art reference cited in the combinations described below (i.e., Tekuza, Tung, Simonelli, and Conway) qualifies as prior art to the '178 Patent.

B. Legal Standard for Priority Date

31. I understand that the “priority date” (or “earliest effective filing date” or “Critical Date”) of a patent is the date on which it is filed, or the date on which an earlier application was filed if the patentee properly claims the benefit of the earlier application’s filing date. For purposes of my analysis in this declaration, I have assumed that the '178 Patent is entitled to a priority date of December 21, 2010.

C. Legal Standard for Obviousness

32. I understand that a claim is unpatentable as obvious “if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.” 35 U.S.C. § 103. Obviousness may be based upon a combination of references.

33. If a patent claim describes a combination of known elements, there must be some apparent reason to combine the known elements in the fashion

claimed. Reasons to combine may be obtained by considering the teachings of prior art references, the effects of demands known to people working in the field or present in the marketplace, and the background knowledge possessed by a POSITA. I understand that identifying a reason that a POSITA would have been motivated to combine different teachings of the prior art is important because inventions in many instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, was already known. The prior art references themselves may provide a suggestion, motivation, or reason to combine, but the nexus linking two or more prior art references is sometimes simple common sense.

34. An obviousness inquiry involves consideration of the following factors: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) any objective indicia of non-obviousness, such as commercial success, long-felt but unresolved need, failure of others, industry recognition, copying, and unexpected results.

35. If a technique has been used to improve one device, and a person of ordinary skill at the time of invention would have recognized that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond their skill.

36. I understand that when a patent claim simply arranges old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, the claim is obvious.

37. Practical and common-sense considerations should guide a proper obviousness analysis, because familiar items may have obvious uses beyond their primary purposes. A POSITA looking to overcome a problem will often be able to fit together the teachings of multiple prior art references. An obviousness analysis therefore takes into account the inferences and creative steps that a person of ordinary skill would have employed at the time of invention.

38. A proper obviousness analysis focuses on what was known or obvious to a POSITA at the time of invention, not to the patentee. Accordingly, any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.

39. Prior art teachings are properly combined if one of ordinary skill, having the understanding and knowledge reflected in the prior art and motivated by the general problem facing the inventor, would have been led to make the combination of elements recited in the claims. Under this analysis, the prior art references themselves, or any need or problem known in the field of endeavor at the time of the invention, can provide a reason for combining the elements of multiple prior art references in the claimed manner.

VI. Overview of the '178 Patent

A. Subject Matter Overview

40. The '178 Patent describes “transistor devices having reduced parasitic contact resistance relative to conventional devices.” EX1001, Abstract. The specification’s background discussion notes that “it is often desired to minimize the parasitic resistance associated with contacts otherwise known as external resistance R_{ext} ,” especially since “[d]ecreased R_{ext} enables higher current from an equal transistor design.” EX1001, 1:30-33; *see also id.*, 2:33-36. According to the specification, in “standard” transistor contacts, the contact resistance is effectively limited by the Si or SiGe valence band alignment to the pinning level in the metal,” and “using industry standard silicides such as nickel (or other suitable silicides, such as titanium, cobalt, or platinum), this results in a band misalignment of about 0.5 eV.” *Id.*, 2:39-44.

41. The inventors purportedly sought to “reduce the band misalignment value and contact resistance” in MOSFET devices by introducing an “**intermediate boron doped germanium layer**” (also referred to as a germanium “**cap layer**”) “between the source/drain and contact metals,” where the “cap layer” has a high concentration of germanium (Ge) in excess of 90%. *Id.*, 2:45-49, 7:17-20, 10:41-50, 12:12-31, 14:3-6.

42. To illustrate, Figure 5F depicts an example in which boron-doped Ge cap layers 317/319 have been formed over source/drain regions 318/320. *Id.*, 12:49-57. A suitable contact metal 325/327, such as titanium (Ti), is deposited over cap layers 317/319. A contact structure is then annealed so that the metals 325/327 and their respective Ge cap layers 317/319 chemically react to form low-resistance metal germanide layers, which electrically couple the source and drain regions 318/320 to the metal contact plugs 329/331 and external circuitry. *Id.*, 11:56-12:31, 12:64-13:2.

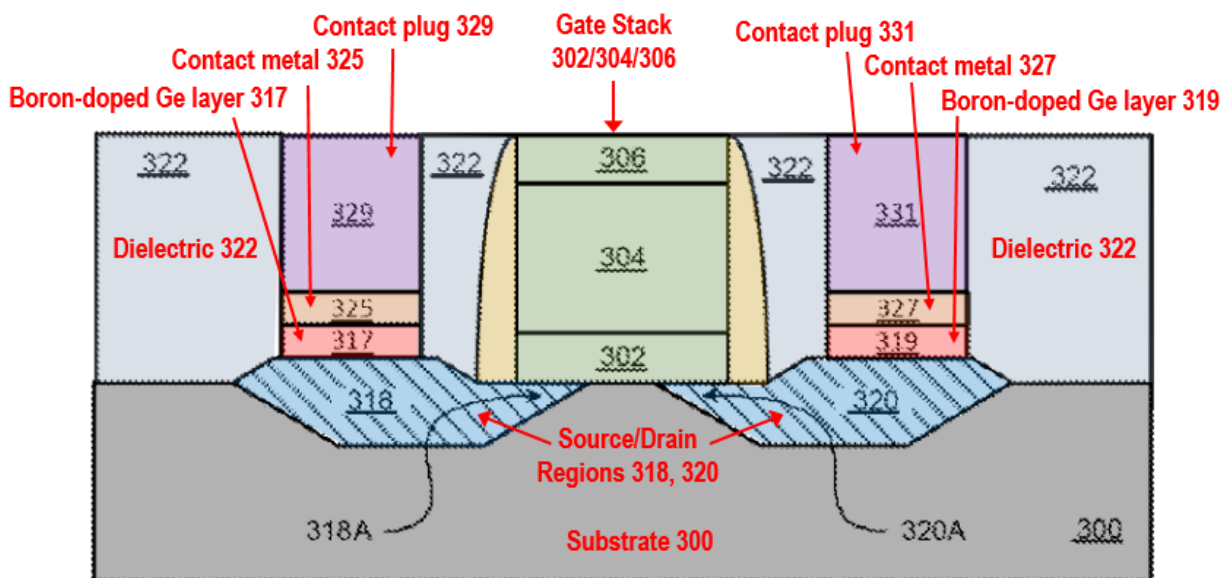
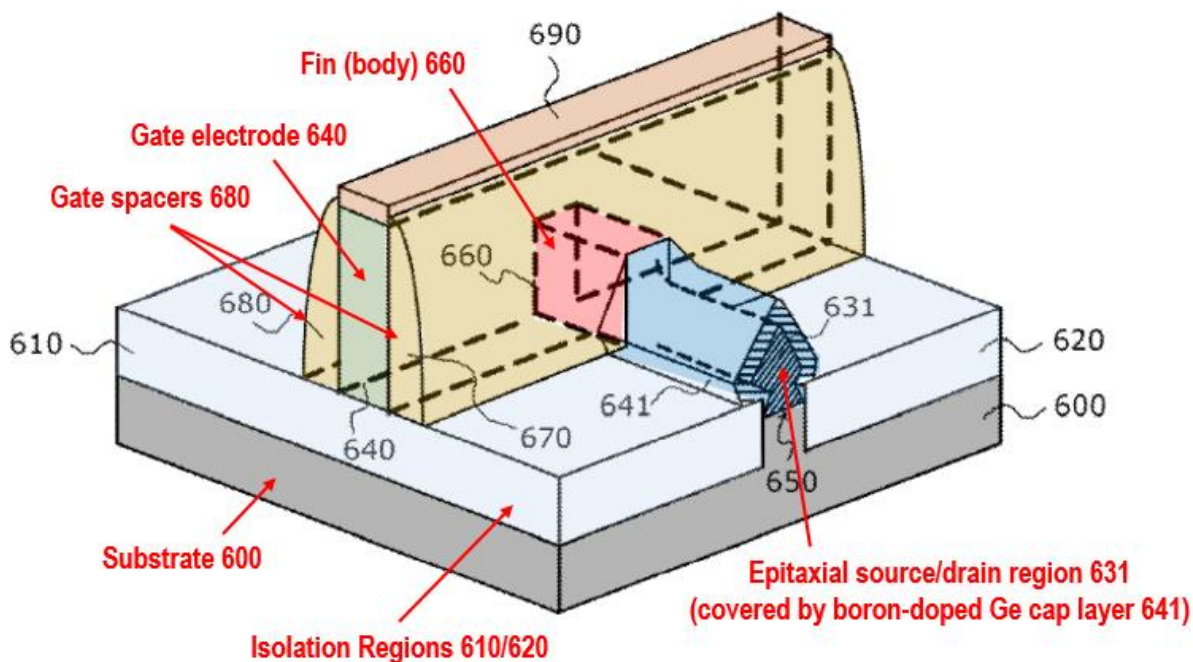


FIG. 5F

EX1001, FIG. 5F (annotated); *see also id.*, FIG. 3I.

43. The '178 Patent further explains how the boron-doped germanium caps can be used to improve contact resistance in a range of MOSFET devices, “including both planar and non-planar transistor structures (e.g., FinFETs).” *Id.*, 2:25-28. The claims of the '178 Patent are specifically directed to non-planar devices (e.g.,

FinFETs or other devices that were known to have multiple gates that would wrap a “fin” or channel body on multiple sides), an embodiment of which is depicted in Figure 6:



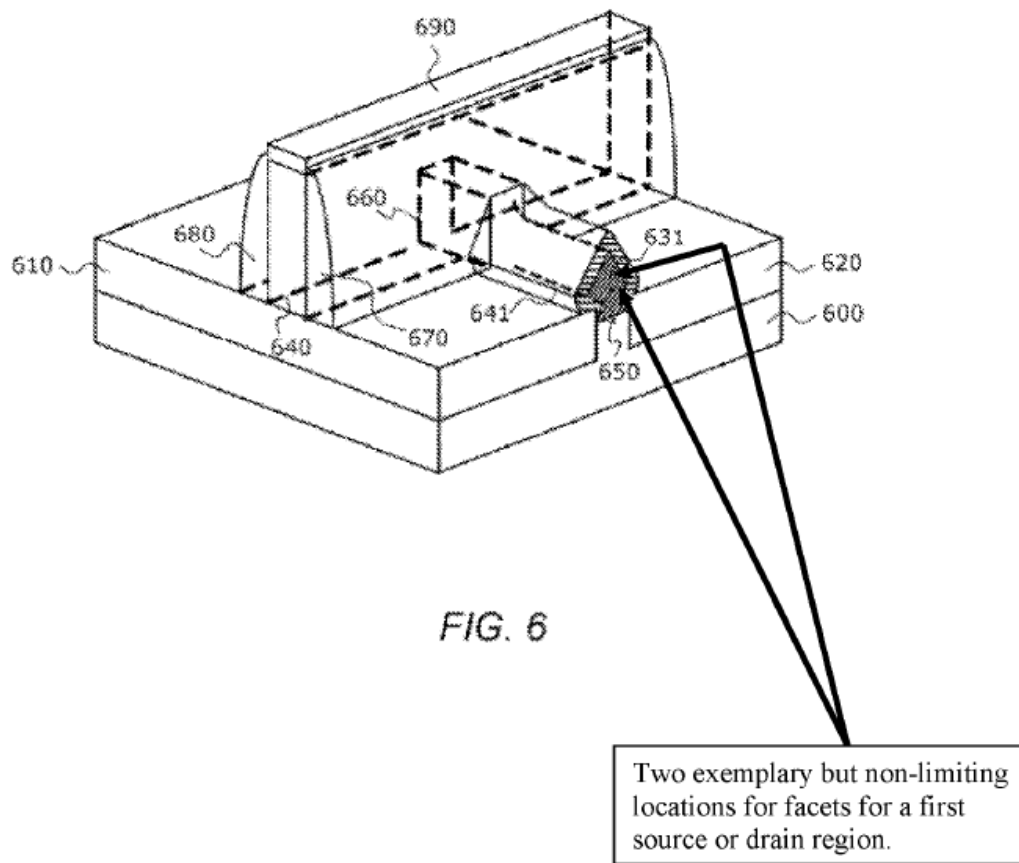
EX1001, FIG. 6; *see also id.*, 13:3-14:2.

44. As shown in Figure 6, “[a] cap layer 641 is deposited over the epitaxial regions 631” of the source and drain regions. *Id.*, 13:36-40. This results in a “bilayer structure” consisting of an epitaxially grown SiGe region 631 (which is the source / drain of the device) and a cap layer 641. *Id.*

B. File History of the '178 Patent

45. The '178 Patent was filed May 20, 2019, claiming priority to the application filed on December 21, 2010. EX1002, 322-329.

46. In the only substantive action issued during original examination of the '178 Patent, the Examiner made no prior art rejections, but rejected the claims for lacking written description support for the limitations directed to “two or more facets” of the source and drain regions. EX1002, 70-72. The applicant responded by arguing that Figure 6 depicted facets in the source/drain regions, and provided the following annotated version of Figure 6 to point out the supposed facets:



Annotated Figure 6 of Applicant's specification.

EX1002, 62.

47. The Examiner accepted the applicant's identification of support for "two or more facets," and allowed the application thereafter. EX1002, 34-41.

C. Interpretation of the '178 Patent Claims at Issue

48. For purposes of my analysis in this IPR proceeding, I understand that the terms that appear in the claims of the '178 Patent should be interpreted according to their plain and ordinary meaning. I understand that the plain and ordinary meaning of a claim term reflects the ordinary meaning that the term would have had to a POSITA at the time of the alleged invention in the context of the technology described in the patent. I also understand that the structure of the claims, the specification and file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, I understand that even treatises and dictionaries may be used, albeit under limited circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of the alleged invention.

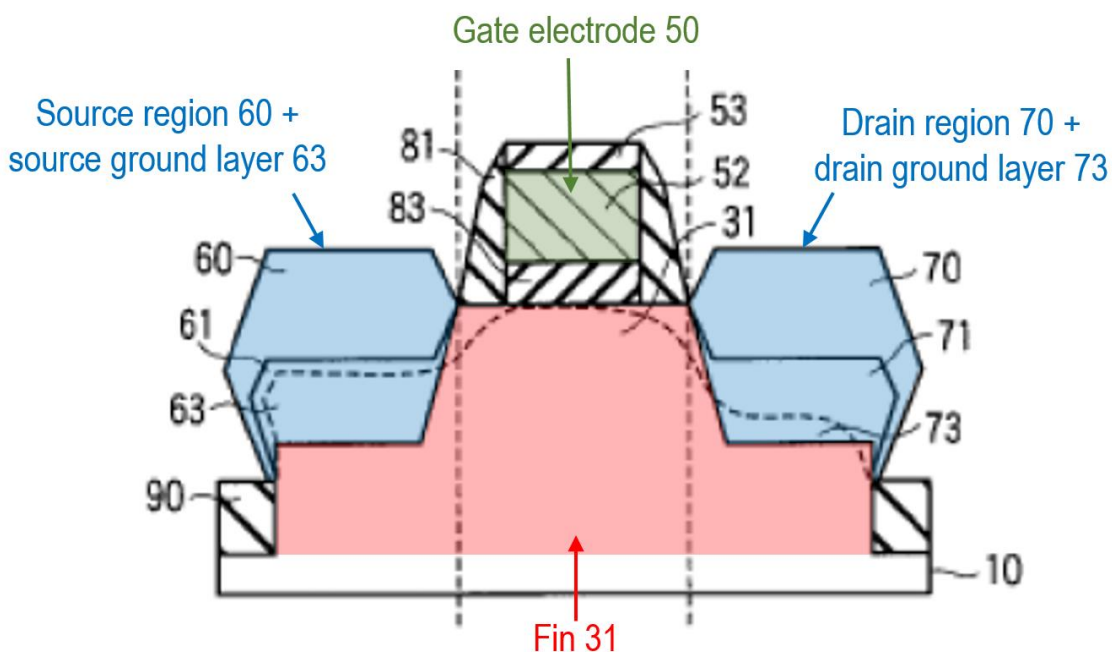
49. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the invention was made (not today). For purposes of my analysis here, I have used December 21, 2010 (i.e., the earliest alleged priority date or "Critical Date" of the '178 Patent) as the date of invention. Without exception, however, my analysis of the proper meanings of the

terms recited in the Challenged Claims would remain substantially the same even if the date of invention occurred anywhere in the early-to-mid 2010s.

VII. Overview of the Cited References

A. Tezuka

50. Tezuka generally describes “a field effect transistor that can reduce leakage current when a strained channel is used, suppress the occurrence of defects, and improve the yield.” EX1005, [0005]; *see also id.*, [0006]-[0010], [0117]-[0143]. Figure 8 depicts the structure of Tezuka’s transistor in a multi-gate embodiment for a fin-type field effect transistor:



Tezuka, FIG. 8(b) (annotated).

51. As shown in FIG. 8(b), Tezuka discloses a semiconductor fin 31 formed on a semiconductor substrate 10 that is perpendicular to the main surface of the

substrate. A bottom periphery of the fin 31 is buried with a buried insulating film 90, and a channel region is formed above the embedded insulating film 90 of the fin 31. An optional cap layer 83 is formed on the upper surface of the fin 31. A gate electrode 50 is formed on both side surfaces of the upper portion of the fin 31, and a gate insulating film 40 is disposed between the gate electrode 50 and the fin 31. EX1005, [0118]; *see also id.*, Fig. 8(c).

52. Tezuka's source region 60/63 and drain region 70/73 are formed having "a composition ratio" difference, thus creating a lattice mismatch between the source/drain regions 60/63, 70/73 and the substrate 10, and within the source region 60/63 and within the drain region 70/73, respectively. *Id.*, [0119]. A force is thereby created in the channel region of the fin 31, and the ground layers 63/73 experience strain. *Id.*, [0119]-[0120]. Moreover, by controlling the film thickness of the source region 60/63 and drain region 70/73, undesirable dislocations are less likely to occur in the source/drain. *Id.*, [0120]-[0121]. As noted above, a reduction in leakage current and the suppression of defects are among the advantages of Tezuka's transistor. *Id.*, [0005], [0010].

53. Tezuka further teaches that "[a] metal compound layer (NiGeSi or the like) ... may be formed on the surfaces of the source/drain regions 60 and 70." EX1005, [0170]; *see also id.*, [0066] ("Ni and Ge are reached by heat treatment to

form the source/drain electrodes 65 and 75 made of NiGe germanide”), [0039], [0054], [0089].

B. Tung

54. Tung generally describes techniques for fabricating non-planar MOSFET devices with low resistance source and drain contacts. EX1006, [0005]-[0006], [0019]-[0021]. Tung’s device lowers the Schottky barrier height between the semiconductor source/drain region and metal silicide contacts, thereby reducing the contact resistance. The reduction in contact resistance is accomplished by forming a metal silicide over doped semiconductor layer 55 (e.g., doped Ge) rather than by forming a metal silicide directly over a surface of source/drain region 51 itself. *Id.* For example, FIG. 4d shows a doped semiconductor layer 55 (e.g., doped Ge) grown epitaxially over a semiconductor material 51 (e.g., SiGe) of a source/drain region in a fin 28, and a silicide metal 57 (e.g., Ti) is further deposited over layer 55. *Id.*, [0039]-[0045]. The silicide metal 57 is annealed to form a metal silicide 59, as shown in FIG. 4e. *Id.*, [0043]-[0045].

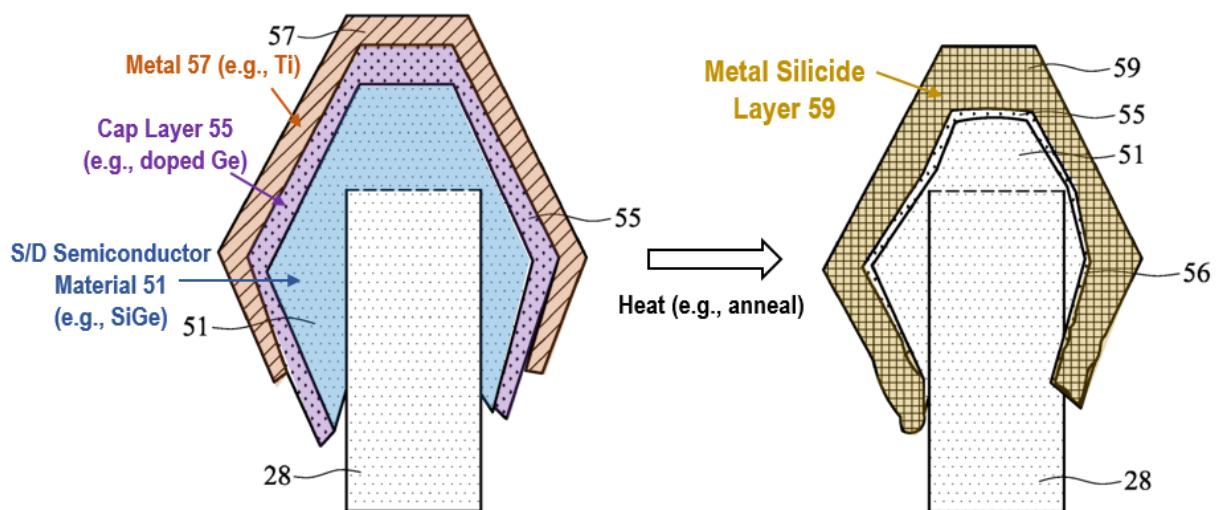


FIG. 4d

FIG. 4e

Tung, FIGS. 4d-4e (annotated)

C. Simonelli

55. Simonelli generally describes “planar and three-dimensional complementary metal oxide semiconductor (CMOS) devices comprising a compound layer with graded germanium content.” EX1008, [0001], Abstract. For example, Simonelli describes techniques for epitaxially growing source/drain regions in a multi-gate device (e.g., a FinFET) “using a graded high-germanium content silicon-germanium film stack 1400” like that illustrated in FIG. 14 (see [0051]-[0058]):



FIG. 14

Simonelli, FIG. 14 (annotated)

D. Conway

56. Conway generally describes “systems and techniques for generating graphical display elements and controls.” EX1010, [0002]; *see also id.*, Abstract, [0005], [0028]-[0030]. Conway’s techniques are performed on a computing system such as a mobile computing device (e.g., a smartphone). EX1010, Abstract, FIGS. 5-9. Figure 9 “shows an example of a generic computer device 900 and a generic mobile computer device 950, which may be used with the techniques described” in Conway. EX1010, [0147].

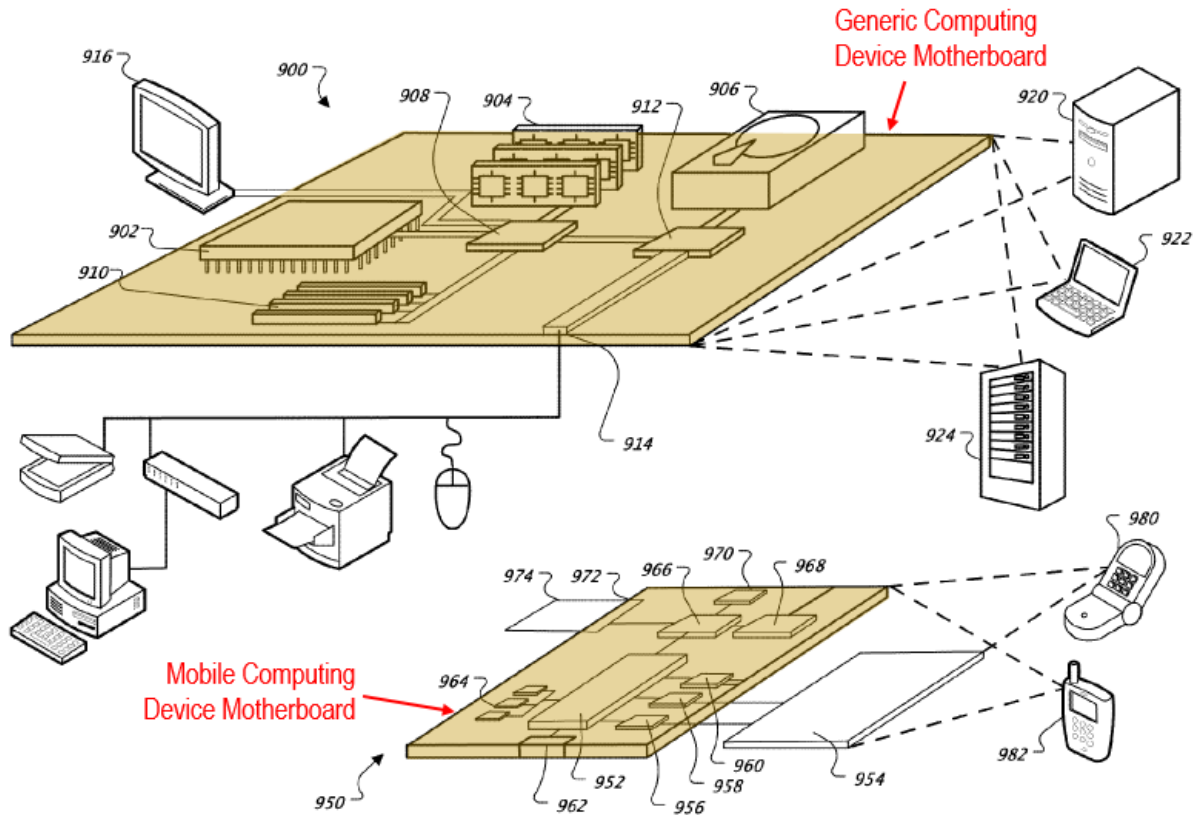


FIG. 9

EX1010, FIG. 9 (annotated)

57. Conway explains that the various components of the computing devices can be “mounted on a common motherboard or in other manners as appropriate.” *Id.*, [0148], [0153]. Moreover, Conway’s “[v]arious implementations ... can be realized in digital electronic circuitry, integrated circuitry, specially designed ASICs ..., computer hardware, firmware, software, and/or combinations thereof.” *Id.*, [0162]; *generally id.*, [0147]-[0165], FIGS. 5-8 and associated text (providing additional detail of the computing devices used in Conway’s system).

VIII. [Ground 1A] Tezuka in Combination with Tung Renders Obvious Claims 1, 4-6, and 9-10

58. Based on my review, the teachings of Tezuka in combination with Tung would have rendered obvious claims 1, 4-6, and 9-10 of the '178 Patent. The following sub-sections describe obvious modifications of Tezuka's FinFET in view of Tung, and further describe how the modified FinFET in the combination provides each element recited in claims 1, 4-6, and 9-10.

A. Manner and Motivations to Combine

59. As described below, it would have been obvious to implement Tezuka's metal compound layers as germanide layers over the source and drain regions of the FinFET according to Tung's suggestions (1) to include Ti in the germanide layers and (2) to form the germanide layers by annealing the Ti over a Ge cap layer like Tung's semiconductor layer 55.

1. Titanium for the Germanide Layers

60. Tezuka discloses a "metal compound layer" that is formed over the source and drain regions of the FinFET and that includes "NiGeSi or the like." EX1005, [120]. While NiGeSi is provided as one example, a POSITA nonetheless would have known that various other metal compounds were commonly used to form germanide or silicide layers over the source/drain regions of transistors like Tezuka's. Tung, for instance, describes the use of "Ni, Pd, Pt, Pa, Co, Ti, Al, Au, Lanthanoids ..., or combinations thereof," to form a silicide or germanide metal

contact layer 57. EX1006, [0042], [0061], [0080], Abstract. Relevant to the claims of the '178 Patent, Tung expressly recognizes Ti as one such metal that would be suitable for forming metal compound layers like Tezuka's. *Infra*, [1g], [1l]. Based on my review, it would have been obvious to a POSITA to select Ti for use in forming the metal compound layers in Tezuka's FinFET, and multiple reasons would have motivated a POSITA to do so.

61. First, Tezuka specifically notes that compounds other than NiGeSi would be suitable for use in the metal compound layer, and Tezuka leaves the selection of a particular compound to the discretion of a POSITA. EX1005, [0015] ("a metal compound layer (NiGeSi **or the like**)"), [0053], [0089], [0120]. Tung's disclosure of additional metals indicates that the selection of any one of them, including Ti, would have amounted to a non-innovative design choice, i.e., a routine and predictable choice that a POSITA would have made to optimize one or more well-known properties of the transistor or fabrication process that depend at least in part on the selection of a particular metal (e.g., properties relates to Schottky barrier height, contact resistivity, and reactivity of the metal compound).¹

¹ The specification of the '178 Patent indicates that a POSITA would have known how to choose an appropriate metal for the germanide layer, and the specification attributes no particular significance, benefit, or criticality to the selection of Ti over any other metal. EX1001, 7:40-44, 12:11-17. To the contrary, the specification admits that Ti was merely one of several "industry standard" metals that were known to be suitable forming germanide or silicide contacts. EX1001, 2:49-56.

62. Second, Ti would have been obvious to use in forming Tezuka's metal compound layer to enjoy the benefit of various well-established characteristics of Ti-based contacts. Titanium-based contacts were commonly used before the '178 Patent owing, among other things, to their low resistivity, high chemical reactivity, and capability of forming compounds with lower Schottky barrier heights. Titanium was also known to promote formation of low-leakage junctions, which also would have led a POSITA toward the use of Ti in the resulting device of the Tezuka-Tung combination.²

² The use of a range of metals for forming contacts to the source and drain regions of field-effect transistors had been actively studied for years before the '178 Patent. Elsevier's Encyclopedia of Materials, for example, covered the topic of "Silicides for S/D Contacts" in 2001, and specifically described the properties and comparative advantages of different metals, including Ti, in forming source/drain contacts on devices similar to Tezuka's. See EX1026. The Encyclopedia explains that "[a] silicide layer reduces the resistance of a S/D contact" because "the low sheet resistance of the silicide layer shunts the heavily doped diffusion region of the S/D to reduce its in-plane resistance" and further "the silicide reaction leads to intimate and more reliable metal-semiconductor (MS) contact and improves the conduction in the vertical direction." EX1026, 1. According to the Encyclopedia, "the most important properties of a silicide material are its electrical resistivity and its Schottky barrier height." *Id.* The Encyclopedia shows that titanium-based compounds such as C54 TiSi₂ can provide both low resistivity and a low Schottky barrier height. *Id.*, Table 1. The Encyclopedia notes "[t]he popularity of titanium-based contacts is due, to some degree, to its low resistivity and high chemical reactivity," and "[b]ecause the titanium silicide reaction can proceed right through residual and native oxide on the silicon surface, intimate and reliable contacts are easily made." *Id.*, 3. Further, "[c]ompared with other silicides such as CoSi₂, low-leakage junctions are relatively easy to form in titanium silicide contacts" and "[a]nother advantage of titanium silicide is its interface Fermi level position, which is near midgap of silicon, allowing low contact resistance to be achieved on both *n*- and *p*-type silicon." *Id.* Stavitski

63. Third, the use of Ti in the metal compound layer of the Tezuka-Tung device would have amounted to a simple substitution of nickel as taught in Tezuka with Ti as taught in Tung to produce predictable results (i.e., a metal compound layer based on Ti, Ge, and Si).

64. Fourth, the use of Ti in the metal compound layer of the Tezuka-Tung combination would have amounted to no more than an obvious use of a known technique (e.g., a titanium-based metal compound layer for source/drain contacts in a FinFET) to improve a similar device (e.g., Tezuka's FinFET) in substantially the same way as taught in Tung.

65. A POSITA would have had a reasonable expectation of success forming a metal compound layer that includes Ti. This is evident from the popularity of Ti in forming silicides and germanides before the '178 Patent³, and is reinforced by the '178 Patent's own identification of Ti as admitted prior art (an "industry standard" metal for this purpose). EX1001, 2:49-56.

(EX1029) also noted that "[t]he first SALICIDE process in CMOS production was introduced using titanium silicide (TiSi₂)," and similarly discloses low resistivity for titanium silicide. EX1029, 4-5; *see also id.*, 11 ("In general, for metal-semiconductor junctions at room temperature, the choice of the metal ... and the dopant level in the semiconductor ... will determine the value of" the specific contact resistance). Demeurisse (EX1030) also describes Ti as a "preferred metal[]" for a "metal-germanide compound." EX1030, [0019].

³ *Supra*, Footnote 2.

2. Metal Compound Layers Formed From Germanium Cap Layers Over the Source and Drain Regions

66. To the extent that Tezuka does not describe in detail how its metal compound layer is formed over the source and drain regions of the FinFET, Tung describes techniques for forming an analogous layer (referred to in Tung as “metal silicide layer 59”) from a chemical reaction of a metal with a doped Ge cap layer (referred to in Tung as “semiconductor layer 55”). For example, Tung’s process involves growing a cap layer 55 over a surface of the source and drain regions, depositing a metal 57 over the cap layer 55, and annealing the resulting structure to form a metal silicide layer 59 over the source and drain regions. EX1006, [0078]-[0082], [0039]-[0045], FIGS. 4, 13-16.

67. Based on my review, a POSITA would have found it obvious to form Tezuka’s metal compound layer according to Tung’s process for forming a metal silicide layer 59 from a metal layer and a doped Ge cap layer formed over at least a portion of the source and drain regions. (A POSITA would understand that a “metal silicide” containing Ge is chemically equivalent to “a metal germanide” containing Si). A POSITA would have been motivated to form a metal silicide layer from a metal layer and a doped Ge cap layer in order to achieve benefits like those described in Tung, including reducing the Schottky barrier height and lowering the contact resistance to the source and drain regions. EX1006, [0034] (“The metal silicide layer 59 comprises a suitable metal silicide to lower the Schottky barrier height of the

majority carriers. ...The Schottky barrier height between the doped semiconductor layer 55 and the metal silicide layer 59 determines the source/drain series resistance of the transistor” and “the doped semiconductor layer 55 is heavily doped so as to minimize this resistance.”); *see also id.*, [0005]-[0006], [0032].

68. According to Tung, “the low Schottky barrier height at the source of the transistor and the ultra-shallow junction depths ... achievable with metal silicides significantly improve[s] short channel effects of the transistor.” EX1006, [0031]. A POSITA would have known that Ge exhibits certain favorable characteristics compared to Si, including higher mobility and lower resistivity, which would have made a doped Ge cap attractive in various designs for forming germanide contact structures to the source and drain regions. The use of such a cap layer composed of doped germanium or a doped germanium-rich SiGe alloy would have allowed the FinFET in the combination to more fully realize the benefits of Ge due to its high concentration in the cap layer even if the Ge concentration in the source/drain regions is significantly lower (e.g., 50-70% Ge in layers 60/70).⁴ EX1005, [0140].

⁴ Favorable properties of germanium for use in forming metallized contacts to the source and drain regions of field-effect transistors had been recognized long before the '178 Patent. For instance, Aronowitz (EX1031) notes that “at normal integrated circuit operating temperatures ..., the drift mobility of electrons and holes in germanium exceeds the drift mobility in silicon by a factor of from 3-10.” EX1031, 1:15-21. Further, “the intrinsic resistivity of germanium ... is four orders of magnitude smaller than the intrinsic resistivity of silicon.” *Id.*, 1:26-29. In view of these and other favorable properties of germanium, Aronowitz described the benefits

A POSITA would have understood that concentrations of Ge in the source/drain regions toward the lower portion of Tezuka's disclosed composition ranges would have been preferable in certain designs to promote thicker film growth in larger areas over a silicon-based substrate.⁵

69. Further, based on Tung, it would have been obvious to use a doped Ge cap in forming Tezuka's metal compound layer to increase the uniformity of dopants at or near an interface to the metal from which the germanide layer is formed, as well as to reduce "residual defects that may result in poor silicide formation or result in leakage currents" that can otherwise result when implanting dopants for contact formation directly into the source/drain regions rather than in a Ge cap layer. EX1006, [0005], [0020] ("The use of epitaxial process prevents nucleation effects.

of forming contacts to the S/D regions of a FET from germanium. *Id.*, 3:38-42 ("[T]he germanium is a low resistivity material. Second, the germanium layer provides silicide contact resistance lowering. ... All of this leads to enhanced contact conductance in the source/drain regions."). Simonelli similarly recognized that "use of a strained high germanium compound film ... can provide the ... effect of contact resistance reduction" EX1008, [0024]; *see also* EX1024, 454 ("integration of Ge layers in Si-based structures has been considered due to its superior carrier mobilities compared to silicon"); EX1025 (disclosing comparative properties of Si and Ge at room temperature and showing germanium's lower bandgap energy and higher electron and hole mobilities than Si). To enjoy the benefits of germanium-based contacts, it would have been obvious to anneal a metal with a doped germanium layer.

⁵ *See infra*, Footnotes 12-13.

Further, a uniformly controlled doping is achievable even in non-planar structures.”).

70. Moreover, the use of a doped Ge cap in the FinFET of the resulting combination would have amounted to an obvious use of a known technique as taught in Tung to improve a similar device (e.g., Tezuka’s FinFET) to yield no more than predictable results. A POSITA would have had a reasonable expectation of success implementing the combination in light of the similar devices described in Tezuka and Tung. Notably, Tezuka and Tung each describe metal contact formation on the source/drain regions of non-planar devices (e.g., FinFETs), and Tung expressly teaches that the doped Ge cap layer can be formed over an epitaxially grown SiGe source/drain region (e.g., SiGe material 51 of source/drain regions 39) analogous to the upper source/drain layers 60/70 of Tezuka’s device. EX1006, [0040], [0058], [0074], [0078]. Tung also acknowledges that a POSITA would have known how to apply its techniques across a range of devices and integrated circuit structures. EX1006, [0019]-[0020], [0083]-[0084]. In this context, implementing the combination would have been within the skill of a POSITA, and a POSITA would have had a reasonable expectation of success.

B. Claim Element Analysis

1. Independent Claim 1

71. Claim 1 of the ’178 Patent recites:

1. An integrated circuit structure, comprising:
 - a fin comprising silicon;
 - a gate electrode over the fin;
 - a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
 - a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
 - a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
 - a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

72. The Tezuka-Tung combination would have rendered obvious and taught each element of claim 1 as described below.

[1pre] An integrated circuit structure, comprising:

73. Tezuka describes and would have rendered obvious [1pre]. Tezuka describes a fin-type field effect transistor 400, which a POSITA would have understood to be a type of component commonly used in integrated circuits.⁶

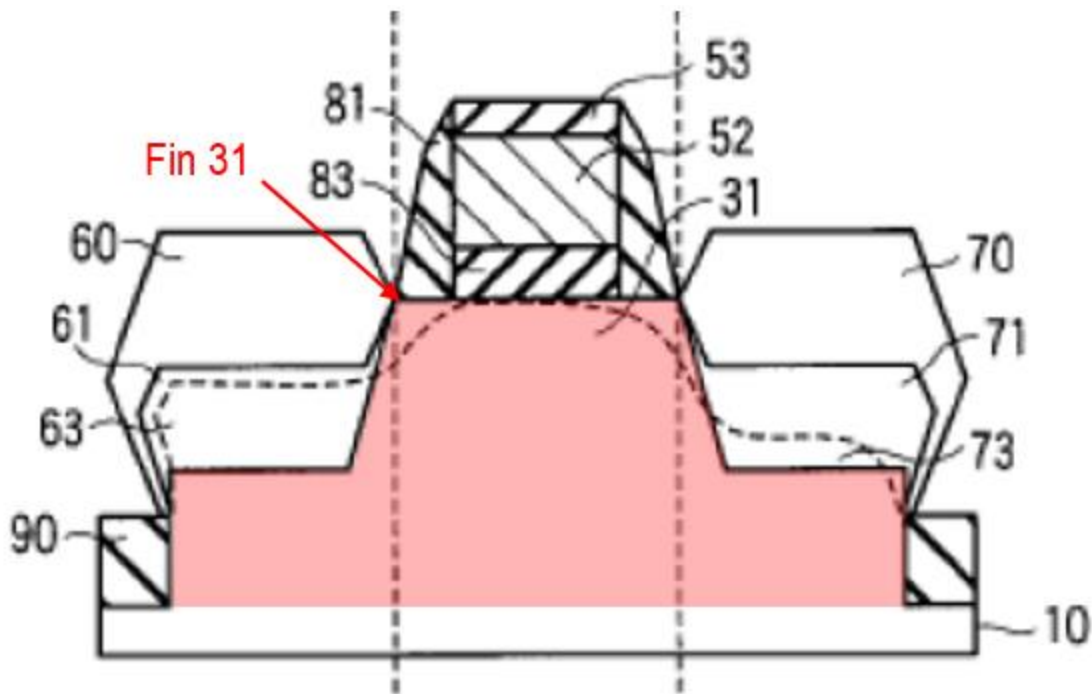
⁶ See EX1016, 6 (“In a multi-gate device, the channel is surrounded by several gates on multiple surfaces, allowing more effective suppression of ‘off-state’ leakage current. Multiple gates also allow enhanced current in the ‘on’ state, also known as drive current. These advantages translate to lower power consumption and enhanced

EX1005, [0117]-[0143], FIG. 8; *generally id.*, FIGS. 8-17. In one example, Tezuka teaches that “the fin-type field effect transistor is a strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).” EX1005, [0138].

[1a] a fin comprising silicon;

74. Tezuka describes and would have rendered obvious [1a], e.g., in view of Tezuka’s disclosure of a fin 31 in transistor 400. EX1005, [0118]-[0119], [0139]. According to Tezuka, “fin 31 and the channel region are made of n-type Si.” EX1005, [0139]; *see also id.*, [0150], FIG. 8b.

device performance. Non-planar devices are also more compact than conventional planar transistors, enabling higher transistor density which translates to smaller overall microelectronics.”), 7 (“In the technical literature, FinFET is used somewhat generically to describe any fin-based, multi-gate transistor architecture regardless of number of gates.”); EX1006, [0003] (“Semiconductor devices comprise integrated circuits that are formed on semiconductor wafers by depositing many types of thin films of material over the semiconductor wafers[] ... Integrated circuits include field-effect transistors (FETs)[] ...”), [0004] (“One of the goals of the semiconductor industry is to continue shrinking the size and increasing the speed of individual FETs. To achieve these goals, three dimensional (3-D) or non-planar transistor structures such as fin FETs (FINFETS)[] ... are being investigated for use in sub 22 nm transistor nodes. Such transistors not only improve area[] density, but also improve gate control of the channel.”).



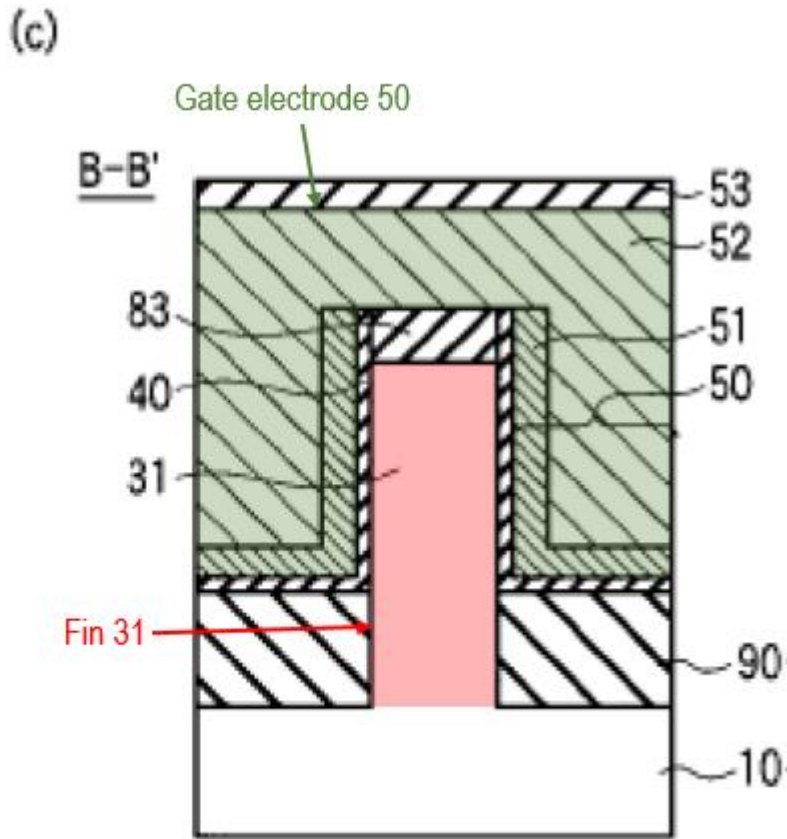
Tezuka, FIG. 8b (annotated)

75. Further, as described below in reference to feature [1c], and consistent with the plain and ordinary meaning of the term “fin” in the field before the Critical Date of the ’178 Patent (and consistent with how the term “fin” is used in the claims of the ’178 Patent), a POSITA would have understood Tezuka’s fin to include not only the indicated portion of Si beneath the gate, but also the epitaxially-formed source and drain regions. *Infra*, [1c].

[1b] a gate electrode over the fin;

76. Tezuka describes and would have rendered obvious [1b], e.g., based on Tezuka’s disclosure of a gate electrode 50 disposed over fin 31. Tezuka explains that “[a] gate electrode 50 is formed on both side surfaces of the upper portion of the

also *id.*, [0127], [0139].⁷

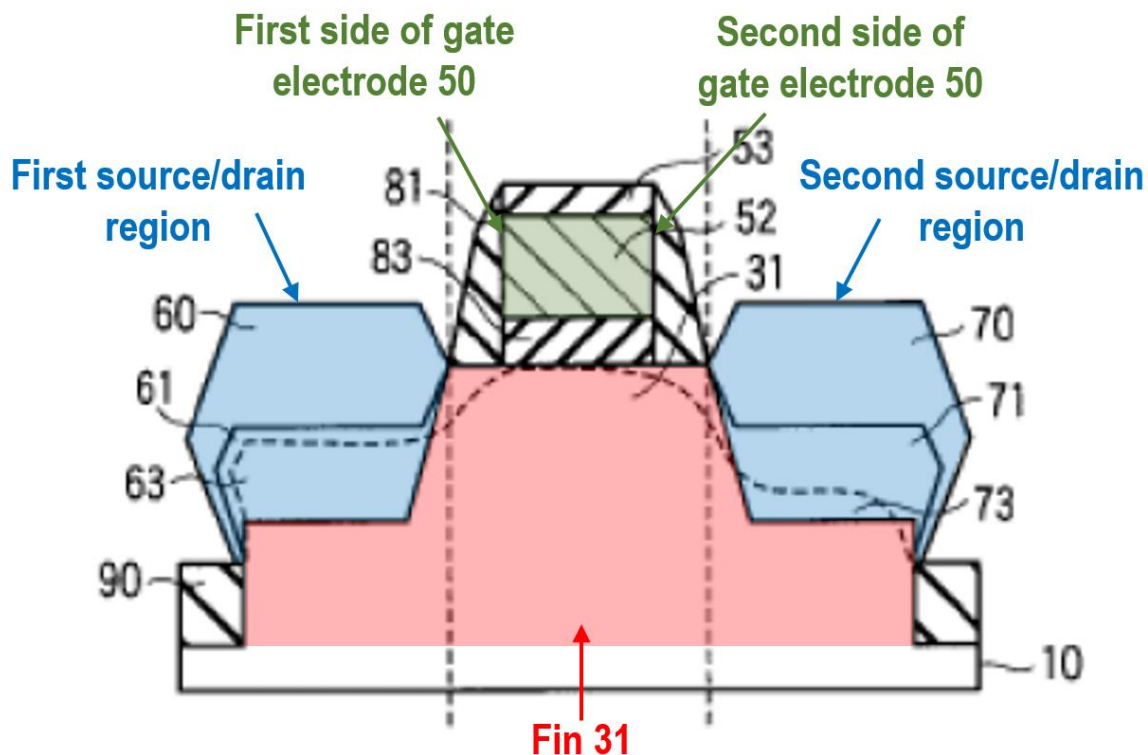


Tezuka, FIG. 8c (annotated)

[1c] a first source or drain region in the fin proximate a first side of the gate electrode;

77. Tezuka describes and would have rendered obvious [1c], e.g., in view of Tezuka's disclosure of a first source or drain region comprising, collectively, source ground layer 63 and source region 60.

⁷ Alternatively, Tezuka’s poly SiGe film 52 alone would have rendered obvious the claimed “gate electrode.”



Tezuka, FIG. 8b (annotated)

78. Tezuka further teaches that source/drain ground layers 63/73 are epitaxially grown in etched recesses 82 on either side of fin 31, and upper source/drain layers 60/70 are epitaxially grown over layers 63/73. EX1005, [0135]-[0136], FIGS. 16-17; *see also id.*, [0120]-[0121], [0139]-[0140]. Upper layers 60 and 70 are doped oppositely from fin 31 and the channel region, and thus provide a source and drain for charge carriers conducted along the channel. *Id.*, [0139]. Furthermore, with ground source/drain layers 63/73 being formed intermediately between fin 31 and upper source/drain layers 60/70 and within the same depression or recesses 82 as upper source/drain layers 60/70), layers 60/63 are each within a same “source **region**” as claimed, and layers 70/73 are each within a same “drain

region” as claimed. This understanding is consistent with Tezuka’s identification of both layers 60/63 as respective “**source**” components and Tezuka’s labeling of both layers 70/73 as respective “**drain**” components, and is further consistent with the ’178 Patent’s own broad descriptions of source and drain regions and related components.⁸

79. Tezuka’s source region 60/63 abuts a first S/D sidewall of Tezuka’s fin 31 proximate a first side of the gate electrode 50, while Tezuka’s drain region 70/73 abuts a second sidewall of Tezuka’s fin 31 proximate an opposite side of the gate electrode 50. A POSITA thus would have found it obvious that the source/drain

⁸ Notably, the ’178 Patent broadly describes how “the source/drain regions can be implemented with any number of suitable processes and configurations” and can be “**p-type and/or n-type**”—thus indicating that the source and drain regions can include both p-type and n-type doping. EX1001, 8:60-66 (emphasis added). It follows that, in the context of the ’178 Patent, a source or drain region is not restricted to a region with a single p-type or n-type doping. Often, for example, a region includes both n-type and p-type impurities, and “the impurity present in a higher concentration determines the type of conductivity in the semiconductor.” EX1028, 9 (“If donor and acceptor impurities are introduced together, the impurity present in a higher concentration determines the type of conductivity in the semiconductor.”). A POSITA also would have understood that a source or drain “region” can encompass multiple structures or materials. Tung, for example, teaches that its source and drain regions 39 can each include both a fin 28 and a semiconductor material 51 grown over the fin 28. See EX1006, [0033] (“source/drain regions 39 is disposed within the fins 28”), [0039]-[0041] and FIGS. 4b-e (depicting semiconductor material 51 grown over fin 28), [0074] (“a selective epitaxial growth is performed to form semiconductor material 51” and “[t]he semiconductor material 51 forms the source/drain regions 39 ...”).

regions in the device taught by Tezuka and Tung are “in the fin” because they are part of the fin.⁹ This observation is consistent with the ’178 Patent itself, which discloses epitaxially grown source/drain regions 631 formed on opposite sidewalls of a channel body or fin 660. EX1001, 13:22-50, FIG. 6; *see also* EX1013, 32 (applicant’s claims in a counterpart EP application refer to a “first source or drain region in the fin” and “comprising an epitaxial region (631) ... formed on ... one fin sidewall”). It appears that the ’178 Patent discloses that the S/D regions are formed on the fin, yet become part of the fin so that they are located in the fin. For the epitaxially grown source/drain regions 631 to be “in the fin,” it would have been obvious that the claimed “fin” is not limited to a structure like fin 660 that projects directly from the underlying substrate 600 in a region surrounded by the gate electrode. The claimed “fin” would instead encompass epitaxially grown source/drain regions like Tezuka’s source region 60/63 and drain region 70/73. Moreover, Tezuka reinforces the obviousness of forming first and second source or

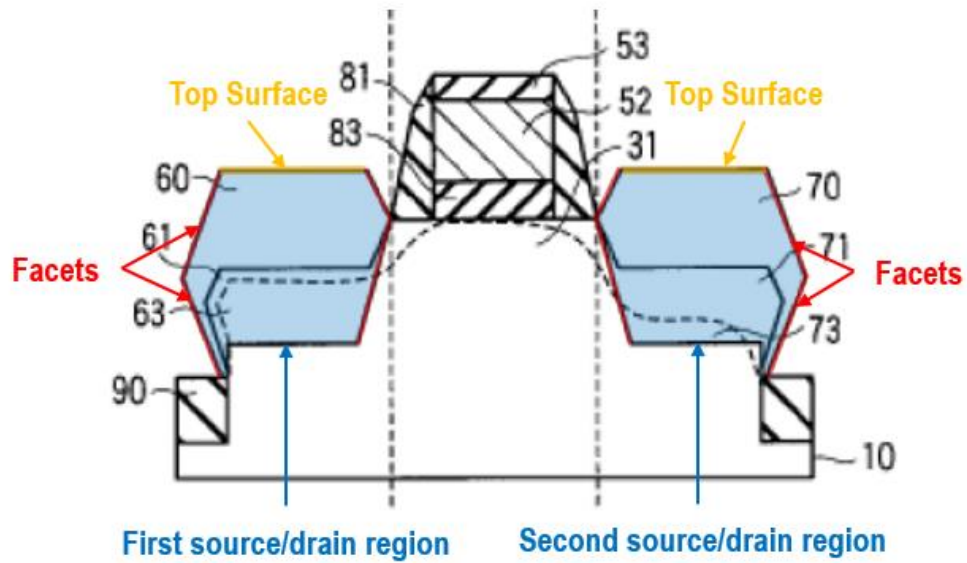
⁹ Epitaxially re-grown source and drain regions like those described in Tezuka were commonly characterized as part of the “fin” of a non-planar semiconductor device (e.g., a FinFET) before the ’178 patent. *See, e.g.*, EX1017, [0024] (“Disclosed herein is a multi-gate device including epitaxial source and drain fin regions ...”), [0040] (“the source/drain cavity 420, including the source/drain extension cavity 421, is filled with a material using a selective epitaxial deposition process to form regrown source/drain fin”), FIGS. 6A-6B (depicting source/drain fins 618).

drain regions “in the fin” by growing the source region 60/63 and drain region 70/73 in a recess 82 of fin 31. EX1005, [0119], [0135]-[0136].

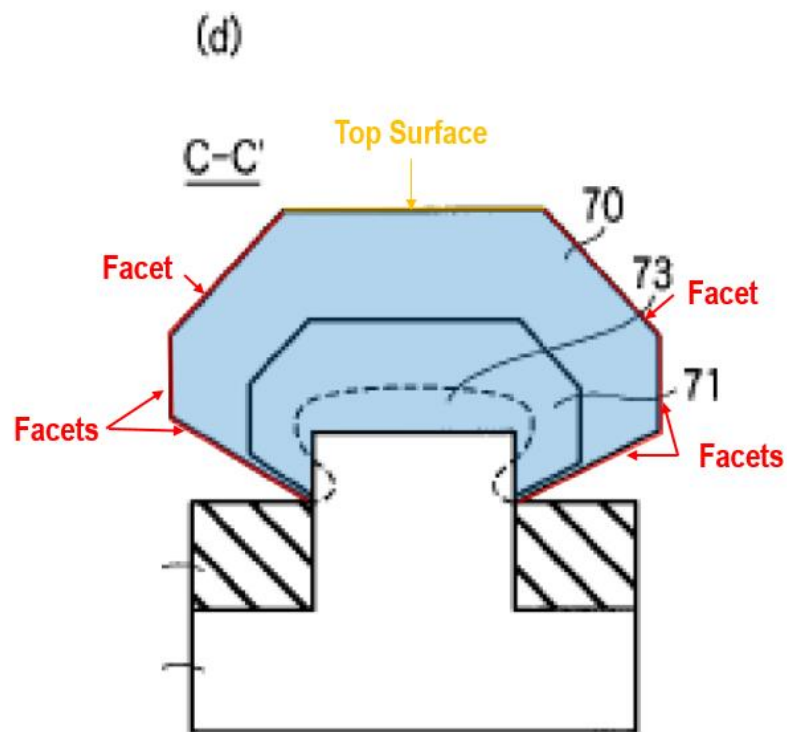
80. The '178 Patent does not define any bounds for the term “proximate,” but under any reasonable interpretation, it would have been obvious that Tezuka’s source region 60/63 is proximate a first side of the gate electrode 50 and Tezuka’s drain region 70/73 is proximate a second side of the gate electrode 50 opposite the first side. Indeed, much as FIG. 6 of the '178 Patent shows the epitaxial source/drain regions 631 extending from opposing sidewalls of a fin structure 660 on opposite sides of a gate electrode 640, Tezuka’s source and drain regions similarly extend from opposing S/D sidewalls of fin 31 on opposite sides of a gate electrode 50. *Cf.* EX1001, FIG. 6; EX1005, FIGS. 8(a)-(d).

[1d] the first source or drain region comprising two or more facets and a top surface;

81. Tezuka describes and would have rendered obvious [1d], e.g., in view of Tezuka’s disclosure of at least two facets and a top surface of the first source region 60/63. EX1005, [0136], [0118]-[0121], FIGS. 8, 17; *supra*, [1c]. Example structures meeting [1d] are shown in FIGS. 8b and 8d:



Tezuka, FIG. 8b (annotated)



Tezuka, FIG. 8d (annotated)

[1e] wherein the first source or drain region comprises silicon and germanium;

82. Tezuka describes and would have rendered obvious [1e], e.g., in view of Tezuka's disclosures that ground layer 63 and source region 60 (i.e., a "first source or drain region") each comprise alloys of Si and Ge. EX1005, [0139] ("source ground layer 63 and the drain ground layer 73 are made of n-type $\text{Si}_{0.95}\text{Ge}_{0.05}$ "), [0140] ("source/drain regions 60 and 70 have a preferable Ge composition range of 50% to 90% ... from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation"); *see also id.*, [0119]-[0121], [0135]-[0136], [0123]-[0124].

[1f] having a germanium concentration graded to a concentration in excess of 50%;

83. Tezuka describes and would have rendered obvious [1f], e.g., in view of Tezuka's description of a first source or drain region having a Ge concentration graded to a concentration in excess of 50%. Tezuka discloses a bilayer construction in the first source or drain region (i.e., layers 60/63) and the second source or drain region (i.e., layers 70/73), where the source and drain regions are each graded such that ground layers 63/73 are formed from SiGe with a lower concentration of Ge than the concentration of Ge in the SiGe alloy of upper layers 60/70. The Ge concentration in upper layers 60/70 is preferably as high as 90% (i.e., "in excess of 50%"). EX1005, [0140] ("source/drain regions 60 and 70 have a preferable Ge

composition range of 50% to 90% ... from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation”); see *also id.*, [0020], [0059], [0076], [0093], [0119], [0135]-[0136], [0139], [0123]-[0124]. The Ge concentration in ground layers 63/73 is lower than upper layers 60/70, e.g., “Si_{0.95}Ge_{0.05}”, but in any event is calibrated to a level that ensures “no dislocation occurs between the ground layers 63 and 73 and the substrate 10” while also being able to support the higher Ge concentration in upper layers 60/70.” *Id.*, [0139]-[0140]; see *also id.*, [0119] (“source region 60 and a drain region 70 made of an alloy semiconductor that ... has a composition ratio different from that of ... the ground layers 63 and 73, and has a different lattice constant”), [0120]-[0121]. Tezuka thus discloses and renders obvious first and second source or drain regions having a Ge concentration graded to a concentration in excess of 50% based at least on bilayer grading between ground layers 60/63 and upper layers 70/73.¹⁰

¹⁰ The ’178 Patent specification describes no requirement for a “graded” region to include continuous (or smooth) grading, nor does the specification describe any requirement for a “graded” region to include more than two concentrations of the graded component (e.g., germanium). See, e.g., EX1001, 6:25-32 (“In addition, as used herein, the term ‘fixed’ with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level.”). Thus, a region that includes at least two concentrations of a component intentionally differentiated by more than 10-percent would provide a graded region as described in the ’178 Patent. Simonelli (EX1008), which names a common inventor with the ’178 Patent (Anand S. Murthy), also refers

84. A POSITA also would have known and it would have been obvious to implement additional stepped or continuous grading of the Ge concentration within each of upper layers 60/70 and/or ground layers 63/73. Graded epitaxial growth was a common and well-known technique before the '178 Patent¹¹, and a POSITA would have known that further grading within layers 60/70 and/or 63/73 would have been beneficial to enable growth of thicker crystalline films for layers 60/70 and/or 63/73 that have increasingly higher Ge concentrations while reducing the risk of growth

to a stepped/layered film stack as a graded region. EX1008, [0019]-[0020], [0051], FIGS. 14-15.

¹¹ A POSITA would have known that grading could be performed in a region of a semiconductor structure either continuously (e.g., smoothly) or stepwise (e.g., using layers or a film stack), and both continuous and stepped grading were commonly implemented techniques before the '178 Patent. *See, e.g.*, EX1008, [0051] (“formed using a graded high germanium content silicon-germanium film stack”), FIGS. 14-15; EX1018, 2:53-55 (“the source and drain 40 on either side of the gate have a gradation of germanium having a maximum value at the top and reducing in magnitude toward the BOX (buried oxide) layer 20”); EX1019, [0123] and FIG. 6b (describing smooth grading of germanium content through source/drain regions); EX1020, [0058] (“The graded silicon-germanium layer may be formed by an epitaxial growth process which gradually increases the amount of germanium source gases. As a result, the germanium concentration of the graded silicon-germanium layer gradually increases from bottom to top.”); EX1021, [0032] (describing a layered grading technique: “[m]ultiple layers containing Si, SiGe, SiC, or SeGeC may be deposited in varying order to form graded elemental concentrations of silicon-containing layer 140”); EX1024 (“Growth of strain-relaxed layers of lattice-mismatched III-V compounds have, since the seventies, exploited the phenomenon that the concentration of threading dislocations can be reduced significantly by grading the composition [7]. ... This growth procedure was successfully taken over by the SiGe community ...”).

defects such as dislocations or plastic deformation.¹² The high Ge concentrations and thicker films that could be achieved through additional grading would have

¹² Techniques for growing semiconductor material having increasingly high concentrations of germanium over Si (or over silicon-germanium compounds having a lower concentration of germanium) had been well studied and developed before the '178 patent. For example, Kim II (EX1027) explains that “[h]igh Ge-content strained SiGe-on-Si is of interest for several applications,” but notes that “due to the 4% lattice mismatch between Si and Ge, growing SiGe on bulk Si is challenging due to the onset of misfit dislocation formation above the critical thickness T_{crit} .” EX1027, 1. Misfit dislocations between layers of material containing different concentrations of germanium can lead to undesirable effects including strain relaxation and leakage currents. Because a germanium-containing layer can only be grown free of misfit dislocations to a critical thickness limited by the degree of lattice mismatch between layers, and because dislocations also tend to increase with the area of epitaxial growth, the thickness and size of germanium-containing layers that can be grown over a silicon-containing layer is limited by the difference in germanium content between successive layers. EX1024 (“Because of the lattice mismatch of 4.2% between Si and Ge only very thin layers of Ge can be grown defect free on (0 0 1)-oriented Si substrates”), EX1027, 1 (“misfit dislocation nucleation is dominated by sources or microdefects with a fixed area[] density, [and] for small area, it is reported that the misfit dislocation density is lower than for large areas”); EX1022, 5917 (“As the size of the square SiO₂ opening area decreased, the misfit dislocation density rapidly decreased”). Accordingly, graded epitaxial growth was a well-known technique to obtain higher concentrations of germanium with thicker films and over larger areas, while reducing or eliminating defects such as misfit dislocations that would otherwise result from a substantial increase in germanium content over a silicon-containing layer. See, e.g., EX1024 (“the concentration of threading dislocations can be reduced significantly by grading the composition”), FIG. 1; EX1023, 782 (“mildly lattice-mismatched systems are used and the epilayer thicknesses are kept below the critical thickness for defect formation, resulting in totally elastically strained layers”); EX1018, 1:59-64 (“Since graded germanium profile does not have a sharp interface (where the dislocations are generated) between SiGe and Si, dislocations are not easily produced. This can reduce leakage of devices caused by dislocations. Graded germanium profiles also provide a method to optimize stress in order to enhance device performance.”), 3:18-25, 5:7-22; EX1008, [0024] (“use of a strained high germanium compound film

motivated a POSITA to implement further grading within each of layers 60/70 and/or layers 63/73 to increase stress (e.g., compressive strain) applied to the channel region, thereby increasing the mobility of charge carriers and conductivity in the channel region.¹³ EX1005, [0140]; *infra*, Ground 1B at Claims [1], [6].

including a graded transition layer in the source/drain (S/D) regions of a pMOS device can provide the combined effect of contact resistance reduction and mobility enhancement resulting from the strained configuration”), FIGS. 14-15; EX1019, [0123] (“Typically, we need a relatively high Ge concentration ... in the stressor to induce sufficiently high stress in the channel. However, this may cause a lot of defects (such as stacking fault, dislocations, misfits, etc.) in the stressor film, especially at the SiGe/Si interface. ... Hence, by having a graded Ge stressor region, e.g. low Ge concentration at the SiGe/Si interface[] ... the epitaxy quality will improve ...”).

¹³ The use of silicon-germanium compounds to impart strain on the channel region of a MOSFET for the purpose of increasing the mobility of charge carriers and increasing the conductivity of the channel was well known and commonly implemented before the '178 Patent. *See, e.g.*, EX1016, 10 (“When silicon is allowed to deposit on top of a substrate with atoms spaced farther apart than in silicon lattice, the atoms in silicon are naturally stretched to align with the substrate atoms underneath, leading to 'strained silicon.' Moving these silicon atoms farther apart reduces the atomic forces that interfere with the movement of electrons through the transistors, subsequently resulting in better chip performance and lower energy consumption Strained silicon strategy involves either inserting germanium atoms into silicon lattice or adding intermediate layer of silicon-germanium compound semiconductor.”); EX1017, [0042] (“stress increases the strain within the channel region 205, thereby increasing mobility in the channel and increasing drive current”), [0040] (“deciding whether to induce a tensile stress or a compressive stress will depend on whether an NMOS or a PMOS transistor is being formed”); EX1008, [0024] (“use of a strained high germanium compound film including a graded transition layer in the source/drain (S/D) regions of a pMOS device can provide the combined effect of contact resistance reduction and mobility enhancement resulting from the strained configuration”), FIGS. 14-15; EX1033, [0006] (“The higher the Ge concentration, the larger the strain and thus better

[1g] a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;

85. The combined teachings of Tezuka and Tung would have rendered obvious a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising Si, Ge, and Ti, based on the teachings of Tezuka in view of Tung.

86. Tezuka discloses that “[a] metal compound layer (NiGeSi or the like) having a thickness of about 5 to 20 nm may be formed on the surface of the source / drain regions 60 and 70.” EX1005, [0120]. A POSITA would have known and it would have been obvious that Tezuka’s metal compound layer would provide electrodes or contacts to the source and drains of the FinFET so that electrical signals could be coupled to the source and drain from external circuitry.¹⁴ For example,

performance”), [0005] (“As the atoms in the silicon layer align with the atoms of the underlying silicon germanium layer, which are arranged farther apart with respect to those of a bulk silicon crystal, the links between the silicon atoms become stretched- -thereby leading to strained silicon.”), [0089]-[0094]. A common and well-known approach to using SiGe material to impart strain in a non-planar device (e.g., a FinFET) involved epitaxially growing or re-growing SiGe source and drain regions over a substrate on either side of the channel such that the SiGe source and drain regions would abut S/D sidewalls of the fin in the channel region. *See, e.g.*, EX1017, [0040], FIGS. 6A-6B, 7; EX1007, [0017]-[0019], FIG. 3; EX1008, [0024], [0051], FIGS. 11-12 and *generally* [0044]-[0058]; EX1005, [0120]-[0121], FIG. 8.

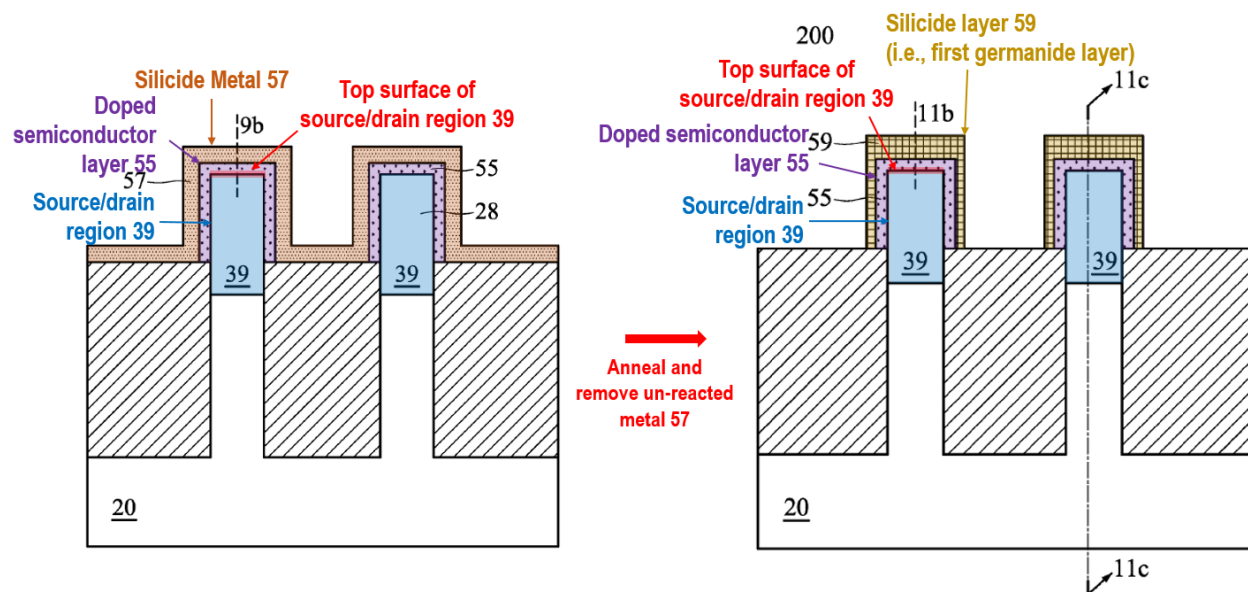
¹⁴ Integrated circuits typically include one or more layers of wiring and interconnect structures above a layer of semiconductor components (e.g., a transistor). The semiconductor components can be connected in a circuit formation by the interconnect structures, which commonly include metal contact plugs that extend

with respect to its planar embodiments, Tezuka teaches that “source/drain **electrodes** 65 and 75 made of NiGe **germanide**” are formed “after Ni and Ge are reacted by heat treatment.” EX1005, [0066], FIGS. 5(e)-(f). It would have been obvious that Tezuka’s “metal compound layer” in its non-planar embodiments would similarly couple the source/drain regions of the FinFET to external circuitry, i.e., a fact that is further suggested by Tezuka’s disclosure that the FinFET “is completed through a normal wiring formation process” that would predictably involve coupling external conductors to the source and drain regions through the metal compound layer. *Id.*, [0137], [0143].

87. To the extent Tezuka does not specifically teach that the metal compound layer is formed over respective **top** surfaces of the source and drain layers 60/70, a POSITA would have found it obvious to do so based on Tung. As shown in FIGS. 9a and 11a, Tung’s metal 57 and doped semiconductor layer 55 are

from a higher interconnect layer to a metal compound such as a silicide or germanide on the source and drain regions of the transistor to form electrical connections. *See, e.g.*, EX1009, FIG. 1 (depicting contact plugs 55 extending down through openings in a dielectric layer 10 to metal alloy contacts 20 on source and drain regions 40/45 of a transistor); EX1026, 1 (“Silicide has been the preferred material for contact to the source/drain (S/D) regions of silicon field effect transistor (FET) devices for many year.”), FIG. 1; EX1029, 10 (“Electrical connections must be made between any semiconductor device or an integrated circuit, and the outside world. These connections are made via *ohmic contacts*. An ohmic contact is a low resistance junction providing similar conduction in both current directions between the metal and the semiconductor”).

deposited around all sides of each source/drain region 39, including over a top surface of the source/drain region 39. EX1006, FIGS. 9a, 11a, [0059]-[0065]; see *also id.*, [0039]-[0045], FIGS. 4a-4d. As a result, a germanide layer 59 is formed around all sides of the source/drain region 39, including the top surface:



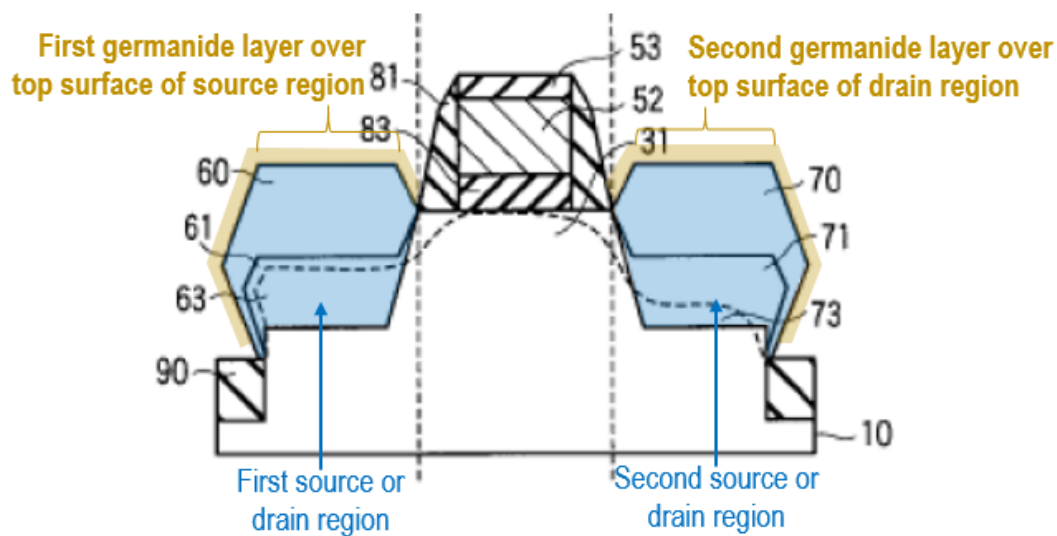
Tung, FIGS. 9a (left, annotated), 11a (right, annotated)

See also EX1006, FIGS. 4a-4e, 15-16.

88. In the combination, it would have been obvious based on Tung to form Tezuka's "metal compound layer" (i.e., germanide layer¹⁵) around the sides and top surface of the first and second source or drain regions (or at least over the top surface), similar to Tung's germanide layer 59, as illustrated below this paragraph. Although Tung's FIG. 11a shows a portion of doped semiconductor layer 55 that

¹⁵ *Infra*, Footnote 18.

remains after the annealing process, Tung also provides that “all of the doped semiconductor layer 55 may be consumed” by the annealing. EX1006, [0045], [0081]. Thus, to the extent required by the claim, the metal compound layer in the Tezuka-Tung FinFET can be positioned directly over a top surface of the first and second source or drain region without an intervening semiconductor layer 55 remaining after the anneal.



Tezuka, FIG. 8(b) (modified and annotated)

89. It would have been obvious and a POSITA would have been motivated to implement Tezuka’s germanide layer over a **top surface** of the source and drain regions to align the germanide layer with the location of contact plugs that would ordinarily be formed in vias above a silicide or germanide layer of the source and

drain regions of a multi-gate (non-planar) FET.¹⁶ A POSITA also would have appreciated that the top surfaces of Tezuka's source and drain regions provide the widest surfaces of the source and drain regions when viewed from the top of the FET, and therefore, forming germanide layers over the top surfaces would have been more practical and beneficial to increase the surface area by which metal plugs filled from atop the FET would contact the germanide layers. Increasing the surface area of the contact would have been beneficial to reduce contact resistance given that contact resistance was known to be inversely proportional to the contact area.¹⁷

90. Tezuka discloses that its germanide layer can include "NiGeSi or the like." EX1005, [120]. By annealing a metal directly over layers 60 and 70 of the first and second source and drain regions—which are comprised of a silicon-germanium alloy—the metal compound layer (i.e., germanide layer) that results from the annealing would include both the deposited metal and the Si and Ge from layers 60 and 70. This follows because annealing causes a chemical reaction between the deposited metal and the underlying semiconductor material to form a chemical compound made of the same atoms as the original metal and

¹⁶ *Supra*, Footnote 14.

¹⁷ In general, contact resistance is inversely proportional to the size of the contact. EX1029, 70 ("It can clearly be seen that R_K ... decreases with increasing contact size."), 10-11.

semiconductor material. Tung confirms that Ti was a known and suitable metal for use in forming germanide over a source and drain region of a FinFET. EX1006, [0042] (“The silicide metal 57 comprises Ni, Pd, Pt, Pa, Co, **Ti**, Al, Au, Lanthanoids ..., or combinations thereof.”), [0061], [0080], Abstract. As described above (Section VIII.A.1), it would have been obvious to use Ti in forming the metal compound layer over the source and drain regions of the FinFET in the Tezuka-Tung combination.

91. Further, as explained above (Section VIII.A.2), it would have been obvious to form Tezuka’s metal compound layers as germanide layers by annealing a metal (including Ti) over a doped Ge cap layer as taught in Tung (rather than depositing the metal directly over a surface of the source and drain regions). As discussed above, Tung describes techniques for forming a metal germanide layer 59 analogous to Tezuka’s metal compound layer by first growing a cap layer 55 over source and drain regions 39, depositing a metal 57 over the semiconductor layer 55, and annealing the metal 57 over layer 55 to form metal silicide 59. EX1006, [0078]-[0082], [0039]-[0045], FIGS. 4, 13-16. Tung explains that semiconductor layer 55 can be doped Ge; semiconductor material 51 can be epitaxially grown SiGe grown over source/drain regions 39; and silicide metal 57 can include Ti. *Id.*, [0040], [0042], [0061], [0058], [0074], [0078], [0080]. In this case, it would have been

obvious that the germanide¹⁸ layer 59 that results from annealing would comprise Ti, Si, and Ge. Titanium would be present in germanide layer 59 from the deposition of metal 57, Ge would be present at least from the Ge cap 55, and Si would be present from the SiGe material 51.

92. In particular, as to the presence of Si in the metal compound layers (i.e., germanide layers) of the FinFET in the Tezuka-Tung combination, the presence of Si would have been obvious in several ways.

93. First, Tung teaches that the cap layer 55 can be formed from “doped Ge,” and further that germanide layer 59 is formed by annealing a metal (e.g., Ti) over cap layer 55 until the interface of germanide layer 59 extends some amount into SiGe material 51 of the source/drain region 39. EX1006, [0045] (“the silicide interface moves beyond the doped semiconductor layer 55 and into the semiconductor material 51”), [0081]. Consistent with these teachings, in the combination, the metal compound layers that would result from annealing would

¹⁸ Tung uses the term “silicide” to refer to layer 59 generically, despite the presence of Ge and regardless of the actual composition of materials in layer 59. However, a POSITA would have understood that Tung’s layer 59 would more precisely be a “germanide” layer when it is formed by annealing with a **germanium** cap layer 55 such as “doped Ge.” EX1006, [0058], [0078]; EX1001, 9:34-42, 10:43-50, 12:21-27, 16:14-17; EX1030, [0002] (describing “germanides” as “a compound of germanium and a metal”), [0015] (“Germanides, i.e. a compound resulting from the reaction between germanium and a metal, e.g. Ni, are used to ... reduce the resistivity of the source and drain regions ...”), [0019] (“preferred metals that are considered to form a metal-germanide compound” include Ti).

include Si originating from the SiGe material of the source/drain layers 60/70 (and would further include Ge and Ti as described above). EX1006, [0058], [0078].

94. Second, Tung teaches that “all of the doped semiconductor layer 55 may be consumed by the silicidation process” when annealed. EX1006, [0045]. When all of cap layer 55 is consumed without the interface of the resulting germanide layer 59 extending into the source/drain regions themselves (e.g., without extending into source/drain layers 60/70 of the Tezuka-Tung FinFET), the lower surface of germanide layer 59 would contact the respective outer surfaces of source/drain layers 60/70. In this case, it would have been obvious that at least some Si near the outer surfaces of the source/drain layers 60/70 that contact the germanide layers 59 (metal compound layers) would migrate into the metal compound layers due to metal-silicon bonds being stronger and more stable than metal-germanium bonds. When comparing elements of the same column of the periodic system of elements, a lighter element (such as Si) forms stronger bonds and is thermodynamically favorable over a heavier element (such as Ge). This thermodynamic trend represents a driving force for Si to be incorporated into the metal-germanide compound. In general, Si (and silicon-compounds) is more stable than Ge (and germanium-compounds). For example, Si has a bandgap energy of 1.12 eV whereas Ge has a bandgap energy of only 0.66 eV. Consistent with this fact, the paper entitled “Lattice stability and point defect energetics of TiSi_2 and

TiGe₂ allotropes from first-principles calculations,” by Brown, reports a higher reaction enthalpy (heat of formation) for the C54 TiSi₂ allotrope than for C54 TiGe₂ allotrope. As a result, germanide layers 59 in the combination would include Ti, Ge, and Si. EX1037, 2-3.

95. Third, it would have been obvious for the Ge cap layer 55 itself to include a small amount of Si such that the metal compound layers formed by annealing Ti with the cap layer 55 would naturally include Si along with Ti and Ge, regardless of whether cap layer 55 is entirely consumed by annealing. Indeed, Tung not only teaches that cap layer 55 can be “doped Ge,” but further teaches that cap layer 55 can include “doped SiGe” material. EX1006, [0058], [0078]. Given that both doped Ge and doped SiGe are identified in Tung as suitable materials for cap layer 55, it would have been obvious to select a material for cap layer 55 formed predominantly of Ge (e.g., in excess of 90% Ge) to make beneficial use of well-known intrinsically favorable properties of Ge (e.g., a lower band gap and Schottky barrier height that would tend to yield lower contact resistance to the source/drain regions) while still making beneficial use of Si (e.g., to lower the gap in Ge content and reduce dislocations at the interface of the resulting germanide layer 59 and the source/drain regions). See Footnotes 4, 23. At minimum, it was known before the Critical Date that a wide range of concentrations of Ge in cap layers were suitable for forming contact structures to source/drain regions, and it would have been

obvious to select a high concentration of Ge (e.g., in excess of 90%) to optimally reduce contact resistance and the concentration of dislocations/defects in the contact structures to the source/drain regions. See, e.g., EX1036, [0038] (describing a film 410 formed over the source and drain regions of a FinFET and “comprise[d] [of] approximately 1 to 99 atomic percent of the alloy and can even extend to pure (100%) Ge”), FIGS. 4A-4B; see also *id.*, [0074]-[0078] (describing an analogous film 542 that is “consumed during the formation of a silicide film on the source and drain regions”), FIG. 5P.

[1h]-[1l] a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

96. The Tezuka-Tung combination would have rendered obvious the additional features recited in [1h]-[1l] for substantially the same reasons discussed above with respect to [1c]-[1g].

97. For example, Tezuka discloses, and the combination provides, a drain region 70 and a drain ground layer 73 (i.e., collectively, “a second source or drain region”) opposite the first side of the gate electrode 50. EX1005, [0117]-[0121], [0138]-[0143], FIGS. 8, 17. According to Tezuka, drain region 70 and drain ground layer 73 exhibit substantially the same properties as source region 60 and source

ground layer 63 (i.e., collectively “a first source or drain region”), and thus regions 70/73 similarly (i) include two or more facets and a top surface and (ii) comprise Si and Ge with a Ge concentration graded to a concentration in excess of 50%. *Id.*; *supra*, [1d]-[1f]. A second germanide layer over the top surface of drain region 70, and comprising Si, Ge, and Ti, also would have been obvious based on the teachings of Tezuka in view of Tung, as described above with respect to [1g].

2. Claim 4

98. Claim 4 of the '178 Patent recites:

4. The integrated circuit structure of claim 1, wherein the fin comprises a strained channel between the first and second source or drain regions.

99. Tezuka describes and would have rendered obvious the additional features recited in [4]. For example, Tezuka discloses that “source region 60 and a drain region 70 ... [have] a composition ratio different from that of the substrate 10 and the ground layers 63 and 73, and [have] a different lattice constant,” so that “[a] force is applied to the channel region of fin 31 by the source/drain regions 60 and 70.” EX1005, [0119]; *see also id.*, [0120]-[0121], [0138] (“strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction)”), [0140] (“the source/drain regions 60 and 70 have a preferable Ge composition range of 50% to 90%[] ... from the viewpoint of generating as large a stress as possible”), Claim 5 (FinFET in which “stress is applied to the channel

region in the channel length direction”), FIG. 8 (showing channel in fin between first and second source/drain regions); *see also id.*, [0002]-[0003], [0005], [0031]-[0034], [0146], [0151], Claims 4-5 (“compressive strain”).

3. Claim 5

100. Claim 5 of the ’178 Patent recites:

5. The integrated circuit structure of claim 1, wherein the first and second source or drain regions are P-type.

101. Tezuka describes and would have rendered obvious the additional features recited in [5]. For example, Tezuka discloses that the first and second source or drain regions (i.e., 60/63 and 70/73) can be p-type.¹⁹ EX1005, [0138] (“strained Si-pMOSFET”), [0139] (“both source region 60 and the drain region 70 are ... doped with B as a p-type impurity at a high concentration”), [0143] (“B is used as the source/drain impurity”); *see also id.*, [0032], [0039], [0046], [0145].

¹⁹ Notably, the ’178 Patent broadly describes how “the source/drain regions can be implemented with any number of suitable processes and configurations” and can be “**p-type and/or n-type**”—thus indicating that the source and drain regions can include both p-type and n-type doping. EX1001, 8:60-66 (emphasis added). It follows that, in the context of the ’178 Patent, a source or drain region is not restricted to a region with a single p-type or n-type doping. Often, for example, a region includes both n-type and p-type impurities, and “the impurity present in a higher concentration determines the type of conductivity in the semiconductor.” EX1028, 9 (“If donor and acceptor impurities are introduced together, the impurity present in a higher concentration determines the type of conductivity in the semiconductor.”). To form a “strained Si-pMOSFET” as taught in Tezuka, it would have been obvious for the upper layers 60 and 70 of the source and drain regions to have a higher concentration of p-type impurities than n-type impurities in ground layers 60 and 70.

4. Independent Claim 6

102. Claim 6 of the '178 Patent recites:

6. An integrated circuit structure, comprising:
a body comprising silicon;
a gate electrode over the body;
a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises
a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

103. The Tezuka-Tung combination would have rendered obvious and taught each element of claim 6 as described below.

[6pre] An integrated circuit structure, comprising:

104. For the reasons discussed above with respect to [1pre], the Tezuka-Tung combination would have rendered obvious [6pre].

[6a] a body comprising silicon;

105. For the reasons discussed above with respect to [1pre], the Tezuka-Tung combination would have rendered obvious [6a], e.g., in view of Tezuka's

disclosure of a fin comprising Si. *See supra*, [1a], [1c], [1h]. For example, just as the specification of the '178 Patent identifies structure 660 alternately as a “body” or a “fin,” the same structures from Tezuka that would have rendered obvious a “fin” also would have provided the recited “body” in claim 6. *Cf.* EX1001, 13:24-27, FIG. 6.

[6b]-6[l] a gate electrode over the body; a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second source or drain region in the body proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

106. For the reasons discussed above with respect to [1b]-[1l], the Tezuka-Tung combination would have rendered obvious [6b]-[6l].

5. Claim 9

107. Claim 9 of the '178 Patent recites:

9. The integrated circuit structure of claim 6, wherein the body comprises a strained channel between the first and second source or drain regions.

108. For the reasons discussed above with respect to [4], the Tezuka-Tung combination would have rendered obvious [9].

6. Claim 10

109. Claim 10 of the '178 Patent recites:

10. The integrated circuit structure of claim 6, wherein the first and second source or drain regions are P-type.

110. For the reasons discussed above with respect to [5], the Tezuka-Tung combination would have rendered obvious [10].

IX. [GROUND 1B] Tezuka in Combination with Tung and Simonelli Renders Obvious Claims 1-10

Claims [1], [6]

111. As explained above in Ground 1A, the Tezuka-Tung combination would have rendered obvious independent claims 1 and 6 when Tezuka's ground layer 63 and source region 60 are collectively mapped to the claimed "first source or drain region" and when Tezuka's ground layer 73 and drain region 70 are collectively mapped to the claimed "second source or drain region."

112. Alternatively, a POSITA would have understood that Tezuka's source region 60 and drain region 70 alone (without the ground layers 63 and 73) would provide the claimed first and second source or drain regions, and in this case, a combination based on Tezuka, Tung, and Simonelli would have rendered obvious claims 1 and 6.²⁰ Tezuka discloses that the source and drain regions 60 and 70 are

²⁰ Apart from the alternative mapping for the first and second source or drain regions, the combination based on Tezuka, Tung, and Simonelli would have disclosed and rendered obvious each of the other elements of claims 1 and 6 for substantially the

composed of SiGe with a “preferable Ge composition range of 50% to 90%” (i.e., in excess of 50%). EX1004, [0140].

113. Simonelli teaches that the Ge concentration in the source/drain regions of a multi-gate device like Tezuka’s FinFET can be graded from a lower concentration to a higher concentration. EX1008, [0051], [0053]-[0058], FIGS. 14-15. It would have been obvious to modify Tezuka’s device by grading the Ge concentration in regions 60/70 as taught in Simonelli, and a POSITA would have been motivated to grade the Ge concentration in Tezuka’s source/drain regions 60/70 to achieve known and predictable benefits. Simonelli explains, for example, that “use of a strained high germanium compound film including a graded transition layer in the source/drain (S/D) regions of a pMOS device can provide the combined effect of contact resistance reduction and mobility enhancement resulting from the strained configuration.” EX1008, [0024]. Moreover, although Tezuka’s original solution provides a relatively high concentration of Ge in source/drain regions 60/70 (i.e., 50%-90% Ge), a POSITA would have understood that the size and thickness of ungraded source/drain regions 60/70 would be limited for higher Ge contents if crystalline defects and dislocations at the interfaces of layers 60/63 and 70/73 are to

same reasons discussed above in Ground 1A. Since both of the alternative mappings for the first and second source or drain regions apply in Ground 1B, claims 2-10 also would have been rendered obvious under both mappings.

be avoided due to overly high lattice mismatch. By contrast, Ge grading in the source/drain regions 60/70, as taught in Simonelli, would have allowed the device to achieve high Ge concentrations and thicker films grown over larger areas without or with fewer dislocations. Reducing the concentration of defects and dislocations with thicker films grown over a larger growth area would have been desirable to maximize the compressive strain imparted by the high Ge content in the uppermost portions of the source/drain regions 60/70.²¹

114. A POSITA would have had a reasonable expectation of success implementing a graded Ge content in Tezuka's source/drain regions 60/70, especially since the graded Ge content would be applied to the Tezuka-Tung-Simonelli device in substantially the same context described in Simonelli—i.e., in epitaxially grown SiGe source/drain regions of a non-planar multi-gate FET. See EX1008, [0051], [0053]-[0055], FIG. 12; EX1005, [0138]-[0143], [0136]. Tezuka also already employs Ge grading between ground layers 63/73 and upper layers 60/70 to obtain high Ge content in the upper layers 60/70.

Claim [2]

115. Claim 2 of the '178 Patent recites:

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

²¹ *Supra*, Footnotes 12-13.

116. The teachings of Tezuka and Simonelli in the combination would have rendered obvious [2].

117. Tezuka teaches that the first and second source and drain regions, and regions 60 and 70, can be “doped with B as a p-type impurity at a high concentration.” EX1005, [0139]; *see also id.*, [0032], [0039], [0065], [0102], [0145]; *supra*, Ground 1A, [1c], [1h]. To the extent that Tezuka and Tung do not expressly disclose that the doped “boron concentration [is] greater than $1E20$ ” this feature would have been obvious in the combination based on Simonelli.

118. For example, Simonelli describes a “multi-gate device 600” such as a tri-gate or dual-gate FinFET (similar to Tezuka’s transistor 400) having “epitaxially form[ed] source and drain regions 1210.” EX1008, [0051]; *see also id.*, [0045]-[0051], FIGS. 6-12. “The epitaxially formed source/drain regions 1210 may be formed using a graded high-germanium content silicon film stack 1400.” *Id.*, [0051]. In Simonelli’s film stack 1400, higher layers in the stack are formed with increasing concentrations of Ge and are doped with increasing concentrations of boron (B). *Id.*, [0053]-[0058], FIGS. 14-15. In each layer, however, and even including the “seed layer” with the lowest concentrations of Ge and B, Simonelli describes a B concentration in excess of 1×10^{20} atoms/cm³. *Id.*

119. In view of Simonelli’s teachings, a POSITA would have found it obvious to dope Tezuka’s first and second source and drain regions, including at

least regions 60 and 70, with B at a concentration greater than 1E20. It is fundamental in semiconductor physics that doping of the source/drain regions in a MOSFET with p-type impurities such as B yields holes as charge carriers that facilitate conduction of an electric current along a channel.²² Hence, Tezuka teaches that the source/drain regions 60/70 should be “doped with B as a p-type impurity at a high concentration” to form “Si-pMOSFET.” EX1005, [0138]-[0140]. A POSITA would have looked to Simonelli’s teaching of a B concentration of greater than 1E20 to obtain further detail on B concentrations consistent with Tezuka’s instruction to dope with B at a high concentration, particularly since Simonelli describes a similar MOSFET device. Higher concentrations of B doping also would have promoted a lower contact resistance in electrodes formed by reacting a metal with the boron-doped source/drain regions 60/70.²³

²² See, e.g., EX1028, 1 (“Without exaggeration almost all of the basic MOSFET parameters are affected by the distribution of dopants in the device. Doping refers to the process of introducing impurity atoms into a semiconductor region in a controllable manner in order to define the electrical properties of this region.”), 7 (“Boron is referred to as an acceptor impurity and doping with boron forms a p-type semiconductor.”), 7 (“dopant impurities used in controlling the conductivity type of a semiconductor”); EX1006, [0027] (“the dopant rich region 56 is heavily doped so as to minimize [the series] resistance”).

²³ Stavitsky describes how the “dopant level” and “Schottky barrier height” of a metal compound layer “determines the electrical characteristics of silicide-to-silicon junctions, i.e. the contact resistance.” EX1029, 5. Thus, the specific contact resistance of an ohmic contact is a function of both “the choice of the metal” and “the dopant level in the semiconductor.” *Id.*, 10-11, 20 (“the dopant level in the

120. A POSITA would have understood dopant concentrations in the source/drain regions of a MOSFET like that in the combined device taught by Tezuka, Tung, and Simonelli to be a result-effective variable impacting the conductivity and ON-current of the transistor.²⁴ Accordingly, it would have been obvious to apply Simonelli's suggested B doping to a concentration in excess of $1E20$ in the first and second source or drain regions so as to optimize the conductivity of the resulting device, which a POSITA would have arrived at through routine optimization and experimentation. A POSITA would have had a reasonable expectation of success implementing doping at a concentration in excess of $1E20$,

semiconductor determines the actual contact resistance to a large extent"). Higher concentrations of dopants in the semiconductor from which the silicide or germanide contact is formed generally leads to lower contact resistance. *Id.*, 52 ("It was found that [the specific contact resistance] decreased with increasing As or B concentrations, as expected from Eq. 1.9 ..."), 10-11. The relationship between higher impurity concentrations and lower contact resistance observed in Stavitsky similarly led Simonelli and Tung to use high concentrations of impurities in the semiconductor material over which a metallized contact is formed. See EX1008, [0024] ("use of a strained high germanium compound film including a graded transition layer in the source/drain (S/D) regions of a pMOS device can provide the combined effect of contact resistance reduction and mobility enhancement resulting from the strained configuration"), [0058] ("The high germanium content layer 1430 may optionally be doped with boron to a concentration ranging between 2.0×10^{20} atoms/cm³ to 3.0×10^{20} atoms/cm³."), FIGS. 14-15; EX1006, [0027]-[0028] ("the dopant rich region 56 is heavily doped so as to minimize [the series] resistance"), [0034] ("the doped semiconductor layer 55 is doped to a concentration greater than about 1×10^{18} cm⁻³, and greater than about 5×10^{19} cm⁻³ in another embodiment").

²⁴ *Supra*, Footnote 22.

particularly since Simonelli's teaching is applied in the combination to a similar non-planar MOSFET. Based on my review, the '178 Patent discloses nothing critical or unexpected about doping the source/drain regions with B to a concentration greater than 1E20.

Claim [3]

121. Claim 3 of the '178 Patent recites:

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.

122. The teachings of Tezuka and Simonelli in the combination would have rendered obvious [3]. As discussed above with respect to claim 2, Tezuka teaches that a portion of the first and second source or drain regions (i.e., regions 60 and 70) can be "doped with B as a p-type impurity at a high concentration," and it would have been obvious based on Simonelli for the B concentration in regions 60 and 70 to be greater than 1E20 (i.e., 1×10^{20} atoms/cm³). *Supra*, [2]; EX1005, [0139]. By contrast, Tezuka explains that the lower portions of the first and second source or drain regions (i.e., ground layers 63 and 73) are made of an n-type SiGe alloy, and are not doped with B like the upper portions of the first and second source or drain regions (i.e., regions 60 and 70). EX1005, [0139]. Therefore, the first and second source or drain regions in the combination would have a B concentration graded

from a base level (e.g., no B) in the ground layers 63 and 73 to a concentration in excess of $1E20$ in upper regions 60 and 70.

123. To the extent that claim 3 requires further non-zero gradations of B, such features would have been obvious based on Simonelli. Simonelli discloses a silicon-germanium (SiGe) film stack 1400 for use in, among other things, source or drain regions in a FinFET. EX1008, [0044]-[0058], FIGS. 6-15. Simonelli's film stack includes graded concentrations of B as follows:

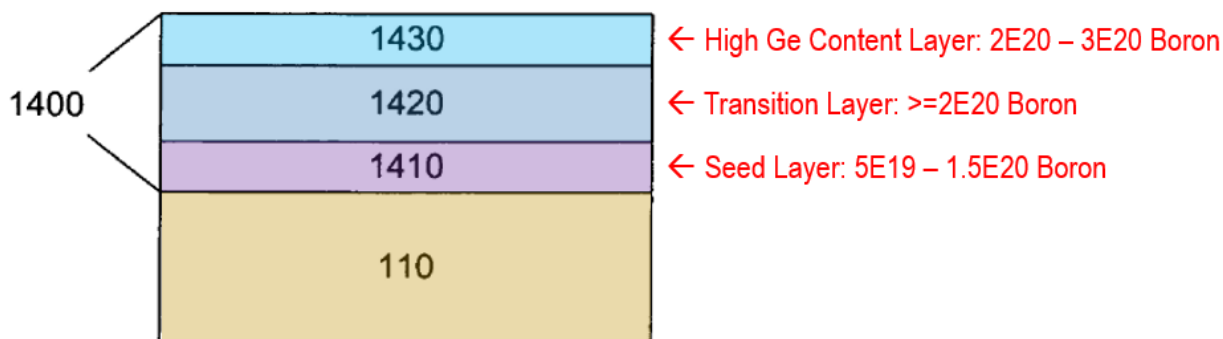


FIG. 14

Simonelli, FIG. 14 (annotated)

124. It would have been obvious based on Simonelli to similarly grade the concentration of B from a base level to a level in excess of $1E20$ in Tezuka's source and drain regions 60 and 70, and a POSITA would have been motivated to implement Simonelli-like grading in the combination to maintain proportionality between the concentrations of B and Ge in each graded SiGe layer within source/drain regions 60/70. *See supra*, Ground 1B at [1], [6]. A POSITA would

have sought to maintain this proportionality to gain the benefit of higher B concentrations that could be accommodated by crystalline structures with higher Ge content, while also avoiding overly high concentrations of B in lower portions of the graded source/drain regions with lower Ge content (especially since overly high B levels can produce precipitations and defects, and B more easily diffuses in Si than Ge).²⁵ For example, increasing B concentration in regions of higher Ge would have been advantageous to increase conductivity and obtain higher levels of electrical activation without undue B diffusion. *See, e.g.*, EX1035, 3 (“[It] has become clear that the B diffusivity in Ge was extremely low, up to 5 orders of magnitude lower than in Si at homologous temperatures, and that a very high electrical activation level can be obtained, well higher than in Si.”). The graded B concentration would also be beneficial for reducing the series resistance in layers with high Ge concentration, and to allow the carrier profile to be tuned such that the B concentration is higher in the stressor regions and lower elsewhere to reduce junction capacitance.²⁶

²⁵ *Supra*, Footnote 23.

²⁶ It was known, as evidenced by Chong, for example, that “[t]ypically, we need a relatively high Ge concentration ... in the stressor to induce sufficiently high stress in the channel,” although “this may cause a lot of defects (such as stacking fault, dislocations, misfits, etc.) in the stressor film, especially at the SiGe/Si interface.” EX1019, [0123]. Thus, similar to Simonelli's graded film stack, the concentration of germanium in the source and drain regions can be increased further from the interface with the Si substrate to reduce defects while still providing an effective stressor region. *Id.*, [0107]-[0108], [0123]. Further, the “the B concentration n the

Moreover, a graded B concentration would have been an obvious application of a known technique as taught in Simonelli to Tezuka's device to yield predictable results like those described in Simonelli. A POSITA would have had a reasonable expectation of success implementing the combination since Simonelli and Tezuka contemplate B doping in similar devices using similar processes.

Claim [4]

125. Claim 4 of the '178 Patent recites:

4. The integrated circuit structure of claim 1, wherein the fin comprises a strained channel between the first and second source or drain regions.

126. For the reasons discussed above with respect to Ground 1A at [4], the Tezuka-Tung-Simonelli combination would have rendered obvious [4].

Claim [5]

127. Claim 5 of the '178 Patent recites:

5. The integrated circuit structure of claim 1, wherein the first and second source or drain regions are P-type.

stressor region should be as high as possible to reduce the series resistance" of the transistor, but that "if it is too high, the transistor may suffer from severe short channel effects." *Id.*, [0124]. Thus, a POSITA would have appreciated that a "graded (e.g., B) impurity stressor gives the flexibility to tune the active carrier profile in the S/D region" to achieve concentrations that would minimize the series resistance of the transistor while avoiding undesirable short channel effects that could result from too much doping, especially near the channel region. Further, the graded doping profile would allow "the lowest portion of the S/D region" to "be graded to reduce the junction capacitance." *Id.*

128. For the reasons discussed above with respect to Ground 1A at [5], the Tezuka-Tung-Simonelli combination would have rendered obvious [5].

Claim [7]

129. Claim 7 of the '178 Patent recites:

7. The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration greater than 1E20.
--

130. For the reasons discussed above with respect to [2], the Tezuka-Tung-Simonelli combination would have rendered obvious [7].

Claim [8]

131. Claim 8 of the '178 Patent recites:

8. The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.
--

132. For the reasons discussed above with respect to [3], the Tezuka-Tung-Simonelli combination would have rendered obvious [8].

Claim [9]

133. Claim 9 of the '178 Patent recites:

9. The integrated circuit structure of claim 6, wherein the body comprises a strained channel between the first and second source or drain regions.

134. For the reasons discussed above with respect to Ground 1A at [9], the Tezuka-Tung-Simonelli combination would have rendered obvious [9].

Claim [10]

135. Claim 10 of the '178 Patent recites:

10. The integrated circuit structure of claim 6, wherein the first and second source or drain regions are P-type.

136. For the reasons discussed above with respect to Ground 1A at [10], the Tezuka-Tung-Simonelli combination would have rendered obvious [10].

X. [GROUND 2] – Obviousness based on Tung in view of Simonelli (Claims 1-10)

137. Based on my review, the teachings of Tung in combination with Simonelli would have rendered obvious claims 1-10 of the '178 Patent. The following sub-sections describe obvious modifications of Tung's FinFET in view of Simonelli, including motivations for the modifications, and further describe how the modified FinFET in the combination provides each element recited in claims 1-10.

A. Manner and Reasons to Combine

138. Tung discloses techniques for fabricating a non-planar field-effect transistor ("FET") (e.g., a FinFET) by epitaxially growing a semiconductor material 51 over a fin 28 to form a source or drain region 39. *Supra*, Section VII.B. In certain embodiments, semiconductor material 51 is doped silicon-germanium (SiGe). EX1006, [0040], [0074]. To the extent that Tung is viewed as not explicitly describing numerical values of the Ge content in semiconductor material 51, nor does Tung describe the effects that would predictably result from varying the Ge

content when forming material 51. On the other hand, Simonelli describes techniques for grading the Ge content of SiGe material in the source and drain regions of a FinFET so that a layer of the material closest to the substrate has the lowest Ge content and upper layers of the material in the source and drain regions have increasingly higher contents of Ge (e.g., up to 50-atomic % Ge). *Supra*, Section VII.C.

139. A POSITA would have found it obvious to form Tung's SiGe material 51 in the source and drain regions 39 according to Simonelli's teachings such that the concentration of Ge in the SiGe material 51 would increase from a lowest level near the growth substrate to a highest level furthest from the growth substrate. As explained below, it would have been obvious and multiple reasons would have motivated a POSITA to grade the Ge content in the FinFET of the Tung-Simonelli combination to a concentration in excess of 50%.

140. **First**, a POSITA would have been motivated and would have found it obvious to grade the Ge content in the material 51 of the Tung-Simonelli FinFET to a concentration in excess of 50% to ease the transition between the bulk Si or silicon-rich substrate material (e.g., fin 28 (*see infra* [1a])) over which material 51 is grown and the Ge material of cap layer 55 (e.g., doped Ge or a silicon-germanium cap layer 55 having a very high concentration of Ge). EX1006, [0058], [0078]. Grading the Ge content in semiconductor material 51 in this manner would have yielded

beneficial effects including material on which material 51 is grown, reducing defects through the entire formation of SiGe material 51, and reducing misfit dislocations at the interface between SiGe material 51 and the Ge cap layer 55.²⁷ A POSITA would have appreciated that reducing or even eliminating misfit dislocations and other defects in the growth of semiconductor material 51 would significantly improve performance of the FinFET in the resulting combination, especially since such defects were known to produce unwanted leakage currents, parasitic capacitances, and to prevent or relax forces intended to impart stress on the channel to increase the mobility of charge carriers in the channel and increase ON-currents through the transistor.²⁸

141. Additionally, absent grading between the silicon-rich growth substrate (e.g., fin 28) and the Ge cap layer 55, the thickness and surface area over which semiconductor material 51 could be grown without defects would be severely limited—i.e., a limitation that would in turn risk (i) restricting the ON-current that could flow through the transistor, (ii) increasing contact resistance at the source and drain regions due to decreased growth area, and (iii) limiting the amount of stress that could be imparted on the channel in a strained configuration.²⁹ In contrast, by

²⁷ *Supra*, Footnote 12.

²⁸ *Supra*, Footnotes 11-13.

²⁹ *Supra*, Footnote 12-13.

grading the Ge content in SiGe material 51, lattice mismatch between the silicon-rich substrate material and SiGe material 51 would be reduced to an appropriate amount that would not yield misfit dislocations by ensuring a lower Ge content near the substrate interface. Similarly, lattice mismatch between the Ge cap layer 55 and SiGe material 51 would be reduced by ensuring a higher Ge content near the interface of cap layer 55. For similar reasons, it would have been obvious to implement one or more transition layers in SiGe material 51 as taught in Simonelli (or to implement smooth transitional grading) to bridge the otherwise large difference in Ge content between the silicon-rich growth substrate (e.g., fin 28) and the cap layer 55. Indeed, grading the Ge to a concentration in excess of 50% in SiGe material 51 would have been obvious to bridge the gap in Ge content between the growth substrate and cap layer 55 and to reduce lattice mismatch at the interfaces between the growth substrate, SiGe material 51, and cap layer 55.

142. **Second**, a POSITA would have been motivated and would have found it obvious to grade the Ge content in the material 51 of the Tung-Simonelli FinFET to a concentration exceeding 50% to increase the mobility of charge carriers in the source and drain regions 39, and consequently decrease parasitic resistance in the FinFET. It was well known that the mobility of electrons and holes through Ge is greater than the mobility of electrons and holes through Si, and hence increasing the Ge content in SiGe material 51 would predictably lead to an increase in charge

carrier mobilities in the source and drain regions.³⁰ Increased mobility decreases parasitic resistance and would improve performance of the FinFET.

143. **Third**, a POSITA would have been motivated and would have found it obvious to grade the Ge content in the material 51 to a concentration in excess of 50% to better accommodate high dopant concentrations (e.g., B) with greater dopant confinement and higher electrical activation than would be achieved in a matrix with a higher concentration of Si. *See, e.g.*, EX1035, 3 (“[It] has become clear that the B diffusivity in Ge was extremely low, up to 5 orders of magnitude lower than in Si at homologous temperatures, and that a very high electrical activation level can be obtained, well higher than in Si.”). Furthermore, the smaller bandgap energy of Ge (compared with Si) would result in a lower Schottky barrier height, thereby reducing the contact resistance.

144. **Fourth**, a POSITA would have been motivated and would have found it obvious to grade the Ge content in the material 51 of the Tung-Simonelli FinFET’s

³⁰ *See, e.g.*, EX1031, 1:15-21 (“at normal integrated circuit operating temperatures ..., the drift mobility of electrons and holes in germanium exceeds the drift mobility in silicon by a factor of from 3-10”), 1:26-29 (“the intrinsic resistivity of germanium ... is four orders of magnitude smaller than the intrinsic resistivity of silicon”); EX1024, 454 (“integration of Ge layers in Si-based structures has been considered due to its superior carrier mobilities compared to silicon”); EX1025 (disclosing comparative properties of Si and Ge at room temperature and showing Ge’s lower bandgap energy and higher electron and hole mobilities than Si).

source and drain regions 39 to a concentration in excess of 50% to induce greater stress in the channel region—i.e., a technique that was commonly employed before the '178 Patent to increase the mobility of charge carriers in the channel region of field-effect transistors (which would in turn increases drive currents).³¹ EX1008, [0042]; *see also id.*, [0024], [0038], [0044], [0058].

145. For example, in a p-type FET, when the channel is formed of doped Si and the source and drain regions are formed of an oppositely doped SiGe material, a lattice mismatch results between the materials that induces compressive strain on the channel due to the presence of larger Ge atoms in the source and drain regions. Tung's FIG. 2d, for example, shows how the source and drain regions 39 extend beneath gate spacers 36, and this configuration would have led to compression of the channel region in many typical FETs. EX1006, FIG. 2d; *see also* EX1008, [0038] ("stress in the channel region of the MOS transistor ... is accentuated by depositing the high Ge compound alloy in the source extension cavity 330 and the drain extension cavity 340"), [0044] ("formation of strain-inducing source/drain regions in a non-planar device"), [0042], [0053], [0058], FIGS. 11-12 (depicting source/drain regions 1210 protruding through spacers 1010).

³¹ *Supra*, Footnote 13.

146. To the extent Tung does not expressly disclose that source and drain regions 39 are formed in a manner specifically designed to induce strain in the channel region, it would have been obvious to implement the source and drain regions 39 in this fashion in the FinFET of the Tung-Simonelli combination.³² Strained channel FETs were exceedingly common in both planar and non-planar designs before the '178 Patent, and a POSITA would have sought to implement a strained channel in the Tung-Simonelli FinFET to obtain well-known benefits including increased channel mobility and drive current levels.³³ For example, strained configurations are frequently realized by growing SiGe source and drain regions over a surface or cavity of a substrate on either side of a channel region like Simonelli's source and drain regions 1210. See EX1008, [0051], FIGS. 11-12 (depicting source and drain regions 1210 formed on either side of channel region 110); see also *id.*, [0034]-[0039], [0042], [0044]-[0051]. It would have been obvious to similarly form the source and drain regions 39 by re-growing SiGe material 51 on

³² Although increasing strain in the channel region would have provided an additional motivation to grade the germanium content in the source and drain regions 39 of the Tung-Simonelli FinFET, any modifications made to achieve a strained configuration are not essential to the combination. Multiple other reasons would have independently motivated a POSITA to implement grading in FinFET of the Tung-Simonelli combination, even if such grading did not induce significant strain in the channel region.

³³ *Supra*, Footnote 13.

either side of the channel (e.g., rather than overgrowing SiGe material on fin 28) to impart strain on the channel region according to known and predictable techniques. Indeed, such techniques would have amounted to an obvious use of Simonelli's teachings to improve a similar device (i.e., Tung's FinFET) in a similar way.

147. A POSITA would have had a reasonable expectation of success grading the Ge content in the SiGe material 51 of the Tung-Simonelli FinFET to a concentration in excess of 50%. Simonelli and Tung both describe non-planar FETs (e.g., FinFETs), and both describe techniques for epitaxially growing SiGe material in the source/drain regions of a device. Simonelli's teachings for grading Ge content in the source and drain regions would thus be applied to Tung's FinFET in a substantially similar context. Further, graded epitaxial growth was well known before the '178 Patent,³⁴ and it would have been well within the skill of a POSITA to vary the relative concentrations of Si and Ge during the growth process of SiGe material 51 according to Simonelli's teachings.³⁵ Moreover, for implementations of the Tung-Simonelli combination that involve modifications of Tung's FinFET to

³⁴ *Supra*, Footnotes 11-12.

³⁵ Based on my review, the '178 Patent also lacks any detail as to any special fabrication processes or criticality involved in grading the germanium concentration in the source and drain regions in excess of 50%. These details are instead left to the knowledge and skill of a POSITA. See EX1001, 3:10-17, 4:21-25, 6:39-54, 16:43-44. The '178 Patent discloses that a range of 30-70% germanium would be suitable, for example. *Id.*

achieve a strained channel region, a POSITA would have had a reasonable expectation of success in light of the substantially similar types of FinFET devices described in each of Tung and Simonelli, the long-established practice of introducing strain in the channel regions of FETs using techniques like those disclosed in Simonelli, and Tung's own acknowledgment that a POSITA would have known how to make a range of modifications to its device. EX1006, [0019]-[0020], [0082]-[0084].

B. Claim Element Analysis

1. Independent Claim 1

148. Claim 1 of the '178 Patent recites:

1. An integrated circuit structure, comprising:
 - a fin comprising silicon;
 - a gate electrode over the fin;
 - a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
 - a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
 - a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
 - a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

149. The Tung-Simonelli combination would have rendered obvious and taught each element of claim 1 as described below.

[1pre] An integrated circuit structure, comprising:

150. Tung describes and would have rendered obvious [1pre], e.g., in view of Tung's disclosure of a non-planar field-effect transistor, which a POSITA would have understood to be an integrated circuit structure.³⁶ EX1006, [0002]-[0004].

³⁶ See EX1016, 6 ("In a multi-gate device, the channel is surrounded by several gates on multiple surfaces, allowing more effective suppression of 'off-state' leakage current. Multiple gates also allow enhanced current in the 'on' state, also known as drive current. These advantages translate to lower power consumption and enhanced

Tung, in FIGS. 13-16, for example, describes “various stages of manufacturing” of a non-planar transistor having “a doped semiconductor layer and a metal silicide [] formed on a raised source/drain structure.” EX1006, [0072]; *see also id.*, [0073]-[0082], FIGS. 13-16. Tung further explains that although FIGS. 13-16 “illustrate the fabrication of a device with at least two fins 28,” “the method described in FIG. [sic] 13-16” can also be “used in fabrication of a device with a single fin” to form the device “corresponding to the embodiment described in FIG. 2.” *Id.*, [0082]; *see also id.*, [0032]-[0034], FIG. 2. Tung’s description of FIGS. 4a-4e provides additional detail of a single-fin embodiment consistent with the embodiments described with respect to FIGS. 13-16. *Id.*, [0039]-[0045]; FIGS. 4a-4e.

device performance. Non-planar devices are also more compact than conventional planar transistors, enabling higher transistor density which translates to smaller overall microelectronics.”), 7 (“In the technical literature, FinFET is used somewhat generically to describe any fin-based, multi-gate transistor architecture regardless of number of gates.”); EX1006, [0003] (“Semiconductor devices comprise integrated circuits that are formed on semiconductor wafers by depositing many types of thin films of material over the semiconductor wafers[] ... Integrated circuits include field-effect transistors (FETs)[] ...”), [0004] (“One of the goals of the semiconductor industry is to continue shrinking the size and increasing the speed of individual FETs. To achieve these goals, three dimensional (3-D) or non-planar transistor structures such as fin FETs (FINFETS)[] ... are being investigated for use in sub 22 nm transistor nodes. Such transistors not only improve area[] density, but also improve gate control of the channel.”).

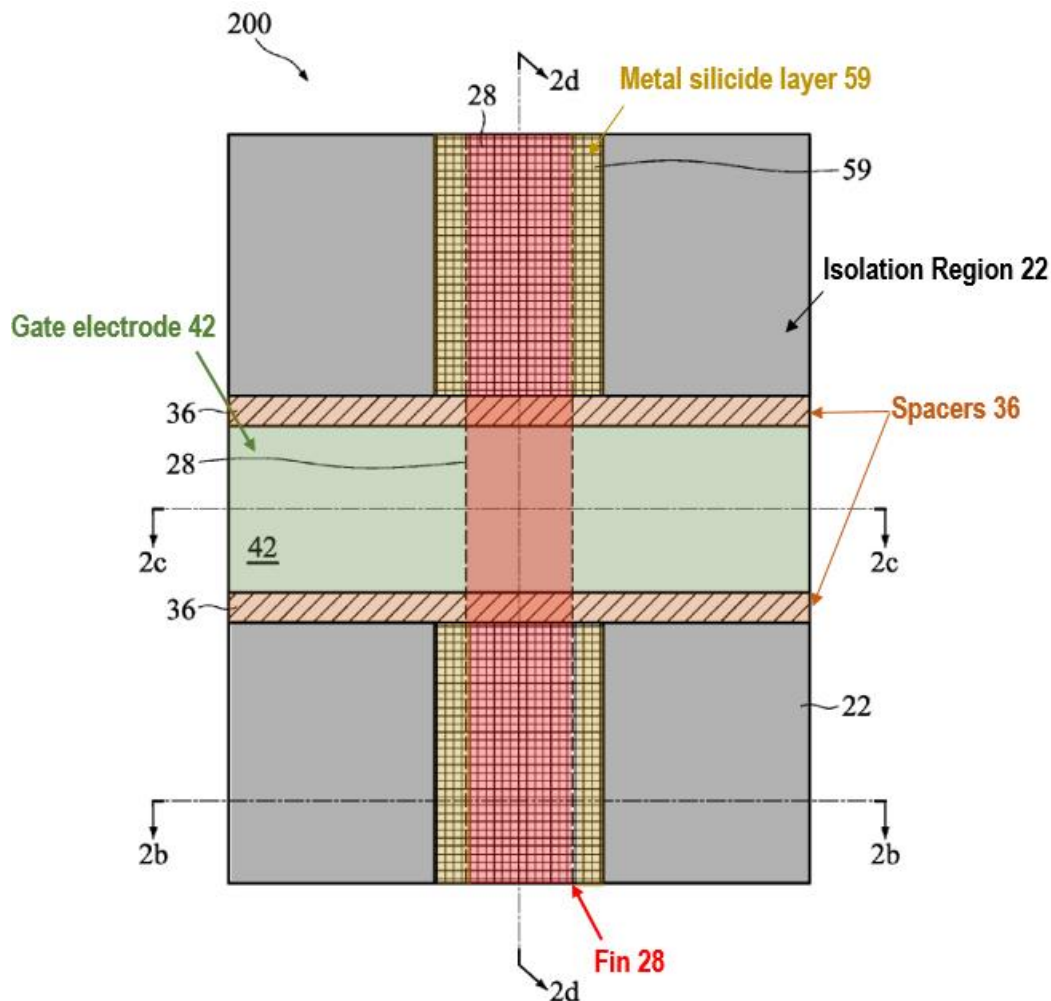


FIG. 2a

Tung, FIG. 2a (annotated)

[1a] a fin comprising silicon;

151. Tung describes and would have rendered obvious [1a], e.g., in view of Tung's disclosure of a fin 28 comprised of Si. Tung teaches that fin 28 can be formed from substrate 20, which Tung explains is made from material including Si. EX1006, [0048] ("substrate 20 comprises bulk silicon" or "substrate 20 comprises bulk silicon germanium (SiGe)"), [0051] ("Fins 28 may be formed by recessing the

top surfaces of the isolation regions 22, and hence leaving the fins 28” of substrate 20), [0049], FIGS. 2, 5, 6a-6b, 13-16; *supra*, [1pre]. Tung also teaches that the source and drain regions 39 can be formed in the fin, and that the source and drain regions 39 can include semiconductor material 51 including Si. EX1006, [0074], [0040], [0033]; *infra*, [1c]/[1h].

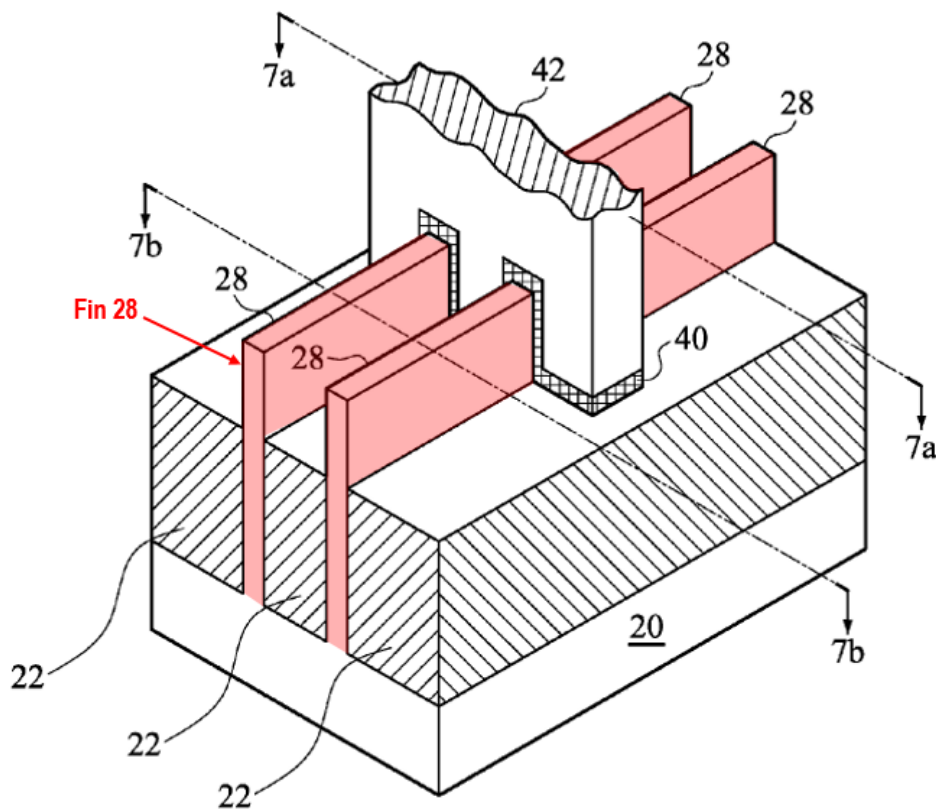


FIG. 7c

Tung, FIG. 7c (annotated)

[1b] a gate electrode over the fin;

152. Tung describes and would have rendered obvious [1b], e.g., in view of Tung's disclosure of a gate electrode 42 over fin 28. EX1006, [0053]-[0055], FIGS. 2a, 2c, 7c.

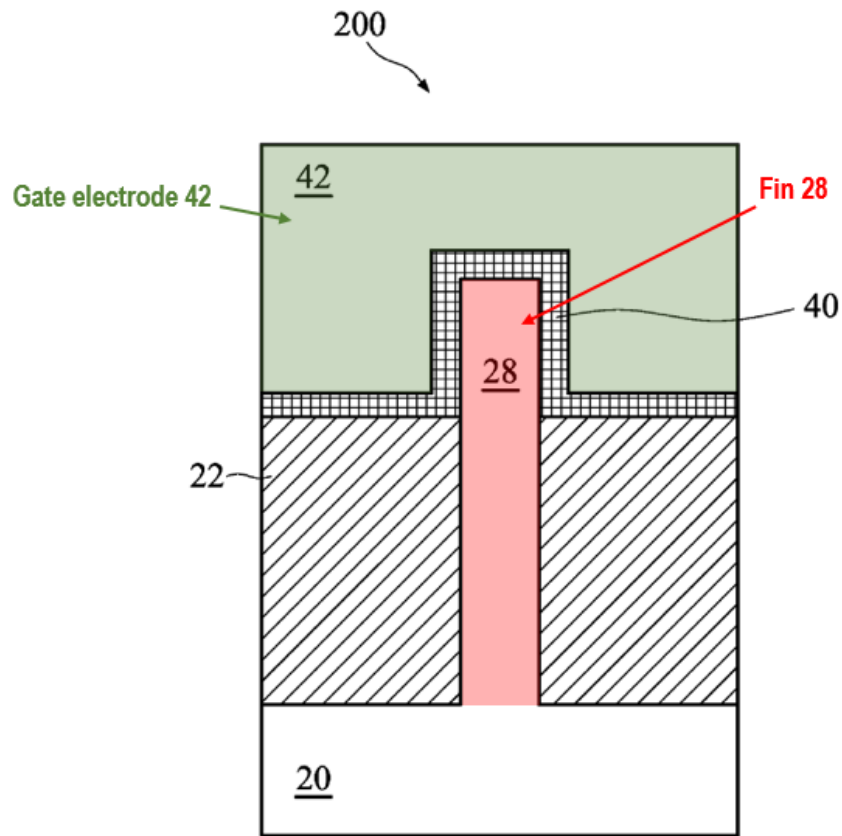


FIG. 2c

Tung, FIG. 2c (annotated)

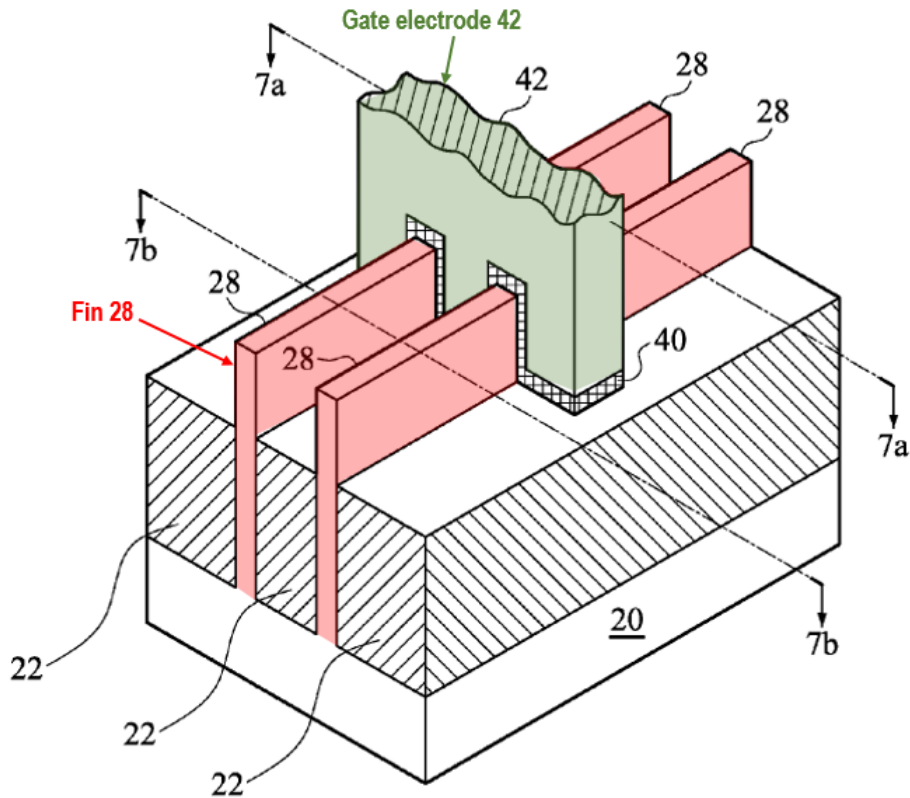


FIG. 7c

Tung, FIG. 7c (annotated)

[1c], [1h] a first source or drain region in the fin proximate a first side of the gate electrode; a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side,

153. Tung describes and would have rendered obvious [1c] and [1h], e.g., in view of Tung's disclosure of first and second source or drain regions 39 formed proximate either side of gate electrode 42. EX1006, [0032]-[0034], [0057], [0074]-[0078], FIGS. 2a, 2d, 8, 13; *supra*, Ground 1A at [1c]; *cf.* EX1001, FIG. 6 (depicting source/drain epitaxial regions 631 similarly proximate to either side of gate electrode 640).

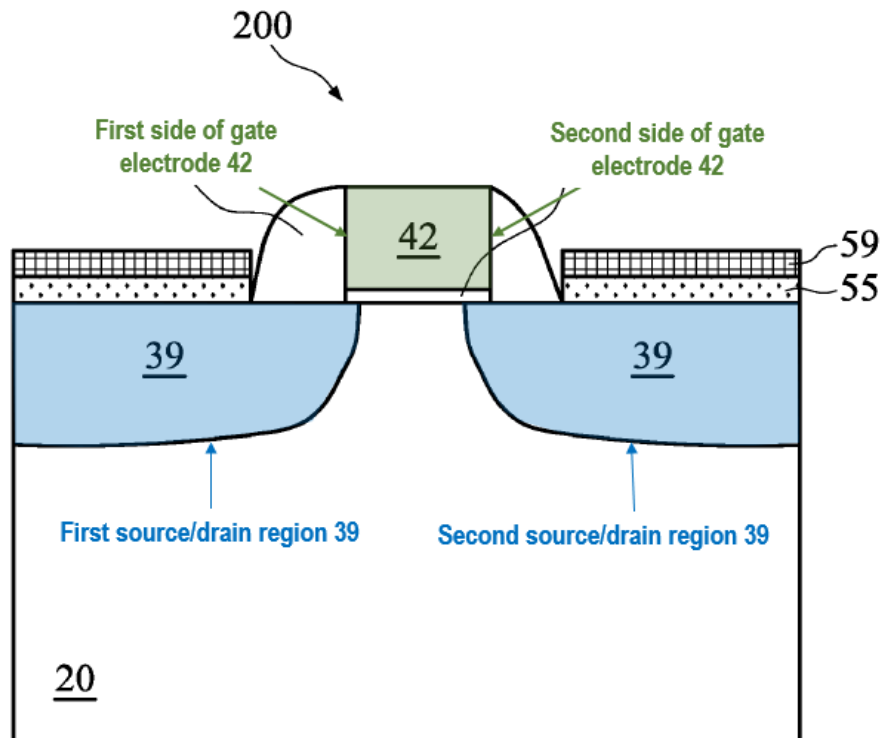


FIG. 2d

Tung, FIG. 2d (annotated)

154. Tung further discloses and would have rendered obvious source/drain regions 39 that are each formed “in the fin.” EX1006, [0033] (“source/drain regions 39 is [sic] **disposed within the fins 28**”); see also *id.*, [0057], [0074]-[0077], FIGS. 2b, 13; *supra*, Ground 1A at [1c].

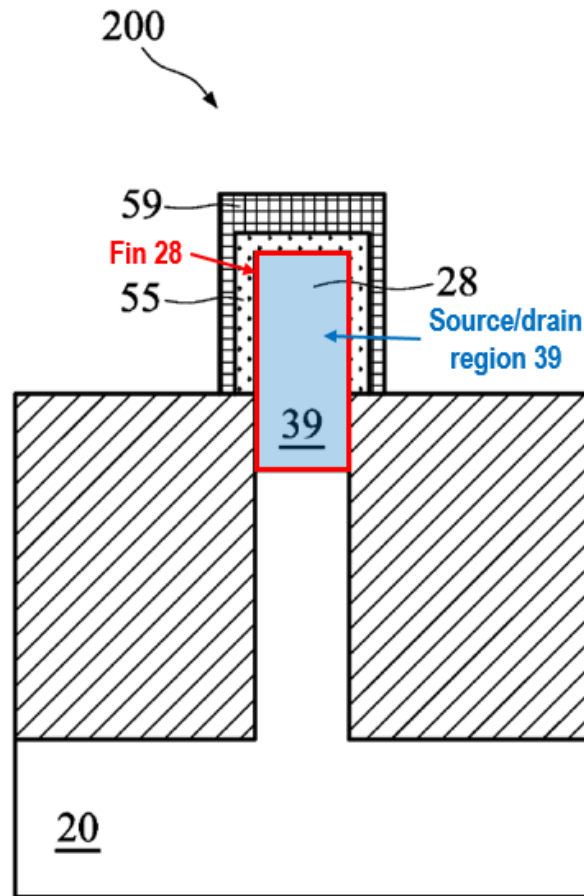


FIG. 2b

Tung, FIG. 2b (annotated)

155. Tung also teaches that the source and drain regions 39 can include an epitaxially grown semiconductor material 51 such as SiGe. EX1006, [0074], [0040]; *see also id.*, [0039]-[0045] and FIGS. 4a-4e, [0072]-[0082] and FIGS. 13-16. According to Tung's teaching that the source and drain regions 39 are disposed within the fin, SiGe material 51 would also be disposed within the fin. *Id.*, [0033]. Moreover, it would have been obvious and a POSITA would have understood that

epitaxially grown SiGe material 51, whether formed over fin 28 or grown from the substrate 20, would be “in the fin.”³⁷ Cf. EX1001, 13:22-50, FIG. 6; *see also* EX1013, 32; *supra*, Ground 1A at [1c].

[1d], [1i] the first source or drain region comprising two or more facets and a top surface; the second source or drain region comprising two or more facets and a top surface,

156. Tung describes and would have rendered obvious [1d] and [1i], e.g., in view of Tung’s disclosure of facets and a top surface that are formed by epitaxial growth of SiGe material 51 to form source/drain regions 39. More specifically, Tung discloses that “a selective epitaxial growth is performed to form semiconductor material 51,” and “[t]he semiconductor material 51 forms the source/drain regions 39 (raised source/drain) of the non-planar transistor 400” ... “on the fins 28.” EX1006, [0074]. According to Tung, “[t]he epitaxial growth includes vertical growth and horizontal growth,” and if the device includes just a single fin 28 or “the separation between adjacent fins 28 ... [is] large,” then “each fin 28 forms a separate raised source/drain region comprising the semiconductor material 51.” *Id.*, [0075].

³⁷ Epitaxially grown source and drain regions like those described in Tezuka were commonly characterized as part of the “fin” of a non-planar semiconductor device (e.g., a FinFET) before the ‘178 patent. *See, e.g.*, EX1017, [0024] (“Disclosed herein is a multi-gate device including **epitaxial source and drain fin regions** ...”), [0040] (“the source/drain cavity 420, including the source/drain extension cavity 421, is filled with a material using a selective epitaxial deposition process to form regrown source/drain fin”), FIGS. 6A-6B (depicting source/drain fins 618).

157. Tung's FIG. 4b illustrates the use of a "selective epitaxial growth process" to form a "semiconductor material 51" over a fin 28, where "[t]he growth proceeds in both lateral and vertical directions, for example at different rates on different crystal planes" to form two or more facets and a top surface. *Id.*, [0040]; *see also id.*, [0058].

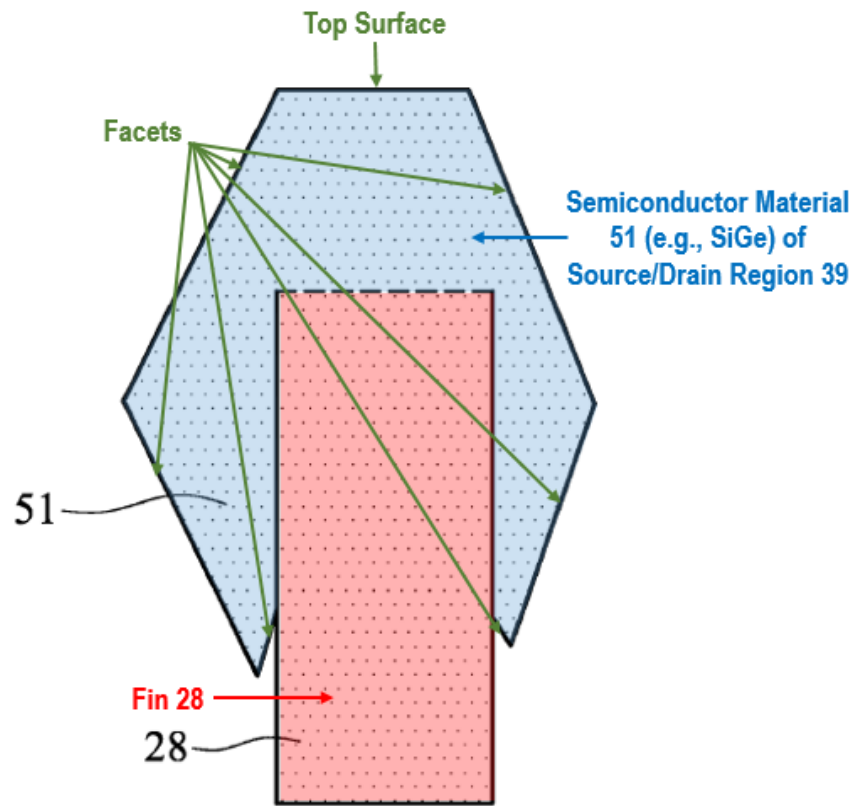


FIG. 4b

Tung, FIG. 4b (annotated)

[1e], [1j] wherein the first source or drain region comprises silicon and germanium; wherein the second source or drain region comprises silicon and germanium

158. Tung describes and would have rendered obvious [1e] and [1j], e.g., in view of Tung's disclosure that the first and second source and drain regions 39, including semiconductor material 51, and optionally fin 28, can each include Si and Ge. EX1006, [0040] ("semiconductor material 51 comprises SiGe"), [0074] ("semiconductor material 51 forms the source/drain regions 39" and "is formed of ... silicon germanium (SiGe)"), [0048] (substrate 20 from which fins 28 are formed can be "bulk silicon" or "bulk silicon germanium (SiGe)").

[1f], [1k] having a germanium concentration graded to a concentration in excess of 50%; having a germanium concentration graded to a concentration in excess of 50%; and

159. The combined teachings of Tung and Simonelli would have rendered obvious [1f] and [1k]. Tung teaches that "a selective epitaxial growth is performed to form semiconductor material 51" over fin 28 and the resulting structure including "semiconductor material 51 forms the source/drain regions 39." EX1006, [0074], [0040]. In Tung, the substrate 20—and, hence, fin 28 (which is formed from substrate 20)—can be bulk Si, while semiconductor material 51 can be "formed of a material different from that of substrate 20, for example, silicon germanium (SiGe)" *Id.*, [0074], [0048].

160. Simonelli further describes techniques for forming SiGe source and drain regions 1210 in a non-planar device (e.g., a FinFET) through epitaxial growth that involves gradually increasing the Ge content further from the substrate. EX1008, [0053]-[0058].

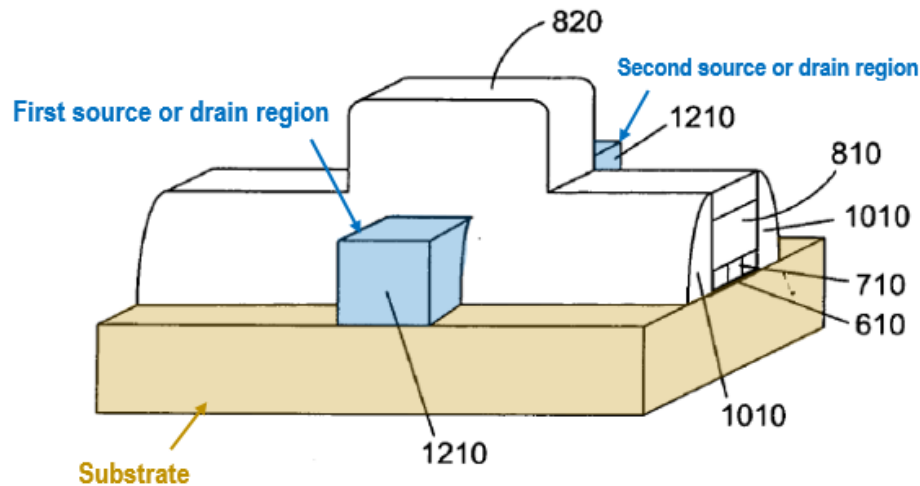


FIG. 12

Simonelli, FIG. 12 (annotated)

161. Simonelli's source/drain regions 1210 are epitaxially grown "using a graded high-germanium content silicon-germanium film stack 1400." EX1008, [0051]. Film stack 1400 includes a series of layers 1410, 1420, 1430, each additional layer having higher Ge content than the preceding layer:

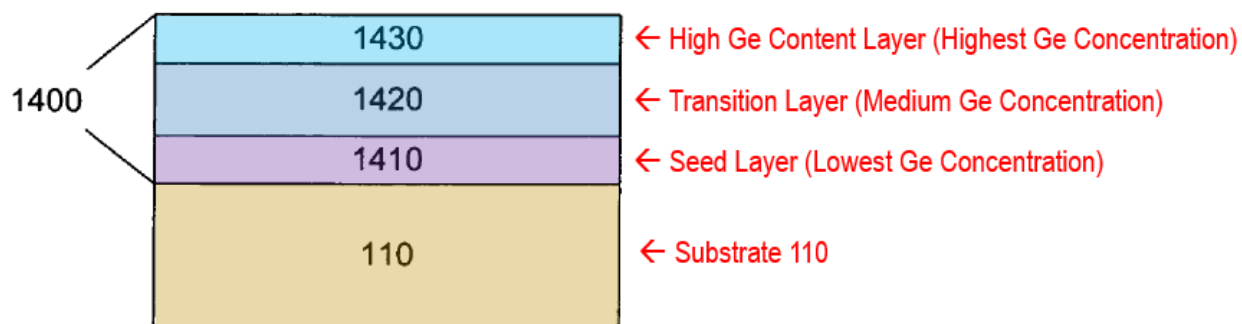


FIG. 14

Simonelli, FIG. 14 (annotated)

See also EX1008, [0053]-[0058], [0021]-[0024], FIGS. 14-15.

162. In some examples, Simonelli discloses that the concentration of Ge in the film stack is graded from 20-25 atomic weight % in the seed layer 1410 to 40-55 atomic weight % in the high Ge content layer 1430. *Id.*, [0054], [0058]. As another example, Simonelli discloses that source/drain regions “may be filled with a graded germanium silicon alloy ... according to one or more methods such as the embodiment described below in FIG. 15,” and in which “[t]he graded germanium silicon alloy may be epitaxially deposited with a graded germanium concentration that may range from 10 atomic % to **50 atomic %**.” *Id.*, [0039].

163. As described above in the overview of the Tung-Simonelli combination, it would have been obvious and a POSITA would have been motivated based on Simonelli to grade the Ge content in the material 51 of the source and drain

regions 39 of Tung's FinFET to a concentration in excess of 50%.³⁸ *Supra*, Section X.A. Further, to the extent Simonelli does not expressly identify a Ge concentration "in excess of 50%" as recited in [1f] and [1k], Simonelli's disclosed ranges including up to 50% Ge would have rendered obvious a Ge concentration graded to a concentration in excess of 50%. To start, fabrication processes, including processes for selective epitaxial growth, are imperfect and will always include some variance around targeted or nominal design parameters. Hence, even if SiGe material 51 were intended to have a Ge concentration graded to a concentration of just 50 atomic % as expressly taught in Simonelli, it would have been obvious that tolerances in ordinary manufacturing processes would yield devices that in practice have a Ge concentration in excess of 50%—even if the excess is just a small or negligible

³⁸ The '178 Patent specification describes no requirement for a "graded" region to include continuous (or smooth) grading. *See, e.g.*, EX1001, 6:25-32 ("In addition, as used herein, the term 'fixed' with respect to a concentration level is intended to indicate a relatively constant concentration level (e.g., the lowest concentration level in the layer is within 10% of the highest concentration level within that layer). In a more general sense, a fixed concentration level is intended to indicate the lack of an intentionally graded concentration level."). Thus, a region that includes at least two concentrations of a component intentionally differentiated by more than 10 % would provide a graded region as described in the '178 Patent. Simonelli (EX1008), which names a common inventor with the '178 Patent (Anand S. Murthy), also refers to a stepped/layered film stack as a graded region. EX1008, [0019]-[0020], [0051], FIGS. 14-15. Even if the claims did require either continuous or smooth grading, such continuous grading techniques were well known and would have been another obvious manner in which to implement grading like that suggested by Simonelli to avoid any sudden jumps in the concentration between films/layers in the source and drain regions. *See* Footnotes 11-12.

amount. Indeed, if the resulting graded SiGe material 51 at its highest concentration had even minutely more Ge than Si atom, then it would be graded to a concentration **in excess** of 50% as claimed. In 2010, no epitaxial growth process or other practical fabrication process could possibly have controlled the Ge content in SiGe material 51 down to, for example, 0.1%, let alone the level of atoms.

164. Moreover, as described above in the overview of the Tung-Simonelli combination (*supra*, Section X.A), a POSITA would have understood that the concentration of Ge in SiGe material 51 of the source and drain regions 39 would impact a range of properties of the FinFET, including the lattice constant at different depths of the SiGe material 51, the lattice mismatch at the interfaces on either side of SiGe material 51, the thickness and size at which the SiGe material 51 could be grown without defects, the mobility and parasitic resistance of the source and drain regions, and the amount of strain that could be imparted on a channel region.³⁹ *Supra*, Section X.A. It would have been obvious for a POSITA to try grading the Ge content in SiGe material 51 to a concentration in excess of 50% through routine experimentation to optimize one or more of these properties of the FinFET.

³⁹ *Supra*, Footnotes 11-13.

[1g], [1l] a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

165. Tung would have rendered obvious [1g] and [1l], e.g., in view of Tung's disclosure of a metal germanide layer 59 formed over respective top surfaces of the first and second source or drain regions 39.

166. For example, Tung describes a process for forming a germanide layer 59 that involves first forming a doped semiconductor layer 55 over a semiconductor material 51 of the source/drain regions 39, then depositing a metal 57 over the doped semiconductor layer 55, and finally annealing the metal 57 to form the germanide layer 59. EX1006, [0078]-[0081], FIGS. 14-16; *see also id.*, [0039]-[0045], FIGS. 4a-4e, FIG. 2a and 2d (depicting layer 59 formed over both source and drain regions 39).

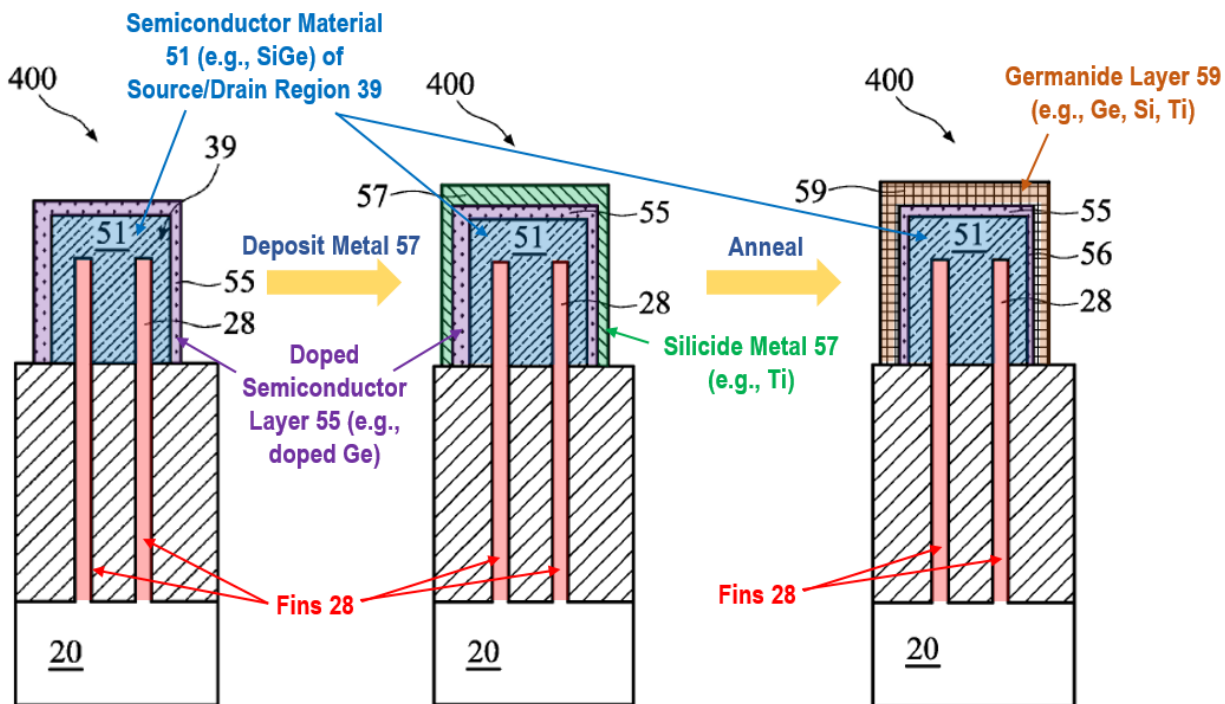


FIG. 14

FIG. 15

FIG. 16

Tung, FIGS. 14-16 (annotated)

167. FIGS. 14-16 depict the formation of silicide layer 59 on a device having multiple fins 28 spaced closely to each other such that a continuous semiconductor material 51 is grown across each fin 28. Tung also explains, however, that “the method described in FIGS. 13-16 is used in fabrication of a device with a single fin.” See EX1006, [0082]. and FIGS. 4b-4e depict Tung’s process as applied in the context of a single fin:

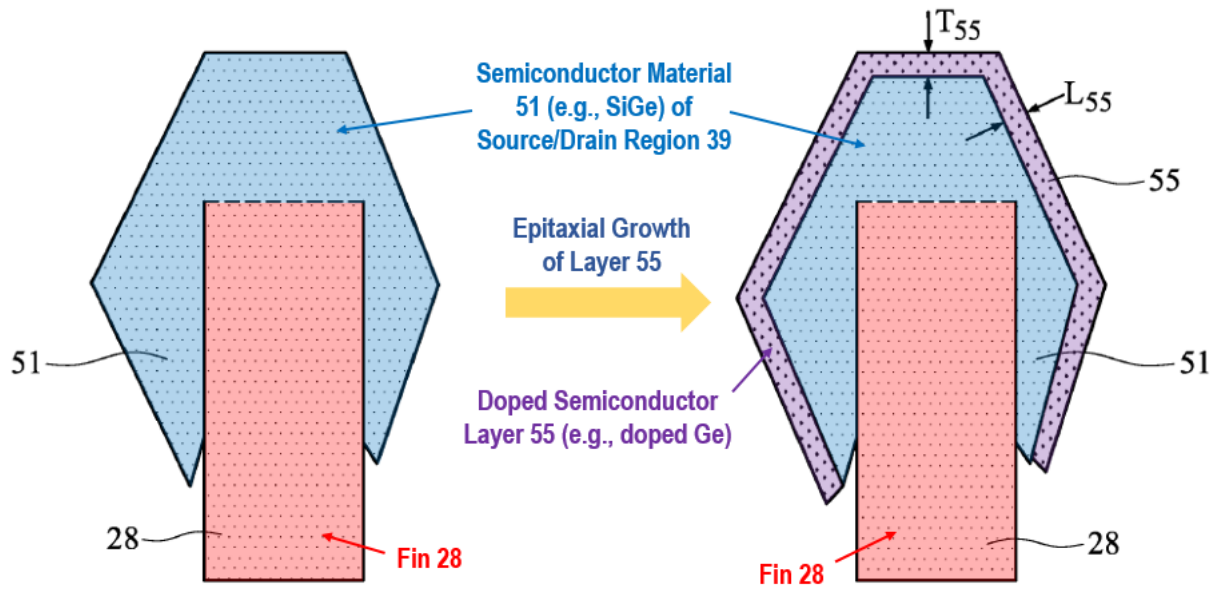


FIG. 4b

FIG. 4c

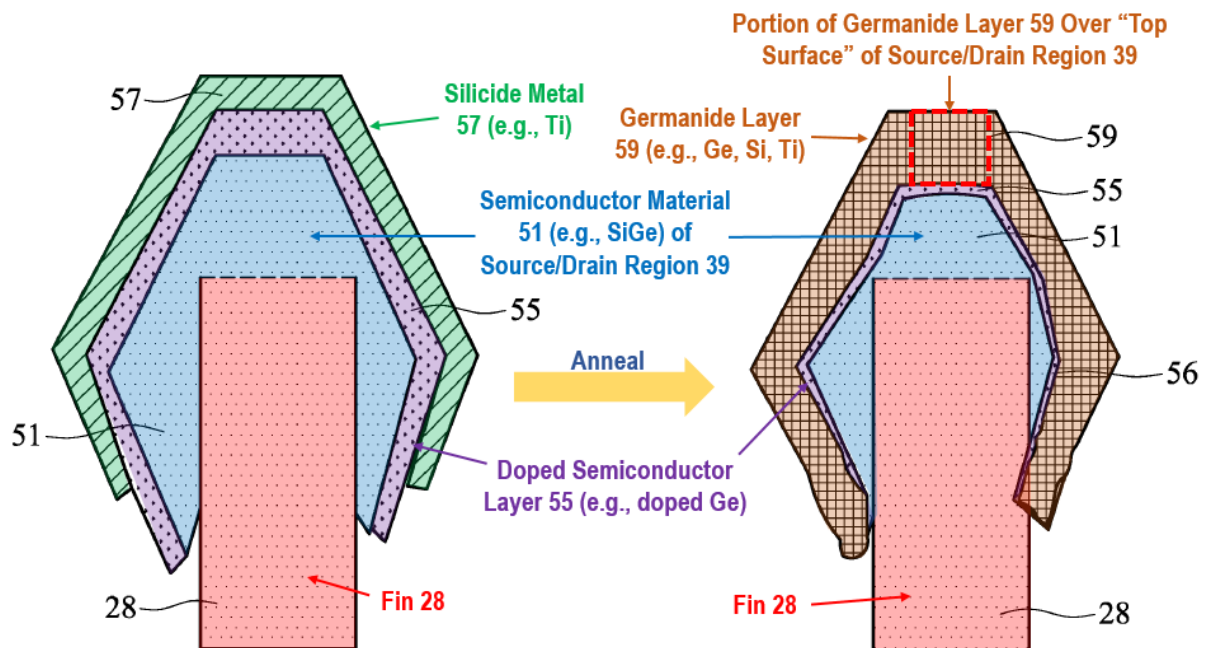


FIG. 4d

FIG. 4e

Tung, FIGS. 4b-4e (annotated)

168. As shown in FIG. 4e, a portion of germanide⁴⁰ layer 59 is formed over a top surface of semiconductor material 51 of source/drain region 39. And although Tung's figures show a portion of doped semiconductor layer 55 that remains after the annealing process, Tung also describes alternative embodiments in which "all of the doped semiconductor layer 55 may be consumed" by the annealing. EX1006, [0045], [0081].

169. Tung explains that semiconductor layer 55 can be doped Ge; semiconductor material 51 can be epitaxially grown SiGe grown over source/drain regions 39; and silicide metal 57 can include Ti. *Id.*, [0040], [0042], [0061], [0058], [0074], [0078], [0080]. In this case, it would have been obvious that the germanide layer 59, that results from annealing, would comprise Ti, Si, and Ge. Titanium would be present in germanide layer 59 from the deposition of metal 57, Ge would be present at least from the Ge cap 55, and Si would be present from the SiGe material 51.

170. In particular, as to the presence of Si in the germanide layers 59, this feature would have been obvious in several ways.

171. First, Tung teaches that the cap layer 55 can be formed from "doped Ge," and further that germanide layer 59 is formed by annealing a metal (e.g., Ti)

⁴⁰ *Supra*, Footnote 18.

over cap layer 55 until the interface of germanide layer 59 extends some amount into SiGe material 51 of the source/drain region 39. EX1006, [0045] (“the silicide interface moves beyond the doped semiconductor layer 55 and into the semiconductor material 51”), [0081]. In this case, the germanide layers 59 that result from annealing would naturally include Si originating from the SiGe material 51 (and would further include Ge and Ti as described above). EX1006, [0058], [0078].

172. Second, Tung teaches that “all of the doped semiconductor layer 55 may be consumed by the silicidation process” when annealed. EX1006, [0045]. When all of cap layer 55 is consumed without the interface of the resulting germanide layer 59 extending into the source/drain regions themselves (e.g., without extending into SiGe material 51), the lower surface of the germanide layer 59 would contact the outer surface of the SiGe material 51 of the source/drain region 39. In this case, it would have been obvious that at least some Si near the outer surfaces of the SiGe material 51 of the source/drain region 39 that contact the germanide layers 59 would migrate into the germanide layers 59 due to metal-silicon bonds being stronger and more stable than metal-germanium bonds. When comparing elements of the same column of the periodic system of elements, a lighter element (such as Si) forms stronger bonds and is thermodynamically favorable over a heavier element (such as Ge). This thermodynamic trend represents a driving force for Si to be

incorporated into the metal-germanide compound. *See supra*, [1g], ¶ 94. As a result,, germanide layers 59 in the combination would include Ti, Ge, and Si.

173. Third, it would have been obvious for the Ge cap layer 55 itself to include a small amount of Si such that the germanide layers 59 formed by annealing Ti with the cap layer 55 would naturally include Si along with Ti and Ge, regardless of whether cap layer 55 is entirely consumed by annealing. Indeed, Tung not only teaches that cap layer 55 can be “doped Ge,” but further teaches that cap layer 55 can include “doped SiGe” material. EX1006, [0058], [0078]. Given that both doped Ge and doped SiGe are identified in Tung as suitable materials for cap layer 55, it would have been obvious to select a material for cap layer 55 formed predominantly of Ge (e.g., in excess of 90% Ge) to make beneficial use of well-known intrinsically favorable properties of Ge (e.g., a lower band gap and Schottky barrier height that would tend to yield lower contact resistance to the source/drain regions) while still making beneficial use of Si (e.g., to lower the gap in Ge content and reduce dislocations at the interface of the resulting germanide layer 59 and the source/drain regions). *See* Footnotes 4, 23. At minimum, it was known before the Critical Date that a wide range of concentrations of Ge in cap layers were suitable for forming contact structures to source/drain regions, and it would have been obvious to select a high concentration of Ge (e.g., in excess of 90%) to optimally reduce contact resistance and dislocations/defects in the contact structures to the source/drain

regions. *See, e.g.*, EX1036, [0038] (describing a film 410 formed over the source and drain regions of a FinFET and “comprise[d] [of] approximately 1 to 99 atomic percent of the alloy and can even extend to pure (100%) Ge”), FIGS. 4A-4B; *see also id.*, [0074]-[0078] (describing an analogous film 542 that is “consumed during the formation of a silicide film on the source and drain regions”), FIG. 5P.

2. Claim 2

174. Claim 2 of the '178 Patent recites:

2. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than $1E20$.

175. Tung describes and would have rendered obvious [2], e.g., in view of Tung's disclosure that “[d]uring the growth of semiconductor material 51” in the source and drain regions 39, “a p-type impurity ... may be in-situ doped” at a concentration up to “about $5 \times 10^{20}/\text{cm}^3$ ” (i.e., greater than $1E20$). EX1006, [0076]. Tung further discloses B as a p-type impurity. *Id.*, [0028] (“p-type dopant such as boron”), [0034], [0052].

3. Claim 3

176. Claim 3 of the '178 Patent recites:

3. The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of $1E20$.

177. The additional features recited in claim 3 would have been obvious based on Simonelli's disclosure of a silicon-germanium film stack 1400 for use in, among other things, source or drain regions of a FinFET. EX1008, [0044]-[0058], FIGS. 6-15. Simonelli's film stack includes graded concentrations of B as follows:

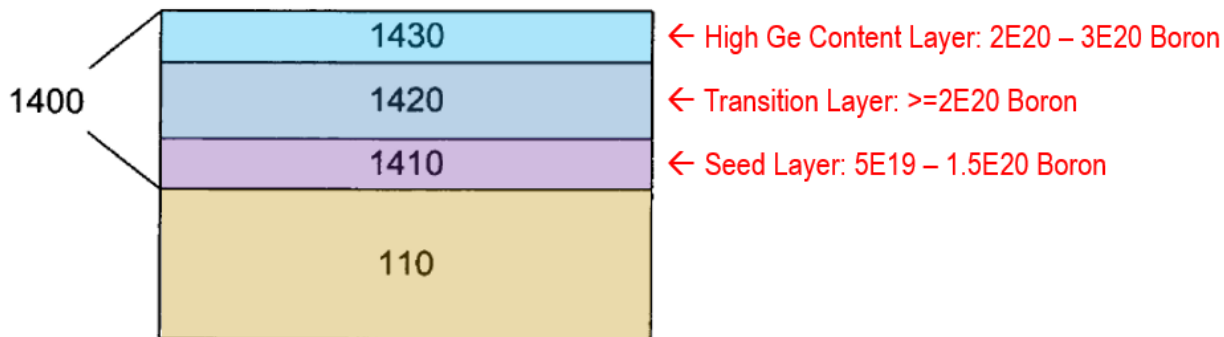


FIG. 14

Simonelli, FIG. 14 (annotated)

178. It would have been obvious to implement graded B concentrations like those disclosed in Simonelli in the source and drain regions of the FinFET in the Tung-Simonelli combination and a POSITA would have had a reasonable expectation of success for substantially the same reasons discussed above with respect to claim [3] in Ground 1B. *Supra*, Ground 1B at [3].

4. Claim 4

179. Claim 4 of the '178 Patent recites:

4. The integrated circuit structure of claim 1, wherein the fin comprises a strained channel between the first and second source or drain regions.

180. The combined teachings of Tung and Simonelli would have rendered obvious claim [4]. Tung teaches that the non-planar transistor includes a channel region “disposed under the gate electrode 42 on a top surface and sidewalls of the fin 28” between the first and second source or drain regions 39. EX1006, [0025], FIGS. 1d, 2d, 11; *see also id.*, [0026]-[0031], [0052] (“fins 28 are implanted to uniformly dope the channel region”), [0065] (“source/drain region 39 are separated by a channel 11”). Further, as described above in the overview of the Tung-Simonelli combination (Section X.A), it would have been obvious to form a graded SiGe material 51 in the first and second source or drain regions 39 that would apply a compressive strain to the channel region to increase the hole mobility in the channel. *Supra*, Section X.A; EX1008, [0024], [0042], [0044].

5. Claim 5

181. Claim 5 of the '178 Patent recites:

5. The integrated circuit structure of claim 1, wherein the first and second source or drain regions are P-type.

182. Tung describes and would have rendered obvious [5], e.g., in view of Tung’s disclosure that the semiconductor material 51 and/or fin 28 of the source and drain regions 39 can be doped with p-type impurities such as B. EX1006, [0073], [0076]-[0077]; *see also id.*, [0034] (“PMOS transistor is being fabricated”), [0041], [0052].

6. Independent Claim 6

183. Claim 6 of the '178 Patent recites:

6. An integrated circuit structure, comprising:
a body comprising silicon;
a gate electrode over the body;
a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

184. The Tung-Simonelli combination would have rendered obvious and taught each element of claim 6 as described below.

[6pre] An integrated circuit structure, comprising:

185. For the reasons discussed above with respect to [1pre], the Tung-Simonelli combination would have rendered obvious [6pre].

[6a] a body comprising silicon;

186. For the reasons discussed above with respect to [1pre], the Tung-Simonelli combination would have rendered obvious [6a], e.g., in view of Tung's

disclosure of a fin comprising Si. *See supra*, [1a], [1c], [1h]. For example, just as the specification of the '178 Patent identifies structure 660 alternately as a “body” or a “fin,” the same structures from Tung that would have rendered obvious a “fin” also would have provided the recited “body” in claim 6. *Cf.* EX1001, 13:24-27, FIG. 6.

[6b]-[6l] a gate electrode over the body; a first source or drain region in the body proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second source or drain region in the body proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

187. For the reasons discussed above with respect to [1b]-[1l], the Tung-Simonelli combination would have rendered obvious [6b]-[6l].

7. Claim 7

188. Claim 7 of the '178 Patent recites:

7. The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration greater than 1E20.

189. For the reasons discussed above with respect to [2], the Tung-Simonelli combination would have rendered obvious [7].

8. Claim 8

190. Claim 8 of the '178 Patent recites:

8. The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of $1E20$.

191. For the reasons discussed above with respect to [3], the Tung-Simonelli combination would have rendered obvious [8].

9. Claim 9

192. Claim 9 of the '178 Patent recites:

9. The integrated circuit structure of claim 6, wherein the body comprises a strained channel between the first and second source or drain regions.

193. For the reasons discussed above with respect to [4], the Tung-Simonelli combination would have rendered obvious [9].

10. Claim 10

194. Claim 10 of the '178 Patent recites:

10. The integrated circuit structure of claim 6, wherein the first and second source or drain regions are P-type.

195. For the reasons discussed above with respect to [5], the Tung-Simonelli combination would have rendered obvious [10].

XI. [GROUND 3A] – Obviousness based on Conway, Tezuka, and Tung (Claims 11-20)

A. Manner and Motivations to Combine

196. As discussed above, Conway describes computing devices that can be “realized in digital electronic circuitry, integrated circuitry, specially designed ASICs ..., computer hardware, firmware, software, and/or combinations thereof.” *Id.*, [0162]; *generally id.*, [0147]-[0165], FIGS. 5-8 and associated text. Conway does not, however, address details about the transistors or low-level integrated circuitry that may be used to implement its electronic components. A POSITA seeking to design or fabricate integrated circuitry for a computing device like that described in Conway would have looked to additional references such as Tezuka and Tung for such details, and a POSITA would have found it obvious to use a multi-gate transistor (e.g., a FinFET transistor) like that of the device taught by Tezuka and Tung of Ground 1A to implement one or more of the electronic components in Conway’s system.

197. Multiple reasons would have motivated a POSITA to combine the teachings of Conway, Tezuka and Tung, specifically to use a transistor like that described in Ground 1A to implement an electronic component in Conway’s system. First, as noted above, Conway proposes the use of integrated circuitry but lacks detail about the transistors or semiconductors in the ICs. A POSITA would have looked to other sources such as Tezuka and Tung to implement such ICs. For

example, A POSITA would be motivated to use advanced transistor architectures, such as FinFETs, as disclosed in Tezuka and Tung, to implement an advanced system such as Conway. Second, FinFETs and other multi-gate transistors like those described in Tezuka were known to exhibit advantages over other technologies (e.g., planar FETs), including providing capabilities for improved channel control, lower leakage currents, smaller size, and increased speed.⁴¹ A POSITA would have sought to use multi-gate transistors like those described in Ground 1A in Conway's ICs to leverage these advantages and realize predictable performance improvements in Conway's ICs. Third, the combination amounts to an obvious application of known techniques based on Tezuka and Tung to a known device as described in Conway ready for improvement to yield predictable results. For example, Conway teaches

⁴¹ See, e.g., EX1016, 6 (“In a multi-gate device, the channel is surrounded by several gates on multiple surfaces, allowing more effective suppression of ‘off-state’ leakage current. Multiple gates also allow enhanced current in the ‘on’ state, also known as drive current. These advantages translate to lower power consumption and enhanced device performance. Non-planar devices are also more compact than conventional planar transistors, enabling higher transistor density which translates to smaller overall microelectronics.”), 7 (“In the technical literature, FinFET is used somewhat generically to describe any fin-based, multi-gate transistor architecture regardless of number of gates.”); EX1006, [0004] (“One of the goals of the semiconductor industry is to continue shrinking the size and increasing the speed of individual FETs. To achieve these goals, three dimensional (3-D) or non-planar transistor structures such as fin FETs (FINFETs), multiple gate transistors, or gate all around transistors are being investigated for use in sub 22 nm nodes. Such transistors not only improve area[] density, but also improve gate control of the channel.”).

advanced image processing techniques (such as “panning” an image) which would have motivated a POSITA to implement Conway’s system using advanced FET technologies such as the FinFETs disclosed in Tezuka and Tung. Conway does not impose any restrictions on the types of transistors or semiconductors that must be used in its ICs, and a POSITA would have had a reasonable expectation of success implementing the combination.⁴²

B. Claim Element Analysis

1. Independent Claim 11

198. Claim 11 of the ’178 Patent recites:

⁴² For example, non-planar field-effect transistors (FETs) were proposed for use in electronic components on motherboards of computing devices years before the ’178 Patent. *See, e.g.*, EX1032, [0061]-[0063], FIGS. 5-6, 23.

11. A computing device, comprising:
a board; and
a component coupled to the board, the component including an integrated circuit structure, comprising:
a fin comprising silicon;
a gate electrode over the fin;
a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and
a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

199. The Conway-Tezuka-Tung combination would have rendered obvious and taught each element of claim 11 as described below.

[11pre] A computing device, comprising:

200. The Conway-Tezuka-Tung combination would have rendered obvious [11pre], e.g., in view of Conway’s disclosure of various “generic” mobile and non-mobile computing devices. EX1010, FIG. 9 and [0147]-[0165]; *see also id.*, FIGS. 5-8 and associated text.

[11a] a board; and

201. The Conway-Tezuka-Tung combination would have rendered obvious [11a], e.g., in view of Conway's disclosure of "a common motherboard" for mounting various components of a computing system. EX1010, [0148], [0153], FIG. 9; *supra*, Section VII.D.

[11b] a component coupled to the board, the component including an integrated circuit structure, comprising:

202. The Conway-Tezuka-Tung combination would have rendered obvious [11b]. Conway teaches that "the systems and techniques described here can be realized in digital electronic circuitry, integrated circuitry, specially designed ASICs (application specific integrated circuits), computer hardware, firmware, software, and/or combinations thereof." EX1010, [0162]. Conway also describes various components coupled to a "common motherboard." EX1010, [0148], [0153], FIG. 9; *see also id.*, FIGS. 5-8 and associated text. Further, in the combination, and as described above in the overview of the combination (Section XI.2), it would have been obvious to utilize the Tezuka-Tung integrated circuit structure of Ground 1A in one or more of Conway's components coupled to the motherboard.

[11c]-[11n] a fin comprising silicon; a gate electrode over the fin; a first source or drain region in the fin proximate a first side of the gate electrode, the first source or drain region comprising two or more facets and a top surface, wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium; a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side, the second source or drain region comprising two or more facets and a top surface, wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%; and a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

203. For the reasons discussed above in Ground 1A with respect to claim elements [1a]-[1l], the Conway-Tezuka-Tung combination would have rendered obvious [11c]-[11n].

2. Claim 12

204. Claim 12 of the '178 Patent recites:

12. The computing device of claim 11, further comprising: a memory coupled to the board.
--

205. Conway discloses a memory coupled to the board. EX1010, [0148]-[0151] and FIG. 9 (memories 904, 906), [0153]-[0157] and FIG. 9 (memories 964, 974), [0123]-[0125] and FIG. 6, [0011] (“memory storing code”), [0078] (“memory devices”), [0148] and [0153] (“mounted on a common motherboard”).

3. Claim 13

206. Claim 13 of the '178 Patent recites:

13. The computing device of claim 11, further comprising: a communication chip coupled to the board.

207. Conway discloses a “communication interface” such as interface 966 that includes “digital signal processing circuitry” for implementing various communication capabilities on the device. EX1005, [0152]-[0153], [0158], FIG. 9; *see also id.*, [0148] (“mounted on a common motherboard”), FIG. 6 (607) A POSITA would have understood and it would have been obvious to implement the communications circuitry on a communication chip.

4. Claim 14

208. Claim 14 of the ’178 Patent recites:

14. The computing device of claim 11, further comprising: a camera coupled to the board.

209. Conway discloses a camera coupled to the board. EX1010, [0113] (“device 500 includes ... a camera 507”), [0118] (“camera”), [0121] (“camera 507”), [0123] (“a camera interface 608 that provides a communication interface and processing functions for capturing digital images from the camera 507”), FIG. 6; *see also id.*, [0148] (“Each of the components ... may be mounted on a common motherboard”), [0153], FIG. 9.

5. Claim 15

210. Claim 15 of the ’178 Patent recites:

15. The computing device of claim 11, further comprising: a global positioning system coupled to the board.
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211. Conway discloses a GPS receiver module coupled to the board. EX1010, [0095] (“GPS device located on the mobile device”), [0102], [0130], [0158] (“GPS (Global Positioning System) receiver module 970 may provide additional navigation- and location-related wireless data to device 950”); *see also id.*, [0148] (“Each of the components ... may be mounted on a common motherboard”), [0153], FIG. 9.

6. Claim 16

212. Claim 16 of the ’178 Patent recites:

16. The computing device of claim 11, further comprising: a battery coupled to the board.
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213. Conway discloses and would have rendered obvious a battery coupled to the board. For example, Conway describes that the computing device can include a “battery life indicator 516 that indicates a measurement of the remaining battery life,” which a POSITA would have understood or found obvious to mean that the device includes a battery. EX1010, [0114], FIG. 5. Conway also discloses “a power source 619 that provides an appropriate alternating current (AC) or direct current (DC) to power components.” EX1010, [0123], FIG. 6. In a mobile device, and other devices, the power source 619 would include a battery coupled to the Board, e.g., to

deliver power to components on the board. EX1010, [0148] (“Each of the components ... may be mounted on a common motherboard”), [0153], FIG. 9.

7. Claim 17

214. Claim 17 of the ’178 Patent recites:

17. The computing device of claim **11**, further comprising:
an antenna coupled to the board.

215. Conway discloses an antenna coupled to the board. EX1010, [0113]-[0114], [0119], [0120], [0123], FIGS. 5-6 (antenna 505); *see also id.*, [0148] (“Each of the components ... may be mounted on a common motherboard”), [0153], FIG. 9.

8. Claim 18

216. Claim 18 of the ’178 Patent recites:

18. The computing device of claim **11**, wherein the component is a packaged integrated circuit die.

217. Conway describes in paragraph [0162] “integrated circuitry” components, and FIG. 9 shows various integrated circuit chips mounted on a motherboard. EX1010, [0148], [0162], FIG. 9. A POSITA would have understood and it would have been obvious that the mounted components include a packaged integrated circuit die.

9. Claim 19

218. Claim 19 of the ’178 Patent recites:

19. The computing device of claim **11**, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

219. It would have been obvious in the Conway-Tezuka-Tung combination for the component to be selected from a group consisting of a processor, a communications chip, and a digital signal processor, e.g., in view of Conway’s teachings of computing device components such as a central processor 902, processor 952, or various other processing components. EX1010, [0148] (“device 900 includes a processor 902”), [0153] (“device 950 includes a processor 952”), FIG. 9; *see also id.*, [0162]-[0163], [0168] (“digital signal processing circuitry”); *supra*, [13]. As discussed above in the overview of the combination, it would have been obvious to implement Conway’s electronic components using a FinFET like that described in the device taught by Tezuka and Tung of Ground 1A.

10. Claim 20

220. Claim 20 of the ’178 Patent recites:

20. The computing device of claim **11**, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

221. Conway discloses that the computing device can be a mobile phone, a laptop, a desktop computer, or a server. EX1010, [0147], FIG. 9.

XII. [GROUND 3B] – Obviousness based on Conway, Tezuka, Tung, and Simonelli (Claims 11-20)

222. A POSITA seeking to design or fabricate integrated circuitry for a computing device like that described in Conway would have looked to additional references such as Tezuka, Tung, and Simonelli for such details, and a POSITA would have found it obvious to use a multi-gate transistor (e.g., a FinFET transistor) like that of the device taught by the combination of Tezuka, Tung, and Simonelli of Ground 1B to implement one or more of the electronic components in Conway's system for the reasons discussed above in the overview of Ground 3A. *Supra*, Section XI.A.

223. The Conway-Tezuka-Tung-Simonelli combination would have rendered obvious each of claims 11-20, and would have provided each element of these claims for the reasons discussed above with respect to claims 11-20 in Ground 3A. The combination also would have rendered obvious [11c]-[11n] for the reasons described above with respect to the corresponding elements of claim 1 in Grounds 1A-1B.

XIII. [GROUND 3C] – Obviousness based on Conway, Tung, and Simonelli (Claims 11-20)

224. A POSITA seeking to design or fabricate integrated circuitry for a computing device like that described in Conway would have looked to additional references such as Tung and Simonelli for such details, and a POSITA would have

found it obvious to use a multi-gate transistor (e.g., a FinFET transistor) like that of the device taught by the combination of Tung and Simonelli of Ground 2 to implement one or more of the electronic components in Conway's system for the reasons discussed above in the overview of Ground 3A. *Supra*, Section XI.A.

225. The Conway-Tung-Simonelli combination would have rendered obvious each of claims 11-20, and would have provided each element of these claims for the reasons discussed above with respect to claims 11-20 in Ground 3A. The combination also would have rendered obvious [11c]-[11n] for the reasons described above with respect to the corresponding elements of claim 1 in Ground 2.

XIV. Additional Remarks

226. I currently hold the opinions expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

227. I hereby declare that all statements made are of my own knowledge are true and that all statements made on information and belief are believed to be true. I further declare that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of the Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this proceeding.

Dated: February 23, 2023

By: 2023

E. Fred Schubert, Ph.D.
Troy, New York

APPENDIX A

Curriculum Vitae: E. Fred Schubert

Contact information

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Citizenship

Born in Stuttgart, Germany (1956)
Naturalized United States Citizen (1995)

Education

University of Stuttgart	Electrical Engineering	Vordiplom	(U. S. equivalent BSEE)	1978
University of Stuttgart	Electrical Engineering	Diplom Ingenieur (Honors)	(U. S. equivalent MSEE)	1981
Oregon State University	Electrical Engineering	Exchange Student		1977–1978
University of Stuttgart	Electrical Engineering	Doktor Ingenieur (Honors)	(U. S. equivalent Ph.D.)	1986

Current appointment

2002 – present: Professor, Department of Electrical, Computer, and Systems Engineering; Rensselaer Polytechnic Institute, Troy NY

Previous appointments

2002 – 2015: Head and Founder of the Future Chips Constellation; Rensselaer Polytechnic Institute
2002 – 2015: Wellfleet Senior Constellation Professor, Future Chips (Chaired Professor); Rensselaer Polytechnic Institute
2002 – 2012: Professor Department of Physics, Applied Physics, and Astronomy; Rensselaer Polytechnic Institute
2008 – 2009: Director, Founding Director, and Principal Investigator, NSF Engineering Center for Smart Lighting, Rensselaer Polytechnic Institute
2002 – 2003: Adjunct Professor, Boston University
1995 – 2002: Professor, Boston University, Department of Electrical and Computer Engineering; Director of the Semiconductor Devices Research Laboratory; Affiliated Faculty of the Photonics Center.
1988 – 1995: Member of Technical Staff; Principal Investigator; and Member of Management at AT&T Bell Laboratories in Murray Hill, New Jersey
1985 – 1987: Post-Doctoral Member of Technical Staff at AT&T Bell Laboratories in Holmdel, New Jersey.
1981 – 1985: Scientific Member of Staff in the Department of Solid-State Chemistry at the Max Planck Institute for Solid-State Research in Stuttgart, Germany. Ph.D. Dissertation title: “Modern Schottky gate field-effect transistors based on III–V semiconductors”

Fields of Technical Expertise, Hands-on Experience, and Teaching

- Expertise, hands-on experience, and teaching in semiconductor opto-electronics including the following devices: LED, semiconductor laser, vertical cavity surface-emitting laser (VCSEL), solar cell, photo-detector, LED displays, micro-LED displays, and LCD displays. The activities include the design, fabrication, processing, and packaging of the devices, and the use of the devices in circuits and systems. (1981 to present)
- Expertise, hands-on experience, and teaching in semiconductor electronics including the following devices: MESFET, HFET, MOSFET, CMOS-FET, LDD MOSFET, LD MOS FET, FinFET, GAA FET, Vertical MOSFET (high-power MOSFET), thyristor, GTO thyristor, and IGBT. The activities include the design, fabrication, processing, and packaging of the devices, and the use of the devices in discrete and integrated circuits. (1979 to present)
- Expertise, hands-on experience, and teaching in thin-film deposition of metal, semiconductor, and insulator

films by PVD (physical vapor deposition) and CVD (chemical vapor deposition) including PECVD (plasma enhanced CVD), MOCVD (metal-organic CVD), ALE (atomic layer epitaxy), ALD (atomic layer deposition), and bulk crystal growth (AlN, GaN, and sapphire). Epitaxial growth of silicon, III-V arsenide, phosphide and nitride epitaxial layers on GaAs, sapphire, Si, and GaN substrates by epitaxy including molecular beam epitaxy (MBE), metal-organic chemical vapor deposition (MOCVD), and vapor-phase epitaxy (VPE). High-k materials, low-k-materials, phosphors, resins, polymers, encapsulants, alloy semiconductors and their deposition technologies such as epitaxy, CVD, and PVD. Doping of semiconductors by various means including delta doping and atomic monolayer doping. (1981 to present)

- Expertise, hands-on experience, and teaching in the design, operation, and usage of semiconductor devices in lighting systems, communication systems, and power-supply systems and in the analysis and development of LED power supplies using Boost and Buck Converters. (1993 to present)

Technical Research Activities

- Design, development and fabrication of a Si pressure sensor based on the piezo-resistivity of Si using a bridge configuration of four thin-film Si resistors (1979 – 1980)
- Design of an electro-optic Mach-Zehnder Interference Modulator based on Lithium niobate (LiNbO_3) operating at a wavelength of 1300 nm (1980 – 1981)
- First study of hot electron effects in selectively doped $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterostructures (1983)
- Demonstration and elimination of parallel conduction in $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterostructures (1984)
- First analysis of semiconductors doped with simultaneously shallow and deep donors (1984).
- Development and use of thyristor circuits (including GTO thyristor circuits) for the control of a lamp heating system (1984 – 1985)
- Proposal and demonstration of the δ -doped field-effect transistor. Short-channel effects in sub-micron field-effect transistors can be reduced to their theoretical minimum by using δ -doped structures (1985)
- Development of the theory of alloy broadening in luminescence spectra of alloy semiconductors such as $\text{Al}_x\text{Ga}_{1-x}\text{As}$. The current understanding of the low-temperature spectral linewidths of ternary and quaternary alloy semiconductors is based on this theoretical model. The publication analyzing the phenomenon of alloy broadening has been referenced far in excess of 100 times (1984)
- First demonstration of a light-emitting diode with a doping superlattice active region (1985)
- Application of δ -doping to selectively doped heterostructures; Demonstration of high-electron-mobility transistors (HEMTs) with highest free electron concentrations; Analysis of structures by SEM, TEM, and SIMS (1986).
- Demonstration of delta-doped non-alloyed ohmic contacts with very low contact resistance and subsequent demonstration of self-aligned field-effect transistor with delta-doped non-alloyed ohmic contacts (1986)
- Demonstration of the spatial localization of dopants within 20 Å for a number of doping elements in delta-doped semiconductors including GaAs and Si for MESFET and lightly-doped drain (LDD) MOSFET applications and the analysis of delta-doped structures by SIMS (secondary ion mass spectrometry) (with colleague Henry S. Luftman, 1983-1995)
- Significant improvement of the optical properties of doping superlattices by employment of delta doping. Improvement is demonstrated by the first observation of quantized interband transitions in the absorption (1988) and in the emission spectra (1989)
- First demonstration of tunable doping superlattice laser (1989)
- First quantitative analysis of the capacitance-voltage (CV) profiling technique in semiconductors with quantum-confined carriers. Demonstration that resolution of CV profiles in quantum-confined semiconductors is not limited to the Debye screening length (1990)
- Invention and demonstration a new concept by which heterojunction band discontinuities occurring between two different semiconductors are eliminated. The *elimination of heterojunction barriers* is based on parabolic compositional grading of doped heterojunctions. This concept is widely used in the fabrication of vertical cavity surface emitting lasers and other heterojunction devices (1991)
- Invention and first demonstration of resonant cavity light-emitting diode (RCLED) which uses photon quantization in microcavities to enhance the spontaneous emission properties (1992)
- Demonstration of giant enhancement of luminescence intensity in Er-doped Si-SiO_2 microcavities (1992)
- First demonstration of a resonant-cavity detector which is useful for wavelength-selective detection (1993)

- Demonstration of resonant-cavity light-emitting diode (RCLED) with very high brightness. The experimental brightness of the RCLED is five times higher than that of conventional LEDs. Based on calculations, the brightness of RCLEDs is expected to exceed that of conventional LEDs by more than a factor of ten (1994)
- Demonstration of delta doping in silicon for the fabrication of shallow junctions in scaled-down Si lightly-doped drain (LDD) MOSFETs for integrated circuits (Si ICs) (with colleague Dr. H. J. Gossmann, 1990–1995)
- Invention of a new concept, *superlattice doping*, for enhanced p-type doping of GaN. All acceptors in GaN are deep, resulting in a low electrical acceptor activation of only 5 %. The new concept of superlattice doping is expected to increase the electrical activation of acceptors by more than a factor of ten (with post-doctoral associate Dr. W. Grieshaber, 1995)
- Investigation of yellow luminescence in GaN and the use of microcavity effects in Ag / GaN / sapphire structures to determine the refractive index of GaN (with post-doctoral associate Dr. W. Grieshaber, 1996)
- Demonstration of the first GaN / GaInN double heterostructure laser. The laser has cleaved facets and was optically pumped. Laser action was demonstrated by (i) a threshold in the light-versus-current characteristic, (ii) spectral narrowing below kT above threshold, (iii) a TE / TM polarization ratio greater than one hundred above threshold, and (iv) increased slope efficiency with increasing back-side facet reflectivity (with graduate student D. A. Stocker, 1997)
- Co-inventor of photonic-crystal light-emitting diode, PC-LED, jointly with group of Prof. John D. Joannopoulos at MIT (publication by Shanhui Fan *et al.* appeared in *Physical Review Letters* in 1997; US patent 5,955,749 was issued in 1999)
- First demonstration of crystallographic etching of GaN (with graduate student D. A. Stocker, 1998). The discovery, crystallographic etching, can be implemented by wet chemical etching, including photo-enhanced electrochemical (PEC) wet etching. The discovery is widely used in the LED industry to strongly enhance light extraction from LED chips and is found in LED light bulbs.
- Experimental demonstration of a ten-fold enhancement of p-type doping activation in $\text{Al}_x\text{Ga}_{1-x}\text{N}$ /GaN doped superlattices as compared to bulk GaN and $\text{Al}_x\text{Ga}_{1-x}\text{N}$ (with graduate students D. A. Stocker and I. D. Goepfert, 1999)
- Invention and demonstration of the photon-recycling semiconductor light-emitting diode (PRS-LED) which emits *white* light and many other colors with very high luminous performance of $> 300 \text{ lm/W}$ (with graduate students X. Guo and J. W. Graff, 1999). Invention of the monolithically integrated GaInN/GaN PRS-LED (with graduate students X. Guo and J. W. Graff, 2000)
- Invention and demonstration of polarization-enhanced ohmic contacts in p-type and n-type GaN (with graduate students Y.-L. Li and J. W. Graff 2000)
- Invention and demonstration of AlGaInP light-emitting diode with omni-directional reflector (ODR) for high light extraction efficiency (with post-doctoral associate Th. Gessmann and graduate student J. W. Graff, 2001)
- Developed novel model for high diodes ideality factors ($n \gg 2.0$) in UV LEDs based on multiple rectifying elements (with graduate student J. M. Shah and Prof. Th. Gessmann, 2003)
- Developed new class of materials, low-refractive index materials, or low- n materials, with an unprecedented low refractive index of $n < 1.10$; use of these materials as low- k materials for inter-metal-layer dielectrics in Si lightly-doped drain (LDD) MOSFETs in conjunction with ALD-deposited high- k gate dielectric MOSFETs for integrated circuits (Si ICs) (with Dr. Jong Kyu Kim, “JQ” Xi, Professors Joel Plawsky, Bill Gill, starting in 2003)
- Developed theory for temperature coefficient of forward voltage in light-emitting diodes, particularly UV light-emitting diodes (with graduate student Yangang “Andrew” Xi, Dr. Jong Kyu Kim, and collaborators at Sandia National Laboratories, 2004, 2005)
- Invented highly efficient “remote phosphor configurations” in white light-emitting diodes (with Jong Kyu Kim, Hong Luo, and collaborators at SAIT-Samsung) (2004, 2005)
- Discovered whispering gallery modes in white LEDs with remote phosphors (with graduate student Hong Luo, Jong Kyu Kim, Yangang “Andrew” Xi, and collaborators at SAIT-Samsung, 2005)
- Developed graded-index antireflection coatings that, unlike conventional anti-reflection coatings, have broadband omni-directional characteristics; the graded-index antireflection coatings use novel low- n materials (with Jingqun “JQ” Xi, Jong Kyu Kim, 2007)
- Developed efficiency-droop reducing GaInN / GaInN and GaInN / AlGaInN LED active regions grown by MOCVD and ALE that were demonstrated to reduce the efficiency droop by as much as 40% (with Jong Kyu Kim, Martin F. Schubert, Di Zhu, Jiuru Xu, Mary Crawford, and Dan Koleske, starting in 2007)
- Developed analytic model for efficiency droop based on drift-induced reduction of the carrier-injection

efficiency (with Guan Bo Lin, Jaehee Cho, and others, 2012)

Honors and awards

- Google Scholar profile, including the Hirsch-index (h-index) can be found at < <http://scholar.google.com> > under profile "E. Fred Schubert"
- Elected to *Senior Member* of the *IEEE* "in recognition of professional standing" (1993)
- Recipient of the Literature Prize of the *Verein Deutscher Elektrotechniker (VDE)* for "Doping in III–V semiconductors" (Cambridge University Press, Cambridge, 1993). Citation: "The book concerns all aspects of doping in III–V semiconductors. Fundamental, practical, and technological issues of doping are addressed. The book covers the basic theory of shallow donors, shallow acceptors, deep levels, and their influence on the free carrier concentration. It also discusses doping during growth, epitaxy, diffusion, and ion implantation. In the field of semiconductor devices, the book emphasizes applications requiring highly controlled doping distributions. It is an excellent monograph equally suited for study, research, and industry" (1994)
- Elected as a member of the *Bohemian Physical Society* (Cornell University, Ithaca, NY). Citation: "For seminal contributions to the control of spontaneous emission by use of wavelength-size optical cavities, specifically the first demonstration in a glass host using rare earth implanted Si/SiO₂ resonant microcavities" (1994)
- Listed in "Who's Who In Science And Engineering" and "Who's Who in America" published by *Marquis Who's Who*, publishers of the original *Who's Who in America*. (*Marquis Who's Who*, New Providence, NJ) ISBN 0-8379-5755-9 (1996 – present)
- Elected *Fellow of the SPIE* "For pioneering research in semiconductor doping and sustained contributions to the development of high-efficiency light-emitting diodes and lasers". According to the Society's bylaws, a Fellow "shall be distinguished through his achievements and shall have made outstanding contributions in the field of optics, or optoelectronics, or in a related scientific, technical, or engineering field" (1999)
- Recipient of the *Alexander von Humboldt Senior Research Award* of the Alexander von Humboldt Foundation, a Bonn-based non-profit organization promoting the exchange of scientific knowledge between German and highly qualified foreign scholars. According to the Alexander von Humboldt Foundation, academic qualification is the only selection criterion for the award. The award resulted in two extended visits with the Microoptics Laboratory of Professor Jürgen Jahns at the University of Hagen, Germany (1999)
- Elected to *Fellow of the IEEE* "for contributions to semiconductor doping and resonant-cavity devices". According to the IEEE definition "the grade of Fellow is one of unusual professional distinction conferred by the Board of Directors only upon a person of extraordinary qualifications and experience" (1999)
- Listed in the "Dictionary of International Biography, 29th Edition" published by the *International Biography Center*, Cambridge, United Kingdom (2000)
- Recipient of the 2000 *Discover Magazine Award for Technological Innovation* presented by the *Christopher Columbus Foundation* in the category "Energy". The prize was awarded "for the invention and demonstration of the photon recycling semiconductor light-emitting diode", an all-semiconductor LED capable of emitting white light with very high efficiency, see < www.discover.com/awards > (2000)
- Recipient of the *RD100 Award* of the R&D Magazine that honors the "100 most technologically significant products of the year" (with Klaus Streubel of Osram-Sylvania Corp. and Rickard Marcks von Wurtemberg of Mitel Corp.). The prize was awarded for the "*Resonant-cavity light-emitting diode*" that uses enhanced spontaneous emission occurring in resonant cavities. The device is used in plastic optical fiber communication links, in telescopes for rifles, and many other applications (2000).
- Elected to *Fellow of the OSA* "for the invention and demonstration of the resonant-cavity LED and the photon-recycling semiconductor LED". OSA Fellows are elected by the OSA Board of Directors (2001)
- Recipient of the Boston University Provost Innovation Fund Award (Provost Dennis D. Berkey) valued at \$ 25,000 for research and development of promising technologies (2001)
- Elected to *Fellow of the APS* "for pioneering contributions to the doping of semiconductors including delta doping, doping of compositionally graded structures resulting in the elimination of band discontinuities, and superlattice doping to enhance acceptor activation" (2001)
- Honored with RPI Medal as Senior Constellation Chair during Investiture Ceremony (2002)
- Received "2002 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award" (2002)
- Inducted as Wellfleet Senior Constellation Professor, Future Chips, Rensselaer Polytechnic Institute, November 21 (November 2003)

- Distinguished Lecturer of the IEEE Electron Devices Society (2003–2006)
- Elected member in Eta Kappa Nu (2004)
- “Best Oral Presentation Award” was won by Ph. D. student Hong Luo (who was the presenter), J. K. Kim, Y. A. Xi, J. M. Shah, Th. Gessmann and E. F. Schubert “Improvement of extraction efficiency of GaInN light-emitting diodes by employment diffuse omni-directional reflectors” *Connecticut Microelectronics & Optoelectronics Consortium (CMOC)*, 14th annual symposium, New Haven CT, March 17 (March 2005).
- “Best Student Poster Award” of the *International Semiconductor Device Research Symposium (ISDRS)* was won by Ph. D. student J.Q. Xi (presenter), Jong Kyu Kim, Dexian Ye, Jasbir S. Juneja, T.-M. Lu, Shawn-Yu Lin, and E. Fred Schubert “Optical Thin Films with Very Low Refractive Index and Their Application in Photonic Devices”, *International Semiconductor Device Research Symposium (ISDRS)*, Dec. 7–9, Bethesda, MD (December 2005)
- “MRS Silver Award” of the Materials Research Society was won by Ph. D. student Yangang Andrew Xi (who was the presenter), K. X. Chen, F. Mont, J. K. Kim, C. Wetzel, E. F. Schubert, W. Liu, X. Li, J. A. Smart “Extremely high quality AlN grown on (0001) sapphire by using metal-organic vapor-phase epitaxy” *Materials Research Society (MRS) Fall Meeting*, Boston MA, November 27 – December 1 (2006) Boston MA (December 2006)
- “25 Most Innovative Micro- and Nano-Products of 2007 Award” in July 2007 issue of *R&D Magazine* and *Micro/Nano Newsletter*. This recognition was given for the “Non-Reflective Coating” product that was published in *Nature Photonics* in 2007; full citation: Xi, J.-Q., Martin F. Schubert, J. K. Kim, E. F. Schubert, Minfeng Chen, Shawn-Yu Lin, Wayne Liu, and Joe A. Smart “Optical thin-film materials with low refractive index for broadband elimination of Fresnel reflection” *Nature Photonics* **1**, 176, March 2007 (July 2007)
- “SCIENTIFIC AMERICAN 50 AWARD” of 2007, as published in the January 2008 issue of *Scientific American*. According to the *Scientific American Magazine*, this award “celebrates visionaries from the worlds of research, industry and politics whose recent accomplishments point toward a brighter technological future for everyone” (January 2008)
- “EDITORS’ CHOICE” of *Science Magazine*, *Science*, Volume **319**, page 1163, February 29 (February 2008). This distinction was awarded for the publication: Jong Kyu Kim et al., “Light-extraction enhancement of GaInN light-emitting diodes by graded-refractive-index indium tin oxide anti-reflection contact” that appeared in *Advanced Materials* **20**, 801, 2008 (February / March 2008)
- Received “2008 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award” (2008)
- “Best Oral Presentation Award” won by David J. Poxson (who was the presenter), Frank W. Mont, Jong Kyu Kim, and E. Fred Schubert “Multilayer nano-structured anti-reflection coating with broad-band omni-directional characteristics” *Connecticut Microelectronics and Optoelectronics Conference (CMOC)*, University of Connecticut, Storrs, Connecticut, April 9 (April 2008)
- “Best Oral Presentation Award” for presentation: David Meyaard, Sameer Chhajed, Jaehee Cho, E. Fred Schubert, Jong Kyu Kim, Daniel D. Koleske, and Mary H. Crawford “Temperature-dependent light-output characteristics of GaInN light-emitting diodes with different dislocation densities” *Connecticut Microelectronics and Optoelectronics Consortium (CMOC) Symposium*, New Haven CT, March 2 (March 2011)
- Identified as top 1% of patentees in the field of optoelectronics by study conducted by Professor Erica Fuchs of Carnegie Mellon University under a study supported by the US National Science Foundation (July 2011)
- Received “2012 Rensselaer Polytechnic Institute Trustee Faculty Achievement Award” (November 2012)
- My “LinkedIn” profile was one of the top 10% most viewed “LinkedIn” profiles during 2012 (January 2013)
- My graduate student, Mr. Ming Ma, received the \$ 30,000.00 Lemelson-Rensselaer Student Prize for the invention entitled “Graded-refractive-index (GRIN) structures for brighter and smarter light-emitting diodes”; The Prize is awarded annually by the Lemelson Foundation (March 2013)

Service to the technical community

- Current or former member of the *American Physical Society* (Member of the *Division of Materials Physics*, Member of the *Division of Condensed Matter Physics*), *Institute of Electrical and Electronics Engineers*, *Materials Research Society*, *Optical Society of America*, *Society for Optical Engineering (SPIE)*, and the *Verein Deutscher Elektrotechniker*
- Co-author of hundreds of research articles, co-inventor of more than 30 United States patents, and numerous foreign patents (1981 – present)
- Gave many invited talks at scientific conferences organized by the *American Physical Society*, *Institute of Electrical and Electronic Engineers*, *Materials Research Society*, *SPIE (The International Society for Optical*

Engineering), *Electrochemical Society*, *American Vacuum Society*, *Engineering Foundation*, and other professional societies (1985 – present).

- Co-editor (with A. M. Glass) of a Special Issue of the *Journal of Optical and Quantum Electronics* (Vol. **22**, 1990) on “Charge-transport assisted optical non-linearities in semiconductors” (1990)
- Symposium chair of the *American Vacuum Society Greater New York and New Jersey Chapter* on “Epitaxially grown semiconductors with atomic level control” (1991).
- Moderator of MRS Internet discussion on “Doping and Dopants in GaN” (MRS Internet Journal, 1995 – 1997)
- Member of review panels of the National Science Foundation (1995 – present)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose, CA (1997)
- Technical work has been featured in popular journals, magazines and newspapers including the *New Scientist*, *Discover Magazine*, *Wall Street Journal*, *Boston Globe*, *Focus*, and on National Public Radio (1996 – present)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose, CA (1998)
- Program Committee Member: IEEE IEDM, International Electron Devices Meeting (1999 and 2000)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose, CA (1999)
- Program Committee Member: ISBLLED, International Symposium on Blue Laser and Light-Emitting Diodes, Berlin, Germany, March 5 – 10 (2000)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose, CA (2000)
- Conference Chair and Co-Organizer of the TMS- and ONR-sponsored conference on “Doping, Dopants, and Low Field Carrier Dynamics in Wide Gap Semiconductors”, Copper Mountain, Colorado, April 2 - 6 (2000)
- Chair, IEEE LEOS, Central New England Chapter. During my tenure as Chair, the Central New England Chapter won the IEEE LEOS Chapter award for the highest membership growth (1999 – 2000)
- Expert Witness involving semiconductor materials, devices, and packaging including elemental and compound semiconductors such as Si, SiGe, SiC, as well as III–V arsenides, phosphides and nitrides (1998 – present)
- Member of the Board of Governors, IEEE Laser and Electro-Optics Society (LEOS) (1999 – 2000)
- Member of the Optoelectronics Industry Development Association (OIDA) Roadmap Panel on Solid-State Lighting, Albuquerque NM Oct. 26 – 28 (2000)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose, CA (2001)
- Panel Member of National Research Council meeting on “Solid-State Lighting:” held at NAS and NAE, Washington DC, March 26 (2001)
- Program Committee Member of SPIE Photonics West conference on “Laser and LED Applications” chaired by Dr. Kurt Linden, San Jose CA Jan (2002)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose, CA (2002)
- Program Committee Member: ISBLLED, International Symposium on Blue Laser and Light-Emitting Diodes, Cordoba, Spain, March 11–15 (2002)
- Program Committee Member for subcommittee on “Semiconductor lasers and LEDs” for OSA Conference on Lasers and Electro-Optics and Quantum Electronics and Laser Science Conference (CLEO / QELS) (2002 – 2003) Baltimore MD June 1–6 (2003)
- Reviewer for the National Research Council of report entitled “Partnerships for Solid-State Lighting: Report of a Workshop” authored by the Board on Science, Technology, and Economic Policy. This report is forwarded to the US Congress for the initiation of a national Solid-State Lighting Initiative. (2002)
- Program Committee Member “Lester Eastman conference on high performance devices” University of Delaware, Newark, Delaware, August 6 – 8 (2002)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose CA (2003)
- OIDA Next Generation Lighting (NGL) Consortium. Member of “Light-Emitting Diode” Committee (2003)
- Program Committee Member, International Semiconductor Device Research Symposium (ISDRS) Washington DC, Dec. 8 – 12 (2003)
- Program Committee Member of “Display and Solid-State Lighting Devices” conference for OSA/IEEE

- Conference on Lasers and Electro-Optics (CLEO) (2003 – 2004)
- Elected Member of the IEEE Electron Device Society Administration Committee (IEEE AdCom) (2003–2008)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose CA (2004)
- Program Committee Member “Fourth International Conference on Solid-State Lighting” August 2 – 6 Denver, CO (2004)
- Program Committee Member for the “Blue 2004: Advanced LEDs and Lasers Conference” Hsinchu, Taiwan, May 10–12 (2004)
- Conference Chair of SPIE Photonics West conference on “Light-emitting diodes: Research, Manufacturing, and Applications” San Jose CA (2005)
- Program Committee Member “International Semiconductor Device Research Symposium” December 7 – 9 Washington, DC (2005)
- Chair of “Display and Solid-State Lighting Devices” conference of OSA/IEEE Conference on Lasers and Electro-Optics (CLEO) (2005)
- Best Oral Presentation Award (Presenter: Hong Luo) at *Connecticut Microelectronics & Optoelectronics Consortium* (CMOC), 14th annual symposium, New Haven CT, March 17 (March 2005)
- Conference Chair of MRS Spring meeting “Symposium DD: Solid-State Lighting Materials and Devices” San Francisco, April 17–21 (April 2006)
- Member on the International Advisory Committee of *First International Conference on Display LEDs* (ICDL 2007), Seoul, Korea, January 31 to February 2 (2007)
- Member, Program Committee of *SPIE Photonics West* conference “Light-Emitting Diodes: Research, Manufacturing, and Applications XI” San Jose, CA, January 20 – 25 (2007)
- Program Chair of *SPIE Photonics West* conference “Semiconductor Lasers and LEDs” San Jose, CA, January 20 – 25 (2007)
- Member, Executive Organizing Committee *SPIE Photonics West* conference “LASE 2007” San Jose, CA, January 20–25 (2007)
- Opto Track Chair of *SPIE Photonics West* conference “Semiconductor Lasers and LEDs” San Jose, CA, January 21 – 24 (January 2008)
- Member, Program Committee, Light-emitting diodes: Research, Manufacturing, and Applications, SPIE Photonics West 2008, San Jose, California, January 19 – 24 (January 2008)
- Program Committee Member of the 7th International Symposium on Semiconductor Light Emitting Devices (ISSLED-2008) held in Phoenix, Arizona (USA), April 27 – May 2 (April 2008)
- Member, Program Committee, China SSL 2008, Shenzhen Convention & Exhibition Center, China, July 24 – 26 (July 2008)
- Member, Program Committee, International Workshop on Nitride Semiconductors, IWN 2008, Montreux, Switzerland, October 6 – 10 (October 2008)
- Opto Track Chair of *SPIE Photonics West* conference “Semiconductor Lasers and LEDs” San Jose, CA, January 25 – 29 (January 2009)
- Guest Editor of Special Issue on *Solid-State Lighting* published in the *IEEE Journal of Selected Topic in Quantum Electronics*, July / August edition (August 2009)
- Honorable Conference Chair, 6th China International Forum on Solid-State Lighting (China SSL), Shenzhen Convention & Exhibition Center, China, October 14 – 16 (October 2009)
- Program Committee Member, International Conference on Nitride Semiconductors (ICNS), Jeju, South Korea, October 18 – 23 (October 2009)
- Program Committee Member, The Second International Conference on White LEDs and Solid-State Lighting, Taipei, Taiwan, December 13 – 16 (December 2009)
- Editor, *Compound Semiconductors and Energy Applications and Environmental Sustainability*, Materials Research Society (MRS) Symposium Proceedings Volume 1167 (MRS, Warrendale PA, 2009)
- Conference Chair, OPTO, *SPIE Photonics West 2010*, San Francisco, California, January 23 – 27 (January 2010)
- Guest Editor of Special Issue on *Light-Emitting Diodes* published in the *IEEE Transactions on Electron Devices* (January 2010)
- Program Committee Member, *8th International Symposium on Semiconductor Light Emitting Devices* (ISSLED), Beijing, China, May 16 – 21 (May 2010)

- International Advisory Committee Member of the 16th *Microoptics Conference* (MOC'10) held in Hsinchu, Taiwan, sponsored and endorsed by OSA and IEEE/Photonics Society and organized by National Chiao Tung University, Oct. 31 to Nov. 3 (October 2010)
- Member of Academic Committee of *China Solid-State Lighting Conference* (CHINA SSL 2010) Shenzhen, China, October 14 – 16 (October 2010)
- Conference Co-Chair, OPTO, *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Executive Organizing Committee OPTO, *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XV *SPIE Photonics West 2011*, San Francisco, California, January 22 – 27 (January 2011)
- Member of CLEO Subcommittee 15, entitled "LEDs, Photovoltaics and Energy-Efficient ("Green") Photonics" for the 2011 Conference on Lasers and Electro-Optics (CLEO), Baltimore, Maryland May 1 – 6 (May 2011)
- Member of the Academic Committee of the 8th China International Forum on Solid-State Lighting (CHINA-SSL-2011) Guangzhou November 8 – 10 (November 2011)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XV *SPIE Photonics West 2012*, San Francisco, California, January 21 – 26 (January 2012)
- Member of CLEO Subcommittee 15, entitled "LEDs, Photovoltaics and Energy-Efficient ("Green") Photonics" for the 2012 Conference on Lasers and Electro-Optics (CLEO), San Jose, California, May 6 – 11 (May 2012)
- Member of Academic Committee of the 9th China International Forum on Solid-State Lighting (CHINA SSL 2012), Guangzhou, China, November 5 – 7, 2012 (November 2012)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XVI *SPIE Photonics West 2013*, San Francisco, California, 2 – 7 February 2013 (February 2013)
- Member of CLEO Subcommittee in the topic area: "Science & Innovation 15: LEDS, Photovoltaics and Energy-Efficient ("Green") Photonics" for the CLEO 2013 conference, April 28 – May 3, 2013 in Baltimore, Maryland (May 2013)
- Member, International Advisory Committee of the International Conference on Advanced Electromaterials (ICAE 2013) held on Jeju Island, Korea, from November 12 – 15, 2013 (November 2013)
- Program Committee Member, *Solid-State and Organic Lighting (SOLED)*, OSA Topical Meeting, 3 – 7 November 2013, Marriott Tucson Star Pass, Tucson, Arizona, USA (November 2013)
- Co-Chair, OPTIC International Conference, Chung Li, Taiwan, National Central University, December 5 – 7, 2013 (December 2013)
- Program Committee Member of conference entitled: "Light-Emitting Diodes: Materials, Devices, and Applications for Solid-State Lighting XVII" *SPIE Photonics West 2013*, San Francisco, California, 1 – 8 February (2014)
- Publication Committee Member, *5th International Conference on White LEDs and Solid-State Lighting* (White LEDs), Jeju Island, Korea, May 25 – 28, 2014 (May 2014)
- Sub-Committee Chair of Track 6: Displays, Solid-State Lighting, Photovoltaics, and Energy-Efficient Photonics of *Asia Communications and Photonics Conference 2014* (ACP 2014). ACP is the largest and the most influential conference in Asia and Pacific Rim for communications and photonics technologies. ACP 2014, Shanghai International Convention Center, Shanghai, China, November 11 – 14 (2014)
- International Consultant of technical seminar of the 11th China International Forum on Solid-State Lighting (SSL-China 2014) Guangzhou, China, November 6 – 8 (2014)
- Member of the International Advisory Committee of the 11th International Symposium on Semiconductor Light Emitting Devices (ISSLED 2017) held in Banff, Canada on October 8 – 13 (2017)
- Assisting the US Judicial Government Branch (various US District Courts), the USPTO (US Patent and Trademark Office) and the ITC (International Trade Commission) by serving as an independent Technical Expert Witness (1997 to present)

Books

- ***Doping in III-V semiconductors*** (author) Hardback and paperback, 628 pages (Cambridge University Press, Cambridge, UK, 1993). The following excerpt is from a book review by D. L. Miller, *University of Pennsylvania*, University Park PA, which appeared in *Physics Today*, Oct. 1994, p. 71: “[...] Fred Schubert has written a book that very nicely fills two roles: It serves as a reference volume for those of us who use III-V materials, and it provides enlightening explanations of interesting and important problems in semiconductor physics. [...] Schubert, who is employed by AT&T Bell Laboratories, brings his extensive research involvement with III-V materials physics straight to this book. His lucid explanations of some of the important physics of doped semiconductors is a major strength. For example, the chapter on deep centers provides the clearest treatment of the DX center I can remember reading, and it uses the large lattice distortion model and configurational coordinates introduced for the DX center to describe the EL2 deep level. This book can also serve as an excellent reference volume, because it briefly describes epitaxial growth techniques and the doping methods used with them, catalogs dopant-related phenomena, describes characterization techniques and provides 45 pages of citations to published articles and books. [...] I will use it to help my graduate students in the physics of semiconductors. [...] It will certainly be available on my bookshelf, in part to remind me what the Burstein-Moss shift is and in part for the literally hundreds of references that it provides on nearly every topic related to III-V semiconductor doping. Because of its clarity in treating some interesting phenomena of modern semiconductor physics, you too might want to get a copy of this book, even if you believe that Ga and As are just poor alternatives for doping silicon”
- ***Delta doping in semiconductors*** (editor) Hardback and paperback, 616 pages (Cambridge University Press, Cambridge, U. K., 1996)
- ***Light-emitting diodes*** (author) Hardback and paperback, 328 pages (Cambridge University Press, Cambridge, UK, 2003). The following excerpt is from a book review by David Bour, *Agilent Laboratories*, Palo Alto CA, which appeared in *Physics Today*, Nov. 2004, p. 66: “[...] In “*Light-emitting diodes*”, E. Fred Schubert provides an excellent review of the physics and technology of semiconductor LEDs. [...] Interesting anecdotes like [the first demonstration of electroluminescence], clearly written by someone with a broad perspective and expertise, appear throughout the book, making it enjoyable to read. [...] Schubert provides an excellent description of the undesirable [non-radiative] recombination pathway. [...] Schubert has made pioneering contributions to those devices, and this variety of LEDs may become more widely used in the future. [...] Overall, “*Light-emitting diodes*” is an excellent examination of the physics and technology of semiconductor LEDs. The narration is simple and direct, and the book is well referenced for those seeking a deeper understanding of the topic. Written for the graduate level, the text will appeal to a broad audience; and for specialists who make semiconductor LEDs and laser diodes, it will serve as a useful connection to the scientific literature.”
- ***Light-emitting diodes, second edition*** (author) Hardback, 422 pages (Cambridge University Press, Cambridge, UK, 2006)
- ***Physical Foundations of Solid-State Devices*** (author) eBook, 275 pages, ISBN-13: 978-0-9863826-2-8 (Google Books, Mountain View CA, 2015)
- ***Light-emitting diodes, 3rd edition*** (author) eBook, 672 pages with hundreds of colored illustrations, ISBN: 978-0-9 863826-6-6 (Google Books, Mountain View CA, 2018) “The 1st edition of the book “*Light-Emitting Diodes*” was published in 2003. The 2nd edition was published in 2006. The current 3rd edition of the book is a substantial expansion of the second edition and has 37 chapters. The book includes a thorough discussion of white light-emitting diodes (LEDs), phosphor materials used in white LEDs, packaging technology, and the various efficiencies and efficacies encountered in the context of LEDs. The background of light, color science, and human vision is provided as well. The fully colored illustrations of the 3rd edition are undoubtedly beneficial given the prominent role of light and color in the field of LEDs. The book is a comprehensive discussion of the LED, particularly its semiconductor physics, electrical, optical, material science, thermal, mechanical, and chemical foundations. The 3rd edition is published in electronic format in order to make the book affordable and easily accessible to a wide readership.”

Courses and laboratories developed at Boston University

- Developed first laboratory for “Physics of semiconductor devices” (SC-471) Fall (1998)
- Developed course “Quantum mechanics applied to semiconductor devices” (SC-574) Fall (1999)

- Developed course “Semiconductor light emitters” (SC-760) Fall (2000)
- Developed distance-learning course and NTU course on “Light-emitting diodes – Device physics and applications” Fall (2000)

Courses taught at Boston University

- Undergraduate Course “Physics of semiconductor devices” (SC-471)
- Graduate course “Fiber optic communication systems” (SC-563)
- Graduate course “Quantum mechanics applied to semiconductor devices” (SC-574)
- Graduate course “Introduction to solid-state physics of devices” (SC-577)
- Graduate course “Quantum electronics” (SC-700)
- Graduate course “Integrated optoelectronics” (SC-770)
- Graduate course “Compound semiconductor devices” (SC-771)
- Graduate course “Light-emitting diodes” (SC-760)
- Graduate course “Research seminar” (SC-860, SC-892)
- Other courses “Research”, “Guided Study”, “Master Thesis”, and “Dissertation” (SC-900)

Courses taught at Rensselaer Polytechnic Institute

- Graduate Course “Semiconductor devices and models II” (ECSE-6290)
- Undergraduate course “Microelectronics technology” (ECSE-2210)
- Undergraduate course “Fields and Waves 1” (ECSE-2100)
- Graduate course “Quantum mechanics applied to semiconductor devices” (ECSE-6968)
- Graduate course “Physical foundations of solid-state devices” (SC-6960)
- Graduate course “Light-emitting diodes and solid-state lighting” (SC-6961)
- Undergraduate course “Introduction to Electronics” (ECSE-2050)
- Other courses “Research”, “Guided Study”, “Master Thesis”, and “Dissertation”

Teaching evaluations and students’ comments

1997 – Students made the following comments: “Clear ... organized ... excellent explanations ... I’ve never had a professor like him – I wish all were like him ... very clear and concise presentations ... strong response to students’ questions and concerns ... Professor provided excellent notes ... laid out lectures in a clear and precise manner which worked out wonderfully ... well organized and confident ... responsive to students’ concerns ... excellent for students going into the semiconductor industry ... excellent hand-outs and course materials ... well prepared ... clear lectures ... I was strongly encouraged ... materials are very interesting ... hand-outs were excellent ... material is very important ... the presentation of materials was very clear ... hand-outs were excellent support to the class ... efforts made by Prof. Schubert in keeping everyone at the same pace was remarkable ...”

1998 – Students made the following comments: “Professor was always well prepared ... excellent content ... very relevant for the field of solid-state devices ... excellent preparation for the class ... handouts were very good ... very well-organized teacher ... excellent knowledge of material ... provided a complete background of all material ... easy to talk to ... excellent overall teaching skills ... really enjoyed coming to class ... his choice of topics and homework helped me a lot ... enthusiastic in teaching and helpful during the office hours ... one of the best professors I have had at BU ... course gave a very good overview of the different solid-state physics principles ... the course was very well organized ... relevant examples and homework were given ... good explanations were given ... presented clearly ... presentation was clear ... communicated effectively ... very knowledgeable ... good demonstrations in class ... gives clear descriptions ... asks questions of class ... grades homework fairly ... good at answering questions ... no weak points ... excellent instructor and scientist ... inspiring professor ... thorough ... the instructor is very precise and well prepared ... his knowledge of the material is exact ... very responsive to feedback ... encourages student questions, class participation and discussion ... the instructor cared about whether students understood material ... the instructor used applications immediately after showing theory ... handouts were excellent ... guest lecture and lab tour excellent idea ... excellent class notes ... presented topics neatly ... well prepared ... review of ongoing research topics was great ... Professor Schubert is undoubtedly an expert in his area ...”

1999 – Students made the following comments: “He enjoyed teaching the material and was very clear ... the presentation of the material in class was excellent ... he helped me to understand a lot about semiconductors ... Prof. Schubert always tried to make sure that we would all have a clear understanding of the material ... manuscripts were very helpful ... encouraged lots of class participation and was always readily available for help ... presentation was excellent ... the instructor was always willing to help me ... very helpful ... Clearly, Prof. Schubert is *more* than just extremely knowledgeable about this material ... very thorough and exact communication of points ... excellent course packet written by the instructor ... he was very well prepared for class ... He is extremely fair and encourages participation ... he is also very accessible ... excellent instructor ... very approachable and easy to ask questions of ... handouts were very effective and helpful ... Prof. Schubert is very prepared and concepts are well explained ... materials will be very useful for my future ... very open to questions”

2000 – Students made the following comments: “He did a lot of experiments which really helped ... the material is very interesting and cutting edge ... clear presentations ... good in-class demonstrations ... very clear lectures ... the material really does challenge you ... takes the time to answer your questions ... very interesting material ... relevant to today's world of communication ... the field trip was fun ... in-class demonstrations really added to class ... good understanding of course material ... excellent details, willing to help, good explanations ... in-depth details on quantum mechanics ... the instructor was extremely accessible to students ... he encouraged participation in class ... he gave intuitive arguments and explained concepts in a very physical way ... I very much enjoyed Professor Schubert and would like to take more classes with him ... material was very beautiful ... I *very much* enjoyed the papers that were discussed ... everything is well organized ... hand-out material is very complete and clear ... lectures are clear ... the professor prepared an excellent manuscript ... explained things very clearly ... he has strong enthusiasm to solve students' questions ... it's a very important course ... Professor follows the course notes exactly, so one can concentrate on material without having to focus on details ... clearly presented material ... the course is great preparation for future courses in solid-state physics ... I greatly admire Professor Schubert ...”

2001 – Students made the following comments: “He has a thorough understanding of the subject ... I like the fact that he shows us examples in class demonstrations ... the manuscript was good ... instructor provides good notes ... materials are presented clearly ... in this course you learn a lot ... very illustrative and in depth ... very interesting course ... Professor presented the material well ... Professor seemed to have a strong grasp on what he was teaching ... the basics were presented correctly ... smooth transition into more complex materials ... presented basics well ... Professor's strong points are knowledge, organization and class materials ... clear conception ... very important and useful class ... Professor knew what was going on ... manuscript and his notes were very helpful ... responded to suggestions ... notes were comprehensive ... just fine ... manuscript was good ... knows the material very well ... notes handed out are good ... expert knowledge of material ... developed lectures logically and straightforward ... lecture notes were prepared for us - very nice touch ... Professor has deep knowledge of the materials ... Professor is always prepared for lectures ... he emphasizes principles and the concepts ... good preparation ... good stuff and clear presentation ... good research and industry experience ... excellent handout notes and materials ... excellent teaching skills ... inspires the interest of students ... great knowledge of material ... well organized course notes ... Professor Schubert gave very clear instructions ... listening to his presentation is a true enjoyment of an excellent art of lecture style ... the manuscript has the quality of an excellent book ... the manuscript was an excellent reference source book ... the instructor was very clear and well organized and encouraged participation ... text [written by Schubert] was extremely good ... expert knowledge of materials ... class demonstrations were very beneficial ... can clearly relate complex ideas – very good ... has a high amount of patience ... excellent understanding of material ... very enthusiastic in teaching ... always available for discussion ... very knowledgeable ... I don't see any weak points ... he explains the theory very clearly ...”

2002 – Students made the following comments: “Always prepared ... presented difficult material in a manner that was easy to understand ... presented everything neatly ... very helpful and organized ... presents subjects in a very easy and friendly format ... very well qualified ... great experience ... very detailed notes ... well organized ... very useful ... very good diagrams and explanations ... he knows the material extremely well ... notes given to us are extremely helpful ... professor was very knowledgeable ... was able to answer any of our questions ... very informative course ... very knowledgeable and a great teacher ... the instructor is enthusiastic to teach students ... the instructor can explain the theory very clearly ...”

2003 – Students made the following comments: “Great overall knowledge ... good organization skills ... demonstrations were very interesting and useful ... effective instructor ... handouts were extremely useful and

organized ... good course for completely understanding many points of fiber optics ..."

2004 – SPIE short course: "Encouraged questions and handled them well ... excellent short course ... I really appreciated and enjoyed this course ... good course – covered very broad matters ... the instructor was very knowledgeable on the topic ... excellent! ..."; RPI Semiconductor devices and models II (ECSE 6290): Overall excellence of teacher: 4.8 out of 5.0. Student comments: "course was very well prepared ... [course] was very organized ... this is an excellent course ... I learned a lot from this course ... the course was very good ... thanks Prof. Schubert for a wonderful course ... it's been a great course ... thank you ..." RPI Microelectronics Technology (ECSE 2210): Overall excellence of teacher: 4.7 (average 4.2). Overall excellence of course: 4.3 (average 3.9). Student comments: "Understandable presentation ... great job [of] Prof. Schubert ... very nicely done class ... very helpful throughout the entire course ... provided timely explanations to complicated material ... very informative ... course was fun and interesting ... very interesting lecturer ... very down to earth and easy to ask for help ... [instructor] did a good job in presenting [material] ... good course ... fun course ... excellent instructor ... he is a great guy and very knowledgeable ... I would definitely take a class from him again" **Book review** by Neal Oldham (San Jose, CA, USA) on "Doping in III–V semiconductors" (E. F. Schubert, Cambridge University Press, Cambridge UK, 1993) on amazon.com (May 17, 2002): "[This is the] best book I've encountered in the semiconductor field. This is, no question, the best book that I've encountered in the entire field of semiconductor physics. It is expertly organized and indexed, easy to follow, complete in its treatment of electrical and materials-science aspects of III–V semiconductor production and measurement, well-written ... worth every penny if you even have the most remote interest in the subject." **Book review** by Debdeep Jena (Santa Barbara, CA, United States) on "Doping in III–V semiconductors" (E. F. Schubert, Cambridge University Press, Cambridge UK, 1993) on amazon.com (July 6, 2001): "Very useful text for semiconductor crystal growers. Doping is a big, big issue in semiconductors; this text does appreciable justice in its treatment of the issue. In addition, Schubert treats heterostructure physics appreciably well (in fact better than many textbooks on semiconductor physics!). Perusal of this book has proved very rewarding for me, and I expect it will do the same wonder for you too."

2005 – SPIE Photonics West short course student comments: "Very good instructor! ... very knowledgeable ... clear on complex subjects ... good job fielding questions ... (numerical score 4.3 out of 5.0). Educational materials on the web: ... I have greatly enjoyed your LED slideshow. CLEO short course: ... very good and well-organized course!" ECSE 6968: "Class presentations were very helpful in learning ... very useful in learning the details of fundamental concepts ... the course is very good ... the course is excellent for engineers ... your [...] treatment brought about a much better understanding ... examples were great and helpful ... [discussion of] history and photons [...] helped increase interest ... After your course now, I can actually approach a quantum mechanics text book without fear ... overall, I just wanted to say – *thank you* ... excellent course ... the instructor made it interesting and taught very effectively ... the manuscript provided was also very well written ... class was excellently structured ... will benefit my studies in the future ... especially liked the term paper requirement ... Prof. Schubert is an excellent instructor, who is well prepared ..." (excellence of instructor: 4.8 out of 5.0). SPIE Photonics North short course: "Very good and clear in presentation ..." (numerical score 4.4 out of 5.0). ECSE 6960 mid-course and final feedback by students: "Professor has provided all course materials ... I really appreciate it ... well presented ... technical support was great ... my learning experience has been good ... responses to my homework questions have been very timely ... I have enjoyed the course and found it interesting and useful ... homework assignments have been extremely beneficial ... the set of notes is very comprehensive ... good class structure ..." (numerical scores of students' course and instructor evaluation: 5.0 out of 5.0). Comment on web educational materials: "Notes look very thorough and clear ..."

2006 – SPIE Photonics West short course student feedback: "Excellent, knowledgeable ... excellent presentation ..." (numerical score 3.91 out of 5.0). ECSE 6961 (Light-emitting diodes and solid-state lighting): "excellent ... Informative, comprehensive and interesting ... the best part of this course, in terms of my learning experience, has been the course materials ... just an outstanding class ... so much is newly discovered and so much is current on-going research and commercially relevant ... Dr. Schubert is obviously a leading researcher and did a great job of conveying his experience and understanding to the class ... a highly technical topic that still makes a good general conversational topic ... I liked the course material ... I liked the fact that Prof. Schubert lectured directly from the textbook ... I liked the structure of the course ... I learned a lot about lasers and LEDs and other optical devices ... it is a basic and fundamental class ... the instructor gives ideas, concepts, and samples very clearly ... very good course ... students interested in LEDs and solid-state lighting are strongly recommended to take it ... liked the overall coverage ... the teaching pace was good ... he covered a lot of material that is important for the subject, but it was clearly always related to the topic ... the manuscript that he let us use was

excellent in my opinion ... the most important thing I liked about the course was the course material and the structure of the course ... right amount of homework and the two exams and the term paper presentation ... it was great to learn this course from someone who is a world leader in this field ... well-organized material ... liked the course format ... organization was good ... allowed me to know exactly what we were covering so I could look through the material prior to the lecture ... course content was good, starting with LED basics and covering materials through modern technologies, and then a look at solid-state lighting and sort of an intro to communication devices ... good fundamentals in LEDs ... GREAT Professor ... awesome course ... informative course ... ability to view course materials online was helpful ... very fruitful course ... covering a lot of materials ... very good and very important for graduate students to take this one ... for people in industry it's also useful ... for the instructor, this course is thought through very clearly ... the text book is also very good ... great course ... excellent instructor ... cute instructor ... course is very good ... I benefited a lot from it ..." (numerical scores: 4.7 out of 5.0). ECSE 2210 (Microelectronics Technology) student comments "Excellent teaching method ... I like that the Professor asks random questions at the end of class – it helped me understand the subject better ... I thought Prof. Schubert was fabulous ... his organization of the class encouraged learning ... I highly recommend this class to everyone ... a devoted and involved teacher ... displayed more enthusiasm in teaching than other Professors I had ... he also seemed to have a philosophy about teaching that was beyond helping students get good grades ... he emphasized real-world applications of material and had general advice about working in the real world after leaving academia ... helpful ... although he was harder in grading and exams, Prof. Schubert challenged us more and made the course more interesting ... the many class activities provide lots of practice of materials just learned ... provided good back-up information ... made sure students understand concepts ... thank you for asking students questions during class to reinforce concepts ... thank you for allowing open book exams ..." (numerical scores: excellence of teacher 4.4 out of 5.0; excellence of course 4.3 out of 5.0; overall average of ratings 4.4 out of 5.0)

2007 – Book review by Steven J. Wojtczuk (Lexington, MA, USA) on "Light-Emitting Diodes" (E.F. Schubert, Cambridge University Press, Cambridge UK, 2003) on amazon.com (March 14, 2006): "Schubert (RPI) has written an excellent book on LEDs that manages to explain and derive simple quantitative models for many phenomena of current interest ... many monographs are a compendium of results in the field with hundreds of references ... in contrast, Schubert, while giving copious references, is the sole author, leading to a coherent presentation well suited to learning ... there are plentiful and good figures and drawings, as well as many exercises and solutions integrated into the text ..." SPIE photonics West Short Course: "Excellent talk ..." ECSE 2210 (Microelectronics Technology) "Thank you ... great course ... excellent instructor ... interesting course ... appreciated that you did not lecture completely from the slides and that you probed the class to ensure that we were understanding the key points ... course is fine ... good professor ... Professor Schubert is one of the best lecturers I had ... the pace at which he moves the topic, the way he explains things, and the manner in which he asks students questions all came together to help me learn much more from his lectures than I could on my own ... instructors are absolutely very intelligent ... Professor Schubert was a good professor ... I actually learned things when Professor Schubert taught ..." ECSE 6968 (Physical Foundations of Solid-State Devices) "The instructor explained every concept in a very simple and effective manner ... I really enjoyed taking this course ..." (numerical scores: 4.5 out of 5.0)

2008 – SPIE Photonics West short course feedback: "Very good ... clear ... very nice ... answered questions readily ..." (numerical score 4.3 out of 5.0) ... ECSE 6961 (Light-emitting diodes and solid-state lighting) feedback: "It was great for me to have the opportunities to take two consecutive classes, *Physical Foundation* and *LEDs*, from you ... both these classes have taught me a lot ... they were very well organized ... thank you for all the help ... I have really enjoyed your classes ... relevant material ... very good professor ..." (numerical scores: 4.3 out of 5.0) ... Internet educational materials feedback: "I recently came across your course notes while trying to get a basic understanding about semiconductors and I wanted to thank you. Your notes for course "ECSE-2210 Microelectronics Technology" are the most useful and informative thing I have found on semiconductors on the Internet. I'm a chemist by trade and this is a great introduction for me ..." 2007 Chautauqua Short Course and High School Teacher Summer Course, held at RPI June 26 and July 12, 2007 (numerical average of scores: 9 out of 10) ... ECSE 6968 (Physical Foundations of Solid-State Devices) feedback: "Prof. Schubert is one of the best professors I've ever had ... his ability to explain difficult and complex materials in a clear and concise manner is unmatched ... the presentations, although time consuming, I felt were a great idea ... thanks for your efforts professor! ... I have really enjoyed taking this course ..." By email: "Thank you professor ... it has been a pleasure taking this course with you ..." (numerical scores: 4.4 out of 5.0)

2009 – SPIE Photonics West short course feedback by students: "One of the best short courses I have taken ...

it was very nice to hear about the history of LEDs ... very interesting but also very theoretical ...” (numerical score 4.1 out of 5.0). ECSE 2210 (Microelectronics Technology) “Great course ... instructors were excellent ... encourages students to stay up to date with the subject matter ... Thanks for this well-organized class ... [the instructor] tries to get students to come out with the best grade possible ... this was a good class ...” ECSE 6968 (Physical Foundations of Solid-State Devices) feedback by students: “It is really an excellent course ... clear hand script ... great professor! ...” (numerical scores: 4.7 out of 5.0)

2010 – SPIE Photonics West short course feedback by students: “Good to get the latest data and charts ... very good ... very broad course and well organized ... it was great ...” (numerical score 4.04 out of 5.0) ... ECSE 6961 (Light-emitting diodes and solid-state lighting) feedback by students: “A good course ... this was a wonderful course ... it has given me a lot of understanding ... the course has inspired me to take up LED research ... useful ... straight forward ... very good advisor ... good course ...” (numerical scores: 4.3 out of 5.0) ... ECSE 6220 (Physical Foundations of Solid-State Devices) feedback by students: “Overall excellent course ... Professor Schubert is a good teacher ... he can explain every discipline very clearly and relate them to practical applications ... I like his teaching style very much ... overall, it was a nice course ... material explained in a clear organized manner ...” (numerical scores: 4.7 out of 5.0)

2011 – SPIE Photonics West short course feedback: “Very nice overview ... instructor was excellent! ... very good instructor ... I would recommend lengthening to 6 hours ... excellent presentation, materials and text ... thanks ... very clear and easy to follow ... to be recommended ... excellent presentation ... good compromise for a person with a busy schedule ...” (numerical score 4.45 out of 5.0); ... ECSE 2210 (Microelectronics Technology) “This was a great course ... I enjoyed Professor Schubert’s views ... I was successful ... this course was taught very well ... this subject I now find quite interesting and am no longer intimidated by it ... I liked the material of this course ... thank you ...” (numerical scores: 3.3 out of 5.0); Feedback on book *Light-Emitting Diodes*: “I am a graduate student from National Chiao Tung University, Taiwan ... your wonderful book *Light-Emitting Diodes*, both first- and second-edition, gave me a lot of information and help ... I would like to ask when can the third of the masterpiece be published? I wish I can get it as soon as possible and study more about the lighting devices; Feedback on Internet pages: I found your website and information [...] quite enlightening and provides a great start ... I simply wish to quickly express my thanks and gratitude.” Feedback on book *Physical Foundations of Solid-State Devices*: “Dear Prof. Schubert, I have read your book *Physical Foundations of Solid-State Devices* and I must say it is amazing the explanations are really good and I am most thankful that you have decided to put the book online thank you.” Itamar Jade Balla, The Israel Institute Of Technology. Feedback on book *Light-Emitting Diodes* by Trung Nguyen (San Jose, California): “It is a good book about Light Emitting Diodes (LEDs). It provides very good info and it is a good reference for engineers who work in the LED field”; ... ECSE 6220 (Physical Foundations of Solid-State Devices) feedback: “Amazing course ... great instructor ... very good course ... The text and lectures were very useful and informative ... I definitely learned a lot from taking this course ... I liked the course materials! ...” (numerical scores: 4.6 out of 5.0)

2012 – Feedback on Internet-based materials: “I’m Cheng Liu [Wuhan National Laboratory for Optoelectronics, China], currently a graduate student major in Physical Electronics ... I deeply admire your profound knowledge on this field and your unselfish sharing of it ...”; ... SPIE Photonics West short course feedback: “Dr. Schubert was very clear and very patient with people who had questions ... the materials were comprehensive ...”; Feedback on Internet-based materials: “Supremely-rich course contents posted on your website. Thank you very much for showing such awesome materials for the world to see ...” (Prof. Natee Tangtrakarn, Thailand) ... ECSE 6962 (Light-Emitting Diodes and Solid-State Lighting) feedback: “... very interesting course ... Professor Schubert did a great job explaining the material ... his textbook is very clear and understandable ... nice course ... I learned a lot of new things by taking it ...” (numerical scores: 4.7 out of 5.0)

2013 – **SPIE Photonics West short course** feedback (SC-052, Light-Emitting Diodes): “Great instructor with admirable combination of knowledge in academic and commercial knowledge ... I appreciated the depth of his knowledge and experience ... the length of the course was good ... Overall this was an excellent course ... Thank you ... course is very easy and I understand it easily ... Excellent course! ... Instructor was fantastic -- clear, explicit, took questions as we went and answered well ... One of the best SPIE courses I've taken (and I've taken lots)! ... Great course -- thanks! ... I was happy that the slides were updated with 2012 data”. **RPI course numerical scores (ECSE-6962, Light-Emitting Diodes and Solid-State Lighting)**: Numerical score of students’ evaluations: 4.67 out of 5.0; Verbatim comments: “The course is pretty good ... needs no improvement ... I can appreciate the more wide-angle approach from the course ... These areas are very important and previously I had no knowledge of

them ... It was a pleasure attending your class ...” *RPI course numerical scores (ECSE-6968, Physical Foundations of Solid-State Devices)*; Verbatim comments: “It has been an awesome experience of learning for me in this course ... Thank you for everything ... Thank you for the great semester ... Have a good break ... Thank you for the great semester ... Have a good break ... Professor, thank you for an engaging and interesting class this semester ... I enjoyed the subject of my paper and learned quite a bit particularly about GaN, which I had not had a chance to really do any research into before ... Very good and interactive class ... I liked the style of the class ... I thought the topics covered were very interesting ... I think I got much more out of the class this way than if we would have followed the manuscript chapter by chapter ...” Numerical score of students’ evaluations: 4.83 out of 5.0

2014 – SPIE Photonics West short course verbatim feedback (SC-052, Light-Emitting Diodes): “Very knowledgeable instructor ... the course was packed with information ... handouts are excellent ... Excellent presentation and contents ... the color rendering section which was interesting and fun ...” Numerical score of students’ evaluations: 4.36 out of 5.0; *RPI Course ECSE-2210 Microelectronics Technology*; Verbatim comments: “Instructor is clearly very knowledgeable about the topics ... Very clear and comprehensive ... This is the best class ever ... I’m quite enjoying this course ... I don’t really have any recommendations on things to change ... The homework and lectures being sent out at the beginning was very helpful ... Both the TA and the professor were able to explain things very well ... I think he is a good lecturer ... I think the homework each was very, very good at teaching me the material, and the exam was fairly graded and easy to understand ... I definitely like the professor and I would have him again ... A good class ... I enjoyed Prof. Schubert’s style of teaching ... I would still recommend Prof. Schubert as a professor ... Microelectronics is a good class ... Prof. Schubert keeps it interesting though ... he’s a great professor ... The two TAs are also great ...” Numerical score of students’ evaluations of instructor: 4.25 out of 5.0. *RPI Course ECSE-6220 Physical Foundations of Solid-State Devices*; Verbatim comments: “The book and lectures seem to be entirely in sync with one another ... it really enforces the material covered in the book ... the material is covered thoroughly and improves students’ understanding of quantum physics ... The class was interesting with excellent learning materials ... I loved how the course was so well organized ... The lectures were very well put together ...” Numerical score of students’ evaluations of instructor: 4.75 out of 5.0.

2015 – SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes, Verbatim comments: “I was very satisfied with this short course” Numerical score of students’ evaluations: 4.53 out of 5.0; *RPI Course ECSE-6960 Light-Emitting Diodes*; Verbatim comments: “the class has been excellent! ... I’ve learned a good amount about LEDs ... Also I’d like to thank you for a great semester and say that you’ve peaked my interest in the LED field! ... I would like to add that the course was an excellent experience for me and that I really enjoyed learning about LED technology! ... Thank you very much for teaching such a wonderful class ... It was a great learning course” Numerical score of students’ evaluations: 5.0 out of 5.0. *RPI Course ECSE-2100 Fields and Waves 1*; Verbatim comments: “This class is going perfectly and I love the way it’s run ... The material is great and understandable ... the pace is perfect ... I like the pacing of the course and the fact that we spend time really developing an understanding of the theory and concepts that we will be using ... I like the Professor ... The lectures are great ... I really enjoy this professor and he is very understanding of the students’ levels of learning and focused on that ... Professor Schubert is clear and easy to understand ... Overall a very good professor ... very knowledgeable and helpful ... I thought the professor was very knowledgeable and was an excellent instructor ...” Numerical score of students’ evaluations of instructor: 4.17 out of 5.0.

2016 – SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes, Verbatim comments: “This has been my favorite course (over 3 years) ... Well-structured presentation, and well given ... I was surprised by how much I didn’t know. I learned a lot ... Explained difficult concepts in a clear and simple manner ... Able to go “off script” to clarify during questions.” Numerical score of students’ evaluations: 4.56 out of 5.0; *RPI Course ECSE-2100 Fields and Waves 1*; Verbatim comments: “This is cool material ... This class was one of the most well put together I have ever taken in terms of lecture pace, lecture clarity, TA support, and quality of teaching and communication ... The lectures never felt too long or too short, the pace was good, I never felt lost or without an option to turn for help ... The homework was neither too long nor too short, and was well balanced with conceptual and quantitative questions ... Prof. Schubert’s lecture style was very clear, concise, and to the point, with many useful examples in real life scenarios which made the material more interesting ... Very well done ... Great class ... I liked the pace of the class ... it helps with understanding the material a lot ... The labs [...] were fun and very educational ... Overall, I learned a lot from this course ... The speed of the class is perfect ... I really got a chance to learn ... This professor is very good ... Also, [in] the lab section I was able to really break down what I learned in class ... Schubert has the neatest handwriting of any professor I’ve ever had in my 3 years here ... His diagrams are extremely neat and he is

easy to understand verbally too ... Lots of conceptual knowledge covered ... Overall [...] it was an enjoyable class ...” Numerical score of students’ evaluations: 5.0 out of 5.0. **RPI Course ECSE-2210 Microelectronics Technology**; Verbatim comments: “So far, this has been one of my favorite courses at RPI ... I’m a huge fan of Prof. Schubert’s ability to clearly describe concepts both conceptually and mathematically ... Class activities [...] were really helpful! ... Otherwise the class is great! ... Prof Schubert knows his stuff ... Best professor I have had ... This course was well taught ... Professor Schubert’s explanations were very clear and understandable ... he took time to address student questions with in-depth answers ... I feel as though I gained a lot from this course, especially with regards to explanations of why certain things in ECSE-2050 (Intro to Electronics) occur the way they do like where the diode property comes from and how material properties of electronic components give rise to the very real circuit characteristics we see in ECSE-2050 labs ... In this sense, Microelectronics Tech is a very good companion class to Intro to Electronics, and I highly recommend future students take them at the same time ... this was a quite good class ... Best MET instructor ... I was so actively engaged during the lectures that it was kind of scary ... The lecture notes and lectures were mostly great ... The material covered in it was succinct and interesting, yet still covered the knowledge needed to tackle engineering problems in semiconductors ...” Numerical score of students’ evaluations: 4.64 out of 5.0.

2017 – RPI Course ECSE-2100 Fields and Waves 1; Verbatim comments: “I thoroughly enjoy this class ... Schubert is awesome! ... Enjoyed the class ... He is a good teacher ... Most teachers talk really fast making it hard to follow ... Schubert talks slow and explains things really well ... Professor Schubert is an excellent professor, and has been one of my favorites at RPI so far ... He made a difficult topic approachable, interesting and understandable ... I hope I have him as a professor in the future ... Thank you ... I enjoyed this class, especially the labs ... Lectures were good too ... great class! ... The professor does a great job of engaging the students by asking questions and making students ask questions to make them think about the labs ... This course is overall excellent in that the professor does know the pace of class and gives feedback appropriately ...”; Numerical score of students’ evaluations: 4.63 out of 5.0. **SPIE Photonics West Short Course SC-052 titled Light Emitting Diodes**, Verbatim comments: “the course covered a wide variety of concepts ...” Numerical score of students’ evaluations: 4.03 out of 5.0.

2018 – RPI Course ECSE-2100 Fields and Waves 1; Verbatim comments: “Professor Schubert is great and very entertaining to listen to in the lab and in lecture ... Really appreciate how Prof. Schubert structures lectures ... Schubert is great! ... The professor is excellent at relaying concepts ... This course is very interesting and it goes at a good pace ... One of the better professors here at RPI ... He cares about his students and helps them to learn the most through lectures and labs ... Fantastic course that goes into great detail into not only knowing the material but also understanding the material ... [the course] has been clarified and allowed for a greater learning process.” Numerical score of students’ evaluations of instructor: 4.17 out of 5.0. **RPI Course ECSE-6220 Physical Foundations of Solid-State Devices**; Verbatim comments: “Perfect professor, no complaints.” Numerical score of students’ evaluations (median): 5.0 out of 5.0.

2019 – RPI Course ECSE-2100 Fields and Waves 1; Verbatim comments by students: “Schubert is excellent in relating information in a practical manner especially in the lab ... Overall, both the professor and TAs prioritize if students understand material over semantics in reports and homework, which is really helping me in the course, and feedback given is incredibly helpful in both ... Schubert is a mystery. He speaks very slowly and clearly, but you somehow learn everything at a very fast rate ... Class [...] being just the right amount focused and adequately paced ... Overall great class ... Labs were educational and we were allowed to have fun with it ... Otherwise great lectures, notes were available and understandable ... this was one of my favorite classes ... Very well run by Schubert ... lectures were informative and easy ... labs were fun ... The TA’s were allowed to have personalities and interact with the students ... 10/10 would take again ... Schubert was okay ... The best parts about the course for me were everything was online and I could copy the notes at my leisure with my busy schedule ... I also liked that exams were open book and we had a lot of opportunities for practice ... I have nothing but good things to say about both TAs and Professor Schubert – this has been my favorite class this semester ... Though challenging, I have found the course material very interesting and all teachers have been excellent ... Course was good ... I like Professor Schubert’s class notes online. They’re super well written and helpful.” Numerical score of students’ evaluations of instructor: 4.63 out of 5.0 (average) and 5.0 out of 5.0 (median).

2019 – RPI Course ECSE-6280 Light Emitting Diodes; Verbatim comments by students: “This was a great course ... I learned a lot during the semester ... Great class ... Really enjoyed Professor Schubert’s expertise on the subject ... Gives both in-depth technical knowledge as well as high level background to better understand the

driving factors of the LED industry ... Would highly recommend it to anyone in ECSE.” Numerical score of students’ evaluations: 4.83 out of 5.0 (average) 5.0 out of 5.0 (median).

2020 – RPI Course ECSE-2100 Fields and Waves 1; Verbatim comments by students: “I really enjoyed this class ... the cool labs with good help and good lectures made me really enjoy this class and help the information stick in my head better ... The labs provided a great use to show theory in practice and how certain concepts are applied to real-life applications ... The laboratory session was also a great time to ask questions and have in-depth talks about the material ... I would have already commended this professor for class organization and material availability prior to online courses (course material easily available, organized well, and easy to understand; interactive lectures; interactive labs better than most other ECSE courses), Prof. Schubert handled the change to online coursework best of all of my professors and maintained the quality of lecture almost perfectly ... The 'live' online classes were interactive and courteous by students and the professor, organized, and just as in-depth as before, even including miniature homemade demonstrations and experiments ... The course was taught very fundamentally which allowed me to think and learn more ... Thank you, Professor Schubert ... I really missed your live lectures and labs! ... Professor Schubert made the best of the situation of online learning ... Great class ... I learn a lot from this class ... I enjoy lab sessions and try never to miss any class ... Prof. Schubert is really good!” Numerical score of students’ evaluations: 4.75 out of 5.0 (average) 5.0 out of 5.0 (median).

2020 – RPI Course ECSE-2050 Introduction to Electronics; Verbatim comments by students: “I really enjoyed how easy it was to follow along with the lecture ... I really enjoyed the content of this course, and I feel that the applications of this content in the lab were extremely effective to help students understand the content ... the concepts in general were extremely interesting ... I liked how the lecture sessions for this class provided much more room for discussion and examples than nearly any other ECSE course I have taken at RPI so far ... Schubert was very aware of the students ability to fully comprehend the topic ... He was very patient with the students that needed extra explaining ... I learned a lot about the course material ... I liked the one-on-one attention we received in the in-person lab ... I enjoyed the in person laboratory sessions, they were a good place to get all my questions answered ... I really like the lecture notes and the detailed diagrams / graphs that help explain the concepts ... Professor Schubert does a great job of breaking down the material, he always tries to engage the students in every lecture ... Very clear notes, responded quickly, answered any confusing questions really well, and very nice and accommodating towards the current COVID situation everyone is going through ... He had very organized notes that helped especially with the difficulties of online learning ... I loved the explanation of diodes, it's never been so clear to me before! ... Examples were excellent ... The course was great! ... I learned a lot and this course stimulated my interest ... Very engaging ... stimulates participation ... Professor Schubert was a refreshing exception ... the professor was very knowledgeable in the subject area ... explanations were clear and easy to understand ... I really like the format of this class compared to my other classes ... I really enjoyed the format ... Very detailed lecture, very helpful with students, made very complex material easy to understand ... Prof is really understanding and cares about his students ... He is really willing to work with us which I found is really rare at RPI ... He is easily one of the best professors I have had ... He cares most about whether we are learning and understanding, rather than following his desired schedule perfectly ... Cannot say anything bad about Prof Schubert ... Class is great” Overall instructor rating: 4 out of 5. Overall course rating: 4 out of 5.

2021 – RPI Course ECSE-2050 Introduction to Electronics; Verbatim comments by students: “Class has been going smoothly ... Professor Schubert includes real world-examples of devices in his lectures, showing the importance of our course materials ... He is always very considerate of students, trying to adapt to what would help people most ... He engages students in lectures.” Overall instructor rating: 4.8 out of 5.0. Overall course rating: 4.6 out of 5.0.

2021 – RPI Course ECSE-2050 Introduction to Electronics; Verbatim comments by students: “Professor is always able to conceptually answer our questions, and run through circuit analysis with us if the results we're measuring don't match up ... I tried taking this class once before, and I failed it. This time around, I feel like I know everything about everything. I had never imagined just what a difference teaching style could make in my ability to learn information, but this class is so much more welcoming to me this time around. It was with a different professor the first time. I much prefer Professor Schubert and the way he conveys information so effortlessly. He also seems like he's passionate about teaching the information and his handwritten notes are astonishingly detailed ... Great professor! I appreciate Professor Schubert taking the time to clarify different topics and always checking in with the students. He seems to genuinely care about our education. He is strict about deadlines, more so than other professors at least, but I think he has earned that ... Professor Schubert is very friendly to his students ... He was very helpful and one of the few professors who actually stays and talks to students all

throughout the lab period. It was very helpful because often I would think that I fully understood a concept and then he would ask a question that would either stump me or reinforce information. Additionally he kept lectures short and to-the-point, which I appreciate.” Overall instructor rating: 4.3 out of 5.0. Overall course rating: 4.3 out of 5.0.

2022 – RPI Course ECSE-2050 Introduction to Electronics; Verbatim comments by students: “Great professor! ... Handwriting is amazing ... His notes are flawless and easy to understand ... This course covers much more than most other EE courses I've taken, and yet I feel as though this has been the easiest EE course due to his teaching abilities ... Professor Schubert is a very knowledgeable professor ... It's clear that he wants his students to learn ...” Overall instructor rating: 4.3 out of 5.0. Overall course rating: 4.4 out of 5.0.

2022 – RPI Course ECSE-2210 Microelectronics Technology; Verbatim comments by students: “I think Schubert does a great job of teaching ... He makes the pn junctions as interesting as he can ... I also love the chalk-board! So great, every professor should be forced to use it, because you can follow the work so smoothly (not like powerpoints) ... I would not change the class ... I also like how Prof. Schubert asks for feedback from everyone after class ... Course was at a great pace and the level of difficulty ... Professor Fred Schubert is one of my most favorite professors at RPI ... I am sad to see in the course schedule for Spring 2023 that he is not teaching any 4000 level ECSE courses ... I think that the department and students are missing out by not having someone as knowledgeable as him teaching more conceptually hard topics because Professor Schubert does that exceptionally ... Best ever lecture experience, clear structure of lecture notes, comprehensive homework that helps to improve students' understandings, and always eager to solve students' questions ... Thanks for another great course Professor!”

Post-doctoral & visiting personnel for which I served as Major Research Advisor

Dr. Li-Wei Tu	Post-Doctoral Fellow	1988–1990
Dr. Neil Hunt	Post-Doctoral Fellow	1991–1993
Dr. Matthias Passlack	Post-Doctoral Fellow	1993–1995
Dr. Wolf Grieshaber	Post-Doctoral Fellow	1995–1997
Dr. Thomas Gessmann	Post-Doctoral Fellow	2000–2002
Dr. Jong Kyu Kim	Post-Doctoral Fellow	2003–2005
Dr. Min Ho Kim, SEMCo	Visiting Engineer	2007–2008
Prof. Ji-Myon Lee, Sunchon University	Visiting Professor	2007–2008
Dr. Jaehee Cho	Post-Doctoral Fellow	2008–2009
Dr. Yongjo Park, Samsung LED	Visiting Vice President	2010–2012
Dr. Yangang Andrew Xi	Visiting Scientist	2013–2014
Dr. Guan-Bo Lin	Post-Doctoral Fellow	2014–2015

Graduate students for which I served as Major Research Advisor

Dr. Dean A. Stocker	Ph.D. Dissertation	Ph. D. completed in 1999
Xiaoyun (Jane) Guo	Master Thesis	M.S.E.E. completed in 1999
John W. Graff	Master Thesis	M.S.E.E. completed in 1999
Dr. Ian D. Goepfert	Ph.D. Dissertation	Ph. D. completed in 2000
Yun-Li Li	Master Thesis	M.S.E.E. completed in 2000
Dr. Xiaoyun (Jane) Guo	Ph.D. Dissertation	Ph. D. completed in 2001
Dr. John W. Graff	Ph.D. Dissertation	Ph. D. completed in 2002
Dr. Erik L. Waldron	Ph.D. Dissertation	Ph. D. completed in 2002
Jay M. Shah	Master Thesis	M.S.E.E. completed in 2002
Dr. Yun-Li Li	Ph.D. Dissertation	Ph. D. completed in 2003
Jingqun (“JQ”) Xi	Master Thesis	M.S. completed in 2003
Yangang Andrew Xi	Master Thesis	M.S. completed in 2003
Ronald Jackson	Master Thesis	M.S. completed in 2004
Sameer Chhajed	Master Thesis	M.S. completed in 2004
Hong Luo	Master Thesis	M.S. completed in 2005
Xiaolu Li	Master Thesis	M.S. completed in 2005
Kaixuan Chen	Master Thesis	M.S. completed in 2005

Curriculum Vitae: E. Fred Schubert

Dr. Jay M. Shah	Ph.D. Dissertation	Ph. D. completed in 2006
Frank Mont	Master Thesis	M.S.E.E. completed in 2006
Dr. Hong Luo	Ph.D. Dissertation	Ph. D. completed in 2006
Dr. Jingqun ("JQ") Xi	Ph.D. Dissertation	Ph. D. completed in 2006
Dr. Yangang Andrew Xi	Ph.D. Dissertation	Ph. D. completed in 2006
Won Seok Lee	Master Thesis	M.S. completed in 2007
Qi Dai	Master Thesis	M.S. completed in 2007
Di Zhu	Master Thesis	M.S. completed in 2007
Jiuru Xu	Master Thesis	M.S. completed in 2007
Ahmed Noemaun	Master Thesis	M.S. completed in 2007
Roya Mirhosseini	Master Thesis	M.S. completed in 2008
David Poxson	Master Thesis	M.S. completed in 2008
Qifeng Shan	Master Thesis	M.S. completed in 2009
Ming Ma	Master Thesis	M.S. completed in 2010
Xing Yan	Master Thesis	M.S. completed in 2010
Dr. Roya Mirhosseini	Ph.D. Dissertation	Ph. D. completed in 2010
Dr. Sameer Chhajed	Ph.D. Dissertation	Ph. D. completed in 2010
Dr. Jiuru Xu	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Frank Mont	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Wonseok Lee	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Di Zhu	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Qi Dai	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Ahmed Noemaun	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. David Poxson	Ph.D. Dissertation	Ph. D. completed in 2011
Dr. Qifeng Shan	Ph.D. Dissertation	Ph. D. completed in 2012
Dr. Ann Mao	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. Xing Yan	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. Ming Ma	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. David Meygaard	Ph.D. Dissertation	Ph. D. completed in 2013
Dr. Guan-Bo Lin	Ph.D. Dissertation	Ph. D. completed in 2013

Technical Expert Witness Service

- 1997** ***Action:*** Hewlett-Packard Company versus CEO of United Epitaxy Company (Taiwan)
Nature: Trade secret misappropriation
Venue: U.S. District Court.
Law firm: Morrison & Foerster LLP, Washington DC.
Role: I served as technical expert witness on behalf of United Epitaxy (Defendant). I wrote one or more expert reports.
- 1998** ***Action:*** Hewlett-Packard Company versus United Epitaxy Company (Taiwan)
Nature: Patent infringement.
Venue: U.S. District Court for the Northern District of California.
Law firm: Quinn Emanuel Urquhart Oliver and Hedges LLP
Role: I served as technical expert witness on behalf of United Epitaxy (Defendant). I wrote one or more expert reports.
- 2006** ***Action:*** Kerr Company versus 3M and Dentsply International Company.
Nature: Patent infringement.
Venue: U.S. District Court for the Western District of Wisconsin.
Law Firm: Woodcock Washburn LLP, Philadelphia, Pennsylvania.
Role: I served as technical expert witness on behalf of Dentsply (Defendant). I wrote one or more expert reports.
- 2006** ***Action:*** Nichia Corporation (Japan) versus Seoul Semiconductor Company (Korea).
Nature: Design patent infringement.
Venue: U.S. District Court for Northern District of California, San Francisco Division.
Law firm: Foley & Lardner LLP Washington DC.
Role: I served as technical expert witness on behalf of Nichia (Plaintiff). I wrote one or more expert reports; I was deposed.
- 2008** ***Action:*** Seoul Semiconductor (SSC) Company LTD (Korea) versus Nichia Corporation (Japan).
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Beaumont Division.
Law firm: Morrison & Foerster LLP, Palo Alto, California.
Role: I served as technical expert witness on behalf of Nichia (Defendant). I wrote one or more expert reports; I testified in District Court during the claim construction / Markman hearing.
- 2008** ***Action:*** Professor Gertrude Rothschild versus Toshiba Company (Japan).
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: DLA Piper LLP, San Francisco California.
Role: I served as technical expert witness on behalf of Toshiba (Defendant). I wrote one or more expert reports; I was deposed.
- 2008** ***Action:*** Honeywell Company versus Cree Company and Lumileds Company.
Nature: Patent infringement and Reexamination of patent.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division. Reexamination before the USPTO's Patent Trial and Appeal Board.

- Law firms:** Paul Hastings LLP, Washington DC and Ingrassia, Fisher & Lorenz PC, Washington DC.
Role: I served as technical expert witness on behalf of Honeywell (Plaintiff). I wrote one or more expert reports. I testified at the USPTO during a re-examination hearing.
- 2010** **Action:** Landmark Screens Company versus MLB Company and Kohler.
Nature: Mishandling of a patent application.
Venue: U.S. District Court for the Northern District of California, San Jose Division.
Law firm: Kecker & Van Nest LLP, San Francisco, California.
Role: I served as technical expert witness on behalf of MLB and Kohler (Defendant). Negligence in conjunction with a patent application; I wrote one or more expert reports.
- 2011** **Action:** Koninklijke Philips Electronics N.V. versus Seoul Semiconductor (SSC) Company LTD.
Nature: Patent infringement.
Venue: U.S. District Court for the Central District of California Southern Division
Law firm: Latham & Watkins LLP, Washington DC.
Role: I served as technical expert witness on behalf of SSC (Defendant). I wrote one or more expert reports.
- 2011** **Action:** Jeou-Nan Tseng versus Home Depot USA Inc. and Guangde LEDup Enterprise Inc.
Nature: Patent infringement.
Venue: U.S. District Court for the Western District of Washington at Seattle.
Law firm: DLA Piper, Philadelphia, Pennsylvania.
Role: I served as technical expert witness on behalf of Home Depot (Defendant). I wrote one or more expert reports.
- 2011** **Action:** Lightpanels Ltd. Company versus Fuzhou F&V Photographic Company.
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Locke Lord LLP, New York, New York.
Role: I served as technical expert witness on behalf of Fuzhou F&V and Nanguang Photographic (Defendant). I wrote one or more expert reports; I was deposed.
- 2012** **Action:** Osram Company versus LG Company.
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of LG (Defendant). I wrote one or more expert reports; I was deposed; I testified at the ITC Hearing.
- 2012** **Action:** Osram Company versus LG Company and Samsung Company.
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Covington & Burling LLP, Washington DC.
Role: I served as technical expert witness on behalf of LG and Samsung (Defendant). I wrote one or more expert reports; I was deposed; I testified at the ITC Hearing.
- 2013** **Action:** Chao Tai Electron Co. LTD. versus LEDup Enterprise Inc. and others.
Nature: Patent infringement.

- Venue:** U.S. District Court for the Central District of California.
Law firm: Hunton & Williams LLP, Washington DC.
Role: I served as technical expert witness on behalf of LEDup Enterprise Inc. and others (Defendants). I wrote one or more expert reports.
- 2013** **Action:** Nichia Corporation versus Everlight Company and Emcore Company.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Foley & Lardner LLP, Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Petitioner). I wrote one or more expert reports; I was deposed.
- 2014** **Action:** Everlight Electronics Co. LTD. versus Nichia Corporation.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Michigan, Southern Division.
Law firm: Foley & Lardner LLP, Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Defendant). I wrote one or more expert reports; I was deposed; I testified at Phase 1 of trial (jury trial) and I testified at Phase 2 of trial (bench trial).
- 2014** **Action:** LEDup Company versus Nicolas Holiday Company.
Nature: Patent infringement.
Venue: U.S. District Court for the Central District of California.
Law firm: Pendleton, Wilson, Hennessey, and Crow PC, Denver, Colorado.
Role: I served as technical expert witness on behalf of LEDup (Plaintiff). I wrote one or more expert reports.
- 2014** **Action:** Nichia Corporation versus Everlight Electronics Co. LTD.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division.
Case number: 02:13-cv-702-JRG (E.D. Texas).
Law firm: Rothwell, Figg, Ernst & Manbeck PC, Washington DC.
Role: I served as technical expert witness on behalf of Nichia (Plaintiff). I wrote one or more expert reports; I was deposed; I testified at trial (bench trial).
- 2015** **Action:** Cree Company versus Unity Opto, Unity Microelectronics, and Feit Electric Company
Nature: Patent infringement.
Venue: U.S. International Trade Commission (ITC), Washington DC.
Law firm: Alston & Bird LLP, Silicon Valley, East Palo Alto, California.
Role: I served as expert witness on behalf of Unity Opto Technology *et al.* (Defendants). I wrote one or more expert reports; I was deposed; I testified at trial (ITC Hearing).
- 2015** **Action:** Honeywell International Inc. versus Cree Inc.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Arnold & Porter LLP, San Francisco, California.
Role: I served as expert witness on behalf of Honeywell International Inc. (Plaintiff). I wrote one or more expert reports.

- 2015** *Action:* Honeywell International Inc. versus Cree Inc.
Nature: Patent infringement.
Venue: U.S. District Court for the District of New Jersey.
Law firm: Arnold & Porter LLP, San Francisco, California.
Role: I served as expert witness on behalf of Honeywell International Inc. (Plaintiff).
- 2015** *Action:* Cree Inc. versus Kingbright Electronic Co. LTD and SunLED Corporation.
Nature: Patent infringement.
Venue: U.S. District Court for the Western District of Wisconsin.
Law firm: Hansen Reynolds Dickinson Crueger LLC, Milwaukee, Wisconsin.
Role: I served as technical expert witness on behalf of Kingbright and SunLED (Defendants). I wrote one or more expert reports; I was deposed.
- 2016** *Action:* Acuity Brands Lighting Inc. versus Lynk Labs Inc.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Haynes Boone LLP, Chicago, Illinois.
Role: I served as technical expert witness on behalf of Lynk Labs (Plaintiff). I wrote one or more expert reports.
- 2016** *Action:* Godo Kaisha IP Bridge 1 Company versus Broadcom Company and others.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division.
Law firm: Ropes and Gray LLP, New York City, New York.
Role: I served as technical expert witness on behalf of IP Bridge 1 (Plaintiff). I wrote one or more expert reports; I was deposed.
- 2016** *Action:* TSMC Company versus Godo Kaisha IP Bridge 1 Company.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Law firm: Greenblum & Bernstein, P.L.C., Reston, Virginia.
Role: I served as technical expert witness on behalf of IP Bridge (Patent Owner). I wrote one or more expert reports; I was deposed.
- 2017** *Action:* Harvard University versus Micron Technology Company.
Nature: Patent infringement.
Venue: U.S. District Court for MA, Boston; U.S. District Court for Delaware, Wilmington.
Law firm: Weil Gotshal & Manges LLP, Redwood Shores, California.
Role: I served as technical expert witness on behalf of Micron Technology Company (Defendant). I wrote one or more expert reports; I was deposed.
- 2017** *Action:* Seoul Viosys Company versus P3 Company.
Nature: Patent infringement.
Venue: U.S. District Court, Southern District of New York, New York City.
Law firm: Holland & Knight LLP, New York City, New York.
Role: I served as technical expert witness on behalf of Seoul Viosys (Plaintiff). I wrote one or more expert reports.

- 2017** *Action:* Nitride Semiconductor Company versus Rayvio Company.
Nature: Patent infringement.
Venue: US District Court for the Northern District of California.
Law firm: Dentons LLP, Palo Alto, California.
Role: I served as technical expert witness on behalf of Rayvio (Defendant).
- 2018** *Action:* CRX Tech LLC versus Samsung Electronics Co. LTD.
Nature: Patent infringement.
Venue: U.S. District Court for the Eastern District of Texas, Marshall Division.
Law firm: Arnold & Porter LLP, Los Angeles, California.
Role: I served as technical expert witness on behalf of Samsung (Defendant).
- 2018** *Action:* Macom Technology Solutions Holdings Inc. versus Infineon Technologies AG.
Nature: Patent infringement.
Venue: U.S. District Court Central District of California Western Division, Los Angeles.
Law firm: Perkins Coie LLP, Denver, Colorado.
Role: I served as technical expert witness on behalf of Macom (Plaintiff). I wrote one or more expert reports; I was deposed.
- 2018** *Action:* Vizio Inc. versus Nichia Corporation.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Case number: Case No. IPR-2017-01608 and IPR-2017-01623 (PTAB).
Law firm: Rothwell, Figg, Ernst & Manbeck, P.C., Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Patent Owner). I wrote one or more expert declarations.
- 2018** *Action:* Lowe's Companies Inc. versus Nichia Corporation.
Nature: Inter Partes Review (IPR).
Venue: USPTO Patent Trial and Appeal Board.
Case number: Case No. IPR2017-02014 (PTAB).
Law firm: Rothwell, Figg, Ernst & Manbeck, P.C., Washington DC.
Role: I served as technical expert witness on behalf of Nichia Corporation (Patent Owner). I wrote one or more expert declarations.
- 2018** *Action:* Ultravision Technologies LLC versus Prismaflex USA Inc.
Nature: Patent infringement.
Venue: US International Trade Commission (ITC), Washington DC.
Case number: Investigation No. 337-TA-1114 (ITC)
Law firm: Womble Bond Dickinson LLP, Winston-Salem, NC
Role: I served as technical expert witness on behalf of Prismaflex USA (Defendant). I wrote one or more expert reports. I was deposed.
- 2019** *Action:* Carl Zeiss AG versus Nikon USA Inc.
Nature: Patent infringement.
Venue: US International Trade Commission (ITC), Washington DC.
Case number: Investigation No. 337-TA-1129 (US ITC)
Law firm: Morrison & Foerster LLP, Los Angeles CA.

- Role:** I served as technical expert witness on behalf of Nikon USA (Defendant). I wrote one or more expert reports. I was deposed.
- 2019** **Action:** ASM IP Holding B.V. versus Hitachi Kokusai Electric Inc.
Nature: Arbitration related to IP licensing dispute.
Venue: ICDR (International Center for Dispute Resolution), Palo Alto CA.
Case number: Case No. ICDR 01-17-0005-1963 (Palo Alto CA)
Law firm: Quinn Emanuel Urquhart & Sullivan LLP, San Francisco CA.
Role: I served as technical expert witness on behalf of ASM IP Holding B.V. (Complainant). I authored multiple witness statements. I testified at the Arbitration Hearing.
- 2019** **Action:** Power Integrations Inc. versus C. W. Park.
Nature: Breach of employment contract.
Venue: US District Court, Northern District of California, San Jose Division.
Case number: 5:16-cv-02366-BLF (Northern District of California)
Law firm: Miclean Gleason LLP, San Mateo CA.
Role: I served as technical expert witness on behalf of Power Integrations Inc. (Complainant). I performed analyses relating to switched-mode power supplies (SMPS) including flyback transformers. The matter ended in settlement.
- 2019** **Action:** Omni MedSci Inc. versus Apple Inc.
Nature: Patent infringement.
Venue: US District Court, Eastern District of Texas, Marshall Division.
Case number: Civil Action No. 2:18-cv-134-RWS (E.D. Texas)
Law firm: Sidley Austin LLP, Washington DC.
Role: I served as technical expert witness on behalf of Apple Inc. (Defendant). I performed a non-infringement analysis relating to the heart rate monitor of the Apple Watch, authored an expert report, and testified at a deposition.
- 2019** **Action:** Fluxwerx Illumination Inc., versus OKT Lighting USA LLC
Nature: Design patent infringement.
Venue: US District Court, Southern District of Texas, Houston Division.
Case number: Civil Action No. 4:19-CV-01113 (S.D. Texas)
Law firm: Burns & Levinson LLP, Boston MA.
Role: I served as technical expert witness on behalf of Fluxwerx Illumination, Inc. (Plaintiff). I performed an infringement analysis.
- 2020** **Action:** Lighting Science Group Corporation versus Nichia Corporation and others
Nature: Patent infringement.
Venue: US ITC, OUII (Office for Unfair Import Investigations), Washington DC
Case number: Investigation No. 337-TA-1168
Law firm: Shearman & Sterling LLP, New York, NY.
Role: I served as technical expert witness on behalf of Nichia Corporation. I performed a non-infringement analysis, authored an expert report, was deposed, and testified at the ITC hearing as key technical witness on behalf of Nichia and Respondents (6 hours live testimony).
- 2020** **Action:** Regents of the University of California versus Amazon, Walmart, Ikea, Target, and others
Nature: Patent infringement.
Venue: US ITC, OUII (Office for Unfair Import Investigations), Washington DC

Case number: Investigation No. 337-TA-1172

Law firm: Nixon Peabody LLP, Los Angeles CA.

Role: I served as technical expert witness on behalf of the Regents of the University of California. I performed an infringement analysis, authored an expert report, and was deposed.

2020 Action: Samsung Electronics Company versus Acorn Technologies Company.

Nature: USPTO Inter Partes Review.

Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.

Case numbers: IPR-2020-01183 ('261), IPR-2020-01182 ('423), IPR-2020-01204 ('336), IPR-2020-01264 ('336), IPR-2020-01205 ('167), IPR-2020-01241 ('167), IPR-2020-01206 ('691), IPR-2020-01279 ('691), IPR-2020-01207 ('395), and IPR-2020-01282 ('395)

Law firm: Desmarais LLP, New York NY.

Role: I served as technical expert witness on behalf of Samsung Electronics Company. I authored several expert declarations and was deposed multiple times.

2020 Action: Satco Company versus The Regents of the University of California.

Nature: USPTO Inter Partes Review.

Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.

Case number: IPR-2020-00579, IPR-2020-00695, IPR-2020-00780, and IPR-2020-00813.

Law firm: Nixon Peabody LLP, Los Angeles CA.

Role: I served as technical expert witness on behalf of The Regents of the University of California. I authored several expert declarations and was deposed.

2020 Action: Godo Kaisha IP Bridge 1 Company versus Micron Technology Company.

Nature: Patent infringement.

Venue: US District Court for the Western District of Texas, Waco Division.

Case number: C.A. No. 6:20-cv-178-ADA.

Law firm: Orrick Herrington & Sutcliffe LLP, Menlo Park CA.

Role: I served as technical expert witness on behalf of Micron Technology Company. I authored multiple expert reports and was deposed.

2020 Action: Nichia Company versus Healtel Company and Lighting Science Group Company.

Nature: Patent infringement.

Venue: US District Court for the Middle District of Florida, Orlando Division.

Case number: 6:19-cv-1332-RBD-EJK and 6:19-cv-1333-RBD-EJK.

Law firm: Rothwell, Figg, Ernst & Manbeck, PC, Washington DC.

Role: I served as technical expert witness on behalf of Nichia Company. I authored one or more expert reports.

2020 Action: Semiconductor Energy Laboratory (SEL) Co., Ltd. versus BOE Technology Group Co., Ltd.

Nature: Patent infringement.

Venue: US District Court for the Northern District of California.

Case number: 3:20-cv-04297-EMC, N.D. Cal.

Law firm: Fish and Richardson, P.C., Redwood City CA.

Role: I served as technical expert witness on behalf of SEL.

2021 Action: The University of California versus General Electric, Ikea, Home Depot and others

Nature: Patent infringement.

Venue: US ITC, OUII (Office for Unfair Import Investigations), Washington DC

- Case number:** Investigation No. 337-TA-1220
Law firm: Nixon Peabody LLP, Los Angeles CA.
Role: I served as technical expert witness on behalf of the University of California. I performed multiple analyses, authored several expert reports, was deposed multiple times, and testified at trial.
- 2021 Action:** Tianma Microelectronics Co., Ltd. versus Japan Display Inc. (JDI)
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA
Case numbers: IPR-2021-01029, IPR-2021-01057 and IPR-2021-01058
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of Tianma. I performed multiple analyses and authored several declarations.
- 2021 Action:** Japan Display Inc. (JDI) versus Tianma Microelectronics Co., Ltd.
Nature: Patent infringement.
Venue: US District Court for the Eastern District of Texas, Marshall Division.
Case numbers: Civil Action No. 2:20-cv-00283-JRG; 2:20-cv-00284-JRG; and 2:20-cv-00285-JRG
Law firm: Finnegan, Henderson, Farabow, Garrett & Dunner, LLP, Washington DC.
Role: I served as technical expert witness on behalf of Tianma. I performed multiple analyses, authored several expert reports, and was deposed multiple times.
- 2022 Action:** Satco Products Inc. versus The Regents of the University of California.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR-2021-00662.
Law firm: Nixon Peabody LLP, Los Angeles CA.
Role: I served as technical expert witness on behalf of The Regents of the University of California, authored one expert declaration, and was deposed.
- 2022 Action:** Samsung Electronics Co. Ltd. versus Bishop Display Tech LLC.
Nature: USPTO Inter Partes Review.
Venue: USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case numbers: IPR-2022-00500 and IPR-2022-00502.
Law firm: Baker Botts LLP, New York City NY.
Role: I served as technical expert witness on behalf of Samsung Electronics and have authored two expert declarations.
- 2022 Action:** Semiconductor Energy Laboratory (SEL) Co. Ltd. versus TCL China Star Optoelectronics Technology Co., Ltd.
Nature: Patent infringement.
Venue: US District Court for the Central District of California, Southern Division.
Case number: 8:21-cv-00554-JAK-ADS.
Law firm: Fish and Richardson, P.C., Redwood City CA.
Role: I served as technical expert witness on behalf of SEL, authored multiple expert reports, and was deposed.
- 2022 Action:** Nvidia Corporation versus Ocean Semiconductors LLC
Nature: USPTO Inter Partes Review.

- Venue:** USPTO, Patent Trial and Appeal Board, Alexandria VA.
Case number: IPR2022-01288.
Law firm: Sheppard Mullin LLP, Menlo Park CA.
Role: I served as technical expert witness on behalf of Nvidia and authored one expert report.
- 2022** **Action:** Nicor, Inc. versus SourceBlue LLC and Infinilux Corporation
Nature: Patent infringement.
Venue: US District Court for the Central District of California.
Case number: 2:21-cv-05876-AB(PDx) (C.D. Cal.).
Law firm: Loza & Loza IP LLP, Upland CA.
Role: I served as technical expert witness on behalf of Nicor, Inc., and authored one expert report.

United States Patents

1. A. Fischer, Y. Horikoshi, K. Ploog, and E. F. Schubert "Semiconductor devices with at least one monoatomic layer of doping atoms" European Patent No. 0183 146 A2; US Patent No. 4,882,609; issued on November 15 (1985)
2. J. E. Cunningham, E. F. Schubert, and W. T. Tsang "Delta doped ohmic metal to semiconductor contacts" US Patent No. 4,772,934; issued on September 20 (1988)
3. J. E. Cunningham, E. F. Schubert, and W. T. Tsang "Field-effect transistor having a delta-doped ohmic contact" US Patent No. 4,780,748; issued on October 25 (1988)
4. J. E. Cunningham, E. F. Schubert, and W. T. Tsang "Method for fabricating a field-effect transistor with a self-aligned gate" US Patent No. 4,784,967; issued on November 15 (1988)
5. E. Fred Schubert "Optical communications modulator device" US Patent No. 4,929,064; filed on July 21 (1988) issued on May 29 (1990)
6. J. E. Cunningham, A. M. Glass, and E. F. Schubert "Devices having asymmetric delta-doping" US Patent No. 4,974,044; issued on November 27 (1990)
7. J. E. Cunningham, A. M. Glass, and E. F. Schubert "Devices having asymmetric delta-doping" US Patent No. 5,031,012; issued on July 9 (1991)
8. J. E. Cunningham, T. D. Harris, E. F. Schubert, and J. P. van der Ziel "Optical system including wavelength tunable semiconductor laser" US Patent No. 4,980,892; issued on December 25 (1990)
9. R. F. Kopf, J. M. Kuo, H. S. Luftman, and E. F. Schubert "Doping procedures for semiconductor devices" US Patent No. 5,024,967; issued on June 18 (1991)
10. D. G. Deppe, R. D. Dupuis, and E. F. Schubert "Vertical cavity semiconductor lasers" US Patent No. 5,018,157; issued on May 21 (1991)
11. D. G. Deppe, L. C. Feldman, R. F. Kopf, E. F. Schubert, L.-W. Tu, and G. J. Zydzik "Vertical cavity surface emitting lasers with electrically conducting mirrors" US Patent No. 5,068,868; issued on November 26 (1991)
12. D. G. Deppe, E. F. Schubert, L.-W. Tu, and G. D. Zydzik "Optical devices with electron-beam evaporated multilayer mirror" US Patent No. 5,206,871; issued on April 27 (1993)
13. R. F. Kopf, E. F. Schubert, H. O'Brian, L.-W. Tu, Y. H. Wang, and G. J. Zydzik "Vertical cavity surface emitting lasers with transparent electrodes" US Patent No. 5,115,441; issued on May 19 (1992)
14. E. F. Schubert, L.-W. Tu, and G. J. Zydzik "Elimination of heterojunction band discontinuities" US Patent No. 5,170,407; issued on December 8 (1992)
15. S. W. Downey, A. B. Emerson, R. F. Kopf, and E. F. Schubert "Devices having repetitive layers" US Patent No. 5,226,055; issued on July 6 (1993)

16. A. Y. Cho, E. F. Schubert, L.-W. Tu, and G. J. Zydzik "Resonant cavity light emitting diode" US Patent No. 5,226,053; issued on July 6 (1993)
17. L. C. Feldman, N. E. J. Hunt, D. C. Jacobson, J. M. Poate, E. F. Schubert, A. M. Vredenberg, Y. H. Wong, and G. J. Zydzik "Erbium-doped optical devices" US Patent No. 5,249,195; issued on September 28 (1993)
18. R. F. Kopf and E. F. Schubert "PN junction devices with group IV element-doped group III-V compound semiconductors" US Patent No. 5,268,582; issued on December 7 (1993)
19. N. E. J. Hunt and E. F. Schubert "Single mirror light-emitting diodes with enhanced intensity" US Patent No. 5,362,977; issued on November 8 (1994)
20. N. E. J. Hunt, E. F. Schubert, and G. J. Zydzik "Photodetector with a resonant cavity" US Patent No. 5,315,128; issued on May 24 (1994)
21. A. M. Glass, N. E. J. Hunt, J. M. Poate, E. F. Schubert, and G. J. Zydzik "Absorption resonant rare-earth-doped microcavities" US Patent No. 5,363,398; issued on November 8 (1994)
22. N. E. J. Hunt, M. Passlack, E. F. Schubert, and G. J. Zydzik "Electron beam deposition of gallium oxide thin films using a single high purity crystal source" US Patent No. 5,451,548; issued on September 19 (1995)
23. N. K. Dutta, R. J. Fischer, N. E. J. Hunt, M. Passlack, E. F. Schubert, and G. J. Zydzik "Gallium oxide coatings for optoelectronic devices using electron beam evaporation of a high purity single crystal $Gd_3Ga_5O_{12}$ source" US Patent No. 5,550,089; issued on August 27 (1996)
24. U. K. Chakrabarti, J. de Jong, E. F. Schubert, J. Wynn, and G. J. Zydzik "Mechanical fixture and procedure for in-vacuum coating of semiconductor laser facets" US Patent No. 5,719,077; issued on February 17 (1998)
25. E. F. Schubert "Enhanced p-type doping of wide-gap semiconductors" US Patent No. 5,932,899; issued on August 3 (1999)
26. J. D. Joannopoulos, S. Fan, P. R. Villeneuve, and E. F. Schubert "Light emitting device utilizing a periodic dielectric structure" US Patent No. 5,955,749; issued on September 21 (1999)
27. E. F. Schubert and D. A. Stocker "Crystallographic wet chemical etching on GaN" US Patent No. 6,294,475; issued on September 25 (2001)
28. E. F. Schubert "Light-emitting diode with omni-directional reflector" US Patent No. 6,784,462; issued on August 31 (2004)
29. Jaehee Cho, Hong Luo, Jong Kyu Kim, Yong Jo Park, Cheolsoo Sone, and E. Fred Schubert "Light emitting device having protection element and method of manufacturing the light emitting device" US Patent No. 7,411,221 B2; issued on August 12 (2008)
30. Jaehee Cho, Frank Wilhelm Mont, Cheolsoo Sone, Jong-kyu Kim, June-o Song, E. Fred Schubert "Optical thin film, semiconductor light emitting device having the same and methods of fabricating the same" US Patent No. 7,483,212; issued on January 27 (2009)

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Patent Licensing: Several patents listed above have been licensed to companies, including the Luminus Devices Company, Samsung Company, Epistar Company, Cree Company, Osram Company, and Lumileds Company.

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