

(19) Japanese Patent Office (JP) (12) **Unexamined Patent Gazette (A)**(11) Unexamined Patent Application (Kokai) No.:
Unexamined Patent Application Publication No. 2010-171337
(P2010-171337A)

(43) Publication Date: August 5, 2010

(51) Int. Cl.		F1		Theme Code (Reference)
H01L 29/78	(2006.01)	H01L 29/78	301B	4M104
H01L 21/20	(2006.01)	H01L 29/78	301N	5F110
H01L 29/417	(2006.01)	H01L 29/78	301S	5F140
H01L 21/336	(2006.01)	H01L 29/78	301X	5F152
H01L 29/786	(2006.01)	H01L 21/20		

Request for Examination: Not Requested Number of Claims: 10 OL (Total of 27 pages)

Continued on the past page

(21) Application No.: Unexamined Patent Application
Publication No. 2009-14541 (P2009-14541)

(22) Filing Date: January 26, 2009

[Items to be stated regarding the results of government-commissioned study] (Declaration by Applicant) Patent application subject to 2008 New Energy and Industrial Technology Development Organization "Next Generation Semiconductor Material and Process Infrastructure (MIRAI) Project/Next Generation Semiconductor Materials and Process Infrastructure (MIRAI) Project (General Account)/ New Structure Limit CMOS Transistor "Related Technology Development" consigned study, Article 19 of the Industrial Technology Enhancement Act

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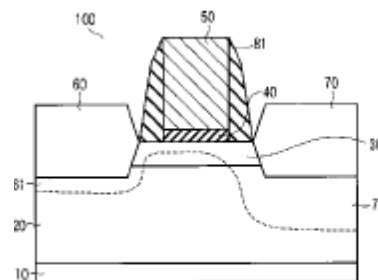
(54) [Title of the Invention] Field effect transistor

(57)[Problem] To be able to reduce leakage current when a strained channel is used so as to suppress the occurrence of defects and improve yield.

[Solution Means] A field effect transistor, equipped with an underlying layer 20 made of an alloy semiconductor having a lattice constant different from that of a semiconductor substrate 10 and provided on the substrate 10; a channel semiconductor layer 30, provided on the underlying layer 20, which has a lattice constant different from that of the underlying layer 20, and to which tensile stress is applied in one direction of the channel length direction and the channel width direction and compressive stress is applied to the other; source/drain regions 60 and 70 provided on the underlying layer 20 so as to sandwich the channel semiconductor layer 30; and a gate electrode 50 provided on the channel semiconductor layer 30 with a gate insulating film 40 interposed therebetween; wherein in the underlying layer 20, depletion layers 61 and 71 formed under the source/drain regions 60 and 70 are formed thicker than the underlying layer 20 and thinner than the thermal equilibrium critical thickness.

[Selected Drawing] FIG. 1

FIG. 1



[Claims]

[Claim 1]

A field effect transistor, equipped with
a stressed channel region,
a gate electrode provided on the channel region via a gate insulating film,
source/drain regions provided on both sides of the channel region, and
an underlying layer made of an alloy semiconductor provided at least under the source/drain regions;
wherein the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[Claim 2]

A field effect transistor, equipped with
an underlying layer provided on a semiconductor substrate and made of an alloy semiconductor containing the same elements as the substrate and having a lattice constant different from that of the substrate;
a channel semiconductor layer provided on a part of the underlayer, having a lattice constant different from that of the underlayer, and having a tensile stress applied in one direction of the channel length direction and the channel width direction and a compressive stress applied in the other;
source/drain regions provided on the underlying layer so as to sandwich the channel semiconductor layer; and
a gate electrode provided on the channel semiconductor layer via a gate insulating film;
wherein the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[Claim 3]

A field effect transistor, equipped with
a gate electrode provided on a part of a semiconductor substrate with a gate insulating film interposed therebetween;
a source/drain underlayer, embedded in a groove provided in the substrate to the middle of the groove with the channel region under the gate electrode interposed therebetween, containing the same element as the substrate, and made of an alloy semiconductor having a lattice constant different from that of the substrate; and
a source/drain region having a lattice constant different from that of the underlying layer, provided on the underlying layer so as to sandwich the channel region;
wherein tensile stress is applied to the channel region in one direction of the channel length direction and the channel width direction, and compressive stress is applied to the other; and
the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[Claim 4]

The field effect transistor according to any one of claims 1 to 3,
wherein the source/drain regions are n-type, tensile strain is applied to the channel region or channel semiconductor layer in the channel length direction and compressive strain in the channel width direction.

[Claim 5]

The field effect transistor according to any one of claims 1 to 3,
wherein the source/drain regions are p-type, compressive strain is applied to the channel region or channel semiconductor layer in the channel length direction and tensile strain in the channel width direction

[Claim 6]

A field effect transistor, equipped with
a plate-like semiconductor fin, formed on a semiconductor substrate substantially perpendicular to the main surface of the substrate, in which a first region where a channel region is to be formed is formed higher than a second region where source/drain regions are to be formed on both sides of the channel region;
a buried insulating film buried around a lower portion of the fin;
a gate electrode provided via a gate insulating film on at least both side surfaces of the first region of the fin;
a source/drain underlying layer made of an alloy semiconductor containing the same element as the substrate and having a lattice constant different from that of the substrate, provided in the second region of the fin to a position lower than the upper end of the first region; and
a source/drain region having a lattice constant different from that of the underlying layer, provided on the underlying layer so as to sandwich an upper portion of the first region;

wherein stress is applied to the channel region in the channel length direction; and the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[Claim 7]

The field effect transistor according to any one of claims 1 to 3 and 6, wherein the source/drain regions are made of the same alloy semiconductor as that of the underlying layer but have a different composition ratio from that of the underlying layer, are formed lattice-matched on the underlying layer, and act as a stressor that applies stress to the channel region or the channel semiconductor layer.

[Claim 8]

The field effect transistor according to any one of claims 1 to 3 and 6, wherein a stressor film surrounding the source/drain regions and the gate electrode is provided, and stress is applied to the channel region or the channel semiconductor layer by the stressor film.

[Claim 9]

The field effect transistor according to claim 7, wherein the substrate and the channel region or channel semiconductor layer are both Ge, the underlying layer is Si_{1-x}Ge_x, and the source/drain regions are Si_{1-y}Ge_y ($y < x$).

[Claim 10]

The field effect transistor according to claim 8, wherein the substrate and the channel region or channel semiconductor layer are both made of Si, the underlying layer is made of Si_{1-x}Ge_x, and the source/drain is made of Si_{1-y}Ge_y ($y > x$).

[Detailed Description of the Invention]

[Technical Field]

The present invention relates to a MOS type field effect transistor (MOSFET).

[Prior Art]

[0002]

In recent years, in order to improve the performance of MOSFETs, a technique of increasing carrier mobility by applying strain to the channel has been used. An attempt to use a Ge channel, which has both higher electron and hole mobilities than Si, is also under study. Furthermore, studies on a strained Ge channel have been initiated by combining the two (see, for example, Non-Patent Document 1).

[0003]

When such a strained channel is used, there is concern about deterioration of device characteristics and occurrence of defects due to the generation of strain-induced dislocations. For example, if dislocations occur in the depletion layer under the source/drain, there is concern about an increase in leakage current due to impurities abnormally diffused along the dislocations. In the worst case, a short circuit between the source and drain occurs. These factors lead to the occurrence of defects, leading to a decrease in yield.

[Prior Art Documents]

[Non-Patent Literature]

[0004]

[Non-Patent Document 1] Y.-J. Yang, et al., Appl. Phys. Lett. 91, 102103 (2007).

[Non-Patent Document 2] D. C. Houghton, J. Appl. Phys. 70, 2136 (1991).

[Non-Patent Document 3] I. Yonenaga and K. Sumino, J. Appl. Phys. 80, 3244 (1996).

[Outline of the invention]

[Problems to be solved by the invention]

[0005]

SUMMARY OF THE INVENTION An object of the present invention is to provide a field effect transistor that can reduce leakage current when a strained channel is used, suppress the occurrence of defects, and improve the yield.

[Means for solving the problem]

[0006]

A field effect transistor according to one aspect of the present invention is equipped with a stressed channel region, a gate electrode provided on the channel region via a gate insulating film, source/drain regions provided on both sides of the channel region, and an underlying layer made of an alloy semiconductor provided at least under the source/drain regions; wherein the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[0007]

In addition, a field effect transistor according to another aspect of the present invention is equipped with an underlying layer provided on a semiconductor substrate and made of an alloy semiconductor containing the same elements as the substrate and having a lattice constant different from that of the substrate; a channel semiconductor layer provided on a part of the underlayer, having a lattice constant different from that of the underlayer, and having a tensile stress applied in one direction of the channel length direction and the channel width direction and a compressive stress applied in the other; source/drain regions provided on the underlying layer so as to sandwich the channel semiconductor layer; and a gate electrode provided on the channel semiconductor layer via a gate insulating film; wherein the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[0008]

Further, a field effect transistor according to another aspect of the present invention is equipped with a gate electrode provided on a part of a semiconductor substrate with a gate insulating film interposed therebetween; a source/drain underlayer, embedded in a groove provided in the substrate to the middle of the groove with the channel region under the gate electrode interposed therebetween, containing the same element as the substrate, and made of an alloy semiconductor having a lattice constant different from that of the substrate; and a source/drain region having a lattice constant different from that of the underlying layer, provided on the underlying layer so as to sandwich the channel region; wherein tensile stress is applied to the channel region in one direction of the channel length direction and the channel width direction, and compressive stress is applied to the other; and the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[0009]

Moreover, a field effect transistor according to another aspect of the present invention is equipped with a plate-like semiconductor fin, formed on a semiconductor substrate substantially perpendicular to the main surface of the substrate, in which a first region where a channel region is to be formed is formed higher than a second region where source/drain regions are to be formed on both sides of the channel region; a buried insulating film buried around a lower portion of the fin; a gate electrode provided via a gate insulating film on at least both side surfaces of the first region of the fin; a source/drain underlying layer made of an alloy semiconductor containing the same element as the substrate and having a lattice constant different from that of the substrate, provided in the second region of the fin to a position lower than the upper end of the first region; and a source/drain region having a lattice constant different from that of the underlying layer, provided on the underlying layer so as to sandwich an upper portion of the first region; wherein stress is applied to the channel region in the channel length direction; and the underlying layer is formed thicker than the thickness at which the depletion layer formed under the source/drain regions is accommodated in the underlying layer, and is formed thinner than the thermal equilibrium critical thickness at which misfit dislocations are introduced into a crystal in a thermal equilibrium state.

[Effects of the Invention]

[0010]

According to the present invention, since the depletion layer under the source/drain regions is substantially included in the mixed crystal underlayer (metal semiconductor layer) in which dislocations are unlikely to occur, off-leakage current can be reduced when using a strained channel. Therefore, it is possible to suppress the occurrence of defects and improve the yield.

[Brief Description of the Drawings]

[0011]

FIG. 1 is a cross-sectional view showing the element structure of a MOS field effect transistor according to a first embodiment; FIGS. 2A and 2B are schematic diagrams showing states of lattice distortion in specific examples according to the first embodiment; FIG.

FIGS. 3A and 3B are cross-sectional views showing a manufacturing process of the MOS field effect transistor of the first embodiment; FIG.

FIG. 4 is a cross-sectional view showing the device structure of a MOS field effect transistor according to a second embodiment; FIGS. 5A and 5B are cross-sectional views showing the manufacturing process of the MOS field effect transistor of the second embodiment;

FIG. 6 is a cross-sectional view showing the element structure of a MOS field effect transistor according to a third embodiment; FIGS. 7A and 7B are cross-sectional views showing the manufacturing process of the MOS field effect transistor of the third embodiment;

FIGS. 8A and 8B are a plan view and a cross-sectional view showing the element structure of a MOS field effect transistor according to a fourth embodiment; FIG.

FIGS. 9A and 9B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment;

FIGS. 10A and 10B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment; FIG.

FIGS. 11A and 11B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment;

FIGS. 12A and 12B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment;

FIGS. 13A and 13B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment;

FIGS. 14A and 14B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment;

FIGS. 15A and 15B are a plan view and a cross-sectional view showing the manufacturing process of the MOS field effect transistor according to a fourth embodiment;

FIGS. 16A and 16B are a plan view and a cross-sectional view showing the manufacturing process of the MOS field effect transistor according to a fourth embodiment;

FIGS. 17A and 17B are a plan view and a cross-sectional view showing a manufacturing process of a MOS field effect transistor according to a fourth embodiment;

[Mode for Carrying Out the Invention]

[0012]

The details of the present invention will now be described with reference to the illustrated embodiments.

[0013]

(First embodiment)

The structure of a MOS field effect transistor 100 according to a first embodiment of the invention is shown in FIG. 1.

[0014]

A base layer 20 made of an alloy semiconductor containing the same element as the substrate 10 and a channel semiconductor layer (channel region) 30 are sequentially laminated on a semiconductor substrate 10 in a lattice-matched manner. A gate electrode 50 is formed on the channel semiconductor layer 30 with a gate insulating film 40 interposed therebetween. A source region 60 and a drain region 70 made of semiconductors having different composition ratios and different lattice constants from the substrate 10 and the underlying layer 20, containing the same element

as the substrate 10 across the gate electrode 50, are formed on the underlying layer 20 so as to be lattice-matched. Stress is applied to the channel semiconductor layer 30 by these source/drain regions 60 and 70. A sidewall insulating film 81 is formed on the side surface of the gate electrode 50.

[0015]

Here, the underlying layer 20 generally has a lattice constant different from that of the substrate 10, and therefore has strain. Therefore, in order to prevent the generation of dislocations, the thickness of the underlying layer 20 is less than the thermal equilibrium critical thickness at which misfit dislocations are introduced into the crystal in the thermal equilibrium state (Non-Patent Document 2). Further, the thickness of the underlying layer 20 is set thicker than the widths of the depletion layer 61 under the source region 60 and the depletion layer 71 under the drain region 70. That is, the underlying layer 20 is formed to be thicker than the thickness at which depletion layers 61 and 71 formed under the source/drain regions 60 and 70 are accommodated within the underlying layer 20. In addition, a metal compound layer (NiGeSi or the like) having a thickness of about 5 to 20 nm may be formed on the surfaces of the source/drain regions 60 and 70.

[0016]

In this embodiment, since the underlying layer 20 is an alloy semiconductor, compared with a conventional structure using a source/drain structure for applying stress to a substrate of a single element such as Si or Ge, dislocations are less likely to occur in the region below the source/drain. This feature is due to the hardening phenomenon resulting from alloying observed in SiGe bulk crystals (Non-Patent Document 3).

[0017]

Moreover, since the depletion layers 61 and 71 of the source/drain lower regions are all included in the underlying alloy layer, there is a feature wherein dislocations that cause leakage current do not occur in the depletion layers. Furthermore, since the thickness of the underlying layer 20 is less than the thermal equilibrium critical thickness, there is no occurrence of dislocation due to lattice mismatch between the substrate 10 and the underlying layer 20. Due to these effects, it is possible to suppress an increase in leakage current caused by dislocations or the occurrence of defects caused thereby.

[0018]

(Specific Example 1-1)

As a first specific example of the first embodiment, the field effect transistor 100 is a strained Ge-nMOSFET having tensile strain in the electron conduction direction (channel length direction). Note that "MOS" also includes so-called "MIS" which uses an insulating film other than a silicon oxide film for the gate insulating film.

[0019]

Here, the substrate 10 is p-type Ge, the ground layer 20 is p-type $\text{Si}_{0.05}\text{Ge}_{0.95}$ with a film thickness of 70 nm, channel semiconductor layer 30 is p-type Ge with a film thickness of 8 nm, gate insulating film 40 is LaAlO_3 with a film thickness of 5 nm and GeO_2 interlayer with a film thickness of less than 1 nm, gate electrode 50 is Tin with a film thickness of 20 nm, and both source region 60 and drain region 70 are $\text{Si}_{0.3}\text{Ge}_{0.7}$ with a film thickness of 30 nm doped with P (phosphorus) as a high-concentration n-type impurity.

[0020]

Further, from the viewpoint that the depletion layers 61 and 71 in the lower regions of the source/drain regions 60 and 70 are all included in the ground layer 20 and dislocations do not occur between the ground layer 20 and substrate 10 the preferable Ge composition range of the ground layer 20 is 85% or higher and 99% or lower. Furthermore, the lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 95%); the higher the Ge composition, the larger the upper limit. Also, regarding the source/drain regions 60 and 70, the Ge composition range preferable is 50% to 85%, and the preferable film thickness is 5 nm to 50 nm.

[0021]

Other components can be modified within the scope that can be easily conceived by those skilled in the art. In terms of the plane index of the substrate and the channel length direction, the (111) plane and the [110] direction are optimal, respectively, from the viewpoint of maximizing the drive current, but other orientations may be used since the dependence of the drive current on the channel orientation is small on the (111) plane. Furthermore, a driving current comparable to that on the (111) plane can be obtained even in the $[-110]$ direction on the (110) plane.

[0022]

In addition, in this specific example, the substrate 10 is not limited to bulk Ge substrate, and substrates such as substrate in which a Ge single crystal layer is formed on a Si substrate, a substrate in which a Ge single crystal layer is formed on an SOI (Si-on-insulator) substrate, or a substrate in which a Ge single crystal layer is formed on an SGOI (SiGe-on-insulator) substrate can be used.

[0023]

SiGe:C or Ge:C with carbon added, or SiGeSn with Sn added may be used as the ground 20. In this case, the atomic composition of C is preferably from 0.1% to 2%, and the atomic composition of Sn is preferably from 0.1% to 3%. Furthermore, SiGe:C or Ge:C to which carbon is added may be used for the source/drain regions 60 and 70. In this case, the atomic composition of C is preferably in the range of 0.1% to 5%. Also, the channel semiconductor layer 30 may be SiGe having a higher Ge composition than the ground layer 20.

[0024]

In the first specific example, the lattice constant when the channel is viewed from above extends in the channel length direction, as shown in FIG. 2(a). This is due to the tensile stress from the SiGe source/drain regions 60, 70, which have a smaller lattice constant than the Ge channel. On the other hand, it is compressed in the channel width direction orthogonal to the channel length direction. This is a synergistic effect between the effect of lattice shrinkage in the channel width direction due to tensile stress applied in the channel length direction in a state where elastic deformation in the direction is possible due to element isolation in the gate width direction, and the lattice constant of ground layer 20 being smaller than the channel semiconductor layer 30. Such a strained configuration is the optimum configuration for increasing current in Ge-nMOSFETs.

[0025]

Next, the manufacturing method of the first specific example will be described referring to FIG. 3.

[0026]

First, as shown in FIG. 3(a), a ground layer 20 made of SiGe and a channel semiconductor layer 30 made of Ge are epitaxially grown in sequence on a Ge substrate 10 by a low-pressure chemical vapor deposition method (LP-CVD method) or the like. Subsequently, element isolation is performed by a method such as STI, and B ions are implanted deeper than the ground layer 20 as a p-type channel impurity (not shown).

[0027]

Next, as shown in FIG. 3(b), gate insulating film 40 and gate electrode 50 are sequentially deposited on the channel semiconductor layer 30 by CVD method or the like. Subsequently, after forming a gate pattern (not shown) by photolithography, the gate electrode 50 and the gate insulating film 40 are patterned by reactive ion etching (RIE), as shown in FIG. 3(c).

[0028]

Next, as shown in FIG. 3(d), a Si nitride film (Si₃N₄) 80 which will be the side wall is deposited on the entire surface by CVD method or the like. Subsequently, as shown in FIG. 3(e), sidewall insulating film 81 is formed by etching the Si nitride film 80 by RIE method, and channel semiconductor layer 30 is etched to form recess 82 reaching the ground layer 20 and having a depth of about 20 nm.

[0029]

Next, as shown in FIG. 3(f), source/drain regions 60 and 70 made of SiGe in which P is heavily incorporated as an n-type dopant are epitaxially grown by the LP-CVD method or the like.

[0030]

Thereafter, activation annealing is performed, and the strained Ge-nMOSFET 100 is completed through a normal wiring formation process.

[0031]

(Specific Example 1-2)

As a second specific example of the first embodiment, the field effect transistor 100 is a strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).

[0032]

Here, substrate 10 is n-type Si, ground layer 20 is n-type $\text{Si}_{0.95}\text{Ge}_{0.05}$ with a film thickness of 70 nm, channel semiconductor layer 30 is n-type Si with a film thickness of 8 nm, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, both the source region 60 and drain region 70 are $\text{Si}_{0.7}\text{Ge}_{0.3}$ with a thickness of 30 nm heavily doped with B.

[0033]

Furthermore, the preferable Ge composition range of ground layer 20 is 1% or more and 15% or less, from the viewpoint that the depletion layers 61 and 71 in the lower region of the source / drain regions 60 and 70 are all included in the ground layer 20, and dislocations do not occur between the ground layer 20 and substrate 10. Furthermore, the lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 5%); the lower the Ge composition, the higher the upper limit. Also, regarding the source/drain regions 60 and 70, the preferable Ge composition range is 15% to 50%, and the preferable range for film thickness is 5 nm to 50 nm from the viewpoint of generating as large stress as possible while avoiding stress reduction due to plastic deformation.

[0034]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the art. From the viewpoint of maximizing the driving current, the plane index of the substrate and the channel length direction are optimal in the (110) plane and the [110] direction, respectively, but the effect of increasing the drive current due to strain is obtained even on the (111) plane and the (100) planes.

[0035]

In this specific example, not only a bulk Si substrate but also an SOI substrate may be used as substrate 10. SiGe:C to which carbon is added or SiGeSn or SiSn to which Sn is added may be used as ground layer 20. In this case, the atomic composition of C is preferably from 0.1% to 2%, and the atomic composition of Sn is preferably from 0.1% to 3%. Furthermore, SiGe:C or Ge:C to which carbon is added may be used for the source/drain regions 60 and 70.

[0036]

In the second example, the lattice constant when the channel is viewed from above is compressed in the channel length direction, as shown in FIG. 2(b). This is due to the compressive stress from the SiGe source/drain regions 60, 70, which have a larger lattice constant than the Si channel. On the other hand, it is pulled in the channel width direction. This is a synergistic effect between the effect of expanding the lattice in the channel width direction due to the compressive stress applied in the channel length direction in a state where elastic deformation is possible in that direction due to the element isolation in the gate width direction, and that ground layer 20 has a larger lattice constant than the channel semiconductor layer 30. Such a strained configuration is the optimum configuration for increasing current in Si-pMOSFETs.

[0037]

The manufacturing method of the second specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0038]

(Specific Example 1-3)

As a third specific example of the first embodiment, the field effect transistor 100 is a strained Ge-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).

[0039]

Here, substrate 10 is n-type Ge, ground layer 20 is n-type $\text{Si}_{0.04}\text{Ge}_{0.95}\text{Sn}_{0.01}$ with a film thickness of 70 nm, channel semiconductor layer 30 is n-type Ge with a film thickness of 8 nm, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a GeO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both the source region 60 and the drain region 70 are $\text{Sn}_{0.05}\text{Ge}_{0.95}$ with a film thickness of 30 nm doped with B as a p-type impurity at a high concentration.

[0040]

Furthermore, the preferable Ge composition range of the ground layer is 85% or more and 99% or less from the viewpoint that all the depletion layers 61 and 71 in the lower regions of the source/drain regions 60 and 70 are included in the ground layer 20 and that dislocations do not occur between the ground layer 20 and substrate 10. The lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[\text{Sn composition} \times 5 - \text{Si composition}] = 5\%$), and the Ge composition and lower the Sn, the higher the upper limit. In addition, regarding the source/drain regions 60 and 70, the preferable range of Sn composition is from 1% to 10%, and the preferable range of film thickness is 5 nm to 50 nm.

[0041]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the art. In terms of the plane index of the substrate and the channel length direction, the 111 plane and the 110 direction are optimal, respectively, from the viewpoint of maximizing the drive current, but the effect of increasing the drive current due to strain is obtained even on the 111 plane and the 100 plane.

[0042]

In the third specific example, the lattice constant when the channel is viewed from above is compressed in the channel length direction, as shown in FIG. 2(b). This is due to compressive stress from the SnGe source/drain regions 60, 70, which have a larger lattice constant than the Ge channel. On the other hand, it is pulled in the channel width direction. This is the effect of expanding the lattice in the channel width direction because compressive stress is applied in the channel length direction in a state where elastic deformation in the direction is possible due to element isolation in the gate width direction. Such a strained configuration is the optimum configuration for increasing current in Ge-pMOSFETs.

[0043]

In this specific example, substrate 10 is not limited to bulk Ge substrate, and substrates in which a Ge single crystal layer is formed on a Si substrate, a substrate in which a Ge single crystal layer is formed on an SOI substrate, or a substrate in which a Ge single crystal layer is formed on an SGOI substrate can be used. SiGeSn:C to which carbon is added may be used as ground layer 20. In this case, the atomic composition of C is preferably from 0.1% to 2%, and the atomic composition of Sn is preferably from 0.1% to 3%. Furthermore, SiGe:C or Ge:C to which carbon is added may be used for the source/drain regions 60 and 70. In this case, the atomic composition of C is preferably in the range of 0.1% to 5%. Also, SiGe may be used as ground layer 20, but in this case, $y > 2x$, where x and y are the Ge atomic compositions of the ground layer and the source/drain regions 60 and 70, respectively. This composition condition is for the above-described strained configuration. Also, the channel semiconductor layer 30 may be SiGe having a higher Ge composition than ground layer 20.

[0044]

The manufacturing method of the third specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0045]

(Specific Example 1-4)

As a fourth specific example of the first embodiment, the field effect transistor 100 is a strained Si-nMOSFET having tensile strain in the electron conduction direction (channel length direction).

[0046]

Here, substrate 10 is p-type Si, ground layer 20 is p-type $\text{Si}_{0.95}\text{Ge}_{0.045}\text{C}_{0.005}$ with a film thickness of 70 nm, channel semiconductor layer 30 is p-type Si with a film thickness of 8 nm, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both the source region 60 and the drain region 70 are $\text{Si}_{0.97}\text{C}_{0.03}$ with a film thickness of 30 nm heavily doped with P.

[0047]

Furthermore, the preferred Ge composition range of ground layer 20 is 1% or higher and 15% or lower, and the atomic composition of C is 0.1% to 2% from the viewpoint that all the depletion layers 61 and 71 in the lower regions of the source/drain regions 60 and 70 are included in the ground layer 20 and that dislocations do not

occur between ground layer 20 and substrate 10. In addition, the lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[C \text{ composition} \times 10 - \text{Ge composition}] = 5\%$), and the lower the Ge composition, the larger the upper limit. More preferably, the conditions are such that the Ge composition and the C composition $\times 10$ are almost equal, as in the above $\text{Si}_{0.95}\text{Ge}_{0.045}\text{C}_{0.005}$, and under this condition, the lattice mismatch between the ground layer 20 and the substrate 10 can be substantially ignored. Furthermore, with respect to the source/drain regions 60 and 70, the preferable Ge composition range is 15% to 50%, and film thickness is 5 nm to 50 nm from the viewpoint of generating as large stress as possible while avoiding stress reduction due to plastic deformation.

[0048]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the art. From the viewpoint of maximizing the driving current, the plane index of the substrate and the channel length direction are optimal in the (110) plane and the [110] direction respectively, but the effect of increasing the drive current due to strain is obtained even on the (111) plane and the (100) plane.

[0049]

In the fourth specific example, the lattice constant when the channel is viewed from above extends in the channel length direction, as shown in FIG. 2(a). This is due to the tensile stress from the Si:C source/drain regions 60, 70 which have a smaller lattice constant than the Si channel. On the other hand, it is compressed in the channel width direction. This is the effect that the lattice is reduced in the channel width direction because the tensile stress is applied in the channel length direction in a state where elastic deformation in the direction is possible due to the element isolation in the gate width direction.

[0050]

In this specific example, substrate 10 is not limited to bulk Si substrate, and SOI substrate may also be used. Further, SiGe:C to which carbon is added may be used for the ground layer 20 or the source/drain regions 60 and 70. In this case, the atomic composition of C is preferably in the range of 0.1% to 2%. SiGe may be used as ground layer 20, but in this case, $10y > 2x$, where x and y are the Ge atomic composition of the ground layer and the C atomic composition of the source/drain regions 60 and 70, respectively. This composition condition is for the above-described strained configuration.

[0051]

The manufacturing method of the fourth specific example conforms to the first specific example.

[0052]

In the above first to fourth specific examples, examples using group IV elements such as Si, Ge, C and Sn are shown, but combinations of other material systems are also possible. For example, the substrate 10 may be a Group III-V compound semiconductor substrate (GaAs, InP, InAs, etc.) or a substrate in which a compound semiconductor single crystal layer is formed directly or via a Ge layer on a Si substrate. Further, alloys thereof (GaAlAs, InGaAs, InGaAlAs, InAsP, etc.) may be used for the ground layer 20 and the source/drain regions 60 and 70.

[0053]

(Embodiment 2)

The structure of a MOS field effect transistor 200 according to a second embodiment of the invention is shown in FIG. 4.

[0054]

On semiconductor substrate 10, ground layer 20 made of an alloy semiconductor containing the same element as the substrate 10 and a channel semiconductor layer (channel region) 30 are laminated in order with lattice matching. Gate electrode 50 is formed on channel semiconductor layer 30 with a gate insulating film 40 interposed therebetween. A source electrode 65 and a drain electrode 75 made of a metal compound layer containing a channel layer element are formed on the ground layer 20 with the gate electrode 50 interposed therebetween. Here, the source/drain electrodes 65 and 75 may cut into the ground alloy layer 20. Regions 62 and 72 doped with high-concentration impurities may be formed in the lower part of the source/drain electrodes 65 and 75. Sidewall insulating film 81 is formed on the side surface of gate electrode 50.

[0055]

Force application film 90 containing strain is formed so as to cover the gate electrode 50, the source/drain electrodes 65 and 75, and the sidewall insulating film 81, and force is applied to the channel semiconductor layer 30 by the force application film 90. Here, ground layer 20 generally has a lattice constant different from that of the substrate 10, and therefore has strain. Therefore, in order to prevent the generation of dislocations, it is desirable that the film thickness is less than the thermal equilibrium critical film thickness. Further, the thickness of ground layer 20 is set thicker than the width of the depletion layers 61 and 71 on the lower part of the source/drain regions.

[0056]

In this embodiment, it is characterized in that dislocation is less likely to occur in the source/drain lower region compared to the conventional structure using a force application film for applying strain to a substrate of a single element such as Si or Ge since the ground layer 20 is an alloy semiconductor. Moreover, since the depletion layers 61 and 71 of the source/drain lower regions are all included in the ground alloy layer, there is a feature that dislocations that cause leak current do not occur in the depletion layers. Furthermore, since the thickness of ground layer 20 is less than the thermal equilibrium critical thickness, there is no occurrence of dislocation due to lattice mismatch between the substrate 10 and the ground layer 20. Therefore, effects similar to those of the first embodiment can be obtained.

[0057]

(Specific Example 2-1)

As a first specific example of the second embodiment, the field effect transistor 200 is a strained Ge-nMOSFET having tensile strain in the electron conduction direction (channel length direction).

[0058]

Here, substrate 10 is p-type Ge, ground layer 20 is p-type $\text{Si}_{0.05}\text{Ge}_{0.95}$ with a film thickness of 70 nm, channel semiconductor layer 30 is p-type Ge with a film thickness of 8 nm, gate insulating film 40 is LaAlO with a thickness of 5 nm and a GeO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both the source electrode 65 and the drain electrode 75 are NiGe with a film thickness of 12 nm. Regions 62 and 72 doped with high-concentration P are formed in the lower part of the source/drain electrodes 65 and 75, respectively. Force application film 90 is a silicon nitride film or a DLC (Diamond-Like Carbon) film.

[0059]

In addition, the preferable Ge composition range of the ground layer 20 is 85% or higher and 99% or lower, from the viewpoint that all of the depletion layers 61 and 71 in the lower regions of the source/drain electrodes 65 and 75 are included in the ground layer 20 and that dislocations do not occur between the ground layer 20 and the substrate 10. Furthermore, the lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 95%), and the higher the Ge composition, the higher the upper limit. Moreover, force application film 90 contains compressive force and applies tensile stress parallel to the current direction to the channel.

[0060]

Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer, channel layer material, etc.) can be modified in the same manner as described above (Specific Example 1-1).

[0061]

In the first specific example, the lattice constant when the channel is viewed from above extends in the channel length direction, as shown in FIG. 2(a). This is due to the tensile stress from the force application film 90 having compressive force. On the other hand, it is compressed in the channel width direction. This is a synergistic effect between the effect of lattice shrinkage in the channel width direction due to tensile stress applied in the channel length direction in a state where elastic deformation in the direction is possible due to element isolation in the gate width direction, and the lattice constant of ground layer 20 being smaller than the channel semiconductor layer 30. Such a strained configuration is the optimum configuration for increasing current in Ge-nMOSFETs.

[0062]

Next, the manufacturing method of the first specific example will be described referring to FIG. 5.

[0063]

First, as in FIG. 3 (a), a ground layer 20 made of SiGe and a channel semiconductor layer 30 made of Ge were epitaxially grown in order on a Ge substrate 10 by the LP-CVD method or the like, and then element isolation is

performed by a method such as STI, and B ions are implanted deeper than the ground layer 20 as a p-type channel impurity.

[0064]

Next, as shown in FIG. 5(a), gate insulating film 40, gate electrode 50, and a cap layer 83 are sequentially deposited by CVD method or the like. Subsequently, after forming a gate pattern (not shown) by photolithography, as shown in FIG. 5(b), gate electrode 40, the gate insulating film 50, and the cap layer 83 are patterned by RIE method.

[0065]

Next, as shown in FIG. 5(c), Si nitride film 80 to be a sidewall is deposited on the entire surface by the CVD method or the like. Subsequently, as shown in FIG. 5(d), sidewall insulating film 81 is formed by etching the Si nitride film 80 by RIE method, and Ni film 84 with a thickness of about 7 nm is deposited by sputtering method or CVD method.

[0066]

Next, as shown in FIG. 5(e), after Ni and Ge are reacted by heat treatment to form the source/drain electrodes 65 and 75 made of NiGe germanide, and the unreacted Ni film 84 is removed by acid treatment.

[0067]

Next, as shown in FIG. 5(f), when P is ion-implanted into NiGe as an n-type dopant and activation annealing is performed, P is segregated under the NiGe source/drain electrodes 65 and 75 to form high-concentration P layers 62 and 72. Subsequently, a force application film 90 is deposited by the CVD method or the like so as to cover the entire surface. After that, the strained Ge-nMOSFET 200 is completed through a normal wiring formation process.

[0068]

(Specific Example 2-2)

As a second specific example of the second embodiment, the field effect transistor 200 is a strained Si-pMOSFET having compressive strain in the electron conduction direction (channel length direction).

[0069]

Here, substrate 10 is n-type Si, ground layer 20 is n-type $\text{Si}_{0.95}\text{Ge}_{0.05}$ with a film thickness of 70 nm, the channel semiconductor layer 30 is Si with a film thickness of 8 nm, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both the source electrode 65 and the drain electrode 75 are NiSi with a film thickness of 12 nm. Regions 62 and 72 doped with B at a high concentration are formed on the lower side of source/drain electrodes 65 and 75, respectively. Force application film 90 is a silicon nitride film or a DLC (Diamond-Like Carbon) film.

[0070]

Furthermore, the preferable Ge composition range of the ground layer 20 is 1% or higher and 15% or less, from the viewpoint that all of the depletion layers 61 and 71 in the lower regions of the source/drain electrodes 65 and 75 are included in the ground layer 20 and that dislocations do not occur between the ground layer 20 and the substrate 10. Furthermore, the lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 5%); the lower the Ge composition, the higher the upper limit.

[0071]

Force application film 90 contains tensile stress and applies compressive stress parallel to the current direction to the channel. Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer material, etc.) can be modified in the same manner as described above (Specific Example 1-2).

[0072]

In the second specific example, the lattice constant when the channel is viewed from above is compressed in the channel length direction, as shown in FIG. 2(b). This is due to the compressive stress from the force application film 90 having elastic stress. On the other hand, it is pulled in the channel width direction. This is the effect of expanding the lattice in the channel width direction because compressive stress is applied in the channel length direction in a state where elastic deformation in the direction is possible due to element isolation in the gate width direction. Such a strained configuration is the optimum configuration for increasing current in Ge-pMOSFETs.

[0073]

The manufacturing method of the second specific example conforms to the first specific example. However, since the electrical polarities are opposite, B is used as the channel impurity, and P is used as the source/drain impurity.

[0074]

(Specific Example 2-3)

As a third example of the second embodiment, the field effect transistor 200 is a strained Ge-pMOSFET with compressive strain in the direction of hole conduction.

[0075]

Here, substrate 10 is n-type Ge, ground layer 20 is n-type $\text{Si}_{0.04}\text{Ge}_{0.95}\text{Sn}_{0.01}$ with a film thickness of 70 nm, channel semiconductor layer 30 is n-type Ge with a film thickness of 8 nm, gate insulating film 40 is LaAlO with a thickness of 5 nm and a GeO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both the source electrode 65 and the drain electrode 75 are NiGe with a film thickness of 12 nm. Regions 62 and 72 doped with high-concentration P are formed on the lower part of the source/drain electrodes 65 and 75, respectively. Force application film 90 is a silicon nitride film or a DLC (Diamond-Like Carbon) film.

[0076]

Furthermore, the preferable Ge composition range of ground layer 20 is 85% or higher and 99% or lower, and the atomic composition of Sn is 3% or lower from the viewpoint that all of the depletion layers 61 and 71 in the lower regions of the source/drain electrodes 65 and 75 are included in the ground layer 20 and that dislocations do not occur between the ground layer 20 and the substrate 10. The lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[\text{Sn composition} \times 5 - \text{Si composition}] = 5\%$); the higher the Ge composition and the lower the Sn composition, the higher the upper limit.

[0076]

The force application film 90 contains tensile stress and applies compressive stress parallel to the current direction to the channel. Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer, channel layer material, etc.) can be modified in the same manner as described above (Specific Example 1-3).

[0078]

In the third specific example, the lattice constant when the channel is viewed from above is compressed in the channel length direction, as shown in FIG. 2(b). This is due to the compressive stress from the force application film 90 having elastic stress. On the other hand, it is pulled in the channel width direction. This is the effect of expanding the lattice in the channel width direction because compressive stress is applied in the channel length direction in a state where elastic deformation in the direction is possible due to element isolation in the gate width direction. Such a strained configuration is the optimum configuration for increasing current in Ge-pMOSFETs. In particular, in $\text{Sn composition} \times 5 > \text{Si composition}$, the tensile strain in the channel width direction becomes larger since the lattice constant of the ground layer 20 is larger than the lattice constant of the channel layer 30, which is more preferable from the viewpoint of improving mobility.

[0079]

The manufacturing method of the third specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0080]

(Specific Example 2-4)

As a fourth specific example of the second embodiment, the field effect transistor 200 is a strained Si-nMOSFET with tensile strain in the electron conduction direction.

[0081]

Here, substrate 10 is p-type Si, ground layer 20 is p-type $\text{Si}_{0.95}\text{Ge}_{0.045}\text{C}_{0.005}$ with a film thickness of 70 nm, channel semiconductor layer 30 is p-type Si with a film thickness of 8 nm, gate insulating film 40 is LaAlO with a thickness of 5 nm and a SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both the source electrode 65 and the drain electrode 75 are NiSi with a film thickness of 12 nm. Regions 62 and 72 doped with high-concentration P are formed on the lower part of the source/drain electrodes 65 and 75, respectively. Force application film 90 is a silicon nitride film or a DLC (Diamond-Like Carbon) film.

[0082]

Furthermore, the preferred Ge composition range of ground layer 20 is 1% or higher and 15% or lower, and the atomic composition of C is 0.1% to 2% from the viewpoint that all of the depletion layers 61 and 71 in the lower regions of the source/drain electrodes 65 and 75 are included in the ground layer 20 and that dislocations do not occur between the ground layer 20 and the substrate 10. In addition, the lower limit of the film thickness of the ground layer 20 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if [Ge composition - C composition $\times 10$] = 5%); the lower the Ge composition, the larger the upper limit. More preferably, as in the above $\text{Si}_{0.95}\text{Ge}_{0.045}\text{C}_{0.005}$, this is a condition in which the Ge composition and the value of C composition $\times 10$ are almost equal, and under this condition, the lattice mismatch between the ground layer 20 and the substrate 10 can be substantially ignored.

[0083]

Force application film 90 contains a compressive stress and applies a tensile stress parallel to the current direction to the channel. Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer material, etc.) can be modified in the same manner as described above (Specific Example 1-4).

[0084]

In the fourth specific example, the lattice constant when the channel is viewed from above extends in the channel length direction, as shown in FIG. 2(a). This is due to the tensile stress from the force application film 90 containing compressive stress. On the other hand, it is compressed in the channel width direction. This is the effect that the lattice is reduced in the channel width direction because the tensile stress is applied in the channel length direction in a state where elastic deformation in the direction is possible due to the element isolation in the gate width direction.

[0085]

The manufacturing method of the fourth specific example conforms to the first specific example.

[0086]

Of course, the modifications described in the first embodiment are also possible in the above-described first to fourth specific examples.

[0087]

(Embodiment 3)

The structure of a MOS field effect transistor 300 according to a third embodiment of the invention is shown in FIG. 6.

[0088]

Gate electrode 50 is formed on semiconductor substrate 10 with a gate insulating film 40 interposed therebetween. A groove is formed in the substrate 10 with the gate electrode 50 interposed therebetween, and this groove contains source/drain ground layers 63 and 73 made of an alloy semiconductor containing the same element as the substrate and the same element as the substrate, both the substrate 10 and the ground layers 63 and 73 have different composition ratios, and source/drain regions 60 and 70 made of alloy semiconductors having different lattice constants are formed on the ground layer 20 so as to be lattice-matched. A force is applied to the channel region 35 under the gate electrode by these source/drain regions 60 and 70.

[0089]

Here, the ground layers 63 and 73 generally have a lattice constant different from that of the substrate 10, and therefore have strain. Therefore, the film thickness is less than the thermal equilibrium critical film thickness in order to prevent the generation of dislocations. The thickness of the ground layers 63 and 73 is set thicker than the width of the depletion layer 61 under the source region 60 and the depletion layer 71 under the drain region 70. A metal compound layer (NiGeSi or the like) having a thickness of about 5 to 20 nm may be formed on the surfaces of the source/drain regions 60 and 70.

[0090]

In the present embodiment, the ground layers 63 and 73 are alloy semiconductors. Therefore, it is characterized in that dislocation is less likely to occur in the source/drain lower region compared to a conventional structure using a source/drain structure for applying strain to a substrate of a single element such as Si or Ge. In addition, it is characterized in that dislocations that cause leakage current do not occur in the depletion layer, since

the depletion layers 61 and 71 of the source/drain lower regions are all included in the ground layers 63 and 73. Furthermore, since the thickness of the ground layers 63 and 73 is less than the thermal equilibrium critical thickness, it is characterized in that no dislocation occurs due to lattice mismatch between the substrate 10 and the ground layers 63 and 73.

[0091]

(Specific Example 3-1)

As a first specific example of the third embodiment, the field effect transistor 300 is a strained Ge-n MOSFET having tensile strain in the electron conduction direction (channel length direction).

[0092]

Here, substrate 10 is p-type Ge, the source ground 63 and the drain ground 73 are p-type $\text{Si}_{0.05}\text{Ge}_{0.95}$ with a film thickness of 70 nm, channel region 35 is p-type Ge, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a GeO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, cap layer 83 is a Si nitride film with a film thickness of 10 nm, and both source region 60 and the drain region 70 are $\text{Si}_{0.3}\text{Ge}_{0.7}$ with a film thickness of 30 nm doped with P as a high-concentration n-type impurity.

[0093]

Furthermore, the preferable Ge composition range for ground layers 63 and 73 is 85% or higher and 99% or lower from the viewpoint that the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are all included in the source/drain ground layers 63, 73, and no dislocation occurs between the ground layers 63 and 73 and the substrate 10. In addition, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 95%); the higher the Ge composition, the larger upper limit. Furthermore, a favorable Ge composition range are 50% to 85%, and a favorable film thickness range is 5 nm to 50 nm.

[0094]

Other constituent elements (substrate plane index, channel length direction, substrate material, base layer material, etc.) can be modified in the same manner as described above (Specific Example 1-1).

[0095]

Next, a manufacturing method of the first specific example of the third embodiment will be described with reference to FIG. 7.

[0096]

First, as shown in FIG. 7(a), after element isolation (not shown) is performed on the Ge substrate 10 by a method such as STI, gate insulating film 40, a gate electrode 50, and a cap layer 83 are sequentially deposited on the Ge substrate 10 by CVD method or the like.

[0097]

Next, as shown in FIG. 7(b), after forming a gate pattern (not shown) by photolithography, cap layer 83, the gate electrode 50, and the gate insulating film 40 are patterned by RIE method.

[0098]

Next, as shown in FIG. 7(c), Si nitride film (Si_3N_4) 80, which will be a side wall, is deposited on the entire surface by the CVD method or the like. Subsequently, as shown in FIG. 7(d), sidewall insulating film 81 is formed by etching the Si nitride film 80 by RIE method, and the substrate 10 is etched to form a recess 82 with a depth of 80 nm.

[0099]

Next, as shown in Figure 7(e), p-type SiGe ground layers 63 and 73 are formed up to the middle of the recess 82 by the LP-CVD method or the like. Subsequently, as shown in FIG. 7(f), SiGe source/drain regions 60 and 70 in which P is heavily incorporated as an n-type dopant are epitaxially grown by the LP-CVD method or the like.

[0100]

Thereafter, activation annealing is performed, and the strained Ge-nMOSFET 300 is completed through a normal wiring formation process.

[0101]

(Specific Example 3-2)

As a second specific example of the third embodiment, the field effect transistor 300 is a strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).

[0102]

Here, substrate 10 is n-type Si, source ground layer 63 and the drain ground layer 73 are n-type $\text{Si}_{0.95}\text{Ge}_{0.05}$ with a film thickness of 70 nm, channel region 35 is n-type Si, gate insulating film 40 is LaAlO with a thickness of 5 nm and a SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, cap layer 83 is a Si nitride film with a film thickness of 10 nm, and both source region 60 and the drain region 70 are $\text{Si}_{0.3}\text{Ge}_{0.7}$ with a film thickness of 30 nm doped with B as a p-type impurity at a high concentration.

[0103]

Furthermore, the preferable Ge composition range of the ground layers 63 and 73 is 1% or higher and 15% or lower, from the viewpoint that the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are all included in the source/drain ground layers 63, 73, and from the viewpoint that no dislocation occurs between the ground layers 63, 73 and the substrate 10. Furthermore, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 95%); the lower the Ge composition, the larger the upper limit. In addition, the preferable Ge composition range is preferably from 15% to 50%, and the preferable film thickness is 5 nm to 50 nm.

[0104]

Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer material, etc.) can be modified in the same manner as described above (Specific Example 1-2).

[0105]

The manufacturing method of the second specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0106]

(Specific Example 3-3)

As a third specific example of the third embodiment, the field effect transistor 300 is a strained Ge-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).

[0107]

Here, substrate 10 is n-type Ge, source ground layer 63 and the drain ground layer 73 are made of n-type $\text{Si}_{0.04}\text{Ge}_{0.95}\text{Sn}_{0.01}$ with a film thickness of 70 nm, channel region 35 is n-type Ge, gate insulating film 40 is LaAlO with a thickness of 5 nm and a GeO interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both source region 60 and the drain region 70 are $\text{Sn}_{0.05}\text{Ge}_{0.95}$ with a film thickness of 30 nm doped with B as a p-type impurity at a high concentration.

[0108]

Furthermore, the preferable Ge composition range of the ground layers 63 and 73 is 85% or higher and 99% or lower from the viewpoint that the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are all included in the source/drain ground layers 63, 73, and that no dislocation occurs between the ground layers 63, 73 and the substrate 10. Moreover, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[\text{Sn composition} \times 5 - \text{Si composition}] = 5\%$); the higher the Ge composition and the lower the Sn composition, the larger the upper limit. In addition, the preferable Sn composition range is 1% to 10%, and the preferable range of film thickness is 5 nm to 50 nm.

[0109]

Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer material, etc.) can be modified in the same manner as described above (Specific Example 1-3).

[0110]

The manufacturing method of the third specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0111]

(Specific Example 3-4)

As a fourth specific example of the third embodiment, the field effect transistor 300 is a strained Si-nMOSFET having tensile strain in the electron conduction direction (channel length direction).

[0112]

Here, substrate 10 is p-type Si, source ground layer 63 and the drain ground layer 73 are p-type $\text{Si}_{0.95}\text{Ge}_{0.045}\text{C}_{0.005}$ with a film thickness of 70 nm, channel region 35 is p-type Si, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 is TiN with a film thickness of 20 nm, and both source region 60 and the drain region 70 are $\text{Si}_{0.97}\text{C}_{0.03}$ with a film thickness of 30 nm heavily doped with P.

[0113]

Furthermore, the preferable Ge composition range in the ground layers 63 and 73 is 1% or higher and 15% or lower, and the atomic composition of C is 0.1% to 2% from the viewpoint that all the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are included in the source/drain ground alloy layers 63, 73, and no dislocation occurs between the ground layers 63, 73 and the substrate 10. In addition, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[\text{Ge composition} - \text{C composition} \times 10] = 5\%$); the lower the Ge composition, the larger the upper limit. More favorably, like $\text{Si}_{0.95}\text{Ge}_{0.045}\text{C}_{0.005}$ above, this is a condition in which the Ge composition and the value of $\text{C composition} \times 10$ are almost equal, and under this condition the lattice mismatch between the ground layers 63 and 73 and the substrate 10 can be substantially ignored. Furthermore, the preferable range of atomic composition of C is from 0.1% to 5%, and the preferable range of film thickness is 5 nm to 50 nm.

[0114]

Other constituent elements (substrate plane index, channel length direction, substrate material, ground layer material, etc.) can be modified in the same manner as described above (Specific Example 1-4).

[0115]

The manufacturing method of the fourth specific example conforms to the first specific example.

[0116]

Of course, the modifications described in the first embodiment are also possible in the above-described first to fourth specific examples.

[0117]

(Embodiment 4)

FIG. 8 shows the structure of a MOS field effect transistor 400 according to the fourth embodiment of the invention. In FIG. 8, (a) is a top view, (b) is A-A' cross section in (a), (c) is a B-B' cross section, and (d) is a C-C' cross section.

[0118]

A plate-shaped semiconductor region (semiconductor fin) 31 is formed on the semiconductor substrate 10 substantially perpendicular to the main surface of the substrate, the bottom periphery of the fin 31 is buried with a buried insulating film 90, and channel region is formed above the embedded insulating film 90 of the fin 31. A cap layer 83 is formed on the upper surface of the fin 31, but the cap layer 83 is not necessarily required. A gate electrode 50 is formed on both side surfaces of the upper portion of the fin 31 with a gate insulating film 40 interposed therebetween.

[0119]

A depression portion is formed in the fin 31 with the gate electrode 50 interposed therebetween, and within this depression, a source ground layer 63 and a drain ground layer 73 made of an alloy semiconductor containing the same element as the substrate 10 are formed in a lattice-matched manner. Furthermore, on the ground layers 63 and 73, source region 60 and a drain region 70 made of an alloy semiconductor that contains the same elements as those of the substrate 10, has a composition ratio different from that of the substrate 10 and the ground layers

63 and 73, and has a different lattice constant, have formed in a lattice-matched manner. A force is applied to the channel region of fin 31 by the source/drain regions 60 and 70.

[0120]

Here, the ground layers 63 and 73 generally have a lattice constant different from that of the substrate 10, and therefore have strain. Therefore, the film thickness is less than the thermal equilibrium critical film thickness in order to prevent the generation of dislocations. The thickness of the ground layers 63 and 73 is set thicker than the width of the depletion layer 61 under the source region 60 and the depletion layer 71 under the drain region 70. A metal compound layer (NiGeSi or the like) having a thickness of about 5 to 20 nm may be formed on the surfaces of the source/drain regions 60 and 70.

[0121]

In this embodiment, it is characterized in that dislocation is less likely to occur in the source/drain lower region compared to a conventional structure using a source/drain structure for applying strain to a substrate of a single element such as Si or Ge, since the ground layers 63 and 73 are alloy semiconductors. In addition, it is characterized in that dislocations that cause leakage current do not occur in the depletion layer, since the depletion layers 61 and 71 of the source/drain lower regions are all included in the ground layers 63 and 73. Furthermore, it is characterized in that no dislocation occurs due to lattice mismatch between the substrate 10 and the ground layers 63 and 73 since the thickness of the ground layers 63 and 73 is less than the thermal equilibrium critical thickness. Therefore, effects similar to those of the first embodiment can be obtained.

[0122]

(Specific Example 4-1)

As a first specific example of the fourth embodiment, the fin-type field effect transistor 400 is a strained Ge-n MOSFET having tensile strain in the electron conduction direction (channel length direction).

[0123]

Here, substrate 10 is p-type Ge, source ground layer 63 and the drain ground layer 73 are p-type $\text{Si}_{0.05}\text{Ge}_{0.95}$ with a film thickness of 50 nm, fin 31 and the channel region are p-type Ge, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a GeO interface layer with a thickness of less than 1 nm, gate electrode 50 has a laminated structure of a TiN film 51 with a film thickness of 10 nm and an n-type poly SiGe film 52, cap layer 83 is a Si nitride film with a film thickness of 30 nm, and both source region 60 and the drain region 70 are $\text{Si}_{0.3}\text{Ge}_{0.7}$ with a film thickness of 30 nm doped with P as a high-concentration n-type impurity. Instead of the poly-SiGe film 52, poly-Si, poly-Ge, their metal compounds (such as NiSiGe), and metals such as TaN may be used.

[0124]

Furthermore, the preferable Ge composition range of ground layers 63 and 73 is 85% or higher and 99% or lower from the viewpoint that all the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are included in the source/drain ground layers 63, 73, and that no dislocation occurs between the ground layers 63, 73 and the substrate 10. The lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 95%); the higher the Ge composition, the larger the upper limit. In addition, the source/drain regions 60 and 70 have a preferable Ge composition range of 50% to 90%, and a preferable range of film thickness from 5 nm to 50 nm, from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation.

[0125]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the art. Further, from the viewpoint of maximizing the drive current, the plane index and channel direction of the side surface (the plane serving as the channel) of the fin 31 are optimal for the (111) plane and the [110] direction, respectively, but other orientations may be used since the dependence of the drive current on the channel orientation is small on the (111) plane. In addition, a driving current comparable to that on the (111) plane can be obtained even in the $[-110]$ direction on the (110) plane. Also on other planes such as the (100) plane, the effect of increasing the drive current due to strain can be obtained.

[0126]

In this specific example, the substrate 10 is not limited to bulk Ge substrate, and substrate in which a Ge single

crystal layer is formed on a Si substrate, substrate in which a Ge single crystal layer is formed on an SOI substrate, or substrate in which a Ge single crystal layer is formed on an SGOI substrate can also be used. SiGe:C or Ge:C with carbon added, or SiGeSn with Sn added may be used as the ground layers 63 and 73. In this case, the atomic composition of C is preferably from 0.1% to 2%, and the atomic composition of Sn is preferably from 0.1% to 3%.

[0127]

Further, SiGe:C or Ge:C to which carbon is added may be used for the source/drain regions 60 and 70. In this case, the atomic composition of C is preferably in the range of 0.1% to 5%. Furthermore, instead of the cap layer 83 on the upper portion of the fin 31, the gate insulating film 40 and the gate electrode 50 are also formed on the upper surface of the fin 31, and there is also a structure (tri-gate structure) possible in which three surfaces, the both side surfaces and the upper surface, serve as channels.

[0128]

A manufacturing method of the first specific example of the fourth embodiment will be described with reference to Figs. 9 to FIG. 17. Here, in FIG. 9 to FIG. 17, (a) is a top view, (b) is a sectional view taken along line A-A' in FIG. 9(a).

[0129]

First, as shown in FIG. 9(a) (b), after cap layer 83 is formed on Ge substrate 10, and this cap layer 83 is patterned by photolithography, a plate-shaped semiconductor region (semiconductor fin) 31 with a cap layer 83 placed thereon is formed by etching the substrate 10 by the RIE method.

[0130]

Next, as shown in FIG. 10 (a) (b), an insulating film 90 is buried around the lower portion of the fin 31. Specifically, after burying the fin 31 and the cap layer 83 with the insulating film 90, planarization is performed by CMP, and the insulating film 90 is etched by a predetermined amount by the RIE method. Furthermore, the upper portion of fin 31 is exposed on the insulating film 90 by removing the insulating film remaining on the side wall of the fin 31 with dilute hydrofluoric acid.

[0131]

Next, as shown in FIG. 11 (a) (b), a gate insulating film 40 and a TiN film 51 are formed on the protruding region of the fin 31 above the embedded insulating film 90 by CVD or the like, and a poly-SiGe film 52 is further deposited thereon.

[0132]

Next, as shown in FIG. 12 (a) (b), after planarizing the polySiGe film 52, the TiN film 51, and the gate insulating film 40 to the surface of the cap layer 83 by CMP, a poly SiGe film 52 is deposited again on the poly SiGe film 52, and a second cap layer 53 is deposited thereon.

[0133]

Next, as shown in FIG. 13 (a) (b), a gate pattern consisting of a cap layer 83, a poly-SiGe layer 52 and a second cap layer 53 is formed by photolithography and RIE method.

[0134]

Next, as shown in FIG. 14 (a) (b), after depositing a Si nitride film 80 for gate sidewalls over the entire surface, gate sidewall insulating films 81 are formed by RIE method as shown in Figure 15 (a) (b).

[0135]

Next, as shown in FIG. 16 (a) (b), recess 82 is formed in the source/drain forming region by RIE method. As a result, the second region where the source/drain should be formed on both sides of the first region where the channel of the fin 31 should be formed is lower than the first region where the channel of the fin 31 should be formed.

[0136]

Next, as shown in FIG. 17 (a) (b), ground layers 63 and 73 made of p-type $\text{Si}_{0.05}\text{Ge}_{0.95}$ are epitaxially grown in the recess 82, source/drain regions 60 and 70 of n-type $\text{Si}_{0.3}\text{Ge}_{0.7}$ are epitaxially grown thereon.

[0137]

Thereafter, activation annealing is performed, and the fin-type strained Ge-nMOSFET 400 is completed through a normal wiring formation process.

[0138]

(Specific Example 4-2)

As a second specific example of the fourth embodiment, the fin-type field effect transistor 400 is a strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).

[0139]

Here, substrate 10 is n-type Si, source ground layer 63 and the drain ground layer 73 are made of n-type $\text{Si}_{0.95}\text{Ge}_{0.05}$ with a film thickness of 50 nm, fin 31 and the channel region are made of n-type Si, gate insulating film 40 is LaAlO_3 with a thickness of 5 nm and a SiO_2 interface layer with a thickness of less than 1 nm, gate electrode 50 has a laminated structure of a TiN film 51 with a film thickness of 10 nm and a p-type poly-Si film 52, the cap layer 83 is a Si nitride film with a film thickness of 30 nm, and both source region 60 and the drain region 70 are $\text{Si}_{0.7}\text{Ge}_{0.3}$ with a film thickness of 30 nm doped with B as a p-type impurity at a high concentration. Instead of the poly-Si film 52, poly-SiGe, poly-Ge, their metal compounds (such as NiSiGe), and metals such as TaN may be used.

[0140]

Furthermore, the preferable Ge composition range for ground layers 63 and 73 is 1% or higher and 15% or lower from the viewpoint that depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are included in the source/drain ground layers 63, 73, and no dislocation occurs between the ground layers 63 and 73 and the substrate 10. In addition, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm when the Ge composition is 5%); the lower the Ge composition, the larger the upper limit. Furthermore, the source/drain regions 60 and 70 have a preferable Ge composition range of 50% to 90%, and a preferable range of film thickness from 5 nm to 50 nm from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation.

[0141]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the art. In addition, from the viewpoint of maximizing the drive current, the plane index and channel direction of the side surfaces of the fins 31 (the planes serving as channels) are optimal in the (110) plane and in the [110] direction, respectively, and the effect of increasing the drive current due to strain is obtained on the (111) plane and the (100) plane.

[0142]

In this specific example, substrate 10 is not limited to bulk Ge substrate, and an SOI substrate may also be used. SiGe:C to which carbon is added may be used as the ground layers 63 and 73. In this case, the atomic composition of C is preferably in the range of 0.1% to 2%. SiGe:C or Ge:C with carbon added, or SiGeSn or SiSn with Sn added may be used for the source/drain regions 60 and 70. In this case, the atomic composition of C is preferably from 0.1% to 2%, and the atomic composition of Sn is preferably from 0.1% to 10%. Furthermore, a gate insulating film and a gate electrode are also formed on the upper surface of the fin instead of the cap layer on the fin, wherein a structure (tri-gate structure) in which three surfaces, both side surfaces and an upper surface, serve as channels is also possible.

[0143]

The manufacturing method of the second specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0144]

(Specific Example 4-3)

As a third specific example of the fourth embodiment, the fin-type field effect transistor 400 is a strained Ge-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).

[0145]

Here, substrate 10 is n-type Ge, source ground layer 63 and the drain ground layer 73 are made of n-type $\text{Si}_{0.05}\text{Ge}_{0.94}\text{Sn}_{0.01}$ with a film thickness of 50 nm, fin 31 and the channel region are n-type Ge, gate insulating film 40

is LaAlO with a thickness of 5 nm and a GeO interface layer with a thickness of less than 1 nm, gate electrode 50 has a laminated structure of a TiN film 51 and a poly SiGe film 52 with a thickness of 10 nm, cap layer 83 is a Si nitride film with a film thickness of 30 nm, and both source region 60 and the drain region 70 are $\text{Sn}_{0.05}\text{Ge}_{0.95}$ with a thickness of 30 nm doped with B as a p-type impurity at a high concentration.

[0146]

Furthermore, the preferable Ge composition range for the ground layers 63 and 73 is 85% or higher and 99% or lower from the viewpoint that the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are all included in the source/drain ground layers 63, 73, and no dislocation occurs between the ground layers 63 and 73 and the substrate 10. In addition, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, and the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[\text{Sn composition} \times 5 - \text{Si composition}] = 5\%$); the higher the Ge composition, the larger the upper limit. More preferably, as in the case of $\text{Si}_{0.05}\text{Ge}_{0.94}\text{Sn}_{0.01}$ above, this is a condition in which the Si composition and the value of $\text{Sn composition} \times 5$ are almost equal, and under this condition, the lattice mismatch between the ground layers 63 and 73 and the substrate 10 can be substantially ignored. The preferable Sn composition range is 1% to 10%, and the preferable film thickness is 5 nm to 5 nm from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation regarding the source/drain regions 60 and 70.

[0147]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the art. In terms of the plane index of the fin sidewall and the channel direction, the (110) plane and the [110] direction are optimal, respectively, from the viewpoint of maximizing the drive current, but the effect of increasing the drive current due to strain is obtained even on the (111) plane and the (100) plane.

[0148]

The manufacturing method of the third specific example conforms to the first specific example. However, since the electrical polarities are opposite, P is used as the channel impurity, and B is used as the source/drain impurity.

[0149]

(Specific Example 4-4)

As a fourth specific example of the fourth embodiment, the fin-type field effect transistor 400 is a strained Si-nMOSFET having tensile strain in the electron conduction direction (channel length direction).

[0150]

Here, substrate 10 is p-type Si, source ground layer 63 and the drain ground layer 73 are p-type $\text{Si}_{0.945}\text{Ge}_{0.05}\text{C}_{0.005}$ with a film thickness of 50 nm, fin 31 and the channel region are p-type Si, gate insulating film 40 is LaAlO with a thickness of 5 nm and a SiO interface layer with a thickness of less than 1 nm, gate electrode 50 has a laminated structure of a TiN film 51 and a poly SiGe film 52 with a thickness of 10 nm, cap layer 83 is a Si nitride film with a film thickness of 30 nm, and both source region 60 and the drain region 70 are $\text{Si}_{0.97}\text{C}_{0.03}$ with a film thickness of 30 nm doped with P as a high-concentration n-type impurity.

[0151]

Furthermore, the preferable Ge composition range of ground layer 63 and 73 is 1% or higher and 15% or lower, and the atomic composition of C is 0.1% to 2% from the viewpoint the depletion layers 61, 71 in the lower regions of the source/drain regions 60, 70 are all included in the source/drain ground layers 63, 73, and no dislocation occurs between the ground layers 63 and 73 and the substrate 10. Furthermore, the lower limit of the film thickness of the ground layers 63 and 73 is 30 nm, the upper limit of the film thickness is the thermal equilibrium critical film thickness according to the composition (for example, 80 nm if $[\text{C composition} \times 10 - \text{Ge composition}] = 5\%$); the lower the Ge composition, the larger the upper limit. More preferably, as in $\text{Si}_{0.945}\text{Ge}_{0.05}\text{C}_{0.005}$ above, this is a condition in which the Ge composition and the value of $\text{C composition} \times 10$ are almost equal, and under this condition the lattice mismatch between the ground layer 20 and the substrate 10 can be substantially ignored. In addition, the preferable atomic composition range of C is from 0.1% to 5%, and the preferable range of film thickness is 5 nm to 50 nm from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation regarding the source/drain regions 60 and 70.

[0152]

Other constituent elements can be modified within the scope that can be easily conceived by those skilled in the

art. In terms of the plane index of the fin sidewall and the channel direction, the (100) plane and the [110] direction are optimal, respectively, from the viewpoint of maximizing the drive current, but the effect of increasing the drive current due to the strain can be obtained even on the (111) plane and the (110) plane.

[0153]

The manufacturing method of the Fourth specific example conforms to the First specific example.

[0154]

Also, in the above First to Fourth specific examples, of course, the modifications described in the first embodiment are possible.

[Description of Reference Numerals]

[0155]

10: semiconductor substrate

20: ground layer

30: channel semiconductor layer

31: Semiconductor fin

35: channel region

40: gate insulating film

50: gate electrode

51: TiN film

52: SiGe film

53, 83: cap layer

60: source region

61: source lower depletion layer

62: impurity doping region

63: source ground layer

65: source electrode

70: drain region

71: drain lower depletion layer

72: impurity doping region

73: drain ground layer

75: drain electrode

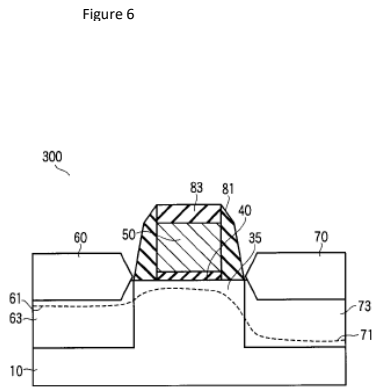
80: Si oxide film

81: gate side wall insulating film

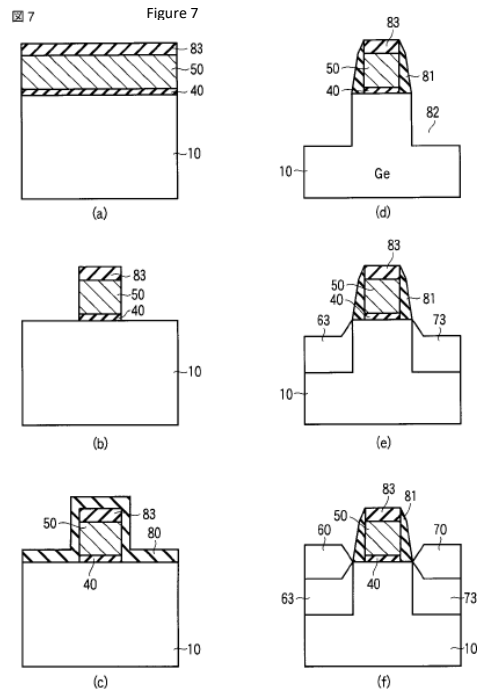
82: recess

90: force application film

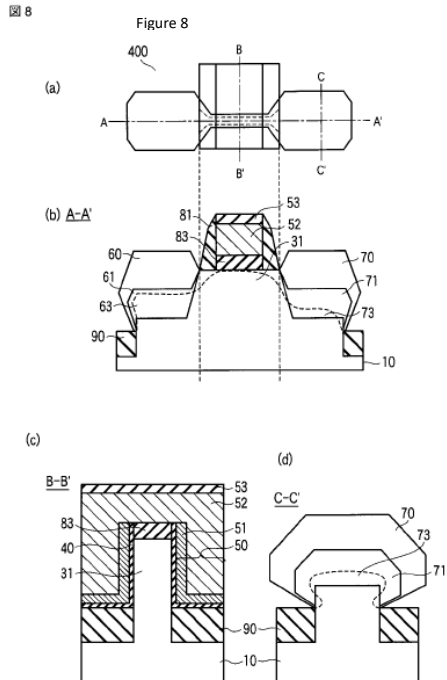
[FIG. 6]



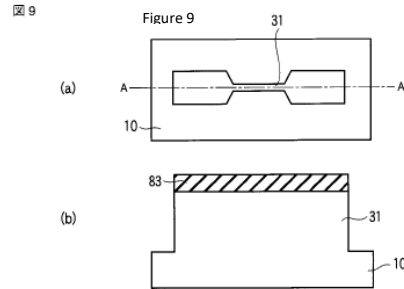
[FIG. 7]



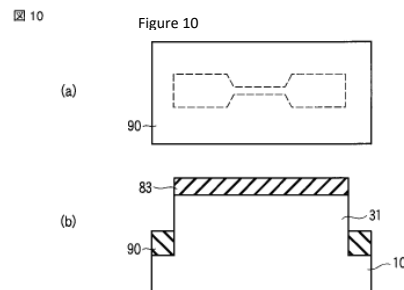
【 図 8 】 [FIG. 8]



【 図 9 】 [FIG. 9]

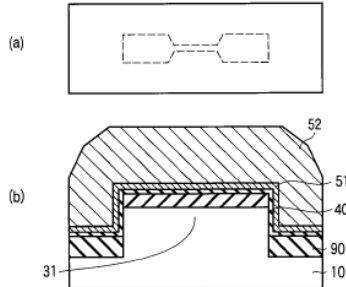


【 図 10 】 [FIG. 10]



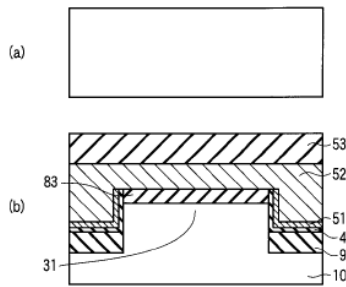
[FIG. 11]

Figure 11



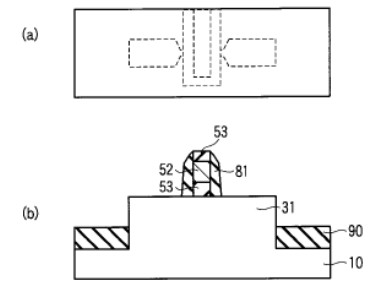
[FIG. 12]

Figure 12



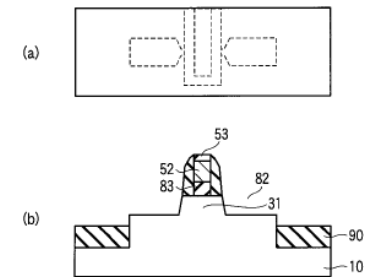
[FIG. 15]

Figure 15



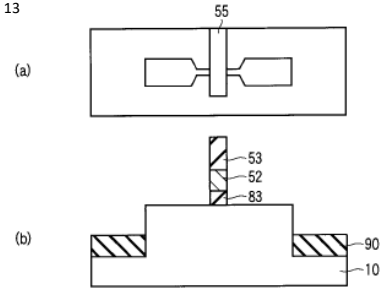
[FIG. 16]

Figure 16



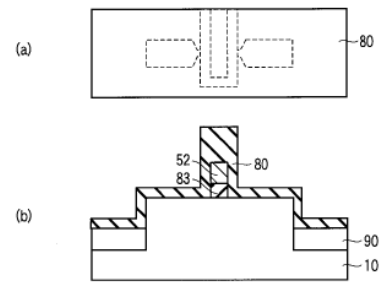
[FIG. 13]

Figure 13



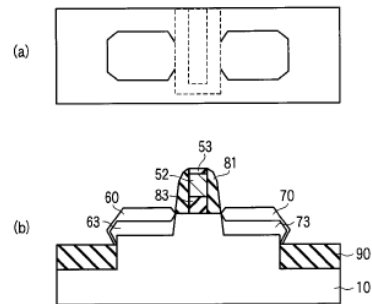
[FIG. 14]

Figure 14



[FIG. 17]

Figure 17



Continued from the front page

(51)Int.Cl.	F I	Theme code (reference)
	H O I L 29/50	M
	H O I L 29/78	6 1 8 Z
	H O I L 29/78	6 1 6 U
	H O I L 29/78	6 1 6 V

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F Term (Reference)	4M104	AA01	AA02	AA09	BB21	BB30	BB36	CC01	CC05	DD04	DD37
		DD43	DD65	DD83	EE03	EE16	FF13	GG09	GG10	GG14	
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		FF29	GG01	GG02	GG03	GG06	GG07	GG17	GG19	GG22	GG25
		GG47	HK05	HK06	HK08	HK18	HK25	HK37	HK39	HK42	HM02
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		BH50	BJ01	BJ06	BJ30	BK09	BK15	BK17	BK21	BK34	CC08

CC12
5F152 LL03 LN03 LN08 MMO4 NN03 NN04 NN06 NN07 NN08 NN15
NN27 NN29 NP02 NP04 NP05 NP08 NQ03 NQ04 NQ05 NQ08

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I am conversant in the English and Japanese languages and am a competent translator thereof. The accompanying English language translation is a true and correct translation of JP2010171337A to the best of my knowledge and belief.

I further declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable under Section 1001 of Title 18 of the United States Code.



Signature of Translator

December 10, 2022

Date