

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Glenn A. Glass
U.S. Patent No.: 10,700,178 Attorney Docket No.: 39843-0153IP1
Issue Date: June 30, 2020
Appl. Serial No.: 16/416,445
Filing Date: May 20, 2019
Title: CONTACT RESISTANCE REDUCTION EMPLOYING GERMA-
NIUM OVERLAYER PRE-CONTACT METALIZATION

Mail Stop Patent Board

Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

**PETITION FOR *INTER PARTES* REVIEW OF UNITED STATES PATENT
NO. 10,700,178 PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42**

TABLE OF CONTENTS

I.	REQUIREMENTS FOR IPR	1
A.	Grounds for Standing.....	1
B.	Challenge and Relief Requested.....	1
II.	OVERVIEW OF THE '178 PATENT	2
A.	Subject Matter Overview	2
B.	Summary of the File History	4
C.	Level of Ordinary Skill in the Art.....	5
III.	Claim Construction.....	6
IV.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	6
A.	[GROUND 1A] – Obviousness based on Tezuka and Tung (Claims 1, 4-6, 9-10).....	6
1.	Overview of Tezuka	6
2.	Overview of Tung	7
3.	Obviousness Analysis	8
B.	[GROUND 1B] – Obviousness based on Tezuka, Tung, and Simonelli (Claims 1-10)	35
1.	Overview of Simonelli	35
2.	Obviousness Analysis	36
C.	[GROUND 2] – Obviousness based on Tung in view of Simonelli (Claims 1-10)	44
1.	Obviousness Analysis	44
D.	[GROUND 3A] – Obviousness based on Conway, Tezuka, and Tung (Claims 11-20)	73
1.	Overview of Conway	73
2.	Obviousness Analysis	74
E.	[GROUND 3B] – Obviousness based on Conway, Tezuka, Tung, and Simonelli (Claims 11-20).....	80
F.	[GROUND 3C] – Obviousness based on Conway, Tung, and Simonelli (Claims 11-20)	80
V.	DISCRETIONARY CONSIDERATIONS	81
A.	§ 325(d) – <i>Advanced Bionics</i>	81
B.	§314(a) - <i>Fintiv</i>	81
VI.	MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1).....	82
A.	Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1).....	82
B.	Related Matters Under 37 C.F.R. § 42.8(b)(2)	82
C.	Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3).....	82

D. Service Information	83
VII. FEES	83
VIII. CONCLUSION.....	83

EXHIBITS

- SAMSUNG-1001 U.S. Patent No. 10,700,178 to Glass (“the ’178 Patent”)
- SAMSUNG-1002 File History of the ’178 Patent
- SAMSUNG-1003 Expert Declaration of Dr. Fred Schubert
- SAMSUNG-1004 [RESERVED]
- SAMSUNG-1005 Certified English Translation of Japanese Patent Application
Publication No. 2010-171337 (“Tezuka”)
- SAMSUNG-1006 U.S. Patent App. Pub. No. 2010/0276761 (“Tung”)
- SAMSUNG-1007 U.S. Patent App. Pub. No. 2011/0073952 (“Kwok”)
- SAMSUNG-1008 U.S. Patent App. Pub. No. 2010/0148217 (“Simonelli”)
- SAMSUNG-1009 U.S. Patent App. Pub. No. 2012/0139015 (“Yu”)
- SAMSUNG-1010 U.S. Patent App. Pub. No. 2009/0325607 (“Conway”)
- SAMSUNG-1011 U.S. Patent App. Pub. No. 2011/0042748 (“Anderson”)
- SAMSUNG-1012 Japanese Patent Application Publication No. 2010-171337
(Original Japanese version of Tezuka)
- SAMSUNG-1013 Excerpts of the File History of EP Patent App. No. 19188924.5
- SAMSUNG-1014 Complainant Daedalus Prime LLC’s Infringement Claim Chart
for U.S. Patent No. 10,700,178 (Exhibit 47 to Complaint), *In
the Matter of Certain Semiconductor Devices, Mobile Devices
Containing the Same, and Components Thereof* (ITC Investiga-
tion No. 337-TA-1336)
- SAMSUNG-1015 Complainant Daedalus Prime LLC’s Infringement Claim Chart
for U.S. Patent No. 11,251,281 (Exhibit 48 to Complaint), *In
the Matter of Certain Semiconductor Devices, Mobile Devices*

Containing the Same, and Components Thereof (ITC Investigation No. 337-TA-1336)

- SAMSUNG-1016 Findlay Shearer, *Power Management in Mobile Devices - A View of Energy Conservation - Part IV*, EE Times, May 5, 2008, available at <https://www.eetimes.com/power-management-in-mobile-devices-a-view-of-energy-conservation-part-iv/>
- SAMSUNG-1017 U.S. Patent App. Pub. No. 2011/0147842 (“Cappellani”)
- SAMSUNG-1018 U.S. Patent No. 7,288,443 (“Zhu”)
- SAMSUNG-1019 U.S. Patent No. 2007/0235802 (“Chong”)
- SAMSUNG-1020 U.S. Patent App. Pub. No. 2005/0184316 (“Kim I”)
- SAMSUNG-1021 U.S. Patent App. Pub. No. 2007/0082451 (“Samoilov”)
- SAMSUNG-1022 A. Nishida et al., *Elimination of Misfit Dislocations in Si_{1-x}Ge_x/Si Heterostructures by Limited-area Molecular-beam Epitaxial Growth*, J. Appl. Phys 71 at 5913-5917 (1992) (“Nishida”)
- SAMSUNG-1023 E.A. Fitzgerald, *The Effect of Substrate Growth Area on Misfit and Threading Dislocation Densities in Mismatched Heterostructures*, J. Vac. Sci. Tech. B7 at 782-788 (1989) (“Fitzgerald”)
- SAMSUNG-1024 Arne Larsen, *Epitaxial Growth of Ge and SiGe on Si Substrates*, Materials Science in Semiconductor Processing 9 at 454-459 (2006) (“Larsen”)
- SAMSUNG-1025 Schubert, *Room Temperature Properties of Si, Ge, GaAs, and GaN* (“Schubert Materials Datasheet”)
- SAMSUNG-1026 Elsevier, *Encyclopedia of Materials: Science and Technology* at pp. 8479-8486 (2001) (“Elsevier”)

- SAMSUNG-1027 Kim et al., *Increased Critical Thickness for High Ge-Content Strained SiGe-on-Si Using Selective Epitaxial Growth*, American Institute of Physics, Applied Physics Letter 97, 262106 (2010) (“Kim II”)
- SAMSUNG-1028 Semiconductor Doping Technology, *available at* <https://www.iue.tuwien.ac.at/phd/wittmann/node7.html>
- SAMSUNG-1029 Natalie Stavitski, *Silicide-to-Silicon Specific Contact Resistance Characterization: Test Structures and Models* (2009) (“Stavitski”)
- SAMSUNG-1030 EP Application No. 1 575 082 A2 (“Demeurisse”)
- SAMSUNG-1031 U.S. Patent No. 5,296,386 (“Aronowitz”)
- SAMSUNG-1032 U.S. Patent App. Pub. No. 2006/0286755 (“Brask”)
- SAMSUNG-1033 U.S. Patent App. Pub. No. 2011/0024804 (“Chang”)
- SAMSUNG-1034 [RESERVED]
- SAMSUNG-1035 Mirabella et al., *Mechanisms of Boron Diffusion in Silicon and Germanium*, Journal of Applied Physics 113, 031101 (2013) (“Mirabella”)
- SAMSUNG-1036 U.S. Patent App. Pub. No. 2006/0071275 (“Brask”)
- SAMSUNG-1037 Brown et al., *Lattice stability and point defect energetics of TiSi₂ and TiGe₂ allotropes from first-principles calculations*, Journal of Applied Physics 129, 085104 (2021) (“Brown”)
- SAMSUNG-1038-1100 [RESERVED]
- SAMSUNG-1101 Daedalus Prime LLC’s Complaint *In the Matter of Certain Semiconductor Devices, Mobile Devices Containing the Same, and Components Thereof* (ITC Investigation No. 337-TA-1336)

SAMSUNG-1102 Complaint, *Daedalus Prime LLC v. Samsung Electronics Co. Ltd. et al.*, Civil Action No. 2:22-cv-352 (E.D. Tex.) (September 12, 2022)

SAMSUNG-1103 Order Granting Stay, *Daedalus Prime LLC v. Samsung Electronics Co. Ltd. et al.*, Civil Action No. 2:22-cv-352 (E.D. Tex.) (November 1, 2022)

SAMSUNG-1104 Director Katherine K. Vidal's Memorandum re Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation (June 21, 2022)

CLAIM LISTING

Element	Claim Language
[1pre]	An integrated circuit structure, comprising:
[1a]	a fin comprising silicon;
[1b]	a gate electrode over the fin;
[1c]	a first source or drain region in the fin proximate a first side of the gate electrode;
[1d]	the first source or drain region comprising two or more facets and a top surface;
[1e]	wherein the first source or drain region comprises silicon and germanium;
[1f]	having a germanium concentration graded to a concentration in excess of 50%;
[1g]	a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[1h]	a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side,
[1i]	the second source or drain region comprising two or more facets and a top surface,
[1j]	wherein the second source or drain region comprises silicon and germanium
[1k]	having a germanium concentration graded to a concentration in excess of 50%; and
[1l]	a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.

Element	Claim Language
[2]	The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration greater than 1E20.
[3]	The integrated circuit structure of claim 1, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of 1E20.
[4]	The integrated circuit structure of claim 1, wherein the fin comprises a strained channel between the first and second source or drain regions.
[5]	The integrated circuit structure of claim 1, wherein the first and second source or drain regions are P-type.
[6pre]	An integrated circuit structure, comprising:
[6a]	a body comprising silicon;
[6b]	a gate electrode over the body;
[6c]	a first source or drain region in the body proximate a first side of the gate electrode,
[6d]	the first source or drain region comprising two or more facets and a top surface,
[6e]	wherein the first source or drain region comprises silicon and germanium
[6f]	having a germanium concentration graded to a concentration in excess of 50%
[6g]	a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[6h]	a second source or drain region in the body proximate a second side of the gate electrode opposite the first side,

Element	Claim Language
[6i]	the second source or drain region comprising two or more facets and a top surface,
[6j]	wherein the second source or drain region comprises silicon and germanium
[6k]	having a germanium concentration graded to a concentration in excess of 50%; and
[6l]	a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.
[7]	The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration greater than $1E20$.
[8]	The integrated circuit structure of claim 6, wherein the first and second source or drain regions have a boron concentration graded from a base level to a concentration in excess of $1E20$.
[9]	The integrated circuit structure of claim 6, wherein the body comprises a strained channel between the first and second source or drain regions.
[10]	The integrated circuit structure of claim 6, wherein the first and second source or drain regions are P-type.
[11pre]	A computing device, comprising:
[11a]	a board; and
[11b]	a component coupled to the board, the component including an integrated circuit structure, comprising:
[11c]	a fin comprising silicon;
[11d]	a gate electrode over the fin;

Element	Claim Language
[11e]	a first source or drain region in the fin proximate a first side of the gate electrode,
[11f]	the first source or drain region comprising two or more facets and a top surface,
[11g]	wherein the first source or drain region comprises silicon and germanium
[11h]	having a germanium concentration graded to a concentration in excess of 50%;
[11i]	a first germanide layer over the top surface of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[11j]	a second source or drain region in the fin proximate a second side of the gate electrode opposite the first side,
[11k]	the second source or drain region comprising two or more facets and a top surface,
[11l]	wherein the second source or drain region comprises silicon and germanium
[11m]	having a germanium concentration graded to a concentration in excess of 50%; and
[11n]	a second germanide layer over the top surface of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium.
[12]	The computing device of claim 11, further comprising: a memory coupled to the board.
[13]	The computing device of claim 11, further comprising: a communication chip coupled to the board.
[14]	The computing device of claim 11, further comprising: a camera coupled to the board.

Element	Claim Language
[15]	The computing device of claim 11, further comprising: a global positioning system coupled to the board.
[16]	The computing device of claim 11, further comprising: a battery coupled to the board.
[17]	The computing device of claim 11, further comprising: an antenna coupled to the board.
[18]	The computing device of claim 11, wherein the component is a packaged integrated circuit die.
[19]	The computing device of claim 11, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.
[20]	The computing device of claim 11, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) petitions for *In-ter Partes* Review (“IPR”) of claims 1-20 (“the Challenged Claims”) of U.S. Patent No. 10,700,178 (“the ’178 Patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’178 Patent is available for IPR. This petition is being filed within one year of service of a complaint against Samsung. Samsung is not barred or estopped from requesting review of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds set forth in the table shown below. Additional explanation and support for each ground is set forth in the expert declaration of Dr. Fred Schubert (SAMSUNG-1003), referenced throughout this Petition. Dr. Schubert’s analysis is corroborated by citation to various exhibits including exhibits from SAMSUNG-1016 through -1037.

Ground	Claims	Basis Under 35 U.S.C. §103
1A	1, 4-6, 9-10	Tezuka-Tung
1B	1-10	Tezuka-Tung-Simonelli
2	1-10	Tung-Simonelli
3A	11-20	Conway-Tezuka-Tung

Ground	Claims	Basis Under 35 U.S.C. §103
3B	11-20	Conway-Tezuka-Tung-Simonelli
3C	11-20	Conway-Tung-Simonelli

The '178 Patent, filed May 20, 2019, claims priority to an application filed on December 21, 2010 (“Critical Date”). Without acquiescence, Petitioner has applied prior art in this Petition that predates the Critical Date. Each of the prior art references qualifies as prior art to the '178 Patent as shown below:

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Tezuka	N/A	08/05/2010	§102(a)
Tung	01/06/2010	11/04/2010	§§102(a), (e)
Simonelli	12/11/2008	06/17/2010	§§102(a), (e)
Conway	05/28/2009	12/31/2009	§102(a), (e)

II. OVERVIEW OF THE '178 PATENT

A. Subject Matter Overview

The '178 Patent generally describes techniques for forming germanide-based contacts to the source and drain regions of a field-effect transistor (“FET”). SAMSUNG-1001, Abstract; SAMSUNG-1003, ¶40; *see also id.*, ¶¶40-44. The inventors purportedly sought to “reduce the band misalignment value and contact resistance” of such contacts by forming the germanide from an “**intermediate boron**

doped germanium layer” (also referred to as a germanium **“cap layer”**) “between the source/drain and contact metals,” where the “cap layer” is composed of more than ninety atomic-percentage germanium. SAMSUNG-1001, 2:45-49, 7:17-20, 10:41-50, 12:12-31, 14:3-6.

To illustrate, Figure 5F depicts an example in which boron-doped germanium cap layers 317/319 have been formed over source/drain regions 318/320. *Id.*, 12:49-57. A suitable contact metal 325/327, such as titanium, is deposited over cap layers 317/319. The contact metals 325/327 are then annealed with their respective cap layers 317/319 to form germanide layers that electrically couple the source and drain regions 318/320 to external circuitry via metal contact plugs 329/331. *Id.*, 11:56-12:31, 12:64-13:2.

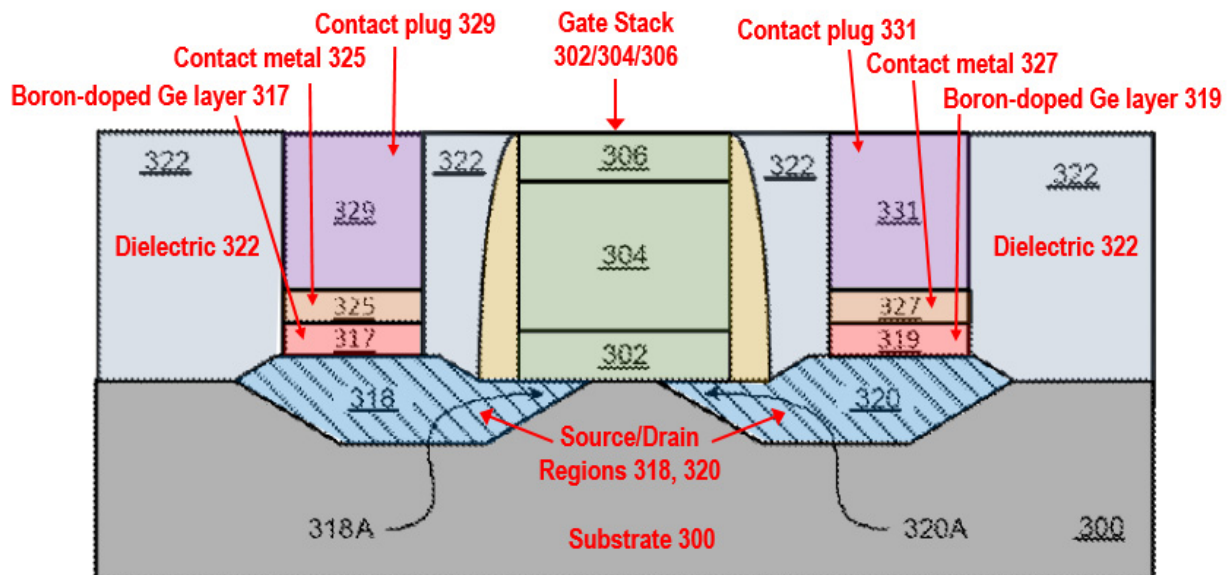
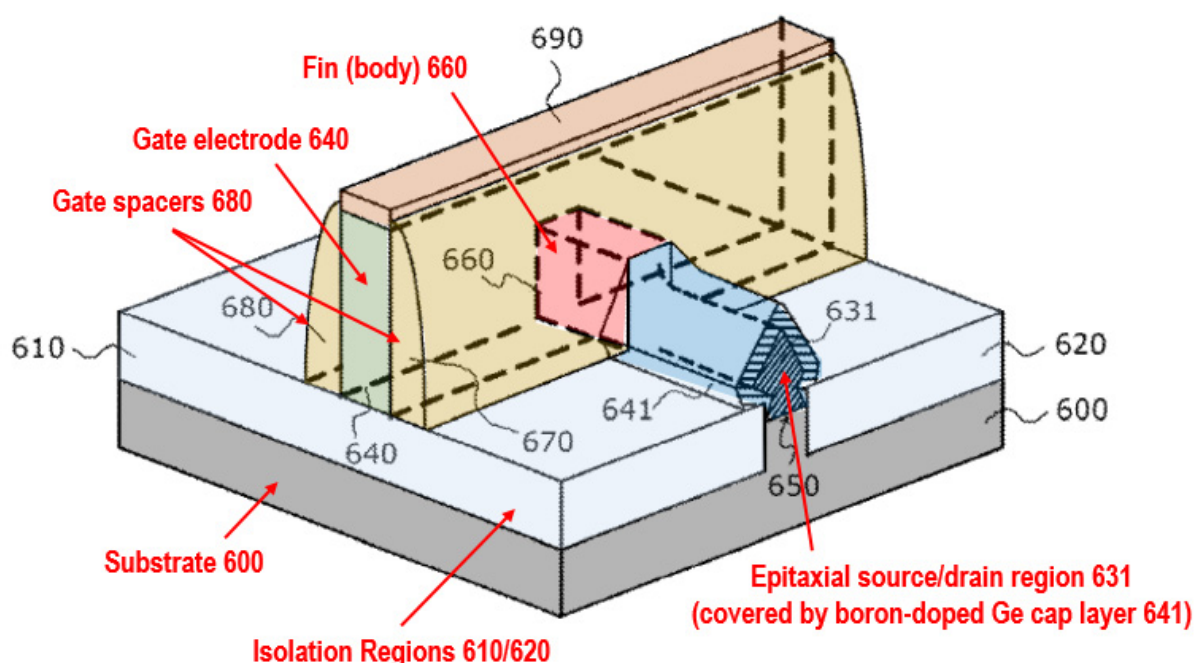


FIG. 5F

SAMSUNG-1001, FIG. 5F (annotated); *see also id.*, FIG. 3I.

The '178 Patent further explains how the boron-doped germanium caps can be used to improve contact resistance in a range of FETs, “including both planar and non-planar transistor structures (e.g., FinFETs).” *Id.*, 2:25-28. The Challenged Claims are specifically directed to non-planar devices (e.g., FinFETs or other devices that were known to have multiple gates that would wrap a “fin” or channel body on multiple sides), an embodiment of which is depicted in Figure 6:



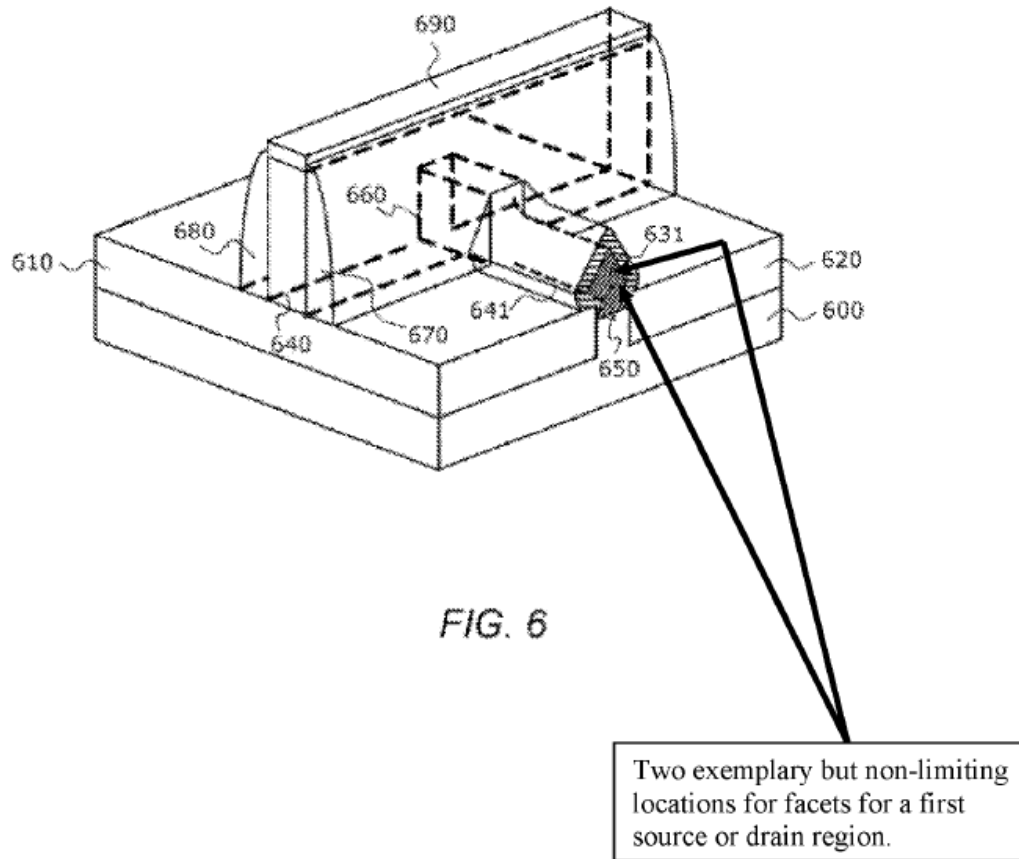
SAMSUNG-1001, FIG. 6; *see also id.*, 13:3-14:2.

B. Summary of the File History

In the only substantive action issued during original examination of the '178 Patent, the Examiner made no prior art rejections, but rejected the claims for lacking written description support for the limitations directed to “two or more facets”

of the source and drain regions. SAMSUNG-1002, 70-72; SAMSUNG-1003,

¶¶45-47. The applicant responded by arguing that Figure 6 depicted facets in the source/drain regions, and provided the following annotated version of Figure 6 to point out the supposed facets:



Annotated Figure 6 of Applicant's specification.

SAMSUNG-1002, 62.

The Examiner accepted the applicant's identification of support for "two or more facets," and allowed the application thereafter. SAMSUNG-1002, 34-41.

C. Level of Ordinary Skill in the Art

A person of ordinary skill as of the Critical Date ("POSITA") would have

had a Master's degree in electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing. Additional education could substitute for professional experience, or significant experience in the field could substitute for formal education. SAMSUNG-1003, ¶¶23-25.

III. Claim Construction

All claim terms should be construed according to the *Phillips* standard.

Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100.

“[C]laim terms need only be construed to the extent necessary to resolve the controversy.” *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); SAMSUNG-1003, ¶¶48-49.

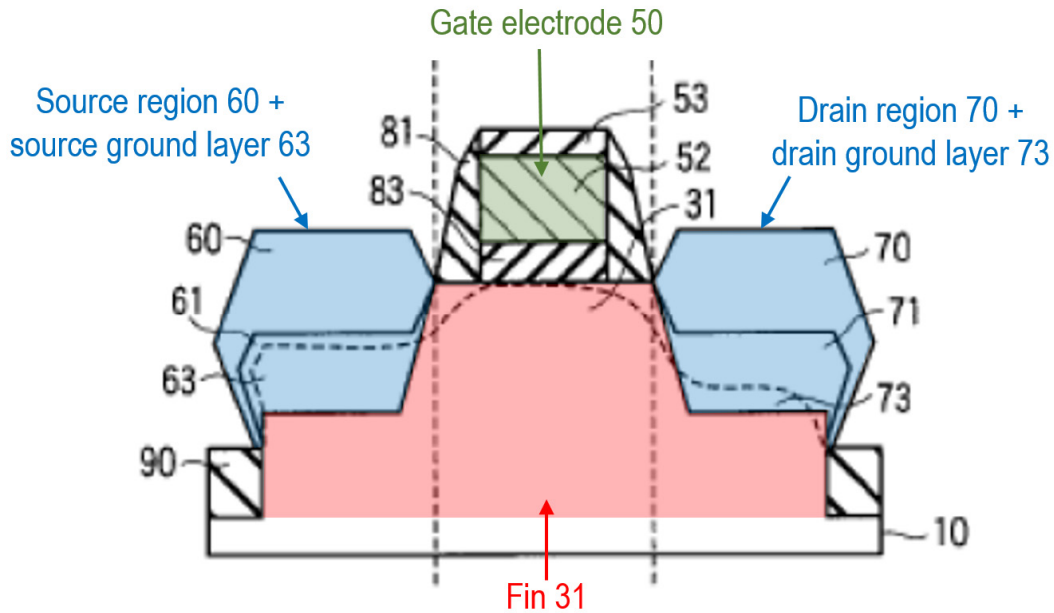
Petitioner is not conceding that the Challenged Claims satisfy all statutory requirements including those under 35 U.S.C. § 112.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. [GROUND 1A] – Obviousness based on Tezuka and Tung (Claims 1, 4-6, 9-10)

1. Overview of Tezuka

Tezuka generally describes “a field effect transistor that can reduce leakage current when a strained channel is used, suppress the occurrence of defects, and improve the yield.” SAMSUNG-1005, [0005]; *see also id.*, [0006]-[0010], [0117]-[0143]; SAMSUNG-1003, ¶50; *see also id.*, ¶¶51-53. Figure 8 depicts the structure of Tezuka's FinFET embodiment:



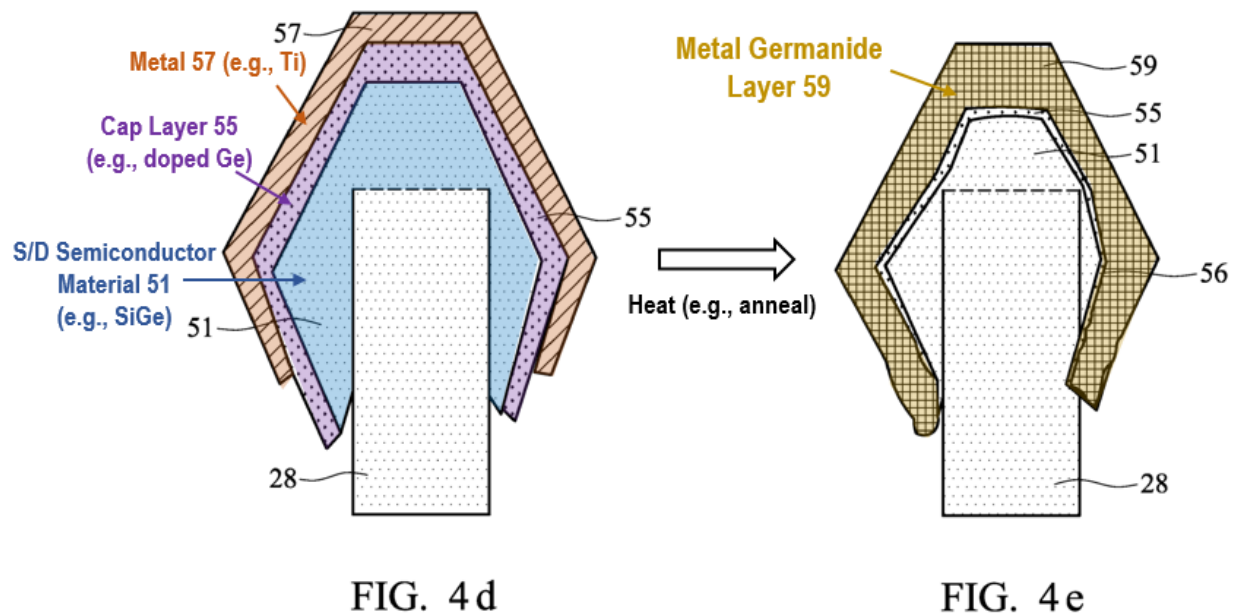
Tezuka, FIG. 8(b) (annotated)

Tezuka further teaches that “[a] metal compound layer (NiGeSi or the like) ... may be formed on the surfaces of the source/drain regions 60 and 70.” SAMSUNG-1005, [0170]; *see also id.*, [0066] (“Ni and Ge are reached by heat treatment to form the source/drain electrodes 65 and 75 made of NiGe germanide”), [0039], [0054], [0089].

2. Overview of Tung

Tung describes techniques for forming non-planar FETs (e.g., FinFETs) with improved contacts to the source and drain regions. SAMSUNG-1006, [0005]-[0006], [0019]-[0021]. Tung’s process involves forming a doped semiconductor cap layer 55 over an outer surface of a semiconductor material 51 of the source or

drain region, depositing a metal 57 such as titanium over the cap layer 55, and annealing the metal 57 over the cap layer 55 to form a metal silicide or germanide layer 59. *Id.*, [0043]-[0045]. The cap layer 55 can be a doped germanium layer, and the resulting germanide layer 59 provides a contact structure to the source or drain region with a low contact resistance and reduced Schottky barrier height. *Id.*, [0058], [0078]; SAMSUNG-1003, ¶54.



Tung, FIGS. 4d-4e (annotated)

3. Obviousness Analysis

As discussed in further detail below, it would have been obvious in view of Tung to form Tezuka's metal compound layers as germanide layers (1) using titanium and (2) from a germanium cap layer like Tung's semiconductor layer 55. SAMSUNG-1003, ¶58-59.

Tezuka-Tung: Metal Compound Layer Having Titanium

Tezuka describes a “metal compound layer” that is formed over the source and drain layers 60/70 of a FinFET, where the metal compound layer includes “Ni-GeSi or the like.” SAMSUNG-1005, [0120]. While NiGeSi is identified as one suitable compound, it would have been obvious that any number of common germanide or silicide materials formed from different metals could be used in Tezuka’s metal compound layers to form contacts to the source and drain regions. SAMSUNG-1003, ¶60; *see also id.*, ¶¶60-65. Tung, for instance, teaches that “Ni, Pd, Pt, Pa, Co, Ti, Al, Au, Lanthanoids ..., or combinations thereof” all would have been suitable to form a metal silicide or germanide layer 59 over the source and drain regions of a non-planar FET. SAMSUNG-1006, [0042], [0061], [0080], Abstract. Relevant to the claims of the ’178 Patent, Tung identifies titanium (Ti) as one such metal that would be suitable for forming metal compound layers like Tezuka’s. *Infra*, [1g], [11]. It would have been obvious to select titanium for the metal compound layers in Tezuka’s FinFET, and multiple reasons would have prompted a POSITA to do so. SAMSUNG-1003, ¶60.

First, Tezuka specifically notes that compounds other than NiGeSi would be suitable for use in the metal compound layer, and Tezuka leaves the selection of a particular compound to the discretion of a POSITA. SAMSUNG-1005, [0015] (“a

metal compound layer (NiGeSi **or the like**)”), [0053], [0089], [0120]. Tung’s disclosure of additional metals indicates that the selection of any one of them, including titanium, would have amounted to a non-innovative design choice, i.e., a routine and predictable choice that a POSITA would have made to optimize one or more well-known properties of the transistor or fabrication process that depend at least in part on the selection of a particular metal (e.g., properties related to Schottky barrier height, contact resistivity, and/or reactivity of the metal compound). SAMSUNG-1003, ¶61.

Second, titanium would have been obvious to use in forming Tezuka’s metal compound layer to enjoy the benefit of various well-known characteristics of titanium-based contacts. SAMSUNG-1003, ¶62. Titanium-based contacts were commonly used before the ’178 Patent, owing, among other things, to their low resistivity, high chemical reactivity, and capability of forming compounds with lower Schottky barrier heights. *Id.* Titanium was also known to promote formation of low-leakage junctions, which also would have led a POSITA toward the use of titanium in the resulting device of the Tezuka-Tung combination. *Id.*

Third, the use of titanium in the metal compound layer of the Tezuka-Tung device would have amounted to a simple substitution of nickel as taught in Tezuka with titanium as taught in Tung to produce predictable results (i.e., a metal compound layer based on titanium, germanium, and silicon). SAMSUNG-1003, ¶63.

A POSITA likewise would have been led to select titanium as a matter of routine experimentation and optimization (e.g., as part of experimentation to select a metal that would facilitate formation of a germanide layer with a suitably low contact resistance and Schottky barrier height). *Id.*

Fourth, the use of titanium in the metal compound layer of the Tezuka-Tung combination would have amounted to no more than an obvious use of a known technique (e.g., a titanium-based metal compound layer for source/drain contacts in a FinFET) to improve a similar device (e.g., Tezuka's FinFET) in substantially the same way as taught in Tung. SAMSUNG-1003, ¶64.

A POSITA would have had a reasonable expectation of success forming a metal compound layer that includes titanium. This is particularly evident from the popularity of titanium in silicides and germanides before the '178 Patent, and is further underscored by the '178 Patent's own identification of titanium as an "industry standard" contact metal. SAMSUNG-1001, 2:49-56; SAMSUNG-1003, ¶65.

Tezuka-Tung: Metal Compound Layers Formed from Germanium Cap Layers

Tezuka does not describe in detail how to form its metal compound layers over the source and drain regions of the FinFET, but Tung nonetheless focuses on

techniques for forming analogous layers (referred to in Tung as “metal silicide layers 59”¹) by annealing metal with a doped germanium cap layer (referred to in Tung as “semiconductor layer 55”). *Supra*, Section IV.A.2; SAMSUNG-1005, [0120]. For example, Tung’s process involves growing cap layer 55 over an outer surface of a semiconductor material 51 of source and drain regions 39, depositing a metal 57 over the cap layer 55, and annealing the resulting structure to form a germanide layer 59 over the source and drain regions 39. SAMSUNG-1006, [0078]-[0082], [0039]-[0045], FIGS. 4, 13-16.

A POSITA would have found it obvious to form Tezuka’s metal compound layer by annealing a metal including titanium with a doped germanium cap layer formed over at least a portion of the source and drain regions as taught in Tung,

¹ Tung’s generically labeled “silicide” layer 59 would have been understood to be a “germanide” layer at least when it is formed by annealing a metal such as titanium over a **germanium** cap layer 55 composed of “doped Ge” or “doped SiGe” formed predominantly of germanium (e.g., in excess of 90% Ge). SAMSUNG-1006, [0058], [0078]; SAMSUNG-1001, 9:34-42, 10:43-50, 12:21-27, 16:14-17; SAMSUNG-1003, ¶91, FN18. By contrast, for example, a layer formed by annealing metal with pure silicon would be understood to be a silicide rather than a germanide. SAMSUNG-1003, ¶91, FN18; *see also id.*, ¶62, FN2, ¶95, ¶173.

and multiple reasons would have prompted a POSITA to integrate these teachings in the Tezuka-Tung combination. SAMSUNG-1003, ¶67; *see also id.*, ¶¶66, 68-70.

To start, for example, a POSITA would have sought to form Tezuka's metal compound layer using a germanium cap layer to realize the benefits of such techniques as expressly taught in Tung. SAMSUNG-1003, ¶67. These include reducing the Schottky barrier height and lowering contact resistance between the resulting germanide layer and the source and drain regions. SAMSUNG-1006, [0034] ("The metal silicide layer 59 comprises a suitable metal silicide to lower the Schottky barrier height of the majority carriers. ...The Schottky barrier height between the doped semiconductor layer 55 and the metal silicide layer 59 determines the source/drain series resistance of the transistor" and "the doped semiconductor layer 55 is heavily doped so as to minimize this resistance."); *see also id.*, [0005]-[0006], [0032]; SAMSUNG-1003, ¶¶67-68.

According to Tung, "the low Schottky barrier height at the source of the transistor and the ultra-shallow junction depths ... achievable with metal silicides significantly improve[s] short channel effects of the transistor." SAMSUNG-1006, [0031]. A POSITA would have known that various properties of germanium render it favorable to silicon in certain respects, e.g., including germanium's higher carrier mobilities and lower resistivity; accordingly, a germanium cap layer would

have been obvious and beneficial to use in forming metal compound layers over the source and drain regions of Tezuka's FinFET as germanide layers. SAMSUNG-1003, ¶68. The use of such a germanium cap layer would have allowed the FinFET in the Tezuka-Tung combination to more fully obtain the benefits of Ge's intrinsically favorable properties as a result of its high content in the cap layer—even if the Ge content in the SiGe source/drain regions is significantly lower than the Ge content in the cap layer as permitted in various embodiments in Tezuka (e.g., Tezuka's teachings encompasses Ge in excess of 50% by even a small amount in the source/drain layers 60/70). SAMSUNG-1005, [0140] ("Ge composition range of 50% to 90%"); SAMSUNG-1003, ¶68.

Further, based on Tung, it would have been obvious to use a cap layer in forming Tezuka's metal compound layer so as to increase the uniformity of dopants at or near an interface to the metal from which the germanide layer is formed, as well as to reduce "residual defects that may result in poor silicide formation or result in leakage currents" that can otherwise result when implanting dopants for contact formation directly into the source/drain regions rather than in a germanium cap layer. SAMSUNG-1006, [0005], [0020] ("The use of epitaxial process prevents nucleation effects. Further, a uniformly controlled doping is achievable even in non-planar structures."); SAMSUNG-1003, ¶69.

Moreover, the use of a doped germanium cap in the FinFET of the resulting

combination would have amounted to a merely obvious use of a known technique as taught in Tung to improve a similar device (e.g., Tezuka's FinFET) to yield no more than predictable results. SAMSUNG-1003, ¶70. Here, "when a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

A POSITA would have had a reasonable expectation of success implementing the combination in light of the similar types of devices described in Tezuka and Tung. SAMSUNG-1003, ¶65 and ¶70. Notably, Tezuka and Tung each describe techniques for forming metal compound layers over the source/drain regions of non-planar devices (e.g., FinFETs), and Tung expressly teaches that the doped germanium-cap layer can be formed over an epitaxially grown SiGe source/drain region (e.g., SiGe material 51 of source/drain regions 39) analogous to the upper source/drain layers 60/70 of Tezuka's device. SAMSUNG-1006, [0040], [0058], [0074], [0078]. Tung also expressly confirms that a POSITA would have known how to apply its techniques across a range of devices and integrated circuit structures. SAMSUNG-1006, [0019]-[0020], [0083]-[0084]. In this context, implementing the combination would have been within the skill of a POSITA, and a POSITA would have had a reasonable expectation of success. SAMSUNG-1003,

¶70.

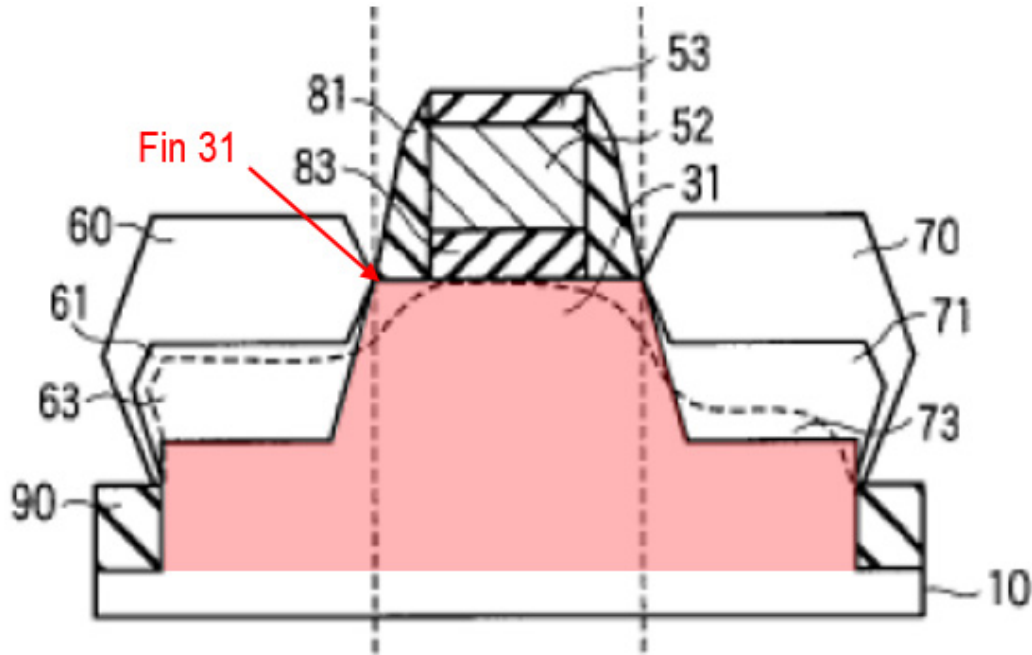
The Tezuka-Tung combination would have rendered obvious each of claims 1, 4-6, and 9-10 for the reasons described below. SAMSUNG-1003, ¶¶71-73; *see also id.*, ¶¶74-110.

Element [1pre]

To the extent the preamble is a limitation, the Tezuka-Tung combination would have rendered obvious [1pre]. SAMSUNG-1003, ¶73. Tezuka describes a fin-type field effect transistor 400, which a POSITA would have understood to be a type of component commonly used in integrated circuits. SAMSUNG-1005, [0117]-[0143], FIG. 8; *generally id.*, FIGS. 8-17; SAMSUNG-1003, ¶73. In one example, Tezuka teaches that “the fin-type field effect transistor is a strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction).” SAMSUNG-1005, [0138].

Element [1a]

The Tezuka-Tung combination would have rendered obvious [1a], e.g., in view of Tezuka’s disclosure of a fin 31 in transistor 400. SAMSUNG-1005, [0118]-[0119], [0139]; SAMSUNG-1003, ¶74. According to Tezuka, “fin 31 and the channel region are made of n-type Si.” SAMSUNG-1005, [0139]; *see also id.*, [0150].



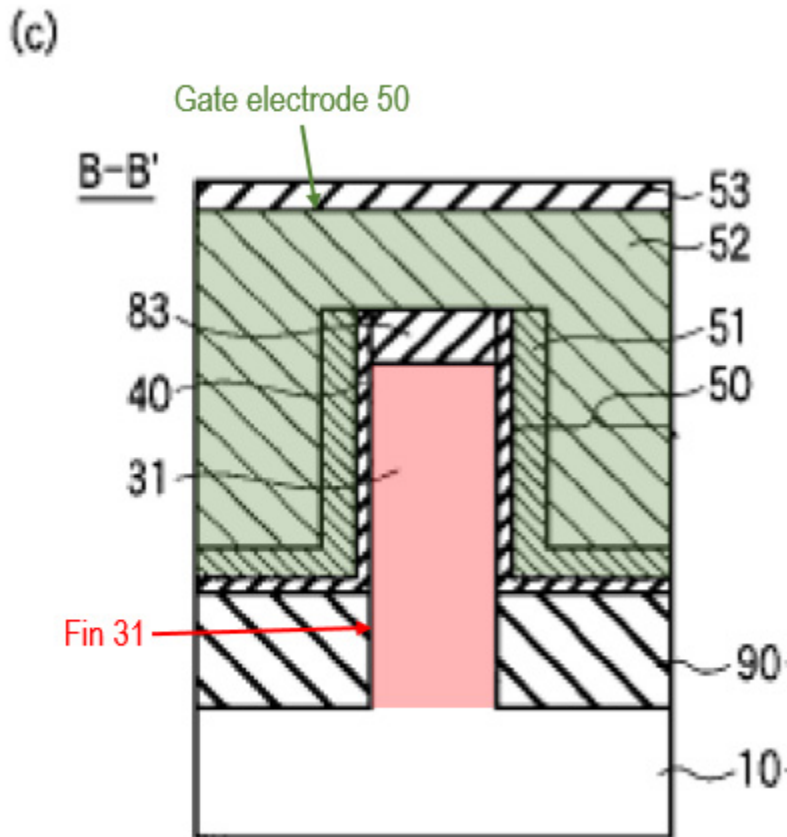
Tezuka, FIG. 8b (annotated)

Further, as described below in reference to feature [1c], and consistent with common usage of the term “fin” in the field before the ’178 Patent (and with how the term “fin” is used in the Challenged Claims), a POSITA would have understood Tezuka’s fin to include not only the indicated portion of silicon beneath the gate, but also the epitaxially-formed source and drain regions. *Infra*, [1c]; SAM-SUNG-1003, ¶75.

Element [1b]

The Tezuka-Tung combination would have rendered obvious [1b] based on Tezuka’s disclosure of a gate electrode over the fin, e.g., the gate electrode 50 of

the transistor 400 disposed over the fin 31.² SAMSUNG-1003, ¶76. Tezuka discloses that “[a] gate electrode 50 is formed on both side surfaces of the upper portion of the fin 31 with a gate insulating film 40 interposed therebetween.” SAMSUNG-1005, [0118]; *see also id.*, [0127], [0139].

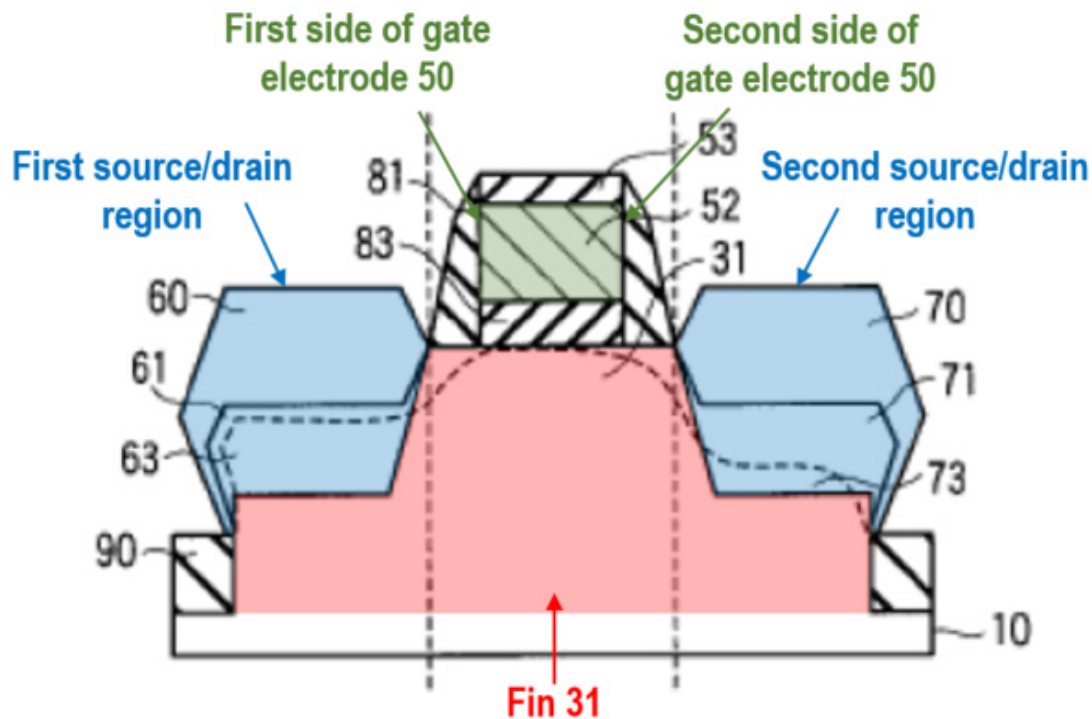


Tezuka, FIG. 8c (annotated)

² In the alternative, Tezuka’s poly-SiGe film 52 would have rendered obvious the claimed “gate electrode.” SAMSUNG-1005, [0123]; SAMSUNG-1003, ¶76, FN7; *see also id.*, ¶¶96-97.

Elements [1c], [1h]

The Tezuka-Tung combination would have rendered obvious [1c]/[1h], e.g., in view of Tezuka's disclosure of a first source or drain region comprising, collectively, source ground layer 63 and upper layer 60, and a second source or drain region comprising, collectively, drain ground layer 73 and upper layer 70. SAMSUNG-1003, ¶77; *see also id.*, ¶¶78-80, ¶¶96-97.



Tezuka, FIG. 8b (annotated)

Tezuka explains that source/drain ground layers 63/73 are epitaxially grown in etched recesses 82 on either side of fin 31, and upper source/drain layers 60/70 are epitaxially grown over layers 63/73. SAMSUNG-1005, [0135]-[0136], FIGS. 16-17; *see also id.*, [0120]-[0121], [0139]-[0140]. Upper layers 60 and 70 are

doped oppositely from fin 31 and the channel region, and thus provide a source and drain for charge carriers conducted across the channel. *Id.*, [0139]; SAMSUNG-1003, ¶78. Furthermore, source/drain ground layers 63/73 are formed within the same recesses 82 as source/drain upper layers 60/70, and ground layers 63/73 are each within a same respective source or drain “**region**” as upper layers 60/70. SAMSUNG-1003, ¶78. This understanding is consistent with Tezuka’s identification of both layers 60/63 as respective “**source**” components and Tezuka’s identification of both layers 70/73 as respective “**drain**” components. *Id.* It is further consistent with descriptions of the source and drain regions in the ’178 Patent. *Id.*; SAMSUNG-1001, 8:60-66.

Tezuka’s source region 60/63 abuts a first source/drain sidewall of Tezuka’s fin 31 proximate a first side of the gate electrode 50, while Tezuka’s drain region 70/73 abuts a second source/drain sidewall of Tezuka’s fin 31 proximate an opposite side of the gate electrode 50. SAMSUNG-1005, FIG. 8(b). A POSITA would have understood and it would have been obvious that the source/drain regions in the Tezuka-Tung combination are “in the fin” according to a common understanding of epitaxially grown source/drain regions in FinFET devices as being part of or “in” the fin. SAMSUNG-1003, ¶79. The ’178 Patent embraces a similar view, which is apparent in light of the specification’s disclosure of epitaxially grown source/drain regions 631 formed on opposite source/drain sidewalls of a channel

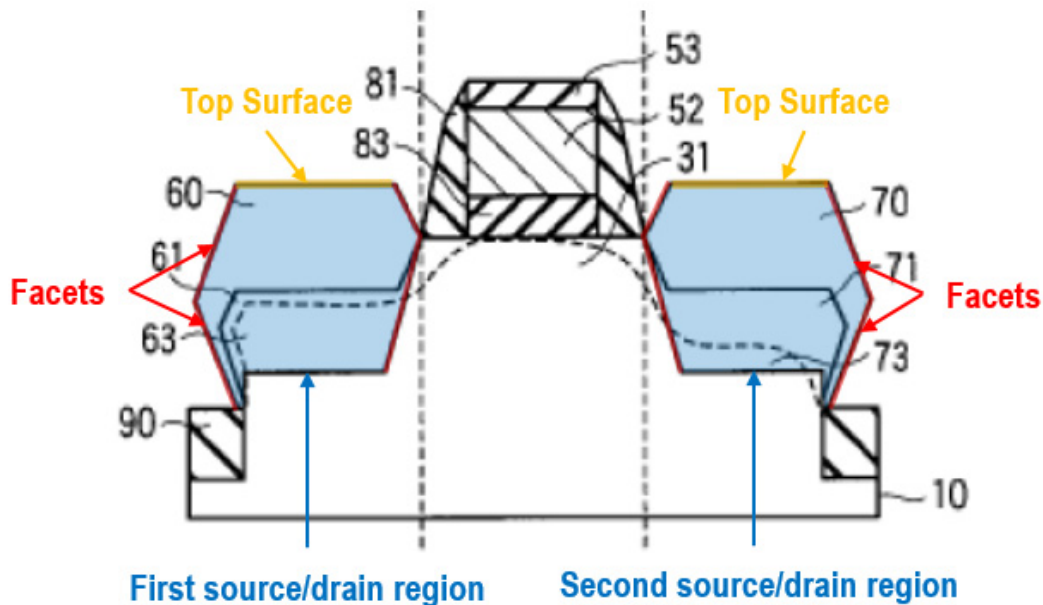
body or fin 660. SAMSUNG-1001, 13:22-50, FIG. 6; *see also* SAMSUNG-1013, 32 (applicant's claims in a counterpart EP application refer to a "first source or drain region **in** the fin" that "compris[es] an epitaxial region (631) ... **formed on** ... one fin sidewall"); SAMSUNG-1003, ¶79. For the epitaxially grown source/drain regions 631 to be "in the fin," it would have been obvious that the claimed "fin" is not limited to a structure in the channel region like fin 660. *Id.* The claimed "fin" would instead encompass epitaxially grown source/drain regions like Tezuka's source region 60/63 and drain region 70/73. *Id.* Tezuka reinforces the obviousness of forming first and second source or drain regions "in the fin" by virtue of growing the source region 60/63 and drain region 70/73 in a recess 82 of fin 31. SAMSUNG-1003, [0119], [0135]-[0136]; SAMSUNG-1003, ¶79.

The '178 Patent does not define any bounds for the term "proximate," but under any reasonable interpretation, it would have been obvious that Tezuka's source region 60/63 is proximate a first side of the gate electrode 50 and Tezuka's drain region 70/73 is proximate a second side of the gate electrode 50 opposite the first side. SAMSUNG-1003, ¶80. Indeed, much as FIG. 6 of the '178 Patent shows the epitaxial source/drain regions 631 extending from opposing sidewalls of a fin structure 660 on opposite sides of a gate electrode 640, Tezuka's source and drain regions similarly extend from opposing source/drain sidewalls of fin 31 on opposite sides of a gate electrode 50, rendering the source and drain regions 60/63

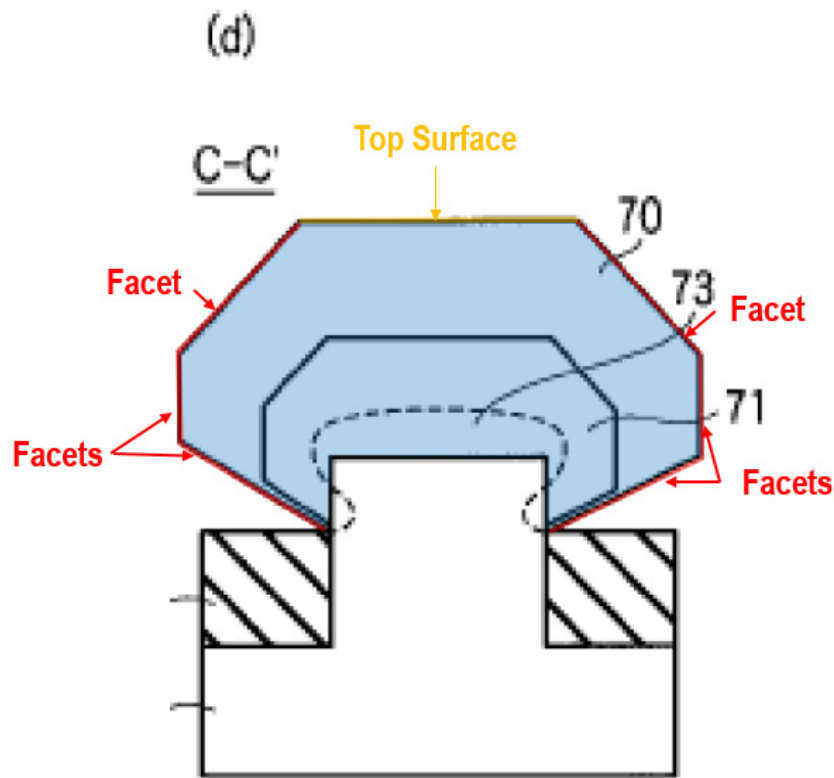
and 70/73 very near and close to the first and second sides of the gate electrode 50 respectively. *Cf.* SAMSUNG-1001, FIG. 6; SAMSUNG-1005, FIGS. 8(a)-(d).

Elements [1d], [1i]

The Tezuka-Tung combination would have rendered obvious [1d]/[1i], e.g., in view of Tezuka's disclosure of at least two facets and a top surface at each of source region 60/63 and drain region 70/73. SAMSUNG-1005, [0136], [0118]-[0121], FIGS. 8, 17; *supra*, [1c]; Section II.B; SAMSUNG-1003, ¶81; *see also id.*, ¶¶96-97.



Tezuka, FIG. 8b (annotated)



Tezuka, FIG. 8d (annotated)

Elements [1e], [1j]

The Tezuka-Tung combination would have rendered obvious [1e]/[1j], e.g., in view of Tezuka’s disclosure that source region 60/63 and drain region 70/73 each comprise alloys of silicon and germanium. SAMSUNG-1005, [0139] (“source ground layer 63 and the drain ground layer 73 are made of n-type $\text{Si}_{0.95}\text{Ge}_{0.05}$ ”), [0140] (upper source/drain layers 60/70 “have a preferable Ge composition range of 50% to 90%”), [0139] (upper source/drain layers 60/70 can be “ $\text{Si}_{0.7}\text{Ge}_{0.3}$ ”); *see also id.*, [0119]-[0121], [0135]-[0136], [0123]-[0124]; SAMSUNG-1003, ¶82; *see also id.*, ¶¶96-97.

Elements [1f], [1k]

The Tezuka-Tung combination would have rendered obvious [1f]/[1k], e.g., in view of Tezuka's description of source region 60/63 and drain region 70/73 each having germanium graded to a concentration in excess of 50%. SAMSUNG-1003, ¶¶83-84; *see also id.*, ¶¶96-97. According to Tezuka, the source/drain ground layers 63/73 are formed from SiGe material having a lower concentration of Ge than the SiGe material of source/drain upper layers 60/70. For example, the Ge concentration in upper layers 60/70 is preferably as high as 90% (i.e., "in excess of 50%"). SAMSUNG-1005, [0140] ("source/drain regions 60 and 70 have a preferable Ge composition range of 50% to 90% ... from the viewpoint of generating as large a stress as possible while avoiding stress reduction due to plastic deformation"); *see also id.*, [0020], [0059], [0076], [0093], [0119], [0135]-[0136], [0139], [0123]-[0124]; SAMSUNG-1003, ¶83. The Ge concentration in ground layers 63/73 is lower than upper layers 60/70, e.g., " $\text{Si}_{0.95}\text{Ge}_{0.05}$ ", but in any event is calibrated to a level designed to prevent "dislocations [from] occur[ring] between the ground layers 63 and 73 and the substrate 10" while also supporting the higher Ge concentration in upper layers 60/70. *Id.*, [0139]-[0140]; *see also id.*, [0119] ("source region 60 and a drain region 70 made of an alloy semiconductor that ... has a composition ratio different from that of ... the ground layers 63 and 73, and has a different lattice constant"), [0120]-[0121]. Tezuka thus discloses and

renders [1f]/[1k] obvious based at least on bilayer grading between ground layers 60/63 and upper layers 70/73. *Id.*

Further, a POSITA would have known and it would have been obvious to implement additional stepped or continuous grading of the Ge concentration within each of upper layers 60/70 and/or ground layers 63/73. SAMSUNG-1003, ¶84. Graded epitaxial growth was a common and well-known technique before the '178 Patent, and a POSITA would have known that further grading within layers 60/70 and/or 63/73 would have been beneficial to enable growth of thicker crystalline films for layers 60/70 and/or 63/73 that have increasingly higher Ge concentrations while reducing the risk of growth defects, misfit dislocations, and plastic deformation. SAMSUNG-1003, ¶83. The high Ge concentrations, thicker films, and larger growth areas that could be achieved through additional grading would have motivated a POSITA to implement further grading within each of layers 60/70 and/or layers 63/73 to reduce leakage currents, improve yield, and increase stress (e.g., compressive strain) applied to the channel region (thereby increasing the mobility of charge carriers and conductivity in the channel region). SAMSUNG-1005, [0140]; SAMSUNG-1003, ¶84; *infra*, Ground 1B at Claims [1], [6].

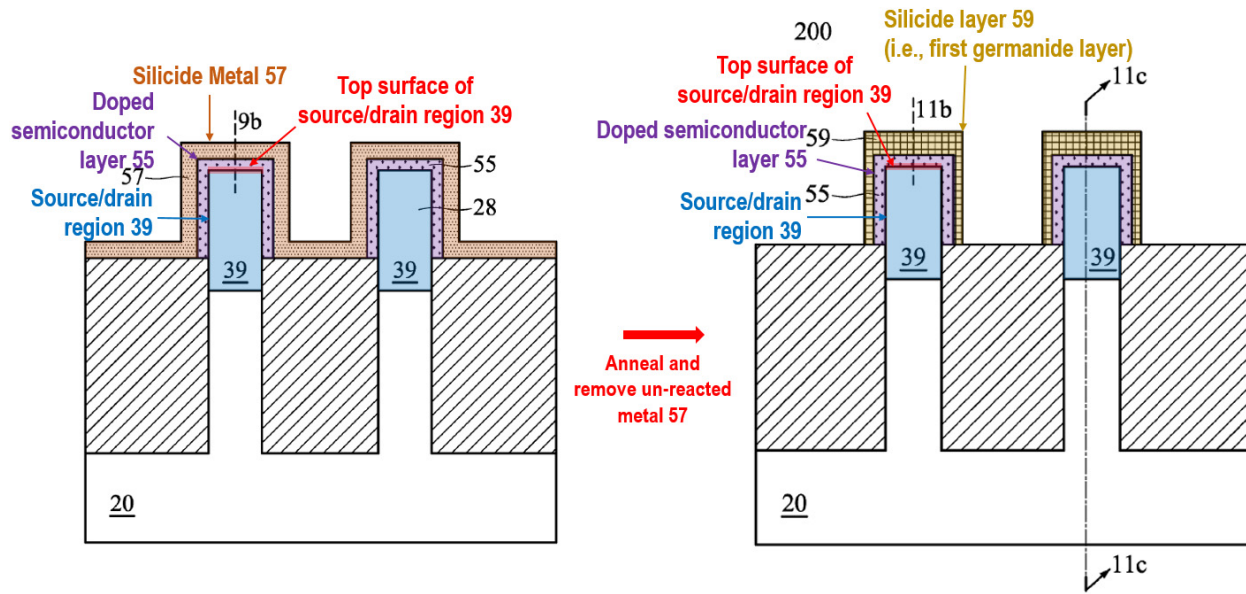
Elements [1g], [11]

The Tezuka-Tung combination would have rendered obvious [1g]/[11] based on the teachings of Tezuka in view of Tung. SAMSUNG-1003, ¶¶85-95; *see also*

id., ¶¶96-97.

Tezuka discloses that “[a] metal compound layer (NiGeSi or the like) ... may be formed on the surface of the source / drain regions 60 and 70.” SAMSUNG-1005, [0120]. Tezuka’s metal compound layers provide contacts or electrodes to the source and drain regions. SAMSUNG-1005, [0066] (“source/drain **electrodes** 65 and 75 made of NiGe **germanide**”), FIGS. 5(e)-(f); SAMSUNG-1003, ¶86.

To the extent Tezuka does not specifically teach that the metal compound layer is formed over respective **top** surfaces of the source and drain layers 60/70, a POSITA would have found it obvious to do so based on Tung. SAMSUNG-1003, ¶87. As shown in FIGS. 9a and 11a, Tung’s metal 57 and doped semiconductor layer 55 are deposited around all sides of each source/drain region 39, including over a top surface of the source/drain region 39. SAMSUNG-1006, FIGS. 9a, 11a, [0059]-[0065]; *see also id.*, [0039]-[0045], FIGS. 4a-4d. As a result, a germanide layer 59 is formed around all sides of the source/drain region 39, including the top surface:

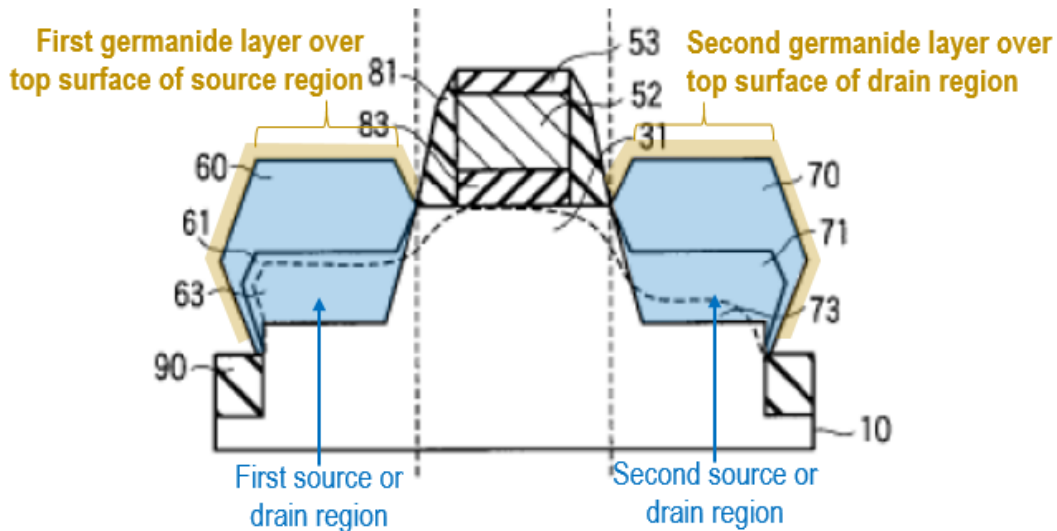


Tung, FIGS. 9a (left, annotated), 11a (right, annotated)

See also SAMSUNG-1006, FIGS. 4a-4e, 15-16.

In the combination, it would have been obvious based on Tung to form each of Tezuka's metal compound layers over at least the respective top surface of the source and drain layers 60 and 70 (e.g., over the top surface and all sides of the source and drain regions), similar to Tung's germanide layer 59, as illustrated below.³ SAMSUNG-1003, ¶88.

³ Although Tung's FIG. 11a (and others such as FIGS. 4c-4e) show a portion of layer 55 that remains after annealing, in other embodiments, "all of the doped semiconductor layer 55 may be consumed" leaving the germanide layer 59 in direct contact with an outer surface of the SiGe material 51 of the source/drain regions. SAMSUNG-1006, [0045], [0081].



Tezuka, FIG. 8(b) (annotated)

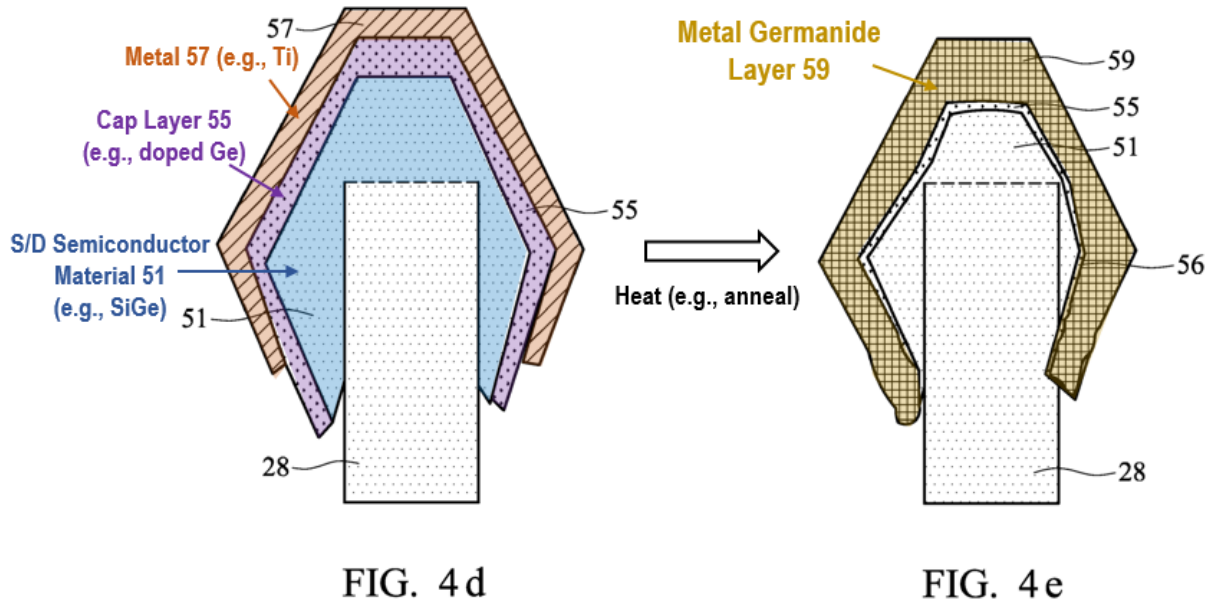
It would have been obvious and a POSITA would have been motivated to form Tezuka's metal compound layers (i.e., germanide layers) over the **top surfaces** of the source and drain regions to align the germanide layers with the location of contact plugs that are ordinarily formed above the source and drain regions in an integrated circuit so as to electrically couple the source and drain regions to other components through one or more layers of interconnect wiring formed above the FET. SAMSUNG-1003, ¶89. The top surfaces of Tezuka's source and drain regions would also provide the widest surfaces of the source and drain regions when viewed from the top of the FET, and therefore, forming germanide layers over the top surfaces would have been useful to increase the contact surface area and thereby reduce contact resistance. *Id.*

Tezuka discloses that its metal compound layers can include "NiGeSi or the

like.” SAMSUNG-1005, [120]. To the extent Tezuka does not expressly disclose titanium in the metal compound layers, Tung discloses titanium as a suitable metal for use in forming metal compound layers over the source/drain regions of devices such as non-planar FETs. SAMSUNG-1006, [0042], [0061], [0080], Abstract. It would have been obvious and a POSITA would have been motivated to use titanium in forming the metal compound layers (i.e., germanide layers) of the FinFET in the Tezuka-Tung combination for the reasons described above in the overview of the combination. *Supra*, Section IV.A.3; SAMSUNG-1003, ¶90.

Tung further describes techniques for forming a germanide layer 59⁴ over a source or drain region of a FinFET by annealing a metal such as titanium with a doped germanium cap layer 55 over SiGe material 51 of the source and drain regions. SAMSUNG-1006, [0078]-[0082], [0039]-[0045], FIGS. 4(b)-(e), 13-16.

⁴ *Supra*, Footnote 1.



Tung, FIGS. 4d-4e (annotated)

For the reasons described above in the overview of the Tezuka-Tung combination, it would have been obvious and a POSITA would have been motivated to form Tezuka's metal compound layers as germanide layers based on Tung's process—e.g., by growing a doped germanium cap layer 55 over SiGe source and drain layers 60/70, depositing a metal such as titanium over cap layer 55, and annealing titanium over cap layer 55. *Supra*, Section IV.A.3; SAMSUNG-1003, ¶91. In this context, the metal compound layers (i.e., germanide layers) in the Tezuka-Tung combination would each predictably include titanium, silicon, and germanium. SAMSUNG-1003, ¶91. Titanium would be present in the metal compound layers as a result of its deposition over cap layers 55, germanium would be present at least from the doped germanium cap layers 55, and silicon would be present

from the cap layers 55 (which can further include a small amount of silicon in addition to germanium) and/or from the underlying silicon-germanium material of source and drain layers 60/70. *Id.* A POSITA would have known that annealing metal with semiconductor material causes the constituent elements to mix and chemically react to form a metal compound (e.g., a germanide layer). *Id.*

More specifically, as to the presence of silicon in the metal compound layers (germanide layers) of the FinFET in the Tezuka-Tung combination, this feature would have been obvious in several ways. SAMSUNG-1003, ¶¶92-95. In a first example, Tung teaches that the cap layer 55 can be formed from “doped Ge,” and further that germanide layer 59 is formed by annealing a metal (e.g., titanium) over cap layer 55 until the interface of germanide layer 59 extends some amount into SiGe material 51 of the source/drain region 39.⁵ SAMSUNG-1006, [0045] (“the silicide interface moves beyond the doped semiconductor layer 55 and into the semiconductor material 51”), [0081]; SAMSUNG-1003, ¶93. Consistent with

⁵ Patent Owner’s infringement charts in the co-pending ITC proceeding similarly appear to identify structures allegedly constituting germanide layers that extend at least partially beneath the top surfaces of or within the indicated source and drain regions. *See* SAMSUNG-1014, 8-10 (depicting alleged germanide layers extending into S/D regions).

these teachings, in the combination, the metal compound layers that would result from annealing would include silicon originating from the SiGe material of the source/drain layers 60/70 (and would further include germanium and titanium as described above). SAMSUNG-1006, [0058], [0078]; SAMSUNG-1003, ¶93.

In a second example, Tung teaches that “all of the doped semiconductor layer 55 may be consumed by the silicidation process” when annealed. SAMSUNG-1006, [0045]. When all of cap layer 55 is consumed without the interface of the resulting germanide layer 59 extending into the source/drain regions themselves (e.g., without extending into source/drain layers 60/70 of the Tezuka-Tung FinFET), the lower surface of germanide layer 59 would contact the respective outer surfaces of source/drain layers 60/70. In this case, it would have been obvious that at least some silicon near the outer surfaces of the source/drain layers 60/70 that contact the germanide layers 59 (metal compound layers) would migrate into the metal compound layers due to the attraction of silicon from the source/drain layers 60/70 to metal or other elements or compounds in the metal compound layer. SAMSUNG-1003, ¶94. Here again, germanide layers 59 in the combination would include titanium, germanium, and silicon (even when cap layer 59 is formed from doped Ge). *Id.*

In a third example, it would have been obvious for the germanium cap layer 55 itself to include a small amount of silicon such that the metal compound layers

formed by annealing titanium with the cap layer 55 would naturally include silicon along with titanium and germanium, regardless of whether cap layer 55 is entirely consumed by annealing. SAMSUNG-1003, ¶95. Indeed, Tung not only teaches that cap layer 55 can be “doped Ge,” but further teaches that cap layer 55 can include “doped SiGe” material. SAMSUNG-1006, [0058], [0078]. Given that both doped Ge and doped SiGe are identified in Tung as suitable materials for cap layer 55, it would have been obvious to select a material for cap layer 55 formed predominantly of Ge (e.g., in excess of 90% Ge) to make beneficial use of well-known intrinsically favorable properties of Ge (e.g., a lower band gap and Schottky barrier height that would tend to yield lower contact resistance to the source/drain regions) while still making beneficial use of Si (e.g., to lower the gap in Ge content and reduce mislocations at the interface of the resulting germanide layer 59 and the source/drain regions). SAMSUNG-1003, ¶95. At minimum, it was known before the Critical Date that a wide range of concentrations of Ge in cap layers were suitable for forming contact structures to source/drain regions, and it would have been obvious to select a high concentration of Ge (e.g., in excess of 90%) to optimally reduce contact resistance and dislocations/defects in the contact structures to the source/drain regions. SAMSUNG-1003, ¶95.

Claim [4]

The Tezuka-Tung combination would have rendered obvious the additional

features recited in [4], e.g., in view of Tezuka's teachings. SAMSUNG-1003, ¶¶98-99.

For example, Tezuka discloses that “source region 60 and a drain region 70 ... [have] a composition ratio different from that of the substrate 10 and the ground layers 63 and 73, and [have] a different lattice constant,” so that “[a] force is applied to the channel region of fin 31 by the source/drain regions 60 and 70.” SAMSUNG-1005, [0119]; *see also id.*, [0120]-[0121], [0138] (“strained Si-pMOSFET having compressive strain in the direction of hole conduction (channel length direction)”), [0140] (“the source/drain regions 60 and 70 have a preferable Ge composition range of 50% to 90%[] ... from the viewpoint of generating as large a stress as possible”), Claim 5 (FinFET in which “stress is applied to the channel region in the channel length direction”), FIG. 8 (showing channel in fin between first and second source/drain regions); *see also id.*, [0002]-[0003], [0005], [0031]-[0034], [0146], [0151], Claims 4-5 (“compressive strain”). SAMSUNG-1003, ¶99.

Claim [5]

The Tezuka-Tung combination would have rendered obvious the additional features recited in [5], e.g., in view of Tezuka's teachings that the first and second source or drain regions can be p-type. SAMSUNG-1005, [0138] (“strained Si-pMOSFET”), [0139] (“both source region 60 and the drain region 70 are ... doped with B as a p-type impurity at a high concentration”), [0143] (“B is used as the

source/drain impurity”); *see also id.*, [0032], [0039], [0046], [0145]; SAMSUNG-1003, ¶¶100-101.

Element [6pre]

Supra, [1pre]. SAMSUNG-1003, ¶¶102-104.

Element [6a]

Supra, [1a]. The Tezuka-Tung combination would have rendered obvious [6a], e.g., in view of Tezuka’s disclosure of a fin comprising silicon. *See supra*, [1a], [1c], [1h]. For example, just as the specification of the ’178 Patent identifies structure 660 alternately as a “body” or a “fin,” the same structures from the Tezuka-Tung combination that would have rendered obvious a “fin” would also have rendered obvious the recited “body” in Claim 6. *Cf.* SAMSUNG-1001, 13:24-27, FIG. 6; SAMSUNG-1003, ¶105.

Elements [6b]-[6l]

Supra, [1b]-[1l]. SAMSUNG-1003, ¶¶105-106.

Claim [9]

Supra, [4]. SAMSUNG-1003, ¶¶107-108.

Claim [10]

Supra, [5]. SAMSUNG-1003, ¶¶109-110.

B. [GROUND 1B] – Obviousness based on Tezuka, Tung, and Simonelli (Claims 1-10)

1. Overview of Simonelli

Simonelli generally describes “planar and three-dimensional complementary

metal oxide semiconductor (CMOS) devices comprising a compound layer with graded germanium content.” SAMSUNG-1008, [0001], Abstract; SAMSUNG-1003, ¶55. For example, Simonelli describes techniques for epitaxially growing source/drain regions in a multi-gate device (e.g., a FinFET) “using a graded high-germanium content silicon-germanium film stack 1400” like that illustrated in FIG. 14 (*see* [0051]-[0058]):

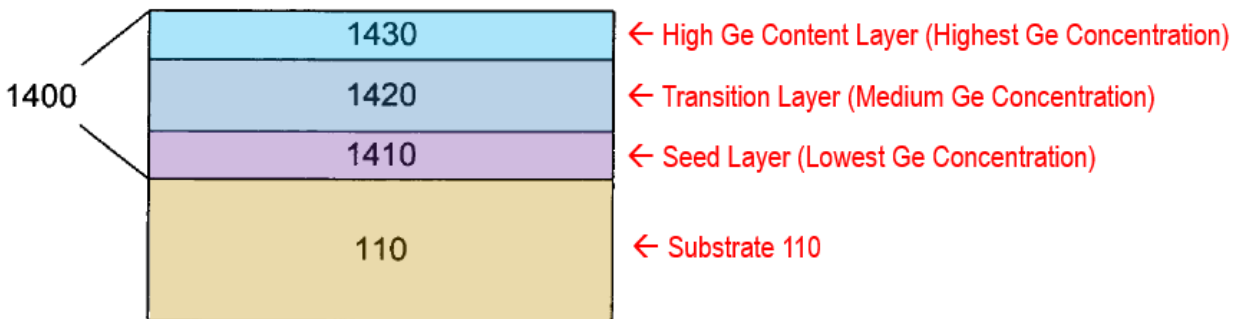


FIG. 14

Simonelli, FIG. 14 (annotated)

2. Obviousness Analysis

Claims [1], [6]

In Ground 1A, it was shown that the Tezuka-Tung combination would have rendered obvious independent claims 1 and 6 when Tezuka’s source layers 60/63 and drain layers 70/73 are respectively mapped to the claimed first and second source or drain regions. *Supra*, Ground 1A.

Here (Ground 1B), the first and second source or drain regions are alternatively mapped to Tezuka’s source (upper) region 60 and drain (upper) region 70,

respectively—i.e., without further inclusion of ground layers 63 and 73 in the mappings.⁶ SAMSUNG-1003, ¶¶111-114. Source and drain regions 60/70 are each comprised of SiGe with a “preferable Ge composition range of 50% to 90%” (i.e., in excess of 50%). SAMSUNG-1005, [0140].

Simonelli further teaches grading Ge content in the source and drain regions of a FinFET. SAMSUNG-1008, [0051], [0053]-[0058], FIGS. 14-15; *supra*, Section IV.B.1. It would have been obvious to modify Tezuka’s FinFET by grading the Ge content in each of the source and drain regions 60 and 70 based on Simonelli’s teachings, and a POSITA would have sought to introduce such grading in the source and drain regions 60 and 70 for at least the reasons that would have led

⁶ Ground 1B would have rendered obvious claims 1-10 under either or both mappings for the claimed first and second source or drain regions (i.e., layers 60/63 and 70/73 together or layers 60 and 70 alone). SAMSUNG-1003, ¶¶111-114. Both alternative mappings to the first and second source or drain regions are applied against each of claims 1-10 in Ground 1B. Apart from the addition of the alternative mapping for the first and second source or drain regions, the Tezuka-Tung-Simonelli combination would have disclosed or rendered obvious each of the other elements of claims 1 and 6 for substantially the same reasons addressed above in Ground 1A. *Id.*

a POSITA to introduce additional grading in Tezuka's device as discussed above with respect to [1f]/[1k] in Ground 1A. *Supra*, Ground 1A at [1f]/[1k]; SAMSUNG-1003, ¶¶83-84, ¶¶96-97.

A POSITA would have had a reasonable expectation of success grading the Ge content in Tezuka's source/drain regions 60/70, especially since the graded Ge would be applied to the Tezuka-Tung-Simonelli FinFET in substantially the same context described in Simonelli—i.e., in epitaxially grown SiGe source/drain regions of a non-planar multi-gate FET. *See* SAMSUNG-1008, [0051], [0053]-[0055], FIG. 12; SAMSUNG-1005, [0138]-[0143], [0136]. Tezuka also already employs Ge bilayer grading between ground layers 63/73 and upper layers 60/70 to obtain high Ge concentrations in the upper layers 60/70. SAMSUNG-1003, ¶¶ 84, 114.

Claim [2]

The Tezuka-Tung-Simonelli combination would have rendered obvious [2] based at least on the teachings of Tezuka and Simonelli. SAMSUNG-1003, ¶¶115-120.

Tezuka teaches that the first and second source and drain regions, and regions 60 and 70, can be “doped with B as a p-type impurity at a high concentration.” SAMSUNG-1005, [0139]; *see also id.*, [0032], [0039], [0065], [0102], [0145]; *supra*, Ground 1A, [1c], [1h]. To the extent that Tezuka and Tung do not

expressly disclose that the doped “boron concentration [is] greater than 1E20” this feature would have been obvious in the combination based on Simonelli. SAMSUNG-1003, ¶117.

For example, Simonelli describes a “multi-gate device 600” such as a tri-gate or dual-gate FinFET (similar to Tezuka’s transistor 400) having “epitaxially form[ed] source and drain regions 1210.” SAMSUNG-1008, [0051]; *see also id.*, [0045]-[0051], FIGS. 6-12. “The epitaxially formed source/drain regions 1210 may be formed using a graded high-germanium content silicon film stack 1400.” *Id.*, [0051]. In Simonelli’s film stack 1400, higher layers in the stack are formed with increasing concentrations of germanium and are doped with increasing concentrations of boron. *Id.*, [0053]-[0058], FIGS. 14-15. In each layer, however, and even including the “seed layer” with the lowest concentrations of germanium and boron, Simonelli describes a boron concentration in excess of 1×10^{20} atoms/cm³. *Id.*

Based on Simonelli, a POSITA would have found it obvious to dope Tezuka’s source and drain regions, including at least regions 60 and 70, with boron at a concentration greater than 1E20. SAMSUNG-1003, ¶119. It was common for source/drain regions in a FET to be doped with p-type impurities such as boron and the channel region between the source/drain regions to be doped oppositely with n-type impurities. SAMSUNG-1003, ¶119. Consistent with this approach, Tezuka

teaches that the source/drain regions 60/70 should be “doped with B as a p-type impurity at a high concentration” to form an “Si-pMOSFET.” SAMSUNG-1005, [0138]-[0140]. A POSITA would have looked to Simonelli’s teaching of a boron concentration greater than $1E20$ for further explanation of boron concentrations consistent with Tezuka’s instruction to dope with boron at a high concentration, particularly since Simonelli describes a similar FET. SAMSUNG-1003, ¶119. Higher boron content also would have promoted a lower contact resistance in electrodes formed by reacting a metal deposited over the boron-doped source/drain regions 60/70. *Id.*

A POSITA would have understood dopant concentrations in the source/drain regions of a FET like that in the Tezuka-Tung-Simonelli combination to be a result-effective variable impacting the conductivity, contact resistance, and ON-current of the transistor. SAMSUNG-1003, ¶120. Accordingly, it would have been obvious to apply Simonelli’s suggested boron doping to a concentration in excess of $1E20$ in the first and second source or drain regions so as to optimize the conductivity, contact resistance, and ON-current of the resulting device, which a POSITA would have arrived at through routine optimization and experimentation. *E.I. du Pont de Nemours & Co. v. Synvina C.V.*, 904 F.3d 996, 1006 (Fed. Cir. 2018) (“For decades, this court and its predecessor have recognized that ‘where the

general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.”) (quoting *In re Aller*, 220 F.2d 454, 456 (CCPA 1955)); *id.*, 1006 (“[a] prima facie case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art”) (quoting *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003)); MPEP §2144.05. A POSITA would have had a reasonable expectation of success implementing doping at a concentration in excess of $1\text{E}20$, particularly since Simonelli’s teaching is applied in the combination to a similar non-planar FET. SAMSUNG-1003, ¶120. The ’178 Patent discloses nothing critical or unexpected about doping the source/drain regions with boron to a concentration greater than $1\text{E}20$. *Id.*

Claim [3]

The Tezuka-Tung-Simonelli combination renders obvious claim 3. SAMSUNG-1003, ¶¶121-123. As discussed above with respect to claim 2, Tezuka teaches that a portion of the first and second source or drain regions (i.e., regions 60 and 70) can be “doped with B as a p-type impurity at a high concentration,” and it would have been obvious based on Simonelli for the boron concentration in regions 60 and 70 to be greater than $1\text{E}20$ (i.e., 1×10^{20} atoms/cm³). *Supra*, [2]; SAMSUNG-1005, [0139]. By contrast, Tezuka explains that the lower portions of the first and second source or drain regions (i.e., ground layers 63 and 73) are

made of an n-type SiGe alloy, and are not doped with boron like the upper portions of the first and second source or drain regions (i.e., regions 60 and 70). SAMSUNG-1005, [0139]. Therefore, the first and second source or drain regions in the combination would have a boron concentration graded from a base level (e.g., no boron) in the ground layers 63 and 73 to a concentration in excess of $1E20$ in upper regions 60 and 70. SAMSUNG-1003, ¶122.

To the extent that claim 3 requires further non-zero gradations of boron, such features would have been obvious based on Simonelli. SAMSUNG-1003, ¶123. Simonelli discloses a silicon-germanium film stack 1400 for use in, among other things, source or drain regions in a FinFET. SAMSUNG-1008, [0044]-[0058], FIGS. 6-15. Simonelli's film stack includes graded concentrations of boron as follows:

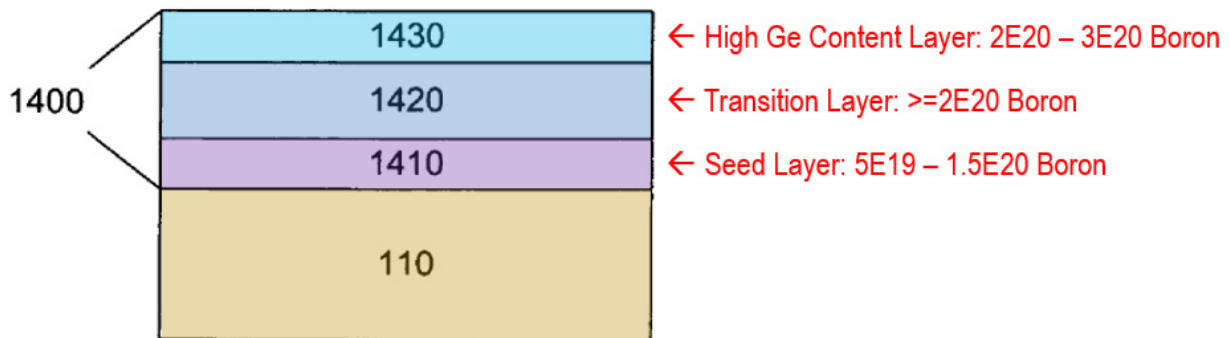


FIG. 14

Simonelli, FIG. 14 (annotated)

It would have been obvious based on Simonelli to similarly grade the concentration of boron from a base level to a level in excess of $1E20$ in Tezuka's source and drain regions 60 and 70, and a POSITA would have been motivated to implement Simonelli-like grading in the combination to maintain proportionality between the concentrations of B and Ge in each graded SiGe layer within source/drain regions 60/70. *See supra*, Ground 1B at [1], [6]; SAMSUNG-1003, ¶124. A POSITA would have sought to maintain this proportionality to gain the benefit of higher boron concentrations than could be accommodated by crystalline structures with higher Ge, while also avoiding overly high concentrations of boron in lower portions of the graded source/drain regions with lower Ge (especially since overly high boron levels can produce precipitations and defects, and since boron more easily diffuses in silicon than germanium). SAMSUNG-1003, ¶124. For example, increasing boron content in regions of higher Ge would have been advantageous to increase conductivity and obtain higher levels of electrical activation without undue boron diffusion. *Id.* Graded boron concentration would also be beneficial to reduce the series resistance where the germanium concentration is highest, and to allow the carrier profile to be tuned such that the boron concentration is higher in the stressor regions and lower elsewhere to reduce junction capacitance. *Id.* Moreover, a graded boron concentration would have been an obvious application of a known technique as taught in Simonelli to Tezuka's device to yield

predictable results like those described in Simonelli. *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success implementing the combination since Simonelli and Tezuka contemplate boron doping in similar devices using similar processes. SAMSUNG-1003, ¶124.

Claims [4]-[5]

Supra, Ground 1A at [4]-[5]. SAMSUNG-1003, ¶¶125-128.

Claims [7]-[8]

Supra, Ground 1B at [2]-[3]. SAMSUNG-1003, ¶¶129-132.

Claims [9]-[10]

Supra, Ground 1A at [9]-[10]. SAMSUNG-1003, ¶¶133-136.

**C. [GROUND 2] – Obviousness based on Tung in view of Simonelli
(Claims 1-10)**

1. Obviousness Analysis

Tung describes techniques for fabricating a non-planar field-effect transistor (e.g., a FinFET) that involves epitaxial growth of a SiGe material 51 over fins 28 to form source and drain regions 39. *Supra*, Section IV.A.2; SAMSUNG-1006, [0040], [0074]. Nonetheless, Tung provides no numerical values for the germanium concentration in SiGe material 51, nor does Tung describe well-known techniques for varying the germanium content in films like SiGe material 51. SAMSUNG-1003, ¶¶137-138; *see also id.*, ¶¶139-195. On the other hand, Simonelli expressly describes techniques for grading germanium within SiGe material of the

source and drain regions of a FinFET such that portions of the SiGe material closest to the silicon-based growth substrate has a lower concentration of germanium and portions of the SiGe material further from the silicon-based growth substrate have increasingly higher germanium content (e.g., 50-atomic percent germanium). *Supra*, IV.B.1.

A POSITA would have found it obvious to form Tung's SiGe material 51 in the source and drain regions 39 according to Simonelli's teachings such that the concentration of germanium in the SiGe material 51 would increase from a lower level near the growth substrate to a higher level near the outer surfaces further from the substrate. SAMSUNG-1003, ¶139. Multiple reasons would have motivated a POSITA to grade the germanium content in the FinFET of the Tung-Simonelli combination in this manner to a concentration in excess of 50%. *Id.*

First, it would have been obvious to grade the germanium content in the SiGe material 51 of the Tung-Simonelli FinFET to a concentration in excess of 50% to ease the transition between the bulk silicon or silicon-rich substrate material (e.g., fin 28 (*see infra* [1a])) over which material 51 is grown and the germanium material of cap layer 55. SAMSUNG-1006, [0058], [0078]; SAMSUNG-1003, ¶140. Grading the germanium content in semiconductor material 51 in this manner would have been beneficial to reduce misfit dislocations at the interface between SiGe material 51 and the silicon-rich substrate material on which material

51 is grown, reduce defects through the entire formation of SiGe material 51, and reduce misfit dislocations at the interface between SiGe material 51 and the germanium cap layer 55. SAMSUNG-1003, ¶140. A POSITA would have appreciated that reducing or even eliminating misfit dislocations and other defects in the growth of semiconductor material 51 would significantly improve performance of the FinFET in the resulting combination, especially since such defects were known to produce unwanted leakage currents, parasitic capacitances, and to prevent or relax forces intended to impart stress on the channel to increase the mobility of charge carriers in the channel and improve ON-currents through the transistor. SAMSUNG-1003, ¶140.

Additionally, absent grading between the silicon-rich growth substrate (e.g., fin 28) and the germanium cap layer 55, the thickness and surface area over which semiconductor material 51 could be grown without defects would be significantly limited—i.e., a limitation that would in turn risk (i) restricting the ON-current that could flow through the transistor, (ii) increasing contact resistance at the source and drain regions due to decreased growth area, and (iii) limiting the amount of stress that could be imparted on the channel in a strained configuration. SAMSUNG-1003, ¶141. In contrast, by grading the germanium content in SiGe material 51, lattice mismatch between the silicon-rich substrate material and SiGe mate-

rial 51 would be reduced to avoid misfit dislocations by ensuring a lower germanium content near the substrate interface. *Id.* Similarly, lattice mismatch between the germanium cap layer 55 and SiGe material 51 would be reduced by ensuring a higher germanium content near the interface of cap layer 55. *Id.* For similar reasons, it would have been obvious to implement one or more transition layers in SiGe material 51 as taught in Simonelli (or to implement smooth transitional grading) to bridge the otherwise large difference in germanium content between the silicon-rich growth substrate (e.g., fin 28) and the cap layer 55. *Id.* Indeed, grading the germanium to a concentration in excess of 50% in SiGe material 51 would have been obvious to bridge the gap in germanium content between the growth substrate and cap layer 55 and to reduce lattice mismatch at the interfaces between the growth substrate, SiGe material 51, and cap layer 55. *Id.*

Second, it would have been obvious to grade the germanium content in the material 51 of the Tung-Simonelli FinFET to a concentration in excess of 50% to increase the mobility of charge carriers in the source and drain regions 39 (i.e., in material 51), and consequently decrease parasitic resistance in the FinFET. SAM-SUNG-1003, ¶142. It was well known that the mobility of electrons and holes through germanium is greater than the mobility of electrons and holes through silicon, and hence increasing the germanium content in SiGe material 51 would pre-

dictably lead to an increase in charge carrier mobilities in the source and drain regions 39. SAMSUNG-1003, ¶142. Increasing carrier mobility and decreasing parasitic resistance would improve performance of the FinFET. *Id.*

Third, it would have been obvious to grade the germanium content in the material 51 to a concentration in excess of 50% to better accommodate high dopant concentrations (e.g., boron) with greater dopant confinement and higher electrical activation than would be achieved in a matrix with a higher concentration of silicon. SAMSUNG-1003, ¶143.

Fourth, it would have been obvious to grade the germanium content in the material 51 of the Tung-Simonelli FinFET's source and drain regions 39 to a concentration in excess of 50% to induce greater stress in the channel region—i.e., a technique that was commonly employed before the '178 Patent to increase the mobility of charge carriers in the channel region of field-effect transistors (which would in turn increase drive currents). SAMSUNG-1008, [0042]; *see also id.*, [0024], [0038], [0044], [0058]; SAMSUNG-1003, ¶144, FN13, 31-35,

For example, in a p-type FET, when the channel is formed of doped silicon and the source and drain regions are formed of an oppositely doped SiGe material, a lattice mismatch results between the materials that induces compressive strain on the channel due to the presence of larger Ge atoms in the source and drain regions. SAMSUNG-1003, ¶145. Tung's FIG. 2d, for instance, shows how the source and

drain regions 39 extend beneath gate spacers 36, and this configuration would have led to compression of the channel region in typical FETs. SAMSUNG-1006, FIG. 2d; *see also* SAMSUNG-1008, [0038] (“stress in the channel region of the MOS transistor ... is accentuated by depositing the high germanium compound alloy in the source extension cavity 330 and the drain extension cavity 340”), [0044] (“formation of strain-inducing source/drain regions in a non-planar device”), [0042], [0053], [0058], FIGS. 11-12 (depicting source/drain regions 1210 protruding through spacers 1010); SAMSUNG-1003, ¶145.

To the extent Tung does not expressly disclose that source and drain regions 39 are formed in a manner specifically designed to induce strain in the channel region, it would have been obvious to implement the source and drain regions 39 in this fashion in the FinFET of the Tung-Simonelli combination. SAMSUNG-1003, ¶146. Strained channel FETs were exceedingly common in both planar and non-planar designs before the '178 Patent, and a POSITA would have sought to implement a strained channel in the Tung-Simonelli FinFET to obtain well-known benefits including increased channel mobility and drive current levels. SAMSUNG-1003, ¶146. For example, strained configurations are frequently realized by growing SiGe source and drain regions over a surface or cavity of a substrate on either side of a channel region like Simonelli's source and drain regions 1210. *See* SAMSUNG-1008, [0051], FIGS. 11-12 (depicting source and drain regions 1210

formed on either side of channel region 110); *see also id.*, [0034]-[0039], [0042], [0044]-[0051]. It would have been obvious to similarly form the source and drain regions 39 by re-growing SiGe material 51 on either side of the channel (e.g., rather than overgrowing SiGe material on fin 28) to impart strain on the channel region according to known and predictable techniques. Indeed, such techniques would have amounted to an obvious use of Simonelli's teachings to improve a similar device (i.e., Tung's FinFET) in a similar way. *KSR*, 550 U.S. at 417; *SAMSUNG-1003*, ¶146.

A POSITA would have had a reasonable expectation of success grading the germanium content in the SiGe material 51 of the Tung-Simonelli FinFET to a concentration in excess of 50%. Simonelli and Tung both describe non-planar FETs (e.g., FinFETs), and both describe techniques for epitaxially growing SiGe material in the source/drain regions of a device. *SAMSUNG-1003*, ¶147. Simonelli's teachings for grading germanium content in the source and drain regions would thus be applied to Tung's FinFET in a substantially similar context. Further, graded epitaxial growth was well known before the '178 Patent, and it would have been well within the skill of a POSITA to vary the relative concentrations of silicon and germanium during the growth process of SiGe material 51 according to Simonelli's teachings. *SAMSUNG-1003*, ¶147. Moreover, for implementations of the Tung-Simonelli combination that involve modifications of Tung's FinFET to

achieve a strained channel region, a POSITA would have had a reasonable expectation of success in light of the substantially similar types of FinFET devices described in each of Tung and Simonelli, the long-established practice of introducing strain in the channel regions of FETs using techniques like those disclosed in Simonelli, and Tung's own acknowledgment that a POSITA would have known how to make a range of modifications to its device. SAMSUNG-1006, [0019]-[0020], [0082]-[0084]; SAMSUNG-1003, ¶147.

The Tung-Simonelli combination would have rendered obvious each of claims 1-10 for the reasons described in detail below.

Element [1pre]

To the extent the preamble is a limitation, the Tung-Simonelli combination would have rendered obvious [1pre], e.g., in view of Tung's disclosure of an integrated circuit structure as a non-planar FET. SAMSUNG-1006, [0002]-[0004]; SAMSUNG-1003, ¶150; *see also id.*, ¶¶148-149. Tung, in FIGS. 13-16, for example, describes "various stages of manufacturing" of a non-planar transistor having "a doped semiconductor layer and a metal silicide [] formed on a raised source/drain structure." SAMSUNG-1006, [0072]; *see also id.*, [0073]-[0082], FIGS. 13-16. Tung further explains that, although FIGS. 13-16 "illustrate the fabrication of a device with at least two fins 28," "the method described in FIG. [sic] 13-16" can also be "used in fabrication of a device with a single fin" to form the

device “corresponding to the embodiment described in FIG. 2.” *Id.*, [0082]; *see also id.*, [0032]-[0034], FIG. 2. Tung’s description of FIGS. 4a-4e provides additional detail of a single-fin embodiment consistent with the embodiments described with respect to FIGS. 13-16. *Id.*, [0039]-[0045]; FIGS. 4a-4e.

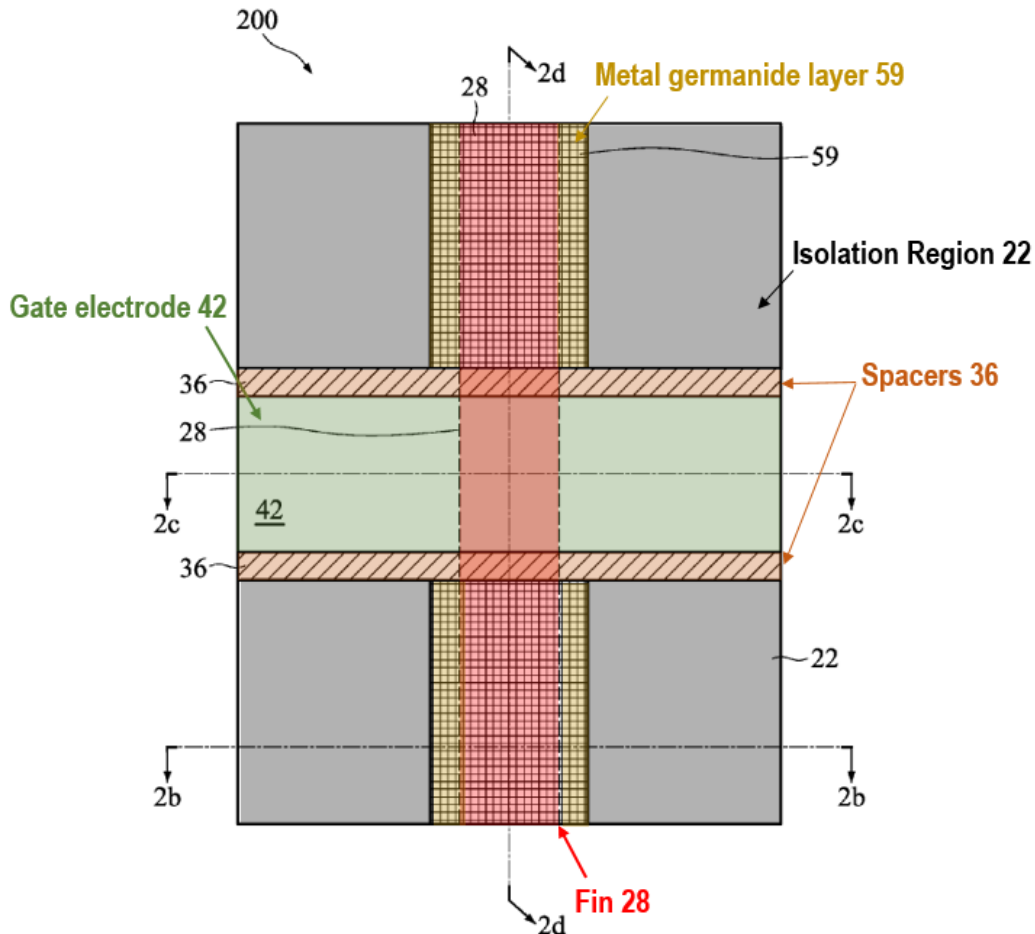


FIG. 2a

Tung, FIG. 2a (annotated)

Element [1a]

The Tung-Simonelli combination would have rendered obvious [1a], e.g., in view of Tung’s disclosure of a fin 28 comprised of silicon. In particular, in various

embodiments, fin 28 is formed from substrate 20, which Tung explains is made from material including silicon. SAMSUNG-1006, [0048] (“substrate 20 comprises bulk silicon” or “substrate 20 comprises bulk silicon germanium (SiGe)”), [0051] (“Fins 28 may be formed by recessing the top surfaces of the isolation regions 22, and hence leaving the fins 28” of substrate 20), [0049], FIGS. 2, 5, 6a-6b, 13-16; *supra*, [1pre]; SAMSUNG-1003, ¶151. Tung also teaches that the source and drain regions 39 can be formed in the fin, and that the source and drain regions 39 can include semiconductor material 51 including silicon. SAMSUNG-1006, [0074], [0040], [0033]; *infra*, [1c]/[1h].

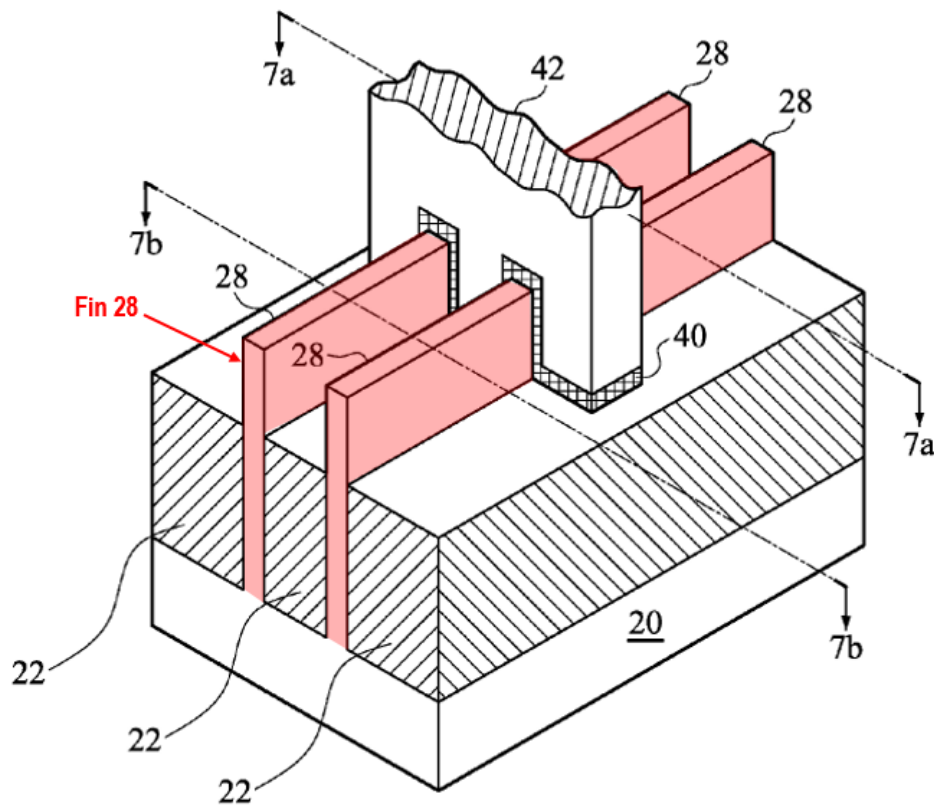


FIG. 7c

Tung, FIG. 7c (annotated)

Element [1b]

The Tung-Simonelli combination would have rendered obvious [1b], e.g., in view of Tung's disclosure of a gate electrode 42 over fin 28. SAMSUNG-1006, [0053]-[0055], FIGS. 2a, 2c, 7c; SAMSUNG-1003, ¶152.

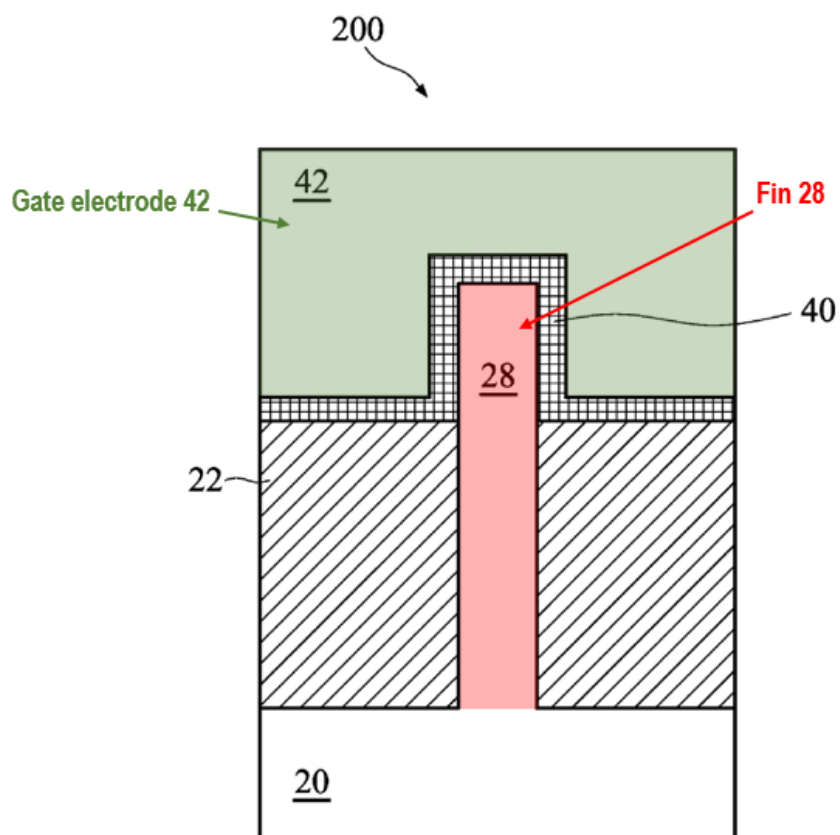


FIG. 2c

Tung, FIG. 2c (annotated)

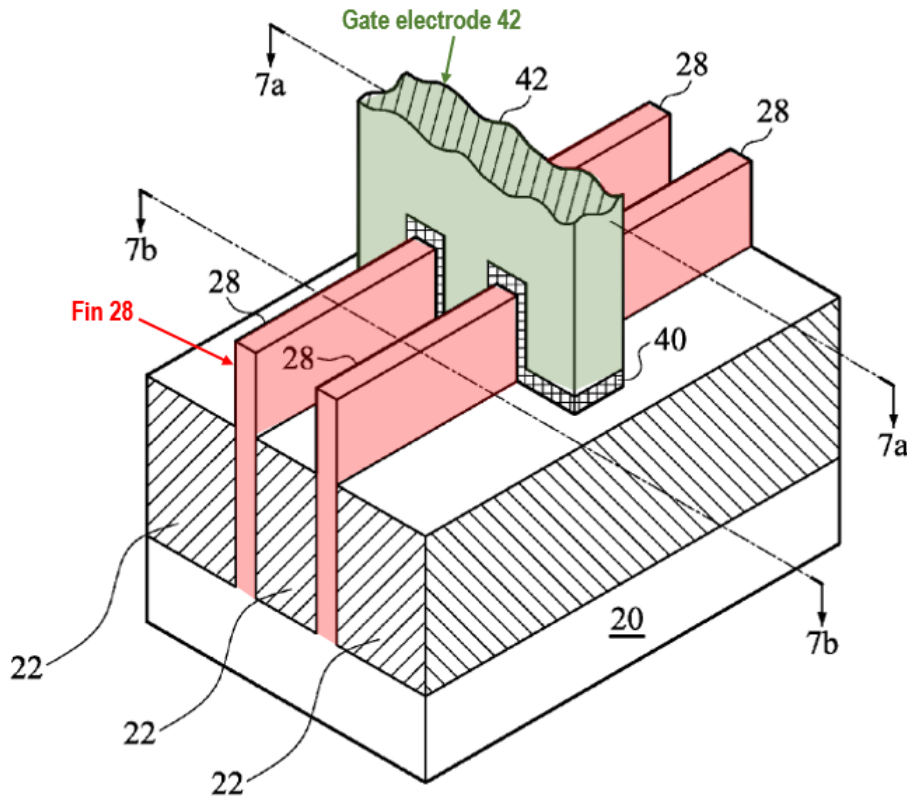


FIG. 7c

Tung, FIG. 7c (annotated)

Elements [1c], [1h]

The Tung-Simonelli combination would have rendered obvious [1c] and [1h], e.g., in view of Tung's disclosure of first and second source or drain regions 39 formed very near/close and proximate either side of gate electrode 42. SAMSUNG-1006, [0032]-[0034], [0057], [0074]-[0078], FIGS. 2a, 2d, 8, 13; *supra*, Ground 1A at [1c]; SAMSUNG-1003, ¶153; *see also id.*, ¶¶154-155; *cf.* SAMSUNG-1001, FIG. 6 (depicting source/drain epitaxial regions 631 similarly proximate to either side of gate electrode 640).

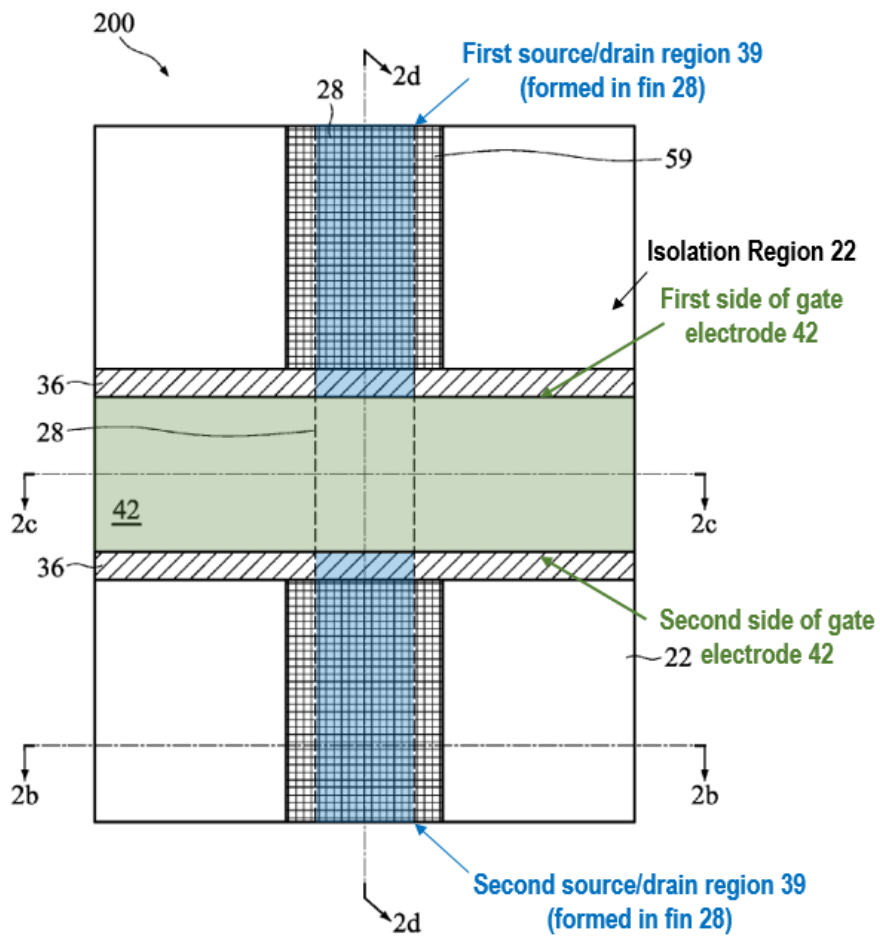


FIG. 2a

Tung, FIG. 2a (annotated)

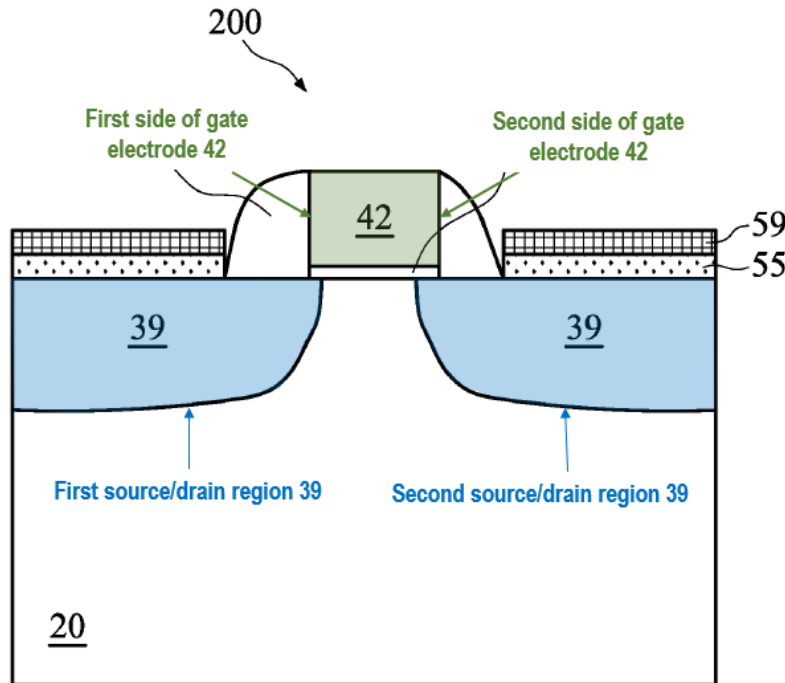


FIG. 2d

Tung, FIG. 2d (annotated)

Tung further discloses and would have rendered obvious source/drain regions 39 that are each formed “in the fin.” SAMSUNG-1006, [0033] (“source/drain regions 39 is [sic] **disposed within the fins 28**”); *see also id.*, [0057], [0074]-[0077], FIGS. 2b, 13; *supra*, Ground 1A at [1c].

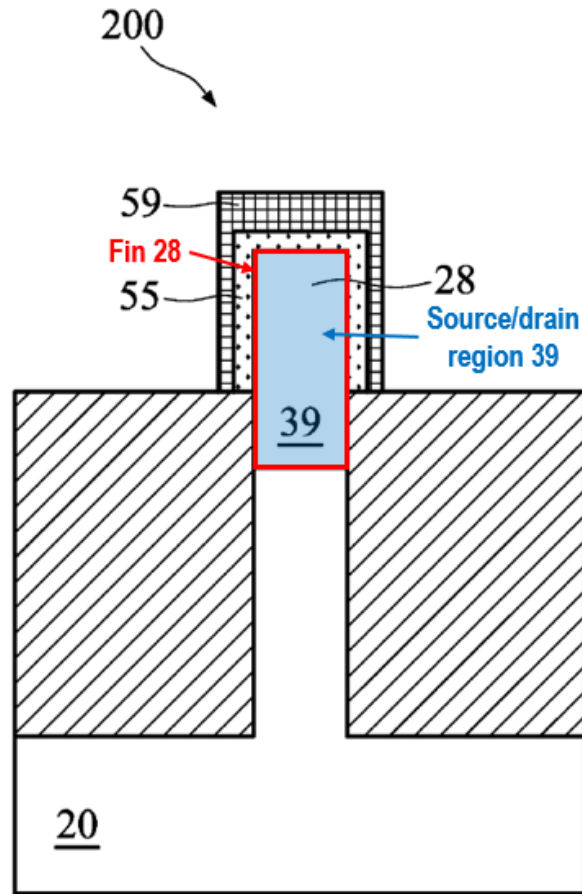


FIG. 2b

Tung, FIG. 2b (annotated)

Tung also teaches that the source and drain regions 39 can include an epitaxially grown semiconductor material 51 such as SiGe. SAMSUNG-1006, [0074], [0040]; *see also id.*, [0039]-[0045] and FIGS. 4a-4e, [0072]-[0082] and FIGS. 13-16. According to Tung's teaching that the source and drain regions 39 are disposed within the fin, semiconductor material 51 would also be disposed within the fin. *Id.*, [0033]. Moreover, it would have been obvious and a POSITA would have

understood that the epitaxially grown source/drain regions 39 adjacent to a portion of the fin in the channel region, whether formed over fin 28 or grown from the substrate 20 based on Simonelli's teachings (*see infra*, [1f]/[1k]), would be "in the fin" at least to the same extent disclosed in the '178 Patent. *Cf.* SAMSUNG-1001, 13:22-50, FIG. 6; *see also* SAMSUNG-1013, 32; *supra*, Ground 1A at [1c]; SAMSUNG-1003, ¶154.

Elements [1d], [1i]

The Tung-Simonelli combination would have rendered obvious [1d] and [1i], e.g., in view of Tung's disclosure of facets and a top surface that are formed when a semiconductor material 51 (e.g., SiGe) is epitaxially grown over a substrate such as fin 28 to form source/drain regions 39. SAMSUNG-1003, ¶156. More specifically, Tung discloses that "a selective epitaxial growth is performed to form semiconductor material 51," and "[t]he semiconductor material 51 forms the source/drain regions 39 (raised source/drain) of the non-planar transistor 400" ... "on the fins 28." SAMSUNG-1006, [0074]. According to Tung, "[t]he epitaxial growth includes vertical growth and horizontal growth," and if the device includes just a single fin 28 or "the separation between adjacent fins 28 ... [is] large," then "each fin 28 forms a separate raised source/drain region comprising the semiconductor material 51." *Id.*, [0075].

Tung's FIG. 4b illustrates the use of a "selective epitaxial growth process" to

form a “semiconductor material 51” over a fin 28, where “[t]he growth proceeds in both lateral and vertical directions, for example at different rates on different crystal planes” to form two or more facets and a top surface. *Id.*, [0040]; *see also id.*, [0058]; *supra*, Section II.B; SAMSUNG-1003, ¶157.

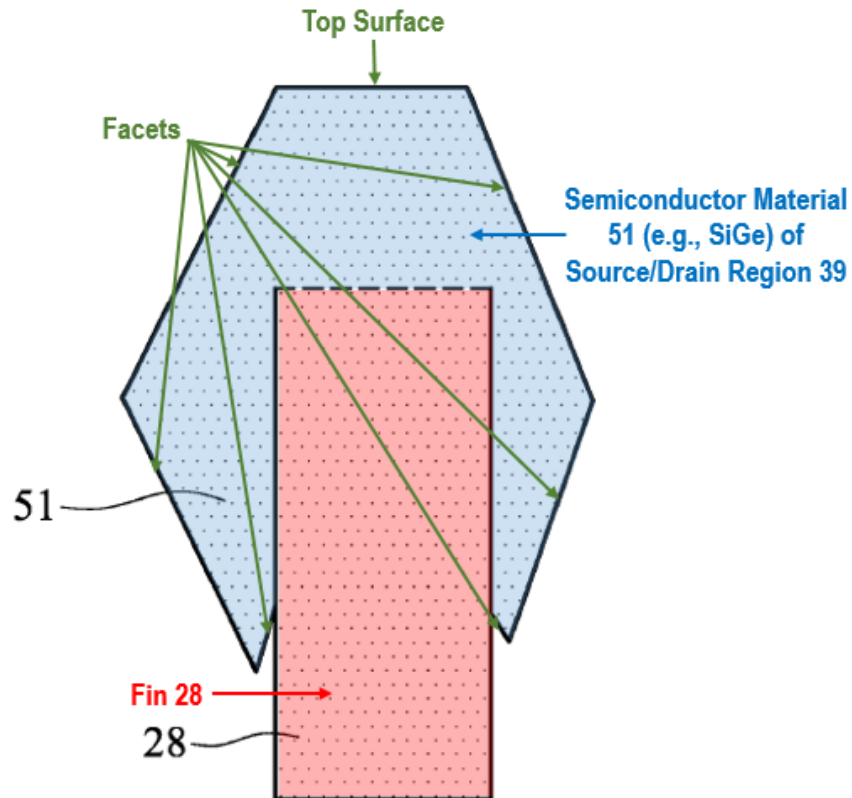


FIG. 4b

Tung, FIG. 4b (annotated)

Elements [1e], [1j]

The Tung-Simonelli combination would have rendered obvious [1e] and [1j], e.g., in view of Tung’s disclosure that components of the first and second

source and drain regions 39, including semiconductor material 51, and optionally fin 28, can each include silicon and germanium. SAMSUNG-1006, [0040] (“semiconductor material 51 comprises SiGe”), [0074] (“semiconductor material 51 forms the source/drain regions 39” and “is formed of ... silicon germanium (SiGe)”), [0048] (substrate 20 from which fins 28 are formed can be “bulk silicon” or “bulk silicon germanium (SiGe)”); SAMSUNG-1003, ¶158.

Elements [1f], [1k]

The Tung-Simonelli combination would have rendered obvious [1f] and [1k]. SAMSUNG-1003, ¶159; *see also id.*, ¶¶160-164. As noted above with respect to [1e]/[1j], Tung teaches that “a selective epitaxial growth is performed to form semiconductor material 51” over fin 28, and the resulting structure including “semiconductor material 51 forms the source/drain regions 39.” SAMSUNG-1006, [0074], [0040]. In Tung, the substrate 20—and, hence, fin 28 (which is formed from substrate 20)—can be bulk silicon, while semiconductor material 51 can be “formed of a material different from that of substrate 20, for example, silicon germanium (SiGe)” *Id.*, [0074], [0048].

Although Tung does not expressly disclose the relative concentrations of silicon and germanium in semiconductor material 51, or whether the concentrations of silicon and germanium are uniform or graded during growth of layer 51, a

POSITA would have understood that different options could be pursued to optimize one or more attributes of the device's performance and/or fabrication. SAMSUNG-1003, ¶¶163-164. Simonelli, for example, describes solutions for achieving high concentrations of germanium in the source/drain regions of a non-planar FET through an epitaxial growth that involves increasing the germanium content in a SiGe material as growth progresses away from the substrate (e.g., a bulk silicon substrate). SAMSUNG-1008, [0053]-[0058]. FIG. 12, reproduced below, illustrates Simonelli's non-planar FET, similar to Tung's FinFET:

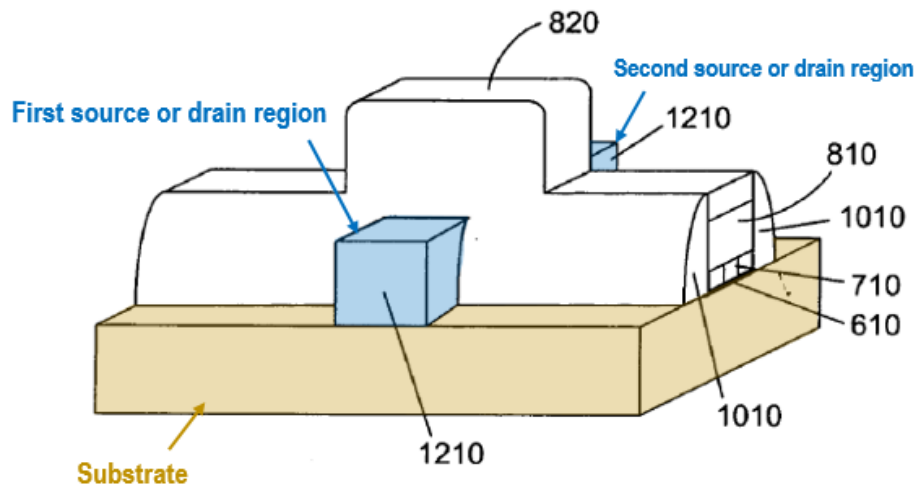


FIG. 12

Simonelli, FIG. 12 (annotated)

In Simonelli, source/drain regions 1210 are epitaxially grown “using a graded high-germanium content silicon-germanium film stack 1400.” SAMSUNG-1008, [0051]. Film stack 1400 includes a series of layers 1410, 1420, 1430, each additional layer having higher germanium content than the preceding

layer:

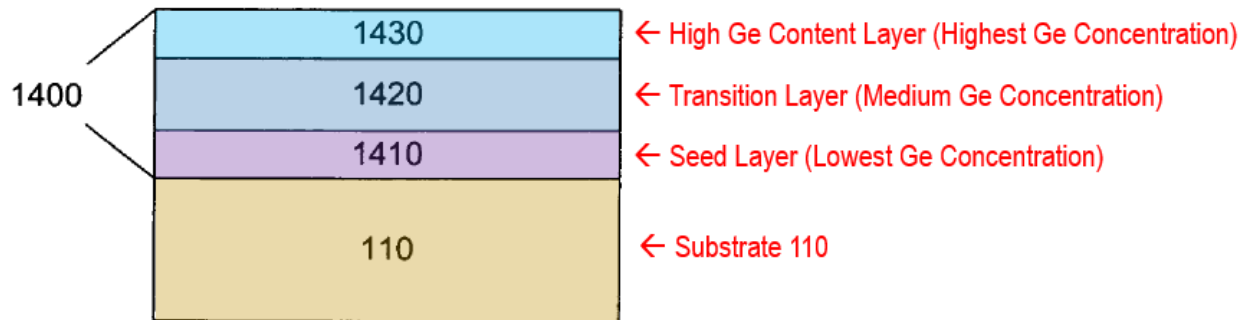


FIG. 14

Simonelli, FIG. 14 (annotated)

See also SAMSUNG-1008, [0053]-[0058], [0021]-[0024], FIGS. 14-15.

Simonelli further teaches that the concentration of germanium in the film stack can be graded from 20-25 atomic weight % in the seed layer 1410 to 40-55 atomic weight % in the high Ge content layer 1430. SAMSUNG-1008, [0054], [0058]. As another example, Simonelli discloses that source/drain regions “may be filled with a graded germanium silicon alloy ... according to one or more methods such as the embodiment described below in FIG. 15” in which “[t]he graded germanium silicon alloy may be epitaxially deposited with a graded germanium concentration that may range from 10 atomic % to **50 atomic %.**” *Id.*, [0039].

For the reasons described in detail above in the overview of the Tung-Simonelli combination, it would have been obvious and a POSITA would have had ample motivation to grade the germanium content in material 51 of the source and

drain regions 39 of the FinFET in the combination to a concentration in excess of 50%. *Supra*, Section IV.C.1; SAMSUNG-1003, ¶¶163-164.

To the extent that neither Tung nor Simonelli expressly disclose a germanium concentration “**in excess of 50%**” as recited in [1f] and [1k], the claimed range nonetheless would have been obvious in view of Simonelli’s disclosure of grading to 50% germanium. SAMSUNG-1008, [0039]; SAMSUNG-1003, ¶¶163-164. As an initial matter, a POSITA would have understood that no fabrication process is perfectly controlled, and hence it would have been obvious that a FinFET intended to have germanium in its source and drain regions graded to a concentration of 50% as taught in Simonelli would commonly include a small or negligible amount more germanium than silicon. SAMSUNG-1003, ¶¶163-164. Even a single additional germanium atom would yield a germanium concentration in excess of 50%. *Id.*

Moreover, as described above in the overview of the Tung-Simonelli combination (*supra*, Section IV.C.1), a POSITA would have understood that the concentration of germanium in SiGe material 51 of the source and drain regions 39 impacts various properties of the FinFET, including the lattice constant at different depths of the SiGe material 51, the lattice mismatch at the interfaces on either side of SiGe material 51, the thickness and size at which the SiGe material 51 could be grown without defects, the mobility and parasitic resistance of the source and drain

regions, and the amount of strain that could be imparted on a channel region. It would have been obvious for a POSITA to grade germanium content in SiGe material 51 to a concentration in excess of 50% through routine experimentation to optimize one or more of these properties.⁷ SAMSUNG-1003, ¶164; *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003) (“a *prima facie* case of obviousness exists when the claimed range and the prior art range do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties”); *du Pont*, 904 F.3d at 1006; *In re Brandt*, 886 F.3d 1171, 1176-1177 (Fed. Cir. 2018) (claimed range of “less than 6 pounds per cubic feet” rendered obvious by prior art disclosing an abutting range of “between 6lbs/ft³ and 25 lbs/ft³”); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 783 (Fed. Cir. 1985); *In re Aller*, 220

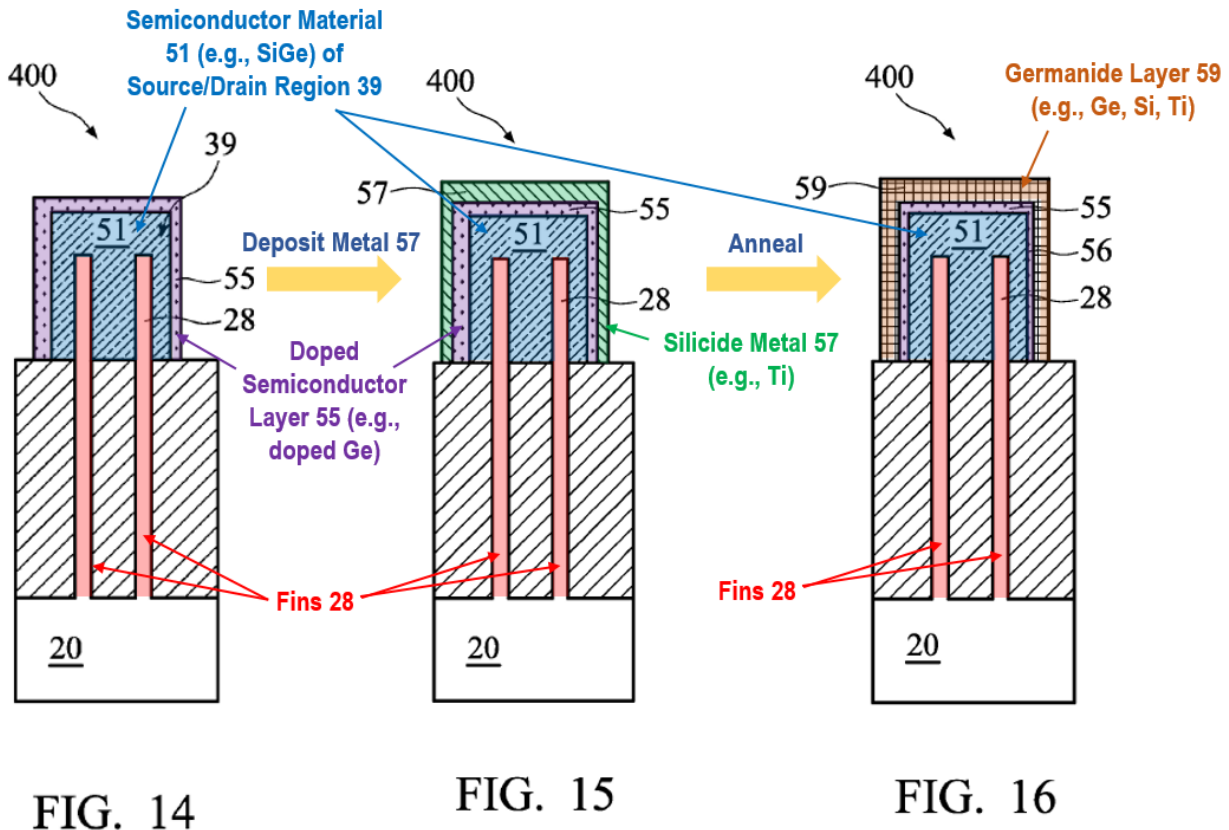
⁷ Notably, the ’178 Patent identifies nothing critical about a germanium concentration “in excess of 50%” in the source/drain regions. *Supra*, Section II.B; SAMSUNG-1001, 3:10-17, 4:21-25, 6:39-54, 16:43-44. The ’178 Patent discloses that a range of 30-70% germanium would be suitable, for example. *Id.*; SAMSUNG-1003, FN35. Notably, the ’178 patent distinguishes germanium concentrations in the source/drain regions from germanium concentrations in the overlays used to form germanide layers. *Supra*, Section II.A.

F.2d 454, 456 (CCPA 1955)); MPEP §2144.05 (describing result-effective variables).

Elements [1g], [11]

The Tung-Simonelli combination would have rendered obvious [1g] and [11], e.g., in view of Tung's disclosure of a germanide layer⁸ 59 formed over respective top surfaces of a semiconductor material 51 of the first and second source or drain regions 39. SAMSUNG-1003, ¶165; *see also id.*, ¶¶163-164 and ¶¶166-173; *supra*, Ground 1A at [1g]/[11]. For example, Tung describes a process for forming a germanide layer 59 that involves first forming a doped semiconductor layer 55 over a semiconductor material 51 of the source/drain regions 39, then depositing a metal 57 over the doped semiconductor layer 55, and finally annealing the metal 57 to form the germanide layer 59. SAMSUNG-1006, [0078]-[0081], FIGS. 14-16; *see also id.*, [0039]-[0045], FIGS. 4a-4e, FIG. 2a and 2d (depicting layer 59 formed over both source and drain regions 39).

⁸ *Supra*, Footnote 1.



Tung, FIGS. 14-16 (annotated)

FIGS. 14-16 depict the formation of germanide layer 59 on a device having multiple fins 28 spaced closely to each other such that a continuous semiconductor material 51 is grown across each fin 28. Tung also explains, however, that “the method described in FIG[S]. 13-16 is used in fabrication of a device with a single fin” or fins spaced further from each other. *See* SAMSUNG-1006, [0082]. FIGS. 4b-4e depicting Tung’s process as applied to a single fin (or a fin spaced sufficiently far from others):⁹

⁹ *Supra*, Footnote 3.

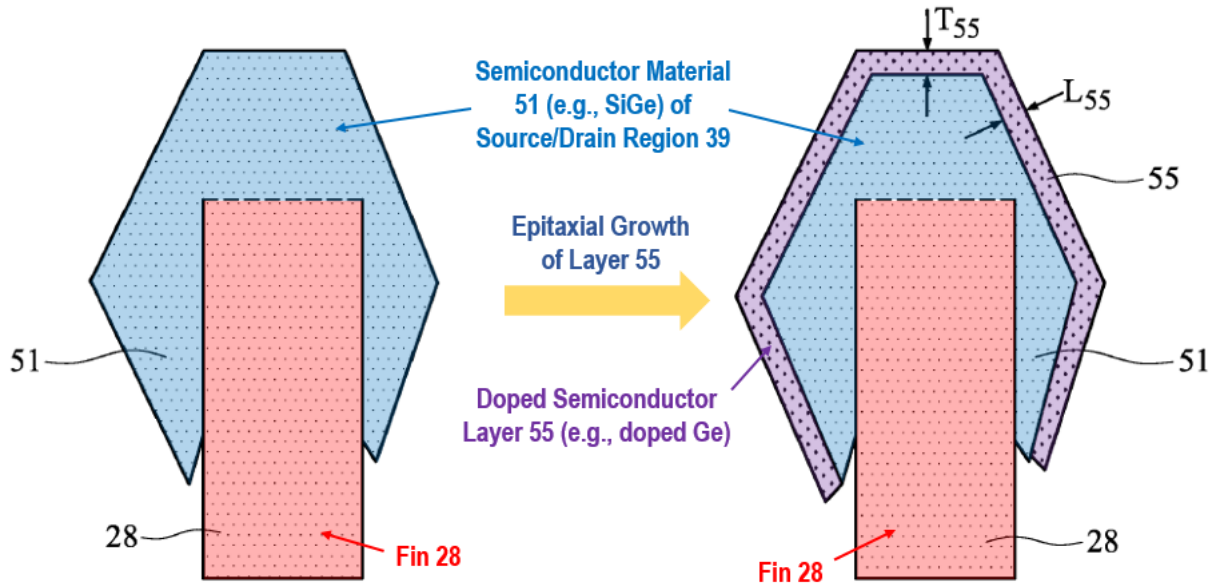


FIG. 4b

FIG. 4c

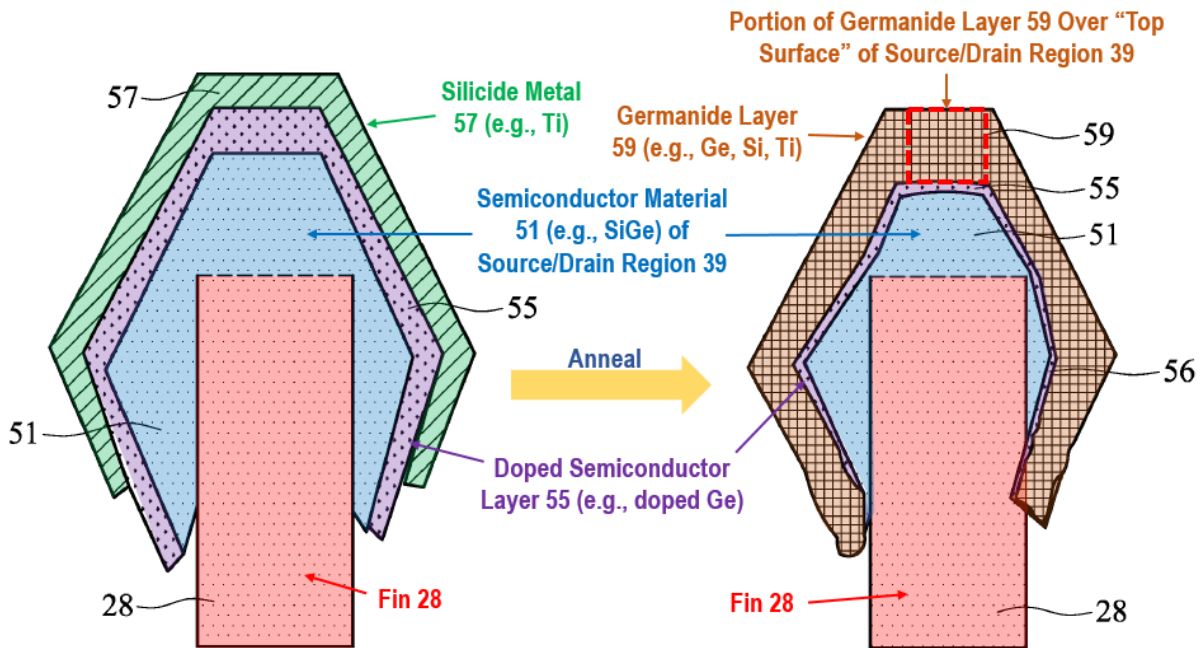


FIG. 4d

FIG. 4e

Tung, FIGS. 4b-4e (annotated)

Tung explains and it would have been obvious that semiconductor layer 55 can be a doped germanium layer; semiconductor material 51 in source/drain regions 39 can be epitaxially grown SiGe; and the germanide metal 57 can include titanium. *Id.*, [0040], [0042], [0061], [0058], [0074], [0078], [0080]; SAMSUNG-1003, ¶169; *see also id.*, ¶¶170-173. In this context, it would have been obvious for substantially similar reasons to those described above with respect to [1g]/[11] in Ground 1A that the germanide layer 59 that results from annealing would comprise titanium, silicon, and germanium. *Supra*, Ground 1A at [1g]/[11]; SAMSUNG-1003, ¶85; *see also id.*, ¶¶96-97, 170-173.

Claim [2]

The Tung-Simonelli combination would have rendered obvious [2], e.g., in view of Tung's disclosure that, "[d]uring the growth of semiconductor material 51" in the source and drain regions 39, "a p-type impurity ... may be in-situ doped" at a concentration up to "about $5 \times 10^{20}/\text{cm}^3$ " (i.e., greater than $1\text{E}20$). SAMSUNG-1006, [0076]. Tung further would have rendered obvious boron as a p-type impurity. *Id.*, [0028] ("p-type dopant such as boron"), [0034], [0052]; SAMSUNG-1003, ¶¶174-175.

Claim [3]

The Tung-Simonelli combination would have rendered obvious [3], e.g., based on Simonelli's disclosure of a silicon-germanium film stack 1400 for use in,

among other things, source or drain regions of a FinFET. SAMSUNG-1008, [0044]-[0058], FIGS. 6-15. Simonelli's film stack includes graded concentrations of boron as follows:

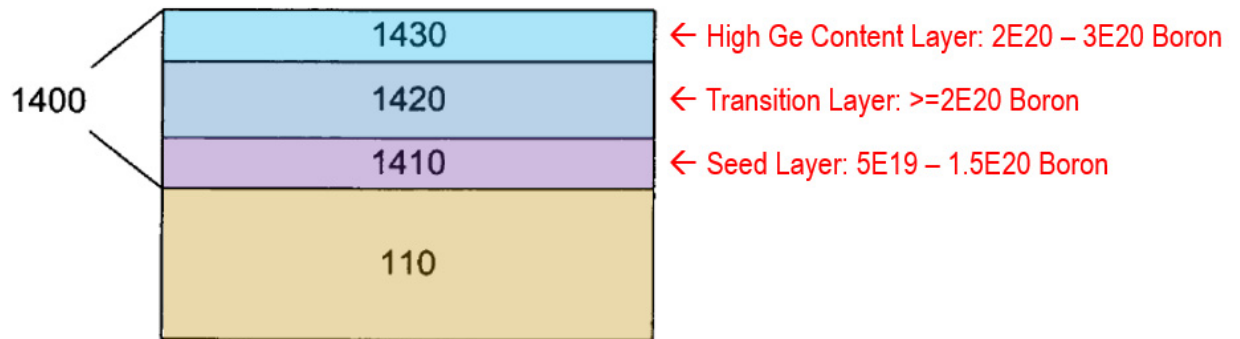


FIG. 14

Simonelli, FIG. 14 (annotated)

It would have been obvious to implement graded boron concentrations like those disclosed in Simonelli in the source and drain regions of the device in the Tung-Simonelli combination, and a POSITA would have had a reasonable expectation of success, for substantially the same reasons discussed above with respect to [3] in Ground 1B. SAMSUNG-1003, ¶178; *see also id.*, ¶¶176-177; *supra*, Ground 1B at [3].

Claim [4]

The Tung-Simonelli combination would have rendered obvious [4]. SAMSUNG-1003, ¶¶179-180. In the combination, Tung teaches that the non-planar transistor includes a channel region “disposed under the gate electrode 42 on a top

surface and sidewalls of the fin 28” between the first and second source or drain regions 39. SAMSUNG-1006, [0025], FIGS. 1d, 2d, 11; *see also id.*, [0026]-[0031], [0052] (“fins 28 are implanted to uniformly dope the channel region”), [0065] (“source/drain region 39 are separated by a channel 11”). Further, as described above in the overview of the Tung-Simonelli combination (*supra*, Section IV.C.1), it would have been obvious to form a graded SiGe material 51 in the first and second source or drain regions 39 that would apply a compressive strain to the channel region to increase the hole mobility in the channel. SAMSUNG-1008, [0024], [0042], [0044]; SAMSUNG-1003, ¶¶179-180.

Claim [5]

The Tung-Simonelli combination would have rendered obvious [5], e.g., in view of Tung’s disclosure that the semiconductor material 51 and/or fin 28 of the source and drain regions 39 can be doped with p-type impurities. SAMSUNG-1006, [0073], [0076]-[0077]; *see also id.*, [0034] (“PMOS transistor is being fabricated”), [0041], [0052]; SAMSUNG-1003, ¶¶181-182.

Element [6pre]

Supra, [1pre]. SAMSUNG-1003, ¶¶183-185.

Element [6a]

Supra, [1a]. The Tung-Simonelli combination would have rendered obvious [6a], e.g., in view of Tung’s disclosure of a fin comprising silicon. *See supra*, [1a],

[1c], [1h]. For example, just as the specification of the '178 Patent identifies structure 660 alternately as a “body” or a “fin,” the same structures from the Tung-Simonelli combination that would have rendered obvious a “fin” would also have rendered obvious the recited “body” in Claim 6. *Cf.* SAMSUNG-1001, 13:24-27, FIG. 6; SAMSUNG-1003, ¶186.

Elements [6b]-[6l]

Supra, [1b]-[1l]. SAMSUNG-1003, ¶187.

Claim [7]

Supra, [2]. SAMSUNG-1003, ¶¶188-189.

Claim [8]

Supra, [3]. SAMSUNG-1003, ¶¶190-191.

Claim [9]

Supra, [4]. SAMSUNG-1003, ¶¶192-193.

Claim [10]

Supra, [5]. SAMSUNG-1003, ¶¶194-195.

D. [GROUND 3A] – Obviousness based on Conway, Tezuka, and Tung (Claims 11-20)

1. Overview of Conway

Conway describes a computing device having a range of components implemented as integrated circuit structures “mounted on a common motherboard” SAMSUNG-1010, [0148], [0153], [0162]; *generally id.*, [0147]-[0165], FIGS. 5-8.

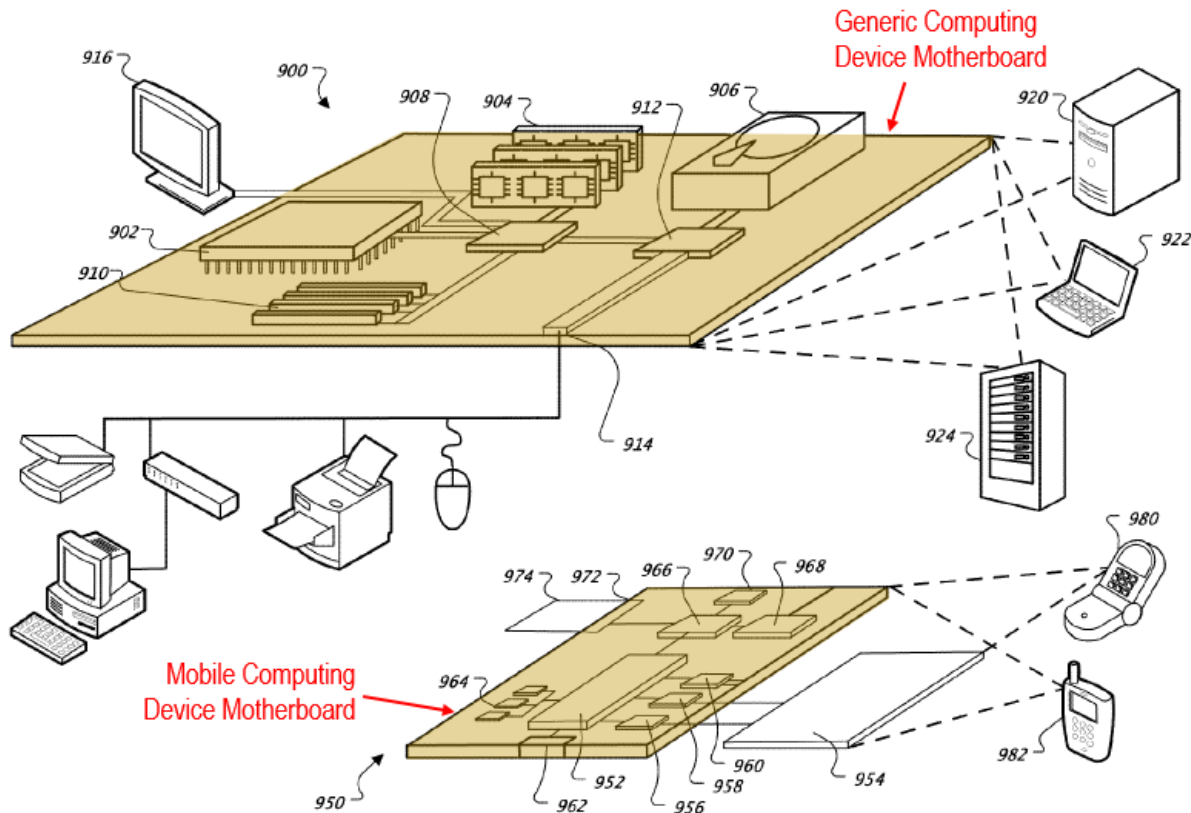


FIG. 9

SAMSUNG-1010, FIG. 9 (annotated).

2. Obviousness Analysis

A POSITA would have found it obvious and would have been motivated by multiple reasons to use a FinFET like that of the Tezuka-Tung combination of Ground 1A to implement one or more of the electronic components in Conway's computing device. SAMSUNG-1003, ¶196; *see also id.*, ¶197.

First, Conway indicates that integrated circuit structures can form the building blocks of Conway's device components, but provides little detail about these structures. It would have been obvious to look to other sources, such as Tezuka

and Tung, for details of known and predictable transistor designs. SAMSUNG-1003, ¶¶196-197.

Second, a POSITA would have sought to exploit well-known advantages of non-planar FinFETs like those described in Tezuka (and Tung), including improved channel control, lower leakage currents, smaller size, and increased switching speeds relative to many conventional planar devices. SAMSUNG-1003, ¶197.

Third, the combination would have amounted to a merely obvious application of the Tezuka-Tung techniques to Conway's device, which was ripe for improvement and in a manner that would yield no more than predictable results. *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success implementing the combination. SAMSUNG-1003, ¶197.

The Conway-Tezuka-Tung combination would have rendered obvious each of claims 11-20. SAMSUNG-1003, ¶¶196-197.

Claim [11pre]

To the extent the preamble is a limitation, the Conway-Tezuka-Tung combination would have rendered it obvious, e.g., in view of Conway's disclosure of various "generic" mobile and non-mobile computing devices. SAMSUNG-1010, FIG. 9 and [0147]-[0165]; *see also id.*, FIGS. 5-8 and associated text; SAMSUNG-1003, ¶200; *see also id.*, ¶¶198-199.

Element [11a]

The Conway-Tezuka-Tung combination would have rendered obvious [11a],

e.g., in view of Conway's disclosure of "a common motherboard" for mounting various components of a computing device. SAMSUNG-1010, [0148], [0153], FIG. 9; *supra*, Section IV.D.1; SAMSUNG-1003, ¶201.

Element [11b]

The Conway-Tezuka-Tung combination would have rendered obvious [11b]. SAMSUNG-1003, ¶202. Conway teaches that "the systems and techniques described here can be realized in digital electronic circuitry, integrated circuitry, specially designed ASICs (application specific integrated circuits), computer hardware, firmware, software, and/or combinations thereof." SAMSUNG-1010, [0162]. Conway also describes various components coupled to a "common motherboard." SAMSUNG-1010, [0148], [0153], FIG. 9; *see also id.*, FIGS. 5-8 and associated text. Further, in the combination, and as described above in the overview of the combination (Section IV.D.2), it would have been obvious to utilize the Tezuka-Tung integrated circuit structure of Ground 1A in one or more of Conway's components coupled to the motherboard. SAMSUNG-1003, ¶202.

Elements [11c]-[11n]

Supra, Ground 1A at [1a]-[11]; SAMSUNG-1003, ¶¶203.

Claim [12]

The Conway-Tezuka-Tung combination would have rendered obvious [12], e.g., in view of Conway's disclosure of a memory coupled to the board. SAMSUNG-1010, [0148]-[0151] and FIG. 9 (memories 904, 906), [0153]-[0157] and

FIG. 9 (memories 964, 974), [0123]-[0125] and FIG. 6, [0011], [0078], [0148], [0153]; SAMSUNG-1003, ¶¶204-205.

Claim [13]

The Conway-Tezuka-Tung combination would have rendered obvious [13], e.g., in view of Conway’s disclosure of a “communication interface” such as interface 966 that includes “digital signal processing circuitry” for implementing various communication capabilities on the device. SAMSUNG-1005, [0152]-[0153], [0158], FIG. 9; *see also id.*, [0148] (“mounted on a common motherboard”), FIG. 6 (607) SAMSUNG-1003, ¶207. A POSITA would have understood and it would have been obvious to implement the communications circuitry on a communication chip. SAMSUNG-1003, ¶¶206-207.

Claim [14]

The Conway-Tezuka-Tung combination would have rendered obvious [14], e.g., in view of Conway’s disclosure of a camera coupled to the board. SAMSUNG-1010, [0113] (“device 500 includes ... a camera 507”), [0118], [0121], [0123] (“camera interface 608 ... for capturing digital images from the camera 507”), FIG. 6; *see also id.*, [0148], [0153], FIG. 9; SAMSUNG-1003, ¶¶208-209.

Claim [15]

The Conway-Tezuka-Tung combination would have rendered obvious [15], e.g., in view of Conway’s disclosure of a GPS receiver module coupled to the board. SAMSUNG-1010, [0095] (“GPS device”), [0102], [0130], [0158] (“GPS

(Global Positioning System) receiver module 970”); *see also id.*, [0148], [0153],

FIG. 9; SAMSUNG-1003, ¶¶210-211.

Claim [16]

The Conway-Tezuka-Tung combination would have rendered obvious [16], e.g., in view of Conway’s teachings of a battery coupled to the board. SAMSUNG-1003, ¶¶212-213. For example, Conway describes that the computing device can include a “battery life indicator 516 that indicates a measurement of the remaining battery life,” which a POSITA would have understood or found obvious to mean that the device includes a battery. SAMSUNG-1010, [0114], FIG. 5; SAMSUNG-1003, ¶213. Conway also discloses “a power source 619 that provides an appropriate alternating current (AC) or direct current (DC) to power components.” SAMSUNG-1010, [0123], FIG. 6; SAMSUNG-1003, ¶213. In a mobile device, and other devices, it would have been obvious that the power source 619 would include a battery coupled to the board, e.g., to deliver power to components on the board. SAMSUNG-1003, ¶212; SAMSUNG-1010, [0148], [0153], FIG. 9.

Claim [17]

The Conway-Tezuka-Tung combination would have rendered obvious [17], e.g., in view of Conway’s teachings of an antenna coupled to the board. SAMSUNG-1010, [0113]-[0114], [0119], [0120], [0123], FIGS. 5-6 (antenna 505); *see also id.*, [0148], [0153], FIG. 9; SAMSUNG-1003, ¶¶214-215.

Claim [18]

The Conway-Tezuka-Tung combination would have rendered obvious [18], e.g., in view of Conway’s teachings of integrated circuit dies packaged for mounting on a motherboard. Conway describes in paragraph [0162] “integrated circuitry” components, and FIG. 9 shows various integrated circuit chips mounted on a motherboard. SAMSUNG-1010, [0148], [0162], FIG. 9; SAMSUNG-1003, ¶¶216-217. A POSITA would have understood and it would have been obvious that the mounted components include a packaged integrated circuit die. SAMSUNG-1003, ¶217.

Claim [19]

The Conway-Tezuka-Tung combination would have rendered obvious [19], e.g., in view of Conway’s teachings of computing device components such as a central processor 902, processor 952, or various other processing components. SAMSUNG-1010, [0148] (“device 900 includes a processor 902”), [0153] (“device 950 includes a processor 952”), FIG. 9; *see also id.*, [0162]-[0163], [0168] (“digital signal processing circuitry”); *supra*, [13]. It would have been obvious to implement Conway’s electronic components using a FinFET like that described in the Tezuka-Tung combination of Ground 1A. *Supra*, Section IV.D.2; SAMSUNG-1003, ¶¶218-219.

Claim [20]

The Conway-Tezuka-Tung combination would have rendered obvious [20],

e.g., in view of Conway's disclosure of the computing device being a mobile phone, a laptop, a desktop computer, or a server. SAMSUNG-1010, [0147], FIG. 9; SAMSUNG-1003, ¶¶220-221.

E. [GROUND 3B] – Obviousness based on Conway, Tezuka, Tung, and Simonelli (Claims 11-20)

Supra, Ground 3A at [11]-[20]. SAMSUNG-1003, ¶222. It would have been obvious to use a FinFET like that of the Tezuka-Tung-Simonelli combination of Ground 1B in at least one board component in Conway's device for the reasons discussed in the overview of Ground 3A. *Supra*, Section IV.D.2; SAMSUNG-1003, ¶¶222-223. The resulting combination would have rendered claims 11-20 obvious as described above in Ground 1B and 3A. *Id.*

F. [GROUND 3C] – Obviousness based on Conway, Tung, and Simonelli (Claims 11-20)

A POSITA would have found it obvious to use a FinFET like that of the Tung-Simonelli combination of Ground 2 to implement one or more of the electronic components in Conway's device for the reasons discussed in the overview of Ground 3A. *Supra*, Section IV.D.2; SAMSUNG-1003, ¶224.

The resulting combination would have rendered obvious each of claims 11-20, and would have provided each element of these claims for the reasons discussed above with respect to claim 1 in Ground 2 and claims 11-20 in Ground 3A. SAMSUNG-1003, ¶¶224-225.

V. DISCRETIONARY CONSIDERATIONS

A. § 325(d) – *Advanced Bionics*

Neither Tezuka, Tung, nor Conway were previously cited to or by the Office in connection with the '178 Patent, let alone applied in a rejection. Simonelli was cited during original examination, but it also was not addressed substantively during original examination. *Supra*, Section II.B.

Because the '178 Patent's prosecution did not involve negotiation between the applicant and the Examiner regarding the teachings of the prior art combinations applied in the instant Petition, none of Grounds 1A-3C can be said to be the same as, or substantially similar to, art or arguments that the Office previously considered in connection with the '178 Patent. To the extent Simonelli was previously considered at all during examination, the Examiner erred in overlooking its pertinent teachings cited in this Petition. The Examiner also did not have the benefit of considering Simonelli's teachings in combination with Tezuka, Tung, or Conway.

Under these circumstances, Petitioner respectfully submits that exercise of the Board's discretion to deny institution under § 325(d) is unwarranted.

B. §314(a) - *Fintiv*

The '178 Patent is the subject of complaints filed by Patent Owner in both district court and the ITC on September 12, 2022. SAMSUNG-1102, SAMSUNG-1103. The district court case is currently stayed pending resolution of the ITC mat-

ter, and thus only the ITC matter is proceeding at this time. Pursuant to the Director's Interim Guidance, the "PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding." SAMSUNG-1104, 6-7, 9. Accordingly, the *Fintiv* factors do not provide a reason to discretionarily deny institution based on the co-pending ITC proceeding.

VI. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, "Samsung") are the real parties-in-interest. No other parties had access to or control over this Petition, and no other parties funded this Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

The '178 Patent is the subject of civil actions in *In the Matter of Semiconductor Devices, Mobile Devices Containing the Same, and Components Thereof* (ITC Inv. No. 337-TA-1336) and *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352 (E.D. Tex.) (stayed). Taiwan Semiconductor Manufacturing Co. Ltd. has also been named as a respondent in the ITC proceeding and a defendant in the E.D. Tex. proceeding.

Petitioner is not aware of any other disclaimers, reexamination certificates, or IPR petitions addressing the '178 Patent.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
W. Karl Renner, Reg. No. 41,265 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR39843-0153IP1@fr.com	Jeremy J. Monaldo, Reg. No. 58,680 Nicholas Stephens, Reg. No. 74,320 Patrick King, Reg. No. 60,816 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 PTABInbound@fr.com

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR39843-0153IP1@fr.com

(referencing No. 39843-0153IP1 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, jjm@fr.com, nstephens@fr.com, and pking@fr.com).

VII. FEES

Petitioner authorizes charge of Deposit Account No. 06-1050 for any fees.

VIII. CONCLUSION

Petitioner requests IPR and cancellation of the Challenged Claims.

Attorney Docket No. 39843-0153IP1
IPR of U.S. Patent No. 10,700,178
Respectfully submitted,

Dated: February 24, 2023

/Jeremy J. Monaldo/

W. Karl Renner, Reg. No. 41,265
Jeremy J. Monaldo, Reg. No. 58,680
Nicholas Stephens, Reg. No. 74,320
Patrick King, Reg. No. 60,816
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2023-00536)

Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,986 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: February 24, 2023

/Jeremy J. Monaldo/

W. Karl Renner, Reg. No. 41,265
Jeremy J. Monaldo, Reg. No. 58,680
Nicholas Stephens, Reg. No. 74,320
Patrick King, Reg. No. 60,816
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on February 24, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided via Federal Express, to the Patent Owner, by serving the correspondence address of record as follows:

KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

/Diana Bradley/
Diana Bradley
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
(858) 678-5667