

Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Intel Corporation,  
Petitioner

v.

Greenthread, LLC,  
Patent Owner

**U.S. PATENT NO. 9,190,502**

Case IPR2023-TBD

**PETITION FOR *INTER PARTES* REVIEW  
UNDER 35 U.S.C. §312 AND 37 C.F.R. §42.104**

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| 1007               | U.S. Patent No. 6,043,114 to Kawagoe, et al., (“Kawagoe”)                                                                |
| 1008A              | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol 1, Lattice Press (2000) (“Wolf.1”)  |
| 1008B              | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 2, Lattice Press (2000) (“Wolf.2”) |
| 1008C              | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 3, Lattice Press (2000) (“Wolf.3”) |
| 1008D              | Stanley Wolf and Richard N. Tauber, <i>Silicon Processing For The VLSI Era</i> , Vol. 4, Lattice Press (2000) (“Wolf.4”) |
| 1009               | U.S. Patent No. 4,160,985 (“Kamins”)                                                                                     |
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| 1012               | U.S. Patent Application Publication No. 2002/0102783 (“Fujimoto”)                                                        |
| 1013               | Wang and Agrawal, <i>Single Event Upset: An Embedded Tutorial</i> , 21st Intl Conf on VLSI Design, IEEE 2008 (“Wang”)    |
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| 1018               | U.S. Pat. No. 11,316,014 (the “’014 Patent”)                                                                             |

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| 1022        | U.S. Patent Application Publication No. 2004/0063288 (“Kenney”)                                                                                                                                                                                                                                                                                                                                                                                     |
| 1023        | Jaeger, <i>Introduction to Microelectronic Fabrication</i> , Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) (“Jaeger”)                                                                                                                                                                                                                                                                                                         |
| 1024        | U.S. District Courts – Case Statistics, obtained at <a href="https://www.uscourts.gov/statistics-reports/analysisreports/federal-court-management-statistics">https://www.uscourts.gov/statistics-reports/analysisreports/federal-court-management-statistics</a> , per Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation” at n.4, dated June 21, 2022 |
| 1025        | U.S. Patent No. 4,435,896 (“Parrillo”)                                                                                                                                                                                                                                                                                                                                                                                                              |
| 1026        | L.C. Parrillo, R.S. Payne et al., <i>Twin-Tub CMOS - A Technology for VLSI Circuits</i> , IEEE 1980 (“Parrillo2”)                                                                                                                                                                                                                                                                                                                                   |
| 1027        | U.S. Patent Application Publication No. 2007/0045682 to Hong <i>et al.</i> (“Hong”)                                                                                                                                                                                                                                                                                                                                                                 |
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| 1039               | Parrillo IEEE Citation List                                                                                                                   |
| 1040               | Prosecution History of U.S. Pat. No. 8,421,195                                                                                                |
| 1041               | Rabaey <i>et al.</i> , <i>Digital Integrated Circuits, A Design Perspective</i> , Prentice Hall Electronics and VLSI Series (2003) (“Rabaey”) |
| 1042               | Sze, <i>Semiconductor Devices Physics and Technology</i> , 2d Ed., John Wiley & Sons (2002)                                                   |
| 1043               | Publication Declaration of Martin L. Knott for Rabaey (“Knott Decl.”)                                                                         |
| 1044               | Maziasz and Hayes, <i>Layout Minimization of CMOS Cells</i> , Kluwer Academic Publishers (1992) (“Maziasz”)                                   |
| 1045               | Publication Declaration of Sean O’Bryan for Maziasz (“O’Bryan Decl.”)                                                                         |
| 1046               | U.S. Patent No. 5,986,924 (“Yamada”)                                                                                                          |
| 1047               | U.S. Patent No. 8,421,195 to Rao (the “’195 Patent”)                                                                                          |

Petitioner Intel Corporation (“Intel or Petitioner”) requests *inter partes* review (“IPR”) of claims 7-11 (the “Challenged Claims”) of U.S. Patent No. 9,190,502 (Ex.1001, “the ’502 Patent”).

## **I. INTRODUCTION**

The ’502 Patent is directed to a Complementary Metal-Oxide Semiconductor (CMOS) device having graded dopant concentrations. Ex.1001, 4:52-67. This Petition demonstrates that the Challenged Claims are unpatentable as obvious.

## **II. MANDATORY NOTICES**

### **A. Real Party-In-Interest**

Intel Corporation is the real party-in-interest.

### **B. Related Matters**

The ’502 Patent is the subject of Civil Action No. 6:22-cv-105 in the Western District of Texas (“Texas Case”), filed January 27, 2022. That case, as it pertains to Petitioner, was recently transferred to the District of Oregon on December 21, 2022 (No. 3:22-cv-02001-JR). This Petition refers to these cases collectively as the “District Court Case.”

The ’502 Patent was the subject of prior Civil Action No. 2:19-cv-147 in the Eastern District of Texas (“EDTX Case”), which was terminated on July 9, 2020. Ex.1035. The ’502 Patent was also the subject of prior IPR2020-00290 filed on December 23, 2019, which was terminated on July 10, 2020, before an institution decision was reached. Ex.1036. Petitioner was not a party in the EDTX Case or in

IPR2020-00290.

Related U.S. Patent No. 10,734,481 (the “’481 Patent”) is the subject of *Intel Corporation v. Greenthread, LLC*, IPR2023-00260, filed November 28, 2022, and *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00375, filed December 17, 2022. Related U.S. Patent No. 10,510,842 (the “’842 Patent”) is the subject of *Intel Corporation v. Greenthread, LLC*, IPR2023-00308, filed December 5, 2022, and of *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00376, filed December 17, 2022. Related U.S. Patent No. 11,316,014 (the “’014 Patent”) is the subject of *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00325, filed December 12, 2022, and *Intel Corporation v. Greenthread, LLC*, IPR2023-00386, filed December 19, 2022. Related U.S. Patent No. 11,121,222 (the “’222 Patent”) is the subject of *Sony Group Corporation v. Greenthread, LLC*, IPR2023-00324, filed December 12, 2022, and *Intel Corporation v. Greenthread, LLC*, IPR2023-00420, filed December 28, 2022.

The following related patents were the subject of IPRs that were all terminated before an institution decision was reached: U.S. Patent No. 8,106,481 (IPR2020-00288); U.S. Patent No. 8,421,195 (IPR2020-00289); U.S. Patent No. 9,647,070 (IPR2020-00292 and IPR2020-00291). Petitioner was not a party in any of these IPRs.

**C. Counsel Service Information**

| <b>Lead Counsel</b>                                                                                                                                                                                                                       | <b>Back-Up Counsel</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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**D. 37 C.F.R. §42.8(b)(4): Service Information**

Intel concurrently submits a Power of Attorney, 37 C.F.R. §42.10(b), and consents to electronic service directed to the following email address:  
Intel\_Greenthread\_IPR@kirkland.com.

### **III. PAYMENT OF FEES UNDER 37 C.F.R. §42.103**

The undersigned authorizes the Office to charge the fee set forth in 37 C.F.R. §42.15(a)(1) for this Petition to Deposit Account No. 506092. Review of 5 claims is requested. The undersigned further authorizes payment for any additional fees that may be due in connection with this Petition.

### **IV. CERTIFICATION OF GROUNDS FOR STANDING**

Petitioner certifies under Rule 42.104(a) that the '502 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR of the Challenged Claims on the grounds identified in this Petition.

### **V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED**

#### **A. Prior Art Printed Publications**

The '502 Patent claims priority to September 3, 2004.<sup>1</sup> Petitioner's challenge is based on the following prior-art references, none of which were before the Patent Office during prosecution of the '502 Patent:

- **Payne** – U.S. Patent No. 4,684,971 to Payne (Ex.1005) issued on August 4, 1987 and is prior art under 35 U.S.C. §102(b).<sup>2</sup>
- **Sakai** – U.S. Patent No. 4,907,058 to Sakai (Ex.1006) issued on March 6, 1990 and is prior art under 35 U.S.C. §102(b).

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<sup>1</sup> Petitioner reserves the right to challenge the priority date in other proceedings.

<sup>2</sup> Cites to 35 U.S.C. §§102 and 103 are to the pre-America Invents Act (pre-AIA).

- **Kawagoe** – U.S. Patent No. 6,043,114 to Kawagoe et al., (Ex.1007) issued on March 28, 2000 and is prior art under 35 U.S.C. §102(b).
- **Wolf** – Stanley Wolf and Richard N. Tauber, *Silicon Processing*, Lattice Press (2000) (Ex.1008A-D), was published and publicly available no later than 2002, and is prior art under 35 U.S.C. §102(b).
- **Parrillo** - U.S. Patent No. 4,435,896 to Parrillo and Payne (Ex.1025) issued on March 13, 1984 and is prior art under 35 U.S.C. §102(b).

## **B. Relief Requested**

Petitioner requests cancellation of the Challenged Claims as unpatentable under 35 U.S.C. §103. The specific grounds of the challenge are set forth below and are supported by the declaration of Dr. Blalock (Ex.1003).

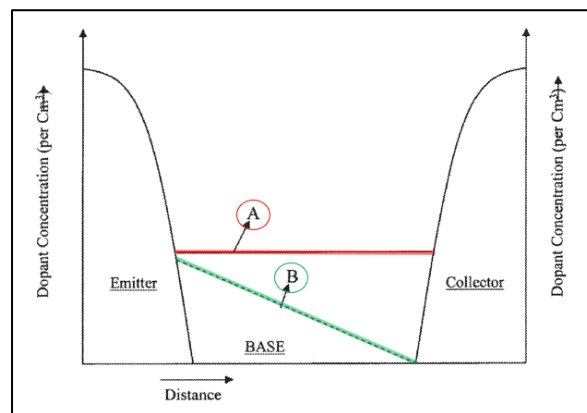
| <b>Ground</b> | <b>Basis</b> | <b>Challenged Claims</b> | <b>Reference(s)</b> |
|---------------|--------------|--------------------------|---------------------|
| I             | § 103        | 7                        | Payne               |
| II            | § 103        | 7-11                     | Sakai, Kawagoe      |
| III           | § 103        | 9-11                     | Payne, Wolf         |
| IV            | § 103        | 8                        | Payne, Parrillo     |

## **VI. THE '502 PATENT**

The '502 Patent is directed to “grading the dopant concentration” in certain regions of a semiconductor device. Ex.1001, Title, Abstract. The Challenged Claims claim that a single drift layer (SDL) and a well region of a semiconductor device

have graded dopant concentrations to aid movement of minority carriers from the surface layer to the substrate. *Id.*, Cl. 7.

The '502 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration “B” (green) in Figure 1 below is described as one of “the two most popular” doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile “A” (red). Ex.1001, 2:17-19.



Ex.1001, FIG. 1 (“Prior Art”).<sup>3</sup> The '502 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the movement of carriers, but alleges, without support, that prior attempts were met with “little success.” *Id.*, 1:63-2:9.

The claims of the '502 Patent issued after a terminal disclaimer was filed to overcome a double patenting rejection over the issued claims of the parent '195 Patent. Ex.1002, 50-53, 104. There were no prior art rejections. *Id.*, 53. During

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<sup>3</sup> All colors and colored annotations to figures added.

prosecution of the parent '195 Patent, the Examiner found that the prior art, including Kamins and Jastrzebski, teaches all the elements of then-pending independent claim 10. Ex.1040 (12/20/11 Office Action), 3–5; (8/13/12 Office Action), 3-5. In response, Applicant amended claim 10 to add an element which recites “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants ....” and which is substantially the same as current element [7.6]. Ex.1040 (10/15/12 Office Action Response), 3. The Examiner allowed the amended claim 10 (issued claim 1 of the '195 Patent) and claims depending therefrom, citing this added element as the reason for allowance of these claims. Ex.1040, (12/12/12 Notice), 2-3; Ex.1047, claim 1.

## **VII. PERSON OF ORDINARY SKILL IN THE ART**

A person of ordinary skill in the art (“POSITA”) of the subject matter of the '502 Patent would have had a Bachelor’s degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Ex.1003, ¶¶53-56. Additional education might compensate for a deficiency in experience, and vice-versa. *Id.*

## **VIII. CLAIM CONSTRUCTION**

Claims in an IPR are construed under *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). 37 C.F.R. §42.100(b). Ex.1033 lists proposed

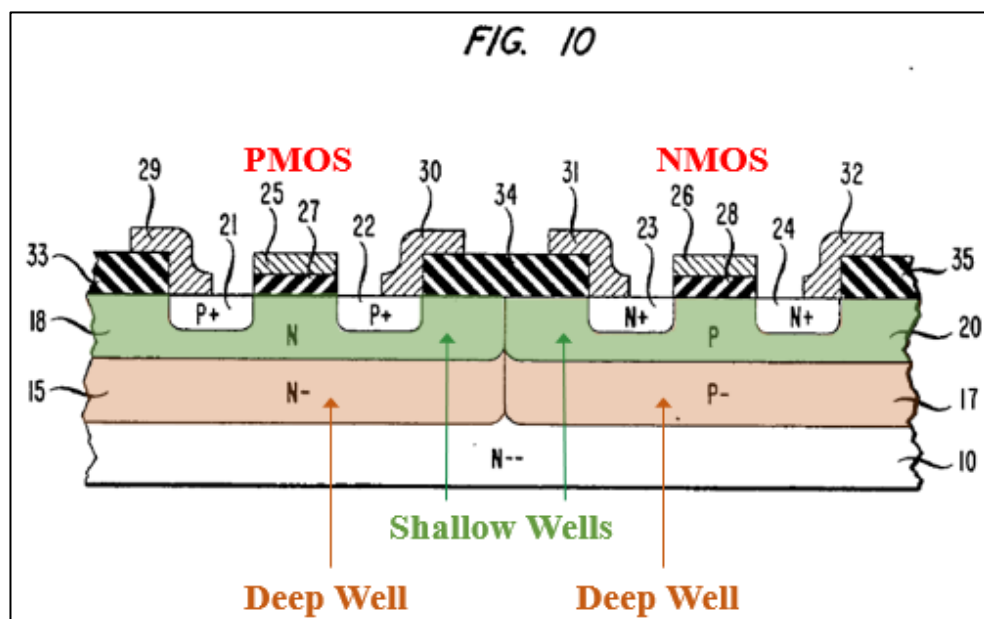
constructions in the District Court Case. Exs.1029-1032. In a tentative ruling in the Texas Case (in which Intel is no longer a party) issued in advance of the Markman hearing (canceled and not yet rescheduled), the District Court indicated that Patent Owner's plain-meaning constructions will likely be adopted. Ex.1037.

Petitioner does not believe any terms need be construed to resolve the issues presented in this Petition, as the Challenged Claims are unpatentable under either party's proposed constructions (except for "surface layer" which is addressed under Patent Owner's proposed construction). Ex.1003, ¶¶57-61.

## IX. OVERVIEW OF THE PRIOR ART

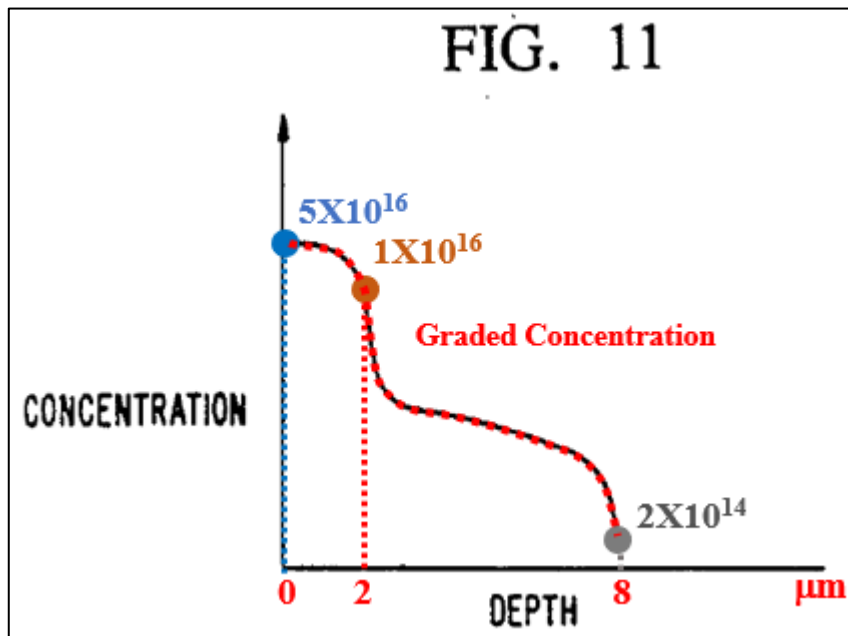
### A. Payne

Payne teaches forming a nested well structure, whereby shallow wells (18 and 20) of "greater impurity concentration" are formed in deep twin-wells (15 and 17), as shown below. *Id.*, 1:5-15, 1:51-2:2, 5:18-55, 6:35-51.



*Id.*, FIG. 10; *id.*, 2:3-28, 2:56-5:21, 5:44-50, FIGS. 2-9.

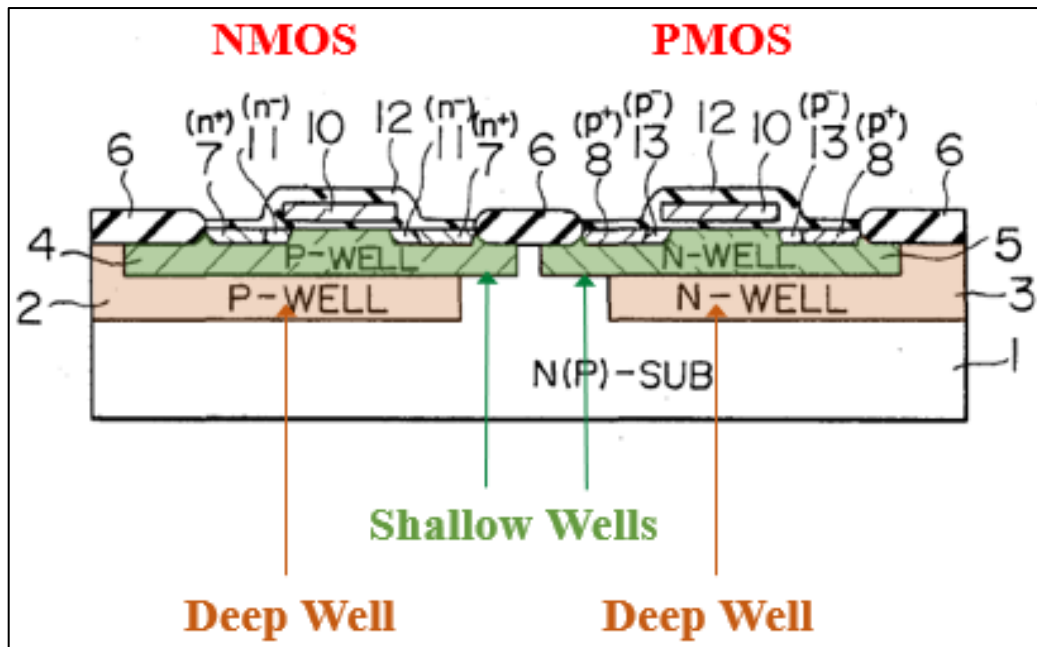
Payne further teaches that the nested well structure has a graded dopant concentration (“high-low implant profile”) that decreases with depth, as shown below in Figure 11. *Id.*, 2:38-41, 5:14-17, 5:51-57 6:7-17, FIG. 11.



*Id.*, FIG. 11; *id.*, 2:56-59, 5:48-55; §X.A.1.f.

## B. Sakai

Like Payne, Sakai discloses the use of a nested well structure (“twin double well structure”) in CMOS devices to achieve high-packing density. Ex.1006, 1:6-13, 1:55-2:5, 2:51-3:7, 7:19-37, 8:9-24. Figure 10 below illustrates Sakai’s “twin double well structure,” and shows “shallow P-well” 4 and “shallow N-well” 5 (green) formed in a surface portion of “deep P-well” 2 and “deep N-well” 3 (tan), respectively. Ex.1006, 1:53-2:39, 5:53-6:19.

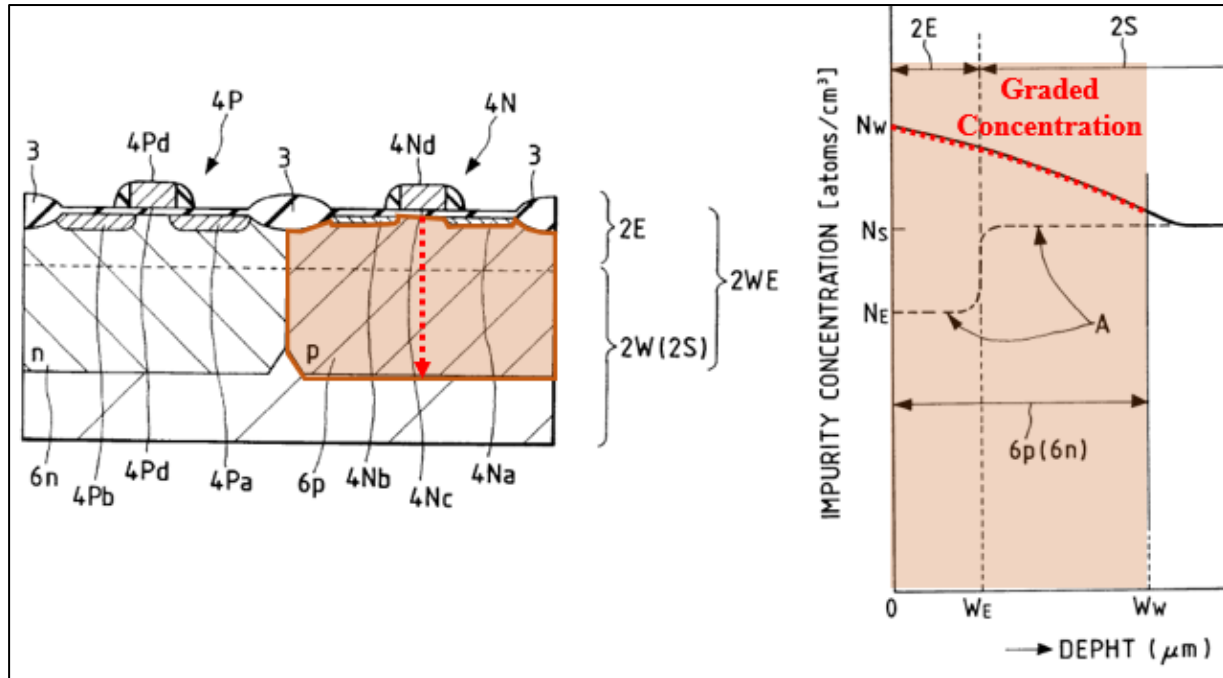


*Id.*, FIG. 10D. Sakai further discloses that the dopant concentration in the shallow wells is greater than the dopant concentration in the deep wells. *Id.*, 5:56-6:4.

### C. Kawagoe

Kawagoe discloses a CMOS device in which wells have graded dopant concentrations that decrease with depth, as illustrated below right. Ex.1007, 14:46-55, 15:26-40, 15:62-16:40 (“p-well 6p and n-well 6n have their impurity concentrations *gradually lowered* in the depthwise direction ...”).<sup>4</sup>

<sup>4</sup> All emphases added unless otherwise noted.



*Id.*, FIGS. 17, 23 The graded dopant concentrations reduce soft errors by sweeping unwanted carriers into the substrate body. *Id.*, 16:2-11 (“electrons produced by the  $\alpha$ -ray are *attracted to the substrate body 2S* by that concentration gradient ... so that the soft errors can be reduced ...”).

## X. SPECIFIC GROUNDS FOR PETITION

### A. Ground I:

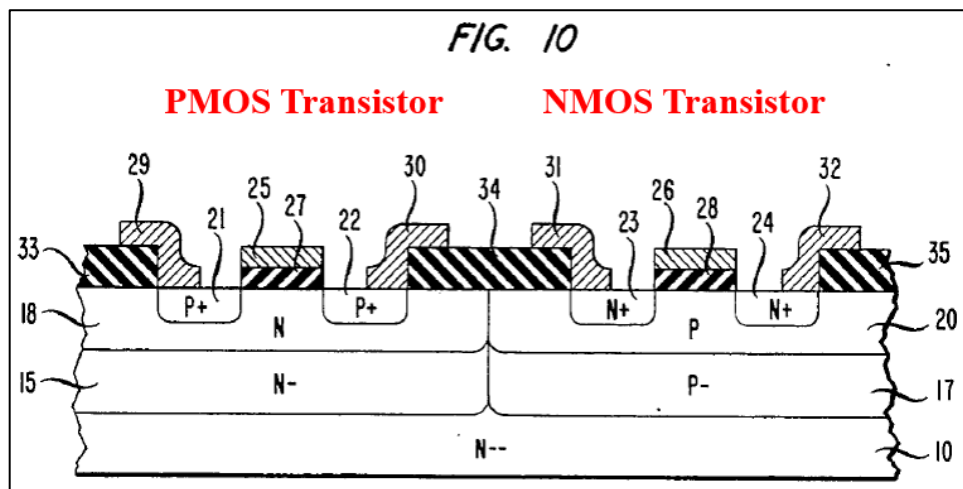
Payne renders claim 7 obvious. Ex.1003, ¶¶69-121.

#### 1. Independent Claim 7

##### a. Preamble: “A semiconductor device comprising:”

Payne is directed to a semiconductor device. Ex.1003, ¶70; Ex.1005, Title, Abstract, 1:51-54 (“it is a primary object of the invention to provide a CMOS structure and method of manufacture which requires little semiconductor space and

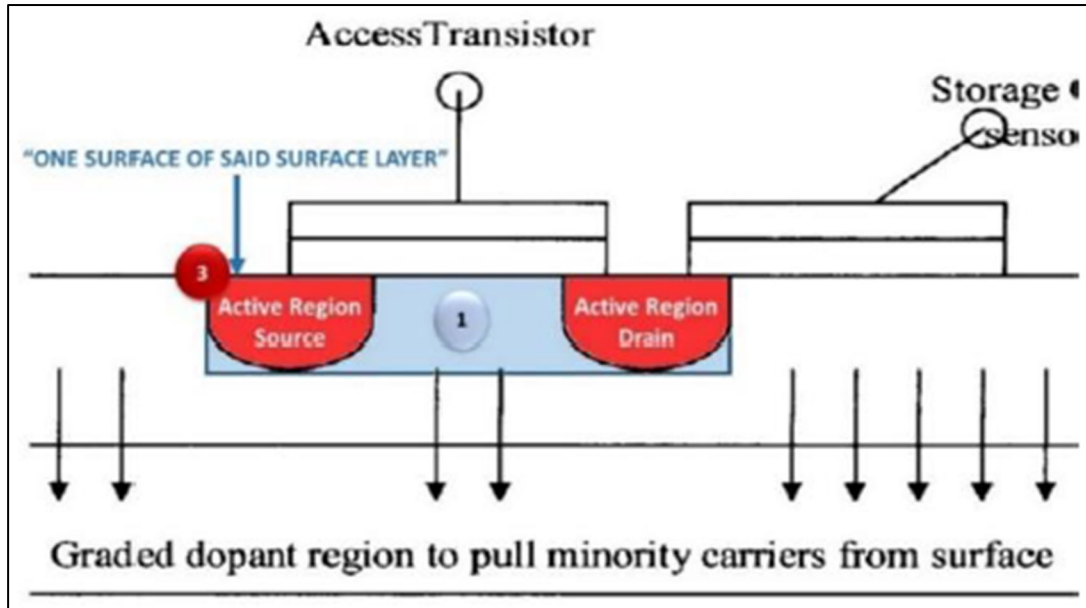
therefore permits a high packing density.”), 1:5-15 (“Complementary field effect transistors (hereinafter designated CMOS) [] comprise n-channel and p-channel devices ...”). Payne Figure 10 illustrates a “p-channel” (PMOS) transistor (with “P+” source/drain regions 21/22) adjacent to an “n-channel” (NMOS) transistor (with “N+” source/drain regions 23/24) of a CMOS semiconductor device. *Id.*, 2:50-60, 5:18-34, 6:57-59.



Ex.1005, FIG. 10.

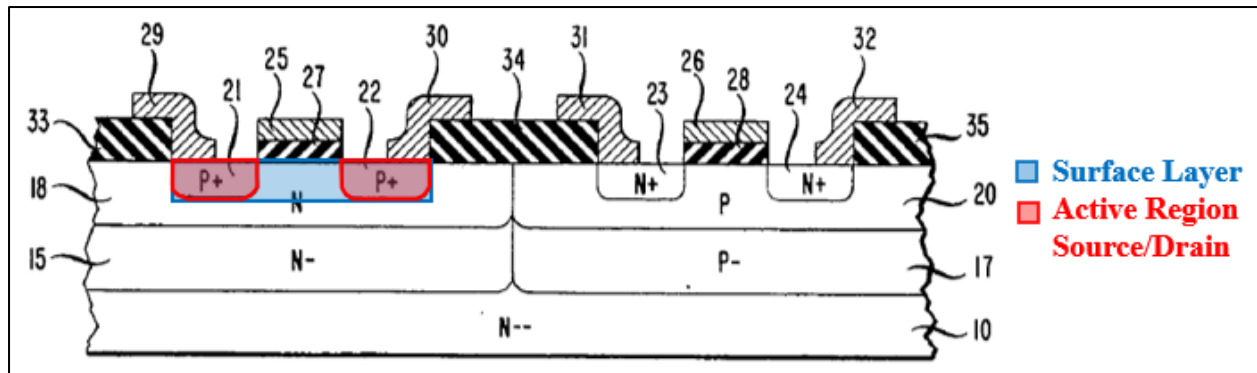
**b. Element [7.1]: “a surface layer;”**

Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶71-73. According to Patent Owner (“PO”), a “surface layer” is “a layer at the surface of the silicon” (also phrased as “a layer at the surface of the semiconductor device”)—which PO annotated in blue in Figure 5(b) below—“where the active region [(red)] is located.” Ex.1030, 6, 9, 12, 13; Ex.1033.



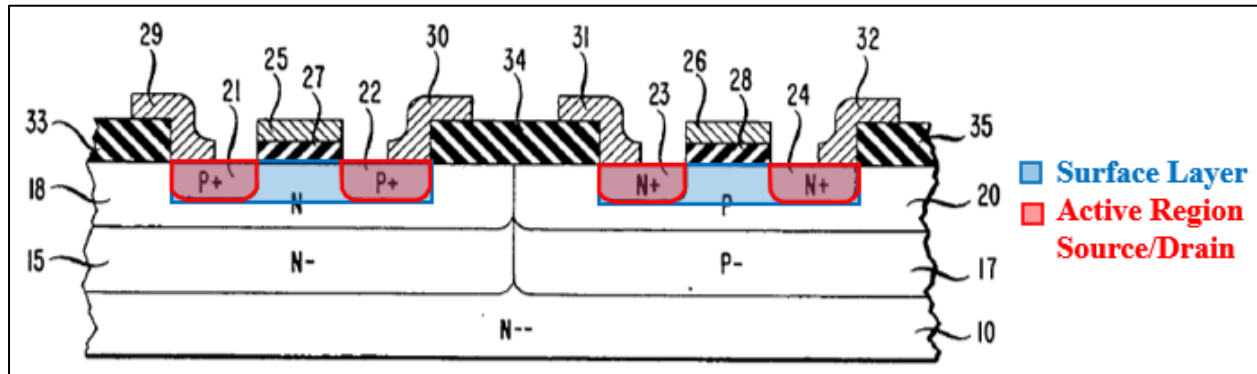
Ex.1001, Fig. 5(b); Ex.1030, 7, 12.

Payne satisfies element [7.1] to the same extent that Figure 5(b) meets it. Ex.1003, ¶72. Payne's Figure 10 discloses a surface layer (blue) that matches the surface layer PO identified in Figure 5(b). Payne's surface layer is at the surface of Payne's silicon substrate 10, and the "source and drain regions, 21 and 22 [(red)] of P+ conductivity" of Payne's p-channel transistor (left) are located in it. Ex.1005, 2:50-60; 5:21-27, 6:57-59, FIG. 1.



Ex.1005, FIG. 10. Payne likewise discloses a surface layer containing the "source

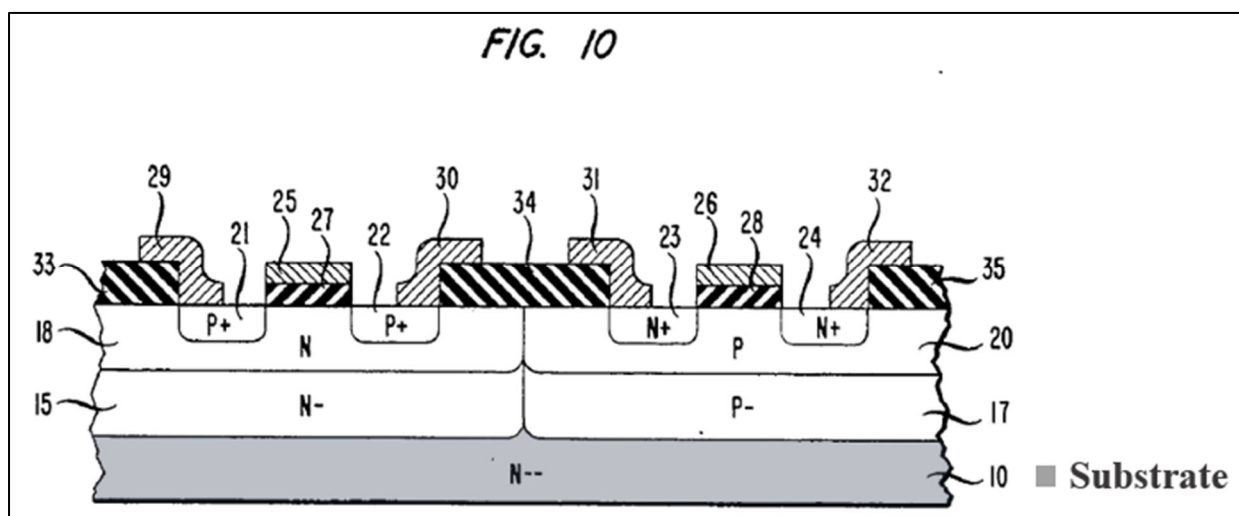
and drain regions, 23 and 24, of N+ conductivity” of Payne’s n-channel transistor (right). *Id.*, 5:24-27, 6:57-59; Ex.1003, ¶73.



Ex.1005, Fig. 10.

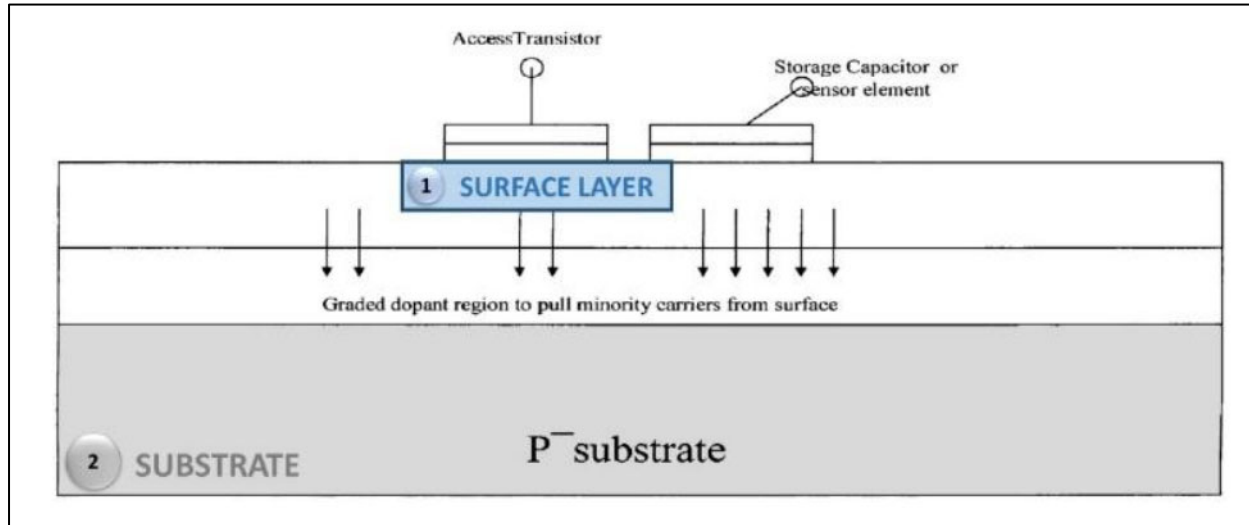
**c. Element [7.2]: “a substrate;”**

Payne discloses this element. Ex.1003, ¶¶74-76. Payne’s Figure 10 illustrates a CMOS device “fabricated in a silicon semiconductor *substrate* [(grey)], 10 of ‘N-’ conductivity type which typically has a doping concentration of approximately  $1-2 \times 10^{14}$  ions/cm<sup>3</sup>[.]” Ex.1005, 1:60-65, 2:50-60.



Ex.1005, FIG. 10.

Payne satisfies element [7.2] under PO's proposed construction of "plain and ordinary meaning, where the plain and ordinary meaning is 'an underlying layer.'" Ex.1033. Payne's substrate also matches PO's identification of the substrate (grey) in Figure 5(b) of the '502 Patent.

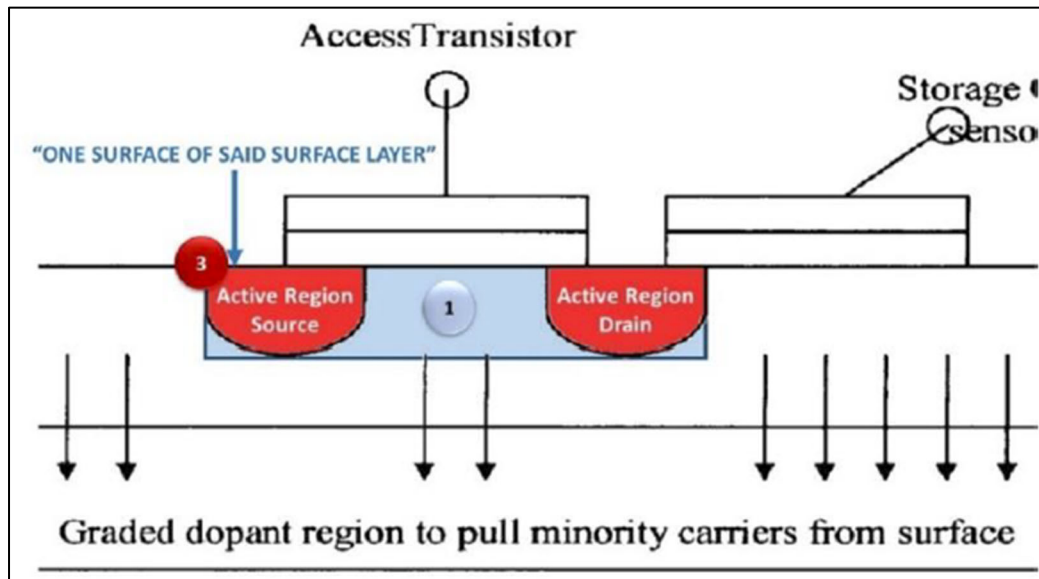


Ex.1030, 6-7, 16-17 (well region and drift layer can be part of substrate); Ex.1001, FIG. 5(b).

Payne also satisfies this element under Petitioner's proposed construction that a substrate is "the initial material within which or on which the semiconductor device is fabricated." Ex.1033; Ex.1003, ¶76. Payne's substrate is the initial material within which or on which Payne's semiconductor device is later fabricated. Ex.1005, 1:60-65, 2:50-60 ("the [CMOS] device is fabricated in a silicon semiconductor substrate, 10"), FIGS. 1, 10.

- d. **Element [7.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"**

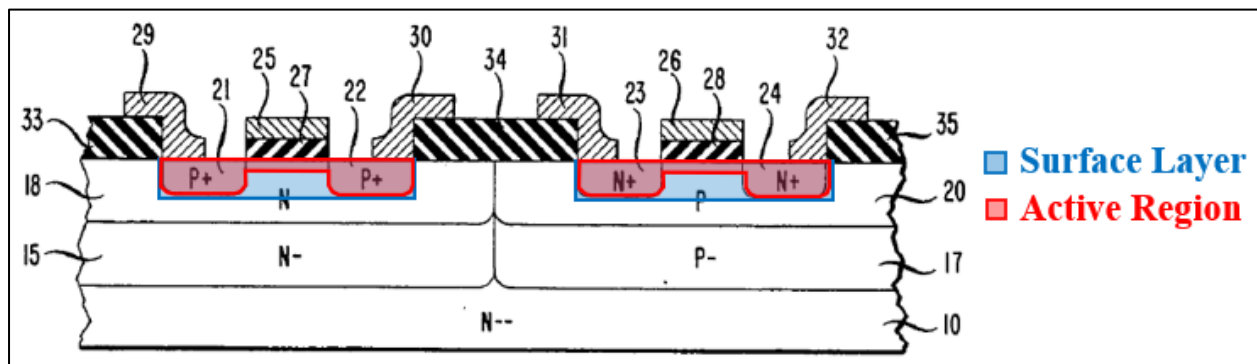
Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶77-82. According to PO, Figure 5(b) of the '502 Patent depicts an active region (red) “disposed on one surface [(top surface)] of said surface layer,” as shown below:



Ex.1001, FIG. 5(b); Ex.1030, 6-7, 11 (“[T]he ‘active region’ is part of the ‘surface layer’ ... When the claim says the active region is ‘disposed on one surface of the surface layer,’ it means the active region is located on the ‘ceiling’ of the silicon *inside* the silicon.”) (emphasis in original), 12.

Payne satisfies element [7.3] under PO’s interpretation. Ex.1003, ¶¶78-80. Payne’s Figure 10 below illustrates a “p-channel” transistor with source/drain regions 21/22 (left), and an “n-channel” transistor with source/drain regions 23/24 (right). Ex.1005, 5:18-29, 1:5-19, 6:57-59. These source/drain regions are formed with “a surface impurity concentration of approximately  $10^{19}$ - $10^{20}$  ions/cm<sup>3</sup>.” *Id.* 5:21-29, 1:43-45. The channel region between these source and drain regions is part

of the surface region, which has an impurity concentration of “typically  $0.5\text{-}5 \times 10^{16}$  ions/cm<sup>3</sup>.” *Id.*, 5:51-52, 4:31-39, 4:63-5:5. The source/drain regions of a transistor, together with the channel region in between them, form an active region. Ex.1003 ¶¶79-80; Ex.1008B, 299 (“The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The **active regions** are those in which transistor action occurs; i.e., the **channel** and the heavily doped **source** and **drain** regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e). The active region (red) of each of Payne’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in PO’s annotated Figure 5(b) above. Ex.1003, ¶80; §X.A.1.b.

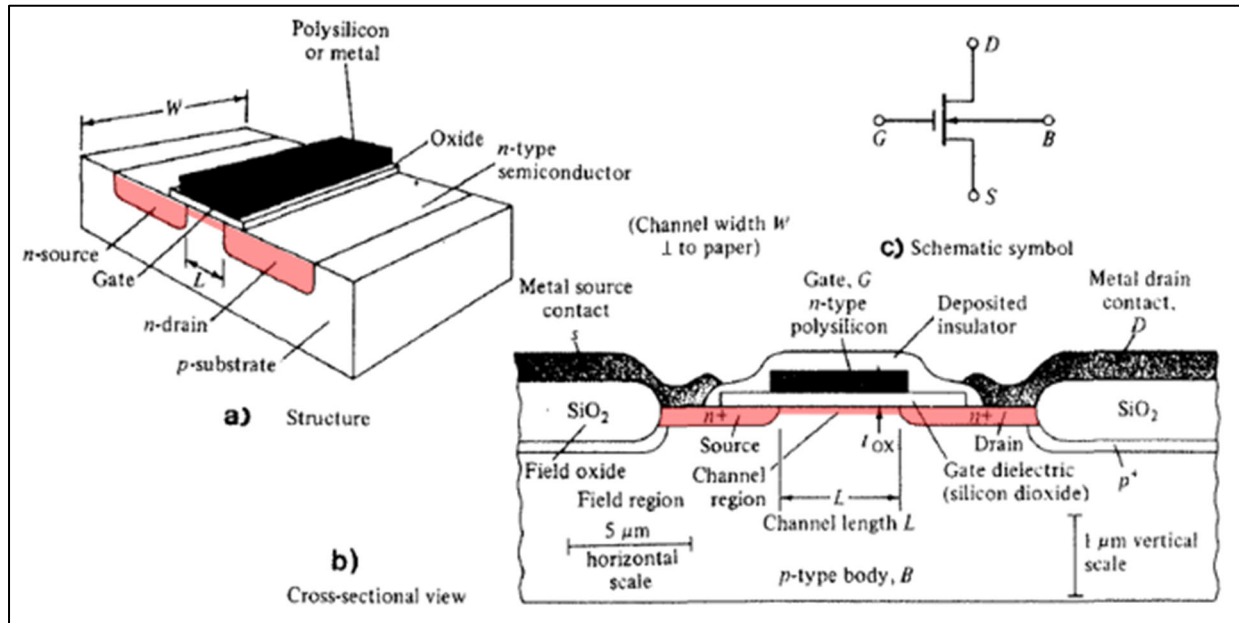


Ex.1005, FIG. 10.

Payne satisfies element [7.3] under PO’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (e.g., the source and drain and silicon between them) where a transistor can be formed” (Ex.1033) because the active region of a MOS transistor is “[its] channel and [its]

*heavily doped* source and drain regions,” highlighted in red in the figure below.

Ex.1008B, 299; Ex.1003, ¶81.

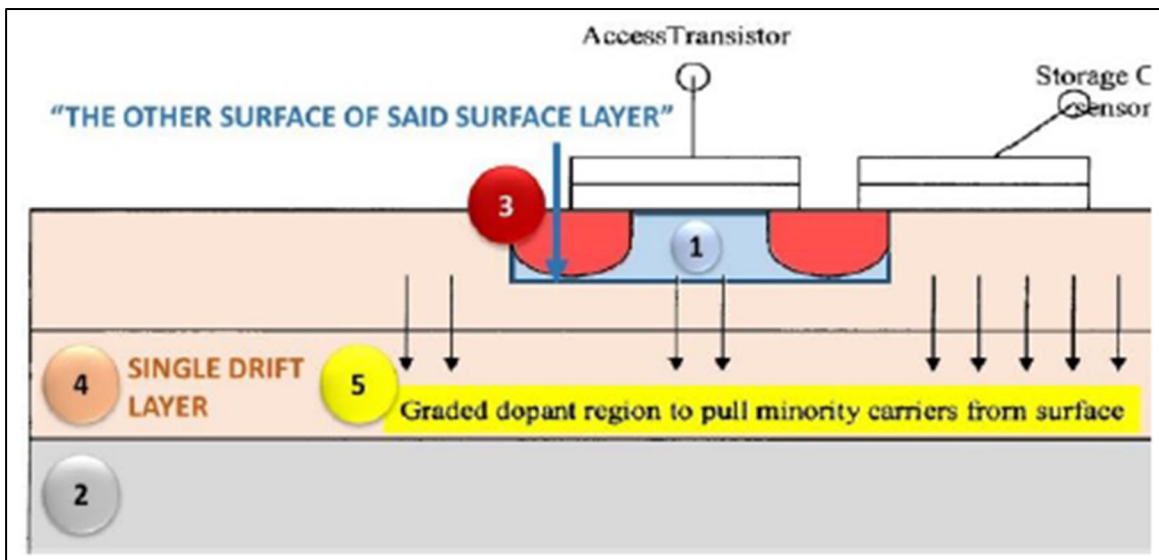


Ex.1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4. Payne also satisfies this claim element under Petitioner’s proposed construction that an active region is the “region that forms the current path of a device” or “the source, drain and channel region of a device” because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Ex.1033; Ex.1008B, 299-301, FIGS. 5-1, 5-2; Ex.1008D, 197, FIG. 5-13; Ex.1003 ¶82. PO does not dispute this. Ex.1030, 3-4 (“when a positive voltage is applied to the gate ... a conductive *channel* [is formed] between the *source* and the *drain*, and *current* can begin to flow through the transistor”).

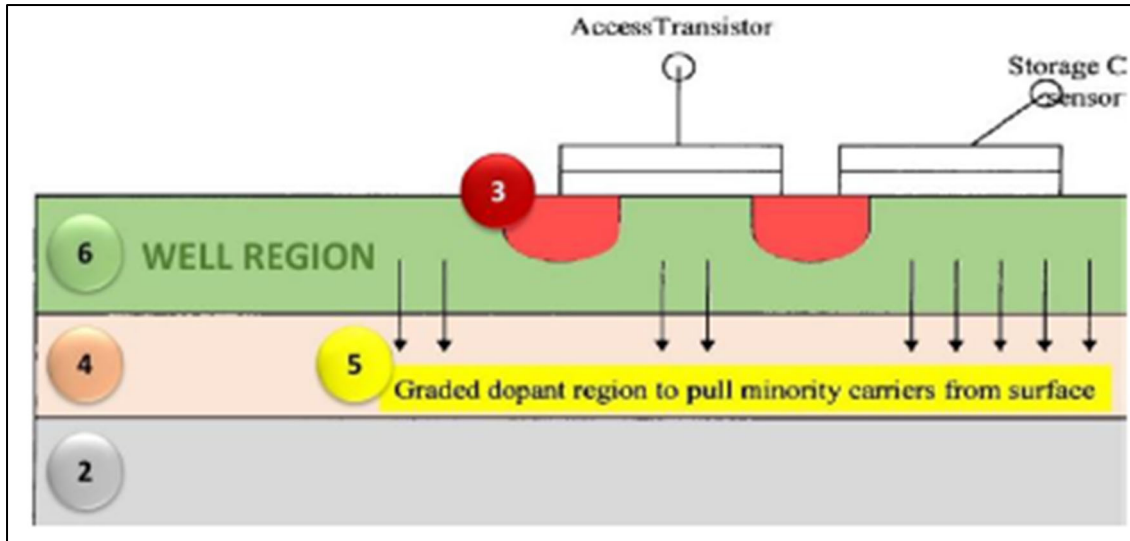
- e. **Element [7.4]: “a single drift layer disposed between the other surface of said surface layer and said substrate,”**

Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶83-87.

**Single drift layer (“SDL”)** – In its claim construction brief, PO identified the single drift layer in tan in Figure 5(b). Ex.1030, 7. According to PO, the SDL (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:

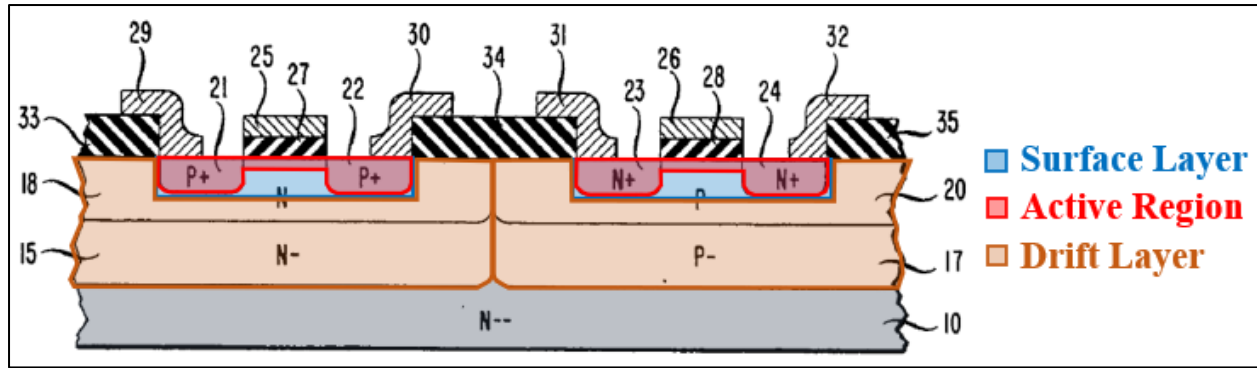


Ex.1001, FIG. 5(b); Ex.1030, 7. The SDL in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* Element [7.6]), and as shown below:



Ex.1001, FIG. 5(b); Ex.1030 at 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

Payne discloses a SDL to the same extent the ’502 Patent’s Figure 5(b) does. Ex.1003, ¶¶84-86. In Payne’s Figure 10, the “**first tub region**” **15 (tan)** of Payne’s nested well structure—with shallow well (“surface region”) 18 disposed in it—is an example of the claimed SDL. *Id.*; Ex.1005, 3:28-42 (ion implantation for tub 15), 4:19-30 (thermal drive-in to achieve the desired depth for tub 15), 4:31-39, 5:7-17, 5:44-48, 5:48-50 (“In a typical device, the final depth of surface regions 18 and 20 would be approximately 1-2 $\mu$  and the depth of the **tub regions 15 and 17** would be typically 3-8 $\mu$ .”). This SDL (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]” under PO’s interpretation, and in exactly the same way as depicted in PO’s annotated Figure 5(b) above.



Ex.1005, FIG. 10. Payne’s tub 17 (right), in which shallow well 20 is disposed, is likewise a SDL (tan) disposed between a surface layer (blue) and the substrate (grey). Ex.1005, 4:3-30, 4:63-5:17, 5:44-50; Ex.1003, ¶86; §X.A.1.b.

Payne meets all other claim requirements associated with the SDL to the same extent Figure 5(b) meets them. *See* below and elements [7.5]-[7.6]; Ex.1003, ¶87. Notably, as detailed in element [7.5], each of Payne’s tubs 15/17 is a *single* drift layer because it has a graded-dopant concentration that, according to PO, generates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. Ex.1030, 7: Ex.1040, 253-54, 289-290; §X.A.1.f.

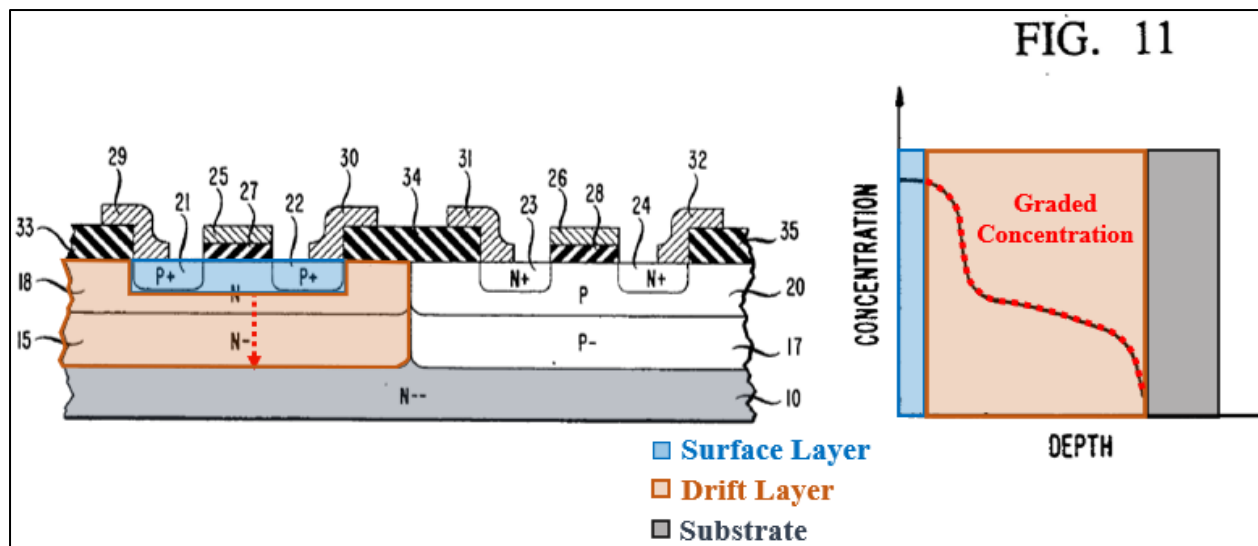
- f. **Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”**

Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶88-108.

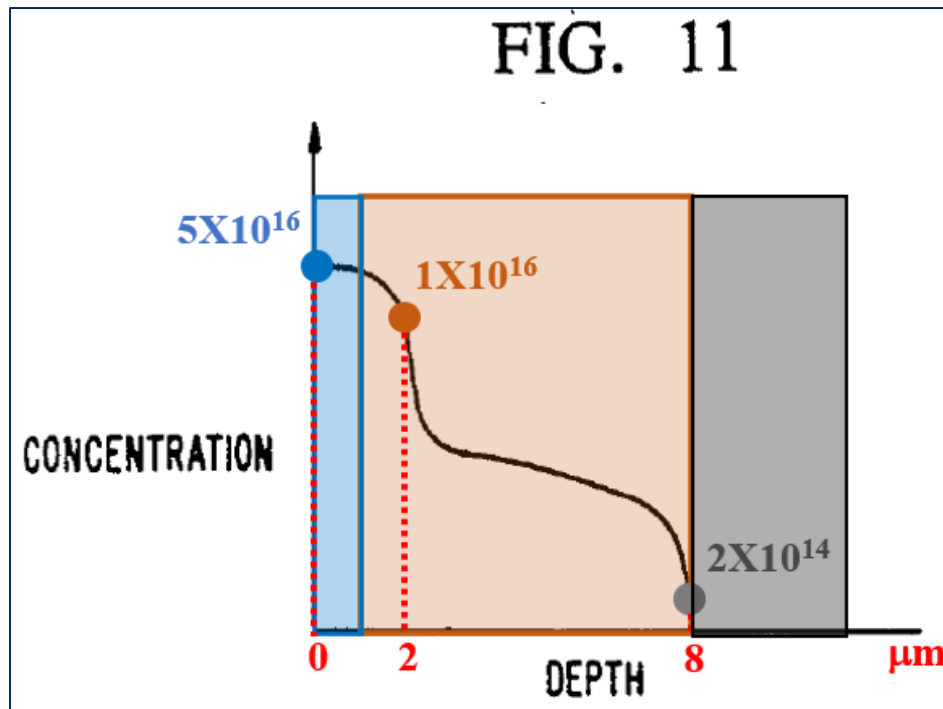
**Graded dopant concentration** – The '502 Patent admits that graded-dopant concentrations were known, Ex.1001, 2:17-19, FIG. 1 (“Prior Art”), and that it was known to grade the dopant concentration in CMOS devices to affect the movement of minority carriers. *Id.*, 1:34-2:5, FIGS. 3(a)-3(d) (all “Prior art”). Payne’s SDL has a graded-dopant concentration extending between the surface layer and the substrate. Ex.1003 ¶89. Payne explains that the “impurity profile in both tubs [15/17] thereby has the general shape illustrated in FIG. 11” which exhibits “[t]he major advantage” of a “***high-low implant profile***.” Ex.1005, 2:38-41, 5:14-17, 5:56-57. Payne’s Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left), which starts at the bottom of the surface layer (blue) and extends to the substrate (grey). As shown below, Payne discloses a downward-sloping graded-dopant concentration in the SDL (tan) associated with Payne’s PMOS transistor (left).<sup>5</sup>

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<sup>5</sup> *Kingsford Prod. Co., LLC v. Creative Spark, LLC*, No. IPR2016-01831, Paper 32 at 32 (P.T.A.B. Mar. 9, 2018) (“Figures that are not drawn to scale may be relied upon to disclose ***qualitative relationships*** between measured quantities, even though they may not be relied upon to disclose precise quantitative relationships between those same quantities ...”).



Ex.1005, FIGS. 10-11. Dr. Blalock has annotated Figure 11 to reflect exemplary (maximum) dopant concentrations at various depths disclosed in Payne: (1)  $5 \times 10^{16}$  ions/cm<sup>3</sup> at the surface of the shallow wells (depth 0 μm), (2)  $10^{16}$  ions/cm<sup>3</sup> at a depth of ~2 μm (corresponding to the boundary of the deep and shallow wells), and (3)  $2 \times 10^{14}$  ions/cm<sup>3</sup> at a depth of ~8 μm (corresponding to the boundary of the substrate and the deep wells). Ex.1003, ¶¶91-92.

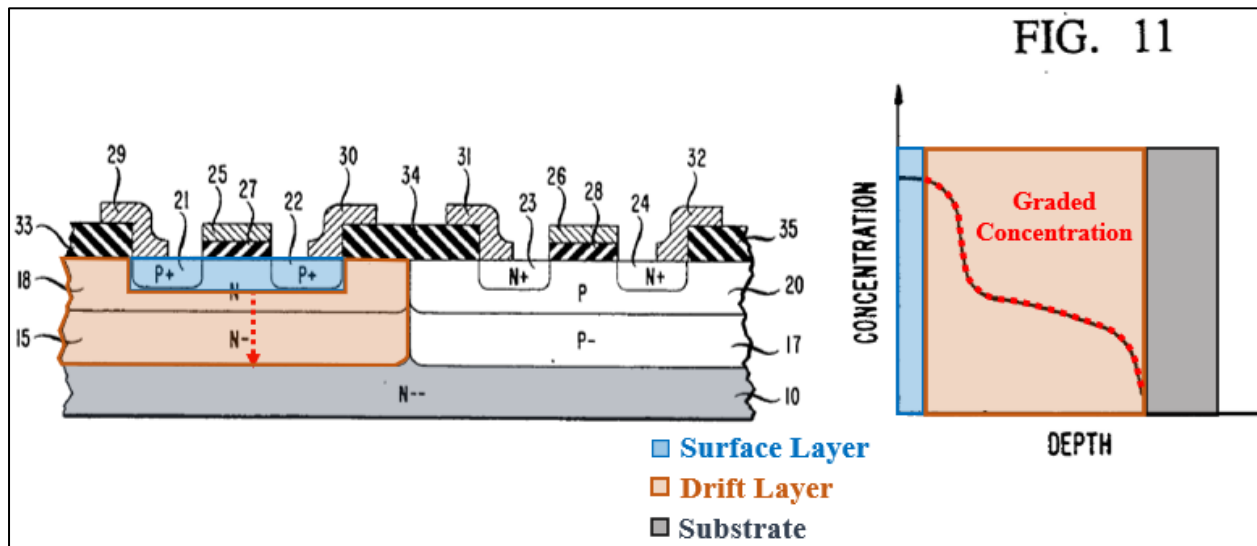


Ex.1005, FIG. 11. Indeed, Payne explains that “[t]he surface impurity concentration of the surface regions [18/20] is typically  $0.5\text{-}5 \times 10^{16}$  ions/cm<sup>3</sup> and that [the surface impurity concentration] of the tub regions [15/17] is typically  $10^{15}\text{-}10^{16}$  ions/cm<sup>3</sup>, with the former concentration being *at least twice as much* as the latter over these ranges.” *Id.*, 5:51-55. The concentration is lowest at the substrate, where it is “ $1\text{-}2 \times 10^{14}$  ions/cm<sup>3</sup>.” *Id.*, 2:56-59. Payne also explains that “the final depth of surface regions 18 and 20 would be approximately 1- $2\mu$  and the depth of tub regions 15 and 17 would be typically 3- $8\mu$ .” *Id.*, 5:48-50.

While the above discusses the SDL associated with Payne’s PMOS transistor (left in Figure 10), Payne teaches that the SDL associated with Payne’s NMOS transistor (right) also has a downward-sloping graded dopant concentration.

Ex.1005, 5:14-17; Ex.1003, ¶93.

**First static unidirectional electric drift field to aid the movement of minority carriers** - As shown below, Payne's SDL (tan) has a downward-sloping graded-dopant concentration extending between the surface layer (blue) and the substrate (grey).



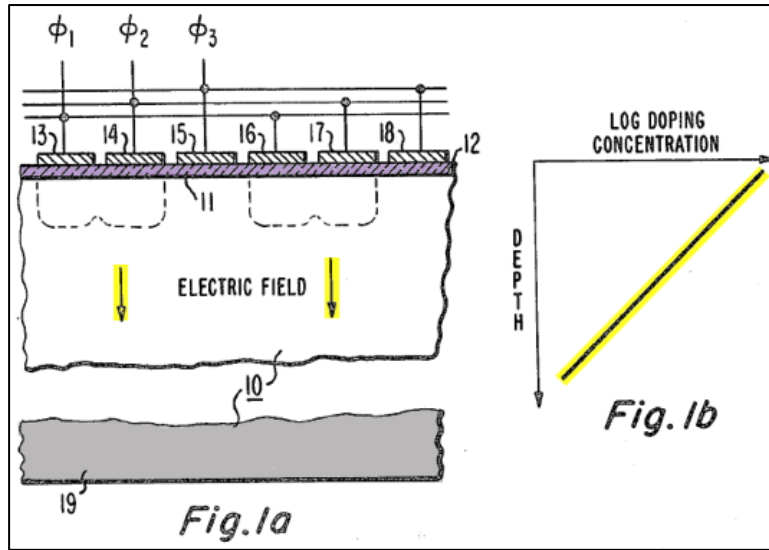
Ex.1005, FIGS. 10-11.

Payne's downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. Ex.1003, ¶¶94-99. During prosecution of the parent '195 Patent, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep

into the substrate (while an upward-sloping concentration, not at issue in Payne, would move those carriers in the opposite direction towards the surface):

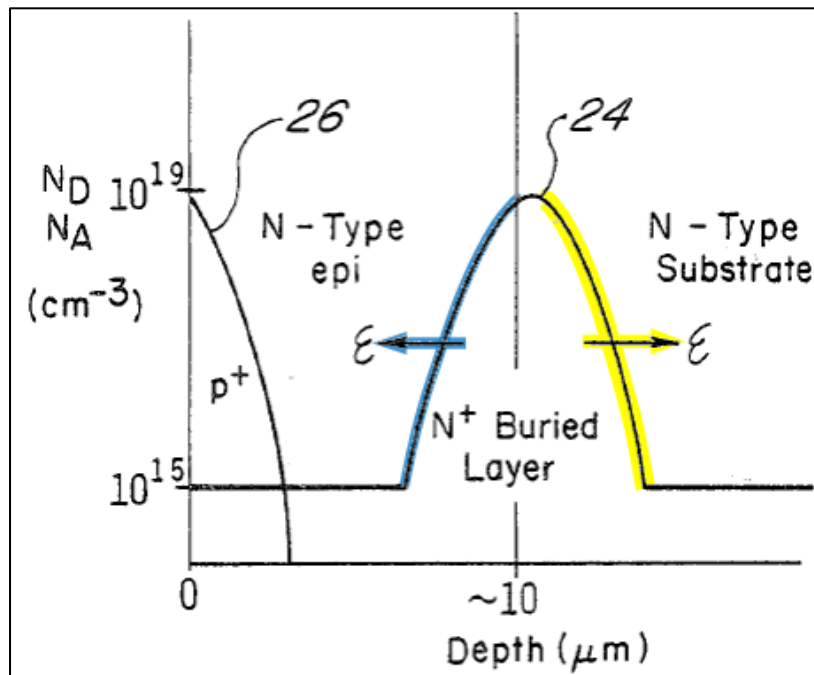
[T]he graded dopant concentration itself creates a ‘***built-in***’ ***electrical field*** that forces the movement of carriers into a particular direction, whereby ***the ‘direction’ of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

Ex.1040, 289-290 (underlining in original); Ex.1003, ¶95. Applicant further represented that “a unidirectional drift (electric) field necessarily affects ***all*** the present ***minority*** carriers in the same way.... Depending on the particular slope of the graded concentration of dopant, ***all minority*** carriers are either ***swept*** ‘down’ ... or ‘up...’” Ex.1040, 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the graded-dopant concentration is “decreasing with depth” from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex.1010, 5:14-22. Jastrzebski teaches that this downward-sloping graded-dopant concentration generates an electric drift field that “force[s] most of the charge carriers ... ***deep into the substrate***[.]” *Id.*, 5:14-22; *id.*, 2:27-32 (“This is done by creating a field, such as a drift field, in the semiconductor substrate to ***sweep minority charge carriers...into the bulk [substrate], away from the electrode-bearing surface of the substrate.***”).



Ex.1010, FIGS. 1a-1b. Applicant made the same representation to the Patent Office regarding Kamins. Ex.1040, 237-238, 253-254. According to Applicant, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. *Id.*, 237, 253 (citing Ex.1009, 3:6-13, FIGS. 2-3). Applicant explained that Kamins "show[s] **minority carrier[s] accelerated into the substrate.**" *Id.*, (citing Ex.1009, FIG. 2 and quoting Ex.1009, 3:6-13 ("carriers... accelerated... **away from the surface... into the substrate**")). According to Applicant, the electric field associated with the downward-sloping graded concentration at depth beyond  $\sim 10\mu\text{m}$  (red) causes "[minority] carriers created [in that region to be] ... **accelerated into the substrate** ...." *Id.* (citing Ex.1009, 3:6-13, FIGS. 2-3); Ex.1030 at 24 (Kamin's "bottom electric field [(yellow)] draws a **minority carrier** from the substrate to a **deeper** part of the substrate."); Ex.1009,

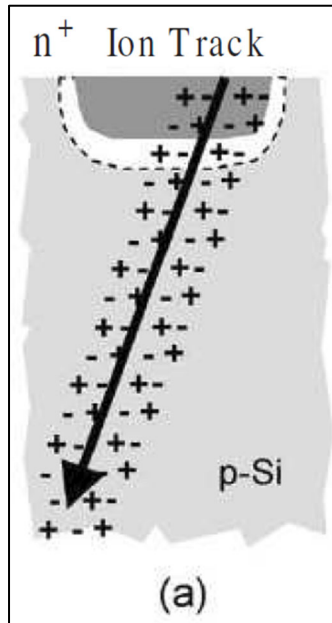
2:67-3:14 (“The non-uniform dopant concentration in the substrate creates electric fields in the substrate, indicated by arrows labeled ‘ $\epsilon$ ’ in FIGS. 2 and 3” such that “[minority] carriers created below the maximum dopant concentration are accelerated into the substrate.”), FIG. 2 (referring to these carriers as “photogenerated minority carriers”), 2:11-16 (same).



Ex.1009, FIG. 3.

Dr. Blalock explains that during a so-called single event upset (SEU), an  $\alpha$ -ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. Ex.1003, ¶100; Ex.1013, 431 (“A[n] [ $\alpha$ -]particle can induce SEU when it strikes at the **channel region** of an off NMOS transistor or the **drain region** of an off PMOS transistor.”), FIG. 2. As shown in Figure 2, such event generates both types of carriers (holes, denoted “+” and

electrons, denoted “-”), one of which will be the minority carrier in any given surface layer. Ex.1003, ¶100.



Ex.1013, FIG. 2(a).

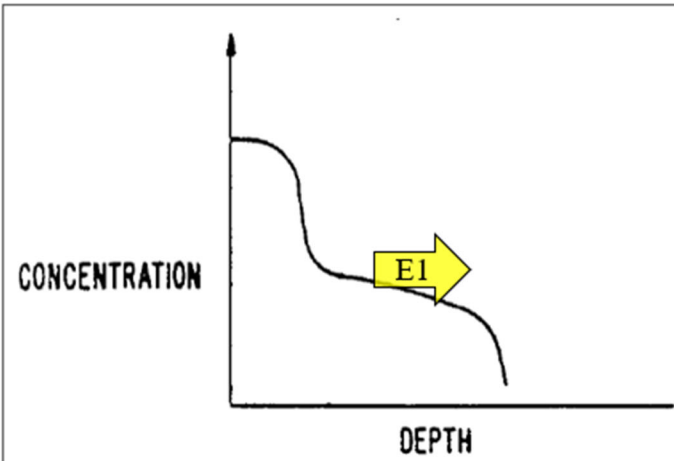
Like Jastrzebski and the right-hand side of Kamins Figure 3 (yellow), Payne’s graded dopant concentration is downward-sloping, as shown in Figure 11. Moreover, this graded-dopant profile is determined by the ion implantation and drive-in steps of the chip fabrication processes (those steps are described in Payne in relation to Figures 2 and 5-9 in particular) and thus the profile (and any resulting electric field) is static—it is set once the device has been fabricated and does not change afterwards. Ex.1003, ¶¶101-102; Ex.1005, 5:7-17, 5:44-55 (describing “the *final* depth” of tubs and surface regions and their typical ranges of impurity concentrations). During prosecution of the parent ’195 Patent, Applicant described

“static” similarly, conceding that “Kamins (US 4,160,985), just like Applicant, discloses the presence of a ‘static’ drift field, ‘because the drift field is created by graded concentration of dopants which does not change over time.’” Ex.1040, 318 (citing Ex.1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and Ex.1040, 302-03), 333 (same).

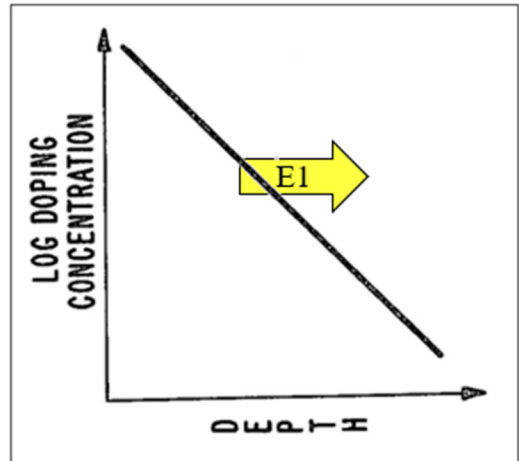
Thus, according to Jastrzebski, Kamins, Applicant, and PO, Payne’s profile generates a (first) “built-in” static unidirectional electric drift field (illustrated by the yellow arrow labelled “E1” below left) that aids the movement of minority carriers from the surface layer to the substrate.<sup>6</sup> Ex.1003, ¶¶102-103.

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<sup>6</sup> The figures of this Petition depict electric fields in N-wells, *e.g.*, Payne’s nested N-wells 15/18 or Sakai’s nested N-wells 3/5. §§X.A.1.g, X.B.1.f-g, X.B.2, X.D.1. The electric fields would be pointing in the opposite direction in Payne’s and Sakai’s nested P-wells. In both cases, these electric fields result from the downward-sloping graded concentrations in Payne’s and Sakai’s N-wells and P-wells and aid the movement of minority carriers (holes in N-wells, electrons in P-wells) downward to the substrate. *Id.*; Ex.1003, ¶¶104-105.

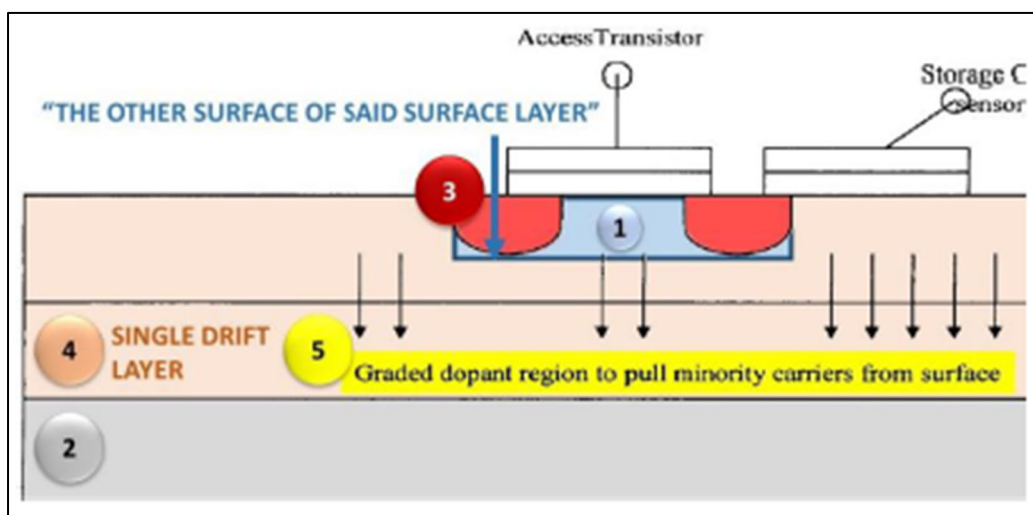


Ex.1005, FIG. 11



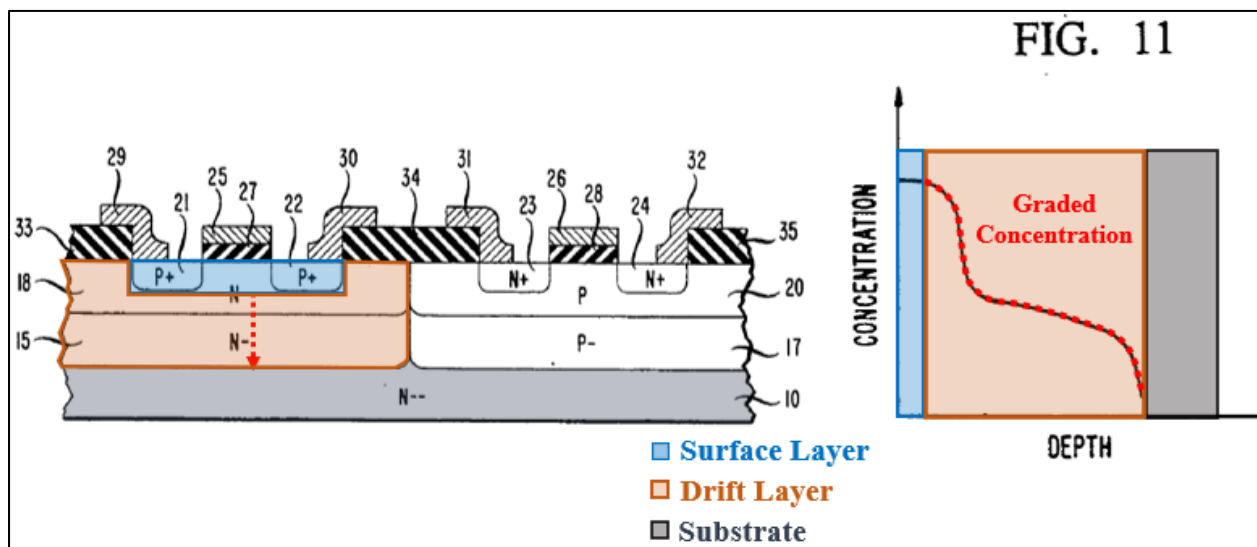
Ex.1010, FIG. 1b

Notably, Payne satisfies element [7.5] to the same extent the '502 Patent's Figure 5(b) meets it. Ex.1003, ¶¶104-106. While the '502 Patent does not disclose any single drift layer's dopant profile, PO contends that annotated Figure 5(b) below shows that "[t]he single drift layer has a graded concentration of dopants ... [that] create[s] an electric field that aids the movement of minority carriers [] from the surface layer to the substrate." Ex.1030, 7.



Ex.1001, FIG. 5(b); Ex.1030, 7.

In light of the above, Payne satisfies element [7.5] under PO’s plain-meaning constructions. Ex.1033; Ex.1003, ¶¶104-107. Payne’s Figure 11 shows a graded-dopant concentration that is downward-sloping over the entire SDL (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the SDL—and thus, according to PO (and also in light of Applicant’s representations to the Patent Office discussed above), this graded-dopant concentration generates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex.1005, FIG. 11; Ex.1003, ¶107.



Ex.1005, FIGS. 10-11.

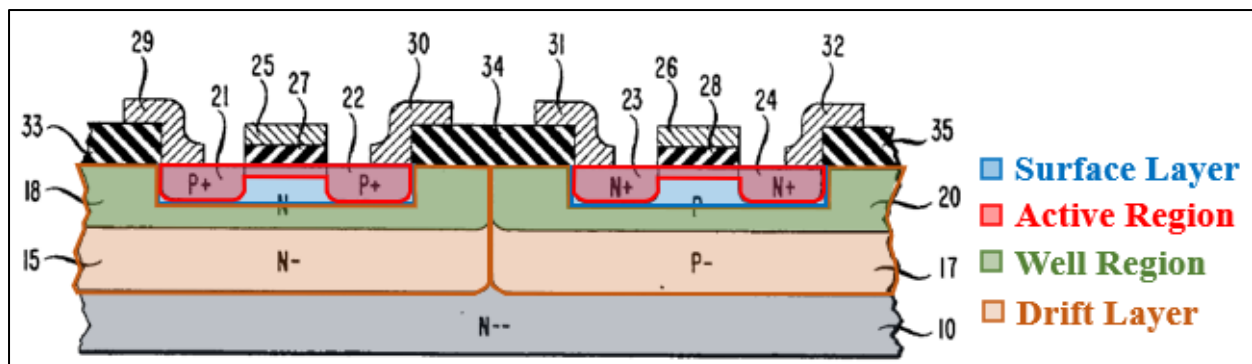
For the same reasons, Payne satisfies Petitioner’s construction that the first static unidirectional electric drift field must be “unidirectional *over* the drift layer,” and also satisfies Petitioner’s alternative proposed construction of the sub-phrase “to aid the movement of minority carriers” from said surface layer to said substrate to

mean “to sweep the minority carriers from said surface layer to said substrate.” *Id.*, Ex.1033; Ex.1040, 289-290; Ex.1003, ¶108.

- g. **Element [7.6]: “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”**

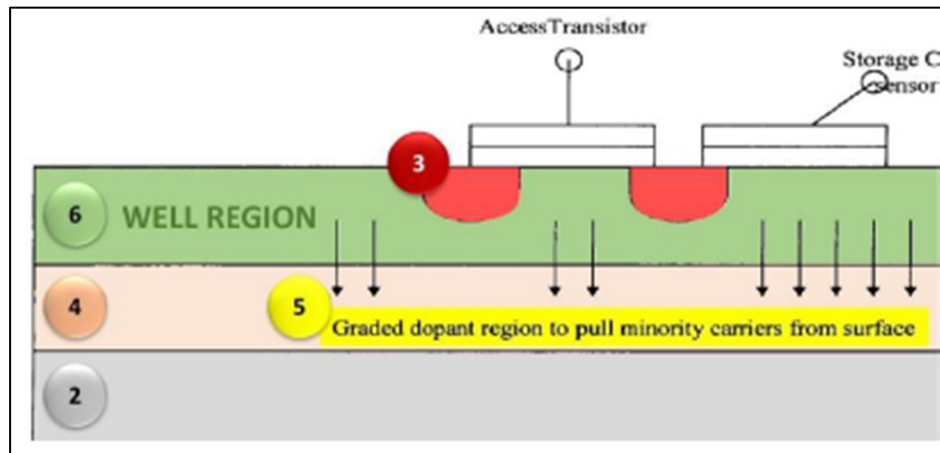
Payne discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶109-121.

**Well region disposed in said single drift layer...having a graded concentration of dopants** – As detailed above in §§X.A.1.e-f regarding elements [7.4] and [7.5], Payne’s “tub region” 15 is an example of the claimed single drift layer (SDL). As shown below, Payne’s “**surface region**” 18 (green) disposed in tub region 15 (tan) is an example of a well region (a shallow well) disposed in Payne’s SDL (tub). Ex.1005, 1:65-68, 4:31-39, 5:7-14, 5:44-55; Ex.1003, ¶¶110-113. Payne’s **surface region 20 (green)** is another well region disposed in an SDL (tub 17). *Id.*, 1:65-68, 4:63-5:14, 5:44-55; Ex.1003, ¶110; §X.B.1.e.



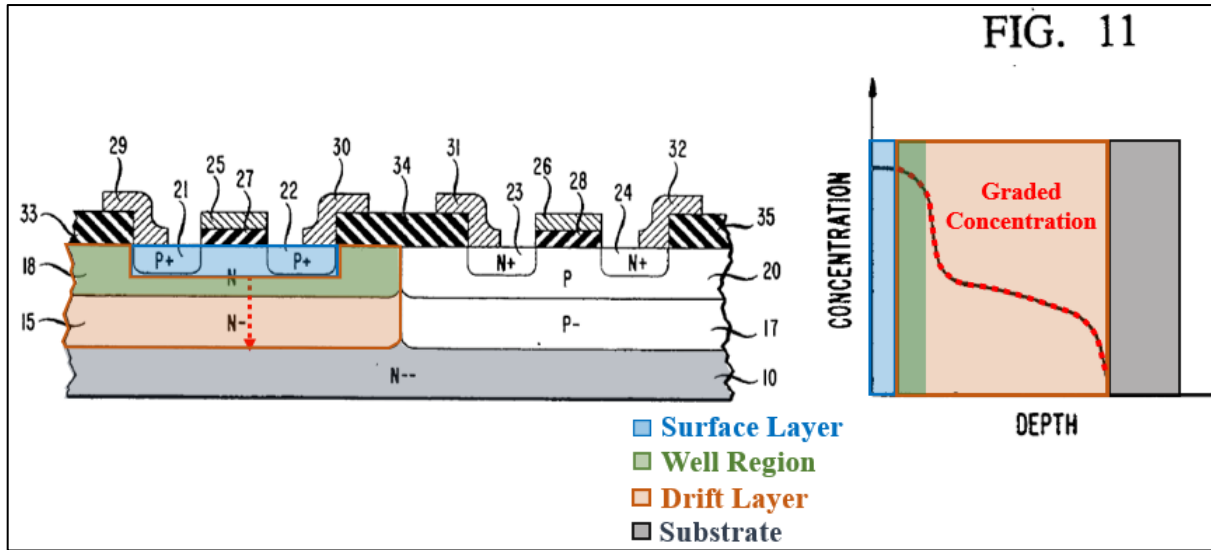
Ex.1005, FIG. 10.

Notably, Payne satisfies element [7.6] to the same extent that Figure 5(b) of the '502 Patent, annotated by PO (as shown below), meets it:

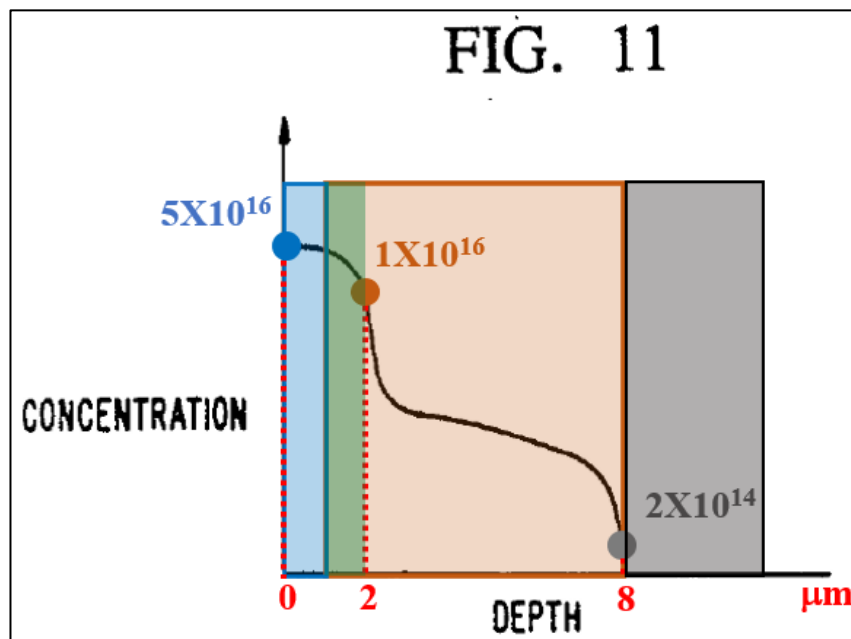


Ex.1001, FIG. 5(b); Ex.1030, 7.

As detailed above with respect to element [7.5], Payne's Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left). As shown, Payne's well region ("surface region 18") (green)—disposed in the SDL (tub 15) (tan border)—has a graded-dopant concentration that is downward-sloping with increasing depth. Ex.1003, ¶112; §X.A.1.f.

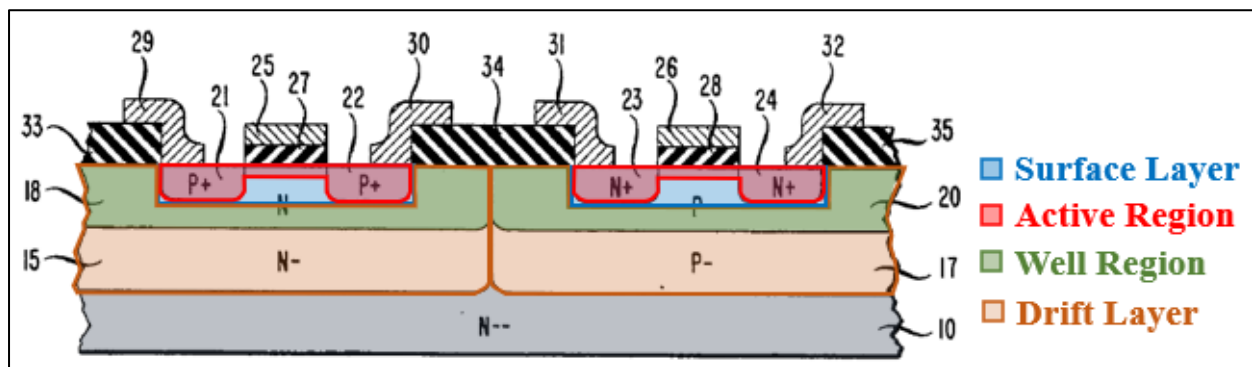


Ex.1005, FIGS. 10-11. As discussed in §X.A.1.f, Payne discloses that Figure 11 illustrates a “*high-low implant profile*” that is downward-sloping with depth, such as from  $5 \times 10^{16}$  ions/cm<sup>3</sup> (near the top surface of the silicon/surface layer (blue)) to  $1 \times 10^{16}$  ions/cm<sup>3</sup> near the bottom of well 18 (green), to  $2 \times 10^{14}$  ions/cm<sup>3</sup> near the bottom of the SDL (tub 15) (tan). *Id.*, 2:56-59, 5:48-57; Ex.1003, ¶113.



Ex.1005, FIG. 11.

In light of the above, Payne satisfies element [7.6] under PO's construction that the term "well region" should be accorded plain meaning and is "a doped region that surrounds the active region of a semiconductor device." Ex.1033. As shown in Figure 10 below, the well region (green) is a doped region that surrounds the surface layer (blue) and the active region (red) therein. Ex.1003, ¶¶110-114.

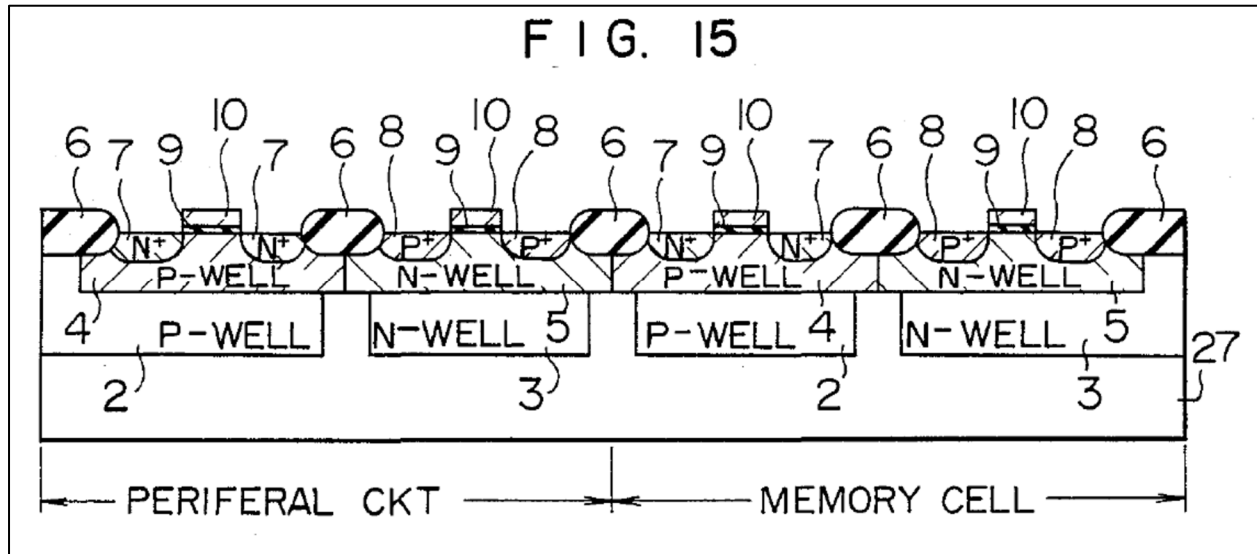


Ex.1005, FIG. 10.

Payne also satisfies Petitioner's proposed construction of "well region" to mean "a well, whether formed by single or multiple implants. Portions of a well are not well regions." Ex.1033. Each surface region 18/20 is a well (and not a portion of a well) formed with an ion implant of phosphorous or boron. Ex.1003 ¶115; Ex.1005, 4:31-39, 4:63-5:5, FIGS. 7, 9.

In addition, as discussed in §X.B, Sakai teaches a nested structure similar to Payne, which Sakai refers to as "twin double well." See, e.g., Ex.1006, 7:19-37 ("The memory of FIG. 15 has a *twin double well* structure ... made up of the *deep* P-well

region 2, the *deep* N-well region 3, the *shallow* P-well region 4 and the *shallow* N-well region 5”).



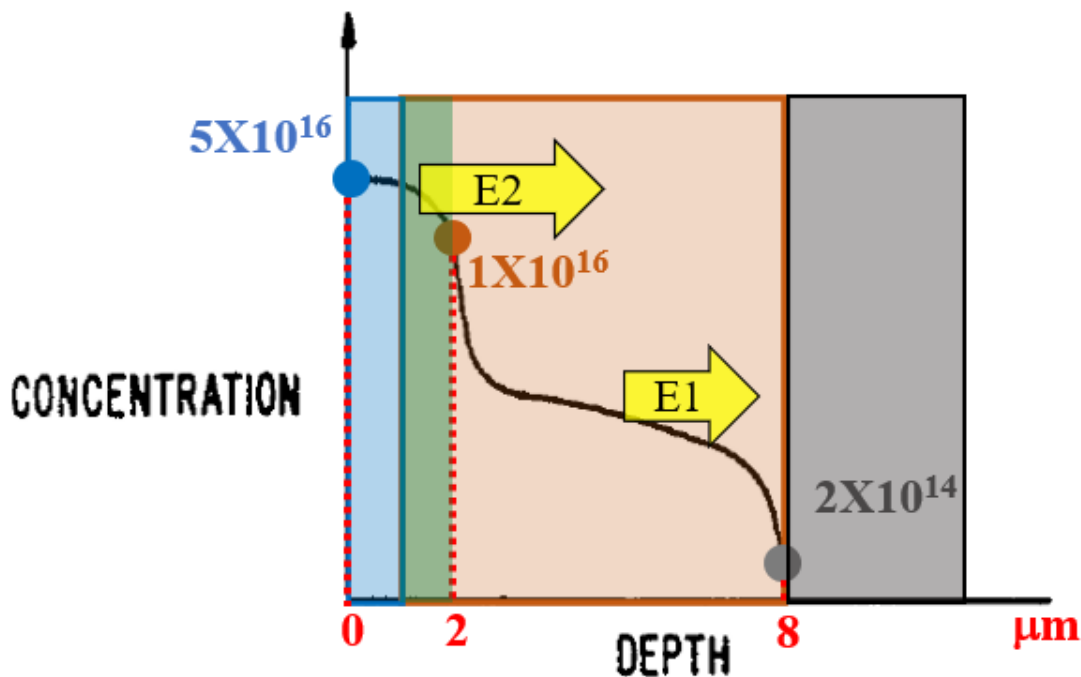
Ex.1006, FIG. 15; 1:57-67, 5:56-6:4, FIG. 10B, FIGS. 3, 8-9, 11E. Sakai confirms that Payne’s “surface region” is a shallow well region. Ex.1003, ¶116.

**Second static unidirectional electric drift field to aid the movement of minority carriers** – According to §X.A.1.f—including Applicant’s repeated representations during prosecution of the parent ’195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO’s statements in its claim construction brief—the downward-sloping graded-dopant concentration in the well region generates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. §X.A.1.f; Ex.1003, ¶117. Further, Payne’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not

change, making the profile (and any resulting electric field) static, as described in §X.A.1.f.

Payne’s Figure 11 is further annotated below to show the exemplary first static unidirectional electric drift field (“E1”) present in a deep portion of the SDL (discussed in §X.A.1.f), and a different, exemplary second static unidirectional electric drift field (“E2”) present in the well region disposed in the SDL. Ex.1003, ¶118; *see also* fn.6.

FIG. 11



Ex.1005, FIG. 11. Moreover, E1 and E2 are illustrated as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the graded-dopant profile. Ex.1003, ¶119; Ex.1022, [0071] (“the vertical  $\epsilon$ -field is established

by the rate of change in the graded dopant concentration, i.e., the greater the rate of change ... the greater the intensity of the  $\epsilon$ -field.”).

In light of the above, Payne satisfies element [7.6] under PO’s plain-meaning construction of “to aid the movement of minority carriers”. Ex.1033; Ex.1003, ¶¶118-120. Payne’s Figure 11 shows that the dopant concentration is downward-sloping with increasing depth over the entire well region, and thus, according to PO (and also in light of Applicant’s representations to the Patent Office, discussed in §X.A.1.f), generates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate. Ex.1030, 2, 29; Ex.1003 ¶¶118-120. For the same reasons, Payne also satisfies this claim element under Petitioner’s construction that the second static unidirectional electric drift field must be “unidirectional over the well region,” and also satisfies Petitioner’s alternative proposed construction that “to aid the movement of minority carriers” means “to sweep the minority carriers from said surface layer to said substrate.” Ex.1033; §X.A.1.f; Ex.1040, 289-290; Ex.1003, ¶¶118-121.

## **B. Ground II**

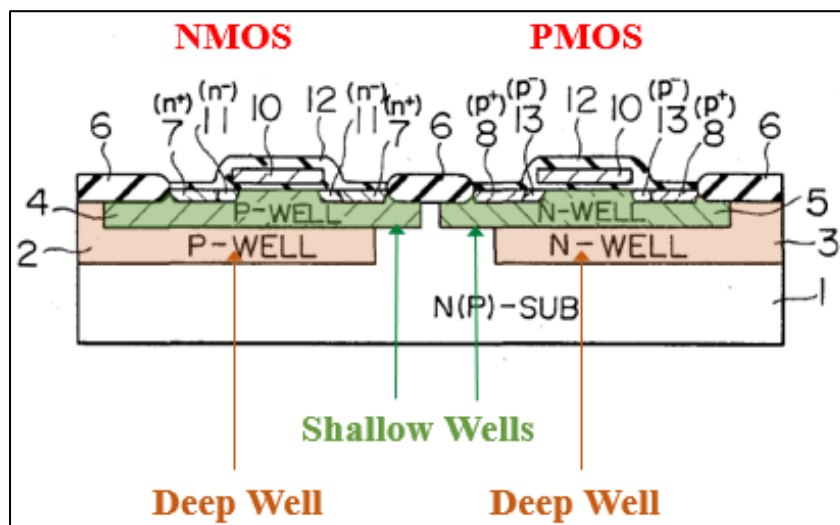
Sakai in combination with Kawagoe (hereinafter, “Sakai-Kawagoe”) renders claims 7-11 obvious. Ex.1003, ¶¶122-187.

### **1. Independent Claim 7**

#### **a. Preamble: “A semiconductor device comprising:”**

Sakai is directed to CMOS semiconductor devices. Ex.1003, ¶¶123-126;

Ex.1006, Title, 1:6-13 (“The present invention relates to a complementary semiconductor device (hereinafter referred to as ‘CMOS’)”), 1:55-2:5 (“It is an object of the present invention to provide a CMOS”). A CMOS device has “N-channel MOS [(NMOS)] transistor[s]” and “P-channel MOS [(PMOS)] transistors.” *Id.*, 4:15-29; Ex.1008A, 807-09. “[T]win-well” CMOS technology is a conventional structure that uses separate, side-by-side wells for the p- and n-type transistors, and is the technology focus of both Sakai and Kawagoe. Ex.1008B, 387-88; Ex.1006, 1:6-13, 7:19-23; Ex.1007, 14:46-55, 15:26-40, FIGS. 16, 21-24, 26-28. Sakai teaches a “twin *double* well” structure, whereby shallow wells (p-well 4 and n-well 5) (green) are formed in the wells (p-well 2 and n-well 3) (tan) of a conventional twin-well CMOS semiconductor device, as shown in Figure 10D below. Ex.1006, 1:55-2:5, 5:53-6:4, 7:19-23, 7:32-37, 8:6-8; *compare* Ex.1006, FIG. 1 *with* FIGS. 2A, 3.

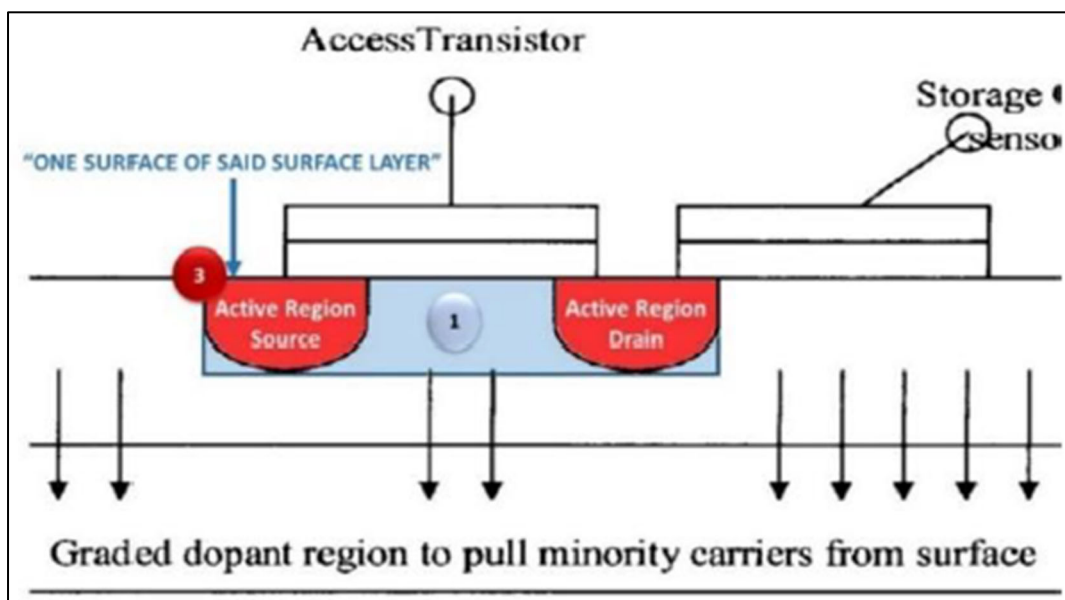


Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 10A-10E, 11A-11E, 15-17, 3:18-43.

While this Ground relies primarily on Sakai's Embodiment V (FIGS. 10A-E and accompanying discussion), which itself is based on Embodiment I (FIGS. 2A-B) (Ex.1006, 5:53-55), Sakai discloses similar “twin double well” structures in the other embodiments and those embodiments are applicable for the same reasons as explained throughout this Ground. *Id.*, FIGS. 3, 8-9, 11A-11E, 15-17 (and accompanying discussion).

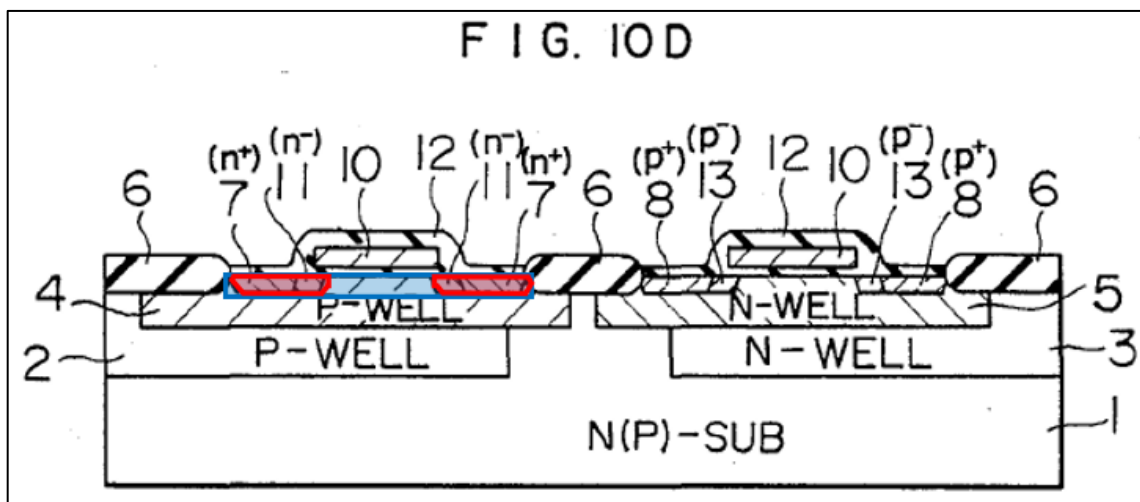
**b. Element [7.1]: “a surface layer;”**

Sakai discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶127-129. According to PO, a “surface layer” is “a layer at the surface of the silicon” (also phrased as “a layer at the surface of the semiconductor device”)—which PO annotated in blue in Figure 5(b) below—“where the active region [(red)] is located.” Ex.1030, 6, 9, 12, 13; Ex.1033; §X.A.1.b.

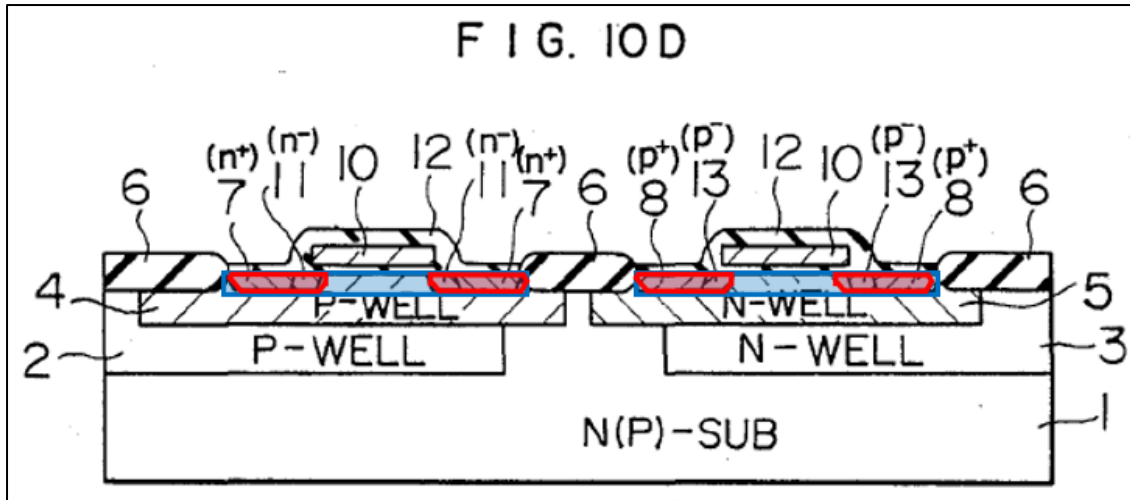


Ex.1001, FIG. 5(b); Ex.1030, 7, 12.

Sakai satisfies element [7.1] to the same extent that Figure 5(b) meets it. Ex.1003, ¶128. Sakai's Figure 10D discloses a surface layer (blue) that matches the surface layer PO identified in Figure 5(b). Sakai's surface layer is at the surface of Sakai's silicon substrate 1, and the source and drain regions ("highly-doped N-diffusion layer 7") [(red)] of Sakai's N-channel MOS transistor (left) are located in it. Ex.1006, 1:28-30, 1:68-2:5, 4:25-29, 5:53-55, 5:59, 6:16-17; *id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:54-55.



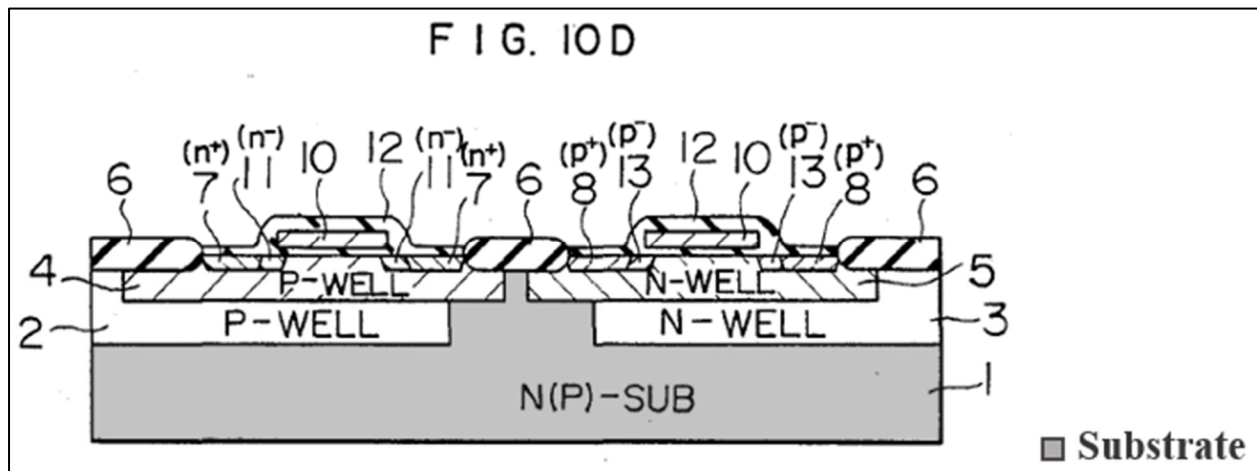
Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai likewise discloses a surface layer containing the "highly-doped P-diffusion layer 8," which serves as the source and drain regions in the "P-channel MOS transistor" (below right). *Id.*, 1:68-2:5, 4:25-29, 5:53-55, 6:16-17; *id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:54-55.



Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

**c. Element [7.2]: “a substrate;”**

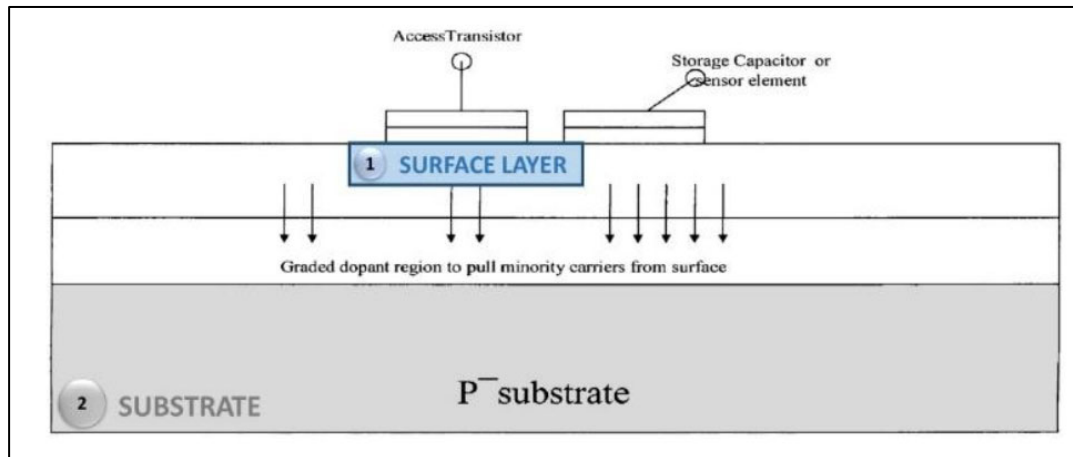
Sakai discloses “a silicon substrate 1 [(grey below)] made of N-silicon or P-silicon.” Ex.1003, ¶¶130-132; Ex.1006, 4:13-14, 5:59; *id.*, 1:61, 6:26-27.



Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

Sakai satisfies element [7.2] under PO’s proposed construction of “[p]lain and ordinary meaning, where the plain and ordinary meaning is ‘an underlying layer.’” Ex.1033. Sakai’s substrate also matches PO’s identification of substrate (grey) in

Figure 5(b) of the '502 Patent.

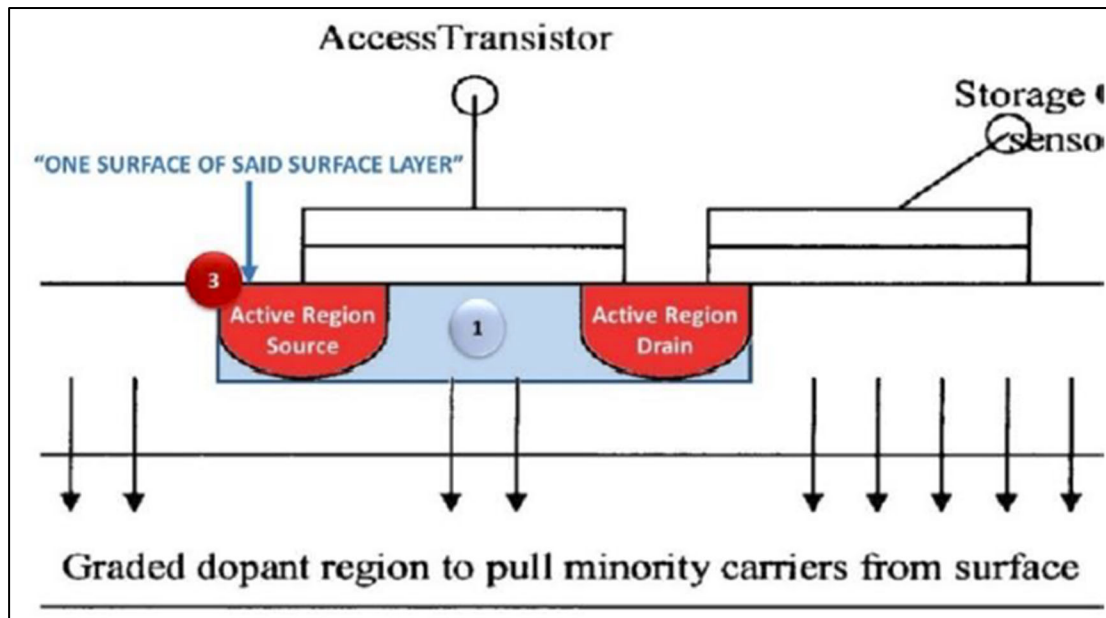


Ex.1030, 6-7, 16-17 (well region and drift layer can be part of substrate); Ex.1001, FIG. 5(b).

Sakai also satisfies this element under Petitioner's proposed construction of "substrate" because Sakai's substrate is the initial material within which or on which Sakai's semiconductor device is fabricated. Ex. 1033; Ex. 1003 ¶¶131-132; Ex.1006, 1:6-8, 5:53-61; *id.*, 1:57-2:5, 3:18-43, FIGS. 2A, 3, 8-9, 10A-10E, 11A-11E, 15-17.

**d. Element [7.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"**

Sakai discloses or, at a minimum, renders obvious this element. Ex.1003, ¶¶133-138. As described in §X.A.1.d, according to PO, Figure 5(b) of the '502 Patent depicts an active region (red) "disposed on one surface [(top surface)] of said surface layer."

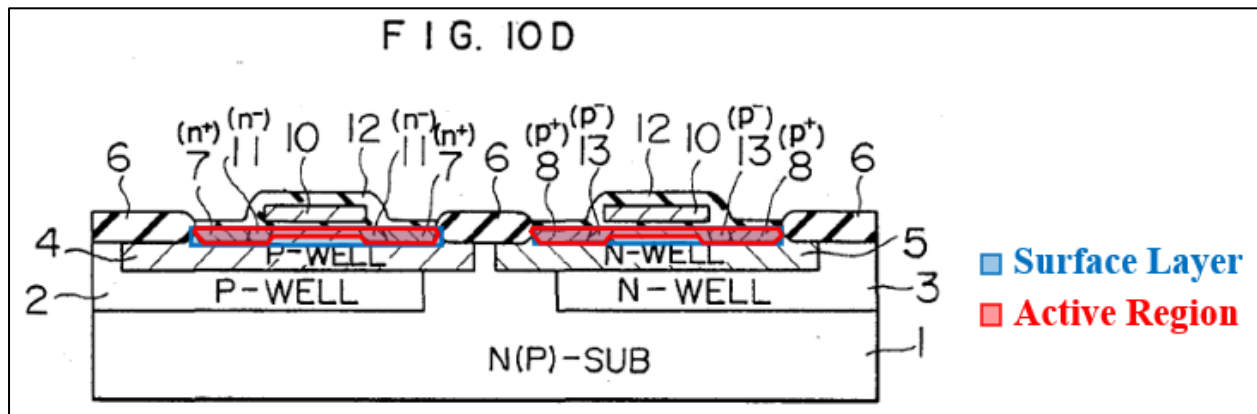


Ex.1001, FIG. 5(b); Ex.1030, 6-7, 10-12; §X.A.1.d.

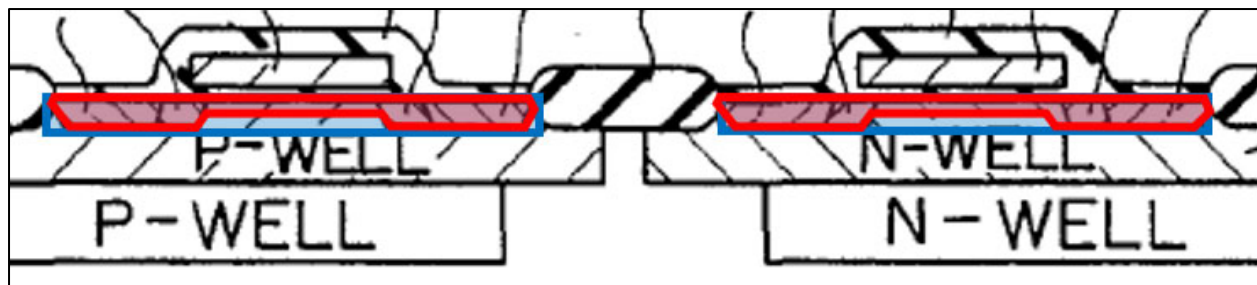
Sakai satisfies element [7.3] under PO's interpretation. Ex.1003, ¶¶134-135. Sakai Figure 10D below illustrates an "N-channel" MOS transistor with source/drain regions ("highly-doped N...diffusion layers" 7) (left) in a doped shallow P-well 4, and a "P-channel" MOS transistor with source/drain regions ("highly-doped ... P-diffusion layers" 8) (right) in a doped shallow N-well 5. Ex.1006, 1:28-30, 1:57-2:5, 4:25-29, 5:53-55, 5:64-6:4, 6:16-17; *id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:52-58; §X.B.1.b. The source/drain regions of a p-channel or n-channel transistor, together with the channel region between them, form an active region. Ex.1003 ¶135; Ex.1008B, 299 ("The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The *active regions* are those in which transistor action occurs; i.e., the *channel* and the heavily doped *source* and

*drain* regions.”), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex.1008C, 525, FIG. 8-1(e).

The active region (red) of each of Sakai’s transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in PO’s annotated Figure 5(b) above. Ex.1003, ¶136; §X.B.1.b.



Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. For clarity, an enlarged version of Sakai’s active regions and surface layers is below.

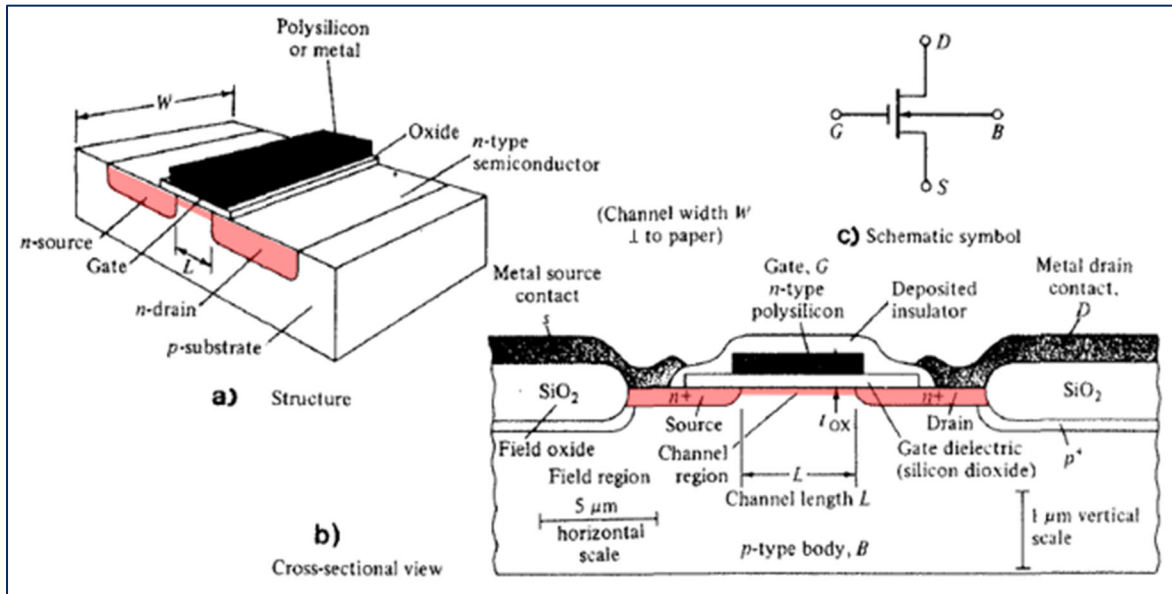


Ex.1006, FIG. 10D (excerpted).

Sakai satisfies element [7.3] under PO’s position that the term “active region” means “a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed”

(Ex.1033) because the active region of a MOS transistor is “[its] channel and [its] heavily doped source and drain regions,” highlighted in red in the figure below.

Ex.1008B, 299; Ex.1003, ¶137.

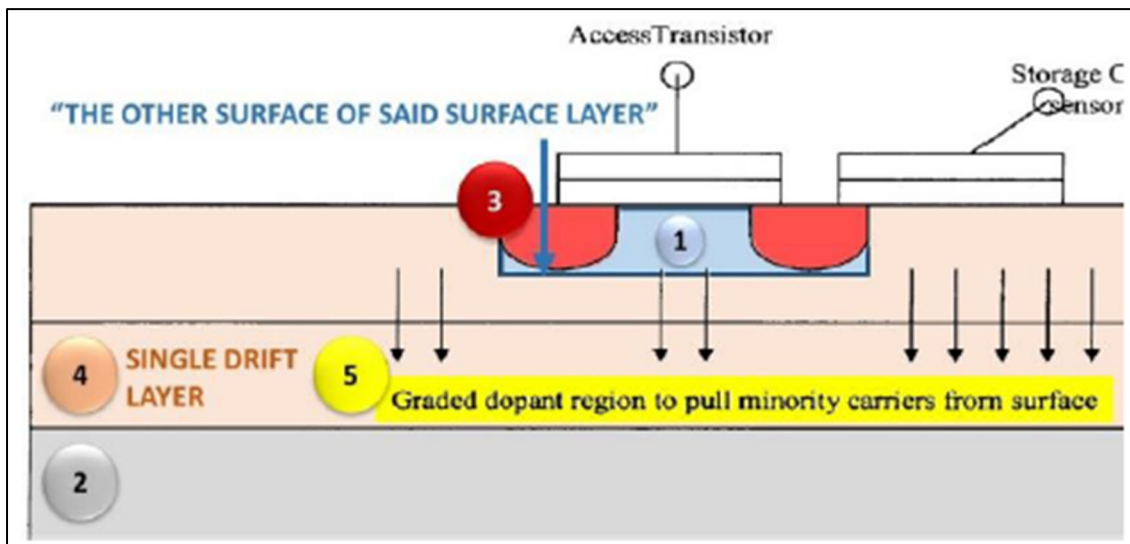


Ex.1008B, FIG. 5-1; *id.*, 298-301, 374, FIGS. 5-2, 6-4. Sakai also satisfies this element under Petitioner’s proposed construction that an active region is the “region that forms the current path of a device” or “the source, drain and channel region of a device” because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Ex.1033; Ex.1008B, 299-301, FIGS. 5-1, 5-2; Ex.1008D, 197, FIG. 5-13; Ex.1003 ¶138. PO does not dispute this. Ex.1030, 3-4 (“[w]hen a positive voltage is applied to the gate ... a conductive channel [is formed] between the source and the drain, and current can begin to flow through the transistor”).

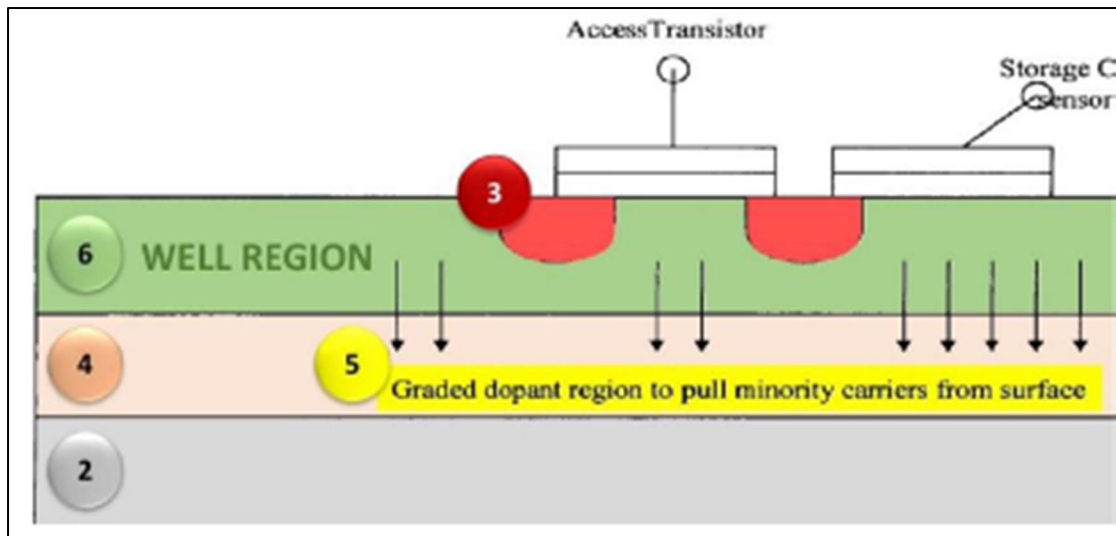
- e. **Element [7.4]: “a single drift layer disposed between the other surface of said surface layer and said substrate,”**

Sakai-Kawagoe renders obvious this element. Ex.1003, ¶¶139-143.

**Single drift layer (“SDL”)** – As described in §X.A.1.e, according to PO, Figure 5(b) of the ’502 Patent depicts a single drift layer (tan) “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and [said] substrate [(grey)]”:

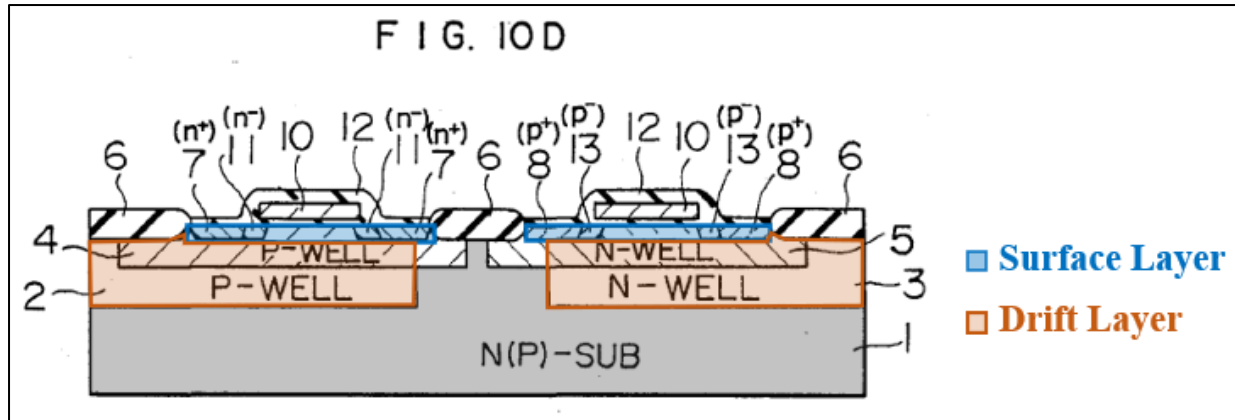


Ex.1001, FIG. 5(b); Ex.1030 at 7. The SDL in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [7.6]):



Ex.1001, FIG. 5(b); Ex.1030, 7; *id.*, 11 (“the ‘well region’ is part of the ‘single drift layer.’”).

Sakai-Kawagoe meets a single drift layer to the same extent Figure 5(b) of the ’502 Patent does. Ex.1003, ¶¶140-142. In Sakai’s Figure 10D, the “deep P-well region 2” (left) of Sakai’s nested well structure—with shallow P-well region 4 disposed in it—is an example of the claimed drift layer. *Id.*; Ex.1006, 5:56-6:4, 1:57-67, 7:32-37; *id.*, 6:24-28, 6:52-58. This SDL (tan) is “disposed between ‘the other surface [(bottom surface)] of said surface layer [(blue)]’ and said substrate [(grey)]” under PO’s interpretation, and in exactly the same way as depicted in PO’s annotated Figure 5(b) above.



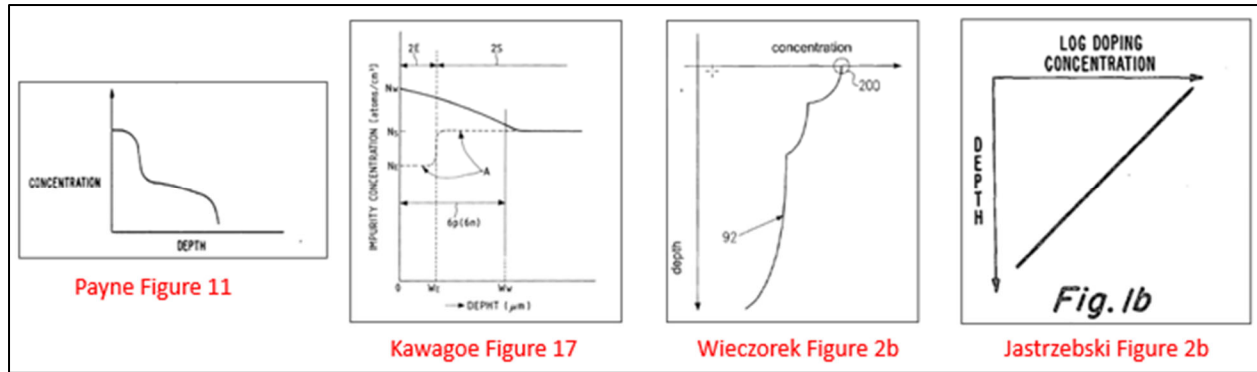
Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai’s “deep N-well region 3” (right), in which “shallow N-well region 5” is disposed, is likewise an SDL (tan) disposed between a surface layer (blue) and the substrate (grey). *Id.*, 5:56-6:4, 1:57-67, 7:32-37; *id.*, 6:24-28, 6:52-58; Ex.1003, ¶142; §X.B.1.b.

Sakai-Kawagoe meets all other claim requirements associated with the SDL to the same extent Figure 5(b) meets them, as explained below. *See* elements [7.5]-[7.6]; Ex.1003, ¶143. Notably, as detailed in element [7.5], each of the deep wells 2/3 in Sakai-Kawagoe is a *single* drift layer because it has a graded-dopant concentration that, according to PO, generates a unidirectional electric drift field that aids the movement of minority carriers in a *single* direction—from the surface layer to the substrate. Ex.1030, 7: Ex.1040, 253-54, 289-290; §X.B.1.f.

- f. **Element [7.5]: “said drift layer having a graded concentration of dopants generating a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and”**

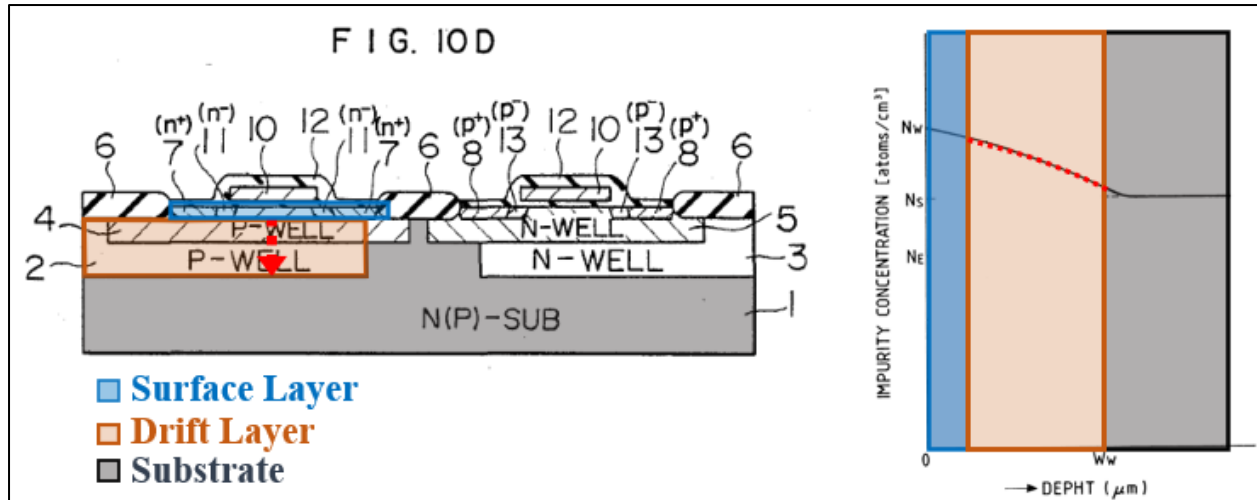
Sakai-Kawagoe renders obvious this element. Ex.1003, ¶¶144-165.

**Graded concentration of dopants**— Sakai-Kawagoe renders obvious a single drift layer having a graded concentration of dopants extending between the surface layer and the substrate. Ex.1003, ¶¶145-152. For example, the SDL (*e.g.*, deep P-well 2 (above left) with shallow P-well 4 disposed in it) has a ***high-to-low*** dopant concentration, whereby the “shallow P-well region 4” has “an impurity concentration of  $5 \times 10^{16}$  to  $10^{18}$  atoms per  $\text{cm}^3$ ,” which is up to ***two orders of magnitude higher*** than the dopant concentration in the deep “P-well region 2,” which is in the range of “ $10^{15}$  to  $10^{16}$  atoms per  $\text{cm}^3$ .” Ex.1006, 5:56-6:4. The same applies to the SDL formed by deep N-well 3 (above right) with shallow N-well 5 disposed in it. *Id.* A POSITA would have understood that Sakai’s ***high-to-low*** concentration is ***gradually decreasing*** across Sakai’s SDL because it is formed “through ion implantation techniques and thermal diffusion techniques.” Ex.1006, 5:56-6:4, 6:24-28, 6:52-58, 8:35-38; Ex.1003, ¶¶145-146. Indeed, a downward-sloping graded-dopant concentration formed through ion implantation and thermal diffusion was well-known in the art. And such profile was disclosed in many prior art references, such as Payne, Kawagoe, Wiczorek and Jastrzebski, as shown below.



Ex.1005, FIG. 11, 3:28-42, 4:19-39, 5:7-17; Ex.1007, FIG. 17, 15:62-16:2, 17:31-61; Ex.1038, FIG. 2b, [0008], [0010]-[0011]; Ex.1010, FIG. 1b, 5:5-27; 9:2-8. Significantly, Payne’s Figure 11 illustrates a graded-dopant profile that is downward-sloping over a *nested well structure* similar to Sakai’s “*twin double well*” structure, as detailed under X.A.1.e-f. Ex.1003, ¶147. Additionally, the ’502 Patent mentions dopant gradients (“linear, quasi linear, exponential or complimentary error function”) only once and does not describe how to make them, confirming implementing them in CMOS devices was well-known. Ex.1001, 2:44-46. *Ex Parte Nico Hawley-Weld, Dan Volpe, & Ben Silverman*, No. APPEAL 2023-000345, 2022 WL 17495059, at \*7 (P.T.A.B. Dec. 6, 2022) (“in the absence of specific description [in the specification], it is appropriate to assume that anyone desiring to perform the claimed function would know how to do so.”); *In re Epstein*, 32 F.3d 1559, 1568 (Fed. Cir. 1994). The ’502 Patent also lists linear/quasi-linear among a few gradients without giving any reason to use one over another. Ex.1001, 2:44-46. And, as further detailed below, a POSITA would have been motivated to

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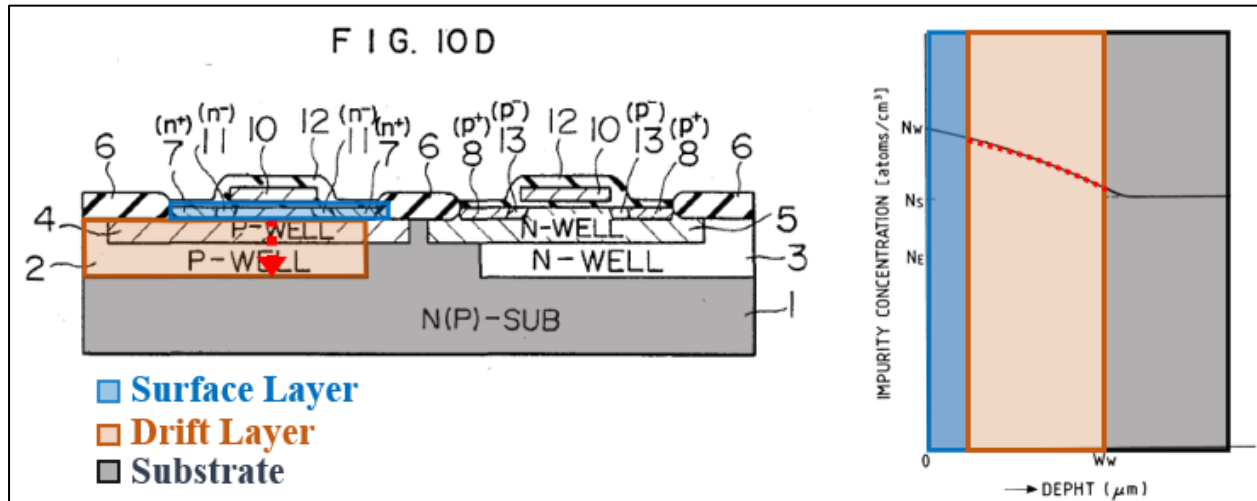
Ex.1006, FIG. 10D; Ex.1007, FIG. 17 (excerpted); Ex.1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai's high-to-low dopant concentration across deep N-well 3 (right side of Figure 10D) implemented in accordance with the same teachings of Kawagoe would similarly result in a gradual downward-sloping profile. Ex.1003, ¶¶151-152. Accordingly, Sakai-Kawagoe meets a single drift layer having a downward-sloping graded concentration of dopants extending between the surface layer and the substrate. *Id.*

**Motivation to combine Sakai and Kawagoe** - A POSITA would have been motivated to combine Sakai and Kawagoe for numerous reasons. Ex.1003, ¶¶153-160. Both are Hitachi patents. Ex.1006, cover; Ex.1007, cover. Both are directed to CMOS devices that were (and still are) "widely used" to form memories and microcomputers because of their "low [] power dissipation" and because CMOS devices "can operate at high speed." Ex.1006, 1:7-17, Ex.1007, 3:32-38, 19:15-16, 20:1-8, 21:5-12, 22:14-21, 24:28-31.

Sakai teaches improving the circuit density (packing density) of CMOS chips by disposing shallow wells into deep wells of a “twin-well” CMOS device to form a “twin double well” structure (nested well structure). Ex.1006, 1:55-2:5, 7:19-37, 8:9-24, FIGS. 2A, 10D, 15. Sakai’s “twin double well” structure is used to form high-packing-density memory devices, including SRAM memory devices illustrated in Figure 15 and discussed in Kawagoe. *Id.*, 7:24-37 (“[CMOS] static memory of...6 MOS transistors”); Ex.1008B, 572-573 (“SRAMS... are... static memories), FIG. 8-2 (CMOS SRAM cell); Ex.1007, 21:5-12, FIG. 27(B). High-packing-density SRAMs are susceptible to soft errors. Ex.1008B, 583 (“SRAMs offer better resistance than DRAMs to [soft-errors] ... However, as geometries have been scaled down to produce circuits of greater density, alpha-particle-induced soft-error rates have also become a concern in SRAMs.”).

A POSITA would thus have been motivated to apply Kawagoe’s teachings directed to protecting memories against alpha-particle-induced soft errors to Sakai’s twin double well structure (including for SRAM memory). Ex.1003, ¶¶154-156. A POSITA would have engineered the dopant profile across each of Sakai’s single drift layers (tan) so that it is downward-sloping from the top surface of the silicon substrate to the bottom of the deep well—as illustrated in the dopant profile at right—because Kawagoe teaches that such a profile causes alpha-particle-generated minority carriers to move to the substrate. Ex.1007, 16:2-11 (the “gradient [in the p-

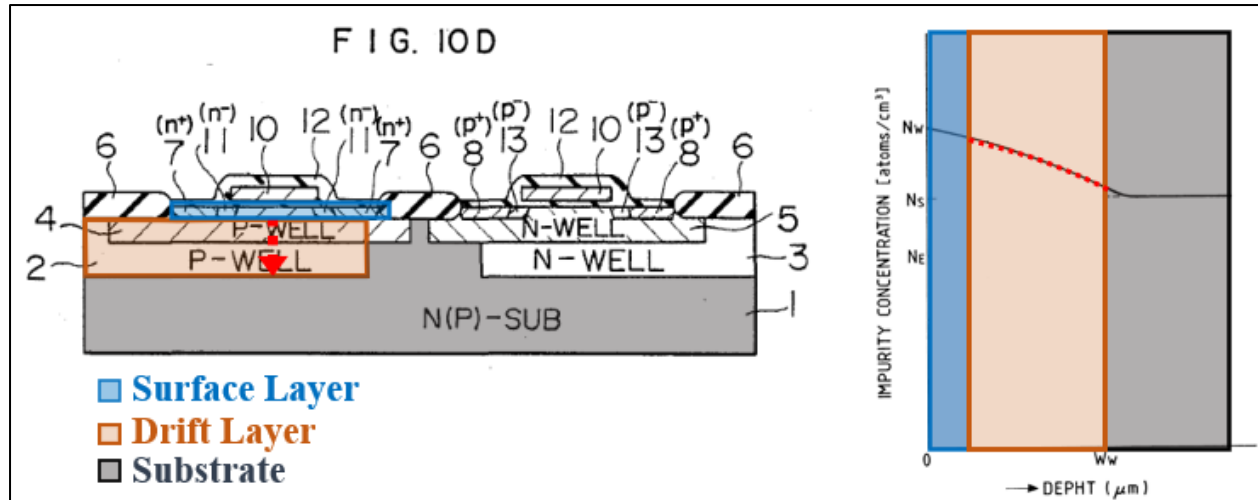
well] is ***gradually lowered*** in the depthwise direction” and, as a result, “electrons produced by the  $\alpha$ -ray are attracted to the substrate body 2S by that concentration gradient ... so that the soft errors can be reduced....”), 21:20-23; Ex.1003, ¶156.



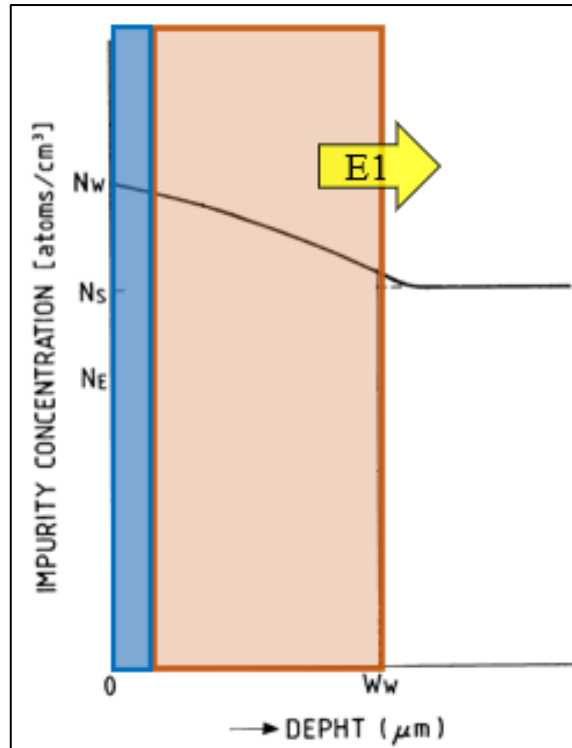
Ex.1006, FIG. 10D; Ex.1007, FIG. 17 (excerpted); Ex.1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Such a downward-sloping dopant profile is consistent with Sakai’s teachings of (1) higher dopant concentration in the shallow wells compared to the deep wells, and (2) the use of ion implantation followed by thermal drive-in, which naturally results in a non-uniform, graded-dopant concentration, discussed above. Ex.1006, 5:56-6:4; Ex.1003, ¶¶156-157. There is a reasonable expectation of success because it was well-known that various ion-implantation and thermal drive-in processes enable different dopant profiles to be readily engineered and fabricated as needed, Ex.1008A, 371, 373 (“Complex-doping profiles can be produced” using ion implantation), and because the prior art is replete with teachings on how to form downward-sloping dopant concentrations, as in Kawagoe, Payne, Jastrzebski and

Wieczorek. Ex.1003, ¶158. Further, the '502 Patent specification mentions various dopant gradients (including ones with a one-way slope, *e.g.*, quasi-linear) and does not illustrate or otherwise describe how to make them, confirming that such gradients were well-known and a POSITA would have known how to manufacture a CMOS device having them. Ex.1001, 2:44-46; *Ex Parte Hawley-Weld* at \*7; *In re Epstein*, 32 F.3d 1568. Accordingly, a POSITA would have equally known how to implement an SDL in Sakai to result in a known downward-sloping graded-dopant concentration profile. This combination also merely amounts to (1) combining prior art elements (Sakai's CMOS device and Kawagoe's dopant profile) according to known methods (well-known ion implantation and thermal drive in techniques) to yield predictable results and (2) use of a known technique (creating Kawagoe's profile) to improve similar devices (Sakai's CMOS devices) in the same way (to reduce soft errors).

**First static unidirectional electric drift field to aid the movement of minority carriers** - As discussed above, Sakai-Kawagoe renders obvious a single drift layer (tan) having a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (grey), similar to Kawagoe Figure 17 below.



Ex.1006, FIG. 10D; Ex.1007, FIG. 17 (excerpted); Ex.1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Thus, according to §X.A.1.f, including Applicant’s repeated representations to the Patent Office and the Jastrzebski and Kamins cited art relied on by Applicant, such a downward-sloping graded-dopant concentration generates a “built-in” unidirectional electric drift field (illustrated “E1” below) to aid the movement of minority carriers from the surface layer to the substrate. Ex.1003, ¶¶161-162; §X.A.1.f; *see also* fn.6.



Ex.1007, FIG. 17 (excerpted). Such a profile is created “through ion implantation techniques and thermal diffusion techniques” and thus the profile (and any resulting electric drift field) is static—it is set once the CMOS device has been fabricated and does not change afterwards. Ex.1003, ¶¶162-163; Ex.1006, 5:56-6:4, 6:24-28, 6:52-58, 8:35-38; §X.A.1.f. As discussed in §X.A.1.f, Applicant described “static” similarly during prosecution of the parent ’195 Patent. Ex.1040, 318 (citing Ex.1009), 333 (same).

In light of the above, Sakai-Kawagoe satisfies element [7.5] under PO’s plain-meaning constructions. Ex.1033; Ex.1030, 2, 29; Ex.1003, ¶¶161-164. Sakai-Kawagoe’s graded-dopant concentration is downward-sloping over the entire SDL (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the

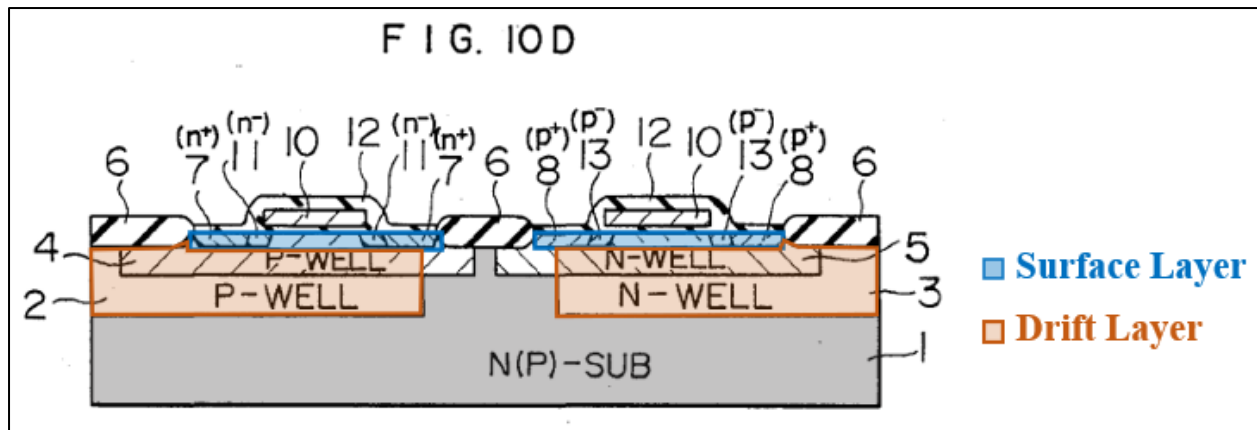
SDL—and thus, according to PO (and also in light of Applicant’s representations to the Patent Office discussed above), generates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex.1007, FIG. 17; Ex.1003, ¶164.

For the same reasons, Sakai-Kawagoe satisfies Petitioner’s construction that the first static unidirectional electric drift field must be “unidirectional *over* the drift layer,” and also satisfies Petitioner’s alternative proposed construction of the subphrase “to aid the movement of minority carriers from said surface layer to said substrate” to mean “to sweep the minority carriers from said surface layer to said substrate.” *Id.*, Ex.1033; §X.A.1.f; Ex.1040, 289-290; Ex.1003, ¶165.

- g. **Element [7.6]: “at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants generating a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.”**

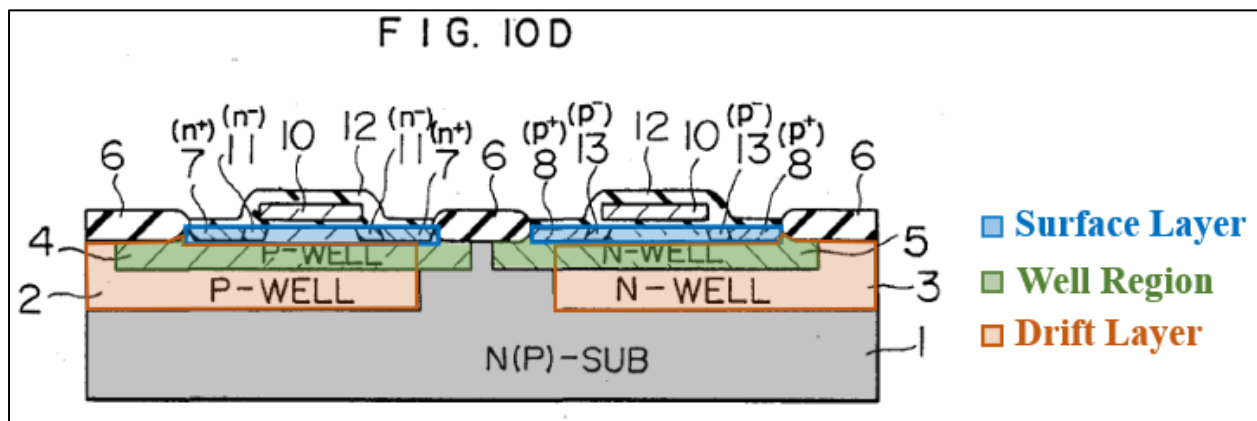
Sakai-Kawagoe renders obvious this element. Ex.1003, ¶¶166-176.

**Well region disposed in said single drift layer...having a graded concentration of dopants** – As detailed above, Sakai-Kawagoe renders obvious a single drift layer (deep P-well 2 or deep N-well 3) (tan), as shown below. Ex.1006, 5:56-6:4. §§X.B.1.e-f.



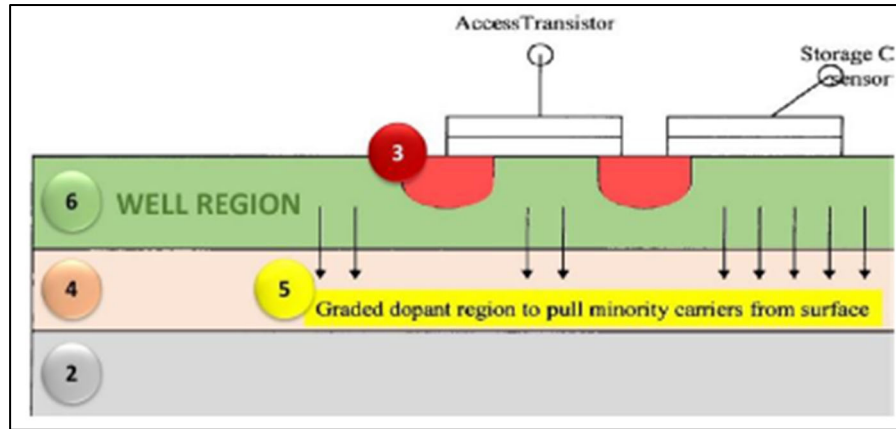
Ex.1006, FIG. 10D; *id.*, Ex.1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

Each shallow well in Sakai’s nested well structures (“twin double wells”)—*e.g.*, the “**shallow P-well region 4**” (left) or “**shallow N-well region 5**” (right)—is an example of a well region (green) disposed in an SDL (tan). Ex.1006, 1:57-67, 5:56-6:4, 7:32-37.

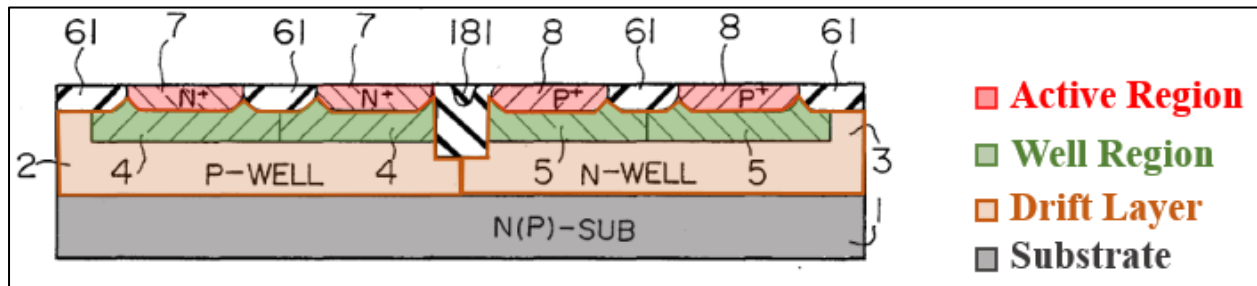


Ex.1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

Notably, Sakai-Kawagoe satisfies element [7.6] to the same extent that Figure 5(b) of the ’502 Patent, annotated by PO in its claim construction brief, meets it:

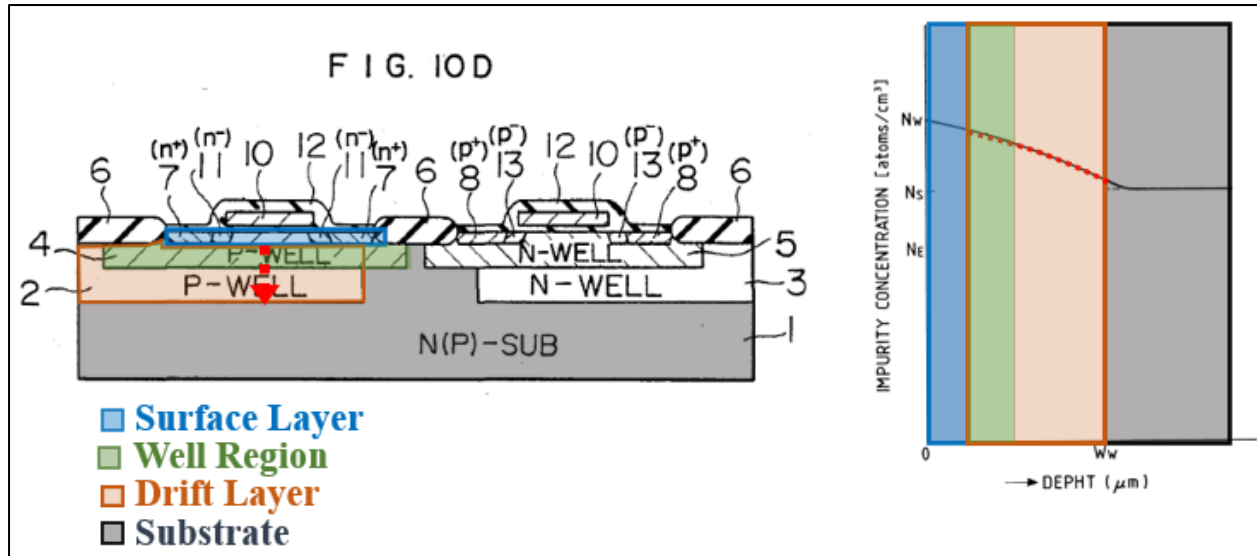


Ex.1001, FIG. 5(b); Ex.1030, 7. To the extent PO argues that the well region must be entirely contained within the SDL, Sakai discloses that too. *See, e.g.*, Ex.1006, FIGS. 11E (below), 3, 8-9, 16.



Ex.1006, FIG. 11E; *id.*, 1:29-30, 2:60-61, 6:22-31, 6:52-58.

Further, as also detailed above with respect to element [7.5], Sakai-Kawagoe's structure has a downward-sloping graded-dopant concentration extending between the surface layer and the substrate, such that each well region (e.g., shallow well 4) (green) also has such downward-sloping graded-dopant concentration. Ex.1007, 15:62-16:7 (dopant "concentrations gradually lowered in the depthwise direction from the principal surface"); Ex.1003, ¶¶166-170; §X.B.1.f.

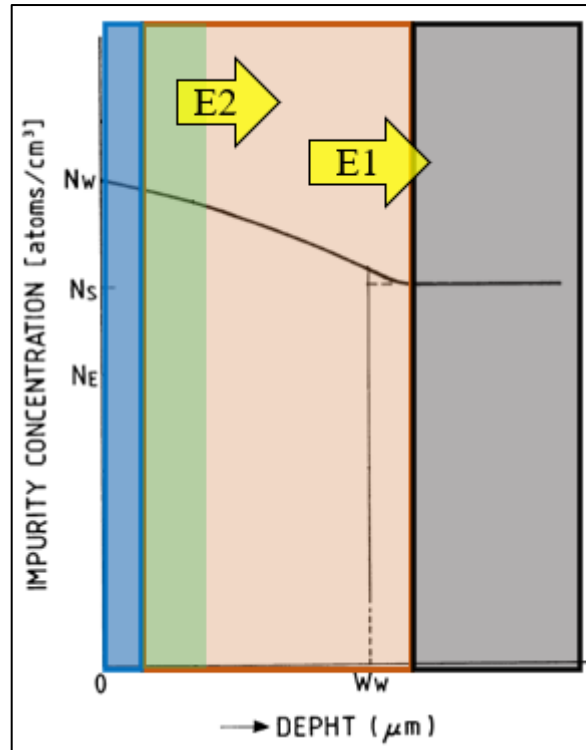


Ex.1006, FIG. 10D; Ex.1007, FIG. 17 (excerpted); Ex.1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

In light of the above, Sakai-Kawagoe satisfies element [7.6] under PO's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Ex.1033; Ex.1003, ¶¶166-172. As shown in Sakai's Figure 10D (with graded-dopant concentration shown in Kawagoe's Figure 17) above, the exemplary shallow well region (green) is a doped region that surrounds both the surface layer (blue) and the active region therein. Ex.1003, ¶¶170-172; §X.B.1.d. Sakai-Kawagoe also satisfies Petitioner's proposed construction of this term. Ex.1033; Ex.1003 ¶172. The mapping of "well region" to each shallow well 4/5 satisfies Petitioner's construction because they are formed with an ion implant of P-type or N-type impurities. Ex.1006, 5:64-6:4, 6:52-58; Ex.1033; Ex.1003 ¶172.

**Second static unidirectional electric drift field to aid the movement of minority carriers** – According to §X.A.1.f—including Applicant’s repeated representations during prosecution of the parent ’195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO’s statements in its claim construction brief—the downward-sloping graded-dopant concentration in the well region generates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. *Id.*; §X.A.1.f. Further, Sakai-Kawagoe’s graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in §X.B.1.f.

Kawagoe’s Figure 17 is further annotated below to show the exemplary first static unidirectional electric drift field (“E1”) described in §X.B.1.f, at a depth corresponding to Sakai’s deep well (tan), and an exemplary second static unidirectional electric drift field (“E2”), at a depth corresponding to Sakai’s shallow well (green) (exemplary well region disposed in the SDL). Ex.1003, ¶¶173-174; *see also* fn.6.



Ex.1007, FIG. 17 (excerpted). Moreover, E1 and E2 are illustrated as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the dopant profile. Ex.1003, ¶174; Ex.1022, [0071] (“the vertical  $\epsilon$ -field is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change ... the greater the intensity of the  $\epsilon$ -field.”).

In light of the above, Sakai-Kawagoe satisfies element [7.6] under PO’s plain-meaning construction of “to aid the movement of minority carriers.” Ex.1033; Ex.1003, ¶¶172-175. As shown in Kawagoe Figure 17 above, Sakai-Kawagoe’s graded-dopant concentration is downward-sloping over the entire well region, and thus, according to PO (and also in light of Applicant’s representations to the Patent Office, discussed in §X.A.1.f), generates a static unidirectional electric drift field

that aids the movement of minority carriers downward from the surface layer to the substrate. Ex.1003 ¶175.

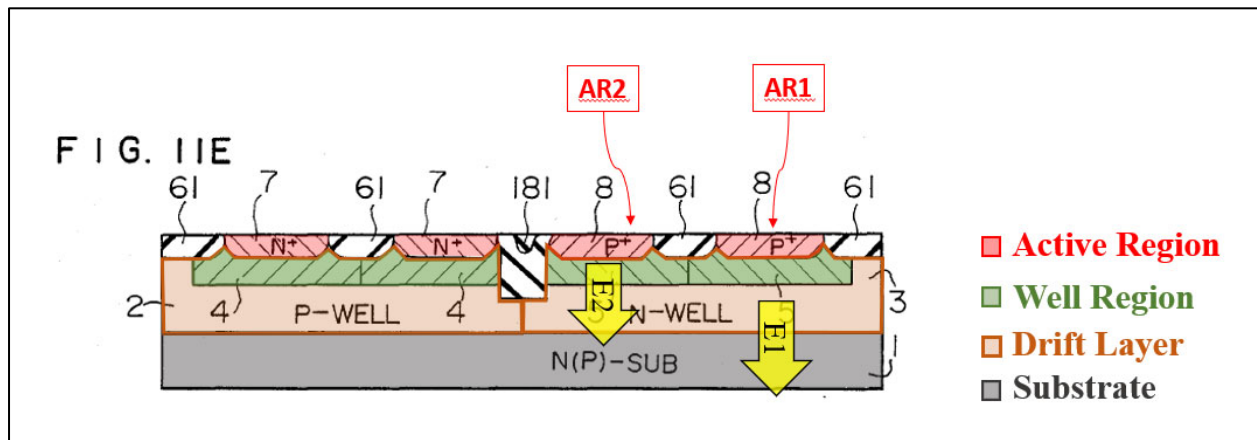
For the same reasons, Sakai-Kawagoe also satisfies this element under Petitioner’s construction that the second static unidirectional electric drift field must be “unidirectional over the well region,” and also satisfies Petitioner’s alternative proposed construction that the term “to aid the movement of minority carriers” means “to sweep the minority carriers from said surface layer to said substrate.” Ex.1033; §X.A.1.f; Ex.1040, 289-290; Ex.1003, ¶¶172-176.

**2. Dependent Claim 8: “The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions.”**

Sakai-Kawagoe renders claim 7 obvious. §X.B.1. Sakai-Kawagoe also renders obvious claim 8. Ex.1003, ¶¶177-180.

As explained in §X.B.1.a, Sakai’s Figure 11E embodiment is also applicable in meeting claim 7 (in combination with Kawagoe) and is described and cited throughout §X.B.1. As shown below and discussed in §X.B.1.f, deep N-well 3 (SDL) (tan) generates a first static unidirectional electric field E1 (yellow) that aids movements of carriers that are in, or originate from, active region AR1 (red) above it. Ex.1003, ¶¶178-180; Ex.1006, 1:68-2:5 (“highly-doped N and P-diffusion layers [(7/8)] each serving as the source and drain regions of MOS transistor are formed in the shallow P- and N-well regions”), 1:29-30, 2:20-2:27, 2:33-39, 2:51-64, 6:22-58;

§X.A.1.f; Ex.1013, 431; §§X.B.1.d-g. Likewise, as discussed in §X.B.1.g, shallow N-well 5 (well region) (green) generates a second static unidirectional electric field E2 (yellow) that aids movements of carriers that are in, or originate from, active region AR2 (red) above it. *Id.* For this mapping, the surface layer of claim 7 includes both active regions AR1 and AR2. Ex.1003, ¶¶178-179.



Ex.1006, FIG. 11E. Electric fields E1 and E2 are adapted to the grading of dopants in deep N-well 3 (SDL) (tan) and shallow N-well 5 (well region) (green), respectively, because the direction of electric fields E1 and E2 (*i.e.*, toward the surface or away from the surface) is dependent on the local slope of the graded-dopant profile according to Applicant's repeated representations during prosecution of the parent '195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO's statements in its claim construction brief as discussed in §X.A.1.f (including fn.6). Additionally, the magnitude of electric fields E1 and E2 also depends on the local grading of dopants. §X.B.1.g; Ex.1022, [0071]; Ex.1003, ¶180.

**3. Dependent Claim 9: “The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU).”**

Sakai-Kawagoe renders claim 7 obvious. §X.B.1. Sakai-Kawagoe also renders obvious claim 9. Ex.1003, ¶¶181-182. In particular, Sakai discloses use of its invention, the twin double well structure, to increase packing density in a microcomputer, which Sakai recognized as a “widely used” CMOS semiconductor device. Ex.1006, 1:6-17, 1:55-2:5, 7:21-23, 8:9-24. Kawagoe likewise teaches that its “techniques ... can ... be applied to ... a *logic circuit* such as [a] ‘*microcomputer*.’” Ex.1007, 8:46-52, 14:46-55, 15:26-40, 24:28-31. A POSITA would have understood a microcomputer to include a central processing unit (CPU). Ex.1037, 1334; Ex.1003, ¶182. In combining Kawagoe with Sakai, a POSITA would have therefore known to implement the combination of Sakai-Kawagoe in a CPU. §X.B.1.f (Motivation to Combine subsection).

**4. Dependent Claim 10: “The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device.”**

Sakai-Kawagoe renders claim 7 obvious. §X.B.1. Sakai-Kawagoe also renders obvious claim 10. Ex.1003, ¶¶183-184. Notably, Sakai discloses use of its invention, the twin double well structure, to increase packing density in “a dynamic memory using a memory cell of the stacked capacitor type,” which is a semiconductor DRAM device. Ex.1006, 1:55-2:5, 3:41-43, 7:19-23, 7:62-8:24, FIG. 17; Ex.1008B, 609-615 (stacked capacitor DRAM cells), FIGS. 8-26 to 8-29.

Kawagoe also explains that its “embodiment 4” (Figures 16-17, 20-24), relied upon for claim 7, can be advantageously used to fabricate DRAM devices (having “MOS capacitors”) with reduced soft errors, reduced defect density, and “excellent gate breakdown performance.” Ex.1007, 16:2-11 (explaining that the graded dopant concentration in p-well 6p (illustrated in Figure 17) moves “electrons produced by the  $\alpha$ -ray” to the substrate body 2S so that “soft errors can be reduced in case ... DRAM or the like is formed in the p-well 6p”), 19:15-23 (“the structure of the present embodiment 4 is applied to a 4M.DRAM”), 19:31-32, 19:43-48, 20:1-33 (DRAM with “transfer MOS.FET[s] [] and [] capacitor[s]” formed in accordance with embodiment 5, which uses Embodiment 4’s downward sloping graded dopant concentration); Ex.1003, ¶184. In combining Kawagoe with Sakai, a POSITA would have therefore known to implement the combination of Sakai-Kawagoe in a DRAM device. §X.B.1.f (Motivation to Combine subsection).

**5. Dependent Claim 11: “The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.”**

Sakai-Kawagoe renders claim 7 obvious. §X.B.1. Sakai-Kawagoe also renders obvious the additional limitation of claim 11. Ex.1003, ¶¶185-187. Notably, Kawagoe teaches a semiconductor flash memory device. Ex.1007, 22:14-18 (“The semiconductor integrated circuit device 1 of the present embodiment 7, as shown in FIG. 28, is exemplified by a flash memory.”). The flash memory device includes a

CMOS “peripheral circuit region [] formed with the nMOS 4N and the pMOS 4P....” Ex.1007, 22:51-23:2. This peripheral circuit is fabricated according to twin-well CMOS technology, whereby NMOS transistors (*e.g.*, 4N) are formed in “p-well 6p3,” and PMOS transistors (*e.g.*, 4P) are formed in “n-well 6n2.” *Id.*, 22:51-65, FIG. 28. Significantly, Kawagoe explains that the teachings of Embodiment 4 (relied upon in mapping for claim 7) are applicable to Embodiment 7 and therefore flash memory. Ex.1003, ¶¶185-186. In particular, Embodiment 7 applies the teachings of Embodiment 4 to form a twin-well architecture with pMOS transistor 4P formed in an n-well and nMOS transistor 4N formed in a p-well, where both wells have a downward-sloping graded dopant concentration. Ex.1007, 22:22-29 (“In the present embodiment 7, too, the semiconductor substrate 2 is formed thereover with a p-well 6p3 and an n-well 6n2. The p-well 6p3 and n-well 6n2 are formed, ***as in the foregoing embodiments 4 and 6***, to extend from the surface of the epitaxial layer 2E to the upper portion of the semiconductor substrate body 2S. Moreover, their impurity concentrations are made gradually lower depthwise of the semiconductor region 2, ***as in the foregoing embodiment 4.***”), FIG. 28.

Sakai discloses use of its invention, the twin double well structure, to increase packing density in a peripheral circuit of a memory device, which Sakai recognized as a “widely used” CMOS semiconductor device. Ex.1006, 1:6-17, 1:55-2:5, 7:21-23, 8:9-24. In combining Kawagoe with Sakai, a POSITA would have known to

implement the combination of Sakai-Kawagoe in a flash memory device to realize the benefits of both increased packing density and aid in movement of alpha-particle-generated minority carriers to the substrate. Ex.1007, 16:2-11; §X.B.1.f (Motivation to Combine subsection); Ex.1003, ¶187.

### **C. Ground III**

Payne in combination with Wolf (“Payne-Wolf”) renders claims 9-11 obvious. Ex.1003, ¶¶188-203. Payne is directed to CMOS devices. Ex.1005, 1:5-10, 1:51-54, 6:57-59. Wolf is a well-known textbook that teaches fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS. *See generally* Ex.1008A; *id.*, Chapter 16 (“CMOS Process Integration”); Ex.1003, ¶¶188-189. Wolf also published over 20 years after Payne was filed. Exs.1014-15. A POSITA would have therefore understood and expected that the teachings of Wolf would apply to Payne, and would have looked to Wolf for the description of commercial applications of CMOS technologies, as well as advances and additional process details to the extent not covered in Payne. *Id.*

#### **1. Dependent Claim 9: “The semiconductor device of claim 7 wherein the semiconductor device is a central processing unit (CPU).”**

Payne renders obvious claim 7. §X.A.1. Payne-Wolf renders obvious the additional limitation of claim 9. Ex.1003, ¶¶190-194.

Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS

technology in IC production.” Ex.1008D, 181; Ex.1003, ¶190. It was also known to fabricate microprocessors (CPUs) using CMOS technology to achieve the benefits of “lower power-dissipation” in such devices. Ex.1008B, 368-370; Ex.1032, 1334 (see “microcomputer”); Ex.1003, ¶190.

Rabaey confirms this. Ex.1041, 180 (“The [CMOS] inverter is truly the nucleus of all digital [logic] designs” and, together with other “[logic] gates such as NAND, NOR, or XOR ... form the building blocks for modules such as multipliers and processors.”), 37 (“Modern [CMOS] processes are increasingly using a dual-well [(twin-well)] approach that uses both n- and p-wells ...”), 383-84, FIG. 8-6 (showing Intel Pentium processor “designed in a 0.18μm CMOS technology.”); Ex.1003, ¶191. Sze also confirms this, describing a system-on-a-chip that includes CMOS “*logic IC (e.g., CPU)*” fabricated using twin-well CMOS technology. Ex.1042, 525-26, FIGS. 37-38; Ex.1003, ¶191.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A.

It would have been obvious to fabricate known CPUs using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶¶192-194. Additionally, using Payne’s technology to form CPUs would have

merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known CPU designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art CPUs) with another (Payne’s improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne’s twin-well CMOS process was a known improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing known CPUs, designed for implementation using CMOS technology. *Id.*

**2. Dependent Claim 10: “The semiconductor device of claim 7 wherein the semiconductor device is a DRAM device.”**

Payne renders obvious claim 7. §X.A.1. Payne-Wolf renders obvious the additional limitation of claim 10. Ex.1003, ¶¶195-198.

Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex.1008D, 181; Ex.1003, ¶195. It was also known to fabricate DRAM devices for “the advantages of cost per bit, device density, and flexibility of use (i.e., both read and write operations are possible) [which] have made DRAMs the most widely used form of semiconductor memory to date,” and to do so using CMOS technology to take advantage of “lower power dissipation [] and smaller soft error rates.” Ex.1008B, 587, 596-597; Ex.1003, ¶195.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology

to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A.

It would have been obvious to fabricate known DRAM devices using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶¶196-198. Additionally, using Payne’s technology to form DRAMs would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known DRAM designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology contemplated by Wolf for DRAM) with another (Payne’s improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne’s improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known DRAM designed for implementation using CMOS technology. *Id.*

**3. Dependent Claim 11: “The semiconductor device of claim 7 wherein the semiconductor device is a flash memory device.”**

Payne renders obvious claim 7. §X.A.1. Payne-Wolf renders obvious the additional limitation of claim 11. Ex.1003, ¶¶199-203.

Twin-well CMOS technology was, by the early 2000s, “the dominant CMOS technology in IC production.” Ex.1008D, 181; Ex.1003, ¶199. It was also known to fabricate semiconductor flash memory devices to achieve the benefits of “high density [], small-die size, lower cost, and hot-electron writability of EPROMs, together with the easy erasability, on-board reprogrammability, and electron-tunneling erasure features of EEPROMs,” and to do so using CMOS technology for “lower power-dissipation.” Ex.1008B, 632-634; Ex.1008A, 808-810; Ex.1003, ¶199. Indeed, flash memory devices commonly used CMOS technology. Ex.1008B, 633-635 (describing known “CMOS flash-EEPROM” devices); Ex.1007, 22:16-17 (flash EEPROM is flash memory), 22:10-23:2, FIG. 28 (peripheral flash memory circuit with CMOS transistors); Ex.1003, ¶200.

Payne teaches an improvement on “twin tub” (twin-well) CMOS technology to reduce separation “between source and drain regions of adjacent [transistor] devices” and thus increase packing density of CMOS semiconductor devices. Ex.1005, Abstract, 1:5-8, 1:51-68, 6:17-21, 6:57-59, 1:9-50; §IX.A.

It would have been obvious to fabricate known flash memory devices using Payne’s improved twin-well CMOS technology for the benefit of increased packing density. Ex.1003, ¶¶201-203. Additionally, using Payne’s technology to form flash memory would have merely amounted to (1) use of a known technique (Payne’s improved twin-well CMOS process) to improve similar devices (known CMOS flash

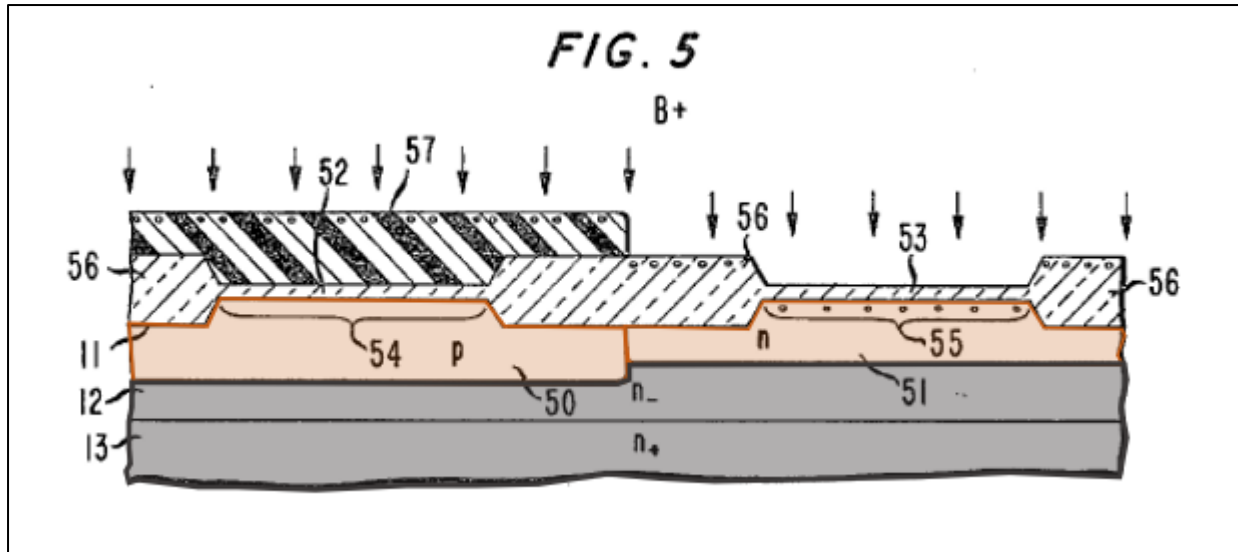
memory designs) in the same way (to increase packing density) and (2) a simple substitution of one known element (CMOS technology for prior art flash memory) with another (Payne's improved CMOS technology). *Id.* There would have been a reasonable expectation of success with predictable results because Payne's improved CMOS process was an improvement over conventional twin-well CMOS process and would have been used for its intended purpose in manufacturing a known flash memory designed for implementation using CMOS technology. *Id.*

**D. Ground IV**

**1. Dependent Claim 8: "The semiconductor device of claim 7 wherein said first and second static unidirectional electric fields are adapted to respective grading of dopants to aid movements of carriers in respective active regions."**

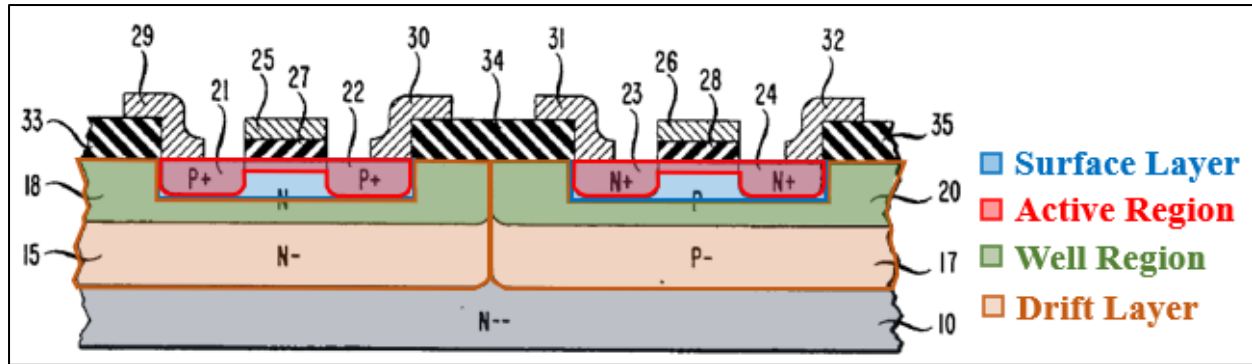
Payne discloses or renders obvious claim 7. §X.A.1. Payne in combination with Parrillo ("Payne-Parrillo") renders obvious the additional limitation of claim 8. Ex.1003, ¶¶204-221. Parrillo and Payne are contemporaneous patents that share a common inventor (Richard S. Payne). Ex.1025; Ex.1005. Both patents were originally assigned to AT&T Bell Labs. *Id.*

Parrillo is directed to "twin-tub" (twin well) CMOS semiconductor devices. Ex.1025, 1:13-20, 2:22-25 ("[T]he invention is a twin-tub complementary CMOS integrated circuit in which the n-tubs and p-tubs are contiguous with one another with no spacing between."). Parrillo's Figure 5 below illustrates contiguous p-tub (p-well) 50 (left, tan) and n-tub (n-well) 51 (right, tan).



Ex.1025, FIG. 5. Parrillo explains that each tub (well) of its “twin-tub” CMOS device contains “one or more transistors.” *Id.*, 3:22-25 (“The device may, for example, be a VLSI circuit in which case there would be a large number of tubs of each type, each of which might contain *one or more transistors.*”). Indeed, a VLSI device contains a very large number of transistors. *Id.*, 1:13-20, 3:34-38 (“a VLSI circuit employ[s] a large number of p-channel and n-channel transistors.”).

Payne is directed to improving the “twin-tub” (twin-well) CMOS technology similar to that described in Parrillo by adding a shallow well (“surface region”) (green) in each deep well (“tub”) (tan) of a twin-tub CMOS device, as illustrated in Payne’s Figure 10 below. Ex.1005, 1:5-14, 1:59-2:28, 6:20-21; *id.*, 1:15-50; §§ X.A.1.e-g; Ex.1003, ¶¶205-208. Payne teaches that this nested well structure improves packing density. *Id.*, Abstract, 1:51-54, 6:17-19, 6:57-59.



Ex.1005, FIG. 10. A POSITA would have been motivated to apply Payne's improved CMOS technology to a known twin-tub CMOS semiconductor device that has individual tubs containing multiple transistors, such as that described by Parrillo, to achieve high packing density as taught by Payne. Ex.1003, ¶¶209-211. Doing so would have resulted in forming Payne's nested well structure in the tubs to reduce the spacing between active regions of adjacent transistors. *Id.*; Ex.1005, Abstract, 1:51-54, 6:17-19, 6:57-59. There is reasonable expectation of success because the Payne and Parrillo patents are closely related (as discussed above) and Payne shows that a POSITA knew how to use Payne's CMOS technology to improve a twin-tub CMOS device similar to that described by Parrillo. Ex.1005, 6:20-21 (Payne's technology "is designed primarily for twin-tub structures"); Ex.1003, ¶210. This combination of Payne and Parrillo would have merely amounted to (1) use of a known technique (Payne's improved twin-tub CMOS technology) to improve similar devices (known twin-tub CMOS devices with individual tubs having multiple transistors) in the same way (to increase packing density) and (2) a simple

substitution of one known element (Parrillo's twin-tub CMOS technology) with another (Payne's improved twin-tub CMOS technology) to fabricate a known twin-tub CMOS device with individual tubs having multiple transistors.

While Payne's Figure 10 illustrates a single transistor formed in each tub, Payne expressly discloses that "the figures show fabrication of a device which is typically part of an integrated circuit including many other [transistor] devices." Ex.1005, 2:53-55, 6:17-19, 6:57-59. And given the jagged edges to the left and right of Payne's Figure 10, Payne is at least suggestive that its illustrated tubs contain multiple transistors just like Parrillo describes. Ex.1025, 3:22-25. To illustrate this, Dr. Blalock has prepared Figure 10M below, which extends Payne's Figure 10 past its left jagged edge and shows two PMOS transistors, each with its active region 21/22 (red), formed in the nested n-well structure (left) that consists of n-tub 15 (tan) and shallow n-well 18 (green) disposed in it. Ex.1003, ¶¶212-213. As detailed in §§X.A.1.e-g, tub 15 is an exemplary SDL. §§X.A.1.e-g.

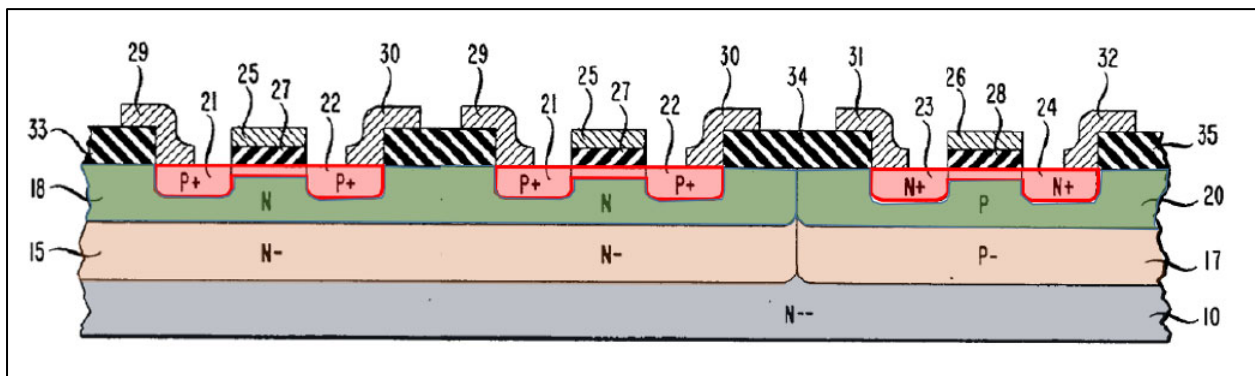
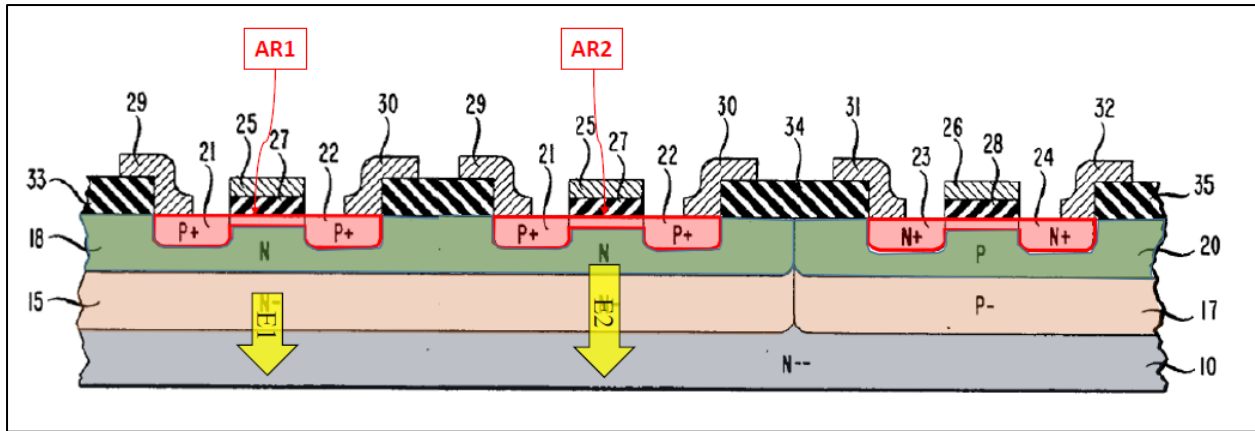


FIG. 10M. Dr. Blalock explains that Figure 10M not only reflects the teachings of

Payne and Parrillo, it also reflects standard practice in CMOS layout and fabrication. Ex.1003, ¶¶213-217. Other prior art references confirm this. *Id.*; Ex.1044 (Maziasz), 27 (“Each cell consists of two horizontal diffusion rows for pMOS and nMOS transistors. This implies that single p- and n-wells can be used.”), Figure 2.3(b); Ex.1046 (Yamada), 6:51-53 (“diffusion layers [(active regions)] 60 and 61 [of] NMOS transistors” formed in “a common p-well 43” as shown in Figures 5-6).

Figure 10M, reproduced below, makes clear that Payne-Parrillo satisfies claim 8. Ex.1003, ¶¶218-221. The figure shows that, as discussed in §X.A.1.f, tub 15 (SDL) (tan) generates a first static unidirectional electric field E1 (yellow) that aids movements of carriers that are in, or originate from, active region AR1 (red) above it. Ex.1003, ¶¶218-221; Ex.1005, 1:60-68, 5:21-29; §X.A.1.f; Ex.1013, 431; §§X.A.1.d-g. Likewise, as discussed in §X.A.1.g, well region 18 (green) generates a second static unidirectional electric field E2 (yellow) that aids movements of carriers that are in, or originate from, active region AR2 (red) above it. *Id.* For this mapping, the surface layer of claim 7 includes both active regions AR1 and AR2. Ex.1003, ¶¶218-221.



Ex.1005, FIG. 10. Electric fields E1 and E2 are adapted to the grading of dopants in tub 15 (SDL) (tan) and well region 18 (green), respectively, because the direction of electric fields E1 and E2 (*i.e.*, toward the surface or away from the surface) is dependent on the local slope of the graded-dopant profile according to Applicant's repeated representations during prosecution of the parent '195 Patent, the Jastrzebski and Kamins prior art relied on by Applicant during its prosecution, and PO's statements in its claim construction brief as discussed in §X.A.1.f (including fn.6). Additionally, the magnitude of electric fields E1 and E2 also depends on the local grading of dopants. §X.A.1.g; Ex.1022, [0071]; Ex.1003, ¶¶218-221.

## XI. THE BOARD SHOULD INSTITUTE IPR

### A. 35 U.S.C. § 314(a)

The merits of this Petition are strong, which alone warrants institution. On June 21, 2022, the Director issued an interim procedure regarding application of the *Fintiv* factors (Interim Procedure) in which the Director clarified that “the PTAB will not deny institution [] under *Fintiv* (i) when a petition presents compelling

evidence of unpatentability.” Director Vidal, Memorandum, “Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation,” 9 (June 21, 2022). As just one example of compelling evidence here, Ground I is a single-reference obviousness ground explaining how Payne discloses or, at a minimum, renders obvious independent claim 7. While Payne was relied on in IPR2020-00290, that IPR proceeding was terminated prior to reaching institution decision. Ex.1036. Further, Sakai, Kawagoe, Wolf and Parrillo were not relied on in IPR2020-00290, and none of the ground references were before the Examiner during prosecution of the ’502 Patent. This evidence, “if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable” (*Id.*, 4) and the Board must decline to exercise its discretion under §314(a) to deny institution. *Id.*; *PopSockets LLC v. Flygrip, Inc.*, IPR2022-00938, Paper 8 at 9 (P.T.A.B. Nov. 1, 2022).

### **Fintiv Factors**

The *Fintiv* factors also weigh in favor of institution. A final written decision (FWD) in this case should issue in July 2024. The recent transfer of the District Court Case (as it pertains to Petitioner) to the District of Oregon (Ex.1034), means the district court has not yet invested significant resources and that trial is not yet set. Further, the Director directed the PTAB to consider “statistics on median time-to-trial for civil actions in the district court in which the parallel litigation resides.”

Interim Procedure, 8-9. The median time to trial in the District of Oregon is 44.3 months (Ex.1024, 74), giving a trial date of October 2025 or later and well after the statutory deadline for FWD.

**General Plastics Factors**

The *General Plastics* factors weigh in favor of institution. *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 15–16 (P.T.A.B. Sep. 6, 2017) (hereinafter, “*General Plastics*”). The instant Petition is Petitioner’s first and only petition challenging claims of the ’502 Patent. Three years ago, Samsung Electronics Co. filed IPR2020-00290 (“Samsung Petition”) challenging claims 7, 10, and 11 of the ’502 Patent. The Samsung Petition was terminated more than two years ago on July 10, 2020, before an institution decision. Ex.1036. The fact that the instant Petition is filed years after the Samsung Petition is entirely due to PO’s litigation strategy. *Unified Pats Inc. v. Bradium Techs. LLC*, No. IPR2018-00952, 2018 WL 6721788, at \*9 (P.T.A.B. Dec. 20, 2018); *Xilinx, Inc. v. Arbor Global Strategies, LLC*, IPR2020-01568, Paper 12 at 10 (P.T.A.B. Mar. 5, 2021). Further, there is no relationship between Samsung and Petitioner, and this Petition challenges additional claims under different grounds. This “factor alone weighs heavily against ... exercis[ing] discretion under §314(a) to deny institution” and the Board should not “impute the actions of an unrelated petitioner on this Petitioner.” *Unified Pats*, 2018 WL 6721788, at \*9.

The PTAB has found that the second factor has “little probative value” when, as here, the “Petitioner was not a petitioner in the prior proceeding challenging” the ’502 Patent. *Id.* For the third, fourth, and fifth factors, the Board never issued an institution decision in the Samsung Petition and Petitioner did not learn of the prior art in the Samsung Petition until after the District Court Case was filed. The time elapsed between the Samsung Petition and this Petition is a function of PO waiting over two years to file the District Court Case after filing against Samsung (and 18 months after the Samsung case was terminated). Furthermore, Petitioner asserts four additional references (Sakai, Kawagoe, Wolf and Parrillo) that were not asserted in the Samsung Petition, and against different challenged claims. For the sixth and seventh factors, “given that [Samsung’s Petition] was terminated due to settlement,” institution here will not waste the Board’s resources, nor will it impact the requirement under 35 U.S.C. §316(a)(11). *Id.* at \*10. Thus, these factors weigh in favor of institution. *Id.* at \*11.

**B. 35 U.S.C. § 325(d)**

The Board should likewise not deny institution under §325(d) because all six *Becton Dickinson* factors weigh in favor of institution. *Becton, Dickinson, & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (P.T.A.B. Dec. 15, 2017); *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020).

The Board has consistently “held that a reference that ‘was neither applied against the claims nor discussed by the Examiner’ does not weigh in favor of exercising [] discretion under §325(d).” *Fasteners for Retail, Inc. v. RTC Indus., Inc.*, IPR2019-00994, Paper 9 at 7–11 (P.T.A.B. Nov. 5, 2019); *Bowtech Inc. v. MCP IP, LLC*, IPR2019-00383, Paper 14 at 5-6 (P.T.A.B. Aug. 6, 2019). That is the case here because none of the ground references (Payne, Sakai, Kawagoe, and Wolf) is cited art, and the arguments presented herein were not considered during prosecution of the ’502 Patent.

**Payne and Sakai are not cumulative with the Rhodes cited art** – In its POPR to the terminated IPR2022-00290, PO argued that Payne is cumulative with Rhodes on the alleged ground that the nested well structure of Payne is nothing more than a single well formed with multiple implants. Ex.1016, 25-41. This is incorrect.

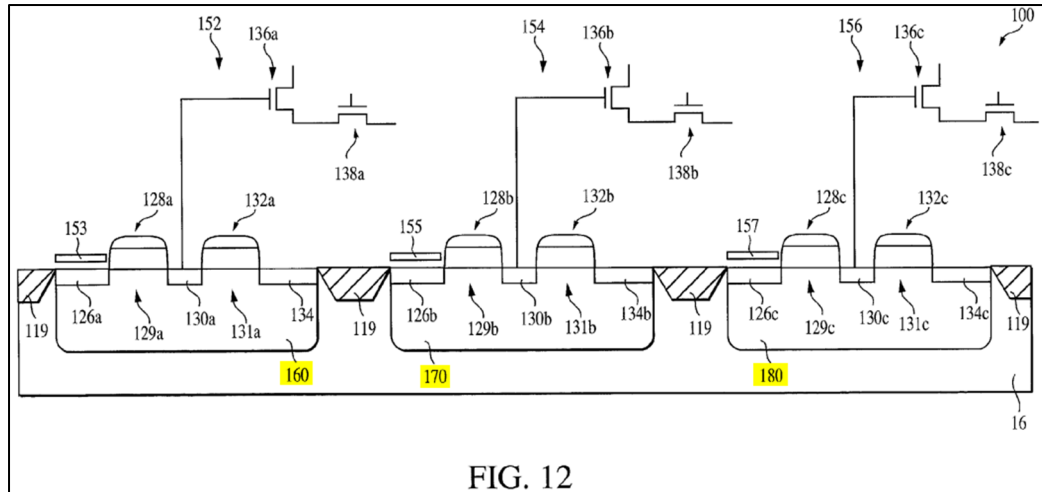
**First**, Sakai expressly discloses having a twin **double well** structure with a shallow **well** region disposed in a deep **well** region. Ex.1006, 1:57-67, 7:32-37, FIGS. 10D, 11E, 15. These well regions are all labeled as “P-WELL” or “N-WELL” in Sakai’s figures. *Id.* Sakai’s nested wells clearly do not form one single well. They are expressly disclosed and labeled as distinct wells.

**Second**, Payne’s nested well structure, in which shallow wells are formed in deeper wells with **separate** implants **and** annealing steps, differentiates Payne from Rhodes which does not teach a nested well structure. Ex.1003, ¶¶224-225. As Payne

describes and illustrates in Figures 2 and 5-9, the deep wells (“tub regions”) of Payne’s nested well structure are formed first, using their own specific masks, ion implantation and thermal drive-in process steps. Ex.1005, 3:17-4:30. The shallow wells (“surface regions”) are then separately formed, using different masks, ion implantation and thermal drive-in process steps. Ex.1005, 4:31-5:17, 5:44-55. Payne’s separately formed deep and shallow wells, such as wells 15 and 18, are not a single well formed using multiple implants. *Id.*

***Third,*** Sakai likewise uses separate implants and annealing steps to form each well of its nested well structure. Ex.1006, 5:56-6:4, 6:24-28, 6:52-58, FIGS. 10A, 10B. A POSITA would have therefore understood Payne’s tub and surface regions to constitute distinct wells just as Sakai used that term. Ex.1003, ¶226.

In contrast to Payne and Sakai’s structures, Rhodes teaches a twin well architecture with side-by-side wells 160/170/180 (shown below) that Payne and Sakai seek to improve upon with their nested well structure. Ex.1011, [0064]; Ex.1005, 1:24-68; Ex.1006, 1:6-2:39.



Ex.1011, FIG. 12, [0064]. Rhodes does not mention or suggest (in paragraph [0064] or otherwise) forming a nested well structure and thus does not teach a “well region disposed in [a] single drift layer.” Ex.1003, ¶228. And none of its figures shows a deep well and a shallow well. *Id.* As discussed in Section VI, this was the reason the Examiner allowed the claims of the parent ’195 Patent to issue over Rhodes (and other art, including Kamins and Jastrzebski). Ex.1040, 346. Nowhere in the prosecution of the ’502 Patent or parent ’195 Patent did the Applicant or Examiner discuss nested well structures, as Payne and Sakai disclose. Thus, there is no support for PO’s argument in the POPR that “it is reasonable to infer that the Examiner agreed with the argument PO makes explicitly herein that a multiple-implant well does not disclose a well region disposed in a single drift layer.” Ex.1016, 27.

PO also implied in its POPR that the Applicant overcame Rhodes-based rejections during prosecution of the parent ’195 Patent by adding the “drift layer” limitation to the pending claims. Ex.1016, 22-24. This is incorrect. Applicant

overcame Rhodes-based rejections on the basis that Rhodes is a “CMOS imaging device,” and by amending claims to include a “graded dopant concentration in the...active channel regions,” (a limitation that was later removed). Ex.1040, 94-96. The “drift layer” limitation was added later in the process after several intervening rejections. There is no indication the Examiner specifically considered Rhodes in relation to the “drift layer” limitation, let alone the “well region disposed in said single drift layer” limitation.

**Payne and Sakai were misapprehended or overlooked during prosecution of later patents** – PO disclosed Payne, IPR2020-00290, and Sakai during later prosecution of the ’222 and ’014 Patents. Ex.1020, 111-116; Ex.1021, 71-76. However, there is no indication that the Examiner of either patent ever evaluated Payne, the IPR proceedings, or Sakai, nor understood their significance. In particular, the Examiner may not have understood the significance of IPR2020-00290, which challenges certain claims of the ’502 Patent, because, except for one claim of the ’222 Patent (claim 44), the other 43 claims of the ’222 Patent and 30 claims of the ’014 Patents are wholly different from the claims of the ’502 Patent, at least because they do not claim a “surface layer” and a “single drift layer.” Ex.1018, claims 1-30; Ex.1017, claims 1-43. Notably, the Examiner did not issue any art-based rejection for either patent. Ex.1020, 226-229; Ex.1021, 176-179. Nor did the Examiner address Payne or Sakai in the notice of allowance for either patent. *Id.* In

fact, the prosecution history record is clear that the Examiner erroneously considered Hong (Ex.1027)—which is not prior art because it was filed on August 31, 2005, long after the claimed priority date of the '502 Patent—to be “the closest reference.” *Id.* Even if the Examiner is deemed to have considered Payne, the IPR proceedings, or Sakai, the Examiner “misapprehended or overlooked” their relevance and made a “material error,” warranting institution here. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020) (precedential); *Apple Inc. v. Seven Networks, LLC*, No. IPR2020-00506, 2020 WL 5223106, at \*12-13 (P.T.A.B. Sept. 1, 2020); *Peloton Interactive, Inc. v. Ifit, Inc.*, IPR2022-00030, Paper 12 at 16 (P.T.A.B. Apr. 22, 2022).

Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502

Dated: January 30, 2023

Respectfully submitted,

/s/ Robert A. Appleby, P.C.

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**CERTIFICATION OF WORD COUNT**

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502 contains, as measured by the word-processing system used to prepare this paper, 13,884 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Dated: January 30, 2023

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**CERTIFICATE OF SERVICE ON PATENT OWNER  
UNDER 37 C.F.R. § 42.105**

I hereby certify that on January 30, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 9,190,502 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on the USPTO Patent Center

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