

U.S. Patent No. 10,705,588		
1[pre]. A processor comprising:	8[pre]. A system comprising:	20[pre]. An apparatus comprising:
	8[a]. a system memory;	
1[a]. a plurality of cores including a first core operable at a first voltage and at a first frequency, and	8[b]. a plurality of cores coupled to the system memory; [c]. a first core of the plurality of cores operable at a first voltage and at a first frequency, and	20[a]. means for operating a first core at a first voltage and at a first frequency while concurrently operating a second core at a second voltage independent of the first voltage and at a second frequency different from the first frequency;
1[b]. a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;	8[d]. a second core of the plurality of cores operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;	
1[c]. graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and	8[e]. graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and	20[b]. means for independently operating a graphics processor at a third frequency different from the first frequency and the second frequency; and
1[d]. an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.	8[f]. an interconnect to couple the graphics processing circuitry to the system memory, the interconnect operable at a fourth frequency different from at least the first and second frequencies.	20[c]. interconnect means to couple the graphics processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies.

2. The processor of claim 1, further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and to cause the second core to independently operate at the second frequency.	9. The system of claim 8, further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and to cause the second core to independently operate at the second frequency.	
3. The processor of claim 1, further comprising: a non-core power domain comprising a cache shared by the plurality of cores.	10. The system of claim 8, further comprising: a non-core power domain comprising a cache shared by the plurality of cores.	
4. The processor of claim 2, further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.	11. The system of claim 9, further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.	
5. The processor of claim 4, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.	12. The system of claim 11, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.	

6. The processor of claim 5, wherein the second power management circuitry and/or logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.	13. The system of claim 12, wherein the second power management circuitry and/or logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.	
7. The processor of claim 3, further comprising: power management circuitry and/or logic to cause the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores, respectively.	14. The system of claim 10, further comprising: power management circuitry and/or logic to cause the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores, respectively.	
	15. The system of claim 8, further comprising: a chipset coupled to the plurality of cores, the chip set comprising a plurality of interfaces to couple the cores to a plurality of I/O devices.	
	16. The system of claim 15, wherein one of the I/O devices comprises an audio generation device.	
	17. The system of claim 16, wherein one of the I/O devices comprises a video rendering device.	
	18. The system of claim 17, wherein one of the I/O devices comprises a user input device.	

	19. The system of claim 18, wherein one of the I/O devices comprises a network communication device.	
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