



Intel® E8501 Chipset North Bridge (NB)

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Revision History

Revision Number	Description	Date
-001	• Initial public release	April 2006

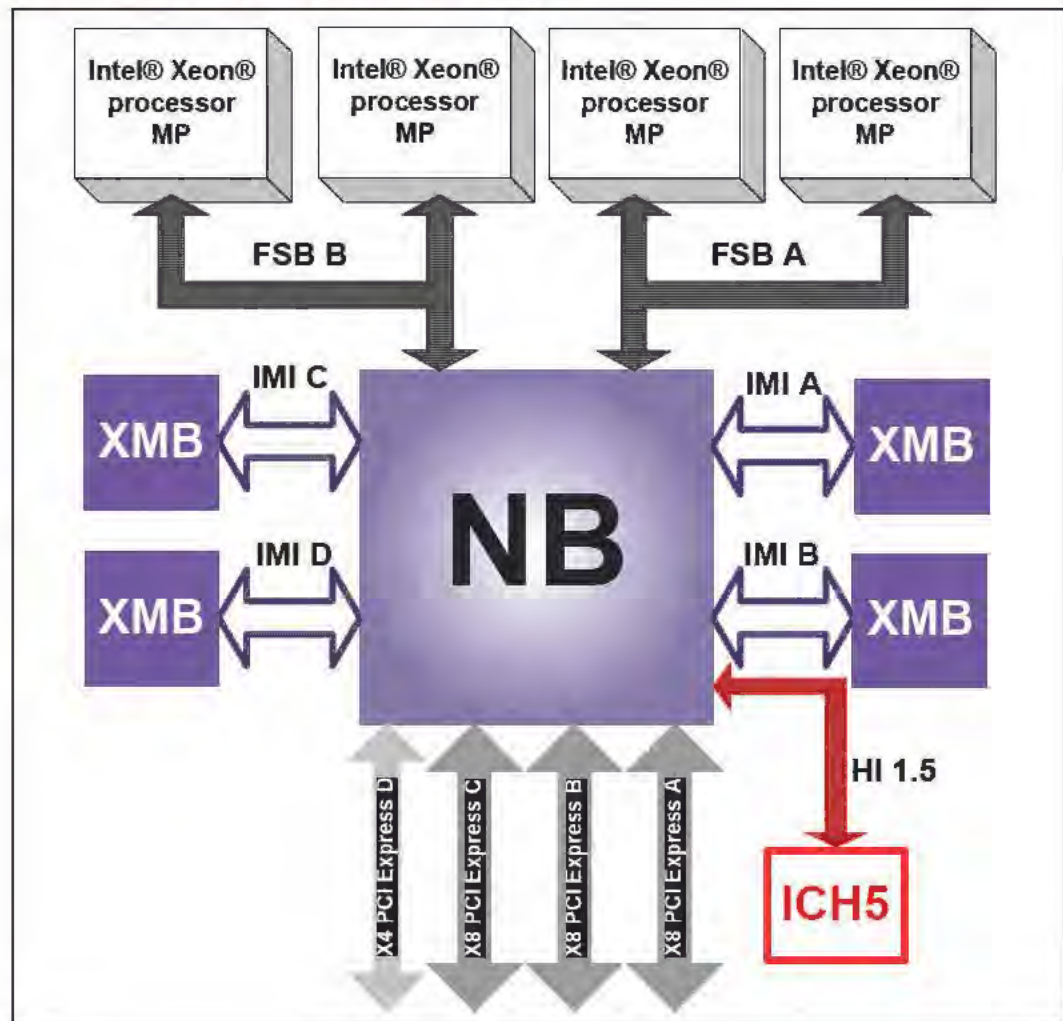
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1 Introduction

The Intel® E8501 chipset is a 4-way server chipset offering world class performance. The chipset is built architecturally around the Intel® E8501 chipset north bridge (NB) and the Intel® E8501 chipset external memory bridge (XMB).

This document, the *Intel® E8501 Chipset North Bridge (NB) Datasheet*, describes the features, modes and registers supported by the Intel® E8501 chipset north bridge (NB) component only. Additional details on the Intel® E8501 chipset external memory bridge (XMB) are described in a separate document, the *Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet*. For details on any other platform component, please refer to the component's respective documentation. This chapter is an introduction to the entire platform.

Figure 1-1. Intel® E8501 Chipset System Block Diagram



1.1 Intel® E8501 Chipset North Bridge (NB) Feature List

The NB is the center of the Intel® E8501 Chipset architecture (refer to [Figure 1-1](#)). The NB provides the interconnect to:

- 64-bit Intel® Xeon® processor MP or Dual-Core Intel® Xeon® processor 7000 sequence via two 667 MHz or 800 MHz front side buses optimized for server applications
- XMBs via four Independent Memory Interfaces (IMI)
- I/O components via one x4 & three x8 PCI Express* links and Intel® 82801EB I/O Controller Hub 5 (ICH5) via the HI 1.5

1.1.1 Processor Front Side Bus Support

- Supports up to 4 64-bit Intel® Xeon® processor MP or Dual-Core Intel® Xeon® processor 7000 sequence
- 667 MHz or 800 MHz operation
- Maintains coherency across both buses
- Double-pumped 40-bit address buses with ADS every other clock which provides a total address bandwidth of 167 million addresses/second
- Quad-pumped, 64-bit data bus providing a bandwidth of 5.3 GB/s per bus at 667 MHz or 6.4 GB/s per bus at 800 MHz
- In-Order-Queue depth of 12
- Maintains coherency across both buses
- Return data by Enhanced Deferred Acknowledgment to allow out-of-order completion
- ECC protection on data signals and parity protection on address signals

1.1.2 Independent Memory Interface

- 4 Independent Memory Interface (IMI) ports, each with up to 5.33 GB/s inbound (read) bandwidth and 2.67 GB/s outbound (write) bandwidth simultaneously
- 40-bit addressing support provides one terabyte (2^{40} bytes) addressing capability (this is in excess of maximum physical memory supported by the Intel® E8501 chipset platform)
- Memory technology independent
- Hot-plug support on each IMI

1.1.3 I/O Interfaces

The Intel® E8501 chipset relies primarily on PCI Express to provide the interconnect between the NB and the I/O subsystem. The I/O subsystem is based on one x4 PCI Express link, three x8 PCI Express links (each of which can be split into two x4 links), and one HI1.5 link.

PCI Express*

- One x4 and three x8 links. Each x8 link can be configured as two x4 links, making a total of seven x4 links
- 1 GB/s bandwidth in each direction for x4 links and 2 GB/s for x8 links
- All ports support Hot-Plug

HI 1.5

- 8-bit wide, 4x data transfer, 66 MHz base clock
- 266 MB/s bandwidth
- Legacy I/O interconnection to the ICH5

1.1.4 Transaction Processing Capabilities

- 64 transactions processed concurrently
- 128-entry Common Data Cache (CDC) for write combining and write buffering

1.1.5 RASUM

- ECC on all internal data paths
- Error Detection and Logging Registers on all interfaces
- CRC32 and CRC16 on PCI Express links
- Packet level CRC on IMI's
- IMI error recovery support via read or write retry
 - Transient DRAM read error recovery
 - Transient single IMI wire failure recovery
- Memory mirroring support
- Parity protection on Hub Interface 1.5 (address, control & data)
- Hot-Plug support on PCI Express and IMI ports
- SMBus and JTAG interfaces for system management
- Support for Mirroring of memory
- Parity protected Hub Interface (Address, Control & Data)

1.1.6 Package

- 1432 pin FC-BGA3 (42.5 x 42.5 mm) with a pin-pitch of 1.09 mm.

1.2 Intel® E8501 Chipset eXternal Memory Bridge (XMB) Feature List

The Intel® E8501 chipset external memory bridge (XMB) is an intelligent memory controller that bridges the IMI and DDR interfaces. Each XMB connects to one of the NB's four IMI interfaces. The Intel® E8501 chipset may operate with 1 to 4 XMBs.

1.2.1 DDR Memory Support

- Dual DDR memory channels operating in lockstep with four DIMM slots per channel
- DIMMS must be populated in pairs, and DIMMS within a pair must be identical
- Supports either DDR at 266 MHz or 333 MHz or DDR2 at 400 MHz
- Supports 256-Mb, 512-Mb, and 1-Gb technologies
- Registered ECC DIMMS required
- Integrated I²C* controller for reading DIMM SPD data

1.2.2 IMI Support

- High speed, point-to-point, differential, recovered clock interconnect
- 2.67 GB/s outbound (to the XMB) and 5.33 GB/s inbound (from the XMB) simultaneous bandwidth
- Hot-Plug support

1.2.3 RASUM Features

- ECC on all internal data paths
- Error detection and logging registers on all interfaces
- Packet level CRC protection on IMI
- IMI error recovery support via read or write retry
 - Transient single IMI wire failure recovery
- Intel® x8 Single Device Data Correction (x8 SDDC) technology
- DIMM demand and patrol scrubbing
- DIMM sparing
- Hardware memory initialization
- Performance counters
- SMBus and JTAG interfaces for system management
- Hot-plug capable IMI

1.2.4 Intel® E8501 Chipset eXternal Memory Bridge (XMB) Package

- 829-pin FC-BGA3 (37.5 x 37.5 mm) with a pin-pitch of 1.27 mm

1.3 Terminology

Term	Description
Agent	A logical device connected to a bus or shared interconnect that can either initiate accesses or be the target of accesses.
Asserted	Signal is set to a level that represents logical true.
Asynchronous	1. An event that causes a change in state with no relationship to a clock signal. 2. When applied to transactions or a stream of transactions, a classification for those that do not require service within a fixed time interval
Atomic operation	A series of two or more transactions to a device by the same initiator which are guaranteed to complete without intervening accesses by a different master. Most commonly required for a read-modify-write (RMW) operation.
Bit Interleave, Address Bit Permting	The way the bits in a cache line are mapped to DIMM rows, banks, and columns (DDR SDRAM) of memory.
Buffer	1. A random access memory structure. 2. The term I/O buffer is also used to describe a low level input receiver and output driver combination.
Cache Line	The unit of memory that is copied to and individually tracked in a cache. Specifically, 64 bytes of data or instructions aligned on a 64-byte physical address boundary.
Cache Line Interleave	The way a series of cache lines are mapped to DRAM devices.
Cfg	Used as a qualifier for transactions that target PCI configuration address space.
Character	The raw data Byte in an encoded system (e.g. the 8b value in a 8b/10b encoding scheme). This is the meaningful quantum of information to be transmitted or that is received across an encoded transmission path.
Coherent	Transactions that ensure that the processor's view of memory through the cache is consistent with that obtained through the I/O subsystem.
Command	The distinct phases, cycles, or packets that make up a transaction. Requests and Completions are referred to generically as Commands.
Completion	A packet, phase, or cycle used to terminate a Transaction on a interface, or within a component. A Completion will always refer to a preceding Request and may or may not include data and/or other information.
Core	The internal base logic in the NB.
CRC	Cyclic Redundancy Check; A number derived from, and stored or transmitted with, a block of data in order to detect corruption. By recalculating the CRC and comparing it to the value originally transmitted, the receiver can detect some types of transmission errors.

Term	Description
Critical Word First	The Independent Memory Interface specification constrains the XMB to deliver the words of a cache line in a particular order such that the word addressed in the request appears in the first data transfer.
DDR	Double Data-Rate memory.
DDR Channel	One electrical interface to one or more DIMMs, supporting 8 bytes of data and 1 byte of ECC.
Deasserted	Signal is set to a level that represents logical false.
DED	Double-bit Error Detect.
Deferred Transaction	A front side bus Split Transaction. The requesting agent receives a Deferred Response which allows other transactions to occur on the bus. Later, the response agent completes the original request with a separate Deferred Reply transaction.
Delayed Transaction	A transaction where the target retries an initial request, but unknown to the initiator, forwards or services the request on behalf of the initiator and stores the completion or the result of the request. The original initiator subsequently re-issues the request and receives the stored completion.
DFM	Design for Manufacturability.
DFT	Design for Testability.
DIMM	Dual-in-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Rank	That set of SDRAMs on one DDR branch which provides the data packet.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR channel.
DIMM Stack	A set of DIMMs that share data lines.
Direct Memory Access	Method of accessing memory on a system without interrupting the processors on that system.
DMA	See Direct Memory Access.
Downstream	Describes commands or data flowing away from the processor-memory complex and toward I/O. The terms Upstream and Downstream are never used to describe transactions as a whole. (e.g. Downstream data may be the result of an Outbound Write, or an Inbound Read. The Completion to an Inbound Read travels Downstream).
DRAM Page (Row)	The DRAM cells selected by the Row Address.
DW	A reference to 32 bits of data on a naturally aligned four-byte boundary (i.e. the least significant two bits of the address are 00b).
ECC	Error Correcting Code.
Front Side Bus	Processor-to-NB interface. The front side bus in this document refers to operation at 166/333/667 MHz (Bus Clock/Address/Data) or 200/400/800 MHz (Bus Clock/Address/Data). The front side bus is not compatible with the P6 front side bus.
Full Duplex	A connection or channel that allows data or messages to be transmitted in opposite directions simultaneously.

Term	Description
GB/s	Gigabytes per second (10^9 bytes per second).
Gb/s	Gigabits per second (10^9 bits per second).
Half Duplex	A connection or channel that allows data or messages to be transmitted in either direction, but not simultaneously.
HI1.5	The Intel proprietary hub interface that connects the NB to the ICH5
Host	This term is used synonymously with Processor.
I/O	1. Input/Output. 2. When used as a qualifier to a transaction type, specifies that transaction targets Intel architecture-specific I/O space. (e.g., I/O read).
Intel® ICH5	The I/O Controller Hub component that contains the legacy I/O functions. It communicates with the NB over a proprietary interconnect called Hub Interface.
Implicit Writeback	A snoop initiated data transfer from the bus agent with the modified Cache Line to the memory controller due to an access to that line.
Inbound	A transaction where the request destination is the processor-memory complex and is sourced from I/O. The terms Inbound and Outbound refer to transactions as a whole and never to Requests or Completions in isolation. (e.g. An Inbound Read generates Downstream data, whereas an Inbound Write has Upstream data. Even more confusing, the Completion to an Inbound Read travels Downstream.)
Inbound (IB)/Outbound (OB) AKA Upstream/ DownStream, Northbound/Southbound, Upbound/Downbound	Up, North, or Inbound is in the direction of the Independent Memory Interface, Down, South, or Outbound is in the direction of other IO (SDRAM, SMBus). or Inbound is towards the NB, Outbound is away from it.
Initiator	The source of requests. (IBA) An agent sending a request packet on PCI Express is referred to as the Initiator for that Transaction. The Initiator may receive a completion for the Request. [PCI Express]
Isochronous	A classification of transactions or a stream of transactions that require service within a fixed time interval.
Layer	A level of abstraction commonly used in interface specifications as a tool to group elements related to a basic function of the interface within a layer and to identify key interactions between layers.
Legacy	Functional requirements handed down from previous chipsets or PC compatibility requirements from the past.
Line	Cache line
Line-Atomically	Atomic operation on one cache lines. Operations on other lines proceed normally during the line-atomic operation. Other operations to the same cache line are suspended until the line-atomic operation is complete.
Link	A full duplex transmission path between any two PCI Express devices.
LSb	Least Significant Bit
LSB	Least Significant Byte

Term	Description
Master	A device or logical entity that is capable of initiating transactions. A Master is any potential Initiator.
Master Abort	A response to an illegal request. Reads receive all 1s data. Writes have no effect.
MB/s	Megabytes per second (10^6 bytes per second)
Mem	Used as a qualifier for transactions that target memory space. (e.g. A Mem read to I/O)
Memory Issue	Committing a request to DDR or, in the case of a read, returning the read header.
Mesochronous	Distributed or common referenced clock
Metastability	A characteristic of flip flops that describes the state where the output becomes non-deterministic. Most commonly caused by a setup or hold time violation.
MSb	Most Significant Bit
MSB	Most Significant Byte
MTBF	Mean Time Between Failure
NB	Intel® E8501 Chipset North Bridge (NB)
Non-Coherent	Transactions that may cause the processor's view of memory through the cache to be different with that obtained through the I/O subsystem.
Outbound	A transaction where the request destination is I/O and is sourced from the processor-memory complex. The terms Inbound and Outbound refer to transactions as a whole and never to Requests or Completions in isolation. (e.g. An Outbound Read generates Upstream data, whereas an Outbound Write has Downstream data. Even more confusing, the Completion to an Outbound Read travels Upstream.)
PCI-PCI (P-P)	Peer-to-Peer Transactions that occur between two devices independent of memory or the processor.
Packet	The indivisible unit of data transfer and routing, consisting of a header, data, and CRC.
Page Hit	An access to an open page, or DRAM row. The data can be supplied from the sense amps at low latency. The two halves of the cache line are always placed on the same page, so that only one row command is used. Outside of a cache line the XMB maps address bits to optimize random accesses, at the expense of page hits. Thus page hits outside a cache line are rare.
Page Miss (Empty Page)	An access to a page that is not buffered in sense amps and must be fetched from DRAM array. Address Bit Permuted Address bits are distributed among channel selects, DRAM selects, bank selects so that a linear address stream accesses these resources in a certain sequence.
Page Replace Aka Page Miss, Row Hit/Page Miss.	An access to a row that has another page open. The page must be transferred back from the sense amps to the array, and the bank must be precharged.
PCI Bus	Peripheral Component Interconnect Local Bus. A 32-bit or 64-bit bus with multiplexed address and data lines that is primarily intended for use as an interconnect mechanism within a system between processor/memory and peripheral components or add-in cards.
PCI 2.3 compliant	Refers to compliance to the <i>PCI Local Bus Specification, Revision 2.3</i>

Term	Description
Plesiochronous	Each end of a link uses an independent clock reference. Support of this operational mode places restrictions on the absolute frequency difference, as specified by PCI Express, which can be tolerated between the two independent clock references.
Posted	A Transaction that is considered complete by the initiating agent or source before it actually completes at the Target of the Request or destination. All agents or devices handling the Request on behalf of the original Initiator must then treat the Transaction as being system visible from the initiating interface all the way to the final destination. Commonly refers to memory writes.
Push Model	Method of messaging or data transfer that predominately uses writes instead of reads.
Queue	A first-in first-out structure (FIFO).
RASUM	Reliability, Availability, Serviceability, Usability, and Manageability
Receiver	1. The Agent that receives a Packet across an interface regardless of whether it is the ultimate destination of the packet. 2. More narrowly, the circuitry required to convert incoming signals from the physical medium to more perceptible forms.
Request	A packet, phase, or cycle used to initiate a Transaction on a interface, or within a component.
Reserved	The contents or undefined states or information are not defined at this time. Using any reserved area is not permitted. Reserved register bits must have their values preserved.
RMW	Read-Modify-Write operation
SDRAM	Synchronous Dynamic Random Access Memory
SEC	Single-bit Error Correct
Serial Presence Detect (aka I ² C* protocol)	A 2-signal serial bus used to read and write control registers in the SDRAMs.
Simplex	A connection or channel that allows data or messages to be transmitted in one direction only.
SMBus	System Management Bus. Mastered by a system management controller to read and write configuration registers. Signaling and protocol are loosely based on I ² C, limited to 100 KHz.
Snooping	A means of ensuring cache coherency by monitoring all memory accesses on a common multi-drop bus to determine if an access is to information resident within a cache.
Split Lock Sequence	A sequence of transactions that occurs when the target of a lock operation is split across a front side bus data alignment or Cache Line boundary, resulting in two read transactions and two write transactions to accomplish a read-modify-write operation.
Split Transaction	A transaction that consists of distinct Request and Completion phases or packets that allow use of bus, or interconnect, by other transactions while the Target is servicing the Request.
SSTL	Stub-Series Terminated Logic

Term	Description
Symbol	An expanded and encoded representation of a data Byte in an encoded system (e.g. the 10-bit value in a 8-bit/10-bit encoding scheme). This is the value that is transmitted over the physical medium.
Symbol Time	The amount of time required to transmit a symbol.
Target	A device that responds to bus Transactions. (PCI-X*) The agent receiving a request packet is referred to as the Target for that Transaction. [PCI Express].
Tenured Transaction	A transaction that holds the bus, or interconnect, until complete, effectively blocking all other transactions while the Target is servicing the Request.
TID	Transaction Identifier; A multi-bit field used to uniquely identify a transaction. Commonly used to relate a Completion with its originating Request in a Split Transaction system.
Transaction	An overloaded term that represents an operation between two or more agents that can be comprised of multiple phases, cycles, or packets.
Transmitter	1. The Agent that sends a Packet across an interface regardless of whether it was the original generator of the packet. 2. More narrowly, the circuitry required to drive signals onto the physical medium.
Upstream	Describes commands or data flowing toward the processor-memory complex and away from I/O. The terms Upstream and Downstream are never used to describe transactions as a whole. (e.g. Upstream data may be the result of an Inbound Write, or an Outbound Read. The Completion to an Outbound Read travels Upstream.)
XMB	Intel® E8501 Chipset eXternal Memory Bridge (XMB)

1.4 References

This revision of the *Intel® E8501 Chipset North Bridge (NB) Datasheet* is consistent with the following documentations:

- *Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet*
- *PCI Express Specification*
- *PCI Local Bus Specification*
- *Intel® 6700PXH 64-bit PCI Hub and Intel® 6702PXH 64-bit PCI Datasheet*
- *Intel® 82801EB I/O Controller Hub5 (ICH5) and Intel® 82801ER I/O Controller Hub5 R (ICH5R) Datasheet*
- *64-bit Intel® Xeon® Processor MP with 1MB L2 cache Datasheet*
- *64-bit Intel® Xeon® Processor MP with up to 8MB L3 cache Datasheet*
- *Dual-Core Intel® Xeon® Processor 7000 Sequence Datasheet*

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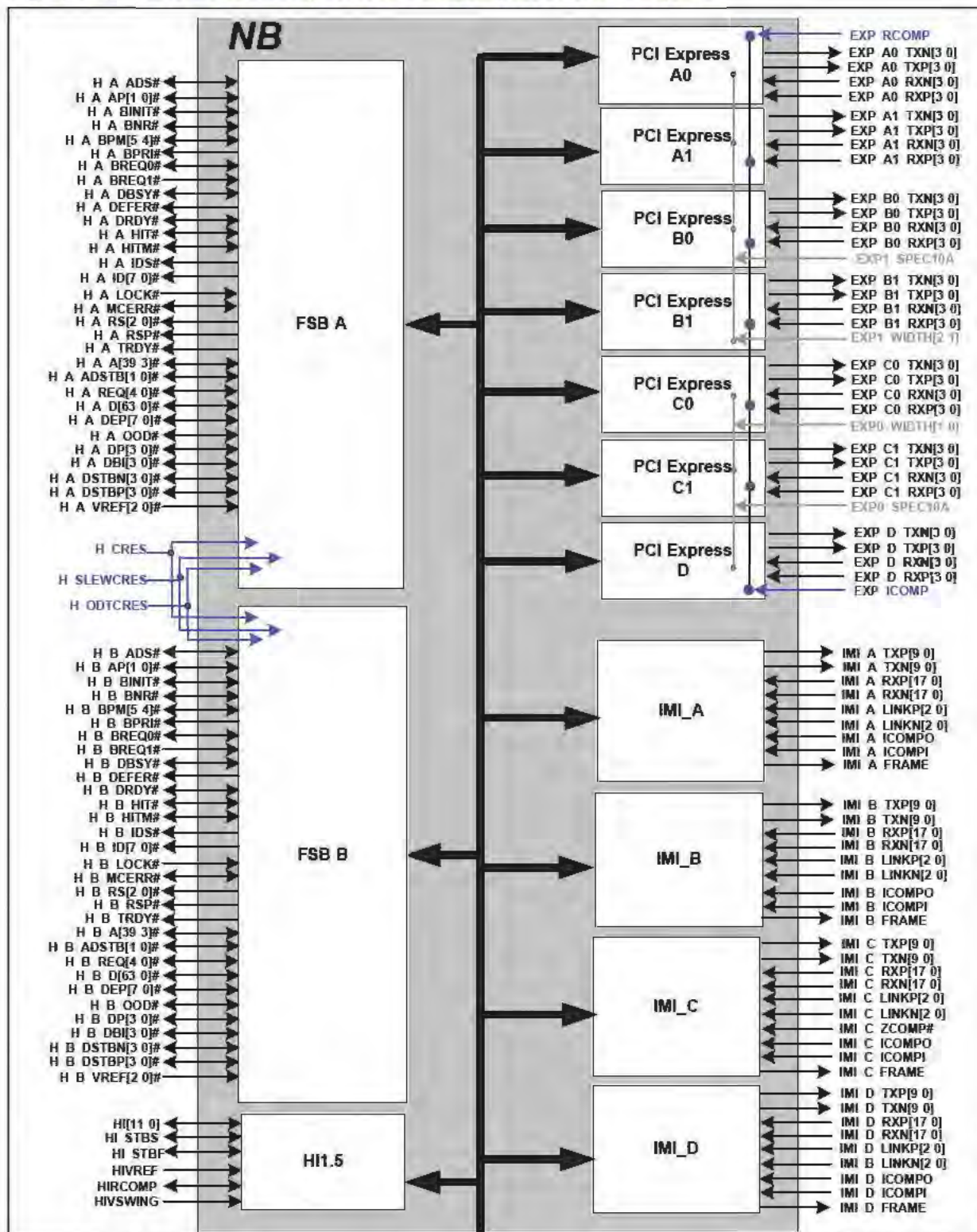
2 Overview

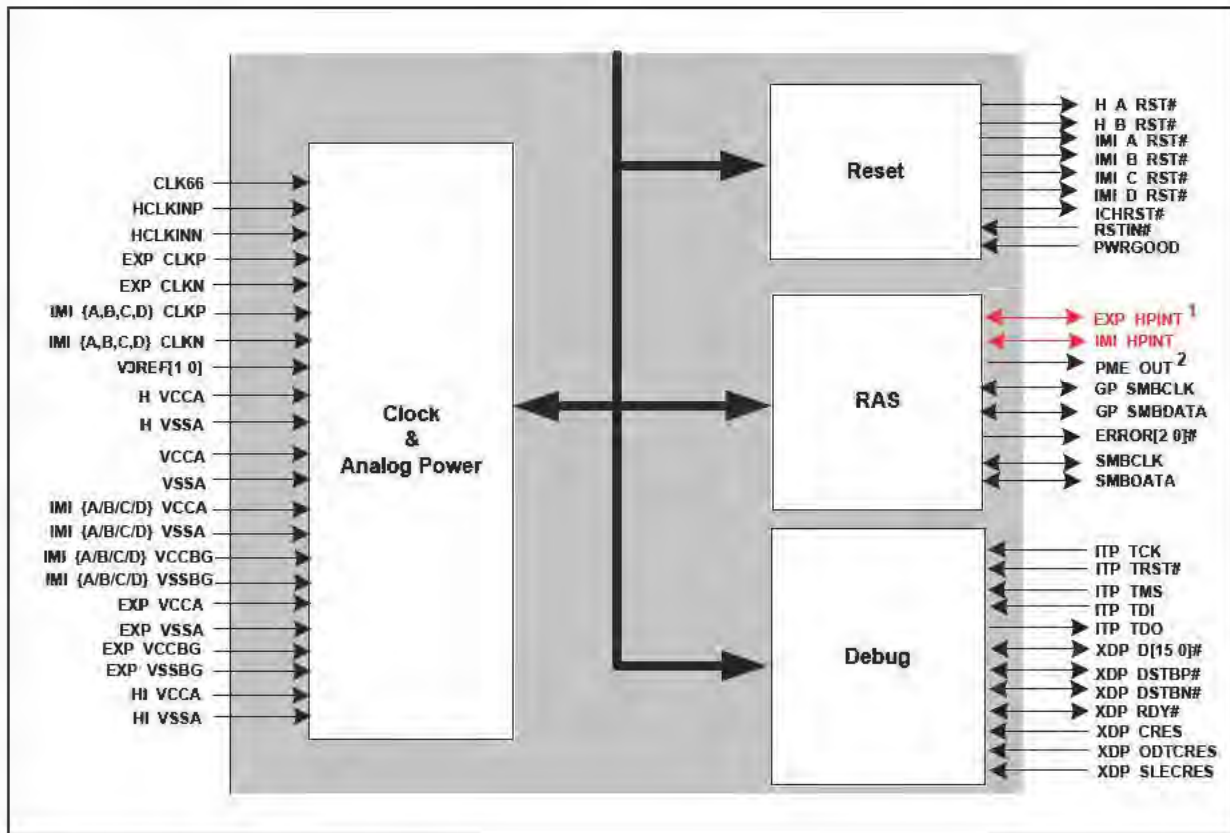
This chapter provides a general overview of the Intel® E8501 chipset North Bridge (NB) and its properties. For functionality details on each interface, please refer to [Section 6](#).

2.1 Logical Pin Grouping

[Figure 2-1](#) provides a complete list of the NB signals. The signals are arranged in functional groups according to their associated logical interfaces: FSB{A,B}, IMI{A/B/C/D}, PCI Express{A0/A1/B0/B1/C0/C1/D}, HII.5, Clock, RAS and Debug. For the complete description of each signal, please refer to [Section 3](#).

Figure 2-1. Intel® E8501 Chipset North Bridge (NB) Interface Signals





NOTES:

1. EXP_HPINT and EXP1_WIDTH1 are muxed names
2. PME_OUT and EXP1_WIDTH2 are muxed names

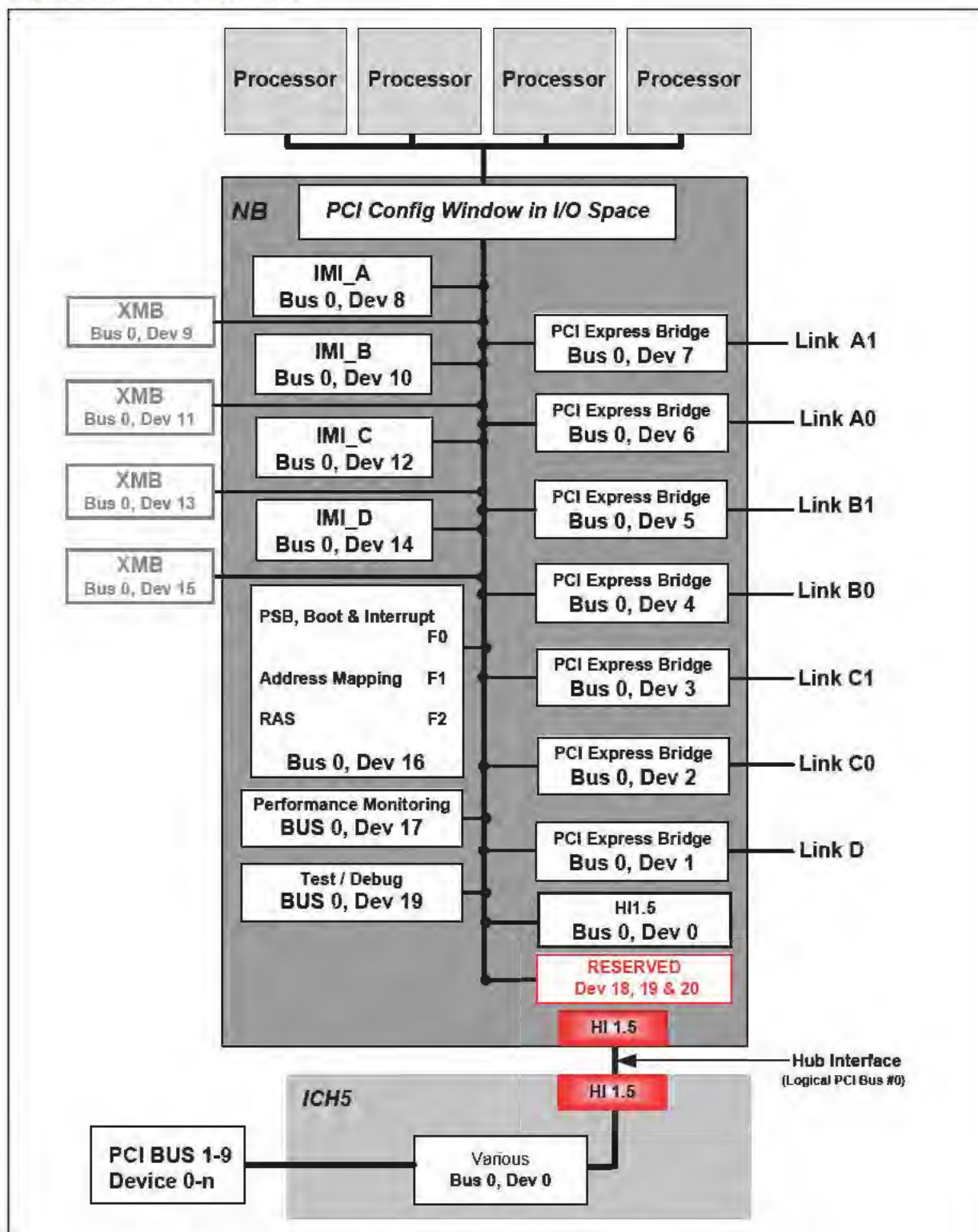
2.2 Quadrant Placement

For the quadrant and ball placement, refer to Figure 7-1.

2.3 Register Devices

Intel® E8501 chipset configuration registers reside in the NB and the XMB. The registers are grouped into buses, devices, and functions. Figure 2-2 shows the hard-coded bus and function numbers for the NB. All configuration devices in this figure are hard-coded to Bus #0. For detailed information on the register configuration, please refer to Section 4. For hard-coded XMB devices, please refer to the *Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet*.

Figure 2-2. PCI Device Map



2.4 Intel® E8501 Chipset North Bridge (NB) Clocking

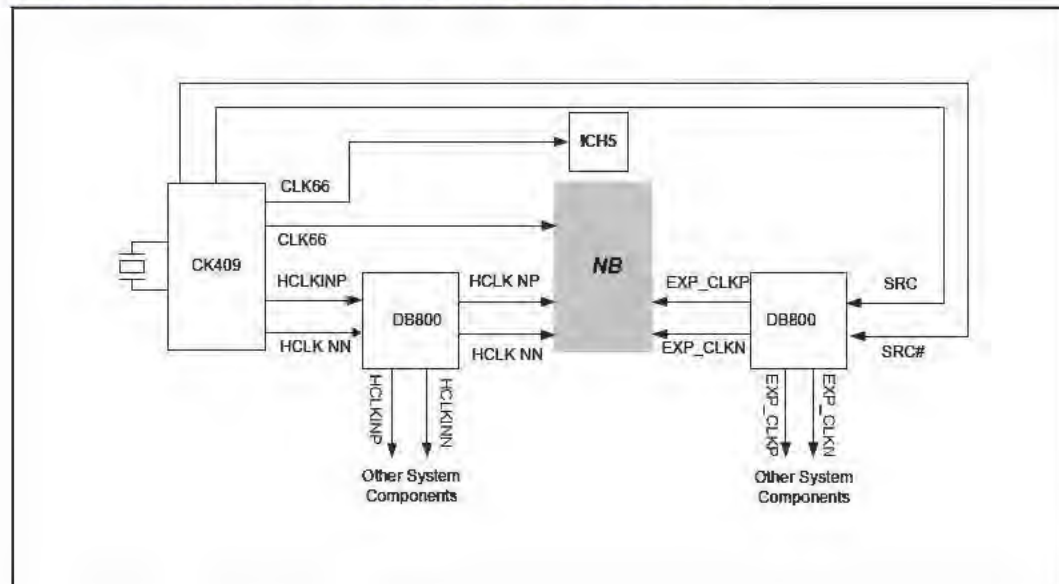
The CK409 is the only clock generator required in a Intel® E8501 chipset platform. Paired with DB800 and DB400 fan-out buffers, this clock solution supplies the reference clocks to all processor and chipset agents. The NB derives the front side bus request and data strobes, XDP debugger data strobes, General Purpose I/O (GPIO) I²C clock, and the SMBus clock from its reference clock.

The reference clock supplying the processors and NB is called “HCLKIN”. The processors and NB populate a low-skew, highly phase-coherent “Common Clock” HCLKIN domain.

Another clock supplied the NB and ICH5 is the Hub Interface Clock, or “CLK66”. The NB and ICH5 populate a low-skew, highly phase-coherent “Common Clock” CLK66 domain. CLK66 can be asynchronous to any other clock on the platform. There is no phase coherence required between HCLKIN and CLK66.

The CK409 also supplies the NB with the PCI Express Clock, or “EXP_CLK”. The PCI Express connections between the NB and PCI Express may be driven from different DB800/DB400 buffers due to their tight part-per-million (ppm) frequency tolerance. Clock skew control between these agents is not required.

Figure 2-3. Intel® E8501 Chipset North Bridge (NB) Reference Clocks



2.5 Interrupt Delivery

The Intel® E8501 chipset supports both the xAPIC and traditional 8259 methods of interrupt delivery. I/O interrupts, and Inter-Processor Interrupts (IPIs) appear as write or interrupt transactions in the system and are delivered to the target processor via the front side bus. This chipset does not support the three-wire sideband bus (the APIC bus). xAPIC interrupts that are generated from I/O devices will need to go through an I/O(x)APIC device unless the device

supports Message Signalled Interrupts (MSI). In this document, I/O(x)APIC is an interrupt controller. This functionality will be embedded into the Intel 6700PXH 64-bit PCI Hub and ICH5 components of the chipset.

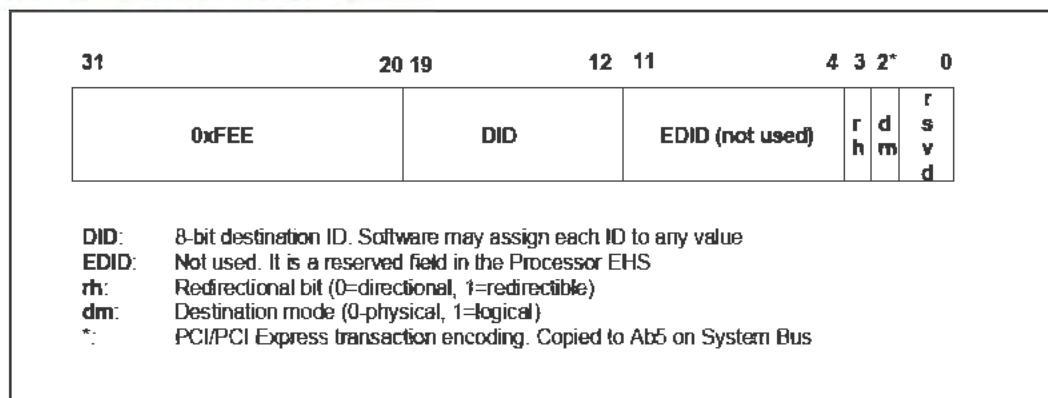
The legacy 8259 functionality is embedded in the ICH5 component. The Intel® E8501 chipset will support inband 8259 interrupt messages from PCI Express devices for boot. The chipset also supports the processor-generated “interrupt acknowledge” (for legacy 8259 interrupts), and “end-of-interrupt” transactions (xAPIC).

2.5.1 xAPIC Interrupt Message Delivery

The xAPIC interrupt architectures deliver interrupts to the target processor core via interrupt messages presented on the front side bus. Interrupts can originate from I/O(x)APIC devices or processors in the system. Interrupts generated by I/O(x)APIC are in the form of writes with a specific address encoding. Interrupts generated by the processor appear on the front side bus as transactions with a similar address encoding, and a specific encoding on the REQa/REQb signals (REQa=01001, REQb=11100).

The xAPIC architecture provides for lowest priority delivery through interrupt redirection by the chipset. If the redirectable “hint bit” is set in the xAPIC message, the chipset may redirect the interrupt to another processor. Note that redirection of interrupts can be to any processor on either Front Side Bus ID and can be applied to both I/O interrupts and IPIs. The redirection can be performed in logical (flat or clustered) and physical destination modes (these modes are explained in section 6.8.2.2). Figure 2-4 shows the address definition in an IA-32 system (xAPIC). For more information on xAPIC refer to Section 6.8.1, “xAPIC Interrupt Message Delivery” on page 333.

Figure 2-4. xAPIC Address Encoding



The data field of an interrupt transaction is included in Table 2-1 for reference.

Table 2-1. XAPIC Data Encoding

D[63:16]	D[15]	D[14]	D[13:11]	D[10:8]	D[7:0]
X	Trigger Mode	Delivery Status	X	delivery Mode	Vector

2.6 Intel® E8501 Chipset North Bridge (NB) RAS Features

The NB provides a rich set of RAS (Reliability, Availability and Serviceability) features at all its logical interfaces to assure high data integrity, system availability and manageability of the system.

2.6.1 Data Integrity (Error Detection)

The NB provides data integrity throughout the component by employing ECC (Error Correcting Codes), CRC (Cyclic Redundancy Checks) and parity on its logical interfaces (Front Side Bus, IMI, PCI Express and HII.5) as well as ECC on its own internal data paths and buffers (Refer to Figure 2-5).

2.6.1.1 Front Side Bus Interface

- Parity protection on the address lines.
- ECC protection on the data bus.

2.6.1.2 Independent Memory Interface (IMI)

- CRC on outbound control packets.
- CRC and x8 SDDC on inbound data packets.
- Re-issue capability on detected packets that contain a packet CRC errors (errors bad packet will be discarded).
- Transaction ID contained in each packet.
- Transaction retry on time-out or uncorrectable errors.
- 3 virtual signals for errors: FATAL, Uncorrectable and Correctable.
- Hot-Pluggable

2.6.1.3 PCI Express Interface

- 8B/10B encoding at the physical layer.
- CRC on all packets for further data protection (The illegal codes can be detected since not all 8B/10B encoding is used).
- Additional link level mechanisms:

PCI Express Training

Synchronizes the two end of the interface without software intervention to ensure a robust connection.

PCI Express Retry

If packets contain errors, the packet will be discarded and the sending end of the interface gets signaled. The sending hardware will re-transmit the particular packet in question and all following packets. Although this will cause a temporary interruption in the delivery of packets, it does so in order to maintain the link integrity.

PCI Express Recovery

When enough errors occur, the PCI Express link may enter into a quick training sequence,

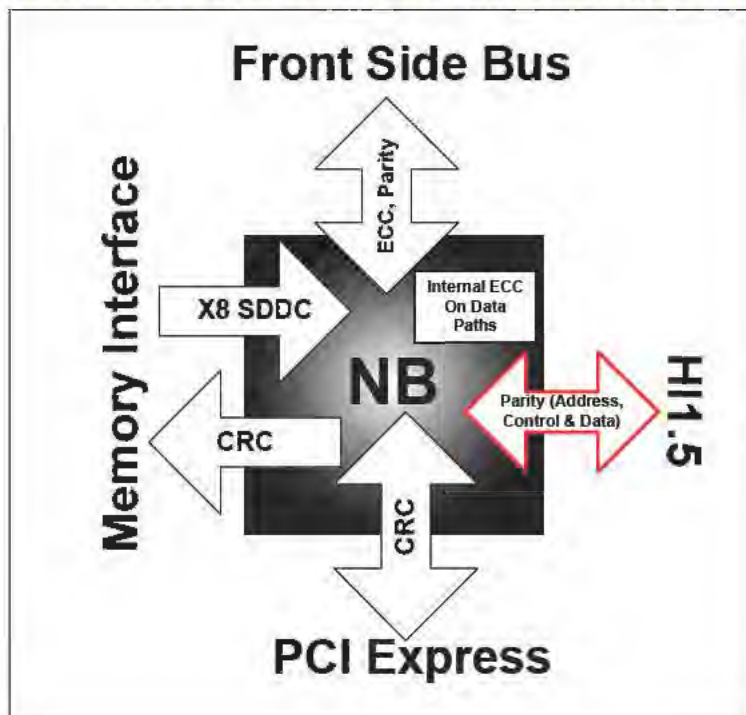
referred to as recovery sequence. At this time, the connections will not be renegotiated, but the adjustment of skew between lanes of the link may occur.

2.6.1.4 Legacy Hub Interface (HI1.5)

- Even parity protection scheme over the data signals.

Figure 2-5 summarizes the error detection method at each logical interface of the NB.

Figure 2-5. Intel® E8501 Chipset North Bridge (NB) Data Integrity Map



2.6.2 Error Reporting

The NB is the collection point for a variety of errors that are either detected internally or signaled from the external interfaces (Front Side Bus, PCI Express and IMI). All detected errors are logged in the two provided registers, FERRST (first error status register), and NERRST (next error status register). First fatal and/or first non-fatal errors are flagged in the FERRST register and subsequent errors are indicated in the NERRST. There are some errors that trigger multiple errors within a component. In that case, these errors will be logged in both FERRST and NERRST. There are control and data logs associated with some of the errors flagged in the FERRST. In some cases, the logs are duplicated for the same error (for example, the four PCI Express interfaces on the NB will have identical error log registers). When error logs are duplicated, a pointer to the interface that reported the first error is provided.

The contents of FERRST and NERRST are “sticky” across a reset (while PWRGOOD remains asserted). This provides the ability for firmware to perform diagnostics across reboots. For more information on the error registers refer to Section 4.

2.6.3 Memory Mirroring

The Memory Mirroring enables redundancy by always keeping an exact duplicate of memory accessible. The Memory Mirroring logic is located in the NB and is a user selectable feature. At configuration time, the user can enable mirroring and select which IMI Ports are mirrored. The IMI port mirroring options are as follows:

- IMI Port A and B are mirrored, IMI Port C and D are mirrored.
- IMI Port A and C are mirrored, IMI Port B and D are mirrored.

Mirroring control registers include REDUN ([Section 4.19.9](#)), IMIST ([Section 4.13.9](#)) and IMIHPC ([Section 4.13.10](#)) registers.

For a detailed description of mirroring, including the Hot-Plug and re-silvering in mirroring mode, refer to [Section 6.3](#).

2.6.4 Memory RAID

The Memory RAID enables the data to be reconstructed upon failure behind the IMI ports. The Memory RAID logic is located in the NB and is a user selectable feature. At configuration time, the user can enable memory RAID.

Note: The NB cannot be configured to be in Memory Mirroring Mode and RAID mode at the same time, as these features are mutually exclusive. Also, in order to enable the Memory RAID, the platform must be configured with four XMBs with matching memory configurations.

Raid control registers include REDUN ([Section 4.19.9](#)), IMIST ([Section 4.13.9](#)) and IMIHPC registers ([Section 4.13.10](#)).

For a detailed description of RAID, including the Hot-Plug and re-silvering in RAID mode, refer to [Section 6.3](#).

2.6.5 Hot-Plug

PCI Express – All the PCI Express ports are Hot-Pluggable. For more information refer to [Section 6.4.8, “Hot-Plug” on page 314](#).

IMI – The NB provides the ability to add or remove each XMB and the memory behind it to or from any IMI port interface from a running OS instance. The details of the support will be provided in the future revision of this document. For more information refer to [Section 6.3.8, “IMI Hot-Plug” on page 287](#).

Note: In addition to the above Hot-Plug support on the NB, the Intel® E8501 chipset offers Hot-Plug support at the Intel® 6700PXH 64-bit PCI Hub (PCI-X*) interface as well. For detail on application and implication of this component, please refer to *Intel® 6700PXH 64-bit PCI Hub and Intel® 6702PXH 64-bit PCI Hub Datasheet*.

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3 Signal Description

This section provides a detailed description of the Intel® E8501 chipset north bridge (NB) signals. The signals are arranged in functional groups according to their associated interface. The summary of all signals are also captured on Figure 2-1 “Intel® E8501 Chipset North Bridge (NB) Interface Signals” on page 28.

3.1 Conventions

The terms *assertion* and *de-assertion* are used extensively when describing signals, to avoid confusion when working with a mix of active-high and active-low signals. The term *assert*, or *assertion*, indicates that the signal is active, independent of whether the active level is represented by a high or low voltage. The term *de-assert*, or *de-assertion*, indicates that the signal is inactive.

Signal names may or may not have a “#” appended to them. The “#” symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “#” is not present after the signal name the signal is asserted when at the high voltage level.

Differential signal pairs adopt a “{P/N}” suffix to indicate the “positive” (P) or “negative” (N) signal in the pair. If a “#” is appended, it will be appended to both.

When discussing data values used inside the component, the logical value is used (i.e. a data value described as “1101b” would appear as “1101b” on an active-high bus, and as “0010b” on an active-low bus). When discussing the assertion of a value on the actual signal, the physical value is used (i.e. asserting an active-low signal produces a “0” value on the signal).

Some signals or groups of signals have multiple versions. These signal groups may represent distinct but similar ports or interfaces, or may represent identical copies of the signal used to reduce loading effects. Table 3-1 shows the conventions used in this document.

Curly-bracketed, non-trailing numerical indices (e.g. “{X/Y}”) represent replications of major buses. Square-bracketed numerical indices (e.g. “[n m]”) represent functionally similar but logically distinct bus signals; each signal provides an independent control, and may or may not be asserted at the same time as the other signals in the grouping). In contrast, trailing curly-bracketed numerical indices, e.g., “{x/y}” typically represent identical duplicates of a signal that are provided for electrical reasons.

Table 3-1. Signal Naming Conventions

Convention	Expands to
RR{A/B/C}XX	Expands to: RRAXX, RRBXX, and RRCXX. This denotes similar signals on replicated buses.
RR[2:0]	Expands to: RR[2], RR[1], and RR[0]. This denotes a bus.
RR{A/B/C}	Expands to: RRA, RRB, and RRC. This denotes electrical duplicates.
RR# or RR[2:0]#	Denotes an active low signal or bus.

Table 3-2 lists the reference terminology used for signal types.

Table 3-2. Buffer Signal Directions

Buffer Direction	Description
I	Input Signal
O	Output Signal
A	Analog
I/O	Bidirectional (Input/Output) Signal

3.2 FSB Signals

Table 3-3. Intel® E8501 Chipset North Bridge (NB) Signals (FSB) (Sheet 1 of 3)

Signal	Type	Description
H_{A/B}_A[39:3]#	I/O	Address Signals: Processor Address Bus. During processor cycles these are inputs. The NB drives A[39:3]# for transactions originating from PCI Express, other FSB, and for deferred reply transactions.
H_{A/B}_ADS#	I/O	Address/Data Strobe: Indicates the first cycle of any request phase. This signal is driven and sampled by the NB.
H_{A/B}_ADSTB[1:0]#	I/O	Address Strobes: Used to transfer requests at the x2 rate. The falling edge of the strobe transfers the 1st subphase. The rising edge of the strobe transfers the 2nd subphase.
H_{A/B}_AP[1:0]#	I/O	Address Parity: Parity protection on the address and request bus. The NB will generate AP[1:0]# for its own transactions. The NB will also monitor AP[1:0]# for all transactions and check parity on the address bus.
H_{A/B}_BINIT#	I/O	Bus Initialization: Processor assertions are logged as "F2" errors. The NB does not assert this signal.
H_{A/B}_BNR#	I/O	Block Next Request: The NB monitors processor assertions of this signal to block any of the NB's transactions from being issued on the bus.
H_{A/B}_BPM[5:4]#	I/O	Breakpoint / Debug Bus: This group of signals is used by the system debug logic and by the NB for communicating debug information. BPM[5:4] are used as breakpoint triggers.
H_{A/B}_BPRI#	O	Priority Agent Bus Request: The NB asserts this signal to drive requests originating from the PCI Express and HI ports, snoops from the other FSB, and to issue a deferred reply transaction in some special cases. The NB will also assert this signal to block the processors from issuing transactions. Symmetric agents do not assert this signal. The NB does not observe this signal.
H_{A/B}_BREQ[0]#	I/O	Physical Bus Request: The NB drives BREQ[0]# during POC and de-asserts it one clock after the NB samples reset de-asserted.
H_{A/B}_BREQ[1]#	I	Physical Bus Request: The NB does not drive BREQ[1]#, but rather observes active BREQ[1:0] from processors to determine de-assertion of BPRI# to transfer bus ownership to the processor.

Table 3-3. Intel® E8501 Chipset North Bridge (NB) Signals (FSB) (Sheet 2 of 3)

Signal	Type	Description
H_{A/B}_D[63:0]#	I/O	Data Bus: 64 bits of data driven by the agent responsible for driving data during the Data phase.
H_{A/B}_DBI[3:0]#	I/O	Data Bus Inversion: Each bit corresponds to one of the FSB data signal group and 8 bits of ECC.
H_{A/B}_DBSY#	I/O	Data Bus Busy: Indicates that the data bus is owned by the agent responsible for driving the data during the Data phase. DBSY# assertion does not imply that data is being transferred during that cycle.
H_{A/B}_DEFER#	O	Defer: The NB asserts DEFER# for all processor-initiated transactions with DEN# asserted. The NB will also generate deferred responses for these transactions except for the case when an in-order retry is forced.
H_{A/B}_DEP[7:0]#	I/O	Data Bus Extended Parity: ECC coverage for 64 bits of data (D). The NB generates this ECC when it drives data during the Data phase. The NB also checks the ECC accompanying incoming data.
H_{A/B}_DP[3:0]#	I/O	Data Bus Parity
H_{A/B}_DRDY#	I/O	Data Ready: Indicates that data is valid on the data bus during any cycle DRDY# is asserted. The NB asserts DRDY# for each valid data transfer.
H_{A/B}_HIT#	I/O	Snoop Hit: The NB captures the value of HIT# for transactions that are deferred and returns it using DHIT# during the Deferred Phase. The NB asserts HIT# to initiate a snoop stall (HIT# and HITM# asserted together).
H_{A/B}_HITM#	I/O	Snoop Hit with Modified: The NB observes HITM# and when asserted drives TRDY# for implicit writeback. The NB asserts HITM# to initiate a snoop stall (HIT# and HITM# asserted together).
H_{A/B}_ID[7:0]#	O	Transaction Identifier: These are driven during the Deferred Phase and indicate the transaction ID of the deferred transaction. On the second clock of the deferred phase (IDS# + 1), IDb[1:0]# carries the parity for the ID signals. IDb[2]# renamed as DHIT# is asserted by NB if the snoop phase of the original transaction resulted in HIT#.
H_{A/B}_IDS#	O	Transaction Identifier Strobe: IDS# is asserted by the NB to indicate the first cycle of the deferred phase.
H_{A/B}_LOCK#	I	Bus Lock: Indicates atomicity of transactions.
H_{A/B}_MCERR#	I/O	Machine Check Error: MCERR# indicates non-recoverable bus protocol violation.
H_{A/B}_REQ[4:0]#	I/O	Request Command: The NB issues requests by driving REQ[4:0]# while asserting ADS#. The NB tracks processor requests on REQ[4:0]# upon observing assertions on ADS#.
H_{A/B}_OOD#	O	Out Of Order Data: OOD# delivers the data for the deferred phase.
H_{A/B}_RS[2:0]#	O	Response Status: Indicates the type of response generated by the NB. Valid responses are Hard Fail, Implicit Writeback, Normal Data, No Data, Deferred, and Retry.
H_{A/B}_RSP#	O	Response Status Parity: Parity protection on RS[2:0]#.

Table 3-3. Intel® E8501 Chipset North Bridge (NB) Signals (FSB) (Sheet 3 of 3)

Signal	Type	Description
H_{A/B}_DSTBN[3:0]#	I/O	Negative Data Strobes: Used to transfer data at the x4 rate. DSTBN[3:0]# is the negative phase data strobe. Data transfer for subphases 2 and 4 occur on the falling edges of STBN#. The NB drives and samples DSTBN[3:0]#.
H_{A/B}_DSTBP[3:0]#	I/O	Positive Data Strobes: Used to transfer data at the x4 rate. DSTBP[3:0]# is the positive phase data strobe. Data transfer for subphases 1 and 3 occur on the falling edges of STBP#. The NB drives and samples DSTBP[3:0]#.
H_{A/B}_TRDY#	O	Target Ready: The NB asserts TRDY# when it is ready to accept data from the processor.
H_{A/B}_VREF[2:0]	A	FSB AGTL+ Receiver Voltage References (0.733 V)
H_CRES	A	FSB Compensation Resistor Common: Common (ground) pin for connection to the H_ODTCRES and H_SLWCRES compensation resistors.
H_ODTCRES	A	FSB On-Die Termination Compensation Resistors: Compensation resistor that determines the FSB on-die termination.
H_SLWCRES	A	FSB Slew Rate Compensation Resistor: Compensation resistor that determines the FSB driver slew rate.

3.3 Independent Memory Interface (IMI) Signals

Table 3-4. Intel® E8501 Chipset North Bridge (NB) Signals (IMI)

IMI_{A/B/C/D}_TXP[9:0]	O	Memory Port Outbound: Signals used for command and write operations.
IMI_{A/B/C/D}_TXN[9:0]	O	Memory Port Outbound Complement: The complement of the signals used for command and write operations.
IMI_{A/B/C/D}_RXP[17:0]	I	Memory Port Inbound Data: Signals used for returning data from read operations.
IMI_{A/B/C/D}_RXN[17:0]	I	Memory Port Inbound Data Complement: The complement of the signals used for returning data from read operations.
IMI_{A/B/C/D}_LINKP[2:0]	I	Memory Port Inbound Link: Link signals used for command completions.
IMI_{A/B/C/D}_LINKN[2:0]	I	Memory Port Inbound Link Complement: The complement of the link signals used for command completions.
IMI_{A/B/C/D}_ICOMP1	A	Memory Port Impedance Compensation
IMI_{A/B/C/D}_ICOMP0	A	Memory Port Impedance Compensation
IMI_{A/B/C/D}_FRAME	O	IMI Frame

3.4 PCI Express Ports Signals

Table 3-5. Intel® E8501 Chipset North Bridge (NB) Signals (PCI Express) (Sheet 1 of 2)

Signal Name	Type	Description						
EXP_{A0/A1/B0/B1/C0/C1/D}_TXP[3:0]	O	PCI Express Transmit Data (Outbound)						
EXP_{A0/A1/B0/B1/C0/C1/D}_TXN[3:0]	O	PCI Express Outbound Complement						
EXP_{A0/A1/B0/B1/C0/C1/D}_RXP[3:0]	I	PCI Express Receive Data (Inbound)						
EXP_{A0/A1/B0/B1/C0/C1/D}_RXN[3:0]	I	PCI Express Inbound Complement						
EXP_ICOMP	A	PCI Express Impedance Compensation						
EXP_RCOMP	A	PCI Express Impedance Compensation						
EXP0_SPEC10A	I	PCI Express Training State Machine Mode for EXP_{D/C0/C1}: This signal is sampled at the assertion of PWRGOOD. <table><tr><th>Value</th><th>Function</th></tr><tr><td>0</td><td>Use 1.0 Specification</td></tr><tr><td>1</td><td>use 1.0 A Specification</td></tr></table>	Value	Function	0	Use 1.0 Specification	1	use 1.0 A Specification
Value	Function							
0	Use 1.0 Specification							
1	use 1.0 A Specification							
EXP1_SPEC10A	I	PCI Express Training State Machine Mode for EXP_{B0/B1/A0/A1}: This signal is sampled at the assertion of PWRGOOD. <table><tr><th>Value</th><th>Function</th></tr><tr><td>0</td><td>Use 1.0 Specification</td></tr><tr><td>1</td><td>use 1.0 A Specification</td></tr></table>	Value	Function	0	Use 1.0 Specification	1	use 1.0 A Specification
Value	Function							
0	Use 1.0 Specification							
1	use 1.0 A Specification							
EXP0_WIDTH[1:0]	I	PCI Express Link Width Force for EXP_{D/C0/C1}: These signals are sampled at the assertion of PWRGOOD.						
EXP1_WIDTH0	I	PCI Express Link Width Force for EXP_{B0/B1/A0/A1}: This signal is sampled at the assertion of PWRGOOD.						
EXP1_WIDTH1 / EXP_HPINT	I/O	PCI Express Link Width Force for EXP_{B0/B1/A0/A1}: This signal is sampled at the assertion of PWRGOOD. PCI Express Hot-Plug Interrupt: The NB asserts this signal to signal a PCI Express hot-plug event.						

Table 3-5. Intel® E8501 Chipset North Bridge (NB) Signals (PCI Express) (Sheet 2 of 2)

Signal Name	Type	Description
EXP1_WIDTH2 / PME_OUT	I/O	PCI Express Link Width Force for EXP_{B0/B1/A0/A1}: This signal is sampled at the assertion of PWRGOOD. Power Management Event Output: Each PCI (and PCI Express) slot supports a signal called Power Management Event (PME). This signal is used by an I/O device (e.g. a LAN adapter) to wake up a system that is in a sleep state. Traditionally, these pins are routed directly to the ICH. However, with PCI Express, these messages will arrive inband through an ON/OFF pair of messages. To manage this transition (since ICH5 is not on PCI Express), the NB implements the PME Status bit in Section 4.11.49, "EXP_RTSTS[7:1]: PCI Express Root Status Register (D1-7, F0)" on page 4-129 for each of the PCI Express ports. There is one bit per port. The NB OR's all the bits together and asserts the PME_OUT signal to the ICH5. When all the bits are clear, the signal is de-asserted.

3.4.1 Industry Standard Naming Convention

The PCI Express signal naming convention used by the NB is different from the standard naming convention specified by PCISIG because the NB naming occurred before the PCISIG convention was ratified.

Table 3-6 correlates the NB signal names to the ratified PCISIG naming convention. Consult this table for help in attaching PCI Express devices to the NB using the standard PCISIG naming convention.

**Table 3-6. Intel® E8501 Chipset North Bridge (NB) Signals (PCI Express)
Correlated to Industry-Standard Naming Convention (Sheet 1 of 2)**

Existing Signal Names	PCISIG Naming Equivalent	Existing Signal Names	PCISIG Naming Equivalent
EXP_A0_RXN0	PE6Rn0	EXP_B0_RXN3	PE4Rn3
EXP_A0_RXN1	PE6Rn1	EXP_B0_RXP0	PE4Rp0
EXP_A0_RXN2	PE6Rn2	EXP_B0_RXP1	PE4Rp1
EXP_A0_RXN3	PE6Rn3	EXP_B0_RXP2	PE4Rp2
EXP_A0_RXP0	PE6Rp0	EXP_B0_RXP3	PE4Rp3
EXP_A0_RXP1	PE6Rp1	EXP_B0_TXN0	PE4Tn0
EXP_A0_RXP2	PE6Rp2	EXP_B0_TXN1	PE4Tn1
EXP_A0_RXP3	PE6Rp3	EXP_B0_TXN2	PE4Tn2
EXP_A0_TXN0	PE6Tn0	EXP_B0_TXN3	PE4Tn3
EXP_A0_TXN1	PE6Tn1	EXP_B0_TXP0	PE4Tp0
EXP_A0_TXN2	PE6Tn2	EXP_B0_TXP1	PE4Tp1
EXP_A0_TXN3	PE6Tn3	EXP_B0_TXP2	PE4Tp2
EXP_A0_TXP0	PE6Tp0	EXP_B0_TXP3	PE4Tp3
EXP_A0_TXP1	PE6Tp1	EXP_B1_RXN0	PE5Rn0
EXP_A0_TXP2	PE6Tp2	EXP_B1_RXN1	PE5Rn1
EXP_A0_TXP3	PE6Tp3	EXP_B1_RXN2	PE5Rn2
EXP_A1_RXN0	PE7Rn0	EXP_B1_RXN3	PE5Rn3
EXP_A1_RXN1	PE7Rn1	EXP_B1_RXP0	PE5Rp0
EXP_A1_RXN2	PE7Rn2	EXP_B1_RXP1	PE5Rp1
EXP_A1_RXN3	PE7Rn3	EXP_B1_RXP2	PE5Rp2
EXP_A1_RXP0	PE7Rp0	EXP_B1_RXP3	PE5Rp3
EXP_A1_RXP1	PE7Rp1	EXP_B1_TXN0	PE5Tn0
EXP_A1_RXP2	PE7Rp2	EXP_B1_TXN1	PE5Tn1
EXP_A1_RXP3	PE7Rp3	EXP_B1_TXN2	PE5Tn2
EXP_A1_TXN0	PE7Tn0	EXP_B1_TXN3	PE5Tn3
EXP_A1_TXN1	PE7Tn1	EXP_B1_TXP0	PE5Tp0
EXP_A1_TXN2	PE7Tn2	EXP_B1_TXP1	PE5Tp1
EXP_A1_TXN3	PE7Tn3	EXP_B1_TXP2	PE5Tp2
EXP_A1_TXP0	PE7Tp0	EXP_B1_TXP3	PE5Tp3
EXP_A1_TXP1	PE7Tp1	EXP_C0_RXN0	PE2Rn0
EXP_A1_TXP2	PE7Tp2	EXP_C0_RXN1	PE2Rn1
EXP_A1_TXP3	PE7Tp3	EXP_C0_RXN2	PE2Rn2
EXP_B0_RXN0	PE4Rn0	EXP_C0_RXN3	PE2Rn3

**Table 3-6. Intel® E8501 Chipset North Bridge (NB) Signals (PCI Express)
Correlated to Industry-Standard Naming Convention (Sheet 2 of 2)**

Existing Signal Names	PCISIG Naming Equivalent	Existing Signal Names	PCISIG Naming Equivalent
EXP_B0_RXN1	PE4Rn1	EXP_C0_RXP0	PE2Rp0
EXP_B0_RXN2	PE4Rn2	EXP_C0_RXP1	PE2Rp1
EXP_C0_RXP2	PE2Rp2	EXP_D_RXN2	PE1Rn2
EXP_C0_RXP3	PE2Rp3	EXP_D_RXN3	PE1Rn3
EXP_C0_TXN0	PE2Tn0	EXP_D_RXP0	PE1Rp0
EXP_C0_TXN1	PE2Tn1	EXP_D_RXP1	PE1Rp1
EXP_C0_TXN2	PE2Tn2	EXP_D_RXP2	PE1Rp2
EXP_C0_TXN3	PE2Tn3	EXP_D_RXP3	PE1Rp3
EXP_C0_TXP0	PE2Tp0	EXP_D_TXN0	PE1Tn0
EXP_C0_TXP1	PE2Tp1	EXP_D_TXN1	PE1Tn1
EXP_C0_TXP2	PE2Tp2	EXP_D_TXN2	PE1Tn2
EXP_C0_TXP3	PE2Tp3	EXP_D_TXN3	PE1Tn3
EXP_C1_RXN0	PE3Rn0	EXP_D_TXP0	PE1Tp0
EXP_C1_RXN1	PE3Rn1	EXP_D_TXP1	PE1Tp1
EXP_C1_RXN2	PE3Rn2	EXP_D_TXP2	PE1Tp2
EXP_C1_RXN3	PE3Rn3	EXP_D_TXP3	PE1Tp3
EXP_C1_RXP0	PE3Rp0	EXP_CLKN	PECLKN
EXP_C1_RXP1	PE3Rp1	EXP_CLKP	PECLKP
EXP_C1_RXP2	PE3Rp2	EXP_HPINT/EXP1_WIDTH1	PE1WIDTH[1]
EXP_C1_RXP3	PE3Rp3	EXP_ICOMPI	PEICOMPI
EXP_C1_TXN0	PE3Tn0	EXP_RCOMP	PERCOMP
EXP_C1_TXN1	PE3Tn1	EXP_VCCA	VCCAPE
EXP_C1_TXN2	PE3Tn2	EXP_VCCBG	VCCABGPE
EXP_C1_TXN3	PE3Tn3	EXP_VSSA	VSSAPE
EXP_C1_TXP0	PE3Tp0	EXP_VSSBG	VSSBGPE
EXP_C1_TXP1	PE3Tp1	EXP0_Spec10A	PE0Spec10a
EXP_C1_TXP2	PE3Tp2	EXP0_WIDTH0	PE0WIDTH[0]
EXP_C1_TXP3	PE3Tp3	EXP0_WIDTH1	PE0WIDTH[1]
EXP_D_RXN0	PE1Rn0	EXP1_Spec10A	PE1Spec10a
EXP_D_RXN1	PE1Rn1	EXP1_WIDTH0	PE1WIDTH[0]

3.5 Hub Interface 1.5 (HI1.5) Signals

Table 3-7. Intel® E8501 Chipset North Bridge (NB) Signals (Hub Interface)

Signal Name	Type	Description
HI[11:0]	I/O	Data pins: The data interface.
HI_STBF	I/O	First Packet Data Interface Strobe: (idle & default voltage level = H_VCCA) together provide timing for 4X and 1X data transfer on the data interface. The agent that is providing data drives this signal. HI_STBF and HI_STBS should be sensed pseudo-differentially at the receiver.
HI_STBS	I/O	Second Packet Data Interface Strobe: See HI_STBF description above.
HIRCOMP	A	HI RCompensation: Connects to the external RCOMP resistor and used for impedance matching.
HIVREF	A	HI Voltage Reference: Receiver threshold (0.35 V reference voltage).
HIVSWING	A	HI Voltage Swing: A voltage reference (0.8 v to 0.7 v) used by the RCOMP circuits to adjust the I/O drivers' strength and maximum signal voltage to be driven onto the board.

3.6 Clocking and Analog Power Signals

Table 3-8. Intel® E8501 Chipset North Bridge (NB) Signals (Clocking and Analog Power) (Sheet 1 of 2)

Signal Name	Type	Description
CLK66	I	Clock 66: 66 MHz clock for HI1.5. Synchronization to EXP_CLK or HCLKIN not required. Bypass clock in bypass mode.
EXP_CLKN	I	PCI EXPRESS Clock Complement: This is the other differential reference clock input to the PCI Express Phase Locked Loops. Synchronization to H_CLK or CLK66 not required.
EXP_CLKP	I	PCI EXPRESS Clock: This is one of the two differential reference clock inputs to the PCI Express Phase Locked Loops. Synchronization to H_CLK or CLK66 not required.
EXP_VCCA	A	VCC: Analog Voltage for the PCI Express PLL's.
EXP_VCCBG	A	VCC: Bandgap Voltage for the PCI Express.
EXP_VSSA	A	VSS: Analog Voltage for the PCI Express PLL's.
EXP_VSSBG	A	VSS: Bandgap Voltage for the PCI Express.
H_VCCA	A	VCC: Analog Voltage for the FSB PLL.
H_VSSA	A	VSS: Analog Voltage for the FSB PLL.

**Table 3-8. Intel® E8501 Chipset North Bridge (NB) Signals
(Clocking and Analog Power) (Sheet 2 of 2)**

Signal Name	Type	Description
HCLKINN	I	FSB Clock Complement: This is the other differential reference clock input to the Phase Locked Loop in the NB core. Phase Locked Loops in the NB will shift this to all frequencies required by the core, FSB, and SMBus ports.
HCLKINP	I	FSB Clock: This is one of the two differential reference clock inputs to the Phase Locked Loop in the NB core. Phase Locked Loops in the NB will shift this to all frequencies required by the core, FSB, and SMBus ports.
HI_VCCA	A	VCC: Analog Voltage for the Hub Interface PLL.
HI_VSSA	A	VSS: Analog Voltage for the Hub Interface PLL.
IMI_{A/B/C/D}_CLKN	I	Independent Memory Interface Clock Complement: This is the other differential reference clock input to the Phase Locked Loop in the NB IMI.
IMI_{A/B/C/D}_CLKP	I	Independent Memory Interface Clock: This is one of the two differential reference clock inputs to the Phase Locked Loop in the NB IMI.
IMI_{A/B/C/D}_VCCA	A	VCC: Analog Voltage for the Independent Memory Interface PLL's. One for each IMI.
IMI_{A/B/C/D}_VCCBG	A	VCC: Bandgap Voltage for the Independent Memory Interfaces. One for each IMI.
IMI_{A/B/C/D}_VSSA	A	VSS: Analog Voltage for the Independent Memory Interface PLL's. One for each IMI.
IMI_{A/B/C/D}_VSSBG	A	VSS: Bandgap Voltage for the Independent Memory Interfaces. One for each IMI.
VCCA	A	VCC: Analog Voltage for the core PLL.
VSSA	A	VSS: Analog Voltage for the core PLL.
V3REF[1:0]	A	Voltage Reference: Reference Voltage for 3.3 V signal tolerance.

3.7 Reset Signals

Table 3-9. Intel® E8501 Chipset North Bridge (NB) Signals (Reset)

Signal Name	Type	Description
H_{A/B}_RST#	O	Host Reset: This signal is the FSB reset. Asserted due to RSTIN# or writes to the SYRE register. Reset on an unpopulated FSB will remain asserted.
ICHRST#	O	ICH5 Reset: 66 MHz synchronized version of the reset input signal to the ICH5.
IMI_{A/B/C/D}_RST#	O	IMI Port Reset: Assertion resets the XMB.
PWRGOOD	I	Power Good: Clears the NB. This signal is held low until all power supplies are in specification. This signal may be pulsed after power-up to completely reset the NB.
RSTIN#	I	Reset Input: This is the hard reset input to the NB.

3.8 Debug Signals

Table 3-10. Intel® E8501 Chipset North Bridge (NB) Signals (Test and Debug) (Sheet 1 of 2)

Signal Name	Type	Description
ITP_TCK	I	Test Clock: Clock input used to drive Test Access Port (TAP) state machine during test and debugging. This input may change asynchronous to HCLK.
ITP_TDI	I	Test Data In: Data input for test mode. Used to serially shift data and instructions into TAP.
ITP_TDO	O	Test Data Out: Data output for test mode. Used to serially shift data out of the device.
ITP_TEST	I	Test Mode: An assertion of this signal places the component into test mode. A leading-edge transition on this signal will also sample static test mode functions from the "overloaded" signals.
ITP_TMS	I	Test Mode Select: This signal is used to control the state of the TAP controller.
ITP_TRST#	I	Test Reset: This signal resets the TAP controller logic. It should be pulled down unless ITP_TCK is active. This input may change asynchronous to BUSCLK.
XDP_CRES	I	Debug Bus Compensation Resistor Common: Common (ground) pin for connection to the XDP_ODTCRES and XDP_SLWCRES compensation resistors.
XDP_D[15:0]#	I/O	Debug Bus Data: XDP debug control/data signals and manufacturing test mode. Includes clock/PLL debug signals.

Table 3-10. Intel® E8501 Chipset North Bridge (NB) Signals (Test and Debug) (Sheet 2 of 2)

Signal Name	Type	Description
XDP_DSTBN#	I/O	Negative Debug Bus Strobe: Used to transfer data at the 4x rate. XDP_DSTBP# is the positive strobe. Transfer occurs on the rising edges of XDP_DSTBN#. The NB drives and samples XDP_DSTBN#.
XDP_DSTBP#	I/O	Positive Debug Bus Strobe: Used to transfer data at the 4x rate. XDP_DSTBN# is the negative strobe. Transfer occurs on the falling edges of XDP_DSTBP#. The NB drives and samples XDP_DSTBP#.
XDP_ODTCRES	I	Debug Bus On-Die Termination Compensation Resistors: Compensation resistor that determines the FSB on-die termination.
XDP_RDY#	I/O	Debug Bus Ready
XDP_SLWCRES	I	Debug Bus Slew Rate Compensation Resistor: Compensation resistor that determines the FSB driver slew rate.

3.9 RAS Signal

Table 3-11. Intel® E8501 Chipset North Bridge (NB) Signals (RAS) (Sheet 1 of 2)

Signal Name	Type	Description						
PME_OUT / EXP1_WIDTH2	I/O	See Table 3-5.						
EXP_HPINT / EXP1_WIDTH1	I/O	See Table 3-5.						
IMI_HPINT	I/O	IMI Hot-Plug Interrupt: The NB asserts IMI_HPINT to signal an IMI hot-plug event. Also used as Processor Strap. <table><tr><th>Strap</th><th>Function</th></tr><tr><td>0</td><td>64-bit Intel® Xeon® processor MP with 1MB L2 cache or Dual-Core Intel® Xeon® processor 7000 sequence</td></tr><tr><td>1</td><td>64-bit Intel® Xeon® processor MP with up to 8MB L3 cache</td></tr></table>	Strap	Function	0	64-bit Intel® Xeon® processor MP with 1MB L2 cache or Dual-Core Intel® Xeon® processor 7000 sequence	1	64-bit Intel® Xeon® processor MP with up to 8MB L3 cache
Strap	Function							
0	64-bit Intel® Xeon® processor MP with 1MB L2 cache or Dual-Core Intel® Xeon® processor 7000 sequence							
1	64-bit Intel® Xeon® processor MP with up to 8MB L3 cache							
GP_SMBCLK	I/O	General Purpose I/O Clock: SMBus master clock for a bank of general-purpose I/O which can be connected to the hot-plug controller.						
GP_SMBDATA	I/O	General Purpose I/O Data: SMBus data for a bank of general-purpose I/O which can be connected to the hot-plug controller						

Table 3-11. Intel® E8501 Chipset North Bridge (NB) Signals (RAS) (Sheet 2 of 2)

Signal Name	Type	Description
SMBCLK	I	System Management Bus Clock: SMBus slave clock for the system management bus. Provides access to configuration registers only. This input may change asynchronously with respect to HCLK.
SMBDATA	I/O	System Management Bus Address/Data: SMBus data for the system management bus. Provides access to configuration registers only. This input may change asynchronously with respect to HCLK.
ERR[2:0]#	O	ERROR: Assertion time is 18 cycles. Multiple errors on the same signal occurring during an assertion will not be distinguishable as separate events.

3.10 Miscellaneous Signals

Table 3-12. Miscellaneous Signals

Signal Name	Type	Description
TESTHI	N/A	High Test Pin: Should be pulled high to P1V5 (VCC) on customer platforms. For the locations of these signals on the NB package, refer to Table 7-2 "NB Pin List (by Signal Name)" on page 7-373.
TESTLO	N/A	Low Test Pin: Should be pulled low to VSS on customer platforms. For the locations of these signals on the NB package, refer to Table 7-2 "NB Pin List (by Signal Name)" on page 7-373.
RESERVED	N/A	Reserved: All reserved pins must be left unconnected. Connection of these pins to VCC, VSS, or to any other signal (including each other) can result in component malfunction. For the location of these signals on the NB package, refer to Table 7-2 "NB Pin List (by Signal Name)" on page 7-373.

§



4 Register Description

The Intel® E8501 chipset North Bridge (NB) configuration registers provide functionality, flexibility and settings that can be used to optimize performance of the chipset.

The NB registers can be accessed by a memory mapped register access mechanism, a PCI configuration access mechanism (only PCI space registers), and register access mechanisms through JTAG and SMBus. The memory mapped access mechanism is further broken down into different ranges. The internal registers of this chipset can be accessed in Byte, Word (16-bit), or Dword (32-bit) quantities, with the exception of CFGADR which can only be accessed as a Dword. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). The NB can also forward accesses to all IMI and PCI/PCI Express device configuration registers through the same mechanisms.

This chapter describes how the configuration spaces in the NB are organized and accessed. Registers are described in the order of the layout by device and offset. For configuration spaces on the XMB, please refer to the *Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet*.

4.1 Register Terminology

Each of the bits in the configuration registers have specific attributes. The following table defines all the attribute types. With the exception of the Sticky bits, all bits will be set to their default values by a hard reset.

Table 4-1. Register Attribute Definition (Sheet 1 of 2)

Attribute	Definition	Description
RO	Read Only	The bit is set by the hardware only and software can only read the bit. Writes to the register have no effect.
WO	Write Only	The bit is not implemented as a bit. The write causes some hardware event to take place.
RW	Read/Write	The bit can be both read and/or written by software.
RWC	Read/Write Clear	The bit can be either read or cleared by software. In order to clear this bit, the software must write a “1” to it. Writing a “0” to this bit will have no effect.
RWS	Read/Write Set	The bit can be either read or set by software. In order to set this bit, the software must write a “1” to it. Writing a “0” to this bit will have no effect. Hardware will clear this bit.
RWL	Read/Write Lock	The bit can be read and written by software. Hardware or a configuration bit can lock this bit and prevent it from being updated.
RWO	Read/Wnte Once	The bit can be read by software. It can also be written by software, but the hardware prevents writing/setting it more than once without a prior hard reset. This protection applies on a bit-by-bit basis. For example, if the RWO field is two bits and only one bit is written, then the written bit cannot be rewritten (unless reset). However, the unwritten byte can still be written once. This is a special form of RWL.

Table 4-1. Register Attribute Definition (Sheet 2 of 2)

Attribute	Definition	Description
Any of the above with "ST" appended to the end	Sticky	The bit is "sticky" or unchanged by a hard reset. These bits can only be cleared by a PWRGOOD reset.
RV	Reserved	This bit is reserved for future expansion and must not be written. The <i>PCI Local Bus Specification, Revision 2.2</i> requires that reserved bits must be preserved. Any software that modifies a register that contains a reserved bit is responsible for reading the register, modifying the desired bits, and writing back the result. Intel highly recommends not changing the default value of Reserved bits.
RRW	Read Restricted Write	This bit can be read and written by software. However, only supported values will be written. Writes of non-supported values will have no effect.

4.2 Platform Configuration

Intel® E8501 chipset registers are organized to adhere to the PCI / PCI Express configuration organization. PCI/PCI Express configuration space registers reside on the NB, XMB, ICH5, and on components attached to the PCI Express ports. It can accommodate PCI's 256 distinct buses, 32 devices per bus, 8 functions per device and 64 registers per function. In addition, it can also accommodate the PCI Express enhanced configuration space addressing. The PCI Express enhanced configuration space includes an additional 4-bit extended register address which allows for 16 PCI compatible ranges. The extended region provides addressability of up to 4x16 M configuration registers. Different levels of abstraction are provided by Buses, Devices, Functions, and PCI Express extended register address. The extended PCI Express region can only be accessed through the memory mapped register mechanism.

The Intel® E8501 chipset register set conforms to the minimum necessary subset of PCI to PCI bridge standard registers to aid in software enumeration (required for the PCI Express ports/links).

The NB and ICH5 are physically connected by a legacy Hub Interface port. From a configuration standpoint, the Hub Interface port is the logical PCI/PCI Express bus #0. The NB, XMB, and ICH5 are hard coded to bus #0. The NB/XMB functions and the NB/PCI Express ports on the NB will be different devices on bus #0. The PCI Express devices connected to the NB/PCI Express ports will have programmable bus numbers. The PCI bus connected to the ICH5 will also have a programmable bus number. For a list of all device numbers please refer to Table 4-8.

4.3 Conflict Resolution and Usage Model Limitations

The following assumptions are made about the different types of configuration accesses and which ones can be concurrent. These are considered software constraints.

- Only one PCI (legacy PCI Express) configuration access from all processors at a time.

In all cases, the NB can serialize all allowable concurrent configuration accesses.

Table 4-2 summarizes what configuration accesses can be attempted concurrently to the Intel® E8501 chipset registers. This table only applies to the NB and XMB registers. It does not apply to registers that truncates forwards such as a register on a downstream PCI Express device.

Table 4-2. Intel® E8501 Chipset Concurrent Configuration Accesses

	Proc MMCFG ¹	Proc CF8/CFC Config	JTAG	SMBus
Proc MMCFG ¹	Yes	Yes	Yes	Yes
Proc CF8/CFC Config	Yes	No	Yes	Yes
JTAG	Yes	Yes	No ²	Yes
SMBus	Yes	Yes	Yes	No ³

NOTES:

1. Includes all types of MMCFG accesses: PCI Express, and fixed boot.
2. A JTAG access to the NB can occur concurrently with a JTAG access to XMB if a system has 2 independent JTAG controllers, but accesses to the same component will occur one at a time.
3. An SMBus access to the NB can occur concurrently with an access to XMB if the system has 2 independent SMBus controller.

4.4 Device Mapping

Each component in an Intel® E8501 chipset system can be uniquely identified. Based on the PCI configuration convention, each component is assigned a Bus Number and Device Number. All the NB registers will appear on Bus #0.

All the NB configuration resides in the configuration space defined by Bus, Device, Function, and Register. Some registers do not appear in all portions of this space and some mechanisms do not access all portions of this space. The following table defines where the various fields of configuration register addresses appear. Each row defines a different access mechanism, register, interface, or decoder. Each column defines a different field of the configuration address.

Table 4-3. Configuration Address Bit Mapping (Sheet 1 of 2)

	Source/Destination	Bus	Device	Function	Dword Offset[11:8]	Dword Offset[5:0]	Byte in Dword	Type
HI1.5 Config	Both	A[24:16] always 0	A[15:11]	A[10:8]	Cannot Access	A[7:2]	1st DW BE	ct
PCI Express Config Txns	Both	Bus[7:0]	Device[4:0]	Function[2:0]	Extended Register Addr[3:0]	Register [5:0]	1st DW BE [3:0]	Fmt, Type ¹
PCI Express MMCFG on Front Side Bus	Source	A[27:20]	A[19:15]	A[14:12]	A[11:8]	A[7:3] BE[7:4] ²	f(BE[7:0]) ³	N/A
PCI Express MMCFG from HI1.5 or PCI Express	Forwarded unmodified to peers and are not permitted to access the NB or XMB regs							

Table 4-3. Configuration Address Bit Mapping (Sheet 2 of 2)

	Source/Destination	Bus	Device	Function	Dword Offset[11:8]	Dword Offset[5:0]	Byte in Dword	Type
CFGADR Register ⁴	Source	Bus Number [7:0]	DeviceID [4:0]	Function Number [2:0]	Not Present	Register Address[5:0]	Not Present	N/A
CFC on PSB	Source	CFGADR Register, see row above					BE[7:4]	N/A
JTAG Config Access	Source	Bus Number [7:0]	DeviceID [4:0]	Function Number [2:0]	Extended Register Addr[3:0]	Register Address[7:2]	Register Address[1:0]	N/A
SMBus Config Access	Source	Bus Number [7:0]	Dev[4:0]	Func[2:0]	Reg Number [11:8]	Reg[7:2]	f(command Register Number) ⁵	N/A
Fixed NB Memory Mapped on Front Side Bus	Source	N/A	N/A	A[18:16] ⁶	Cannot Access	A[15:8]	All accesses are 4 byte	N/A
NB Register Decoding	Destination	00000000	See Table 4-8	Function [2:0]	Dword Offset[9:6]	Dword Offset[5:0]	Byte[3:0]	N/A
IMI Config Cmds	Destination	A[24:16] always 0	A[15:11]	A[10:8]	Cannot Access	A[7:2]	M[3:0]	00

NOTES:

1. Encoded as CfgWr0, CfgWr1, CfgRd0, CfgRd.
2. If BE[7:4]! = 0, DwordOffset[0] = 1.
3. If (BE[3:0]! = 0000, BE[3:0], else BE[7:4]).
4. The fields of this register are written by D[31:0] of a front side bus CF8 access.
5. If Dword Access, 1111. If Byte Access, function of RegisterNumber as follows: BE[0]=RegisterNumber=00, BE[1]=RegisterNumber=01, BE[2]=RegisterNumber=10, BE[3]=RegisterNumber=11.
6. Hard coded value of 00FE60.

4.5 Allowable Configuration Access

Intel® E8501 chipset registers can be accessed by various access mechanisms via different interfaces (JTAG, SMBus, I/O (inbound), processor). Table 4-4 defines which registers are accessible using the various mechanisms. For example, JTAG and SMBus configuration accesses can access all chipset registers. The legends and register definitions are defined directly below the table.

Table 4-4. Configuration Register Accessibility

Initiator	Access Mechanism	Type Of Register			
		PCI EXP EXT	BIOS Fixed	SPD & other NB/XMB Cfg	Registers South of NB
JTAG/SMBus		Y	Y	Y	Y
HM1.5/ PCI Express	Cfg ¹	Y*	Y*	Y*	Y*
	CFC/CF8	N	N/A	N	N
	PCI Express MMCFG	N ²	N	N	N
	Special Mem Range	N/A	Y if BIOS Fixed Range ³	N/A	N/A
Processor	CFG/CF8	N	Y*	Y*	Y*
	PCI Express MMCFG	Y	N/A	Y	Y
	Special Mem Range	N/A	Y if BIOS Fixed Range	N/A	N/A

NOTES:

1. Enable bit per PCI Express link can disable this access (DIS_INB_CFG bit of the EXP_CTRL register – see Section 4.11.28, "EXP_CTRL[7:1]: PCI Express Control Register (D1-7, F0)" on page 102).
2. Internal NB mechanism can be that since the inbound memory write doesn't hit any other valid address region, it is sent to the HI1.5 by default.
3. BIOS fixed registers are mapped to special memory ranges.

Legends for Table 4-2	
Y	Supported
Y*	Supported but can be disabled
N	Not Supported
N/A	Not Applicable

Register Definition For Table 4-2	
PCI Express Ext	PCI Express extended configuration space registers (offset >0xFF).
BIOS Fixed	Chipset registers fixed in memory space. These are the bOFLA[], SPAD[], and SPADSA[] registers.
Other NB/XMB Cfg	NB/XMB registers other than the ones that have already been mentioned above. Also includes DIMM SPD accesses.
Registers South of NB	Registers residing on ICH5, Intel® 6700PXH 64-bit PCI Hub, and other devices connected to the PCI Express ports, plus all the associated children devices.

4.6 I/O Mapped Registers

The PCI configuration access mechanism enables support of legacy/PCI code that utilizes the PCI mechanism. The mechanism is defined in *PCI Local Bus Specification, Revision 2.2*. Two bus cycles are defined to access PCI configuration space:

- Configuration Read
- Configuration Write

These configurations access the registers through two I/O-space locations: CFGADR and CFGDAT. The Intel® E8501 chipset has reserved two special I/O locations (0xCF8 / 0xCFC) for direct configuration accesses. Accesses to configuration space through these registers are commonly referred as CF8/CFC configuration accesses. The PCI configuration access sequence is described as follows:

1. The processor first performs a Dword I/O write to CONFIG_ADDRESS to select the bus number, device number, function number and the specific configuration address in the device.
2. A subsequent read or write of the CONFIG_DATA location causes the data transfer to/from the selected configuration register. Byte enables are valid during accesses to CONFIG_DATA and are used to select the byte(s) within the configuration register.

If the access is targeted to a chipset register that does not reside in the NB, the NB will forward the access to the appropriate interface. Intel® E8501 chipset supports both Type 0 and Type 1 configuration access mechanism as described in the *PCI Local Bus Specification, Revision 2.2* to enable hierarchical PCI buses. Type 0 accesses are used for registers that reside on the secondary bus. Type 1 accesses are used for registers that reside on subordinates buses. For more details, please refer to the *PCI Local Bus Specification Revision 2.2*. Accesses to the memory port follows the format of *Memory Port Specification*. Accesses to devices on the PCI Express link follows the format of *PCI Express Specification*. Both memory port and PCI Express preserves the address mapping of *PCI Local Bus Specification, Revision 2.2*.

4.6.1 CFGADR –Configuration Address Register

This 32-bit-wide register is written only when a processor I/O transaction to CF8 is referenced as a Dword, a Byte or Word reference will not access this register, but will generate an I/O space access.

The CFGADR register contains the Bus Number, Device Number, Function Number, and Register Offset for which a subsequent CFGDAT access is intended. The mapping between fields in this register and PCI Express or Hub Interface configuration transactions is defined by Table 4-3.

Table 4-5. PCI CFGADR Register

31	30		24	23		16	15		11	10		8	7		2	1	0
En	Reserved				Bus Number				Device Number		Function Number		Register Number		0		

* En = Enable Bit
1 = Enabled
0 = Disabled

I/O Address:CF8h			
Bit	Attr	Default	Description
31	RW	0h	CFGE: Configuration Enable Unless this bit is set, accesses to the CFGDAT register will not produce a configuration access, but will be treated as other I/O accesses. This bit is strictly an enable for the CFC/CF8 access mechanism and is not forwarded to HI or PCI Express.
30:24	RV	00h	Reserved
23:16	RW	00h	Bus Number If 0, the NB examines device to determine where to route. If non-zero, route as per PBUSN and SBUSN registers.
15:11	RW	0h	Device Number
10:8	RW	0h	Function Number This field is used to select the function of a locally addressed register.
7:2	RW	00h	Register Offset If this register specifies an access to the NB registers, this field specifies a group of four bytes to be addressed. The bytes accessed are defined by the Byte enables of the CFGDAT register access.
1:0	RW*	0h	Writes to these bits will have no effect, reads return 0.

4.6.2 CFGDAT –Configuration Data Register

CFGDAT provides data for the 4 bytes of configuration space defined by CFGADR. This register is only accessed if there is an access to I/O address CFCh on the front side bus and CFGADR.CFGE is set. The byte enables with the IO access define how many configuration bytes are accessed.

I/O Address:CFCh			
Bit	Attr	Default	Description
31:0	RW	0000h	Configuration Data Window The data written or read to the configuration register (if any) specified by CFGADR.

4.7 Intel® E8501 Chipset North Bridge (NB) Fixed Mapped Registers

These registers are mapped into the fixed chipset-specific range located from FE60_0000-FE6F_FFFF. These appear at fixed addresses to support the boot process. These registers also appear in the regular PCI Express configuration space. Table 4-6 defines the memory address of the registers in this region.

Table 4-6. Mapping of Fixed Memory Mapped Registers

Register	Memory Address
BOFL0	FE60_C000
BOFL1	FE60_C400
BOFL2	FE60_C800
BOFL3	FE60_CC00
SPAD0	FE60_D000
SPAD1	FE60_D400
SPAD2	FE60_D800
SPAD3	FE60_DC00
SPADS0	FE60_E000
SPADS1	FE60_E400
SPADS2	FE60_E800
SPADS3	FE60_EC00

4.8 PCI Express Device Configuration Registers

The PCI Express register structure is exposed to the operating system and requires a separate device per port. Ports A-D will be assigned devices 1 through 7 (refer to Figure 2-2 on page 2-30.) The PCI Express ports determine at reset the width of the devices to which they are connected. If ports are combined to form x8 ports, configuration accesses to the most significant device numbers will still be completed successfully, but only the least significant device number will control and hold status for the wider port.

Table 4-7. When will a PCI Express Device be Accessible?

PCI Express Port	Device	x8	Registers may be accessed if...
A1	7	Possible Combination	Port A1 is connected to a x4 device.
A0	6		Port A0 is connected to a x4 or x8 device.
B1	5	Possible Combination	Port B1 is connected to a x4 device.
B0	4		Port B0 is connected to a x4 or x8.
C1	3	Possible Combination	Port C1 is connected to a x4 device.
C0	2		Port C0 is connected to a x4 or x8 device.
D	1	Cannot be a x8	A 4x device is connected to Port D. This port cannot be combined with any other PORT to form an x8.

Figure 4-1 illustrates how each PCI Express port's configuration space appears to software. Each PCI Express port's configuration space has 4 regions:

- **Standard PCI Header** - This region closely resembles a standard PCI-to-PCI bridge header.
- **PCI Device Dependent Region** - The region is also part of standard PCI configuration space and contains the PCI capability structures. For the NB, the supported capabilities are:
 - Message Signalled Interrupts
 - Hot-Plug
 - PCI Express Capability
- **PCI Express Extended Configuration Space** - This space is an enhancement beyond standard PCI and only accessible with PCI Express aware software. The NB supports the Enhanced Error Signalling capability.
- **Capability Working Register Sets** - These ranges are indirectly accessed through Data and Select registers in the capability structures. For the NB, working register sets exist for the Standard hot-plug Controller and Power Management capabilities.

Figure 4-1. PCI Express Configuration Space

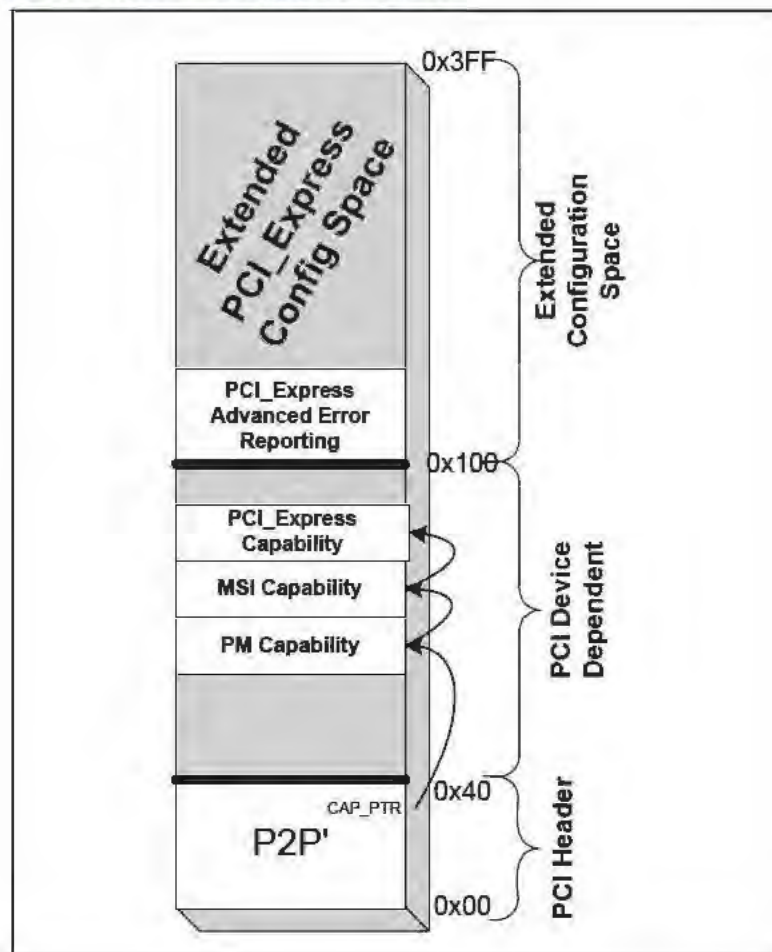


Figure 4-1 shows the configuration register offset addresses. Each port is a separate device. As defined in the *PCI Express Specification*, the PCI 2.3 compatible capability structure is a linked list in which each capability has a pointer to the next capability. For PCI Express capabilities, the first structure is required to start at 0x100 offset.

The PCI Express and Extended PCI Express registers are fully explained in [Section 4.11](#) and [Section 4.12](#).

4.9 Configuration Space Map

All devices on the NB reside on BUS 0. Table 4-8 provides a quick cross-reference for the devices and functions that the NB implements or routes specially, followed by the configuration maps for each device. Please note that this document will only explain the NB devices; hence, for devices not handled by the NB, readers should refer to the corresponding documentations as indicated in the table.

Table 4-8. PCI Devices and Functions Handled by Intel® E8501 Chipset North Bridge (NB) (Sheet 1 of 2)

Component	Register Group	DID Register Value	Device	Function
NB	Hub Interface	2600h	0	0
NB	PCI Express D	2601h	1	0
NB	PCI Express C0	2602h ^a	2	0
NB	PCI Express C1	2603h	3	0
NB	PCI Express B0	2604h ^b	4	0
NB	PCI Express B1	2605h	5	0
NB	PCI Express A0	2606h ^c	6	0
NB	PCI Express A1	2607h	7	0
NB	IMI A	260Ch	8	0
XMB_A	All (Refer to <i>Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet</i>)	2620h - 2627h	9	0 - 7
NB	IMI B	260Ch	10	0
XMB_B	All (Refer to <i>Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet</i>)	2620h - 2627h	11	0 - 7
NB	IMI C	260Ch	12	0
XMB_C	All (Refer to <i>Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet</i>)	2620h - 2627h	13	0 - 7
NB	IMI D	260Ch	14	0
XMB_D	All (Refer to <i>Intel® E8501 Chipset eXternal Memory Bridge (XMB) Datasheet</i>)	2620h - 2627h	15	0 - 7
NB	Front Side Bus, Boot, and Interrupt	2610h	16	0
NB	Address Mapping	2611h	16	1
NB	RAS (FSB and HI Error Registers)	2612h	16	2

Table 4-8. PCI Devices and Functions Handled by Intel® E8501 Chipset North Bridge (NB) (Sheet 2 of 2)

Component	Register Group	DID Register Value	Device	Function
NB	Miscellaneous	2613h - 2615h	17	0-2
NB	Reserved		18	All
NB	Reserved	2617h - 261Eh	19	0-7
NB	Reserved		20	All
ICH5	Compatibility		Other	All

NOTES:

- Software should program this to 2608h if this is connected to an x8 link.
- Software should program this to 2609h if this is connected to an x8 link.
- Software should program this to 260Ah if this is connected to an x8 link.

If a port is disabled or disconnected, then the NB will not forward transactions to the downstream side of the link. These accesses will be Master Aborted by the NB. Configuration registers resident on the NB will still be accessible, however, and it is the responsibility of Software to comprehend the presence of configuration registers even for ports that are disabled even if disabled simply because a wider port (e.g. x8) is using the link wires.

To comply with the PCI specification, accesses to these non-existent functions, registers, and bits will be treated as follows:

Table 4-9. Access to “Non-Existent” Register Bits

Access to	Writes	Reads
Functions not listed in Table 4-8	Have no effect	NB returns all ones
Registers not listed in Table 4-3	Have no effect	NB returns all zeroes
Reserved bits in registers	Software must read modify-write to preserve the value	NB returns all zeroes

Table 4-10. Device 0, Function 0: Hub Interface 1.5 Registers

DID	VID	00h		80h
PCISTS	PCICMD	04h		84h
CCR	RID	08h		88h
HDR		0Ch		8Ch
		10h		90h
		14h		94h
		18h		98h
		1Ch		9Ch
		20h		A0h
		24h		A4h
		28h		A8h
SID	SVID	2Ch		ACH
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
		40h		C0h
		44h		C4h
		48h		C8h
HINERR	HIFERR	4Ch		CCh
NRECHI		50h	HICTL	D0h
RECHI		54h		D4h
	HIEMASK	58h	HICTL2	D8h
HIMCERR	HIERR2	5Ch		DCh
HIERR1	HIERR0	60h		E0h
		64h		E4h
		68h		E8h
		6Ch		ECh
		70h		F0h
		74h		F4h
		78h		F8h
		7Ch		FCh

Table 4-11. Device 1 - 7, Function 0: PCI Express Space Registers

DID		VID		00h	EXP_SLOTCAP		80h	
EXP_STS		EXP_CMD		04h	EXP_SLOTSTS	EXP_SLOTCTRL	84h	
CCR			RID	08h		EXP_RTCTRL	88h	
BIST	HDR	PRI_LT	CLS	0Ch	EXP_RTSTS			8Ch
				10h				90h
				14h				94h
SEC_LT	SUBUSN	SBUSN	PBUSN	18h				98h
SECSTS		IOLIM	IOBASE	1Ch				9Ch
MLIMIT		MBASE		20h				A0h
PMLIMIT		PMBASE		24h				A4h
PMBU				28h				A8h
PMLU				2Ch				ACH
			CAPPTR	30h				B0h
				34h				B4h
				38h				B8h
BCTRL		INTP	INTL	3Ch				BCh
				40h				C0h
				44h				C4h
EXP_CTRL				48h				C8h
			EXP_CTRL2	4Ch				CCh
PMCAP				50h				D0h
PMSCR				54h				D4h
MSICTRL		MSINXPTR	MSICAPID	58h				D8h
MSIAR				5Ch				DCh
MSIDR				60h				E0h
				64h				E4h
				68h				E8h
EXP_CAP		EXP_CAPL		6Ch				ECh
EXP_DEVCAP				70h				F0h
EXP_DEVSTS		EXP_DEVCTRL		74h				F4h
EXP_LNKCAP				78h				F8h
EXP_LNKSTS		EXP_LNKCTRL		7Ch				FCh

Table 4-12. Device 1 - 7, Advanced Function 0: PCI Express Extended Registers

ENHCAPSTS	100h		180h
UNCERRSTS	104h		184h
UNCERRMSK	108h		188h
UNCERRSEV	10Ch		18Ch
CORERRSTS	110h		190h
CORERRMSK	114h		194h
AERCACR	118h		198h
HDRLOG0	11Ch		19Ch
HDRLOG1	120h		1A0h
HDRLOG2	124h		1A4h
HDRLOG3	128h		1A8h
RPERRCMD	12Ch		1ACh
RPERRMSGSTS	130h		1B0h
ERRSID	134h		1B4h
	138h		1B8h
	13Ch		1BCh
NBSPCAPID	140h		1C0h
EXP_UNITERR	144h		1C4h
EXP_ERR_DOCMD	148h		1C8h
UNCEDMASK	14Ch		1CCh
COREDMASK	150h		1D0h
RPEDMASK	154h		1D4h
EXP_UNITDMASK	158h		1D8h
	15Ch		1DCh
EXP_FERR	160h		1E0h
EXP_NERR	164h		1E4h
EXP_UNITEMASK	168h		1E8h
	16Ch		1ECh
	170h		1F0h
	174h		1F4h
	178h		1F8h
	17Ch		1FCh

Table 4-13. Device 8,10,12,14 Function 0: IMI Registers

DID	VID	00h		80h
		04h		84h
CCR	RID	08h		88h
HDR		0Ch		8Ch
		10h		90h
		14h		94h
		18h		98h
		1Ch		9Ch
		20h		A0h
		24h		A4h
		28h		A8h
SID	SVID	2Ch		ACh
		30h		B0h
		34h		B4h
		38h		B8h
		3Ch		BCh
IMISC		40h	IMI_FERR	C0h
		44h	IMI_NERR	C4h
IMIST		48h		C8h
IMIHPC		4Ch		CCh
		50h		D0h
		54h	RECIMI	D4h
		58h	NRECIMI	D8h
		5Ch	REDIMIL	DC
IMICHNK	IMILINE	60h	EMASK_IMI	DCh
IMIOFF	IMIAPR	64h	IMI_ERR1	E0h
	IMICODE	68h	IMI_ERR0	E4h
		6Ch	IMI_MCERR	E8h
		70h		EC
		74h		ECh
		78h		F0h
		7Ch		F4h
				F8h
				FC

Table 4-14. Device 16, Function 0: Front Side Bus, Boot and Interrupt Registers

DID	VID	00h	XTPR0	80h
		04h	XTPR1	84h
CCR	RID	08h	XTPR2	88h
HDR		0Ch	XTPR3	8Ch
		10h	XTPR4	90h
		14h	XTPR5	94h
		18h	XTPR6	98h
		1Ch	XTPR7	9Ch
		20h	XTPR8	A0h
		24h	XTPR9	A4h
		28h	XTPR10	A8h
SID	SVID	2Ch	XTPR11	ACH
		30h	XTPR12	B0h
		34h	XTPR13	B4h
		38h	XTPR14	B8h
		3Ch	XTPR15	BCh
	SYRE	40h	BOFL0	C0h
		44h	BOFL1	C4h
		48h	BOFL2	C8h
		4Ch	BOFL3	CCh
	REDIRCTL	50h	SPAD0	D0h
REDIRDIS		54h	SPAD1	D4h
REDIRBUCKETS		58h	SPAD2	D8h
		5Ch	SPAD3	DCh
POC_FSBA		60h	SPADS0	E0h
	POC_AUXA	64h	SPADS1	E4h
		68h	SPADS2	E8h
		6Ch	SPADS3	ECh
POC_FSBB		70h		F0h
	POC_AUXB	74h		F4h
		78h		F8h
		7Ch		FCh

Table 4-15. Device 16, Function1: Address Mapping Registers

DID		VID		00h	IMIR0	80h
				04h	IMIR1	84h
CCR		RID		08h	IMIR2	88h
HDR				0Ch	IMIR3	8Ch
				10h	IMIR4	90h
				14h	IMIR5	94h
				18h		98h
				1Ch		9Ch
				20h	AIMIR0	A0h
				24h	AIMIR1	A4h
				28h	AIMIR2	A8h
SID		SVID		2Ch	AIMIR3	ACh
				30h	AIMIR4	B0h
				34h	AIMIR5	B4h
				38h		B8h
				3Ch		BCh
				40h	SB_A_IMIR0	C0h
				44h	SB_A_IMIR1	C4h
				48h	SB_A_IMIR2	C8h
				4Ch	SB_A_IMIR3	CCh
				50h	SB_A_IMIR4	D0h
				54h	SB_A_IMIR5	D4h
PAM2		PAM1	PAM0	58h		D8h
PAM6	PAM5	PAM4	PAM3	5Ch		DCh
EXSMRTOP	EXSMRC	SMRAMC	FDHC	60h	SB_B_IMIR0	E0h
				64h	SB_B_IMIR1	E4h
EXP_ECBASE				68h	SB_B_IMIR2	E8h
		TOLM		6Ch	SB_B_IMIR3	ECh
				70h	SB_B_IMIR4	F0h
				74h	SB_B_IMIR5	F4h
				78h		F8h
				7Ch		FCh

Table 4-16. Device 16, Function 2: RAS Registers

DID	VID	00h	FSBA_NERR	FSBA_FERR	80h
		04h	RECF_SBA_LOG		84h
CCR	RID	08h	NRECF_SBA_LOG0		88h
HDR		0Ch	NRECF_SBA_LOG1		8Ch
		10h	NRECF_SBA_LOG2		90h
		14h	ERR0_FSBA	EMASK_FSBA	94h
		18h	ERR2_FSBA	ERR1_FSBA	98h
		1Ch	ICHRST_FSBA	MCERR_FSBA	9Ch
		20h	FSBB_NERR	FSBB_FERR	A0h
		24h	RECF_SBB_LOG		A4h
		28h	NRECF_SBB_LOG0		A8h
SID	SVID	2Ch	NRECF_SBB_LOG1		ACH
		30h	NRECF_SBB_LOG2		B0h
		34h	ERR0_FSBB	EMASK_FSBB	B4h
		38h	ERR2_FSBB	ERR1_FSBB	B8h
		3Ch	ICHRST_FSBB	MCERR_FSBB	BCh
Global_FERR		40h	INT_NERR	INT_FERR	C0h
Global_NERR		44h	NRECNB		C4h
		48h	RECNB		C8h
		4Ch			CCh
		50h	MCERR_INT	ERR2_INT	D0h
		54h	INT1_INT	ERR0_INT	D4h
		58h	RECINT_LOG0		D8h
		5Ch	RECINT_LOG1		DCh
		60h	RECINT_LOG2		E0h
		64h	RECINT_LOG3		E4h
		68h	RECINT_LOG4		E8h
		6Ch	INTLOGC		ECh
		70h			F0h
		74h			F4h
		78h			F8h
		7Ch			FCh

Table 4-17. Device 17, Function 0: Miscellaneous Registers

DID	VID	00h	80h
		04h	84h
CCR	RID	08h	88h
HDR		0Ch	8Ch
		10h	90h
		14h	94h
		18h	98h
		1Ch	9Ch
		20h	A0h
		24h	FSBDC[0]A4h
		28h	A8h
SID	SVID	2Ch	ACH
		30h	FSB[0]AC2B0h
		34h	B4h
		38h	FSB[0]ACB8h
		3Ch	BCh
		40h	C0h
		44h	C4h
		48h	C8h
		4Ch	CCh
		50h	D0h
		54h	D4h
		58h	D8h
		5Ch	DCh
		60h	E0h
		64h	E4h
		68h	E8h
		6Ch	ECh
		70h	F0h
		74h	F4h
		78h	F8h
		7Ch	FCh

Table 4-18. Device 17, Function 1: Miscellaneous Registers

DID	VID	00h	80h
		04h	84h
CCR	RID	08h	88h
HDR		0Ch	8Ch
		10h	90h
		14h	94h
		18h	98h
		1Ch	9Ch
		20h	A0h
		24h	FSBDC[1] A4h
		28h	A8h
		2Ch	ACH
SID	SVID	30h	FSB[1]AC2 B0h
		34h	B4h
		38h	FSB[1]AC B8h
		3Ch	BCCh
		40h	C0h
		44h	C4h
		48h	C8h
		4Ch	CCCh
		50h	D0h
		54h	D4h
		58h	D8h
		5Ch	EXP_GCTRL DCh
		60h	E0h
		64h	E4h
		68h	E8h
		6Ch	ECh
		70h	F0h
		74h	F4h
		78h	F8h
		7Ch	FCh

Table 4-19. Device 17, Function 2: Miscellaneous Registers

DID	VID	00h	80h
		04h	84h
CCR	RID	08h	88h
HDR		0Ch	8Ch
		10h	90h
		14h	94h
		18h	98h
		1Ch	9Ch
		20h	A0h
		24h	A4h
		28h	A8h
SID	SVID	2Ch	ACH
		30h	IML_HPTIM
		34h	REDUN
		38h	B8h
		3Ch	BCh
		40h	C0h
		44h	C4h
		48h	C8h
		4Ch	CCh
		50h	D0h
		54h	D4h
		58h	D8h
		5Ch	DCh
		60h	E0h
		64h	E4h
		68h	E8h
		6Ch	ECh
		70h	F0h
		74h	F4h
		78h	F8h
		7Ch	FCh

4.10 Hub Interface 1.5 (Device 0, Function 0)

The Hub Interface 1.5 (HI1.5) registers are in device 0 (D0), function 0 (F0). For quick reference on the register address map, please refer to Table 4-10.

Warning: Address locations that are not listed are considered reserved locations. Writes to “Reserved” registers may cause unpredictable behavior. Reads to “Reserved” registers may return a non-zero value.

4.10.1 VID: Vendor Identification Register (D0, F0)

This register identifies Intel as the manufacturer of the Intel® E8501 chipset North Bridge (NB). Writes to this register have no effect.

Device 0 Function: 0 Offset: 00 - 01h			
Bit	Attr	Default	Description
15:0	RO	8086h	Vendor Identification Number The value assigned to Intel.

4.10.2 DID: Device Identification Register (D0, F0)

This register, combined with the Vendor Identification register uniquely, identifies the NB Function in the event that a driver is required. Writes to this register have no effect.

Device 0 Function: 0 Offset: 02h - 03h			
Bit	Attr	Default	Description
15:0	RO	2600h	Device Identification Number Identifies each function of the NB.

4.10.3 PCICMD:PCI Command Register (D0, F0)

Device: 0 Function: 0 Offset: 04h			
Bit	Attr	Default	Description
15:9	RV	00h	Reserved
8	RO	0	SIG_SYS_ERR: Signalled System Error. The NB never initiates a system error special cycle (DO_SERR), so this bit will always return a 0 when read.
7	RV	0b	Reserved
6	RWST	0	IERRE: Parity Error Response (IERRE). Controls the NB response when a parity error (on function 0) or multi-bit ECC error is detected on the Hub Interface. This bit only controls the detection in PCISTS.DetIntErr and PCISTS.MstrDataIE. The NB reports all parity errors on the Hub Interface.
5:4	RV	00b	Reserved
3	RO	0b	spec_cyc_en: Special Cycle Enable. Controls the ability to forward PCI-type (legacy) special cycles. Devices on the Hub Interface are not capable of accepting legacy special cycles. This bit does not apply to Hub Interface specific special cycles.
2	RO	1b	BM_en: Bus Master Enable. Controls the ability for the NB to initiate Hub Interface cycles. The NB can always issue Hub Interface bus cycles.
1	RO	1b	MemAccEn: Memory Access Enable. Controls the ability for the NB to respond to memory transactions initiated on the Hub Interface. The NB can always accept memory transactions.
0	RO	0b	IOAccEn: I/O Access Enable. Controls the ability for the NB to respond to I/O transactions initiated on the Hub interface. This chipset does not support inbound I/O cycles.

4.10.4 PCISTS: PCI Status Register (D0, F0)

Device: 0 Function: 0 Offset: 06h - 07h			
Bit	Attr	Default	Description
15	RWC	0	DetIntErr: Detected Integrity Error This bit indicates that a parity error was observed on the Hub Interface. This bit is not affected by the state of PCICMD.IERR.
14	RO	0	SSE: Signalled System Error This bit indicates if a system error special cycle (DO_SERR) is initiated by the NB component. This bit should never be asserted since the NB never initiates DO_SERR.
13	RWC	0	RcvMstrAbSts: Received Master Abort Status This bit indicates if the NB receives a Master Abort completion cycle or an unimplemented Special Cycle command.

Device: 0 Function: 0 Offset: 06h - 07h			
Bit	Attr	Default	Description
12	RWC	0	RcvTgtAbSts: Received Target Abort Status This bit indicates if the NB receives a Target Abort completion cycle in response to a NB-initiated Hub Interface cycle.
11	RWC	0	SigTgtAbSts: Signalled Target Abort Status The NB sets this bit when it issues a Target Abort completion cycle to the Hub Interface agent.
10:9	RV	00h	Reserved
8	RWC	0	MstrDataIE: Master Data Integrity Error This bit indicates that a data parity or multi-bit ECC error was detected on the Hub Interface. This bit is set when all of the following conditions are met: • The NB detected a data parity for an outbound read completion • PCICMD.IERR is set to 1
7:0	RV	00h	Reserved

4.10.5 RID: Revision Identification Register (D0, F0)

This register contains the revision number of the Intel® E8501 chipset North Bridge (NB).

Intel® E8501 chipset North Bridge (NB) implements the Revision Identification Registers with a Compatibility Revision Id function in addition to standard revision identification functionality. This Compatibility Revision Id functionality is present in order to allow vendors to replace hardware while maintaining the software visible hardware revision identification registers the same as in previous steppings of the NB.

In order to access the Compatibility Revision Id functionality, the RID registers as a whole can be written to exactly one time with a specific code value (key). This key, when written correctly as the first write to any of the RID registers inside NB will cause NB to return the *compatibility id* value for all future reads of any NB RID register. Table 4-20 describes this compatibility revision identification functionality.

Table 4-20. Intel® E8501 Chipset North Bridge (NB) Compatibility Revision ID Function

Key value written to any RID register	B0 read value	Description
0x79	0x0	Return compatibility id
Any other value	0x10	Return stepping id

Device: 0 Function: 0 Offset: 08h			
Bit	Attr	Default	Description
7:4	RO	0h	Major_rev: Major Revision Steppings which require all masks to be regenerated. 1: B stepping
3:0	RO	0h	Minor_rev: Minor Revision Incremented for each stepping which does not modify all masks. Reset for each major revision. 0h : x0 stepping 1h : x1 stepping 2h : x2 stepping

4.10.6 CCR: Class Code Register (D0, F0)

This register contains the Class Code for the device.

Device: 0 Function: 0 Offset: 09h - 0Bh			
Bit	Attr	Default	Description
23:16	RO	06h	BaseClass: Base Class This field indicates the general device category. For the NB, this field is hardwired to 06h, indicating it is a "Bridge Device".
15:8	RO	00h	SubClass: Sub-Class This field qualifies the Base Class, providing a more detailed specification of the device function. For device 0, this field is hardwired to 00h, indicating it is a "Host Bridge".
7:0	RO	00h	RLPI: Register-Level Programming Interface This field identifies a specific programming interface (if any), that device-independent software can use to interact with the device. There are no such interfaces defined for "Host Bridge" types, and this field is hardwired to 00h.

4.10.7 HDR: Header Type Register (D0, F0)

This register identifies the header layout of the configuration space.

Device: 0 Function: 0 Offset: 0Eh			
Bit	Attr	Default	Description
7	RO	0h	Mfd: Multi-function Device. Selects whether this is a multi-function device, that may have alternative configuration layouts.
6:0	RO	00h	CfgLayout: Configuration Layout. This field identifies the format of the configuration header layout for a PCI-to-PCI bridge from bytes 10h through 3Fh. For this device the default is 00h, indicating a conventional type 00h PCI header.

4.10.8 SVID: Subsystem Vendor Identification Register (D0, F0)

This register identifies the manufacturer of the system. This 16-bit register, combined with the Device Identification Register, uniquely identifies any PCI device.

Device: 0 Function: 0 Offset: 2Ch			
Bit	Attr	Default	Description
15:0	RWO	8086h	Vin: Vendor Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to a byte will have no effect.

4.10.9 SID: Subsystem Identity (D0, F0)

This register identifies the system.

Device: 0 Function: 0 Offset: 2Eh - 2Fh			
Bit	Attr	Default	Description
15:0	RWO	8086h	Sid: Subsystem Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to a byte will have no effect.

4.10.10 HIFERR: Hub Interface First Fatal Error Register (D0, F0)

For a description of the Errors (IOxx) refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 0 Function: 0 Offset: 4Ch			
Bit	Attr	Default	Description
7	RWCST	0	IO6bErr: Received STOP during SRC Fatal Error
6	RWCST	0	IO6Err: Parity error on Address Fatal Error
5	RWCST	0	IO5Err: Illegal Access Fatal Error
4	RWCST	0	IO4Err: Outbound poison Non-fatal Error
3	RWCST	0	IO3Err: Parity Error on outbound data Non-fatal Error
2	RWCST	0	IO2Err: Data Phase Parity Error Non-fatal Error
1	RWCST	0	IO1Err: Cmd Parity Error Non-fatal Error
0	RWCST	0	IO0Err: Target Abort Non-fatal Error

NOTES:

- a. Transaction is retried.

4.10.11 HINERR: Hub Interface Next Fatal Error Register (D0, F0)

Device: 0 Function: 0 Offset: 4Eh			
Bit	Attr	Default	Description
7	RWCST	0	IO6bErr: Received STOP during SRC Fatal Error
6	RWCST	0	IO6Err: Parity error on Address Fatal Error
5	RWCST	0	IO5Err: Illegal Access Fatal Error
4	RWCST	0	IO4Err: Outbound poison Non-fatal Error

Device: 0 Function: 0 Offset: 4Eh			
Bit	Attr	Default	Description
3	RWCST	0	IO3Err: Parity Error on outbound data Non-fatal Error
2	RWCST	0	IO2Err: Data Phase Parity Error Non-fatal Error
1	RWCST	0	IO1Err: Cmd Parity Error Non-fatal ^a Error
0	RWCST	0	IO0Err: Target Abort Non-fatal Error

NOTES:

- a. Transaction is retried.

4.10.12 NRECHI: Non-Recoverable Hub Interface Error Log Register (D0, F0)

The contents of this register depends on whether the error is detected on a request or a response. This is the bit mapping for Hub Interface *Requests* (IF Bit 31 = 0).

Device: 0 Function: 0 Offset: 50h - 53h			
Bit	Attr	Default	Description
31	ROST	0h	NRECHI31: Rq/Cp Request/completion field
30	ROST	0h	NRECHI30: R/W Read/Write field
29	ROST	0h	NRECHI29: CR Completion required field
28	ROST	0h	NRECHI28: AF Address format
27	ROST	0h	NRECHI27: LK Lock cycle
26:21	ROST	0h	NRECHI26DT21: TD Routing Transaction Description routing field
20	ROST	0h	NRECHI20 Reserved Field on the packet
19:16	ROST	0h	NRECHI19DT16: TD Attribute Transaction Descriptor Attribute
15:14	ROST	00	NRECHI15DT14: Spac Address space

Device: 0 Function: 0 Offset: 50h - 53h			
Bit	Attr	Default	Description
13:8	ROST	0h	NRECH13DT8: Data Length Dword data length
7:0	ROST	0h	NRECH7DT0: Byte Enables 7:4 is the Last DW Byte Enables and 3:0 is the First Byte Enables <i>Special Cycle Encoding: when Space field indicates a Special Cycle</i>

This is the bit mapping for Hub Interface *Completions* (IF Bit 31 = 1).

Device: 0 Function: 0 Offset: 50h - 53h			
Bit	Attr	Default	Description
31	ROST	0b	NRECH31: Rq/Cp Request/completion field
30	ROST	0b	NRECH30: R/W Read/Write field
29	ROST	0b	NRECH29 Reserved 1b Field of the packet
28	ROST	0b	NRECHI28 Reserved 1a field of the packet
27	ROST	0b	NRECH27: LK Lock cycle
26:21	ROST	00h	NRECH26DT21: TD Routing Transaction Description routing field
20	ROST	0b	NRECH20 Reserved field on the packet
19:16	ROST	00h	NRECH19DT16: N TD Attribute Transaction Descriptor Attribute
15:14	ROST	00h	NRECH15DT14: Space Address space
13:8	ROST	00h	NRECH13DT8: Data Length Dword data length
7:0	ROST	00h	NRECH7DT0: Completion Status Indicates the status of the request.

4.10.13 RECH: Recoverable Hub Interface Error Log Register (D0, F0)

The contents of this register depends on whether the error is detected on a request or a response. This is the bit mapping for Hub Interface *Requests* (RECH[31] = 0):

Device: 0 Function: 0 Offset: 54h - 57h			
Bit	Attr	Default	Description
31	ROST	0b	RECH31: Rq/Cp Request/completion field
30	ROST	0b	RECH30: R/W Read/Write field
29	ROST	0b	RECH29: CR Completion required field
28	ROST	0b	RECH28: AF Address Format
27	ROST	0b	RECH27: LK Lock Cycle
26:21	ROST	0b	RECH26DT21: TD Routing Transaction Description routing field
20	ROST	0b	RECH20 Reserved Field on the packet
19:16	ROST	00h	RECH19DT16: TD Attribute Transaction Descriptor Attribute
15:14	ROST	00h	RECH15DT14: Space Address Space
13:8	ROST	00h	RECH13DT8: Data Length Dword Data Length
7:0	ROST	00h	RECH7DT0: Byte Enables 7:4 is the Last DW Byte Enables and 3:0 is the First Byte Enables <i>Special Cycle Encoding: when Space field indicates a Special Cycle</i>

This is the bit mapping for Hub Interface *Completions* (RECHI[31] = 1):

Device: 0 Function: 0 Offset: 54h - 57h			
Bit	Attr	Default	Description
31	ROST	0b	RECHI31: Rq/Cp Request/completion field
30	ROST	0b	RECHI30: R/W Read/Write field
29	ROST	0b	RECHI29 Reserved 1b Field of the packet
28	ROST	0b	RECHI28 Reserved 1a Field of the packet
27	ROST	0b	RECHI27: LK Lock cycle
26:21	ROST	00h	RECHI26DT21: TD Routing Transaction Description routing field
20	ROST	0b	RECHI20 Reserved Field on the packet
19:16	ROST	0h	RECHI19DT16: TD Attribute Transaction Descriptor Attribute
15:14	ROST	00b	RECHI15DT14: Space Address Space
13:8	ROST	00h	RECHI13DT8: Data Length Dword Data Length
7:0	ROST	00h	RECHI7DT0: Completion Status Indicates the status of the request.

4.10.14 HIEMASK: Hub Interface Error Mask Register (D0, F0)

A '0' in any field enables that error.

Device: 0 Function: 0 Offset: 58h			
Bit	Attr	Default	Description
7	RW	1	IO6bMsk : Received STOP during SRC Suggested value: 0h
6	RW	1	IO6Msk : Parity error on Address Suggested value: 0h
5	RW	1	IO5Msk : Illegal Access Suggested value: 0h

Device: 0 Function: 0 Offset: 58h			
Bit	Attr	Default	Description
4	RW	1	IO4Msk : Outbound poison Suggested value: 0h
3	RW	1	IO3Msk : Parity Error on outbound data Suggested value: 0h
2	RW	1	IO2Msk : Data Phase Parity Error Suggested value: 0h
1	RW	1	IO1Msk : Cmd Parity Error Suggested value: 0h
0	RW	1	IO0Msk : Target Abort Suggested value: 0h

4.10.15 HIERR0: Hub Interface Error 0 Mask Register (D0, F0)

This register enables the signaling of Err[0] when an error flag is set. Note that one and only one error signal should be enabled at a time.

Device: 0 Function: 0 Offset: 5Ch			
Bit	Attr	Default	Description
7	RWST	0	IO6bErr0 : Received STOP during SRC
6	RWST	0	IO6Err0 : Parity error on Address
5	RWST	0	IO5Err0 : Illegal Access
4	RWST	0	IO4Err0 : Outbound poison
3	RWST	0	IO3Err0 : Parity Error on outbound data
2	RWST	0	IO2Err0 : Data Phase Parity Error
1	RWST	0	IO1Err0 : Cmd Parity Error
0	RWST	0	IO0Err0 : Target Abort

4.10.16 HIERR1: Hub Interface Error 1 Mask Register (D0, F0)

This register enables the signaling of Err[1] when an error flag is set. Note that one and only one error signal should be enabled at a time.

Device: 0 Function: 0 Offset: 5Dh			
Bit	Attr	Default	Description
7	RWST	0	IO6bErr1: Received STOP during SRC
6	RWST	0	IO6Err1: Parity error on Address
5	RWST	0	IO5Err1: Illegal Access
4	RWST	0	IO4Err1: Outbound poison
3	RWST	0	IO3Err1: Parity Error on outbound data
2	RWST	0	IO2Err1: Data Phase Parity Error
1	RWST	0	IO1Err1: Cmd Parity Error
0	RWST	0	IO0Err1: Target Abort

4.10.17 HIERR2: Hub Interface Error 2 Mask Register (D0, F0)

This register enables the signaling of Err[2] when an error flag is set. Note that one and only one error signal should be enabled at a time.

Device: 0 Function: 0 Offset: 5Eh			
Bit	Attr	Default	Description
7	RWST	0	IO6bErr2: Received STOP during SRC
6	RWST	0	IO6Err2: Parity error on Address
5	RWST	0	IO5Err2: Illegal Access
4	RWST	0	IO4Err2: Outbound poison
3	RWST	0	IO3Err2: Parity Error on outbound data
2	RWST	0	IO2Err2: Data Phase Parity Error
1	RWST	0	IO1Err2: Cmd Parity Error
0	RWST	0	IO0Err2: Target Abort

4.10.18 HIMCERR: Hub Interface MCERR Mask Register (D0, F0)

This register enables the signaling of MCERR when an error flag is set. Note that one and only one error signal should be enabled at a time.

Device: 0 Function: 0 Offset: 5Fh			
Bit	Attr	Default	Description
7	RWST	0	IO6bMCErr : Received STOP during SRC
6	RWST	0	IO6MCErr : Parity error on Address
5	RWST	0	IO5MCErr : Illegal Access
4	RWST	0	IO4MCErr : Outbound poison
3	RWST	0	IO3MCErr : Parity Error on outbound data
2	RWST	0	IO2MCErr : Data Phase Parity Error Suggested value: 1h
1	RWST	0	IO1MCErr : Cmd Parity Error
0	RWST	0	IO0MCErr : Target Abort

4.10.19 HICTL: Hub Interface Command Control Register (D0, F0)

Device: 0 Function: 0 Offset: D0h - D3h			
Bit	Attr	Default	Description
31:29	RO	0h	HUB_SUB_FIRST : This field stores the lowest subordinate Hub Interface hub number. This information is compared with the Hub ID to determine whether a completion packet should be forwarded further down the Hub Interface hierarchy.
28	RV	0h	Reserved
27:25	RO	0h	HUB_SUB_LAST : This field stores the highest subordinate Hub Interface hub number. This information is compared with the Hub ID to determine whether a completion packet should be forwarded further down the Hub Interface hierarchy.
24	RV	0h	Reserved
23:21	RO	0h	HUB_ID : This field identifies the Hub Interface ID number for the NB. The NB uses this field to determine when to accept a Hub Interface request packet and send any corresponding completion packets.
20	RV	0	Reserved
19:16	RW	0h	HI_TIMESLICE : This field sets the Hub Interface arbiter time-slice value with four base-clock granularity. A value of zero means that the timer immediately expires and the NB will allow the agent interfacing Hub Interface access to the bus every other transaction.
15:14	RO	0h	HI_WIDTH : This field sets the Hub Interface data bus width. A value of 01 indicates a 16-bit data bus and 00 indicates an 8-bit data bus.

Device: 0 Function: 0 Offset: D0h - D3h			
Bit	Attr	Default	Description
13	RO	1h	HI_RATE_VALID: This bit is sampled by software and indicates when the Hub Interface bus rate is valid.
12:10	RO	010b	HI_RATE: This field indicates the Hub Interface data rate. Function 0 only supports a 4x data rate encoded with 010.
9:8	RW	0h	RCOMP_INT: Determines the time interval for impedance compensation. Encodings are: 00: 128 ms 01: 250 μ s 10: 16 ms 11: 2 ms
7:5	RV	0h	Reserved
4	RWO	0	DIS_INB_CFG: Disable Inbound Configs This bit is used for controlling configuration accesses to the chipset registers through the Hub Interface. 0: Allows access to the NB or XMB registers. 1: Inbound accesses to the NB or XMB registers will be dropped and logged as an illegal access. This register bit is of type "write once" and is controlled by BIOS/special initialization firmware.
3:1	RO	001	MAX_DATA: This field is programmed with the longest data stream the NB is permitted to send on the Hub Interface. MAX_DATA applies to both write request cycles and read completion cycles. 000: 32 bytes 001: 64 bytes 01X: 128 bytes 1XX: 256 bytes
0	RV	0	EN64: Enable 64 bit Addressing The NB does not support 64-bit addressing on the Hub Interface

4.10.20 HICTL2: Hub Interface Command Control Register (D0, F0)

Device: 0 Function: 0 Offset: D4h			
Bit	Attr	Default	Description
7:5	RV	0	Reserved
4:0	RW	0	STOPGRANTACKCNT: The NB will forward every (N+1)th StopGrantAck to the Hub Interface. The default provides for every StopGrantAck to be sent to the Hub Interface. Software is expected to set this to a value of THREADS-1 where THREAD is the number of threads that will issue a StopGrantAck in response to a StopClock request.

4.11 PCI Express Ports (Device 1 - 7, Function 0)

The PCI Express registers are in Device 1 - 7 (D1-7), Function 0 (F0). For the register address map, please refer to Table 4-11. The following registers define the standard PCI 2.3 compatible and extended PCI Express configuration space for each of the PCI Express x4 links in the NB. Unless otherwise specified, the registers are enumerated as a vector [7:1] mapping to each of the seven PCI Express ports uniquely.

Warning: Address locations that are not listed are considered reserved locations. Writes to “Reserved” registers may cause unpredictable behavior. Reads to “Reserved” registers may return a non-zero value.

4.11.1 VID[7:1]: Vendor Identification Register (D1-7, F0)

The VID Register contains Intel as the manufacturer of the NB. Writes to this register have no effect.

Device: 1 - 7 Function: 0 Offset: 00 - 01h			
Bit	Attr	Default	Description
15:0	RO	8086h	Vendor Identification Number The value is assigned to Intel's standard notation.

4.11.2 DID[7:1]: Device Identification Register (D1-7, F0)

This register combined with the Vendor Identification register uniquely identifies the NB function in the event that a driver is required. Writes to this register have no effect.

Device: 1 - 7																											
Function: 0																											
Offset: 02h - 03h																											
Bit	Attr	Default	Description																								
15:0	RWO	See Description	Device Identification Number Identifies each function of the NB. <table><tr><th>Register Group</th><th>Device</th><th>DID</th></tr><tr><td>PCI Express D</td><td>1</td><td>2601h</td></tr><tr><td>PCI Express C0</td><td>2</td><td>2602h</td></tr><tr><td>PCI Express C1</td><td>3</td><td>2603h</td></tr><tr><td>PCI Express B0</td><td>4</td><td>2604h</td></tr><tr><td>PCI Express B1</td><td>5</td><td>2605h</td></tr><tr><td>PCI Express A0</td><td>6</td><td>2606h</td></tr><tr><td>PCI Express A1</td><td>7</td><td>2607h</td></tr></table>	Register Group	Device	DID	PCI Express D	1	2601h	PCI Express C0	2	2602h	PCI Express C1	3	2603h	PCI Express B0	4	2604h	PCI Express B1	5	2605h	PCI Express A0	6	2606h	PCI Express A1	7	2607h
Register Group	Device	DID																									
PCI Express D	1	2601h																									
PCI Express C0	2	2602h																									
PCI Express C1	3	2603h																									
PCI Express B0	4	2604h																									
PCI Express B1	5	2605h																									
PCI Express A0	6	2606h																									
PCI Express A1	7	2607h																									

4.11.3 EXP_CMD[7:1]: Command Register (D1-7, F0)

This register defines the PCI 2.3 compatible command register values applicable to PCI Express space.

Device: 1 - 7 Function: 0 Offset: 04h - 05h			
Bit	Attr	Default	Description
15:11	RV	00h	Reserved (by PCI SIG)
10	RO	0	INTxDisable: Interrupt Disable Controls the ability of the PCI Express port to generate INTx messages. Note that the NB does not have INTx pins and cannot generate interrupts internally. The default value is 0h (interrupt disabled). This bit does not affect the ability of the NB to route interrupt messages received at the PCI Express port for operations such as hot-plug, power management or MSI to either hub interface or the FSB's.
9	RO	0	FB2B: Fast Back-to-Back Enable Not applicable to PCI Express and is hardwired to '0'.
8	RW	0	SERRE: SERR Message Enable This field handles the reporting of fatal and non-fatal errors by enabling the error pins ERR[2:0]. 0: The NB is disabled from generating fatal/non-fatal errors. 1: The NB is enabled to send fatal/non-fatal errors. The errors are also enabled by the EXP_DEVCTRL register (See Section 4.11.40)

Device: 1 - 7 Function: 0 Offset: 04h - 05h			
Bit	Attr	Default	Description
7	RO	0	IDSELWCC: IDSEL Stepping/Wait Cycle Control Not applicable to PCI Express. Hardwired to 0.
6	RW	0	PERRE: Parity Error Enable When set, this field enables parity checking.
5	RO	0	VGAPSE: VGA palette snoop Enable Not applicable to PCI Express. Hardwired to 0.
4	RO	0	MWIEN: Memory Write and Invalidate Enable Not applicable to PCI Express. Hardwired to 0.
3	RO	0	SCE: Special Cycle Enable Not applicable to PCI Express. Hardwired to 0.
2	RW	0	BME: Bus Master Enable Controls the ability of the PCI Express port to forward memory or I/O transactions: 1: Enables the PCI Express port to successfully complete the memory or I/O read/write requests. 0: The Bus Master is disabled. The NB will treat upstream memory writes/reads, IO writes/reads, and MSIs as illegal cycles and return Unsupported Request Status (equivalent to Master abort) in PCI Express. When the BME is disabled, the NB will treat upstream memory writes/reads, IO writes/reads, and MSIs as illegal cycles and return Unsupported Request Status (equivalent to Master abort) in PCI Express. Requests other than inbound memory or I/O (e.g. configuration, outbound) are not controlled by this bit. The BME is typically used by the system software for operations such as Hot-plug device configuration.
1	RW	0	MSE: Memory Space Enable 1: Enables the Memory and Pre-fetchable memory address ranges (MMIO) defined in the MBASE/MLIMIT , PMBASE/PMLIMIT registers. 0: Disables the entire memory space seen by the PCI Express port on the primary side (NB). Requests will then be subtractively claimed by ICH5.
0	RW	0	IOAE: Access Enable 1: Enables the I/O address range defined in the IOBASE and IOLIMIT registers. 0: Disables the entire I/O space seen by the PCI Express port on the primary. Requests will then be subtractively claimed by ICH5.

4.11.4 EXP_STS[7:1]: Status Register (D1-7, F0)

The EXP_STS is a 16-bit status register that reports the occurrence of error conditions associated with the primary side of the “virtual” PCI-PCI bridge embedded in the selected PCI Express cluster of the NB.

Device: 1 - 7 Function: 0 Offset: 06 - 07h			
Bit	Attr	Default	Description
15	RWC	0	DPE: Detected Parity Error This bit is set when the PCI Express port gets an uncorrectable data error or Address/Control parity errors regardless of the Parity Error Enable bit (PERRE). The detected parity error maps to T10 as defined in Table 6-39 'Errors Detected by the NB' on page 328 of this document.
14	RWC	0h	SSE: Signaled System Error 1: The PCI Express port enables system errors through ERR[2:0] pins such as ERR_FATAL and ERR_NONFATAL messages provided SERRE is set. Software clears this bit by writing a 1 to it. 0: No system errors are generated by the PCI Express Port.
13	RWC	0h	RMA: Received Master Abort Master Abort does not exist on the primary side of the PCI Express port. This bit is hardwired to 0.
12	RWC	0h	RTA: Received Target Abort Target Abort does not exist on the primary side of the PCI Express port. This bit is hardwired to 0.
11	RWC	0h	STA: Signaled Target Abort Target Abort does not exist on the primary side of the PCI Express port. This bit is hardwired to 0.
10:9	RO	0h	DEVSEL#: DEVSEL# Timing Not applicable to PCI Express. This bit is hardwired to 0.
8	RWC	0h	MDPERR: Master Data Parity Error This bit is set by the PCI Express port if the Parity Error Enable bit (PERRE) is set and it receives error T10 (uncorrectable data error or Address/Control parity errors or an internal failure). If the Parity Error Enable bit is cleared, this bit is never set. See Table 6-39 'Errors Detected by the NB' on page 328 of this document.
7	RO	0	FB2B: Fast Back-to-Back Not applicable to PCI Express. This bit is hardwired to 0.
6	RV	0	Reserved (by PCI SIG)

Device: 1 - 7 Function: 0 Offset: 06 - 07h			
Bit	Attr	Default	Description
5	RO	0	66MHZCAP: 66 MHz capable Not applicable to PCI Express. This bit is hardwired to 0.
4	RO	1	CAPL: Capabilities List This bit indicates the presence of PCI Express capabilities list structure in the PCI Express port. This bit is hardwired to 1(Mandatory).
3	RO	0	INTxSTAT: INTx Status Indicates that an INTx interrupt message is pending internally in the PCI Express port. This bit does not get set for interrupts forwarded up from downstream devices in the hierarchy or for messages converted to interrupts by the root port.
2:0	RV	00	Reserved (by PCI SIG)

4.11.5 RID[7:1]: Revision Identification Register (D1-7, F0)

This register contains the revision number of the Intel® E8501 chipset North Bridge (NB).

Device: 1 - 7 Function: 0 Offset: 08h			
Bit	Attr	Default	Description
7:4	RO	0h	Major_rev: Major Revision Steppings which require all masks to be regenerated. 1h : B stepping
3:0	RO	0	Minor_rev: Minor Revision Incremented for each stepping which does not modify all masks. Reset for each major revision. 0h: x0 stepping 1h: x1 stepping 2h: x2 stepping

4.11.6 CCR[7:1]: Class Code Register (D1-7, F0)

This register contains the Class Code for the device.

Device: 1 - 7 Function: 0 Offset: 09-0Bh			
Bit	Attr	Default	Description
23:16	RO	06h	BaseClass: Base Class This field indicates the general device category. For the NB, this field is hardwired to 06h, indicating it is a "Bridge Device".
15:8	RO	04h	SubClass: Sub-Class This field qualifies the Base Class, providing a more detailed specification of the device function. For PCI Express Devices 1,2,3,4,5,6,7 default is 040h, indicating "PCI to PCI Bridge".
7:0	RO	00h	RLPI: Register-Level Programming Interface This field identifies a specific programming interface (if any), that device independent software can use to interact with the device. There are no such interfaces defined for "Host Bridge" types, and this field is hardwired to 00h.

4.11.7 CLS[7:1]: Cache Line Size (D1-7, F0)

This register contains the Cache Line Size and is set by BIOS/Operating System. It does not affect the PCI Express port functionality in the NB.

Device: 1 - 7 Function: 0 Offset: 0Ch			
Bit	Attr	Default	Description
7:0	RW	00h	ClS: Cache Line Size (CLS) This is an 8-bit value that indicates the size of the cache line and is specified in DWORDs. It does not affect the NB.

4.11.8 PRI_LT[7:1]: Primary Latency Timer (D1-7, F0)

This register denotes the maximum timeslice for a burst transaction in legacy PCI 2.3 on the primary interface. It does not affect or influence PCI Express functionality.

Device: 1 - 7 Function: 0 Offset: 0Dh			
Bit	Attr	Default	Description
7:0	RO	00h	PLatTim: Primary Latency Timer Not applicable to PCI Express. Hardwired to 00h.

4.11.9 HDR[7:1]: Header Type Register (D1-7, F0)

This register identifies the header layout of the configuration space.

Device: 1 - 7 Function: 0 Offset: 0Eh			
Bit	Attr	Default	Description
7	RO	00h	Mfd: Multi-function Device. Selects whether this is a multi-function device, that may have alternative configuration layouts.
6:0	RO	01h	CfgLayout: Configuration Layout. This field identifies the format of the configuration header layout for a PCI-to-PCI bridge from bytes 10h through 3Fh. For PCI Express Devices 1,2,3,4,5,6,7 default is 01h, indicating "PCI to PCI Bridge".

4.11.10 BIST[7:1]: Built-In Self Test (D1-7, F0)

This register is used for reporting control and status information of BIST checks within a PCI Express port. It is not supported in the NB.

Device: 1 - 7 Function: 0 Offset: 0Fh			
Bit	Attr	Default	Description
7:0	RO	00h	Btest: BIST Tests Not supported. Hardwired to 00h

4.11.11 PBUSN[7:1]: Primary Bus Number (D1-7, F0)

This register identifies that "virtual" PCI-PCI bridge is connected to bus #0.

Device: 1 - 7 Function: 0 Offset: 18h			
Bit	Attr	Default	Description
7:0	RO	00h	PBUSN: Primary Bus Number Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since the PCI Express virtual PCI-PCI bridge is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 00h.

4.11.12 SBUSN[7:1]: Secondary Bus Number (D1-7, F0)

This register identifies the bus number assigned to the secondary side of the “virtual” PCI-PCI bridge (the PCI Express connection). This number is programmed by the PCI configuration software to allow mapping of configuration cycles to a second bridge device connected to PCI Express.

Device: 1 - 7 Function: 0 Offset: 19h			
Bit	Attr	Default	Description
7:0	RW	0h	BUSN: Secondary Bus Number This field is programmed by configuration software with the lowest bus number of the buses connected to PCI Express. Since both bus 0, device (1 - 7) and the PCI-PCI bridge on the other end are considered by configuration software to be PCI-PCI bridges, this bus number will always correspond to the bus number assigned to PCI Express.

4.11.13 SUBUSN[7:1]: Subordinate Bus Number (D1-7, F0)

This register identifies the subordinate bus (if any) that resides at the level below the secondary PCI Express interface. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to devices subordinate to the secondary PCI Express port.

Device: 1 - 7 Function: 0 Offset: 1Ah			
Bit	Attr	Default	Description
7:0	RW	0h	SUBUSN: Subordinate Bus Number This register is programmed by configuration software with the number of the highest subordinate bus that is behind the PCI Express port.

4.11.14 SEC_LT[7:1]: Secondary Latency Timer (D1-7, F0)

This register denotes the maximum time-slice for a burst transaction in legacy PCI 2.3 on the secondary interface. It does not affect or influence PCI Express functionality.

Device: 1 - 7 Function: 0 Offset: 1Bh			
Bit	Attr	Default	Description
7:0	RO	00h	SEC_LT: Secondary Latency Timer Not applicable to PCI Express. Hardwired to 00h.

4.11.15 IOBASE[7:1]: I/O Base Register (D1-7, F0)

The I/O Base and I/O Limit (Section 4.11.16) registers define an address range that is used by the PCI Express bridge to determine when to forward I/O transactions from one interface to the other using the following formula:

$$IO_BASE \leq A[15:12] \leq IO_LIMIT$$

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. The bottom of the defined I/O address range will be aligned to a 4KB boundary while the top of the region specified by IO_LIMIT will be *one less than a 4 KB multiple*.

Note: If IOLIM < IOBASE, then the aperture is closed.

Device: 1 - 7 Function: 0 Offset: 1Ch			
Bit	Attr	Default	Description
7:4	RW	00h	IOBASE: I/O Base Address Corresponds to A[15:12] of the I/O addresses passed by the PCI Express device.
3:0	RO	00h	IOCAP: I/O Address Capability 0h: 16-bit I/O addressing (supported) Others: <i>Reserved</i> NOTE: The NB only supports 16-bit I/O addressing. These bits are hardwired to 00h.

4.11.16 IOLIM[7:1]: I/O Limit Register (D1-7, F0)

The I/O Base and I/O Limit registers define an address range that is used by the PCI Express bridge to determine when to forward I/O transactions from one interface to the other using the following formula:

$$IO_BASE \leq A[15:12] \leq IO_LIMIT$$

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] of the I/O limit register is treated as FFFh.

Device: 1 - 7 Function: 0 Offset: 1Dh			
Bit	Attr	Default	Description
7:4	RW	00h	I/O Address Limit (IOLIMIT) - Corresponds to A[15:12] of the I/O addresses passed by the PCI Express device.
3:0	RO	00h	I/O Address Limit Capability (IOLCAP) 0h: 16-bit I/O addressing (supported) Others: <i>Reserved</i> NOTE: The NB only supports 16-bit I/O addressing. These bits are hardwired to 00h.

4.11.17 SECSTS[7:1]: Secondary Status (D1-7, F0)

SECSTS is a 16-bit status register that reports the occurrence of error conditions associated with the secondary side (i.e. PCI Express side) of the “virtual” PCI-PCI bridge embedded within the NB.

Device: 1 - 7 Function: 0 Offset: 1Eh - 1Fh			
Bit	Attr	Default	Description
15	RWC	0h	SDPE: Detected Parity Error This bit is set by the NB whenever it receives a poisoned TLP in the PCI Express port regardless of the state of the Parity Error Response bit. This corresponds to IO14 as defined in Table 6-39 “Errors Detected by the NB” on page 328 of this document.
14	RWC	0h	SRSE: Received System Error This bit is set by the NB when it receives a ERR_FATAL or ERR_NONFATAL message, and the BCSERRE bit is set in BCTRL register (Section 4.11.27). This corresponds to IO24, IO25 and IO26 as defined in Table 6-39 “Errors Detected by the NB” on page 328 of this document.
13	RWC	0h	SRMAS: Received Master Abort Status This bit is set when the PCI Express port receives a Completion with “Unsupported Request Completion” Status. This corresponds to IO12 as defined in Table 6-39 “Errors Detected by the NB” on page 328 of this document.
12	RWC	0h	SRTAS: Received Target Abort Status This bit is set when the PCI Express port receives a Completion with “Completer Abort” Status. This corresponds to IO17 as defined in Table 6-39 “Errors Detected by the NB” on page 328 of this document.
11	RWC	0h	SSTAS: Signaled Target Abort This bit is set when the PCI Express port completes a request with “Completer Abort” Status. The NB never generates completer aborts internally, therefore this bit is never set.
10:9	RO	00h	SDEVT: DEVSEL# Timing Not applicable to PCI Express. Hardwired to 00h.
8	RWC	0h	SMDPERR: Master Data Parity Error This bit is set by the PCI Express port on the secondary side (PCI Express link) if the Parity Error Response bit (PERRE) is set and either of the following two conditions occurs: - The PCI Express port receives a completion marked poisoned - The PCI Express port poisons a write request If the Parity Error Response bit is cleared, this bit is never set.
7	RO	0h	SFB2BTC: Fast Back-to-Back Transactions Capable Not applicable to PCI Express. Hardwired to 00h.
6	RV	0h	Reserved (by PCI SIG)
5	RO	0h	S66MHCAP: 66 MHz Capability Not applicable to PCI Express. Hardwired to 00h.
4:0	RV	00h	Reserved (by PCI SIG)

4.11.18 MBASE[7:1]: Memory Base (D1-7, F0)

The Memory Base and Memory Limit registers define a memory mapped I/O non-prefetchable address range (32-bit addresses) and the NB directs accesses in this range to the PCI Express port based on the following formula:

$$\text{MEMORY_BASE} \leq A[31:20] \leq \text{MEMORY_LIMIT}$$

The upper 12 bits of both the Memory Base and Memory Limit registers are read/write and corresponds to the upper 12 address bits, A[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, A[19:0], of the memory base address are 00000h. Similarly, the bridge assumes that the lower 20 address bits, A[19:0], of the memory limit address (not implemented in the Memory Limit register) are FFFFFh. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary and the top of the defined memory address range will be one less than a 1 MB boundary.

Note: If MLIMIT < MBASE, then the aperture is closed.

Device: 1 - 7 Function: 0 Offset: 20h - 21h			
Bit	Attr	Default	Description
15:4	RW	0h	MBASE: Memory Base Address Corresponds to A[31:20] of the memory address on the PCI Express port.
3:0	RO	0h	Reserved (by PCI SIG)

4.11.19 MLIMIT[7:1]: Memory Limit (D1-7, F0)

This register controls the processor to PCI Express non-prefetchable memory access routing based on the following formula as described above:

$$\text{MEMORY_BASE} \leq A[31:20] \leq \text{MEMORY_LIMIT}$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32-bit address. The bottom 4 bits of this register are read-only and return 0h when read. This register must be initialized by the configuration software. For the purpose of address decode, address bits A[19:0] are assumed to be FFFFFh.

Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express address ranges (typically where control/status memory-mapped I/O data structures reside). PMBASE and PMLIMIT are used to map prefetchable address ranges.

Note also that configuration software is responsible for programming all address range registers (prefetchable and non-prefetchable) with the values that provide exclusive address ranges (i.e. prevent overlap with each other and/or with the ranges covered with the main memory). There is no provision in the NB hardware to enforce prevention of overlap. Operations of the system in the case of overlap are not guaranteed.

Device: 1 - 7 Function: 0 Offset: 22h - 23h			
Bit	Attr	Default	Description
15:4	RW	0h	MLIMIT: Memory Limit Address Corresponds to A[31:20] of the memory address that corresponds to the upper limit of the range of memory accesses that will be passed by the PCI Express bridge.
3:0	RO	0h	Reserved (by PCI SIG)

4.11.20 PMBASE[7:1]: Prefetchable Memory Base (D1-7, F0)

The Prefetchable Memory Base and Memory Limit registers define a memory mapped I/O prefetchable address range (32-bit addresses) which is used by the PCI Express bridge to determine when to forward memory transactions from one interface to the other based on the following formula:

$$\text{PREFETCH_MEMORY_BASE} \leq \text{A}[31:20] \leq \text{PREFETCH_MEMORY_LIMIT}$$

The upper 12 bits of both the Prefetchable Memory Base and Memory Limit registers are read/write and corresponds to the upper 12 address bits, A[31:20], of 32-bit addresses. For the purpose of address decoding, the bridge assumes that the lower 20 address bits, A[19:0], of the memory base address are 00000h. Similarly, the bridge assumes that the lower 20 address bits, A[19:0], of the memory limit address (not implemented in the Memory Limit register) are FFFFFh. Thus, the bottom of the defined memory address range will be aligned to a 1 MB boundary and the top of the defined memory address range will be one less than a 1 MB boundary.

Note: If PMLIMIT < PMBASE, then the aperture is closed.

Device: 1 - 7 Function: 0 Offset: 24h - 25h			
Bit	Attr	Default	Description
15:4	RW	00h	PMBASE: Prefetchable Memory Base Address Corresponds to A[31:20] of the prefetchable memory address on the PCI Express port.
3:0	RO	01h	PMBASE_CAP: Prefetchable Memory Base Address Capability 00h: 32-bit Prefetchable Memory addressing 01h: 64-bit Prefetchable Memory addressing Others: <i>Reserved</i>

The bottom 4 bits of both the Prefetchable Memory Base and Prefetchable Memory Limit registers are read-only, contain the same value, and encode whether or not the bridge supports 64-bit addresses. If these four bits have the value 0h, then the bridge supports only 32 bit addresses. If these four bits have the value 01h, then the bridge supports 64-bit addresses and the Prefetchable Base Upper 32 Bits and Prefetchable Limit Upper 32 Bits registers hold the rest of the 64-bit prefetchable base and limit addresses respectively.