

4.11.21 PMLIMIT[7:1]: Prefetchable Memory Limit (D1-7, F0)

This register controls the processor to PCI Express prefetchable memory access routing based on the following formula as described above:

$$\text{extPMBASE}[n] = (\text{PMBU}[n] \ll 32) \mid \text{PMBASE}[n].\text{PMBASE}$$

$$\text{extPMLIM}[n] = (\text{PMLU}[n] \ll 32) \mid \text{PMLIMIT}[n].\text{PMBASE}$$

$$\text{extPMBASE}[n] \leq \text{zero_extend}(A[39:20]) \leq \text{extPMLIM}[n]$$

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFh.

Device: 1 - 7 Function: 0 Offset: 26h - 27h			
Bit	Attr	Default	Description
15:4	RW	0h	PMLIMIT: Prefetchable Memory Limit Address Corresponds to A[31:20] of the memory address that corresponds to the upper limit of the prefetchable range of memory accesses that will be passed by the PCI Express bridge.
3:0	RO	1h	PMLIMIT_CAP: Prefetchable Memory Limit Address Capability 00h: 32-bit Prefetchable Memory addressing 01h: 64-bit Prefetchable Memory addressing Others: <i>Reserved</i>

4.11.22 PMBU[7:1]: Prefetchable Memory Base (Upper 32 bits) (D1-7, F0)

The Prefetchable Base Upper 32 Bits is the extension to the Prefetchable Memory Base register. It concatenate with the PMLIMIT address fields to build a full address.

Device: 1 - 7 Function: 0 Offset: 28h - 2Bh			
Bit	Attr	Default	Description
31:0	RW	0h	PUMBASE: Prefetchable Upper 32-bit Memory Base Address A[63:32] of the memory address that corresponds to the upper base of the prefetchable range of memory accesses that will be passed by the PCI Express bridge. The operating system (OS) should program these bits based on the available physical limits of the system.

4.11.23 PMLU[7:1]: Prefetchable Memory Limit (Upper 32 Limit) (D1-7, F0)

The Prefetchable Limit Upper 32 Bits registers is the extension to the Prefetchable Memory Limit register. It concatenate with the PMBASE address fields to build a full address.

Device: 1 - 7 Function: 0 Offset: 2Ch - 2Fh			
Bit	Attr	Default	Description
31:0	RW	0h	PUMLIM: Prefetchable Upper 32-bit Memory Limit Address A[63:32] of the memory address that corresponds to the upper limit of the prefetchable range of memory accesses that will be passed by the PCI Express bridge. The operating system (OS) should program these bits based on the available physical limits of the system.

4.11.24 CAPPTR[7:1]: Capability Pointer (D1-7, F0)

The CAPPTR is used to point to a linked list of additional capabilities implemented by this device.

It provides the offset to the first set of capabilities registers located in the PCI-compatible space from 40h. Currently, the first structure is located at 50h to provide room for other registers.

Device: 1 - 7 Function: 0 Offset: 34h			
Bit	Attr	Default	Description
7:0	RO	50h	CAPPTR: Capability Pointer Points to the first capability structure (PM) in PCI 2.3 compatible space at 50h.

4.11.25 INTL[7:1]: Interrupt Line Register (D1-7, F0)

The Interrupt Line register is used to communicate interrupt line routing information between initialization code and the device driver. The NB does not have a dedicated interrupt line and is not used.

Device: 1 - 7 Function: 0 Offset: 3Ch			
Bit	Attr	Default	Description
7:0	RO	00h	INTL: Interrupt Line BIOS writes the interrupt routing information to this register to indicate which input of the interrupt controller this PCI Express Port is connected to. Not used in the NB since the PCI Express port does not have interrupt lines.

4.11.26 INTP[7:1]: Interrupt Pin Register (D1-7, F0)

The INTP register identifies legacy interrupts for INTA, INTB, INTC and INTD. These features are not supported by the NB.

Device: 1 - 7 Function: 0 Offset: 3Dh			
Bit	Attr	Default	Description
7:0	RO	00h	Interrupt Pin (INTP) Set to '00h' to indicate no interrupt pins.

4.11.27 BCTRL[7:1]: Bridge Control Register (D1-7, F0)

This register provides extensions to the EXP_CMD register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e. PCI Express) as well as some bits that affect the overall behavior of the “virtual” PCI-PCI bridge embedded within the NB (e.g. VGA compatible address range mapping).

Device: 1 - 7 Function: 0 Offset: 3Eh - 3Fh			
Bit	Attr	Default	Description
15:12	RV	00h	<i>Reserved.</i> (by PCI SIG)
11	RO	0h	DTSS: Discard Timer SERR Status Not applicable to PCI Express. This bit is hardwired to 0h.
10	RO	0h	DTS: Discard Timer Status Not applicable to PCI Express. This bit is hardwired to 0h.
9	RO	0h	SDT: Secondary Discard Timer Not applicable to PCI Express. This bit is hardwired to 0h.
8	RO	0h	PDT: Primary Discard Timer Not applicable to PCI Express. This bit is hardwired to 0h.
7	RO	0h	FB2BEN: Fast Back-to-Back Enable Not applicable to PCI Express. This bit is hardwired to 0h.
6	RW	0h	SRESET: Secondary Bus Reset Setting this bit triggers a warm reset on the corresponding PCI Express port and the PCI Express hierarchy domain subordinate to the port.
5	RO	0h	MAMODE: Master Abort Mode Not applicable to PCI Express. This bit is hardwired to 0h.
4	RV	0h	<i>Reserved</i> (by PCI SIG)

Device: 1 - 7 Function: 0 Offset: 3Eh - 3Fh			
Bit	Attr	Default	Description
3	RW	0h	VGAEN: VGA Enable Controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. This bit may only be set for one PCI Express port.
2	RW	0h	ISAEN: ISA Enable Modifies the response by the NB to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 1h: The NB will not forward to PCI Express any I/O transactions addressing the last 768 bytes in each 1 KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express these cycles will be forwarded to HIO where they can be subtractively or positively claimed by the ISA bridge. 0h: All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to PCI Express.
1	RW	0h	BCSERRE: SERR Enable This bit controls forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL messages from the PCI Express port to the primary side. 1h: Enables forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL messages 0h: Disables forwarding of ERR_COR, ERR_NONFATAL and ERR_FATAL messages
0	RW	0h	PRSPEN: Parity Error Response Enable This bit controls the response to poisoned TLPs in the PCI Express port 1h: Enables reporting of poisoned TLP errors. 0h: Disables reporting of poisoned TLP errors.

4.11.28 EXP_CTRL[7:1]: PCI Express Control Register (D1-7, F0)

This 32-bit register implements the chipset-specific operations for general control/accessibility such as device hiding, selective configuration cycles, interrupt signaling and MSI generation.

Device: 1 - 7 Function: 0 Offset: 48h - 4Bh			
Bit	Attr	Default	Description
31:30	RV	0	Reserved
29	RW	0	DISABLE ABP When set prevents bit 0 ABP: Attention Button Pressed in Section 4.11.47 "EXP_SLOTSTS[7:1]: PCI Express Slot Status Register (D1-7, F0)" from getting set. Suggested value: 1
28	RV	0	Reserved
27	RW	0	DIS_TOGGLE_POP_PRI
26	RW	0	READ_INTERLOCK: Cards that violate PCI ordering rules and have a read-to-read in-out dependency must set this bit to avoid deadlock during locks. The dependency is a card that expects the NB to provide completion for its upstream read before it can process a downstream read from the NB. Such cards must not participate in peer-to-peer transactions. Since the default is 0, it assumes that cards follow PCI ordering rules fully.
25:24	RW	3h	COALESCE_MODE: Used to increase the amount of combining for completions. X 1: #CPL_ENTRIES_FREE will restrict coalesce_hint 1 X: f set then #PF_PEND will restrict coalesce hint 0 0: Least restrictive Suggested value: 00h
23	RW	0	TIMEOUT_ENABLE_CFG: 1: Config transactions can time out 0: Config transactions cannot time out Suggested value: 0h
22	RW	1h	TIMEOUT_ENABLE: 1: Non config transactions can time out 0: Non config transactions cannot time out. Suggested value: 1h
21	RW	1h	MALTLP_EN: 1: Check for certain malformed TLP types 0: Do not check for certain malformed TLP types
20	RW	0h	DZLCW: Drop zero length config writes Suggested value: 0h

Device: 1 - 7 Function: 0 Offset: 48h - 4Bh			
Bit	Attr	Default	Description
19	RW	0h	DZLIW: Drop zero length I/O writes Suggested value: 0h
18	RW	0h	DZLMW: Drop zero length memory writes Suggested value: 0h
17	RW	0h	DZLCR: Drop zero length config reads Suggested value: 0h
16	RW	0h	DZLIR: Drop zero length I/O reads Suggested value: 0h
15	RW	0h	DZLMR: Drop zero length memory reads Suggested value: 0h
14	RW	1h	STREAM_INTERLEAVE_CHECK_EN: 1: Not supported 0: Do not check for stream interleaving Suggested value: 0h
13	RW	1h	INTERLEAVE_EN: 1: Interleaved 0: Not interleaved Suggested value: 1h
12	RW	1h	256B_EN: 1: Increases likelihood of 256B return when COALESCE_EN = 1 0: Decreases likelihood of 256B return when COALESCE_EN = 1 Suggested value: 1h
11	RW	0h	CF: Force coalescing of accesses When 1, forces the NB to wait for all coalescable data before sending the transaction as opposed to forwarding as much as possible. Suggested value: 0h
10	RW	1h	COALESCE_EN: When 1, enables read return of >64B 1: Returns of >64B enabled. See 256B_EN 0: Returns are 64B or less Suggested value: 1h

Device: 1-7 Function: 0 Offset: 48h-4Bh			
Bit	Attr	Default	Description
9	RW	0h	MSIPMEN: MSI PME Enable 1: Enables MSI messages to be sent to the CPU for PME events. 0: Disables sending of MSI messages to the CPU for PME events Note that for MSI PME messages to be sent, both MSIPMEN and at least one of MSICTRL[7:1] MSIEN bits have to be set.
8	RW	0h	MSIHPEN: MSI Hot-Plug Enable 1: Enables MSI messages to be sent to the CPU for Hot-plug events and enables signaling hot plug events on the EXP_HPINT pin. 0: Disables sending of MSI messages for Hot-plug events to the CPU Note that for MSI Hot-plug messages to be sent, both MSIHPEN and at least one of MSICTRL[7:1] MSIEN bits defined in Section 4.11.34 have to be set.
7	RWO	0h	DIS_INB_CFG: Disable Inbound Configurations This bit is used for controlling configuration accesses to the chipset registers through the PCI Express device. 1: Inbound accesses to the NB or XMB registers will be master aborted 0: Allows access to the NB or XMB registers. (typically for internal debug, test, etc.) This register bit is of type "write once" and is controlled by BIOS/special initialization firmware.
6:3	RW	00h	VPP: Virtual Pin Port [6:4] = SMBus Address, [3] = IO Port defines the 8-bit IO port that is used for routing power, attention, Hot-Plug, presence, MRL and other events defined in Table 6-34.
2	RW	0h	EN_VPP: Enable VPP The NB will use this bit to decide whether VPP is enabled or disabled for the given PCI Express port as set by configuration software. For example, to distinguish Hot-Plug events for a legacy card or PCI Express module, this bit can be used. 1: VPP is enabled for this PCI Express port 0: VPP is disabled for this PCI Express port
1	RW	0h	DIS_APIC_EOI: Disable APIC EOI The NB will use this bit to decide whether end of interrupts (EOI) need to be sent to an APIC controller/bridge (e.g. PXH) through this PCI Express device 1: No EOIs are sent (disabled). Should be set by BIOS if link never came up. 0: EOIs are dispatched to the APIC Controller Suggested Value: 1 Unless an Intel device is attached.
0	RV	0h	Reserved

4.11.29 EXP_CTRL2: PCI Express Control Register 2 (D1-7, F0)

Device: 1 - 7 Function: 0 Offset: 4Ch			
Bit	Attr	Default	Description
7:1	RV	00h	Reserved
0	RW	0	NO_COMPLIANCE: Set by software to enable link operation in the presence of single wire failures on the link. If clear, then specified link behavior in the presence of a wire failure will be Polling. Suggested value: 1h

4.11.30 PMCAP[7:1]: Power Management Capabilities Register (D1-7, F0)

The PM Capabilities Register defines the capability ID, next pointer and other power management related support. The following PM registers /capabilities are added for software compliance.

Device: 1 - 7
Function: 0
Offset: 50h - 53h

Bit	Attr	Default	Description																																				
31:27	RO	11001b	PMES: PME Support Identifies power states which asserts PME_OUT. Bits 31, 30 and 27 must be set to '1' for PCI-PCI bridge structures representing ports on root complexes. The definition of these bits is taken from the PCI Bus Power Management Interface Specification Revision 1.1. <table><tr><th>Bit 31</th><th>Bit 30</th><th>Bit 29</th><th>Bit 28</th><th>Bit 27</th><th>PME_OUT</th></tr><tr><td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>PME_OUT can be asserted from D0</td></tr><tr><td>X</td><td>X</td><td>X</td><td>1</td><td>X</td><td>PME_OUT can be asserted from D1 (Not supported by the NB)</td></tr><tr><td>X</td><td>X</td><td>1</td><td>X</td><td>X</td><td>PME_OUT can be asserted from D2 (Not supported by the NB)</td></tr><tr><td>X</td><td>1</td><td>X</td><td>X</td><td>X</td><td>PME_OUT can be asserted from D3 hot (Not supported by the NB)</td></tr><tr><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>PME_OUT can be asserted from D3 cold (Not supported by the NB)</td></tr></table>	Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	PME_OUT	X	X	X	X	1	PME_OUT can be asserted from D0	X	X	X	1	X	PME_OUT can be asserted from D1 (Not supported by the NB)	X	X	1	X	X	PME_OUT can be asserted from D2 (Not supported by the NB)	X	1	X	X	X	PME_OUT can be asserted from D3 hot (Not supported by the NB)	1	X	X	X	X	PME_OUT can be asserted from D3 cold (Not supported by the NB)
Bit 31	Bit 30	Bit 29	Bit 28	Bit 27	PME_OUT																																		
X	X	X	X	1	PME_OUT can be asserted from D0																																		
X	X	X	1	X	PME_OUT can be asserted from D1 (Not supported by the NB)																																		
X	X	1	X	X	PME_OUT can be asserted from D2 (Not supported by the NB)																																		
X	1	X	X	X	PME_OUT can be asserted from D3 hot (Not supported by the NB)																																		
1	X	X	X	X	PME_OUT can be asserted from D3 cold (Not supported by the NB)																																		
26	RO	0h	D2S: D2 Support The NB does not support power management state D2.																																				
25	RO	0h	D1S: D1 Support The NB does not support power management state D1.																																				
24:22	RO	0h	AUXCUR: AUX Current																																				
21	RO	0h	DSI: Device Specific Initialization																																				

Device: 1 - 7 Function: 0 Offset: 50h - 53h			
Bit	Attr	Default	Description
20	RV	0h	Reserved
19	RO	0h	PMECLK: PME Clock This field is hardwired to 0h as it does not apply to PCI Express.
18:16	RO	010b	VER: Version This field is set to '010b' as version number from the PCI Express 1.0 specification.
15:8	RO	58h	NXTCAPPTR: Next Capability Pointer This field is set to offset 58h for the next capability structure (MSI) in the PCI 2.3 compatible space.
7:0	RO	01h	CAPID: Capability ID Provides the PM capability ID assigned by PCI-SIG.

4.11.31 PMSCR[7:1]: Power Management Status and Control Register (D1-7, F0)

This register provides status and control information for PM events in the PCI Express ports of the NB.

Device: 1 - 7 Function: 0 Offset: 54h - 57h			
Bit	Attr	Default	Description
31:24	RO	0h	Data: Data Data read out based on data select (DSEL).
23	RO	0h	BPCCEN: Bus Power/Clock Control Enable This field is hardwired to 0h as it does not apply to PCI Express.
22	RO	0h	B2B3S: B2/B3 Support This field is hardwired to 0h as it does not apply to PCI Express.
21:16	RV	0h	Reserved
15	RWCST	0h	PMESTS: PME Status This PME Status is a sticky bit. When set, the PCI Express port generates a PME internally independent of the PMEEN bit defined below. Software clears this bit by writing a '1'. As a root port, the NB will never set this bit, because it never generates a PME internally independent of the PMEEN bit.
14:13	RO	0h	DSCL: Data Scale
12:9	RW	0h	DSEL: Data Select
8	RWST	0h	PMEEN: PME Enable This field, when set enables forwarding of PME messages received at the PCI Express port to the NB core.
7:2	RV	0h	Reserved
1:0	RW	0h	PS: Power State

4.11.32 MSICAPID[7:1]: MSI Capability ID (D1-7, F0)

Message Signaled Interrupts (MSI) is an optional feature that enables a device to request service by writing a system-specified message to a system-specified address in the form of an interrupt message. The transaction address (e.g. FEEx_xxxxh) specifies the message destination and the transaction data specifies the message. The MSI mechanism is supported by the following registers: MSICAPID, MSINXPTR, MSICTRL, MSIAR and MSIDR described below.

Device: 1 - 7 Function: 0 Offset: 58h			
Bit	Attr	Default	Description
7:0	RO	05h	CAPID: Capability ID Assigned by PCI-SIG for message signaling capability.

4.11.33 MSINXPTR[7:1]: MSI Next Pointer (D1-7, F0)

Device: 1 - 7 Function: 0 Offset: 59h			
Bit	Attr	Default	Description
7:0	RO	6Ch	NXTPTR: Next Ptr This field is set to 6Ch for the next capability list (PCI Express capability structure - EXP_CAP) in the chain.

4.11.34 MSICTRL[7:1]: Message Control Register (D1-7, F0)

Device: 1 - 7 Function: 0 Offset: 5Ah - 5Bh			
Bit	Attr	Default	Description
15:8	RV	0h	Reserved

Device: 1 - 7 Function: 0 Offset: 5Ah - 5Bh			
Bit	Attr	Default	Description
7	RO	0h	AD64CAP: 64-bit Address Capable This field is hardwired to 0h since the message writes addresses are only 32-bit addresses (e.g. FEEx_xxxxh).
6:4	RW	0h	MMEN: Multiple Message Enable Software writes to this field to indicate the number of allocated messages which is aligned to a power of two. When MSI is enabled, the software will allocate at least one message to the device. If two MSI messages are enabled, "message 0" is used for normal interrupts and "message 1" is used for abort/error interrupts. If only one MSI message is enabled, "message 0" is used for both normal and error interrupts.
3:1	RO	001	MMCAP: Multiple Message Capable Software reads this field to determine the number of requested messages that are aligned to a power of two. It is set to 2 messages (encoding of 001).
0	RW	0h	MSIEN: MSI Enable The software sets this bit to select legacy interrupts or transmit MSI messages: 0 The NB will not use MSI to communicate an event to the processor. 1 Enables the NB to use MSI messages to request context specific service through register bits defined in the Section 4.11.28, "EXP_CTRL[7:1] PCI Express Control Register (D1-7 F0)" on page 102.

4.11.35 MSIAR[7:1]: MSI Address Register (D1-7, F0)

The MSI Address Register (MSIAR) contains the system specific address information to route MSI interrupts and is broken into its constituent fields.

Device: 1 - 7 Function: 0 Offset: 5Ch - 5Fh			
Bit	Attr	Default	Description
31:20	RW	FEh	AMSB: Address MSB This field specifies the 12 most significant bits of the 32-bit MSI address.
19:12	RW	00h	ADSTID: Address Destination ID This field is initialized by software for routing the interrupts to the appropriate destination.

Device: 1 - 7 Function: 0 Offset: 5Ch - 5Fh			
Bit	Attr	Default	Description
11:4	RW	00h	AEXDSTID: Address Extended Destination ID This field is not used by IA-32 processor.
3	RW	0h	ARDHINT: Address Redirection Hint 0: Directed 1: Redirectable
2	RW	0h	ADM: Address Destination Mode 0: Physical 1: Logical
1:0	RV	0h	Reserved

4.11.36 MSIDR[7:1]: MSI Data Register (D1-7, F0)

The MSI Data Register (MSIDR) contains all the data-related information to route MSI interrupts.

Device: 1 - 7 Function: 0 Offset: 60h - 63h			
Bit	Attr	Default	Description
31:16	RV	00h	Reserved
15	RW	0h	TM: Trigger Mode 0: Edge 1: Level This field Specifies the type of trigger operation
14	RW	0h	LVL: Level If TM is 0h, then this field is a don't care. Edge triggered messages are always treated as assert messages. For level triggered interrupts, this bit reflects the state of the interrupt input if TM is 1h, then 0: Deassert Messages 1: Assert Messages
13:11	RW	0h	These bits are don't care in IOxAPIC interrupt message data field specification.

Device: 1 - 7 Function: 0 Offset: 60h - 63h			
Bit	Attr	Default	Description
10:8	RW	0h	DM: Delivery Mode 000: Fixed 001: Lowest Priority 010: SMI/PMI 011: <i>Reserved</i> 100: NMI 101: INIT 110: <i>Reserved</i> 111: ExtINT
7:0	RW	0h	IV: Interrupt Vector

4.11.37 EXP_CAPL[7:1]: PCI Express Capability List Register (D1-7, F0)

The PCI Express capability structure describes PCI Express related functionality, identification and other information such as control/status associated with the ports. It is located in the PCI 2.3-Compatible space and supports legacy operating system by enabling PCI software transparent features.

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 2.3 configuration space.

Device: 1 - 7 Function: 0 Offset: 6Ch - 6Dh			
Bit	Attr	Default	Description
15:8	RO	00h	NXTCAPPTR: Next Capability Pointer This field is set to NULL (00h) as there is no new structure defined from the current PCI Express capability list (i.e. last in the link list of PCI 2.3 compatible space).
7:0	RO	10h	CAPID: Capability ID Provides the PCI Express capability ID assigned by PCI-SIG.

4.11.38 EXP_CAP[7:1]: PCI Express Capabilities Register (D1-7, F0)

The PCI Express Capabilities register identifies the PCI Express device type and associated capabilities.

Device: 1 - 7 Function: 0 Offset: 6Eh - 6Fh			
Bit	Attr	Default	Description
15:14	RV	0h	Reserved
13:9	RO	00h	IMN: Interrupt Message Number This field indicates the interrupt message number that is generated from the PCI Express port. When there are more than one MSI interrupt Number, this register field is required to contain the offset between the base Message Data and the MSI Message that is generated when the status bits in the slot status register or root port status registers are set.
8	RWO	0h	SLOT: Slot Implemented 0: Indicates that the PCI Express link associated with the port is connected to a non-removable device or is disabled. 1: Indicates that the PCI Express link associated with the port is connected to a slot. This register bit is of type "write once" and is controlled by BIOS/special initialization firmware.
7:4	RO	0100b	DPT: Device/Port Type This field identifies the type of device. It is set to 0100b as defined in the spec since the PCI Express port is a "root port" in the NB.
3:0	RO	0001b	VERS: Capability Version This field identifies the version of the PCI Express capability structure. Set to 0001 by PCI SIG.

4.11.39 EXP_DEVCAP[7:1]: PCI Express Device Capabilities Register (D1-7, F0)

The PCI Express Device Capabilities register identifies PCI Express specific capabilities with this port.

Device: 1 - 7 Function: 0 Offset: 70h - 73h			
Bit	Attr	Default	Description
31:28	RV	0h	Reserved
27:26	RO	0h	CSPLS: Captured Slot Power Limit Scale Specifies the scale used for the Slot Power Limit Value. It does not apply to the NB as it is a Root complex. Hardwired to 0h.

Device: 1 - 7 Function: 0 Offset: 70h - 73h			
Bit	Attr	Default	Description
25:18	RO	00h	CSPLV: Captured Slot Power Limit Value This field specifies upper limit on power supplied by a slot in an upstream port. It does not apply to the NB as it is a Root complex. Hardwired to 00h.
17:15	RV	0h	Reserved
14	RO	0h	PIPD: Power Indicator Present on Device When set, this bit indicates that a Power Indicator is implemented. 0: PIPD is disabled in the NB 1: <i>Reserved</i>
13	RO	0h	AIPD: Attention Indicator Present When set, this bit indicates that an Attention Indicator is implemented. 0: AIPD is disabled in the NB 1: <i>Reserved</i>
12	RO	0h	ABPD: Attention Button Present This bit when set indicates that an Attention Button is implemented. 0: ABPD is disabled in the NB 1: <i>Reserved</i>
11:9	RO	111	EPL1AL: Endpoints L1 Acceptable Latency This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L1 state to the L0 state. 000: Less than 1 μ s 001: 1 μ s to less than 2 μ s 010: 2 μ s to less than 4 μ s 011: 4 μ s to less than 8 μ s 100: 8 μ s to less than 16 μ s 101: 16 μ s to less than 32 μ s 110: 32 μ s to 64 μ s 111: More than 64 μs NOTE: The NB does not support L1 acceptable latency and is set to the maximum value for safety.

Device: 1 - 7 Function: 0 Offset: 70h - 73h			
Bit	Attr	Default	Description
8:6	RO	111b	EPL0AL: Endpoints L0s Acceptable Latency This field indicates the acceptable latency that an Endpoint can withstand due to the transition from L0s state to the L0 state. 000: Less than 64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 μ s 101: 1 μ s to less than 2 μ s 110: 2 μ s to 4 μ s 111: More than 4 μs NOTE: The NB does not support L0s implementation and for safety, this field is set to the maximum value.
5	RO	0h	ETFS: Extended Tag Field Supported This field indicates the maximum supported size of the Tag field. 0: For root ports such as the NB, only 5-bit Tag field is supported 1: <i>Reserved</i>
4:3	RO	0h	PFS: Phantom Functions Supported This field indicates the number of most significant bits of the function number portion of Requester ID in a TLP that are logically combined with the Tag identifier. 0: For root ports, no function number bits for phantom functions are supported 1: <i>Reserved</i>
2:0	RO	001b	MPLSS: Max Payload Size Supported This field indicates the maximum payload size that the PCI Express* port can support for TLPs. Defined encodings are: 000: 128B max payload size 001: 256B max payload size Others: <i>Reserved</i> NOTE: The NB only supports up to a maximum of 256B payload (e.g. writes and read completions) for each TLP and violations will be flagged as PCI Express errors.

4.11.40 EXP_DEVCTRL[7:1]: PCI Express Device Control Register (D1-7, F0)

The PCI Express Device Control register controls PCI Express specific capabilities parameters associated with this port.

Device: 1 - 7 Function: 0 Offset: 74h - 75h			
Bit	Attr	Default	Description
15	RV	0h	Reserved
14:12	RW	101b	MRRS: Max_Read_Request_Size This field sets maximum Read Request size generated by the NB. The PCI Express port must not generate read requests with size exceeding the set value. 000: 128B max read request size 001: 256B max read request size 010: 512B max read request size 011: 1024B max read request size 100: 2048B max read request size 101: 4096B max read request size 110: Reserved 111: Reserved
11	RW	1h	ENNOSNP: Enable No Snoop When set, the PCI Express port is permitted to set the "No Snoop bit" in the Requester Attributes of transactions it initiates that do not require hardware enforced cache coherency. Typically the "No Snoop bit" is set by an originating PCI Express device down in the hierarchy. The NB never sets or modifies the "No snoop bit" in the received TLP even if ENNOSNP is enabled. For outbound traffic, the NB does not need to snoop.
10	RWST	0h	APPME: Auxiliary Power Management Enable 0: Disables the PCI Express port to draw AUX power independent of PME AUX power. 1: Enables the PCI Express port to draw AUX power independent of PME AUX power. Devices that require AUX power on legacy operating systems should continue to indicate PME AUX power requirements. AUX power is allocated as requested in the AUX_Current field on the Power Management Capabilities Register (PMC), independent of the PMEEN bit in the Power Management Control/Status Register (PMSCR) defined in Section 4.11.31.
9	RO	0h	PFE: Phantom Functions Enable This bit enables the PCI Express port to use unclaimed functions as Phantom Functions for extending the number of outstanding transaction identifiers. The NB does not implement this bit (Root complex) and is hardwired to '0'.

Device: 1 - 7 Function: 0 Offset: 74h - 75h			
Bit	Attr	Default	Description
8	RO	0h	ETFE: Extended Tag Field Enable This bit enables the PCI Express port to use an 8-bit Tag field as a requester. The NB does not use this field (Root complex) and is hardwired to '0'.
7:5	RW	01h	MPS: Max Payload Size This field is set by configuration software for the maximum TLP payload size for the PCI Express port. As a receiver, the NB must handle TLPs as large as the set value. As a transmitter, it must not generate TLPs exceeding the set value. Permissible values that can be programmed are indicated by the Max_Payload_Size_Supported in the Device Capabilities register: 000: 128B max payload size 001: 256B max payload size 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: Reserved NOTE: The NB supports max payload sizes up to 256B. These bits should be programmed to the smallest of the max payload size supported between NB and the target.
4	RW	0h	ENRORD: Enable Relaxed Ordering If this bit is set, the device is permitted to set the Relaxed Ordering bit in the Attributes field of transactions it initiates that do not require strong write ordering. The NB enforces strict ordering only and hence it is initialized to '0'.

Device: 1 - 7 Function: 0 Offset: 74h - 75h			
Bit	Attr	Default	Description
3	RW	0h	URREN: Unsupported Request Reporting Enable This bit controls the reporting of unsupported requests to the NB in the PCI Express port. 0: Fatal error reporting is disabled. 1: Fatal error reporting is enabled. Note that the reporting of error messages (such as ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by PCI Express port is controlled exclusively by the PCI Express Root Control register (EXP_RTCTRL) described in Section 4.11.28. Suggested value: 1h
2	RW	0h	FERE: Fatal Error Reporting Enable This bit controls the reporting of fatal errors internal to the NB in the PCI Express port. 0: Fatal error reporting is disabled. 1: Fatal error reporting is enabled. Suggested value: 1h
1	RW	0h	NFERE: Non Fatal Error Reporting Enable This bit controls the reporting of non fatal errors internal to the NB in the PCI Express port. 0: Non Fatal error reporting is disabled. 1: Non Fatal error reporting is enabled. Suggested value: 1h
0	RW	0h	CERE: Correctable Error Reporting Enable This bit controls the reporting of correctable errors internal to the NB in the PCI Express port. 0: Correctable error reporting is disabled. 1: Correctable Fatal error reporting is enabled Suggested value: 1h

4.11.41 EXP_DEVSTS[7:1]: PCI Express Device Status Register (D1-7, F0)

The PCI Express Device Status register provides information about PCI Express device-specific parameters associated with this port.

Device: 1 - 7 Function: 0 Offset: 76h - 77h			
Bit	Attr	Default	Description
15:6	RV	000h	Reserved
5	RO	0h	TP: Transactions Pending 0: A device reports this bit cleared only when all Completions for any outstanding Non-Posted Requests have been received. 1: Indicates that the PCI Express port has issued Non-Posted Requests which have not been completed.
4	RO	0	APD: AUX Power Detected 0: No AUX power is detected. 1: AUX power is detected by the PCI Express port.
3	RWC	0	URD: Unsupported Request Detected This bit indicates that the device received an Unsupported Request in the PCI Express port. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register. 1: Denotes Unsupported Request detected 0: <i>Reserved</i> This records the detection of receiving an unsupported request, error IO12 (Refer to Table 6-39 'Errors Detected by the NB' on page 328).
2	RWC	0	FED: Fatal Error Detected This bit indicates status of fatal errors detected in the PCI Express port. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. 1: Denotes Non Fatal errors detected 0: <i>Reserved</i>
1	RWC	0	NFED: Non Fatal Error Detected This bit indicates the status of non-fatal errors detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. 1: Denotes Non Fatal errors detected
0	RWC	0	CED: Correctable Error Detected This bit indicates the status of correctable errors which are detected in the PCI Express port. Errors are logged in this register regardless of whether error reporting is enabled or not in the PCI Express Device Control register. 1: Denotes correctable errors detected

4.11.42 EXP_LNKCAP[7:1]: PCI Express Link Capabilities Register (D1-7, F0)

The Link Capabilities register identifies the PCI Express specific link capabilities.

Device: 1 - 7 Function: 0 Offset: 78h - 7Bh			
Bit	Attr	Default	Description
31:24	RWO	00h	PN: Port Number This field indicates the PCI Express port number for the link and is initialized by software/BIOS.
23:18	RV	00h	Reserved
17:15	RO	111b	L1EL: L1 Exit Latency This field indicates the L1 exit latency for the given PCI Express port. It indicates the length of time this port requires to complete transition from L1 to L0. 000: <1µs 001: 1 µs to less than 2 µs 010: 2 µs to less than 4 µs 011: 4 µs to less than 8 µs 100: 8 µs to less than 16 µs 101: 16 µs to less than 32 µs 110: 32 µs to 64 µs 111: > 64 µs
14:12	RO	7h	L0sEL: L0s Exit Latency This field indicates the L0s exit latency (i.e L0s to L0) for the PCI Express port. 000: <64 ns 001: 64 ns to less than 128 ns 010: 128 ns to less than 256 ns 011: 256 ns to less than 512 ns 100: 512 ns to less than 1 µs 101: 1 µs to less than 2 µs 110: 2 µs to 4 µs 111: > 4 ns NOTE: Note that NB does not support L0 Exit Latency implementation and for safety, this field is set to the maximum value.

Device: 1 - 7 Function: 0 Offset: 78h - 7Bh			
Bit	Attr	Default	Description
11:10	RO	0h	ACTPMS: Active State Link PM Support This field indicates the level of active state power management supported on the given PCI Express port. 00: Reserved (Disabled) 01: L0s Entry (Supported) 10: Reserved 11: L0s and L1 (Supported) The NB responds to link initiated power management requests, but does not initiate any power management requests on its own even if software attempts to tell the NB to do so
9:4	RO	See Table 4-21	MLW: Maximum Link Width This field indicates the maximum width of the given PCI Express Link attached to the port. 000100: x4 001000: x8 Others: Reserved Refer to Table 4-21 for the allowed port configurations and maximum link width.
3:0	RO	1h	MLS: Maximum Link Speed This field indicates the maximum Link speed of the given PCI Express port. 0001: 2.5 Gb/s Others: Reserved

4.11.43 EXP_LNKCTRL[7:1]: PCI Express Link Control Register (D1-7, F0)

The PCI Express Link Control register controls the PCI Express Link specific parameters.

Device: 1 - 7 Function: 0 Offset: 7Ch - 7Dh			
Bit	Attr	Default	Description
15:8	RV	000h	Reserved
7	RW	0h	EXTENDED_SYNCH: This bit when set forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0. This mode provides external devices monitoring the link time to achieve bit and symbol lock before the link enters L0 state and resumes communication.
6	RW	0h	CCCON: Common Clock Configuration 0: Indicates that this PCI Express port and its counterpart at the opposite end of the Link are operating with an <u>asynchronous reference clock</u> . 1: Indicates that this PCI Express port and its counterpart at the opposite end of the Link are operating with a <u>distributed common reference clock</u> . Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies.
5	WO	0h	RLNK: Retrain Link This bit, when set by software, initiates link retraining in the given PCI Express port. It always returns '0' when read.
4	RW	0h	LNKDIS: Link Disable This field indicates whether the link associated with the PCI Express port is enabled or disabled. 0: Enables the link associated with the PCI Express port 1: Disables the link associated with the PCI Express port
3	RO	0h	RCB: Read Completion Boundary The NB supports only 64B read completion boundary and this bit is hardwired to 0h.
2	RV	0h	Reserved
1:0	RW	0h	ACTPMCTRL: Active State Link PM Control This field controls the level of active state power management supported on the given PCI Express port. 00: Disabled 01: L0s Entry Supported 10: <i>Reserved</i> 11: L0s and L1 Supported The NB responds to link initiated power management requests, but does not initiate any power management requests on its own even if software attempts to tell the NB to do so.

4.11.44 EXP_LNKLSTS[7:1]: PCI Express Link Status Register (D1-7, F0)

The PCI Express Link Status register provides information on the status of the PCI Express Link such as negotiated width, training, etc.

Device: 1 - 7 Function: 0 Offset: 7Eh - 7Fh			
Bit	Attr	Default	Description
15:13	RV	00h	Reserved
12	RO	0h	SCCON: Slot Clock Configuration This bit indicates that the component uses the same physical reference clock that the platform provides on the connector. If the device uses an independent clock irrespective of the presence of a reference on the connector, this bit must be clear. 0: Indicates independent clock on the PCI Express connector from that of the platform. 1: Indicates same physical clock in the PCI Express connector as in the platform.
11	RO	0h	LNKTRG: Link Training This field indicates the status of an ongoing link training session in the current PCI Express port. 0: Indicates Link training not in progress - either it has completed or it has not begun. 1: Indicates Link training is in progress. This read-only bit indicates that Link training is in progress; hardware clears this bit once Link training is complete.
10	RV	0h	Reserved
9:4	RO	See Description	NLNKWD: Negotiated Link Width This field indicates the negotiated width of the given PCI Express link. 000001: x1 000010: x2 000100: x4 001000: x8 Others <i>Reserved</i> For the port and link assignment refer to Table 4-21.
3:0	RO	01h	LNKSPD: Link Speed This field indicates the negotiated Link speed of the given PCI Express Link: 0001: 2.5 Gb/s PCI Express link Others <i>Reserved</i>

Table 4-21. Negotiated Link Width For Different PCI Express Ports

Device	Port	Negotiated Link Width	Default Value
1,2,3,4,5,6,7	D, C0, C1, B0, B1, A0, A1	x1	000001
1,2,3,4,5,6,7	D, C0, C1, B0, B1, A0, A1	X2	000010
1,2,3,4,5,6,7	D, C0, C1, B0, B1, A0, A1	X4	000100
2,4,6	C0, B0, A0	X8	001000 ^a

NOTES:

a. Ports 3,5 and 7 report an undefined value

4.11.45 EXP_SLOTCAP[7:1]: PCI Express Slot Capabilities Register (D1-7, F0)

The Slot Capabilities register identifies the PCI Express specific slot capabilities. When this register is written, the NB sends the Slot Power Limit Value and Slot Power Limit Scale in a Slot Power Limit Message outbound.

Device: 1 - 7 Function: 0 Offset: 80h - 83h			
Bit	Attr	Default	Description
31:19	RWO	0000h	PSN: Physical Slot Number This field indicates the physical slot number connected to the PCI Express* port. It should be initialized to 0 for ports connected to devices that are either integrated on the system board or integrated within the same silicon as the Root port (NB).
18:17	RV	0h	Reserved
16:15	RWO	0h	SPLS: Slot Power Limit Scale This field specifies the scale used for the Slot Power Limit Value. Range of Values: 00: 1.0x 01: 0.1x 10: 0.01x 11: 0.001x
14:7	RWO	00h	SPLV: Slot Power Limit Value This field specifies the upper limit on power supplied by the slot in conjunction with the Slot Power Limit Scale value defined previously Power limit (in Watts) = SPLS x SPLV
6	RWO	0h	HPC: Hot-plug Capable This field defines hot-plug support capabilities for the PCI Express port. 0: Indicates that this slot is not capable of supporting Hot-plug operations. 1: Indicates that this slot is capable of supporting Hot-plug operations.

Device: 1 - 7 Function: 0 Offset: 80h - 83h			
Bit	Attr	Default	Description
5	RWO	0h	HPS: Hot-plug Surprise This field indicates that a device in this slot may be removed from the system without prior notification. 0: Indicates that surprise hot-plug is not supported. 1: Indicates that surprise hot-plug is supported.
4	RWO	0h	PIP: Power Indicator Present This bit indicates that a Power Indicator is implemented on the chassis for this slot. 0: Indicates that Power Indicator is not present. 1: Indicates that Power Indicator is present.
3	RWO	0h	AIP: Attention Indicator Present This bit indicates that an Attention Indicator is implemented on the chassis for this slot. 0: Indicates that an Attention Indicator is not present. 1: Indicates that an Attention Indicator is present.
2	RWO	0h	MRLSP: MRL Sensor Present This bit indicates that an MRL Sensor is implemented on the chassis for this slot. 0: Indicates that an MRL Sensor is not present. 1: Indicates that an MRL Sensor is present.
1	RWO	0h	PCP: Power Controller Present This bit indicates that a Power Controller is implemented on the chassis for this slot. 0: Indicates that a Power Controller is not present. 1: Indicates that a Power Controller is present.
0	RWO	0h	ABP: Attention Button Present This bit indicates that an Attention Button is implemented on the chassis for this slot. 0: Indicates that an Attention Button is not present. 1: Indicates that an Attention Button is present.

4.11.46 EXP_SLOTCTRL[7:1]: PCI EXPRESS Slot Control Register (D1-7, F0)

The Slot Control register identifies the PCI Express specific slot control specific parameters for operations such as Hot-plug and Power Management.

Device: 1 - 7 Function: 0 Offset: 84h - 85h			
Bit	Attr	Default	Description
15:11	RV	0h	Reserved
10	RW	0h	PWRCTRL: Power Control This bit indicates the current state of the Power applied to the slot of the PCI Express port: 0: Power On 1: Power Off
9:8	RW	0h	PWRLED: Power Indicator Control This bit indicates the current state of the Power Indicator of the PCI Express port: 00: <i>Reserved. The NB drives the LED into BLINK state.</i> 01: On 10: Blink (The NB drives 1.5 Hz square wave for Chassis mounted LEDs in the case of legacy card form factor for PCI Express devices) 11: Off When this field is written, the NB sends appropriate POWER_INDICATOR messages through the PCI Express port. For legacy-card-based PCI Express devices, the event is signaled via the virtual pins (Refer to Section 6.6, "RAS" on page 320) of the NB. For PCI Express modules with advanced form factor that incorporate LEDs and on-board decoding logic, the PCI Express messages are interpreted directly (No virtual pins).
7:6	RW	0h	ATNLED: Attention Indicator Control This bit indicates the current state of the Attention Indicator of the PCI Express port: 00: <i>Reserved. The NB drives the LED into BLINK state.</i> 01: On 10: Blink (The NB drives 1.5 Hz square wave for Chassis mounted LEDs in the case of legacy card form factor for PCI Express devices). 11: Off When this field is written, the NB sends appropriate ATTENTION_INDICATOR messages through the PCI Express port. For legacy card based PCI Express devices, the event is signaled via the virtual pins of the NB. For PCI Express modules with advanced form factor that incorporate LEDs and on-board decoding logic, the PCI Express messages are interpreted directly (No virtual pins).

Device: 1 - 7 Function: 0 Offset: 84h - 85h			
Bit	Attr	Default	Description
5	RW	0h	HPINTEN: Hot-plug Interrupt Enable This field enables the generation of Hot-plug interrupts and events in the PCI Express port. 0: Disables Hot-plug events and interrupts. 1: Enables Hot-plug events and interrupts.
4	RW	0h	CCIEN: Command Completed Interrupt Enable This field enables the generation of Hot-plug interrupts when a command is completed by the Hot-plug controller connected to the PCI Express port. 0: Disables hot-plug interrupts on a command completion by a hot-plug Controller. 1: Enables hot-plug interrupts on a command completion by a hot-plug Controller. Suggested Value: 0.
3	RW	0h	PRSINTEN: Presence Detect Changed Enable This bit enables the generation of hot-plug interrupts or wake messages via a presence detect changed event. 0: Disables generation of hot-plug interrupts or wake messages when a presence detect changed event happens 1: Enables generation of hot-plug interrupts or wake messages when a presence detect changed event happens
2	RW	0h	MRLINTEN: MRL Sensor Changed Enable This bit enables the generation of hot-plug interrupts or wake messages via a MRL Sensor changed event. 0: Disables generation of hot-plug interrupts or wake messages when an MRL Sensor changed event happens. 1: Enables generation of hot-plug interrupts or wake messages when an MRL Sensor changed event happens.
1	RW	0h	PWRINTEN: Power Fault Detected Enable This bit enables the generation of hot-plug interrupts or wake messages via a power fault event. 0: Disables generation of hot-plug interrupts or wake messages when a power fault event happens. 1: Enables generation of hot-plug interrupts or wake messages when a power fault event happens.

Device: 1 - 7 Function: 0 Offset: 84h - 85h			
Bit	Attr	Default	Description
0	RW	0h	ATNINTEN: Attention Button Pressed Enable This bit enables the generation of hot-plug interrupts or wake messages via an attention button pressed event. 0: Disables generation of hot-plug interrupts or wake messages when the attention button is pressed. 1: Enables generation of hot-plug interrupts or wake messages when the attention button is pressed.

4.11.47 EXP_SLOTSTS[7:1]: PCI Express Slot Status Register (D1-7, F0)

The PCI Express Slot Status register defines important status information for operations such as Hot-plug and Power Management.

Device: 1 - 7 Function: 0 Offset: 86h - 87h			
Bit	Attr	Default	Description
15:7	RV	0h	Reserved
6	RO	0h	PDS: Presence Detect State This field conveys the Presence Detect status determined via an in-band mechanism or through the Present Detect pins and shows the presence of a card in the slot. 0: Slot Empty 1: Card Present in slot
5	RO	0h	MRLSS: MRL Sensor State This bit reports the status of an MRL sensor if it is implemented. 0: MRL Closed 1: MRL Open
4	RWC	0h	CMDCOMP: Command Completed This bit is set by the NB when the hot-plug controller completes an issued command. It is subsequently cleared by software after the field has been read and processed.

Device: 1 - 7 Function: 0 Offset: 86h - 87h			
Bit	Attr	Default	Description
3	RWC	0h	PRSINT: Presence Detect Changed This bit is set by the NB when a Presence Detect Changed event is detected. It is subsequently cleared by software after the field has been read and processed.
2	RWC	0h	MRLSC: MRL Sensor Changed This bit is set by the NB when an MRL Sensor Changed event is detected. It is subsequently cleared by software after the field has been read and processed.
1	RWC	0h	PWRINT: Power Fault Detected This bit is set by the NB when a power fault event is detected by the power controller. It is subsequently cleared by software after the field has been read and processed.
0	RWC	0h	ABP: Attention Button Pressed This bit is set by the NB when the attention button is pressed. It is subsequently cleared by software after the field has been read and processed. Note: This bit will not be set if bit 29 in 'EXP_CTRL[7:1] PCI Express Control Register (01-7, F0)' is set.

Note: Note that the EXP_HPINT pin (Table 3-11 on page 3-48) is held asserted as long as any of the events defined in bits[4:0] (CMDCOMP, PRSINT, MRLSC, PWRINT, ABP) of the EXP_SLOTSTS register are set provided the corresponding events in bits [4:0] of the EXP_SLOTCTRL are enabled.

4.11.48 EXP_RTCTRL[7:1]: PCI Express Root Control Register (D1-7, F0)

The PCI Express Root Control register specifies parameters specific to the root complex port.

Device: 1 - 7 Function: 0 Offset: 88h 89h			
Bit	Attr	Default	Description
15:4	RV	0h	Reserved
3	RW	0h	PMEINTEN: PME Interrupt Enable This field controls the generation of interrupts for PME messages. 0: Disables interrupt generation for PME messages. 1: Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit defined in the PCI Express RTSTS register. A PME interrupt is also generated if the PME Status register bit is set when this bit is set from a cleared state RW.
2	RW	0h	SEFEEN: System Error on Fatal Error Enable This field controls generation of system errors in the PCI Express port hierarchy for fatal errors: 0: No System Error should be generated on a fatal error (ERR_FATAL) reported by any of the devices in the hierarchy. 1: Indicates that a System Error should be generated if a fatal error (ERR_FATAL) is reported by any of the devices in the hierarchy associated with and including this PCI Express port.
1	RW	0h	SENFEEN: System Error on Non-Fatal Error Enable This field controls generation of system errors in the PCI Express port hierarchy for non-fatal errors: 0: No System Error should be generated on a non-fatal error (ERR_NONFATAL) reported by any of the devices in the hierarchy. 1: Indicates that a System Error should be generated if a non-fatal error (ERR_NONFATAL) is reported by any of the devices in the hierarchy associated with and including this PCI Express port.
0	RW	0h	SECEEN: System Error on Correctable Error Enable This field controls generation of system errors in the PCI Express port hierarchy for correctable errors: 0: No System Error should be generated on a correctable error (ERR_COR) reported by any of the devices in the hierarchy associated with and including this PCI Express port. 1: Indicates that a System Error should be generated if a correctable error (ERR_COR) is reported by any of the devices in the hierarchy associated with and including this PCI Express port.

4.11.49 EXP_RTSTS[7:1]: PCI Express Root Status Register (D1-7, F0)

The PCI Express Root Status register specifies parameters specific to the root complex port.

Device: 1 - 7 Function: 0 Offset: 8Ch - 8Fh			
Bit	Attr	Default	Description
31:18	RV	0h	Reserved
17	RO	0h	PMEPEND: PME Pending This field indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software, the pending PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PMEs are pending.
16	RWC	0h	PMESTS: PME Status^a This field indicates status of a PME that is underway in the PCI Express port: 1: PME was asserted by a requester as indicated by the PMEREQID field. This bit is cleared by software by writing a '1'. Subsequent PMEs are kept pending until the PME Status is cleared.
15:0	RO	0h	PMEREQID: PME Requester ID This field indicates the PCI requester ID of the last PME requestor.

NOTES:

- a. The PME STATUS bit in each of the EXP_RTSTS[7:1] registers are ORed together and the NB will assert the PME_OUT pin to ICH5 for power management. When all the bits are clear, it will deassert PME_OUT.

4.12 PCI Express Advanced Function (Device 1 - 7, Function 0)

The PCI Express Extended Registers are in Devices 1 - 7 (D1-7), function 0 (F0). For the register address map, please refer to Table 4-12.

Warning: Address locations that are not listed are considered reserved locations. Writes to “Reserved” registers may cause unpredictable behavior. Reads to “Reserved” registers may return a non-zero value.

4.12.1 ENHCAPSTS: Enhanced Advanced Error Reporting Capability Structure (D1-7, F0)

This register identifies the capability structure and points to the next structure.

Device: 1 - 7 Function: 0 Offset: 100h 103h			
Bit	Attr	Default	Description
31:20	RO	140h	NXTCAPPTR: Next Capability Pointer This field points to the next Capability in extended configuration space.
19:16	RO	1h	CV: Capability Version Set to 1 for this version of the PCI Express logic.
15:0	RO	1h	ECID: PCI Express Extended CAP_ID Assigned for advanced error reporting.

4.12.2 UNCERRSTS: Uncorrectable Error Status (D1-7, F0)

This register identifies uncorrectable errors detected. for PCI Express Port. If an error occurs and is unmasked in the detect register (UNCEDMASK), the appropriate error bit will be recorded in this register. For details on errors listed on this table, refer to the Table 6-39 "Errors Detected by the NB" on page 328.

Device: 1 - 7 Function: 0 Offset: 104h - 107h			
Bit	Attr	Default	Description
31:21	RV	0h	Reserved
20	RWCST	0h	IO12Err: Received an Unsupported Request
19	RV	0h	Reserved
18	RWCST	0h	IO19Err: Malformed TLP Status
17	RWCST	0h	IO20Err: Receiver Buffer Overflow Status
16	RWCST	0h	IO18Err: Unexpected Completion Status
15	RWCST	0h	IO17Err: Completer Abort Status - Optional
14	RWCST	0h	IO16Err: Completion Time-out Status
13	RWCST	0h	IO15Err: Flow Control Protocol ERROR Status
12	RWCST	0h	IO14Err: Poisoned TLP Status
11:5	RV	0h	Reserved
4	RWCST	0h	IO21Err: Data Link Layer Protocol Status
3:1	RV	0h	Reserved
0	RWCST	0h	IO13Err: Training Error Status

4.12.3 UNCERRMSK: Uncorrectable Error Mask (D1-7, F0)

This register masks uncorrectable errors from being reported. If an error is recorded in the UNCERRSTS register and the appropriate bit is set (along with the severity bit of the UNCERRSEV register), it determines which bit in the EXP_FERR/EXP_NERR register is set. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 1 - 7 Function: 0 Offset: 108h - 10Bh			
Bit	Attr	Default	Description
31:21	RV	0	Reserved
20	RWST	0	IO12Msk : Received an Unsupported Request
19	RV	0	Reserved
18	RWST	0	IO19Msk : Malformed TLP Status
17	RWST	0	IO20Msk : Receiver Buffer Overflow Mask
16	RWST	0	IO18Msk : Unexpected Completion Mask
15	RWST	0	IO17Msk : Completer Abort Status (Optional)
14	RWST	0	IO16Msk : Completion Time-out Mask
13	RWST	0	IO15Msk : Flow Control Protocol ERROR Mask
12	RWST	0	IO14Msk : Poisoned TLP Mask
11:1	RV	00h	Reserved
4	RWST	0	IO21Msk : Data Link Layer Protocol Error Mask
3:1	RV	00	Reserved
0	RWST	0	IO13Msk : Training Error Mask

4.12.4 UNCERRSEV: Uncorrectable Error Severity (D1-7, F0)

This register indicates the severity of the uncorrectable errors. If an error is recorded in the UNCERRSTS register, the appropriate bit of UNCERRSEV determines if the error gets reflected as a device fatal or nonfatal error in the EXP_FERR/EXP_NERR registers. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328

Device: 1 - 7 Function: 0 Offset: 10Ch - 10Fh			
Bit	Attr	Default	Description
31:21	RV	0h	Reserved
20	RWST	0h	IO12Severity: Received an Unsupported Request
19	RV	0h	Reserved
18	RWST	1	IO19Severity: Malformed TLP Severity
17	RWST	1	IO20Severity: Receiver Buffer Overflow Severity
16	RWST	0h	IO18Severity: Unexpected Completion Severity
15	RWST	0h	IO17Severity: Completer Abort Status - Optional
14	RWST	0h	IO16Severity: Completion Time-out Severity
13	RWST	1	IO15Severity: Flow Control Protocol ERROR Severity
12	RWST	0h	IO14Severity: Poisoned TLP Severity
11:5	RV	00h	Reserved
4	RWST	1	IO21Severity: Data Link Layer Protocol Error Severity
3:2	RV	0	Reserved
0	RWST	1	IO13Severity: Training Error Severity

4.12.5 CORERRSTS: Correctable Error Status (D1-7, F0)

This register identifies which unmasked correctable error has been detected. The logical OR of these bits feed the device correctable error bit in the EXP_FERR/EXP_NERR registers (if the error is unmasked in the CORERRMSK register).

Device: 1-7 Function: 0 Offset: 110h - 113h			
Bit	Attr	Default	Description
31:13	RV	0h	Reserved
12	RWCST	0h	IO11Err: Replay Timer Time-out Status
11:9	RWCST	0h	Reserved
8	RWCST	0h	IO10Err: Replay_Num Rollover Status
7	RWCST	0h	IO9Err: Bad DLLP Status
6	RWCST	0h	IO8Err: Bad TLP Status
5:1	RV	0h	Reserved
0	RWCST	0h	IO7Err: Receiver Error Status

4.12.6 CORERRMSK: Correctable Error Mask (D1-7, F0)

This register masks correctable errors to not be reported. They are still logged. The appropriate bit will prevent an error from being signaled in the EXP_FERR/EXP_NERR registers.

Device: 1-7 Function: 0 Offset: 114h - 117h			
Bit	Attr	Default	Description
31:13	RV	0h	Reserved
12	RWST	0h	IO11Msk: Replay Timer Time-out Mask
11:9	RV	0h	Reserved
8	RWST	0h	IO10Msk: Replay_Num Rollover Mask
7	RWST	0h	IO9Msk: Bad DLLP Mask
6	RWST	0h	IO8Msk: Bad TLP Mask
5:1	RV	0h	Reserved
0	RWST	0h	IO7Msk: Receiver Error Mask

4.12.7 AERCACR: Advanced Error Capabilities and Control Register (D1-7, F0)

This register identifies the capability structure and points to the next structure.

Device: 1 - 7 Function: 0 Offset: 118h - 11Bh			
Bit	Attr	Default	Description
31:9	RV	0	Reserved
8	RWST	0	AERCACR[8]: ECRC Check Enable This bit when set enables ECRC checking.
7	RO	0	AERCACR[7]: ECRC Check Capable The NB does not support ECRC.
6	RWST	0	AERCACR[6]: ECRC Generation Enable The NB does not support ECRC.
5	RO	0	AERCACR[5]: ECRC Generation Capable The NB does not support ECRC.
4:0	ROST	0	AERCACR[4:0]: First error pointer The First Error Pointer is a read-only register that identifies the bit position of the first error reported in the Uncorrectable Error. The pointer can be overwritten by a more severe error according to the PCI Express Spec (Left-most error bit if multiple bits occurred simultaneously).

4.12.8 HDRLOG0: Header Log 0 (D1-7, F0)

This register contains the first 32 bits of the header log locked down when the first error occurs. If a subsequent error is more severe, this log will be overwritten, and the header log will be lost for the “true” first error.

Device: 1 - 7 Function: 0 Offset: 11Ch - 11F			
Bit	Attr	Default	Description
31:0	ROST	0h	HDRLOG0[31:0]: Header Log 0

4.12.9 HDRLOG1: Header Log 1 (D1-7, F0)

This register contains the second 32 bits of the header log.

Device: 1 - 7 Function: 0 Offset: 120h - 123h			
Bit	Attr	Default	Description
31:0	ROST	0h	HDRLOG1[31:0]: Header Log 1

4.12.10 HDRLOG2: Header Log 2 (D1-7, F0)

This register contains the third 32 bits of the header log.

Device: 1 - 7 Function: 0 Offset: 124h - 127h			
Bit	Attr	Default	Description
31:0	ROST	0h	HDRLOG2[31:0]: Header Log 2

4.12.11 HDRLOG3: Header Log 3 (D1-7, F0)

This register contains the fourth 32 bits of the header log.

Device: 1 - 7 Function: 0 Offset: 128h - 12Bh			
Bit	Attr	Default	Description
31:0	ROST	0h	HDRLOG3[31:0]: Header Log 3

4.12.12 RPERRCMD: Root Port Error Command (D1-7, F0)

This register controls behavior upon detection of errors.

Device: 1 - 7 Function: 0 Offset: 12Ch - 12Fh			
Bit	Attr	Default	Description
31:8	RV	0h	Reserved
7:3	RV	0h	Reserved
2	RW	0h	RPERRCMD_EN_FAT Enable interrupt on fatal errors when set.
1	RW	0h	RPERRCMD_EN_UNCORR Enable interrupt on uncorrectable errors when set.
0	RW	0h	RPERRCMD_EN_CORR Enable interrupt on correctable errors when set.

4.12.13 RPERRMSGSTS: Root Port Error Message Status (D1-7, F0)

Device: 1 - 7 Function: 0 Offset: 130h - 133h			
Bit	Attr	Default	Description
31:27	RO	0h	RPERRMSGSTS_INT_MSGS[4:0] Advanced Error Interrupt Message Number offset between base message data on the MSI message if assigned more than one message number to be used of any status in this capability.
26:7	RV	0h	Reserved
6	RWCST	0h	FATAL: Fatal Error Message Detected
5	RWCST	0h	NONFATAL: NonFatal Error Message Detected
4	RWCST	0h	1st_UNCOR_FATAL: First Uncorrectable Fatal Error Message Detected
3	RWCST	0h	RPERRMSGSTS_NXT_UNCORR: Next Uncorrectable Error Message Detected.
2	RWCST	0h	RPERRMSGSTS_1ST_UNCORR: First Uncorrectable Error Message Detected.
1	RWCST	0h	RPERRMSGSTS_NXT_CORR: Next Correctable Error Message Detected.
0	RWCST	0h	RPERRMSGSTS_1ST_CORR: First Correctable Error Message Detected.

4.12.14 ERRSID: Error Source ID (D1-7, F0)

This register identifies the ID of the first correctable and uncorrectable errors.

Device: 1 - 7 Function: 0 Offset: 134h - 137h			
Bit	Attr	Default	Description
31:16	ROST	0h	ERRSID_UNCORR_ID[15:0]: Uncorrectable Error Source ID Requestor ID of the source when an uncorrectable error is received and the First Uncorrectable Error Detected is not already set.
15:0	ROST	0h	ERRSID_CORR_ID[15:0]: Correctable Error Source ID Requestor ID of the source when a correctable error is received and the First Correctable Error Detected is not already set.

4.12.15 NBSPCAPID: NB Specific Capability ID (D1-7, F0)

This register identifies the capability structure and points to the next structure.

Device: 1 - 7 Function: 0 Offset: 140h - 143h			
Bit	Attr	Default	Description
31:20	RO	0h	NXT_CAP_PTR[11:0]: Next Capability Pointer This field points to the next Capability in extended configuration space.
19:16	RO	0h	MCH_VENDOR_ID[3:0]: Version Number
15:0	RO	0h	EXT_CAP_ID[15:0]: Extended CAP_ID

4.12.16 EXP_unitERR: PCI Express Unit Error Register (D1-7, F0)

Host Bridge Error Commands for doing the various signaling: ERR[2:0] and MCERR. These errors correspond to the “unit” errors of the PCI Express block. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 1 - 7 Function: 0 Offset: 144h - 147h			
Bit	Attr	Default	Description
31:4	RV	0h	Reserved
3	RWST	0h	T9Err: SMBus Virtual Pin Interface Error (FATAL Error)
2	RWST	0h	T10Err: I/O Unit Detected Failure (FATAL Error)
1	RWST	0h	T2Err: Received an uncorrectable ECC Error from CDC (FATAL Error)
0	RWST	0h	T1Err: Received a correctable ECC Error from CDC (Corr. Error)

4.12.17 EXP_ERR_DOCMD: PCI Express Error Do Command Register (D1-7, F0)

Link Error Commands for doing the various signaling: ERR[2:0] and MCERR. For this Register usage refer to Figure 6-16 “Error Integration Model” on page 6-327.

Device: 1 - 7 Function: 0 Offset: 148h - 14Bh			
Bit	Attr	Default	Description
31:16	RV	0h	Reserved
15	RW	1	COR_RPT_EN: Correctable internal error report enable 1: enable 0: disable
14	RW	1	UNC_RPT_EN: Uncorrectable internal error report enable 1: enable 0: disable
13:12	RW	01	EXP_RP_FAT_MAP: Root Port steering for fatal errors 00: ERR[0] 01: ERR[1] 10: ERR[2] 11: MCERR (This encoding should not be used) If the ERR[2] enable in the Root Command register is set for fatal errors, all fatal errors will be reported via ERR[2] regardless of the setting of this register. MSI enable takes precedence for this capability feature.
11:10	RW	01	EXP_RP_NF_MAP: Root Port steering for non-fatal errors 00: ERR[0] 01: ERR[1] 10: ERR[2] 11: MCERR If the ERR[2] enable in the Root Command register is set for non-fatal errors, all non-fatal errors will be reported via ERR[2] regardless of the setting of this register. MSI enable takes precedence for this capability feature.

Device: 1 - 7 Function: 0 Offset: 148h - 14Bh			
Bit	Attr	Default	Description
9:8	RW	01	EXP_RP_CORR_MAP: Root Port steering for correctable errors 00: ERR[0] 01: ERR[1] 10: ERR[2] 11: MCERR If the ERR[2] enable in the Root Command register is set for correctable errors, all correctable errors will be reported via ERR[2] regardless of the setting of this register. MSI enable takes precedence for this capability feature.
7:6	RV	0h	Reserved
5:4	RW	01	EXP_DEV_FAT_MAP: DEV report steering for fatal errors Fatal error report enable is in the Device control register 00: ERR[0] → Generate ERR[0] if bit 2 (fatal error) is being set in EXP_DEVSTS register and EXP_DEVCTL register has fatal reporting enabled. 01: ERR[1] → Generate ERR[1] if bit 2 (Fatal Error) is being set in EXP_DEVSTS register and EXP_DEVCTL register has fatal reporting enabled. 10: ERR[2] → Generate ERR[2] if bit 2 (fatal error) is being set in EXP_DEVSTS register and DEVCTL has fatal reporting enabled. 11: MCERR → Generate MCERR if bit 2 (Fatal Error) is being set in EXP_DEVSTS register and EXP_DEVCTL register has fatal reporting enabled. MSI enable takes precedence for this capability feature.

Device: 1 - 7 Function: 0 Offset: 148h - 14Bh			
Bit	Attr	Default	Description
3:2	RW	01	EXP_DEV_NF_MAP: DEV report steering for non-fatal errors 00: ERR[0] 01: ERR[1] 10: ERR[2] 11: MCERR Non-fatal error report enable is in the Device control register.
1:0	RW	01	EXP_DEV_CORR_MAP: DEV report steering for correctable errors 00: ERR[0] 01: ERR[1] 10: ERR[2] 11: MCERR Correctable error report enable is in the EXP_DEVCTL register.

4.12.18 UNCEDMASK: Uncorrectable Error Detect Mask (D1-7, F0)

This register masks (blocks) the detection of the selected bits. Normally, all are detected. When a specific error is blocked, it does NOT get reported or logged. For this Register usage, refer to Figure 6-16 “Error Integration Model” on page 6-327. For a description of the Errors (IOxx), refer to Table 6-39 “Errors Detected by the NB” on page 328.

Device: 1 - 7 Function: 0 Offset: 14Ch - 14Fh			
Bit	Attr	Default	Description
31:21	RV	0h	Reserved
20	RW	1	IO12DetMsk : Received an Unsupported Request
19	RV	0h	Reserved
18	RW	1	IO19DetMsk : Malformed TLP Status
17	RW	1	IO20DetMsk : Receiver Buffer Overflow Status
16	RW	1	IO18DetMsk : Unexpected Completion Status
15	RW	1	IO17DetMsk : Completer Abort Status
14	RW	1	IO16DetMsk : Completion Time-out Status
13	RW	1	IO15DetMsk : Flow Control Protocol ERROR Status
12	RW	1	IO14DetMsk : Poisoned TLP Status

Device: 1 - 7 Function: 0 Offset: 14Ch - 14Fh			
Bit	Attr	Default	Description
11:5	RV	0h	Reserved
4	RW	1	IO21DetMsk : Data Link Layer Protocol Error Status
3:1	RV	0h	Reserved
0	RW	1	IO13DetMsk : Training Error Status

4.12.19 COREDMASK: Correctable Error Detect Mask (D1-7, F0)

This register masks (blocks) the detection of the selected bits.

Device: 1 - 7 Function: 0 Offset: 150h - 153h			
Bit	Attr	Default	Description
31:13	RV	0h	Reserved
12	RW	1	IO11DetMsk : Replay Timer Time-out Mask Suggested Value: 1
11:9	RW	0h	Reserved
8	RW	1	IO10DetMsk : Replay_Num Rollover Mask
7	RW	1	IO9DetMsk : Bad DLLP Mask
6	RW	1	IO8DetMsk : Bad TLP Mask
5:1	RV	0h	Reserved
0	RW	1	IO7DetMsk : Receiver Error Mask

4.12.20 RPEDMASK: Root Port Error Detect Mask (D1-7, F0)

This register masks (blocks) the detection of the selected bits.

Device: 1 - 7 Function: 0 Offset: 154h - 157h			
Bit	Attr	Default	Description
31:3	RV	0h	Reserved
2	RW	1	IO26DetMsk : Fatal Message Detect Mask
1	RW	1	IO25DetMsk : Uncorrectable Message Detect Mask
0	RW	1	IO24DetMsk : Correctable Message Detect Mask

4.12.21 EXP_unitDMASK: PCI Express Unit Detect Mask Register (D1-7, F0)

This register masks the non-PCI Express unit errors from being recognized and therefore not logged, and no interrupt/messages are generated. These errors correspond to the “unit” errors of the PCI Express block. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 1 - 7 Function: 0 Offset: 158h - 15Bh			
Bit	Attr	Default	Description
31:4	RV	0h	<i>Reserved</i>
3	RW	1	T9DetMsk: SMBus Virtual Pin Interface Error
2	RW	1	T10DetMsk: I/O Unit Detected Failure
1	RW	1	T2DetMsk: Received an uncorrectable ECC Error from CDC
0	RW	1	T1DetMsk: Received a correctable ECC Error from CDC

4.12.22 EXP_FERR: PCI Express First Error Register (D1-7, F0)

Locks down after first error in each category type. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 1 - 7 Function: 0 Offset: 160h - 163h			
Bit	Attr	Default	Description
31:10	RV	0h	<i>Reserved</i>
9	RWCST	0h	Unit_FAT_Err: Unit Fatal Error Detected
8	RV	0h	<i>Reserved</i>
7	RWCST	0h	Unit_Corr_Err: Unit Correctable Error Detected
6	RWCST	0h	IO26Err: Root Port Fatal Error Received
5	RWCST	0h	IO25Err: Root Port Non-Fatal Error Received
4	RWCST	0h	IO24Err: Root Port Correctable Error Received
3	RWCST	0h	IO12Err: Device Unsupported Request Detected
2	RWCST	0h	Dev_FAT_Err: Device Fatal Error Detected
1	RWCST	0h	Dev_NF_Err: Device Non-Fatal Error Detected
0	RWCST	0h	Dev_Corr_Err: Device Correctable Error Detected

4.12.23 EXP_NERR: PCI Express Next Error Register (D1-7, F0)

See EXP_FERR for bit definitions. Logs errors after corresponding field in FERR register is locked down.

Device: 1 - 7 Function: 0 Offset: 164h - 167h			
Bit	Attr	Default	Description
31:10	RV	0h	<i>Reserved</i>
9	RWCST	0h	Unit_Nxt_FAT_Err: Unit Fatal Error Detected
8	RV	0h	<i>Reserved</i>
7	RWCST	0h	Unit_Nxt_Corr_Err: Unit Correctable Error Detected
6	RWCST	0h	IO26NXT_ERR: Root Port Fatal Error Received
5	RWCST	0h	IO25NXT_ERR: Root Port Non-Fatal Error Received
4	RWCST	0h	IO24NXT_ERR: Root Port Correctable Error Received
3	RWCST	0h	IO12NXT_ERR: Device Unsupported Request Detected
2	RWCST	0h	Dev_Nxt_FAT_Err: Device Fatal Error Detected
1	RWCST	0	Dev_Nxt_NF_Err: Device Non-Fatal Error Detected
0	RWCST	0h	Dev_Nxt_Corr_Err: Device Correctable Error Detected

4.12.24 EXP_unitEMASK: PCI Express Unit Error Mask Register (D1-7, F0)

This register masks the non-PCI Express unit errors from being recognized (and therefore not logged), and no interrupt/messages are generated. These errors correspond to the “unit” errors of the PCI Express block. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328. A ‘1’ in any field enables that error.

Device: 1 - 7 Function: 0 Offset: 168h - 16Bh			
Bit	Attr	Default	Description
31:4	RV	0h	<i>Reserved</i>
3	RW	1	T9Msk: SMBus Virtual Pin Interface Error
2	RW	1	T10Msk: I/O Unit Detected Failure
1	RW	1	T2Msk: Received an uncorrectable ECC Error from CDC
0	RW	1	T1Msk: Received a correctable ECC Error from CDC

4.13 IMI Registers (Device{8,10,12,14}, Function 0)

The IMI registers are in Devices 8,10, 12, 14 (D{8,10,12,14}), Function 0 (F0). For the register address map please refer to Table 4-13.

Note: There are four sets of the following registers, one set for each IMI. They will all appear in function 0 of a different device as defined below in Table 4-22.

Table 4-22. Device Numbers of IMIs and XMBs

IMI	IMI Device Number	Device Number Of Connected XMB
A	8d	9d
B	10d	11d
C	12d	13d
D	14d	15d

4.13.1 VID: Vendor Identification Register (D{8,10,12,14}, F0)

This register identifies Intel as the manufacturer of the Intel® E8501 chipset North Bridge (NB). Writes to this register have no effect.

Device 8, 10, 12, 14 Function: 0 Offset: 00h 01h			
Bit	Attr	Default	Description
15:0	RO	8086h	Vendor Identification Number- The value assigned to Intel.

4.13.2 DID: Device Identification Register (D{8,10,12,14}, F0)

This register combined with the Vendor Identification register uniquely identifies the NB. Writes to this register have no effect. All IMI devices will have the same DID in each function.

Device 8, 10, 12, 14 Function: 0 Offset: 02h - 03h			
Bit	Attr	Default	Description
15:0	RO	260Ch	DIN: Device Identification Number Identifies each function of the NB.

4.13.3 RID: Revision Identification Register (D{8,10,12,14}, F0)

This register contains the revision number of the Intel® E8501 chipset North Bridge (NB).

Device: 8, 10, 12, 14 Function: 0 Offset: 08h			
Bit	Attr	Default	Description
7:4	RO	00h	Major_rev: Major Revision Steppings which require all masks to be regenerated. 1: B stepping
3:0	RO	00h	Minor_rev: Minor Revision Incremented for each stepping which does not modify all masks. Reset for each major revision. 0: x0 stepping 1: x1 stepping 2: x2 stepping

4.13.4 CCR: Class Code Register (D{8,10,12,14}, F0)

This register contains the Class Code for the device.

Device: 8, 10, 12, 14 Function: 0 Offset: 09h - 0Bh			
Bit	Attr	Default	Description
23:16	RO	06h	BaseClass: Base Class. This field indicates the general device category. For the NB, this field is hardwired to 06h, indicating it is a "Bridge Device".
15:8	RO	00h	SubClass: Sub-Class. This field qualifies the Base Class, providing a more detailed specification of the device function. For these Devices default is 00h, indicating "Host Bridge".
7:0	RO	00h	RLPI: Register-Level Programming Interface. This field identifies a specific programming interface (if any), that device independent software can use to interact with the device. There are no such interfaces defined for "Host Bridge" types, and this field is hardwired to 00h.

4.13.5 HDR: Header Type Register (D{8,10,12,14}, F0)

This register identifies the header layout of the configuration space.

Device: 8, 10, 12, 14 Function: 0 Offset: 0Eh			
Bit	Attr	Default	Description
7	RO	0h	Mfd: Multi-function Device. Selects whether this is a multi-function device, that may have alternative configuration layouts. Therefore, the IM! is defined to be a single function device, and this bit is hardwired to '0'.
6:0	RO	00h	CfgLayout: Configuration Layout. This field identifies the format of the configuration header layout for a PCI-to-PCI bridge from bytes 10h through 3Fh. For devices - 8,10,12,14 default is 00h, indicating a conventional type 00h PCI header.

4.13.6 SVID: Subsystem Vendor Identification Register (D{8,10,12,14}, F0)

This register identifies the manufacturer of the system. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device.

Device: 8, 10, 12, 14 Function: 0 Offset: 2Ch - 2Dh			
Bit	Attr	Default	Description
15:0	RWO	8086h	Vendor Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to this register will have no effect.

4.13.7 SID: Subsystem Identity (D{8,10,12,14}, F0)

This register identifies the system.

Device: 8, 10, 12, 14 Function: 0 Offset: 2Eh - 2Fh			
Bit	Attr	Default	Description
15:0	RWO	8086h	Subsystem Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to this register will have no effect.

4.13.8 IMISC: IMI Issue Control (D{8,10,12,14}, F0)

This register controls outbound command issue on the IMI.

Device: 8, 10, 12, 14 Function: 0 Offset: 40h - 43h			
Bit	Attr	Default	Description
31:27	RW	10h	WRO: Number of Writes Outstanding This field controls the number of writes the NB will issue to the XMB.
26:22	RW	10000b	RDO: Number of Reads Outstanding This field controls the number of reads the NB will issue before receiving read returns.
21:19	RV	001b	Reserved
18:16	RV	010b	Reserved
15:0	RW	0AF0h	TIMEOUT_COUNT: Time-out Value Defines the maximum interval between command and read return or write acknowledge. The interval is in NB core clocks. At 333 MHz, this is 3 ns per clock. Any retry will be triggered between 1x - 2x this interval. The default value is 8.4 μ s.

4.13.9 IMIST: IMI Status (D{8,10,12,14}, F0)

These registers are inspected by software when it gets an IMI_HPINT to determine the cause of an IMI_HPINT interrupt. This register contains RAID and Mirroring recovery state, Initialization state, and Hot Plug Sequencing status. The IMI_HPINT pin is asserted whenever MRLINT, XMBINT, ANTINT, FALINT, PRSINT or PWRINT bits are set.

Device: 8, 10, 12, 14 Function: 0 Offset: 48h - 4Bh			
Bit	Attr	Default	Description
31:24	RO	00h	STATE: IMI State This field describes the current state of the IMI. It can be read by software to determine which IMI is being sequenced through recovery, and how far the IMI has progressed. 00h: Reset 10h: Init 20h: Ready 30h: Active 40h: Redundant 50h: Disabled 60h: Redundancy Loss 70h: Recovery Reset 80h: Recovery Init 90h: Recovery Ready A0h: Resilver B0h: Recovered C0h: Recovery Failure
23:9	RW	0	SCRATCH: Software Scratchpad This field is reserved for use by hot-plug software to record the status of an IMI.
8	RW	0	PWRGOOD: Power Good State 0: The virtual pin PWRGOOD# is asserted 1: The virtual pin PWRGOOD# is not asserted. Indicates to software that the IMI_RESET signal can be deasserted.
7	RW	0	MRL: Manually Operated Retention Latch State 0: The MRL is closed. The virtual pin MRL# is not asserted. 1: The MRL is open. The virtual pin MRL# is asserted. Software can cause interrupts by writing this register when true Hot-Plug behavior is not enabled.

Device: 8, 10, 12, 14 Function: 0 Offset: 48h - 4Bh			
Bit	Attr	Default	Description
6	RW	0	PRSNT: Presence Detect State 0: An XMB is not connected to the NB. The virtual pin PRSNT# is not asserted. 1: An XMB is connected to the NB. The virtual pin PRSNT# is asserted. The XMB may or may not be powered. Software can cause interrupts by writing this register when true Hot-Plug behavior is not enabled.
5	RWC	0	XMBINT: XMB Interrupt This bit is set whenever the XMB has asserted the "Assert IMI_HPINT" inband signal on the Independent Memory Interface. The MS register in the XMB holds the cause of the interrupt. After software has handled the event, it writes to 1 to clear.
4	RWC	0	MRLINT: Manually Operated Retention Lever Sensor Changed Event Set when the virtual pin MRL# changes state. After software has handled the event, it writes to 1 to clear.
3	RWC	0	ATNINT: Attention Button Pressed Set when the virtual pin ATNBTN# is pressed for this port. After software has handled the event, it writes to 1 to clear.
2	RWC	0	FAILINT: Disabled State Interrupt This bit is set whenever this IMI enters Disabled State. After software has handled the event, it writes to 1 to clear.
1	RWC	0	PRSINT: Presence Detect Changed Event Set when the virtual pin PRSNT# changes state. After software has handled the event, it writes to 1 to clear.
0	RWC	0	PWRINT: Power Fault Detected Set when the virtual pin PWRFLT# is sampled asserted. After software has handled the event, it writes to 1 to clear.

4.13.10 IMIHPC: IMI Hot-Plug Control (D{8,10,12,14}, F0)

This register controls the IMI for Initialization, Hot-Plug, RAID recovery and Mirroring Recovery. It consists of a State field, Hot-Plug Virtual Pin Controls, and Interrupt Enables. [Section 6.6](#), “RAS” on [page 320](#) describes how the Hot-Plug pins controlled by this register are sampled and driven.

Device: 8, 10, 12, 14 Function: 0 Offset: 4Ch - 4Fh			
Bit	Attr	Default	Description
31:24	RW	00h	NEXTSTATE: IMI State Control field This field is written by software to change the IMI state. It returns the last value written when read. Many states can only be entered under hardware control and should not be written by software. These settings are only valid if bit 18 NNEXTSTATE is set. 00h: Reset 10h: Init 20h: Ready 30h: Active 40h: Redundant 50h: Disabled 60h: Redundancy Loss - may not be written 70h: Recovery Reset 80h: Recovery Init 90h: Recovery Ready - may not be written A0h: Resilver B0h: Recovered - may not be written C0h: Recovery Failure - may not be written
23	RW	1b	PWRCTL: Power Controller Controls the PWREN# virtual pin. 0: Activate PWREN#. Apply power to the Memory Card. 1: De-activate PWREN#. Power is removed from the Memory Card
22:21	RW	11b	PWRLED: Power Indicator Control Controls the Virtual PWRLED# pin. 00: Reserved 01: On (drive low) 10: Blink (PWRLED# VP toggles at 1.5 Hz) 11: Off (high impedance)
20:19	RW	11b	ATNLED: Attention Indicator Control Controls the virtual ATNLED# pin. 00: Reserved 01: On (drive low) 10: Blink (ATNLED# VP toggles at 1.5 Hz) 11: Off (high impedance)

Device: 8, 10, 12, 14 Function: 0 Offset: 4Ch - 4Fh			
Bit	Attr	Default	Description
18	RW	0	NNEXTSTATE: Software writing a 1 to this bit indicates to hardware that the NNEXTSTATE field is also being written at this time and that hardware should change the IMI State according to the new IMI State Control Field. Hardware guarantees a 0 will always be read from this bit.
17:14	RW	00h	PARTNERS: IMI's Redundant with this one This field defines the IMI's which will cause a transition to "Redundancy Loss" state when they fail. If bit [17] is set, IMI[3] is a partner with this one ([16] for IMI[2], [15] for IMI[1], [14] for IMI[0]). If REDUN.MIRROR is set, the bit should be set for any IMI which appears in IMIR[i].IMIG0WAY[j] when this IMI appears in IMIR[j].IMIG1WAY[j] or vice versa for all i and j.
13	RW	0h	XMBHDR: XMB responds to config access to PCI Header Normally, the NB responds to XMB Function 0 configuration requests whether the XMB is present or not. When set, the NB allows the XMB to respond to Function 0 to allow examination of the revision ID of the XMB.
12	RW	0h	HPC: Hot-Plug Capable Set by software to indicate that the I/O Port specified by VPP is valid.
11:8	RW	00h	VPP: Virtual Pin Port [11:9] = SMBus Address [8] = I/O Port Defines the 8-bit IO port that has the Hot-Plug pins for this interface. If the HPC bit is set, the NB will write ANTLED, PWRLED, and PWREN values from this register to the specified IO Port. It will update the ATNBTN, PWRFLT, PRSNT, and MRL values from the IO Port to the IMIHPS register for this port.
7	RV	0h	Reserved
6	RW	0h	HPINTEN: Hot-Plug Interrupt Enable 0: IMI_HPINT may not be asserted due to events on this IMI. 1: IMI_HPINT may be asserted due to events on this IMI. Each event is also individually enabled by bits in this register.
5	RW	0h	XMBINTEN: XMB interrupt enable When set, the NB will assert IMI_HPINT when the "Assert IMI_HPINT" inband signal appears on the IMI.
4	RW	0h	MRLINTEN: Mechanical Retention Latch Interrupt Enable If set, IMI_HPINT will be asserted when the virtual pin MRL# is asserted, indicating latch has opened.
3	RW	0h	ATNINTEN: Attention Button Pressed Interrupt Enable If set, IMI_HPINT will be asserted when the virtual pin ATNBTN# is asserted.
2	RW	0h	FAILINTEN: Redundancy Failure Interrupt Enable If set, IMI_HPINT will be asserted when the IMI transitions to Disabled State.
1	RW	0h	PRSINTEN: Presence Detection Interrupt Enable If set, IMI_HPINT will be asserted when a level change is sampled by the NB on the virtual pin PRSNT#.
0	RW	0h	PWRINTEN: Power Fault Detected Interrupt Enable If set, IMI_HPINT will be asserted when the virtual pin PWRFLT# is asserted.

4.13.11 IMIAPR: IMI Read Return Aperture (D{8,10,12,14}, F0)

This register defines the read return aperture on this IMI.

Device: 8, 10, 12, 14 Function: 0 Offset: 60h			
Bit	Attr	Default	Description
7:6	RV	0h	Reserved
5:0	RWST	000111b	APERTURE: Read Return Aperture This field sets the size of the window in which a data return may appear. Software should only set this register to values of 1, 3, 5 and 7. If set larger than 7, the NB will interpret as 7.

4.13.12 IMIOFF: IMI Read Return Offset (D{8,10,12,14}, F0)

This register defines the read return offset on this IMI.

Device: 8, 10, 12, 14 Function: 0 Offset: 61h			
Bit	Attr	Default	Description
7:6	RV	0h	Reserved
5:0	RWST	000010	OFFSET: Read Return offset This field sets the minimum delay between an early read return and inbound data on the IMI. Maximum legal value is 48. This register has an additional reset behavior. It resets to the default value whenever the IMI_{A,B,C,D}_RST# signal is asserted to the attached XMB. Hardware performs this reset.

4.13.13 IMILINE: IMI Cache Line Size (D{8,10,12,14}, F0)

This register defines the cache line size on this IMI. It is present in case the NB is ever connected to an XMB that does not power up to this parameter value.

Device: 8, 10, 12, 14 Function: 0 Offset: 62h			
Bit	Attr	Default	Description
7:0	RO	40h	LINE: Cache line size This encoding specifies 64B.

4.13.14 IMICHNK: IMI Chunk Size (D{8,10,12,14}, F0)

This register defines the Chunk size used by the NB on the IMI.

Device: 8, 10, 12, 14 Function: 0 Offset: 63h			
Bit	Attr	Default	Description
7:0	RO	10h	CHUNK: Chunk size This encoding specifies 16B.

4.13.15 IMICODE: IMI ECC Code Size (D{8,10,12,14}, F0)

This register defines the Error Correction Code used to cover read returns.

Device: 8, 10, 12, 14 Function: 0 Offset: 64h			
Bit	Attr	Default	Description
7:0	RO	03h	CODE: Error Correction Code This encoding specifies code that corrects x8 DRAM failures used by the NB.

4.13.16 IMI_FERR: IMI First Errors (D{8,10,12,14}, F0)

The first error for an IMI is logged in this register. When an error is logged in this register the corresponding NRECIMI register latches the appropriate log information. For a description of the Errors (IMIxx) refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 8, 10, 12, 14 Function: 0 Offset: C0h - C3h			
Bit	Attr	Default	Description
31:15	RV	00h	Reserved
14	RWCST	0	IMI14Err: NB Received a Fatal Error signal from the XMB Fatal
13	RWCST	0	IMI13Err: Failed on last retry. Co-exist with IMI9Err Nonfatal
12	RWCST	0	IMI12Err: The NB received an uncorrectable error signal from XMB Nonfatal
11	RWCST	0	IMI11Err: The NB received a correctable error signal from XMB Nonfatal
10	RWCST	0	IMI10Err: The NB is sending a “poisoned” Config Write to XMB Nonfatal
9	RWCST	0	IMI9Err: Failed on last retry. Co-exist with IMI13Err Nonfatal

Device: 8, 10, 12, 14 Function: 0 Offset: C0h - C3h			
Bit	Attr	Default	Description
8	RWCST	0	IM18Err: Outstanding Requests are posted to a failed IMI Link Nonfatal
7	RWCST	0	IM17Err: VPP SMBus Hot-Plug error Nonfatal
6	RWCST	0	IM16Err: Abort Nonfatal
5	RWCST	0	IM15Err: Inbound link layer control error Idle Flit Sequence Error Link Layer Format Sequence Errors Bad Data Size, Info Bit Sequence Error Aperture Violation Invalid Tag Nonfatal
4	RWCST	0	IM14Err: Memory write data poisoned The NB has poisoned the flit that contains the error and written the data to memory. Nonfatal
3	RWCST	0	IM13Err: Inbound CRC Error May or may not get a M7 as well. Nonfatal
2	RWCST	0	IM12Err: command time-out Nonfatal
1	RWCST	0	IM11Err: Correctable error in read return packet Nonfatal
0	RWCST	0	IM10Err: Uncorrectable error in read return packet before retry limit exceeded Nonfatal

4.13.17 IMI_NERR: IMI Next Errors (D{8,10,12,14}, F0)

If an error is already logged in the IMI_FERR register, all subsequent errors are logged in the IMI_NERR. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 8, 10, 12, 14 Function: 0 Offset: C4h - C7h			
Bit	Attr	Default	Description
31:15	RV	00h	Reserved
14	RWCST	0	IMI14Err: The NB Received a Fatal Error signal from the XMB Fatal
13	RWCST	0	IMI13Err: Failed on last retry. Co-exist with IMI9Err Nonfatal
12	RWCST	0	IMI12Err: The NB received an uncorrectable error signal from XMB. Nonfatal
11	RWCST	0	IMI11Err: The NB received a correctable error signal from XMB. Nonfatal
10	RWCST	0	IMI10Err: The NB is sending a “poisoned” Config Write to XMB. Nonfatal
9	RWCST	0	IMI9Err: Failed on last retry. Co-exist with IMI13Err Nonfatal
8	RWCST	0	IMI8Err: Outstanding Requests are posted to a failed IMI Link Nonfatal
7	RWCST	0	IMI7Err: SMBus Hot-Plug error. Nonfatal
6	RWCST	0	IMI6Err: Abort Nonfatal
5	RWCST	0	IMI5Err: Inbound link layer control error. Idle flit sequence error Link Layer Format Sequence Errors Bad Data Size, info bit sequence error Aperture Violation Invalid Tag Nonfatal
4	RWCST	0	IMI4Err: Memory write data poisoned. The NB has poisoned the flit that contains the error and written the data to memory. Nonfatal

Device: 8, 10, 12, 14 Function: 0 Offset: C4h - C7h			
Bit	Attr	Default	Description
3	RWCST	0	IMI3Err: Inbound CRC Error May or may not get an M7 as well. Nonfatal
2	RWCST	0	IMI2Err: command time-out Nonfatal
1	RWCST	0	IMI1Err: Correctable error in read return packet Nonfatal
0	RWCST	0	IMI0Err: Uncorrectable error in read return packet before retry limit exceeded Nonfatal

4.13.18 NRECIMI: Non-recoverable IMI Error Log Register (D{8,10,12,14}, F0)

This register latches information when the IMI_FERR latches the first detected fatal error.

Device: 8, 10, 12, 14 Function: 0 Offset: D4h - D5h			
Bit	Attr	Default	Description
15:8	ROST	00h	NR_IMI_Tran_ID : IMI Transaction ID of the failed request
7:0	ROST	00h	NR_IMI_CDC_Tag_ID : CDC TAG ID of the failed request

4.13.19 RECIMI: Recoverable IMI Error Log Register (D{8,10,12,14}, F0)

This register latches information when the IMI_FERR latches the first detected non-fatal error.

Device: 8, 10, 12, 14 Function: 0 Offset: D6h - D7h			
Bit	Attr	Default	Description
15:8	ROST	00h	Rec_IMI_Tran_ID : IMI Transaction ID of the failed request
7:0	ROST	00h	Rec_IMI_CDC_Tag_ID : CDC TAG ID of the failed request

4.13.20 REDIMIL: Recoverable Data IMI Error Log Register (D{8,10,12,14}, F0)

This register latches information when the IMI_FERR latches the first detected non-fatal error.

Device: 8, 10, 12, 14 Function: 0 Offset: D8h - DBh			
Bit	Attr	Default	Description
31:0	ROST	00000000h	Syndrome: Syndrome Bits ECC syndrome of correctable error.

4.13.21 REDIMIH: Recoverable IMI Error Log Register (D{8,10,12,14}, F0)

This register latches information when the IMI_FERR latches the first detected non-fatal error.

Device: 8, 10, 12, 14 Function: 0 Offset: DCh - DDh			
Bit	Attr	Default	Description
15:0	ROST	0000h	ECC_Locator: identifies the symbol in error for correctable errors The bit set identifies which DRAM had the bit in error according to the following list: Bit 0: DRAM0, channel 0 had the error Bit 1: DRAM1, channel 0 had the error Bit 2: DRAM2, channel 0 had the error Bit 3: DRAM3, channel 0 had the error Bit 4: DRAM4, channel 0 had the error Bit 5: DRAM5, channel 0 had the error Bit 6: DRAM6, channel 0 had the error Bit 7: DRAM7, channel 0 had the error Bit 8: DRAM0, channel 1 had the error Bit 9: DRAM1, channel 1 had the error Bit 10: DRAM2, channel 1 had the error Bit 11: DRAM3, channel 1 had the error Bit 12: DRAM4, channel 1 had the error Bit 13: DRAM5, channel 1 had the error Bit 14: DRAM6, channel 1 had the error Bit 15: DRAM7, channel 1 had the error <i>Using the NB locator bits, it is not possible to determine if the error is present in DRAM8 on either channel 0 or channel 1.</i>

4.13.22 EMASK_IMI[3:0]: IMI Error Mask Register (D{8,10,12,14}, F0)

For details on errors listed on this table, refer to the Table 6-39 "Errors Detected by the NB" on page 328. A '0' in any field enables that error.

Device: 8, 10, 12, 14 Function: 0 Offset: DEh - DFh			
Bit	Attr	Default	Description
15	RV	1	Reserved
14	RW	1	IMI14Msk: The NB Received a fatal error from the XMB
13	RW	1	IMI13Msk: Failed on last retry. Co-exist with IMI9Msk
12	RW	1	IMI12Msk: The NB Received a uncorrectable error from the XMB
11	RW	1	IMI11Msk: The NB Received a correctable error signal from XMB
10	RW	1	IMI10Msk: The NB is sending a "poisoned" Config Write to XMB
9	RW	1	IMI9Msk: Failed on last retry. Co-exist with IMI13Msk
8	RW	1	IMI8Msk: Outstanding Requests are posted to a failed IMI Link
7	RW	1	IMI7Msk: SMBus Hot-Plug error
6	RW	1	IMI6Msk: Inbound link abort
5	RW	1	IMI11Msk: Inbound link layer control error. Idle Flit Sequence Error Link Layer Format Sequence Errors Bad Data Size, Info Bit Sequence Error Aperture Violation Invalid Tag
4	RW	1	IMI4Msk: Memory write data poisoned The NB has poisoned the flit that contains the error and written the data to memory.
3	RW	1	IMI3Msk: Inbound CRC Error
2	RW	1	IMI2Msk: 1st Request Time-out
1	RW	1	IMI1Msk: Inbound Correctable ECC Error
0	RW	1	IMI0Msk: Inbound UnCorrectable ECC Error #1

4.13.23 IMI_ERR0: IMI Error 0 Enable Register (D{8,10,12,14}, F0)

This register enables the signaling of Err[0] when an error flag is set. Note that one (and only one) error signal should be enabled. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 8, 10, 12, 14 Function: 0 Offset: E0h - E1h			
Bit	Attr	Default	Description
15	RV	0	Reserved
14	RWST	0	IMI14Err0Sel: The NB Received a fatal error from the XMB
13	RWST	0	IMI13Err0Sel: Failed on last retry. Co-exist with IMI9Err0Sel
12	RWST	0	IMI12Err0Sel: The NB Received a uncorrectable error from the XMB
11	RWST	0	IMI11Err0Sel: The NB Received a correctable error signal from XMB
10	RWST	0	IMI10Err0Sel: The NB is sending a “poisoned” Config Write to XMB
9	RWST	0	IMI9Err0Sel: Failed on last retry Co-exist with IMI13Err0Sel
8	RWST	0	IMI8Err0Sel: Outstanding Requests are posted to a failed IMI Link
7	RWST	0	IMI7Err0Sel: VPP SMBus Hot-Plug error
6	RWST	0	IMI6Err0Sel: Inbound link abort
5	RWST	0	IMI5Err0Sel: Inbound link layer control error Idle Flit Sequence Error Link Layer Format Sequence Errors Bad Data Size, Info Bit Sequence Error Aperture Violation Invalid Tag
4	RWST	0	IMI4Err0Sel: Memory write data poisoned The NB has poisoned the flit that contains the error and written the data to memory
3	RWST	0	IMI3Err0Sel: Inbound CRC Error
2	RWST	0	IMI2Err0Sel: 1st Request Time-out
1	RWST	0	IMI1Err0Sel: Inbound Correctable ECC Error
0	RWST	0	IMI0Err0Sel: Inbound UnCorrectable ECC Error #1

4.13.24 IMI_ERR1: IMI Error 1 Enable Register (D{8,10,12,14}, F0)

This register enables the signaling of Err[1] when an error flag is set. Note that one and only one error signal should be enabled. For details on errors listed on this table, refer to the Table 6-39 "Errors Detected by the NB" on page 328.

Device: 8, 10, 12, 14 Function: 0 Offset: E2h - E3h			
Bit	Attr	Default	Description
15	RV	0	Reserved
14	RWST	0	IMI14Err1Sel: The NB Received a fatal error from the XMB
13	RWST	0	IMI13Err1Sel: Failed on last retry. Co-exist with IMI9Err1Sel
12	RWST	0	IMI12Err1Sel: The NB Received a uncorrectable error from the XMB
11	RWST	0	IMI11Err1Sel: The NB Received a correctable error signal from XMB
10	RWST	0	IMI10Err1Sel: The NB is sending a "poisoned" Config Write to XMB
9	RWST	0	IMI9Err1Sel: Failed on last retry Co-exist with IMI13Err1Sel
8	RWST	0	IMI8Err1Sel: Outstanding Requests are posted to a failed IMI Link
7	RWST	0	IMI7Err1Sel: VPP SMBus Hot-Plug error
6	RWST	0	IMI6Err1Sel: Inbound link abort
5	RWST	0	IMI5Err1Sel: Inbound link layer control error Idle Flit Sequence Error Link Layer Format Sequence Errors Bad Data Size, Info Bit Sequence Error Aperture Violation Invalid Tag
4	RWST	0	IMI4Err1Sel: Memory write data poisoned The NB has poisoned the flit that contains the error and written the data to memory
3	RWST	0	IMI3Err1Sel: Inbound CRC Error
2	RWST	0	IMI2Err1Sel: 1st Request Time-out
1	RWST	0	IMI1Err1Sel: Inbound Correctable ECC Error
0	RWST	0	IMI0Err1Sel: Inbound UnCorrectable ECC Error #1

4.13.25 IMI_ERR2: IMI Error 2 Enable Register(D{8,10,12,14}, F0)

This register enables the signaling of Err{2} when an error flag is set. Note that one and only one error signal should be enabled. For details on errors listed on this table, refer to the Table 6-39 “Errors Detected by the NB” on page 328.

Device: 8, 10, 12, 14 Function: 0 Offset: E4h - E5h			
Bit	Attr	Default	Description
15	RV	0	Reserved
14	RWST	0	IMI14Err2Sel: The NB Received a fatal error from the XMB
13	RWST	0	IMI13Err2Sel: Failed on last retry. Co-exist with IMI9Err2Sel
12	RWST	0	IMI12Err2Sel: The NB Received a uncorrectable error from the XMB
11	RWST	0	IMI11Err2Sel: The NB Received a correctable error signal from XMB
10	RWST	0	IMI10Err2Sel: The NB is sending a “poisoned” Config Write to XMB
9	RWST	0	IMI9Err2Sel: Failed on last retry. Co-exist with IMI13Err2Sel
8	RWST	0	IMI8Err2Sel: Outstanding Requests are posted to a failed IMI Link
7	RWST	0	IMI7Err2Sel: VPP SMBus Hot-Plug error
6	RWST	0	IMI6Err2Sel: Inbound link abort
5	RWST	0	IMI5Err2Sel: Inbound link layer control error IDle Flit Sequence Error Link Layer Format Sequence Errors Bad Data Size, Info Bit Sequence Error Aperture Violation Invalid Tag
4	RWST	0	IMI4Err2Sel: Memory write data poisoned The NB has poisoned the flit that contains the error and written the data to memory
3	RWST	0	IMI3Err2Sel: Inbound CRC Error
2	RWST	0	IMI2Err2Sel: 1st Request Time-out
1	RWST	0	IMI1Err2Sel: Inbound Correctable ECC Error
0	RWST	0	IMI0Err2Sel: Inbound UnCorrectable ECC Error #1

4.13.26 IMI_MCERR: IMI MCERR Enable Register (D{8,10,12,14}, F0)

This register enables the signaling of MCERR when an error flag is set. Note that one and only one error signal should be enabled.

Device: 8, 10, 12, 14 Function: 0 Offset: E6h - E7h			
Bit	Attr	Default	Description
15	RV	0	Reserved
14	RW	0	IMI14MCErrSel: The NB Received a fatal error from the XMB
13	RW	0	IMI13MCErrSel: Failed on Last retry. Co-exist with IMI9MCErrSel
12	RW	0	IMI12MCErrSel: The NB Received a uncorrectable error from the XMB
11	RW	0	IMI11MCErrSel: The NB Received a correctable error signal from XMB
10	RW	0	IMI10MCErrSel: The NB is sending a “poisoned” Config Write to XMB
9	RW	0	IMI9MCErrSel: Failed on Last retry. Co-exist with IMI13MCErrSel
8	RW	0	IMI8MCErrSel: Outstanding Requests are posted to a failed IMI Link
7	RW	0	IMI7MCErrSel: VPP SMBus Hot-Plug error
6	RW	0	IMI6MCErrSel: Inbound link abort
5	RW	0	IMI5MCErrSel: Inbound link layer control error Idle Flit Sequence Error Link Layer Format Sequence Errors Bad Data Size, Info Bit Sequence Error Aperture Violation Invalid Tag
4	RW	0	IMI4MCErrSel: Memory write data poisoned The NB has poisoned the flit that contains the error and written the data to memory
3	RW	0	IMI3MCErrSel: Inbound CRC Error
2	RW	0	IMI2MCErrSel: 1st Request Time-out
1	RW	0	IMI1MCErrSel: Inbound Correctable ECC Error
0	RW	0	IMI0MCErrSel: Inbound UnCorrectable ECC Error #1

4.14 Front Side Bus, Boot and Interrupt Registers (Device 16, Function 0)

The Front Side Bus, Boot and Interrupt registers are in Device 16 (D16), function 0 (F0). For the register address map, please refer to Table 4-14.

Warning: Address locations that are not listed are considered reserved locations. Writes to “Reserved” registers may cause unpredictable behavior. Reads to “Reserved” registers may return a non-zero value.

4.14.1 VID: Vendor Identification Register (D16, F0)

This register identifies Intel as the manufacturer of the Intel® E8501 chipset North Bridge (NB). Writes to this register have no effect.

Device: 16 Function: 0 Offset: 00 - 01h			
Bit	Attr	Default	Description
15:0	RO	8086h	Vendor Identification Number The value assigned to Intel.

4.14.2 DID: Device Identification Register (D16, F0)

This register, combined with the Vendor Identification register, uniquely identifies the NB. Writes to this register have no effect. All PCI Express devices will have the same DID in each function. All IMI devices will have the same DID in each function.

Device: 16 Function: 0 Offset: 02 - 03h			
Bit	Attr	Default	Description
15:0	RO	2610h	Device Identification Number Identifies each function of the NB.

4.14.3 RID: Revision Identification Register (D16, F0)

This register contains the revision number of the Intel® E8501 chipset North Bridge (NB).

Device: 16 Function: 0 Offset: 08h			
Bit	Attr	Default	Description
7:4	RO	0h	Major_rev: Major Revision Steppings which require all masks to be regenerated. 1: B stepping
3:0	RO	0h	Minor_rev: Minor Revision Incremented for each stepping which does not modify all masks. Reset for each major revision. 0: x0 stepping 1: x1 stepping 2: x2 stepping

4.14.4 CCR: Class Code Register (D16, F0)

This register contains the Class Code for the device.

Device: 16 Function: 0 Offset: 09h			
Bit	Attr	Default	Description
23:16	RO	06h	Base Class This field indicates the general device category. For the NB, this field is hardwired to 06h, indicating it is a "Bridge Device"
15:8	RO	00h	Sub-Class This field qualifies the Base Class, providing a more detailed specification of the device function. For the NB, this field is hardwired to 00h, indicating it is a "Host Bridge".
7:0	RO	00h	Register-Level Programming Interface This field identifies a specific programming interface (if any), that device-independent software can use to interact with the device. There are no such interfaces defined for "Host Bridge" types, and this field is hardwired to 00h.

4.14.5 HDR: Header Type Register (D16, F0)

This register identifies the header layout of the configuration space.

Device: 16 Function: 0 Offset: 0Eh			
Bit	Attr	Default	Description
7	RO	1h	Mfd: Multi-function Device. Selects whether this is a multi-function device, that may have alternative configuration layouts.
6:0	RO	00h	CfgLayout: Configuration Layout. This field identifies the format of the configuration header layout for a PCI-to-PCI bridge from bytes 10h through 3Fh. For this device the default is 00h, indicating a conventional type 00h PCI header.

4.14.6 SVID: Subsystem Vendor Identification Register (D16, F0)

This register identifies the manufacturer of the system. This 16-bit register combined with the Device Identification Register, uniquely identifies any PCI device.

Device: 16 Function: 0 Offset: 2Ch			
Bit	Attr	Default	Description
15:0	RWO	8086h	Vendor Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to a byte will have no effect.

4.14.7 SID: Subsystem Identity (D16, F0)

This register identifies the system.

Device: 16 Function: 0 Offset: 2Eh - 2Fh			
Bit	Attr	Default	Description
15:0	RWO	8086h	Subsystem Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to a byte will have no effect.

4.14.8 SYRE: System Reset (D16, F0)

This register controls NB reset behavior. Any resets produced by a write to this register must be delayed until the configuration write is completed on the initiating interface (Front Side Bus, PCI Express, HI, SMBus and JTAG).

Device: 16 Function: 0 Offset: 40h - 41h			
Bit	Attr	Default	Description
15	RV	0	Reserved
14	RW	0	CPURST: Processor Reset If set, the NB will assert processor RESET# immediately on both buses.
13	RV	0	Reserved
12	RW	0	SYSRST: System Hard Reset The rising edge on this bit will lead to the assertion of the ICHRST# pin. The timing of this ICHRST# assertion should not be affected by Hard Reset.
11:10	RW	00h	REFIMI: Refresh from IMI to Gate ROR Designates the PMI to supply the inband REFRESH for ROR-initiated processor reset. 00: IMI A 01: IMI B 10: IMI C 11: IMI D
9	RW	0	ROR: Processor Reset on Refresh If set, the NB will assert processor H_{A/B}_RST# on both buses when a "Refresh Cycle Complete" signal is received on the IMI designated by REFIMI.
8:0	RV	00h	Reserved

4.14.9 REDIRCTL: Redirection Control Register (D16, F0)

This register controls the priority algorithm of the XTPR interrupt redirection mechanism.

Device: 16 Function: 0 Offset: 50h - 51h			
Bit	Attr	Default	Description
15:14	RV	0	Reserved
13	RW	0	FFS: 0: Use an LRU algorithm to send interrupt to highest XTPR index value when tie. 1: Do not use the LRU algorithm in case of ties, instead, the highest XTPR index in the valid pool will always be chosen. This emulates the legacy policy.
12	RW	0	ARBRST: Arbitration Reset Neither BIOS nor the OS should use this bit. 1: This bit resets the arbitration LRU state to a known state for repeatability of tests.
11:8	RW	Ch	BUCKET2: First priority number not in BUCKET0, BUCKET1, or BUCKET2 Must be programmed with the same or larger value than BUCKET1 . Suggested Value: 0h
7:4	RW	8h	BUCKET1: First priority number not in BUCKET0 or BUCKET1 Must be programmed with the same or larger value than BUCKET0 . Suggested Value: 0h
3:0	RW	4h	BUCKET0: First priority number not in BUCKET0 Suggested Value: 0h

4.14.10 REDIRDIS: Redirection Disable Register (D16, F0)

This register allows software to force *xtptr_updates* from the given agent to be ignored. The agent number is specified by the thread index as described in eXternal Task Priority Registers, Section 4.14.14.

Device: 16 Function: 0 Offset: 54h - 57h			
Bit	Attr	Default	Description
31:0	RW	00h	DIS: Disable XTPR_Updates from Agent Each bit corresponds to one agent, and each bit has the following usage semantics: 0: Allow XTPR_Updates from this agent. 1: Ignore XTPR_Updates from this agent.

4.14.11 REDIRBUCKETS: Redirection Bucket Number Register (D16, F0)

This register allows software to read the current hardware bucket number assigned to each XTPR register.

Device: 16 Function: 0 Offset: 58h - 5Bh			
Bit	Attr	Default	Description
31:30	RO	00	BUCKET15: Redirection bucket number for XTPR[15]
29:28	RO	00	BUCKET14: Redirection bucket number for XTPR[14]
27:26	RO	00	BUCKET13: Redirection bucket number for XTPR[13]
25:24	RO	00	BUCKET12: Redirection bucket number for XTPR[12]
23:22	RO	00	BUCKET11: Redirection bucket number for XTPR[11]
21:20	RO	00	BUCKET10: Redirection bucket number for XTPR[10]
19:18	RO	00	BUCKET9: Redirection bucket number for XTPR[9]
17:16	RO	00	BUCKET8: Redirection bucket number for XTPR[8]
15:14	RO	00	BUCKET7: Redirection bucket number for XTPR[7]
13:12	RO	00	BUCKET6: Redirection bucket number for XTPR[6]
11:10	RO	00	BUCKET5: Redirection bucket number for XTPR[5]
9:8	RO	00	BUCKET4: Redirection bucket number for XTPR[4]
7:6	RO	00	BUCKET3: Redirection bucket number for XTPR[3]
5:4	RO	00	BUCKET2: Redirection bucket number for XTPR[2]
3:2	RO	00	BUCKET1: Redirection bucket number for XTPR[1]
1:0	RO	00	BUCKET0: Redirection bucket number for XTPR[0]

4.14.12 POC_FSB{A/B}: Power-on Configuration (D16, F0)

Contrary to its name, this register defines configuration values driven at reset by the NB to the CPU. This register only provides non-default configuration strapping on resets subsequent to the first reset.

The NB drives the contents of this register on A[35:4]# whenever it asserts H_{A/B}_RST#. These values are driven during processor RESET# assertion, and for three host clocks past the trailing edge of processor RESET#.

This register is sticky through reset; that is, the contents of the register remain unchanged during and following a Hard Reset. This allows system configuration software to modify the default values and reset the system to pass those values to all host bus devices. The default values shown in the table represent the state of the register following a *power-good* or *power-up* reset.

The POC_FSB{A/B} bits do not affect the NB operation except for driving A[35:4]#. In order to enable external system logic to override the values driven by the NB, the value sampled on A[7]# can force the NB IOQ depth to 1.

There are other power-on configuration bits in the SYRE register (Section 4.14.8) and POC_AUX{A/B} registers (Section 4.14.13).

Device: 16 Function: 0 Offset: 60h - 63h, 70h - 73h			
Bit	Attr	Default	Description
31:28	RV	0h	Reserved
27	RWST	0h	MTDIS: Disable Multi-Threading If set, A[31]# is asserted, and the processor will disable Multi-threading.
26	RV	0	Reserved
25	RWST	0	A29: A[29]# Value The use of this address bit during reset is reserved by the processor.
24	RV	0	Reserved
23	RWST	0	A27: A[27]# Value The use of this address bit during reset is reserved by the processor.
22	RWST	0	A26: A[26]# Value The use of this address bit during reset is reserved by the processor.
21	RWST	0	A25: A[25]# Value The use of this address bit during reset is reserved by the processor.
20	RWST	0	A24: A[24]# Value The use of this address bit during reset is reserved by the processor.
19	RV	0h	Reserved
18	RWST	0	A22: A[22]# Value The use of this address bit during reset is reserved by the processor.
17:12	RWST	00h	CLKRATIO: Processor core to bus clock ratio A[21:16]# define the bus-to-core clock ratio for the processor.
11	RWST	1	BUSPARK: Request Bus Parking Disable If set, A[15]# is asserted and the processor may not park on the front side bus.
10	RV	0	Reserved
9	RWST	0	A13: Drive A[13]# The use of this address bit during reset is reserved by the processor.
8	RWST	0	APICID1: APIC Cluster ID [1] If set, A[12]# is asserted.
7	RWST	0	APICID0: APIC Cluster ID [0] The NB will always assert A[11]# on FSB B, regardless of the value of APICID0. For FSB A, this bit can control the assertion of A[11]#. The default value of 0 causes A[11]# on FSB A to be deasserted.
6	RWST	0	DISBINIT: Disable BINIT# Observation If set, A[10]# will be asserted and All host bus agents will disable BINIT# observation logic.

Device: 16 Function: 0 Offset: 60h - 63h, 70h - 73h			
Bit	Attr	Default	Description
5	RWST	0	DISERR: Disable MCERR# Input If set, A[9]# will be asserted and all processors will disable MCERR# observation.
4	RWST	0	A8: Drive A[8]# The use of this address bit during reset is reserved by the processor
3	RWST	0	IOQDEP: In-Order Queue Depth 1 If set, A[7]# will be asserted, and all agents on the host bus will limit their In-Order Queue Depth to 1 (i.e. no pipelining support). The NB must sample the value on A[7]# rather than use this register bit directly so that this feature can be forced by external means.
2:0	RWST	0	A6DT4: Drive A[6:4]# The use of these address bits during reset is reserved by the processor A[6]# is not used for 1M reset vector by the processor.

4.14.13 POC_AUX{A/B}: CPU Tristate Control (D16, F0)

These registers are extensions of the POC registers, unique to each bus. POC_AUXA controls FSB A, and POC_AUXB controls FSB B.

The NB drives the contents of these registers on A[39:36]# whenever it asserts H_{A/B}_RST#. These values are driven during processor RESET# assertion and for two host clocks past the trailing edge of processor RESET#.

These registers are sticky through reset; that is, the contents of the registers remain unchanged during and following a Hard Reset. This allows system configuration software to modify the default values and reset the system to pass those values to all host bus devices. The default values shown below represent the state of the register following a *power-good* or *power-up* reset.

Device: 16 Function: 0 Offset: 64h, 74h			
Bit	Attr	Default	Description
7:5	RV	0	Reserved
4	RWST	0h	BISTEN: CPU Built In Self Test Enable If set, A[3]# is asserted and the processor will perform BIST when reset.

Device: 16			
Function: 0			
Offset: 64h, 74h			
Bit	Attr	Default	Description
3:0	RWST	0	CPUKILL: Processor Kill
			Software may set processor kill bits when the corresponding processor is not present so that these bits can be used to reflect the number of working processors connected to the NB.
			When cleared, the associated processor will be allowed to participate in the boot following the next reset.
			When set, the NB will assert the associated front side bus address pin the next time it asserts processor RESET#. A processor is tri-stated when it's address input and it's associated bus request input are asserted during POC according to the following table:
			Bit[3]: A[39]# is asserted, tristating Agent 3
			Bit[2]: A[38]# is asserted, tristating Agent 2
Bit[1]: A[37]# is asserted, tristating Agent 1			
Bit[0]: A[36]# is asserted, tristating Agent 0			

4.14.14 XTPR[15:0]: eXternal Task Priority Registers (D16, F0)

These registers define the re-directable interrupt priority for xAPIC agents connected to the NB.

For convenience and 4-P dual-core, multi thread support, the NB defines a 5-bit thread index to uniquely identify every possible thread. This thread index is formed as:

```
thread_index = (fsb_num, DID[6:3], Attr[6:5])
```

For indexing into the 16 XTPR registers, a carefully chosen function is used:

```
xtpr_index[3] = thread_index[4]
xtpr_index[2] = thread_index[2]
xtpr_index[1] = thread_index[1] XOR thread_index[3]
xtpr_index[0] = thread_index[0] XOR thread_index[1]
```

The NB only has 16 XTPR registers, so to support 16 threads (4 sockets of 2 cores of 2 threads each), the NB allows software to choose which threads will be disabled and ignored. This allows support for 4 sockets of single cores or 4 sockets of dual cores without needing any software reprogramming, and allows 4 sockets of dual cores to operate if the appropriate bits in the REDIRDIS[31:0] register are set.

These registers are used for lowest priority delivery through interrupt redirection by the chipset.

4.14.14.1 XTPR0: External Task Priority 0 (D16, F0)

Device: 16 Function: 0 Offset: 80h - 83h			
Bit	Attr	Default	Description
31	RW	0	CLUSTER: Global Cluster Mode (XTPR[0] only) Used in interrupt redirection for lowest priority delivery. Updated by every xTPR_Update transaction on either bus (Aa[3]). 0: Flat 1: Cluster
30:24	RV	00h	Reserved.
23	RW	0	TPREN: TPR Enable This bit reflects the value of Ab[31]#. When Ab[31]# is asserted, the value of this bit will be 0h.
22:20	RV	0h	Reserved
19:16	RW	0h	PRIORITY: Task Priority The processor with the lowest enabled value will be assigned the re-directable interrupt. This field is updated with Ab[27:24] of the xTPR_Update transaction.
15:8	RW	0	PHYSID: Physical APIC ID The physical ID of the APIC agent associated with the XTPR entry.
7:0	RW	0	LOGID: Logical APIC ID The logical ID of the APIC agent associated with the XTPR entry. This field is updated with Aa[11:4] of the xTPR_Update transaction.

4.14.14.2 XTPR[15:1]: External Task Priority 1-15 (D16, F0)

Device: 16 Function: 0 Offset: (88h - 8Bh), (90h - 93h), (98h - 9Bh), (A0h - A3h), (A8h - ABh), (B0h - B3h), (B8h - BBh)			
Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23	RW	0	TPREN: TPR Enable This bit reflects the value of Ab[31]#. When Ab[31]# is asserted, the value of this bit will be 0h.
22:20	RV	0h	Reserved
19:16	RW	0h	PRIORITY: Task Priority The processor with the lowest enabled value will be assigned the re-directable interrupt. This field is updated with Ab[27:24] of the XTPR_Update transaction.
15:8	RW	00h	PHYSID: Physical APIC ID The physical ID of the APIC agent associated with the XTPR entry
7:0	RW	00h	LOGID: Logical APIC ID The logical ID of the APIC agent associated with the XTPR entry. This field is updated with Aa[11:4] of the xTPR_Update transaction.

4.14.15 BOFL[3:0]: Boot Flag (D16, F0)

These registers can be used to select the system boot strap processor or for other cross processor communication purposes. When this register is read, the contents of the register is cleared. Therefore, a processor that reads a non-zero value owns the semaphore. Any value can be written to this register at any time.

An example of usage would be for all processors to read the register. The first one gets a non-zero value and owns the semaphore. Since the read clears the value of the register, all other processors will see a zero value and will spin until they receive further notification. After the winning processor is done, it writes a non-zero value of its choice into the register, arming it for subsequent uses. These registers are also aliased to fixed memory addresses.

Device: 16 Function: 0 Offset: (C0h - C3h), (C4h - C7h), (C8h - CBh), (CCh - CFh)			
Bit	Attr	Default	Description
31:0	RCW	A5A5A5A5h	SemaVal: Semaphore Value Can be written to any value. Value is cleared when there is a read.

4.14.16 SPAD[3:0]: Scratch Pad (D16, F0)

These scratch pad registers each provide 32 read/writable bits that can be used by software. They are also aliased to fixed memory addresses.

Device: 16 Function: 0 Offset: (D0h - D3h), (D4h - D7h), (D8h - DBh), (DCh - DFh)			
Bit	Attr	Default	Description
31:0	RW	00000000h	Scratch Pad Value These bits have no effect on the hardware.

4.14.17 SPADS[3:0]: Sticky Scratch Pad (D16, F0)

These sticky scratch pad registers each provide 32 read/writable bits that can be used by software. They are also aliased to fixed memory addresses.

Device: 16 Function: 0 Offset: (E0h - E3h), (E4h - E7h), (E8h - EBh), (ECh - EFh)			
Bit	Attr	Default	Description
31:0	RWST	00000000h	Scratch Pad Value These sticky bits have no effect on the hardware.

4.15 Address Mapping (Device 16, Function 1)

The address mapping registers control transaction routing to the Independent Memory Interface types based on address. The Address Mapping registers are in Device 16 (D0), function 1 (F1). For the register address `inap`, please refer to [Table 4-15](#).

Warning: Address locations that are not listed are considered reserved locations. Writes to “Reserved” registers may cause unpredictable behavior. Reads to “Reserved” registers may return a non-zero value.

4.15.1 VID: Vendor Identification Register (D16, F1)

This register identifies Intel as the manufacturer of the NB. Writes to this register have no effect.

Device 16 Function: 1 Offset: 00 - 01h			
Bit	Attr	Default	Description
15:0	RO	8086h	Vendor Identification Number The value assigned to Intel.

4.15.2 DID: Device Identification Register (D16, F1)

This register combined with the Vendor Identification register uniquely identifies the NB Function in the event that a driver is required. Writes to this register have no effect.

Device 16 Function: 1 Offset: 02 - 03h			
Bit	Attr	Default	Description
15:0	RO	2611h	Device Identification Number Identifies each function of the NB.

4.15.3 RID: Revision Identification Register (D16, F1)

This register contains the revision number of the Intel® E8501 chipset North Bridge (NB).

Device: 16 Function: 1 Offset: 08h			
Bit	Attr	Default	Description
7:4	RO	0h	Major_rev: Major Revision Steppings which require all masks to be regenerated. 1: B stepping
3:0	RO	0h	Minor_rev: Minor Revision Incremented for each stepping which does not modify all masks. Reset for each major revision. 0: x0 stepping 1: x1 stepping 2: x2 stepping

4.15.4 CCR: Class Code Register (D16, F1)

This register contains the Class Code for the device.

Device: 16 Function: 1 Offset: 09 - 0Bh			
Bit	Attr	Default	Description
23:16	RO	06h	BaseClass: Base Class This field indicates the general device category. For the NB , this field is hardwired to 06h, indicating it is a "Bridge Device".
15:8	RO	00h	SubClass: Sub-Class This field qualifies the Base Class, providing a more detailed specification of the device function. For this Device the default is 00h, indicating "Host Bridge".
7:0	RO	00h	RLPI: Register-Level Programming Interface This field identifies a specific programming interface (if any), that device independent software can use to interact with the device. There are no such interfaces defined for "Host Bridge" types, and this field is hardwired to 00h.

4.15.5 HDR: Header Type Register (D16, F1)

This register identifies the header layout of the configuration space.

Device: 16 Function: 1 Offset: 0Eh			
Bit	Attr	Default	Description
7	RO	1h	Mfd: Multi-function Device Selects whether this is a multi-function device, that may have alternative configuration layouts. Therefore, the IM! is defined to be a single function device, and this bit is hardwired to '0'.
6:0	RO	0h	CfgLayout: Configuration Layout This field identifies the format of the configuration header layout for a PCI-to-PCI bridge from bytes 10h through 3Fh. For this Device the default is 00h, indicating a conventional type 00h PCI header.

4.15.6 SVID: Subsystem Vendor Identification Register (D16, F1)

This register identifies the manufacturer of the system. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device.

Device: 16 Function: 1 Offset: 2C - 2Dh			
Bit	Attr	Default	Description
15:0	RWO	8086h	VIN: Vendor Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to this register will have no effect.

4.15.7 SID: Subsystem Identity (D16, F1)

This register identifies the system.

Device: 16 Function: 1 Offset: 2E - 2Fh			
Bit	Attr	Default	Description
15:0	RWO	8086h	SID: Subsystem Identification Number The default value specifies Intel. Each byte of this register will be writable once. Second and successive writes to this register will have no effect.

4.15.8 PAM[6:0]: Programmable Attribute MAP (D16, F1)

The NB allows programmable memory attributes on 13 legacy memory segments of various sizes in the 640 KB to 1 MB address range. 7 Programmable Attribute Map (PAM) Registers are used to support these features.

Each PAM Register controls one or two regions (typically 16 KB in size).

4.15.8.1 PAM0: Programmable Attribute Map 0

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h-0FFFFh.

Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the processor read accesses to the corresponding memory segment are claimed by the NB and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to H1.5 (ICH5) to be directed to the PCI bus.

WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the NB and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to H1.5 (ICH5) to be directed to the PCI bus.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Device: 16 Function: 1 Offset: 59h													
Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE0: 0F0000-0FFFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0F0000h to 0FFFFh. Bit 5 = Write enable, Bit 4 = Read enable <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:0	RV	00h	Reserved										

4.15.8.2 PAM1: Programmable Attribute Map 1

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h-0C7FFFh.

Device: 16
Function: 1
Offset: 5Ah

Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE1: 0C4000-0C7FFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0C4000h to 0C7FFFh. Bit 5 = Write enable, Bit 4 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:2	RV	00	Reserved										
1:0	RW	00	LOENABLE1: 0C0000-0C3FFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0C0000h to 0C3FFFh. Bit 1 = Write enable, Bit 0 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												

4.15.8.3 PAM2: Programmable Attribute Map 2

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h-0CFFFFh.

Device: 16													
Function: 1													
Offset: 5Bh													
Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE1: 0CC000h- 0CFFFFh Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0CC000h to 0CFFFFh. Bit 5 = Write enable, Bit 4 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:2	RV	00	Reserved										
1:0	RW	00	LOENABLE1: 0C8000-0CBFFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0C8000h to 0CBFFFh. Bit 1 = Write enable, Bit 0 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled - All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												

4.15.8.4 PAM3: Programmable Attribute Map 3

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h-0D7FFFh.

Device: 16													
Function: 1													
Offset: 5Ch													
Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE3: 0D4000-0D7FFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0D4000h to 0D7FFFh. Bit 5 = Write enable, Bit 4 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:2	RV	00	Reserved										
1:0	RW	00	LOENABLE3: 0D0000-0D3FFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0D0000h to 0D3FFFh. Bit 1 = Write enable, Bit 0 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												

4.15.8.5 PAM4: Programmable Attribute Map 4

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Device: 16
Function: 1
Offset: 5Dh

Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE4: 0DC000-0DFFFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0DC000h to 0DFFFFh. Bit 5 = Write enable, Bit 4 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:2	RV	00	Reserved										
1:0	RW	00	LOENABLE4: 0D8000-0DBFFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0D8000h to 0DBFFFh. Bit 1 = Write enable, Bit 0 = Read enable <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												

4.15.8.6 PAM5: Programmable Attribute Map 5

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Device: 16 Function: 1 Offset: 5Eh													
Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE5: 0E4000-0E7FFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0E4000h to 0E7FFFh. Bit 5 = Write enable, Bit 4 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:2	RV	00	Reserved										
1:0	RW	00	LOENABLE5: 0E0000-0E3FFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0E0000h to 0E3FFFh. Bit 1 = Write enable, Bit 0 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												

4.15.8.7 PAM6: Programmable Attribute Map 6

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h-0EFFFFh.

Device: 16
Function: 1
Offset: 5Fh

Bit	Attr	Default	Description										
7:6	RV	00	Reserved										
5:4	RW	00	HIENABLE4: 0EC000-0EFFFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0EC000h to 0DFFFFh. Bit 5 = Write enable, Bit 4 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												
3:2	RV	00	Reserved										
1:0	RW	00	LOENABLE4: 0E8000-0EBFFF Attribute Register This field controls the steering of read and write cycles that address the BIOS area from 0E8000h to 0EBFFFh. Bit 1 = Write enable, Bit 0 = Read enable. <table><tr><th>Encoding</th><th>Description</th></tr><tr><td>00</td><td>DRAM Disabled- All accesses are directed to H11.5.</td></tr><tr><td>01</td><td>Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.</td></tr><tr><td>10</td><td>Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.</td></tr><tr><td>11</td><td>Normal DRAM Operation - All reads and writes are serviced by DRAM.</td></tr></table>	Encoding	Description	00	DRAM Disabled - All accesses are directed to H11.5.	01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.	10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.	11	Normal DRAM Operation - All reads and writes are serviced by DRAM.
Encoding	Description												
00	DRAM Disabled - All accesses are directed to H11.5.												
01	Read Only - All reads are serviced by DRAM. Writes are forwarded to H11.5.												
10	Write Only - All writes are sent to DRAM. Reads are serviced by H11.5.												
11	Normal DRAM Operation - All reads and writes are serviced by DRAM.												

4.15.9 FDHC: Fixed DRAM Hole Control (D16, F1)

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

Device: 16 Function: 1 Offset: 60h			
Bit	Attr	Default	Description
7	RW	0	HEN: Hole Enable This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0: No memory hole. 1: Memory hole from 15 MB to 16 MB. Accesses in this range will be sent to H11.5.
6:0	RV	00h	Reserved

4.15.10 SMRAMC: System Management RAM Control (D16, F1)

The SMRAMC register controls the accessibility to Compatible and Extended SMRAM spaces. The Open, Close, and Lock bits function only when G_SMROME bit in EXSMRC Register (Section 4.15.11) is set to a "1". Also, the OPEN bit must be reset before the LOCK bit is set.

Device: 16 Function: 1 Offset: 61h			
Bit	Attr	Default	Description
7	RV	0	Reserved
6	RWL	0	D_OPEN: SMM Space Open When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. This register can be locked by D_LCK.
5	RW	0	D_CLS: SMM Space Closed When D_CLS = 1, SMM space DRAM is not accessible to data references (even if SMM decode is active). Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display (even when SMM is mapped over the VGA range). Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	RWL	0	D_LCK: SMM Space Locked When D_LCK is set to 1, then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space (even if the program has knowledge of the D_OPEN function).
3	RV	0	Reserved

Device: 16 Function: 1 Offset: 61h			
Bit	Attr	Default	Description
2:0	RO	010b	C_BASE_SEG: Compatible SMM Space Base Segment This field indicates the location of SMM space. SMM DRAM is not re-mapped. It is simply made visible if the conditions are right to access SMM space. Otherwise, the access is forwarded to H11.5/VGA. Since the NB supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

4.15.11 EXSMRC: Extended System Management RAM Control (D16, F1)

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MByte.

Device: 16 Function: 1 Offset: 62h			
Bit	Attr	Default	Description
7	RWL	0	H_SMRAME: Enable High SMRAM Controls the SMM memory space location (i.e. above 1 MByte or below 1 MByte). When G_SMRAME is 1 and H_SMRAME is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA_0000h to 0FEDB_FFFFh are re-mapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read-only.
6	RO	0	MDAP: MDA Present Since the NB does not support MDA, this bit has no meaning.
5	RW	0	APICDIS:APIC Memory Range Disable When set to '1', the NB forwards accesses to the IOAPIC regions to the appropriate interface, as specified by the memory and PCI configuration registers. When this bit is clear, the NB will send accesses as defined below: between 0_FEC0_0000 and 0_FEC7_FFFF to H11.5, between 0_FEC8_0000 and 0_FEC8_0FFF to PCI Express D, between 0_FEC8_1000 and 0_FEC8_1FFF to PCI Express C0, between 0_FEC8_2000 and 0_FEC8_2FFF to PCI Express C1, between 0_FEC8_3000 and 0_FEC8_3FFF to PCI Express B0, between 0_FEC8_4000 and 0_FEC8_4FFF to PCI Express B1, between 0_FEC8_5000 and 0_FEC8_5FFF to PCI Express A0, between 0_FEC8_6000 and 0_FEC8_6FFF to PCI Express A1.

Device: 16 Function: 1 Offset: 62h			
Bit	Attr	Default	Description
4	RV	0	Reserved
3	RWL	0	G_SMRAME: Global SMRAM Enable If set to a 1, then Compatible SMRAM functions are enabled (providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADS# with SMM decode)). To enable Extended SMRAM function, this bit has to be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes "Read" only. (Moved from SMRAM bit3).
2:1	RWL	00	TSEG_SZ: TSEG Size Selects the size of the TSEG memory block if enabled. Memory from (ESMMTOP - TSEG_SZ) to ESMMTOP is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit (SMMEM#) is set in the request packet. Non-SMM accesses to this memory region are sent to H11.5 when the TSEG memory block is enabled. Note that once D_LCK is set, these bits become read only. The encodings for TSEG_SZ are: 00: 512K 01: 1M 10: 2M 11: 4M
0	RWL	0	T_EN: TSEG Enable Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME = 1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes "Read" only.

4.15.12 EXSMRTOP: Extended System Management RAM Top (D16, F1)

This register defines the location of the Extended (TSEG) SMM range by defining the top of the TSEG SMM range (ESMMTOP).

Device: 16 Function: 1 Offset: 63h			
Bit	Attr	Default	Description
7:4	RV	00h	Reserved

Device: 16 Function: 1 Offset: 63h			
Bit	Attr	Default	Description
3:0	RW	01h	ESMMTOP: Top of Extended SMM Space (TSEG) This field contains address bits 31 to 28. This field points to the top of extended SMM space below 4 GB. Addresses below 4 GB that fall in this range are decoded to be in the extended SMM space and should be routed according to SMM address routing rules: $\text{ESMMTOP-TSEG_SZ} \leq \text{Address} < \text{ESMMTOP}$ ESMMTOP is relocatable to accommodate software that wishes to configure the TSEG SMM space before MMIO space is known. This field defaults to the same value that TOLM defaults to.

4.15.13 EXP_ECBASE: PCI Express Enhanced Configuration Base Address (D16, F1)

This register defines the base address of the enhanced PCI Express configuration memory.

Device: 16 Function: 1 Offset: 68 - 6Bh			
Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23:12	RW	0001h	EXP_ECBASE: PCI Express Enhanced Configuration Base This register contains the address that corresponds to bits 39 to 28 of the base address for PCI Express enhanced configuration space. Configuration software will read this register to determine where the 256 MB range of addresses resides for this particular host bridge. This register defaults to the same address as the default value for TOLM.
11:0	RV	00h	Reserved

4.15.14 TOLM: Top Of Low Memory (D16, F1)

This register contains the maximum address below 4 GB that should be treated as a memory access and is defined on a 256MB boundary.

Device: 16 Function: 1 Offset: 6Ch - 6Dh			
Bit	Attr	Default	Description
15:12	RW	01h	TOLM: Top of Low Memory This register contains the address that corresponds to bits 31 to 28 of the maximum DRAM memory address that lies below 4 GB. Configuration software should set this value to either the maximum amount of memory in the system or to the minimum address allocated for PCI memory (low MMIO), whichever is smaller. Addresses equal to or greater than the TOLM, and less than 4 G, are decoded as low MMIO, MMCFG, Chipset, Interrupt/SMM, or firmware (Hv1.5) as described in the address mapping chapter (Section 5). All accesses less than the TOLM are treated as DRAM accesses (except for the 15-16 MB or PAM gaps). This register must be set to at least 1000h, for a minimum of 256 MB of DRAM. There is also a minimum of 256 MB of PCI space, since this register is on a 256 MB boundary. Configuration software should set this value to either the maximum amount of memory in the system (same as the top IMIR.LIMIT), or to the lower 256 MB boundary of the Memory Mapped I/O range, whichever is smaller. The Memory Mapped I/O range may not get fully configured by software and the NB will send unmapped accesses to ICH5 via subtractive decoding.
11:0	RV	000h	Reserved

4.15.15 IMIR[5:0]: IMI Interleave Range, (D16, F1)

These registers define the IMI that services each address in the main memory space.

Each register defines a range. If the address falls in the range defined by an IMIR, the ways fields in that IMIR define which IMI services accesses with $A[7:6] = A.B.C.D$.

There are 2 sets of ways fields to support mirroring. The first set, Image0, defines the default primary (The default primary is the primary image at reset. After reset, the primary depends on error detection). If $IMG1WAYi$ is set to the same value as $IMG0WAY0$, no mirroring occurs. If they are set to different values, writes are sent to both IMIs and reads are sent to the primary.

To bound validation of this capability and eliminate multiple equivalent configurations, any given configuration must obey one of the following 3 sets of rules for all 4 ways ($i = A,B,C,D$).

- Scenario 1: **No Mirroring:**

Scenario 2: **Mirroring across card:**
If

If

Scenario 3: **Mirroring across XMBs on a card:**
If

If

When the TOLM register is modified, the NB automatically adjusts the IMI interleaving registers to compensate for the new MMIO gap size. This is done by adjusting the limit of each range upward if it is above TOLM as shown in Table 4-23.

Table 4-23. Governing of Interleaving of an Address by IMIR[i]

Limit above TOLM ^a	Match IMIR[i] if
IMIR[i].LIMIT[3:0] <= TOLM[15:12]	IMIR[i].LIMIT[12:0] > A[27:12] >= IMIR[i-1].LIMIT[12:0]
IMIR[i].LIMIT[3:0] > TOLM[15:12]	AIMIR[i].ADJLIMIT[12:0] > A[27:12] >= AIMIR[i-1].ADJLIMIT[12:0] ^b

NOTES:

- a IMIR[i].LIMIT must be greater than or equal to IMIR[i-1].LIMIT
b for IMIR[0], IMIR[i-1] is defined to be 0

Device: 16 Function: 1 Offset: (80h - 83h), (84h - 87h), (88h - 8Bh), (8Ch, 8Fh), (90h, 93h), (94h - 97h)			
Bit	Attr	Default	Description
31:29	RV	0	Reserved
28	RW	0	RFBI: Read from both Images 0: Reads are issued to Image0 when mirroring. Once an error condition occurs that results in degrading to one memory image, reads are directed to the remaining healthy image. 1: Reads are issued to Image1 if A[22] XOR A[12] XOR A[8] when mirroring. Otherwise, the read is issued to Image0. Once an error condition occurs that results in degrading to one memory image, reads are directed to the remaining healthy image.
27:16	RW	000h	LIMIT This field defines the highest address in the range. This field is compared to A[39:28]. To disable range i, set IMIR[i].LIMIT == IMIR[i-1].LIMIT.
15:14	RW	00	IMG1WAY3 This field defines the IMI which services accesses for which A[7:6]=3 and which mirrors the IMI defined by IMG0WAY3.
13:12	RW	00	IMG0WAY3 This field defines the IMI which services accesses for which A[7:6]=3.

Device: 16 Function: 1 Offset: (80h - 83h), (84h - 87h), (88h - 8Bh), (8Ch, 8Fh), (90h, 93h), (94 h - 97h)			
Bit	Attr	Default	Description
11:10	RW	00	IMG1WAY2 This field defines the IMI which services accesses for which A[7:6]=2 and which mirrors the IMI defined by IMG0WAY2.
9:8	RW	00	IMG0WAY2 This field defines the IMI which services accesses for which A[7:6]=2.
7:6	RW	00	IMG1WAY1 This field defines the IMI which services accesses for which A[7:6]=1 and which mirrors the IMI defined by IMG0WAY1.
5:4	RW	00	IMG0WAY1 This field defines the IMI which services accesses for which A[7:6]=1.
3:2	RW	00	IMG1WAY0 This field defines the IMI which services accesses for which A[7:6]=0 and which mirrors the IMI defined by IMG0WAY0.
1:0	RW	00	IMG0WAY0 This field defines the IMI which services accesses for which A[7:6]=0.

4.15.16 AIMIR[6:0]: Address of IMI Range(D16, F1)

For the convenience of software which is trying to determine the physical location to which a front side bus address is sent, 32 scratch bits are associated with each IMIR.

Device: 16 Function: 1 Offset: (A0h - A3h), (A4h - A7h), (A8h - ABh), (ACh - AFh), (B0h - B3h), (B4h - B7h)			
Bit	Attr	Default	Description
31:0	RW	00000000h	ADJLIMIT : Adjusted IMIR Limit

4.15.17 SB_A_IMIR[5:0]: Independent Memory Interface Interleave Range for Front Side Bus A (D16, F1)

This is an additional copy of the IMIR registers duplicated for front side bus A as a micro-architectural convenience. Software must configure SB_A_IMIR[i] the same way as IMIR[i] (for i=0 to 5) before any memory accesses are initiated.

Device: 16 Function: 1 Offset: (C0h - C3h), (C4h - C7h), (C8h - CBh), (CCh - CFh), (D0h - D3h), (D4h - D7h)			
Bit	Attr	Default	Description
31:29	RV	0	Reserved
28	RW	0	RFBI. Read from both Images 0: Reads are issued to Image0 when mirroring. Once an error condition occurs that results in degrading to one memory image, reads are directed to the remaining healthy image. 1: Reads are issues to Image1, if A[22] OR A[12] OR A[8] are asserted when mirroring. Otherwise, the read is issued to Image0. Once an error condition occurs that results in degrading to one memory image, reads are directed to the remaining healthy image.
27:16	RW	000h	LIMIT This field defines the highest address in the range. This field is compared to A[39:28]. To disable range i, set IMIR[i].LIMIT == IMIR[i-1].LIMIT.
15:14	RW	00	IMG1WAY3 This field defines the IMI which services accesses for which A[7:6]=3 and which mirrors the IMI defined by IMG0WAY3.
13:12	RW	00	IMG0WAY3 This field defines the IMI which services accesses for which A[7:6]=3.
11:10	RW	00	IMG1WAY2 This field defines the IMI which services accesses for which A[7:6]=2 and which mirrors the IMI defined by IMG0WAY2.
9:8	RW	00	IMG0WAY2 This field defines the IMI which services accesses for which A[7:6]=2.
7:6	RW	00	IMG1WAY1 This field defines the IMI which services accesses for which A[7:6]=1 and which mirrors the IMI defined by IMG0WAY1.
5:4	RW	00	IMG0WAY1 This field Defines the IMI which services accesses for which A[7:6]=1.
3:2	RW	00	IMG1WAY0 This field defines the IMI which services accesses for which A[7:6]=0 and which mirrors the IMI defined by IMG0WAY0.
1:0	RW	00	IMG0WAY0 This field defines the IMI which services accesses for which A[7:6]=0.

4.15.18 SB_B_IMIR[5:0]: Independent Memory Interface Interleave Range for Front Side Bus B (D16, F1)

This is an additional copy of the IMIR registers duplicated for front side bus B as a micro-architectural convenience. Software must configure SB_B_IMIR[i] the same way as IMIR[i] (for i=0 to 5) before any memory accesses are initiated.

Device: 16 Function: 1 Offset: (E0h - E3h), (E4h - E7h), (E8h - EBh), (ECh - EFh), (F0h - F3h), (F4h - F7h)			
Bit	Attr	Default	Description
31:29	RV	0	Reserved
28	RW	0	RFBI . Read from both Images 0: Reads are issued to Image0 when mirroring. Once an error condition occurs that results in degrading to one memory image, reads are directed to the remaining healthy image. 1: Reads are issues to Image1 if A[22] OR A[12] OR A[8] are asserted when mirroring. Otherwise, the read is issued to Image0. Once an error condition occurs that results in degrading to one memory image, reads are directed to the remaining healthy image.
27:16	RW	000h	LIMIT This field defines the highest address in the range. This field is compared to A[39:28]. To disable range i, set IMIR[i].LIMIT == IMIR[i-1].LIMIT.
15:14	RW	00	IMG1WAY3 This field defines the IMI which services accesses for which A[7:6]=3 and which mirrors the IMI defined by IMG0WAY3.
13:12	RW	00	IMG0WAY3 This field defines the IMI which services accesses for which A[7:6]=3.
11:10	RW	00	IMG1WAY2 This field defines the IMI which services accesses for which A[7:6]=2 and which mirrors the IMI defined by IMG0WAY2.
9:8	RW	00	IMG0WAY2 This field defines the IMI which services accesses for which A[7:6]=2.
7:6	RW	00	IMG1WAY1 This field defines the IMI which services accesses for which A[7:6]=1 and which mirrors the IMI defined by IMG0WAY1.
5:4	RW	00	IMG0WAY1 This field defines the IMI which services accesses for which A[7:6]=1.
3:2	RW	00	IMG1WAY0 This field defines the IMI which services accesses for which A[7:6]=0 and which mirrors the IMI defined by IMG0WAY0.
1:0	RW	00	IMG0WAY0 This field defines the IMI which services accesses for which A[7:6]=0.

4.16 RAS (Device 16, Function 2)

The PCI Express registers are in Device 16 (D16), Function 2 (F2). These registers record the first and next errors, logging, detection masks and signaling mask for the two Front Side Buses and Hub Interface. For the register address map, please refer to Table 4-16.

Warning: Address locations that are not listed are considered reserved locations. Writes to “Reserved” registers may cause unpredictable behavior. Reads to “Reserved” registers may return a non-zero value.

4.16.1 VID: Vendor Identification Register (D16, F2)

This register identifies Intel as the manufacturer of the NB. Writes to this register have no effect.

Device: 16 Function: 2 Offset: 00h - 01h			
Bit	Attr	Default	Description
15:0	RO	8086h	VIN: Vendor Identification Number The value assigned to Intel.

4.16.2 DID: Device Identification Register (D16, F2)

This register combined with the Vendor Identification register uniquely identifies the NB Function in the event that a driver is required. Writes to this register have no effect.

Device: 16 Function: 2 Offset: 02h - 03h			
Bit	Attr	Default	Description
15:0	RO	2612h	DIN: Device Identification Number Identifies each function of the NB.

4.16.3 RID: Revision Identification Register (D16, F2)

This register contains the revision number of the Intel® E8501 chipset North Bridge (NB).

Device: 16 Function: 2 Offset: 08h			
Bit	Attr	Default	Description
7:4	RO	0h	Major_rev: Major Revision Steppings which require all masks to be regenerated. 1: B stepping
3:0	RO	0h	Minor_rev: Minor Revision Incremented for each stepping which does not modify all masks. Reset for each major revision. 0: x0 stepping 1: x1 stepping 2: x2 stepping

4.16.4 CCR: Class Code Register (D16, F2)

This register contains the Class Code for the device.

Device: 16 Function: 2 Offset: 09 - 0Bh			
Bit	Attr	Default	Description
23:16	RO	06h	BaseClass: Base Class This field indicates the general device category. For the NB, this field is hardwired to 06h, indicating it is a "Bridge Device".
15:8	RO	00h	SubClass: Sub-Class This field qualifies the Base Class, providing a more detailed specification of the device function. For this device default is 00h, indicating "Host Bridge".
7:0	RO	00h	RLPI: Register-Level Programming Interface This field identifies a specific programming interface (if any), that device independent software can use to interact with the device. There are no such interfaces defined for "Host Bridge" types, and this field is hardwired to 00h.