

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA, INC., AND
QUALCOMM INCORPORATED,
Petitioner

v.

DAEDALUS PRIME LLC,
Patent Owner.

Case No. IPR2023-00547
U.S. Patent No. 10,705,588

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,705,588**

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LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 10,705,588
Ex-1002	Declaration of Dr. Trevor Mudge
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Ex-1008	U.S. Patent No. 7,392,411 (“Shakkarwar”)
Ex-1009	U.S. Published Patent Application No. 2009/0235108 (“Gold”)
Ex-1010	INTENTIONALLY LEFT BLANK
Ex-1011	INTENTIONALLY LEFT BLANK
Ex-1012	INTENTIONALLY LEFT BLANK
Ex-1013	INTENTIONALLY LEFT BLANK
Ex-1014	INTENTIONALLY LEFT BLANK
Ex-1015	INTENTIONALLY LEFT BLANK
Ex-1016	INTENTIONALLY LEFT BLANK
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Ex-1018	INTENTIONALLY LEFT BLANK
Ex-1019	INTENTIONALLY LEFT BLANK
Ex-1020	Claim Mapping Table

¹ Four-digit pin citations that begin with 0 are to the branded numbers added by Samsung in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

Ex-1021	INTENTIONALLY LEFT BLANK
Ex-1022	Bharadwaj Amrutur, Nandish Mehta, Satyam Dwivedi, and Ajit Gupte, Adaptive Techniques to Reduce Power in Digital Circuits (July 2011)
Ex-1023	Churiwala, Sanjay, Tackling multiple clocks in SoCs, https://www.eetimes.com/tackling-multiple-clocks-in-socs/
Ex-1024	System Bus Fundamentals, http://www.edwardbosworth.com/My5155_Slides/Chapter12/SystemBusFundamentals.htm
Ex-1025	Intel® E8501 Chipset North Bridge (NB), Datasheet (May 2006)
Ex-1026	U.S. Patent No. 8,397,090 to Gunther (“Gunther”)
Ex-1027	U.S. Patent No. 9,086,883 to Thomson (“Thomson”)
Ex-1028	U.S. Patent No. 7,263,457 to White (“White”)
Ex-1029	U.S. Patent No. 8,438,416 to Kocev (“Kocev”)
Ex-1030	U.S. Patent Publication No. 2007/0250736 to Gaskins (“Gaskins”)

I. INTRODUCTION

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Qualcomm, Inc. (collectively, “Petitioner”) request *inter partes* review (“IPR”) of Claims 1-20 of U.S. Patent No. 10,705,588 (“the ’588 Patent”) (Ex-1001), currently assigned to Daedalus Prime LLC (“PO”).

The challenged claims recite a processor with a “plurality of cores,” including a “first core operable at a first voltage and at a first frequency,” and “a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency.” *E.g.*, Ex-1001, Cl. 1. The processor includes “graphics processing circuitry” coupled to the cores that is “independently operable at a third frequency different from the first frequency and the second frequency,” and an “interconnect” that connects the graphics processing circuitry to a memory device. *Id.* The interconnect is also “operable at a fourth frequency different from the first, second, and third frequencies.” *Id.*

The prior art teaches the claimed processor—including the well-known configuration of multiple cores, graphics processing circuitry, an interconnect, and the other elements discussed above—and renders the challenged claims unpatentable. Accordingly, Claims 1-20 of the ’588 Patent are invalid as obvious over the prior art.

This Petition presents grounds that the examiner did not consider during prosecution. These grounds are more than reasonably likely to prevail, and this Petition should be granted.

II. MANDATORY NOTICES UNDER 37 C.F.R. §42.8

Real Parties-in-Interest: Petitioner identifies the following real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Co-Petitioner Qualcomm, Incorporated, and Qualcomm Technologies, Inc.

Petitioner Qualcomm Incorporated further identifies, without conceding any such party is a Real Party-in-Interest, Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, and Visteon Corporation as parties that Patent Owner has accused of infringing the '588 Patent based on incorporation of Qualcomm products in *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01109 (D. Del.) and *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, ITC Inv. No. 337-TA-1332 (Violation).

Related Matters: Patent Owner has asserted the '588 Patent against Petitioner in (1) *Daedalus Prime LLC v. Arrow Electronics, Inc. et al.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*,

1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, U.S. International Trade Commission (“ITC”) Inv. No. 337-TA-1335 (Violation); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, ITC Inv. No. 337-TA-1332 (Violation).

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III. FEE AUTHORIZATION

Pursuant to 37 C.F.R. §42.15(a) and §42.103(a), the PTO is authorized to charge any and all fees to Deposit Account No. LA500639.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '588 Patent is available for review, this Petition is timely filed, and Petitioner is not barred or estopped from requesting review.

V. PRECISE RELIEF REQUESTED

Petitioner requests review and cancellation of Claims 1-20 as unpatentable based on the following grounds, supported by a declaration from Dr. Trevor Mudge Ex-1002.

Ground	Summary
1	Claims 1-2, 4, 8-9, 11, 15-20 are obvious in view of Machnicki (Ex-1006)
2	Claims 3, 7, 10, 14 are obvious over Machnicki (Ex-1006) in view of Aguilar (Ex-1007)
3	Claims 5-6, 12-13 are obvious over Machnicki (Ex-1007) in view of Shakkarwar (Ex-1008)
4	Claims 1-2, 4, 8-9, 11, 20 are obvious over Cho (Ex-1005) in view of Gold (Ex-1009)

Ground	Summary
5	Claims 3, 7, 10, 14-19 are obvious over Cho (Ex-1005) in view of Gold (Ex-1009) and Aguilar (Ex-1007)
6	Claims 5-6, 12-13 are obvious over Cho (Ex-1005) in view of Gold (Ex-1009) and Shakkarwar (Ex-1008)

VI. THE CHALLENGED PATENT

The '588 Patent purports to describe a processor having “multiple domains,” including a “core domain” and a “non-core domain.” Ex-1001, Abstract. Figure 3 illustrates the '588 Patent's claimed processor 300:

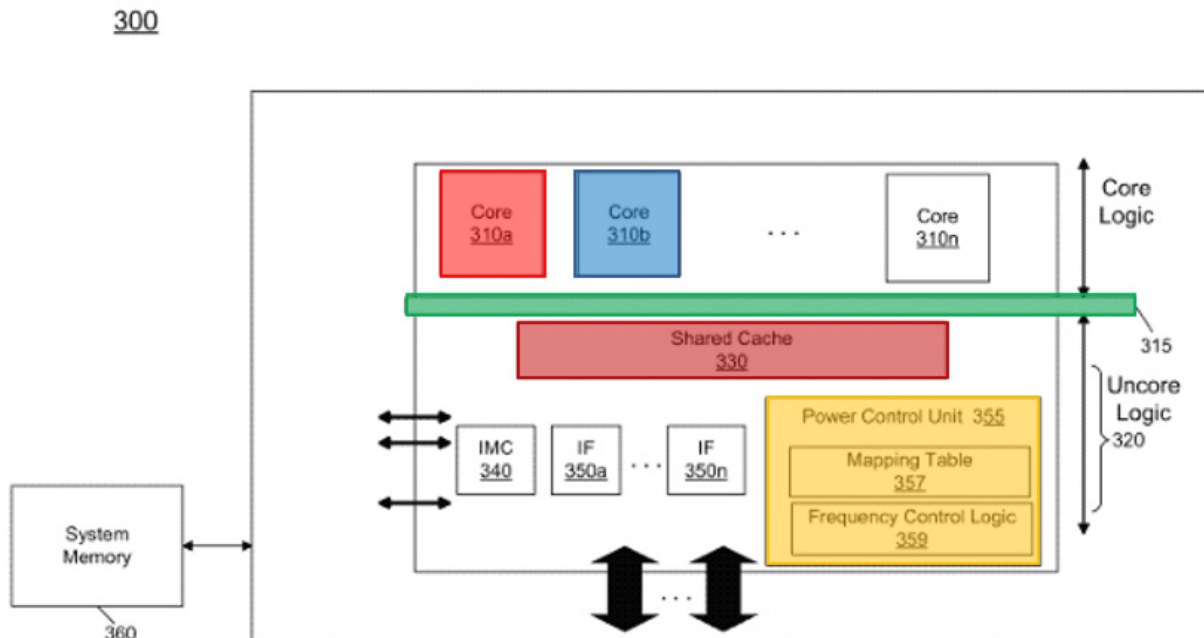


FIG. 3

Id., Fig. 3 (annotated).

As Figure 3 illustrates, the processor includes a “plurality of cores 310_a-310_n” (blue and red). Ex-1001, 5:36-40. Each core may “be of an independent power domain” and “can be configured to operate at an independent voltage and/or frequency” *Id.*, 5:41-44. The cores are connected to “interconnect 315” (green), which in turn connects the cores to a “shared cache 330” (maroon). *Id.*, 5:44-48.

The processor also includes “power control unit 355” (yellow). Ex-1001, 5:46-50. The power control unit 355 may include “frequency control logic 359,” which “perform[s] dynamic control of interconnect frequency” in either the core or non-core domains. *Id.*, 5:51-55. The ’588 Patent also discloses a “graphics domain” that includes “one or more graphics engines.” Ex-1001, 2:19-21.

VII. PROSECUTION HISTORY OF THE ’588 PATENT

The ’588 Patent was filed on January 16, 2019, and claims priority to application No. 13/282,892, filed on October 27, 2011. On December 5, 2019, the applicant terminally disclaimed pending Claims 2, 9, and 21. Ex-1004, 0156. On March 2, 2020, the examiner allowed all pending claims based on the applicant’s terminal disclaimer. *Id.*, 0164.

VIII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art at the relevant time (“POSITA”) would have had a bachelor’s degree in electrical engineering, computer science, computer

engineering, material science, physics, applied physics, or a related field, and at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa. Ex-1002, ¶¶22-26.

IX. PRIORITY DATE

The earliest possible priority for the '588 Patent is October 27, 2011. Petitioner takes no position on the proper priority date for each claim of the '588 Patent. Assuming this earliest date, all references asserted herein are prior art.

X. CLAIM CONSTRUCTION

Petitioner interprets the claims of the '588 Patent according to the *Phillips* claim construction standard. 37 C.F.R. § 42.100(b). The challenged claims recite elements that use the word “means,” creating a rebuttable presumption that they are means-plus-function elements under § 112, ¶6. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015); Ex-1002, ¶¶27-29. For the purposes of this Petition and pursuant to 37 C.F.R. § 42.104(b)(3) and Rule 42.104, Petitioner’s proposed constructions for these terms are below.²

² For each means-plus-function term below, Petitioner has identified the closest disclosed structure in the '588 Patent that relates to the recited function, but by doing so, Petitioner does not intend to, and does not, waive any argument that the structure for performing the claimed function of each term is not sufficiently disclosed.

A. “means for” “operating a first core at a first voltage ...” and “independently operating a graphics processor at a third frequency ...”

Recited Function: “operating a first core at a first voltage and at a first frequency while concurrently operating a second core at a second voltage independent of the first voltage and at a second frequency different from the first frequency, and independently operating a graphics processor at a third frequency different from the first frequency and the second frequency.”

Corresponding Structure: “power control unit 355.” The ’588 Patent explains that the power control unit includes “frequency control logic 359” that controls the frequencies of components within the core and non-core domains. Ex-1001, 5:51-60, 6:45-63.

B. “interconnect means to couple the graphics processor to a memory device ...”

Recited Function: “to couple the graphics processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies.”

Corresponding Structure: “interconnect 315.” *See* Ex-1001, Fig. 3, 5:44-50.

XI. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART

A. Machnicki

Machnicki, titled “Modifying Performance Parameters in Multiple Circuits According to a Performance State Table Upon Receiving a Request to Change a

Performance State,” issued on June 18, 2013, from an application filed on January 14, 2011. Machnicki is § 102(e) prior art.

Machnicki discloses a system that “includes an integrated circuit (IC) 100 forming a system-on-a-chip (SoC) or application-specific integrated circuit (ASIC)” Ex-1006, 4:9-12. The integrated circuit includes “a set of performance domains 120A-F,” which include “component[s]” such as “processor 160A” (red), “graphics subsystem 160B” (purple), “memory control circuit 160E” (green), and a “second processor 160F” (blue). *Id.*, 4:9-25. Figure 1 illustrates Machnicki’s integrated circuit 100:

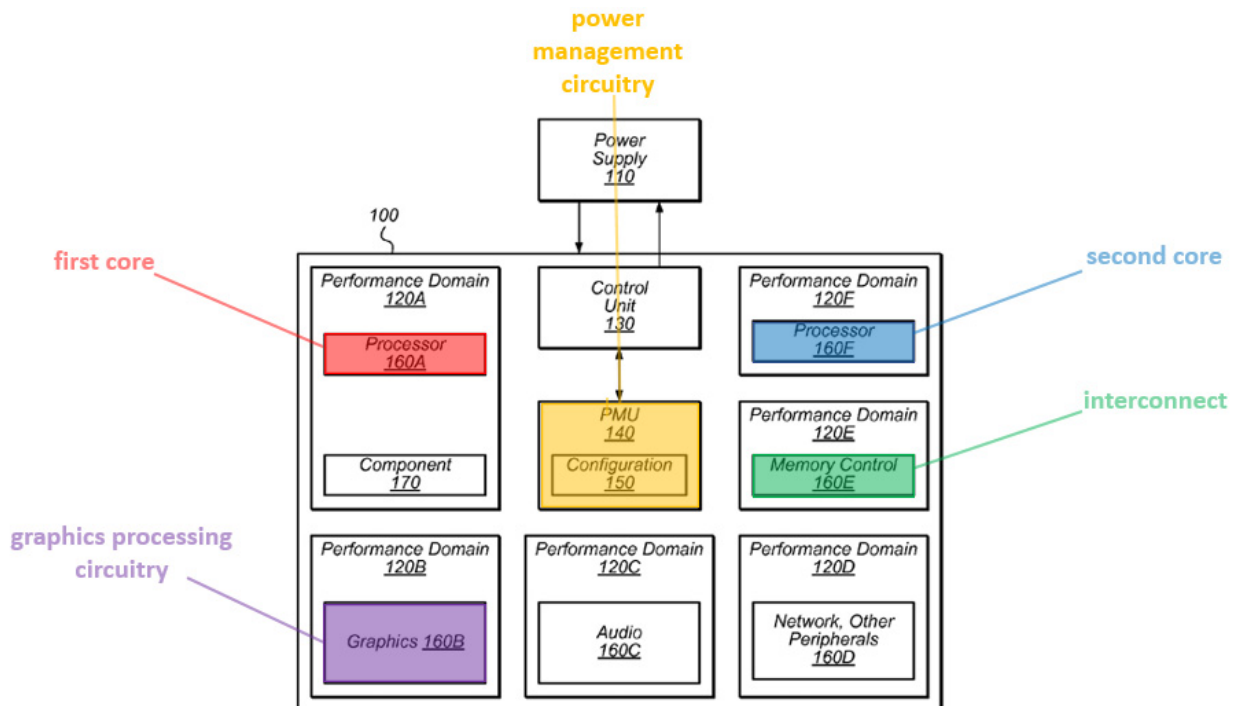


FIG. 1

Id., Fig. 1 (annotated).

Machnicki discloses that “both clock frequencies and voltages are configuration parameters that may be set for each of the performance domains (e.g., domains 1 through m).” Ex-1006, 8:1-4. Shown in Table I, each domain has a voltage, V , and a frequency, f :

TABLE I

	Domain 1	Domain 2	...	Domain m
state 1	$f_{1,1}; V_{1,1}$	$f_{2,1}; V_{2,1}$	...	$f_{m,1}; V_{m,1}$
state 2	$f_{1,2}; V_{1,2}$	$f_{2,2}; V_{2,2}$	...	$f_{m,2}; V_{m,2}$
state 3	$f_{1,3}; V_{1,3}$	$f_{2,3}; V_{2,3}$	...	$f_{m,3}; V_{m,3}$
...	...	...	...	...
state n	$f_{1,n}; V_{1,n}$	$f_{2,n}; V_{2,n}$	...	$f_{m,n}; V_{m,n}$

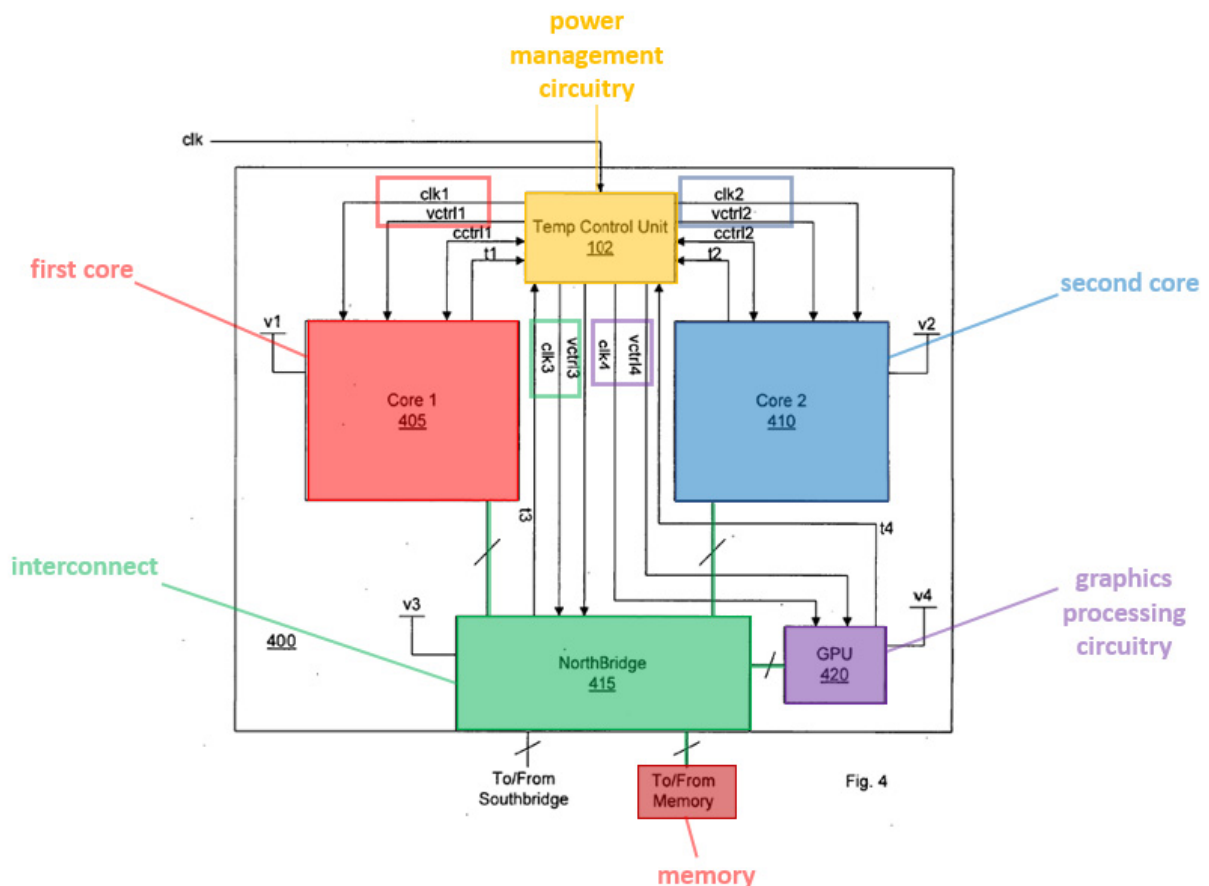
Id., 8:8-17. By using a performance state table, “such as the one illustrated in Table I [], each performance domain may have its parameters changed independently.” *Id.*, 8:37-43. In the case of clock frequencies, Machnicki discloses “the frequencies in each frequency domain for any given state may be different from each other, and may be other than a multiple of each other.” *Id.*, 8:37-43.

B. Cho

Cho, titled “Functional Block Level Thermal Control,” published on March 25, 2010. Ex-1005, Cover. Cho is § 102(b) prior art.

Cho discloses an “integrated circuit” that includes a “plurality of functional units” implemented on a die. Ex-1005, Abstract. Cho’s integrated circuit is a “multi-core processor configured for functional block level thermal control.” *Id.*, ¶38. Cho

discloses that its processor “includes four primary functional units—two processor cores 405 and 410 [red and blue], a memory controller hub (NorthBridge 415) [green], and a graphics processing unit (GPU) 42 [purple].” *Id.* Figure 4 illustrates Cho’s processor 400:



Id., Fig. 4 (annotated).

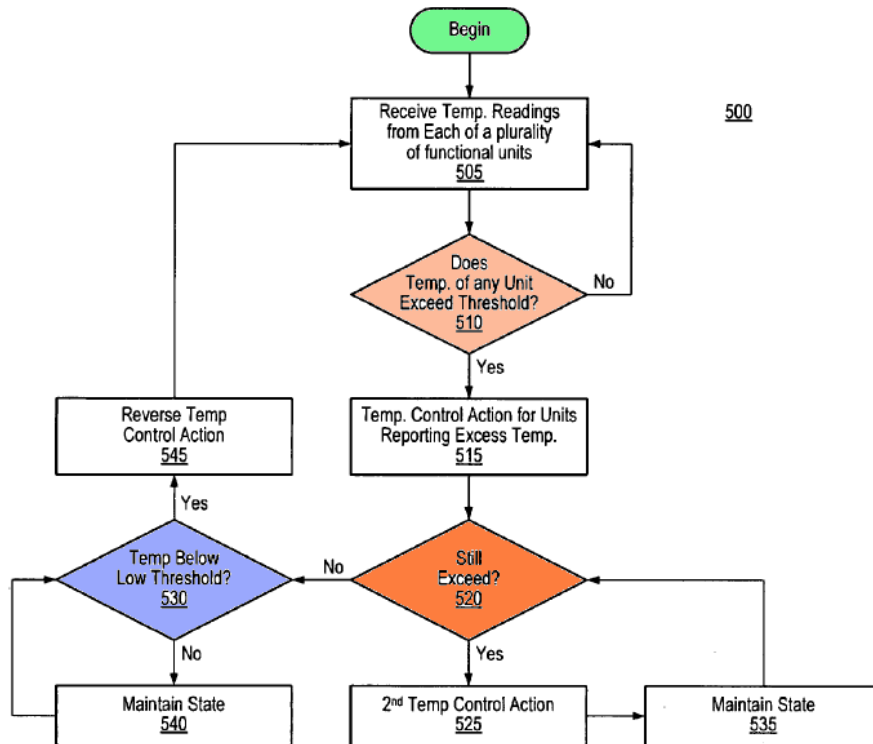
Cho also discloses that “[e]ach of the functional units shown is coupled to receive corresponding clock signals” and “corresponding voltage control signals.” Ex-1005, ¶40. Each functional unit’s voltage “can be set independently of one another, even if all of the functional units initially receive power from the same

source.” *Id.*, ¶21. Moreover, a clock control unit 310, contained in Temperature Control Unit 102 (yellow), is “configured to adjust the frequency of each of clock signals clk1-clk4, independently of one another, based on signals received from control logic 305.” *Id.*

Each functional unit also has a “temperature threshold,” which may include “maximum,” “one or more intermediate,” or “minimum” thresholds at which the “TCU 102 may initiate a temperature control action.” Ex-1005, ¶¶20, 24.

The “temperature thresholds at which TCU 102 may initiate a temperature control action may be different for one or more of the functional units with respect to other ones of the functional units,” including “embodiments wherein the temperature thresholds are unique for each [] functional unit[] 105-120.” *Id.*, ¶20. These temperature control actions include “adjusting the frequency of a clock signal received thereby, adjusting the voltage on a voltage plane of the functional unit, or a combination of both of these actions.” *Id.*, ¶40. Specifically, “[c]hanging the frequency of individual clock signals may be performed for temperature control purposes.” *Id.*, ¶36.

For example, in Figure 5, a flow chart illustrates three temperature control actions based on exceeding a threshold (light orange), still exceeding a threshold (orange), and dropping below a threshold (indigo). *See* Ex-1005, ¶¶43-44.



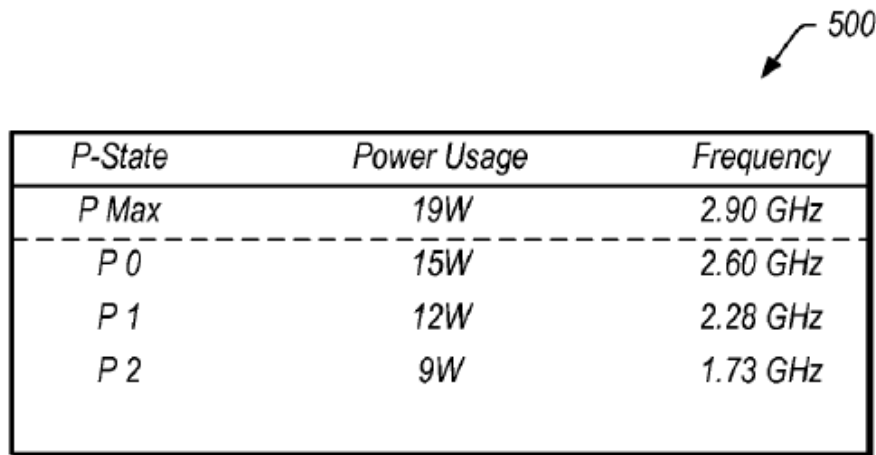
In Figure 5, a first temperature control action (515) may be to “reduce the clock frequency,” and “[the] second temperature control action (525) may be a subsequent reduction of the clock frequency.” Ex-1005, ¶44. Furthermore, if the temperature drops below a low threshold (530), in the next temperature control action (545), “the clock frequency ... may be increased back to its previous value,” which may be the starting value or the first reduced value as shown in Figure 5. *Id.*, ¶45.

C. Gold

Gold, titled “Automatic Processor Overclocking,” was published on September 17, 2009, from an application filed on March 11, 2008. Ex-1009, Cover. Gold is § 102(b) prior art.

Gold discloses methods for “performing overclocking for a plurality of processing units,” including “a plurality of processing cores (each of which has a respective standard operating frequency.” Ex-1009, ¶5. Gold discloses a “clock generation unit” that is coupled to “each of the plurality of processing cores,” and configured to “generate a respective clock signal for each of the plurality of processing cores.” *Id.*

Gold assigns several “performance states” (Pstate) to each core, such as PMax, P0, P1, P2, which each includes a “corresponding input voltage and clock frequency.” *Id.*, ¶39. Figure 5A illustrates Gold’s performance states with corresponding frequencies:



<i>P-State</i>	<i>Power Usage</i>	<i>Frequency</i>
<i>P Max</i>	<i>19W</i>	<i>2.90 GHz</i>
<i>P 0</i>	<i>15W</i>	<i>2.60 GHz</i>
<i>P 1</i>	<i>12W</i>	<i>2.28 GHz</i>
<i>P 2</i>	<i>9W</i>	<i>1.73 GHz</i>

FIG. 5A

Id., Fig. 5A. Each core is operable at at least four different frequencies, corresponding to four different power usages. Gold also teaches “a hardware

throttling control system that aggressively reduces or even stops the clock of a processing core once thermal limitations are exceeded.” *Id.*, ¶53.

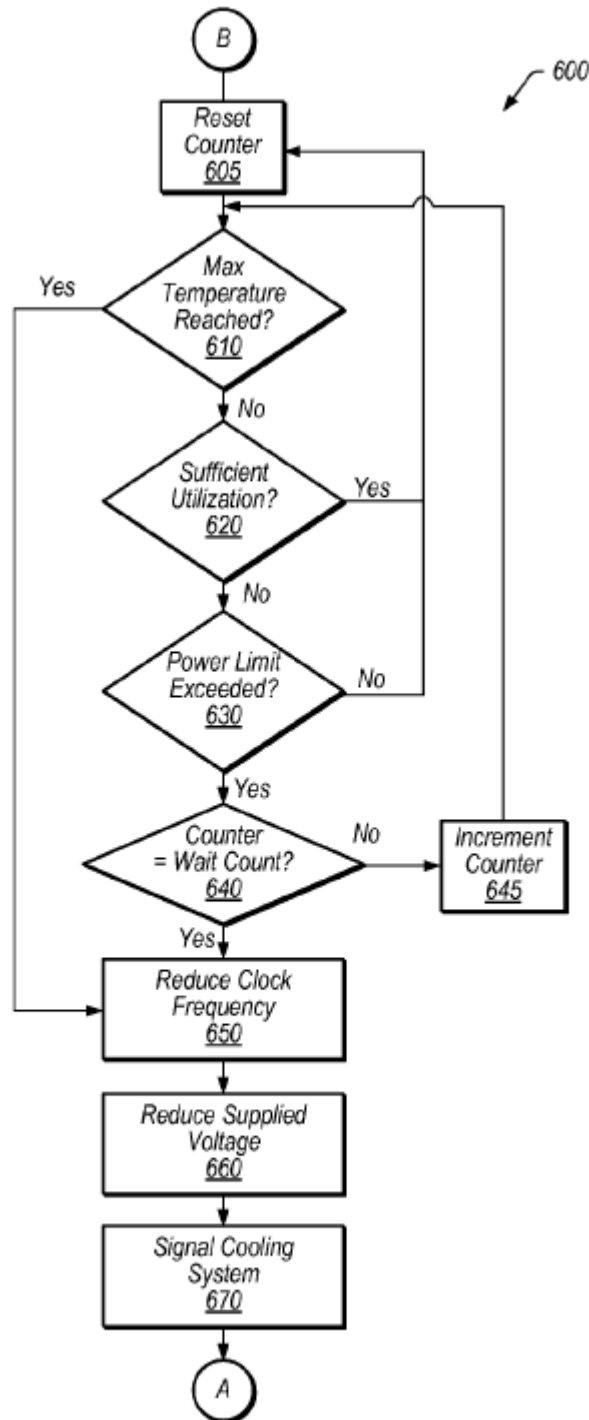


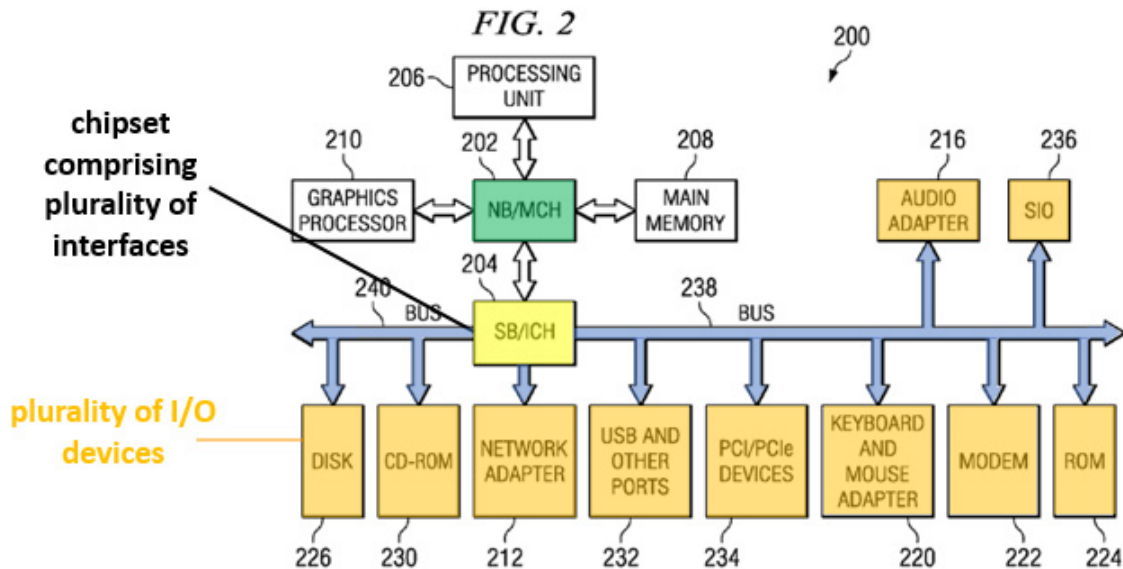
FIG. 6

D. Aguilar

Aguilar, titled “Dynamically Adapting Software for Reducing a Thermal State of a Processor Core Based On Its Thermal Index,” issued on June 23, 2009, from an application filed on May 3, 2006. Ex-1007, Cover. Aguilar is § 102(b) prior art.

Aguilar describes a “processing system 200” that employs a “hub architecture,” including a “north bridge” containing a “cache,” “south bridge,” and “input/output (I/O) controller hub ICH (204).” Ex-1007, 3:44-52, 4:57-60. Aguilar teaches that a plurality of input/output devices, such as “[a]udio adapter 216, keyboard and mouse adapter 220, modem 222, read only memory (ROM) 224, hard disk drive (HDD) 226, CD-ROM drive 230, universal serial bus (USB) ports and other communications ports 232, and PCI/PCIe devices 234 [orange] connect to south bridge [yellow] and I/O controller hub 204 [yellow] through bus 238 and bus 240” (blue). *Id.*, 3:55-60.

Figure 2, illustrates Aguilar’s hub architecture, including the I/O controller hub 204 (yellow) and I/O devices (orange):



Ex-1007, Fig. 2 (annotated).

E. Shakkarwar

Shakkarwar, titled “Systems and Methods for Dynamic Voltage Scaling of Communication Bus to Provide Bandwidth Based on Whether an Application is Active,” issued on June 24, 2008. Ex-1008, Cover. Shakkarwar is § 102(b) art.

Shakkarwar discloses “systems and methods for dynamic power management of electronic devices” Ex-1008, Abstract. Shakkarwar’s dynamic power management system includes “a data controller 302” (green) that is connected to a “graphics controller 305” (purple) through “data connection 314” (green), as illustrated in Figure 3:

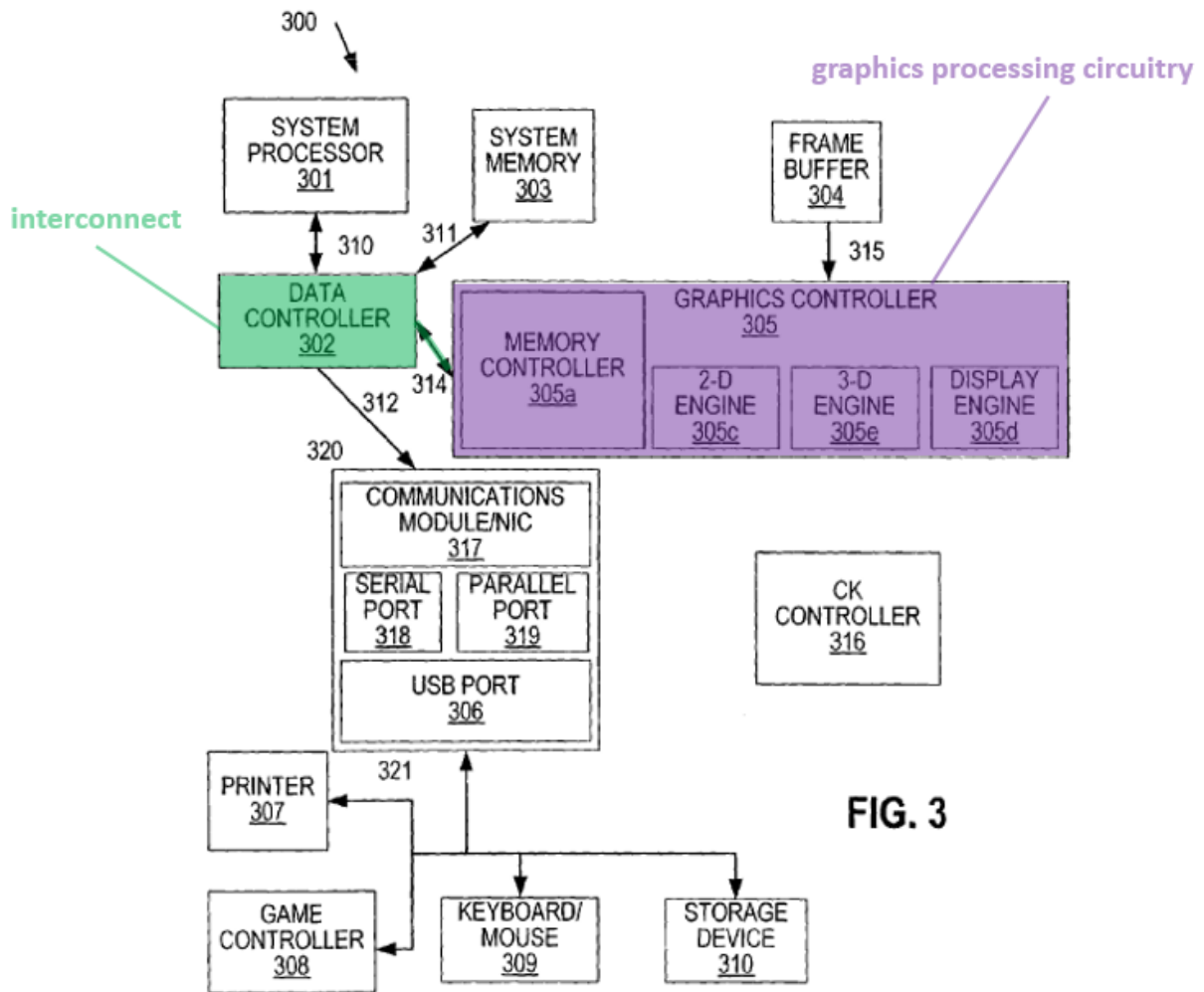


FIG. 3

Id., Fig. 3 (annotated).

Shakkarwar dynamically manages power by monitoring a component's "bandwidth ... for increasing or decreasing communication requirements." *Id.*, 6:41-43. The system then detects "a change in processing condition[s]" for a component, and upon detecting a change, "determines bandwidth 403 for an associated data connection based on the active components." *Id.*, 6:63-7:7. To determine the appropriate bandwidth for a data connection, Shakkarwar utilizes "a look-up table [that] may include a list of clock speeds, and/or voltage levels required to process

information for specific devices and/or groups of devices.” Ex-1008, 7:7-10. At step 405, “the data rate of a data connection is adjusted,” which occurs by “adjusting operating of a clock generation device.” *Id.*, 7:26-29.

XII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

A. Ground 1: Claims 1-2, 4, 8-9, 11, 15-19, and 20 are rendered obvious by Machnicki.

1. Independent Claim 1

a. Element 1[pre]: A processor comprising:

Machnicki discloses Claim 1’s preamble to the extent it is limiting. Ex-1002, ¶¶79-80. Machnicki discloses “an integrated circuit (IC) 100 forming a system-on-a-chip (SoC) or application-specific integrated circuit (ASIC) coupled to power supply 110.” Ex-1006, 4:9-12. The integrated circuit includes “a set of performance domains 120A-F,” which include “component[s]” such as “processor 160A,” “graphics subsystem 160B,” “memory control circuit 160E,” and a “second processor 160F.” *Id.*, 4:9-25. Figure 1 illustrates Machnicki’s integrated circuit 100 (green), which is a “processor” as recited in the preamble:

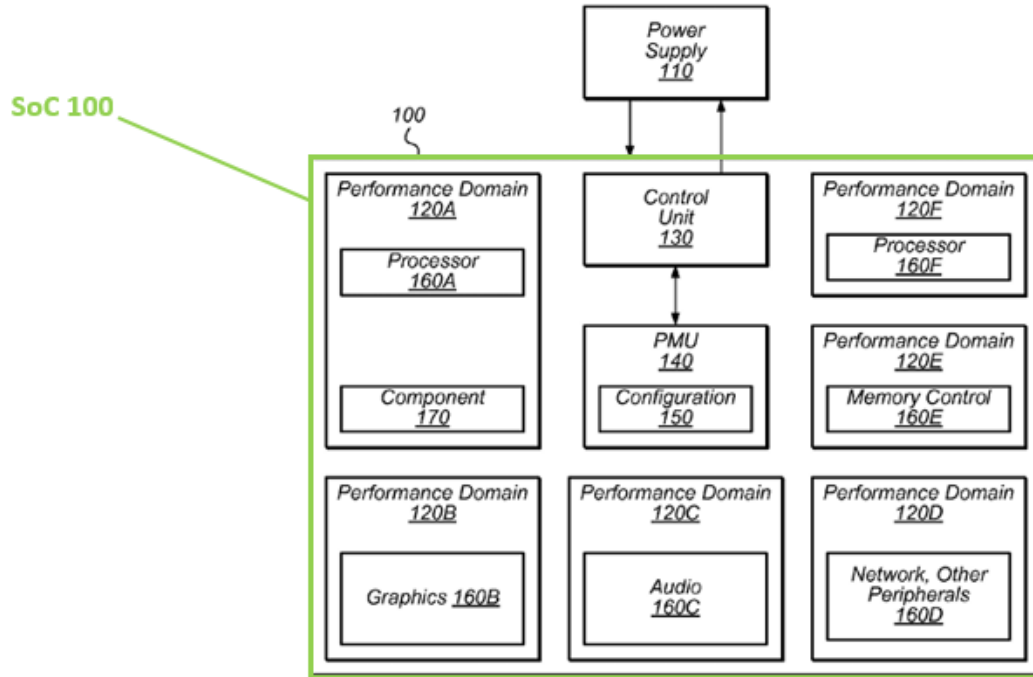


FIG. 1

Ex-1006, Fig. 1 (annotated).

b. Element 1[a]: a plurality of cores including a first core operable at a first voltage and a first frequency, and

Machnicki discloses Element 1[a]. Ex-1002, ¶¶81-83. Machnicki's SoC 100 includes "processor 160A" and "processor 160F." Ex-1006, 4:16-25. Machnicki further discloses that "[i]ntegrated circuit 520 may include one or more instances of elements within integrated circuit 100 of FIG. 1." *Id.*, 10:55-57. Machnicki's processors 160A and 160F disclose a "plurality of cores" because a POSITA would have known that each processor contains at least one core. Ex-1002, ¶81. Indeed, the '588 Patent explains that it was well known that processors could be "multicore" and

include “a plurality of cores 310a-310n.” Ex-1001, 5:37-40. *See also id.*, 1:20-26. Accordingly, processor 160A includes at least a “first core.” Ex-1002, ¶81. Figure 1 illustrates Machnicki’s processors 160A (red) and 160F (blue), each containing at least one core:

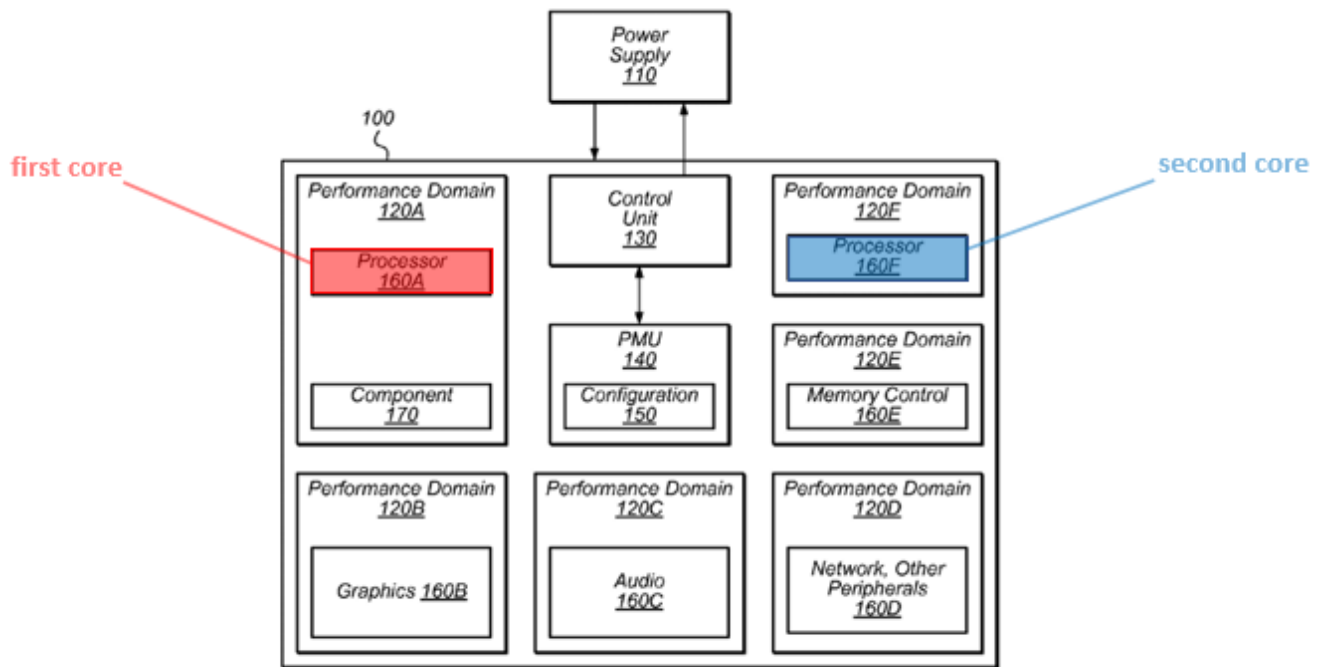


FIG. 1

Ex-1006, Fig. 1 (annotated).

Machnicki’s first core is also operable at a first voltage and first frequency. Ex-1002, ¶82. Machnicki discloses that “both clock frequencies and voltages are configuration parameters that may be set for each of the performance domains (e.g. domains 1 through m).” Ex-1006, 8:1-4. Shown in Table I, each domain has n operating states, and each operating state has a voltage, V, and a frequency, f:

TABLE I

	Domain 1	Domain 2	...	Domain m
state 1	$f_{1,1}; V_{1,1}$	$f_{2,1}; V_{2,1}$	...	$f_{m,1}; V_{m,1}$
state 2	$f_{1,2}; V_{1,2}$	$f_{2,2}; V_{2,2}$	...	$f_{m,2}; V_{m,2}$
state 3	$f_{1,3}; V_{1,3}$	$f_{2,3}; V_{2,3}$	...	$f_{m,3}; V_{m,3}$
...	...	...	...	...
state n	$f_{1,n}; V_{1,n}$	$f_{2,n}; V_{2,n}$	...	$f_{m,n}; V_{m,n}$

Id., 8:8-17. Because each domain has n pairs of operable voltages and frequencies, a POSITA would have understood that processor 160A (“first core”) within a first domain (performance domain 120A) is operable at a first voltage and a first frequency. Ex-1002, ¶83.

- c. **Element 1[b]: a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;**

Machnicki discloses Element 1[b]. Ex-1002, ¶¶84-88. Machnicki’s SoC 100 includes “processor 160F.” Ex-1006, 4:16-25. Processor 160F has at least one core, which is a “second core.” Ex-1002, ¶85. Figure 1 illustrates processor 160F (blue), including the second core:

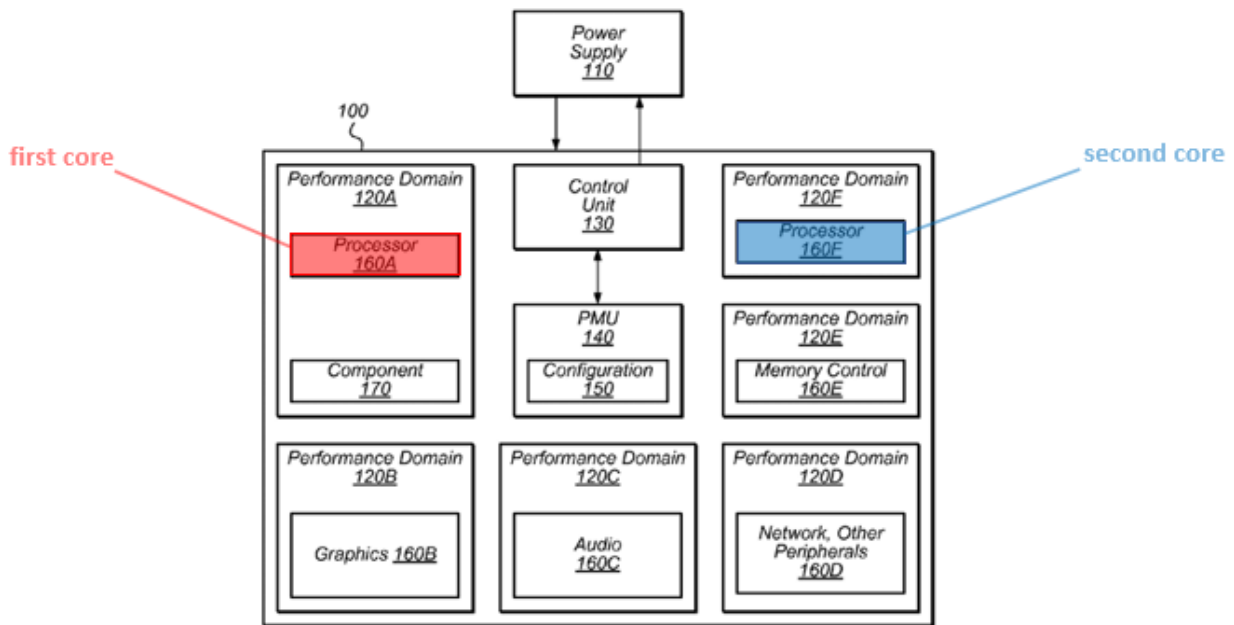


FIG. 1

Ex-1006, Fig. 1 (annotated).

Machnicki's second core is also operable at a second voltage independent of the first voltage. Ex-1002, ¶86. Both “clock frequencies and voltages are configuration parameters that may be set for each of the performance domains” including “performance domain 120F” containing processor 160F (“second core”). Ex-1006, 8:1-4. As shown in Table I, a second domain containing processor 160F has n operating states, and each operating state has a voltage, V , and a frequency, f :

TABLE I

	Domain 1	Domain 2	...	Domain m
state 1	$f_{1,1}; V_{1,1}$	$f_{2,1}; V_{2,1}$	...	$f_{m,1}; V_{m,1}$
state 2	$f_{1,2}; V_{1,2}$	$f_{2,2}; V_{2,2}$	...	$f_{m,2}; V_{m,2}$
state 3	$f_{1,3}; V_{1,3}$	$f_{2,3}; V_{2,3}$	...	$f_{m,3}; V_{m,3}$
...	...	...	...	...
state n	$f_{1,n}; V_{1,n}$	$f_{2,n}; V_{2,n}$	...	$f_{m,n}; V_{m,n}$

Id., 8:8-17.

Furthermore, Machnicki explains that “by using a performance state table such as the one illustrated in Table I [], each performance domain may have its parameters changed *independently*.” Ex-1006, 8:37-43. Thus, because voltage is a configuration parameter that may be set for a performance domain, the second core’s voltage can be set separately and independently of the first voltage. Ex-1002, ¶87.

Moreover, Machnicki’s second core is operable at a second frequency different from the first frequency. Ex-1002, ¶88. Machnicki discloses that “in the case of clock frequencies, *the frequencies in each frequency domain for any given state may be different from each other*, and may be other than a multiple of each other.” *Id.*, 8:37-43. A POSITA would have understood that processor 160F (“second core”), which is within a second performance domain, has a second frequency (e.g., as shown above, $f_{2,2}; V_{2,2}$) different from the first frequency of the first core. Ex-1002, ¶88.

- d. **Element 1[c]: graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and**

Machnicki discloses Element 1[c]. Ex-1002, ¶¶89-94. Machnicki discloses the SoC's "performance domain 120B includes graphics subsystem 160B." Ex-1006, 4:9-25. Graphics subsystem 160B is "graphics processing circuitry" because it is "involved in the display of images on a display device." Ex-1002, ¶90; Ex-1006, 7:1-7. Figure 1 illustrates Machnicki's graphics subsystem 160B (purple):

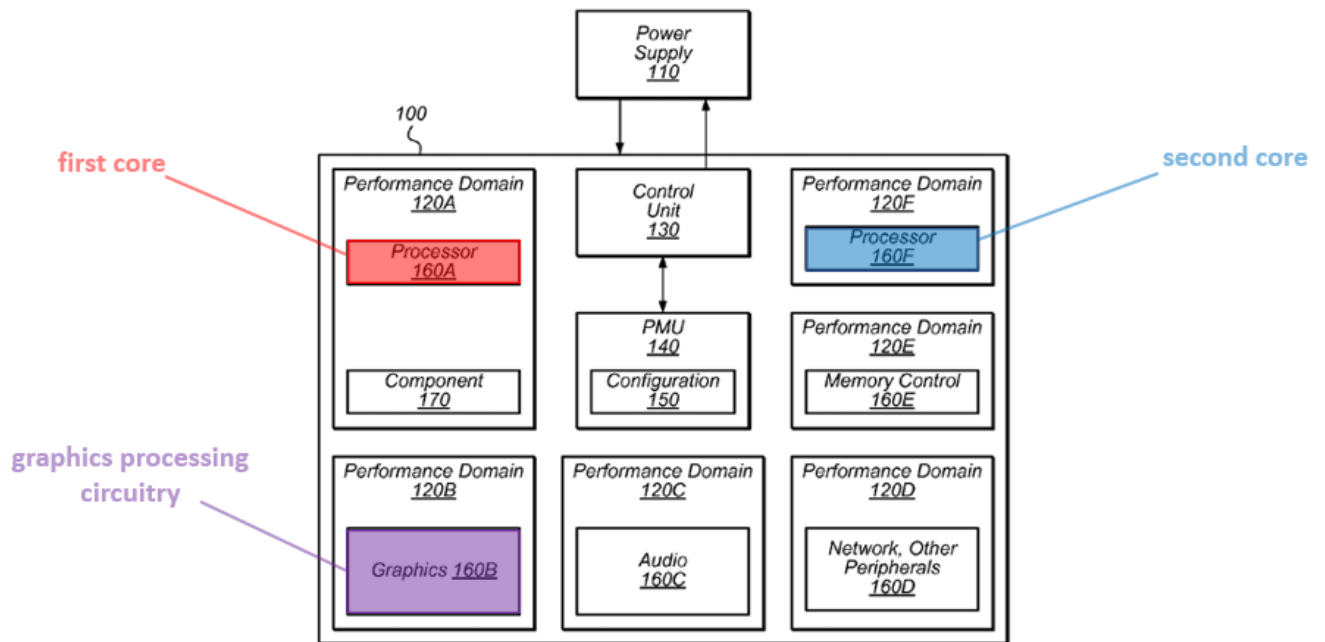


FIG. 1

Ex-1006, Fig. 1 (annotated).

Machnicki also discloses that "[c]omponents within integrated circuit 100 may be *coupled to each other using any suitable bus* and/or interface mechanism."

Ex-1006, 4:31-33. Based on this disclosure, a POSITA would have known that the graphics subsystem 160B (“graphics processing circuitry”) is coupled to the processors 160A and 160F (“plurality of cores”) using “any suitable bus.” Ex-1002, ¶¶91-92.

Furthermore, Machnicki’s graphics processing circuitry is independently operable at a third frequency different from the first frequency and the second frequency. Ex-1002, ¶93. Machnicki discloses that “clock frequencies and voltages are configuration parameters that may be set for each of the performance domains,” including performance domain 120B containing graphics subsystem 160B. Ex-1006, 8:1-4. Furthermore, “by using a performance state table such as the one illustrated in Table I [], each performance domain may have its parameters changed independently.” *Id.*, 8:37-43. As shown in Table I, a third domain containing graphics subsystem 160B has n operating states, and each operating state has a voltage, V, and a frequency, f:

TABLE I

	Domain 1	Domain 2	...	Domain m
state 1	$f_{1,1}; V_{1,1}$	$f_{2,1}; V_{2,1}$	...	$f_{m,1}; V_{m,1}$
state 2	$f_{1,2}; V_{1,2}$	$f_{2,2}; V_{2,2}$	...	$f_{m,2}; V_{m,2}$
state 3	$f_{1,3}; V_{1,3}$	$f_{2,3}; V_{2,3}$	...	$f_{m,3}; V_{m,3}$
...	...	...	...	...
state n	$f_{1,n}; V_{1,n}$	$f_{2,n}; V_{2,n}$	...	$f_{m,n}; V_{m,n}$

Id., 8:8-17. As with the first and second cores, Machnicki also discloses that “*the frequencies in each frequency domain for any given state may be different from each other*, and may be ... a multiple of each other.” *Id.*, 8:37-43. A POSITA would have understood that graphics processor 160B is operable at a voltage and frequency (e.g., $f_{3,3}$; $V_{3,3}$) different from that of the first core and second core. Ex-1002, ¶94.

- e. **Element 1[d]: an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.**

Machnicki discloses Element 1[d]. Ex-1002, ¶¶95-100. Machnicki discloses the SoC’s “performance domain 120E includes memory control circuit 160E.” Ex-1006, 4:9-25. Figure 1 illustrates Machnicki’s memory control circuit 160E (green):

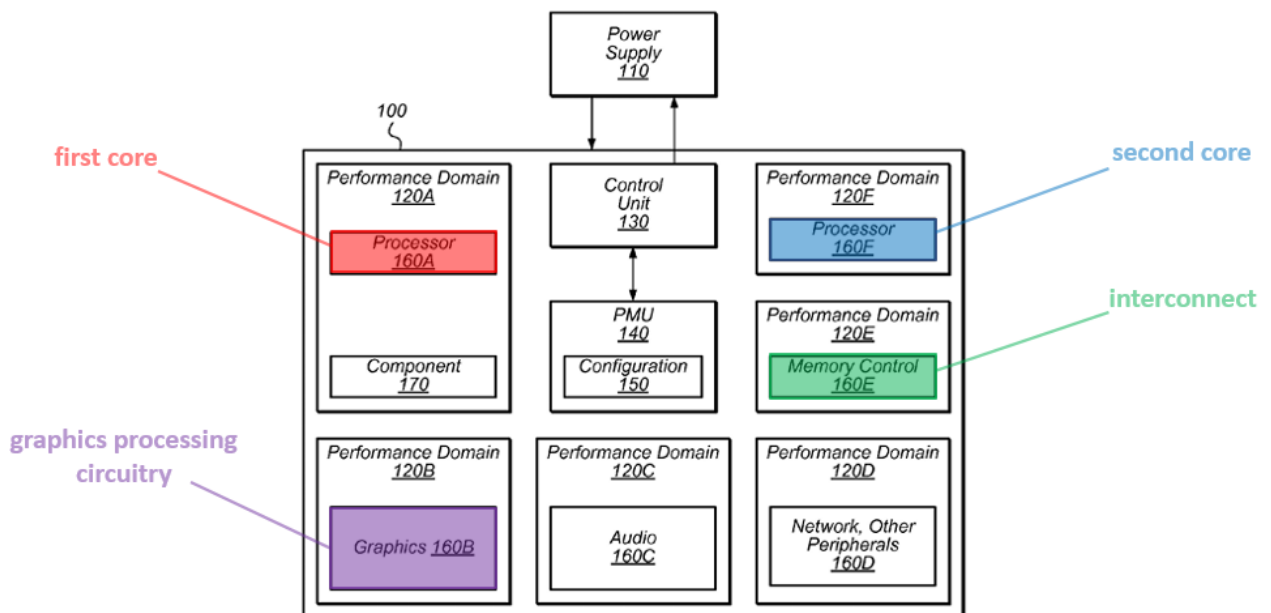


FIG. 1

Id., Fig. 1 (annotated).

Memory control circuit 160E acts to connect the other components within the integrated circuit to memory “*using any suitable bus* and/or interface mechanism.” Ex-1006, 4:31-33; Ex-1002, ¶97. The memory control circuit 160E comprising a bus is an “interconnect” because it is “configured to communicate on the memory interfaces, to queue memory requests from other components in integrated circuit 100, and/or to communicate with the other components to fulfill memory read and write operations,” thus connecting the components. *Id.*, 7:30-34; Ex-1002, ¶97. Indeed, memory control circuit 160E sits between each component within the integrated circuit and memory. By acting as the bridge between each component and memory, memory control circuit 160E is an interconnect. Ex-1002, ¶97.

Memory control circuit 160E also couples the graphics processing circuitry to a memory device. Ex-1002, ¶98. Machnicki discloses that “memory controller 160E may be configured to interface to one or more memory modules ... that include one or more of the memories.” Ex-1006, 7:21-30. Additionally, as discussed above, memory controller 160E communicates with other components and fulfills read and write operations based on those communications. *Id.*, 7:30-34. A POSITA would have known that to do so, memory controller 160E would have been coupled to each component, including the graphics processing circuitry, and configured to couple those components to memory. Ex-1002, ¶98.

Moreover, Machnicki's interconnect is operable at a fourth frequency different than the first, second, and third frequencies. Ex-1002, ¶99. As shown in Table I, a fourth domain containing memory control circuit 160E has n operating states, and each operating state has a voltage, V , and a frequency, f :

TABLE I

	Domain 1	Domain 2	...	Domain m
state 1	$f_{1,1}; V_{1,1}$	$f_{2,1}; V_{2,1}$	...	$f_{m,1}; V_{m,1}$
state 2	$f_{1,2}; V_{1,2}$	$f_{2,2}; V_{2,2}$	...	$f_{m,2}; V_{m,2}$
state 3	$f_{1,3}; V_{1,3}$	$f_{2,3}; V_{2,3}$	...	$f_{m,3}; V_{m,3}$
...	...	...	...	...
state n	$f_{1,n}; V_{1,n}$	$f_{2,n}; V_{2,n}$	...	$f_{m,n}; V_{m,n}$

Id., 8:8-17. Machnicki discloses that “in the case of clock frequencies, the ***frequencies in each frequency domain for any given state may be different from each other***, and may be other than a multiple of each other.” Ex-1006, 8:37-43. Because memory control circuit 160E is in its own domain, a POSITA would have known the memory control circuit 160E is operable at a fourth frequency (e.g., $f_{4,4}$; $V_{4,4}$) different than the cores and graphics processing circuitry's frequencies. Ex-1002, ¶100.

2. **Dependent Claim 2: The processor of claim 1, further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and to cause the second core to independently operate at the second frequency.**

Machnicki discloses Claim 2. Ex-1002, ¶¶101-104. Machnicki discloses that “[i]ntegrated circuit 100 also includes power management unit (PMU) 140,” illustrated in Figure 1 (yellow):

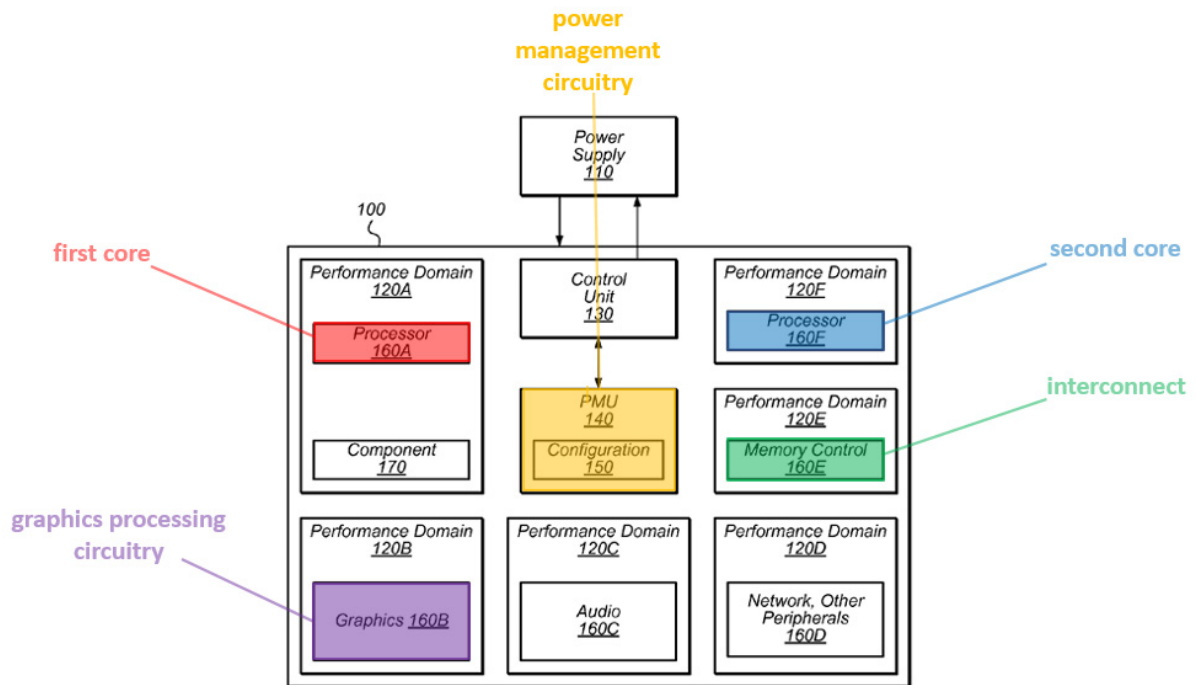


FIG. 1

Ex-1006, 4:25-30, Fig. 1 (annotated).

PMU 140 “may be a logic circuit or the like.” Ex-1006, 5:62-63. PMU 140 is coupled to “clock and/or voltage control unit (control unit) 130” and “may be configured to establish a corresponding performance state for each performance

domain,” in which “each performance domain may have its parameters changed *independently*.” *Id.*, 4:28-4:30, 4:56-60, 8:37-43. The PMU also “may be configured to control transitions between performance states in each performance domain.” *Id.*, 4:56-60. Machnicki’s PMU 140 is “first power management circuitry and/or logic.” Ex-1002, ¶103. Specifically, it is power management “circuitry.” Ex-1002, ¶103.

Moreover, PMU 140 causes the first core to operate at the first frequency and the second core to independently operate at the second frequency. Ex-1002, ¶104. For example, “[i]n the case where performance states or levels are reached by making voltage and/or clock frequency changes, PMU 140 may communicate new voltage and/or frequency settings to the control unit 130.” Ex-1006, 6:14-17. As discussed, the PMU is “configured to establish a corresponding performance state for each performance domain” in which “the *frequencies in each frequency domain for any given state may be different from each other*.” *Id.*, 4:56-60, 8:37-43. Because Machnicki states that the frequencies in each frequency domain for any given state may be different from each other, and PMU 140 is responsible for establishing each performance state within each domain, a POSITA would have understood the PMU causes the first core to operate at the first frequency and the second core to independently operate at the second frequency. Ex-1002, ¶104.

3. Dependent Claim 4: The processor of claim 2, further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.

Machnicki discloses Claim 4. Ex-1002, ¶¶105-107. Machnicki discloses that its software includes “graphics driver 420” that communicates with the graphics subsystem 160B. Ex-1006, 10:23-26. This driver communicates with “PMU driver 460,” which “may be used to interact with PMU 140.” *Id.*, 10:22-27. PMU driver 460 is “second power management circuitry and/or logic.” Ex-1002 ¶106.

Moreover, PMU driver 460 causes the graphics processing circuitry to operate at the third frequency. Ex-1002, ¶107. PMU driver 460 may “monitor the activity in the components driven by the drivers 420-450 in a device activity table or the like,” and based on these monitored activities, “may select the performance state for each performance domain” *Id.*, 10:27-37. Machnicki also discloses that “performance states or levels are reached by making voltage and/or clock frequency changes.” *Id.*, 6:14-17. Thus, a POSITA would have known that Machnicki uses PMU driver 460 to monitor activity in graphics subsystem 160B driven by graphics driver 420, and based on the activities being monitored, PMU driver 460 may select the performance state (in terms of voltage/frequency changes) for graphics subsystem 160B. Ex-1002, ¶107. Accordingly, PMU driver 460 (second power management circuitry

and/or logic) causes the graphics processing circuitry (160B) to operate at the third frequency. *Id.*, Ex-1002, ¶107.

4. Independent Claim 8

a. Element 8[pre]: A system comprising:

Machnicki discloses Claim 8's preamble to the extent it is limiting. Ex-1002, ¶¶108-109. Machnicki explains the "system includes an integrated circuit (IC) 100 forming a system-on-a-chip (SoC) or application-specific integrated circuit (ASIC)" Ex-1006, 4:9-25. The SoC includes performance domains, each with components: "[P]erformance domain 120A includes two components processor 160A [] performance domain 120B includes graphics subsystem 160B, [] performance domain 120E includes memory control circuit 160E, and performance domain 120F includes optional second processor 160F." *Id.*

b. Element 8[a]: a system memory;

Machnicki discloses Element 8[a]. Ex-1002, ¶¶110-111. Machnicki discloses that its system includes "memory 530," which may be "any type of memory," including "SRAM, nonvolatile RAM (NVRAM, such as 'flash' memory), dynamic RAM (DRAM) ... and/or any type of tangible memory." Ex-1006, 11:20-29. Figure 5 illustrates Machnicki's memory 530 (maroon):

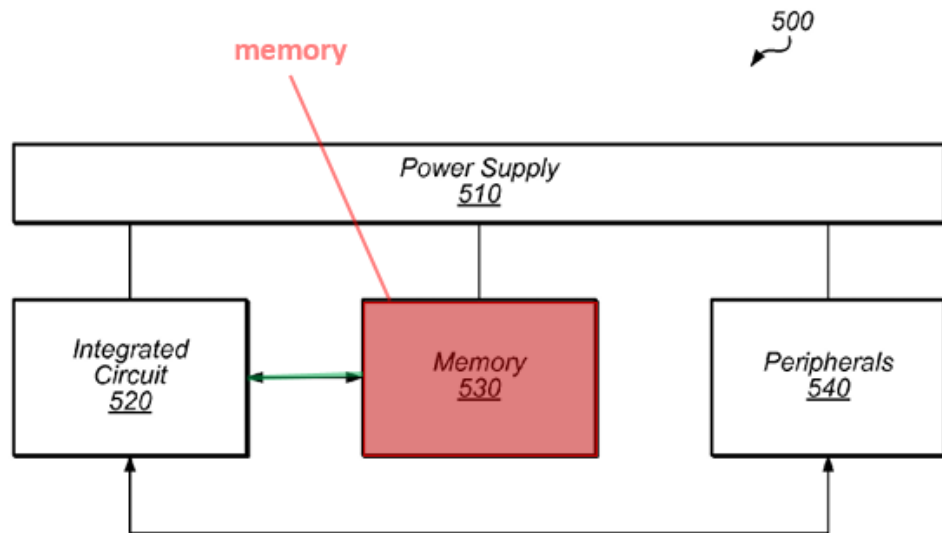


FIG. 5

Id., Fig. 5 (annotated).

c. Element 8[b]: a plurality of cores coupled to the system memory;

As discussed in Section XII.A.1.b, Machnicki discloses a plurality of cores within an integrated circuit. Ex-1002, ¶¶112-113. Shown in Figure 5, the integrated circuit (green), may be integrated circuit 100 discussed above, and therefore the cores of integrated circuit 100 are coupled to the system memory (maroon):

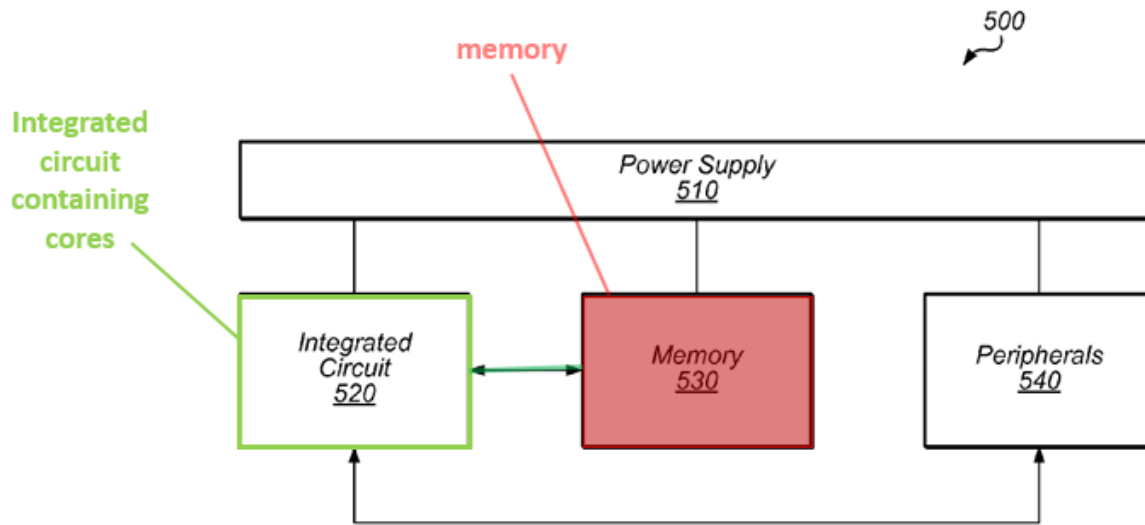


FIG. 5

Id., Fig. 5 (annotated). Machnicki explains that “[i]ntegrated circuit 520 may include one or more instances of elements within integrated circuit 100.” *Id.*, 10:55-57. A POSITA would have understood that system 500 includes elements within integrated circuit 100, such as the cores. Ex-1002, ¶113.

- d. **Element 8[c]: a first core of the plurality of cores operable at a first voltage and at a first frequency, and a second core of the plurality of cores operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;**

As discussed in Section XII.A.1.b-c, Machnicki discloses Element 8[c].

Ex-1002, ¶114.

- e. **Element 8[d]: graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and**

As discussed in Section XII.A.1.d, Machnicki discloses Element 8[d].
Ex-1002, ¶115.

- f. **Element 8[e]: an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first and second frequencies.**

As discussed in Section XII.A.1.e, Machnicki discloses Element 8[e].
Ex-1002, ¶116.

- 5. **Dependent Claim 9: The system of claim 8, further comprising: first power management circuitry and/or logic to cause the first core to operate at the first frequency and to cause the second core to independently operate at the second frequency.**

For the reasons described above for Claim 2, Machnicki discloses Claim 9.
Ex 1002, ¶117.

- 6. **Dependent Claim 11: The system of claim 9, further comprising: second power management circuitry and/or logic to cause the graphics processing circuitry to operate at the third frequency.**

For the reasons described above for Claim 4, Machnicki discloses Claim 11.
Ex 1002, ¶118.

7. **Dependent Claim 15: The system of claim 8, further comprising: a chipset coupled to the plurality of cores, the chip set comprising a plurality of interfaces to couple the cores to a plurality of I/O devices.**

Machnicki discloses Claim 15. Ex-1002, ¶¶119-122. Machnicki's "performance domain 120D may include two or more networking or other peripherals 160D." Ex-1006, 4:16-20. Networking peripherals and other peripherals 160D "may include a variety of circuitry," including "a media access controller (MAC) unit for the supported network, as well as physical layer circuitry." *Id.*, 7:13-15. Other peripherals may also include "any other desired peripherals, and/or peripheral interface controllers configured to control off-chip peripheral interfaces such as Peripheral Component Interconnect (PCI), PCI express (PCIe), firewire, Universal Serial Bus (USB), etc." *Id.*, 7:13-20. A POSITA would have known that the peripherals are a chipset comprising a plurality of interfaces so that the input/output devices described above can connect to Machnicki's SoC. Ex-1002, ¶120. Moreover, as Figure 1 illustrates, the peripherals are coupled to the cores because "[c]omponents within integrated circuit 100 may be *coupled to each other using any suitable bus* and/or interface mechanism":

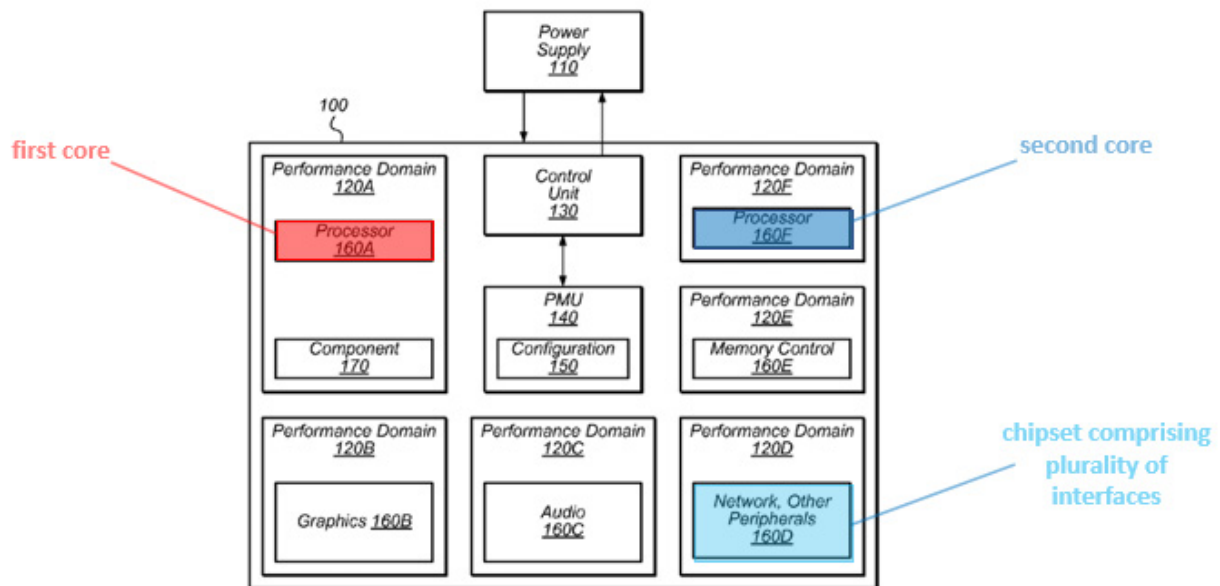
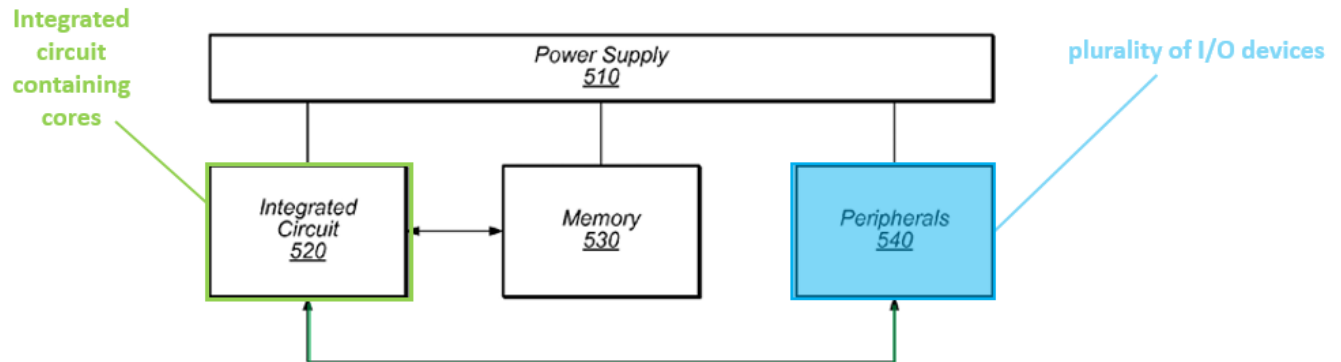


FIG. 1

Ex-1006, Fig. 1 (annotated), 4:31-33.

Machnicki also discloses “[i]ntegrated circuit 520 may include one or more instances of elements within integrated circuit 100,” and “various additional circuitry such as ... video and/or audio processing circuitries, on-chip peripherals and/or peripheral interfaces to couple to off-chip peripherals, etc.” Ex-1006, 10:53-64. Figure 5 illustrates Machnicki’s integrated circuit coupled to one or more “peripherals 540”:



Id., Fig. 5 (annotated). A POSITA would have understood that to couple the integrated circuit to multiple peripherals 540, the circuit would include a chipset with a plurality of interfaces. Ex-1002, ¶122. Moreover, a POSITA would have understood that the chipset would be coupled to the plurality of cores because peripherals 540 are connected to integrated circuit 520 which contains the cores. Finally, peripherals 540 include a plurality of I/O devices, including “a display screen, including touch display screens or multitouch display screens, keyboard or other input devices, microphones, speakers, etc.” *Id.*, 11:10-15.

Machnicki discloses Claim 16. Ex-1002, ¶¶123-124. Machnicki discloses that peripherals 540 include a plurality of I/O devices, including “speakers, etc.” Ex-1006, 11:10-15.

9. Dependent Claim 17: The system of claim 16, wherein one of the I/O devices comprises a video rendering device.

Machnicki discloses Claim 17. Ex-1002, ¶¶125-126. Machnicki discloses that peripherals 540 include a plurality of I/O devices, including “a display screen, including touch display screens or multitouch display screens ...” Ex-1006, 11:10-15.

10. Dependent Claim 18: The system of claim 17, wherein one of the I/O devices comprises a user input device.

Machnicki discloses Claim 18. Ex-1002, ¶¶127-128. Machnicki discloses peripherals 540 include a plurality of I/O devices, including a “keyboard or other input devices ...” *Id.*, 11:10-15.

11. Dependent Claim 19: The system of claim 18, wherein one of the I/O devices comprises a network communication device.

Machnicki discloses Claim 19. Ex-1002, ¶¶129-130. Machnicki discloses “networking peripherals” that may include “a media access controller (MAC) unit for the supported network, as well as physical layer circuitry” and “devices for various types of wireless communication, such as Wi-fi, Bluetooth, cellular, global positioning system, etc.” Ex-1006, 7:11-20, 11:8-10.

12. Independent Claim 20

Claim 20 is nearly identical to Claim 1, except for being written in “means-plus-function” form. Below is a comparison between Claim 1 and Claim 20:

~~1. A processor~~ 20. An apparatus comprising:

~~a plurality of cores including~~ means for operating a first core ~~operable~~ at a first voltage and at a first frequency, ~~and while concurrently operating~~ a second core ~~operable~~ at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

~~graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry~~ means for independently ~~operable~~ operating a graphics processor at a third frequency different from the first frequency and the second frequency; and

~~an interconnect~~ means to couple the graphics ~~processing circuitry~~ processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies.

The “functions” recited in Claim 20 are the same as those recited in Claim 1, so the analysis below cross-references the prior art analysis for Claim 1. Ex-1002, ¶¶131-132.

a. Element 20[pre]: An apparatus comprising:

Machnicki teaches the preamble of Claim 20 to the extent it is limiting. Ex-1002, ¶133. Machnicki teaches an “integrated circuit (IC) 100 forming a system-on-a-chip (SoC) or application-specific integrated circuit (ASIC),” which is an apparatus. Ex-1006, 4:9-12.

b. Element 20[a]: means for operating a first core at a first voltage and at a first frequency while concurrently operating a second core at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

As described in Section XII.A.1.b-d, the equivalent structure is Machnicki’s “power management unit (PMU) 140.” Ex-1006, 4:25-30. As previously explained,

PMU 140 is configured to operate the first core, second core, and GPU at independent and distinct voltages and frequencies. Ex-1002, ¶¶134-135.

c. Element 20[b]: means for independently operating a graphics processor at a third frequency different from the first frequency and the second frequency

As described in Section XII.A.3, the equivalent structure is a “PMU driver 460” and equivalents, performing the function recited in the remainder of this claim element. Notably, this function is the same as those discussed above with respect to Claim 4. PMU driver 460 may be used to interact with PMU 140 and causes the graphics processing circuitry to operate at the third frequency. Ex-1006, 10:22-27; Ex-1002, ¶136.

d. Element 20[c]: interconnect means to couple the graphics processor to a memory device, the interconnect means operable at a fourth frequency different from the first, second, and third frequencies.

As described in Section XII.A.1.e, Machnicki’s equivalent structure is “memory control circuit 160E” that acts to connect the processor’s various components. Ex-1006, 7:30-34. As set forth in those sections, memory control circuit 160E performs the recited function. Ex-1002, ¶¶137-138.

B. Ground 2: Claims 3, 7, 10, and 14 are rendered obvious by Machnicki and Aguilar.

1. A POSITA would have been motivated to combine Machnicki and Aguilar’s teachings and would have had a reasonable expectation of success.

In addition to the reasons set forth below, a POSITA would have been motivated to combine the teachings of Machnicki and Aguilar (Machnicki-Aguilar) and would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. Ex-1002, ¶¶139-142.

Both relate to and describe methods for optimizing performance between multiple components within computer systems. Ex-1006, Abstract; Ex-1007, Abstract. For example, Machnicki discloses “[s]ystems and methods for coordinating performance parameters in multiple domains ...” Ex-1006, Abstract. The system manages performance by “causing a first parameter of a first circuit serving the first domain to be modified” based on “[a] request, and causing a second parameter of a second circuit serving the second domain to be modified” based on “[a] request.” *Id.* The parameter may include “a clock frequency,” and in other cases, “a voltage.” *Id.* Similarly, Aguilar discloses a method for “optimizing thermal performance of a computer system” by requesting “a thermal index” for “***each of the set of system resources*** to form a set of thermal indexes.” Ex-1007, Abstract (emphasis added). Then, “[a]n action from a set of actions is identified to reduce resource utilization” for each resource. *Id.*

A POSITA would have been motivated to combine Machnicki-Aguilar because they would have recognized a benefit of incorporating Aguilar’s teachings of thermal indexes into a system like Machnicki to improve temperature control and resource utilization throughout a computer system. Ex-1002, ¶141. Aguilar discloses that “identification of a set of system resources” associated with a computer system “is performed and a thermal index is requested for *each // set* of system resources.” Ex-1007, Abstract (emphasis added). A “set of actions is identified to reduce resource utilization,” and the actions are “implemented to reduce a thermal state of the computer system.” *Id.* Thus, a POSITA would have known that by incorporating Aguilar’s teachings into Machnicki, temperature control and overall utilization of the computer system could be improved. Ex-1002, ¶141.

A POSITA would also have had a reasonable expectation of success in combining the teachings of Machnicki-Aguilar. Ex-1002, ¶142. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies that would have been amendable to various well-understood and predictable combinations, as explained in further detail below. *Id.*

2. Dependent Claim 3: The processor of claim 1, further comprising: a non-core power domain comprising a cache shared by the plurality of cores.

Machnicki-Aguilar teach Claim 3. Ex-1002, ¶¶143-146. Machnicki discloses non-core power components, which form a “non-core power domain,” including

“graphics 160B” (purple), “memory controller 160E” (green), and “PMU 140” (yellow), as illustrated in Figure 1:

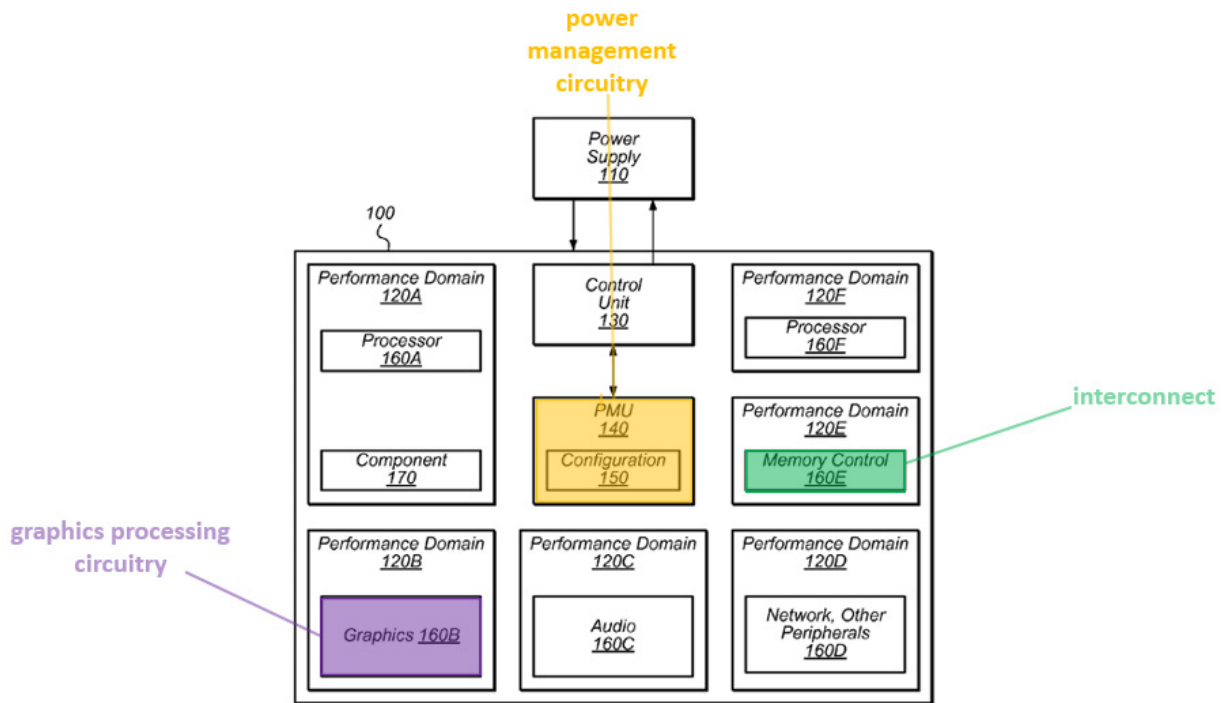


FIG. 1

Ex-1006, Fig. 1 (annotated).

A POSITA would have understood that Machnicki’s memory control 160E contained a cache, specifically an on-chip or “Level 1” cache, because such “L1” caches were common components of high-performance processors at the time of the ’588 Patent. Ex-1002, ¶144. Machnicki also teaches that memory within its system may be a cache. *Id.* For example, Machnicki discloses “configuration parameters may be component specific,” and may depend on “cache sizes in various caches” Ex-1006, 5:18-20. Machnicki also teaches, “[r]educing cache

size may reduce power consumption because a portion of the cache may not need to be accessed, and even more reduction may be realized if the unused portion may be turned off.” *Id.*, 5:43-46.

This cache is shared by the plurality of cores. Ex-1002, ¶145. For example, Machnicki’s memory controller 160E “may be configured to communicate on the memory interfaces, to queue memory requests from other components in integrated circuit 100, and/or to communicate with the other components to fulfill memory read and write operations.” Ex-1006, 7:30-34; *see also id.* at 4:31-33. Through memory controller 160E, the components within the circuit, including the cores, communicate requests to the system memory and fulfill memory read and write operations, thus sharing the memory. Ex-1002, ¶145.

One design choice for memory controller 160E would have included a cache because caches were common components of nearly all memory systems at the time of the ’588 Patent. Ex-1002, ¶146. Indeed, Aguilar discloses such an arrangement in which “memory may be ... a cache such as found in north bridge and memory controller 202 in Fig. 2.” Ex-1007, 4:57-60. A POSITA would have been motivated to implement Machnicki’s memory controller with a cache memory, for example as taught by Aguilar, because including a cache makes retrieving data from a computer’s memory more efficient. Ex-1002, ¶146. Data can be retrieved easily

from cache memory, and data stored in caches is typically more readily available to processors and other system components than data stored in system's main memory.

3. **Dependent Claim 7: The processor of claim 3, further comprising: power management circuitry and/or logic to cause the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores, respectively.**

As discussed in Section XII.A.1.d-e, Machnicki-Aguilar disclose Claim 7.

Ex 1002, ¶147. A POSITA would have known Machnicki's power management circuitry and/or logic causes the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores because Graphics 160B and Memory Control 160E, which are part of the non-core power domain, operate at different frequencies than the cores.

4. **Dependent Claim 10: The system of claim 8, further comprising: a non-core power domain comprising a cache shared by the plurality of cores.**

See discussion in Section XII.A.4, regarding Claim 8. For the reasons described above for Claim 3, Machnicki-Aguilar disclose Claim 10. Ex-1002, ¶148.

5. **Dependent Claim 14: The system of claim 10, further comprising: power management circuitry and/or logic to cause the non-core power domain to operate at a different frequency from the first and second frequencies of the first and second cores, respectively.**

For the reasons described above for Claim 7, Machnicki-Aguilar disclose Claim 14. Ex-1002, ¶149.

C. Ground 3: Claims 5-6 and 12-13 are rendered obvious by Machnicki and Shakkarwar.

1. **A POSITA would have been motivated to combine Machnicki and Shakkarwar’s teachings and would have had a reasonable expectation of success.**

In addition to the reasons set forth below, a POSITA would have been motivated to combine the teachings of Machnicki and Shakkarwar (Machnicki-Shakkarwar) and would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. Ex-1002 ¶¶150-153.

Both relate to and describe similar methods for optimizing performance between multiple components within a computer system. Ex-1006 (Machnicki), Abstract; Ex-1008, Abstract. Machnicki discloses “[s]ystems and methods for coordinating performance parameters in multiple domains” Ex-1006, Abstract. The system manages performance by “causing a first parameter of a first circuit serving the first domain to be modified to a first modified parameter based on [a] request, and causing a second parameter of a second circuit serving the second domain to be modified to a second modified parameter based on [a] request.” *Id.* The

parameter may include “a clock frequency,” and in other cases, “a voltage.” *Id.* Similarly, Shakkarwar relates to the “efficient use of electronic devices and, more particularly, to systems and methods for power management of electronic devices.” Ex-1008, 1:8-10. Shakkarwar discloses “[s]ystems and methods for dynamic power management of electronic devices” so that “power consumption of the system may be dynamically managed while providing sufficient bandwidth for the system.” Ex-1008, Abstract. Shakkarwar dynamically manages power by monitoring a component’s “bandwidth ... for increasing or decreasing communication requirements.” *Id.*, 6:41-43. The system then detects “a change in processing condition[s]” for a component, and upon detecting a change, “determines bandwidth 403 for an associated data connection based on the active components.” *Id.*, 6:63-7:7. The data rate “of a data connection is [then] adjusted,” including by adjusting a clock frequency or voltage, to reach optimal performance levels. *Id.*, 7:26-29. In this manner, “power consumption associated with communicating and processing information via data buses may be optimized while satisfying bandwidth requirements for the computer system.” *Id.*, 3:17-20; *see also id.*, 2:12-15, Cl. 21.

A POSITA would have been motivated to combine the teachings of Machnicki-Shakkarwar because they would have recognized a benefit of implementing a look-up table for dynamically managing power, such as taught by Shakkarwar, to optimize performance of components within a processor as taught

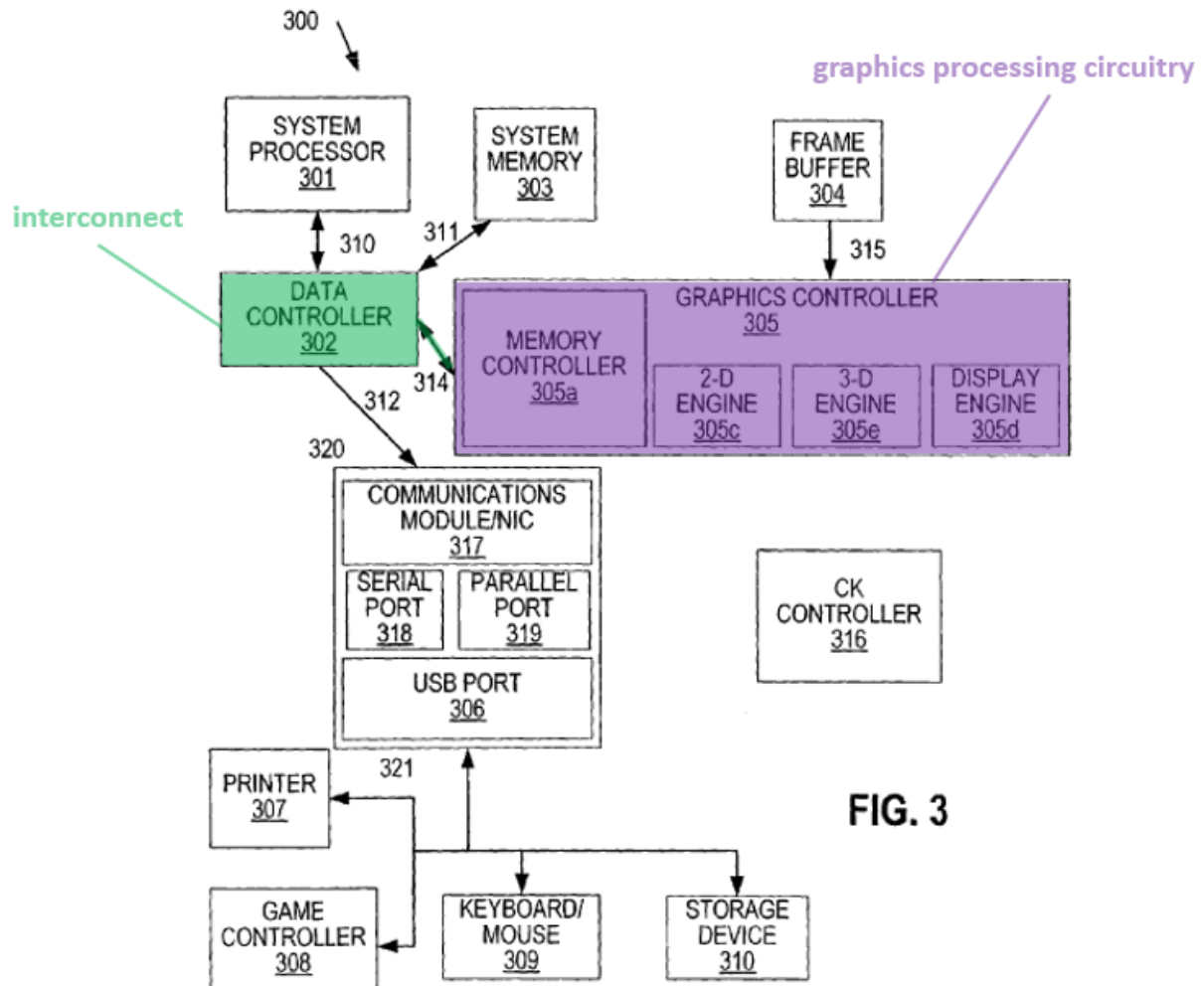
by Machnicki. Ex-1002, ¶152. As noted above, Shakkarwar teaches that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while [also] satisfying bandwidth requirements for communicating and/or processing information.” *Id.*, 2:34-39.

A POSITA would also have had a reasonable expectation of success in combining the teachings of Machnicki-Shakkarwar. Ex-1002, ¶153. A POSITA would have understood that these references disclose interrelated teachings based on routine technologies that would have been amendable to various well-understood and predictable combinations, as explained below. *Id.*

2. Dependent Claim 5: The processor of claim 4, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.

Machnicki-Shakkarwar teach Claim 5. Ex-1002, ¶¶154-160. As explained above in Section XII.A.3, Machnicki discloses a second power management circuitry and/or logic. Machnicki in view of Shakkarwar teaches that this power management circuitry would have been implemented to include a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect. *Id.*, ¶154. *See* section XII.C.1.

Shakkarwar's dynamic power management system includes "a data controller 302" (green) connected to a "graphics controller 305" (purple) through "data connection 314" (green), as illustrated in Figure 3:



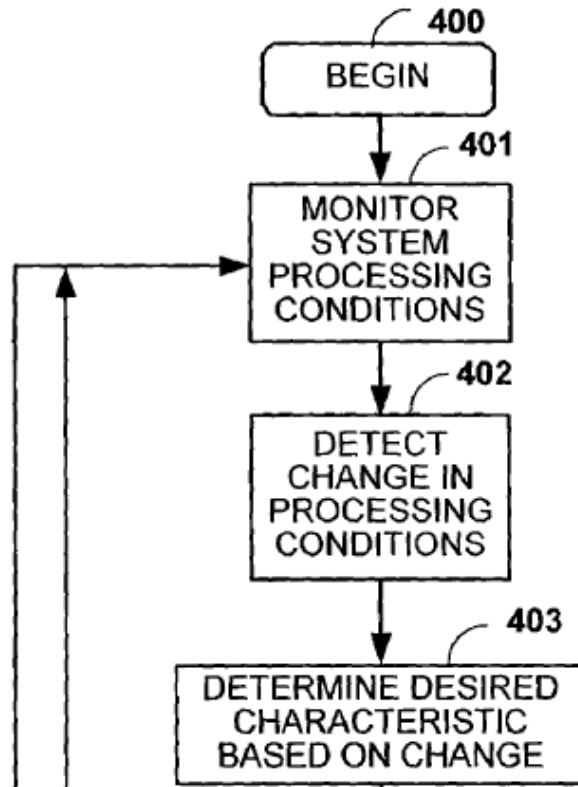
Id., Fig. 3 (annotated).

A POSITA would have understood that data controller 302 and data connection 314 are an "interconnect," and the "graphics controller 305" is "graphic processing circuitry." Ex-1002, ¶156. Data controller 302 connects graphics controller 305 and other components within Shakkarwar to each other and to system

memory 303. Ex-1008, 5:10-15, Fig. 4. Graphics controller 305 includes a “3-D engine 305e” and performs “3-D graphics operations” *Id.*, 6:7-16.

Shakkarwar also maps selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect. Ex-1002, ¶157. At step 401, Shakkarwar monitors “bandwidth for a component,” such as the interconnect or graphics processing circuitry, for “increasing or decreasing communication requirements.” Ex-1008, 6:41-43. For example, “when an application that is known to use 3-D graphics is opened, system software can determine if the bus rate between the data controller [the ‘interconnect’] and the graphics controller [the ‘graphics processing circuitry’] is high enough to support the graphics requirements.” *Id.*, 6:49-52.

At step 402, the system detects “a change in processing condition[s]” for a specific component, and upon detecting a change, it “determines bandwidth 403 for an associated data connection ***based on the active components.***” Ex-1008, 6:63-7:7. To determine the appropriate bandwidth for a data connection, Shakkarwar utilizes “***a look-up table*** [that] may include ***a list of clock speeds, and/or voltage levels required to process information for specific devices and/or groups of devices.***” *Id.*, 7:7-10. Figure 4 illustrates this process:



Id., Fig. 4. Accordingly, Shakkarwar teaches determining the appropriate bandwidth for a component (graphics controller 305) utilizing a look-up table that includes a list of appropriate clock speeds. It also considers other active components, such as the data controller 302 (the “interconnect”) and its clock speeds. As such, a POSITA would have understood that Shakkarwar teaches to map selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect using look-up tables. Ex-1002, ¶159.

A POSITA would have been motivated to implement these teachings of Shakkarwar, such as a look-up table, in Machnicki for the reasons described above in Section XII.C.1, including because Shakkarwar teaches that an advantage to its

system is that it dynamically “manag[es] power consumption of electronic devices while satisfying bandwidth requirements for communicating and/or processing information.” Ex-1008, 2:34-39. A POSITA would have been motivated to include this advantage in Machnicki’s PMU 140 to improve responsiveness of the system and increase the agility of the system to respond to dynamically changing conditions, including the changing bandwidth requirements of Machnicki’s components during various activity states. Ex-1002, ¶160.

3. Dependent Claim 6: The processor of claim 5, wherein the second power management circuitry and/or logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.

Machnicki-Shakkarwar disclose Claim 6. Ex-1002, ¶¶161-163. As explained above for Claim 5, Machnicki-Shakkarwar disclose second power management circuitry that determines bandwidth for an associated data connection based on the other active components by using a look-up table of clock speeds required to process information for specific devices. *See* Section XII.C.1 (discussing Shakkarwar’s teachings).

Shakkarwar further discloses that “[a]t step 405, the data rate of a data connection is adjusted. In one embodiment, the data rate can be adjusted by adjusting operating of a clock generation device.” Ex-1008, 7:26-29. Figure 4 illustrates adjusting the data rate of a data connection:

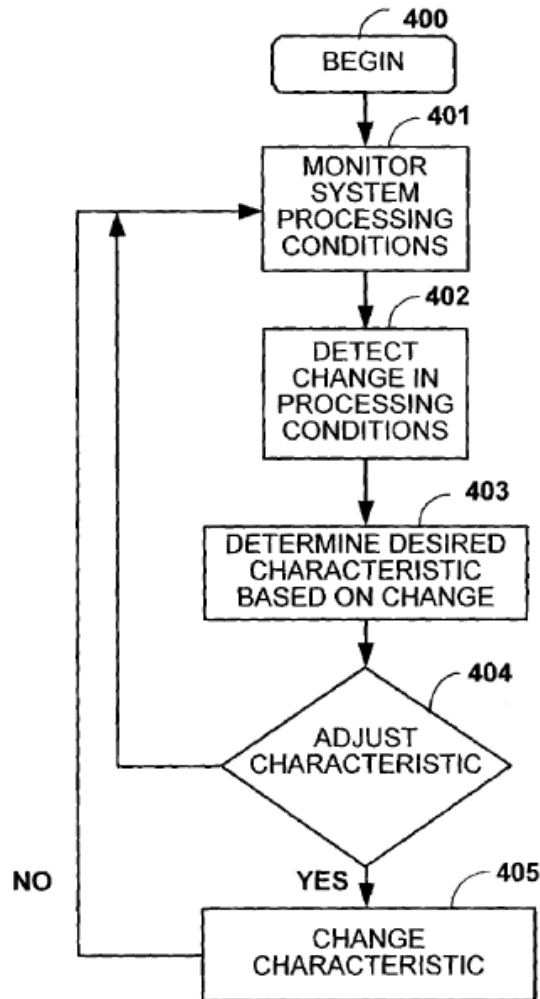


FIG. 4

Id., Fig. 4.

Shakkarwar also specifically discloses selecting “the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.” Ex-1002, ¶163. Shakkarwar discloses that “when an application that is known to use 3-D graphics is opened, system software can determine if *the bus rate between the data controller [the “interconnect”] and the graphics controller [the “graphics processing circuitry”] is high enough to support the*

graphics requirements.” Ex-1008, 6:49-52. A POSITA would have understood that by applying these teachings from Shakkarwar to Machnicki, the fourth frequency for the interconnect would be selected based on detecting the frequency of the graphics processing circuitry. Ex-1002, ¶163.

4. **Dependent Claim 12: The system of claim 11, wherein the second power management circuitry and/or logic includes a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.**

See discussion in Sections XII.A.4 and XII.A.6, regarding Claims 8 and 11.

For the reasons described above for Claim 5, Machnicki-Shakkarwar disclose Claim 12. Ex-1002, ¶164.

5. **Dependent Claim 13: The system of claim 12, wherein the second power management circuitry and/or logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.**

See discussion in Sections XII.A.4 and XII.C.4, regarding Claims 8 and 12.

For the reasons described above for Claim 6, Machnicki-Shakkarwar disclose Claim 13. Ex-1002, ¶165.

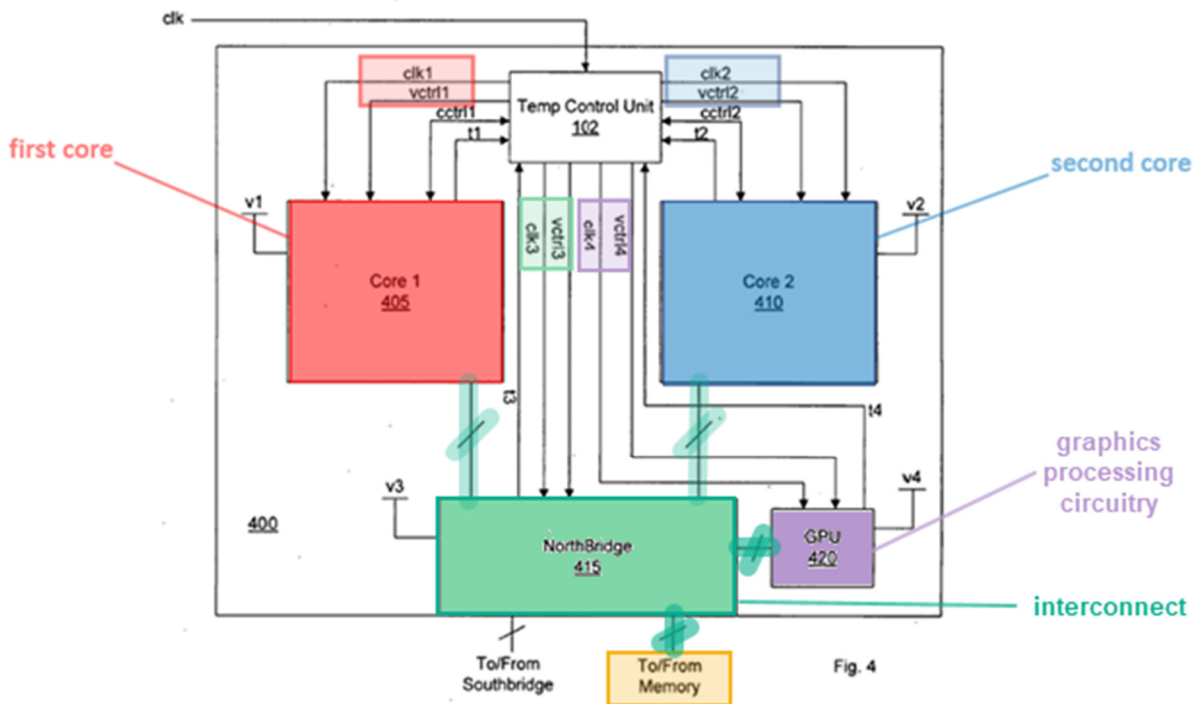
D. Ground 4: Claims 1-2, 4, 8-9, 11, and 20 are rendered obvious by Cho and Gold.

1. A POSITA would have been motivated to combine Cho and Gold's teachings and would have had a reasonable expectation of success.

In addition to the reasons set forth below, a POSITA would have been motivated to combine the teachings of Cho and Gold (Cho-Gold) and would have had a reasonable expectation of success in doing so because each addresses similar issues corresponding to the same well-known technologies. Ex-1002, ¶¶166-177.

Cho and Gold share a common inventor, Hanwoo Cho, and were developed contemporaneously for the same assignee, Global Foundries. Both relate to and describe similar methods for optimizing the performance of components within a computer system by controlling frequency. Ex-1005, Abstract; Ex-1009, Abstract. Additionally, each reference specifically teaches the same direct relationship between temperature and frequency; namely a lower operating frequency will result in a lower operating temperature. Ex-1005, ¶¶24, 33, 36; Ex-1009, Fig. 7.

Cho teaches an SOC device 400 that has at least four different functional units: A first core, a second core, a GPU, and a northbridge. As shown in Figure 4, each of these four functional units are driven by a distinct clock frequency, clk1 through clk4, annotated in the figure in red, blue, green and purple:



Cho teaches that these frequencies are changed “independently of one another, based on signals received from control logic 305.” Ex-1005, ¶35. And, “a change in the clock frequency for a clock signal provided to one functional unit need not affect the frequencies of the respective clock signals provided to other ones of the functional units.” *Id.*, ¶22. Indeed, Cho’s “clock control unit” that is coupled to the four functional units “provide[s] *separate* clock signals to each of the functional units.” *Id.*, ¶35.

Cho does this to individually and separately control the temperature of each of the four functional units. For example, if a particular functional unit is operating at a maximum temperature, its operating frequency may be reduced to lower the operating temperature of that unit. Ex-1005, ¶¶30, 34, 39-40. Cho further teaches

that a functional unit may have four different monitored temperature states: a maximum temperature, a minimum temperature, a first intermediate temperature, and a second intermediate temperature. *Id.*, ¶24. Cho teaches the direct relationship between temperature and operating frequency (lower operating frequency will result in lower operating temperature), but does not specifically identify four explicit frequencies that correspond to each of a maximum temperature, a minimum temperature, a first intermediate temperature, and a second intermediate temperature. One of skill in the art, however, would have understood that, due to the direct relationship between operating temperature and operating frequency, the four corresponding frequencies would have been different from each other. Ex-1002, 170.

This understanding is further made clear by Gold. Gold teaches “a hardware throttling control system that aggressively reduces or even stops the clock of a processing core once thermal limitations are exceeded.” Ex-1009 ¶53. Gold specifically discloses four specific frequencies and corresponding power dissipations:

500
↙

<i>P-State</i>	<i>Power Usage</i>	<i>Frequency</i>
<i>P Max</i>	19W	2.90 GHz
<i>P 0</i>	15W	2.60 GHz
<i>P 1</i>	12W	2.28 GHz
<i>P 2</i>	9W	1.73 GHz

FIG. 5A

As Gold teaches, the four specific frequencies may be reduced, stepping through PMax, P0, P1, and P2. This results in corresponding reductions in power usage, causing commensurate reduction in operating temperature. Ex-1002, ¶172. As the teachings of Cho-Gold make clear, a system that is operable at four different temperatures (as taught by Cho) would have been implemented by operability at four different frequencies (as taught by Gold). *Id.*

Additionally, like Cho, Gold discloses multiple components (e.g., “Core 0” and “Core 1”) that are each operable at different frequencies:

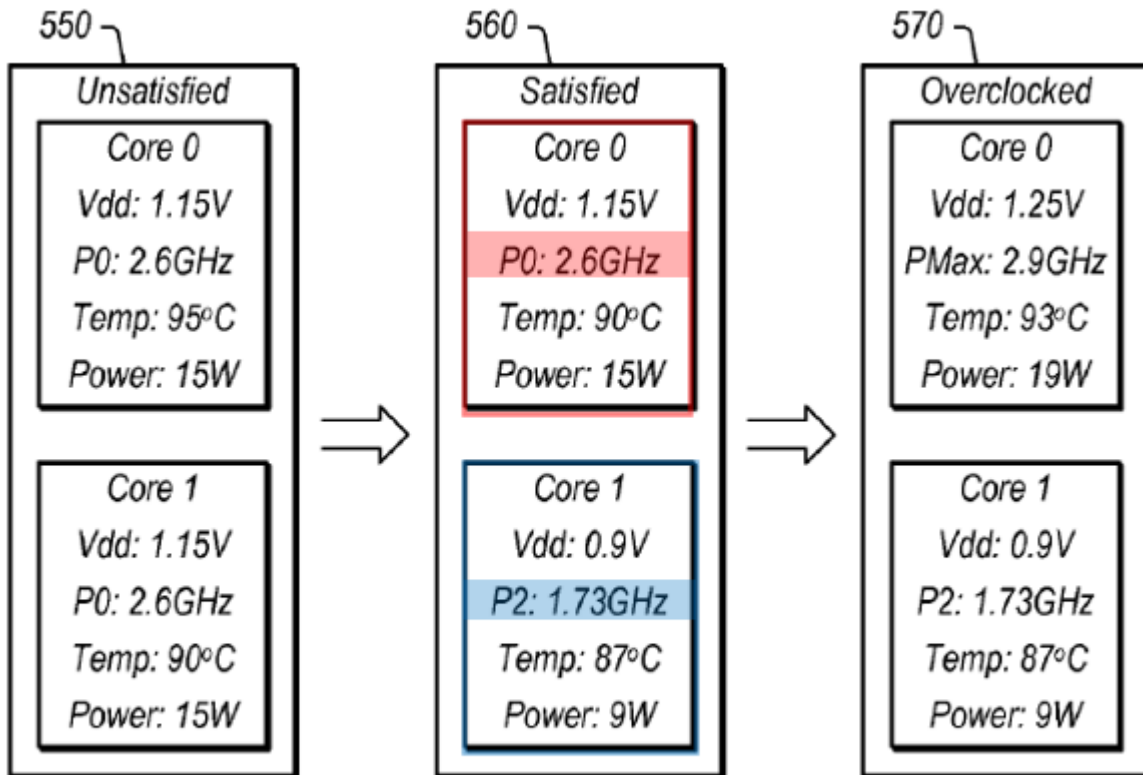


FIG. 5B

Ex-1009, Fig. 5B (annotated), ¶5. A POSITA would have thus recognized Cho and Gold's systems disclose interrelated teachings that would be especially compatible in the combined Gold-Cho system. Ex-1002, ¶174.

Moreover, a POSITA implementing the Cho-Gold teachings would have understood that each of Cho's four independently controlled clocks, clk1-clk4, would have been operable at distinct frequencies, as taught by Gold. Ex-1002, ¶175. A POSITA would have been motivated to implement Cho's teachings with four different frequencies to more particularly control the operating temperature of

each component. *Id.* A POSITA would have been motivated to assign specific and different frequency values (as taught by both Cho-Gold) to Cho's maximum and minimum temperature thresholds, and one or more intermediate temperature thresholds to allow for more predictable and controllable temperature actions using "thermal information corresponding to various utilization, temperature, and power entry/exit criteria" (Ex-1009, ¶6) as taught by Gold. *Id.* As shown in Gold's Figure 7, this predictable relationship allows for improved power and temperature budgeting and controllability of each different component. Ex-1009, ¶66.

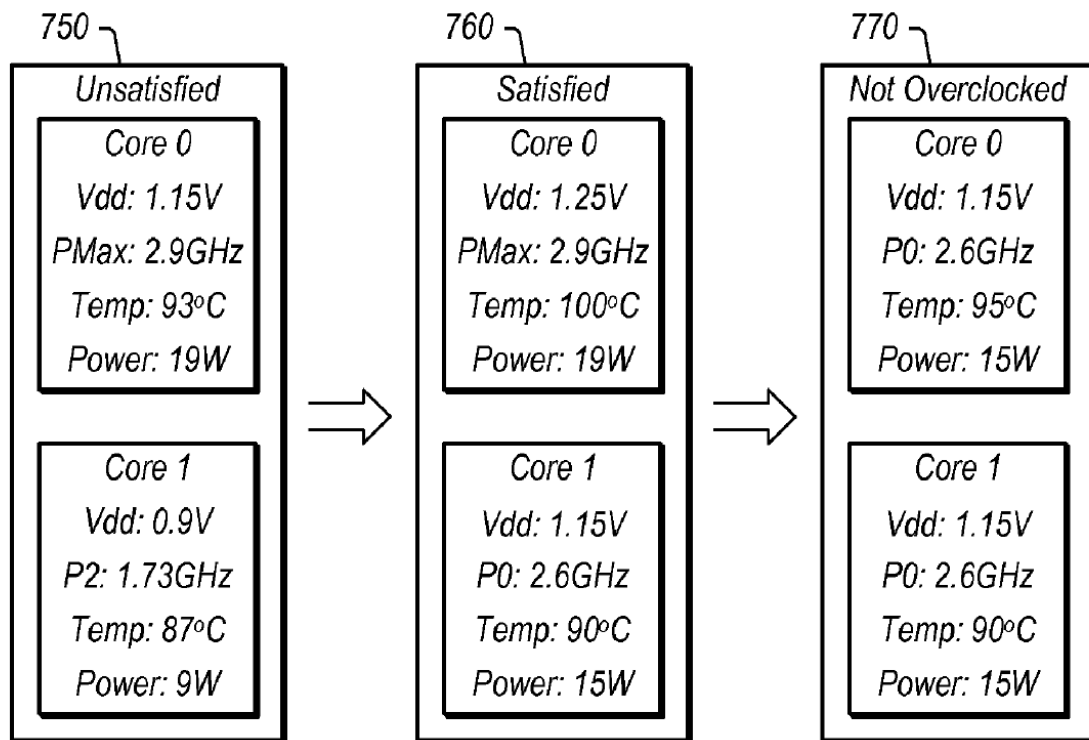


FIG. 7

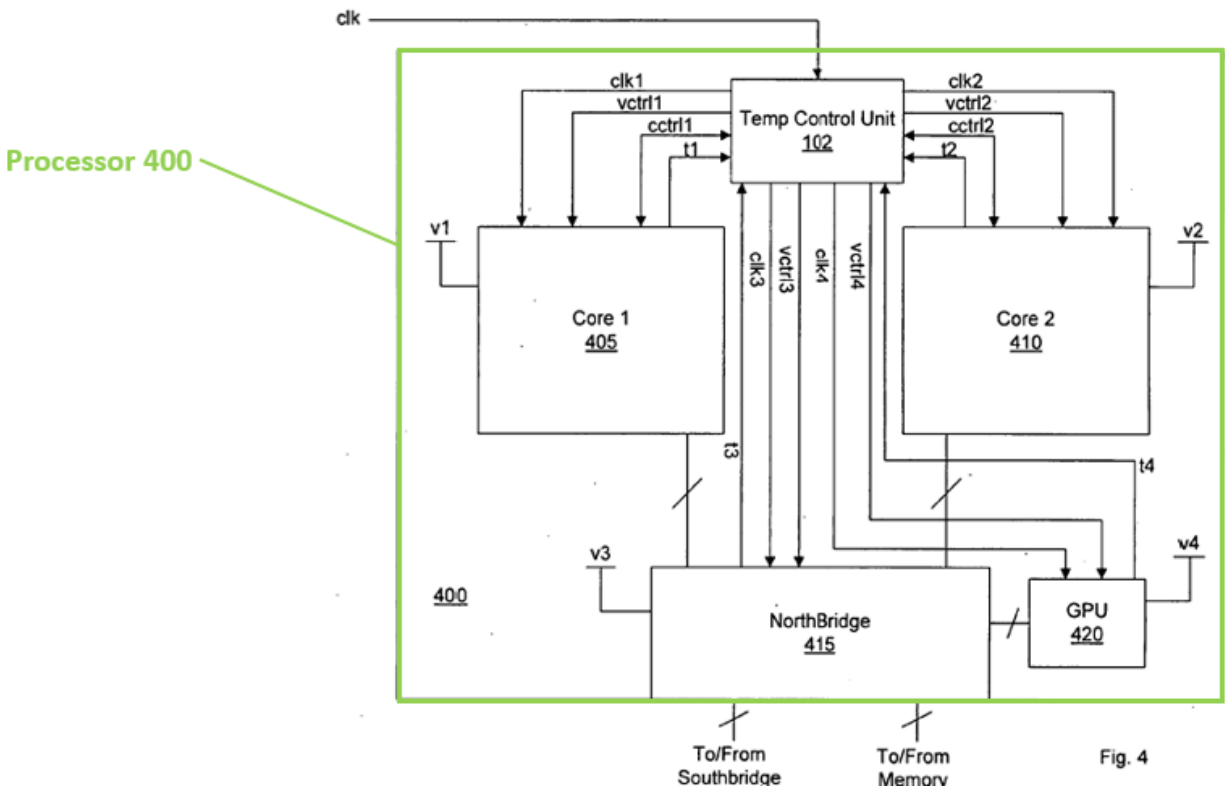
Indeed, Gold specifically teaches to monitor cores to prevent and control overheating *Id.*, ¶57 (“one or more temperatures or thermal characteristics are monitored to ensure that overclocked cores are not overheating.”).

A POSITA would have had a reasonable expectation of success in implementing Gold’s different frequencies with Cho’s temperature reduction actions because Gold specifically explains its temperature and frequency control by including flow charts, such as shown in Figures 3, 4, and 6. Ex-1002, ¶177.

2. Independent Claim 1

a. Element 1[pre]:

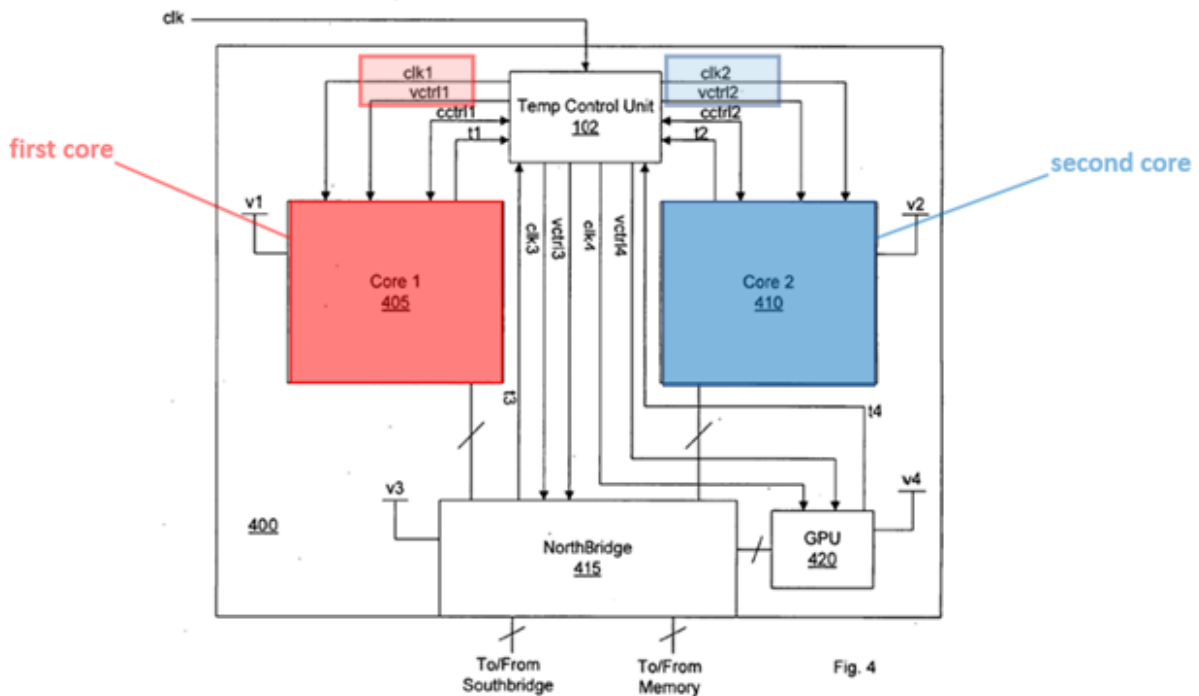
Cho teaches the preamble of Claim 1 to the extent it is limiting. Ex-1002, ¶¶178-180. Cho teaches a “multi-core processor” that is configured for “functional block level thermal control.” Ex-1005, ¶38. Cho’s processor includes “four primary functional units—two processor cores 405 and 410, a memory controller hub (NorthBridge 415), and a graphics processing unit (GPU) 420.” *Id.* Figure 4 illustrates Cho’s processor, 400 (green):



Ex-1005, Fig. 4 (annotated).

**b. Element 1[a]: a plurality of cores including a first core
...**

Cho discloses Element 1[a]. Ex-1002, ¶¶181-184. Cho discloses that “processor 400 includes four primary functional units,” including “two processor cores 405 [red] and 410” (blue). Ex-1005, ¶38. Cho’s processor core 405 (red) in Figure 4, is a “first core.” Ex-1002, ¶181.



Ex-1005, Fig. 4 (annotated).

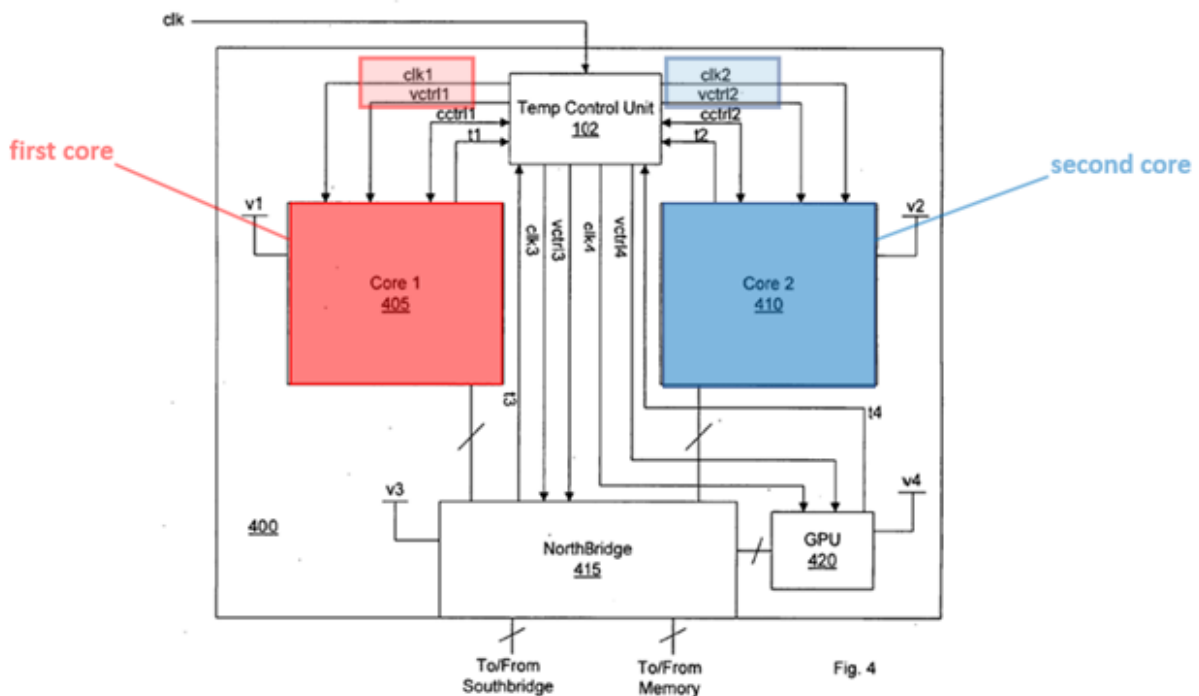
Cho discloses that “each of the functional units ... includes a voltage plane through which power is supplied independent of power supplied to the other functional units.” Ex-1005, ¶21. A “[p]ower control unit 320” provides a “corresponding voltage control signal to each of the functional units,” and each “voltage control signals vctrl1-vctrl4 corresponds to a unique one of the functional units.” *Id.*, ¶37. Cho’s first core is thus operable at a first voltage, set by the “vctrl1” signal. Ex-1002, ¶¶183.

Cho also discloses that a “clock control unit is coupled ... to provide separate clock signals to each of the functional units (e.g., clk1 to a first functional unit, clk2 to a second functional unit, and so forth.” Ex-1005, ¶35. The clock control unit

“adjust[s] the frequency of each of clock signals clk1-clk4, *independently of one another*, based on signals received from control logic 305.” *Id.* Cho’s first core is thus operable at a first frequency, set by “clk1” (*see id.*, Fig. 4 (red box around clk1 and vctrl1)). Ex-1002, ¶184.

c. Element 1[b]: a second core ...

Cho-Gold disclose Element 1[b]. Ex-1002, ¶¶185-197. Cho discloses that “processor 400” includes “two processor cores 405 and 410” Ex-1005, ¶38. Cho’s processor core 410 (blue), shown in annotated Figure 4, is a “second core.” Ex-1002, ¶185.



Ex-1005, Fig. 4 (annotated).

The second core is operable at a “second voltage independent of the first voltage.” Ex-1002, ¶187. Each functional unit, including the second core, has “a voltage plane through which power is supplied independent of power supplied to the other functional units.” Ex-1005, ¶21. Cho also discloses that “*the voltages on the voltage planes for each of the functional units can be set independently of one another.*” *Id.* Each “of the functional units ... is coupled to receive a voltage control signal that can change the voltage on a corresponding voltage plane *without affecting the voltages on the voltage planes* of any of the other ones of the functional units.” *Id.*, ¶40. Thus, the second core is operable at a second voltage, “vctrl2,” independent of the first voltage. Ex-1002, ¶187.

Additionally, the “second core is operable at a ... second frequency different from the first frequency.” Ex-1002, ¶188. First, as noted above, Cho discloses a “clock control unit” that is coupled “to provide *separate* clock signals to each of the functional units.” Ex-1005, ¶35. And, “a change in the clock frequency for a clock signal provided to one functional unit need not affect the frequencies of the respective clock signals provided to other ones of the functional units.” *Id.* The clock signals operate in frequencies “independently of one another, based on signals received from control logic 305.” *Id.* The second frequency of core 2 is set by “clk2,” which is a different signal than “clk1” that sets the frequency for core 1.

Additionally, as discussed above in Section XII.D.1, Cho discloses each functional unit's operating temperature is proportional to a frequency at which the functional unit is operating. Ex-1002, ¶189. Specifically, "TCU 102 is further configured to control the frequency of clock signals clk1-clk4 based on temperature data that is reported by functional units 105-120." Ex-1005, ¶22. Cho explains that "TCU 102 may lower the frequency of the clock signal" of a functional unit if the operating temperature is above a desired setting. *Id.* As explained, Cho teaches at least four different temperature settings: a maximum value, a minimum value, a first intermediate value, and a second intermediate value.³ Cho also teaches four different clock frequency signals: clk1, clk2, clk3, and clk4. Based on Cho's teachings, a POSITA would have understood that core 1 is operable at a maximum temperature, settable by a first frequency clk1, while core 2 is operable at a first intermediate temperature, settable by a different second frequency clk2. Ex-1002, ¶189. While Cho does not state the specific operating frequencies of clk1 and clk2, a POSITA would have understood these frequencies to be operable at different values to correspond to the respective different operating temperatures. *Id.*

³ In fact, Cho teaches that there may be more than four temperature control settings, but 4 is all that is necessary to apply the prior art to the claims. Ex-1005 ("TCU 102 may also perform temperature control actions based on one *or more* intermediate temperature thresholds that are between maximum and minimum values.")

Additionally, to the extent that a POSITA desired additional information about four different operating frequencies and corresponding power dissipations, these teachings are provided by Gold. Like Cho, Gold discloses multiple components (e.g., “Core 0” and “Core 1”) that are each operable at different frequencies:

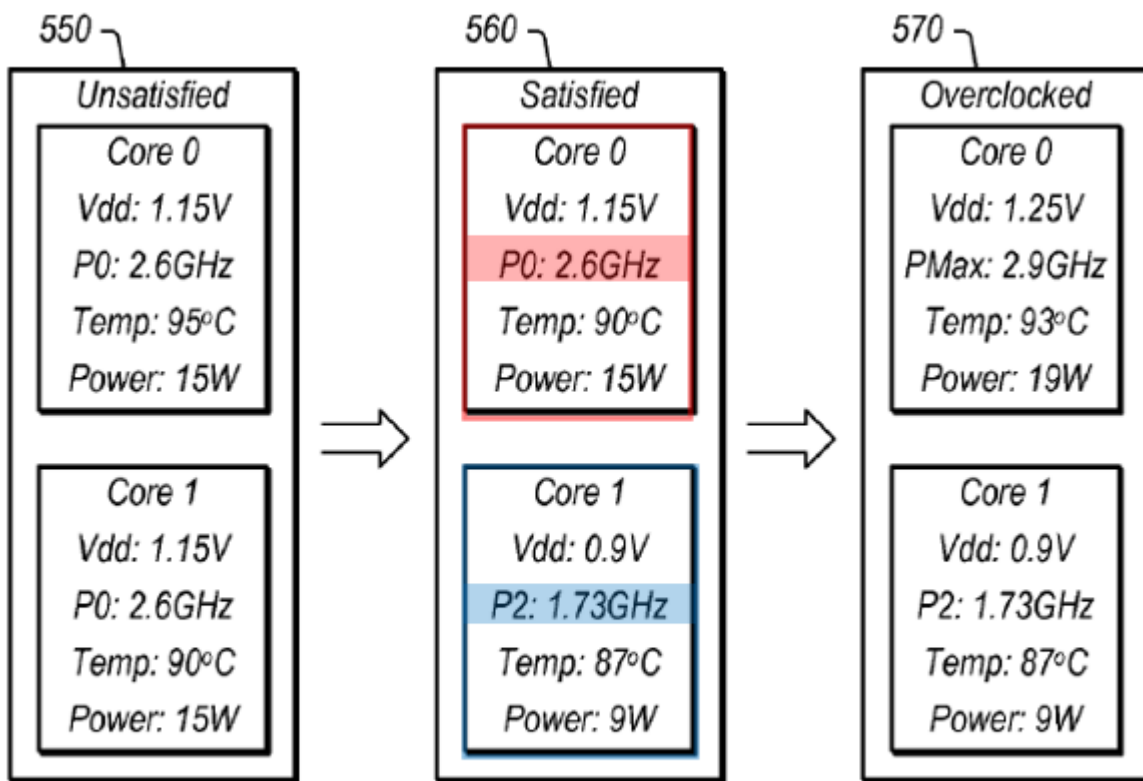
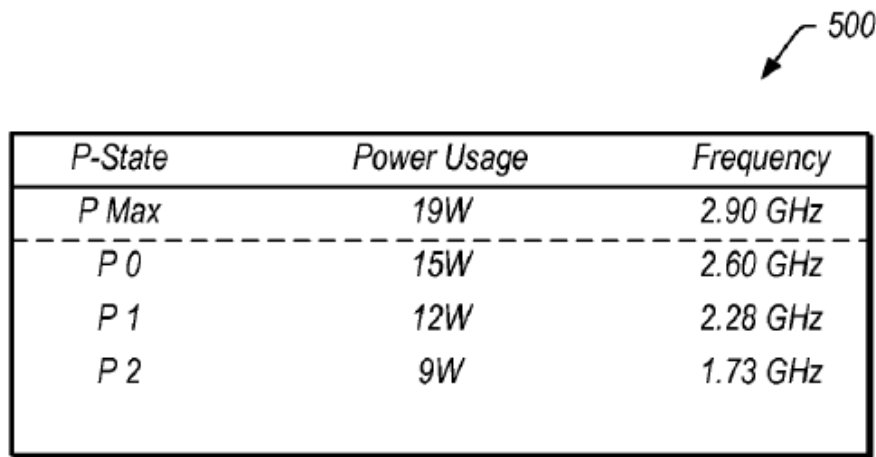


FIG. 5B

Ex-1009, Fig. 5B (annotated), ¶5 (“In one embodiment, an apparatus includes a plurality of processing cores (each of which has a respective standard operating frequency”). Indeed, Gold specifically teaches four *different* operating frequencies.

Gold teaches that its processors may be operable at distinct “performance states” (Pstate), such as PMax, P0, P1, P2, which each includes a “corresponding input voltage and clock frequency.” Ex-1009, ¶39. Figure 5 illustrates Gold’s performance states with four different frequency states and corresponding power usages: 2.9 GHz and 19 Watts, 2.6 GHz and 15 Watts, 2.28 GHz and 12 Watts, and 1.73 GHz and 9 Watts.



<i>P-State</i>	<i>Power Usage</i>	<i>Frequency</i>
<i>P Max</i>	19W	2.90 GHz
<i>P 0</i>	15W	2.60 GHz
<i>P 1</i>	12W	2.28 GHz
<i>P 2</i>	9W	1.73 GHz

FIG. 5A

Id., Fig. 5A.

As detailed in Section XII.D.1, a POSITA would have been motivated to implement Gold’s teachings of different specific frequencies and performance states. Ex-1002, ¶192. A POSITA would have been motivated to assign specific and different frequency values (as taught by Gold) to Cho’s maximum temperature and first intermediate temperature because doing so would have allowed for more predictable and controllable temperature actions using “thermal information

corresponding to various utilization, temperature, and power entry/exit criteria” as taught by Gold. *Id.*; Ex-1009, ¶6. As shown in Gold’s Figure 7, this predictable relationship allows for improved power and temperature budgeting and controllability of each different component. Ex-1009, ¶66.

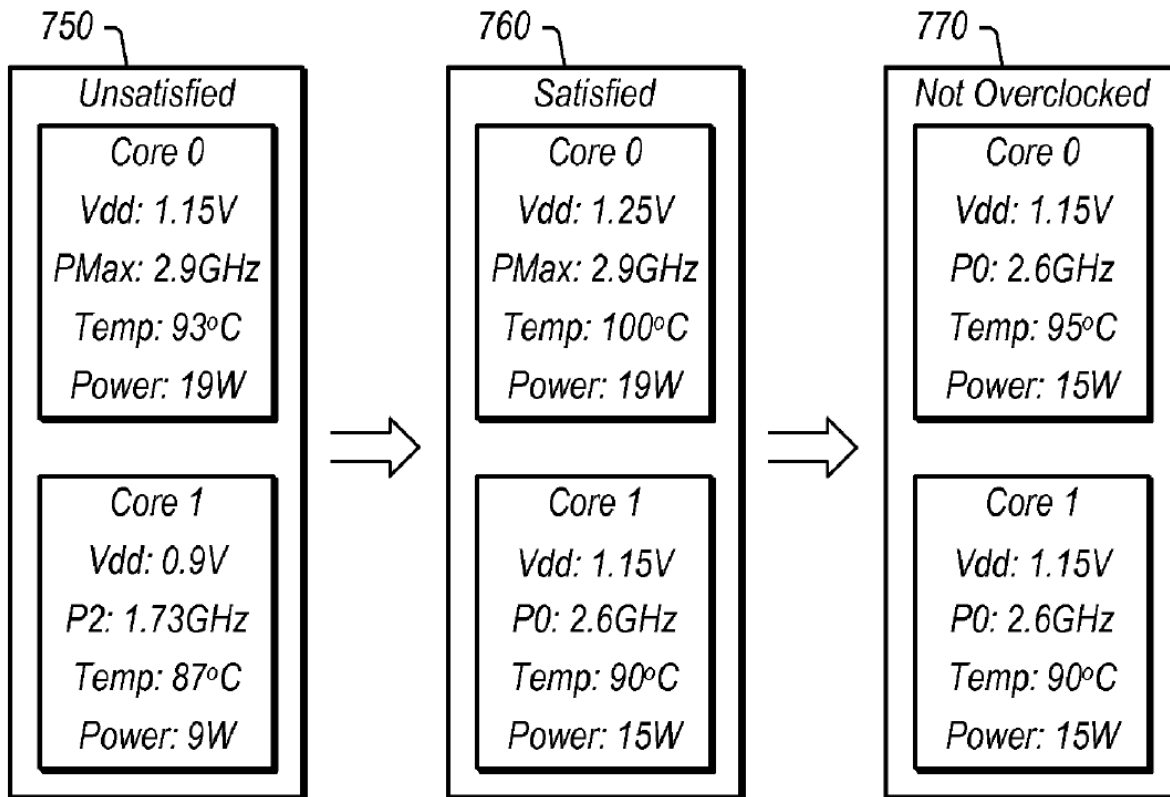


FIG. 7

Additionally, a POSITA would have had a reasonable expectation of success in implementing Gold’s different frequencies with Cho’s temperature reduction actions because Gold specifically includes a flow chart teaching how to make such controlled frequency reductions (step 650) based on temperature (step 610):

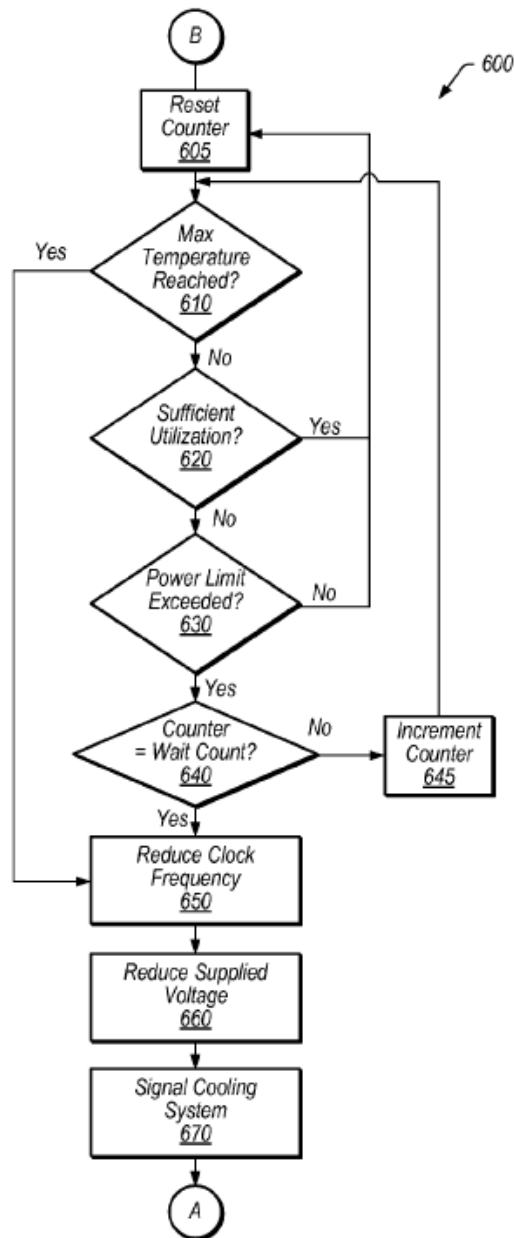
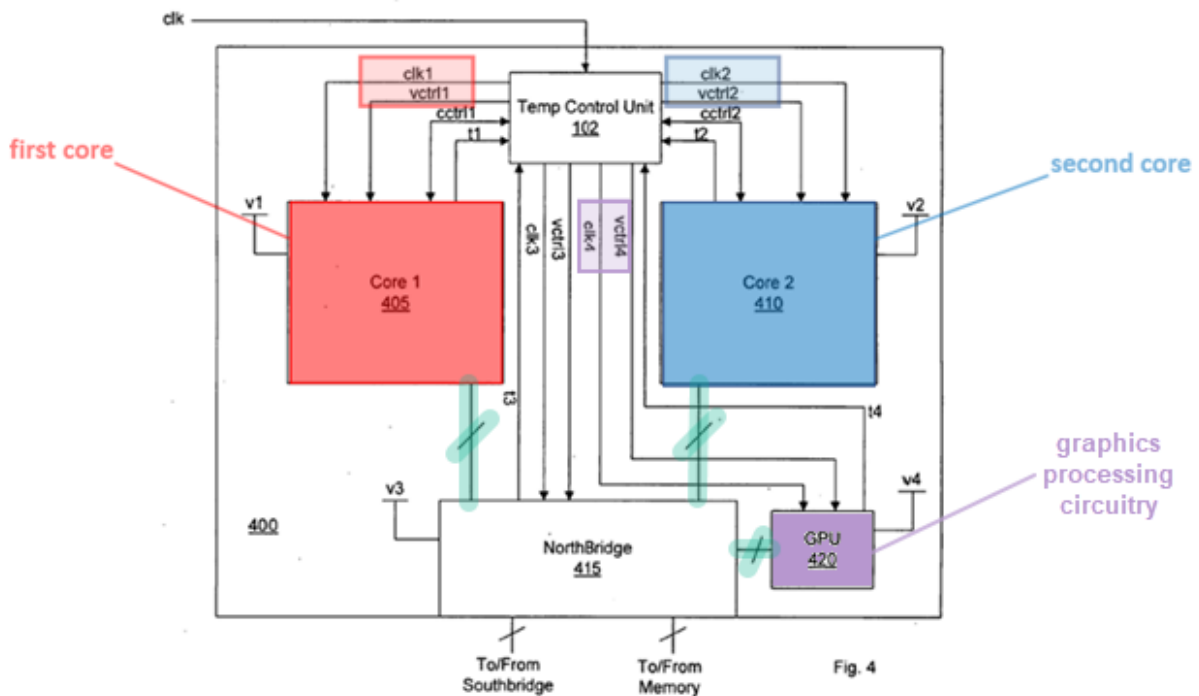


FIG. 6

d. Element 1[c]: graphics processing circuitry ...

Cho discloses Element 1[c]. Ex-1002, ¶¶198-204. Cho's multi-core processor includes "four primary functional units," one of which is a "graphics processing unit (GPU) 420." Ex-1005, ¶38, Fig. 4. The graphics processing unit 420 is "graphics

processing circuitry.” Ex-1002, ¶199. Figure 4 illustrates Cho’s graphics processing unit (GPU) 420 (purple):



Ex-1005, Fig. 4 (annotated). As Figure 4 also demonstrates, the graphics processing unit is coupled to Cho’s first and second cores through NorthBridge 415 and Temperature Control Unit 102 (green lines). *Id.*

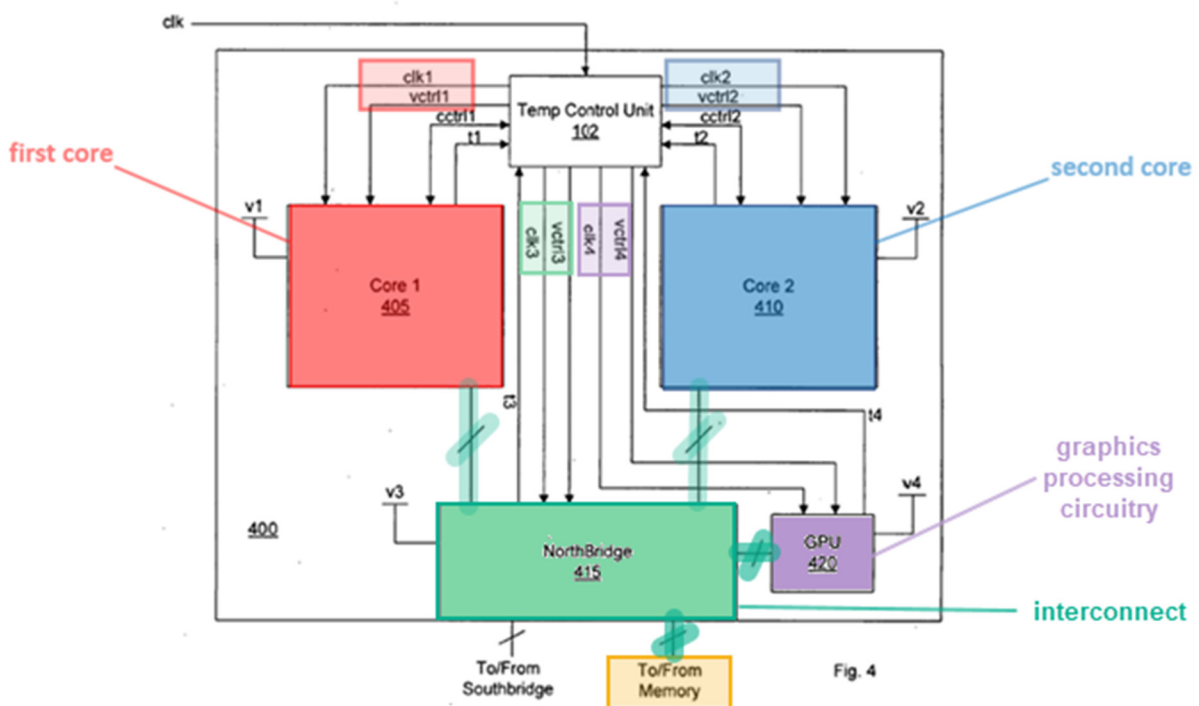
Cho’s graphics processing circuitry is also independently operable at a third frequency different from the first frequency and the second frequency. Ex-1002, ¶201. As explained in Section XII.D.2.b, a “clock control unit” provides “separate clock signals to each of the functional units ...” Ex-1005 ¶35. The clock signals operate in frequencies “*independently of one another*, based on signals received from control logic 305.” *Id.* Specifically, the third frequency of the GPU is set by

“clk4,” which is a different signal than both “clk1” and “clk2” that set the frequencies for core 1 and core 2. And, as discussed above in Section XII.D.1 and XII.D.2.c, “TCU 102 is further configured to control the frequency of clock signals clk1-clk4 based on temperature data that is reported by functional units 105-120.” Ex-1005, ¶22. Thus, a POSITA would have understood that core 1 is operable at a maximum temperature, settable by a first frequency clk1, core 2 is operable at a first intermediate temperature, settable by a different second frequency clk2, and the GPU is operable at a second intermediate temperature, settable by a different third frequency clk4. Ex-1002, ¶201. While Cho does not state the specific operating frequencies of clk1, clk2, or clk4, a POSITA would have understood these frequencies to be operable at different values to correspond to the respective different operating temperatures. *Id.*

Additionally, to the extent that a POSITA desired additional information about four different operating frequencies and corresponding power dissipations, these teachings are provided by Gold, as explained above in sections XII.D.1 and XII.D.2.c. And a POSITA would have been motivated to, and had a reasonable expectation of success in applying these teachings to Cho’s unique and independently operable clock frequency, clk4, for the same reasons. Ex-1002, ¶202.

e. Element 1[d]: an interconnect ...

Cho discloses Element 1[d]. Ex-1002, ¶¶205-211. Cho discloses that one of the four primary functional units is “a memory controller hub (NorthBridge 415).” Ex-1005, ¶38. Cho’s memory controller hub (NorthBridge 415) is an “interconnect” because it connects the processor’s various components. Ex-1002, ¶206. A POSITA would have recognized the slash through the green lines as indicating multibit paths interconnected at NorthBridge 415 and would have further recognized the term “northbridge” as referring to a commonly known interconnect at the time of the ’588 Patent. *Id.* Figure 4 illustrates memory controller hub (NorthBridge 415) (green):



Ex-1005, Fig. 4 (annotated). As Figure 4 illustrates, memory controller hub (NorthBridge 415) (the “interconnect”) connects graphics processing unit (GPU)

420 (the “graphics processing circuitry”) to off-processor memory (orange) via a multibit path (green). *Id.* As shown in Figure 4, “clk3” is the clock signal for Northbridge 415. *Id.*

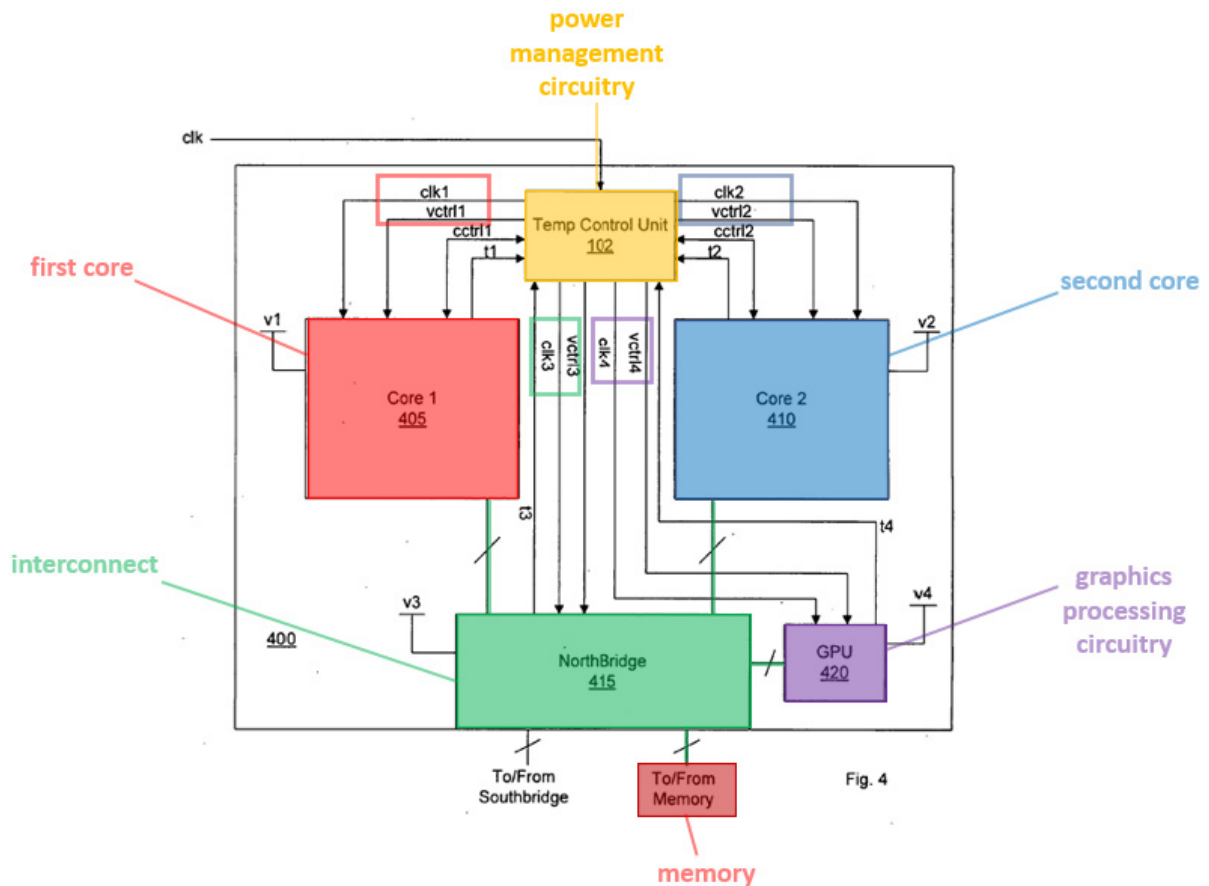
NorthBridge 415 is operable at a fourth frequency different from the first frequency and the second frequency. Ex-1002, ¶208. As explained in Section XII.D.2.b, a “clock control unit” provides “separate clock signals to each of the functional units” Ex-1005 ¶35. The clock signals operate in frequencies “***independently of one another***, based on signals received from control logic 305.” *Id.* Specifically, the fourth frequency of the NorthBridge 415 is set by “clk3,” which is a different signal than both “clk1” and “clk2” that set the frequency for core 1 and core 2. And, as discussed in Section XII.D.1 and XII.D.2.c, “TCU 102 is further configured to control the frequency of clock signals clk1-clk4 based on temperature data that is reported by functional units 105-120.” Ex-1005, ¶22. Thus, a POSITA would have understood that core 1 is operable at a maximum temperature, settable by a first frequency clk1, core 2 is operable at a first intermediate temperature, settable by a different second frequency clk2, and the NorthBridge is operable at a minimum temperature, settable by a different fourth frequency clk3. Ex-1002, ¶208. While Cho does not state the specific operating frequencies of clk1, clk2, or clk3, a POSITA would have understood these

frequencies to be operable at different values to correspond to the respective different operating temperatures. Ex-1002, ¶208.

Additionally, to the extent that a POSITA desired additional information about four different operating frequencies and corresponding power dissipations, Gold provides these teachings, as explained above in sections XII.D.1 and XII.D.2.c. And, a POSITA would have been motivated to, and had a reasonable expectation of success in applying these teachings to Cho's unique and independently operable clock frequency, clk3, for the same reasons. Ex-1002, ¶209.

3. Dependent Claim 2: first power management circuitry

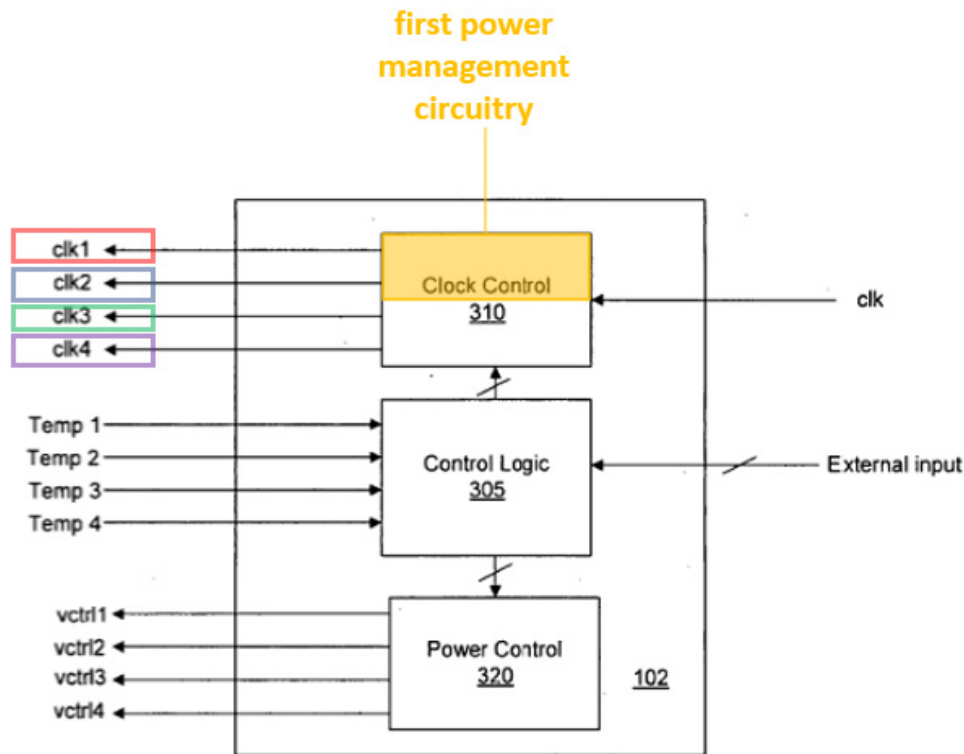
Cho-Gold disclose Claim 2. Ex-1002, ¶¶212-216. Cho discloses that a “temperature control unit 102 includes control logic 305” and “clock control logic 310.” Ex-1005, ¶32. Figure 4 illustrates the temperature control unit 102 (yellow) containing control logic 305 and clock control logic 310:



Id., Fig. 4 (annotated).

The clock control unit 310 “provide[s] separate clock signals to each of the functional units (e.g., clk1 to a first functional unit, clk2 to a second functional unit, and so forth).” Ex-1005, ¶35. The clock control unit 310 includes “a plurality of independently controllable phase locked loops (PLLs), each coupled ... to provide a corresponding one of the clock signals to a functional unit.” *Id.* The PLLs of Cho’s clock control unit are a “first power management circuitry and/or logic.” Ex-1002, ¶214

Figure 3 illustrates Cho’s clock control unit 310 (yellow):



Ex-1005, Fig. 3 (annotated).

Cho also discloses that “[c]lock control unit 310 is configured to adjust the frequency of each of clock signals clk1-clk4, independently of one another, based on signals received from control logic 305.” Ex-1005, ¶35. For example, the clock control unit may cause the first and second cores to operate independently at first and second frequencies “for temperature control purposes.” *Id.*, ¶36. Indeed, “if a given functional unit is reporting a temperature over a predetermined threshold, control logic 305 may direct clock control unit 310 to reduce the frequency of its corresponding clock signal.” *Id.* A POSITA would have known that the PLLs of

clock control unit 310 thus cause the first and second cores to operate independently at first and second frequencies. Ex-1002, ¶216.

4. Dependent Claim 4: second power management circuitry ...

Cho-Gold disclose Claim 4. Ex-1002, ¶¶217-219. The clock control unit 310 includes “a plurality of independently controllable phase locked loops (PLLs), each coupled ... to provide a corresponding one of the clock signals to a functional unit.” Ex-1005, ¶35. The PLL that provides clock signal clk4 to graphics processing unit 420 (orange) is a “second power management circuitry,” as illustrated in Figure 3. Ex-1002, ¶217.

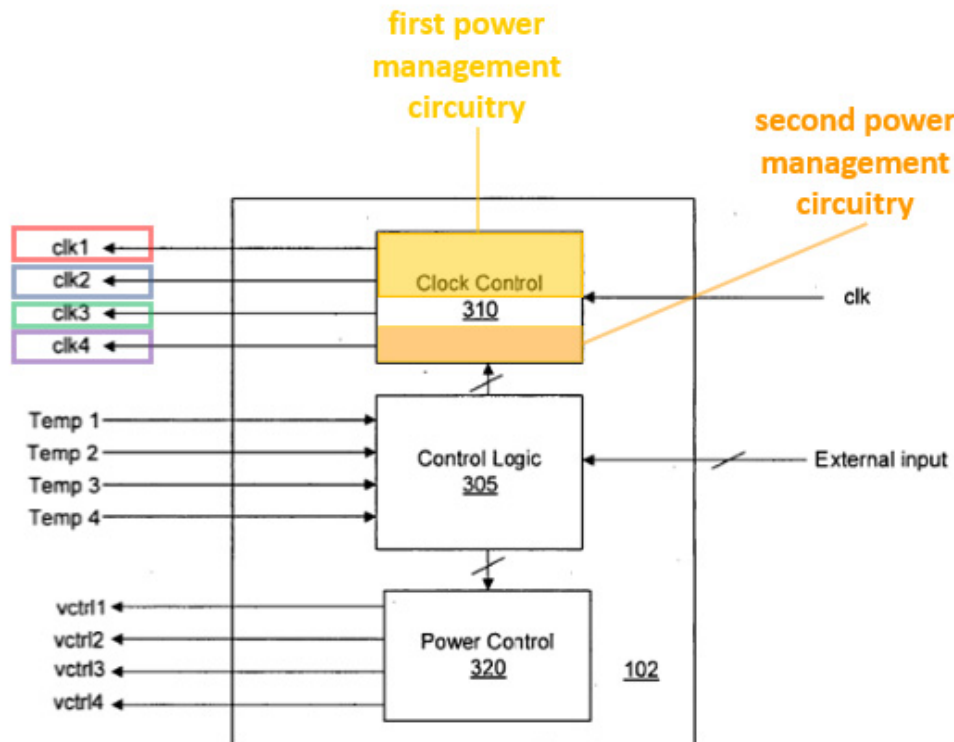


Fig. 3

Id., Fig. 3 (annotated).

As explained in Section XII.D.2.c, “[c]lock control unit 310 is configured to adjust the frequency of each of clock signals clk1-clk4, independently of one another, based on signals received from control logic 305.” Ex-1005, ¶35. For example, the clock control unit may cause graphics processing unit 420 to operate independently at a third frequency “for temperature control purposes.” *Id.*, ¶36.

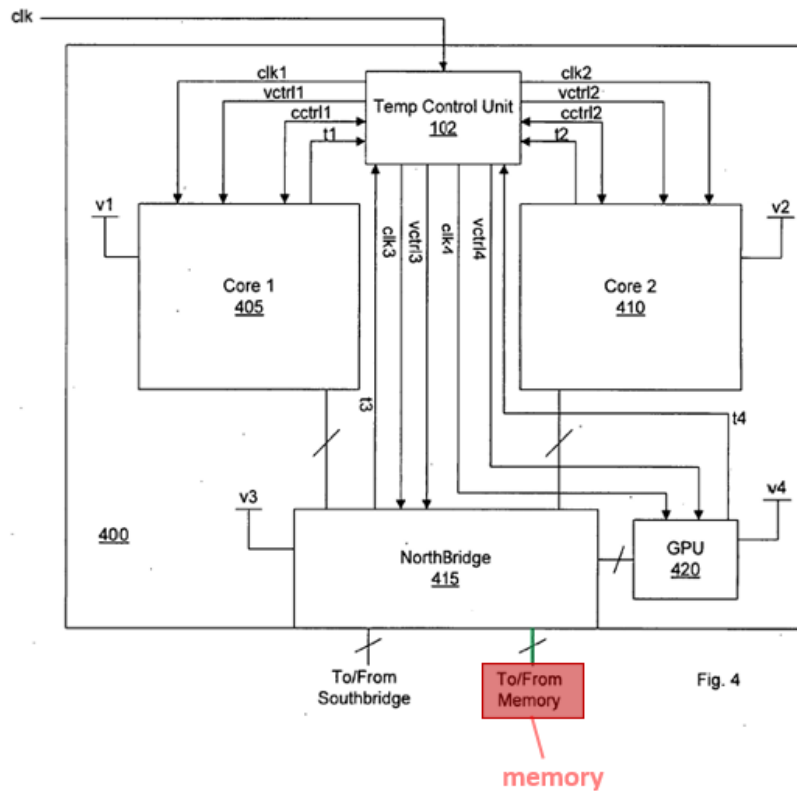
5. Independent Claim 8

a. Element 8[pre]: A system comprising:

Cho discloses Claim 8’s preamble to the extent it is limiting. Ex-1002, ¶¶220-221. Cho discloses that its “integrated circuit” is “a processor, such as a microprocessor suitable for use in a computer system.” Ex-1005, ¶9.

b. Element 8[a]: a system memory;

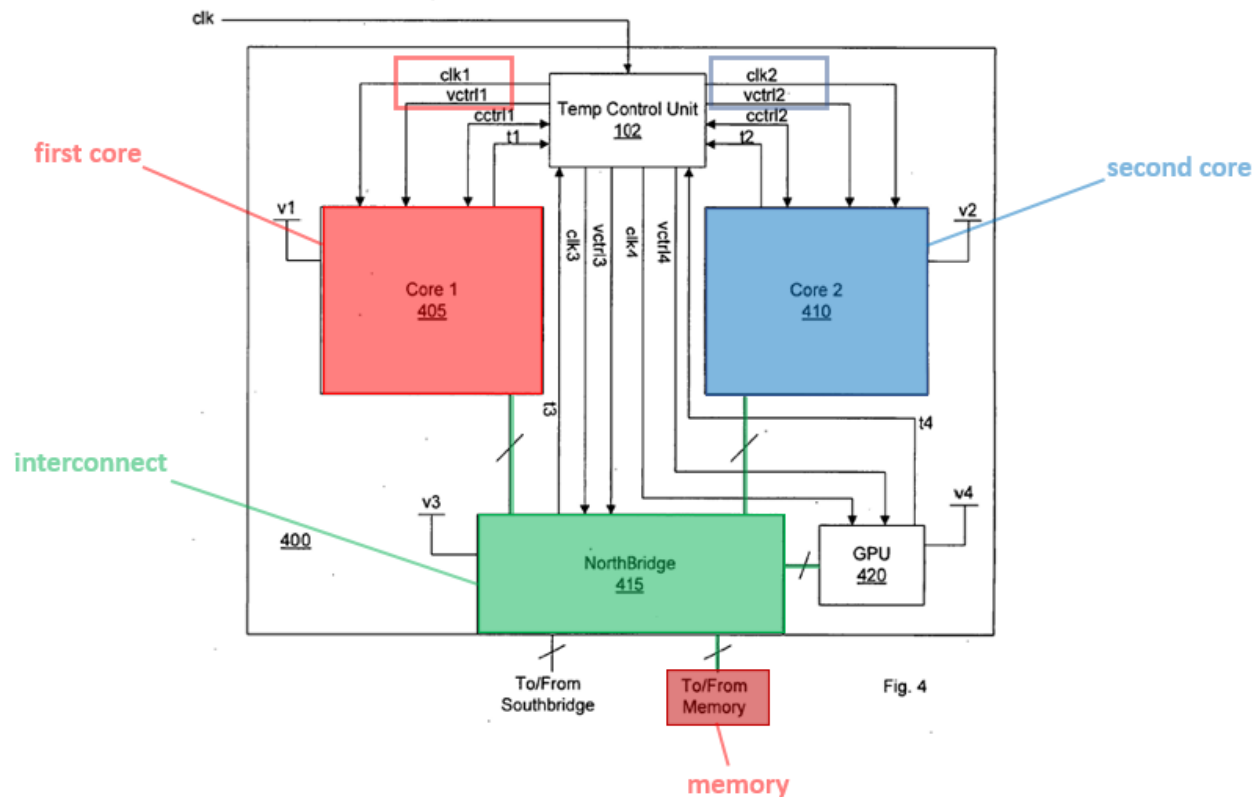
Cho discloses Element 8[a]. Ex-1002, ¶¶22-223. Cho discloses that the processor includes “a memory controller hub (NorthBridge 415).” Ex-1005, ¶38. As Figure 4 illustrates, the memory controller hub (NorthBridge 415) connects to system memory (maroon).



Id., Fig. 4 (annotated).

c. Element 8[b]: a plurality of cores ...

As discussed in Section XII.D.2.b, discloses a plurality of cores. Ex-1002, ¶¶224-225. As illustrated in Figure 4, the first and second cores (red and blue) are connected to memory (maroon) through NorthBridge 415 (green):



Ex-1005, Fig. 4 (annotated).

d. Element 8[c]: a first core ... and a second core ...;

As discussed in Sections XII.D.2.b-c, Cho-Gold disclose Element 8[c].

Ex-1002, ¶¶226.

e. Element 8[d]: graphics processing circuitry ...

As discussed in Section XII.D.2.d, Cho-Gold disclose Element 8[d]. Ex-1002, ¶227.

f. Element 8[e]: an interconnect ...

As discussed in Section XII.D.2.e, Cho-Gold disclose Element 8[e]. Ex-1002, ¶228.

6. Dependent Claim 9: first power management circuitry ...

For the reasons described above for Claim 2, Cho-Gold disclose Claim 9. Ex 1002, ¶229.

7. Dependent Claim 11: second power management circuitry ...

For the reasons described above for Claim 4, Cho-Gold disclose Claim 11. Ex 1002, ¶230.

8. Independent Claim 20

a. Element 20[pre]: An apparatus comprising:

Cho teaches the preamble of Claim 20 to the extent it is limiting. Ex-1002, ¶¶231-232. Cho teaches a “multi-core processor,” which is an apparatus, configured for “functional block level thermal control.” Ex-1005, ¶38.

b. Element 20[a]: means for operating ...

As described in Sections XII.D.1.b-d, the equivalent structure is Cho’s TCU 102, that “perform[s] temperature control actions.” TCU 102 controls each functional unit (e.g., “core” or “GPU”) based on “a number of different [temperature] thresholds,” including maximum, one or more intermediate, or minimum thresholds. Ex-1005, ¶24. For example, if a functional unit’s temperature exceeds a maximum allowable threshold, TCU 102 may “reduc[e] its respective clock frequency or voltage in an attempt to reduce the temperature of the functional unit.” *Id.* Moreover, as explained, TCU 102 provides the capability to operate the

first core, second core, and GPU at independent and distinct voltages and frequencies, respectively. Ex-1002, ¶¶233-234

c. Element 20[b]: means for independently operating ...

As described in Section XII.D.4, the equivalent structure is the “plurality of independently controllable phase locked loops (PLLs)” in clock control unit 310. Ex-1005, ¶35. The PLL that provides clock signal clk4 to graphics processing unit 420 is a “second power management circuitry.” See Figure 3, Ex-1002, ¶235.

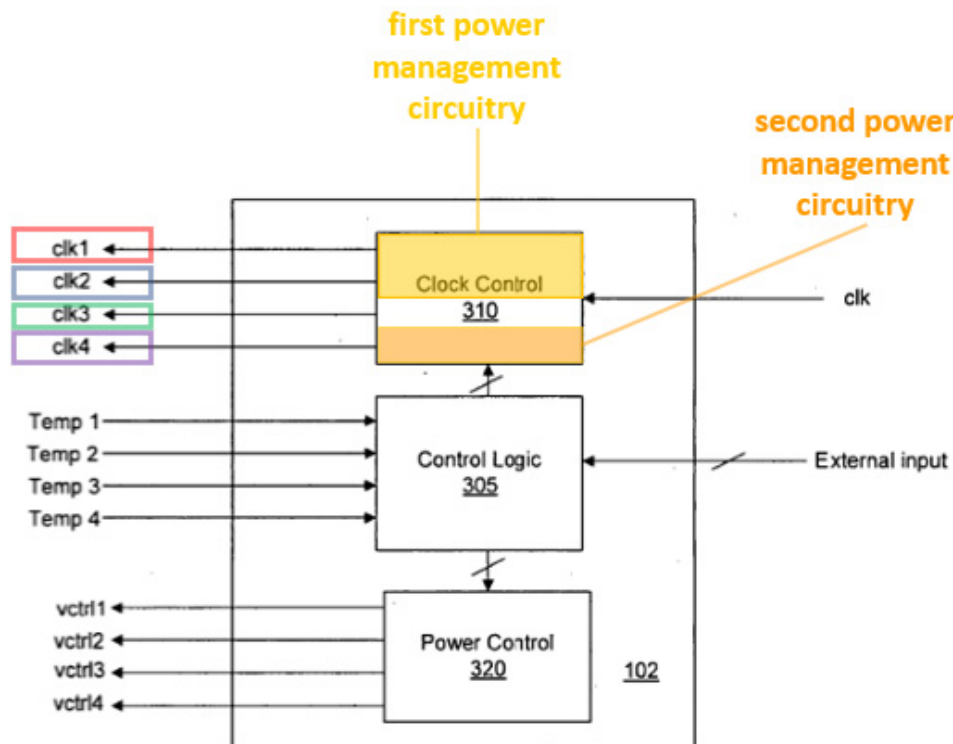


Fig. 3

d. Element 20[c]: interconnect means

As described in Section XII.D.1.e, the equivalent structure is Cho's "memory controller hub (NorthBridge 415)" which acts to connect the processor's various components. Ex-1005, ¶38, Ex-1002, ¶¶236-237.

E. Ground 5: Claims 3, 7, 10, and 14-19 are rendered obvious by Cho, Gold, and Aguilar.

1. A POSITA would have been motivated to combine Cho, Gold, and Aguilar's teachings and would have had a reasonable expectation of success.

In addition to the reasons set forth below, a POSITA would have been motivated to combine the teachings of Cho, Gold, (Cho-Gold) and Aguilar and would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. Ex-1002, ¶¶238-244.

Cho-Gold and Aguilar relate to and describe similar methods for controlling and optimizing temperature within computer systems. Ex-1005, Abstract; Ex-1007, Abstract. For example, Cho discloses "a temperature control unit ... wherein the temperature control unit is configured to monitor a temperature of each of the plurality of functional units based on temperature information provided from the temperature sensors." Ex-1005, Abstract. The temperature control unit is then configured to, if the temperature exceeds a first threshold value, "perform a first temperature control action" *Id.* Likewise, Gold discloses its processor "may be coupled to cooling subsystem 120" to "control the temperature(s) of processing

subsystem 110” and tracks “temperature criteria” to determine whether to apply overclocking. Ex-1009, ¶¶19, 41. Similarly, Aguilar discloses “[a] computer implemented method, data processing system, and computer usable code ... for optimizing thermal performance of a computer system.” Ex-1007, Abstract. Aguilar requests “a thermal index is ... for each of the set of system resources to form a set of thermal indexes.” *Id.* Then, “[a]n action from a set of actions is identified to reduce resource utilization” and “reduce a thermal state of the computer system.” *Id.*

Moreover, Cho and Aguilar include similar NorthBridge-SouthBridge architecture. Ex-1002, ¶240. As illustrated in Figure 4, Cho relies on a connection between NorthBridge 415 (green) and SouthBridge (yellow) to carry out its computer functions:

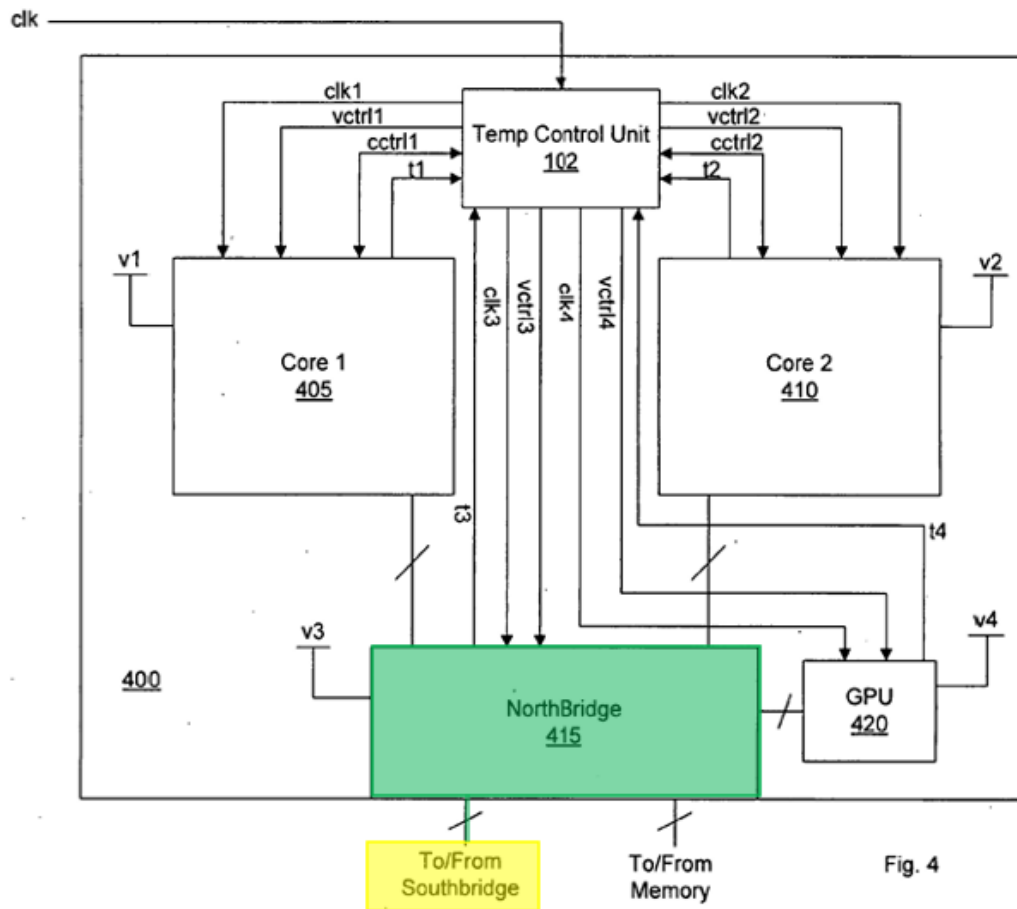
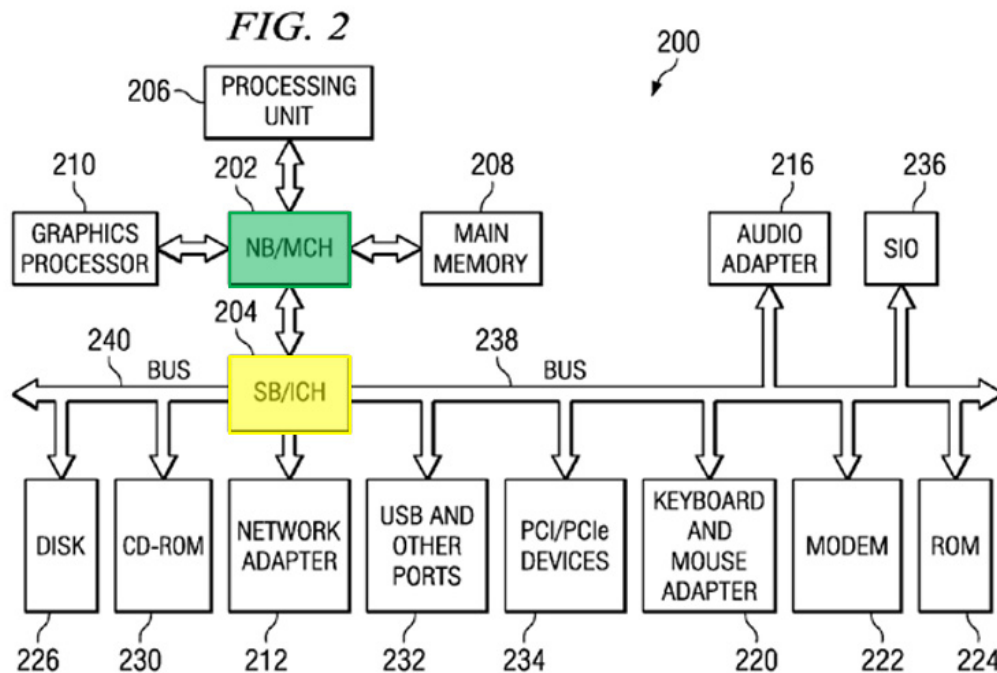


Fig. 4

Ex-1005, Fig.4. Likewise, as illustrated in Figure 2, Aguilar also relies on a NorthBridge (green)-SouthBridge (yellow) structure:



Ex-1007, Fig. 2. Thus, given Cho and Aguilar’s similar computer architecture, a POSITA would have understood that these systems are particularly compatible. Ex-1002, ¶242.

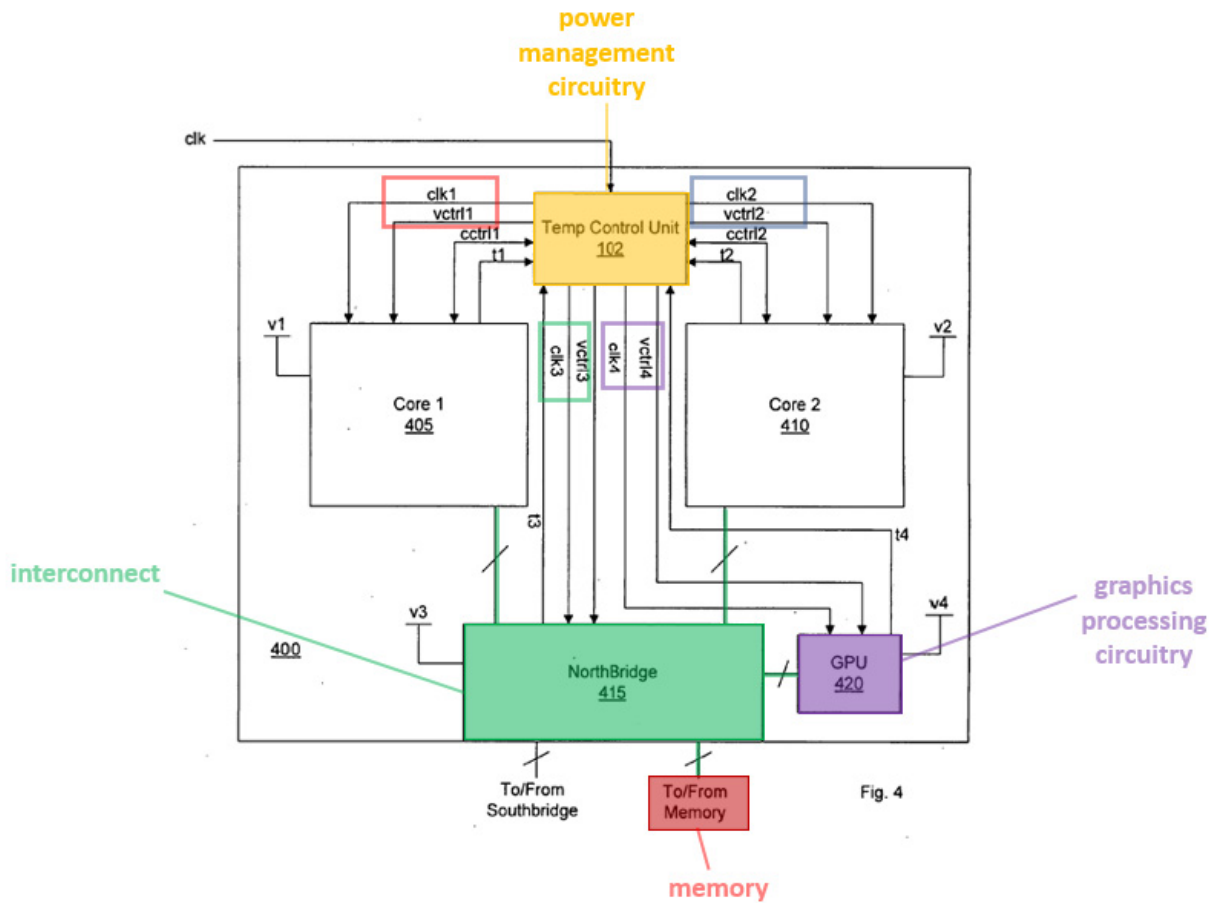
A POSITA would have been motivated to combine the teachings of Cho-Gold and Aguilar because they would have recognized the benefit of implementing an I/O controller hub, such as taught by Aguilar’s element 204, and thermal indexes in the combined Cho-Gold system to improve temperature control and resource utilization throughout a complete computer system. Ex-1002, ¶243. Aguilar teaches that “identification of a set of system resources” associated with a computer system “is performed and a thermal index is requested for *each // set* of system resources.” Ex-1007, Abstract (emphasis added). Aguilar teaches that a “set of actions is identified

to reduce resource utilization,” and the actions are “implemented to reduce a thermal state of the computer system.” *Id.*

A POSITA would also have had a reasonable expectation of success in combining the teachings of Cho-Gold and Aguilar. Ex-1002, ¶244. A POSITA would have understood that these references disclose interrelated teachings, including well-known temperature control methods and NorthBridge/SouthBridge architectures, based on routine technologies that would have been amendable to various well-understood and predictable combinations, as explained in further detail below. *Id.*

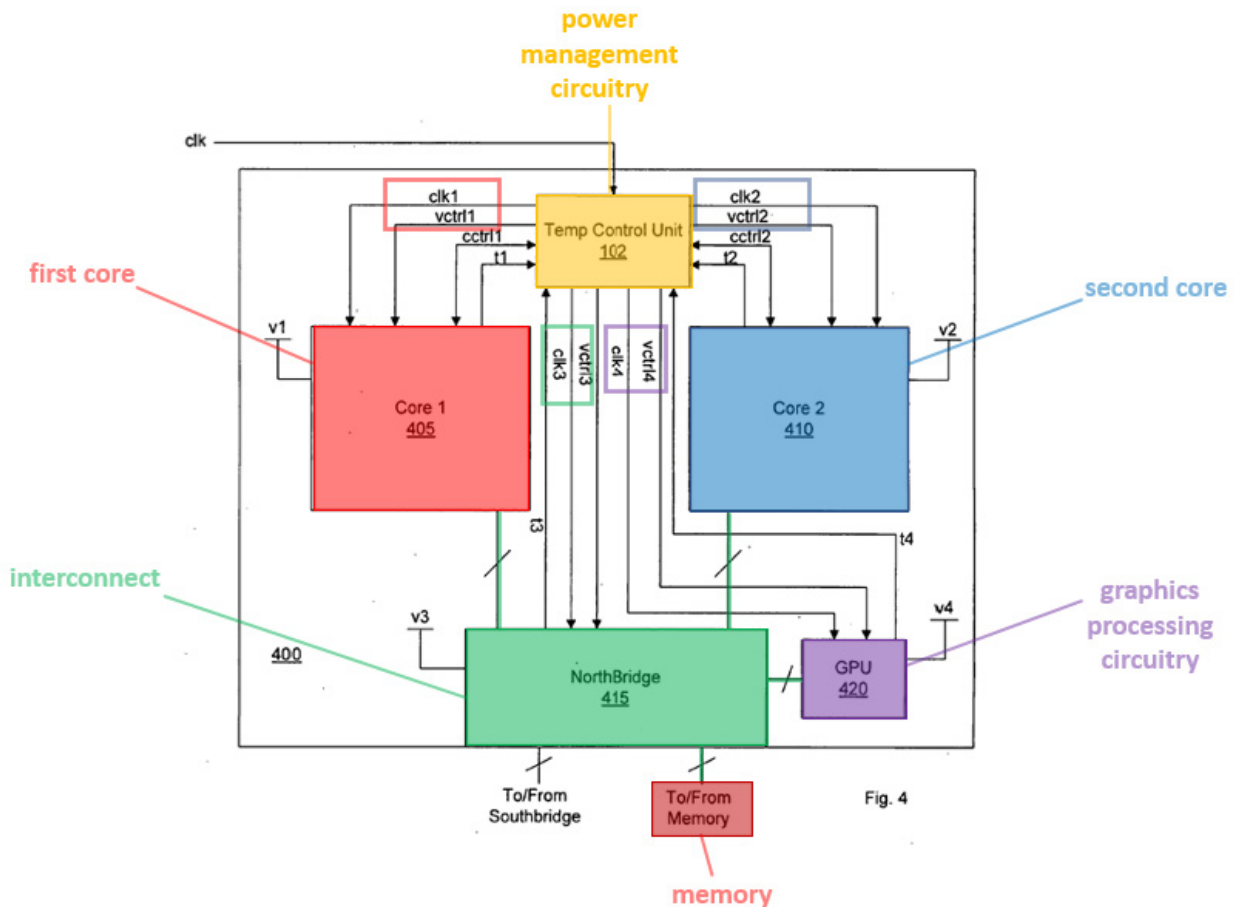
2. Dependent Claim 3: ... comprising a cache ...

Cho-Gold and Aguilar disclose Claim 3. Ex-1002, ¶¶245-246. The non-core components in Cho’s processor, including the GPU 420 (purple), memory controller hub (NorthBridge 415) (green), and Temperature Control Unit 102 (yellow) form a “non-core power domain.” *Id.*



Ex-1005, ¶38, Fig. 4 (annotated).

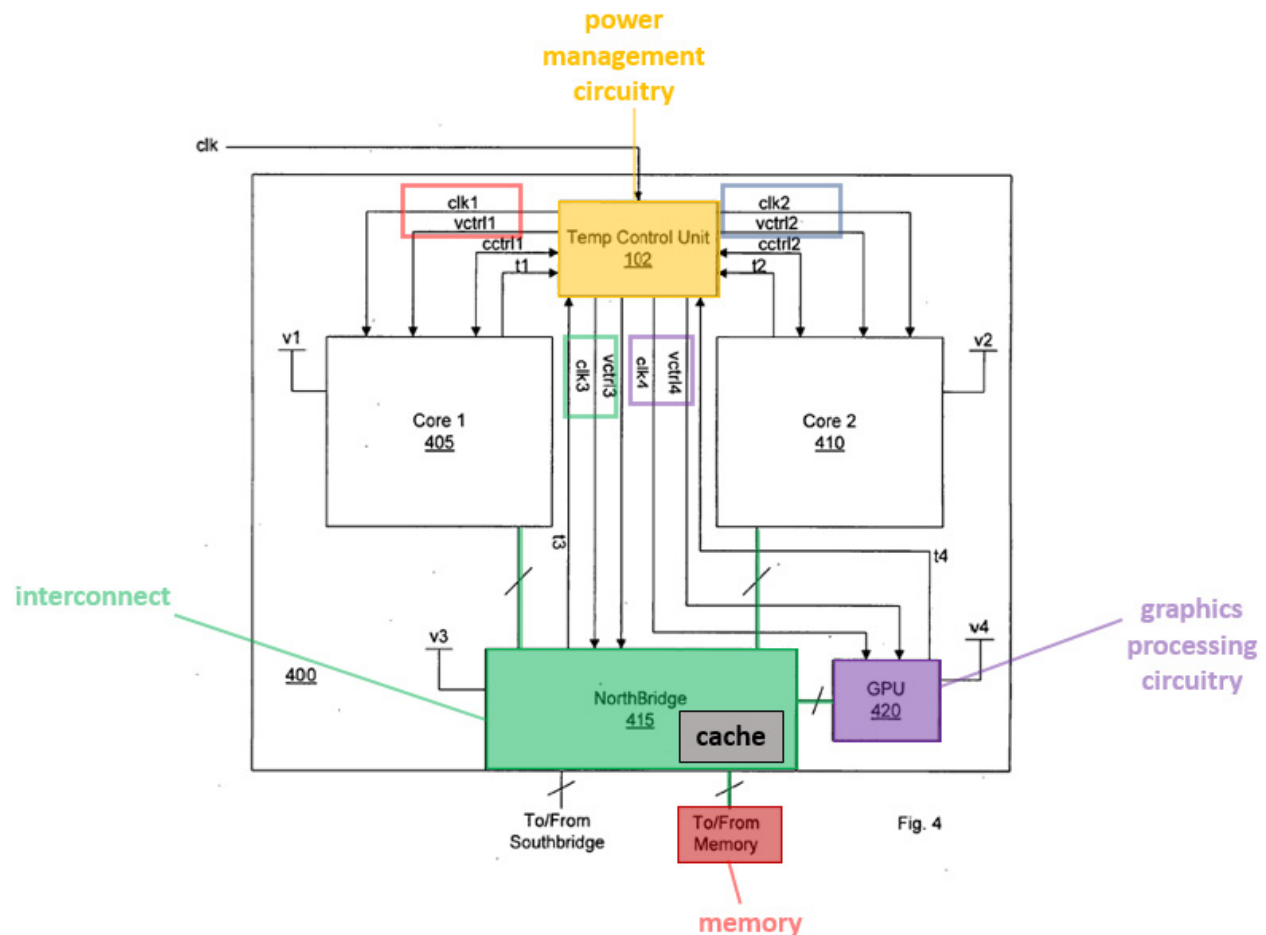
A POSITA would have understood that Cho's memory controller hub NorthBridge 415 contained a cache, specifically an on-chip or "Level 1" cache, because such "L1" caches were common components of high-performance processors at the time of the '588 Patent. Ex-1002, ¶247. Moreover, as Figure 4 illustrates, both Core 1 405 and Core 2 410 are connected to and share memory through controller hub (NorthBridge 415):



Ex-1005, Fig. 4 (annotated).

To the extent that a POSITA would have required any additional teaching that Cho's NorthBridge would have been implemented with a cache, Aguilar provides such teaching. Ex-1002, ¶249. Aguilar discloses that "memory may be ... a cache such as found in *north bridge* and memory controller hub 202 in Fig. 2." Ex-1007, 4:57-60. A POSITA would have been motivated to implement Cho's NorthBridge with a cache memory (illustrated in Figure 4 below), as taught by Aguilar, because including a cache makes retrieving data from a computer's

memory more efficient, data can be retrieved easily from cache memory, and data stored in caches is typically more readily available to system components than data stored in main memory. Ex-1002, ¶249.



Ex-1005, Fig. 4 (annotated).

3. Dependent Claim 7.

As discussed in Sections XII.D.2.d-e, Cho-Gold and Aguilar disclose Claim 7. Ex 1002, ¶250. A POSITA would have known Cho's power management circuitry and/or logic causes the non-core power domain to operate at a different

frequency from the first and second frequencies of the first and second cores because the GPU 420 and controller hub (NorthBridge 415), which are part of the non-core power domain, operate at different frequencies than the cores.

4. Dependent Claim 10.

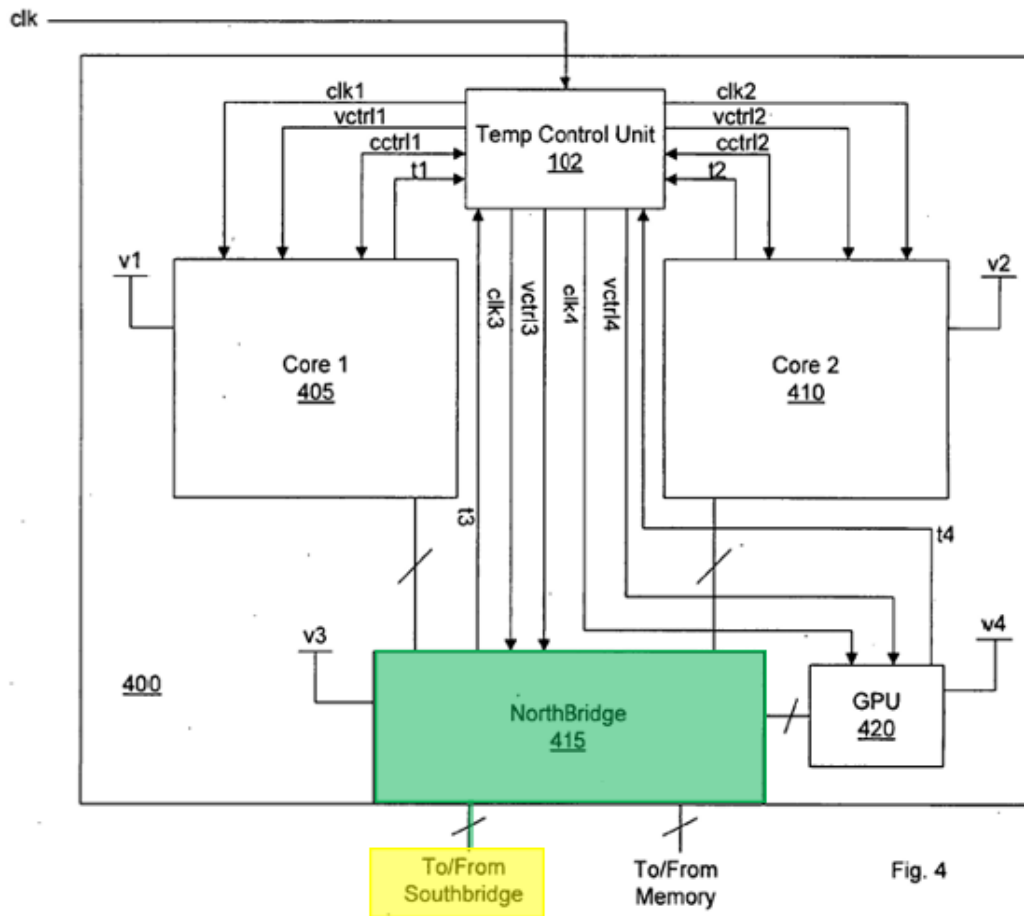
See discussion in Section XII.D.5, regarding Claim 8. For the reasons described above for Claim 3, Cho-Gold and Aguilar disclose Claim 10. Ex-1002, ¶251.

5. Dependent Claim 14.

For the reasons described above for Claim 7, Cho-Gold and Aguilar disclose Claim 14. Ex-1002, ¶252.

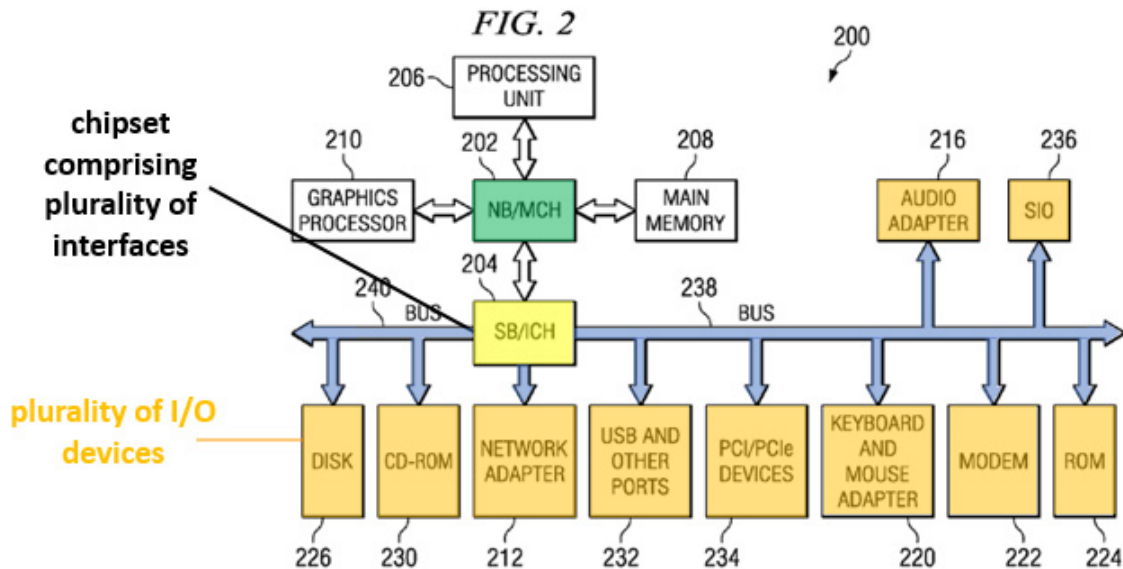
6. Dependent Claim 15: ... a plurality of I/O devices.

Cho-Gold and Aguilar disclose Claim 15. Ex-1002, ¶¶253-257. Cho discloses that NorthBridge 415 (green) is connected to a SouthBridge (yellow), as shown in annotated Figure 4:



Ex-1005, Fig. 4 (annotated). A POSITA would have known that a SouthBridge is “a chipset.” Ex-1002, ¶254. Moreover, as shown in Figure 4, the SouthBridge is connected to Core 1 405 and Core 2 410 through NorthBridge 415. *Id.*; Ex-1005, Fig. 4.

Additionally, Aguilar teaches a “south bridge and input/output (I/O) controller hub (ICH) 204.” Ex-1007, 3:44-52. Figure 2 illustrates Aguilar’s SouthBridge (yellow) and I/O controller hub (yellow):



Ex-1007, Fig. 2 (annotated).

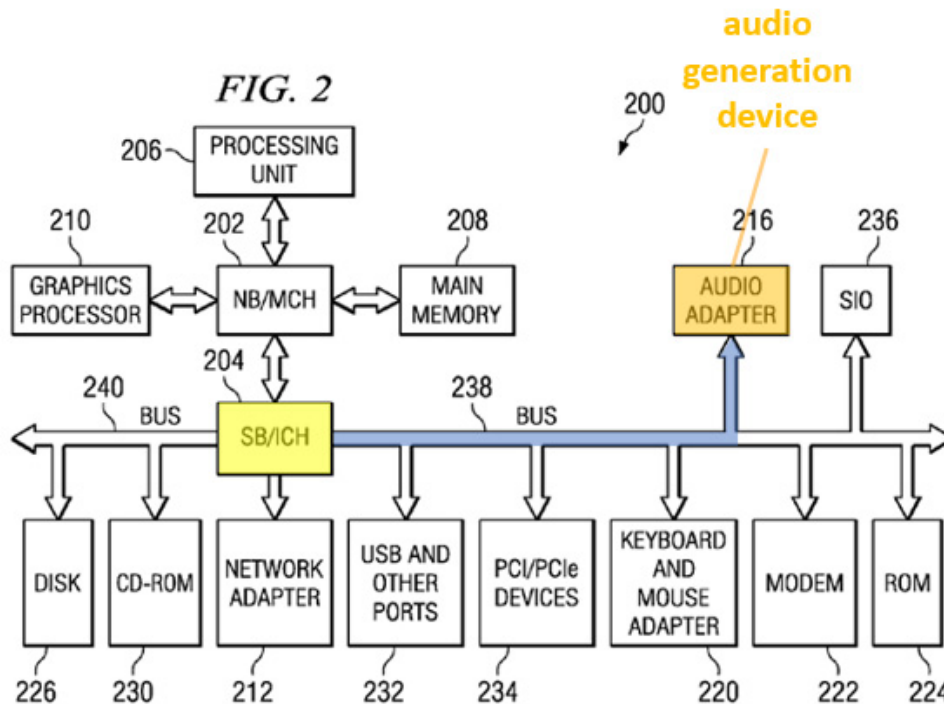
The SouthBridge and I/O controller hub connect to several I/O devices (orange) via buses 240 and 238 (blue), which a POSITA would have known are “interfaces.” Ex-1007, 3:55-4:4; Ex-1002, ¶256. Aguilar discloses, “Audio adapter 216, keyboard and mouse adapter 220, modem 222, read only memory (ROM) 224, hard disk drive (HDD) 226, CD-ROM drive 230, universal serial bus (USB) ports and other communications ports 232, and PCI/PCIe devices 234 connect to south bridge and I/O controller hub 204 through bus 238 and bus 240.” Ex-1007, 3:55:60.

As explained in Section XII.E.1, a POSITA would have been motivated to combine the teachings of Cho-Gold and Aguilar. Ex-1002, ¶257. To the extent that a POSITA would have desired additional teachings about implementing I/O

devices in Cho, those specific teachings are provided by Aguilar as described above. And a POSITA would have had a reasonable expectation of success in implementing in the combined Cho-Gold system a SouthBridge with I/O devices as described by Aguilar, because Cho already teaches using a SouthBridge. *Id.*; Ex-1005, Fig. 4.

7. Dependent Claim 16: ... an audio generation device.

Cho-Gold and Aguilar disclose Claim 16. Ex-1002, ¶¶258-259. Aguilar discloses that an “audio adapter 216” (orange) connects to a “south bridge and I/O controller hub 204 [yellow] through bus 238 and bus 240” (blue).” Ex-1007, 3:53-60.



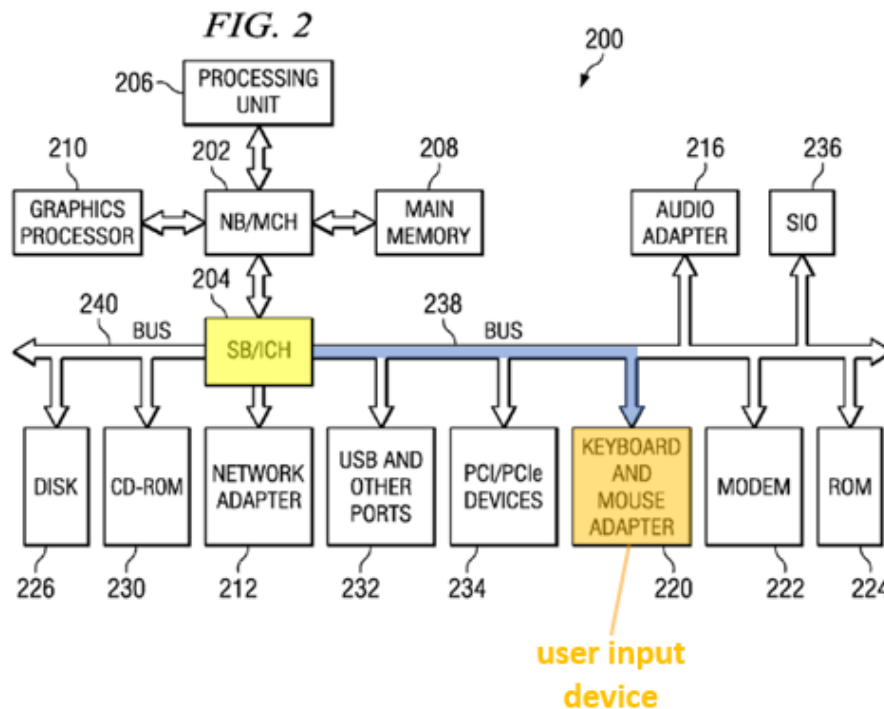
Ex-1007, Fig. 2 (annotated).

8. Dependent Claim 17: ... video rendering device.

Cho-Gold and Aguilar disclose Claim 17. Ex-1002, ¶¶260-261. Aguilar discloses that “[i]nput/output or I/O devices (including, but not limited to ... *displays[]*) can be coupled to the system either directly or through intervening I/O controllers.” Ex-1007, 25:40-43.

9. Dependent Claim 18: ... a user input device.

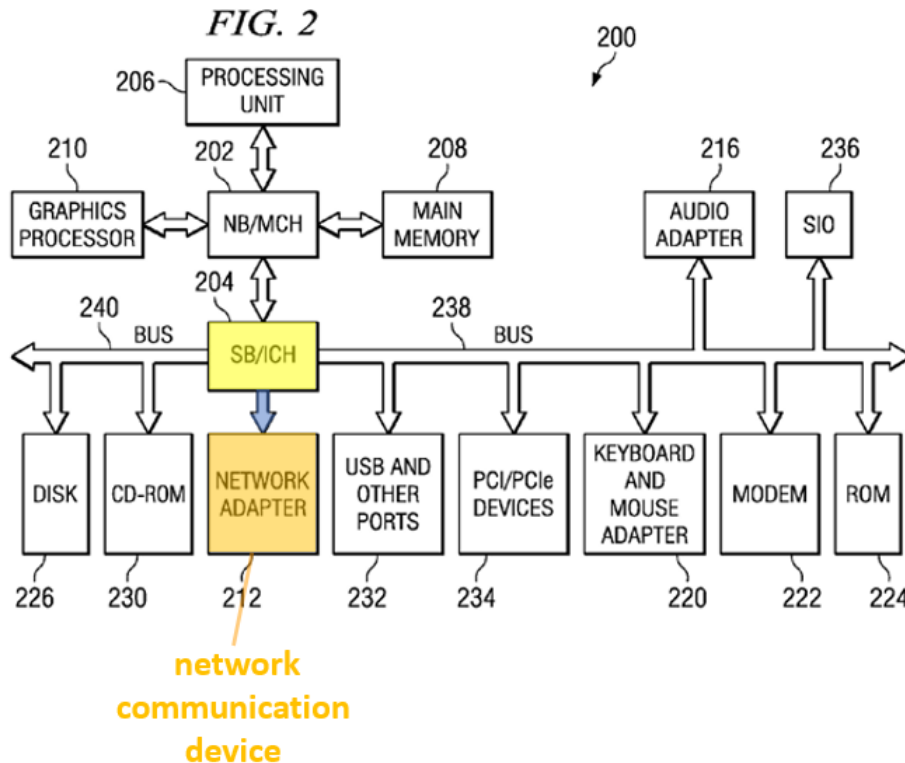
Cho-Gold and Aguilar disclose Claim 18. Ex-1002, ¶¶262-263. Aguilar discloses that a “keyboard and mouse adapter 220” (orange) connect to a “south bridge and I/O controller hub 204 [yellow] through bus 238 and bus 240” (blue). Ex-1007, 3:53-60.



Id., Fig. 2 (annotated).

10. Dependent Claim 19: ... a network communication device

Cho-Gold and Aguilar disclose Claim 19. Ex-1002, ¶¶264-265. Aguilar discloses that a “local area network (LAN) adapter 212” (orange) connect to a “south bridge and I/O controller hub 204 [yellow] through bus 238 and bus 240” (blue). Ex-1007, 3:53-60.



Id., Fig. 2 (annotated).

F. Ground 6: Claims 5-6, and 12-13 are rendered obvious by Cho, Gold, and Shakkarwar.

1. A POSITA would have been motivated to combine Cho, Gold, and Shakkarwar's teachings and would have had a reasonable expectation of success.

In addition to the reasons set forth below, a POSITA would have been motivated to combine the teachings of Cho-Gold and Shakkarwar and would have had a reasonable expectation of success in doing so because each relates to the same well-known technologies. Ex-1002, ¶¶266-269.

Cho-Gold and Shakkarwar relate to and describe similar methods for managing power and optimizing performance within a computer system. Ex-1005, Abstract; Ex-1008, Abstract. Sections XII.D.1 describes Cho and Gold's systems for improving performance within a computer system. Shakkarwar likewise relates to the "efficient use of electronic devices and, more particularly, to systems and methods for power management of electronic devices." Ex-1008, 1:8-10. Shakkarwar discloses "[s]ystems and methods for dynamic power management of electronic devices" so that "power consumption [] may be dynamically managed while providing sufficient bandwidth for the system." Ex-1008, Abstract. Shakkarwar dynamically manages power by monitoring a component's "bandwidth ... for increasing or decreasing communication requirements." *Id.*, 6:41-43. The system then detects "a change in processing condition[s]" for a component, and upon detecting a change, "determines bandwidth 403 for an associated data connection

based on the active components.” *Id.*, 6:63-7:7. The data rate “of a data connection is [then] adjusted” to reach optimal performance levels. *Id.*, 7:26-29. In this manner, “power consumption associated with communicating and processing information via data buses may be optimized while satisfying bandwidth requirements for the computer system.” *Id.*, 3:17-20; *see also id.*, 2:12-15, Cl. 21.

A POSITA would have been motivated to combine the teachings of Cho-Gold and Shakkarwar because they would have recognized a benefit of implementing a look-up table for dynamically managing power, such as taught by Shakkarwar, to optimize performance of components within a processor as taught by Cho. Ex-1002, ¶269. As noted above, Shakkarwar teaches that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while [also] satisfying bandwidth requirements for communicating and/or processing information.” Ex-1008, 2:34-39. Indeed, implementing Shakkarwar’s teachings in the combined Cho-Gold system would have been an obvious implementation detail to achieve the power and bandwidth optimization of Shakkarwar in Cho. Such a benefit would have been achieved in Cho-Gold by, for example, ensuring that Cho’s GPU and interconnect are being driving at compatible frequencies, so as not to generate unnecessary clock cycles and corresponding heat, thus controlling temperature as suggested by Cho. Ex-1002, ¶269.

2. Dependent Claim 5: ... mapping of selectable frequencies ...

Cho-Gold and Shakkarwar teach Claim 5. Ex-1002, ¶¶270-275. As explained above in Section XII.D.4, Cho discloses a second power management circuitry and/or logic. Cho, in view of Shakkarwar teaches that this power management circuitry would have been implemented to include a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect. *Id.*, ¶270.

A POSITA would have been motivated to implement these teachings of Shakkarwar in Cho-Gold for the reasons described above in Section XII.F.1, including because Shakkarwar teaches, for example, that an advantage to its system is that it dynamically “manag[es] power consumption of electronic devices while satisfying bandwidth requirements for communicating and/or processing information.” Ex-1008, 2:34-39. A POSITA would have been motivated to include this advantage in Cho-Gold to improve responsiveness of the system and increase the agility of the system to respond to dynamically changing conditions, including the changing bandwidth requirements of Cho’s components during various activity states. Ex-1002, ¶275.

3. Dependent Claim 6 ... frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency.

Cho-Gold and Shakkarwar disclose Claim 6. Ex-1002, ¶¶276-278. As explained above for Claim 5, Cho and Shakkarwar disclose second power management circuitry that determines bandwidth for an associated data connection based on the other active components by using a look-up table of clock speeds required to process information for specific devices.

A POSITA would have been motivated to implement these teachings of Shakkarwar in Cho-Gold for the reasons described above in Section XII.F.1 and XII.C.3 above. Ex-1002, ¶¶276-278.

4. Dependent Claim 12.

See discussion in Sections XII.D.5 and XII.D.7, regarding Claims 8 and 11. For the reasons described above for Claim 5, Cho-Gold and Shakkarwar disclose Claim 12. Ex-1002, ¶279.

5. Dependent Claim 13.

See discussion in Sections XII.D.5 and XII.F.4, regarding Claims 8 and 12. For the reasons described above for Claim 6, Cho-Gold and Shakkarwar disclose Claim 13. Ex-1002, ¶280.

XIII. THERE IS NO BASIS FOR DISCRETIONARY DENIAL

There is no basis for discretionary denial under §325(d) or §314(a). None of the prior art references asserted in this Petition appear in the file history of the '588 Patent. Nor has any IPR or other post-issuance challenge ever been made against the '588 Patent. Additionally, the only other proceedings relating to the '588 Patent with scheduled hearing dates are in the ITC (the concurrent District court litigations have been statutorily stayed pending the ITC proceedings). Under current USPTO guidance, concurrent ITC proceedings are not a basis to discretionarily deny IPR institution. *See* USPTO Memorandum by Katherine Vidal, June 21, 2022, *Interim Procedure For Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation*, at 5-7.

XIV. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for Claims 1-20 of the '588 Patent based on each of the grounds specified in this Petition.

Dated: February 2, 2023

Respectfully submitted,

/s/ Ben Haber

Ben Haber (Reg. No. 67,129)

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner certifies that this petition includes 13,997 words, as measured by Microsoft Word, exclusive of the table of contents, mandatory notices under § 42.8, certificates of service, word count, and exhibits.

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on February 2, 2023, by filing this document through the Patent Trial and Appeal Board P-TACTS System, as well as delivering a copy via express mail upon the following attorneys of record for the Patent Owner and Petitioner:

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