

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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QUALCOMM INCORPORATED,  
Petitioner,

v.

DAEDALUS PRIME LLC,  
Patent Owner.

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Case No. IPR2023-00547  
U.S. Patent No. 10,705,588

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**PATENT OWNER'S PRELIMINARY RESPONSE  
PURSUANT TO 37 C.F.R. § 42.107(A)**

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| <b>Exhibit</b> | <b>Description</b>                                       |
|----------------|----------------------------------------------------------|
| 2001           | U.S. Pat. No. 8,972,759                                  |
| 2002           | Comparison of Petition to Mudge Declaration              |
| 2003           | Side-by-Side comparison of Petition to Mudge Declaration |
| 2004           | U.S. Pat. No. 9,086,833                                  |

## **I. Introduction**

U.S. Patent No. 10,705,588 (“the ’588 Patent”) simplified how power is managed in computing systems by assigning processor components to separate power domains that can operate at different frequencies so that their power consumption can correlate with need. In the prior art, processors either received a uniform power supply across all components or a set power supply for each component. Whereas, the inventors of the ’588 Patent devised a novel system in which power supply frequency is allocated between domains differently, whereby the power budget is intelligently allocated to components that need processing power, and away from components that do not.

The prior art disclosed by Qualcomm Incorporated (“Petitioner”<sup>1</sup>) fails to disclose or render obvious the power management systems claimed in the ’588 Patent; thus, the Petition should be denied in its entirety.

## **II. Technology Background**

Modern computing devices make use of integrated processors and systems-on-a-chip (“SoCs”) that combine previously-independent circuits within a single

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<sup>1</sup> As filed, the Petition identified Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively “Samsung”) along with Qualcomm Incorporated as Petitioners. However, on June 2, 2023, Patent Owner and Petitioner Samsung jointly moved to terminate as to Samsung. Paper No. 10. On June 27, 2023, The Board granted the motion and terminated the proceedings as to Samsung, and noted that Qualcomm Incorporated would remain as Petitioner. Paper No. 11

package. Ex. 1001, 1:20-26. Processors and SoCs can include multiple different components, such as, for example, processing components, graphics processing components, and interconnects. Different components of a processor or SoC can have different power supply or operational needs, based on, for example, their workloads.

#### **A. Prior Art Failures**

As discussed in the '588 Patent, “suitable mechanisms to ensure that these different units operate at an appropriate frequency are not available” with prior art approaches. Ex. 1001, 1:18-38. Others have also identified a similar problem relating to the need for frequency control but failed to solve this “important,” “challenging,” and “complicated” problem in the manner invented and claimed in the '588 Patent. *See, e.g.*, Ex. 2004 (U.S. Pat. No. 9,086,833), 1:42-56 (“[E]xisting [dynamic clock and voltage scaling (“DCVS”)] solutions for multicore processors require that each processing core include a DCVS module/process and/or adjust the processor’s frequency/voltage independent of other cores. Conventional DCVS solutions exhibit a number of performance problems, and ***implementing an effective DCVS method that correctly scales frequency/voltage for each core of multicore processor system is an important and challenging design criterion.***”) (emphasis added).

### **III. Overview of the '588 Patent**

The '588 Patent describes a multicore processor in which different components can operate at different, independent voltages and/or frequencies. Such components can include individual CPU cores, graphics processing circuitry, and an interconnect. *See, e.g.*, Ex. 1001, 1:57-2:39.

Figure 4 depicts an exemplary embodiment of the invention of the '588 Patent. For example, Figure 4 illustrates a multicore processor 400 that may include multiple cores 410a through 410n. *See, e.g.*, Ex. 1001, 6:11-16. Figure 4 also illustrates that processor 400 may include graphics engine 420 and interconnect 430. *See, e.g.*, Ex. 1001, 6:16-17, 6:37-41. In addition, Figure 4 shows that processor 400 can include power control unit 455 and frequency control logic 459 to dynamically update the frequency of interconnect 430 based on a frequency of the graphics engine 420. *See, e.g.*, Ex. 1001, 6:47-63.

### **IV. The Petition**

The Petition relies extensively on the mere *ipse dixit* of the Mudge Declaration, and in doing so fails as a matter of law. For example, the Petition does not assert that any claim is anticipated, and instead relies on the Mudge Declaration to support otherwise largely unsubstantiated claims regarding what a “POSITA would have understood” and alleged motivations to combine references. *See, e.g.*, Pet., p. 23 (asserting what a “POSITA would have understood” by citation only to

the Mudge Decl.), 25 (same), 28 (same), 32 (same), 36 (same), 40 (same), 45 (same), 46 (same), 51 (same), 52 (same), 54 (same), 57 (same), 69 (same), 75 (same), 77 (same), 91 (same), 92 (same); *see also id.* at 76 (“a POSITA would have recognized”). In fact, where the Petition exclusively cites to the Mudge Declaration as support for what a POSITA would have allegedly understood, the cited paragraphs in the Mudge Declaration often provide no substantiation. For example, on page 45, the Petition asserts that “[a] A POSITA would have understood that these references disclose interrelated teachings based on routine technologies,” and cites to “Ex-1002 ¶142,” which merely makes the same *verbatim* unsubstantiated claim. *See* Ex. 1002, ¶142. The same is true for the Petition’s assertions on page 51 (citing to Ex. 1002 at ¶153), 57 (citing to Ex. 1002 at ¶163), 91 (citing to Ex. 1002 at ¶244) for example.

Reliance on unsubstantiated expert declarations is insufficient to support a finding of obviousness as a matter of law, and has been routinely rejected by the Board. 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight”); *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper No. 12 (Feb. 10, 2023) (Director Review affirming “little weight to Petitioner’s expert because the expert declaration merely offered conclusory assertions without underlying factual support and repeated, *verbatim*, Petitioner’s conclusory arguments.”); *see also TQ Delta, LLC v.*

*Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019)(“This court’s opinions have repeatedly recognized that conclusory expert testimony is inadequate to support an obviousness determination on substantial evidence review”).

Moreover, the Mudge Declaration fails to provide any probative value to the analysis, as it “does not provide any technical detail, explanation, or statements supporting why the expert determines that the feature in question was required or would have been obvious based on the prior art disclosure,” and merely “sets forth Petitioner’s conclusory assertions as though they are facts, rather than setting forth facts and evidence in support of Petitioner’s assertions.” IPR2022-00624, Paper No. 12. For example, Ex. 2002 is a comparison of the Mudge Declaration to the Petition, and shows the insignificant additions (in underlining) made between them.<sup>2</sup> The only substantive contribution made by the Mudge Declaration is the addition of the “Technology Background” section. *See* Ex. 2002 (Mudge Comparison), pp.25-33; *see also* Ex. 1002, pp.25-33. Where an expert’s declaration is merely used as a mouthpiece for a Petitioner’s attorney argument, it is entitled to no weight and cannot support a finding of obviousness.

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<sup>2</sup> Ex. 2002 shows the differences between the two, formatted as additions made to the Mudge Declaration. Ex. 2003 shows a full, side-by-side comparison of the Petition to the Mudge Declaration.

### A. Overview of Machnicki

U.S. Patent No. 8,468,373 to Machnicki et al. (“Machnicki”) is directed to a process for “coordinating performance parameters in multiple domains.” Ex. 1006, Abstract. The methods described in Machnicki are designed to allow “different portions of integrated circuit 100 [to] alternate between their various different states with a single command or register write,” such that “actual underlying hardware changes are made in parallel” and avoiding situations where “the requesting software ... need[s] to program each clock generator individually and/or understand how each generator is configured.” Ex. 1006, 8:32-36. Said another way, Machnicki is directed to the goal of simplifying the process of changing the performance levels of various domains through a mechanism that allows software to change all of the domains in parallel with a single command, rather than requiring the different domains to be independently adjusted or controlled.

The mechanism that Machnicki proposes is a performance state table such as the following:

| TABLE I |                    |                    |     |                    |
|---------|--------------------|--------------------|-----|--------------------|
|         | Domain 1           | Domain 2           | ... | Domain m           |
| state 1 | $f_{1,1}; V_{1,1}$ | $f_{2,1}; V_{2,1}$ | ... | $f_{m,1}; V_{m,1}$ |
| state 2 | $f_{1,2}; V_{1,2}$ | $f_{2,2}; V_{2,2}$ | ... | $f_{m,2}; V_{m,2}$ |
| state 3 | $f_{1,3}; V_{1,3}$ | $f_{2,3}; V_{2,3}$ | ... | $f_{m,3}; V_{m,3}$ |
| ...     | ...                | ...                | ... | ...                |
| state n | $f_{1,n}; V_{1,n}$ | $f_{2,n}; V_{2,n}$ | ... | $f_{m,n}; V_{m,n}$ |

Ex. 1006, 8:10-17.

The performance state table defines, for each programmable performance state, voltages and frequencies that should be used to configure each performance domain together. Ex. 1006, 8:1-7. For example, for state 1, Domain 1 will be set to a frequency of  $f_{1,1}$  and a voltage of  $V_{1,1}$ ; for the same state, Domain 2 will also be set to a frequency  $f_{2,1}$  and a voltage of  $V_{2,1}$ . Frequency and voltages for each domain will be defined up to a Domain  $m$ , and will also be set to a frequency  $f_{m,1}$  and a voltage  $V_{m,1}$ . *See also* Ex. 1006, 8:1-7, 18-22. A similar array is defined for each performance state, up to a state  $n$ . *See* Ex. 1006, 8:1-7, 18-22. “[I]f the software desires to set the frequencies ( $f$ ) and/or voltages ( $V$ ) for each domain in integrated circuit 100 ... the software may write a pointer to the corresponding entry (1 to  $n$ ) in the performance state table to configuration register 150 of PMU 140.” Ex. 1006, 8:18-22. This allows “different portions of integrated circuit 100 [to be] alternate[d] between their various different states with a single command or register write.” Ex. 1006, 8:28-30. In other words, based on the following integrated circuit architecture disclosed in Machnicki, the performance table would define, for each state 1- $n$ , a frequency and voltage pair for each of Processor 160A, Processor 160F, Graphics 160B, Memory Control 160E, and other domains, for each state:

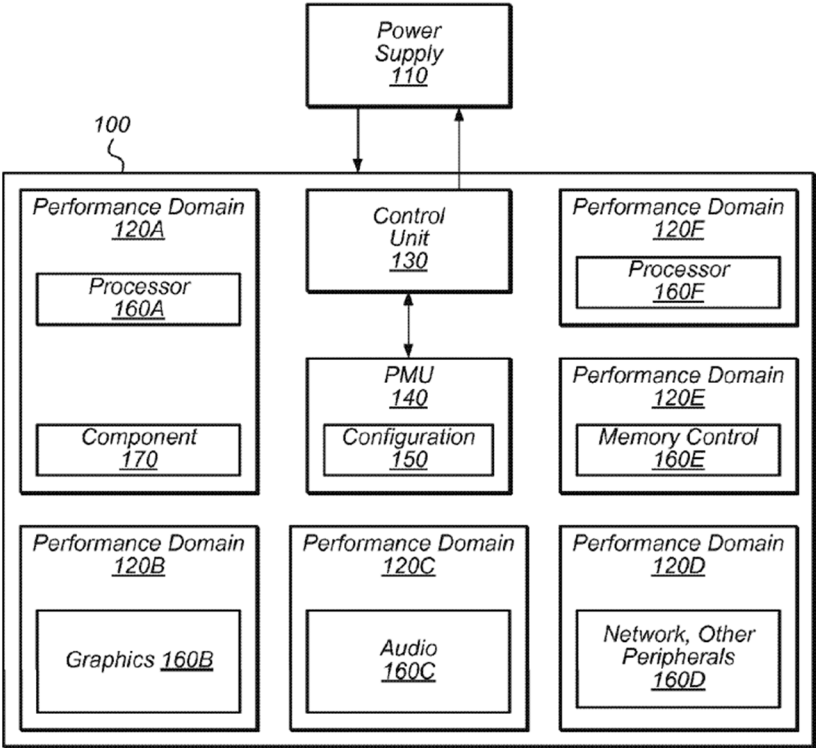


FIG. 1

Ex. 1006, FIG. 1.

The performance state table would look similar to the following:

|                | 160A                     | 160F                     | 160B                     | 160E                     | ... |
|----------------|--------------------------|--------------------------|--------------------------|--------------------------|-----|
| <b>state 1</b> | $F_{1,160A}, V_{1,160A}$ | $F_{1,160F}, V_{1,160F}$ | $F_{1,160B}, V_{1,160B}$ | $F_{1,160E}, V_{1,160E}$ | ... |
| <b>state 2</b> | $F_{2,160A}, V_{2,160A}$ | $F_{2,160F}, V_{2,160F}$ | $F_{2,160B}, V_{2,160B}$ | $F_{2,160E}, V_{2,160E}$ | ... |
| ...            | ...                      | ...                      | ...                      | ...                      | ... |
| <b>state N</b> | $F_{N,160A}, V_{N,160A}$ | $F_{N,160F}, V_{N,160F}$ | $F_{N,160B}, V_{N,160B}$ | $F_{N,160E}, V_{N,160E}$ | ... |

When the software wants to change the performance state of the integrated circuit to state 2, the software would write a pointer to the state 2 row in the performance state table in the configuration register of the PMU. *See, e.g.*, Ex. 1006, 8:20-22. This would cause the frequency and voltage of each of the domains (such as the Processor 160A domain, Processor 160F domain, the Graphics 160B domain, and the Memory Control 160E domain) to all be adjusted to the frequency and voltage defined for that domain within state 2 as a single set :

|                | <b>160A</b>              | <b>160F</b>              | <b>160B</b>              | <b>160E</b>              | <b>...</b> |
|----------------|--------------------------|--------------------------|--------------------------|--------------------------|------------|
| <b>state 2</b> | $F_{2,160A}, V_{2,160A}$ | $F_{2,160F}, V_{2,160F}$ | $F_{2,160B}, V_{2,160B}$ | $F_{2,160E}, V_{2,160E}$ | <b>...</b> |

*See also* Ex. 1006, 9:4-20. Each of the domains will be configured to run at their specified frequency and voltage for state 2 by separately adjusting the clocks and other hardware of the integrated circuit for each domain. *See* Ex. 1006, 9:55-10:7.

## **B. Overview of Cho**

U.S. Patent Application Publication No. 2010/0073068 to Cho et al. (“Cho”) is directed to an integrated circuit containing a temperature control unit coupled to each of a plurality of functional units. Ex. 1005, Abstract. As Cho describes, the temperature control unit is configured to, if the temperature exceeds a first threshold value for a particular one of the plurality of functional units, perform a first temperature control action on the particular one of the plurality of functional units. Ex. 1005, Abstract.

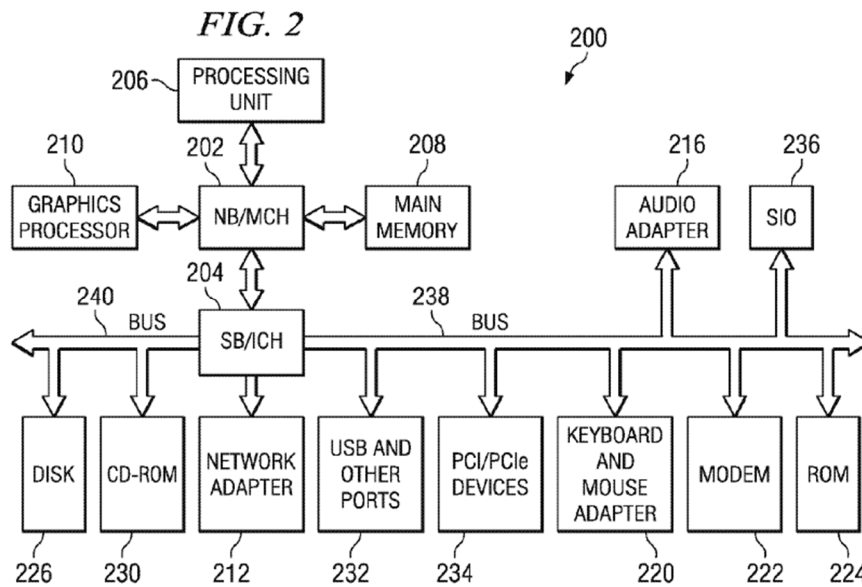
**C. Overview of Gold**

U.S. Patent Application Publication No. 2009/0235108 to Gold et al. (“Gold”) is directed to processor overclocking techniques. Ex. 1009, Abstract. For example, as Gold describes, upon automatically determining that overclocking entry criteria are satisfied, one or more cores are clocked above their standard operation frequencies, until one or more exit criteria are satisfied. Ex. 1009, Abstract.

**D. Overview of Aguilar**

U.S. Patent No. 7,552,346 to Aguilar, Jr. et al. (“Aguilar”) describes “optimizing thermal performance of a computer system.” Ex. 1007, Abstract. For example, Aguilar describes that “[a] set of system resources associated with the computer system are identified and a thermal index is requested for each of the set of system resources to form a set of thermal indexes. An action is identified from a set of actions to reduce resource utilization and the action is implemented to reduce a thermal state of the computer system.” Ex. 1007, 1:51-59. As one example, “[i]f, for any reason, the temperature continues to rise and reaches a temperature at or above the full throttle point, the PowerPC process element or synergistic processor element is stopped until the temperature drops below the full throttle point.” Ex. 1007, 10:24-28.

Figure 2 of Aguilar depicts a data processing system including a north bridge (also known as a memory controller hub (“MCH”)) and a south bridge (also known as an input/output (“I/O”) controller hub (“ICH”)):



Ex. 1007, FIG. 2; *see also* Ex. 1007, 3:44-47. “A memory may be, for example, main memory 208, read only memory 224, or a cache such as found in north bridge and memory controller hub 202 in FIG. 2.” Ex. 1007, 4:57-60.

### **E. Overview of Shakkarwar**

U.S. Patent No. 7,392,411 to Shakkarwar (“Shakkarwar”) is directed to a software-based process for determining an ideal bandwidth for a bus, for example, based on analysis of software being executed by a processor, or based on detecting that certain components connected to the bus are idle or otherwise unused. *See, e.g.*, Ex. 1008, 5:53-7:26. Shakkarwar’s goal is “reduced power consumption attributed

to operating a communication bus and/or one or more electronic components and/or electronic devices at lower clock speed(s) and voltage level(s) based on required bandwidth for processing information ... with minimal effect on overall processing bandwidth.” Ex. 1008, 8:50-56. Thus, Shakkarwar is concerned solely with adjusting bus data rates, and not the frequencies of the components using the bus.

For example, when the system disclosed in Shakkarwar detects that no software applications are using a GPU, the system can decide to reduce the data rate (*i.e.*, reduce the bandwidth) over the bus to save power. *See* Ex. 1008, 6:8-16. Similarly, when the system detects than an application was opened that is likely to require the GPU, the system will increase the data rate between the data controller and the graphics controller to support the functionality of the application, but does not disclose or suggest any changes to the data controller or graphics controller components. *See* Ex. 1008, 6:49-58. Rather, Shakkarwar aims to determine when reducing the data rate of a bus can result in power savings “without sacrificing performance or powering down electronic devices, processors, components, etc.” *See* Ex. 1008, 4:14-18. Shakkarwar determines a frequency to change the bus to by using “a look-up table [that] may include a list of clock speeds ... required to process information for specific devices and/or groups of devices.” Ex. 1008, 7:7-10. Said another way, the bus may have an associated table identifying which clock speed the

bus should operate at based on the device or group of devices the system believes will not be negatively affected if the bus data rate is reduced.

## **V. Ground 1 Fails**

The Petition asserts in Ground 1 that Claims 1-2, 4, 8-9, 11, 15-19, and 20 are rendered obvious by Machnicki.

### **A. Machnicki does disclose or suggest Claim 1(b) and 1(c)**

Machnicki does not disclose or suggest at least “a second core operable at a second voltage *independent* of the first voltage,” as claimed. For example, Machnicki is directed to a process by which *all* domains are adjusted to predefined frequencies and voltages whenever the integrated circuit (“IC”) changes performance states. *See, e.g.*, Ex. 1006, 8:1-10:7. Thus, whenever the IC performance state changes to adjust the voltage of Processor 160A (allegedly the claimed “first core”) the voltage of Processor 160F (allegedly the claimed “second core”) and Graphics 160B are each always also adjusted. The Processor 160F and Graphics 160B voltages are adjusted to specific values defined for that performance state. *See also* Ex. 1006, 10:46-52. The voltage of Processor 160A and the voltage of Processor 160F are always controlled by the same mechanism (*i.e.*, the singular performance state) and are always configured to switch to specific voltages at the same time, in response to the same event (*i.e.*, a change in the performance state). Because the performance state change causes the voltages of all three components

to adjust simultaneously, the performance domains of Machnicki do not render obvious “a second voltage *independent* of the first voltage,” as required.

Similarly, because Machnicki’s Graphics 160B (allegedly the claimed “graphics processing circuitry”) is also a performance domain, controlled with the same performance state table, Machnicki does not disclose or suggest “graphics processing circuitry independently operable at a third frequency,” as recited in independent claim 1.

**B. Machnicki does not render obvious Claim 1(d)**

Machnicki does not render obvious at least “an interconnect to couple the graphics processing circuitry to a memory device” as claimed. Petitioner maps an undisclosed bus within<sup>3</sup> Machnicki’s Memory Control 160E with the claimed “interconnect” by inferring that Memory Control 160E not only contains such an internal bus, but also that the undisclosed bus connects the components in the claimed manner. Petitioner’s inferences are rooted in impermissible hindsight—Petitioner takes a generic disclosure from Column 4 of Machnicki, and merely asserts without explanation that it applies to the Memory Control described in

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<sup>3</sup> To the extent Petitioner maps the Memory Control 160E itself (e.g., as opposed to the alleged undisclosed bus) with the claimed “interconnect,” the Petition fails. The ’588 Patent explicitly distinguishes between a “memory controller” and an “interconnect” as different “domains” within the processor. See Ex. 1001, 1:62-63, 2:3-6, 5:44-50, 6:37-40, 7:20-23, Fig 3 and Fig 4.

Column 7 of Machnicki. Petitioner’s attempts to combine the single sentence having a generic reference to a “bus and/or interface” with descriptions of other, separate, components without alleging a motivation to combine or modify fail as a matter of law. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 405 (“A patent composed of several elements is not proved obvious merely by demonstrating that each element was, independently, known in the prior art.”).

Petitioner then goes further afield of the actual disclosure and asserts that Machnicki’s alleged (undisclosed) Memory Control internal bus makes the requisite connections. Pet., 29. However, Machnicki’s only description of an interconnect does not disclose or suggest that it is “to couple the graphics processing circuitry to a memory device” as required:

Components within integrated circuit 100 may be coupled to each other using any suitable bus and/or interface mechanism. PMU 140 and control unit 130 may also be coupled to

Ex. 1006, 4:31-33. Nor does Petitioner explain the unsupported assertion that it uses to support the imagined connections, i.e., that “memory control circuit 160E sits between each component within the integrated circuit and memory.” Pet., 29. To the extent Petitioner is referring to FIG. 1, Machnicki neither illustrates any connections, nor does it imply a real physical layout of the components: rather, as Machnicki states, “FIG. 1 is a **block diagram**.” Ex. 1006, 3:9. .

Machnicki also does not render obvious “the interconnect operable at a fourth frequency different from the first, second, and third frequencies” as claimed. Petitioner asserts that Machnicki’s *Memory Control 160E* is within a separate performance domain, but fails to demonstrate that the alleged (undisclosed) *bus* within the Memory Control 160E (allegedly the claimed “interconnect”) would operate at a frequency different from the other components.

**C. Machnicki does not render obvious claims 2 or 4**

Claims 2 and 4 depend from non-obvious claim 1, and therefore are nonobvious as well.

**D. Machnicki does not render obvious Claim 8(c)-8(e)**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 1. Thus, for the same reasons discussed above with respect to claim 1, Machnicki does not render obvious claim 8.

**E. Machnicki does not render obvious Claims 9, 11, 15-19**

Claims 9, 11, and 15-19 depend from non-obvious claim 8 and are therefore non-obvious as well.

**F. Machnicki does not render obvious Claim 20**

Petitioner does not assert that this claim is rendered obvious for any reasons other than those articulated for the allegedly similar Claim 1. Thus, for the same

reasons discussed above with respect to claim 1, Machnicki does not render obvious claim 20.

## **VI. Ground 2 Fails**

The Petition asserts in Ground 2 that Claims 3, 7, 10, and 14 are rendered obvious by Machnicki and Aguilar.

### **A. Machnicki would not have been combined with Aguilar**

Petitioner has not demonstrated that a person of ordinary skill in the art would have been motivated to combine Machnicki with Aguilar. *See* Pet., pp. 44-45.

A person of ordinary skill in the art (“POSITA”) would not look nor be motivated to combine Machnicki and Aguilar, as they relate to solving different problems in different types of systems. Machnicki is directed towards modifying the performance of a single System-on-a-Chip (SoC) by coordinating parameter settings, *e.g.*, clock frequencies and/or voltages, for multiple domains defined as a state based on a state change request. *See* Ex. 1006, 1:10-63. These states are used to have the device deliver the performance needed with the least amount of power. Ex. 1006, 5:39-61. Aguilar, conversely, is directed towards the general process of thermal throttling, which involves reducing the temperature of a chip or system when it is too hot by pausing the processing (*e.g.*, by stopping the clock) within the elements that are the primary source(s) of heat within the device and/or system. Ex. 1007, 1:32-46.

Other than conclusory statements based on hindsight, Petitioner fails to articulate any reason why a POSITA would seek to modify the hardware configuration taught in Machnicki to include the specific hardware of Aguilar. For example, Petitioner’s alleged motivation relies on unsupported and unexplained assertions that “a POSITA ... would have recognized the benefit,” and that “a POSITA would have known that ... the computer system could be improved,” but neither the Petition nor the Mudge Declaration explains how or why. The Petition thus is a prime example of hindsight—alleging that if confronted with the combination, a POSITA would have recognized a benefit, but not demonstrating that there was a motivation to have combined them in the first place. As the Federal Circuit has held, where an “expert’s testimony on obviousness was essentially a conclusory statement that a person of ordinary skill in the art would have known, based on the ‘modular’ nature of the claimed components, how to combine” the references, “[t]his is not sufficient and is fraught with hindsight bias.” *ActiveVideo Networks, Inc. v. Verizon Communs., Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012).

For example, Petitioner does not allege that Aguilar provides a solution to a problem identified in Machnicki. Nor does Petitioner allege the proposed combination represent a substitution of any known elements from Aguilar for an element in Machnicki. Nor does Petitioner allege the proposed combination is the

use of a technique disclosed in Aguilar to improve Machnicki. Nor does Petitioner identify any market or other factors creating incentive for a variation of Machnicki.

A POSITA also would not have been motivated to combine Machnicki with Aguilar at least because Machnicki already teaches a method of thermal throttling (*i.e.*, managing the performance state settings so as to avoid an undesired thermal event). For example, in Machnicki, even if a thermal event were to occur, this would simply trigger a state change request to a state with appropriate parameters to counteract the thermal event. Thus, a POSITA would need to look no further than Machnicki itself for a mechanism for thermal throttling.

Petitioner also has not demonstrated that there would be a reasonable expectation of success in combining Machnicki with Aguilar. For example, Machnicki is directed to an SoC where multiple components are contained on a single chip, whereas Aguilar is directed to a system including multiple discrete integrated circuit (“IC”) packages. *See* Ex. 1006, FIG. 1, 4:8-42; Ex. 1007, FIG. 2, 3:44-4:4. As the ’588 Patent explains, for example, when operating within a single SOC there are different bandwidth and other concerns within than in systems comprised of “independent integrated circuits”; these differences require different approaches to power management on an SoC versus a system with discrete ICs. *See, e.g.*, Ex. 1001, 1:18-38; 1:57-3:40. These differences also require different considerations in hardware design; as one example, wiring and bus width constraints

are considerably less, and the speed of interconnects much greater, within an SoC. Petitioner has not explained how a POSITA would allegedly move a discrete IC package as taught in Aguilar, onto an SoC as taught in Machnicki. For example, neither the Petition nor the Mudge declaration addresses the analysis, simulations (experiments), and architectural work that would be needed to determine the configuration of a memory controller within a SoC as would be required under Petitioner's proposed combinations.

Petitioner has also failed to demonstrate that, even if these two references were combined, they would have been combined in the specific way so as to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (requiring “a reason that would have prompted a [POSITA] to combine the elements ***in the way the claimed new invention does***”); *ActiveVideo Networks, Inc. v. Verizon Comms., Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012) (citing *KSR* with same emphasis). Such explanation of the alleged motivation to combine references is particularly important because the primary teaching of Machnicki lies in its *software* configuration, whereas the alleged combination requires a particular *hardware* configuration. Petitioner also fails to articulate why a POSITA would have any reason to look to Aguilar specifically to modify the hardware architecture of the integrated circuit disclosed in Machnicki. For example, the example architecture in

Aguilar is neither the focus nor the primary teaching of Aguilar; the thermal throttling algorithm is.

Petitioner also does not explain how or why, in combining Machnicki with Aguilar, the other teachings of Machnicki would have been unchanged so as to not affect the features allegedly rendering obvious the claims from which the challenged claims of Ground 2 depend.

**B. Machnicki in view of Aguilar does not render obvious Claim 3**

Claim 3 is nonobvious at least because it depends from nonobvious claim 2.

Machnicki in view of Aguilar does not render obvious at least “a non-core power domain comprising a cache shared by the plurality of cores” as claimed. For example, Petitioner merely asserts that “[a] POSITA would have understood that Machnicki’s memory control 160E contained a cache,” but has not demonstrated that the alleged cache would be included in a non-core power domain and further be shared by the plurality of cores. For example, although petitioner asserts that Machnicki states “configuration parameters may be component specific,” and may depend on “cache sizes in various caches,” this does not demonstrate that the memory controller 160E includes a cache that is “shared by the plurality of cores” as required under Petitioner’s reading. Petitioner alleges that because memory controller 160E is allegedly shared by the cores, a cache within it would be as well, but does not explain why that would be the case. Indeed, such a configuration

conflicts with Petitioner’s own assertion that the configuration parameters would be component specific—if the components connected to memory controller 160E all shared a cache, they would not be component specific as they allegedly “depend on ‘cache sizes.’” Pet., p.46.

**C. Machnicki in view of Aguilar does not render obvious Claim 7**

Claim 7 is nonobvious at least because it depends from nonobvious claim 3.

**D. Machnicki in view of Aguilar does not render obvious Claim 10**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 3. Thus, for the same reasons discussed above with respect to claim 3, Machnicki in view of Aguilar does not render obvious claim 10.

**E. Machnicki in view of Aguilar does not render obvious Claim 14**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 7. Thus, for the same reasons discussed above with respect to claim 7, Machnicki in view of Aguilar does not render obvious claim 14.

**VII. Ground 3 Fails**

The Petition asserts in Ground 3 that Claims 5-6 and 12-13 are rendered obvious by Machnicki and Shakkarwar.

**A. Machnicki would not have been combined with Shakkarwar**

Petitioner has not demonstrated that a person of ordinary skill in the art would have been motivated to combine Machnicki with Shakkarwar. *See* Pet., pp. 49-51.

Petitioner also has not demonstrated that there would be a reasonable expectation of success in combining Machnicki with Shakkarwar at least because Machnicki is directed to an SoC, whereas Shakkarwar is directed to a system that includes discrete components. As in Ground 2, Petitioner has failed to explain how a POSITA would have allegedly combined the features from a discrete-component reference into an SoC without experimentation or implementation considerations.

Other than conclusory statements based on hindsight, Petitioner fails to articulate any reason why a POSITA would seek to modify Machnicki to include the aspects of Shakkarwar. For example, Petitioner's alleged motivation relies on unsupported and unexplained assertions that "a POSITA ... would have recognized the benefit," but neither the Petition nor the Mudge Declaration explains how or why. The Petition thus is a prime example of hindsight—alleging that if confronted the combination, a POSITA would have recognized a benefit, but not demonstrating that there was a motivation to have combined them in the first place. For example, Petitioner does not allege that Shakkarwar provides a solution to a problem identified in Machnicki. Nor does Petitioner allege the proposed combination represents a substitution of any known elements from Shakkarwar for an element in Machnicki.

Nor does Petitioner allege the proposed combination is the use of a technique disclosed in Shakkarwar to improve Machnicki. Nor does Petitioner identify any market or other factors creating incentive for a variation of Machnicki.

Petitioner has also failed to demonstrate that, even if these two references were combined, they would have been combined in the specific way so as to arrive at the claimed invention. *See KSR* (requiring “a reason that would have prompted a [POSITA] to combine the elements ***in the way the claimed new invention does***”); *ActiveVideo* (citing *KSR* with same emphasis). For example, Petitioner merely states that Shakkarwar teaches certain concepts, and makes a conclusory statement that a POSITA would have been motivated to combine these concepts with the disclosure in Machnicki. Petitioner also fails to articulate why a POSITA would have any reason to look to Shakkarwar specifically to modify Machnicki.

Petitioner also does not explain how or why, in combining Machnicki with Shakkarwar, the other teachings of Machnicki would have been unchanged so as to not affect the features allegedly rendering obvious the claims from which the challenged claims of Ground 3 depend.

**B. Machnicki in view of Shakkarwar does not render obvious Claim 5**

Shakkarwar does not disclose or suggest mapping or associating selectable frequencies of a GPU with selectable frequencies of a bus, as recited in dependent

claim 5. For example, Shakkarwar does not associate particular GPU frequencies with particular bus frequencies. Instead, Petitioner merely alleges that Shakkarwar monitors “bandwidth for a component” (not the frequency), and maps a clock speed for the bus to a *type* of device connected to the bus. That is in contrast to the claim, which requires “mapping of selectable *frequencies of the* graphics processing circuitry.” *See, e.g.*, Ex. 1008, at 7:7-10.

Additionally, Petitioner alleges that Shakkarwar detects “a change in processing condition[s],” and as a result utilizes the lookup tables. However, the changed processing conditions Shakkarwar detects are not the *frequency* of the components, but rather the anticipated data needs of software. *See* Ex. 1008, 6:8-16. Shakkarwar does not, for example, associate particular GPU frequencies with particular bus frequencies; nor does Shakkarwar disclose or suggest the concept of mapping a plurality of selectable frequencies of a GPU to the selectable frequencies of an interconnect, as required by claim 5. Therefore, Petitioner has not shown that Shakkarwar maps the frequency of the components (let alone the graphics processing circuitry) to the frequency of the interconnect.

**C. Machnicki in view of Shakkarwar does not render obvious Claim 6**

Claim 6 is nonobvious at least because it depends from nonobvious claim 5.

Machnicki in view of Shakkarwar does not disclose or suggest “logic is to select the fourth frequency for the interconnect based on detecting operation of the graphics processing circuitry at the third frequency” as recited. For example, Petitioner asserts that Shakkarwar discloses that “system software can determine if the bus rate between the data controller and the graphics controller is high enough,” but does not allege that Shakkarwar discloses setting a fourth frequency based on the graphics processing circuitry being at a third frequency as claimed. For example, Shakkarwar (and Petitioner’s allegations regarding the same) merely discuss determining if the bandwidth is high enough for processing needs, not if the frequency is higher such that a fourth frequency would be set based on it.

**D. Machnicki in view of Shakkarwar does not render obvious Claim 12**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 5. Thus, for the same reasons discussed above with respect to claim 5, Machnicki in view of Aguilar does not render obvious claim 12.

**E. Machnicki in view of Shakkarwar does not render obvious Claim 13**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 6. Thus, for

the same reasons discussed above with respect to claim 6, Machnicki in view of Aguilar does not render obvious claim 13.

### **VIII. Ground 4 Fails**

The Petition asserts in Ground 4 that 1-2, 4, 8-9, 11, and 20 are rendered obvious by Cho and Gold.

#### **A. Cho would not have been combined with Gold**

Petitioner has not demonstrated that a person of ordinary skill in the art would have been motivated to combine Cho with Gold. *See* Pet., pp. 58-64.

Petitioner alleges that a POSITA would have had a motivation to combine Cho with Gold because they share an inventor and assignee, and “each reference teaches the same direct relationship between temperature and frequency; namely a lower operating frequency will result in a lower operating temperature.” Pet., 58. However, Petitioner does not explain how or why sharing a single inventor or assignee is relevant to the motivation (or lack thereof) of a POSITA, or why the mere restatement of a cardinal understanding in the field would provide such a motivation. For example, the relationship between frequency and temperature is well known. *See* Ex. 2001 (US 8,972,759), 1:37-47. Simply stating the obvious does not provide any reason, motivation, or justification for combining references; otherwise all references in the same field would automatically have a motivation to combine, mooting the analysis entirely.

Petitioner goes on to allege that Cho and Gold teach operating at different temperatures and different frequencies respectively, and that “a POSITA would have thus recognized ... [Cho and Gold] would be especially compatible.” *See* Pet., 59-62. However, this relates to the likelihood of success analysis, not the motivation to combine. Merely being allegedly compatible for a combination does not motivate the combination.

Petitioner alleges that a POSITA would have been motivated to “more particularly control the operating temperature of each component,” but does not explain how the combination accomplishes that goal, or why the goal motivates combining the references together. Petitioner does not allege that Gold provides a solution to a problem identified in Cho. Nor does the proposed combination represent a substitution of any known elements from Gold for an element in Cho. Nor is the proposed combination the use of a technique disclosed in Gold to improve Cho. Nor does Petitioner identify any market or other factors creating incentive for a variation of Cho.

Petitioner has also failed to demonstrate that, even if these two references were combined, they would have been combined in the specific way so as to arrive at the claimed invention. *See KSR* (requiring “a reason that would have prompted a [POSITA] to combine the elements ***in the way the claimed new invention does***”); *ActiveVideo* (citing *KSR* with same emphasis). For example, Petitioner merely states

that Gold teaches certain concepts, and makes a conclusory statement that a POSITA would have been motivated to combine these concepts with the disclosure in Cho. Petitioner also fails to articulate why a POSITA would have any reason to look to Gold specifically to modify Cho.

Petitioner also does not explain how or why, in combining Cho with Gold, the other teachings of Cho would have been unchanged so as to not affect the features allegedly rendering obvious the claims from which the challenged claims of Ground 5 depend.

**B. Cho in view of Gold does not render obvious Claim 1[b]**

Cho in view of Gold does not disclose or suggest at least “operable... at a second frequency different from the first frequency” as claimed. For example, as Petitioner recognizes, Cho does not disclose different components operating at different frequencies, but rather only at different *temperatures*. Whereas Cho discloses that the *voltages* can be different, including because it states that “the voltages on the voltage planes for each of the functional units can be set independently of one another,” Cho does not contain the same disclosure with respect to *frequency*. Ex. 1005, [0021]. As was well-known in the art, temperature of a processing component is affected by voltage. Therefore, the disclosure of different voltages, without the need for different frequencies, explains the operation at the different temperature values that Cho discusses. Petitioner does not allege that

Cho actually discloses operating at different frequencies, and instead relies on a combination with Gold for such alleged disclosures. However, for the reasons set forth above, Cho would not have been combined with Gold, and Petitioner has not demonstrated that there would have been a motivation to combine them.

**C. Cho in view of Gold does not render obvious Claim 1[c] and 1[d]**

Cho in view of Gold does not disclose or suggest “a third frequency different from the first frequency and the second frequency,” or “a fourth frequency different from the first, second, and third frequencies” as recited in claim elements 1[c] and 1[d] for the same reasons discussed above with respect to claim element 1[b].

**D. Cho in view of Gold does not render obvious Claims 2, 4**

Claims 2 and 4 are nonobvious at least because each depends from nonobvious claim 1.

**E. Cho in view of Gold does not render obvious Claim 8**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 1. Thus, for the same reasons discussed above with respect to claim 1, Cho in view of Gold does not render obvious claim 8.

**F. Cho in view of Gold does not render obvious Claims 9, 11**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claims 2 and 4

respectively. Thus, for the same reasons discussed above with respect to claim 2 and 4, Cho in view of Gold does not render obvious claims 9 or 11.

**G. Cho in view of Gold does not render obvious Claim 20**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated for the allegedly similar limitations in Claim 1. Thus, for the same reasons discussed above with respect to claim 1, Cho in view of Gold does not render obvious claim 8.

**IX. Ground 5 Fails**

The Petition asserts in Ground 5 that Claims 3, 7, 10, and 14-19 are rendered obvious by Cho, Gold, and Aguilar.

**A. Cho would not have been combined with Gold and Aguilar**

Petitioner has not demonstrated that a person of ordinary skill in the art would have been motivated to combine Cho with Gold and Aguilar. *See* Pet., pp. 87-91. For example, Cho would not have been combined with Gold for at least the reasons set forth above with respect to Ground 4. Additionally, Cho and Gold would not have further been combined with Aguilar.

For example, Petitioner asserts that Cho would be combined with Gold and Aguilar because each relates to thermal management and has a NorthBridge-SouthBridge architecture, but does not explain how or why such basic things from the art provide a motivation to combine. Pet., pp. 88-90. To the extent such

similarities are relevant, they are relevant to the likelihood of success, not to the motivation to combine analysis. Otherwise, all references having the dominant architecture in the field would automatically have a motivation to combine, thereby mooting the analysis. As the Federal Circuit has held, where an “expert’s testimony on obviousness was essentially a conclusory statement that a person of ordinary skill in the art would have known, based on the ‘modular’ nature of the claimed components, how to combine” the references, “[t]his is not sufficient and is fraught with hindsight bias.” *ActiveVideo Networks, Inc. v. Verizon Communs., Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012).

Petitioner does not allege that Gold or Aguilar provides a solution to a problem identified in Cho. Nor does the proposed combination represent a substitution of any known elements from Gold or Aguilar for an element in Cho. Nor is the proposed combination the use of a technique disclosed in Gold or Aguilar to improve Cho. Nor does Petitioner identify any market or other factors creating incentive for a variation of Cho.

Petitioner has also failed to demonstrate that, even if these references were combined, they would have been combined in the specific way so as to arrive at the claimed invention. *See KSR* (requiring “a reason that would have prompted a [POSITA] to combine the elements ***in the way the claimed new invention does***”); *ActiveVideo* (citing *KSR* with same emphasis). For example, Petitioner merely states

that Gold teaches certain concepts, and makes a conclusory statement that a POSITA would have been motivated to combine these concepts with the disclosure in Cho. Petitioner also fails to articulate why a POSITA would have any reason to look to Gold specifically to modify Cho. Similarly with respect to Aguilar, Petitioner merely asserts that a POSITA “would have recognized the benefit” of doing so, but does not explain how or why that is the case. Pet., pp.90-91.

Petitioner also does not explain how or why, in combining Cho and Aguilar with Gold, the other teachings of Cho would have been unchanged so as to not affect the features allegedly rendering obvious the claims from which the challenged claims of Ground 5 depend.

**B. Cho in view of Gold and Aguilar does not render obvious Claim 3**

Cho in view of Gold and Aguilar does not disclose or suggest at least “a non-core power domain” as recited. For example, Petitioner asserts that “the GPU 420 (purple), memory controller hub (NorthBridge 415) (green), and Temperature Control Unit 102 (yellow) form a ‘non-core power domain’,” but does not explain how they do so. For example, Petitioner does not address how they form a “power domain” as claimed, despite having allegedly different (and independently controllable) voltages for example.

Cho in view of Gold and Aguilar also do not disclose or suggest at least “a cache shared by the plurality of cores” as claimed. For example, Petitioner does not

identify or rely on any disclosures in Cho for its assertion that “[a] POSITA would have understood that Cho’s memory controller hub NorthBdidge 415 contained a cache,” and instead relies solely on conclusory statements from the Mudge Declaration. Pet., p.92 (citing Ex. 1002). For example, Petitioner does not explain why, even assuming there were a cache, the hypothetical cache would not merely be associated with each component, as opposed to being “shared by the plurality of cores” as claimed.

Petitioner’s reliance on Aguilar fares no better in rendering obvious a cache shared by the plurality of cores. For example, Petitioner merely asserts that Aguilar discloses the existence of “a cache such as found in *north bridge* and memory controller hub,” but does not assert that Aguilar discloses or suggests that there is only a single cache between them, or that it is “shared between the plurality of cores” as claimed. For example, as Aguilar discloses, each component can have its own architecture, and for example, its own cache.

**C. Cho in view of Gold and Aguilar does not render obvious Claim 7**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated with respect to Ground 4. Thus, for the same reasons discussed above with respect to Ground 4, Cho in view of Gold and Aguilar does not render obvious claim 7.

**D. Cho in view of Gold and Aguilar does not render obvious Claims 10, 14**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated with respect to claims 3 and 7. Thus, for the same reasons discussed above with respect to those claims, Cho in view of Gold and Aguilar does not render obvious claim 10 or 14.

**E. Cho in view of Gold and Aguilar does not render obvious Claim 15**

Cho in view of Gold and Aguilar does not render obvious claim 15. For example, Petitioner asserts that Aguilar discloses a “south bridge and input/output (I/O) controller hub (ICH) 204,” but does not explain how or why a POSITA, even combining these three references, would have added that disclosure into the combination. For example, Petitioner provides no explanation for why a POSITA would not have used a different SouthBridge architecture for the combination, for example, one more compatible with the teachings of Cho or Gold.

**F. Cho in view of Gold and Aguilar does not render obvious Claim 16**

Cho in view of Gold and Aguilar does not render obvious claim 16. For example, Petitioner asserts that Aguilar discloses that an “audio adapter 216” (orange) connects to a “south bridge and I/O controller hub 204 [yellow] through bus 238 and bus 240” (blue),” but does not explain how or why a POSITA, even

combining these three references, would have added that disclosure into the combination.

**G. Cho in view of Gold and Aguilar does not render obvious Claim 17**

Cho in view of Gold and Aguilar does not render obvious claim 17. For example, Petitioner asserts that Aguilar discloses that “[i]nput/output or I/O devices (including, but not limited to ... displays[]) can be coupled to the system either directly or through intervening I/O controllers,” but does not explain how or why a POSITA, even combining these three references, would have added that disclosure into the combination.

**H. Cho in view of Gold and Aguilar does not render obvious Claim 18**

Cho in view of Gold and Aguilar does not render obvious claim 18. For example, Petitioner asserts that Aguilar discloses that a “keyboard and mouse adapter 220” (orange) connect to a “south bridge and I/O controller hub 204 [yellow] through bus 238 and bus 240” (blue),” but does not explain how or why a POSITA, even combining these three references, would have added that disclosure into the combination.

**I. Cho in view of Gold and Aguilar does not render obvious Claim 19**

Cho in view of Gold and Aguilar does not render obvious claim 19. For example, Petitioner asserts that Aguilar discloses that a “local area network (LAN)

adapter 212” (orange) connects to a “south bridge and I/O controller hub 204 [yellow] through bus 238 and bus 240,” but does not explain how or why a POSITA, even combining these three references, would have added that disclosure into the combination.

## **X. Ground 6 Fails**

The Petition asserts in Ground 6 that Claims 5-6, and 12-13 are rendered obvious by Cho, Gold, and Shakkarwar.

### **A. Cho would not have been combined with Gold and Shakkarwar**

Petitioner has not demonstrated that a person of ordinary skill in the art would have been motivated to combine Cho with Gold and Shakkarwar. *See* Pet., pp. 101-103. For example, Cho would not have been combined with Gold for at least the reasons set forth above with respect to Ground 4. Additionally, Cho and Gold would not have further been combined with Shakkarwar.

For example, Petitioner asserts that Cho would be combined with Gold and Shakkarwar because each relates to power management, but does not explain how or why that provides a motivation to combine. Generally, being directed to the same field of endeavor is required for a motivation to combine, but not sufficient. Petitioner does not allege that Gold or Shakkarwar provides a solution to a problem identified in Cho. Nor does the proposed combination represent a substitution of any known elements from Gold or Shakkarwar for an element in Cho. Nor is the

proposed combination the use of a technique disclosed in Gold or Shakkarwar to improve Cho. Nor does Petitioner identify any market or other factors creating incentive for a variation of Cho.

Petitioner has also failed to demonstrate that, even if these references were combined, they would have been combined in the specific way so as to arrive at the claimed invention. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (requiring “a reason that would have prompted a [POSITA] to combine the elements ***in the way*** the claimed new invention does”). For example, Petitioner merely states that Gold teaches certain concepts, and makes a conclusory statement that a POSITA would have been motivated to combine these concepts with the disclosure in Cho. Petitioner also fails to articulate why a POSITA would have any reason to look to Gold specifically to modify Cho. Similarly with respect to Shakkarwar, Petitioner merely asserts that a POSITA “would have recognized the benefit” of doing so, but does not explain how or why that is the case. Pet., p.102.

Petitioner also does not explain how or why, in combining Cho and Shakkarwar with Gold, the other teachings of Cho would have been unchanged so as to not affect the features allegedly rendering obvious the claims from which the challenged claims of Ground 6 depend.

**B. Cho in view of Gold in view of Shakkarwar does not render obvious Claim 5, 6, 12, 13**

Petitioner does not assert that any of these limitations is met for any reasons other than those articulated with respect to Ground 4. For example with respect to claim 5, Petitioner merely states in conclusory fashion that this claim is rendered obvious with a single sentence regarding the alleged contribution of Shakkarwar, without any explanation, citations to Shakkarwar, or analysis as to the contributions. *See* Pet., 103 (“Cho, in view of Shakkarwar teaches that this power management circuitry would have been implemented to include a mapping of selectable frequencies...”). This renders the Petition insufficient with respect to these claims, as it does not even cite any other explanations regarding the contributions of Shakkarwar to the analysis.

**XI. Conclusion**

For at least the foregoing reasons, the Petition does not meet its burden of demonstrating a reasonable likelihood that Petitioner would prevail with respect to any of the challenged claims. Thus, Patent Owner respectfully requests that the Board deny institution.

Dated: July 17, 2023

Respectfully submitted,

/Peter F. Snell/

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**CERTIFICATE OF WORD COUNT**

The undersigned certifies pursuant to 37 C.F.R. § 42.24(d) that the foregoing Patent Owner Preliminary Response, excluding any table of contents, table of authorities, certificates of service or word count, or appendix of exhibits or claim listing, contains 9,373 words according to the word-processing program used to prepare this paper (Microsoft Word). Patent Owner certifies that this Patent Owner Preliminary Response does not exceed the applicable type-volume limit of 37 C.F.R. § 42.24(a).

Dated: July 17, 2023

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**CERTIFICATE OF SERVICE**

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