

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

Case IPR2023-00547
Patent 10,705,588 B2

Before WILLIAM V. SAINDON, ARTHUR M. PESLAK, and
KRISTIL R. SAWERT, *Administrative Patent Judges*.

SAWERT, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Qualcomm Incorporated (“Petitioner”) filed a petition to institute *inter partes* review of claims 1–20 of U.S. Patent No. 10,705,588 B2 (Ex. 1001, “the ’588 patent”). Paper 1 (“Pet.”). Daedalus Prime LLC (“Patent Owner”) filed a Preliminary Response. Paper 12 (“Prelim. Resp.”).

We have authority under 35 U.S.C. § 314 to determine whether to institute an *inter partes* review. The standard for instituting an *inter partes* review is set forth in 35 U.S.C. § 314(a), which provides that an *inter partes* review may not be instituted unless “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” If the Board institutes trial, it “will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.” 37 C.F.R. § 42.108(a); *see also PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1360 (Fed. Cir. 2018) (interpreting the statute to require “a simple yes-or-no institution choice respecting a petition, embracing all challenges included in the petition”).

Applying those standards, and upon considering the Petition, the Preliminary Response, and the evidence of record, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of at least one of the challenged claims of the ’588 patent. Accordingly, we institute an *inter partes* review of claims 1–20 of the ’588 patent on the grounds asserted in the Petition.

The following preliminary findings of fact and conclusions of law are made solely for determining whether to institute review. Any final decision will be based on the full trial record.

II. BACKGROUND

A. *Related Matters*

Petitioner identifies the following non-PTAB proceedings as related matters involving the '588 patent:

- (1) *Daedalus Prime LLC v. Arrow Electronics, Inc. et al.*, 1:22-cv-01107 (D. Del.);
- (2) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01109 (D. Del.);
- (3) *Daedalus Prime LLC v. Mazda Motor Corporation et al.*, 1:22-cv-01108 (D. Del.);
- (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352 (E.D. Tex.);
- (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, U.S. International Trade Commission (“ITC”) Inv. No. 337-TA-1335 (Violation); and
- (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, ITC Inv. No. 337-TA-1332 (Violation).

Pet. 2–3. Patent Owner identifies above proceedings (4) and (5). Paper 6 (Mandatory Notices) 1.

We note the following Board proceedings involve the same parties and related patents: IPR2023-00550 (Patent 8,775,833 B2); IPR2023-00567 (Patent 10,049,080 B2); and IPR2023-00617 (Patent 8,898,494 B2).

B. *Real Parties in Interest*

Petitioner identifies Qualcomm Incorporated and Qualcomm Technologies, Inc. as its real parties in interest. Pet. 2. Patent Owner identifies Daedalus Prime LLC as its real party in interest. Paper 6, 1.

C. Overview of the '588 Patent

The '588 patent, titled “Enabling a Non-Core Domain to Control Memory Bandwidth in a Processor,” relates to a “multi-domain processor including multiple domains such as a core domain, a non-core domain and a system agent domain” that “enable[s] the non-core domain to control memory bandwidth available to it.” Ex. 1001, code (54), 1:57–60. The '588 patent states that “[b]y allowing a non-core domain to have control over an interconnect frequency and thus bandwidth, memory bandwidth used by non-core domain can be more efficient” than in the processors of the prior art. *Id.* at 1:67–2:2.

Figure 3, reproduced below, is a block diagram of one embodiment of a processor according to the '588 patent. *Id.* at 1:47–48.

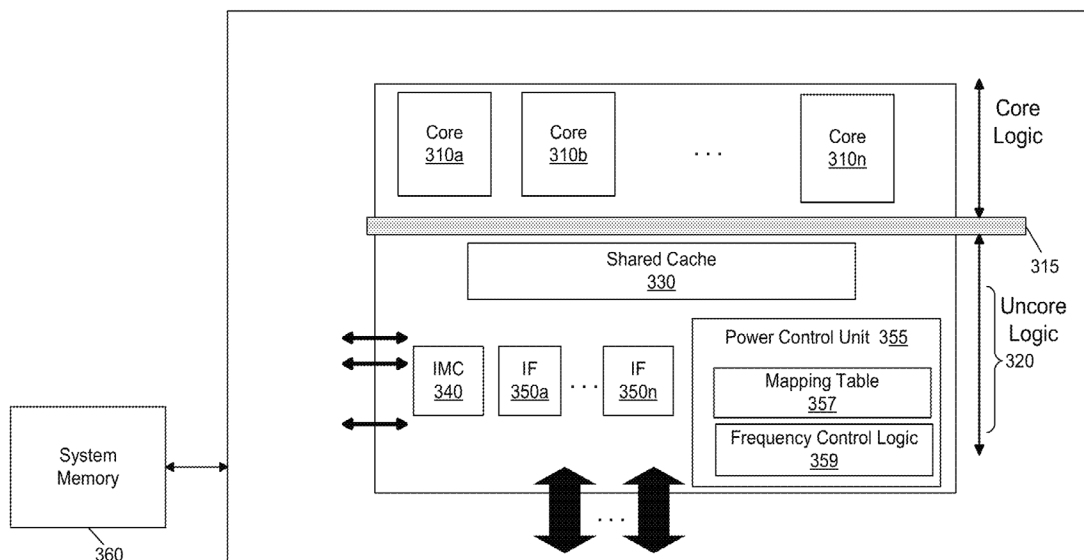


FIG. 3 is a block diagram of a processor according to the '588 patent.

As shown, processor 300 includes: (1) a plurality of cores 310 a –310 n having independent power domains and operating at independent voltages and/or frequencies; (2) a system agent or “uncore” 320 having a shared cache 330, an integrated memory controller (IMC) 340, various interfaces (IF) 350 a –350 n , and a power control unit (PCU) 355; (3) an interconnect 315 that couples the cores 310 a –310 n to the uncore 320; and (4) system memory 360. *Id.* at 5:37–50, 6:4–6. Processor 300 communicates with the system memory 360 via a memory bus and with various off chip components (e.g., peripheral devices and mass storage) via the interfaces 350. *Id.* at 6:4–9.

The ’588 patent states that, in some embodiments, PCU 355 includes a mapping table 357 and frequency control logic 359, whereby each domain (e.g., each core) has a respective mapping table/entries that associate a given domain frequency to a corresponding minimum interconnect frequency. *Id.* at 5:51–66. The frequency control logic 359 dynamically controls the interconnect frequency responsive to a request of a given domain (e.g., of a core) by reference to matching entries of the mapping table 357. *Id.*

Figure 4, reproduced below, is block diagram of another embodiment of a processor according to the ’588 patent. *Id.* at 1:49–51.

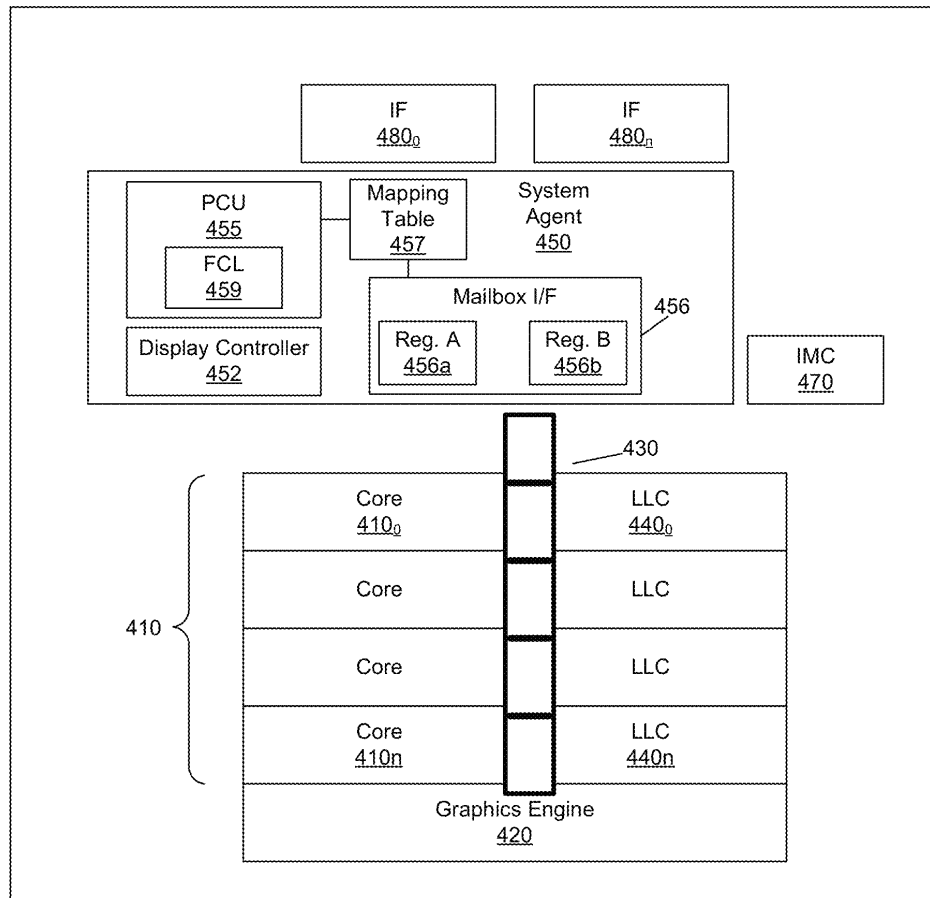


FIG. 4 is a block diagram of a processor according to the '588 patent.

As shown, processor 400 includes: (1) a core domain 410 having a plurality of cores 410₀–410_n; (2) last level caches (LLC) 440₀–440_n associated with each core; (3) a graphics domain 420 having one or more graphics engines; and (4) a system agent domain 450. *Id.* at 6:11–18, 6:32–34. A ring interconnect 430 couples the cores 410₀–410_n and their respective LLCs 440₀–440_n, and further interconnects the core 410, graphics domain 420, and system agent domain 450. *Id.* at 6:32–40.

The system agent domain 450 includes a display controller 452 that provides a user interface, and a power control unit 455 having frequency control logic 459 that dynamically updates the frequency of interconnect 430

by referencing a coupled mapping table 457 (associating a domain's frequency and a corresponding minimum interconnect frequency, as described above). *Id.* at 6:45–58. The system agent domain 450 “may execute at a fixed frequency and may remain powered on at all times to handle power control events and power management such that domains 410 and 420 can be controlled to dynamically enter into and exit low power states.” *Id.* at 6:18–23.

The '588 patent states that a mailbox interface 456 is used to configure the mapping table 457. *Id.* at 6:64–66. The mailbox interface 456 includes a first register 456a and second register 456b providing an interface for handshake-based communications between the PCU and other domains. *Id.* at 6:64–7:2. Graphics domain 420 can write to the mapping table 457 by providing, to the first register 456a, a write command, an entry address of the table, and data to be written. *Id.* at 7:7–12. The data is written to the second register 456b. *Id.* at 7:12–13. PCU 455 then writes the data to the entry address of the table. *Id.* at 7:14–16.

D. The Challenged Claims

Petitioner challenges claims 1–20 of the '588 patent. Pet. 4–6. Of the challenged claims, claims 1, 8, and 20 are independent. Claim 1 is illustrative of the claimed subject matter and reproduced below with Petitioner's added identifiers bolded and in brackets.

1. **[pre]** A processor comprising:

[a] a plurality of cores including a first core operable at a first voltage and a first frequency, and **[b]** a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency;

- [c] graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency; and
- [d] an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.

Ex. 1001, 8:35–49; Pet. i–ii (identifiers).

E. Evidence

Petitioner submits the following evidence:

Evidence	Exhibit No.
Declaration of Dr. Trevor Mudge	1002
U.S. Published Patent Application No. 2010/0073068 (“Cho”)	1005
U.S. Patent No. 8,468,373 B2 (“Machnicki”)	1006
U.S. Patent No. 7,552,346 B2 (“Aguilar”)	1007
U.S. Patent No. 7,392,411 B2 (“Shakkarwar”)	1008
U.S. Published Patent App. No. US 2009/0235108 A1 (“Gold”)	1009

F. Asserted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 4, 8, 9, 11, 15–20	103(a) ¹	Machnicki

¹ Congress amended §§ 102 and 103, among other sections, when it passed the Leahy-Smith America Invents Act (“AIA”). Pub. L. No. 112–29, § 3(c), 125 Stat. 284, 287 (2011). Petitioner does not identify whether the challenges are based on pre-AIA or post-AIA §§ 102 and 103. But, because Petitioner asserts the “earliest possible priority for the ’588 Patent is October 27, 2011” (Pet. 8) and the AIA’s changes to §§ 102 and 103 impact only applications filed on or after March 16, 2013, we herein denote (for institution) Petitioner’s challenges as being based on pre-AIA statutes.

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
3, 7, 10, 14	103(a)	Machnicki, Aguilar
5, 6, 12, 13	103(a)	Machnicki, Shakkarwar
1, 2, 4, 8, 9, 11, 20	103(a)	Cho, Gold
3, 7, 10, 14–19	103(a)	Cho, Gold, Aguilar
5, 6, 12, 13	103(a)	Cho, Gold, Shakkarwar

Pet. 5–6. Patent Owner disputes Petitioner’s asserted grounds of unpatentability. *See generally* Prelim. Resp.

A. Overview of the Asserted Prior Art

We now provide brief summaries of the asserted references.

1. Machnicki (Ex. 1006)

Machnicki “relate[s] to the field of computer systems, and more particularly to systems and methods for coordinating performance parameters in multiple circuits.” Ex. 1006, 1:10–12. Machnicki teaches that there is a need for “managing power and performance tradeoffs in an integrated circuit” by changing “the performance states of various components on the integrated circuit,” but that “[m]anaging the changes over multiple components can be difficult to implement correctly.” *Id.* at 1:27–32.

Machnicki teaches a “power management mechanism” that allows a circuit, component, or device to “switch between various performance levels or states.” *Id.* at 1:49–56. For example, when a device is in a first state, “a first performance domain may operate with a first clock frequency or voltage, while a second performance domain operates with a second clock frequency or voltage,” and, when the device is in a second state, “these performance domains may operate with modified frequencies or voltages.” *Id.* at 1:56–63. Machnicki teaches that changes to the various performance

levels occurs via a “stage change request,” which “may include a value or indication that is written to a single register”—such as a “performance state table”—and “which may then be used [to] look-up or otherwise derive configuration parameters used for switching the first and second frequencies to the first and second modified frequencies (or voltages), respectively.” *Id.* at 2:6–21.

Figure 1, reproduced below, is a block diagram illustrating one embodiment of Machnicki’s power management system. *Id.* at 3:8–9.

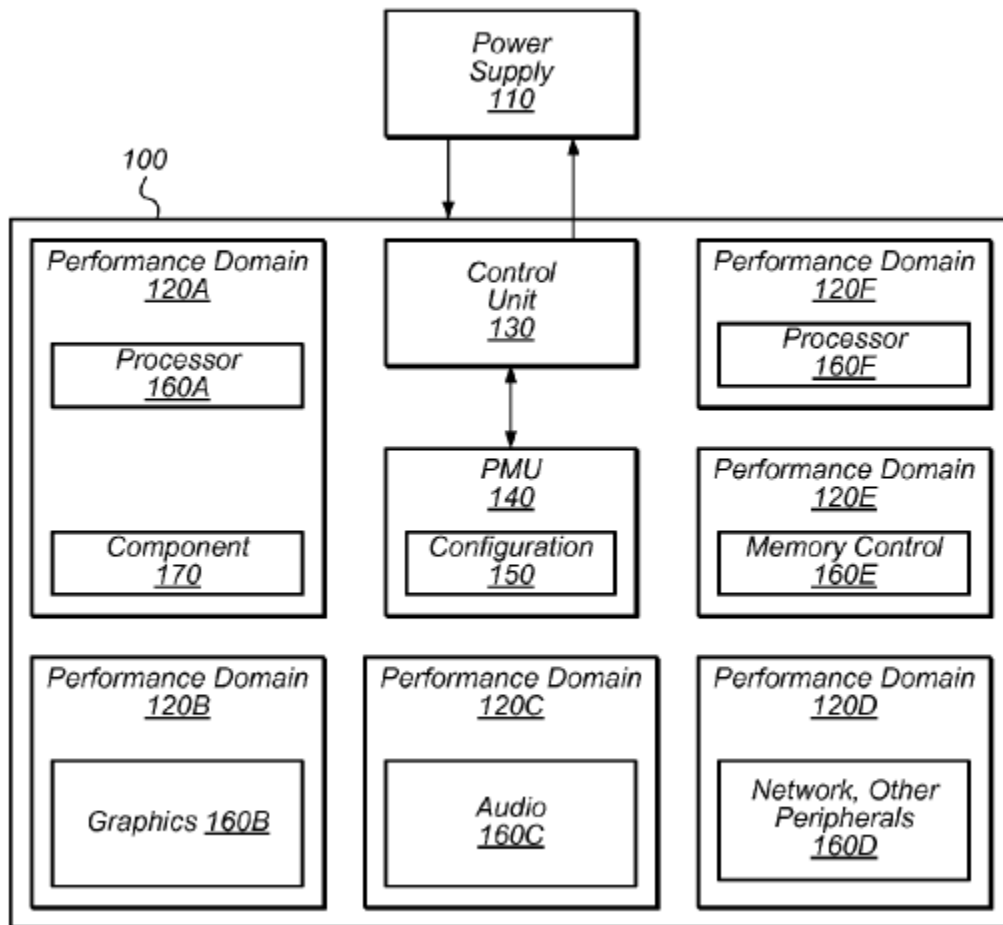


FIG. 1 is a block diagram of a power management system according to Machnicki.

Power supply 110 is coupled to integrated circuit (IC) 100. *Id.* at 4:8–12. IC 100 includes power management unit (PMU) 140 having performance configuration registers 150, a clock and/or voltage control unit (control unit) 130 coupled to the PMU 140, and a set of performance domains 120A–F. *Id.* at 4:8–13, 4:25–30. Machnicki teaches that each of performance domains 120A–F may include at least one component, e.g., performance domain 120A includes processor 160A and component 170; performance domain 120B includes graphics subsystem 160B; performance domain 120C includes audio subsystem 160C; performance domain 120D includes networking peripherals 160D; performance domain 120E includes memory control circuit 160E; and performance domain 120F includes optional second processor 160F. *Id.* at 4:13–25.

Machnicki teaches that PMU 140 and control unit 130 are coupled to domains 120A–F. *Id.* at 4:33–34. The control unit 130 supplies clock signals to performance domains 120A–F and interacts with power supply 110 to request respective supply voltages for the domains 120A–F. *Id.* at 4:33–40. PMU 140 transitions domains 120A–F to different performance states. *Id.* at 4:45–47. Specifically, PMU 140 communicates new frequency settings and/or new voltages to control unit 130, which in turn implements the new parameters by generating the clocks at the requested frequencies and/or requesting the desired supply voltages from the power supply 110. *Id.* at 6:14–20.

Machnicki teaches that PMU 140 determines states of the domains 120A–F by accessing an included state table and, more specifically, one of multiple entries each defining a combination of domains and respective performance states. *Id.* at 4:47–53; 6:6–13. A desired change of state(s) is

communicated to the PMU 140 as an indication of a respective table entry. *Id.* at 6:8–11. Table I of Machnicki, reproduced below, provides an exemplary table where “both clock frequencies and voltages are configuration parameters that may be set for each of the performance domains (e.g. domains 1 through m).” *Id.* at 8:2–4.

TABLE I

	Domain 1	Domain 2	...	Domain m
state 1	$f_{1,1}; V_{1,1}$	$f_{2,1}; V_{2,1}$	...	$f_{m,1}; V_{m,1}$
state 2	$f_{1,2}; V_{1,2}$	$f_{2,2}; V_{2,2}$	...	$f_{m,2}; V_{m,2}$
state 3	$f_{1,3}; V_{1,3}$	$f_{2,3}; V_{2,3}$	...	$f_{m,3}; V_{m,3}$
...	...	...	...	...
state n	$f_{1,n}; V_{1,n}$	$f_{2,n}; V_{2,n}$	...	$f_{m,n}; V_{m,n}$

Id. at 8:8–17. If software desires to set the frequencies (f) and/or voltages (V) for each domain in integrated circuit 100, then the software writes a pointer to the corresponding entry (1 to n) in the table to configuration register 150 of PMU 140. *Id.* at 8:18–22. PMU 140 reads the selected entry and communicates the respective clock frequencies and/or voltages to the control unit 130, which then causes the respective changes. *Id.* at 8:22–27. “As a result,” Machnicki teaches, “different portions of integrated circuit 100 may alternate between their various different states with a single command or register write.” *Id.* at 8:27–30.

2. *Aguilar (Ex. 1007)*

Aguilar “relates generally to use of thermal profiles” and “to a computer implemented method, data processing system, and computer usable code for dynamically adapting software for optimal thermal performance.” Ex. 1007, 1:9–13. For optimizing thermal performance of a computer system, Aguilar teaches that a “set of system resources associated

with the computer system are identified and a thermal index is requested for each of the set of system resources to form a set of thermal indexes,” and then, “[a]n action is identified from a set of actions to reduce resource utilization and the action is implemented to reduce a thermal state of the computer system.” *Id.* at 1:51–59. For example, “[i]f, for any reason, the temperature continues to rise and reaches a temperature at or above the full throttle point, the PowerPC process element or synergistic processor element is stopped until the temperature drops below the full throttle point.” *Id.* at 10:24–28.

Figure 2, reproduced below, is a block diagram illustrating one embodiment of Aguilar’s data processing system. *Id.* at 2:6–8.

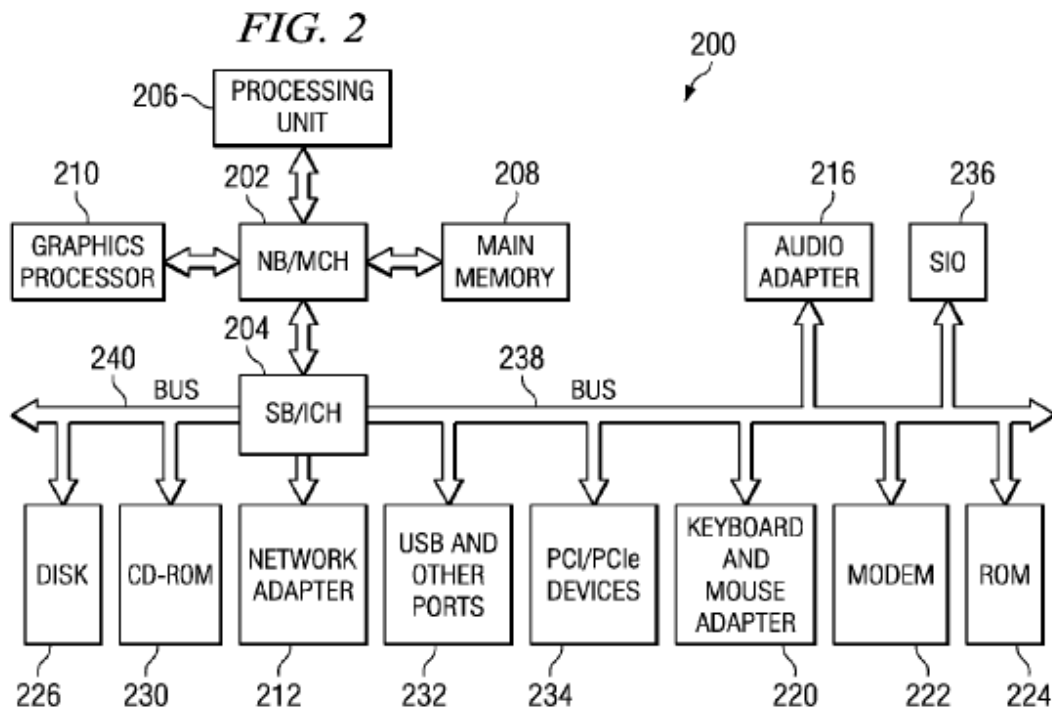


FIG. 2 is a block diagram of a power management system according to Aguilar.

Data processing system 200 employs a hub architecture that connects a north bridge and memory controller hub (NB/MCH) 202 to a south bridge

input/output controller hub (SB/ICH) 204. *Id.* at 3:44–47. The NB/MCH 202 connects to a processing unit 206, main memory 208, and graphics processor 210. *Id.* at 3:47–49. Aguilar teaches that a “memory may be, for example, main memory 208, read only memory 224, or a cache such as found in north bridge and memory controller hub 202 in FIG. 2.” *Id.* at 4:57–60. The SB/ICH 204 connects to a local area network (LAN) adapter 212 and two buses 238, 240. *Id.* at 3:53–60. The buses, in turn, connect to variety of peripheral components, including an audio adapter 216, keyboard and mouse adapter 220, modem 222, read only memory (ROM) 224, hard disk drive (HDD) 226, CD-ROM drive 230, universal serial bus (USB) ports and other communications ports 232, and PCI/PCIe devices 234. *Id.* at 3:55–60.

3. *Shakkarwar (Ex. 1008)*

Shakkarwar “relates to efficient use of electronic devices and, more particularly, to systems and methods for power management of electronic devices.” Ex. 1008, 1:8–10. In one embodiment for dynamic power management, Shakkarwar teaches that “an electronic device employs one or more clocks for latching signals at components associated with the electronic device.” *Id.* at 2:49–51. By monitoring the needed data bandwidth between two or more components, “the clock speed at which data is transferred (data rate) between components can be controlled to optimize power consumption.” *Id.* at 2:54–58. Thus, Shakkarwar teaches, “data rates between components or electronic devices can be matched to meet the bandwidth needed without sacrificing performance.” *Id.* at 2:55–64.

Figure 3, reproduced below, is a block diagram illustrating one embodiment of Shakkarwar’s power management system. *Id.* at 2:19–22.

In this embodiment, the power management system “employ[s] multiple communication buses having associated bandwidths for communicating information.” *Id.*

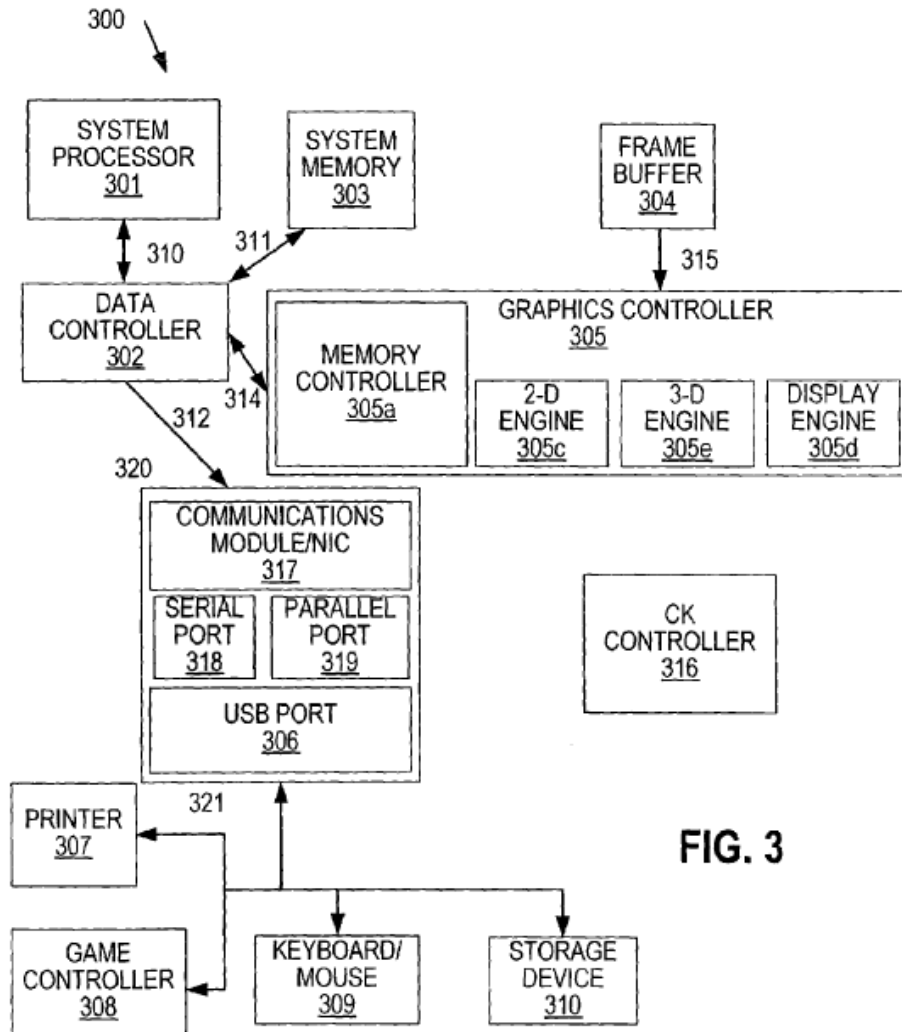


FIG. 3

FIG. 3 is a block diagram of a power management system according to Shakkarwar.

System 300 includes a system processor 301, data controller 302, system memory 303, Input Output (IO) device 320, graphics controller 305, frame buffer memory 304, and USB devices 307–310. *Id.* at 4:65–5:2. Shakkarwar teaches that clock and voltage levels of each processor, device, and/or controller can be altered based on bandwidth requirements for

communicating and processing information. *Id.* at 5:25–30. Specifically, clock/voltage control 316 monitors the processing condition of system 300 “to determine when one or more portions of system 300 are not used and an operating characteristic of an associated data connection can be altered to assure proper operation.” *Id.* at 5:43–47.

As an example, Shakkarwar teaches that, if USB module 306 is not being used (i.e., no USB devices are coupled to USB 306), then the data rate of data connection 312 is reduced by an amount equal to bandwidth needed to support the USB module 306. *Id.* at 5:47–51. But, if one or more devices are coupled to USB module 306, then bandwidth requirements for each device are determined by USB module 306 by accessing a look-up table stored in memory. *Id.* at 5:53–62. According to Shakkarwar, the look-up table “provide[s] device identification and associated operating characteristics of each connected device.” *Id.* at 5:58–62. And the USB module 306 determines “the required bandwidth needed to support the connected device” and alters operating characteristics (e.g., voltage level and/or clock) to support the needed bandwidth for each device. *Id.* at 5:62–6:1.

4. *Cho (Ex. 1005)*

Cho relates to “thermal monitoring and control of electronic circuits.” Ex. 1005 ¶ 2. Cho teaches an integrated circuit (IC) including a plurality of functional units, each in turn including one or more temperature sensors. *Id.* ¶ 7. A temperature control unit coupled to each of the functional units monitors the temperature of its corresponding functional unit. *Id.* If a functional unit’s temperature exceeds a threshold value, then the temperature control unit “perform[s] a first temperature control action on the particular

one of the plurality of functional units independently of other ones of the plurality of functional units.” *Id.* Cho teaches that “temperature control actions may include reducing a clock frequency or reducing a voltage to the particular functional block,” and, in embodiments where the IC is a multi-core processor, temperature control action “may include shifting a processor workload from one core to another.” *Id.* ¶ 10.

Figure 4, reproduced below, is a block diagram illustrating “one embodiment of a multi-core processor having an integrated memory controller hub and graphics processing unit” that is “configured for functional block level thermal control.” *Id.* ¶¶ 15, 38.

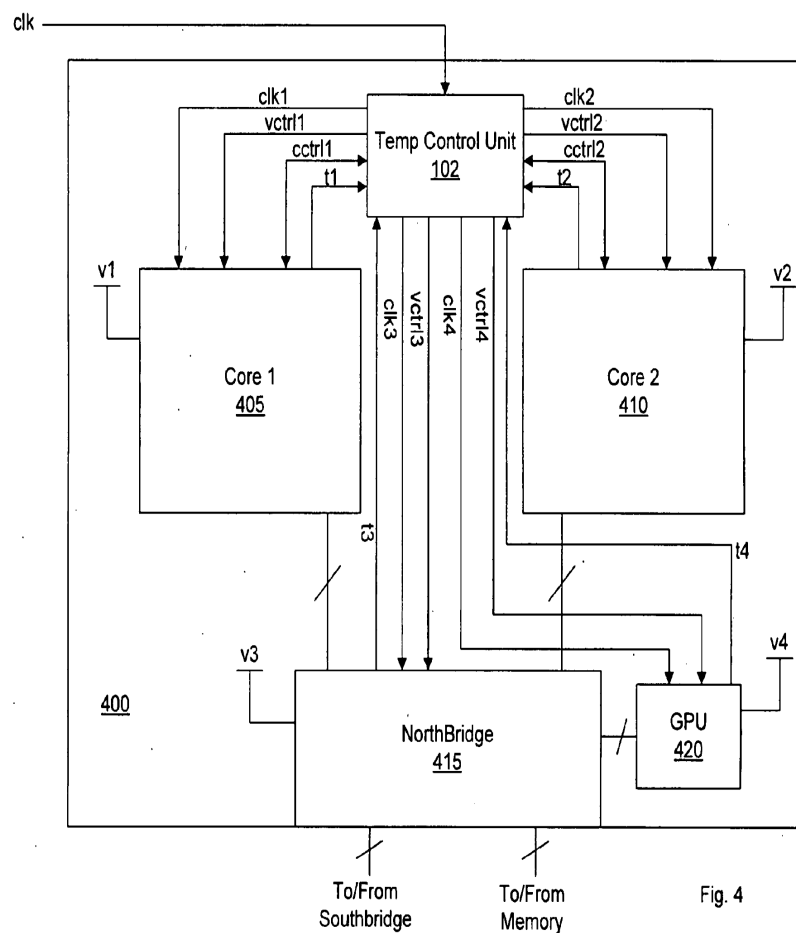


FIG. 4 is a block diagram of a multi-core processor according to Cho.

Processor 400 includes four primary functional units: two processor cores 405 and 410, a memory controller hub (North Bridge 415), and a graphics processing unit (GPU) 420. *Id.* ¶ 38. Temperature control unit (TCU) 102 receives temperature signals from each unit functional unit and “performs temperature control actions on each [unit], independently of any temperature control actions performed on other ones of the functional units.” *Id.* ¶¶ 38–39.

The “temperature control action” may include “changing a voltage, changing a frequency, or reallocating workload.” *Id.* ¶ 43. For changing voltage and/or frequency, Cho teaches that TCU 102 provides a voltage control signal *vctrl* and/or clock signals *clk1–clk4* to each of the units 105–120 to control each unit’s respective voltages and frequencies, respectively. *Id.* ¶¶ 21–22. And, for reallocating workload, Cho teaches that TCU 102 may monitor the processing load of each processing core 405 and 410 and re-allocating the processing load between the processor cores 405, 410 by core control signals *cctrl1* and *cctrl2*. *Id.* ¶ 42.

5. *Gold (Ex. 1009)*

Gold relates to “embodiments for performing overclocking for a plurality of processing units,” where “overclocking” is defined as “operating a processing unit or core above its standard operating frequency to improve performance.” Ex. 1009 ¶¶ 5, 27. Gold teaches that, in one embodiment, each processing core “has a respective standard operating frequency.” *Id.* ¶ 5.

Figure 2, reproduced below, is a block diagram illustrating an embodiment of a computer system for performing overclocking. *Id.* ¶ 9.

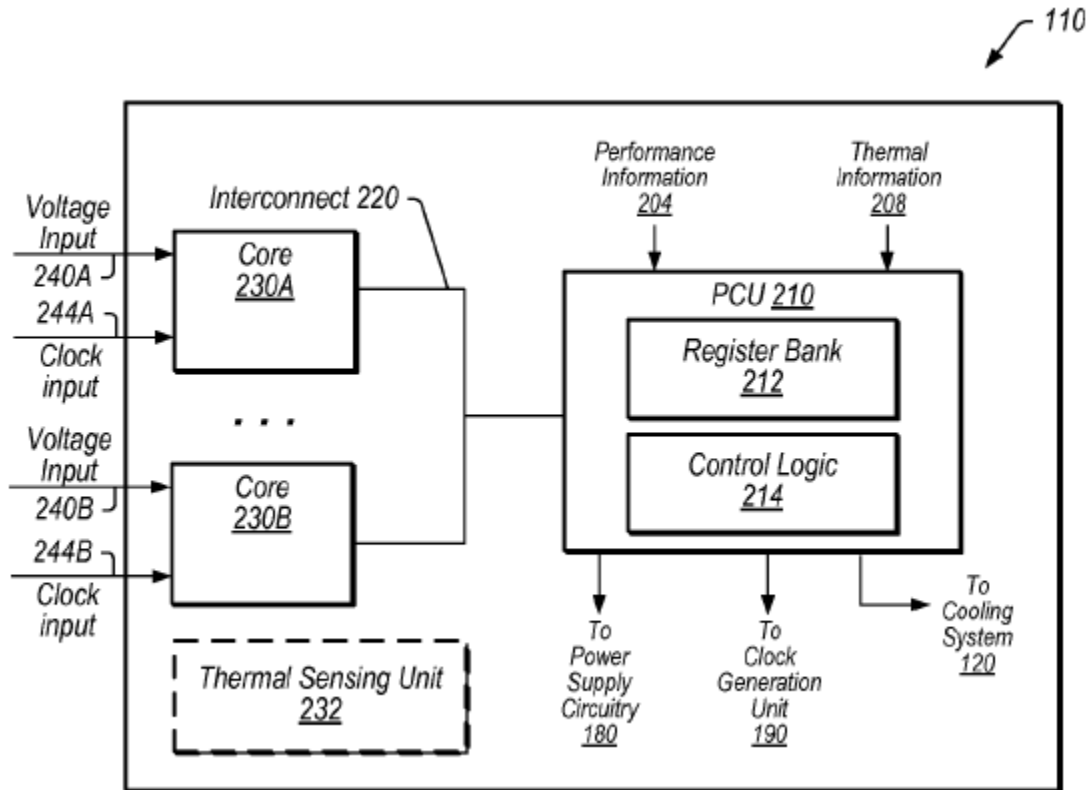


FIG. 2 is a block diagram of a multi-core apparatus according to Gold.

Computer subsystem 110 includes cores 230A and 230B coupled to performance control unit (PCU) 210 via interconnect 220. *Id.* ¶ 25. The PCU is configured to automatically determine whether to overclock one or more of the cores, as well as whether to discontinue overclocking of one or more of the cores based on predetermined set(s) of criteria, such as performance information 204 and thermal information 208. *Id.* ¶¶ 26, 28.

The PCU is coupled to “clock generation unit” 190. *Id.* ¶ 29. To perform overclocking, the PCU sends control signals to the clock generation unit to “increase, for each of a first set of one or more of the plurality of processing cores, the frequency of the respective clock signal above its

standard operating frequency.” *Id.* ¶ 5. And, to discontinue overclocking, the PCU sends control signals to the clock generation unit “to return the frequency of the clock signal for each of the first set of processing cores to its standard operating frequency.” *Id.*

Gold teaches that each core has an assigned “performance state” or P-state, having “a corresponding input voltage and clock frequency.” *Id.* ¶ 39. Figure 5A, reproduced below, presents “an exemplary table of performance states” for a processing core. *Id.* ¶ 12; *see also id.* ¶ 39.

<i>P-State</i>	<i>Power Usage</i>	<i>Frequency</i>
<i>P Max</i>	19W	2.90 GHz
<i>P 0</i>	15W	2.60 GHz
<i>P 1</i>	12W	2.28 GHz
<i>P 2</i>	9W	1.73 GHz

FIG. 5A is a table of exemplary performance states for a processing core according to Gold.

In this example, performance states P0–P2 represent non-overclocked processing states while P Max represents an overclocked processing state. *Id.* ¶ 39.

III. DISCUSSION

Petitioner contends that claims 1–20 of the ’588 patent are unpatentable under 35 U.S.C. § 103 as obvious over various combinations of prior-art references Machnicki, Aguilar, Shakkarwar, Cho, and Gold. A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter

pertains. 35 U.S.C. § 103(a) (2006); *see also* *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved based on underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) any objective indicia of nonobviousness.² *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). An obviousness determination requires finding a reason to combine accompanied by a reasonable expectation of achieving what is claimed in the challenged patent. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016). “[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.” *KSR*, 550 U.S. at 419–20.

We organize our discussion into three sections. First, we address the level of ordinary skill in the art. Second, we address claim construction. And third, taking account of the information presented, we consider whether the Petition satisfies the threshold requirement for instituting an *inter partes* review under 35 U.S.C. § 314(a).

In an *inter partes* review, “the petitioner has the burden from the onset to show with particularity why the patent it challenges is unpatentable.” *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016) (citing 35 U.S.C. § 312(a)(3) (requiring inter partes review petitions to identify “with particularity . . . the evidence that supports the grounds for the challenge to each claim”)). Petitioner ultimately bears the burden of

² At this time, Patent Owner does not assert objective indicia supporting nonobviousness of the challenged claims. *See generally* Prelim. Resp.

persuasion to prove unpatentability of each challenged claim by a preponderance of the evidence. 35 U.S.C. § 316(e). This burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). The Board may authorize an *inter partes* review if we determine that the information presented in the Petition and Patent Owner's Preliminary Response shows that there is a reasonable likelihood that Petitioner will prevail with respect to at least one of the claims challenged in the petition. 35 U.S.C. § 314(a).

1. *Level of Ordinary Skill in the Art*

We consider the asserted grounds of unpatentability in view of the understanding of a person of ordinary skill in the art. In assessing the level of ordinary skill in the art, various factors may be considered, including (1) educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. *Environmental Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983). Not all of these factors may be present in every case, and one or more of these or other factors may predominate in a particular case. *Id.* Moreover, these factors are not exhaustive but are merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. Ltd, Inc. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007).

Relying on the declaration testimony of Dr. Mudge, Petitioner contends that an ordinarily skilled artisan for the '588 patent:

would have had a bachelor's degree in electrical engineering, computer science, computer engineering, material science, physics, applied physics, or a related field, and at least two years

of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.

Pet. 7–8 (citing Ex. 1002 ¶¶ 22–26). Patent Owner does not appear to address the level of ordinary skill in the art. *See generally* Prelim. Resp.

Based on the record presented, including our review of the ’588 patent and cited prior art, we agree with Petitioner’s proposed definition. Thus, we apply Petitioner’s definition for this decision. *See, e.g.*, Ex. 1001, 1:31–2:10 (describing in the “Background” section of the ’588 patent various conventional methods of computation and their alleged deficiencies).

B. Claim Construction

Next, we turn to claim construction. In interpreting the claims of the ’588 patent, we “us[e] the same claim construction standard that would be used to construe the claim[s] in a civil action under 35 U.S.C. [§] 282(b).” 37 C.F.R. § 42.100(b). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as would have been understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (*en banc*).

Petitioner proposes claim constructions for the “means for” limitations of claim 20. Pet. 8–9. Specifically, Petitioner asserts that “[t]he challenged claims recite elements that use the word ‘means,’ creating a rebuttable presumption that they are means-plus-function elements under § 112” and offers correlating structures for “means for operating a first core” (limitation 20[a]); “means for independently operating a graphics processor” (limitation 20[b]); and “interconnect means to couple the graphics processor”

(limitation 20[c]). *Id.*; *see also id.* at iv (Petitioner’s 20[a]–[c] identifiers of the limitations). Patent Owner does not propose claim constructions or respond to the Petitioner’s asserted claim constructions. *See generally* Prelim. Resp.

Having considered the record, we conclude that no terms require express interpretation at this time. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“[W]e need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy.’” (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))). Any final written decision entered in this case may include a final claim construction based on the full trial record that differs from any discussion of claim scope provided in our analysis below.

C. Asserted Grounds of Unpatentability

We now consider whether the Petition satisfies the threshold requirement for instituting an *inter partes* review under 35 U.S.C. § 314(a) by addressing each of Petitioner’s asserted grounds of unpatentability, below.

1. Alleged Obviousness of Claims 1, 2, 4, 8, 9, 11, and 15–20 over Machnicki

Petitioner contends that claims 1, 2, 4, 8, 9, 11, and 15–20 of the ’588 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Machnicki. Pet. 20–43. Patent Owner disputes Petitioner’s contentions. Prelim. Resp. 13–17. Having considered the arguments and evidence before us, we find that the record establishes a reasonable likelihood that Petitioner would prevail on this asserted ground of unpatentability. Nevertheless, we

recognize that the issues in dispute are highly fact-intensive and implicate genuine issues of fact more appropriately resolved on a fully developed record.

a) Currently undisputed limitations 1[pre] and 1[a]

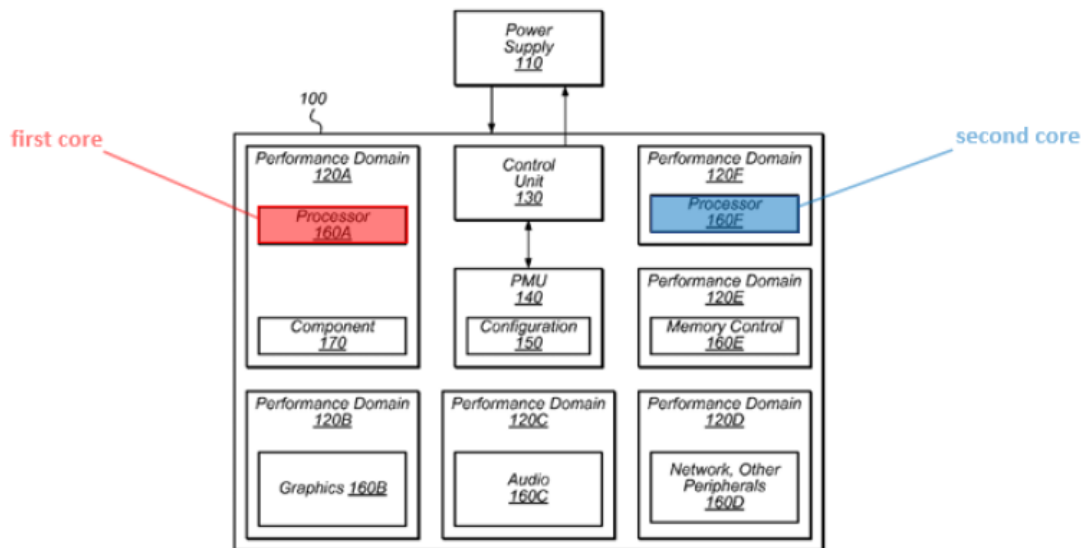
Taking claim 1 as illustrative, Petitioner provides a limitation-by-limitation analysis alleging that Machnicki teaches or suggests each and every limitation of the claim and therefore renders claim 1 unpatentable for obviousness. Pet. 20–30. We have reviewed Petitioner’s contentions and supporting evidence regarding the currently undisputed limitations of claim 1, and are satisfied that the record establishes sufficiently for institution that Machnicki teaches or suggests these limitations.

As to the preamble³ (i.e., “[a] processor comprising”), we agree with Petitioner on this record and for institution that Machnicki’s integrated circuit constitutes a “processor” as recited in the preamble. *See* Pet. 20–21 (citing Ex. 1006, 4:9–25, Fig. 1; Ex. 1002 ¶¶ 79–80). Specifically, Machnicki discloses an integrated circuit forming a system-on-a-chip (SoC) or application-specific integrated circuit (ASIC) coupled to a power supply that includes, *e.g.*, performance domains, processors, graphics circuitry, and memory. Ex. 1006, 4:9–25.

As to limitation 1[a], (i.e., “a plurality of cores including a first core operable at a first voltage and a first frequency”), we agree with Petitioner on this record that Machnicki’s integrated circuit satisfies this claim

³ Neither party takes a position on whether the preambles to the claims are limiting. At this stage of the proceeding, we accept Petitioner’s showing that the preambles are taught by the prior art, without deciding whether the preambles are limiting.

limitation. *See* Pet. 21–23 (citing Ex. 1006, 1:20–26, 4:16–25, 5:37–40, 10:55–57; Ex. 1002 ¶¶ 81–83). For this limitation, Petitioner relies on an annotated version of Machnicki’s Figure 1, which we reproduce below:



Id. at 22. Figure 1 depicts Machnicki’s integrated circuit 100. In its annotated version of Figure 1, Petitioner highlights processor 160A in red and processor 160F in blue. *Id.* We agree with Petitioner, on this record and for institution, that an ordinarily skilled artisan would have understood that these processors constitute a “plurality of cores” as claimed. *Id.* at 21–22 (citing Ex. 1006, 4:16–25, 10:55–57; Ex. 1002 ¶ 81); *see also* Ex. 1001, 1:20–26, 5:37–40 (stating that multicore processors that include multiple processor cores within a single integrated circuit were known in the art).

We also agree with Petitioner, on this record and for institution, that processor 160A constitutes “a first core” that is “operable at a first voltage and a first frequency” as claimed. Pet. 22–23 (citing Ex. 1002 ¶¶ 82–83). Machnicki teaches that “clock frequencies and voltages are configuration parameters that may be set for each of the performance domains (e.g. domains 1 through m).” Ex. 1006, 8:1–4. And, in Table 1, Machnicki lists

three performance domains (or cores), each having their own respective frequencies (f) and voltages (V). *Id.* at 8:8–17, Table 1.

b) Limitation 1[b]

We now turn to the disputed limitations. Limitation 1[b] recites “a second core operable at a second voltage independent of the first voltage and at a second frequency different from the first frequency.” Ex. 1001, 8:37–40. Petitioner contends that Machnicki’s processor 160F satisfies this limitation. Pet. 23–25 (citing Ex. 1002 ¶¶ 84–88; Ex. 1006, 4:16–25, 8:1–4, 8:8–17, 8:37–43, Fig. 1, Table 1). Petitioner points to Machnicki’s disclosure that “each performance domain” of Table 1 “may have its parameters changed *independently*” and that “*the frequencies in each frequency domain for any given state may be different from each other, and may be other than a multiple of each other.*” *Id.* at 25 (quoting Ex. 1006, 8:37–43).

In response, Patent Owner argues that “Machnicki does not disclose or suggest at least ‘a second core operable at a second voltage *independent* of the first voltage,’ as claimed.” Prelim. Resp. 13 (quoting Ex. 1001, 8:37–39). Patent Owner argues that, in Machnicki’s power management system, “*all* domains are adjusted to predefined frequencies and voltages whenever the integrated circuit [IC] changes performance states.” *Id.* (citing Ex. 1006, 8:1–10:7). Patent Owner argues that, whenever the voltage of processor 160A changes, the voltage of processor 160F also necessarily changes because the IC performance state changes. *Id.* (citing Ex. 1006, 10:46–52). Thus, Patent Owner argues, the second voltage is not *independent* of the first voltage. *Id.* at 13–14.

We have considered the parties’ respective arguments and evidence, and determine, on this record and for institution, that Petitioner has met the reasonable likelihood standard for moving forward with trial. As an initial matter, Machnicki expressly states that “by using a performance state table such as the one illustrated in Table I above, each performance domain may have its parameters *changed independently*.” Ex. 1006, 8:37–39 (emphasis added). This disclosure appears to contradict Patent Owner’s argument that the processing domains’ respective voltages cannot be changed independently in Machnicki’s power management system.

But even if Patent Owner’s characterization of Machnicki is correct, the dispute between the parties appears to become one of claim construction, and neither party has set forth a construction for limitation 1[b] at this stage of the proceeding. It is not clear to us, at least on this record, that the claim language “operable at a second voltage independent of the first voltage” requires that the second voltage be *set* independently of the first voltage, as Patent Owner argues.

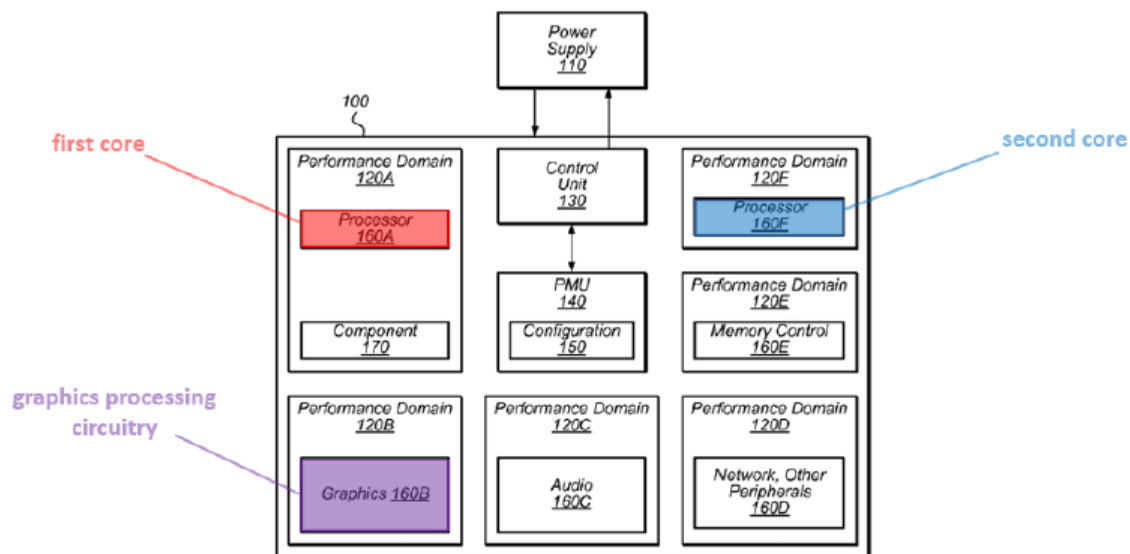
We note that, in claim 1, the second core must be operable at a second voltage *independent of* the first voltage, but a second frequency *different from* the first frequency. Normally, different claim terms are presumed to have different meanings, suggesting that “independent” and “different” should have different meanings. *See, e.g., CAE Screenplates Inc. v. Heinrich Fiedler GmbH & Co. KG*, 224 F.3d 1308, 1317 (Fed. Cir. 2000). But here, it appears—at least on this preliminary record—that the ’588 patent uses the terms “independent” and “different” interchangeably with respect to voltage and frequency. *Compare* Ex. 1001, 5:41–43 (stating that “each such core may be of an independent power domain and can be

configured to operate at an independent voltage and/or frequency”), *with id.* at 6:23–24 (stating that “[e]ach of domains 410 and 420 may operate at different voltage and/or power”).

For these reasons, we agree with Petitioner, on this record and for institution, that Machnicki's processor 160F satisfies limitation 1[b]. The parties are encouraged to further develop the record on claim construction if necessary.

c) *Limitation 1[c]*

Limitation 1[c] recites “graphics processing circuitry coupled to the plurality of cores to perform graphics operations, the graphics processing circuitry independently operable at a third frequency different from the first frequency and the second frequency.” Ex. 1001, 8:41–45. For this limitation, Petitioner relies on another annotated version of Machnicki’s Figure 1, which we reproduce below:



Pet. 26. In this annotated version of Figure 1, Petitioner highlights graphics unit 160B in purple. *Id.* Petitioner contends that graphics unit 160B constitutes the claimed “graphics processing circuitry” because Machnicki

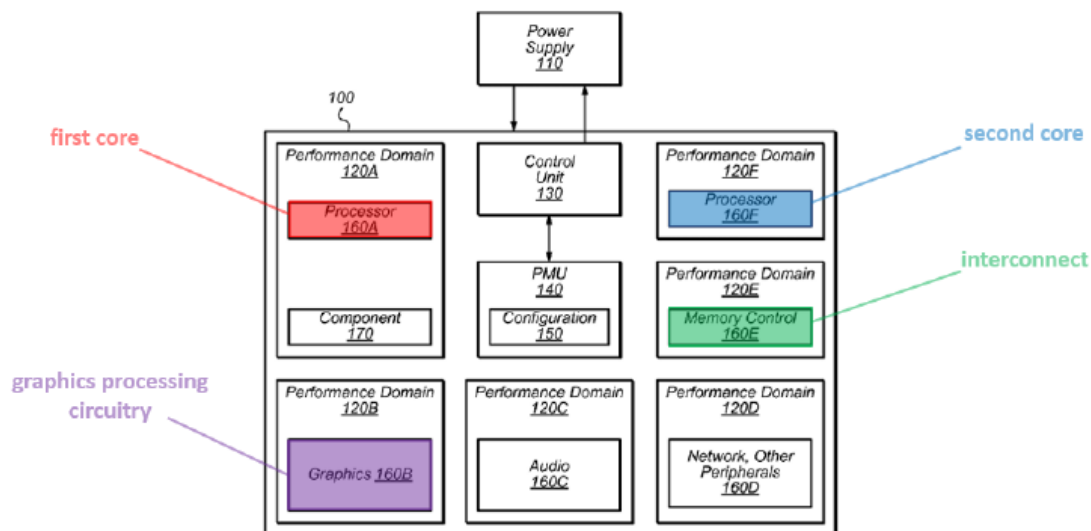
discloses that this component is “involved in the display of images on a display device,” *id.* (quoting Ex. 1006, 7:1–7), and because “Machnicki also discloses that ‘[c]omponents within integrated circuit 100 may be coupled to each other using any suitable bus and/or interface mechanism,” *id.* at 26–27 (quoting Ex. 1006, 4:31–33 (alternation in original); citing Ex. 1002 ¶¶ 91–92). Petitioner also contends that, for the same reasons discussed above as to limitation 1[a], an ordinarily skilled artisan would have understood that graphics unit 160B is “independently operable at a third frequency different from the first frequency and the second frequency.” *Id.* at 26–27 (citing Ex. 1006, 8:1–4, 8:8–17, 8:37–43; Ex. 1002 ¶¶ 93–94).

Patent Owner argues that Machnicki does not disclose or suggest limitation 1[c] for the same reasons it argues that Machnicki does not disclose or suggest limitation 1[b]. Prelim. Resp. 13–14. Specifically, Patent Owner argues that Machnicki’s graphics unit 160B is controlled by the same performance state table as processors 160A and 160F, and thus is not “independently operable at a third frequency” as claimed. *Id.* at 14.

For the same reasons discussed above, however, we are not persuaded on this record that the claim language requires that the graphics processing circuitry be *set* independently of the other processing cores. *Supra* § III.1.b. Indeed, limitation 1[c] appears to be even more removed from Patent Owner’s implicit construction, given that this limitation states that the *circuitry* is “independently operable” at a third frequency that is “different” than the first and second frequencies. And, as Petitioner points out, Machnicki expressly discloses that “the frequencies in each frequency domain for any given state may be different from each other.” Pet. 28 (quoting Ex. 1006, 8:37–43).

d) *Limitation 1[d]*

Turning to the final disputed limitation of claim 1, limitation 1[d] recites “an interconnect to couple the graphics processing circuitry to a memory device, the interconnect operable at a fourth frequency different from the first, second, and third frequencies.” Ex. 1001, 8:46–49. For this limitation, Petitioner relies on another annotated version of Machnicki’s Figure 1, which we reproduce below:



Pet. 28. In this annotated version of Figure 1, Petitioner highlights memory controller 160E in green. *Id.* Petitioner contends that the memory controller constitutes the claimed “interconnect,” *id.* at 29 (citing Ex. 1006, 7:30–34), and “acts to connect the other components within the integrated circuit to memory ‘using any suitable bus and/or interface mechanism,’” *id.* (quoting Ex. 1006, 4:31–33; citing Ex. 1002 ¶ 97). Petitioner contends that the memory controller “couple[s] the graphics processing circuitry to a memory device” as claimed, because “Machnicki discloses that ‘memory controller 160E may be configured to interface to one or more memory modules . . . that include one or more of the memories.’” *Id.* (quoting

Ex 1006, 7:21–30. Petitioner also contends that memory controller 160E is its own domain and, for the same reasoning and support asserted for limitation 1[a], an ordinarily skilled artisan would have recognized that memory controller 160E is operable at a frequency that is different from the other domains. *Id.* at 30 (citing Ex. 1006, 8:8–17, 37–43; Ex. 1002 ¶¶ 99–100).

In response, Patent Owner argues that “Machnicki does not render obvious at least ‘an interconnect to couple the graphics processing circuitry to a memory device’ as claimed.” Prelim. Resp. 14 (quoting Ex. 1001, 8:46–47). Patent Owner argues that Machnicki does not, in fact, disclose a bus (or “interconnect”) within memory controller 160E and that Petitioner’s contention that memory controller 160E “not only contains such an internal bus, but also that the undisclosed bus connects the components in the claimed manner” represents impermissible hindsight. *Id.* Patent Owner also argues that “Machnicki does not render obvious ‘the interconnect operable at a fourth frequency different from the first, second, and third frequencies.’” *Id.* at 16. Specifically, Patent Owner argues that Petitioner “fails to demonstrate that the alleged (undisclosed) *bus* within the Memory Control 160E (allegedly the claimed ‘interconnect’) would operate at a frequency different from the other components.” *Id.*

We have considered the parties’ respective arguments and evidence, and determine, on this record and for institution, that Petitioner has met the reasonable likelihood standard for moving forward with trial. As an initial matter, we agree with Petitioner and Dr. Mudge—on this record and for institution—that an ordinarily skilled artisan would have understood that Machnicki’s memory controller 160E must have a bus to perform the

disclosed functions of “queue[ing] memory requests from other components in integrated circuit 100, and/or to communicate with the other components to fulfill memory read and write operations.” Ex. 1006, 7:30–34; Pet. 29. Indeed, as Dr. Mudge explains, “interconnects and buses are commonly used in system components to interconnect the system to components such as a graphic processing circuitry, memory elements, system components, resources and custom circuitry.” Ex. 1002 ¶ 97. Machnicki also appears to support a finding that interconnects and buses were well known in the art by stating that components within the integrated circuit 100 “may be coupled to each other using any suitable bus and/or interface mechanism.” Ex. 1006, 4:31–33. In addition, we accept for institution the currently unrebutted testimony of Dr. Mudge that Machnicki’s “memory control circuit 160E is an interconnect,” Ex. 1002 ¶ 97, and that “[b]ecause the memory control circuit 160E is in its own domain, [an ordinarily skilled artisan] would have known the memory control circuit 160E is operable at a fourth frequency,” *id.* ¶ 99.

e) Claims 2, 4, 8, 9, 11, and 15–20

We have reviewed Petitioner’s contentions that Machnicki teaches or suggests the limitations recited in claims 2, 4, 8, 9, 11, and 15–20. Pet. 31–43. Patent Owner’s arguments about these claims generally do not go beyond its arguments as to claim 1. *See generally* Prelim. Resp. 16–17. On this record and for institution, we determine that Petitioner has shown sufficiently that Machnicki teaches or suggests the limitations of these claims.

f) Summary

Accordingly, for the reasons set forth above and based on the totality of the evidence currently in the record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 1, 2, 4, 8, 9, 11, and 15–20 of the ’588 patent as unpatentable for obviousness over Machnicki.

2. Alleged Obviousness of Claims 3, 7, 10, and 14 over Machnicki and Aguilar

Petitioner contends that claims 3, 7, 10, and 14 of the ’588 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Machnicki and Aguilar. Pet. 40–47. Briefly, Petitioner contends that the combination of Machnicki and Aguilar teaches or suggests each and every limitation of these claims, and that an ordinarily skilled artisan would have had a reason to combine the references with a reasonable expectation of success. *Id.*

Because we determined above that Petitioner demonstrated a reasonable likelihood of prevailing in its challenge to at least one claim of the ’588 patent, we institute *inter partes* review on all claims and grounds, including these claims (i.e., claims 3, 7, 10, and 14) and this ground. See 37 C.F.R. § 42.108(a) (“When instituting . . . review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.”). In this section, therefore, we will focus on Patent Owner’s arguments.

Taking claim 3 as illustrative, Patent Owner argues that Petitioner has not adequately shown that Machnicki’s “alleged cache would be included in a non-core power domain and further be shared by the plurality of cores” as claimed. Prelim. Resp. 21–22. At this stage of the proceeding, however, we

accept Dr. Mudge’s currently un rebutted testimony that an ordinarily skilled artisan would have characterized Machnicki’s memory controller 160E as a non-core power domain and would have understood—based on the disclosures of Machnicki and Aguilar—that utilizing cache for memory was well known in the art. Ex. 1002 ¶¶ 144–146; see also Ex. 1006, 4:31–33, 4:57–60, 5:18–20, 5:43–46, 7:30–34. Indeed, as Dr. Mudge testifies, it was well known in the art that utilizing cache memory “makes retrieving data from a computer’s memory more efficient.” Ex. 1002 ¶ 146. We further accept for institution Dr. Mudge’s testimony that Machnicki’s memory controller shares cache with other components because, for example, the memory controller “communicate[s] with other components to fulfill memory read and write operations.” Ex. 1006, 7:30–34; Ex. 1002 ¶ 145; Pet. 47.

Patent Owner also argues that Petitioner has failed to provide an adequate rationale for combining Machnicki with Aguilar. Prelim. Resp. 17–21. For example, Patent Owner argues that Petitioner’s rationale for the combination is based on hindsight, and that, because Machnicki already addresses thermal throttling, there would be no reason for the ordinarily skilled artisan to look to Aguilar. *Id.* at 19. But we understand Petitioner’s argument as to claim 3 to be that an ordinarily skilled artisan would have understood—as evidenced by Aguilar—that “caches were common components of nearly all memory systems at the time of the ’588 patent.” Pet. 47 (citing Ex. 1002 ¶ 146). Thus, a skilled artisan implementing Machnicki’s memory controller would have been motivated to provide cache as memory. In this regard, we accept for institution Dr. Mudge’s currently un rebutted testimony that including a cache makes retrieving data from a

computer's memory more efficient. Ex. 1002 ¶ 146; *see also* Pet. 47.

Finally, Patent Owner's arguments for claims 7, 10, and 14 rely on the same arguments Patent Owner presented for claim 3. Prelim. Resp. 12. These arguments are not persuasive on this record for the reasons discussed immediately above. Thus, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 3, 7, 10, and 14 of the '588 patent as unpatentable for obviousness over Machnicki and Aguilar.

3. *Alleged Obviousness of Claims 5, 6, 12, and 13 over Machnicki and Shakkarwar*

Petitioner contends that claims 5, 6, 12, and 13 of the '588 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Machnicki and Shakkarwar. Pet. 49–57. Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claims 5, 6, 12, and 13 on this ground of unpatentability, and therefore will focus on Patent Owner's arguments below.

Claims 5, 6, 12, and 13 are directed to various features of the claimed “second power management circuitry and/or logic.” *See, e.g.*, Ex. 1001, 8:62–65 (claim 5). Taking claim 5 as illustrative, Petitioner contends that “Machnicki in view of Shakkarwar teaches that this power management circuitry would have been implemented to include a mapping of selectable frequencies of the graphics processing circuitry to selectable frequencies of the interconnect.” Pet. 51–55 (citing Ex. 1002 ¶¶ 154–160). Petitioner contends that Shakkarwar teaches utilizing a look-up table containing a list of clock speeds to determine the appropriate bandwidth for a component (e.g., a graphics controller), while also taking into consideration the clock

speeds of other active components, such as the data controller (or “interconnect”). *Id.* at 53–54 (citing Ex. 1008, 6:63–7:10, Fig. 4; Ex. 1002 ¶ 159). Petitioner contends that an ordinarily skilled artisan would have been motivated to include Shakkarwar’s look-up table in Machnicki’s power management system because “Shakkarwar teaches that an advantage to its system is that it dynamically ‘manag[es] power consumption of electronic devices while satisfying bandwidth requirements for communicating and/or processing information.’” *Id.* at 54–55 (quoting Ex. 1008, 2:34–39 (alternation in original)). Patent Owner argues, *inter alia*, that “Shakkarwar does not associate particular GPU frequencies with particular bus frequencies,” because monitoring “bandwidth for a component” is not the same as “mapping . . . selectable *frequencies of the* graphics processing circuitry.” Prelim. Resp. 24–25 (citing Ex. 1008, 7:7–10).

We have considered Patent Owner’s arguments, but determine that Petitioner’s arguments and evidence are sufficient at this stage of the proceeding. Shakkarwar expressly teaches that the look-up table “may include a list of *clock speeds*, and/or voltage levels required to process information for specific devices and/or groups of devices.” Ex. 1008, 7:7–10 (emphasis added). And, Dr. Mudge testifies without rebuttal on this record that an ordinarily skilled artisan would have understood that determining bandwidth using a look-up table that includes a list of clock speeds constitutes “mapping selectable frequencies” as claimed. Ex. 1002 ¶ 159. For these reasons, and because Patent Owner’s arguments for claims 6, 12, and 13 rely substantially on the same arguments Patent Owner presented for claim 5, Prelim. Resp. 26–27, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims

5, 6, 12, and 13 of the '588 patent as unpatentable for obviousness over Machnicki and Shakkarwar.

4. *Alleged Obviousness of Claims 1, 2, 4, 8, 9, 11, and 20 over Cho and Gold*

Petitioner contends that claims 1, 2, 4, 8, 9, 11, and 20 of the '588 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Cho and Gold. Pet. 58–87. Briefly, Petitioner contends that Cho explicitly discloses each and every limitation of claim 1, except for a second core operable “at a second *frequency* different of the first frequency.” *Id.* at 67–71. Petitioner contends that, although Cho discloses multiple cores, each receiving different clock signals from a clock control unit (e.g., “clk1” and “clk2”), Cho does not expressly disclose the specific operating frequencies of the clk1 and clk2 signals. *Id.* at 68–69 (citing Ex. 1005 ¶¶ 22, 35; Ex. 1002 ¶¶ 187–189). Petitioner contends that Gold, however, expressly teaches four different operating frequencies for processing cores. *Id.* at 70–71 (citing Ex. 1009 ¶¶ 5, 39, Figs. 5A–5B). At this stage of the proceeding, Patent Owner argues that an ordinarily skilled artisan would not have been motivated to combine the teachings of Cho and Gold, Prelim. Resp. 27–29, and that, even if combined, Cho and Gold do not disclose or suggest a second core “at least ‘operable . . . at a second frequency different from the first frequency’ as claimed, *id.* at 29–30 (alternation in original).

Having considered the arguments and evidence before us, we find that the record establishes a reasonable likelihood that Petitioner would prevail on this asserted ground of unpatentability. Nevertheless, we recognize that the issues in dispute are highly fact-intensive and implicate genuine issues of fact more appropriately resolved on a fully developed record.

a) *The claim limitations*

Starting with the claim limitations, and taking claim 1 as illustrative, Petitioner contends that Cho teaches each and every limitation of claim 1 except for except for the portion of limitation 1[b] reciting a second core operable “at a second *frequency* different of the first frequency.” Pet. 67–71. As to the remaining limitations of claim 1, we have reviewed Petitioner’s contentions and supporting evidence, and agree with and adopt Petitioner’s detailed mapping of: the preamble, *see id.* at 64–65 (citing Ex. 1005 ¶ 38, Fig. 4; Ex. 1002 ¶¶ 178–180); limitation 1[a], *see id.* at 65–67 (citing Ex. 1005 ¶¶ 21, 35, 37, Fig. 4; Ex. 1002 ¶¶ 181–184); limitation 1[b] (relating to voltage), *see id.* at 67–68 (citing Ex. 1005 ¶¶ 21, 38, 40, Fig. 4; Ex. 1002 ¶¶ 185, 187); limitation 1[c], *see id.* at 73–75 (citing Ex. 1005 ¶¶ 22, 35, 38, Fig. 4; Ex. 1002 ¶¶ 198–204); and limitation 1[d], *see id.* at 76–78 (citing Ex. 1005 ¶¶ 22, 35, 38, Fig. 4; Ex. 1002 ¶¶ 205–211).

Turning to the portion of limitation 1[b] relating to frequency, we have reviewed Petitioner’s contentions and are satisfied on this record and for institution that the combination of Cho and Gold teaches “a second core operable . . . at a second frequency different from the first frequency” as claimed. *See id.* at 68–71 (citing Ex. 1002 ¶¶ 188–189). Specifically, Cho discloses multiple cores, each receiving different clock signals from a clock control unit (e.g., “clk1” and “clk2”). *See* Ex. 1005 ¶ 35 (“Clock control unit 310 is coupled to receive a system clock signal (clk) and to provide separate clock signals to each of the functional units (e.g., clk1 to a first functional unit, clk2 to a second functional unit, and so forth).”). While Cho does not expressly disclose the specific operating frequencies of those signals, Gold expressly teaches different operating frequencies for different

processing cores. *See* Ex. 1009 ¶ 5 (stating that, “[i]n one embodiment, an apparatus includes a plurality of processing cores (each of which has a respective standard operating frequency)”).

We have considered Patent Owner’s argument that the combination of Cho and Gold does not teach limitation 1[b]. Prelim. Resp. 29–30. Patent Owner’s arguments, however, are directed to the individual teachings of Cho and do not take into consideration what the combined teachings of Cho and Gold would have suggested to an ordinarily skilled artisan. *See, e.g., id.* at 29 (arguing that Cho does not disclose operating functional units at different frequencies). Patent Owner’s arguments are therefore not persuasive on this record. *See In re Merck & Co.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986) (the proper test for obviousness is what the references, taken as a whole, would have suggested to the ordinarily skilled artisan).

b) Motivation to combine/reasonable expectation of success

We now turn to motivation to combine/reasonable expectation of success. Briefly, Petitioner contends that an ordinarily skilled artisan would have had a reason to combine Cho and Gold with a reasonable expectation of success, *see, e.g.,* Pet. 71–73, whereas Patent Owner disputes Petitioner’s contentions, *see* Prelim. Resp. 27–30. We have reviewed Petitioner’s contentions and supporting evidence and determine, on this record and for institution, that Petitioner has met the reasonable likelihood standard for moving forward with trial.

Specifically, on this record, we agree with Petitioner that Cho suggests that each core is operable at a different frequency given that each core receives a different signal setting the frequency—e.g., clk1 sets the

frequency for core 1 whereas clk2 sets the frequency for core 2—and Cho states that “a change in the clock frequency for a clock signal provided to one functional unit need not affect the frequencies of the respective clock signals provided to other ones of the functional units.” Ex. 1005 ¶ 22; *see also id.* ¶ 35; Pet. 68–69; Ex. 1002 ¶¶ 188–189. And while Cho does not expressly disclose the specific frequencies of clk1 and clk2, we agree with Petitioner, on this record, that Gold expressly discloses different operating frequencies (in GHz) for different cores. *See, e.g.*, Ex. 1009 ¶ 5, Figs. 5A–5B.

We further agree with Petitioner, on this record, that an ordinarily skilled artisan seeking additional information on the specific operating frequencies on the clk signals, would have looked to Gold, which expressly discloses that information. *See* Pet. 71–72. Indeed, both references relate to controlling lowering operating frequencies. Ex. 1005 ¶¶ 24, 33, 36; Ex. 1009, Fig. 7. And, as Dr. Mudge testifies without rebuttal, ordinarily skilled artisans were well aware of the predictable correlation between temperature and frequency. *See, e.g.*, Ex. 1002 ¶ 170.

c) Summary

Accordingly, for the reasons set forth above and based on the totality of the evidence currently in the record, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing in its challenge to claims 1, 2, 4, 8, 9, 11, and 20 of the ’588 patent as unpatentable for obviousness over Cho and Gold.

5. *Alleged Obviousness of Claims 3, 7, 10, and 14–19 over Cho, Gold, and Aguilar*

Petitioner contends that claims 3, 7, 10, and 14–19 of the ’588 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Cho, Gold, and Aguilar. Pet. 87–100. Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claims 3, 7, 10, and 14–19 on this ground of unpatentability. Patent Owner’s arguments about this particular ground of unpatentability appear to be substantially similar to those presented with respect to the above grounds, and are not persuasive on this record for the reasons discussed above. *See* Prelim. Resp. 31–37. Given the fact-intensive nature of the parties’ dispute, we will evaluate this ground on the record that is developed during trial.

6. *Alleged Obviousness of Claims 5, 6, 12, and 13 over Cho, Gold, and Shakkarwar*

Petitioner contends that claims 5, 6, 12, and 13 of the ’588 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Cho, Gold, and Shakkarwar. Pet. 101–104. Again, in light of 35 U.S.C. § 314(a), we institute *inter partes* review of claims 3, 7, 10, and 14–19 on this ground of unpatentability. Patent Owner’s arguments about this particular ground of unpatentability appear to be substantially similar to those presented with respect to the above grounds, and are not persuasive on this record for the reasons discussed above. *See* Prelim. Resp. 37–39. Given the fact-intensive nature of the parties’ dispute, we will evaluate this ground on the record that is developed during trial.

IV. CONCLUSION

After considering the arguments presented in the parties’ papers and the evidence of record, we determine that Petitioner has demonstrated at

least a reasonable likelihood of success in proving that at least one claim of the '588 patent is unpatentable. Thus, we institute an *inter partes* review of all challenged claims on all grounds set forth in the Petition. Our determinations at this stage of the proceeding are based on the evidentiary record currently before us. This decision to institute trial is not a final decision as to patentability of any claim for which we have instituted an *inter partes* review. *See TriVascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016) (noting that “there is a significant difference between a petitioner’s burden to establish a ‘reasonable likelihood of success’ at institution, and actually proving invalidity by a preponderance of the evidence at trial”). We will base any final decision on the full record developed during trial.

V. ORDER

Accordingly, it is

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review is instituted for claims 1–20 of the '588 patent on the unpatentability grounds asserted in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial, which commences on the entry date of this decision.

IPR2023-00547
Patent 10,705,588 B2

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