UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner

v.

GREENTHREAD LLC,
Patent Owner

U.S. PATENT NO. 8,421,195

Case IPR2023-TBD

DECLARATION OF TRAVIS BLALOCK, PH.D.

TABLE OF CONTENTS

I. BACKGROUND AND QUALIFICATIONS 4

II. MATERIALS AND OTHER INFORMATION CONSIDERED 8

III. UNDERSTANDING OF PATENT LAW 11

A. Claim Construction 11

B. Obviousness 11

C. Cumulativeness 14

IV. SUMMARY OF OPINIONS 15

V. OVERVIEW OF THE TECHNOLOGY 16

VI. THE '195 PATENT 19

A. Claims 19

B. Summary of the Specification 20

C. Summary of the Prosecution History 22

VII. LEVEL OF ORDINARY SKILL IN THE ART 23

VIII. CLAIM CONSTRUCTION 24

IX. OVERVIEW OF THE PRIOR ART 26

A. Payne 26

B. Sakai 28

C. Kawagoe 29

D. Wolf 30

X. SPECIFIC GROUNDS FOR PETITION 31

A. Ground I: 31

1. Independent Claim 1 31

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 59
3. Dependent Claims 4 and 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a linear gradient"; "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient." 61
4. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient." 64

B. Ground II 67

1. Independent Claim 1 67
2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 93
3. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein said drift layer is an epitaxial layer." 95
4. Dependent Claims 4 and 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a linear gradient"; "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient." 97
5. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient." 99

C. Ground III 101

1. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 102
2. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein said drift layer is an epitaxial layer." 105

D. Ground IV 107

1. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein said drift layer is an epitaxial layer." 107

E. Ground V 110

1. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer." 110

XI. CUMULATIVENESS 111

XII. CONCLUSION.....115

I, Dr. Travis Blalock, declare as follows:

1. My name is Travis Blalock.

2. I have been retained as an expert witness on behalf of Intel Corporation ("Intel" or "Petitioner") for the above-captioned Petition for Inter Partes Review ("Petition") of U.S. Patent No. 8,421,195 (the "'195 Patent") (Ex. 1001). I am being compensated for my time in connection with this Petition at my standard consulting rate of $450 per hour. My compensation is not affected by the outcome of this matter.

3. I have been asked to provide my opinions regarding whether claims 1-6 of the '195 Patent (the "Challenged Claims") are invalid as obvious to a person having ordinary skill in the art at the time of the alleged invention.

4. The '195 Patent issued on April 16, 2013, from Application No. 11/622,496, filed on January 12, 2007. The '195 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004.

5. I am not currently, and have not at any time in the past been, an employee of Intel. I have no financial interest in Intel.

I. BACKGROUND AND QUALIFICATIONS

6. I am currently an Associate Professor at the University of Virginia. I served as an Associate Professor from 1998 until 2013 when I moved to a non-resident Associate Professor position so I could lead a Handheld Ultrasound R&D team for Analogic, Inc. I earned my Bachelor of Science and Master of Science in

Electrical Engineering from the University of Tennessee at Knoxville in 1985 and 1988 respectively. I earned my Ph.D. from Auburn University in 1991. The primary emphasis of my doctoral research was CMOS analog and digital integrated circuit design.

7. From 1991 through August 1998, I worked at Hewlett Packard Laboratories, first as a Member of the Technical Staff, and then as a Principal Scientist. My work at Hewlett Packard Laboratories involved design and implementation of digital and analog integrated circuits. I was the principal architect and designer of integrated circuits having a diverse range of applications, including CMOS analog signal processing integrated circuits for mass storage devices and optoelectronic image acquisition and processing integrated circuits. I also have experience with software and custom design tools that allow for improved analysis, modeling, and simulation of integrated circuit analysis and design.

8. While I was employed at Hewlett-Packard Laboratories (now Agilent Laboratories) I was the lead designer on several mixed-signal CMOS chips. One of these was a massively parallel analog signal processing prototype integrated circuit [1]. The chip measures position with an accuracy of better than 100 μm over 10 inches by cross-correlating past and present images acquired by the integrated photo-array. The photodetector design was based on an understanding of dopant profiles and the resulting effects on detector sensitivity. This was incorporated into the

detection circuit design to optimize response. The chip has a 2048 element 25,000 frame/second photoreceiver array coupled with an analog signal processing cross-correlation array. The array performs a set of 9 nearest-neighbor cross-correlations between the two images at a total computation throughput of 1.5 billion operations per second. Over 100 million second generation versions of this chip have been sold and the architecture forms the core of most optical mice.

9. I was also the technical lead in the design of a 1024 x 768 silicon backplane ferro-electric liquid-crystal microdisplay. The chip also includes 1024 compact, offset-corrected column amplifiers and high-speed analog signal distribution. Both of the above chip designs were the highest density mixed-signal integrated circuits ever produced within Hewlett-Packard (at that time) and were fully functional at first silicon. I was also directly involved in the testing and verification of these chips in the laboratory.

10. At the University of Virginia, I led research in design of low-power mixed-signal integrated circuits. This work covered a broad range of application areas including medical ultrasound, subthreshold RFID for mobile health applications, wearable sensors, custom RFID for bio-tracking of plaque propagation, infrared imaging, cryptographic hardening, and sensors for CMOS process reliability.

11. More recently, I have led the development of a CMOS 600 channel low power medical imaging front-end integrated circuit. The chip simultaneously amplifies, filters, and digitizes signals from 600 independent ultrasound transducer elements. The chip development was part of an independent medical ultrasound startup (PocketSonics, Inc.) I founded which was acquired by Analogic, Inc in 2013. This work led to the development and release of a handheld medical ultrasound product by Analogic, Inc. This device was powered by a lithium-ion battery and included circuits to manage high peak currents, pulse-width modulation for controlled power delivery, charge management, and battery protection circuits.

12. I am currently a collaborator with the Integrated Electromagnetics, Circuits, and Systems Lab at the University of Virginia. In this group we design a variety of high frequency RF integrated circuits and merged RF/Optical circuits. Of particular interest are low power wake-up receivers, clock recovery, and high efficiency power amps for battery powered RF circuits.

13. I have written widely in the field of electrical engineering, including several editions of a textbook that is used across the world to teach principles of microelectronic circuit design to undergraduate and graduate students. I have authored or co-authored over 50 journal and conference papers. My textbook includes discussions of the solid-state physics needed to understand the operation of semiconductor diodes, BJT transistors, and CMOS transistors. In the course of

integrated circuit design teaching and practice, particularly the low noise, high sensitivity circuits I have focused on, it has been essential to understand the device physics and how neighboring devices may interact to understand subtle effects that impact the success of both industrial and academic designs.

14. I have contributed to or consulted on the design, fabrication, and/or operation of integrated circuits, including microelectronic integrated circuits, for organizations such as Hewlett-Packard, NASA Langley Research Center, Agilent Technologies, Displaytech, PocketSonics, and Analogic.

15. I am a named inventor on at least 27 U.S. patents. Several of these concern analog circuitry or semiconductor design, including guard rings, charge storage devices, and photosensors.

16. My qualifications and publications are set forth more fully in my curriculum vitae, attached.

II. MATERIALS AND OTHER INFORMATION CONSIDERED

17. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art and have considered the viewpoint of a person having ordinary skill in the art (POSITA) at the time of the alleged invention.

18. I have considered the materials referenced herein, including the ’195 Patent (Ex. 1001), the file history of the ’195 Patent (Ex. 1002), the parent and

related applications, the file histories of the parent and related applications, the Petition, and other documents listed in the Exhibit List of the Petition, including:

Description	Date of Public Availability
U.S. Patent No. 4,684,971 to Payne ("Payne") (Ex. 1005)	Filed March 13, 1981 and issued August 4, 1987.
U.S. Patent No. 4,907,058 to Sakai ("Sakai") (EX. 1006)	Filed July 1, 1988 (with priority to July 3, 1987) and issued on March 6, 1990.
U.S. Patent No. 6,043,114 to Kawagoe, et al. ("Kawagoe") (Ex. 1007)	Filed on September 22, 1997 (with priority to July 28, 1995) and issued on March 28, 2000.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol 1, Lattice Press (2000) ("Wolf.1") (Ex. 1008A)	Published and publicly available no later than 2002.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 2, Lattice Press (2000) ("Wolf.2") (Ex. 1008B)	Published and publicly available no later than 2002.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 3, Lattice Press (2000) ("Wolf.3") (Ex. 1008C)	Published and publicly available no later than 2002.
Stanley Wolf and Richard N. Tauber, *Silicon Processing For The VLSI Era,* Vol. 4, Lattice Press (2000) ("Wolf.4") (Ex. 1008D)	Published and publicly available no later than 2002.
U.S. Patent No. 4,160,985 to Kamins *et al.* ("Kamins") (Ex. 1009)	Filed November 25, 1977 and issued July 10, 1979.
U.S. Patent No. 4,014,522 ("Jastrzebski") (Ex. 1010)	Filed March 24, 1982 and issued on November 6, 1984.
U.S. Patent Application Publication No. 2003/0042511 ("Rhodes") (Ex. 1011)	Filed on August 30, 2001.

Description	Date of Public Availability
U.S. Patent Application Publication No. 2002/0102783 ("Fujimoto") (Ex. 1012)	Filed on October 24, 2001 (with priority to October 26, 2000).
Wang and Agrawal, *Single Event Upset: An Embedded Tutorial*, 21st Intl Conf on VLSI Design, IEEE 2008 ("Wang") (Ex. 1013)	Published and publicly available in 2008.
U.S. Patent Application Publication No. 2004/0063288 ("Kenney") (Ex. 1022)	Published and publicly available in 2004.
Jaeger, *Introduction to Microelectronic Fabrication*, Vol. V, Addison-Wesley Modular Series on Solid State Devices (1988) ("Jaeger") (Ex. 1023)	Published and publicly available in 1988.
U.S. Patent No. 4,435,896 ("Parrillo") (Ex. 1025)	Filed on June 29, 1983 (with priority to December 7, 1981) and issued on March 13, 1984.
L.C. Parrillo, R.S. Payne et al., *Twin-Tub CMOS - A Technology for VLSI Circuits*, IEEE 1980 ("Parrillo2") (Ex. 1026)	Published and publicly available in 1980.
U.S. Patent Application Publication No. 2007/0045682 to Hong *et al*. ("Hong") (Ex. 1027)	Filed on August 31, 2005.
The Oxford American Dictionary and Language Guide, Oxford University Press (1996) (Ex. 1028)	Published and publicly available in 1996.
U.S. Patent Application Publication No. 2003/0183856 to Wieczorek ("Wieczorek") (Ex. 1038)	Filed on October 29, 2002 (with priority to March 28, 2002).
Dictionary of Engineering, McGraw Hill (2003) (Ex. 1040)	Published and publicly available in 2003.
Rubin et al., *Ranges and Moments of Depth Distributions of Boron and Phosphorus Implanted into Silicon in the Energy Range 1.7 - 5.0 MeV with*	Published and publicly available in 1997.

Description	Date of Public Availability
an Eaton NV-GSD/VHE Implanter, IEEE 1997 ("Rubin") (Ex. 1041)	

19. The references listed above include prior art to the '195 Patent which is entitled to a priority date not earlier than September 3, 2004. Payne, Kawagoe, Sakai, and Wolf.1-4 (Exs. 1008A-D) were not cited.

III. UNDERSTANDING OF PATENT LAW

20. I am not an attorney. For purposes of this declaration, I have been informed about certain aspects of the law that are relevant to my opinions. My understanding of the law is as listed below.

A. Claim Construction

21. I understand that in an IPR petition filed after November 13, 2018, a claim must be construed under the *Phillips* standard. Under that standard, words of a claim are given their plain and ordinary meaning as understood by a POSITA at the time of invention, in light of the specification and prosecution history, unless those sources show an intent to depart from such meaning, as well as pertinent evidence extrinsic to the patent.

B. Obviousness

22. I have been informed and understand that a patent claim can be considered to have been obvious to a POSITA at the time the application was filed. This means that, even if all of the requirements of a claim are not found in a single prior art reference, the claim is not patentable if the differences between the subject

matter in the prior art and the subject matter in the claim would have been obvious to a POSITA at the time the application was filed.

23. I have been informed and understand that a determination of whether a claim would have been obvious should be based upon several factors, including, among others:

- the level of ordinary skill in the art at the time the application was filed;
- the scope and content of the prior art; and
- what differences, if any, existed between the claimed invention and the prior art.

24. I have been informed and understand that the teachings of two or more references may be combined in the same way as disclosed in the claims, if such a combination would have been obvious to a POSITA. In determining whether a combination based on either a single reference or multiple references would have been obvious, it is appropriate to consider at least the following factors:

- whether the teachings of the prior art references disclose known concepts combined in familiar ways, which, when combined, would yield predictable results;
- whether a POSITA could implement a predictable variation, and would see the benefit of doing so;
- whether the claimed elements represent one of a limited number of known design choices, and would have a reasonable expectation of success by a POSITA;
- whether a POSITA would have recognized a reason to combine known elements in the manner described in the claim;

- whether there is some teaching or suggestion in the prior art to make the modification or combination of elements claimed in the patent; and
- whether the innovation applies a known technique that had been used to improve a similar device or method in a similar way.

25. I understand that a POSITA has ordinary creativity, and is not an automaton.

26. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

27. I understand that prior art to the '195 Patent includes patents and printed publications in the relevant art that predate the Priority Date of the '195 Patent.

28. I understand that certain factors—often called "secondary considerations"—may support or rebut an assertion of obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the alleged invention, skepticism of those having ordinary skill in the art at the time of the alleged invention, unexpected results of the alleged invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field.

29. I further understand that there must be a nexus—a connection—between any such secondary considerations and the alleged invention. I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

C. Cumulativeness

30. I understand that, under 35 U.S.C. § 325(d), the Board may exercise its discretion to deny institution of inter partes review if the IPR petition presents the same or substantially the same prior art or arguments that were previously presented to the Patent Office.

31. When deciding whether to exercise its discretion to deny institution under 35 U.S.C. § 325(d), I understand the Board weighs several non-exclusive factors, including:

(a) the similarities and material differences between the asserted art and the prior art involved during examination;

(b) the cumulative nature of the asserted art and the prior art evaluated during examination;

(c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;

(d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;

(e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and

(f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

IV. SUMMARY OF OPINIONS

32. It is my opinion that claims 1-2 and 4-6 are disclosed or, at a minimum, rendered obvious by Payne (Ground I).

33. It is my opinion that claims 1-6 are rendered obvious by Sakai in combination with Kawagoe (Ground II).

34. It is my opinion that claims 2 and 3 are rendered obvious by Payne in combination with Wolf (Ground III).

35. It is my opinion that claim 3 is rendered obvious by Payne in combination with Parrillo (Ground IV).

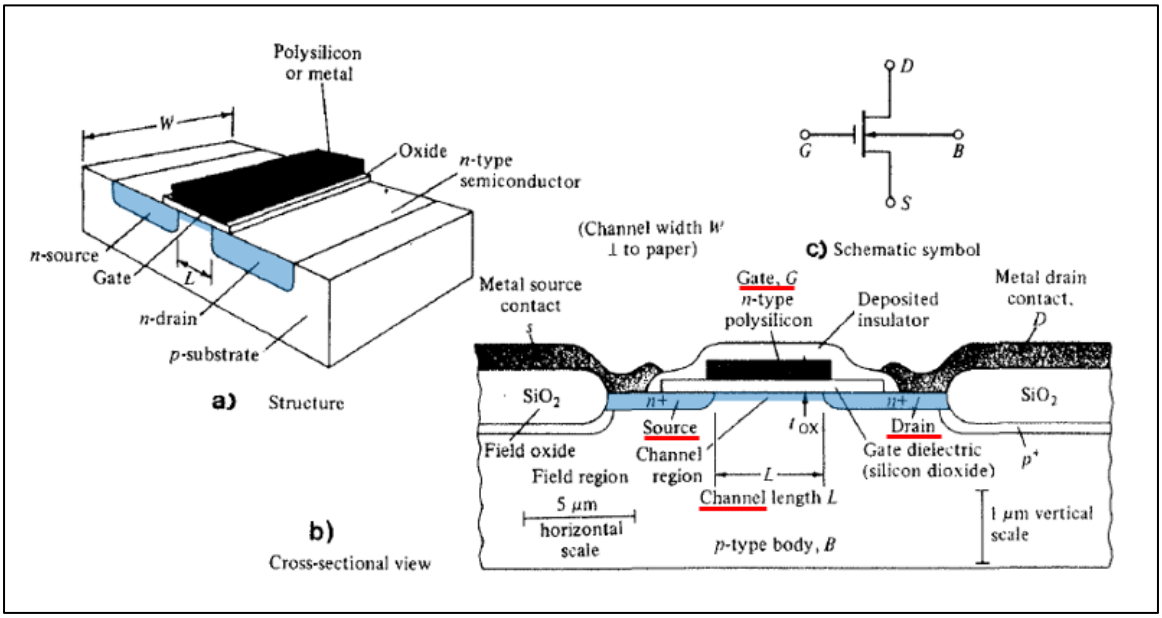
36. It is my opinion that claim 2 is rendered obvious by Sakai in combination with Kawagoe and Wolf (Ground V).

37. It is my opinion that none of the prior art references relied on in this petition are cumulative with prior art considered by the Examiner during prosecution of the '195 Patent.

38. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

V. OVERVIEW OF THE TECHNOLOGY

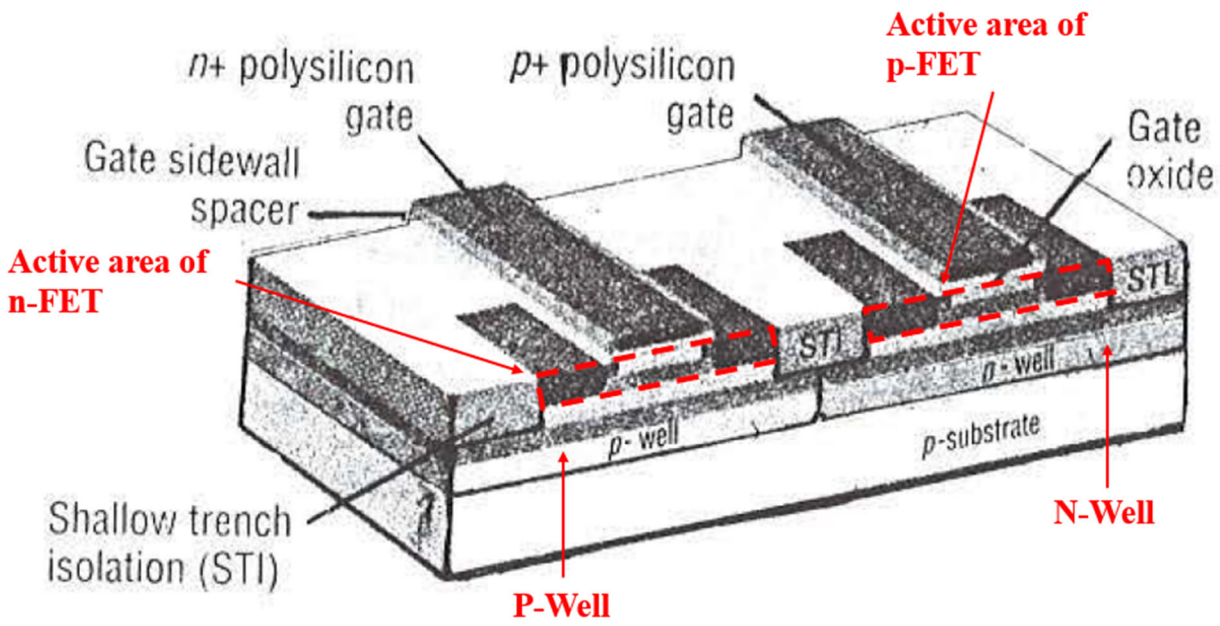
39. A Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is a transistor that switches from an OFF state to an ON state when a voltage is applied to a gate terminal. Ex. 1008B, 402. In the ON, or active state, current flows from a source to a drain through a channel region (the length of such channel region is labelled "L" below). The channel region is under the gate and gate oxide, and between the source and drain.



Ex. 1008B, FIG. 5-1 (annotations in red);[1] *id.*, 298-301, FIGS. 5-2, 6-4. The combination of the source, drain, and channel regions form the active region of a transistor. Ex. 1008B, 299-300 ("The top surface of the [substrate] body consists of active or transistor regions as well as passive or (field) regions. The active regions are those in which transistor action occurs; i.e., the channel and the heavily doped source and drain regions."), FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

40. MOSFETs are characterized by the material used in the source and drain. A MOSFET with source/drain regions made from "p-type" material in such areas (as shown in the figure above, labelled "p^+") is known as a PMOS or p-FET, while a MOSFET with source/drain regions made from "n-type" material ("n+") in such areas is known as a NMOS or n-FET. In the mid-1980s, Complementary MOS (CMOS) devices became popular, which have both PMOS (p-FET) and NMOS (n-FET) transistors on the same device. In such devices, the active areas (and associated transistors) are generally formed in regions called "wells," which have opposite dopant type to the dopants of the source/drain, as illustrated below.

[1] All emphases and annotations added unless otherwise noted.



Ex. 1008A, FIG. 16-28 (annotations in red).

41. Impurities known as "dopants" are added to the active areas and wells to add charge carriers and tailor the electrical properties of these regions such as their conductivity. Charge carriers can be electrons or holes. Ex. 1008C, 86. When a region is doped with p-type dopants, the holes are majority carriers and the electrons are minority carriers. Ex. 1008C, 86. When a region is doped with n-type dopants, the electrons are majority carriers and the holes are minority carriers. Ex. 1008C, 86.

42. A "dopant profile" refers to the "map" of concentration of dopants over a doped region and, in certain simplified scenarios, can be expressed as as a function of depth. For example, a dopant concentration that does not change with depth is a uniform concentration. A non-uniform dopant concentration that varies for example with depth, *e.g.*, increases or decreases with depth, is a non-uniform dopant

concentration called "graded." A graded dopant concentration that peaks at some depth of the doped region(s) instead of at the top or bottom of the doped region(s) is called "retrograde." In my opinion, all such doping profiles were known in the art.

VI. THE '195 PATENT

43. The '195 Patent issued on April 16, 2013, from Application No. 11/622,496, filed on January 12, 2007. The '195 Patent claims priority to Application No. 10/934,915, filed on September 3, 2004. Ex. 1001, cover.

A. Claims

44. The '195 Patent has 14 claims, including two independent claims numbered 1 and 8. Ex. 1001, 4:12-5:5. Claims 1-3 and 5-6 are the Challenged Claims.

45. Exemplary Claim 1 is reproduced below:

> **1.** A CMOS Semiconductor device, comprising:
>
> a surface layer;
>
> a substrate;
>
> an active region including a source and a drain, disposed on one surface of said surface layer;
>
> a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate, said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and
>
> at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second

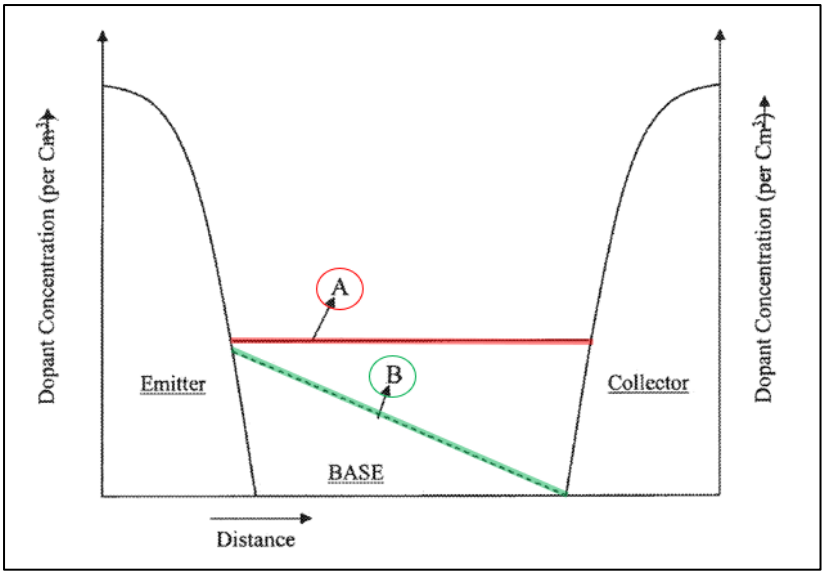
> static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate.

Ex. 1001, 4:13-29.

B. Summary of the Specification

46. The ’195 Patent is directed to “grading the dopant concentration” in certain regions of a semiconductor device. Ex. 1001, Title, Abstract. The Challenged Claims claim that a single drift layer and a well region of a semiconductor device have graded dopant concentrations to aid movement of minority carriers from the surface layer to the substrate. *Id*., Cl. 1. I understand that those claims are asserted against CMOS products in the District Court Case. In my opinion, the references relied on in the Petition (*i.e.*, Payne, Sakai, Kawagoe, and Wolf) are also directed to CMOS devices and technology.

47. The ’195 Patent admits that graded dopant concentrations were known. For example, the graded dopant concentration “B” (green) in Figure 1 below is described as one of “the two most popular” doping profiles used in prior art bipolar transistors, in contrast to the uniform doping profile “A” (red). Ex. 1001, 2:13-15.



Id., FIG. 1 ("Prior Art").[2] The '195 Patent further admits that it was known to grade the dopant concentration in well regions of CMOS devices to affect the movement of carriers, but alleges, without support, that prior attempts were met with "little success." *Id.*, 1:34-2:5.

48. The '195 Patent explains that "[r]etrograde wells have been attempted, with little success, to help improve soft error immunity in SRAMs and visual quality in imaging circuits." Ex. 1001, 1:59-61. The '195 Patent further states that "[r]etrograde and halo wells have also been attempted to improve refresh time in DRAM's (dynamic random-access memories), as well as, reducing dark current (background noise) and enhance RGB (Red, Green, Blue) color resolution in digital camera ICs." *Id.*, 1:64-2:2.

---

[2] All colors and colored annotations to figures added.

49. The ’195 Patent also explains that “these techniques” in the prior art “either divert the minority carriers away from the active regions of critical charge storage nodes at the surface, or, increase minority carrier density locally as the particular application requires.” *Id*., 2:2-5.

50. In my opinion, the only description of graded dopant concentrations and purported carrier movement in CMOS devices (the only types of devices accused of infringement in the District Court Case) in the ’195 Patent is in two paragraphs of the specification and associated Figures 5A-5C. Ex. 1001, 3:14-61, FIGS. 5A-5C.

51. In my opinion, the specification does not provide any guidance, such as dopant concentration ranges or doping gradients, on the grading of dopant concentration that would accomplish “aid[ing]” carrier movement in CMOS devices as recited in the Challenged Claims.

52. It is my further opinion that the specification does not provide any guidance as to the degree or nature of the “aiding” referenced in the Challenged Claims. Instead, the specification contrasts “graded channel[s]” with “uniformly doped channel (as practiced in the prior art).” *Id*. at 3:45-49. Thus, in my opinion, the specification uses “graded” dopant to describe a dopant concentration that is not uniform.

C. Summary of the Prosecution History

53. None of the references relied on in this Petition were discussed during prosecution and Payne, Sakai, Kawagoe, Wolf were not cited. I note that during prosecution, the Examiner found that the prior art, including Kamins and Jastrzebski, teaches all the elements of then-pending independent claim 10. Ex. 1002 (12/20/11 Office Action), 3–5; (8/13/12 Office Action), 3-5.

54. In response, Applicant amended claim 10 to add current Element [1.6] which recites "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants …." Ex. 1002 (10/15/12 Office Action Response), 3. The Examiner allowed the as-amended claim 10 (issued claim 1) and claims depending therefrom, citing this added element as the reason for allowance of these claims. Ex. 1002, (12/12/12 Notice), 2-3.

VII. LEVEL OF ORDINARY SKILL IN THE ART

55. I understand that there are multiple factors relevant to determining the level of ordinary skill in the pertinent art, including the educational level of active workers in the field at the time of the alleged invention, the sophistication of the technology, the type of problems encountered in the art, and the prior art solutions to those problems.

56. In determining the characteristics of a hypothetical person of ordinary skill in the art of the '195 Patent at the time of the alleged invention, I considered several things, including the type of problems encountered in this field, and the

rapidity with which innovations were made. I also considered the sophistication of the technology involved, and the educational background and experience of those actively working in the field, and the level of education that would be necessary to understand the '195 Patent. Finally, I placed myself back in the relevant periods of time, and considered the state of the art and the level of skill of the engineers working in this field in those times.

57. It is my opinion that a POSITA at the time of the '195 Patent would have had a Bachelors degree in electrical engineering, material science, applied physics, or a related field, and four years of experience in semiconductor design and manufacturing or equivalent work experience. Additional education might compensate for a deficiency in experience, and vice-versa.

58. I also note that my opinions provided in this Declaration would not change in view of any minor modifications to this level of skill.

VIII. CLAIM CONSTRUCTION

59. It is my opinion that for purposes of this proceeding, the claim terms need not be construed to resolve the prior art issues presented in this Petition.

60. Nothing in this section should be construed as expressing any opinion as to whether the claims constitute patentable subject matter under 35 U.S.C. § 101, or whether they satisfy the definiteness, enablement, best mode, or written description requirements under § 112.

61. I understand that the parties have proposed claim constructions in the District Court Case as set forth in the table below. Exs. 1029-1033. I further understand that in a tentative ruling in the Texas Case (in which Intel is no longer a party) issued in advance of the Markman hearing (canceled and not yet rescheduled), the District Court indicated that Patent Owner's plain-meaning constructions will likely be adopted. Ex. 1037.

Claim Term	Patent Owner's Proposed Construction	Petitioner's Proposed Construction
"surface layer"	Plain meaning ("a layer at the surface")	Indefinite
"substrate"	Plain Meaning ("an underlying layer")	"the initial material within which or on which the semiconductor device is fabricated"
"active region"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed")	"region that forms the current path of a device" or "the source, drain and channel region of a device"
"to aid the movement of minority carriers from … to …"	Plain Meaning	Indefinite Alternative Construction: "to sweep the minority carriers from … to …"
"well region"	Plain Meaning ("a doped region that surrounds the active region of a semiconductor device")	"A well, whether formed by single or multiple implants. Portions of a well are not well regions."

"active region … within which transistors can be formed"	Plain Meaning ("a doped silicon region at the surface of a semiconductor device where a transistor can be formed")	Indefinite

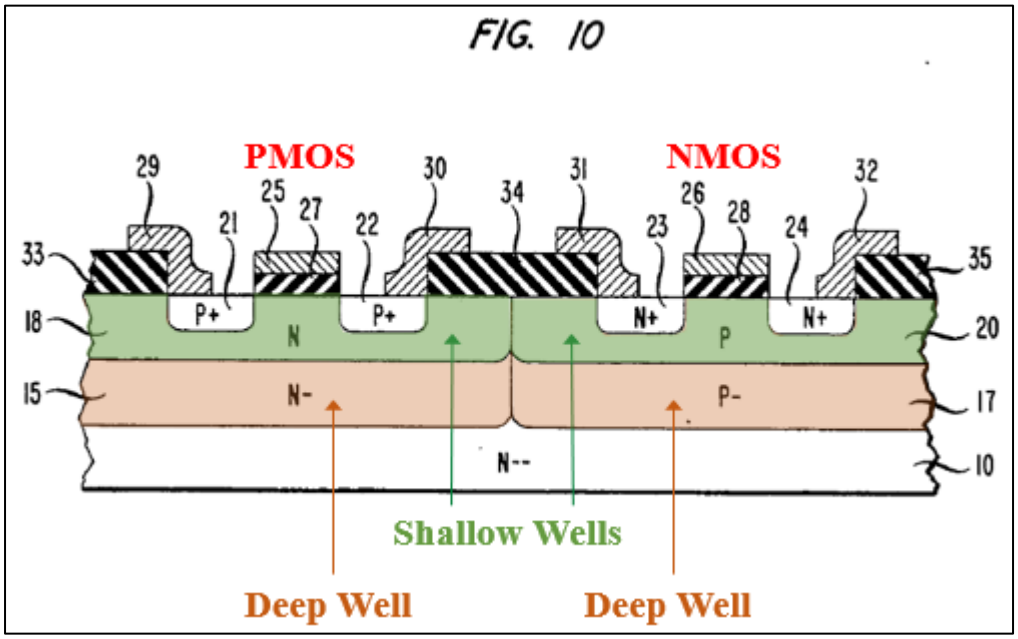
62. I support Petitioner's proposed constructions. However, I do not believe any terms need be construed to resolve the issues presented in this Petition because, in my opinion, as the Challenged Claims are unpatentable under either party's proposed constructions (except for "surface layer" which is addressed under Patent Owner's proposed construction). I reserve the right to respond to any purported claim constructions that Patent Owner raises.

IX. OVERVIEW OF THE PRIOR ART

A. Payne

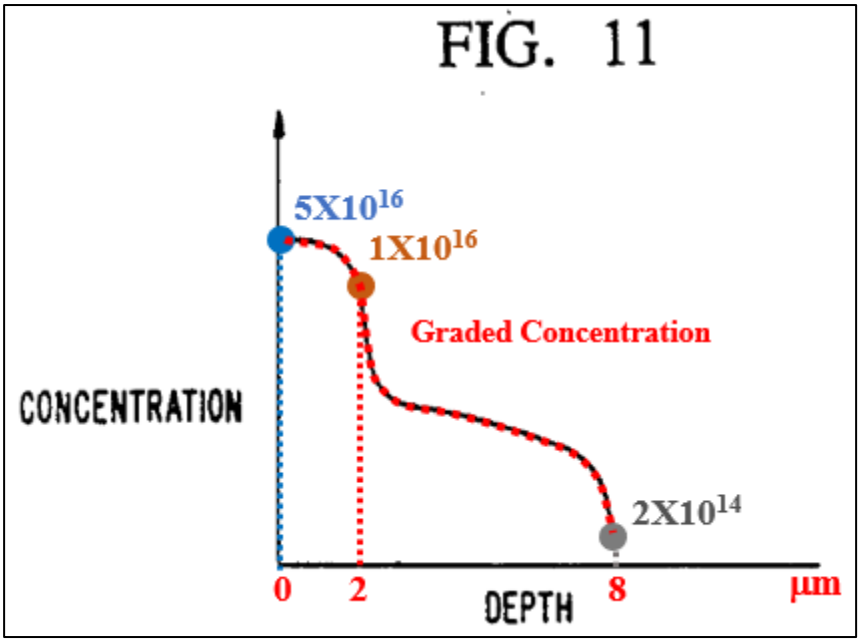
63. Payne discloses a "CMOS structure and method of manufacture ... for achieving a high packing density in integrated circuits." Ex. 1005, Abstract. CMOS devices comprise "n-channel" (NMOS) and "p-channel" (PMOS) transistors. *Id.*, 1:1-14, 5:18-27. According to Payne, the traditional CMOS fabrication processes using "single tub or twin tub approach[es]" (single-well or twin-well architecture) require source/drain regions of NMOS and PMOS transistors to be sufficiently spaced apart (*e.g.,* at least 12μm), which hinders high packing density. *Id*., 1:10-50.

64. Payne teaches forming a double-deck well structure, whereby shallow twin-wells (18 and 20) of "greater impurity concentration" are formed in deep wells (15 and 17), as shown below. *Id.*, 1:5-15, 1:51-2:2, 5:18-55, 6:35-51.



Id., FIG. 10; see also 2:3-28, 2:56-5:21, 5:44-50, FIGS. 2-9.

65. Payne further teaches that the double-deck well structure has a graded dopant concentration ("high-low implant profile") that decreases with depth, as shown below in Figure 11. *Id.*, 2:38-41, 5:14-17, 5:51-57 6:7-17, FIG. 11.

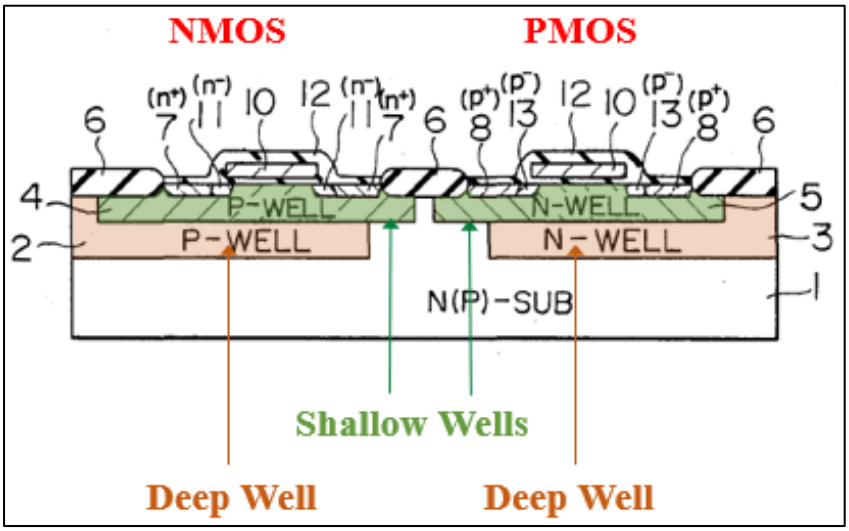


Id., FIG. 11 (annotated with exemplary maximum dopant concentrations at different depths disclosed in Payne); *id.*, 2:56-59, 5:48-55; *see also* Section X.A.1.e. Payne's double-deck well structure having the "high-low implant profile of FIG. 11" advantageously allows source and drain regions to be placed closer (*e.g.,* less than 5µm separation) resulting in "a high packing density." *Id.*, Abstract, 1:43-54, 5:56-6:20.

B. Sakai

66. Like Payne, Sakai discloses the use of a double-deck well structure ("twin double well structure") in CMOS devices to achieve high-packing density. Ex. 1006, 1:6-13, 1:55-2:5, 2:51-3:7, 7:19-37, 8:9-24. Figure 10 below illustrates Sakai's "twin double well structure," and shows "shallow P-well" 4 and "shallow

N-well" 5 (green) formed in a surface portion of "deep P-well" 2 and "deep N-well" 3 (tan), respectively. Ex. 1006, 1:53-2:39, 5:53-6:19.



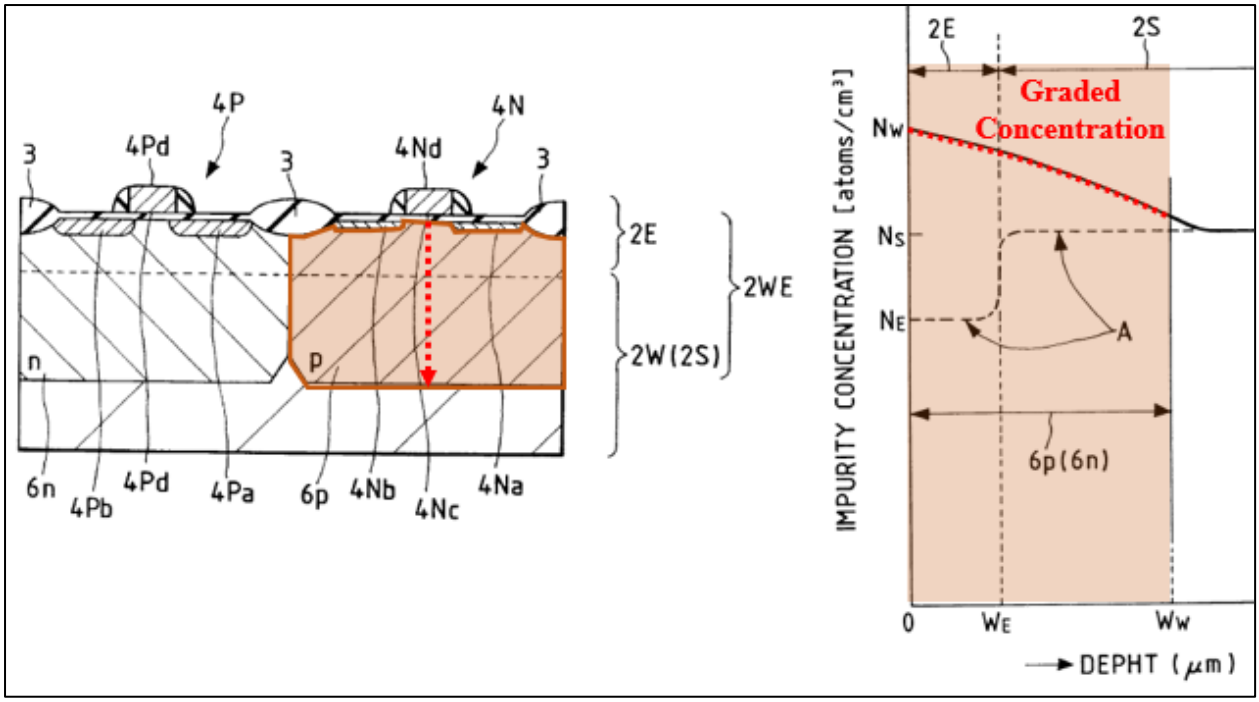
Id., FIG. 10D.

67. Sakai further discloses that the dopant concentration in the shallow wells is greater than the dopant concentration in the deep wells. *Id.*, 5:56-6:4.

C. Kawagoe

68. Kawagoe discloses a CMOS device in which wells have graded dopant concentrations that decrease with depth, as illustrated below right. *Id.*, 14:46-55, 15:26-40, 15:62-16:40 ("p-well 6p and n-well 6n have their impurity concentrations ***gradually lowered*** in the depthwise direction …").[3]

[3] All emphases added unless otherwise noted.



Id., FIGS. 17, 23 The graded dopant concentrations reduce soft errors by sweeping unwanted carriers into the substrate body. *Id*., 16:2-11 ("electrons produced by the α-ray are ***attracted to the substrate body 2S*** by that concentration gradient … so that the soft errors can be reduced ...").

D. Wolf

69. *Silicon Processing For The VLSI Era* by Stanley Wolf is a four volume textbook related to semiconductor devices, with particular focus on CMOS devices. Exs. 1008A-D. I am familiar with the Wolf textbook. An internet search for this textbook title limited to the ".edu" domain yields over 800 results. Thus, it is clearly used as a teaching resource in engineering courses in many, many universities and is widely cited in scientific works.

X. SPECIFIC GROUNDS FOR PETITION

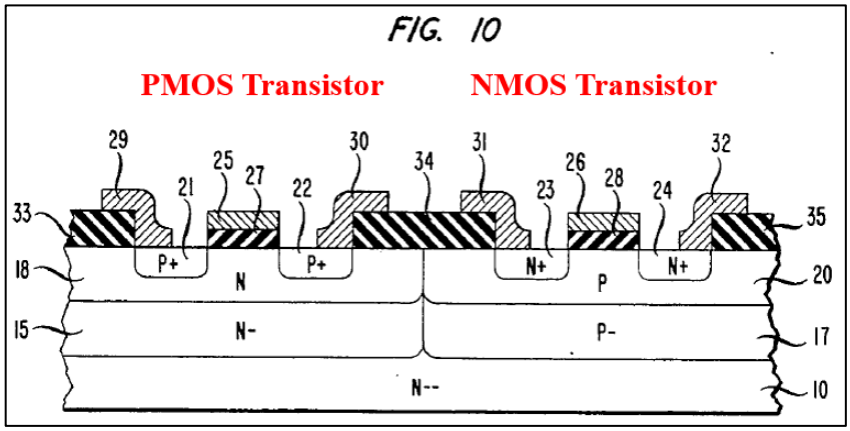
A. Ground I:

70. In my opinion, Payne renders claims 1-2 and 4-6 obvious.

1. Independent Claim 1

a. Preamble: "A CMOS semiconductor device comprising:"

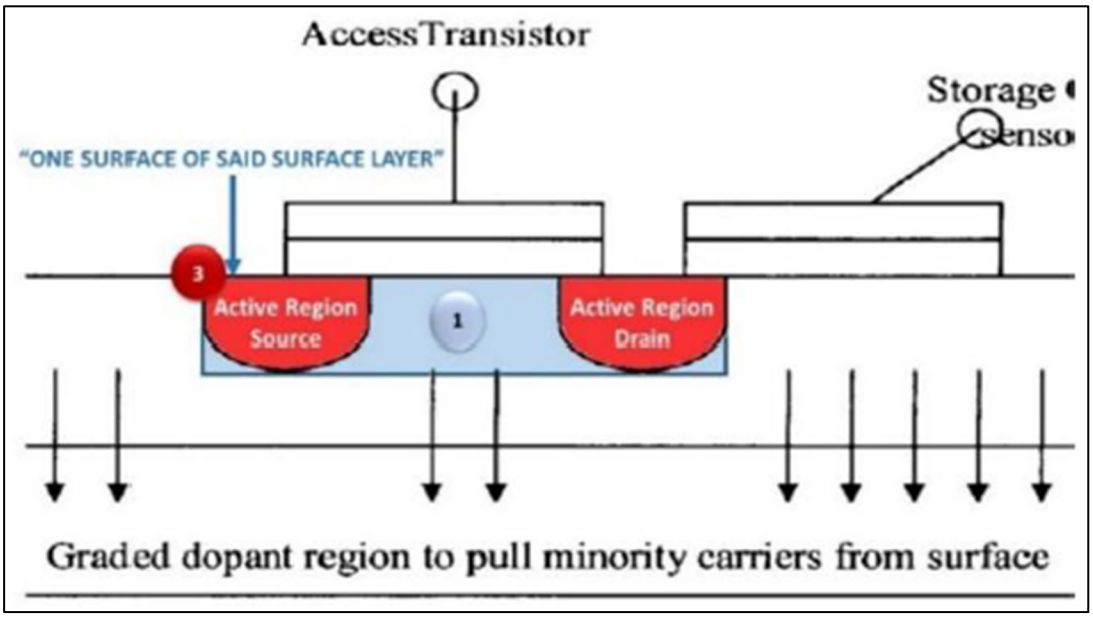
71. In my opinion, Payne discloses this element. Payne is directed to a CMOS semiconductor device. Ex. 1005, Title, Abstract, 1:51-54 ("it is a primary object of the invention to provide a CMOS structure and method of manufacture which requires little semiconductor space and therefore permits a high packing density."); 1:5-15. Payne Figure 10 illustrates a "p-channel" (PMOS) transistor (with "P+" source/drain regions 21/22) adjacent to an "n-channel" (NMOS) transistor (with "N+" source/drain regions 23/24) of a CMOS semiconductor device. *Id.*, 2:50-60, 5:18-34, 6:57-59.



Ex. 1005, FIG. 10.

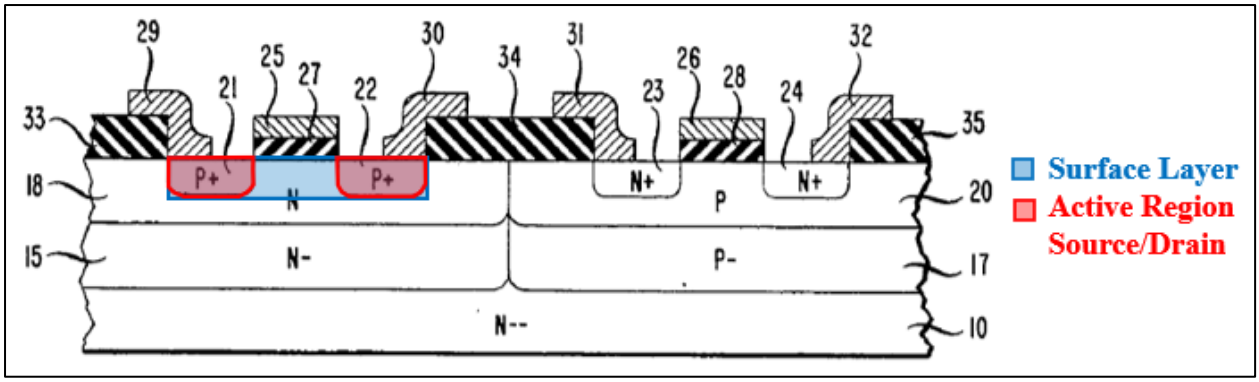
b. Element [1.1]: "a surface layer;"

72. In my opinion, Payne discloses, or at a minimum, renders obvious this element. According to Patent Owner, a "surface layer" is "a layer at the surface of the silicon" (or "a layer at the surface of the semiconductor device")—which Patent Owner annotated in blue below—"where the active region [(red)] is located." Ex. 1030, 6, 9, 12, 13; Section VIII.



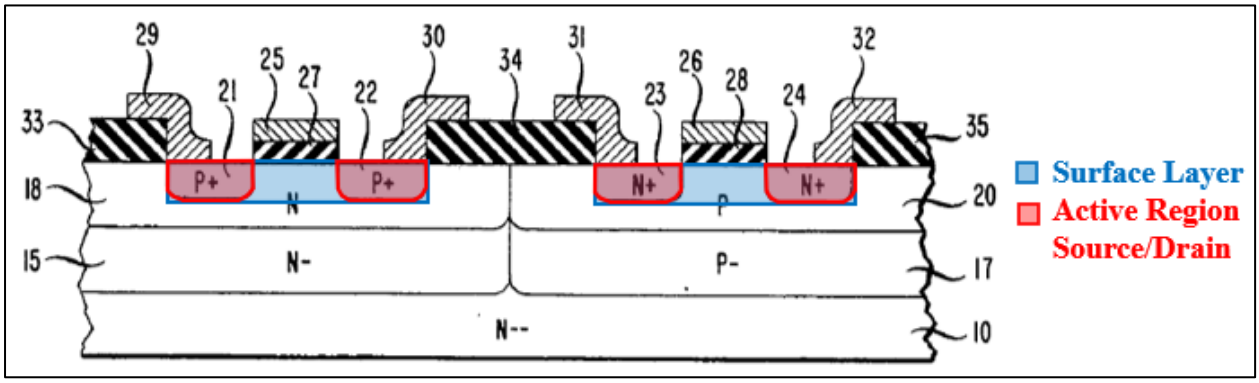
Ex. 1001, FIG. 5(b); Ex. 1030, 7, 12.

73. In my opinion, Payne satisfies element [1.1] to the same extent that Figure 5(b) meets it. Payne's Figure 10 discloses a surface layer (blue) that matches the surface layer Patent Owner identified in Figure 5(b). Payne's surface layer is at the surface of Payne's silicon substrate 10, and "source and drain regions, 21 and 22 [(red)] of P+ conductivity" of Payne's p-channel transistor (left) are located in it. Ex. 1005, 2:50-60; 5:21-27, 6:57-59, FIG. 1.



Ex. 1005, FIG. 10.

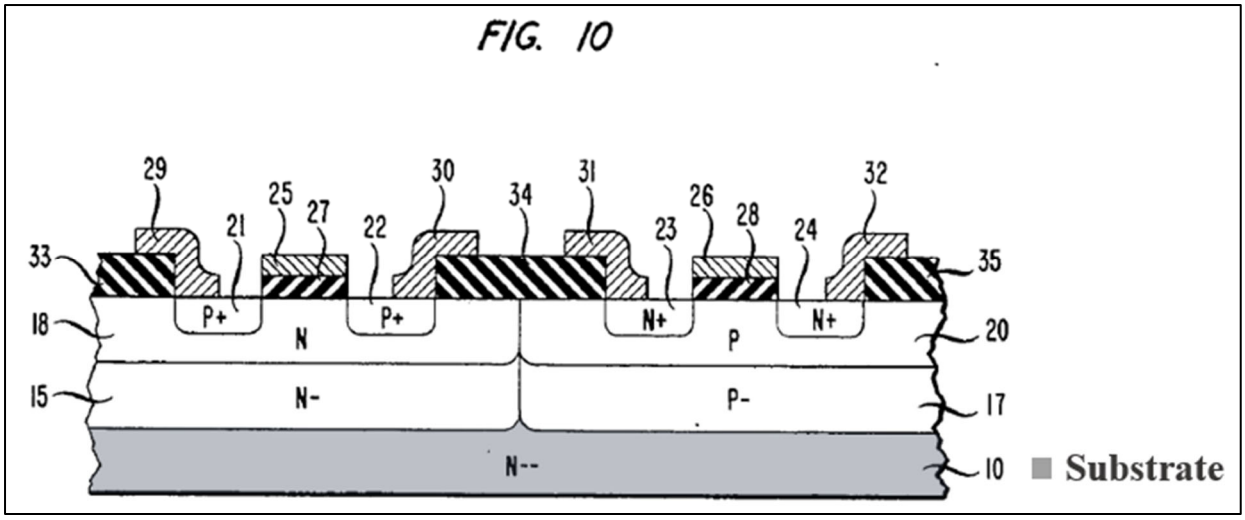
74. Payne likewise discloses a surface layer containing "source and drain regions, 23 and 24, of N+ conductivity" of Payne's n-channel transistor (right). *Id.*, 5:24-27, 6:57-59.



Ex. 1005, FIG. 10.

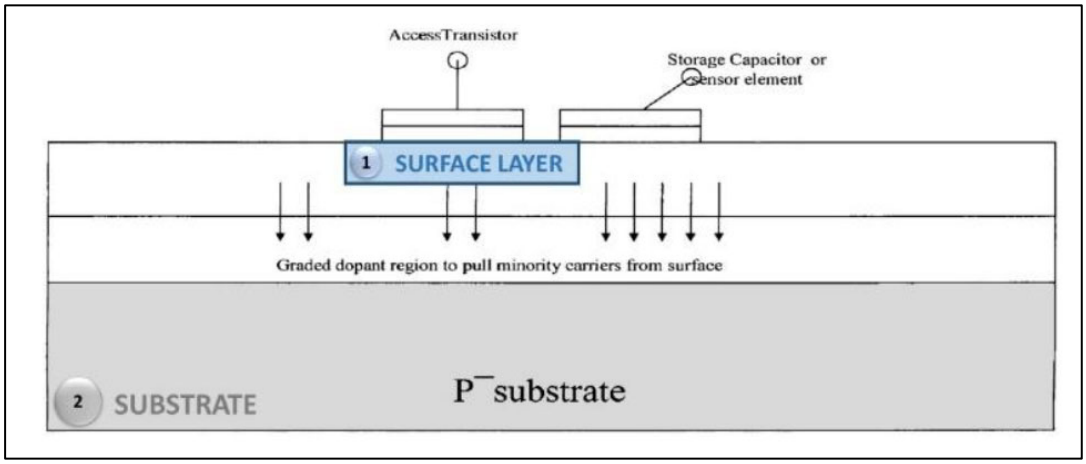
c. Element [1.2]: "a substrate;"

75. In my opinion, Payne discloses this element. Payne's Figure 10 illustrates a CMOS device "fabricated in a silicon semiconductor ***substrate*** [(grey)], 10 of 'N--' conductivity type which typically has a doping concentration of approximately 1-2x10^{14} ions/cm^3[.]" Ex. 1005, 1:60-62, 2:50-60.



Ex. 1005, FIG. 10.

76. In my opinion, Payne satisfies element [1.2] under Patent Owner's proposed construction of "plain and ordinary meaning, [*i.e.*] 'an underlying layer.'" Section VIII. Payne's substrate also matches Patent Owner's identification of the substrate (grey) in Figure 5(b) of the '195 Patent.

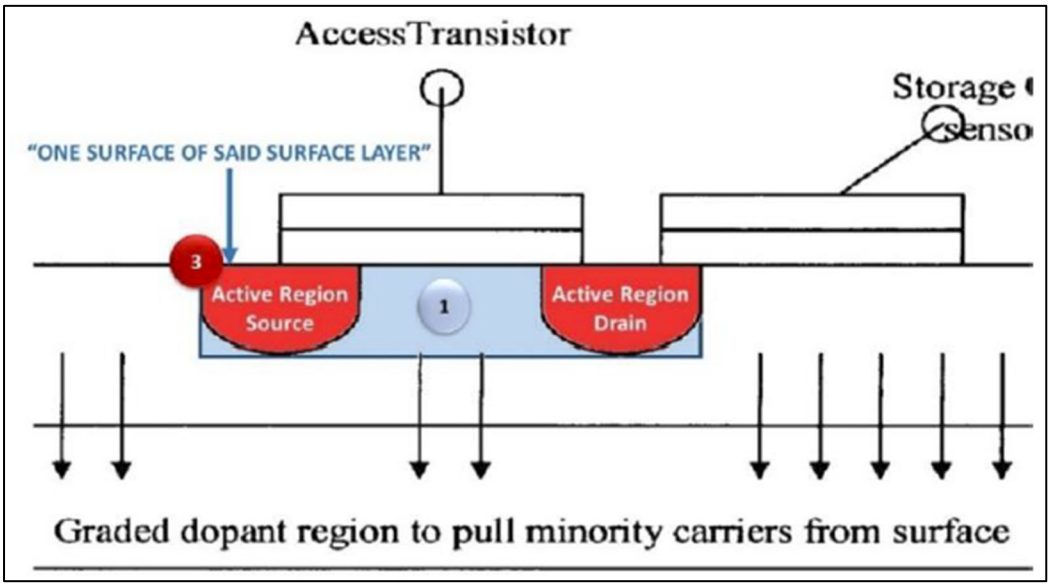


Ex. 1030, 6-7, 16-17 (well region and drift layer can be part of substrate); Ex. 1001, FIG. 5(b).

77. In my opinion, Payne also satisfies this element under Petitioner's proposed construction because Payne's substrate is "the initial material within which or on which the semiconductor device is fabricated." *See* Section VIII; Ex. 1005, 1:60-65, 2:50-60 ("the [CMOS] device is fabricated in a silicon semiconductor substrate, 10"), FIGS. 1, 10.

d. Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

78. In my opinion, Payne discloses or, at a minimum, renders obvious this element. According to Patent Owner, Figure 5(b) of the '195 Patent depicts an active region (red) "disposed on one surface [(top surface)] of said surface layer":



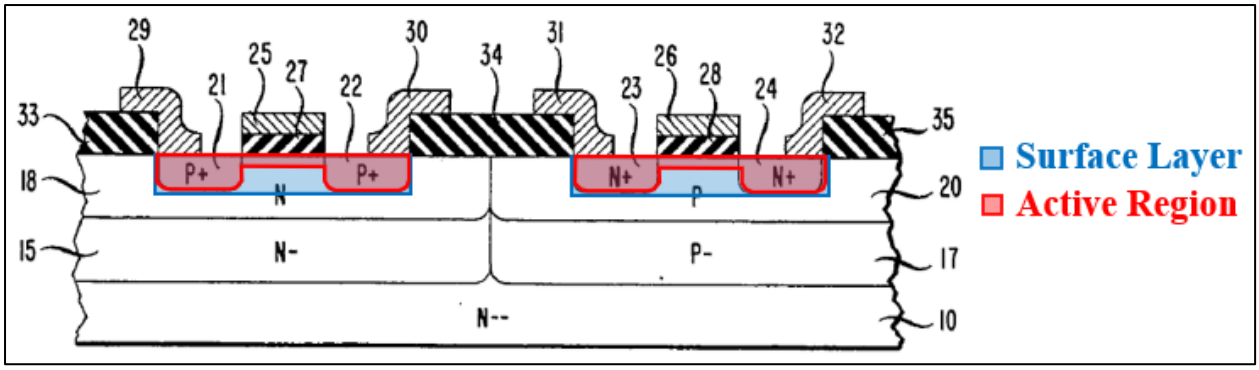
Ex. 1001, FIG. 5(b); Ex. 1030, 6-7, 11 ("[T]he 'active region' is part of the 'surface layer' … When the claim says the active region is 'disposed on one surface of the

surface layer,' it means the active region is located on the 'ceiling' of the silicon ***inside*** the silicon.") (emphasis in original), 12.

79. In my opinion, Payne satisfies element [1.3] under Patent Owner's interpretation. Payne's Figure 10 below illustrates a "p-channel" transistor with source/drain regions 21/22 (left), and an "n-channel" transistor with source/drain regions 23/24 (right). Ex. 1005, 5:18-29, 1:5-19, 6:57-59. These source/drain regions are formed with "a surface impurity concentration of approximately 10^{19}-10^{20} ions/cm^3." Ex. 1005, 5:21-29, 1:43-45.

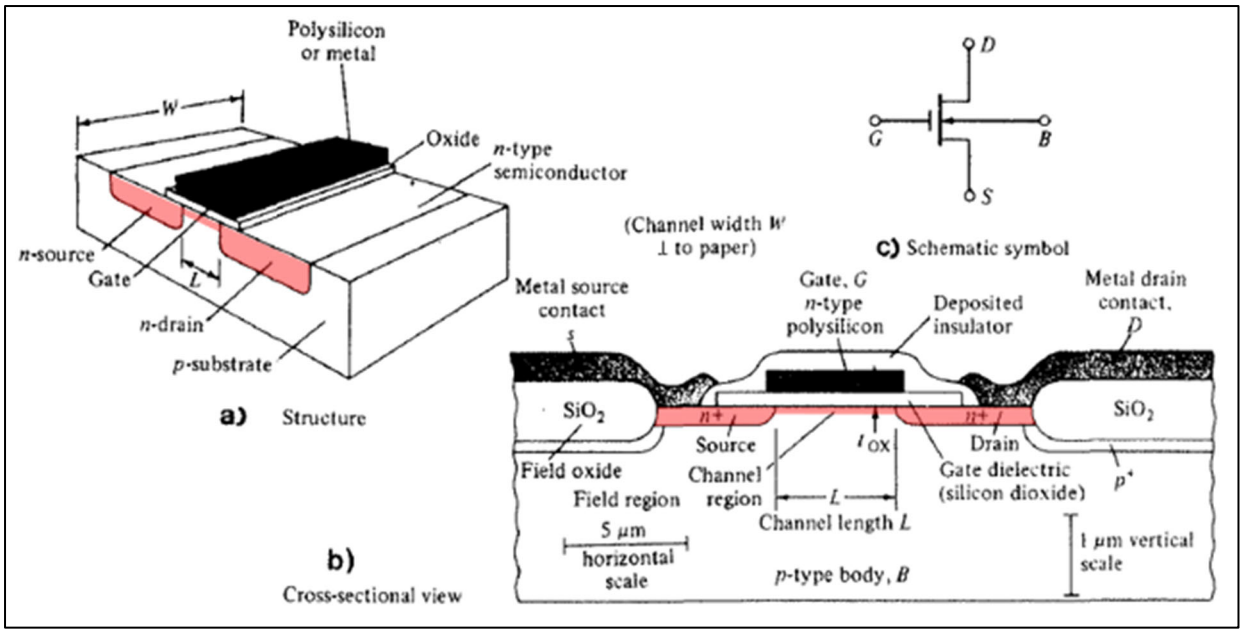
80. The channel region between these source/drain regions is part of the surface region, which has an impurity concentration of "typically 0.5-5X1016 ions/cm3." Ex. 1005, 5:51-52, 4:31-39, 4:63-5:5. The source/drain regions of a transistor, together with the channel region in between them, form an active region. Ex. 1008B, 299 ("The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

81. The active region (red) of each of Payne's transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner's annotated Figure 5(b) above. Section X.A.1.b.



Ex. 1005, FIG. 10.

82. In my opinion, Payne satisfies element [1.3] under Patent Owner's position that "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" (Section VIII) because the active region of a MOS transistor is "[its] channel and [its] ***heavily doped*** source and drain regions," highlighted in red below. Ex. 1008B, 299.



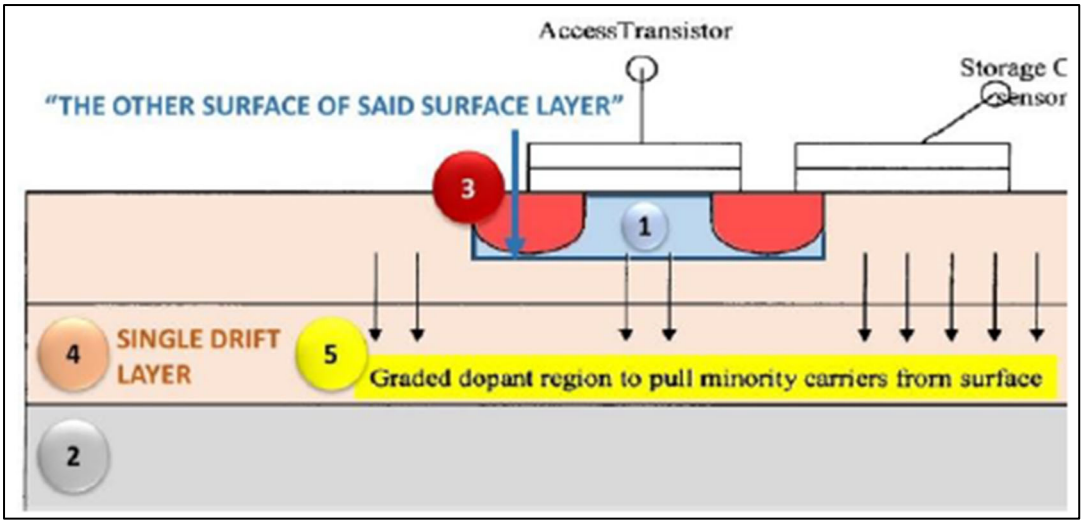
Ex. 1008B, FIG. 5-1; *id*., 298-301, 374, FIGS. 5-2, 6-4.

83. Payne also satisfies this claim element under Petitioner's proposed construction that an "active region" is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Section VIII; Ex. 1008B, 299-301, FIGS. 5-1, 5-2; Ex. 1008D, 197, FIG. 5-13. I note that Patent Owner does not dispute this. Ex. 1030, 3-4 ("when a positive voltage is applied to the gate … a conductive ***channel*** [is formed] between the ***source*** and the ***drain***, and ***current*** can begin to flow through the transistor").

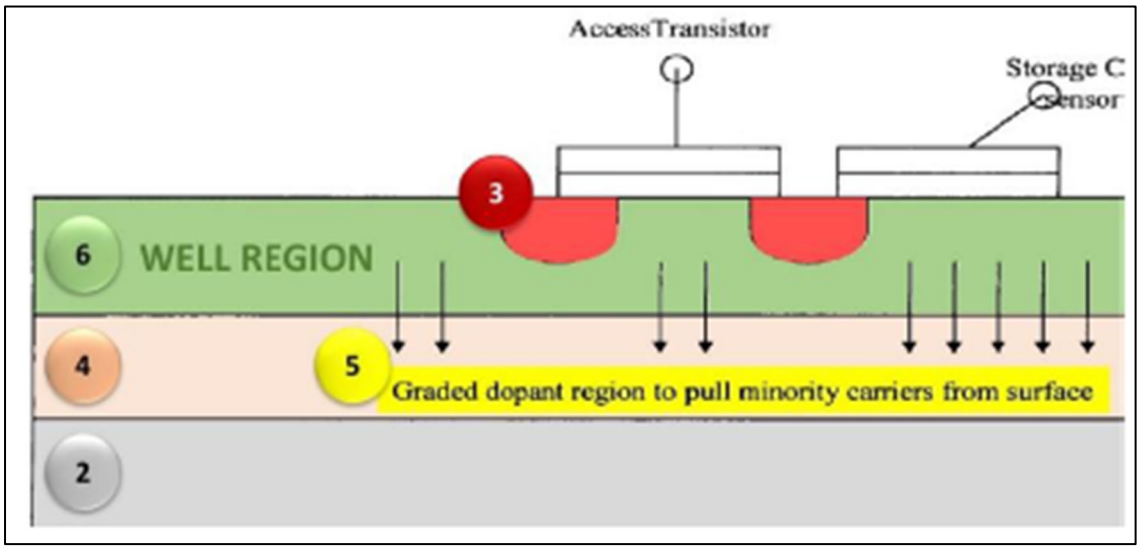
e. Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate,"

84. In my opinion, Payne discloses or, at a minimum, renders obvious this element.

85. **<u>Single drift layer</u>** – In its claim construction brief, Patent Owner identified the single drift layer in tan in Figure 5(b). Ex. 1030, 7. According to Patent Owner, the single drift layer (tan) is "disposed between 'the other surface [(bottom surface)] of said surface layer [(blue)]' and [said] substrate [(grey)]":



Ex. 1001, FIG. 5(b); Ex. 1030, 7. The single drift layer in Figure 5(b) has a well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [1.6]), and as shown below:

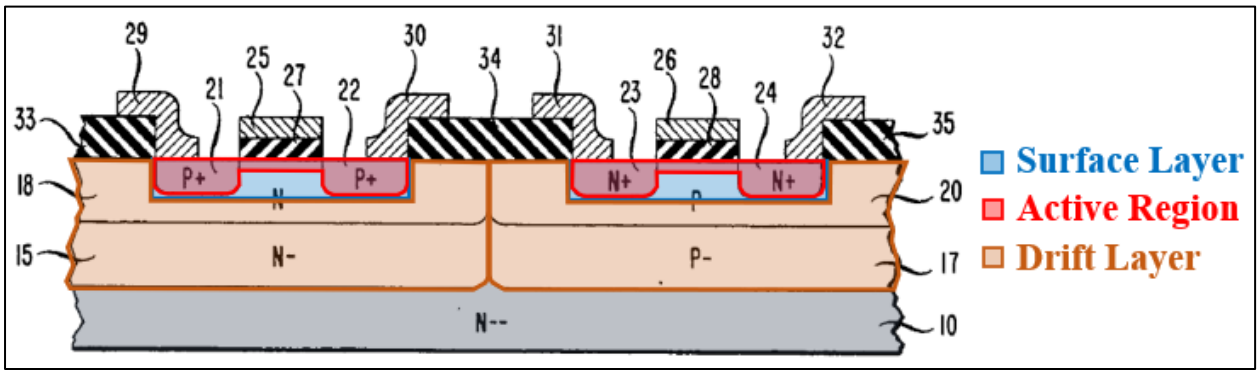


Ex. 1001, FIG. 5(b); Ex. 1030 at 7; *id.*, 11 ("the 'well region' is part of the 'single drift layer.'").

86. In my opinion, Payne discloses a single drift layer to the same extent the '195 Patent's Figure 5(b) does. In Payne's Figure 10, the **"first tub region" 15**

(tan) of Payne's nested well structure—with shallow well ("surface region") 18 disposed in it—is an example of the claimed single drift layer. *Id.*; Ex. 1005, 3:28-42 (ion implantation for tub 15), 4:19-30 (thermal drive-in to achieve the desired depth for tub 15), 4:31-39, 5:7-17, 5:44-48, 5:48-50 ("In a typical device, the final depth of surface regions 18 and 20 would be approximately 1-2μ and the depth of the ***tub regions 15 and 17*** would be typically 3-8μ.").

87. This single drift layer (tan) is "disposed between the other surface [(bottom surface)] of said surface layer [(blue)] and [said] substrate [(grey)]" under Patent Owner's interpretation, and in exactly the same way as depicted in Patent Owner's annotated Figure 5(b) above.



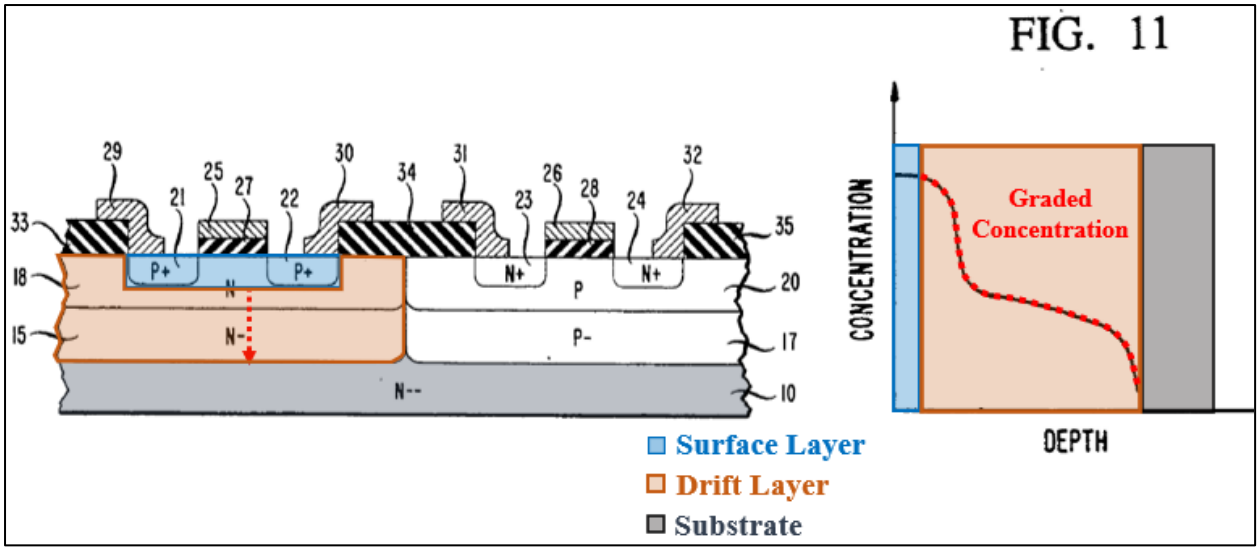
Ex. 1005, FIG. 10. Payne's tub 17 (right), in which shallow well 20 is disposed, is likewise a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). Ex. 1005, 4:3-30, 4:63-5:17, 5:44-50; Section X.A.1.b.

88. In my opinion, Payne meets all other claim requirements associated with the single drift layer to the same extent Figure 5(b) meets them. *See* below and

elements [1.5]-[1.6]. Notably, as detailed in element [1.5], each of Payne's tubs 15/17 is a ***single*** drift layer because it has a graded-dopant concentration that, according to Patent Owner, creates a unidirectional electric drift field that aids the movement of minority carriers in a ***single*** direction—from the surface layer to the substrate. Ex. 1030, 7; Ex. 1002, 253-54, 289-290; Section X.A.1.f.

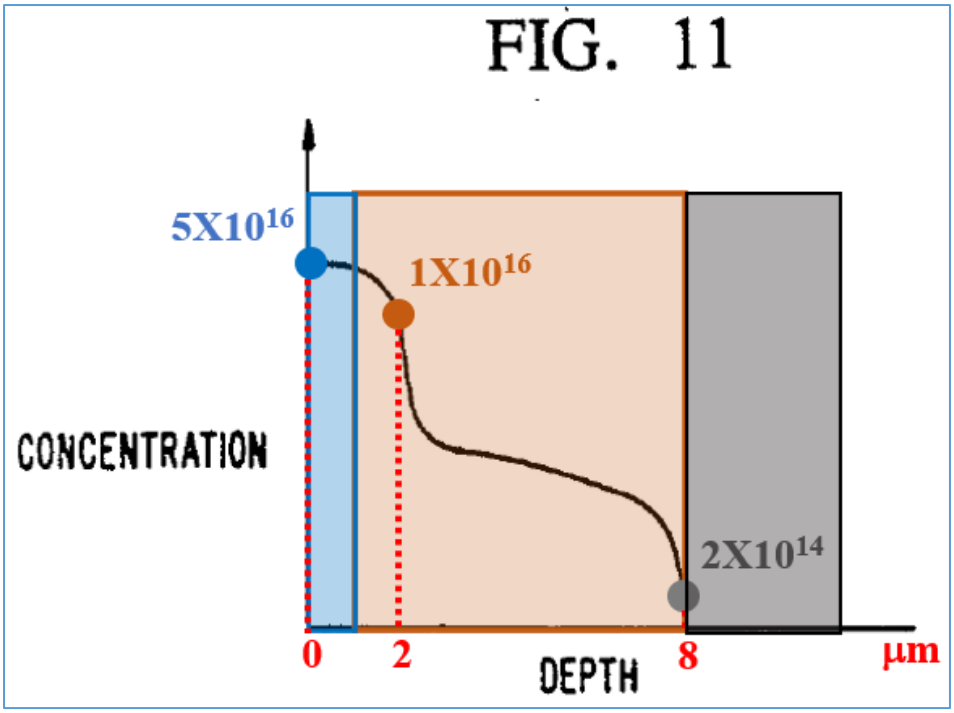
89. **Graded dopant concentration** – The '195 Patent admits that graded-dopant concentrations were known, Ex. 1001, 2:13-15, FIG. 1 ("Prior Art"), and that it was known to grade the dopant concentration in CMOS devices to affect the movement of minority carriers. *Id.*, 1:34-2:5, FIGS. 3(a)-3(d) (all "Prior art"). Payne's single drift layer has a graded-dopant concentration extending between the surface layer and the substrate. Payne explains that the "impurity profile in both tubs [15/17] thereby has the general shape illustrated in FIG. 11" which exhibits "[t]he major advantage" of a "***high-low implant profile***." Ex. 1005, 2:38-41, 5:14-17, 5:56-57.

90. Payne's Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left), which starts at the bottom of the surface layer (blue) and extends to the substrate (grey). As shown below, Payne discloses a downward-sloping graded-dopant concentration in the single drift layer (tan) associated with Payne's PMOS transistor (left).



Ex. 1005, FIGS. 10-11.

91. I have annotated Figure 11 to reflect exemplary (maximum) dopant concentrations at various depths disclosed in Payne: (1) **5X10^{16}** ions/cm^3 at the surface of the shallow wells (depth 0μm), (2) **10^{16}** ions/cm^3 at a depth of ~2μm (boundary of deep and shallow wells), and (3) **2X10^{14}** ions/cm^3 at a depth of ~8μm (boundary of substrate and deep wells).



Ex. 1005, FIG. 11.

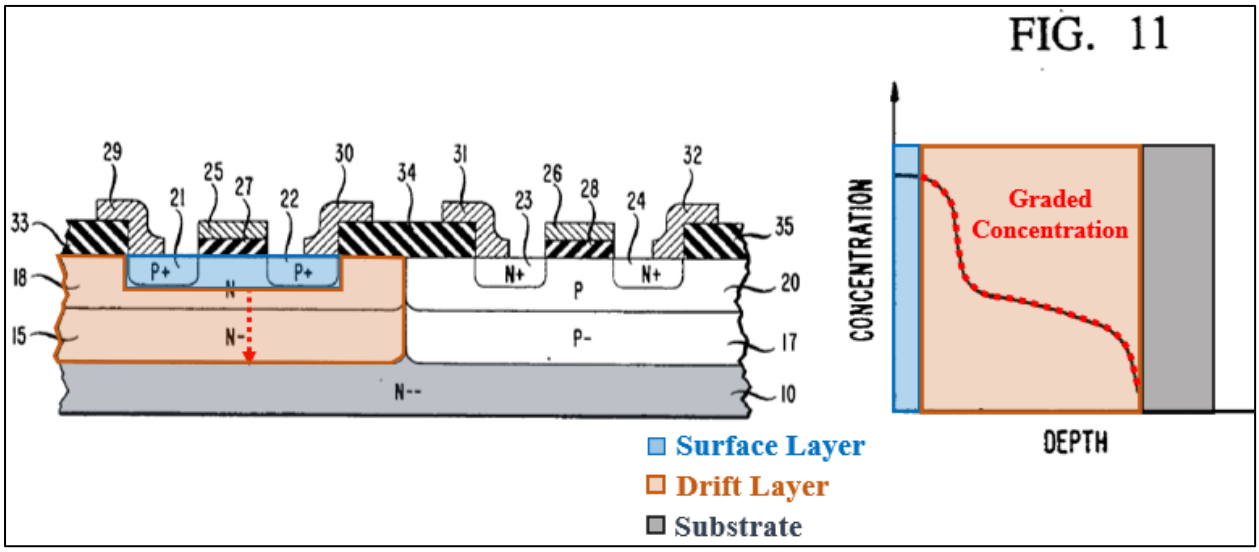
92. Payne explains that "[t]he surface impurity concentration of the surface regions [18/20] is typically **0.5-5X10^{16}** ions/cm^3 and that [the surface impurity concentration] of the tub regions [15/17] is typically **10^{15}-10^{16}** ions/cm^3, with the former concentration being ***at least twice as much*** as the latter over these ranges." *Id.*, 5:51-55. The concentration is lowest at the substrate, where it is "**1-2X10^{14}** ions/cm^3." *Id.*, 2:56-59. Payne also explains that "the final depth of surface regions 18 and 20 would be approximately 1-2µ and the depth of tub regions 15 and 17 would be typically 3-8µ." *Id.*, 5:48-50.

93. While the above discusses the single drift layer associated with Payne's PMOS transistor (left in Figure 10), Payne teaches that the single drift layer

associated with Payne's NMOS transistor (right) also has a downward-sloping graded dopant concentration. Ex. 1005, 5:14-17.

f. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

94. In my opinion, Payne discloses or, at a minimum, renders obvious this element. As shown below, Payne's single drift layer (tan) has a downward-sloping graded-dopant concentration extending between the surface layer (blue) and the substrate (grey). Section X.A.1.e.



Ex. 1005, FIGS. 10-11.

95. Payne's downward-sloping graded-dopant concentration aids the movement of minority carriers from the surface layer to the substrate to the same extent to which Applicant relied on the prior art and admitted to the Patent Office that such carrier movement would occur under the same scenario. During

prosecution, Applicant represented to the Patent Office that a downward-sloping graded-dopant concentration was known in the prior art to create an "inherent 'built-in' unidirectional electric field" that moves carriers deep into the substrate (while an upward-sloping concentration, not at issue in Payne, would move those carriers in the opposite direction towards the surface):

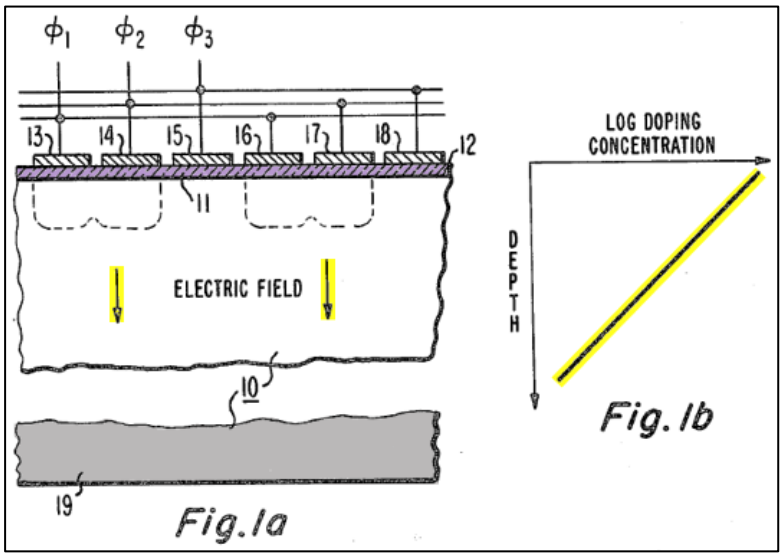
> [T]he graded dopant concentration itself creates a ***'built-in' electrical field*** that forces the movement of carriers into a particular direction, whereby ***the 'direction' of the electrical field and the resulting direction of the carrier movement depends solely on the slope of the graded concentration of dopant.***

Ex. 1002, 289-290 (underlining in original).

96. Applicant further represented that "a unidirectional drift (electric) field necessarily affects ***all*** the present minority carriers in the same way…. Depending on the particular slope of the graded concentration of dopant, ***all*** minority carriers are either ***swept*** 'down' … or 'up…'" Ex. 1002, 289. Applicant cited Jastrzebski in support. *Id.*, 290. In Jastrzebski, the graded-dopant concentration is "decreasing with depth" from the top surface 11 (purple) of the substrate 10, as shown in Figure 1b below. Ex. 1010, 5:14-22.

97. Jastrzebski teaches that this downward-sloping graded-dopant concentration creates an electric drift field that "force[s] most of the charge carriers

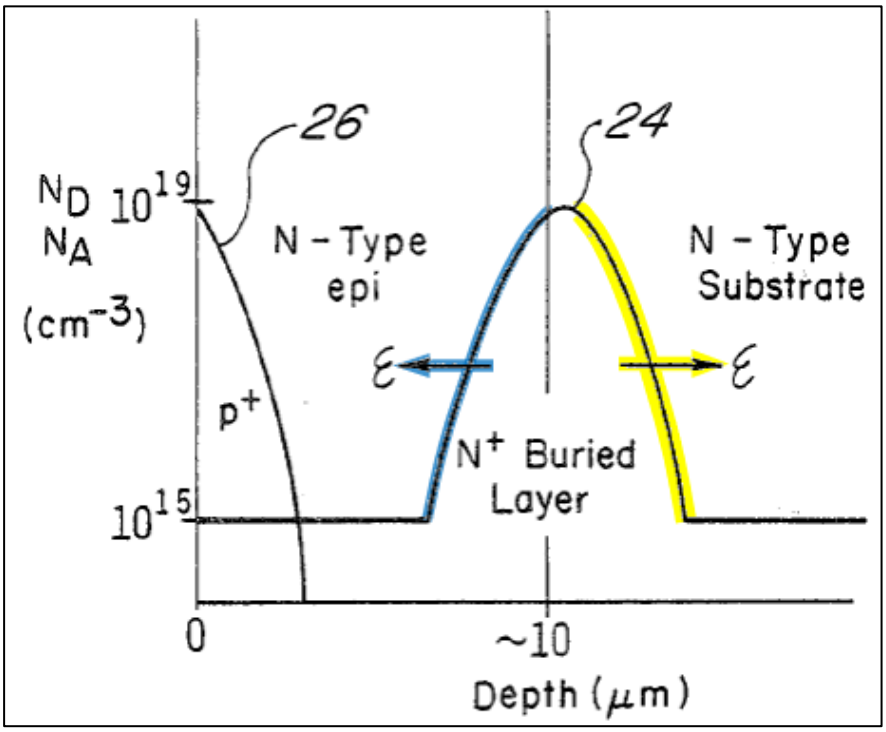
… ***deep into the substrate***[.]" *Id.*, 5:14-22; *Id.*, 2:27-32 ("This is done by creating a field, such as a drift field, in the semiconductor substrate to ***sweep minority charge carriers***…into the bulk [substrate], away from the electrode-bearing surface of the substrate.").



Ex. 1010, FIGS. 1a-1b.

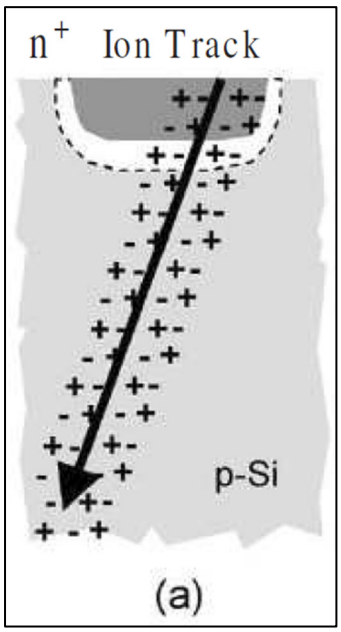
98. Applicant made the same representation to the Patent Office regarding Kamins. Ex. 1002, 237-238, 253-254. According to Applicant, Kamins' Figure 3 shows "two electrical fields with opposing directions" (highlighted in blue and yellow) that correspond to increasing and decreasing graded-dopant concentrations, respectively. *Id.*, 237, 253 (citing Ex. 1009, 3:6-13, FIGS. 2-3). Applicant explained that Kamins "show[s] ***minority carrie[r]s accelerated into the substrate.***" *Id.*, (citing Ex. 1009, FIG. 2 and quoting Ex. 1009, 3:6-13 ("carriers… accelerated… ***away from the surface*… *into the substrate***")).

99. According to Applicant, the electric field associated with the downward-sloping graded concentration at depth beyond ~10μm (red) causes "[minority] carriers created [in that region to be] … ***accelerated into the substrate*** …." *Id.* (citing Ex. 1009, 3:6-13, FIGS. 2-3); Ex. 1030 at 24 (Kamin's "bottom electric field [(yellow)] draws a ***minority carrier*** from the substrate to a ***deeper*** part of the substrate."); Ex. 1009, 2:67-3:14 ("The non-uniform dopant concentration in the substrate creates electric fields in the substrate indicated by arrows labeled 'ε' in FIGS. 2 and 3" such that "[minority] carriers created below the maximum dopant concentration are accelerated into the substrate."), FIG. 2 (referring to these carriers as "photogenerated minority carriers"), 2:11-16 (same).



Ex. 1009, FIG. 3.

100. During a so-called single event upset (SEU), an α-ray generates millions of carriers, some of which are produced in or near the active regions at the surface of the substrate. Ex. 1013, 431 ("A[n] [α-]particle can induce SEU when it strikes at the ***channel region*** of an off NMOS transistor or the ***drain region*** of an off PMOS transistor."), FIG. 2. As shown in Figure 2, such event generates both types of carriers (holes, denoted "+" and electrons, denoted "-"), one of which will be the minority carrier in any given surface layer.



Ex. 1013, FIG. 2(a).

101. Like Jastrzebski and the right-hand side of Kamins Figure 3 (yellow), Payne's graded dopant concentration is downward-sloping, as shown in Figure 11. Moreover, this graded-dopant profile is determined by the ion-implantation and drive-in steps of the chip fabrication processes (described in Payne in relation to

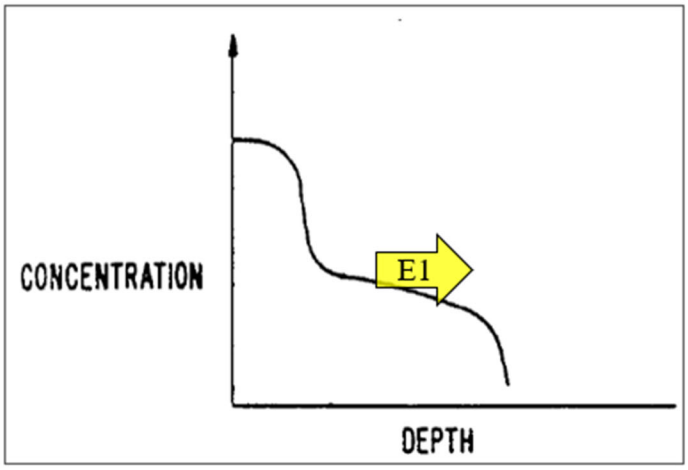
Figures 2 and 5-9 in particular) and thus the profile (and any resulting electric field) is static—it is set once the device has been fabricated and does not change. Ex. 1005, 5:7-17, 5:44-55 (describing "the ***final*** depth" of tubs and surface regions and their typical ranges of impurity concentrations).

102. I note that during prosecution, Applicant described "static" similarly, conceding that "Kamins (US 4,160,985), just like Applicant, discloses the presence of a 'static' drift field, 'because the drift field is created by graded concentration of dopants which does not change over time.'" Ex. 1002, 318 (citing Ex. 1009, 2:15-16, 2:64-3:2, 1:38-46, 3:8-11 and Ex. 1002, 302-03), 333 (same).

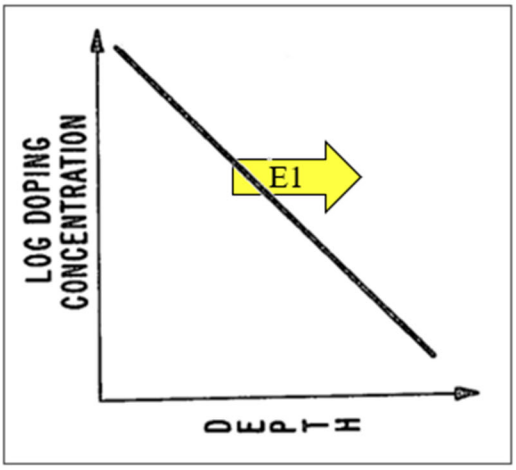
103. Thus, according to Jastrzebski, Kamins, Applicant, and Patent Owner, Payne's profile generates a (first) "built-in" static unidirectional electric drift field (illustrated by the yellow arrow labelled "E1" in Payne FIG. 11, below) that aids the movement of minority carriers from the surface layer to the substrate. As a POSITA would understand, the direction convention of the E-field will depend on the material type, due to electrons for n-type and holes for p-type.

104. The figures of this declaration depict electric fields in N-wells, *e.g.*, Payne's nested N-wells 15/18 or Sakai's nested N-wells 3/5. Sections X.A.1.g, X.B.1.f-g, X.B.2, X.D.1. The electric fields would be pointing in the opposite direction in Payne's and Sakai's nested P-wells.

105. In both cases, these electric fields result from the downward-sloping graded concentrations in Payne's and Sakai's N-wells and P-wells and aid the movement of minority carriers (holes in N-wells, electrons in P-wells) downward to the substrate, particularly under Patent Owner's and Applicant's position as I discuss in Sections X.A.1.g, X.B.1.f-g, X.B.2, X.D.1.

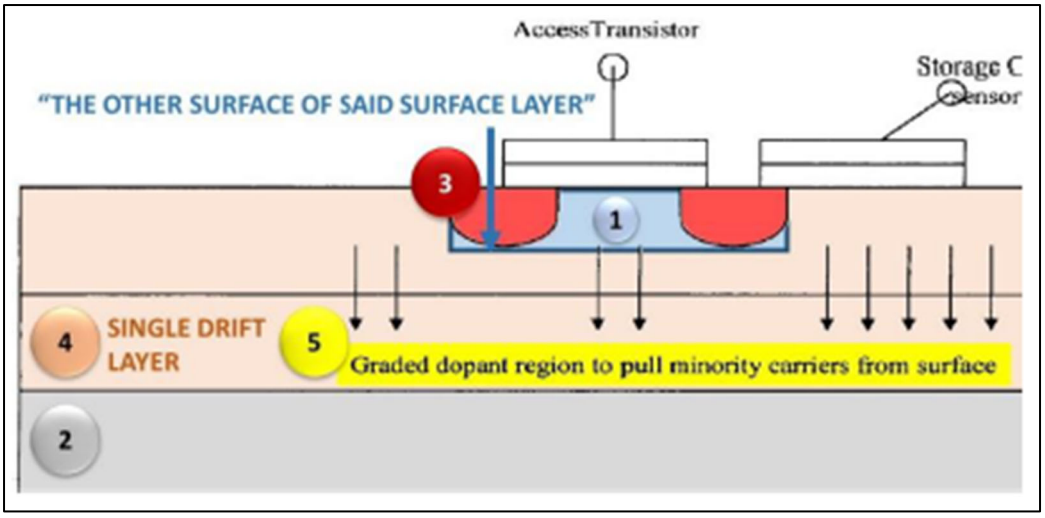


Ex.1005, FIG. 11



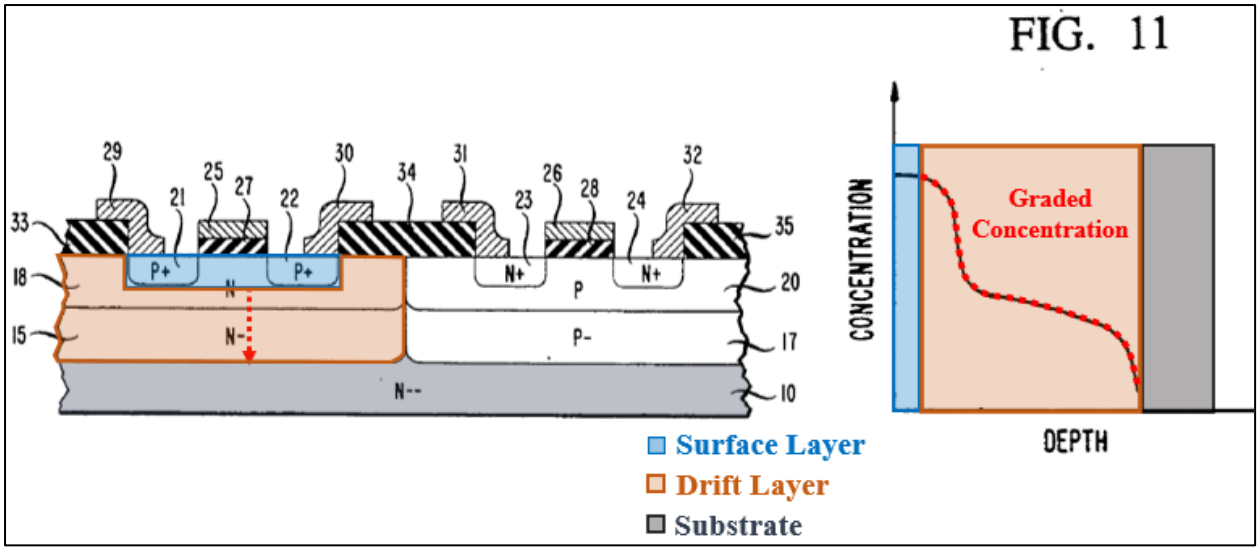
Ex.1010, FIG. 1b

106. In my opinion, Payne satisfies element [1.5] to the same extent the '195 Patent's Figure 5(b) meets it. While the '195 Patent does not disclose any single drift layer's dopant profile, Patent Owner contends that annotated Figure 5(b) below shows that "[t]he single drift layer has a graded concentration of dopants … [that] create[s] an electric field that aids the movement of minority carriers [] from the surface layer to the substrate." Ex. 1030, 7.



Ex. 1001, FIG. 5(b); Ex. 1030, 7.

107. In light of the above, it is my opinion that Payne satisfies element [1.5] under Patent Owner's plain-meaning constructions. Section VIII. Payne's Figure 11 shows a graded-dopant concentration that is downward-sloping over the entire single drift layer (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the single drift layer—and thus, according to Patent Owner (and Applicant's representations to the Patent Office discussed above), this graded-dopant concentration creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex. 1005, FIG. 11.



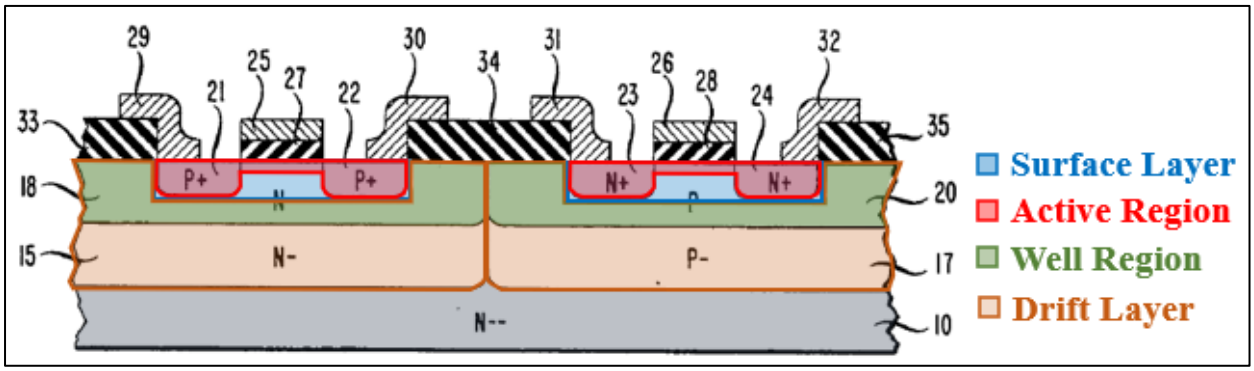
Ex. 1005, FIGS. 10-11.

108. For the same reasons, in my opinion, Payne satisfies Petitioner's construction that the first static unidirectional electric drift field must be "unidirectional ***over*** the drift layer," and also satisfies Petitioner's alternative proposed construction of the sub-phrase "to aid the movement of minority carriers from said surface layer to said substrate" to mean "to sweep the minority carriers from said surface layer to said substrate." *Id.*, Section VIII; Ex. 1002, 289-290.

g. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

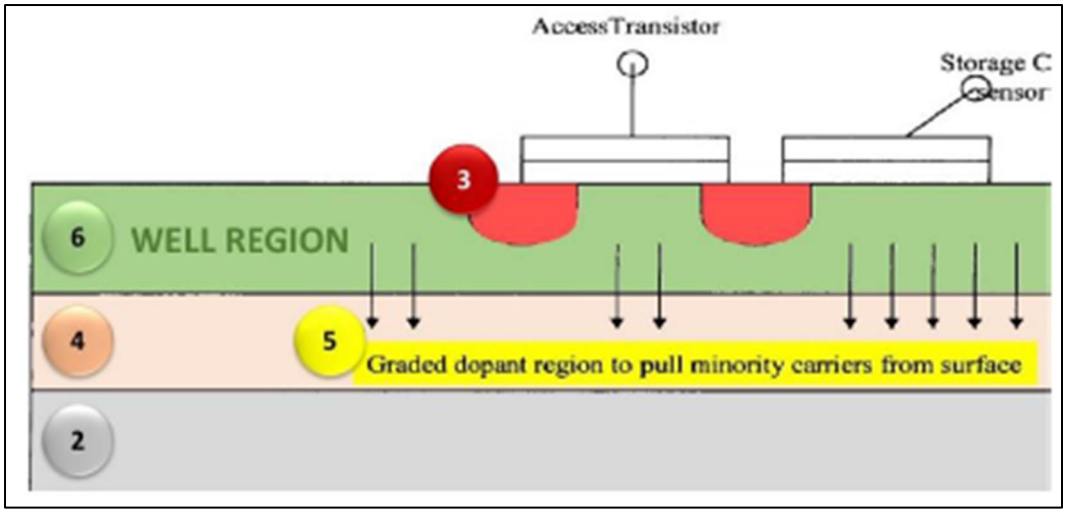
109. In my opinion, Payne discloses or, at a minimum, renders obvious this element.

110. **<u>Well region disposed in said single drift layer…having a graded concentration of dopants</u>** – As detailed above in Sections X.A.1.e-f regarding elements [1.4] and [1.5], Payne's "tub region" 15 is an example of the claimed single drift layer. As shown below, Payne's **"surface region" 18 (green)** disposed in tub region 15 (tan) is an example of a well region (a shallow well) disposed in Payne's single drift layer (tub). Ex. 1005, 1:65-68, 4:31-39, 5:7-14, 5:44-55; Payne's **surface region 20 (green)** is another well region disposed in a single drift layer (tub 17). *Id.*, 1:65-68, 4:63-5:14, 5:44-55; *see* Section X.B.1.e.



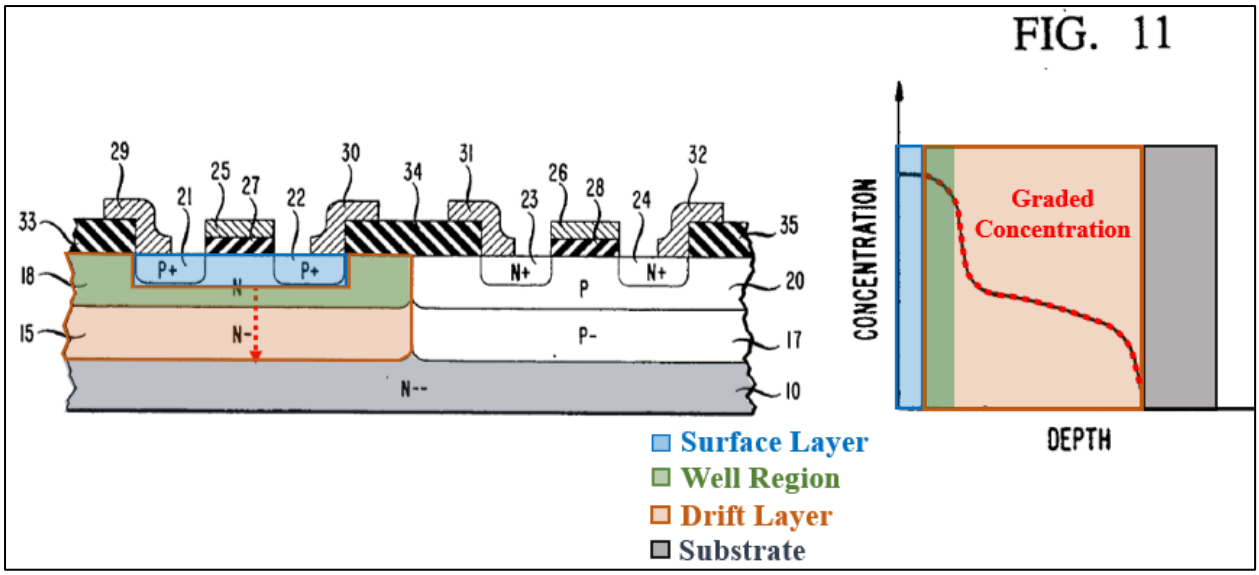
Ex. 1005, FIG. 10.

111. Notably, Payne satisfies element [1.6] to the same extent that Figure 5(b) of the '195 Patent, annotated by Patent Owner (as shown below), meets it:



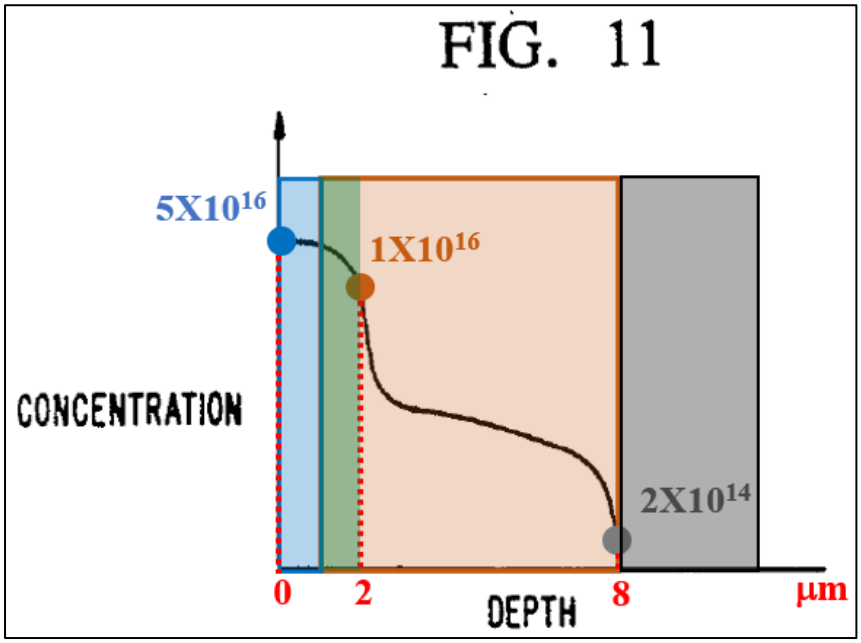
Ex. 1001, FIG. 5(b); Ex. 1030, 7.

112. As detailed above with respect to element [1.4], Payne's Figure 11 (below right) illustrates the dopant concentration measured along the red dotted line in Figure 10 (below left). As shown, Payne's well region ("surface region 18") (green)—disposed in the single drift layer (tub 15) (tan border)—has a graded-dopant concentration that is downward-sloping with increasing depth. Section X.A.1.e.



Ex. 1005, FIGS. 10-11.

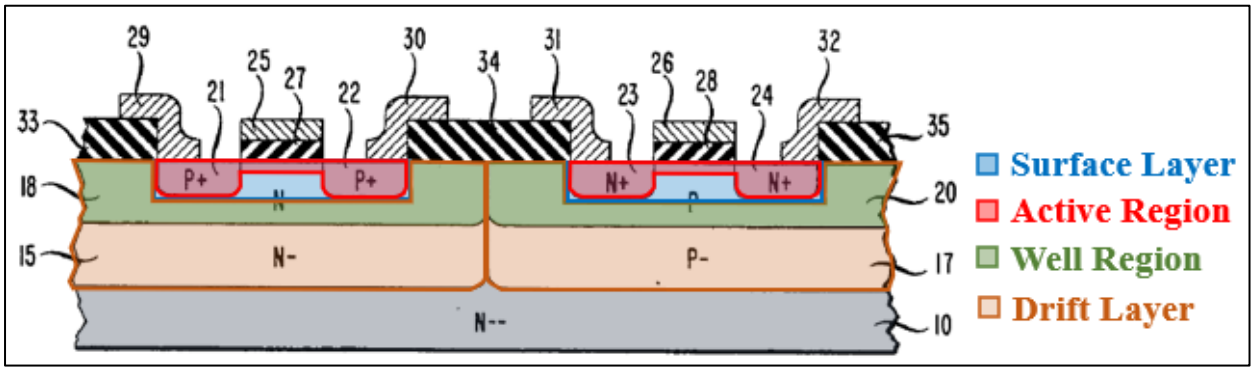
113. As discussed in Section X.A.1.e, Payne discloses that Figure 11 illustrates a "***high-low implant profile***" that is downward-sloping with depth, such as from **5x10^{16}** ions/cm^3 (near the top surface of the silicon/surface layer (blue)) to **1x10^{16}** ions/cm^3 near the bottom of well 18 (green), to **2x10^{14}** ions/cm^3 near the bottom of the single drift layer (tub 15) (tan). *Id.,* 2:56-59, 5:48-57.



Ex. 1005, FIG. 11.

114. In my opinion and in light of the above, Payne satisfies element [1.6] under Patent Owner's construction that the term "well region" should be accorded plain meaning and is "a doped region that surrounds the active region of a semiconductor device." Section VIII. As shown in Figure 10 below, the well region

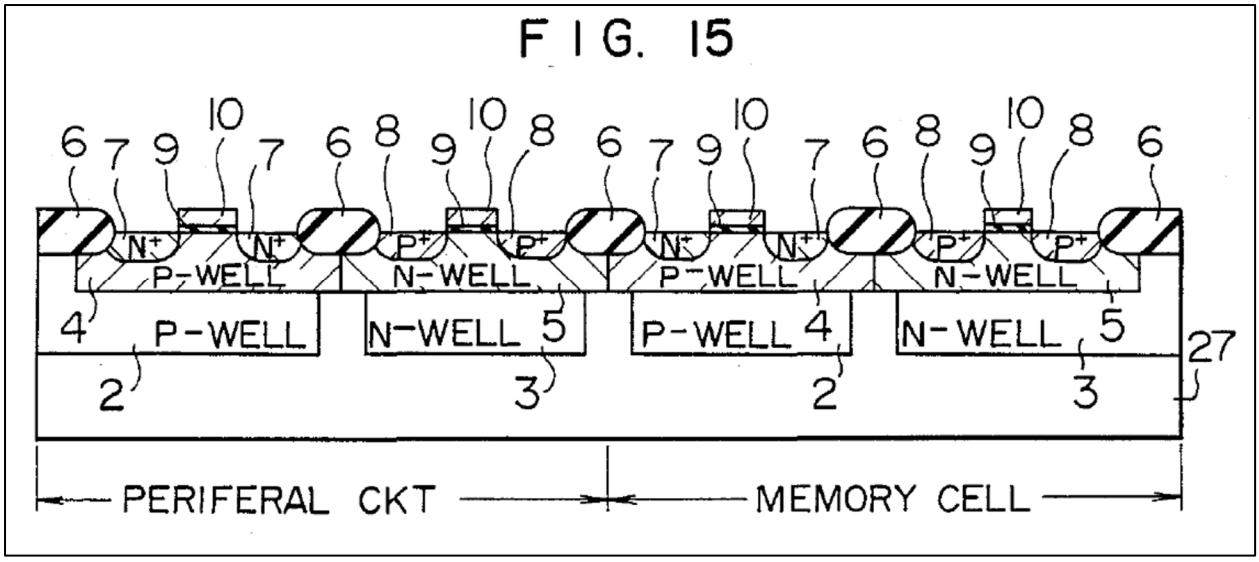
(green) is a doped region that surrounds the surface layer (blue) and the active region (red) therein.



Ex. 1005, FIG. 10.

115. In my opinion, Payne also satisfies Petitioner's proposed constructions of "well region" to mean "a well, whether formed by single or multiple implants. Portions of a well are not well regions." Section VIII. Each surface region 18/20 is a well (and not a portion of a well) formed with an ion implant of phosphorous or boron. Ex. 1005, 4:31-39, 4:63-5:5, FIGS. 7, 9.

116. In addition, as discussed in Section X.B, Sakai teaches a nested structure similar to Payne, which Sakai refers to as "twin double well." *See, e.g.,* Ex. 1006, 7:19-37 ("The memory of FIG. 15 has a ***twin double well*** structure … made up of the ***deep*** P-well region 2, the ***deep*** N-well region 3, the ***shallow*** P-well region 4 and the ***shallow*** N-well region 5").

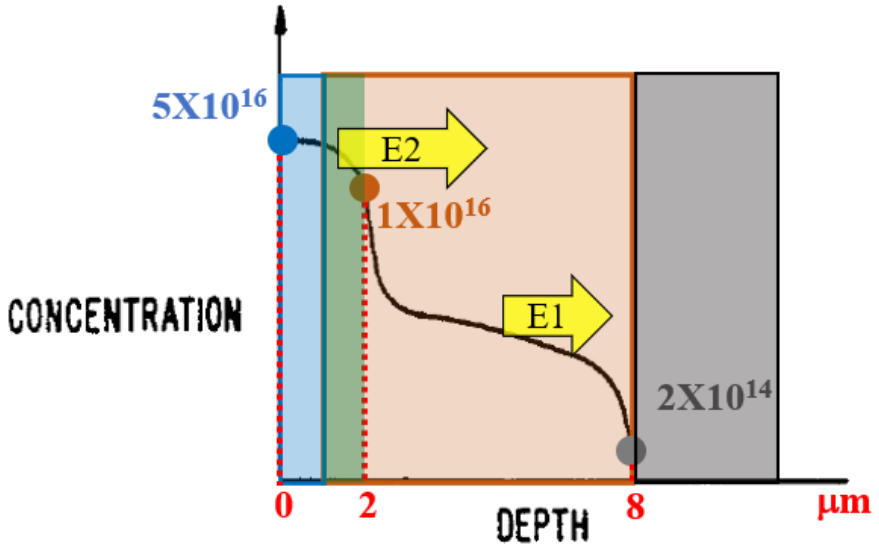


Ex. 1006, FIG. 15; 1:57-67, 5:56-6:4, FIG. 10B, FIGS. 3, 8-9, 11E. Sakai confirms that Payne's "surface region" is a shallow well region.

117. **Second static unidirectional electric drift field to aid the movement of minority carriers** – According to Section X.A.1.f—including Applicant's repeated representations during prosecution, Jastrzebski and Kamins relied on by Applicant during prosecution, and Patent Owner's statements in its claim construction brief—the downward-sloping graded-dopant concentration in the well region creates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Section X.A.1.f. Further, Payne's graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in Section X.A.1.f.

118. I have further annotated Payne's Figure 11 below to show the exemplary first static unidirectional electric drift field ("E1") present in a deep portion of the single drift layer (discussed in Section X.A.1.f), and a different, exemplary second static unidirectional electric drift field ("E2") present in the well region disposed in the single drift layer. *See* ¶¶104-105.

FIG. 11



Ex. 1005, FIG. 11.

119. I have also shown E1 and E2 as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the graded-dopant profile. Ex. 1022, [0071] ("the vertical €-field is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change … the greater the intensity of the €-field.").

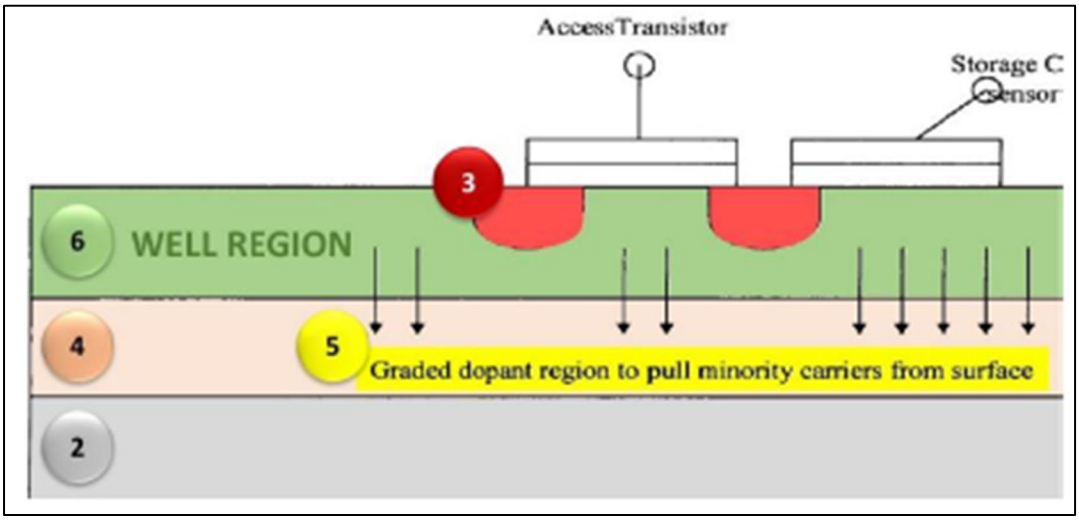
120. In my opinion and in light of the above, Payne satisfies Element [1.6] under Patent Owner's plain-meaning construction of "to aid the movement of minority carriers". Section VIII. Payne's Figure 11 shows that the dopant concentration is downward-sloping with increasing depth over the entire well region, and thus, according to Patent Owner (and also in light of Applicant's representations to the Patent Office, discussed in Section X.A.1.f), creates a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate. Ex. 1030, 2, 29.

121. For the same reasons, in my opinion, Payne also satisfies this claim element under Petitioner's construction that the second static unidirectional electric drift field must be "unidirectional over the well region," and also satisfies Petitioner's alternative proposed construction that "to aid the movement of minority carriers" means "to sweep the minority carriers from said surface layer to said substrate." Section VIII; Section X.A.1.f; Ex. 1002, 289-290.

2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

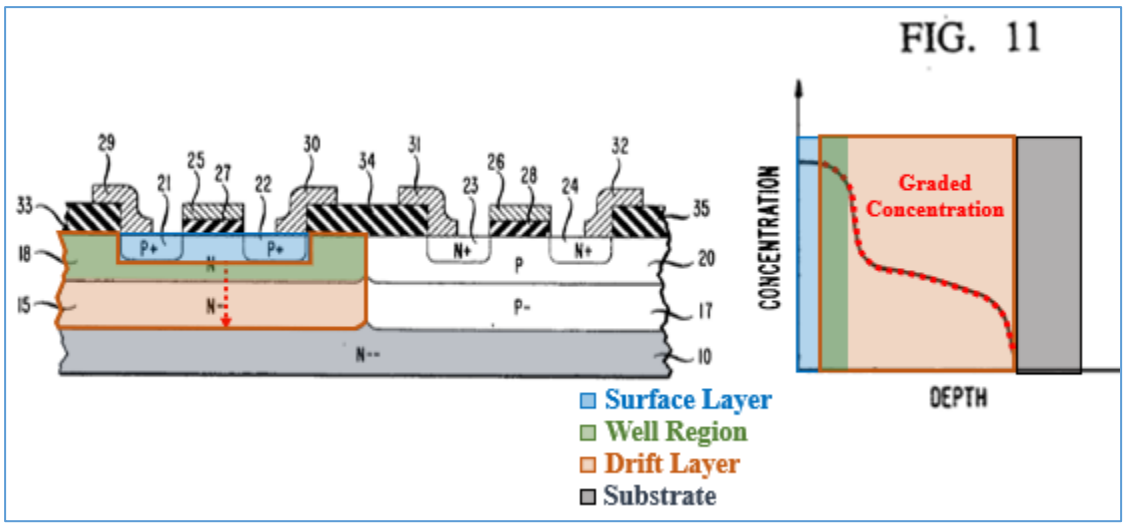
122. In my opinion, Payne renders obvious claim 2. The '195 Patent mentions "deeply-implanted layer" just once, suggesting that the "subterrain n^- layer" (tan) in Patent Owner's annotated Figure 5(b) below "can be a deeply-implanted

layer." Ex. 1001, 3:33-38. I note that the specification does not discuss the depth of this "deeply-implanted layer" or the process for forming such a layer.



Ex. 1001, FIG. 5(b); Ex. 1030, 7.

123. As detailed above in Section X.A.1, Payne's Figure 10 (below left) discloses a double-deck well structure that matches Figure 5(b) of the '195 Patent. *See* Section X.A.1.e-g.

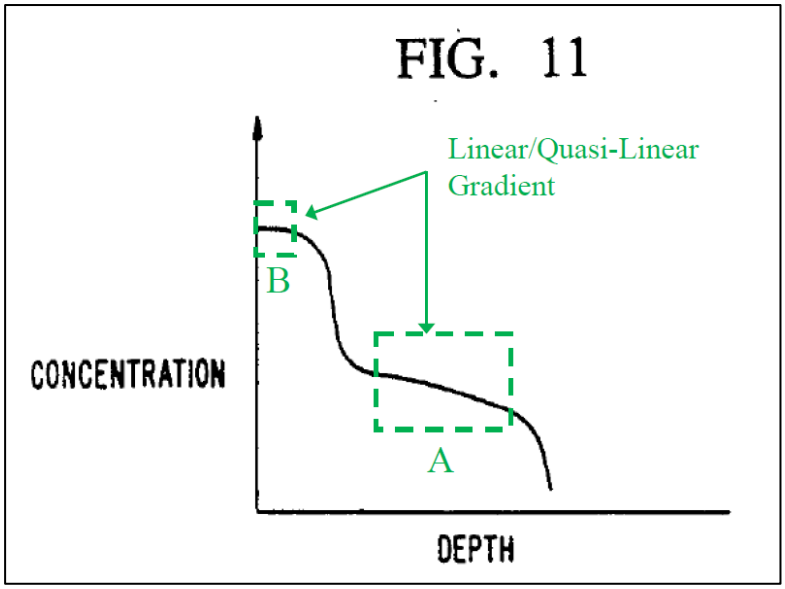


Ex. 1005, FIGS. 10-11.

124. Payne's nested well structure is formed by multiple distinct ion-implantation process steps illustrated in its figures. *Id.*, 1:5-6, 3:17-5:17, FIGS. 2-9. In particular, "tub region 15" (left) (tan) and "tub region 17" (right) are deep wells that are formed by ion implantation and drive-in annealing, and they extend to a depth of 3-8μm. *Id.*, 5:48-50, 3:28-42, 4:3-25, FIGS. 2, 5, 6; Ex. 1008A, 403 ("high-energy machines are used to produce the deeper (1-2 μm) CMOS wells"). Each of Payne's tub regions (*e.g.,* tub region 15 (tan)) is a deeply-implanted layer to the same extent Figure 5(b) of the '195 Patent shows a deeply-implanted layer.

3. Dependent Claims 4 and 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a linear gradient"; "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient."

125. In my opinion, Payne discloses or renders obvious claims 4 and 5. As shown in Figure 11 below, Payne teaches a graded-dopant profile that follows a linear/quasi-linear gradient in at least the regions of the deep well ("tub region") (A) and shallow well ("surface region") (B), outlined in green, where the dopant concentration decreases gradually in a linear or nearly-linear (quasilinear) manner. Sections X.A.1.e, X.A.1.g; Ex. 1040, 437 (defining "quasi-linear" as "substantially linear").

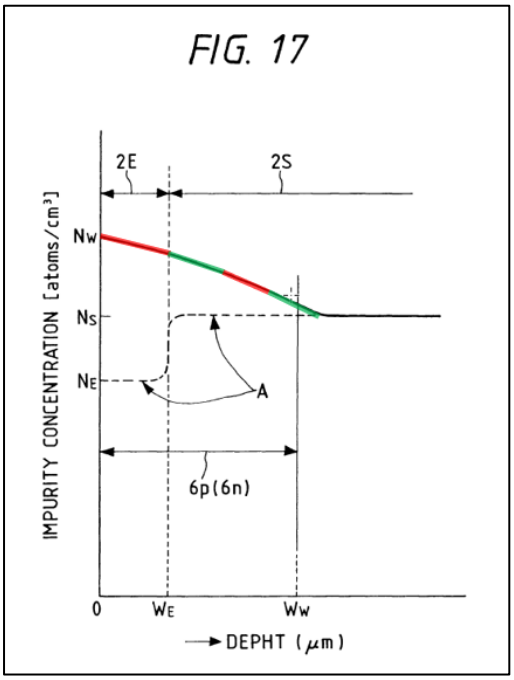


Ex. 1005, FIG. 11. Payne's illustrative graded-dopant profile of Figure 11 in fact comprises many small linear/quasilinear segments— smaller segments become even more linear/quasilinear.

126. Linear/quasi-linear doping profiles were also well-known and obvious. The '195 Patent only mentions a "linear [or] quasi linear" gradient once and does not illustrate it or describe any process for obtaining it, which in my opinion confirms that such a gradient was well-known and that a POSITA would have known how to manufacture a CMOS device with such a profile. Ex. 1001, 2:40-42. The '195 Patent also lists linear/quasi-linear among a few likewise well-known gradients without giving any reason to use one over another. Ex. 1001, 2:40-42.

127. Kawagoe provides further evidence that dopant profiles with linear/quasi-linear gradients were indeed well-known. Kawagoe's Figure 17 below is an example of a linear/quasi-linear dopant profile. *Id.* It is also a combination of

linear/quasi-linear segments, illustrated in green/red— smaller segments become even more linear/quasi-linear.



Ex. 1007, FIG. 17.

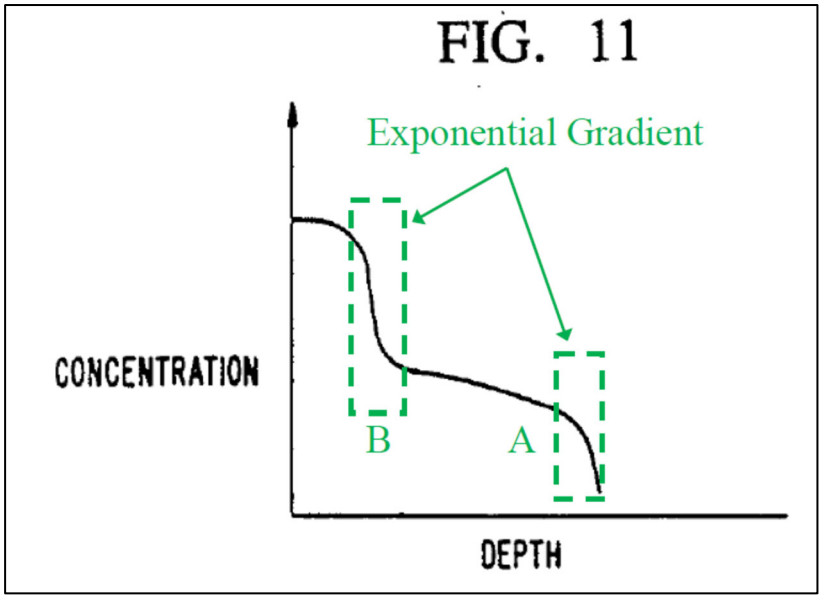
128. In my opinion, it would also have been obvious to modify Payne's graded-dopant profile based on the POSITA's general knowledge in the art to achieve a known linear/quasi-linear gradient as in Kawagoe's graded-dopant profile. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement (Sections X.A.1.f-g; Ex. 1007, 16:2-11), with a reasonable expectation of success,

as shown by Kawagoe's implementation of CMOS devices similar to Payne's. Ex. 1007, 14:46-55, 15:26-40, FIG. 16. *Id.*

129. Indeed, it was well-known that the ion-implantation process described in Payne is a versatile process that enables different dopant profiles to be readily engineered and fabricated as needed. Ex. 1005, 1:1-9 ("Ion Implanted CMOS Devices"); Ex. 1008A, 371 ("Ion implantation is superior" for many reasons, including that "***Depth profiles of the implanted species can be established*** … This capability can be extended to produce the depth profiles needed in complex applications by using multiple-energy implants."), 373 ("Complex-doping profiles can be produced" using ion implantation).

4. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient."

130. In my opinion, Payne discloses or renders obvious claim 6. As shown in Figure 11 below, Payne teaches a dopant profile that follows a rapidly changing, exponential gradient in at least the border region of the deep well and the substrate (A), and the border region of the shallow well and the deep well (B), outlined in green. Sections X.A.1.e, X.A.1.g; Ex. 1028, 337 (defining "exponential" as "more and more rapid").

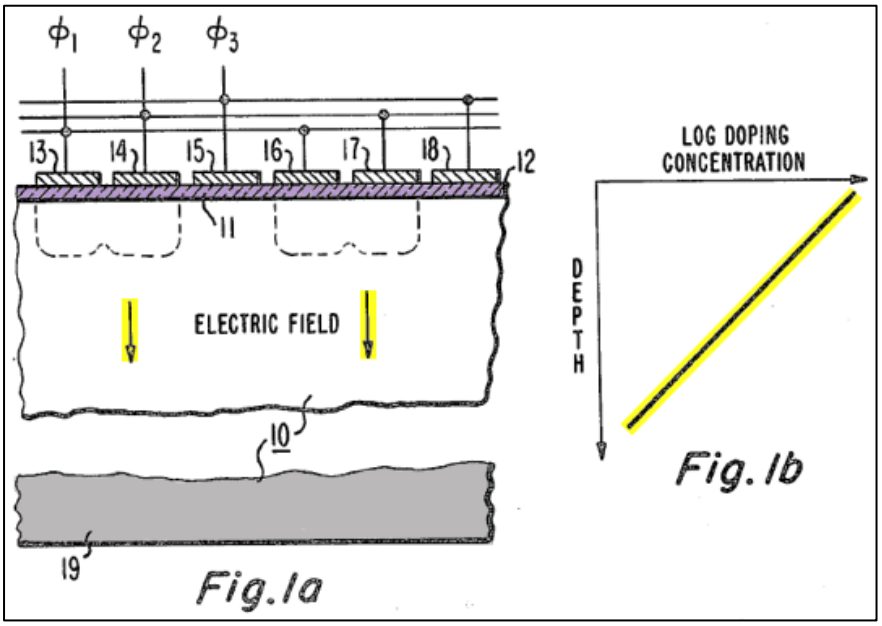


Ex. 1005, FIG. 11.

131. Dopant profiles with exponential gradients were also well-known and obvious. The '195 Patent only mentions "exponential" gradient once and does not illustrate or otherwise describe it or describe any process steps for obtaining it, which in my opinion confirms that such a gradient was well-known and that a POSITA would have known how to manufacture a CMOS device with such a profile. Ex. 1001, 2:40-42. The '195 Patent also lists exponential among a few likewise well-known gradients without giving any reason to use one over another. Ex. 1001, 2:40-42.

132. Jastrzebski provides further evidence that dopant profiles with exponential gradients were indeed well-known. As explained in Jastrzebski, "FIG. 1b is a graph of the ***logarithm*** of doping concentration versus depth." Ex. 1010, 5:25-

27. As shown below, the "log doping concentration" in Figure 1b is linear, meaning that the dopant concentration follows a rapidly changing, exponential gradient.



Ex. 1010, FIGS. 1a-1b.

133. In my opinion, it would have been obvious to modify Payne's graded-dopant profile based on the POSITA's general knowledge in the art to achieve a known exponential gradient as in Jastrzebski's graded-dopant profile. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known downward-sloping graded-dopant profile for another while retaining the same known benefit of aiding minority carrier movement (Sections X.A.1.f-g; Ex. 1007, 16:2-11), with a reasonable expectation of success. Ex. 1010, 2:27-32, 5:11-21. Indeed, as discussed above in Section X.A.3, it was

well-known that the ion-implantation process described in Payne enables different dopant profiles to be readily engineered and fabricated as needed. Ex. 1005, 1:1-9; Ex. 1008A, 371, 373 ("Complex-doping profiles can be produced" using ion implantation).

B. Ground II

134. In my opinion, Sakai in combination with Kawagoe (hereinafter, "Sakai-Kawagoe") renders claims 1-6 obvious.

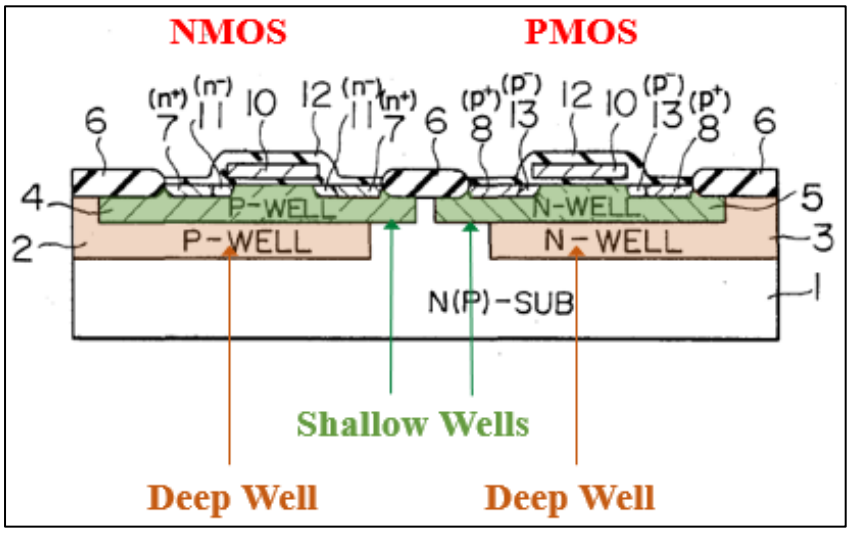
1. Independent Claim 1

a. Preamble: "A CMOS semiconductor device comprising:"

135. In my opinion, Sakai-Kawagoe discloses the preamble. Sakai is directed to CMOS semiconductor devices. Ex. 1006, Title, 1:6-13 ("The present invention relates to a complementary semiconductor device (hereinafter referred to as 'CMOS')"), 1:55-2:5.

136. A CMOS device has "N-channel MOS [(NMOS)] transistor[s]" and "P-channel MOS [(PMOS)] transistors." *Id.*, 4:15-29; Ex. 1008A, 807-09. "[T]win-well" CMOS technology is a conventional structure that uses separate, side-by-side wells for the p- and n-type transistors, and is the technology focus of both Sakai and Kawagoe. Ex. 1008B, 387-88; Ex. 1006, 1:6-13, 7:19-23; Ex. 1007, 14:46-55, 15:26-40, FIGS. 16, 21-24, 26-28.

137. Sakai teaches a "twin *double* well" structure, whereby shallow wells (p-well 4 and n-well 5) (green) are formed in the wells (p-well 2 and n-well 3) (tan) of a conventional twin-well CMOS device, as shown in Figure 10D below. Ex. 1006, 1:55-2:5, 5:53-6:4, 7:19-23, 7:32-37, 8:6-8; *compare* Ex. 1006, FIG. 1 *with* FIGS. 2A, 3.

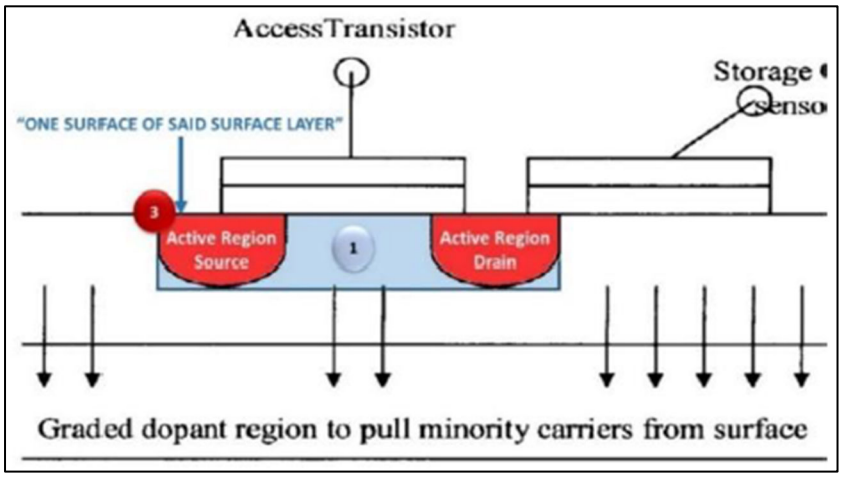


Ex. 1006, FIG. 10D; *id*., FIGS. 2A, 3, 8-9, 10A-10E, 11A-11E, 15-17, 3:18-43.

138. While this Ground relies primarily on Sakai's Embodiment V (FIGS. 10A-E and accompanying discussion), which itself is based on Embodiment I (FIGS. 2A-B) (Ex. 1006, 5:53-55), Sakai discloses similar "twin double well" structures in the other embodiments and those embodiments are applicable for the same reasons as explained throughout this Ground. *Id.,* FIGS. 3, 8-9, 11A-11E, 15-17 (and accompanying discussion).

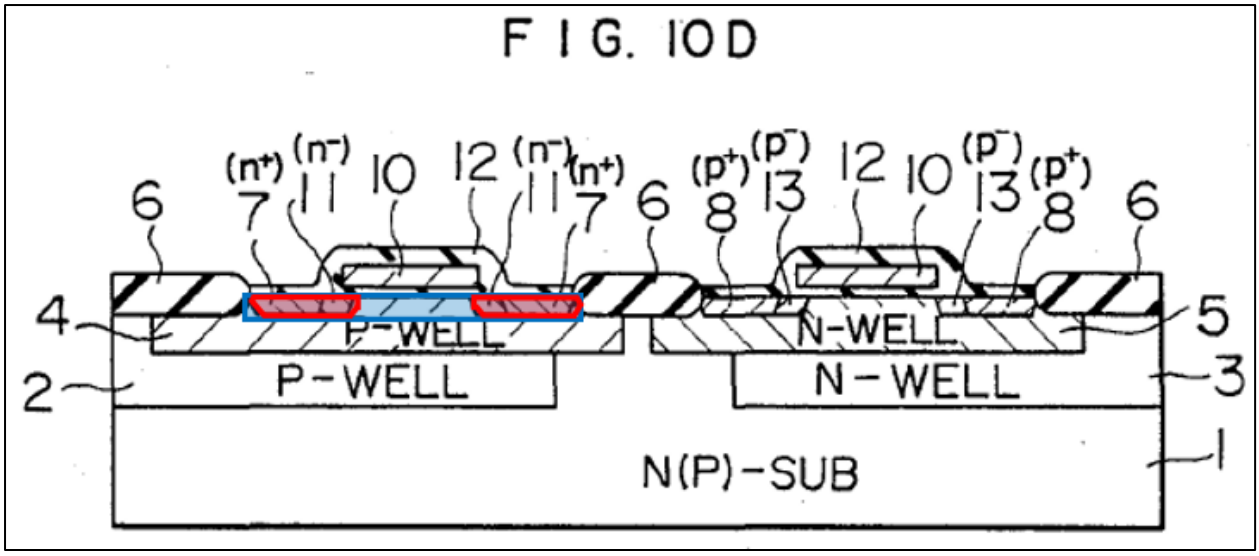
b. Element [1.1]: "a surface layer;"

139. In my opinion, Sakai discloses or, at a minimum, renders obvious this element. According to Patent Owner, a "surface layer" is "a layer at the surface of the silicon" (or "a layer at the surface of the semiconductor device")—which Patent Owner annotated in blue in Figure 5(b) below—"where the active region [(red)] is located." Ex. 1030, 6, 9, 12, 13; Section VIII; Section X.A.1.b.



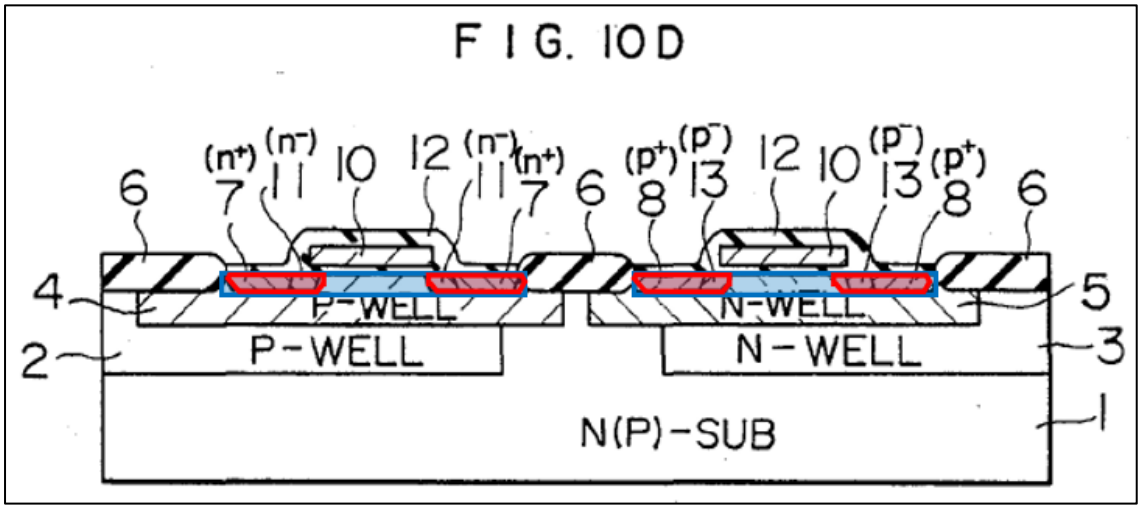
Ex. 1001, FIG. 5(b); Ex. 1030, 7, 12.

140. In my opinion, Sakai satisfies element [1.1] to the same extent that Figure 5(b) meets it. Sakai's Figure 10D discloses a surface layer (blue) that matches the surface layer Patent Owner identified in Figure 5(b). Sakai's surface layer is at the surface of Sakai's silicon substrate 1, and the source and drain regions ("highly-doped N-diffusion layer 7") [(red)] of Sakai's N-channel MOS transistor (left) are located in it. Ex. 1006, 1:28-30, 1:68-2:5, 4:25-29, 5:53-55, 5:59, 6:16-17; *id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:54-55.



Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

141. Sakai likewise discloses a surface layer containing "highly-doped P-diffusion layer 8," which serves as the source/drain regions in the "P-channel MOS transistor" (below right). *Id.*, 1:68-2:5, 4:25-29, 5:53-55, 6:16-17; *id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:54-55.

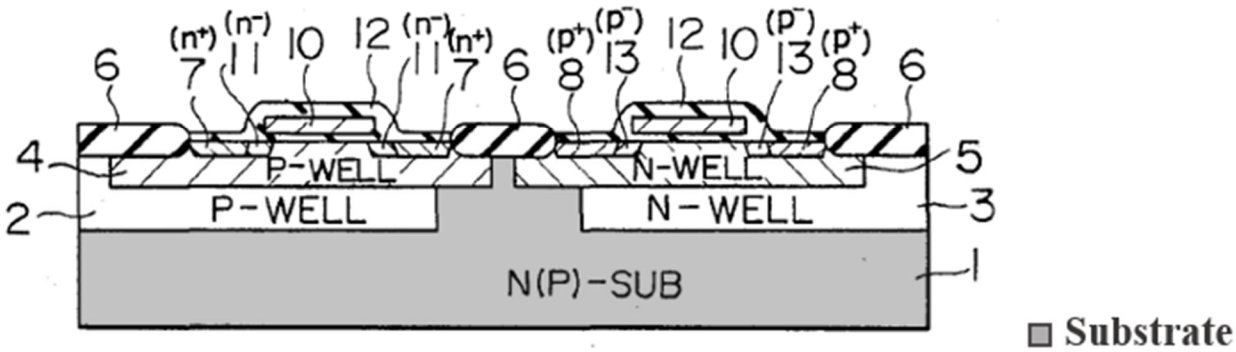


Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

c. Element [1.2]: "a substrate;"

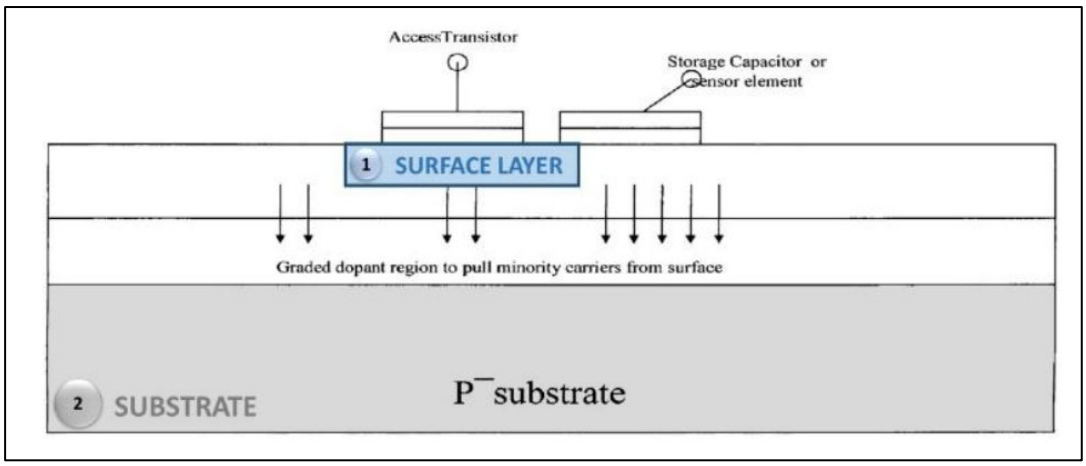
142. Sakai discloses "a silicon substrate 1 [(grey below)] made of N-silicon or P-silicon." Ex. 1006, 4:13-14, 5:59; *id.*, 1:61, 6:26-27.

FIG. 10D



Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

143. In my opinion, Sakai satisfies element [1.2] under Patent Owner's proposed construction of "plain and ordinary meaning [*i.e.*] 'an underlying layer.'" Section VIII. Sakai's substrate also matches Patent Owner's identification of substrate (grey) in Figure 5(b) of the '195 Patent.

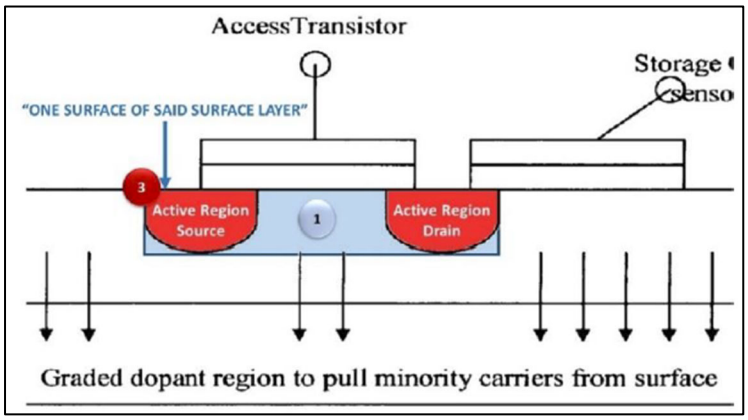


Ex. 1030, 6-7, 16-17 (well region and drift layer can be part of substrate); Ex. 1001, FIG. 5(b).

144. Sakai also satisfies this element under Petitioner's proposed construction of "substrate" because Sakai's substrate is the initial material within which or on which Sakai's semiconductor device is fabricated. Ex. 1006, 1:6-8, 5:53-61; *see also id.*, 1:57-2:5, 3:18-43, FIGS. 2A, 3, 8-9, 10A-10E, 11A-11E, 15-17.

d. Element [1.3]: "an active region including a source and a drain, disposed on one surface of said surface layer;"

145. In my opinion, Sakai discloses or, at a minimum, renders obvious this element. As described in Section X.A.1.d, according to Patent Owner, Figure 5(b) of the '195 Patent depicts an active region (red) "disposed on one surface [(top surface)] of said surface layer."



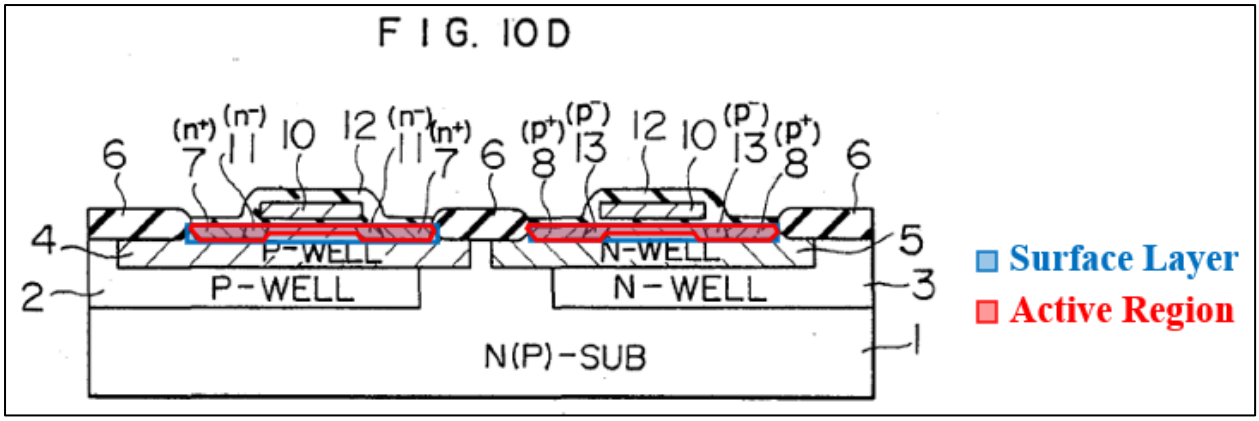
Ex. 1001, FIG. 5(b); Ex. 1030, 6-7, 10-12; Section X.A.1.d.

146. In my opinion, Sakai satisfies element [1.3] under Patent Owner's interpretation. Sakai Figure 10D below illustrates an "N-channel" MOS transistor

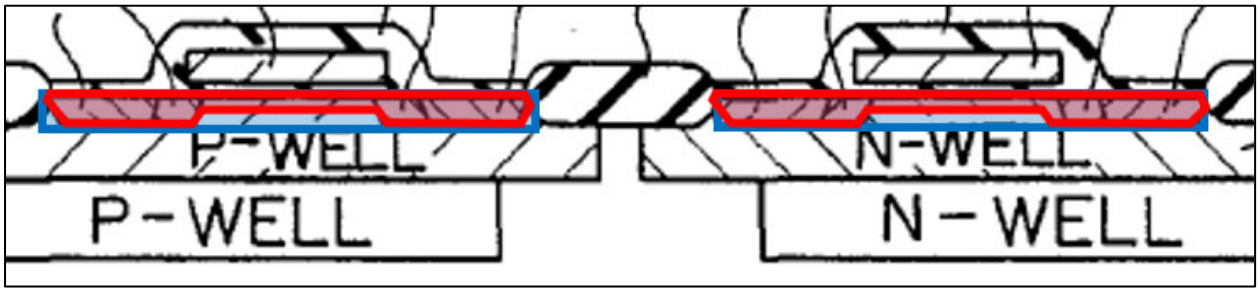
with source/drain regions ("highly-doped N…diffusion layers" 7) (left) in a doped shallow P-well 4, and a "P-channel" MOS transistor with source/drain regions ("highly-doped … P-diffusion layers" 8) (right) in a doped shallow N-well 5. Ex. 1006, 1:28-30, 1:57-2:5, 4:25-29, 5:53-55, 5:64-6:4, 6:16-17; *id.*, 2:51-58, 3:52-4:14, 5:24-32, 6:52-58; Section X.B.1.b.

147. The source/drain regions of a p-channel or n-channel transistor, together with the channel region between them, form an active region. Section X.A.1.d; Ex. 1008B, 299 ("The top surface of the [silicon substrate] body consists of active or transistor regions as well as passive or (field) regions. The ***active regions*** are those in which transistor action occurs; i.e., the ***channel*** and the heavily doped ***source*** and ***drain*** regions."), 300, FIG. 5-2, 382, FIG. 6-8(c), 387, FIG. 6-10; Ex. 1008C, 525, FIG. 8-1(e).

148. The active region (red) of each of Sakai's transistors is disposed on one surface (top surface) of a corresponding surface layer (blue), exactly as depicted in Patent Owner's annotated Figure 5(b) above. Section X.B.1.b.

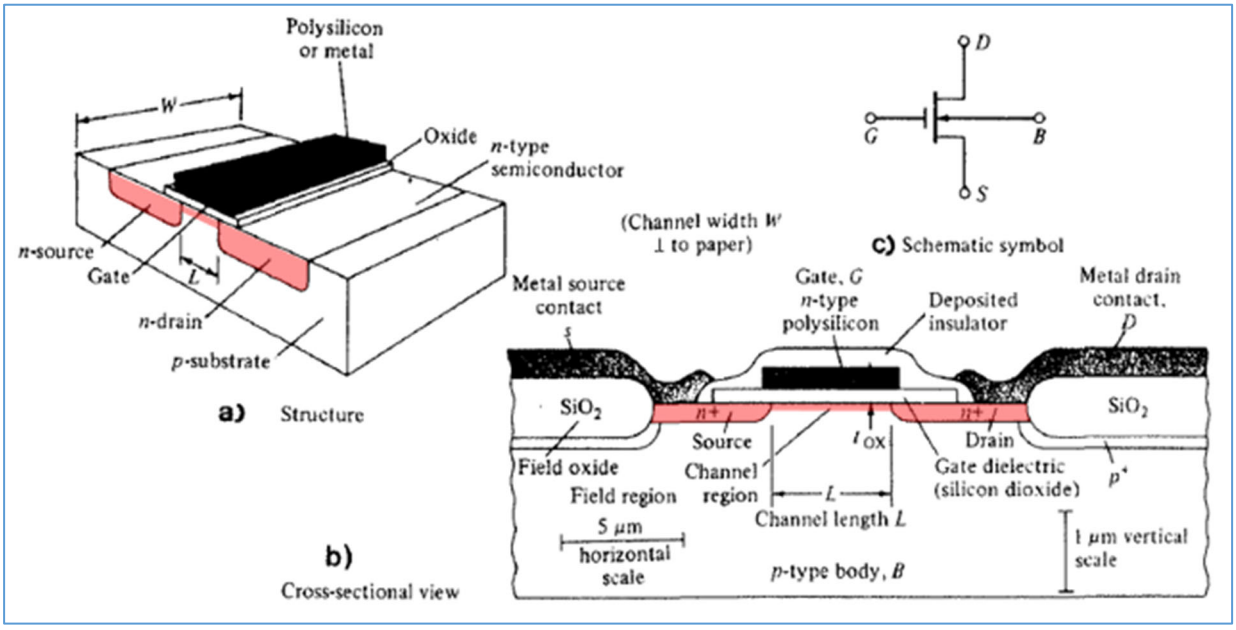


Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. For clarity, an enlarged version of Sakai's active regions and surface layers is below.



Ex. 1006, FIG. 10D (excerpted).

149. In my opinion, Sakai satisfies element [1.3] under Patent Owner's position that the term "active region" means "a doped silicon region at the surface of a semiconductor device (*e.g.*, the source and drain and silicon between them) where a transistor can be formed" (Section VIII) because the active region of a MOS transistor is "[its] channel and [its] heavily doped source and drain regions," highlighted in red below. Ex. 1008B, 299.



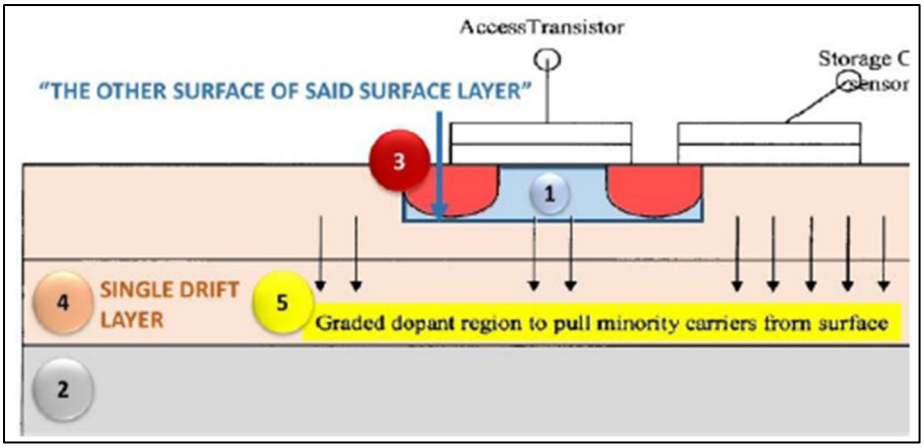
Ex. 1008B, FIG. 5-1; *id*., 298-301, 374, FIGS. 5-2, 6-4.

150. In my opinion, Sakai also satisfies this element under Petitioner's proposed construction that an active region is the "region that forms the current path of a device" or "the source, drain and channel region of a device" because current flows through the channel region that connects the source and drain regions of a transistor when the transistor is active (when an appropriate voltage is applied to its gate). Section VIII; Ex. 1008B, 299-301, FIGS. 5-1, 5-2; Ex. 1008D, 197, FIG. 5-13. I note that Patent Owner does not dispute this. Ex. 1030, 3-4 ("[w]hen a positive voltage is applied to the gate … a conductive channel [is formed] between the source and the drain, and current can begin to flow through the transistor").

e. Element [1.4]: "a single drift layer disposed between the other surface of said surface layer and said substrate, said drift layer having a graded concentration of dopants extending between said surface layer and said substrate,"

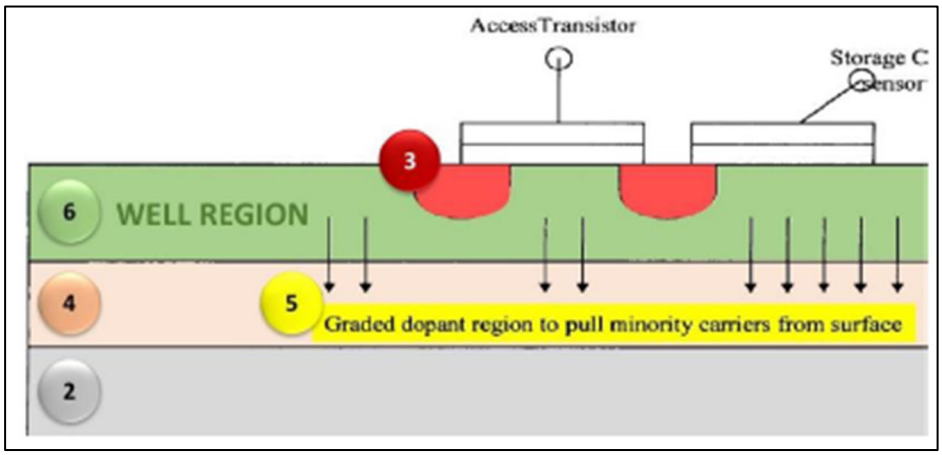
151. In my opinion, Sakai-Kawagoe renders obvious this element.

152. **<u>Single drift layer</u>** – As described in Section X.A.1.e, according to Patent Owner, Figure 5(b) of the '195 Patent depicts a single drift layer (tan) "disposed between the other surface [(bottom surface)] of said surface layer [(blue)] and said substrate [(grey)]":



Ex. 1001, FIG. 5(b); Ex. 1030 at 7.

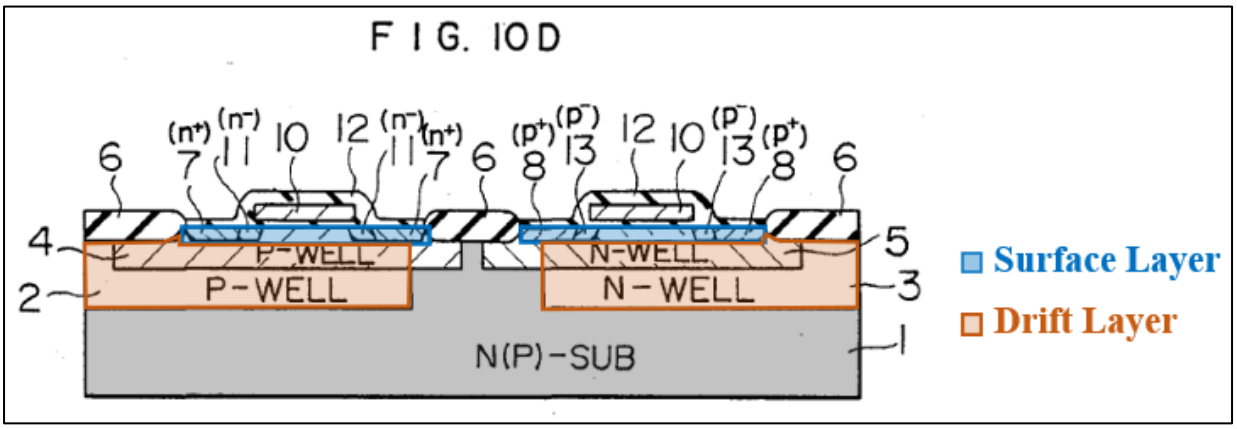
153. The single drift layer in Figure 5(b) has well region (green) disposed in it, forming a nested structure, as required by the claim (*see* element [1.6]):



Ex. 1001, FIG. 5(b); Ex. 1030, 7; *id.*, 11 ("the 'well region' is part of the 'single drift layer.'").

154. Sakai-Kawagoe meets a single drift layer to the same extent Figure 5(b) of the '195 Patent does. In Sakai's Figure 10D, the "deep P-well region 2" (left) of Sakai's nested well structure—with shallow P-well region 4 disposed in it—is an example of the claimed drift layer. *Id.*; Ex. 1006, 5:56-6:4, 1:57-67, 7:32-37; *id.*,

6:24-28, 6:52-58. This single drift layer (tan) is "disposed between 'the other surface [(bottom surface)] of said surface layer [(blue)]' and said substrate [(grey)]" under Patent Owner's interpretation, and in exactly the same way as depicted in Patent Owner's annotated Figure 5(b) above.



Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17. Sakai's "deep N-well region 3" (right), in which "shallow N-well region 5" is disposed, is likewise a single drift layer (tan) disposed between a surface layer (blue) and the substrate (grey). *Id.,* 5:56-6:4, 1:57-67, 7:32-37; *see also id.*, 6:24-28, 6:52-58; Section X.B.1.b.

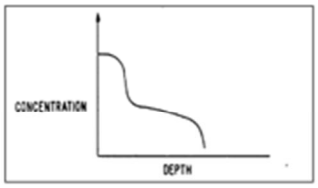
155. In my opinion, Sakai-Kawagoe meets all other claim requirements associated with the single drift layer to the same extent Figure 5(b) meets them, as explained below. *See* elements [1.5]-[1.6]. Notably, as detailed in element [1.5], each of the deep wells 2/3 in Sakai-Kawagoe is a ***single*** drift layer because it has a graded-dopant concentration that, according to Patent Owner, creates a unidirectional electric drift field that aids the movement of minority carriers in a ***single*** direction—

from the surface layer to the substrate. Ex. 1030, 7: Ex. 1002, 253-54, 289-290; Section X.B.1.f.

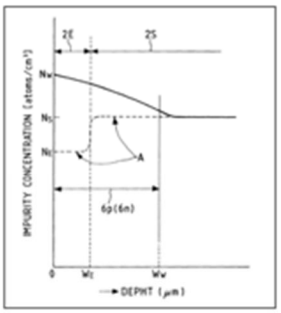
156. **Graded concentration of dopants extending between said surface layer and said substrate** – Sakai-Kawagoe renders obvious a single drift layer having a graded concentration of dopants extending between the surface layer and the substrate. For example, the single drift layer (e.g., deep P-well 2 (above left) with shallow P-well 4 disposed in it) has a ***high-to-low*** dopant concentration, whereby the "shallow P-well region 4" has "an impurity concentration of $5x10^{16}$ to $\mathbf{10^{18}}$ atoms per cm^3," which is up to ***two orders of magnitude higher*** than the dopant concentration in the deep "P-well region 2," which is in the range of "10^{15} to $\mathbf{10^{16}}$ atoms per cm^3." Ex. 1006, 5:56-6:4. The same applies to the single drift layer formed by deep N-well 3 (above right) with shallow N-well 5 disposed in it. *Id.*

157. In my opinion a POSITA would have understood that Sakai's ***high-to-low*** concentration is ***gradually decreasing*** across Sakai's single drift layer because it is formed "through ion implantation techniques and thermal diffusion techniques." Ex. 1006, 5:56-6:4, 6:24-28, 6:52-58, 8:35-38

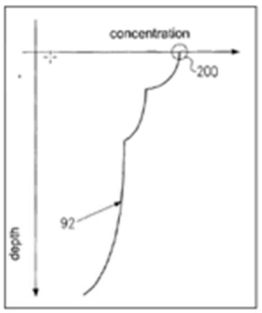
158. Indeed, a downward-sloping graded-dopant concentration formed through ion implantation and thermal diffusion was well-known in the art. Such gradients were disclosed in many prior art references, such as Payne, Kawagoe, Wieczorek and Jastrzebski, as shown below.



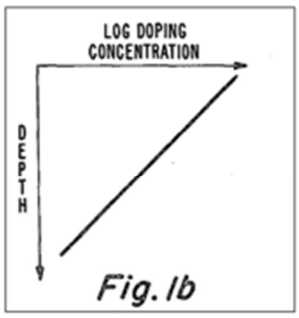
Payne Figure 11



Kawagoe Figure 17



Wieczorek Figure 2b



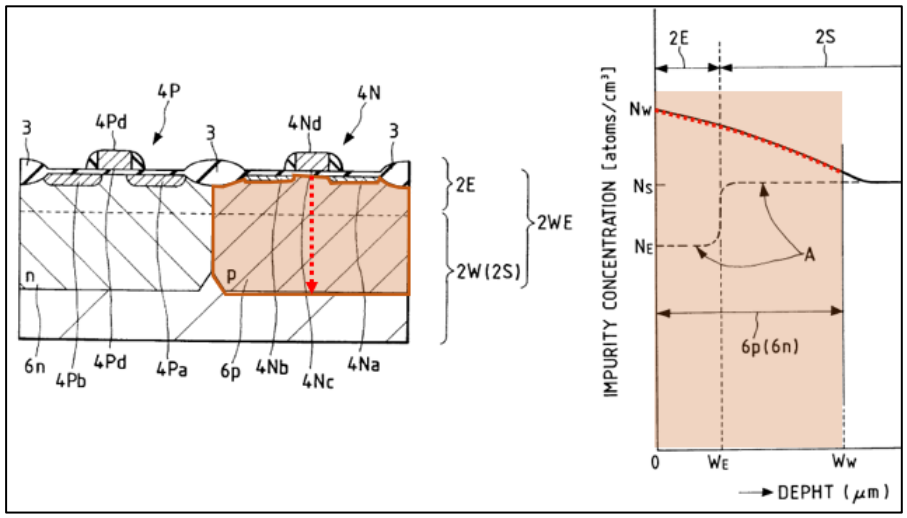
Jastrzebski Figure 2b

Ex. 1005, FIG. 11, 3:28-42, 4:19-39, 5:7-17; Ex. 1007, FIG. 17, 15:62-16:2, 17:31-61; Ex. 1038, FIG. 2b, [0008], [0010]-[0011]; Ex. 1010, FIG. 1b, 5:5-27; 9:2-8. Significantly, Payne's Figure 11 illustrates a graded-dopant profile that is downward-sloping over a ***nested well structure*** similar to Sakai's ***"twin double well"*** structure, as detailed under X.A.1.e-f.

159. Additionally, the '195 Patent mentions "linear [and] quasi linear" dopant gradients only once and does not describe how to make them, confirming implementing them in CMOS devices was well-known. Ex. 1001, 2:40-42. The '195 Patent also lists linear/quasi-linear among a few likewise well-known gradients without giving any reason to use one over another. Ex. 1001, 2:40-42.

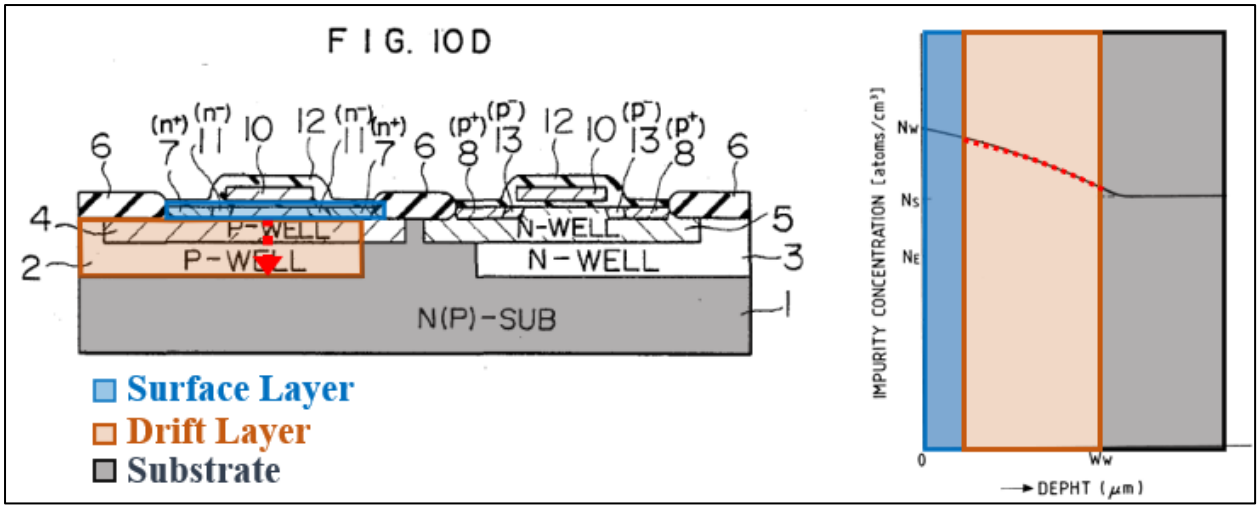
160. And, as further detailed below, it is my opinion that a POSITA would have been motivated to combine Sakai with Kawagoe to ensure that the high-to-low dopant concentration taught by Sakai is implemented as a graded, downward-sloping concentration to protect Sakai's devices against soft errors.

161. Kawagoe teaches that wells of a CMOS device such as "p-well 6p and n-well 6n" in Figure 23 (below left) "have their impurity concentrations ***gradually lowered*** in the depthwise direction" from the top surface of the silicon substrate ("principal surface") to the bottom of the wells, as illustrated in Figure 17 (below right). Ex. 1007, 5:41-45, 8:46-52, 14:46-15:6, 15:26-40, 15:62-16:40, FIG. 16.



Ex. 1007, FIGS. 23, 17.

162. A side-by-side association of Sakai's "twin double well" structure Figure 10D with Kawagoe's dopant profile Figure 17 illustrates an example of Sakai's high-to-low dopant concentration implemented in accordance with Kawagoe's teaching that the overall dopant profile should be "gradually lowered in the depthwise direction." Ex. 1007, 15:62-16:7.



Ex. 1006, FIG. 10D; Ex. 1007, FIG. 17 (excerpted); Ex. 1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

163. In my opinion, Sakai's high-to-low dopant concentration across deep N-well 3 (right side of Figure 10D) implemented in accordance with the same teachings of Kawagoe would similarly result in a gradual downward-sloping profile. Accordingly, Sakai-Kawagoe meets a single drift layer having a downward-sloping graded concentration of dopants extending between the surface layer and the substrate. *Id.*

164. **<u>Motivation to combine Sakai and Kawagoe</u>** - In my opinion, a POSITA would have been motivated to combine Sakai and Kawagoe for numerous reasons. Both are Hitachi patents. Ex. 1006, cover; Ex. 1007, cover. Both are directed to CMOS devices that were (and still are) "widely used" to form memories and microcomputers because of their "low [] power dissipation" and because CMOS

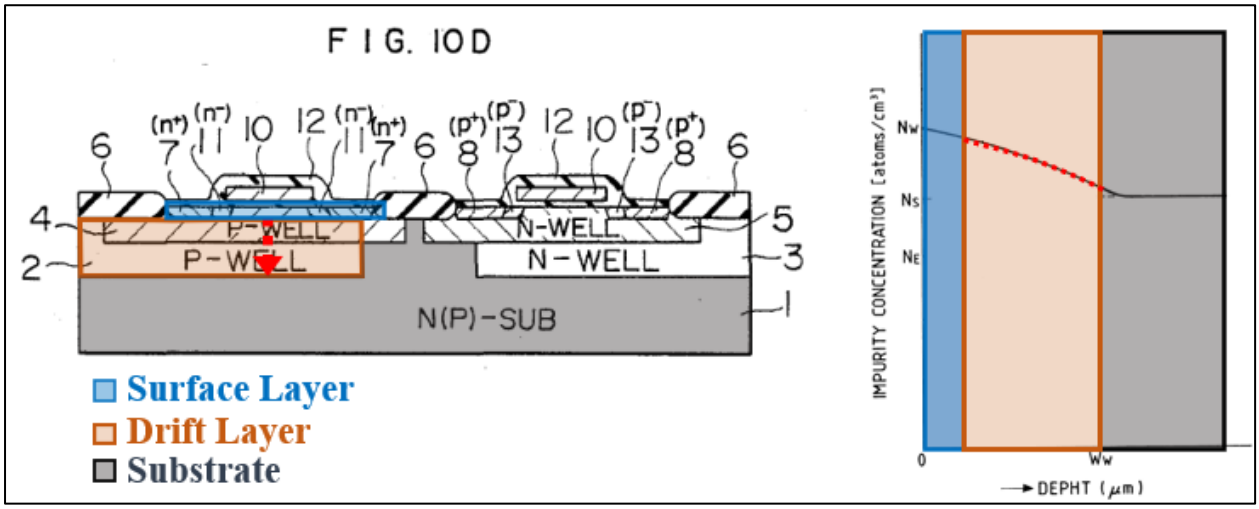
devices "can operate at high speed." Ex. 1006, 1:7-17, Ex. 1007, 3:32-38, 19:15-16, 20:1-8, 21:5-12, 22:14-21, 24:28-31.

165. Sakai teaches improving the circuit density (packing density) of CMOS chips by disposing shallow wells into deep wells of a "twin-well" CMOS device to form a "twin double well" structure (nested well structure). Ex. 1006, 1:55-2:5, 7:19-37, 8:9-24, FIGS. 2A, 10D, 15.

166. Sakai's "twin double well" structure is used to form high-packing-density memory devices, including SRAM memory devices illustrated in Figure 15 and discussed in Kawagoe. *Id.*, 7:24-37 ("[CMOS] static memory of…6 MOS transistors"); Ex. 1008B, 572-573 ("SRAMS… are… static memories), FIG. 8-2 (CMOS SRAM cell); Ex. 1007, 21:5-12, FIG. 27(B). High-packing-density SRAMs are susceptible to soft errors. Ex. 1008B, 583 ("SRAMs offer better resistance than DRAMs to [soft-errors] … However, as geometries have been scaled down to produce circuits of greater density, alpha-particle-induced soft-error rates have also become a concern in SRAMs.").

167. Thus, in my opinion, a POSITA would have been motivated to apply Kawagoe's teachings directed to protecting memories against alpha-particle-induced soft errors to Sakai's twin double well structure (including for SRAM memory). A POSITA would have engineered the dopant profile across each of Sakai's single drift layers (tan) so that it is downward-sloping from the top surface of the silicon

substrate to the bottom of the deep well—as illustrated in the dopant profile at right—because Kawagoe teaches that such a profile causes alpha-particle-generated minority carriers to move to the substrate. Ex. 1007, 16:2-11 (the "gradient [in the p-well] is ***gradually lowered*** in the depthwise direction" and, as a result, "electrons produced by the α-ray are attracted to the substrate body 2S by that concentration gradient … so that the soft errors can be reduced…."), 21:20-23.



Ex. 1006, FIG. 10D; Ex. 1007, FIG. 17 (excerpted); Ex. 1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

168. Such a downward-sloping dopant profile is consistent with Sakai's teachings of (1) higher dopant concentration in the shallow wells compared to the deep wells, and (2) the use of ion implantation followed by thermal drive-in, which naturally results in a non-uniform, graded-dopant concentration, discussed above. Ex. 1006, 5:56-6:4.

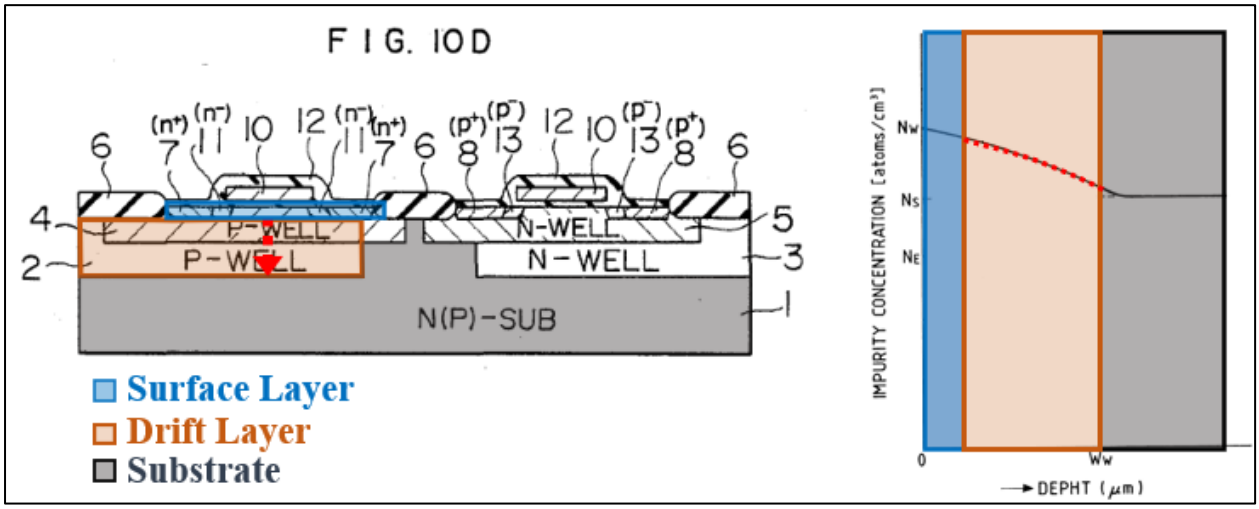
169. In my opinion, there is a reasonable expectation of success because it was well-known that various ion-implantation and thermal drive-in processes enable different dopant profiles to be readily engineered and fabricated as needed, Ex. 1008A, 371, 373 ("Complex-doping profiles can be produced" using ion implantation), and because the prior art is replete with teachings on how to form downward-sloping dopant concentrations, as in Kawagoe, Payne, Jastrzebski and Wieczorek.

170. Further, the '195 Patent specification mentions various dopant gradients (including ones with a one-way slope, e.g., quasi-linear) and does not illustrate or otherwise describe how to make them, confirming that such gradients were well-known and, in my opinion, a POSITA would have known how to manufacture a CMOS device having them. Ex. 1001, 2:40-42. Accordingly, a POSITA would have equally known how to implement a single drift layer in Sakai to result in a known downward-sloping graded-dopant concentration profile.

171. In my opinion, this combination also merely amounts to (1) combining prior art elements (Sakai's CMOS device and Kawagoe's dopant profile) according to known methods (well-known ion implantation and thermal drive in techniques) to yield predictable results and (2) use of a known technique (creating Kawagoe's profile) to improve similar devices (Sakai's CMOS devices) in the same way (to reduce soft errors).

f. Element [1.5]: "said drift layer further having a first static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate; and"

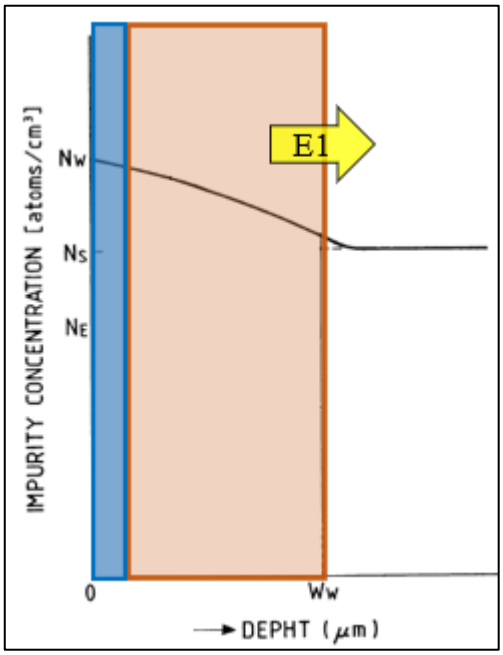
172. In my opinion, Sakai-Kawagoe renders obvious this element. As discussed above with regard to element [1.4], Sakai-Kawagoe renders obvious a single drift layer (tan) having a downward-sloping dopant concentration extending between the surface layer (blue) and the substrate (grey), similar to Kawagoe Figure 17 below. Section X.B.1.e.



Ex. 1006, FIG. 10D; Ex. 1007, FIG. 17 (excerpted); Ex. 1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

173. Thus, according to Section X.A.1.f—including Applicant's repeated representations to the Patent Office and the Jastrzebski and Kamins cited art relied on by Applicant—such a downward-sloping graded-dopant concentration creates a "built-in" unidirectional electric drift field (illustrated "E1" below) to aid the

movement of minority carriers from the surface layer to the substrate. *See* Section X.A.1.f; *see also* ¶¶104-105.



Ex. 1007, FIG. 17 (excerpted).

174. Such a profile is created "through ion implantation techniques and thermal diffusion techniques" and thus the profile (and any resulting electric drift field) is static—it is set once the CMOS device has been fabricated and does not change afterwards. Ex. 1006, 5:56-6:4, 6:24-28, 6:52-58, 8:35-38; Section X.A.1.f. As discussed in Section X.A.1.f, Applicant described "static" similarly during prosecution. Ex. 1002, 318 (citing Ex. 1009), 333 (same).

175. In light of the above, it is my opinion that Sakai-Kawagoe satisfies Element [1.5] under Patent Owner's plain-meaning constructions. Section VIII. Sakai-Kawagoe's graded-dopant concentration is downward-sloping over the entire

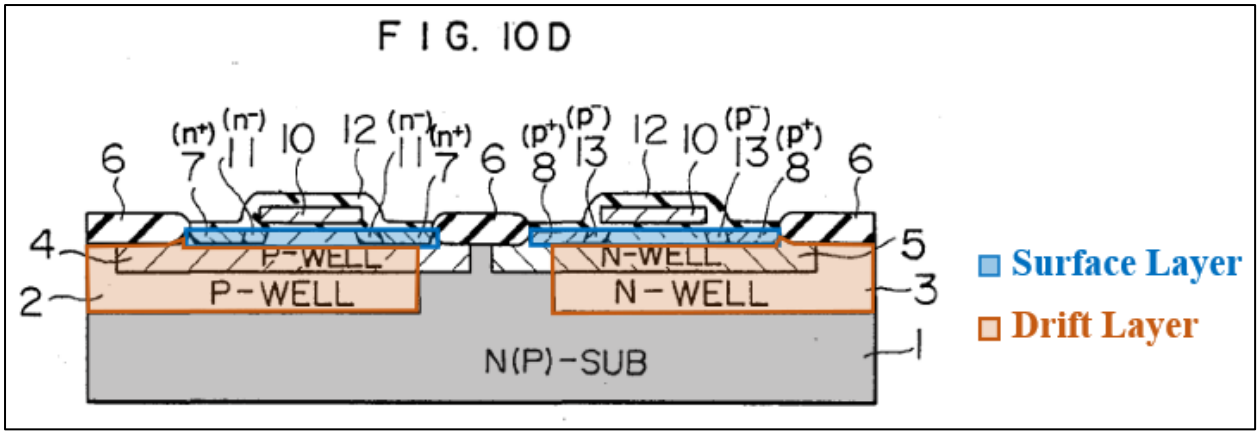
single drift layer (tan)—in fact, from the top of the silicon/surface layer (blue) to the bottom of the single drift layer—and thus, according to Patent Owner (and also in light of Applicant's representations to the Patent Office discussed above), creates a static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Ex. 1007, FIG. 17.

176. For the same reasons, in my opinion, Sakai-Kawagoe satisfies Petitioner's construction that the first static unidirectional electric drift field must be "unidirectional ***over*** the drift layer," and also satisfies Petitioner's alternative proposed construction of the sub-phrase "to aid the movement of minority carriers from said surface layer to said substrate" to mean "to sweep the minority carriers from said surface layer to said substrate." *Id.*, Section VIII; Section X.A.1.f; Ex. 1002, 289-290.

g. Element [1.6]: "at least one well region disposed in said single drift layer, said well region having a graded concentration of dopants and a second static unidirectional electric drift field to aid the movement of minority carriers from said surface layer to said substrate."

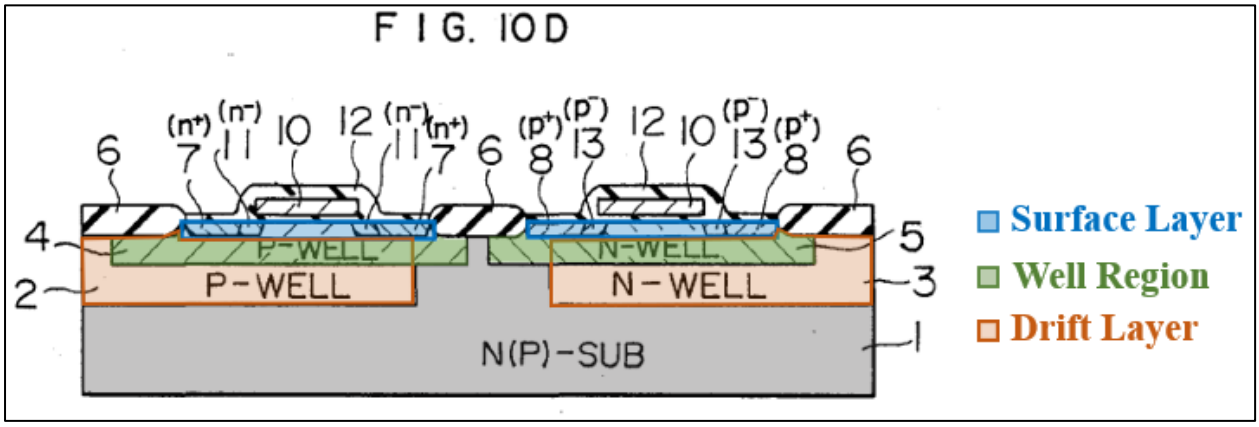
177. In my opinion, Sakai-Kawagoe renders obvious this element.

178. **Well region disposed in said single drift layer…having a graded concentration of dopants** – As detailed above, Sakai-Kawagoe renders obvious a single drift layer (deep P-well 2 or deep N-well 3) (tan), as shown below. Ex. 1006, 5:56-6:4. Sections X.B.1.e-f.



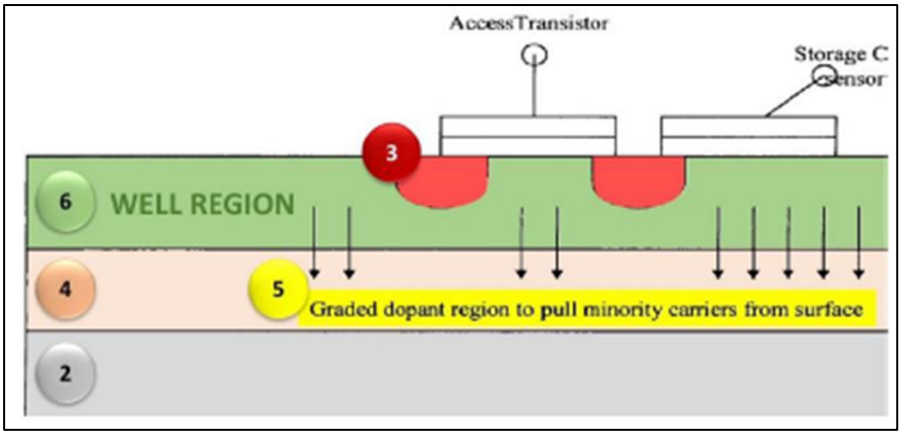
Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

179. Each shallow well in Sakai's nested well structures ("twin double wells")—*e.g.,* the **"shallow P-well region 4"** (left) or **"shallow N-well region 5"** (right)—is an example of a well region (green) disposed in a single drift layer (tan). Ex. 1006, 1:57-67, 5:56-6:4, 7:32-37.

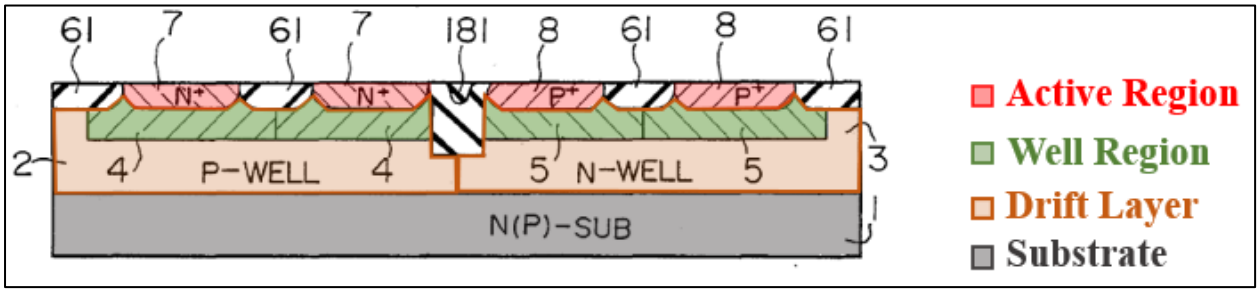


Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

180. Notably, Sakai-Kawagoe satisfies element [1.6] to the same extent that Figure 5(b) of the '195 Patent, annotated by Patent Owner in its claim construction brief, meets it:

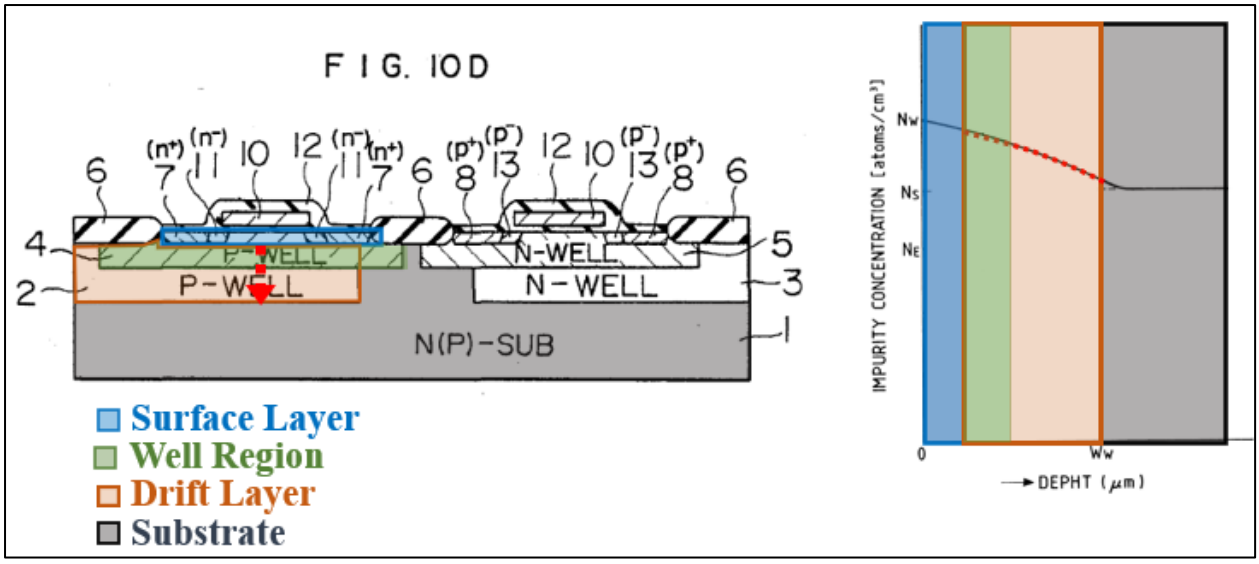


Ex. 1001, FIG. 5(b); Ex. 1030, 7. In my opinion, if Patent Owner argued that the well region must be entirely contained within the single drift layer, Sakai discloses that too. *See, e.g.,* Ex. 1006, FIGS. 2A, 11E (below), 3, 8-9, 16.



Ex. 1006, FIG. 11E, 6:52-58.

181. Further, in my opinion and as also detailed above with respect to element [1.4], Sakai-Kawagoe's structure has a downward-sloping graded-dopant concentration extending between the surface layer and the substrate, such that each well region (e.g., shallow well 4) (green) also has such downward-sloping graded-dopant concentration. Ex. 1007, 15:62-16:7 (dopant "concentrations gradually lowered in the depthwise direction from the principal surface"); Section X.B.1.e.



Ex. 1006, FIG. 10D; Ex. 1007, FIG. 17 (excerpted); Ex. 1006, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

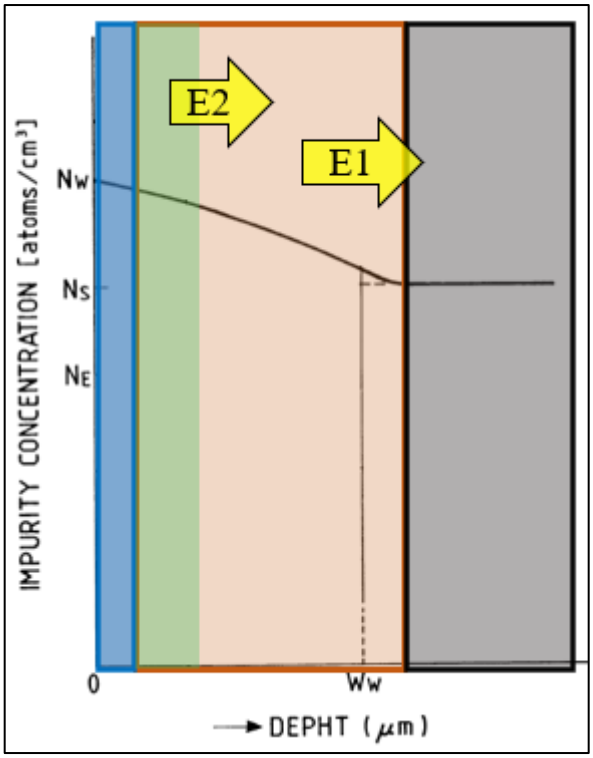
182. In light of the above, it is my opinion that Sakai-Kawagoe satisfies element [1.6] under Patent Owner's construction that the term "well region" means "a doped region that surrounds the active region of a semiconductor device." Section VIII.

183. As shown in Sakai's Figure 10D (with graded-dopant concentration shown in Kawagoe's Figure 17) above, the exemplary shallow well region (green) is a doped region that surrounds both the surface layer (blue) and the active region therein. Section X.B.1.d. In my opinion, Sakai-Kawagoe also satisfies Petitioner's proposed constructions of this term. Section VIII. The mapping of "well region" to each shallow well 4/5 satisfies Petitioner's construction because they are formed

with an ion implant of P-type or N-type impurities. Ex. 1006, 5:64-6:4, 6:52-58; Section VIII.

184. **Second static unidirectional electric drift field to aid the movement of minority carriers** – According to Section VIII.A.1.f—including Applicant's repeated representations during prosecution, and according to the Jastrzebski and Kamins prior art relied on by Applicant during prosecution, and Patent Owner's statements in its claim construction brief—the downward-sloping graded-dopant concentration in each of these well regions creates a (second) static unidirectional electric drift field that aids the movement of minority carriers from the surface layer to the substrate. Section X.A.1.f. Further, Sakai-Kawagoe's graded-dopant profile, including the profile in the well region, is set once the device has been fabricated and does not change, making the profile (and any resulting electric field) static, as described in Section X.B.1.f.

185. I have further annotated Kawagoe's Figure 17 below to show the exemplary first static unidirectional electric drift field ("E1") described in Section X.A.1.f, at a depth corresponding to Sakai's deep well (tan), and an exemplary second static unidirectional electric drift field ("E2"), at a depth corresponding to Sakai's shallow well (green) (exemplary well region disposed in the single drift layer). *See* ¶¶104-105.



Ex. 1007, FIG. 17 (excerpted). Moreover, I have illustrated E1 and E2 as electric fields having different magnitudes, to reflect the different local slopes (gradients) of the dopant profile. Ex. 1022, [0071] ("the vertical €-field is established by the rate of change in the graded dopant concentration, i.e., the greater the rate of change … the greater the intensity of the €-field.").

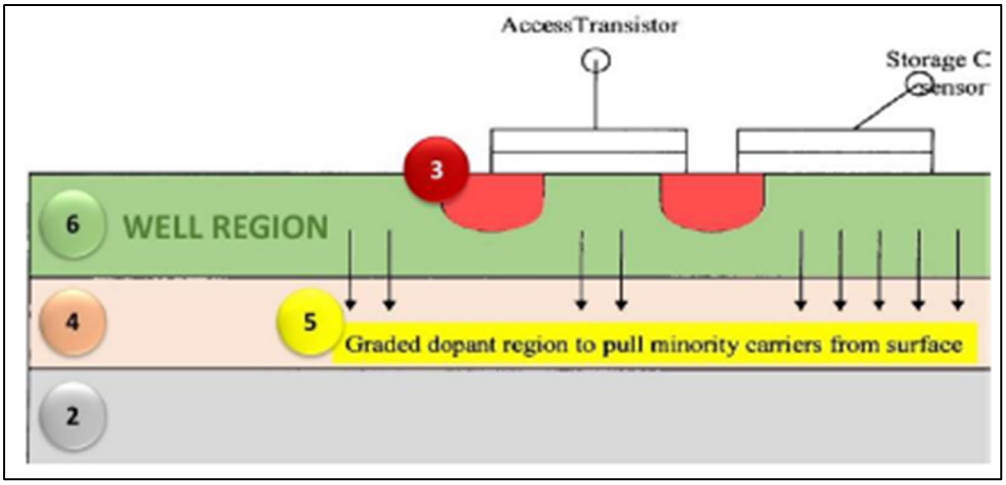
186. In light of the above, it is my opinion that Sakai-Kawagoe satisfies element [1.6] under Patent Owner's plain meaning construction of "to aid the movement of minority carriers." Section VIII. As shown in Kawagoe Figure 17 above, Sakai-Kawagoe's graded-dopant concentration is downward-sloping over the entire well region, and thus, according to Patent Owner (and also in light of Patent Owner's representations to the Patent Office, discussed in Section X.A.1.f), creates

a static unidirectional electric drift field that aids the movement of minority carriers downward from the surface layer to the substrate.

187. For the same reasons, it is my opinion that Sakai-Kawagoe also satisfies this element under Petitioner's construction that the second static unidirectional electric drift field must be "unidirectional over the well region," and also satisfies Petitioner's alternative proposed construction that the term "to aid the movement of minority carriers" means "to sweep the minority carriers from said surface layer to said substrate." Section VIII; Section X.A.1.f; Ex. 1002, 289-290.

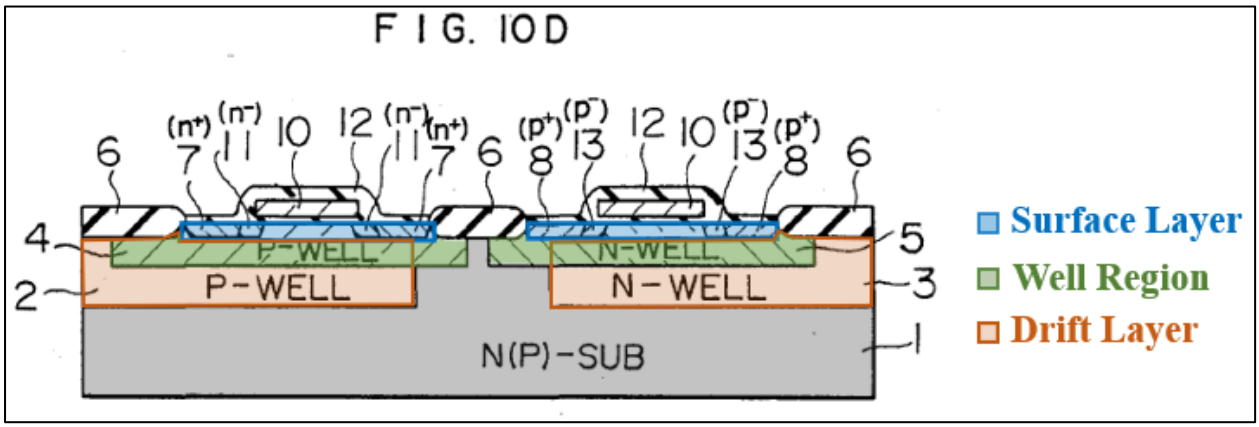
2. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

188. In my opinion, Sakai renders obvious the additional limitation of claim 2. As discussed in Section X.A.2, the only mention of a "deeply-implanted layer" in the '195 Patent is a suggestion that the "subterrain n^- layer" (tan) in Patent Owner's annotated Figure 5(b) below "can be a deeply-implanted layer." Ex. 1001, 3:33-38. The specification does not discuss the depth of this "deeply-implanted layer" or the process for forming such a layer.



Ex. 1001, FIG. 5(b); Ex. 1030, 7.

189. As detailed above in Section X.B.1, Sakai teaches a nested well structure that matches Figure 5(b) of the '195 Patent. Section X.B.1.e-g.



Ex. 1006, FIG. 10D; *id.*, FIGS. 2A, 3, 8-9, 11A-11E, 15-17.

190. Sakai explicitly teaches that its lower wells (tan above) are "***deep***" wells formed through "ion ***implantation*** techniques." *Id.*, 3:53-58 ("***deep*** P-well region 2" and "***deep*** N-well region 3"), 5:56-61 ("P-well region 2 and an N-well region 3…are formed…through ion implantation techniques"), 6:24-31. These wells have "a depth of 3 to 5 µm." *Id.*, 3:58-59, 5:56-61; Ex. 1008A, 403. Each of Sakai's deep wells

(*e.g.*, deep P-well region 2 (tan)) is a deeply-implanted layer to the same extent Figure 5(b) of the '195 Patent shows a deeply-implanted layer.

3. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein said drift layer is an epitaxial layer."

191. In my opinion, Sakai-Kawagoe renders obvious claim 3. Sakai is directed to the fabrication of CMOS devices, which are susceptible to latchup failures, as was well-known in the art. Ex. 1006, 1:6-13; Ex. 1008B, 400 ("A major problem in CMOS circuits is the inherent, self-destructive phenomenon known as *latchup* …[which] can cause the circuit to cease functioning or even to destroy itself …").

192. It was also well-known that placing NMOS and PMOS transistors closer together (Sakai's core objective) has the drawback of increased latchup susceptibility. Ex. 1006, Abstract, 1:55-56, 3:3-7, 7:28-37; Ex. 1008B, 381. Thus, while not discussed in Sakai, in my opinion a POSITA would have understood that a high-packing-density CMOS device according to Sakai's teachings would require latchup protection.

193. In my opinion, a POSITA would have known that using a lightly doped epitaxial layer over a bulk substrate, is effective to reduce latchup susceptibility. Ex. 1007, 1:33-40, 15:7-17; Ex. 1008B, 385, 414. The POSITA would thus have been motivated to look to Kawagoe, which teaches the manufacturing of twin-well CMOS devices (Ex. 1007, 3:32-38, 4:46-55, 15:26-40, FIGs. 20-24), the same type of

CMOS devices taught in Sakai (Ex. 1006, 1:6-13, 7:18-23) using epitaxial wafers to improve latchup resistance, in ways that also reduce manufacturing costs.

194. Combining Kawagoe's epitaxial substrate with Sakai is critical to provide Sakai's devices with improved latchup resistance, and in my opinion, there was a reasonable expectation of success because Kawagoe shows a POSITA knew how to use epitaxial substrates to make CMOS devices similar to Sakai's, especially given that epitaxial substrates were widely-used in building twin-well CMOS devices. Ex. 1008A, 226-27; Ex. 1008B, 387-388. Using an epitaxial substrate in Sakai would also have been a simple substitution of one known element (Kawagoe's epitaxial substrate) for another (Sakai's general substrate) to obtain predictable results (Sakai's device with reduced latchup risk and lower cost) (Ex. 1007, 1:33-40, 15:7-17; Ex. 1008B, 385, 414), and would have been use of a known technique (use of an epitaxial layer) to improve a similar device (Sakai's device) in the same way (to reduce latchup risk and lower cost). *Id*.

195. Sakai-Kawagoe would result in forming Sakai's deep n- and p-wells, each of which is an exemplary single drift layer, in the epitaxial portion of Kawagoe's epitaxial substrate, and thus Sakai-Kawagoe's single drift layer is an epitaxial layer. Indeed, Sakai's deep n- and p-wells have "a depth of 3 to 5 μm" (Ex. 1006, 5:56-61), whereas Kawagoe teaches that the "preferred" thickness of the epitaxial layer of its low-cost epitaxial substrate can be as high as 5μm, and that

epitaxial layers up to 3μm thick were "frequently employed[.]" Ex. 1007, 8:36-39; 15:23-25.

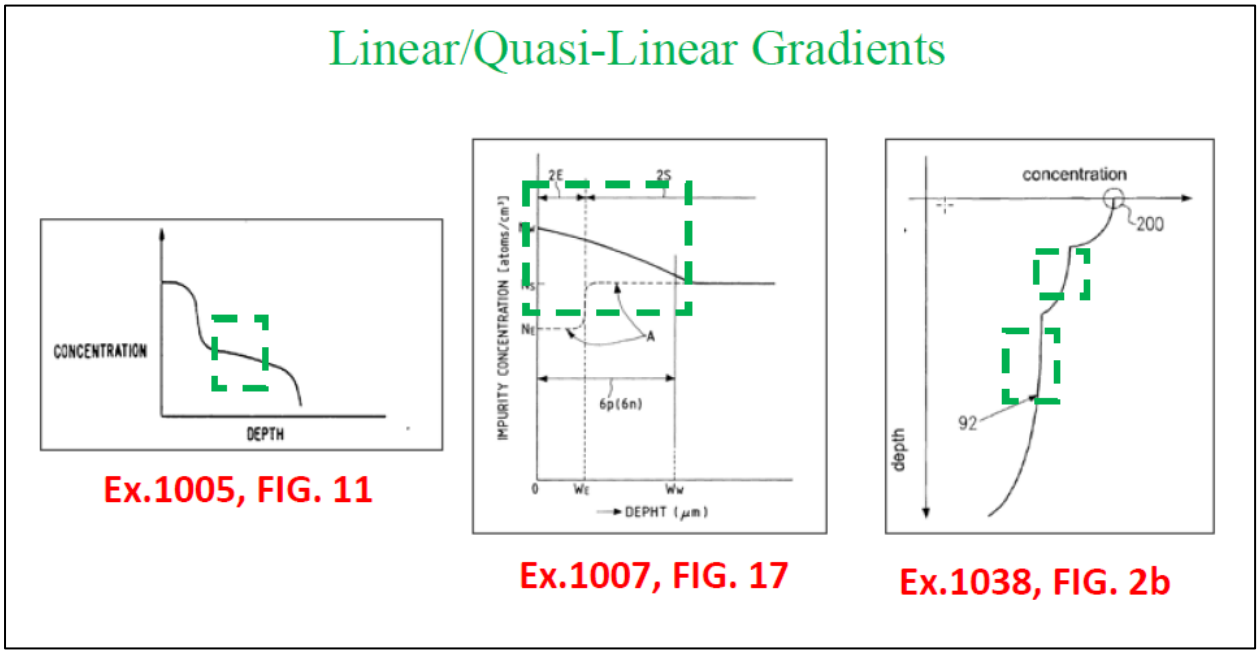
196. In my opinion, a POSITA would have understood that Sakai-Kawagoe's single drift layer (formed by one or more deep wells) can be as thick as the epitaxial layer of the substrate. Ex. 1008B, 386 ("The epitaxial layer is made thicker than the well depth … The process is designed so that the bottom of the well [tub] is eventually adjacent to the heavily doped substrate region.").

197. Even if Sakai-Kawagoe would result in deep wells that extend beyond the thickness of the epitaxial layer, the epitaxial portion of each deep well would correspond to a single drift layer that meets the claimed epitaxial layer, while lower non-epitaxial portions of the deep wells are considered part of the claimed substrate.

4. Dependent Claims 4 and 5: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a linear gradient"; "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows a quasi-linear gradient."

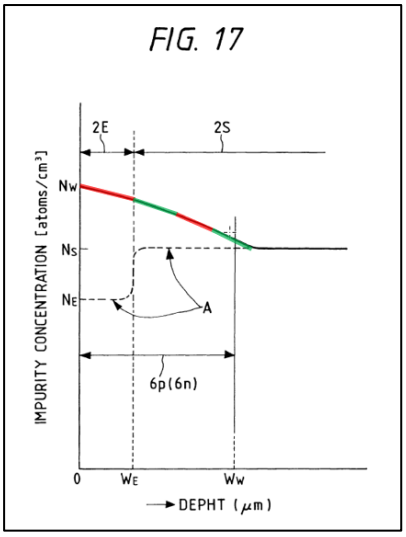
198. In my opinion, Sakai-Kawagoe renders obvious claims 4 and 5. The '195 Patent does not describe how to make linear/quasi-linear gradients, confirming implementing them in CMOS devices was well-known. Ex. 1001, 2:40-42; Section X.A.3. The '195 Patent also lists linear/quasi-linear among a few likewise well-known gradients without giving any reason to use one over another. Ex. 1001, 2:40-42.

199. Three out of the four exemplary profiles described in Section X.B.1.e have a downward-sloping graded-dopant concentration that follows a linear or nearly-linear (quasilinear) gradient, as shown below. Ex. 1040, 437 (defining "quasi-linear" terms as "substantially linear").



Ex. 1005, FIG. 11; Ex. 1007, FIG. 17; Ex. 1038, FIG. 2b.

200. Sakai-Kawagoe would have had a downward-sloping graded-dopant concentration that follows a linear or nearly-linear (quasilinear) gradient, as shown in Kawagoe's Figure 17 below. For example, Kawagoe's graded-dopant profile follows a linear/quasilinear gradient along segments that are linear/quasilinear, as illustrated below with individual green/red segments, with smaller segments becoming even more linear/quasilinear.

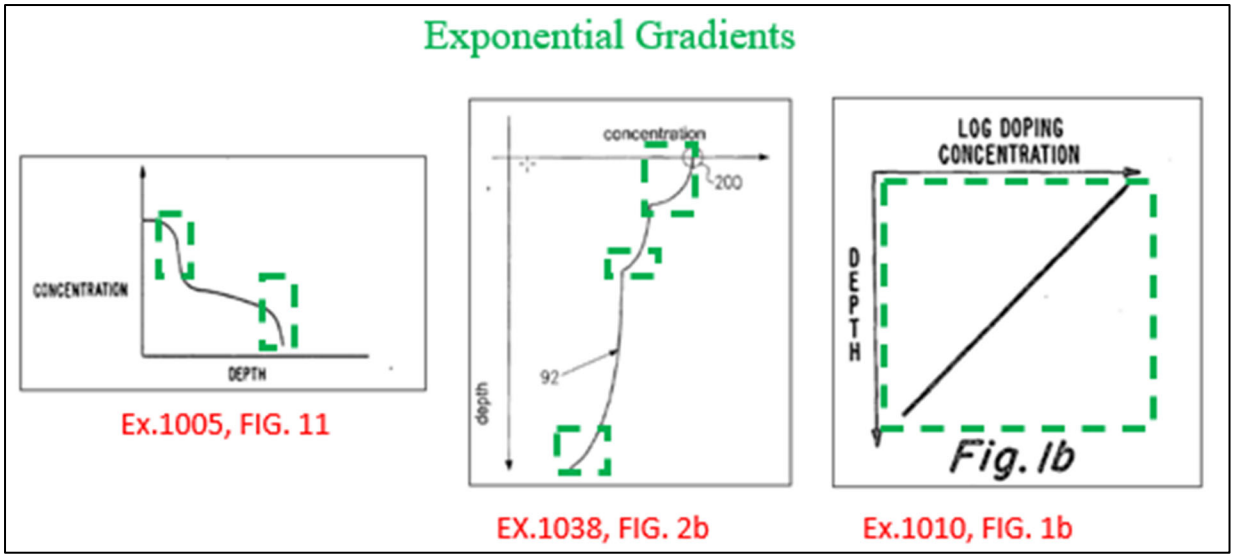


Ex. 1007, FIG. 17.

5. Dependent Claim 6: "The CMOS Semiconductor device of claim 1, wherein said graded concentration follows an exponential gradient."

201. In my opinion, Sakai-Kawagoe renders obvious claim 6. The '195 Patent specification does not describe how to make "exponential" gradients, confirming implementing them in CMOS devices was well-known. Ex. 1001, 2:40-42; Section X.A.4. The '195 Patent also lists exponential among a few likewise well-known gradients without giving any reason to use one over another. Ex. 1001, 2:40-42.

202. Dopant profiles with exponential gradients were well-known and obvious. For example, three of the four exemplary profiles described in Section X.B.1.e have a downward-sloping dopant profile that follows an exponential gradient, as shown below. Ex. 1028, 337 (defining "exponential" as "more and more rapid").



203. And, as described above in Section X.A.5, while Jastrzebski's figure 1b appears linear, Jastrzebski explains, as indicated in the figure, that "FIG. 1b is a graph of the ***logarithm*** of doping concentration versus depth." Ex. 1010, 5:25-27. In my opinion, a POSITA would have understood that Jasztrebski's logarithmic dopant profile follows a rapidly changing, exponential gradient.

204. In my opinion, it would have been obvious to modify the downward-sloping graded-dopant profile of Sakai-Kawagoe based on the POSITA's general knowledge in the art to achieve a known exponential gradient as in Payne's, Wieczorek's, or Jastrzebski's graded-dopant profile. This would have been obvious to try as one of a finite number of known gradients to use for a downward-sloping graded-dopant profile and would have also been a simple substitution of one known element (Kawagoe's downward-sloping graded-dopant profile) for another (a known downward-sloping graded-dopant profile following an exponential gradient)

while retaining the same known benefit of aiding minority carrier movement (Sections X.B.1.f-g; Ex. 1007, 16:2-11). There was reasonable expectation of success as Payne, Wieczorek, and Jastrzebski all show that a POSITA knew how to implement such a profile.

205. Indeed, it was well-known that the ion-implantation process described in Sakai is a versatile process that enables different dopant profiles to be readily engineered and fabricated as needed. Ex. 1006, 5:56-6:4, 6:24-28, 6:52-58; Ex. 1008A, 371, 373 ("Complex-doping profiles can be produced" using ion implantation).

C. Ground III

206. In my opinion, Payne in combination with Wolf renders claims 2 and 3 obvious. Payne is directed to CMOS devices. Ex. 1005, 1:5-10, 1:51-54, 6:57-59. Wolf is a well-known textbook that teaches fundamental features and concepts related to semiconductor manufacturing, with particular emphasis on CMOS. *See generally* Ex. 1008A; *id*., Chapter 16 ("CMOS Process Integration"). Wolf also published over 20 years after Payne was filed. Exs.1014-15. A POSITA would have therefore understood and expected that the teachings of Wolf would apply to Payne, and would have looked to Wolf for advances in CMOS technology and additional process details to the extent not covered in Payne. *Id*.

1. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

207. In my opinion, Payne in combination with Wolf (hereinafter, "Payne-Wolf") renders claim 2 obvious. As described in Section X.A.2, Payne teaches forming its nested well structures with tub regions 15/17 (single drift layers) which are deeps wells formed by ion implantation and drive-in annealing, extending 3-8μm deep. Ex1005, 5:48-50, 3:28-42, 4:3-25, Ex. 1008A, 403.

208. While Payne describes implanting ions at an initial, as-implanted, depth of 400-500 Angstroms (Ex. 1005, 3:39-41, 4:14-16), Wolf teaches using high-energy ion-implantation ("MeV implantation") to implant ions deeper (as-implanted depth of "~1-2 μm") for CMOS wells and minimize damage to surface structures. Ex. 1008A, 406-407 ("A key advantage of MeV implantation is that most of the ion damage is confined within the ion range distribution, ***which is buried deep to a region near the bottom of the CMOS wells***, so that near-surface regions (such as the transistor channel), are relatively undisturbed."), 830 ("The well formation step employs ***high-energy ion implantation*** to locate the well dopant peak ***~1-2 μm*** below the Si surface."), Table 10.2 ("Key Application" of high-energy ion implantation is "CMOS Wells"). Rubin confirms that it was known to implant ions even deeper. Ex. 1041, 567-68 (as-implanted depths beyond 3μm using a high-energy implanter), FIGS. 1-7.

209. Wolf also teaches using "multiple-energy implants" to establish a desired dopant depth profile. Ex. 1008A, 371 ("Ion implantation is superior" for many reasons, including that "***Depth profiles of the implanted species can be established*** … This capability can be extended to produce the depth profiles needed in complex applications by using ***multiple-energy implants***."), 373 ("Complex-doping profiles can be produced" using multiple ion implants). Indeed, high-energy ion-implantation was used in CMOS processes "to set doping levels in the wells." Ex. 1008A, 423-424 (section heading "High-Energy Implantation").

210. Accordingly, in my opinion, a POSITA would have been motivated to use high-energy implantation technology to form Payne's tub regions 15/17 as deeply-implanted layers to realize the benefits of avoiding damage to critical near-surface structures while establishing a desired dopant profile.

211. In my opinion, this combination also merely amounts to (1) combining prior art elements (Wolf's high-energy implantation technique and Payne's CMOS structure) according to known methods (using known high-energy implantation techniques to shape depth profiles as evidenced by Wolf) and (2) use of a known technique (Wolf's high-energy implantation) to improve similar devices (Payne's CMOS devices) in the same way (to avoid near-surface damage and establish depth profile).

212. A POSITA would also have had a reasonable expectation of success with predictable results using high-energy ion-implantation systems and processes to form Payne's deep wells because, as discussed above, Wolf and Rubin show that POSITAs knew how to use high-energy ion implantation to form CMOS wells and establish a desired dopant depth profile.

213. Additionally, Wieczorek illustrates the use of multiple-energy implants to form a desired dopant profile, described in Wolf. Ex. 1038, FIGS. 1a, 2a-2b; Ex. 1008A, 406. Wieczorek Figure 2b (below right) illustrates a graded-dopant profile formed by the four well implants shown in Figure 2a (below left) followed by an annealing step. Ex. 1038, [0007]-[0011], FIGS. 1a, 2a-b; *id.,* FIG. 4.

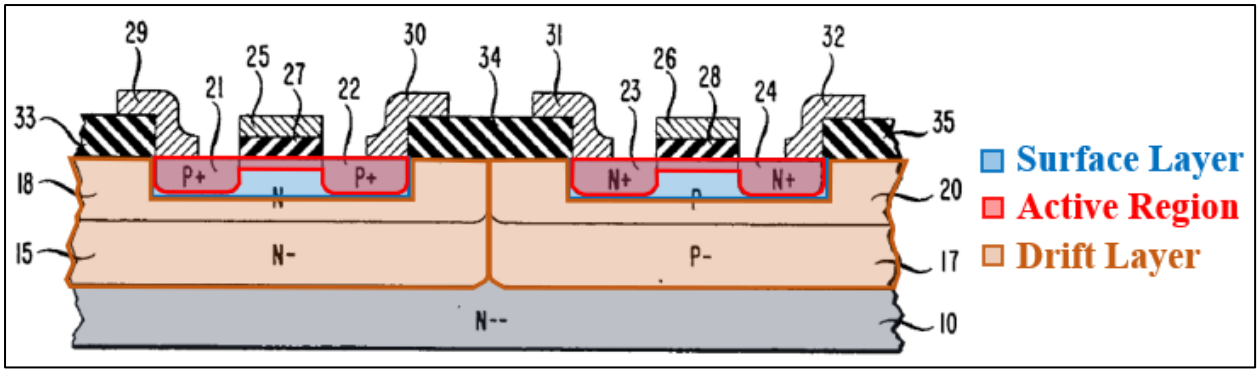
214. In Figure 2a, at least the "buried implant" (also shown in FIG. 1a) is a deep, high-energy ("400-800KeV"), well implant. *Id.*, [0028]-[0029]; Ex. 1008A, 423 ("High-Energy Implantation" - "[T]he doping of CMOS well junctions requires ion energies ranging from a few hundred KeV to several MeV"); Ex. 1041, Abstract ("High energy implantation of dopant atoms is used to form ***buried layers*** [that] have many potential applications, including triple wells …").

Ex. 1038, FIGS. 2a-b. Wieczorek explains that the implantation profiles in Figure 2a are "smeared out" by the annealing process, resulting in the composite downward-sloping graded-dopant profile shown in Figure 2b. *Id.*, [0009]-[0010].

2. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein said drift layer is an epitaxial layer."

215. In my opinion, Payne-Wolf renders claim 3 obvious.

216. Payne is directed to improving twin-well ("twin-tub") CMOS technology by adding a shallow well ("surface region") in each deep well ("tub") (serving as a single drift layer) of a twin-well CMOS device, as shown below. Ex. 1005, 1:5-14, 1:59-2:28, 6:20-21; *id.*, 1:15-50; Section X.A.1.e.



Ex. 1005, FIG. 10.

217. This nested well structure allowed transistors to be closer to improve packing density. *Id.*, Abstract, 1:51-54, 6:17-19, 6:57-59. That however has the drawback of increased latchup susceptibility. Ex. 1008B, 381. Thus, a POSITA would have understood that a high-packing-density CMOS device according to Payne's teachings would require latchup protection.

218. In my opinion, a POSITA would thus have been been motivated to fabricate Payne's device using an epitaxial substrate to protect it against latchup failures. Ex. 1008B, 385 ("CMOS on Epitaxial Substrates"; "[H]eavily doped substrates with a more lightly doped surface epitaxial layer have been utilized to ***suppress latchup*** in CMOS."), 387-88 ("With the twin-tub approach, two separate wells are formed for *n*- and *p*-channel transistors [as taught in Payne]. The substrate may be either a lightly doped wafer of *n* or *p* material, ***or a thin, lightly doped epitaxial layer on a heavily doped substrate***.").

219. A POSITA would have had a reasonable expectation of success, in my opinion, because Wolf shows that a POSITA knew how to use n-type epitaxial substrates to implement twin-well CMOS devices similar to Payne's. *Id.*, 389. Combining Wolf with Payne in this manner would have been the use of a known technique (using epitaxial substrate to make CMOS devices) to improve similar devices (Payne's twin-tub CMOS devices) in the same way (with improved latchup resistance), and a simple substitution of one known element (n- epitaxial substrate) for another (Payne's n-- substrate) to obtain predictable results.

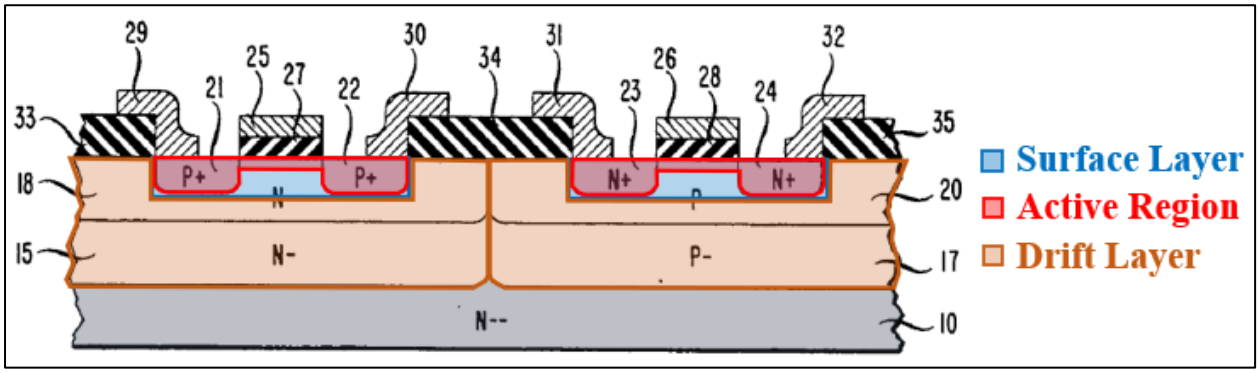
220. In my opinion, a POSITA would also have understood that, when Payne's "twin tub" CMOS device is fabricated using an epitaxial substrate, its single drift layer (tub, especially tub less than 4μm deep) is entirely epitaxial and, moreover, can be as thick as the epitaxial layer of the substrate. Ex. 1005, 5:48-50; Ex. 1008A, Table 7-1 at 228 ("commonly used" epi thickness in CMOS devices is 2-4μm); Ex. 1008B, 386 ("The epitaxial layer is made thicker than the well depth … The process is designed so that the bottom of the well [tub] is eventually adjacent to the heavily doped substrate region.").

D. Ground IV

1. Dependent Claim 3: "The CMOS semiconductor device of claim 1 wherein said drift layer is an epitaxial layer."

221. In my opinion, Payne in combination with Parrillo renders claim 3 obvious. Payne is directed to improving twin-well ("twin-tub") CMOS technology

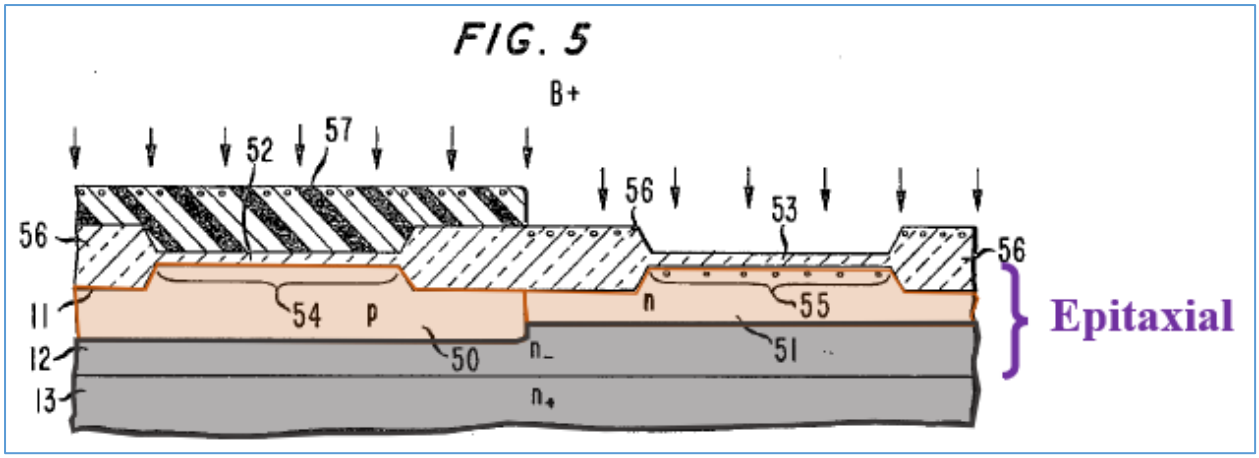
by adding a shallow well ("surface region") in each deep well ("tub") of a twin-well CMOS device. Ex. 1005, 1:5-14, 1:59-2:28, 6:20-21; *id.*, 1:15-50; Section X.A.1.e. This nested well structure allowed transistors to be closer to improve packing density. *Id.*, Abstract, 1:51-54, 6:17-19, 6:57-59. As an example, Payne describes its devices fabricated in a "silicon semiconductor substrate [] of 'N--' conductivity type …", as shown below. *Id.*, 2:50-60.



Ex. 1005, FIG. 10.

222. Parrillo is a contemporaneous patent that shares a common inventor (Richard S. Payne) with Payne and, like Payne, was originally assigned to AT&T Bell Labs. Ex. 1025; Ex. 1005.

223. Parrillo teaches a CMOS device with twin-tubs 50 and 51 (tan) formed in an epitaxial layer 12 (purple) of Parrillo's epitaxial substrate (12+13, grey). Ex. 1025, 3:19-41, 3:45-4:14 ("tubs 50 and 51 are [] driven to a depth of 5-6 µm"), 3:28-33 (the epitaxial layer 12 is "10-20 µm thick").



Ex. 1025, FIG. 5; Ex. 1026, FIG. 1(e).

224. In my opinion, a POSITA would have been motivated to fabricate Payne's "twin-tub" device using Parrillo's epitaxial substrate to protect Payne's high-density CMOS device, which POSITAs knew were susceptible to latchup failures due to the close proximity of their transistors. Ex. 1008B, 381; Ex. 1025, 3:38-41 ("The use of a relatively lightly doped (n-) epitaxial layer on a relatively doped (n+) substrate provides ***protection against SCR latch-up*** in the device."); Ex. 1008B, 414 ("The use of lightly doped epitaxial layers on heavily doped substrates is effective in reducing latchup susceptibility …").

225. A POSITA would have had a reasonable expectation of success with predictable results because, as shown by Parrillo and Wolf, POSITAs knew how to use an n-type ***epitaxial*** substrate for latchup protection in a "twin-tub" (twin-well) CMOS device. Ex. 1025, 1:13-33, 2:21-24, 3:28-41; Ex. 1008B, 385, 387-89; Ex. 1026 (Parrillo2), Abstract ("The combination of ***n on n$^+$ epi*** and careful I/O layout

renders the circuits ***latch-up free***."); Ex. 1023, 192-193 (discussing the use of n-type epitaxial substrate to improve latchup resistance in twin-well CMOS devices, citing Parrillo2), 196. Forming Payne's single drift layer (tubs 15/17 (tan above), as detailed in Section X.A.1.e) in Parrillo's epitaxial substrate would make Payne's drift layer an ***epitaxial*** layer, satisfying claim 3.

226. In my opinion, combining Parrillo with Payne in this manner would have been the use of a known technique (using epitaxial substrate to make CMOS devices) to improve similar devices (Payne's twin-tub CMOS devices) in the same way (with improved latchup resistance), and a simple substitution of one known element (n- epitaxial substrate) for another (Payne's n-- substrate) to obtain predictable results.

E. Ground V

1. Dependent Claim 2: "The CMOS semiconductor device of claim 1 wherein the said drift layer is a deeply-implanted layer."

227. In my opinion, Sakai-Kawagoe in combination with Wolf renders claim 2 obvious. As described in Section X.B.2, Sakai teaches forming its nested well structures with "deep" wells formed by ion implantation and thermal diffusion, extending 3-5μm deep. Ex. 1006, 3:53-59, 5:56-61, 6:24-31. Given Sakai's similarity to Payne, which likewise teaches a nested well structure (Sections X.A.1.e-g, X.C.1), a POSITA would be motivated to combine Wolf with Sakai-

Kawagoe for the same reasons as discussed in Section X.C.1, and would have had a reasonable expectation of success for the same reasons. Section X.C.1.

228. For example, a POSITA would have been motivated to form Sakai's deep wells as deeply-implanted layers using high-energy implantation techniques to avoid damage to critical near-surface structures while establishing a desired dopant profile. Ex. 1008A, 403, 406-07, Table 10.2, 371-73, 423-24, 830; Ex. 1041, 567-68.

XI. CUMULATIVENESS

229. In my opinion, none of the references relied on in this petition are cumulative of references cited during prosecution. I understand that in its POPR to the terminated IPR2022-00289, Patent Owner argued that Payne is cumulative with Rhodes on the alleged ground that the nested well structure of Payne is nothing more than a single well formed with multiple implants. Ex. 1016, 25-41. In my opinion, this is incorrect.

230. ***First***, Sakai expressly discloses having a twin ***double well*** structure with a shallow ***well*** region disposed in a deep ***well*** region. Ex. 1006, 1:57-67, 7:32-37, FIGS. 10D, 11E, 15. These well regions are all labeled as "P-WELL" or "N-WELL" in Sakai's figures. *Id*. Sakai's nested wells clearly do not form one single well. They are expressly disclosed and labeled as distinct wells.

231. ***Second*,** Payne's nested well structure, in which shallow wells are formed in deeper wells with ***separate*** implants ***and*** annealing steps, differentiates Payne from Rhodes which does not teach a nested well structure. As Payne describes and illustrates in Figures 2 and 5-9, the deep wells ("tub regions") of Payne's nested well structure are formed first, using their own specific masks, ion implantation and thermal drive-in process steps. Ex. 1005, 3:17-4:30.

232. The shallow wells ("surface regions") are then separately formed, using different masks, ion implantation and thermal drive-in process steps. Ex. 1005, 4:31-5:17, 5:44-55. Payne's separately formed deep and shallow wells, such as wells 15 and 18, are not a single well formed using multiple implants. *Id.*

233. ***Third,*** Sakai likewise uses separate implants and annealing steps to form each well of its nested well structure. Ex. 1006, 5:56-6:4, 6:24-28, 6:52-58, FIGS. 10A, 10B. In my opinion, a POSITA would have therefore understood Payne's tub and surface regions to constitute distinct wells just as Sakai used that term.

234. In my opinion, in contrast to Payne and Sakai's structures, Rhodes teaches a twin-well architecture with side-by-side wells 160/170/180 (shown below) that Payne and Sakai seek to improve upon with their nested well structure. Ex. 1011, [0064]; Ex. 1005, 1:24-68; Ex. 1006, 1:6-2:39.

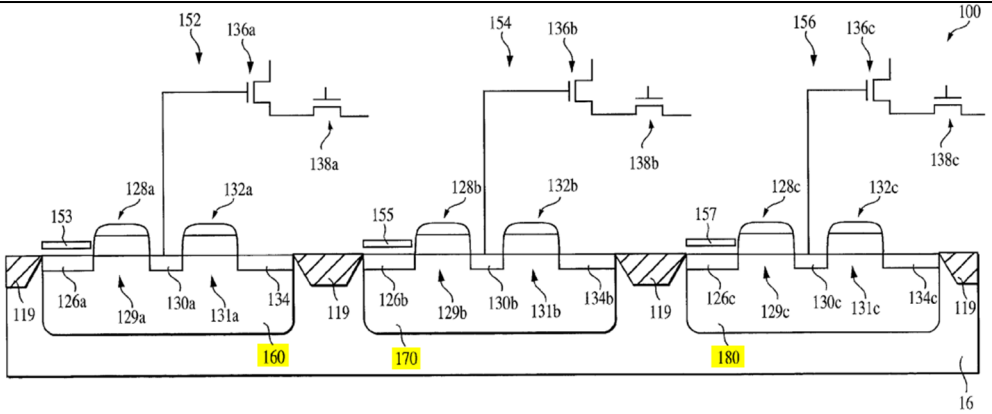


FIG. 12

Ex. 1011, FIG. 12, [0064].

235. It is also my opinion that Rhodes does not mention or suggest (in paragraph [0064] or otherwise) forming a nested well structure, and thus does not teach a "well region disposed in [a] single drift layer." This was the reason the Examiner allowed the claims to issue over Rhodes (and other art, including Kamins and Jastrzebski). Ex. 1002, 346.

236. I have reviewed the file histories. I note that nowhere in the prosecution did the Applicant or Examiner discuss nested well structures, as Payne and Sakai disclose. Thus, in my opinion, there is no support for Patent Owner's argument in the POPR that "it is reasonable to infer that the Examiner agreed with the argument Patent Owner makes explicitly herein that a multiple-implant well does not disclose a well region disposed in a single drift layer." Ex. 1016, 27.

237. I understand that Patent Owner also implied in its POPR that the Applicant overcame Rhodes-based rejections during prosecution by adding the "drift

layer" limitation to the pending claims. Ex. 1016, 22-24. In my opinion, this is incorrect. Applicant overcame Rhodes-based rejections on the basis that Rhodes is a "CMOS imaging device," and by amending claims to include a "graded dopant concentration in the…active channel regions," (a limitation that was later removed). Ex. 1002, 94-96. The "drift layer" limitation was added much later in the process after several intervening rejections. There is no indication the Examiner specifically considered Rhodes in relation to the "drift layer" limitation, let alone the "well region disposed in said single drift layer" limitation.

238. **Payne and Sakai were misapprehended or overlooked during prosecution of later patents** – I understand that Patent Owner disclosed Payne, IPR2020-00289, and Sakai during later prosecution of the '222 and '014 Patents. Ex. 1020, 111-116; Ex. 1021, 71-76. But I found no indication that the Examiner evaluated Payne, the IPR proceedings, or Sakai, or understood their significance. In my opinion, the Examiner may have overlooked IPR2020-00289 directed to the ´195 Patent because, except for claim 44 of the '222 Patent, the other 73 claims of the '222 and '014 Patents are significantly different from the '195 Patent claims, at least because they do not claim a "surface layer" and a "single drift layer." Ex. 1018, claims 1-30; Ex. 1017, claims 1-43.

239. I understand the Examiner did not issue any art-based rejection. Ex. 1020, 226-229; Ex. 1021, 176-179. Nor did the Examiner address Payne or Sakai in

the notice of allowances. *Id.* In fact, the Examiner erroneously considered Hong—which is not prior art because it was filed after the claimed priority date of the '195 Patent—to be "the closest reference." *Id.*; Ex. 1027.

240. Even if the Examiner is deemed to have considered Payne, the IPR filings, or Sakai, it is my opinion that the Examiner misapprehended or overlooked their relevance and made a material error, warranting institution here.

XII. CONCLUSION

241. For the aforementioned reasons, in my opinion, to a person of ordinary skill in the art, the Challenged Claims of the '195 Patent are rendered obvious by the prior art.

242. I understand that the Patent Owner has not asserted secondary considerations of non-obviousness. I reserve the right to respond to any such assertions.

243. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the results of the proceedings.

Date: January 30, 2023

Respectfully submitted,

Travis Blalock, Ph.D.