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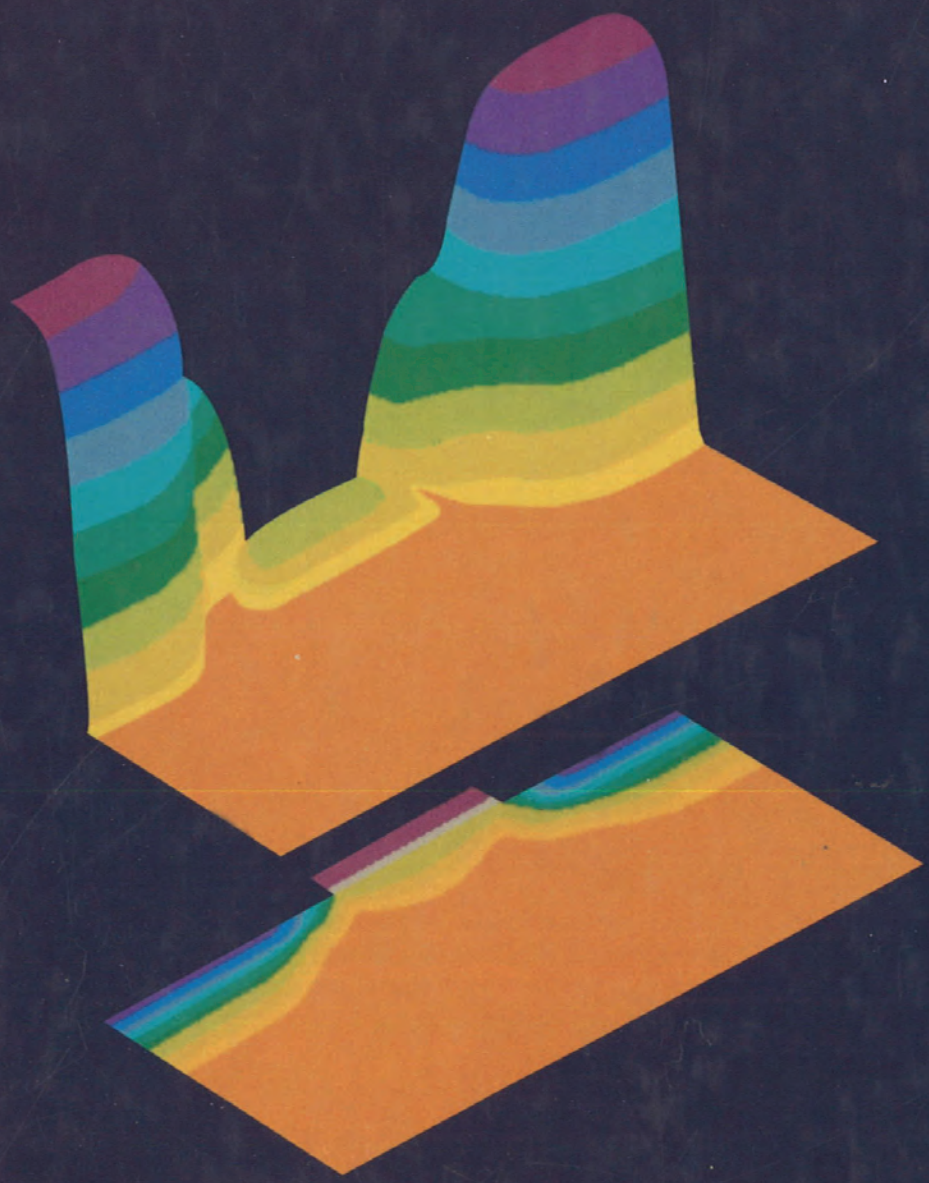

S. Wolf

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By STANLEY WOLF and RICHARD N. TAUBER

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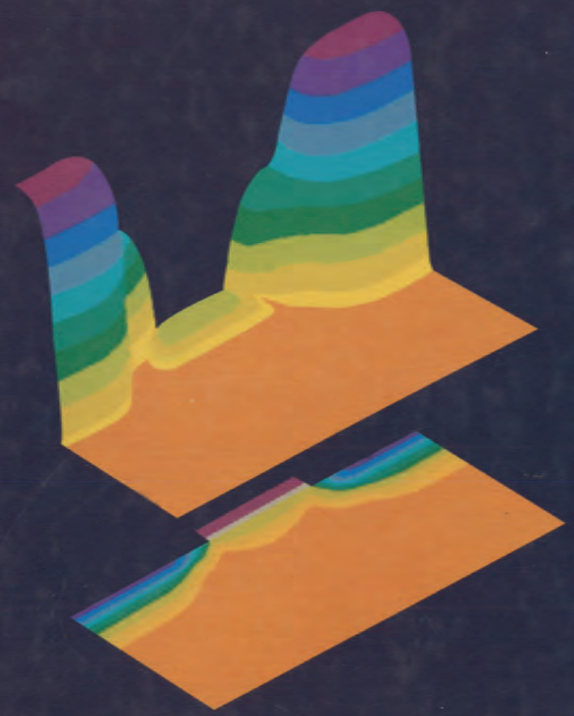

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SILICON PROCESSING FOR THE VLSI ERA

VOLUME 3:

THE SUBMICRON MOSFET

STANLEY WOLF Ph.D.
Professor, Department of Electrical Engineering
California State University, Long Beach
Long Beach, California

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Published by:

Lattice Press,
Post Office Box 340
Sunset Beach, California 90742, U.S.A.

Cover design by Roy Montibon, Visionary Art Resources, Inc., Los Angeles, CA.

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Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 3 : The Submicron MOSFET

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

ISBN 0-961672-5-3

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Holdings	Steenbock Library: Steenbock Stacks; TK7874 W635 1986 1
Holdings ID	22873617190002122
	View all holdings
Barcode	89066551995
Item ID	23613441390002122
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MMS ID	9942116843602122
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Barcode	89066551995
Copy ID	1
Material type	Book
Item policy	general (book)
Provenance	-
Is magnetic	No
PO Line	
Issue date	-
Receiving date	02/12/2002
Expected receiving date	-
Enumeration A	3
Enumeration B	-
Chronology I	-
Chronology J	-
Description	3
Pages	-
Pieces	1
Replacement cost	-
Receiving operator	import
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Inventory Information

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Inventory date	-
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Location Information

Permanent location	**Steenbock Library: Steenbock Stacks (stk)**
Item call number type	-
Item call number	-
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Item is in temporary location	**No**
Temporary location	-
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Published by:

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Cover design by: S. C. Ross Wolf.

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Library of Congress Cataloging in Publication Data
Wolf, Stanley

Silicon Processing for the VLSI Era
Volume 4: Deep-Submicron Process Technology

Includes Index
1. Integrated circuits-Very large scale integration. 2. Silicon. I. Title

ISBN 0-9616721-7-X

9 8 7 6 5 4 3 2 1

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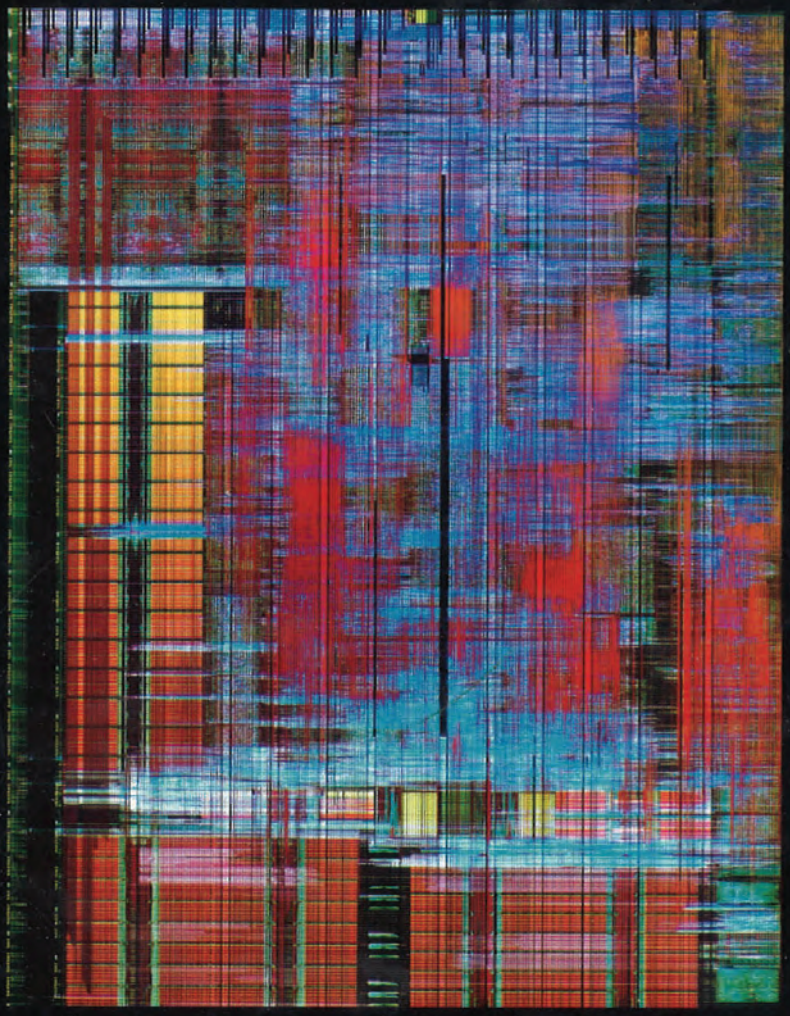

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Prentice Hall Series in Solid State Physical Electronics, Nick Holonyak, Jr., Series Editor

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This is the fifth edition of the most widely used introductory book on semiconductor materials physics, devices and technology. Previous editions have been translated and Polish. The book was written with two basic goals in mind: 1) develop t physics concepts to understand current and future devices; 2) provide a sou of current semiconductor devices and technology so that their applications optoelectronic circuits and systems can be appreciated.

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- extensive discussion of circuit and other application examples to provide students with feedback about the practical relevance of the theory.
- completely updated discussion of MOS devices, both in the underlying theory as well as discussion of short channel, high field and hot carrier effects in scaled MOSFETs, recognizing the current preponderance of CMOS.
- updated, consolidated treatment of optoelectronic devices, including sources such as blue GaN-based LEDs and semiconductor vertical-cavity surface-emitting lasers, as well as detectors such as avalanche and resonant-cavity photodiodes.
- includes a listing of the key equations for semiconductor devices on the inside covers of the book, arranged thematically to help students digest the concepts.
- about 200 problems and current references which extend concepts in the text.

BEN G. STREETMAN is Dean of the College of Engineering at The University of Texas at Austin and holds the Dula D. Cockrell Centennial Chair in Engineering. He is a Professor of Electrical and Computer Engineering and was the founding Director of the Microelectronics Research Center. He has taught at the University of Illinois at Urbana-Champaign as well as the University of Texas at Austin. He has received numerous awards including the Education Medal of IEEE, The Frederick Emmons Terman Medal of the ASEE, and membership in the National Academy of Engineering. He has published more than 270 articles in the technical literature. Thirty-three students of Electrical Engineering, Materials Science, and Physics have received their Ph.D.s under his direction.

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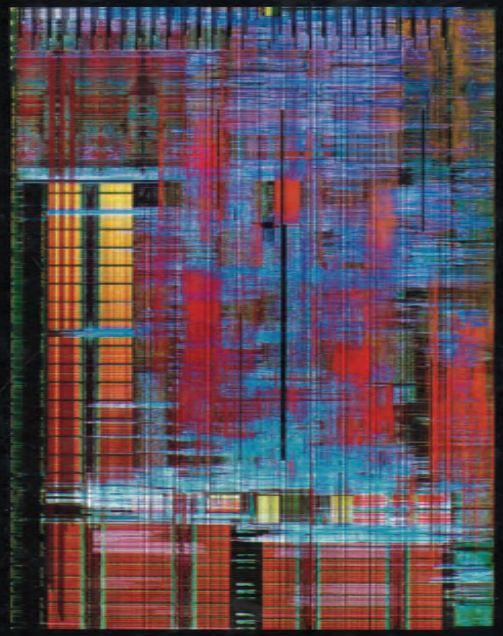

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Department of Electrical and Computer Engineering
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Library of Congress Cataloging-in-Publication Data
Streetman, Ben G.
Solid state electronic devices / Ben G. Streetman and Sanjay Banerjee -- 5th ed.
p. cm. -- (Prentice Hall series in solid state physical electronics)
Includes bibliographical references and index.
ISBN 0-13-025538-6 (casebound)
1. Semiconductors. I. Banerjee, Sanjay. II. Title. III. Series
TK7871.85.S77 2000
621.3815'2--dc21 99-16963
CIP

Publisher: **Tom Robbins**
Assistant Vice President of Production and Manufacturing: **David W. Riccardi**
Editor-in-Chief: **Marcia Horton**
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Cover Design: **Joseph Sengotta**
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Receiving date	01/22/2004
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Enumeration A	
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Chronology I	
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Description	Generate
Pages	
Pieces	1
Replacement cost	
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Retention Reason

Retention Note

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