A Dynamic Electro–Thermal Model for the IGBT[1]

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***Abstract*–A physics-based dynamic electro-thermal model is developed for the IGBT by coupling a temperature-dependent IGBT electrical model with dynamic thermal models for the IGBT silicon chip, packages, and heatsinks. The temperature-dependent IGBT electrical model describes the instantaneous electrical behavior in terms of the instantaneous temperature of the IGBT silicon chip surface. The instantaneous power dissipated in the IGBT is calculated using the electrical model and determines the instantaneous rate that heat is applied to the surface of the silicon chip thermal model. The thermal models determine the evolution of the temperature distribution within the thermal network and thus determine the instantaneous value of the silicon chip surface temperature used by the electrical model. The IGBT electro-thermal model is implemented in the Saber circuit simulator and is connected to external circuits in the same way as the previously presented Saber IGBT model, except that it has an additional thermal terminal that is connected to the thermal network component models for the silicon chip, package, and heatsink. The IGBT dynamic electro-thermal model and the thermal network component models are verified for the range of temperature and power dissipation levels (heating rates) that are important for power electronic systems.**

I. Introduction

The IGBT (Insulated Gate Bipolar Transistor) is a relatively new power semiconductor device that is rapidly being incorporated into applications such as motor drives and power converters. To effectively design the power electronic circuits that utilize IGBTs, accurate models for these devices are needed in circuit simulators. However, IGBTs cannot be described by the traditional microelectronic integrated circuit semiconductor models because IGBTs are designed for high voltages and high currents and thus have significantly different structures than microelectronic devices. A physics-based IGBT model has been developed and experimentally verified for typical power electronic circuit operating conditions [1]. This model has recently been made available to circuit designers in various circuit simulation software tools [2-6]. An IGBT model parameter extraction sequence has also been developed and used to characterize various IGBTs from different manufacturers [2,3,7].

The purpose of this paper is to extend the IGBT model to include the dynamic electro-thermal interactions, to provide a methodology for extracting the temperature-dependent model parameters, and to make the IGBT electro-thermal model available to power electronic circuit and system designers by implementing it into the Saber[2] circuit simulator [4,5]. The SPICE (Simulation Program with Integrated Circuit Emphasis) IGBT model developed in [6] can also be rewritten to include the dynamic electro-thermal effects, but this requires the evaluation and implementation of an additional partial derivative of each model function with respect to temperature. In this work, the Saber circuit simulator is used because of the ease of implementing new modes with the Saber MAST modeling language.

Although traditional microelectronic semiconductor models include temperature dependence, the temperature used by the semiconductor models in programs such as SPICE must be chosen by the user prior to the simulation and must remain constant at the predetermined value during the simulation. However, the temperature dependence of power devices are not adequately described using this traditional approach because the devices are heated significantly by the power dissipated within the device (self-heating) and by power dissipated within adjacent devices (thermal coupling). The unique approach taken in this paper is to define the temperatures at various positions within the silicon chip, the device package, and the heatsink as simulator system variables so that the temperature rise due to self-heating is determined by the simulator and is used by the temperature-dependent device model. The number of internal thermal nodes and the distribution of the nodes within the chip, package, and heatsink determine the accuracy of the thermal component models for dynamic conditions. Therefore, a methodology is also developed to derive accurate and computationally efficient thermal network component models for the silicon chip and for the various device packages and heatsinks.

II. Dynamic Electro–Thermal Interactions

Fig. 1 indicates the way in which the electrical and thermal networks of a power electronic system are interdependent. As indicated, the electro-thermal models for the power semiconductor devices (IGBTs and power diodes in Fig. 1) are connected to both the electrical and thermal networks. The IGBT electro-thermal model has three electrical terminals and one thermal terminal. The IGBT electrical terminals are connected to the electrical network component models, and the thermal terminal is connected to the thermal network component models. The thermal network is represented using thermal network component models so that the thermal models for different packages and heatsinks can be readily interconnected in the same way that the electrical network components are interconnected. The thermal network models for power modules and heatsinks contain multiple terminals and account for the thermal coupling between the adjacent semiconductor devices.

As an example, Fig. 2a is a schematic of an electro-thermal network, and Fig. 2b is the corresponding Saber netlist using the IGBT electro-thermal model and the thermal component models of the silicon chip, the T0247 package, and the TTC1406 heatsink developed in this work. The first column of the Saber netlist in Fig. 2b specifies the name of the template that contains the model equations for each component (left-hand side of the

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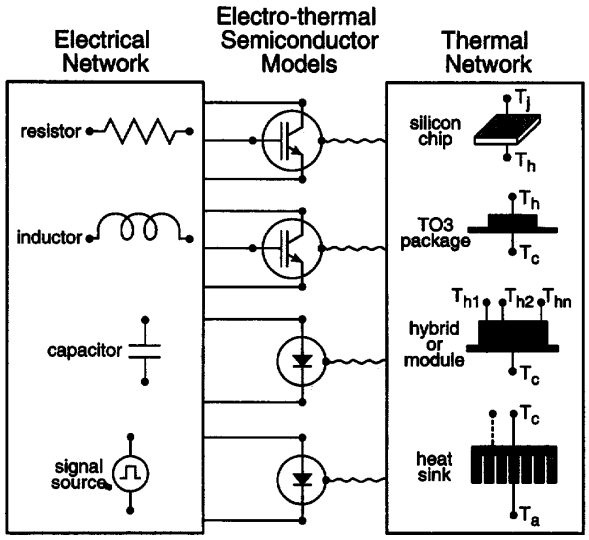
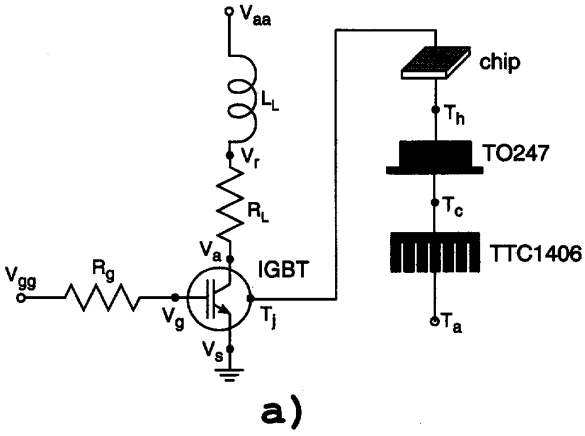


Fig. 1. Diagram indicating interconnection of electrical and thermal networks through electro-thermal models for semiconductor devices.




```
#IGBT electro-thermal simulation

#Electronic network components
v.vaa          vaa  0          = 300
l.ll           vaa  vr         = 80u
r.rl           vr   va         = 30
r.rg           vgg  vgs        = 10
pulsgen.1      vgg  0          = 20

#IGBT electro-thermal model
igbt_therm.1  va   vgs  0  tj = tauhl_1=1.6,
                                kp_1=1.5

#Thermal network components
chip_therm.1      tj   th       = thick=0.05,
                                  a_chip=0.1
to247_therm.1     th   tc       = a_chip=0.1
ttc1406_therm.1   tc   ta       = a_heat=0.4
t.ta              ta   0        = 300
```

b)

Fig. 2. a) Schematic and b) Saber netlist of an example electro-thermal network.

period) and the instance within the circuit (right-hand side of the period). The remaining columns on the left-hand side of the equal sign indicate the terminal connection points of the components within the network. The parameters used by the model templates to describe the specific components are listed on the right-hand side of the equal sign. For example, the temperature coefficients of the IGBT base lifetime and transconductance parameter are changed from the default values. It is evident from Fig. 2 that the thermal network component models developed in this work enable the thermal network to be described in the same manner as the electrical network.

III. IGBT Electro–Thermal Model

To couple the electrical and thermal networks, the IGBT electro-thermal model describes the instantaneous electrical behavior in terms of the instantaneous temperature of the device silicon chip surface T_j (temperature at the device thermal terminal). The temperature-dependent electrical model is based upon the temperature-dependent IGBT model parameters and the temperature-dependent physical properties of silicon. The IGBT electro-thermal model also calculates the instantaneous power dissipation from the internal components of current because a portion of the electrical power delivered to the device terminals is dissipated as heat and the remainder charges the internal capacitances. The dissipated power calculated by the electrical model supplies heat to the surface of the silicon chip thermal model through the thermal terminal.

A. Saber Simulator Implementation

Fig. 3 is an abbreviated outline of the Saber IGBT electro-thermal template. The first statement in the template header defines the name of the model template, the names of the terminal connection points, and the names of the model parameters and their temperature coefficients. The next two statements define the terminal types of the anode,[3] cathode, and gate to be electrical, and the terminal type of the thermal terminal tnode to be thermal_k. The electrical type terminals have units of voltage (V) across the terminals and units of current flowing through the terminals, whereas the thermal_k type terminals have units of temperature (K) across the terminals and units of power (W) flowing through the terminals. The number statements in the header section define the default values of the model parameters and the default values of their temperature coefficients.

```
# ———————— Template Header ————————
template  igbt_therm  anode,gate,cathode,tnode  =tauhl,tauhl_1,
electrical   anode,gate,cathode      # electrical terminals
thermal_k   tnode                    # thermal type terminal
number   tauhl =1.0u      # default parameter values
number   tauhl_1 =1.5     # default temperature coefficients
{   # ———————— Template Body ————————
    # local declarations
    parameters { # parameters calculated prior to simulation }
    values { # nonlinear function of system variables }
    control { # simulator dependent control statements }
    equations { # equations for system variables }
}
```

Fig. 3. Abbreviated outline of Saber IGBT electro-thermal template.

[3] The sans serif symbols throughout the text represent computer mnemonics.

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The model equations that describe the terminal electro-thermal behavior of the IGBT are defined in the body of the template. To implement the IGBT electro-thermal model into the Saber template, the model is formulated such that the currents between each of the electrical nodes and the power between the thermal nodes are expressed in terms of nonlinear functions of the system variables and in terms of the time rate-of-change of these functions of the system variables. System variables are electrical node voltages, thermal node temperatures, and explicitly defined system variables which account for implicit model equations. The nonlinear model functions are implemented in the values section of the template body (Fig. 3), and the equations section is used to describe how the model functions are assembled to solve for the system variables.

Fig. 4a shows the equations section of the Saber IGBT electro-thermal template, and Fig. 4b shows a schematic of the components of current and power dissipation within the IGBT electro-thermal model. The first six statements in the equations section of the Saber IGBT electro-thermal template specify the components of current between the device electrical terminals and the internal electrical nodes [4]. The next five statements explicitly define additional system variables and the implicit equations that are solved by the simulator for each of the system variables [4]. Finally, the last statement in the equations section of the Saber IGBT electro-thermal template specifies the power delivered to the thermal terminal (tnode).

B. Temperature-Dependent Model

The temperature-dependent model functions used to calculate the electrical characteristics and power dissipation in the equations section of Fig. 4a (e.g., Qgs, Cgd, Imos,..., power) are evaluated in the values section of the Saber template in terms of the instantaneous values of the simulator system variables. The simulator system variables for the electro-thermal IGBT model are the voltages at the electrical nodes v(anode), v(cathode), v(gate), v(base), and v(emitter); the temperature at the thermal node tk(tnode); and the explicitly defined system variables Q, dVdgdt, dVecdt, nsat, and mucinv. The temperature-dependent model functions are similar to those described for the previously presented nonthermal IGBT model (Table 1 of [4]) except that the IGBT model parameters (Table 2 of [4]) and the physical properties of silicon (Table 3 of [4]) are replaced by the temperature-dependent expressions given in Tables 1 and 2.

The expressions in Tables 1 and 2 are implemented at the beginning of the values section of the Saber IGBT electro-thermal template, because they depend upon the silicon chip surface temperature T_j = tk(tnode) which is a simulator system variable in the approach taken in this work. The parameters in Table 2 with subscript 0 are the extracted values of the model parameters at the reference temperature T_0 and the parameters with subscript 1 are the extracted temperature coefficients of the model parameters. The names used in the template for the parameters at the reference temperature are the same as the parameter names in the existing nonthermal template [4,5], so that the model parameters of existing Saber netlists do not need to be changed to use the new electro-thermal model. The names of the temperature coefficients are also added to the template parameter list because they vary from one device type to another. The default values of the temperature coefficients of the IGBT model parameters are listed in Table 3.

The physical origin and empirical expressions for the temperature-dependent physical properties of silicon (Table 1) are well documented in the literature [8]. Equations (T1.1) through (T1.7) are obtained from [8], and (T1.8) and (T1.9) are obtained by comparing (4.1-33) of [8] with (2) of [4]. The temperature

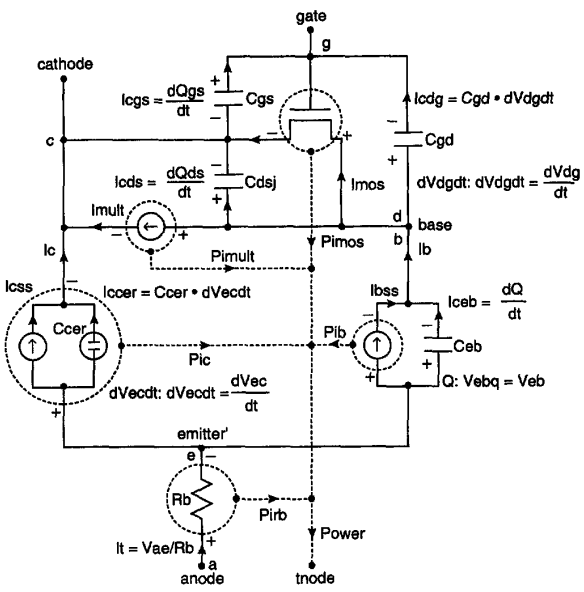
```
equations {
   i(gate - > cathode)     += d_by_dt(Qgs)
   i(drain - > gate)       += Cgd * dVdgdt
   i(drain - > cathode)    += Imos + Imult + d_by_dt(Qds)
   i(emitter - > cathode)  += Icss + Ccer * dVecdt
   i(emitter - > drain)    += Ibss + d_by_dt(Q)
   i(anode - > emitter)    += Vae/Rb

   dVdgdt :  dVdgdt= d_by_dt(Vdg)
   dVecdt :  dVecdt= d_by_dt(Vec)
   Q      :  Vebq=Veb

   Nsat   :  Nsat=Ic/(q*A*vpsat) - Imos/(q*A*vnsat)
   mucinv :  mucinv = Pm*log( 1. + alpha2/Pm**(2./3.) )/alpha1

   p(tnode)  -= power.
      }
```

a)



b)

Fig. 4. a) Equations section of Saber IGBT electro-thermal template, and b) schematic of components of current and dissipated power within IGBT electro-thermal model.

dependence of the p-n junction avalanche breakdown voltage is discussed on p. 2-55 of [9], and (T1.10) is obtained empirically from the p-n junction breakdown voltage versus temperature curves specified in manufacturer's data sheets. The quantity BV_k of (T1.10) replaces the constant coefficient in the BV_{cb0} expression in Table 1 of [4] which is used to calculate the multiplication factor M.

The expressions for the temperature-dependent IGBT model parameters given in Table 2 are developed using the extracted values of the model parameters versus temperature (Fig. 5) for various device types [7]. An accurate extraction sequence [2,3,7] is required to resolve the variations of the model parameters with temperature. The temperature coefficient for the threshold voltage V_{T1} depends upon the channel dopant density and gate oxide

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TABLE 1
TEMPERATURE–DEPENDENT PROPERTIES OF SILICON

$\mu_n(T_j) = 1500 \cdot (300/T_j)^{2.5}$	$(T1.1)$
$\mu_p(T_j) = 450 \cdot (300/T_j)^{2.5}$	$(T1.2)$
$D_n(T_j) = \mu_n \cdot kT_j/q$	$(T1.3)$
$D_p(T_j) = \mu_p \cdot kT_j/q$	$(T1.4)$
$n_i(T_j) = 3.88 \times 10^{16} \cdot (T_j)^{1.5}/\exp(7000/T_j)$	$(T1.5)$
$v_{nsat}(T_j) = 10^7 \cdot (300/T_j)^{0.87}$	$(T1.6)$
$v_{psat}(T_j) = 8.37 \times 10^6 \cdot (300/T_j)^{0.52}$	$(T1.7)$
$\alpha_1(T_j) = 1.04 \times 10^{21} \cdot (T_j/300)^{1.5}$	$(T1.8)$
$\alpha_2(T_j) = 7.45 \times 10^{13} \cdot (T_j/300)^2$	$(T1.9)$
$BV_k(T_j) = 5.34 \times 10^{13} \cdot (T_j/300)^{0.35}$	$(T1.10)$

TABLE 2
TEMPERATURE–DEPENDENT IGBT PARAMETERS

$\tau_{HL}(T_j) = \tau_{HL0} \cdot (T_j/T_0)^{\tau_{HL1}}$	$(T2.1)$
$I_{sne}(T_j) = \dfrac{I_{sne0} \cdot (T_j/T_0)^{I_{sne1}}}{\exp[14000 \cdot (1/T_j - 1/T_0)]}$	$(T2.2)$
$V_T(T_j) = V_{T0} + V_{T1} \cdot (T_j - T_0)$	$(T2.3)$
$K_p(T_j) = K_{p0} \cdot (T_0/T_j)^{K_{p1}}$	$(T2.4)$

TABLE 3
DEFAULT TEMPERATURE COEFFICIENTS

τ_{HL1}	1.5
I_{sne1}	0.5
V_{T1}	-0.9 V/K
K_{p1}	0.8

thickness (p. 452 of [10]), but the value in Table 3 is typical for the highly doped channel of VDMOSFETs. The temperature coefficient of the transconductance parameter K_{p1} varies between device types, from a value of 1.5 for surface mobility-dominated conduction in the channel, to a value of 0.6 for saturation velocity limited transport in the channel (p. 3-5 of [9]). The temperature dependence of τ_{HL} is not well documented in the literature but it is generally believed that the Shockley-Read-Hall lifetime increases with temperature similarly to the extracted expression in Table 2 [11].

The preferred method to extract I_{sne} is from the slope of $1/\beta_{tr,v}$ (relative size of the turn-off current tail) versus current $(\beta_{tr,v}^{max} \cdot I_k)^{-1}$ [2,3,7]. Because the extracted value of I_{sne} depends upon the values of the other temperature-dependent parameters in the extraction equation (inset in Fig. 5d), the temperature-dependent values used in the extraction equation must be consistent with those used for the simulation. The empirical expression for the temperature dependence of I_{sne} is obtained by substituting the expressions in Table 1 into the expression in Fig. 5d, where I_{sne1} is the measured temperature coefficient of $(\beta_{tr,v}^{max} \cdot I_k)^{-1}$.

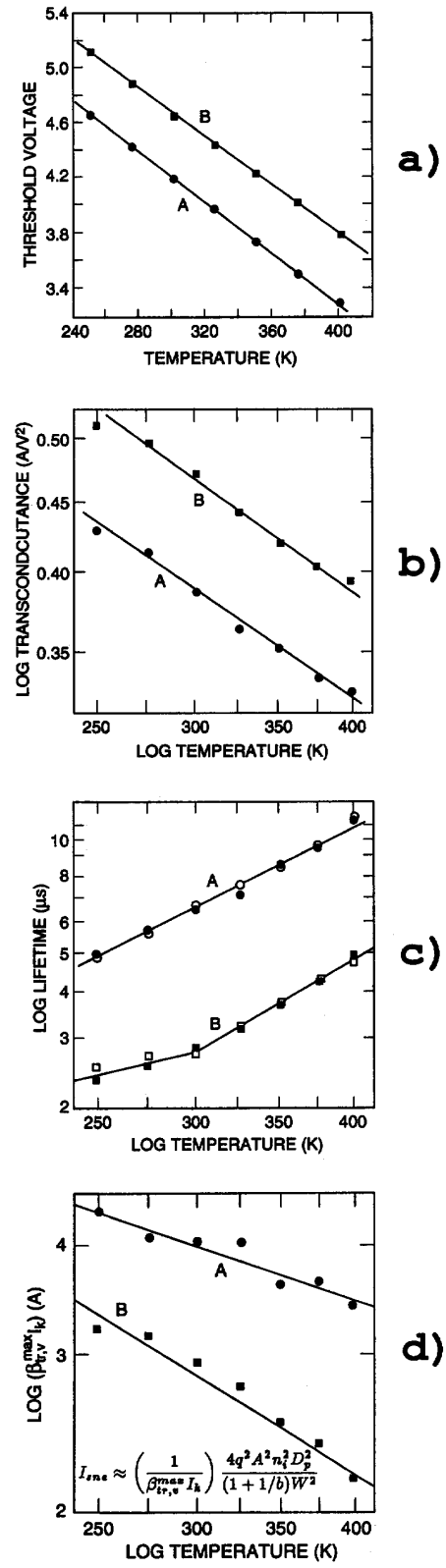

Fig. 5. Extracted values of model parameters versus temperature.

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The physical mechanisms resulting in the temperature dependence of I_{sne} vary significantly from one device type to another. From the solution to the diffusion equation in the emitter,

$$I_{sne} = \frac{qn_{ie}^2 D_{ne} A}{N_E L_E} \tag{1}$$

where $L_E = \sqrt{D_{ne}\tau_e}$ for a wide emitter region and $L_E = W_E$ for a narrow emitter. Using the values in Tables 1 and 2, one would expect the temperature dependence in Table 2 but with $I_{sne1} = 1.5$. However, for the high dopant densities in the emitter region ($N_E > 10^{18}$ cm^{-3}), the effect of band gap narrowing changes the temperature dependence of n_{ie} (p. 38 of [8]), the effect of ionized impurity scattering changes the temperature dependence of D_{ne} (p. 88 of [8]), and Auger recombination changes the temperature dependence of τ_e [11].

C. Temperature-Dependent Characteristics

The temperature dependence of the IGBT electrical characteristics is discussed in [12] based upon measured values and upon the insights provided by traditional bipolar transistor and MOSFET models. The temperature dependence of the IGBT electrical characteristics results from the interaction of several competing mechanisms. The physics-based IGBT model described in this paper [1] provides a precise description of the internal temperature-dependent physical mechanisms and is able to predict the measured temperature dependence using the values of the extracted model parameters and their temperature coefficients. In addition, the temperature dependence of the IGBT electrical characteristics varies substantially between different IGBT types. This occurs because the temperature coefficients of the IGBT model parameters vary between the different devices, but more importantly because the values of the model parameters at the reference temperature vary between the devices, resulting in different dominant physical mechanism for the temperature dependence.

Figs. 6 and 7 are examples of the measured and simulated temperature dependence of selected IGBT characteristics for devices with the same model parameters at 300 K, as in [4] and the temperature coefficients given in Table 3. The measurements are made for pulsed conditions so that self-heating is minimal and the chip surface temperature is determined by the temperature-controlled test fixture. The simulations are performed using the Saber dc transfer analysis to sweep the ambient temperature source T_a which is connected directly to the IGBT thermal terminal. Figs. 6 and 7 demonstrate the ability of the model to predict the temperature dependence of a given IGBT at a given bias point based upon the extracted model parameters and the model parameter temperature coefficients.

Fig. 6 shows the measured and simulated temperature dependence of the IGBT saturation current for $V_{ge} = 9$ V, $V_a = 10$ V, and an IGBT base lifetime at 300 K of $\tau_{HL} = 7.1$ μs. The temperature dependence of the IGBT saturation current is influenced primarily by several factors: 1) The threshold voltage decreases with temperature which increases the saturation current. 2) The MOSFET transconductance parameter decreases with temperature which decreases the saturation current. 3) The bipolar transistor current gain (ratio of I_c to I_{mos} in Fig. 6) decreases slightly with temperature which decreases the saturation current. The temperature dependence of the bipolar transistor current gain is influenced by several factors: 1) The base transport factor is unchanged because the effects of the increasing lifetime and the decreasing diffusivity cancel. 2) However, the emitter efficiency decreases slightly with temperature because the value of $\sqrt{I_{sne}}/n_i$ does not decrease as much as the diffusivity (see I_{ces} and I_{bes} in Table 1 of [4]). For higher gate voltages and/or lower temperatures, the dominant mechanism becomes the decreasing MOSFET transconductance parameter and the saturation current decreases with temperature.

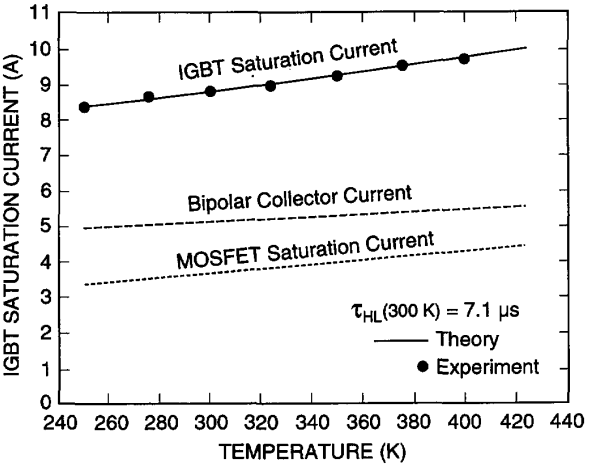

Fig. 6. Simulated and measured temperature dependence of IGBT saturation current for $V_{ge} = 9$ V and $V_a = 10$ V.

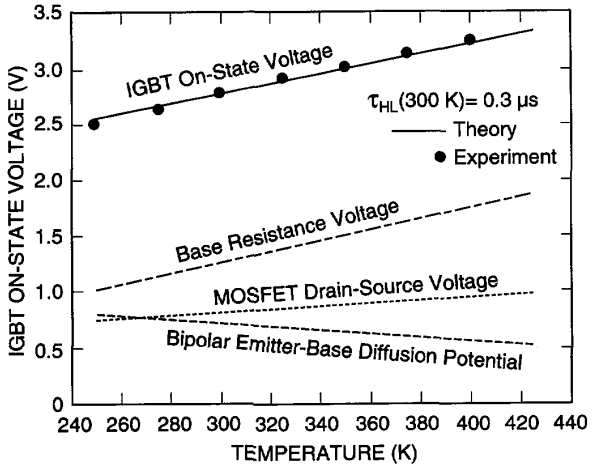

Fig. 7. Simulated and measured temperature dependence of IGBT on-state voltage for $V_{ge} = 20$ V and $I_T = 10$ A.

Fig. 7 shows the measured and simulated temperature dependence of the IGBT on-state voltage for $I_T = 10$ A, $V_{ge} = 20$ V, and an IGBT base lifetime at 300 K of $\tau_{HL} = 0.3$ μs. The temperature dependence of the IGBT on-state voltage is primarily influenced by several factors: 1) The base resistance increases with temperature because the mobility decreases faster than the base charge increases (base charge increases because τ_{HL} and $n_i/\sqrt{I_{sne}}$ increase). 2) The emitter-base junction diffusion potential V_{ebd} [4] decreases with temperature because n_i increases much faster than the base charge. 3) The drain-source voltage increases slightly with temperature because the decreasing MOSFET transconductance parameter dominates the decreasing threshold voltage for the high gate voltage bias condition. The on-state voltage temperature dependence varies significantly between devices with different model parameters and for different bias conditions. For example, at lower current densi-

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ties, the channel resistance and base resistance are small so the on-state voltage decreases with temperature. For higher base lifetimes, the on-state voltage is unchanged for the temperature range of Fig. 7, e.g., for $\tau_{HL}(300\text{ K}) = 7.1\ \mu s$, the base resistance increases from 0.15 to 0.3 V, the emitter base diffusion potential decreases from 0.85 to 0.55 V, and the drain-source voltage increases from 0.45 to 0.65 V.

The temperature dependence of the anode voltage overshoot at turn-off for the series resistor-inductor load (Fig. 9 of [1]) is determined primarily by two competing mechanisms: 1) the nonquasi-static collector-emitter redistribution capacitance of the IGBT increases with temperature and 2) the dynamic avalanche multiplication current decreases with temperature. This behavior can be explained by examining the time rate-of-change of anode voltage at turnoff [3,4]: $dV_a/dt \approx (I_T - M \cdot I_{ces})/(M \cdot C_{cer})$. The effective output capacitance C_{cer} increases with temperature because it is proportional to the base charge [4] which increases with temperature as described above. However, the multiplication factor M at large anode voltages decreases significantly with temperature because BV_k increases. The value of I_{ces} at a given voltage only decreases slightly with temperature because the decreasing diffusivity cancels with the increasing τ_{HL} and $n_i/\sqrt{I_{sne}}$. Therefore, for device and circuit conditions that result in overshoot voltages that approach the BV_{ce0} of the IGBT, the voltage overshoot increases with temperature due to the decreasing M; otherwise, the voltage overshoot decreases with temperature due to the increasing output capacitance.

D. Instantaneous Dissipated Power

The instantaneous power dissipated as heat energy within the IGBT is calculated using the internal components of current and voltage because a portion of the energy delivered to the device electrical terminals is dissipated as heat and the remainder is stored in the internal capacitances. The elements of current within the IGBT that result in instantaneous dissipated power are contained within the dashed circles of Fig. 4b. The energy delivered to the capacitive elements is stored in the electric field energy of the capacitors until it is returned to the external circuit or transferred to other internal current elements. In contrast, the energy delivered to the so-called collector-emitter redistribution capacitance (C_{cer} in Fig. 4b) is dissipated immediately as heat. Although the redistribution component of collector current is proportional to the time rate-of-change of voltage $I_{ccer} = C_{cer} \cdot dV_{ec}/dt$ and interacts with the external circuit in the same manner as a capacitor [1], the capacitance analogy does not apply to the instantaneous dissipated power.

The value of the dissipated power is calculated at the end of the values section of the Saber IGBT electro-thermal template using the values of the other nonlinear model functions (Table 1 of [4]). From Fig. 4b, the total dissipated power is given by:

$$\text{Power} = P_{ic} + P_{imult} + P_{ib} + P_{imos} + P_{irb} \tag{2}$$

where each of the components of power indicated on Fig. 4b is calculated in terms of the node voltages and currents of the power dissipating current elements:

$$P_{ic} = (I_{ces} + I_{ccer}) \cdot V_{ec} \tag{3a}$$

$$P_{imult} = I_{mult} \cdot V_{ds} \tag{3b}$$

$$P_{ib} = I_{bss} \cdot V_{eb} \tag{3c}$$

$$P_{imos} = I_{mos} \cdot V_{ds} \tag{3d}$$

$$P_{irb} = I_T \cdot V_{ae}. \tag{3e}$$

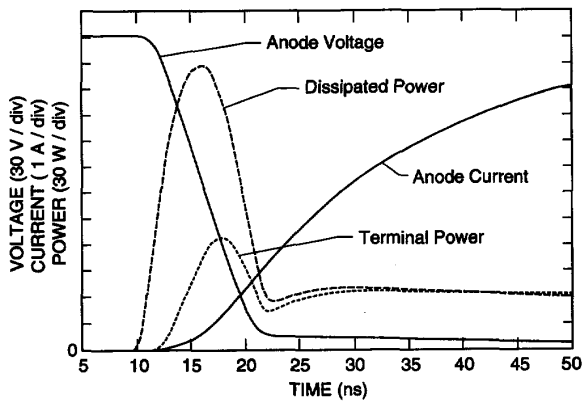

Fig. 8. Comparison of terminal power and instantaneous dissipated power at turn-on.

The instantaneous dissipated power of (2) is used by the last line of the equations section of the Saber IGBT electro-thermal template (Fig. 4a) to specify the power delivered to the thermal network through the IGBT thermal terminal tnode. The power calculated from (2) and (3) can differ substantially from the instantaneous power delivered to the device electrical terminals.

For example, Fig. 8 shows the simulated turn-on anode current, anode voltage, dissipated power, and terminal power waveforms for the circuit condition of the $R_g = 10\ \Omega$ curve of Fig. 10 of [1]. The terminal power waveform is calculated using the Saber PLTOOL waveform calculator to multiply the simulated current and voltage waveforms at the gate and anode terminals. In Fig. 8, the power delivered to the electrical terminals is much less than the dissipated power, because the drain-source and gate-drain capacitances are discharged through the MOSFET and the capacitor energy is dissipated as heat within the device. This energy was stored in the capacitors during the power-up of V_{ga} or during the previous turn-off phase. After the initial phase of the turn-on indicated in Fig. 8, the terminal power becomes larger than the dissipated power as the emitter-base diffusion capacitance is charged. This example demonstrates the ability of the model to determine if and when the terminal power is dissipated as heat within the device. This is important for resonant circuits where much of the energy stored in the internal capacitors is returned to the external circuit and is not dissipated as heat within the transistor. The switching energy is also easily calculated from the dissipated power waveform using the integral function of the Saber PLTOOL waveform calculator.

IV. Thermal Component Models

The power that is dissipated in the semiconductor devices supplies heat to the surface of the silicon chip thermal model and increases the temperature of the nodes of the thermal grid as the heat diffuses from the chip surface toward the heatsink fins. Because the time constants for heat flow within the chip, package, and heatsink are orders of magnitude longer than the time constants of the electronic devices and circuits, the self-heating effects behave dynamically even for circuit conditions that are considered to be static for the electronic devices. In addition, for circuit conditions that result in high power dissipation levels, the heat is applied rapidly to the chip and only diffuses a few micrometers into the chip surface. Therefore, the heating process is nonquasi-static and the temperature distribution within the chip, package, and heatsink depends upon the rate at which the heat is applied (power dissipation level). The

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goal of the new thermal network component modeling methodology is to produce computationally efficient thermal component models that accurately represent the nonquasi-static temperature distribution for the applicable range of power dissipation levels.

A. Modeling Methodology

The new thermal network component modeling methodology presented in this paper is based on several innovations that result in accurate, computationally efficient, and easy-to-use thermal component models. In the new methodology, the temperatures at various positions within the silicon chips, the device packages, and the heatsinks are defined to be simulator system variables, so that the temperature distribution is solved for by the simulator in the same manner as the simulator solves for the node voltages of the electrical network. The equations describing the heat flow between the internal thermal nodes and the heat storage at the thermal nodes are obtained by discretizing the nonlinear heat diffusion equation. In the discretization process, a grid spacing that increases logarithmically with distance from the heat source is used to maximize computation efficiency and to accurately represent the dynamic temperature distribution for the applicable range of heating rates. Finally, the thermal network is represented by an interconnection of thermal component models for the device silicon chips, device packages, and heatsinks, where the individual component models are parameterized in terms of structural information. Hence, the user only needs to specify the interconnection of the thermal components and the values of their structural parameters to represent thermal networks.

Traditionally, several other methods have been used for solving the heat diffusion equation to describe the surface temperature of semiconductor devices. These methods include 1) steady-state Fourier series solution [13], 2) convolution of the thermal step response with analytical power dissipation functions [14], 3) empirical extraction of thermal network element values from the measured thermal step response [15], 4) physics-based thermal resistance and thermal capacitance network element analysis [16], and 5) three-dimensional finite difference and finite element simulation [17]. However, each of these methods has limitations that prevent efficient dynamic electro-thermal simulation. The first method is very efficient for three-dimensional steady-state thermal analysis, but is not applicable to dynamic thermal conditions. The second method is useful for analytical calculation of the dynamic temperature distribution from predetermined power dissipation functions, but is only valid for linear materials and would require the evaluation of a convolution integral by the circuit simulator which is inefficient.

Methods 3) through 5) are numerically similar to the thermal network component modeling methodology used in this work in that they result in a finite number of state equations (coupled first-order ordinary differential equations) that are numerically integrated by the simulator to determine the evolution of the temperature distribution in terms of the instantaneous power dissipation. However, methods 3) through 5) do not result in compact models that are parameterized in terms of structural information and that are both accurate and computationally efficient. For example, the third method uses an assumed thermal network that may not have adequate precision to describe the nonquasi-static heating for high power dissipation levels. The fourth method can be used to derive accurate thermal network models from structural and material information but requires the user to analyze each thermal resistance and thermal capacitance element of each component in the network. The fifth method is generally applicable to three-dimensional structures and nonlinear materials, but is computationally inefficient and requires the user to generate a structural model and an accurate element mesh.

B. Thermal Model Development

The thermal network component models are derived from the heat diffusion equation using the component geometry, the nonlinear thermal properties of the materials, and other nonlinear heat transport mechanisms such as convection. The three-dimensional heat flow is accounted for using appropriate symmetry in the discretization of the heat equation for each region of the component. The silicon chip thermal model is based upon the one-dimensional rectangular coordinate heat diffusion equation and includes the nonlinear thermal conductivity of silicon. The package models describe the two-dimensional lateral heat spreading and the heat capacity of the periphery of the package. The heatsink models describe the heat spreading at the heatsink package interface, the semi-cylindrical heat flow from the package toward the heatsink fins, and the nonlinear forced and natural convection heat transfer at the heatsink fins. The silicon chip thermal model is described briefly in this paper to exemplify the new modeling methodology, and the detailed analysis of the package and heatsink models are given in [18].

The three-dimensional heat diffusion equation for isotropic materials (thermal conductivity is independent of direction) can be written as:

$$\nabla \cdot (k(T)\nabla T) = \rho c \frac{\partial T}{\partial t} \tag{4a}$$

where the thermal conductivity is nonlinear for silicon and is given by (p. 119 of [8]):

$$k(T) = 1.5486 \cdot (300/T)^{4/3}. \tag{4b}$$

For one-dimensional heat flow with y- and z-axis rectangular coordinate symmetry, the heat diffusion equation simplifies to:

$$A\frac{\partial}{\partial x}\left(k(T)\frac{\partial T}{\partial x}\right) = A\rho c\frac{\partial T}{\partial t}. \tag{5}$$

This partial differential equation can be discretized into a finite number of first-order ordinary differential equations by integrating between $(x_{i-1}+x_i)/2$ and $(x_i+x_{i+1})/2$ and by then applying finite differences to evaluate the spatial derivatives:

$$\frac{T_{i+1}-T_i}{R_{i,i+1}} - \frac{T_i - T_{i-1}}{R_{i-1,i}} = \frac{dH_i}{dt}, \tag{6a}$$

where

$$H_i = C_i \cdot T_i \tag{6b}$$

$$C_i = A\rho c \cdot (x_{i+1} - x_{i-1})/2 \tag{6c}$$

$$R_{i,i+1} = (x_{i+1} - x_i)/A/k_{i,i+1}. \tag{6d}$$

For the nonlinear thermal conductivity of silicon, the value of $k_{i,i+1}$ is obtained using the temperature $(T_i + T_{i+1})/2$ to evaluate (4b). This discretization process is also applicable to other coordinate systems where (5) and (6) have different forms for different symmetry conditions.

In the discretization process of (6), it is assumed that the temperature gradient and thermal conductivity do not vary substantially between adjacent grid points. Therefore, the accuracy of the thermal component model is determined by the number and locations of the thermal nodes within the component. For high power dissipation levels during short periods of time (e.g., for switching transients), the surface temperature rises faster

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than the heat diffuses into the chip (nonquasi-static heating), and a high density of thermal nodes is required at the silicon chip surface. However, the thermal gradients disperse as the heat diffuses through the chip, so a grid spacing that increases logarithmically with distance from the heat source (silicon chip surface) results in the minimum number of thermal nodes required to describe the temperature distribution for the range of applicable power dissipation levels (heating rates). To aid in the visualization of the transient temperature distribution, a quasi-logarithmic grid spacing is used which consists of an evenly spaced grid within segments where the segment size increases logarithmically with distance from the heat source. This quasi-logarithmic grid spacing is continued throughout the thermal network, with the segment size increasing from the chip surface through the package, to the heatsink fins.

C. Saber Simulator Implementation

The thermal component models are implemented into Saber similarly to the IGBT electro-thermal model described in section III. For the thermal models, all of the terminal and internal nodes have the thermal_k type, and the model is formulated such that the components of power flow between the thermal nodes are expressed in terms of the node temperatures. For example, the basic chip_therm model has an internal thermal node for each discretization indices i at position x_i, and the terminal nodes are at the silicon chip surface junct and the chip-package interface header. Fig. 9 shows an abbreviated form of the equation section of the chip_therm Saber template where only five internal nodes are indicated for simplicity (the actual model consists of a 15-node quasi-logarithmically spaced grid). The first six statements of Fig. 9 describe the heat conduction between the adjacent nodes using the thermal resistances (left-hand side of (6a)). The last five statements describe the components of power that are stored as heat energy in the thermal capacitance at each thermal node (right-hand side of (6a)).

The parameters of the chip_therm template described in the netlist of Fig. 2b are the chip area a_chip and the chip thickness thick. Using these parameter values, the template calculates the positions of the internal nodes x_i to form the quasi-logarithmic grid spacing. The node positions, the chip area, and the instantaneous node temperatures are used to evaluate the model functions $R_{i,i+1}, C_i$, and H_i that are used by the equations section (Fig. 9). The node positions and the thermal capacitances are evaluated in the parameters section of the Saber template

```
equations {
        p(junct -> node1)      +=   (Tj-T1)/Rj1
        p(node1 -> node2)      +=   (T1-T2)/R12
        p(node2 -> node3)      +=   (T2-T3)/R23
        p(node3 -> node4)      +=   (T3-T4)/R34
        p(node4 -> node5)      +=   (T4-T5)/R45
        p(node5 -> header)     +=   (T5-Th)/R5h

        p(node1)               +=   d_by_dt(H1)
        p(node2)               +=   d_by_dt(H2)
        p(node3)               +=   d_by_dt(H3)
        p(node4)               +=   d_by_dt(H4)
        p(node5)               +=   d_by_dt(H5)
        }
```

Fig. 9. Abbreviated five node equations section of the chip thermal model Saber template.

prior to simulation time because they are independent of node temperature. The calculated values of these parameters can be listed when the templates are loaded by setting the parameter list > 0. The expressions for the thermal resistances and the node heat energies are implemented in the values section of the template and are evaluated at simulation time because they depend upon the node temperatures which are simulator system variables T_i = tk(nodei). At simulation time, the Saber simulator solves for the temperatures at each thermal node so that the net power at each node sums to zero (energy conservation).

The package and heatsink models are discussed in detail in [18] as well as the techniques used to ensure convergence in thermal and electro-thermal templates. The package and heatsink thermal models are formulated similarly to the chip thermal model except that the expressions used to calculate the thermal resistances, thermal capacitances, and the node heat energies are different. In addition, the package models include additional expressions and parameters to account for the die attach thermal resistance, the lateral heat spreading, and the heat capacity of the package periphery. The lateral heat spreading in the package results in an effective heat flow area that increases with depth into the package. The value of the effective heat flow area at the case depends upon the package parameters such as the chip area and the package thickness and is calculated in the parameters section of the package templates. This value is listed when the package templates are loaded because it is used as a parameter for the heatsink models (a_heat of Fig. 2b). The heatsink models also include heat spreading at the package interface, semi-cylindrical heat diffusion, and the nonlinear forced and natural convection heat transfer coefficients.

V. Dynamic Electro–Thermal Simulations

The temperature distribution within the thermal network depends upon the rate that heat is dissipated. Figs. 10 through 12 show the measured and simulated electrical waveforms and the simulated temperature waveforms at selected grid positions within the thermal network for circuit conditions that result in various power dissipation levels. The model parameters at 300 K are the same as those in [4], and the temperature coefficients are given in Table 3. Because the temperature-dependent electrical characteristics have been verified in Figs. 6 and 7, the agreement between the simulated and measured electrical waveforms of Figs. 10 through 12 verifies that the thermal network component models accurately describe the dynamic chip surface temperature waveforms. This is the so-called "temperature-sensitive electrical parameter method" of measuring the junction temperature of semiconductor devices [19,20]. In [18], several other methods are used to verify the predictions of the thermal component models including: 1) infrared microradiometer measurement of chip surface temperature waveforms [19,20], 2) thermocouple probe measurements of heatsink temperature waveforms, and 3) three-dimensional transient finite element simulations of temperature [17].

First, consider Fig. 10 which shows a 300-V, 6-A short-circuit condition for a gate drive voltage of $V_{gon} = 7$ V. Fig. 10 is for a device with a base lifetime at the reference temperature of $\tau_{HL}(300\text{ K}) = 7.1\ \mu$s. The increase in short-circuit current with time is due to the decrease in threshold voltage with temperature (Fig. 6). However, for higher currents (above 15 A), the short-circuit current decreases with time due to the decreasing transconductance. In the intermediate current range (12 through 15 A), the current initially decreases and then increases at high temperatures. In general, the range of short-circuit currents that have positive or negative temperature coefficients varies from one device type to another and can be predicted by

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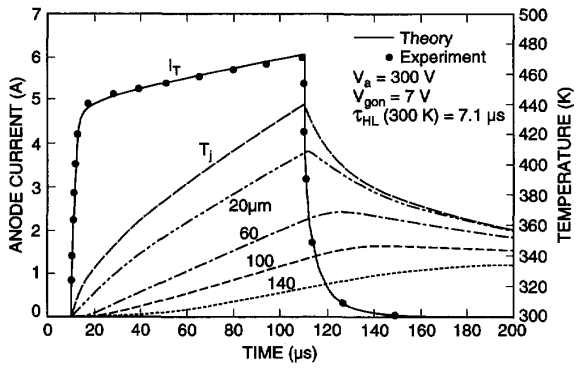

Fig. 10. Simulated and measured short circuit current and simulated temperature waveforms at selected positions within silicon chip.

the model using the model parameters and their temperature coefficients.

The circuit conditions of Fig. 10 result in an 1800-W power dissipation level for the 0.1-cm^2 area chip. For this power dissipation level, only the first 140 μm of silicon are heated during the 100-μs pulse and only 180 mJ of dissipated energy results in a 140-K rise in chip surface temperature. It is evident from Fig. 10 that the grid spacing of 20 μm in the top 100 μm of silicon is necessary to resolve the nonquasi-static temperate distribution for this high power dissipation level (only selected thermal nodes are indicated in Fig. 10). The quasi-logarithmically spaced grid has a 4-μm grid spacing in the top 20 μm of the silicon chip to resolve the temperature distribution for the maximum heating rate of 10,000 W/0.1 cm^2 that occurs for 500-V avalanche sustaining at the 20 A/0.1 cm^2 device current density rating.

Next, consider Fig. 11, which shows the approximately 10-A, 10-V, 60-Hz output characteristics of a device with a base lifetime of $\tau_{HL}(300\text{ K}) = 7.1\ \mu$s. The measured characteristics of Fig. 11a are obtained using the TEK 370 curve tracer single-family digital measurement with the 60-Hz rectified sinewave collector supply and the 0.25-Ω power limiting resistance. The device package is mounted on a water-cooled, temperature-controlled test fixture at 300 K. The simulated results of Figs. 11b through 11d are obtained for an electrical network that is equivalent to the TEK 370 curve tracer and the thermal network of Fig. 2b, but with the ambient temperature source $T_a = 300$ K connected directly to the package case T_c. The simulated output characteristics of Fig. 11b are obtained using the Saber PLTOOL waveform calculator to plot the simulated current waveform as a function of the voltage waveform. The positive slope of the saturation current versus anode voltage in Figs. 11a and 11b is due to the positive saturation region temperature coefficient (Fig. 6). The thermal looping of the saturation characteristics occurs because the chip temperature does not reach a steady-state condition.

Fig. 11c shows the transient anode voltage, anode current, and chip surface temperature waveforms for the 8-V and 9-V curves of Fig. 11b. For this approximately 100-W power dissipation condition, the chip is heated evenly, but the temperature does not reach a steady-state condition as is evident by the delay in the peak temperature with respect to the peak anode voltage waveform. Fig. 11d shows the temperature waveforms at equally spaced positions within the silicon chip (solid lines from 0 through 500 μm) and at selected positions within the package (dashed lines from 500 through 2500 μm). For this 100-W, 60-Hz

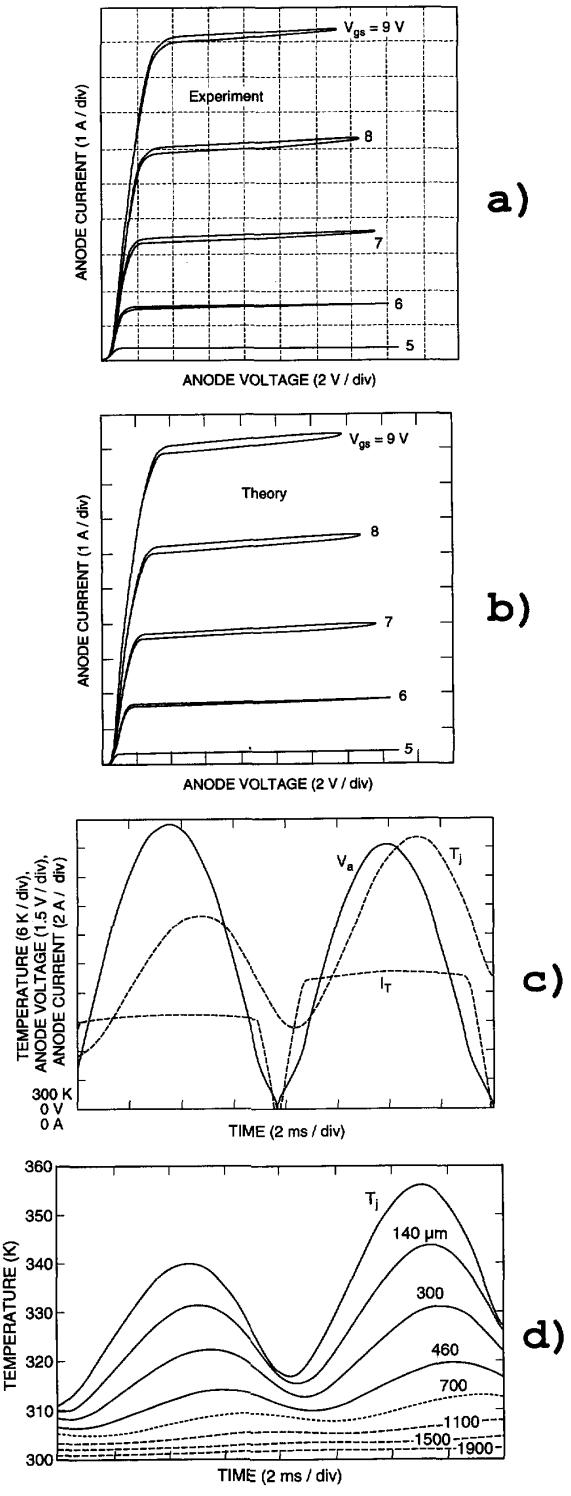

Fig. 11. Output characteristics of a $\tau_{HL}(300\text{ K}) = 7.1\ \mu$s IGBT including self-heating. a) Measured using a TEK 370 curve tracer, with a 60-Hz rectified sinewave collector supply. b) Simulated for same electrical and thermal conditions. c) Simulated curve tracer anode voltage, anode current, and chip surface temperature waveforms. d) Simulated temperature waveforms at selected positions within the silicon chip (solid) and package (dashed).

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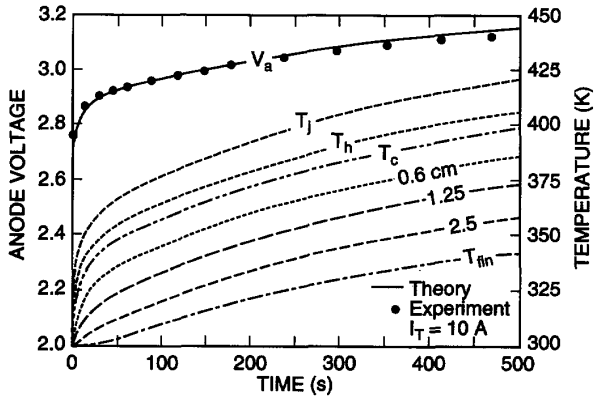

Fig. 12. Simulated and measured thermal drift of the IGBT on-state voltage for V_{gs} = 20 V and τ_{HL}(300 K) = 0.3 μs. Temperature waveforms at the silicon chip surface T_j, the chip-package interface T_h, the package-heatsink interface T_c, the heatsink fins T_{fin}, and selected radii from the heat source within the heatsink.

power dissipation function, the thermal gradient is nearly constant in the silicon chip, and a grid spacing of 100 μm distributed evenly throughout the chip would be sufficient to represent the temperature distribution in the chip. However, only the first 600 μm of the package (500 through 1100 μm) have 60-Hz fluctuation in the temperature waveform, and only the top half of the package (500 through 1500 μm) is heated significantly at the end of the five-member single-family measurement.

Finally, Fig. 12 shows the thermal drift of the on-state voltage for a constant gate voltage of V_{gs} = 20 V and a constant 10-A anode current step, where the heatsink fins are vertically oriented in a 300-K open area. The on-state voltage of the τ_{HL}(300 K) = 0.3 μs device increases with time because it has a positive temperature coefficient (Fig. 7). For the 30-W power dissipation level, several seconds are required for the heat to diffuse to the area of the heatsink beneath the package, several tens of seconds are required for the heat to diffuse to a radius of a few centimeters beyond the heat source, and several hundred seconds are required to heat the entire thermal network to a steady-state fin temperature. Thus for this low power dissipation level, the entire thermal network including the chip, package, and heatsink are heated, and several kJ of dissipated power are required to heat the chip surface to 100 K above the ambient. This is in contrast to the 100 mJ required for the high power short-circuit condition of Fig. 10.

VI. Conclusions

A dynamic electro-thermal model has been developed for the IGBT and has been implemented into the Saber circuit simulator. The model accurately predicts the temperature dependence of the IGBT electrical characteristics, the dynamic self-heating, and the nonquasi-static heating process that occurs for high power dissipation levels. The model is based upon the temperature dependence of the IGBT model parameters and the temperature dependence of the physical properties of silicon. A new methodology has been introduced to develop thermal network component models for the device silicon chip, device packages, and heatsinks. The thermal component models are connected to the IGBT thermal terminal to form electro-thermal networks. The dynamic electro-thermal simulations describe the dynamic temperature distribution within the thermal network as well as the current and voltage waveforms of the electrical network. The electro-thermal simulations are useful for describing the silicon chip surface temperature for arbitrary external circuit conditions and for describing the change in electrical characteristics as the device is heated.

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Certain commercial software products and electronic instruments are identified in this paper in order to specify the experimental procedure adequately. Such identification does not imply recommendation or endorsement by the National Institute of Standards and Technology, nor does it imply that these products are the best available products for the purpose.

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NOMENCLATURE [a]

A	Device active area, heat flow area (cm^2).
$b = \mu_n/\mu_p$	Ambipolar mobility ratio.
BV_k	Break-down voltage coefficient.
BV_{cb0}	Collector-base junction breakdown voltage (V).
BV_{ce0}	Open-base bipolar breakdown voltage (V).
c	Specific heat (J/cm·K).
C_{cer}	Collector-emitter redistribution capacitance (F).
C_i	Thermal capacitance of node i (J/K).
D_n, D_p	Base electron, hole diffusivity (cm^2/s).
D_{ne}	Emitter electron diffusivity (cm^2/s).
H_i	Heat energy at node i (J).
i	Discretization indices.
I_{bss}	Charge control base current (A).
I_c	Collector current (A).
I_{ccer}	Collector-emitter redistribution current (A).
I_{css}	Charge control collector current (A).
I_{mos}	MOSFET channel current (A).
I_{mult}	Multiplication current (A).
I_{sne}	Emitter electron saturation current (A).
I_T	Anode current (A).
k	Boltzmann's constant (J/K).
$k(T)$	Thermal conductivity (W/cm·K).
$k_{i,i+1}$	$k(T)$ between nodes i and $i+1$ (W/cm· K).
K_p	MOSFET transconductance parameter (A/V^2).
M	Impact ionization multiplication factor.
n_i	Base intrinsic carrier concentration (cm^{-3}).
n_{ie}	Emitter intrinsic carrier concentration (cm^{-3}).
N_E	Emitter dopant density (cm^{-3}).
P_{ib}	Base current dissipated power (W).
P_{ic}	Collector current dissipated power (W).
P_{imos}	MOSFET dissipated power (W).
P_{imult}	Multiplication current dissipated power (W).
P_{irb}	Base resistance dissipated power (W).
Power	Total dissipated power (W).
R_b	Conductivity modulated base resistance (Ω).
R_g	Gate drive resistance (Ω).
$R_{i,i+1}$	Thermal resistance between x_i and x_{i+1} (W/K).
T_0	Reference temperature (K).
T_a	Ambient temperature (K).
T_c	Package case temperature (K).
T_{fin}	Heatsink fin temperature (K).
T_h	Package header temperature (K).
T_i	Temperature at node i (K).
T_j	Silicon chip surface temperature (K).
V_a	Anode-cathode voltage (V).
V_{aa}	Anode supply voltage (V).
V_{ae}	Voltage across R_b (V).
$V_{ds} = V_{bc}$	Drain-source, base-collector voltage (V).
V_{eb}	Emitter-base junction voltage (V).
V_{ebd}	Emitter-base diffusion potential (V).
V_{ec}	Emitter-collector voltage (V).
V_{gon}	Gate supply pulse amplitude (V).
V_{gs}	Gate-source voltage (V).
V_T	MOSFET threshold voltage (V).
v_{nsat}, v_{psat}	Electron, hole saturation velocity (cm/s).
W_E	Emitter metallurgical width (cm^2).
x_i	Position of node i (cm).
α_1, α_2	Carrier-carrier scattering coefficients.
$\beta_{tr,v}$	Relative size of current tail.
$1/\beta_{tr,v}^{max} \cdot I_k$	Slope of $1/\beta_{tr,v}$ versus current (A^{-1}).
τ_e	Emitter lifetime (s).
τ_{HL}	High-level injection lifetime (s).
μ_n, μ_p	Electron, hole mobility ($cm^2/V{\cdot}s$).
ρ	Mass density (gm/cm^3).

[a] Model parameters with subscript 1 represent temperature coefficients.

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