

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv353	DATE FILED 9/12/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF Daedalus Prime LLC		DEFENDANT Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Semiconductor, Inc., and Samsung Austin Semiconductor, LLC
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 10,541,334	1/21/2020	Daedalus Prime LLC
2 9,202,699	12/1/2015	Daedalus Prime LLC
3 10,727,183	7/28/2020	Daedalus Prime LLC
4 9,627,321	4/18/2017	Daedalus Prime LLC
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548

CONFIRMATION NO. 1082

POWER OF ATTORNEY NOTICE

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204



OC000000130985367

Date Mailed: 01/10/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/04/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/tmwilliams/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548

CONFIRMATION NO. 1082

POA ACCEPTANCE LETTER

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002



OC000000130985375

Date Mailed: 01/10/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/04/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/tmwilliams/

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	16/559,086
Filing Date	September 3, 2019
First Named Inventor	Boyan Boyanov
Title	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
Art Unit	2898
Examiner Name	Joseph M. Galvin, III
Attorney Docket Number	D0480-PA-13290-US-04

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	January 4, 2022
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
16/559,086	September 3, 2019

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or
Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Lisa Hopkinson

Date (Optional)

December 20, 2021

Name

Lisa Hopkinson

Title

Administrator of Patents

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	44663376
Application Number:	16559086
International Application Number:	
Confirmation Number:	1082
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan BOYANOV
Customer Number:	31817
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	P38794USDC-C1 111548
Receipt Date:	04-JAN-2022
Filing Date:	03-SEP-2019
Time Stamp:	15:14:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2022-01-04_POA_D0480-PA-13290-US-04.pdf	1254736	no	2
			9a1d2f7556a80181c6b3095dceaf64139b7e ec07		
Warnings:					

Information:	
Total Files Size (in bytes):	1254736
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/559,086	07/28/2020	10727183	P38794USDC-C1 111548	1082

31817 7590 07/08/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Boyan BOYANOV, Portland, OR;
Intel Corporation, Santa Clara, CA;
Kanwal Jit SINGH, Hillsboro, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 1 of 4	Attorney Docket No: P38794USDC-C1 111548	

US PATENT DOCUMENTS

Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 7,396,757	07/08/2008	~~IBM CORP~~ Yang	
		US 6,908,847	06/21/2005	SAITO, TATSUYUKI, ET AL.	
		US 5,470,789	11/28/1995	Misawa	
		US 7,338,908	03/04/2008	Koos et al.	
		US 7,396,759	07/08/2008	Van Schravendijk Bart et al.	
		US-8,043,958	10/25/2011	Jonathan D. Reid, et al.	
		US-6,348,731	02/19/2002	Leon Ashley, et al.	
		US-6,114,238	09/05/2000	Kuan-Yang Liao	
		US-6,046,108	04/04/2000	Chung-Shi Liu, et al.	
		US-20050001325	01/06/2005	Andricacos et al.	
		US-20060128144	06/15/2006	Hyun-Mog Park et al.	
		US-20090127097	05/21/2009	Chen kei-Wei et al.	
		US-20090283499	11/19/2009	Mayer Steven T. et al.	
		US-20100081276	04/2010	Ishizaka	

Change(s) applied
to document,
/J.T./
5/28/2020

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		JP 6-275612A	09/30/1994	Misawa, Nobuhiro		
		CN 1364311A	08/14/2002	Kun, Hu Chao et al.		
		CN 1921102A	02/28/2007	Shih, Chien-Hsueh		
		JP 3326698	09/24/2002	Misawa Nobuhiro		
		KR-10-2009-0085066	08/06/2009	IBM		
		CN-101490825A	07/22/2009	IBM		
		CN-1420560	05/28/2003	HITACHI LTD		
		CN 1575508A	02/02/2005	Christopher Thomas et al.		
		KR 1020100109932	10/11/2010	IBM Corporation		
		WO 2009098120A 1	08/13/2009	IBM Corporation		
		JP 2009506536A	02/12/2009	Freescale Semiconductor		
		WO 2007024470A2	03/01/2007	Freescale Semiconductor		
		WO 2002045142	08/06/2002	Christopher Thomas et al.		
		CN 101064295	10/31/2007	Zhang et al.		

EXAMINER /JOSEPH M GALVIN III/

DATE CONSIDERED 03/27/2020

Based on PTO/SB/08A(09-05) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

000197

OR



The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	16/559,086

Completed by (check one):



Applicant/Inventor

/Justin K. Brask/

Signature



Attorney or Agent of record 61080

(Reg. No.)

Justin K. Brask

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

503-222-9981

Requester's telephone number



Assignee recorded at Reel _____ Frame _____

6/23/2020

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.



* Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETE D FORMS TO THIS ADDRESS. SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		16559086		
Filing Date:		03-Sep-2019		
Title of Invention:		METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
First Named Inventor/Applicant Name:		Boyan BOYANOV		
Filer:		Justin K. Brask/Lisa Puccinelli		
Attorney Docket Number:		P38794USDC-C1 111548		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1000

Electronic Acknowledgement Receipt	
EFS ID:	39800247
Application Number:	16559086
International Application Number:	
Confirmation Number:	1082
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan BOYANOV
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38794USDC-C1 111548
Receipt Date:	23-JUN-2020
Filing Date:	03-SEP-2019
Time Stamp:	19:49:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$1000
RAM confirmation Number	E20206MJ50438154
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.21 (Miscellaneous fees and charges) 37 CFR 1.20 (Post Issuance fees)	

37 CFR 1.19 (Document supply fees)
 37 CFR 1.17 (Patent application and reexamination processing fees)
 37 CFR 1.16 (National application filing, search, and examination fees)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P38794USDC-C1_Issue_Fee_06-23-20.pdf	96075	no	1
			ed30fb645a4227dc817974ea08d290c3781241d2		
Warnings:					
Information:					
2	Maintenance Fee Address Change	P38794USDC-C1_Maintenance_Fees.pdf	312397	no	2
			7f7bd8fe2a0bd3e54df31a7e125e6800900d39a5		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30545	no	2
			6ebb7c6c2ef8db04fd2836dde68f099d8c4beb3		
Warnings:					
Information:					
Total Files Size (in bytes):			439017		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 04/02/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Lisa Puccinelli	(Typed or printed name)
/Lisa Puccinelli/	(Signature)
June 23, 2020	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548	1082

TITLE OF INVENTION: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	07/02/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
GALVIN III, JOSEPH M	2898	257-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Schwabe, Williamson & Wyatt, P.C.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Intel Corporation

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 50-0393

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Justin K. Brask/

Date June 23, 2020

Typed or printed name Justin K. Brask

Registration No. 61080



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE

United States Patent and Trademark Office

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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548	1082

31817 7590 05/11/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER

GALVIN III, JOSEPH M

ART UNIT	PAPER NUMBER
----------	--------------

2898

NOTIFICATION DATE	DELIVERY MODE
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05/11/2020

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

(corrected) Notice of Allowability	Application No. 16/559,086	Applicant(s) BOYANOV et al.		
	Examiner JOSEPH M GALVIN III	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%;">Art Unit 2898</td> <td style="width: 50%;">AIA (FITF) Status No</td> </tr> </table>	Art Unit 2898	AIA (FITF) Status No
Art Unit 2898	AIA (FITF) Status No			

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to IDS filed 05/01/2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>05/01/2020</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☐ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	---

/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	
--	--

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	16/559,086
	Filing Date	September 3, 2019
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1		Attorney Docket No: P38794USDC-C1

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance from Taiwan Patent Application No. 107139026 (Attorney Docket No. P38794TW-D1-D1) mailed April 17, 2020, 3 pages.	X
		Office Action from Chinese Patent Application No. 201711404006.5 (Attorney Docket No. P38794CN-D-D1) mailed April 2, 2020, 5 pages.	

EXAMINER /JOSEPH M GALVIN III/

DATE CONSIDERED 05/07/2020

Based on PTO/SB/08A(09-05) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	16/559,086
	Filing Date	September 3, 2019
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1		Attorney Docket No: P38794USDC-C1

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance from Taiwan Patent Application No. 107139026 (Attorney Docket No. P38794TW-D1-D1) mailed April 17, 2020, 3 pages.	X
		Office Action from Chinese Patent Application No. 201711404006.5 (Attorney Docket No. P38794CN-D-D1) mailed April 2, 2020, 5 pages.	

EXAMINER

DATE CONSIDERED

Based on PTO/SB/08A(09-05) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Electronic Patent Application Fee Transmittal				
Application Number:		16559086		
Filing Date:		03-Sep-2019		
Title of Invention:		METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
First Named Inventor/Applicant Name:		Boyan BOYANOV		
Filer:		Justin K. Brask/Lisa Puccinelli		
Attorney Docket Number:		P38794USDC-C1 111548		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
Total in USD (\$)				240

Electronic Acknowledgement Receipt	
EFS ID:	39330783
Application Number:	16559086
International Application Number:	
Confirmation Number:	1082
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan BOYANOV
Customer Number:	31817
Filer:	Justin K. Brask/Lisa Puccinelli
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38794USDC-C1 111548
Receipt Date:	01-MAY-2020
Filing Date:	03-SEP-2019
Time Stamp:	19:07:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$240
RAM confirmation Number	E202051J08247866
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)					
37 CFR 1.20 (Post Issuance fees)					
37 CFR 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794USDC-C1_IDS_05-01-20.pdf	323570	yes	2
			d86247bccb0b646688e42ac272d590794f0492cf		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	Ref_CN-D-D1_04-02-20.pdf	190947	no	5
			9d5f2f9215ced24e97d4912a9f2a110755b76145		
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	Ref_TW-D1-D1_NOA_04-17-20.pdf	208018	no	3
			dd31704ea50e3a00ed53fbee0d4c43c7af9abcbcb		
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30687	no	2
			45ba2ecb82b3644ad3a77a9b9b9dd32c65d2dbe3f		
Warnings:					
Information:					
Total Files Size (in bytes):			753222		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No. 16/559,086

Filing Date September 3, 2019

First Inventor Boyanov et al.

Art Unit 2898

Examiner Name Galvin III, Joseph M.

Attorney Docket No. P38794USDC-C1

Conf. No. 1082

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted after Allowance but prior to payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

- ☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

- ☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

- ☐ None

- ☒ The IDS Filing Fee in the amount of \$240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

- ☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature /Justin K. Brask/

Date (MM-DD-YYYY) 05-01-2020

Name/Print Justin K. Brask

Registration Number 61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli /Lisa Puccinelli/

Date 05-01-2020

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
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www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

31817 7590 04/02/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER

GALVIN III, JOSEPH M

ART UNIT

PAPER NUMBER

2898

DATE MAILED: 04/02/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548	1082

TITLE OF INVENTION: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	07/02/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 04/02/2020
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548	1082

TITLE OF INVENTION: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1000	\$0.00	\$0.00	\$1000	07/02/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
GALVIN III, JOSEPH M	2898	257-758000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548	1082
31817	7590	04/02/2020	EXAMINER	
SCHWABE, WILLIAMSON & WYATT, P.C. 1211 SW 5th Avenue, Suite 1600 Portland, OR 97204			GALVIN III, JOSEPH M	
			ART UNIT	PAPER NUMBER
			2898	

DATE MAILED: 04/02/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/559,086	Applicant(s) BOYANOV et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to documents filed 09/03/2019.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☒ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>09/03/2019, 03/12/2020</u> .	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material ____.	7. ☐ Other ____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. ____.	

/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	
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DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Allowable Subject Matter

Claims 1-25 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 1, Park et al (US 2006/0128144) teaches an integrated circuit structure, comprising: a dielectric layer (104) having an upper surface, the dielectric layer comprising silicon, oxygen and carbon; ([0018] silicon oxide, carbon doped oxide)

a conductive structure (108, 126, 128) in the dielectric layer, the conductive structure comprising:

a first conductive material (126) comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; ([0021] the first conductive material is copper and is below an upper portion of the dielectric layer) and

a second conductive material (128) on the upper surface of the first conductive material (126), the second conductive material comprising cobalt (Co), wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material (128) and the second conductive material (126) meet, wherein the second conductive material (126) has an upper surface having a

portion substantially co-planar with the portion of the upper surface of the dielectric layer (104); ([0023]) and

a barrier layer (108) partially surrounding the conductive structure (126,128), the barrier layer comprising tantalum. ([0018] the barrier layer is tantalum nitride)

Ishizaka et al (US 2010/0081276), teaches a similar device with a copper material (122), a cobalt layer (124) on the copper layer, and a barrier layer (118) formed around the conductive structure, wherein the dielectric material (104) is formed comprising silicon, oxygen, and carbon. ([0021])

However the prior art fails to teach or reasonably suggest a motivation for wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer in combination with the other limitations of claim 1.

With respect to claim 9, Park teaches a method of fabricating an integrated circuit structure, the method comprising:

forming a dielectric layer (104) comprising silicon, oxygen and carbon; ([0018] silicon oxide, carbon doped oxide)

forming a trench (106) in the dielectric layer (104); (Fig. 2 [0018])

forming a barrier layer (108) in the trench (106), the barrier layer comprising tantalum; (Fig. 3 [0018])

forming a first conductive material (126) within the barrier layer (108) , the first conductive material comprising copper; (Fig. 5 [0020])

recessing the first conductive material (126) below a portion of an upper surface of the dielectric layer (104); (Fig. 6 [0022]) and

forming a second conductive material (128) on the upper surface of the recessed first conductive material (126), the second conductive material comprising cobalt (Co), wherein the first conductive material (126) and the second conductive material (128) have a same width at a location where the first conductive material and the second conductive material meet. (Fig. 8 [0023])

Ishizaka et al (US 2010/0081276), teaches a similar device with a copper material (122), a cobalt layer (124) on the copper layer, and a barrier layer (118) formed around the conductive structure, wherein the dielectric material (104) is formed comprising silicon, oxygen, and carbon. ([0021])

However the prior art fails to teach or reasonably suggest a motivation for wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer in combination with the other limitations of claim 9.

With respect to claim 18, Park teaches computing device (310), comprising: a board (320); and a component coupled to the board, the component including an integrated circuit structure, comprising:

a dielectric layer (104) having an upper surface, the dielectric layer comprising silicon, oxygen and carbon; ([0018] silicon oxide, carbon doped oxide)

a conductive structure (108, 126, 128) in the dielectric layer, the conductive structure comprising:

a first conductive material (126) comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive

material below a portion of the upper surface of the dielectric layer; ([0021] the first conductive material is copper and is below an upper portion of the dielectric layer) and a second conductive material (128) on the upper surface of the first conductive material (126), the second conductive material comprising cobalt (Co), wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material (128) and the second conductive material (126) meet, wherein the second conductive material (126) has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer (104); ([0023]) and

a barrier layer (108) partially surrounding the conductive structure (126,128), the barrier layer comprising tantalum. ([0018] the barrier layer is tantalum nitride)

Ishizaka et al (US 2010/0081276), teaches a similar device with a copper material (122), a cobalt layer (124) on the copper layer, and a barrier layer (118) formed around the conductive structure, wherein the dielectric material (104) is formed comprising silicon, oxygen, and carbon. ([0021])

However the prior art fails to teach or reasonably suggest a motivation for wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer in combination with the other limitations of claim 18.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH M GALVIN III whose telephone number is (571)272-0559. The examiner can normally be reached on M-F: 8:30AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 5712721864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOSEPH M GALVIN III/
Primary Examiner, Art Unit 2898

<i>Notice of References Cited</i>	Application/Control No. 16/559,086	Applicant(s)/Patent Under Reexamination BOYANOV et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20100081276-A1	04-2010	Ishizaka; Tadahiro	H01L21/02063	438/653
*	B	US-20060128144-A1	06-2006	Park; Hyun-Mog	H01L21/76849	438/643
	C					
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/559,086	Applicant(s)/Patent Under Reexamination BOYANOV et al.
	Examiner JOSEPH M GALVIN III	Art Unit 2898

CPC - Searched*		
Symbol	Date	Examiner
H01L21/76802,7684,76849,7685,76879,76883	03/27/2020	JG
H01L23/485,5226,528,53209,53238,53295	03/27/2020	JG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST search	03/27/2020	JG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	21/76802,7684,76849,7685,76879,76883	03/27/2020	JG
H01L	23/485,5226,528,53209,53238,53295	03/27/2020	JG
	See EAST search history	03/27/2020	JG

/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	
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Issue Classification 	Application/Control No. 16/559,086	Applicant(s)/Patent Under Reexamination BOYANOV et al.
	Examiner JOSEPH M GALVIN III	Art Unit 2898

CPC						
Symbol					Type	Version
H01L	/	23	/	53238	F	2013-01-01
H01L	/	21	/	76883	I	2013-01-01
H01L	/	21	/	7685	I	2013-01-01
H01L	/	23	/	485	I	2013-01-01
H01L	/	21	/	76849	I	2013-01-01
H01L	/	23	/	528	I	2013-01-01
H01L	/	23	/	53209	I	2013-01-01
H01L	/	23	/	53295	I	2013-01-01
H01L	/	21	/	76802	I	2013-01-01
H01L	/	21	/	7684	I	2013-01-01
H01L	/	21	/	76879	I	2013-01-01
H01L	/	23	/	5226	I	2013-01-01
H01L	/	2924	/	0002	A	2013-01-01

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
H01L	/	2924	/	0002	A	1	1	2013-01-01
H01L	/	2924	/	00	A	1	2	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	25	
/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	27 March 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2H

Issue Classification 	Application/Control No. 16/559,086	Applicant(s)/Patent Under Reexamination BOYANOV et al.
	Examiner JOSEPH M GALVIN III	Art Unit 2898

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L23/532		23	532
H01L21/768		21	768
NON-CLAIMED			

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	25	
/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898 (Primary Examiner)	27 March 2020 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 2H

Issue Classification 	Application/Control No. 16/559,086	Applicant(s)/Patent Under Reexamination BOYANOV et al.
	Examiner JOSEPH M GALVIN III	Art Unit 2898

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 25	
/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898 (Primary Examiner) _____ (Date) _____		27 March 2020 (Date)	O.G. Print Claim(s) 1
			O.G. Print Figure 2H

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	16/559,086
	Filing Date	September 3, 2019
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Maldonado, Julio J.
Sheet 1 of 1		Attorney Docket No: P38794USDC-C1

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. KR-D2-D1), mailed from December 13, 2019, 17 pgs.	X
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. KR-D2-D2), mailed January 22, 2020, 21 pgs.	X
		Office Action from Taiwan Patent Application No. 107139026.0 (Attorney Docket No. P38794TW-D1-D1, mailed December 12, 2020, 12 pgs.	X
		Notice of Allowance from Office Action from Taiwan Patent Application No. 108107479 (Attorney Docket No. P38794TW-D1-D1-D1, mailed September 25, 2019, 5 pgs.	X

EXAMINER /JOSEPH M GALVIN III/

DATE CONSIDERED 03/27/2020

Based on PTO/SB-08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 1 of 4	Attorney Docket No: P38794USDC-C1 111548	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 7,396,757	07/08/2008	IBM CORP	
		US 6,908,847	06/21/2005	SAITO, TATSUYUKI, ET AL.	
		US 5,470,789	11/28/1995	Misawa	
		US 7,338,908	03/04/2008	Koos et al.	
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Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
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EXAMINER /JOSEPH M GALVIN III/

DATE CONSIDERED 03/27/2020

Based on PTO/SB/08A(09-05) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 2 of 4	Attorney Docket No: P38794USDC-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance from Korean Patent Application No. 10-2016-7003215 (Attorney Docket No. P38794KR-D), mailed September 2, 2016, 2 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed March 2, 2017, 9 pages.	
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EXAMINER /JOSEPH M GALVIN III/

DATE CONSIDERED 03/27/2020

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Substitute for form 1449A/PTO	
	Complete if Known	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 3 of 4	Attorney Docket No: P38794USDC-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		3rd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed December 20, 2016, 11 pgs., with English translation	
		Notice of Final Rejection for Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2) Mailed December 5, 2017, 6 pgs., with English translation.	
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		Korean Patent Application No. 10-2016-7003215, Office Action dated April 1, 2016, 5 pages	

EXAMINER /JOSEPH M GALVIN III/

DATE CONSIDERED 03/27/2020

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	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 4 of 4	Attorney Docket No: P38794USDC-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"15477506"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:31
S2	53238	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:54
S3	158	((("BOYANOV") near3 ("Boyan"))) OR ((("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:54
S4	36636	((("INTEL") near3 ("CORPORATION"))).AS,AANM.	USPAT	OR	OFF	2018/11/26 08:54
S5	20	("8043958" "6348731" "6114238" "6046108" "7396757" "6908847" "5470789").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:57
S6	3	"20080027677"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:00
S11	3	"20070049008"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/26 09:03
S12	2	"20090200668"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:05
S13	193	(CuCo copper near2 cobalt) with interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:22
S14	17544	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:24
S15	9779	S14 and cap\$4	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/11/26 09:25

			EPO; JPO; DERWENT			
S17	2228	S15 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:25
S18	391	S17 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:59
S19	160	((("BOYANOV") near3 ("Boyan"))) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
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S21	17972	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S22	10028	S21 and cap\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S23	2289	S22 and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S24	406	S23 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S25	160	((("BOYANOV") near3 ("Boyan"))) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 16:03
S26	3	"20090283499"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:39
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S28	38405	((("INTEL") near3 ("CORPORATION"))).AS,AANM.	USPAT	OR	OFF	2019/06/09 14:42

S29	57250	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
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S31	10205	S30 and cap\$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
S32	2332	S31 and S29	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
S33	426	S32 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
S34	243	(CuCo copper near2 cobalt) with interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
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S41	3	"20090283499"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/08/01 15:39
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S45	1	"16559086"	US-PGPUB; USPAT	OR	OFF	2020/03/27 11:42
S46	14	("7396757" "6908847" "5470789" "7338908" "7396759" "8043958" "6348731" "6114238" "6046108" "20050001325" "20060128144" "20090127097" "20090283499" "20100081276").PN.	US-PGPUB; USPAT	OR	OFF	2020/03/27 11:46
S47	7	(cobalt Co) with (cap capping) with (round\$3 curv\$3) with corner	US-PGPUB; USPAT; USOCR;	OR	OFF	2020/03/27 11:55

			EPO; JPO; DERWENT			
S48	47	(metal) with (cap capping) with (round\$3 curv\$3) with corner	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/03/27 11:55
S49	133446	(Cu copper) with (interconnect via fill)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/03/27 11:58
S50	38108	(Co Cobalt) with (cap capping)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/03/27 11:58
S51	2314	S49 and S50	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2020/03/27 11:58
S52	40681	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT	OR	OFF	2020/03/27 11:58
S53	1348	S51 and S52	US-PGPUB; USPAT	OR	OFF	2020/03/27 11:59
S54	448	S51 and (curv\$3 round\$3)	US-PGPUB; USPAT	OR	OFF	2020/03/27 11:59
S55	0	("2007/0049008").URPN.	USPAT	OR	OFF	2020/03/27 12:11
S56	0	("2007/0049008").URPN.	USPAT	OR	OFF	2020/03/27 12:11

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	166	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US- PGPUB; USPAT	OR	OFF	2020/03/27 13:40
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L8	40681	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US- PGPUB; USPAT	OR	OFF	2020/03/27 13:40
L9	3861	((cobalt Co) near5 cap\$4).clm.	US- PGPUB; USPAT	OR	OFF	2020/03/27 13:40

L10	457	L8 and L9	US-PGPUB; USPAT	OR	OFF	2020/03/27 13:40
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S36	37244	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:47
S37	3679	((cobalt Co) near5 cap\$4).clm.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:47
S38	420	S36 and S37	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:48
S39	281	S38 and (copper Cu).clm.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:48

3/27/2020 2:45:47 PM**C:\Users\jgalvin\Documents\EAST\Workspaces\16559086.wsp**

Bibliographic Data

Application No: 16/559,086

Foreign Priority claimed: ☒ Yes ☐ No

35 USC 119 (a-d) conditions met: ☒ Yes ☐ No ☐ Met After Allowance

Verified and Acknowledged: /JOSEPH M GALVIN III/

Examiner's Signature

Initials

Title:

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
09/03/2019	257	2898	P38794USDC-C1 111548
RULE			

APPLICANTS

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Kanwal Jit SINGH Hillsboro, OR, UNITED STATES

CONTINUING DATA

This application is a CON of 15477506 04/03/2017 PAT 10446493

15477506 is a CON of 14675613 03/31/2015 PAT 9627321

14675613 is a DIV of 13991899 06/05/2013 PAT 9373584

13991899 is a 371 of PCT/US2011/059453 11/04/2011

FOREIGN APPLICATIONS

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	Application Number	16/559,086
	Filing Date	September 3, 2019
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Maldonado, Julio J.
Sheet 1 of 1		Attorney Docket No: P38794USDC-C1

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Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. KR-D2-D1), mailed from December 13, 2019, 17 pgs.	X
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. KR-D2-D2), mailed January 22, 2020, 21 pgs.	X
		Office Action from Taiwan Patent Application No. 107139026.0 (Attorney Docket No. P38794TW-D1-D1, mailed December 12, 2020, 12 pgs.	X
		Notice of Allowance from Office Action from Taiwan Patent Application No. 108107479 (Attorney Docket No. P38794TW-D1-D1-D1, mailed September 25, 2019, 5 pgs.	X

EXAMINER	DATE CONSIDERED
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Based on PTO/SB-08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	38852744
Application Number:	16559086
International Application Number:	
Confirmation Number:	1082
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan BOYANOV
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC-C1 111548
Receipt Date:	12-MAR-2020
Filing Date:	03-SEP-2019
Time Stamp:	20:53:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Other Reference-Patent/App/Search documents	Ref_KR-D2-D1_OA_12-13-19.pdf	2583132 73b900a709de125093e058d66b698b3733dc7e30	no	17
Warnings:					

Information:					
2	Other Reference-Patent/App/Search documents	Ref_KR-D2-D2_OA_01-22-20_.pdf	2204063	no	21
			8c9d5cc2009f23e0c21045b150629da5eadcdc10		
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	Ref_TW-D1-D1_OA_12-12-20-.pdf	613132	no	12
			e6488d973c101988067fc4955faf32d277356abb		
Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	Ref_TW-D1-D1-D1_NOA_09-25-19.pdf	646123	no	5
			12983bd24054513e63ccaa4e59d4b71b67f32b65		
Warnings:					
Information:					
5		P38794USDC-C1_IDS_03-12-20.pdf	430215	yes	2
			d43ee9efa846aedaba645ae3a8e72d15bb50e479		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
Total Files Size (in bytes):			6476665		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No. 16/559,086

Filing Date September 3, 2019

First Inventor Boyanov, et al.

Art Unit 2898

Examiner Name Maldonado, Julio J.

Attorney Docket No. P38794USDC-C1 Conf. No. 1082

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of \$240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature /Michael A. Bernadicou/

Date (MM-DD-YYYY) 03-12-2020

Name/Print Michael A. Bernadicou

Registration Number 35,934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli /Lisa Puccinelli/

Date 03-12-2020

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/559,086	09/03/2019	Boyan BOYANOV	P38794USDC-C1 111548

CONFIRMATION NO. 1082

31817

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

PUBLICATION NOTICE



OC000000113552474

Title:METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

Publication No.US-2019-0393157-A1

Publication Date:12/26/2019

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/559,086	09/03/2019	2812	2220	P38794USDC-CI 111548	25	3

CONFIRMATION NO. 1082

31817

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

FILING RECEIPT



0000000111085589

Date Mailed: 09/16/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Boyan BOYANOV, Portland, OR;
Kanwal Jit SINGH, Hillsboro, OR;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 15/477,506 04/03/2017
which is a CON of 14/675,613 03/31/2015 PAT 9627321
which is a DIV of 13/991,899 06/05/2013 PAT 9373584
which is a 371 of PCT/US2011/059453 11/04/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 09/12/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/559,086**

Projected Publication Date: 12/26/2019

Non-Publication Request: No

Early Publication Request: No

Title

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

page 2 of 4

countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/559,086			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760		
TOTAL CLAIMS (37 CFR 1.16(i))	25	minus 20 = *	5			x 100 =	500		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	2220		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =	x =	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =	x =	=	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x =	x =	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =	x =	=	
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
				TOTAL ADD'L FEE		TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									

Electronic Patent Application Fee Transmittal				
Application Number:		16559086		
Filing Date:				
Title of Invention:		METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
First Named Inventor/Applicant Name:		Boyan BOYANOV		
Filer:		Michael A. Bernadicou/Sheri Villarreal		
Attorney Docket Number:		P38794USDC-C1 111548		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	5	100	500
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2220

Electronic Acknowledgement Receipt	
EFS ID:	37055005
Application Number:	16559086
International Application Number:	
Confirmation Number:	1082
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan BOYANOV
Customer Number:	31817
Filer:	Michael A. Bernadicou/Sheri Villarreal
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC-C1 111548
Receipt Date:	03-SEP-2019
Filing Date:	
Time Stamp:	19:10:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$2220
RAM confirmation Number	E201993J11441968
Deposit Account	500393
Authorized User	Sheri Villarreal
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)
 37 CFR 1.20 (Post Issuance fees)
 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Fee Worksheet (SB06)	fee-info.pdf	36842	no	2
			47016d7101db3697cf1c1f414c54bdf21f88d09		

Warnings:

Information:

Total Files Size (in bytes):	36842
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 1 of 4		Attorney Docket No: P38794USDC-C1 111548

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 7,396,757	07/08/2008	IBM CORP	
		US 6,908,847	06/21/2005	SAITO, TATSUYUKI, ET AL.	
		US 5,470,789	11/28/1995	Misawa	
		US 7,338,908	03/04/2008	Koos et al.	
		US 7,396,759	07/08/2008	Van Schravendijk Bart et al.	
		US-8,043,958	10/25/2011	Jonathan D. Reid, et al.	
		US-6,348,731	02/19/2002	Leon Ashley, et al.	
		US-6,114,238	09/05/2000	Kuan-Yang Liao	
		US-6,046,108	04/04/2000	Chung-Shi Liu, et al.	
		US-20050001325	01/06/2005	Andricacos et al.	
		US-20060128144	06/15/2006	Hyun-Mog Park et al.	
		US-20090127097	05/21/2009	Chen kei-Wei et al.	
		US-20090283499	11/19/2009	Mayer Steven T. et al.	
		US-20100081276	04/2010	Ishizaka	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		JP 6-275612A	09/30/1994	Misawa, Nobuhiro		
		CN 1364311A	08/14/2002	Kun, Hu Chao et al.		
		CN 1921102A	02/28/2007	Shih, Chien-Hsueh		
		JP 3326698	09/24/2002	Misawa Nobuhiro		
		KR-10-2009-0085066	08/06/2009	IBM		
		CN-101490825A	07/22/2009	IBM		
		CN-1420560	05/28/2003	HITACHI LTD		
		CN 1575508A	02/02/2005	Christopher Thomas et al.		
		KR 1020100109932	10/11/2010	IBM Corporation		
		WO 2009098120A 1	08/13/2009	IBM Corporation		
		JP 2009506536A	02/12/2009	Freescale Semiconductor		
		WO 2007024470A2	03/01/2007	Freescale Semiconductor		
		WO 2002045142	08/06/2002	Christopher Thomas et al.		
		CN 101064295	10/31/2007	Zhang et al.		

EXAMINER

DATE CONSIDERED

Based on PTO/SB/08A(09-05) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 2 of 4	Attorney Docket No: P38794USDC-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Notice of Allowance from Korean Patent Application No. 10-2016-7003215 (Attorney Docket No. P38794KR-D), mailed September 2, 2016, 2 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed March 2, 2017, 9 pages.	
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. P38794KR-D2-D1), mailed April 23, 2018, 10 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed March 15, 2018 6 pages.	
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed May 1, 2018, 13 pages.	
		Office Action from Korean Patent Application No.10-2014-7015212 (Attorney Docket No. P38794KR), mailed January 7, 2016, 8 pages.	
		Office Action from Taiwan Patent Application No. 101140536 (Attorney Docket No. P38794TW), mailed March 22, 2017, 4 pages.	
		Office Action from Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN), mailed April 25, 2017, 19 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed February 20, 2018, 8 pages.	
		Notice of Allowance from Taiwan Patent Application No. 101140536 (Attorney Docket No. P38794TW), mailed June 29, 2017, 2 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed April 10, 2015, 7 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed April 10, 2015, 7 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed November 3, 2014, 7 pages.	
		Office Action from US Patent Application No. 14/675,613 (Attorney Docket No. P38794USD) mailed July 5, 2016, 6 pages.	
		Office Action from US Patent Application No. 14/675,613 (Attorney Docket No. P38794USD) mailed January 29, 2016, 8 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed June 28, 2017.	
		2nd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed July 1, 2016, 21 pgs., with English translation.	

EXAMINER

DATE CONSIDERED

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449)
 * EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.¹ Applicant's unique citation designation number (optional) ² Applicant is to place a check mark here if English language Translation is attached

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 3 of 4	Attorney Docket No: P38794USDC-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		3rd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed December 20, 2016, 11 pgs., with English translation	
		Notice of Final Rejection for Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2) Mailed December 5, 2017, 6 pgs., with English translation.	
		4th Non-Final Office Action for Chinese Patent Application No. 20118007 4611 .5 (Attorney Docket No. P38794CN) mailed September 12, 2017, 7 pgs., with English translation.	
		Final Office Action for Korean Patent Application 10-2016-70337 45 (Attorney Docket No. P38794KRD2) mailed July 18, 2017, 5 pgs., with English translation.	
		OTA, Takashi et al. Experimental Evaluation of Out-of-Plane Distortion of Electrostatically Chucked EUV Reticle," Proc of SPIE Vol. 6921, 69213S, 2008.	
		M.M. Antonijevic et al., "Copper Corrosion Inhibitors. A review," Int J. Electrochem Sci. Vol. 3, 2008, 28 pages.	
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		Taiwan Patent Application No. 101140536, Office Action and Taiwan IPO Search Report (with English Translation), dated November 27, 2014, 15 pages.	
		International Preliminary Report on Patentability for PCT/US2011/059453, mailed May 6, 2014, 8 pages.	
		Chih-Kai Hsu "Electromigration Study on SN Capped Air-gap Cu Damascenes Structure," 2006.	
		Korean Patent Application No.10-2014-7015212, Office Action dated August 3, 2015, 14 pages	
		Taiwan Patent Application No. 101140536, Office Action dated August 13, 2015, 17 pages.	
		Chinese Patent Application No. 201180074611.5, Office Action dated November 16, 2015, 20 pages.	
		Korean Patent Application No. 10-2014-7015212, Notice of Allowance, mailed March 2, 2016, 4 pages.	
		Korean Patent Application No. 10-2016-7003215, Office Action dated April 1, 2016, 5 pages	

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	Complete if Known	
	Application Number	Not Yet Assigned
	Filing Date	Herewith
	First Named Inventor	Boyanov, et al.
	Group Art Unit	
	Examiner Name	
Sheet 4 of 4	Attorney Docket No: P38794USDC-C1 111548	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		Taiwan Patent Application No. 101140536, Office Action, dated 04-19-16, 14 pages	
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed November 1, 2018, 7 pages.	
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed December 27, 2018, 5 pages.	
		Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed September 28, 2018, 40 pages.	
		Office Action for Chinese Patent Application 201180074611.5 (Attorney Docket No. P38794CN), mailed March 9, 2018, 7 pages.	
		Office Action from Taiwan Patent Application No. 106120928 (Attorney Docket No. P38794TW-D1), mailed July 6, 2018, 15 pages, with English Translation.	
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. P38794KR-D2-D1), mailed September 27, 2018, 6 pages, with English Translation.	
		Office Action from Korean Patent Application No. 10-2019-7002805 (Attorney Docket No. P38794KR-D2-D2-D1) mailed March 27, 2019, 3 pgs.	
		Office Action from Chinese Patent Application No. 201711404006.5 (Attorney Docket No. P38794CN-D-D1) mailed June 4, 2019, 10 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed February, 19, 2019, 18 pgs.	
		International Search Report and Written Opinion for PCT/US2011/059453, mailed July 16, 2012, 14 pages.	
		1 st Non-Final Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CND) mailed August 28, 2017, 10 pgs., with English translation.	
		Notice of Allowance for Taiwan Patent Application No. 106120928 (Attorney Docket No. P38794TW-D1), mailed January 15, 2019, 3 pages, with English Translation.	

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Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
First Named Inventor/Applicant Name:		Boyan BOYANOV		
Filer:		Michael A. Bernadicou/Sheri Villarreal		
Attorney Docket Number:		P38794USDC-C1 111548		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	5	100	500
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2220

Electronic Acknowledgement Receipt	
EFS ID:	37050186
Application Number:	16559086
International Application Number:	
Confirmation Number:	1082
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan BOYANOV
Customer Number:	31817
Filer:	Michael A. Bernadicou/Sheri Villarreal
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC-C1 111548
Receipt Date:	03-SEP-2019
Filing Date:	
Time Stamp:	16:38:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no				
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	P38794DC-C1_ADS_09_03_19.pdf	1256516 13da65f9c2278b0b78839ba2282e88b08a056e51	no	9
Warnings:					

Information:					
2		P38794DC-C1_APP_09_03_19.pdf	180298	yes	32
			4df853f58206638b13941fab4d5b38577cd29cd		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	25	
	Claims		26	31	
	Abstract		32	32	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P38794DC-C1_FIGS_09_03_19.pdf	143856	no	10
			8771bd039dc1ff97e9e0937caa04e4410830bb9c		
Warnings:					
Information:					
4	Oath or Declaration filed	P38794DC-C1_DEC_Executed.pdf	357722	no	3
			67558cbc8869bdf767f6c62876acc64b6f99baa7		
Warnings:					
Information:					
5		P38794DC-C1_IDS_09_03_19.pdf	385374	yes	5
			f803c0584752868bf7ec850db08923d3beeb9f813		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	5	
Warnings:					
Information:					
6	Non Patent Literature	P38794TW-D1_NOA_w_English_Translation_01_15_19.pdf	671879	no	3
			c40f7732173280f5d8c16c3a14bc25ea6ecf9f84		

Warnings:					
Information:					
7	Fee Worksheet (SB06)	fee-info.pdf	36728	no	2
			ef5bcadec301d957e0f97f13209ba1aa3fe79562		
Warnings:					
Information:					
Total Files Size (in bytes):			3032373		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38794USDC-C1 111548
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor	1				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Boyan		BOYANOV			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	Portland	State/Province	OR	Country of Residence	US	
Mailing Address of Inventor:						
Address 1	15760 NW Rondos Drive					
Address 2						
City	Portland	State/Province	OR			
Postal Code	97229	Country i	US			
Inventor	2				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Kanwal	Jit	SINGH			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	Hillsboro	State/Province	OR	Country of Residence	US	
Mailing Address of Inventor:						
Address 1	1055 NE Creeksedge Drive					
Address 2						
City	Hillsboro	State/Province	OR			
Postal Code	97124	Country i	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.						
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Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38794USDC-C1 111548
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

☐ An Address is being provided for the correspondence information of this application.			
Customer Number	31817		
Email Address	intelpatent@schwabe.com	Add Email	Remove Email

Application Information:

Title of the Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
Attorney Docket Number	P38794USDC-C1 111548	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:			
☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)	
Customer Number	31817		

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38794USDC-C1 111548
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	15477506	2017-04-03		
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15477506	Continuation of	14675613	2015-03-31	9627321	2017-04-18
Prior Application Status	Patented	Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14675613	Division of	13991899	2013-06-05	9373584	2016-06-21
Prior Application Status	Expired	Remove			
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
13991899	a 371 of international	PCT/US2011/059453	2011-11-04		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country ^j	Filing Date (YYYY-MM-DD)	Access Code ^j (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			Add

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38794USDC-C1 111548
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38794USDC-C1 111548
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38794USDC-C1 111548
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

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		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

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METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Patent Application No. 15/477,506 filed April 3, 2017, which is a continuation of co-pending U.S. Patent Application No. 14/675,613 filed on March 31, 2015, now U.S. Patent No. 9,627,321 issued April 18, 2017, which is a divisional application of U.S. Patent Application No. 13/991,899 filed June 5, 2013, now U.S. Patent No. 9,373,584 issued June 21, 2016, which is a U.S. National Phase application under 35 U.S.C. § 371 of International Application No. PCT/US2011/059453, filed November 4, 2011, entitled “METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS” the entire disclosure of which are hereby incorporated by reference in their entirety and for all purposes..

FIELD

[0002] Embodiments of the present invention relate to the field of electronic device manufacturing, and in particular, to forming interconnect structures.

BACKGROUND

[0003] As the feature size of electronic devices shrinks, reliability of interconnects becomes critical to integrated circuit performance. Generally, electromigration refers to the transport of material caused by the movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. The effect is especially important in applications where high current densities are used, for example, in

microelectronics structures involving logic devices. Typically, a metal capping technology is used to prevent electromigration.

[0004] Figure 1A is a cross-sectional view of a typical interconnect structure having metal electromigration caps. As shown in Figure 1A, metal interconnect lines, for example lines 103 and 104, formed on a dielectric substrate 101 are originally spaced apart at a line spacing 105. The electromigration caps, for example, caps 111-113, can be grown on the respective interconnect lines above a flat surface of the substrate using electroless plating. Generally, the growth of the electromigration caps on the interconnect lines is isotropic. The electromigration cap can grow on the interconnect metal line vertically as well as laterally above the substrate. The lateral growth of the metal electromigration caps may generate overhang structures, for example, an overhang 109 that protrude over the substrate 101 outside the width of the interconnect lines. As shown in Figure 1A, the lateral growth of the metal caps reduces a line-to-line spacing from spacing 105 to spacing 107.

[0005] Typically, the size of the overhang 109, is about 50% of the cap thickness. For example, if the two neighboring metal caps have the thickness of about 10 nanometers (“nm”), the total size of their overhangs can be about 2x5nm. As such, the line-to-line spacing can be reduced, for example, by a factor of two from about 20 (nm) to about 10 nm.

Figure 1B is a top view of a typical interconnect structure having metal electromigration caps electrolessly grown over a flat surface of substrate 121 having interconnect lines, such as an interconnect line 123. As shown in Figure 1B, the lateral growth of the metal caps above the substrate increases the line edge roughness (“LER”) and reduces line-to-line spacing. As shown in Figure 1B, the line-to-line spacing, for example, a line-to-line spacing 125, varies uncontrollably. Both the increased LER and reduced line-to-line spacing negatively impact on

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the reliability of the interconnect structures, increase the risk of current shorting that may lead to the failure of the entire integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, in which:

[0007] Figure 1A is a cross-sectional view of a typical interconnect structure having metal electromigration caps.

[0008] Figure 1B is a top view of a typical interconnect structure having metal electromigration caps.

[0009] Figure 2A shows a cross-sectional view of a substrate to fabricate an interconnect structure according to one embodiment of the invention.

[0010] Figure 2B is a view similar to Figure 2A, after a dielectric layer is formed over the substrate according to one embodiment of the invention.

[0011] Figure 2C is a view similar to Figure 2B, after a photoresist layer is deposited over the dielectric layer to form one or more openings in the dielectric layer according to one embodiment of the invention.

[0012] Figure 2D is a view similar to Figure 2C, after one or more openings are formed in the dielectric layer according to one embodiment of the invention.

[0013] Figure 2E is a view similar to Figure 2D, after a conductive layer is deposited over the dielectric layer according to one embodiment of the invention.

[0014] Figure 2F is a view similar to Figure 2E, after portions of conductive layer and the base layer are removed from the top surface of the dielectric layer outside the openings to form patterned conductive lines according to one embodiment of the invention.

[0015] Figure 2G is a view similar to Figure 2F, after conductive lines in a dielectric layer

over a substrate are recessed according to one embodiment of the invention.

[0016] Figure 2H is a view similar to Figure 2G, after capping layers are selectively deposited onto the respective recessed conductive lines in the channels to prevent electromigration according to one embodiment of the invention.

[0017] Figure 3A is a three-dimensional view 300 of an interconnect structure after recessing the conductive lines in a dielectric layer over a substrate according to one embodiment of the invention.

[0018] Figure 3B is a view 310 similar to Figure 3A, after capping layers are deposited into the respective channels formed by the recessed conductive lines according to one embodiment of the invention.

[0019] Figure 4 is a top view of an interconnect structure 400 having capping layers selectively deposited within channels formed by the recessed conductive lines in a dielectric layer over a substrate according to one embodiment of the invention.

[0020] Figure 5 shows a block diagram of an exemplary embodiment of a data processing system 500 having one or more electronic devices, e.g., transistors, memories, such as a memory 504, and a memory 518, processing logic devices, such a processing logic device 526, and any other integrated circuit and microelectronic devices that are built using methods described herein.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0021] In the following description, numerous specific details, such as specific materials, dimensions of the elements, etc. are set forth in order to provide thorough understanding of one or more of the embodiments of the present invention. It will be apparent, however, to one of ordinary skill in the art that the one or more embodiments of the present invention may be practiced without these specific details. In other instances, semiconductor fabrication processes, techniques, materials, equipment, etc., have not been described in great details to avoid unnecessarily obscuring of this description. Those of ordinary skill in the art, with the included description, will be able to implement appropriate functionality without undue experimentation.

[0022] While certain exemplary embodiments of the invention are described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described because modifications may occur to those ordinarily skilled in the art.

[0023] Reference throughout the specification to “one embodiment”, “another embodiment”, or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases “in one embodiment” or “for an embodiment” in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0024] Moreover, inventive aspects lie in less than all the features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly

incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention. While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative rather than limiting.

[0025] Methods and apparatuses to control a line edge roughness (“LER”) and line-to-line spacing in deposition of self-aligned metal caps are described herein. At least one conductive line is recessed to form a channel in a dielectric layer over a substrate. A capping layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is self-aligned to the conductive line. The channel is configured to contain the capping layer within the width of the conductive line. That is, the interconnect line is recessed to contain the cap growth within a channel self aligned to the interconnect line. The channel can be formed by etching the conductive line to a predetermined depth using a chemistry comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation, as described in further detail below. Methods and apparatuses described herein can be used to control the increase in LER associated with selectively deposited electromigration caps, for example, electroless cobalt caps. That is, an increase in LER and reduction in line-to-line spacing typically associated with the electromigration caps selectively deposited on the metal interconnect lines can be prevented by containing an electroless cap within a recess that is self-aligned to an interconnect line. Eliminating an increase in LER and preventing from reducing of the line-to-line spacing can decrease the risk of failure and increase the manufacturing yield of the electronic devices having reduced (e.g., nanometer scale) dimensions. The electronic devices

can be, for example, computer system architecture devices, e.g., transistors, memories, logic devices, and any other integrated circuit and microelectronic devices.

[0026] Figure 2A shows a cross-sectional view 200 of a substrate to fabricate an interconnect structure according to one embodiment of the invention. In one embodiment, substrate 201 includes a monocrystalline silicon. In one embodiment, substrate 201 includes a silicon-on-insulator (“SOI”). For alternate embodiments, substrate may comprise compound semiconductors, e.g., indium phosphide, gallium arsenide, gallium nitride, silicon germanium, and silicon carbide. In another embodiment, substrate 201 may include e.g., glass, and quartz. Substrate 201 may include one or more metallization layers of integrated circuits having active and passive devices, e.g., transistors, switches, optoelectronic devices, capacitors, resistors, interconnects (not shown). The one or more metallization layers of integrated circuits of substrate 201 may be separated from adjacent metallization layers by a dielectric material (not shown), e.g., interlayer dielectric. The adjacent metallization layers may be electrically interconnected by vias (not shown).

[0027] Figure 2B is a view similar to Figure 2A, after a dielectric layer 203 is formed over the substrate 201 according to one embodiment of the invention. In one embodiment, dielectric layer 203 is an interlayer dielectric (“ILD”). In one embodiment, dielectric layer 203 is a low-k dielectric, e.g., silicon dioxide, silicon oxide, and carbon doped oxide (“CDO”), or any combination thereof. In one embodiment, Dielectric layer 203 includes a nitride, oxide, a polymer, phosphosilicate glass, fluorosilicate (“SiOF”) glass, organosilicate glass (“SiOCH”), or any combination thereof. In one embodiment, dielectric layer 203 includes a spin-on low-k dielectric material. In one embodiment, dielectric layer 203 is silicon dioxide. In another embodiment, dielectric layer 203 is silicon nitride. dielectric layer 203 may be deposited using

any suitable deposition technique. In one embodiment, dielectric layer 203 may be deposited using blanket deposition technique, for example, chemical vapor deposition (“CVD”), sputtering, spin-on, or another thin film deposition technique. In one embodiment, dielectric layer 203 is deposited to the thickness in the approximate range of 50nm to 2 μ m.

[0028] Figure 2C is a view similar to Figure 2B, after a photoresist layer 204 is deposited over dielectric layer 203 to form one or more openings in dielectric layer 203 according to one embodiment of the invention. In one embodiment, photoresist layer 204 is deposited on a hard mask layer 202 formed on dielectric layer 203, as shown in Figure 2C. In another embodiment, photoresist layer 204 is deposited directly onto dielectric layer 203. As shown in Figure 2C, photoresist layer 204 and hard mask layer 202 are patterned and etched to form openings, such as an opening 220. Patterning and etching of the photoresist and hard mask is known to one of ordinary skill in the art of microelectronic device manufacturing. Patterning and etching of the photoresist may be performed using one of the techniques known to one of ordinary skill in the art of microelectronic device manufacturing. The technique may include masking the photoresist layer, exposing the masked layer to light, and then developing the unexposed portions to remove the portions of the photoresist layer that are exposed to light to form a window in the photoresist layer. In one embodiment, the process of exposing to light and removing the photoresist layer may be performed in a plasma reactor. The opening in hard mask 202 may be etched to expose a portion of dielectric layer 203 using a dry etching, e.g., reactive ion etching (“RIE”), wet etching, or any combination thereof techniques.

[0029] Figure 2D is a view similar to Figure 2C, after one or more openings, such as an opening 206, are formed in dielectric layer 203 according to one embodiment of the invention. In one embodiment, the openings are, such as opening 206, is etched through openings in hard

mask 203, such as opening 220. In another embodiment, the openings are formed by etching the dielectric layer through the openings in patterned photoresist 204 deposited directly onto dielectric layer 203. In one embodiment, the openings in the dielectric layer 203, for example, trenches, are formed using an anisotropic dry etching, e.g., plasma etching. In another embodiment, the openings in the dielectric layer 203 are formed using dry etching, wet etching, or a combination thereof techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the openings in dielectric layer 203 has the width in the approximate range of 0.005microns ("μm ") to 5 μm, and the depth in the approximate range of 0.005 μm to 10 μm. In one embodiment, the size of openings is determined by the size of a conductive line formed within ILD 203 later on in the process.

[0030] After forming the openings, such as opening 206, the photoresist and hard mask are removed. Removing of the photoresist and the hard mask from dielectric layer 203 is known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the photoresist and hard mask may be removed using a chemical technique, mechanical technique, or both.

[0031] Figure 2E is a view similar to Figure 2D, after a conductive layer 205 is deposited over dielectric layer 203 according to one embodiment of the invention. As shown in Figure 2E, forming of the conductive layer 205 involves filling the one or more openings in dielectric layer 203 with a conductive material to form one or more conductive lines. In one embodiment, a base layer (not shown) is first deposited on dielectric layer 203 covering the internal sidewalls and bottom of the openings, and then a conductive layer 205 is deposited on the base layer. In one embodiment, the base layer includes a conductive seed layer (not shown) deposited on a conductive barrier layer (not shown). The seed layer can include copper, and the conductive

barrier layer can include aluminum, titanium, tantalum, tantalum nitride, and the like metals.

[0032] The conductive barrier layer can be used to prevent diffusion of the conductive material from the seed layer, e.g., copper, into ILD 203. Additionally, the conductive barrier layer can be used to provide adhesion for the seed layer (e.g., copper). In one embodiment, to form the base layer, the conductive barrier layer is deposited onto the dielectric layer 203 covering the sidewalls and bottom of the opening, and then the seed layer is deposited on the conductive barrier layer. In another embodiment, the conductive base layer includes the seed layer that is directly deposited onto dielectric layer 203 covering the sidewalls and bottom of the openings. Each of the conductive barrier layer and seed layer may be deposited using any thin film deposition technique known to one of ordinary skill in the art of semiconductor manufacturing, e.g., by sputtering, blanket deposition, and the like. In one embodiment, each of the conductive barrier layer and the seed layer has the thickness in the approximate range of 1 to 100 nm. In one embodiment, the barrier layer may be a thin dielectric that has been etched to establish conductivity to the metal layer below. In one embodiment, the barrier layer may be omitted altogether and appropriate doping of the copper line may be used to make a “self-forming barrier”.

[0033] Conductive layer 205 fills the openings, such as an opening 206, and covers portions of the base layer (not shown) outside of the openings that are on top of dielectric layer 203. In one embodiment, conductive layer 205 e.g., copper, is deposited onto the seed layer of base layer of copper, by an electroplating process. In one embodiment, conductive layer 205 is deposited into the openings using a damascene process that is known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, conductive layer 205 is deposited onto the seed layer using one of selective deposition techniques known to one of

ordinary skill in the art of semiconductor manufacturing, e.g., electroplating, electroless plating, and the like. In one embodiment, the choice of a material for conductive layer 205 determines the choice of a material for the seed layer. For example, if the material for conductive layer 205 includes copper, the material for the seed layer also includes copper. In one embodiment, conductive layer 205 includes e.g., copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), Vanadium (V), Molybdenum (Mo), palladium (Pd), gold (Au), silver (Au), platinum Pt, or any combination thereof.

[0034] Figure 2F is a view similar to Figure 2E, after portions of conductive layer 205 and the base layer are removed from the top surface of dielectric layer 203 outside the openings to form patterned conductive lines, such as a conductive line 208 according to one embodiment of the invention. Portions of conductive layer 205 may be removed chemically, e.g., using etching, mechanically, e.g., using polishing, or by a combination of thereof techniques, e.g., using a chemical-mechanical polishing (“CMP”) technique known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, one or more patterned conductive lines are formed within dielectric layer 203 using methods described above. In another embodiment, the conductive lines are formed by patterning and etching of the conductive layer deposited on the top surface of dielectric layer 203. Patterning and etching of the conductive layer deposited on the top surface of the dielectric layer 203 is known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the thickness of the conductive line, for example, a thickness 211 is in the approximate range of 0.015 μ m to 1 μ m. In one embodiment, the width of the conductive line, for example, a width 209 is in the approximate range of 5nm to about 500nm. In one embodiment, the spacing between the

conductive lines, for example, a spacing 207, is from about 5nm to about 500nm. In one embodiment, the spacing between the conductive lines is from about 2nm to about 100nm.

[0035] Figure 2G is a view similar to Figure 2F, after the conductive lines, for example, a conductive line 208, in a dielectric layer over a substrate are recessed according to one embodiment of the invention. As shown in Figure 2G, channels, such as a channel 212, are formed in dielectric layer 203. As shown in Figure 2G, channels, such as channel 212, have sidewalls made of dielectric layer 203, such as sidewalls 214 and 216, and a bottom made of a respective conductive line, such as a bottom 218 made of conductive line 208.

[0036] In one embodiment, the channel has depth, such as a depth 213 from about 5 nm to about 50nm. In one embodiment, the depth of the channel is from about 2 nm to about 20nm. In one embodiment, the channel has depth that is from about 10% to about 50% of the thickness of the conductive line, such as a thickness 211 shown in Figure 2F. In one embodiment, the conductive lines are recessed to the depth, which is determined based on the thickness of a capping layer, as described in further detail below.

[0037] Figure 3A is a three-dimensional view 300 of an interconnect structure after recessing the conductive lines, such as a conductive line 305 and a conductive line 304, in a dielectric layer 303 over a substrate 301 according to one embodiment of the invention. Substrate 301, dielectric layer 303, and the conductive lines 305 and 304, can be, for example, any of the respective substrates, dielectric layers, and conductive lines, as described above. As shown in Figure 3A, channels, such as a channel 302 and a channel 307, are formed in a dielectric layer 303 over substrate 301 by recessing the conductive lines. As shown in Figure 3A, the channels are self-aligned to the respective conductive lines. For example, channel 307 is self-aligned to conductive line 305 and channel 302 is self-aligned to conductive line 304. As

shown in Figure 3A, the length of the channel, e.g., a length 315 is along the length of the conductive line, and the width of the channel, e.g., a width 307 is along the width of the conductive line. In one embodiment, the length of the channel is substantially longer than the width of the channel. In one embodiment, the width of the channel is less than 100nm, and the length of the channel is at least 500nm. In one embodiment, the width of the channel is from about 5 nm to about 500nm, and the length of the channel is from about a few hundred nanometers to about a few hundred microns. As shown in Figure 3A, the conductive lines, such as conductive lines 305 and 304 are separated by a distance, such as a spacing 309. In one embodiment, the spacing between the conductive lines, such as lines 305 and 304 is from about 5nm to about 500nm. In one embodiment, the spacing between the conductive lines, such as lines 305 and 304 is from about 2nm to about 100nm.

[0038] In one embodiment, recessing the conductive lines, such as line 208, lines 304 and 305, involves wet etching the conductive lines uniformly independent of a crystallographic orientation using a chemistry containing an etchant, an oxidizer, an inhibitor, and a solvent. That is, adding an inhibitor and a solvent to the etchant provides uniform etching of the conductive material independent of a crystallographic orientation, by forming, during etching, a passivation layer (not shown) on the conductive material. The wet etch chemistry containing an etchant, an oxidizer, an inhibitor, and solvent provides control over the depth of the etching of the conductive line, so that only a portion (e.g., 5% to 50%) of the conductive line can be recessed.

[0039] In one embodiment, the chemistry to wet etch the conductive lines to provide a channel that is free from a pattern dependence and a crystallographic preference comprises between about 1% to about 40% by mass of an etchant, between about 1% to about 10% by mass of an oxidizer, and between about 0.1% to about 1% by mass of an inhibitor, and between

about 1 to about 60% by mass of an organic solvent. In one embodiment, the chemistry to wet etch the conductive lines comprises an etchant from about 0.1% to about 70% by mass (depending on the etch rate of the etchant), an oxidizer from about 0.1% to about 10% by mass (depending on the strength of the oxidizer), an inhibitor from about 50 parts per million (ppm) to about 1% by mass; and a solvent between about 1 to about 60% by mass.

[0040] In one embodiment, the chemistry to etch the conductive lines can include an etchant, for example, a glycine, an ethylenediaminetetraacetic acid, an alpha-amino acid, a polycarboxylic acid, or a combination thereof; the oxidizer, for example, a peroxide, an ozone, a permanganate, a chromate, a perborate, a hypohalite, or a combination thereof; an inhibitor, for example, an azole, an amine, an amino acid, a phosphate, a phosphonate, or a combination thereof; and a solvent. The solvent can be an aqueous system (preferred), e.g., water, or an organic solvent. The examples of an organic solvents are propylene carbonate, sulfolane, glycol ethers, methylene chloride, and the like.

[0041] For example, regarding the etchant in the chemistry to etch copper conductive lines, Cu metal is typically in a zero oxidation state. In order to etch copper, the copper needs to be oxidized into a $0+n$ oxidation state where 'n' can be any of 1, 2, 3 or 4. Typically, 1st state and 2nd state are more common oxidation states of copper. For any molecule to act as an etchant, it needs to be able to bind copper in one of its oxidation states 1, 2, 3 or 4. This binding typically occurs through the use of group 15 (Nitrogen family), group 16 (Oxygen family) or group 17 (Halogen family) atoms in a molecule. In one embodiment, the etchant to etch copper conductive lines is an organic etchant, for example, any of glycine, ethylenediaminetetraacetic, alpha-amino acids, polycarboxylic acids (for example, citric acid that is a tricarboxylic acid), oxalic and malonic acids.

[0042] For example, an oxidizer in the chemistry to etch copper conductive lines is used to change the copper oxidation state from an insoluble copper metal to a soluble copper ion. The oxidizer can be chosen from any of the oxidizers, for example, any of peroxides (e.g., hydrogen peroxide), ozone, permanganates, chromates, perborates and hypohalites, and the like.

[0043] For example, to etch the copper constituting the current carrying line in a uniform and non-crystallographic orientation, it is important to add an inhibitor to the chemistry. The role of an inhibitor is to form a passivation layer (a polymeric compound formed from the molecules of the inhibitor binding copper in a specific and periodic manner). The formation of this passivation layer during the controlled etch of copper is critical to ensure uniformity of etching and preventing etching attacks (e.g., forming voids) along crystallographic (e.g., grain) boundaries. For example, any inhibitor that is not decomposed in the chosen oxidizer and etchant combination may be used in the chemistry to etch copper conductive lines. The classes of inhibitors are known to one of ordinary skill in the art of electronic device manufacturing. For example, any of organic inhibitors including azoles, amines, amino acids, phosphates and phosphonates can be used in the chemistry to etch the copper conductive lines.

[0044] In another embodiment, the conductive copper lines are recessed by wet etching using a chemistry comprising a citric acid and peroxide. A chemistry comprising citric acid and peroxide, however, typically has high etching rate that can be difficult to control. Additionally, an etching rate of the chemistry comprising citric acid and peroxide depends on a crystallographic orientation that may produce rough etched surface. Addition of a corrosion inhibitor, for example, benzotriazole ("BTA") to the chemistry, and dilution of the citric acid and peroxide in organic solvent can slow down the etching rate dramatically and eliminate the crystallographic nature of the etch, such as etching the voids in Cu along the grain boundaries

producing a smooth surface.

[0045] In one embodiment, the conductive lines are recessed by wet etching that involves any of spraying, and pouring the etching chemistry onto the conductive lines. In one embodiment, the conductive lines are recessed by wet etching that involves immersing the conductive lines into the etching chemistry solution. In one embodiment, the conductive lines are recessed by wet etching at a temperature from about 15°C to about 50°C for a predetermined time. In at least some embodiments, the conductive lines are recessed by dry etching, e.g., plasma etching.

[0046] Figure 2H is a view similar to Figure 2G, after the capping layers are selectively deposited onto the respective recessed conductive lines in the channels to prevent electromigration according to one embodiment of the invention. The conductive lines etched using the chemistry as described above, have a smooth uniform top surface to adhere the capping layer. As shown in Figure 2H, a capping layer 215 is deposited onto recessed conductive line 208 within channel 212. In one embodiment, the channel, such as channel 212, is configured to contain a capping layer within the width of the conductive line, e.g., width 209 shown in Figure 2F. That is, the recessed conductive line creates a channel which contains the growth of the capping layer within the channel that mitigates the reduction in line-to-line spacing and increase in LER. As shown in Figure 2H the capping layer 215 is located on the conductive line 208 within the sidewalls of the channel 212. In one embodiment, the capping layer is deposited on the recessed conductive line by an electroless deposition (e.g., plating), a chemical vapor deposition (“CVD”), a physical vapor deposition (“PVD”), or any other selective deposition techniques known to one of ordinary skill in the art of electronic device manufacturing. In one embodiment, a conductive line, such as line 208, comprises a first metal,

and the capping layer comprises a second metal other than the first metal to prevent electromigration of the first metal from the conductive line. In one embodiment, the metal for the capping layer is heavier than the metal for the conductive line to prevent electromigration.

[0047] For example, the conductive line can be made of any of the metals including copper, aluminum. In one embodiment, the capping layer, such as capping layer 215, is made of cobalt (“Co”), cobalt electroless alloys, e.g., CoBP, CoWBP, CoWP, CoWB, CoWP, or a combination thereof. In another embodiment, a capping layer, such as capping layer 215, is made of nickel (“Ni”), Ni electroless alloys, e.g., NiBP, NiWBP, NiWP, NiWB, NiWP, or a combination thereof. In another embodiment, a capping layer, such as capping layer 215, is made of platinum (“Pt”) group metals, for example, Pt, Pd, Ru, Ir, Rh as pure elements or alloys. The typical alloy elements for Pt group metals are W, B, P. In yet another embodiment, a capping layer, such as capping layer 215, is made of refractory metals, for example, Ta, W, Mo, or a combination thereof.

[0048] In one embodiment, the Co capping layer is deposited within a channel onto the recessed Cu conductive layer. In one embodiment, Ni capping layer is deposited within a channel onto the recessed Cu conductive layer. In one embodiment, refractory metal capping layer is deposited within a channel onto the recessed Cu conductive layer.

[0049] In one embodiment, the capping layers comprising a Pt group metal, Co, Ni, or a combination thereof, are deposited onto the conductive layers, e.g., copper, aluminum, using any of an electroless deposition, and a vapor phase deposition, e.g., CVD. In one embodiment, the capping layers including refractory metals are deposited onto the conductive layers, e.g., copper, aluminum, using any of a CVD and PVD techniques known to one of ordinary skill in the art of electronic device manufacturing. In one embodiment, the thickness of the capping layer, e.g., a

thickness 221, is from about 2 nm to about 50 nm. In one embodiment, the thickness of the capping metal layer is sufficient to prevent electromigration from the underlying conductive layer. In one embodiment, the capping layer has the thickness that is no greater than the depth of the channel within which the capping layer is deposited.

[0050] Figure 3B is a view 310 similar to Figure 3A, after capping layers are deposited into the respective channels formed by the recessed conductive lines according to one embodiment of the invention. As shown in Figure 3B, capping layers, such as a capping layer 311 and 319 are selectively deposited into respective channels, such as channel 302 and channel 307, as described above. As shown in Figure 3A, the capping layers are contained within their respective channels. As shown in Figure 3B, the capping layer 319 is separated from capping layer 311 by spacing 309. In one embodiment, the spacing between conductive lines 305 and 304 and the spacing between the capping layers 319 and 311 is the same.

[0051] Figure 4 is a top view of an interconnect structure 400 having capping layers selectively deposited within channels formed by the recessed conductive lines in a dielectric layer 401 over a substrate according to one embodiment of the invention. As shown in Figure 4, the LER of the interconnect lines, such as an interconnect line 403 is substantially reduced, the edges of the interconnect lines are smooth, and a line-to-line spacing, such as a line-to-line spacing 405 is increased and maintained between the lines. In one embodiment, the line-to-line spacing is increased by 2x cap thickness. This can result in rather dramatic decreases in electric field and time to dielectric breakdown, especially, for a future technology node having 20nm lines and 20nm spaces. The minimum cap thickness known to work today is 5nm. This means that with a conventional approach the line-line space would be 10nm instead of the 20nm drawn on a mask. Furthermore, currently, the size of the protrusions in the overhang tends to be about

50% of the cap thickness. For a typical cap thickness of 5-10nm using methods described above LER can be decreased by 3-5nm independent of line width. For a future 20 nm technology node, decrease in LER by 3-5nm can result in 15-20% increase in line-to-line spacing of an interconnect structure.

[0052] Figure 5 shows a block diagram of an exemplary embodiment of a data processing system 500 having one or more electronic devices, e.g., transistors, memories, such as a memory 504, and a memory 518, processing logic devices, such a processing logic device 526, and any other integrated circuit and microelectronic devices that are built using methods described herein. As shown in Figure 5, data processing system 500 includes a processor 502 having processing logic 526. In at least some embodiments, processing logic 526 contains at least one conductive line in a dielectric layer over a substrate, a channel in the dielectric layer over the one conductive line; and a capping layer on the at least one conductive line in the channel to prevent electromigration, as described herein. In at least some embodiments, each of the memories 504 and 518 contains at least one conductive line in a dielectric layer over a substrate, a channel in the dielectric layer over the one conductive line; and a capping layer on the at least one conductive line in the channel to prevent electromigration, as described herein

[0053] In alternative embodiments, the data processing system may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The data processing system may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The data processing system may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a

set of instructions (sequential or otherwise) that specify actions to be taken by that data processing system. Further, while only a single data processing system is illustrated, the term “data processing system” shall also be taken to include any collection of data processing systems that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[0054] The exemplary data processing system 500 includes a processor 502, a main memory 504 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 506 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 518 (e.g., a data storage device), which communicate with each other via a bus 530.

[0055] Processor 502 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 502 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 502 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 502 is configured to execute the processing logic 526 for performing the operations described herein.

[0056] The computer system 500 may further include a network interface device 508. The computer system 500 also may include a video display unit 510 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 512 (e.g., a keyboard), a cursor control device 514 (e.g., a mouse), and a signal

generation device 516 (e.g., a speaker).

[0057] The secondary memory 518 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 531 on which is stored one or more sets of instructions (e.g., software 522) embodying any one or more of the methodologies or functions described herein. The software 522 may also reside, completely or at least partially, within the main memory 504 and/or within the processor 502 during execution thereof by the computer system 500, the main memory 504 and the processor 502 also constituting machine-readable storage media. The software 522 may further be transmitted or received over a network 520 via the network interface device 508.

[0058] While the machine-accessible storage medium 531 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0059] In alternative embodiments, Figure 5 illustrates a computing device 500. The computing device 500 houses a board 530. The board may include a number of components, including but not limited to a processor 502 and at least one communication chip 508. The processor 502 is physically and electrically coupled to the board 530. In some implementations the at least one communication chip 508 is also physically and electrically coupled to the board

530. In further implementations, the communication chip 508 is integrated within the processor 502.

[0060] Depending on its applications, computing device 500 may include other components that may or may not be physically and electrically coupled to the board 530. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, a solid state drive, a compact disk (CD) drive, a digital versatile disk (DVD) drive, and so forth).

[0061] The communication chip 508 enables wireless communications for the transfer of data to and from the computing device 500. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 508 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 500 may include a plurality of communication chips 508. For instance, a first communication chip 508 may be dedicated to shorter range wireless

communications such as Wi-Fi and Bluetooth and a second communication chip 508 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0062] The processor 502 of the computing device 500 includes an integrated circuit die packaged within the processor 502. In some implementations of the invention, the integrated circuit die of the processor includes one or more devices, such as transistors or metal interconnects, that are formed using methods and apparatuses to control a line edge roughness and line-to-line spacing in deposition of self-aligned metal caps as described herein. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0063] The communication chip 508 also includes an integrated circuit die packaged within the communication chip 508. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more devices, such as transistors or metal interconnects, that are formed using methods and apparatuses to control a line edge roughness and line-to-line spacing in deposition of self-aligned metal caps as described herein.

[0064] In further implementations, another component housed within the computing device 600 may contain an integrated circuit die that includes one or more devices, such as transistors or metal interconnects, that are formed using methods and apparatuses to control a line edge roughness and line-to-line spacing in deposition of self-aligned metal caps as described herein.

[0065] In various implementations, the computing device 500 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra

mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be any other electronic device that processes data.

[0066] In the foregoing specification, embodiments of the invention have been described with reference to specific exemplary embodiments thereof. It will be evident that various modifications may be made thereto without departing from the broader spirit and scope of embodiments of the invention as set forth in the following claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

CLAIMS

What is claimed is:

1. An integrated circuit structure, comprising:

a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen and carbon;

a conductive structure in the dielectric layer, the conductive structure comprising:

a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and

a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and

a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.

2. The integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.

3. The integrated circuit structure of claim 1, wherein second conductive material further comprises boron.
4. The integrated circuit structure of claim 3, wherein second conductive material further comprises phosphorous.
5. The integrated circuit structure of claim 3, wherein second conductive material further comprises tungsten.
6. The integrated circuit structure of claim 3, wherein second conductive material further comprises tungsten and phosphorous.
7. The integrated circuit structure of claim 1, wherein second conductive material further comprises phosphorous.
8. The integrated circuit structure of claim 7, wherein second conductive material further comprises tungsten.
9. A method of fabricating an integrated circuit structure, the method comprising:
 - forming a dielectric layer comprising silicon, oxygen and carbon;
 - forming a trench in the dielectric layer;
 - forming a barrier layer in the trench, the barrier layer comprising tantalum;

forming a first conductive material within the barrier layer, the first conductive material comprising copper;

recessing the first conductive material below a portion of an upper surface of the dielectric layer; and

forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer.

10. The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.

11. The method of claim 9, wherein the barrier layer further comprises nitrogen.

12. The method of claim 9, wherein second conductive material further comprises boron.

13. The method of claim 12, wherein second conductive material further comprises phosphorous.

14. The method of claim 12, wherein second conductive material further comprises tungsten.

15. The method of claim 12, wherein second conductive material further comprises tungsten and phosphorous.

16. The method of claim 9, wherein second conductive material further comprises phosphorous.

17. The method of claim 16, wherein second conductive material further comprises tungsten.

18. A computing device, comprising:

a board; and

a component coupled to the board, the component including an integrated circuit

structure, comprising:

a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen and carbon;

a conductive structure in the dielectric layer, the conductive structure comprising:

a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and

a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the

dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and
a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.

19. The computing device of claim 18, further comprising:

a memory coupled to the board.

20. The computing device of claim 18, further comprising:

a communication chip coupled to the board.

21. The computing device of claim 18, further comprising:

a camera coupled to the board.

22. The computing device of claim 18, further comprising:

a battery coupled to the board.

23. The computing device of claim 18, further comprising:

an antenna coupled to the board.

24. The computing device of claim 18, wherein the component is a packaged integrated circuit die.

25. The computing device of claim 18, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.

ABSTRACT

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemistry comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A capping layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the capping layer within the width of the conductive line.

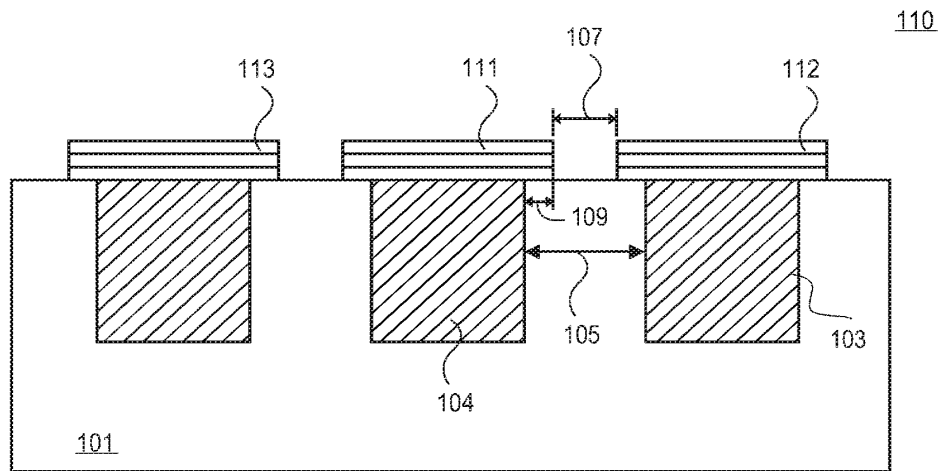


FIG. 1A
(PRIOR ART)

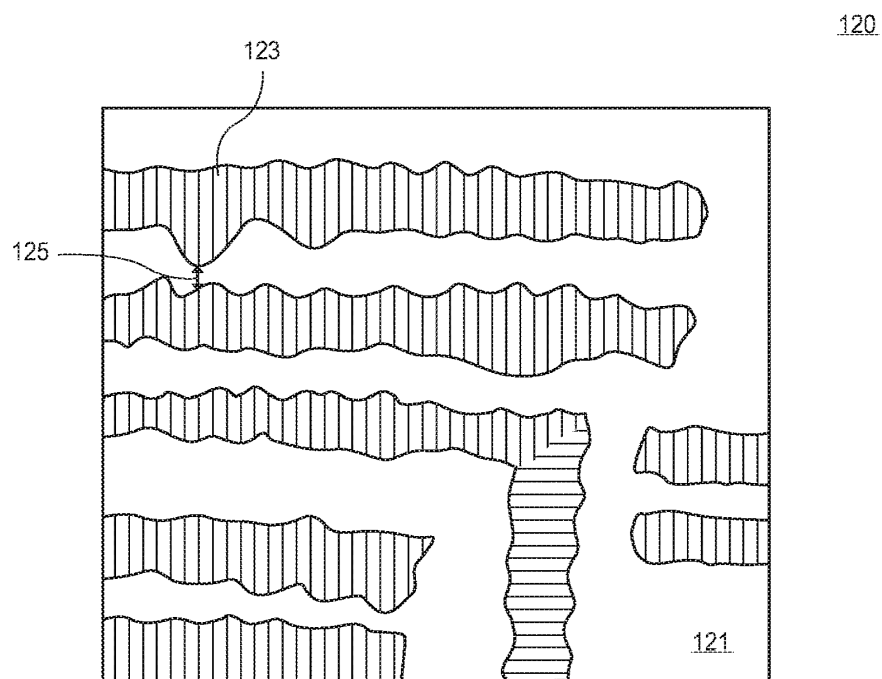


FIG. 1B
(PRIOR ART)

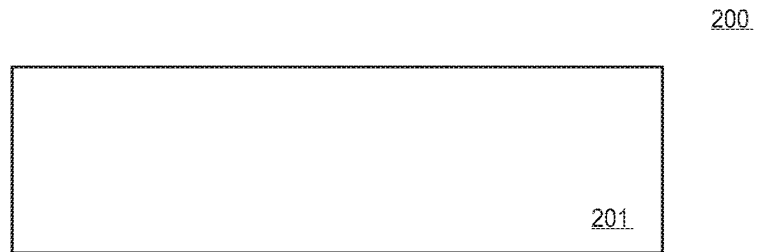


FIG. 2A

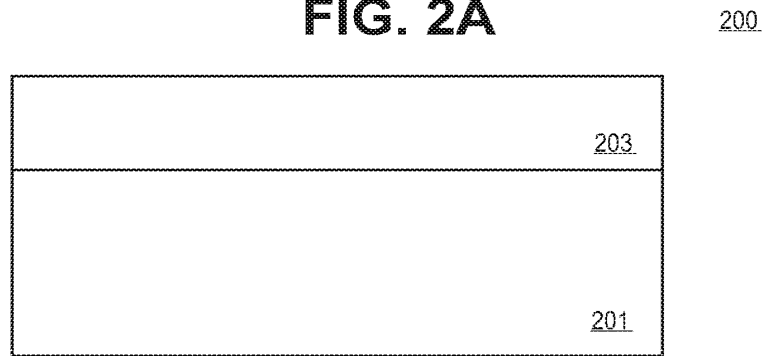


FIG. 2B

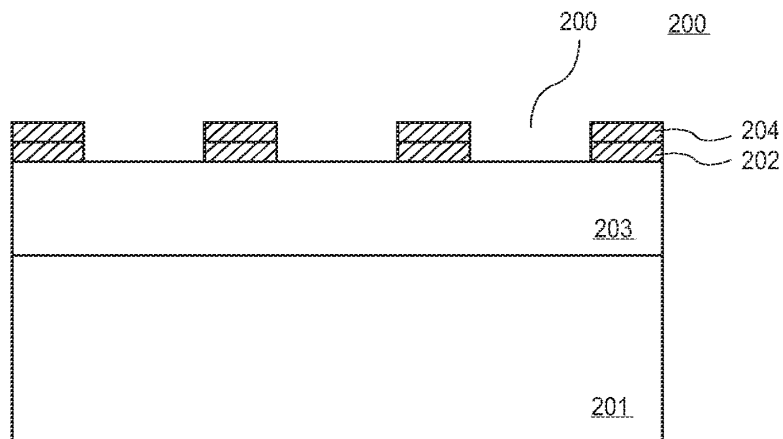


FIG. 2C

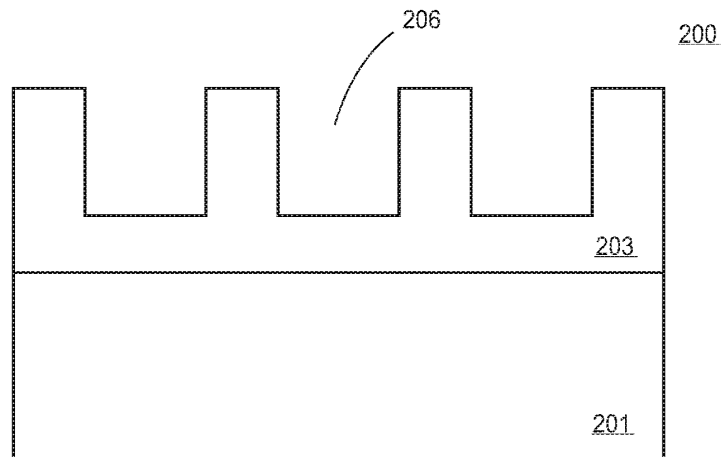


FIG. 2D

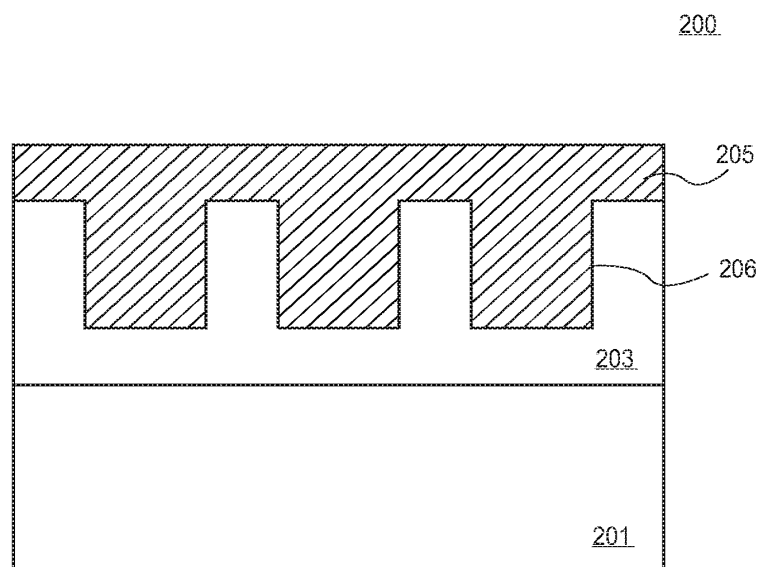


FIG. 2E

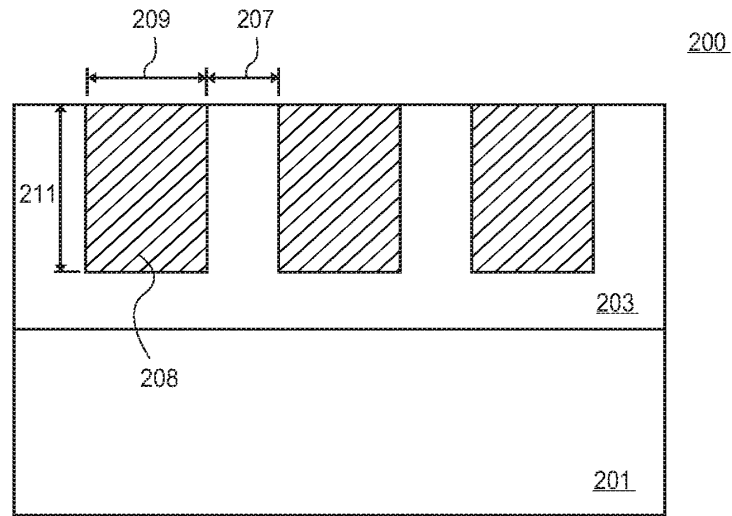


FIG. 2F

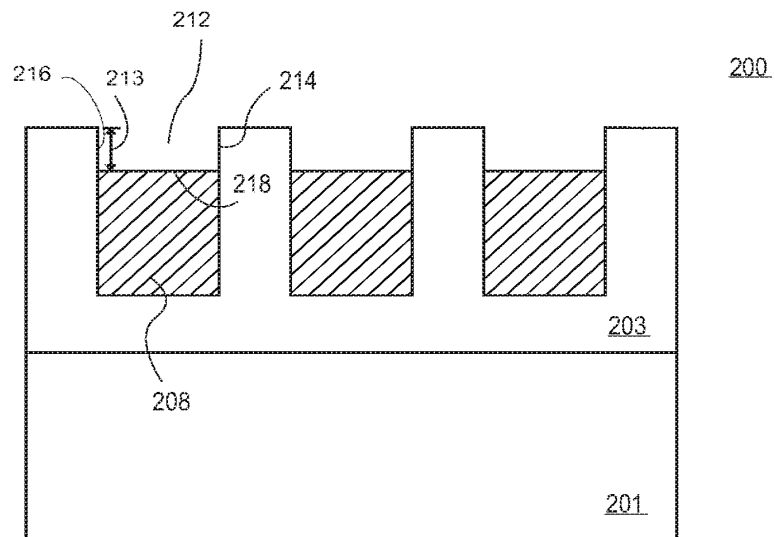


FIG. 2G

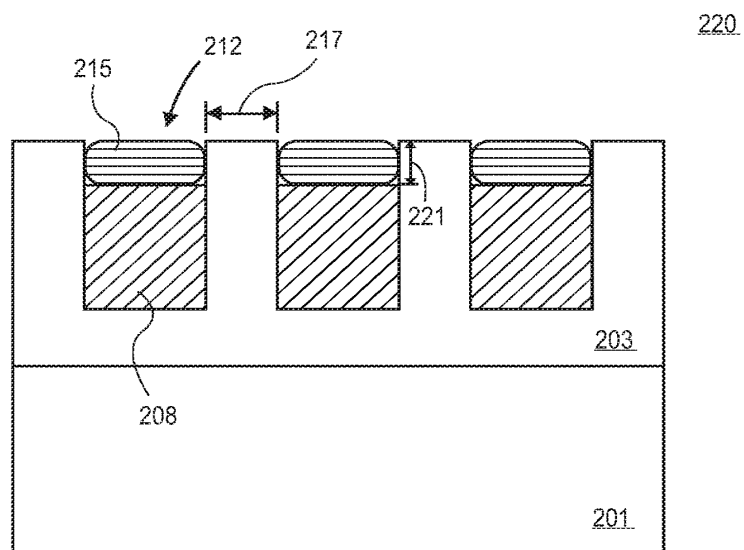
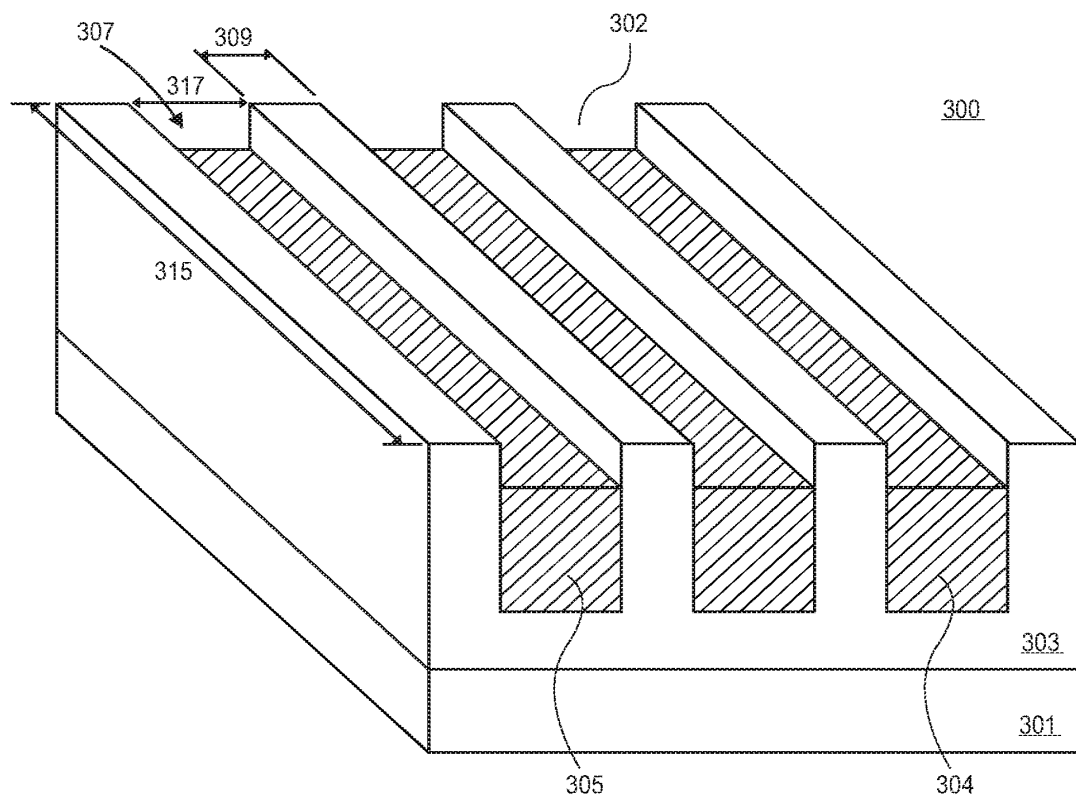


FIG. 2H

**FIG. 3A**

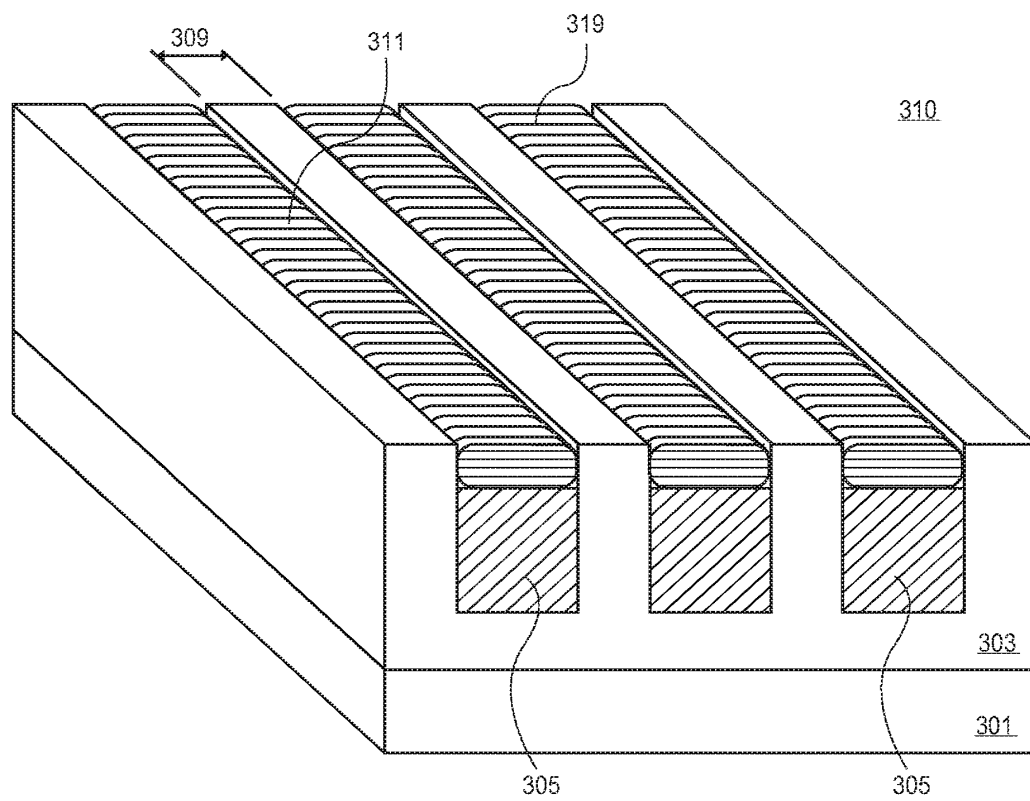


FIG. 3B

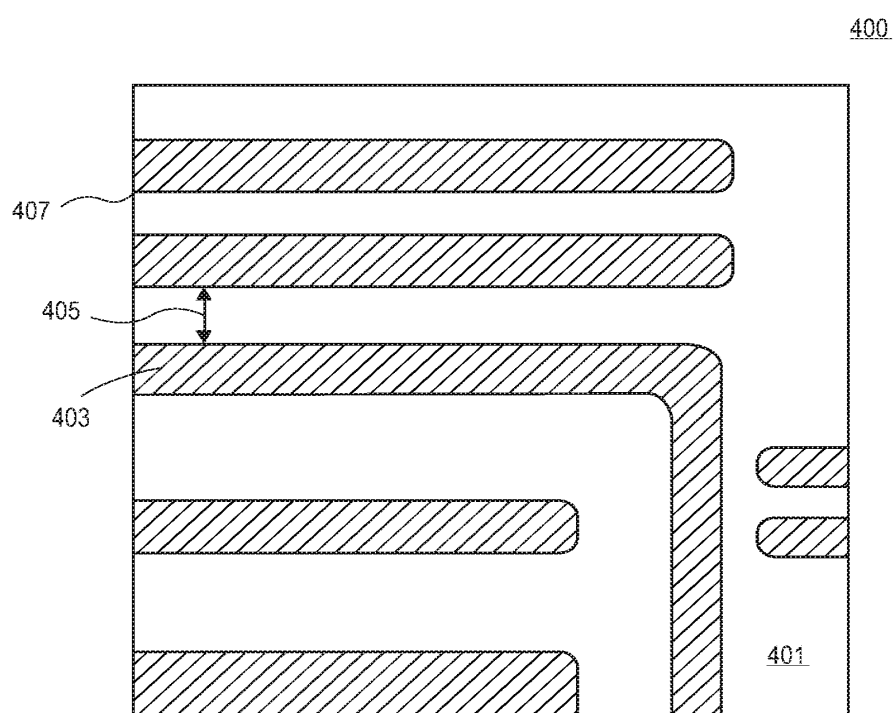
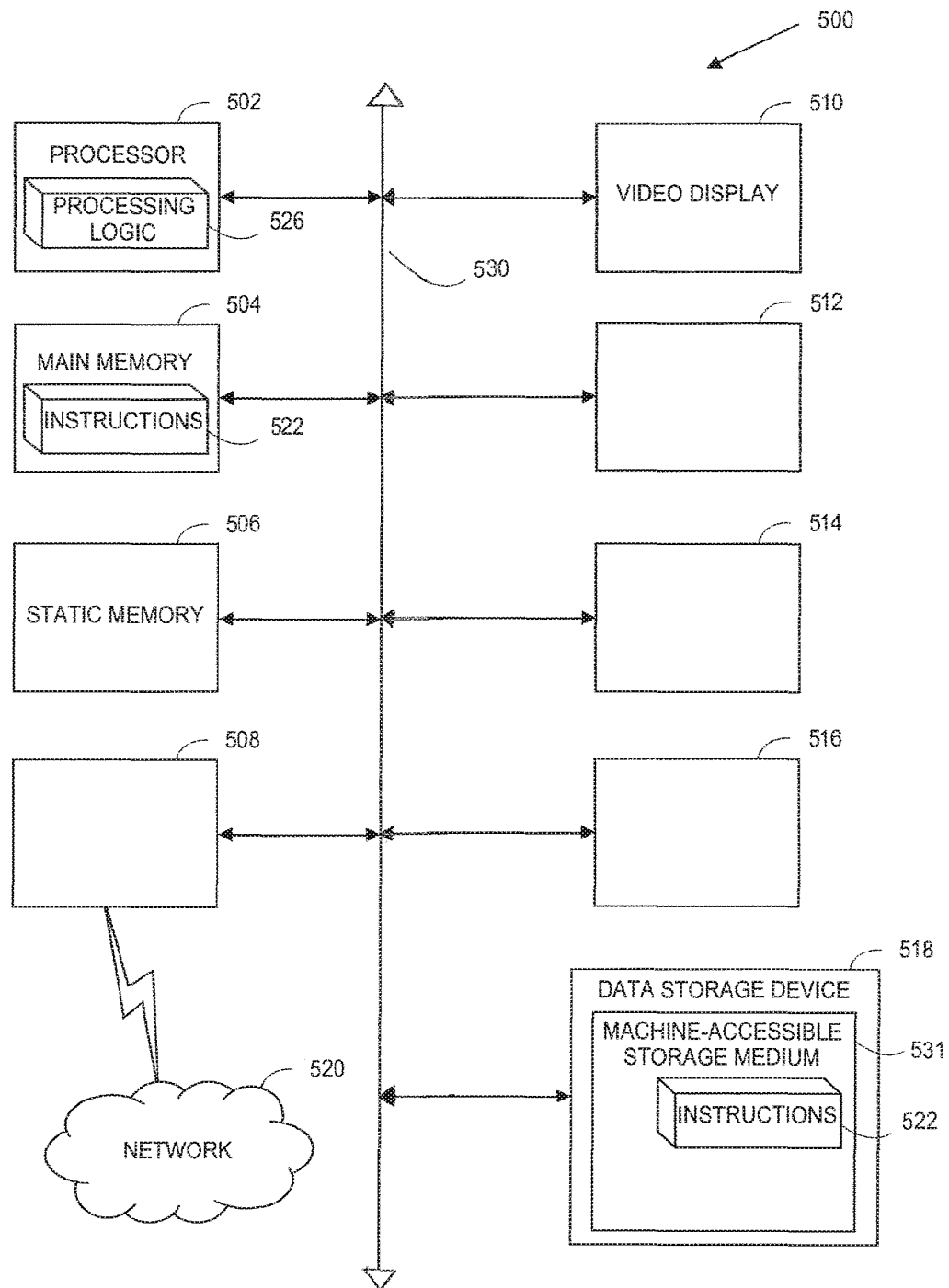
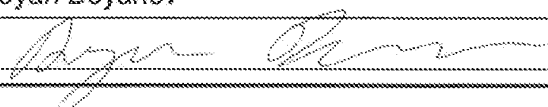


FIG. 4

**FIG. 5**

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>14/675,613</u> filed on <u>March 31, 2015</u> The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR	
Inventor: <u>Boyan Boyanov</u> Date (Optional): <u>7/13/15</u>	
Signature: 	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

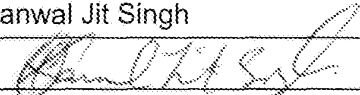
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>14/675,613</u> filed on <u>March 31, 2015</u>. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR	
Inventor: <u>Kanwal Jit Singh</u> Date (Optional): <u>July 13, 2015</u>	
Signature: <u></u>	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No. Not Yet Assigned

Filing Date Herewith

First Inventor Boyanov, et al.

Art Unit

Examiner Name

Attorney Docket No. P38794USDC-C1 111548

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted concurrently with the Non Provisional Application. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 CFR § 1.98(d)(1) copies of the references were provided in prior applications 15/477,506 filed April 3, 2017, 14/675,613 filed March 31, 2015, 13/991,899 filed June 5, 2013 which are relied on for priority.

It is respectfully requested that the examiner consider information which has been previously submitted to the Patent Office in the parent application and any prior related applications.

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of \$240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☐ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature /Michael A. Bernadicou/

Date (MM-DD-YYYY) 09-03-2019

Name/Print Michael A. Bernadicou

Registration Number 35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal /Sheri Villarreal/

Date 09-03-2019

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to assist or retain a benefit to the public which it is the (and by the USPTO to process) an application. Confidentiality is governed by 36 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing the burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.