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(54) Title

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

(57) Abstract

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemical comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A cover layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the cover layer within the width of the conductive line.

Designated representative figure

Brief description of
reference numerals:
301...Substrate
303... Dielectric layer
305... Conductive line
309... Interval
311, 319... Cover layer

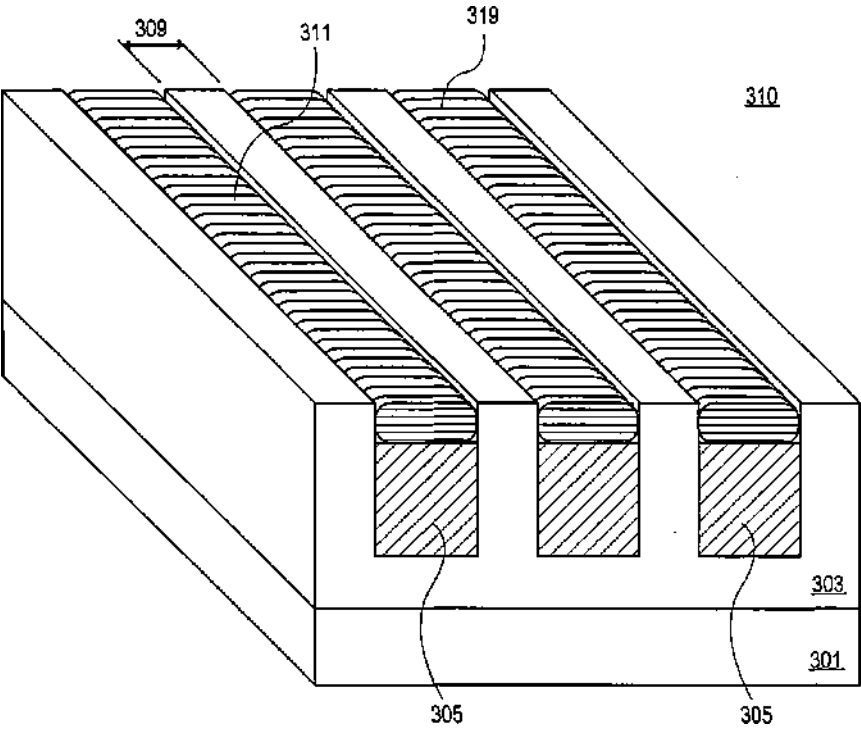


FIG. 3B

Abstract of Invention

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， 【Title of Invention】 (Chinese/ English)

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

【Chinese】

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemical comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A cover layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the cover layer within the width of the conductive line.

【English】

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemical comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A cover layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the cover layer within the width of the conductive line.

【Representative Figure】

【Designated Representative Figure】：FIG. 3B

【Brief description of the reference numerals of the representative figure】：

301 : Substrate

303 : Dielectric layer

305 : Conductive line

309 : Interval

311, 319 : Cover layer

【If this application includes chemical formulas, please disclose the chemical formula that best represents the characteristics of the invention】：None

SPECIFICATION

(Please do not change the format and sequence of this specification)

【Title of Invention】 (Chinese/English)

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

【Technical Field】

Embodiments of the present invention relate to the field of electronic device fabrication, and more particularly to the formation of interconnect structures.

【Background Art】

Since the feature size of electronic devices is reduced, the reliability of the interconnect becomes extremely important to the performance of an integrated circuit. In general, electromigration refers to material migration in a conductor due to ion movement caused by momentum transfer between conductive electrons and diffused metal atoms. This effect is especially important in applications that use high current densities (e.g., in microelectronic structures involving logic devices). Metal cladding techniques are often used to prevent electromigration.

FIG. 1A is a cross-sectional view of a typical interconnect structure having a metal electromigration cap. As shown in FIG. 1A, metal interconnect lines such as lines 103 and 104 formed on a dielectric substrate 101 are originally spaced apart by a line spacing 105. Electromigration caps such as caps 111-113 and the like can be grown on individual interconnects above a plane of the substrate using electroless plating. In general, the growth

of the electromigration caps on the interconnect lines is isotropic. The electromigration caps can be grown on the interconnect metal wire in vertical and lateral manners over the substrate. The lateral growth of the metal electromigration caps can produce an overhanging structure such as an outer edge projection 109 that projects beyond the width of the interconnecting substrate 101. As shown in FIG. 1A, the lateral growth of the metal caps reduces the line-to-line spacing from interval 105 to interval 107.

The size of the outer edge projection 109 is typically about 50% of the thickness of the caps. For example, if two adjacent metal caps have a thickness of about 10 nanometers ("nm"), the overall size of the outer edge projections can be about 2 x 5 nanometers. Thus, the line-to-line spacing can be reduced by, for example, one-half, and from about 20 nanometers to about 10 nanometers.

FIG. 1B is a top view of a typical interconnect structure having some metal electromigration caps grown in an electroless manner over a plane of a substrate 121 having interconnects such as interconnects 123, and the like. As shown in FIG. 1B, the lateral growth of the metal caps over the substrate increases the Line Edge Roughness (LER) and reduces the line-to-line spacing. As shown in FIG. 1B, the line-to-line spacing such as the line-to-line interval 125 or the like is uncontrolledly changed. The increased LER and reduced line-to-line spacing have a detrimental effect on the reliability of the interconnect structure and increase the risk of current shorting that may cause failure of an entire integrated circuit device.

【Summary】

At least one of the conductive lines in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The conductive line can be

etched to a predetermined depth using a chemical to form the channel, wherein the chemical comprises an inhibitor to provide uniformity of etching independent of crystallographic orientation. A cover layer for preventing electromigration is deposited on the recessed conductive line in the channel. The channel is configured to receive the cover layer within the width of the conductive line.

【Brief Description of Drawings】

The invention has been described by way of example and not limitation with reference to the accompanying drawings, and similar reference numerals represent similar elements in the accompanying drawings, in which

FIG. 1A shows a cross-sectional view of a typical interconnect structure with a metal electromigration cap.

FIG. 1B is a top view of a typical interconnect structure with a metal electromigration cap.

FIG. 2A shows a cross-sectional view of a substrate used to fabricate an interconnect structure in accordance with an embodiment of the present invention.

FIG. 2B is a view similar to FIG. 2A after forming a dielectric layer over the substrate in accordance with an embodiment of the present invention.

FIG. 2C is a view similar to FIG. 2B after depositing a photoresist layer over the dielectric layer and forming one or more openings in the dielectric layer in accordance with an embodiment of the present invention.

FIG. 2D is a view similar to FIG. 2C after one or more openings are formed in the dielectric layer in accordance with an embodiment of the present invention.

FIG. 2E is a view similar to FIG. 2D after depositing a conductive layer over the dielectric layer in accordance with an embodiment of the present invention.

FIG. 2F is a view similar to FIG. 2E after forming a patterned conductive line by removing portions other than the conductive layer and the openings in the base layer from the upper surface of the dielectric layer in accordance with an embodiment of the present invention.

FIG. 2G is a view similar to FIG. 2F after recessing a conductive line in a dielectric layer over a substrate in accordance with an embodiment of the present invention.

FIG. 2H is a diagram similar to FIG. 2H 2G after electromigration is prevented by selectively depositing the cover layers into the respective recessed conductive lines in the channels in accordance with an embodiment of the present invention. .

FIG. 3A is a three-dimensional diagram 300 of an interconnect structure after the conductive lines in a dielectric layer recessed into a substrate in accordance with an embodiment of the present invention.

FIG. 3B is a diagram 310 similar to FIG. 3A after deposition of a cover layer to respective channels formed by the recessed conductive lines in accordance with an embodiment of the present invention.

Fig. 4 is a top view of an interconnect structure 400 of a cover layer in a via formed by a recessed conductive line selectively deposited in a dielectric layer over a substrate in accordance with an embodiment of the present invention.

FIG. 5 is a block diagram showing an embodiment of a data processing system.

【Description of Embodiments】

In the following description, numerous specific details are set forth, such as particular materials or elements, in order to provide a thorough understanding of one or more

embodiments of the invention. However, it should be understood by those skilled in the art that the one or more embodiments of the invention may be practiced without the specific details. In other instances, well-known matters of semiconductor processes, techniques, materials, or equipment are not described in detail to avoid unnecessarily obscuring the description. Those of ordinary skill in the art will be able to carry out appropriate functions without undue experimentation.

While certain embodiments of the invention have been described and shown in the drawings, it should be understood that the embodiments are only examples of, rather than limitations to, the invention, and the invention is not limited to the illustrated and described particular structures and configurations, because some modifications can be made by those with the general knowledge of this technology.

References to "an embodiment," "another embodiment," or "an embodiment" in this specification are meant to mean that a particular feature, structure, or characteristic described in a manner in connection with the embodiment is included in at least one embodiment of the invention. Therefore, when the words "in an embodiment" or "for an embodiment" are used throughout the specification, the same embodiments are not necessarily referred to. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

Further, the viewpoints of the present invention illustrate fewer features than all features of a single embodiment disclosed. Therefore, the claims after the embodiments are hereby expressly incorporated in this embodiment, so that each claim independently corresponds to one respective embodiment of the present invention. Although the present invention will be described with reference to a few embodiments, those skilled in the art can understand that the invention is not limited to the embodiments described, but may be modified

and varied within the spirit and scope of the appended claims. This description is therefore to be considered as illustrative and not restrictive.

The present invention describes methods and apparatus for controlling line edge roughness (LER) and line-to-line spacing when depositing self-aligning metal caps. At least one conductive line is recessed to form a channel in a dielectric layer over a substrate. A cover layer for preventing electromigration is deposited on the recessed conductive line in the channel. The channel is self-aligned to the conductive line. The channel is configured to receive the cover layer within the width of the conductive line. That is, the interconnect is recessed and the cap growth is accommodated in a channel that self-aligns with the interconnect. As will be described in further detail below, the conductive line can be etched to a predetermined depth using a chemical to form the channel, wherein the chemical comprises an inhibitor providing uniform etching independent of crystallographic orientation. The methods and apparatus described herein can be used to control the increase in LER associated with selectively deposited electromigration caps such as electroless cobalt caps. That is, an electroless cap can be housed in a recess that self-aligns an interconnect, while preventing an increase in the LER and a decrease in the line-to-line spacing typically associated with the electromigration cap selectively deposited on the metal interconnect. When the increase in LER is eliminated and the line-to-line spacing is prevented from being reduced, the risk of failure can be reduced, and the manufacturing yield of a small-sized (e.g., nano-scale) electronic device can be improved. The electronic devices can be computer system architecture devices such as transistors, memories, logic devices, and the like, as well as any other integrated circuit and microelectronic device.

FIG. 2A shows a cross-sectional view 200 of a substrate used to fabricate an interconnect structure in accordance with an embodiment of the present invention. In one

embodiment, substrate 201 comprises monocrystalline silicon. In one embodiment, substrate 201 includes a Silicon On Insulator (SOI). For alternative embodiments, the substrate may comprise a

compound semiconductor such as indium phosphide, gallium arsenide, gallium nitride, silicon-germanium, and silicon carbide. In another embodiment, substrate 201 can include, for example, glass and quartz. Substrate 201 may comprise one or more metallization layers of integrated circuits having active and passive devices such as transistors, switches, optoelectronic devices, capacitors, resistors, interconnects (not shown), and the like. The one or more metallization layers of the integrated circuits of substrate 201 may be isolated from adjacent metallization layers by a dielectric material (not shown) such as an interlayer dielectric. Vias (not shown) may electrically interconnect the adjacent metallization layers.

FIG. 2B is a view similar to FIG. 2A after forming a dielectric layer 203 over the substrate 201 in accordance with an embodiment of the present invention. In one embodiment, the dielectric layer 203 is an interlayer dielectric (ILD). In one embodiment, dielectric layer 203 is a low-k dielectric such as silicon dioxide, silicon oxide, carbon doped oxides (CDO), or any combination of the above. In one embodiment, the dielectric layer 203 comprises a nitride, an oxide, a polymer, a phosphosilicate glass, a fluorosilicate glass (SiOF), an organosilicate glass (SiOCH), or any combination of the above. In an embodiment, the dielectric layer 203 comprises a spin-on low-k dielectric material. In an embodiment, the dielectric layer 203 is silicon oxide.

In another embodiment, the dielectric layer 203 is silicon nitride. Dielectric layer 203 can be deposited using any suitable deposition technique. In one embodiment, the deposition of the dielectric layer 203 can be performed using blanket deposition techniques such as chemical vapor deposition (CVD), sputtering, spin coating, or another thin film deposition technique. In one embodiment, the dielectric layer 203 is deposited to a thickness ranging from about 50 nanometers to 2 microns.

FIG. 2C is a view similar to FIG. 2B after depositing a photoresist layer 204 over dielectric layer 203 and forming one or more openings in dielectric layer 203 in accordance with an embodiment of the present invention. In one embodiment, as shown in FIG. 2C, a photoresist layer 204 is deposited over a hard mask layer 202 formed over the dielectric layer 203. In another embodiment, the photoresist layer 204 is deposited directly onto the dielectric layer 203. As shown in FIG. 2C, photoresist layer 204 and hard mask layer 202 are patterned and etched to form openings such as openings 220. Patterning and etching of the photoresist and hard masks is well known to those of ordinary skill in the art of microelectronic device fabrication. Pattern generation and etching of the photoresist can be performed using one of the techniques well known to those of ordinary skill in the art of microelectronic device fabrication. The technique can include: masking the photoresist layer; exposing the masked layer; and then developing portions that are not exposed to remove the exposed portions of the photoresist layer to form an opening window in the photoresist layer. In one embodiment, the process of exposure and photoresist layer removal can be performed in a plasma reactor. The opening in the hard mask layer 202 may be etched using dry etching, wet etching, or any combination of the above techniques, such as reactive ion etching (RIE), to expose a portion of the dielectric layer 203.

FIG. 2D is a diagram similar to FIG. 2C after one or more openings, such as openings 206, are formed in dielectric layer 203 in accordance with an embodiment of the present invention. In an embodiment, such openings, such as openings 206, are implemented via openings in dielectric layer 203, such as openings 220. In another embodiment, the openings are formed by etching the dielectric layer through the openings in the patterned photoresist 204 deposited directly onto the dielectric layer 203. In an embodiment, an opening such as a trench or the like in the dielectric layer 203 is formed using anisotropic dry etching such as laser etching. In another embodiment, the openings in the dielectric layer 203 are formed using dry etching, wet etching, or a combination of techniques known to those of ordinary skill in the art of microelectronic device fabrication. In one embodiment, the openings in the dielectric layer 203 have a width ranging from about 0.005 micrometers (μm) to 5 μm , and a depth ranging from about 0.005 μm to 10 μm . In one embodiment, the size of the conductive lines formed later in the ILD 203 during the process determines the size of the openings.

After the openings such as openings 206 are formed, the photoresist and the hard mask are removed. Removal of the photoresist and hard mask from the dielectric layer 203 is well known to those of ordinary skill in the art of microelectronic device fabrication. In one embodiment, the photoresist and hard mask can be removed using a chemical technique, a mechanical technique, or both.

FIG. 2E is a view similar to FIG. 2D after deposition of a conductive layer 205 over dielectric layer 203 in accordance with an embodiment of the present invention. As shown in FIG. 2E, the formation of conductive layer 205 involves filling one or more openings in dielectric layer 203 with a conductive material to form one or more conductive lines. In one embodiment, an inner sidewall and a base layer (not shown) at the bottom for covering the openings are first deposited on the dielectric layer 203, and then a conductive layer 205 is

deposited on the base layer. In one embodiment, the base layer comprises a conductive seed layer deposited on a conductive barrier layer (not shown). The seed layer may comprise copper, and the conductive barrier layer may comprise aluminum, titanium, tantalum, tantalum nitride, and the like. The conductive barrier layer can be used to prevent the conductive material from diffusing from the seed layer such as copper to the ILD 203. Additionally, the conductive barrier layer can be used to provide adhesion of the seed layer (e.g., copper). In one embodiment, to form the base layer, the conductive barrier layer is deposited onto the dielectric layer 203 to cover the sidewalls and bottom of the openings, and then the seed layer is deposited on the conductive barrier layer. In another embodiment, the conductive base layer comprises the seed layer deposited directly onto the dielectric layer 203 to cover the sidewalls and bottom of the openings. Each of the conductive barrier layer and the seed layer can be deposited using any thin film deposition technique known to those of ordinary skill in the art of semiconductor fabrication (e.g., thin film deposition techniques such as sputtering, blanket deposition, etc.). In one embodiment, each of the conductive barrier layer and the seed layer has a thickness ranging from about 1 to 100 nanometers. In an embodiment, the barrier layer may be a thin dielectric that is etched to establish conductivity to the underlying metal layer. In an embodiment, the barrier layer can be omitted altogether, and a "self-forming" barrier can be made using appropriate doping of the copper wire.

Conductive layer 205 fills the openings, such as openings 206, and covers portions of the base layer (not shown) that are outside of the openings on top of the dielectric layer 203. In one embodiment, a conductive layer 205, such as copper, is deposited onto the seed layer of the copper base layer by an electroplating process. In one embodiment, the conductive layer

205 is deposited into the openings using a damascene process known to those of ordinary skill in the art of microelectronic device fabrication. In one embodiment, a conductive layer 205 is deposited onto the seed layer using one of the selective deposition techniques known to those of ordinary skill in the art of semiconductor fabrication, such as electroplating, electroless plating, and the like. In one embodiment, the choice of material for the conductive layer 205 determines the choice of material for the seed layer. For example, if the material of the conductive layer 205 contains copper, the material of the seed layer also contains copper. In an embodiment, the conductive layer 205 includes, for example, copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), vanadium (V), molybdenum (Mo), palladium (Pd), gold (Au), silver (Ag), platinum (Pt), or any combination of the above.

FIG. 2F is a view similar to FIG. 2E after forming a patterned conductive line, such as conductive line 208, by removing portions other than the conductive layer 205 and the openings in the base layer from the upper surface of the dielectric layer 203 in accordance with an embodiment of the present invention. Chemical means (for example, using an etching method), mechanical means (for example, a grinding method), or a combination of such techniques (for example, using a chemical-mechanical polishing (CMP) conventionally known to those skilled in the art of microelectronic device manufacturing) can be used to remove portions of the conductive layer 205. In one embodiment, one or more patterned conductive lines are formed in dielectric layer 203 using the methods previously described. In another embodiment, patterning and etching are performed on the conductive layers deposited on the upper surface of the dielectric layer 203 to form the conductive lines. Patterning and etching of the conductive

layer deposited on the upper surface of dielectric layer 203 is well known to those of ordinary skill in the art of microelectronic device fabrication. In one embodiment, the thickness of the conductive line, such as thickness 211, is in the range of approximately 0.015 microns to 1 micron. In one embodiment, the width of the conductive line, such as width 209, is in the range of from about 5 nanometers to about 500 nanometers. In one embodiment, the spacing between the electrically conductive lines, such as spacing 207, is from about 5 nanometers to about 500 nanometers. In one embodiment, the spacing between the electrically conductive lines is from about 2 nanometers to about 100 nanometers.

FIG. 2G is a diagram similar to FIG. 2F after recessing a conductive line such as conductive line 208 in a dielectric layer over a substrate in accordance with an embodiment of the present invention. As shown in FIG. 2G, a channel such as the channel 212 is formed in the dielectric layer 203. As shown in Fig. 2G, the vias such as vias 212 have sidewalls such as sidewalls 214 and 216 formed by the dielectric layer 203, and bottoms formed by respective conductive lines such as bottom 218 formed by conductive lines 208.

In an embodiment, the channel has a depth such as a depth 213 from about 5 nanometers to about 50 nanometers. In one embodiment, the depth of the channel is from about 2 nanometers to about 20 nanometers. In one embodiment, the channel has a depth from about 10% to about 50% of the thickness of the conductive line, such as thickness 211 shown in FIG. 2F. In an embodiment, as will be described in further detail below, the conductive lines are recessed to a depth that is determined according to the thickness of the cover layer.

FIG. 3A is a three-dimensional diagram 300 of an interconnection structure after a conductive line such as a conductive line 305 and a conductive line 304 in a dielectric layer 303 recessed over a substrate 301 in accordance with an embodiment of the present invention.. Substrate 301, dielectric layer 303, and conductive lines 305 and 304 can be any of respective substrates, dielectric layers, and conductive lines such as those previously described. As shown in FIG. 3A, the conductive lines are recessed, and a channel such as a channel 302 and a channel 307 is formed in the dielectric layer 303 above the substrate 301. As shown in FIG. 3A, the channels self-align with the respective conductive lines. For example, channel 307 self-aligns with conductive line 305, and channel 302 self-aligns with conductive line 304. As shown in FIG. 3A, the length of the channel, such as length 315, is along the length of the conductive line, and the length of the channel, such as width 317, is along the width of the conductive line. In an embodiment, the length of the channel is substantially greater than the width of the channel. In one embodiment, the width of the channel is less than 100 nanometers, and the length of the channel is at least 500 nanometers. In one embodiment, the width of the channel is from about 5 nanometers to about 500 nanometers, and the length of the channel is from about a few hundred nanometers to about several hundred micrometers. As shown in FIG. 3A, the conductive lines such as the conductive lines 305 and 304 are separated by a distance such as the interval 309. In one embodiment, the spacing between the conductive lines, such as the conductive lines 305 and 304, is from about 5 nanometers to about 500 nanometers. In one embodiment, the spacing between the conductive lines, such as the conductive lines 305 and 304, is from about 2 nanometers to about 100 nanometers.

In one embodiment, recessing conductive lines such as lines 208, lines 304, and 305 involves uniformly wet etching the conductive lines using a chemical comprising an etchant,

oxidant, an inhibitor, and a solvent in a manner that is independent of crystal orientation. That is, when an inhibitor and a solvent are added to the etchant, a passivation layer (not shown) may be formed on the conductive material during etching, and the conductive material is uniformly etched in a manner independent of crystal orientation. The wet etching chemical comprising an etchant, an oxidant, an inhibitor, and a solvent can control the etch depth of the conductive line, and thus can only recess a portion of the conductive line (for example, 5% to 50%).

In one embodiment, the chemical used to wet etch the conductive lines to provide a channel having no pattern dependency and crystal orientation preference comprises an etchant having a mass of from about 1% to about 40%, an oxidant with a mass of from about 1% to about 10%, an inhibitor with a mass of from about 0.1% to about 1%, and an organic solvent with a mass of from about 1% to about 60%. In one embodiment, the chemical used to wet etch the conductive lines comprises an etchant having a mass from about 0.1% to about 70% (depending on the etching rate of the etchant), and an oxidant with a mass of from about 0.1% to about 10% (depending on the strength of the oxidant), an inhibitor with a mass of from about 50 parts per million (50 ppm) to about 1%, and a solvent with a mass of from about 1% to about 60%.

In one embodiment, the chemical used to etch the conductive lines may include an etchant such as glycine, ethylenediaminetetraacetic acid, alpha-amino acid, polycarboxylic acid, or any combination of the above; an oxide such as peroxide, ozone, permanganate,

chromate, perborate, hypohalite, or any combination of the above; an inhibitor such as azole, amine, amino acid, phosphate, phosphonate, or any combination of the above; and a solvent. The solvent may be an aqueous system (preferably) such as water or an organic solvent. Examples of the organic solvent are organic solvents of propylene carbonate, sulfolane, glycol ether, and methylene chloride.

For example, with respect to an etchant in a chemical used to etch copper conductive lines, the copper metal is typically in a zero oxidation state. In order to etch copper, it is necessary to oxidize copper to a $0+n$ oxidation state, where n can be any of 1, 2, 3, or 4. The first oxidation state and the second oxidation state are generally the more common oxidation states of copper. For any molecule that is used as an etchant, the molecule must be capable of binding to copper in any of the oxidation states 1, 2, 3, or 4. This binding is usually carried out using a Group 15 (nitrogen), Group 16 (oxygen), or Group 17 (halogen) atom in one molecule. In one embodiment, the etchant used to etch the copper conductive lines is an organic etchant such as any of glycine, ethylenediaminetetraacetic acid, alpha-amino acids, polycarboxylic acids (e.g., citric acid as a tricarboxylic acid), oxalic acid, and malonic acid.

For example, an oxidant in the chemical used to etch copper conductive lines is used to change the copper oxidation state from insoluble copper metal to soluble copper ions. The

oxidant can be selected from any oxidant such as any peroxide (e.g., hydrogen peroxide), ozone, permanganate, chromate, perborate, and hypohalite.

For example, in order to etch the copper constituting the current carrying line in a uniform and without crystal orientation, it is important to add an inhibitor to the chemical. The role of the inhibitor is to form a passivation layer (a polymeric compound formed from the molecules of the inhibitor is used to bind the copper in a specific and periodic manner). The formation of the passivation layer during controlled etching of copper is extremely important to ensure uniformity of etching and to prevent etch attack (e.g., formation of voids) along the crystalline boundary (e.g., grain boundary). For example, any inhibitor that does not decompose in the selected oxidant and etchant can be used in the chemical for etching the copper conductive line. The class of inhibitors is known to those of ordinary skill in the art of fabrication of sub-devices. For example, any organic inhibitor including azole, amine, amino acid, phosphate, and phosphonate is used in the chemical for etching the copper conductive wire.

In another embodiment, the copper conductive lines are recessed by means of wet etching using a chemical comprising citric acid and a peroxide therein. However, chemicals containing citric acid and peroxides often have high etching rates that can be difficult to control. In addition, the etching rate of the chemical comprising citric acid and peroxide depends on the crystallographic orientation that may result in a rough etched surface. When a corrosion inhibitor such as benzothiazole (BTA) is added to the chemical, dilution of the citric acid and the peroxide in the organic solvent can greatly slow down the etching rate and eliminate the crystalline nature of the etching, for example, eliminate etching holes in the copper along the grain boundaries to produce a smooth surface.

In one embodiment, the conductive lines are recessed by means of wet etching that includes spraying or pouring the etch chemical onto the conductive lines. In one embodiment, the conductive lines are recessed by a wet etching process in which the conductive lines are immersed in the etch chemical solution. In one embodiment, the wet etching is performed at a temperature of from about 15 degrees Celsius to about 50 degrees Celsius for a predetermined time to recess the conductive lines. In at least some embodiments, the conductive lines are recessed by dry etching, such as plasma etching.

FIG. 2H is a diagram similar to FIG. 2G after electromigration is prevented by selectively depositing the cover layers into the respective recessed conductive lines in the channels in accordance with an embodiment of the present invention. The conductive lines etched using the chemical described above have a smooth and uniform upper surface to which the cover layer can be adhered. As shown in FIG. 2H, a cover layer 215 is deposited onto the recessed conductive lines 208 in the channel 212. In an embodiment, a channel, such as channel 212, is configured to accommodate a cover layer within a width of the cover layer, such as width 209 shown in FIG. 2F. That is, the recessed conductive lines create channels that accommodate the growth of the cover layer within the channels, thereby reducing line-to-line spacing decrease and LER increase. As shown in FIG. 2H, the cover layer 215 is disposed over the conductive lines 208 in the sidewalls of the channel 212. In one embodiment, the cover layer is deposited onto the recessed conductive line by using electroless plating (e.g., plating), chemical vapor deposition (CVD), physical vapor deposition (PVD), or any other selective deposition technique known to those skilled in the art of electronic device fabrication techniques. In one embodiment, the conductive line such as the line 208 comprises a first metal, and the cover layer comprises a second metal different from the first metal, while the second

metal is used to prevent electromigration from the first metal of the conductive line. In one embodiment, the metal used for the cover layer is heavier than the metal used for the conductive line to prevent electromigration.

For example, the conductive line can be made of any metal including copper or aluminum. In one embodiment, the cover layer such as the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above. In another embodiment, the cover layer such as the cover layer 215 is made of nickel (Ni), such as electroless nickel alloys like nickel borophosphide (NiBP), nickel tungsten borophosphide (NiWBP), nickel tungsten phosphide (NiWP), nickel tungsten boride (NiWB), nickel tungsten phosphide (NiWP), or any combination of the above. In another embodiment, the cover layer such as the cover layer 215 is made of a platinum (Pt) group metal such as platinum (Pt), palladium (Pd), ruthenium (Ru), iridium (Ir), rhodium (Rh), etc. in the form of a pure element or alloys. Typical alloying elements for platinum (Pt) group metals are tungsten (W), boron (B), and phosphorus (P). In still another embodiment, the cover layer such as the cover layer 215 is made of a refractory metal such as tantalum (Ta), tungsten (W), molybdenum (Mo), or a combination thereof.

In one embodiment, a cobalt cover layer is deposited into a channel on the recessed copper conductive layer. In one embodiment, a nickel cover layer is deposited into a channel on the recessed copper conductive layer. In one embodiment, a refractory metal cover layer is deposited into a channel on the recessed copper conductive layer.

In one embodiment, the cover layer containing a platinum (Pt) group, cobalt, nickel, or a combination of the foregoing is deposited onto the conductive layers such as copper, aluminum, and the like using any deposition technique of electroless deposition and vapor deposition such as chemical vapor deposition (CVD). In one embodiment, in one embodiment, such cover layers including refractory metals are deposited onto the conductive layers such as copper, aluminum, etc., using any of the CVD and PVD techniques known to those of ordinary skill in the art of electronic device fabrication. In one embodiment, the thickness of the cover layer, such as thickness 221, is from about 2 nanometers to about 50 nanometers. In an embodiment, the cover layer has a thickness sufficient to prevent electromigration from the underlying conductive layer. In an embodiment, the cover layer has a thickness no greater than the depth of the channel in which the cover layer is deposited.

FIG. 3B is a diagram 310 similar to FIG. 3A after deposition of a cover layer to respective channels formed by the recessed conductive lines in accordance with an embodiment of the present invention. As shown in FIG. 3B, a cover layer such as cover layers 311 and 319 is selectively deposited to respective channels such as channel 302 and channel 307 in the manner previously described. As shown in FIG. 3A, the cover layers are housed in their respective channels. As shown in FIG. 3B, the interval 309 isolates the cover layer 319 from the cover layer 311. In one embodiment, the spacing between the conductive lines 305 and 304 and the spacing between the cover layers 319 and 311 are the same.

FIG. 4 is a top view of an interconnect structure 400 of a cover layer in a channel formed by recessed conductive lines in a dielectric layer 401 selectively deposited onto a substrate in accordance with an embodiment of the present invention. As shown in FIG. 4, the LERs of the interconnect lines, such as interconnect 403, are substantially reduced, the edges

of the interconnect lines are smooth, and line-to-line spacing such as line-to-line spacing 405 is increased and kept between the lines. In one embodiment, the line-to-line spacing is increased by 2 times of the cap thickness. This can result in a significant reduction in electric field and dielectric breakdown time, especially for future technology nodes with 20 nanometer lines and 20 nanometer spacing. The minimum cap thickness that is currently known to be feasible is 5 nm. This means that under the traditional method, the line-to-line spacing drawn on the mask will be 10 nm instead of 20 nm. In addition, the size of the outer edge projection is currently often about 50% of the cap thickness. For a typical cap thickness of 5-10 nm, the LER can be reduced by 3-5 nm using the method described above, regardless of the line width. For future 20 nm technology nodes, a 3-5 nm reduction in LER can result in a 15-20% increase in the line-to-line spacing of the interconnect structure.

FIG. 5 illustrates a block diagram of an embodiment of a data processing system 500 having a memory such as a transistor, memory 504 and memory 518, processing logic devices such as processing logic device 526, and any other integrated circuit and microelectronic device constructed using the methods described above. As shown in FIG. 5, the data processing system 500 includes a processor 502 having processing logic 526. In at least some embodiments, processing logic 526 includes: at least one conductive line in a dielectric layer over a substrate; a channel in the dielectric layer and above the conductive line; and a cover layer on the at least one conductive line in the channel, the cover layer preventing electromigration in the manner previously described. In at least some embodiments, each of the memories 504 and 518

includes: at least one conductive line in a dielectric layer over a substrate; a channel in the dielectric layer and above the conductive line; and a cover layer on the at least one conductive line in the channel, the cover layer preventing electromigration in a manner previously described.

In an alternative embodiment, the data processing system can be connected (e.g., wired to) a local area network (LAN), an intranet, or an inter-enterprise network (Extranet), or other machines on the Internet. The data processing system can operate as a server or a client machine in a master-slave network environment, or operate as a machine of the same class in a peer-to-peer network (or distributed network). The data processing system may be a personal computer (PC), a tablet personal computer, a set-top box (STB), a personal digital assistant (PDA), a mobile phone, a network device, a server, a network router, a switch or bridge, or any machine capable of executing a set of instructions (sequential or in other forms) that can specify actions to be accepted by the data processing system. Moreover, although only a single data processing system is shown, the term "data processing system" will also be understood to include data processing systems for performing, individually or in combination, any set of one group (or multiple groups) of instructions for performing any one or more of the methods described in the present invention. A.

The exemplary data processing system 500 includes a processor 502, a main memory 504 (e.g., Read Only Memory (ROM), flash memory, and Dynamic Random Access Memory

(DRAM) such as Synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM)), a static memory 506 (e.g., flash memory and static random access memory (SRAM)), and an auxiliary memory 518 (for example, a data storage device) that communicate with each other via a bus 530.

The processor 502 represents one or more general purpose processing devices such as a microprocessor or central processing unit. More specifically, the processor 502 can be a Complex Instruction Set Computing (CISC) microprocessor, a Reduced Instruction Set Computing (RISC) microprocessor, a Long Instruction Word (VLIW) microprocessor, a processor that implements other instruction sets, or a processor that implements a combination of some instruction sets. The processor 502 may also be an Application Specific Integrated Circuit (ASIC), a Field-Programmable Gate Array (FPGA), a Digital Signal Processor (DSP), or one or more special purpose processing devices such as a network processor. The processor 502 is configured to process logic 526 to perform the operations described herein.

The computer system 500 can further include a network interface device 508. The computer system 500 can also include a video display unit 510 (for example, a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT), a digital input device 512 (for example, a keyboard), a cursor control device 514 (for example, a mouse), and a signal generating device 516 (for example, a speaker).

The auxiliary memory 518 can include a machine-accessible storage medium (or, in particular, a computer-readable storage medium) 531, the machine-accessible medium storing one or more sets of instructions or functions (e.g., software 522) for implementing any one or more of the methods or functions in the methods or functions described herein. During execution of software 522 by computer system 500, software 522 may be stored entirely or at least partially within main memory 504 and/or processor 502, where main memory 504 and processor 502 also constitute machine readable storage media. Software 522 can be further transmitted or received via network interface device 508 and a network 520.

Although the machine-accessible storage medium 531 is illustrated as a single medium in one embodiment, the term "machine-readable storage medium" shall be construed to include a single medium or multiple media (e.g., centralized or decentralized repositories and/or associated caches and servers) for storing one or more sets of instructions. The term "machine readable storage medium" shall also be construed to include any medium capable of storing or encoding a set of instructions for execution by a machine and causing the machine to perform any one or more of the methods of the present invention. The term "machine readable storage

medium" is thus to be understood to include, but is not limited to, solid state memory, optical media, and magnetic media.

In an alternative embodiment, FIG. 5 illustrates a computing device 500. The computing device 500 is provided with a board 530. The board can include some components including, but not limited to, a processor 502 and at least one communication chip 508. Processor 502 is physically and electrically coupled to the board 530. In some embodiments, the at least one communication chip is also physically and electrically coupled to the board 530. In a further embodiment, the communication chip 508 is integrated within the processor 502.

Computing device 500 can include other components that may or may not be physically and electrically coupled to board 530 depending on its application. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, graphics processors, digital signal processors, cryptographic processors, chipsets, antennas, displays, touch screen controllers, batteries, audio codec, video codec, power amplifiers, Global Positioning System (GPS) devices, compasses, accelerometers, gyroscopes, speakers, cameras, and a large number of storage devices (such as hard disk drives, solid state drives, CD players, and Digital Versatile Disk (DVD) players).

The communication chip 508 is capable of performing wireless communication to transfer data into and out of the computing device 500. The term "wireless" and derivatives thereof can be used to describe items of circuitry, devices, systems, methods, techniques, or

communication channels that can utilize modulated electromagnetic radiation through a non-solid medium. The term does not mean that relevant devices do not contain any wires, but such devices may not include any wires in some embodiments. The communication chip 508 can implement any wireless standard or protocol including, but not limited to, Wi-Fi (IEEE 802.11 series), WiMAX (IEEE 802.16 series), IEEE 802.20, Long Term Evolution (LTE), evolution data optimization (Ev-DO), Enhanced High Speed Packet Access Network (HSPA+), Enhanced High Speed Downlink Packet Access (HSDPA+), Enhanced High Speed Uplink Packet Access (HSUPA+), Enhanced Data GSM Environment (EDGE), Global Operations Communication System (GSM), General Packet Radio Service (GPRS), Code-Division Multiple Access (CDMA), Time Division Multiple Access (TDMA), Digital Enhanced Cordless Telecommunications (DECT), Bluetooth, derivative standards or protocols of the above, and wireless standards or protocols of any other wireless protocols known as third generation (3G), fourth generation (4G), fifth generation (5G), and future generations. Computing device 500 can include a plurality of communication chips 508. For example, a first communication chip 508 can be dedicated to short-range wireless communication such as Wi-Fi and Bluetooth, and a second communication chip 1006 can be dedicated to long-distance wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and other wireless communications.

Processor 502 of computing device 500 includes an integrated circuit die packaged within processor 502. In some embodiments of the invention, the integrated circuit die of the processor comprises one or more devices, such as a transistor or a metal interconnect, wherein the one or more devices are formed by using the method and apparatus that control line edge

roughness and line-to-line spacing during deposition of self-aligning metal caps in the manner in accordance with the invention. The term "processor" may refer to any device used to process electronic data from a register and/or memory and convert the electronic data into other electronic data that can be stored in a register and/or memory or part of the device.

The communication chip 508 also includes an integrated circuit die that is packaged within the communication chip 508. In accordance with another embodiment of the present invention, the integrated circuit die of the communication chip includes one or more devices such as a transistor or a metal interconnect, wherein the one or more devices are formed by using the method and apparatus that control line edge roughness and line-to-line spacing during deposition of self-aligning metal caps in the manner in accordance with the invention.

In a further embodiment, additional components disposed within the computing device 500 can include an integrated circuit die that includes one or more devices, such as a transistor or metal interconnect, wherein the one or more devices are formed by using the method and apparatus that control line edge roughness and line-to-line spacing during deposition of self-aligning metal caps in the manner in accordance with the invention.

In various embodiments, the computing device 500 can be a laptop, a simple laptop, a notebook, an ultra-thin notebook, a smartphone, a tablet, a personal digital assistant (PDA), a super mobile personal computer, a mobile phone, a desktop, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In a further embodiment, the computing device 500 can be any other electronic device used to process data.

In the previous specification, embodiments of the invention have been described with

reference to the specific embodiments of the invention. It is apparent that various modifications may be made to the embodiments of the invention without departing from the broad scope of the invention according to the appended claims. Accordingly, the specification and drawings are to be regarded as illustrative, rather than restrictive.

【List of Reference Numerals】

101: Dielectric substrate
103, 104: Line
105, 107: Line spacing
111-113: Cap
109: Outer edge projection
121, 201, 301: Substrate
123, 403: Interconnect line
125, 405: Line to line interval
203, 303, 401: Dielectric layer
204: Photoresist layer
202: Hard mask layer
206, 220: Opening
205: Conductive layer
208, 304, 305: Conductive line
211, 221: Thickness
209, 317: Width
207, 309: Interval
212, 302, 307: Channel

214, 216: Sidewall

213: Depth

315: Length

215, 311, 319: Cover layer

400: Interconnect structure

500: Data Processing System

504: Memory

526: Processing logic

502: processor

506: Static memory

518: Auxiliary memory

530: Bus bar

508: Network interface device

510: Video display unit

512: Digital input device

514: Cursor control device

516: Signal generator

531: Device-accessible storage media

522: Software

520: Network

530: Board

1006: Communication chip

Claims

1. An integrated circuit structure comprising:
 - a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen, and carbon; and
 - a conductive structure in the dielectric layer, the conductive structure comprising:
 - a first conductive material comprising copper, the first conductive material having an upper surface, and a portion of the upper surface of the first conductive material being below a portion of the upper surface of the dielectric layer; and
 - a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have the same width at a position where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion that is substantially coplanar with a portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and
 - a barrier layer partially surrounding the electrically conductive structure, the barrier layer comprising tantalum.
2. The integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.
3. The integrated circuit structure of claim 1, wherein the second conductive material further comprises boron.
4. The integrated circuit structure of claim 3, wherein the second conductive material further comprises phosphorus.
5. The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten.

6. The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten and phosphorus.

7. The integrated circuit structure of claim 1, wherein the second conductive material further comprises phosphorus.

8. The integrated circuit structure of claim 7, wherein the second conductive material further comprises tungsten.

9. A method of fabricating an integrated circuit structure, the method comprising the steps of:

forming a dielectric layer comprising silicon, oxygen, and carbon;

forming a trench in the dielectric layer; forming a barrier layer in the trench, the barrier layer comprising tantalum;

forming a first conductive material in the barrier layer, the first conductive material comprising copper;

recessing the first conductive material below a portion of an upper surface of the dielectric layer; and

forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have the same width at a position where the first conductive material and the second conductive material meet, and wherein the upper surface of the second electrically conductive material has a curved corner below the portion of the upper surface of the dielectric layer.

10. The method of claim 9, wherein the step of recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.

11. The method of claim 9, wherein the barrier layer further comprises nitrogen.

12. The method of claim 9, wherein the second conductive material further comprises boron.

13. The method of claim 12, wherein the second electrically conductive material further comprises phosphorus.

14. The method of claim 12, wherein the second conductive material further comprises tungsten.

15. The method of claim 12, wherein the second conductive material further comprises tungsten and phosphorus.

16. The method of claim 9, wherein the second electrically conductive material further comprises phosphorus.

17. The method of claim 16, wherein the second conductive material further comprises tungsten.

18. An apparatus for preventing electromigration, comprising:
a substrate;
a dielectric layer over the substrate;
at least one trench in the dielectric layer, the trench having a dielectric sidewall;
a conductive material in the at least one trench, the conductive material comprising copper and cobalt,
a cover region on the conductive material and a portion of the dielectric sidewall over the conductive material, wherein the cover region comprises a rounded corner part facing the conductive material.

19. The apparatus of claim 18, wherein the top of the cover region adjacent to the dielectric layer is no higher than a top boundary of the dielectric layer adjacent to the cover region.

20. The apparatus of claim 18, wherein the electrically conductive material is no higher than a top boundary of the dielectric layer located adjacent the electrically conductive material.

21. The apparatus of claim 18, further comprising: a barrier layer interposed between the conductive material and the dielectric sidewall of the at least one trench.

22. The apparatus of claim 18, wherein the cover region comprises cobalt.

23. The apparatus of claim 18, wherein the dielectric layer comprises a low-k material.

24. The apparatus of claim 18, wherein the dielectric layer comprises silicon, oxygen, and carbon.

25. The apparatus of claim 18, wherein the substrate comprises a semiconductor material.

26. The apparatus of claim 18, wherein the conductive material is part of an interconnect.

27. The apparatus of claim 18, wherein the dielectric layer comprises a carbon-doped silicon oxide.

28. A data processing system comprising
a chip comprising an electronic device comprising a substrate;
a dielectric layer over the substrate;
at least one trench in the dielectric layer, the trench having a dielectric sidewall;
a conductive material in the at least one trench, the conductive material comprising copper and cobalt; and
a cover region on the conductive material and a portion of the dielectric sidewall over the conductive material, wherein the cover region includes a rounded corner facing the conductive material.

29. The data processing system of claim 28, wherein a top of the cover region adjacent to the dielectric layer is no higher than a top boundary of the dielectric layer adjacent the cover region.

30. The data processing system of claim 28, wherein the conductive material is no higher than a top boundary of the dielectric layer located adjacent to the conductive material.

31. The data processing system of claim 28, wherein the electronic device further comprises a barrier layer between the conductive material and the dielectric sidewall of the at least one trench.

32. The data processing system of claim 28, wherein the cover region comprises cobalt.

33. The data processing system of claim 28, wherein the dielectric layer comprises a low-k material.

34. The data processing system of claim 28, wherein the dielectric layer comprises silicon, oxygen, and carbon.

35. The data processing system of claim 28, wherein the substrate comprises a semiconductor material.

36. A data processing system as claimed in claim 28, wherein the conductive material is part of an interconnection.

37. The data processing system of claim 28, wherein the dielectric layer comprises a carbon-doped silicon oxide.

DRAWINGS

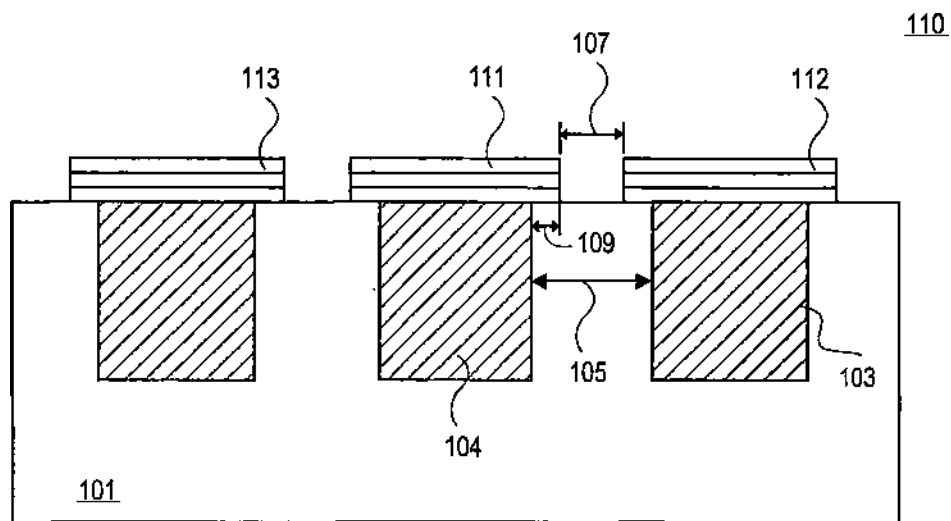


FIG. 1A
(Prior Art)

120

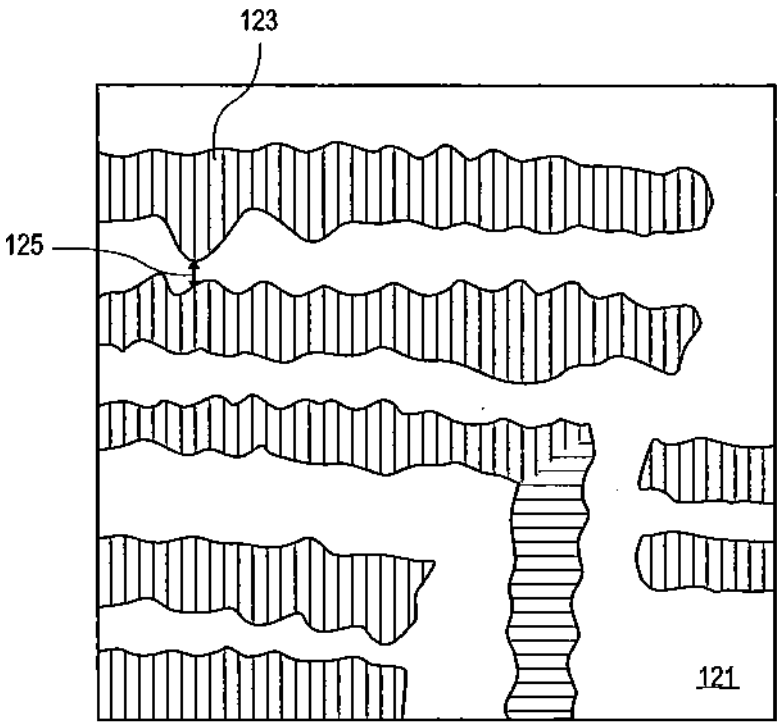


FIG. 1B
(Prior Art)

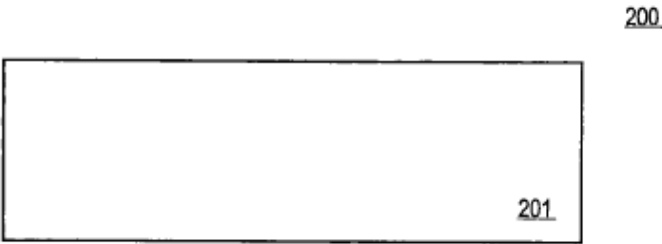


FIG. 2A

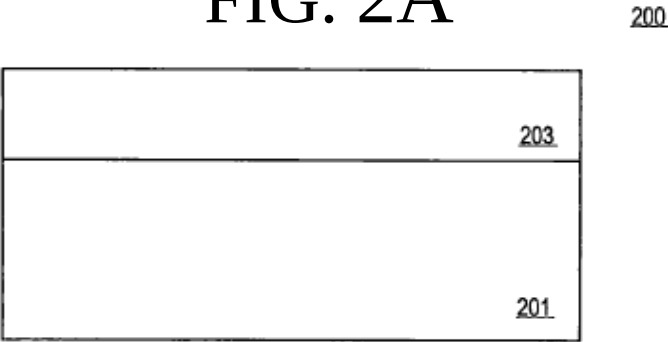


FIG. 2B

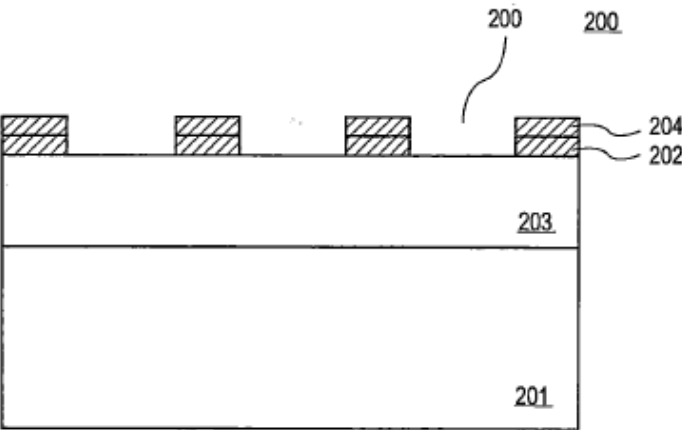


FIG. 2C

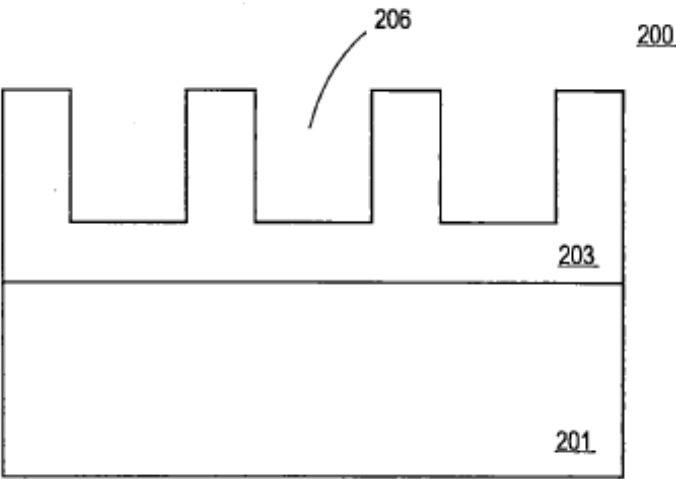


FIG. 2D

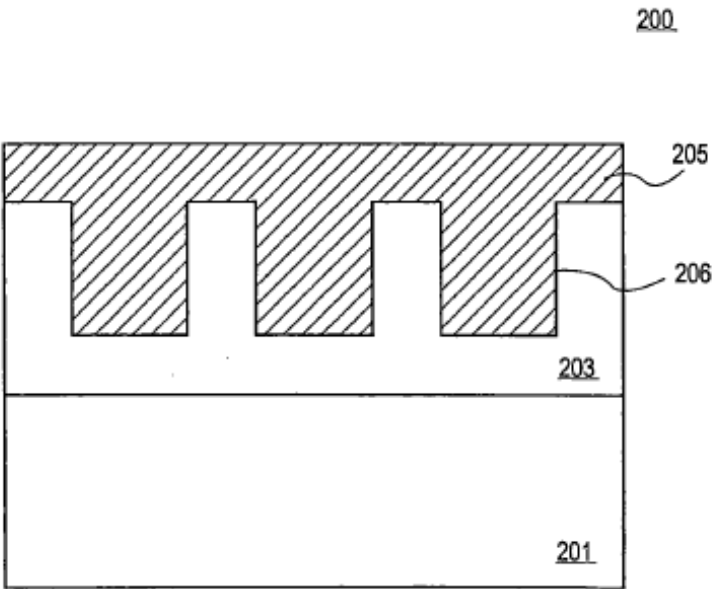


FIG. 2E

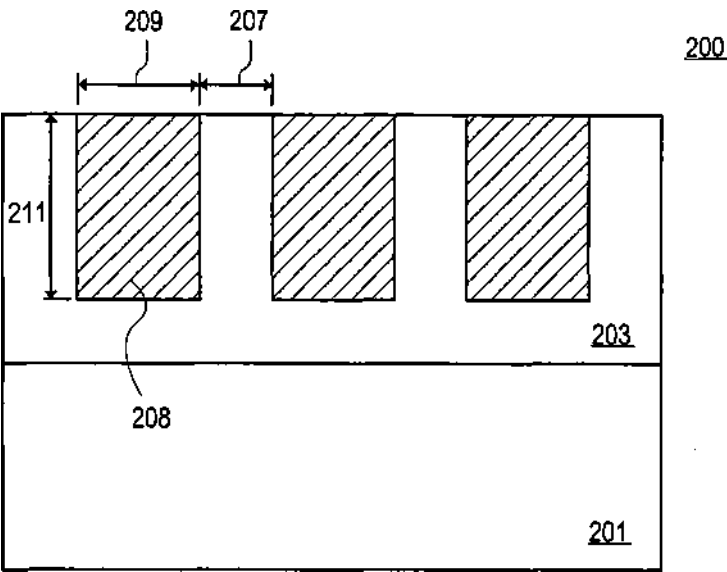


FIG. 2F

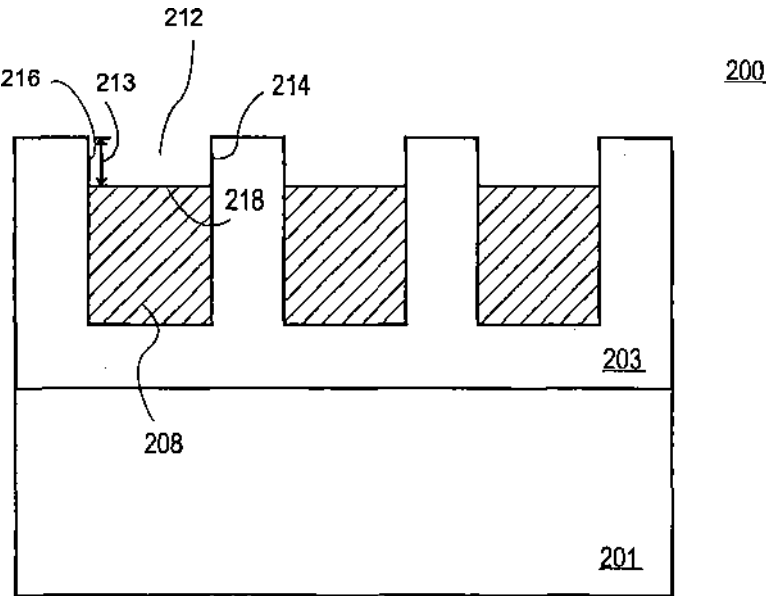


FIG. 2G

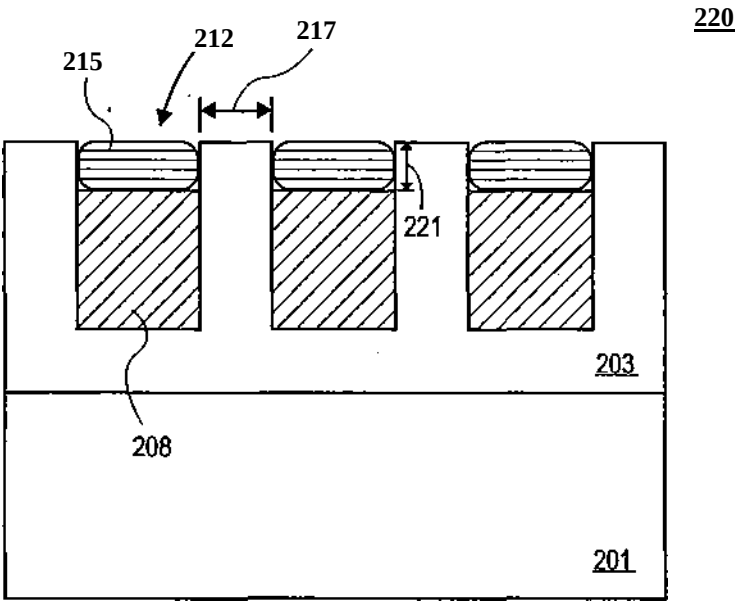


FIG. 2H

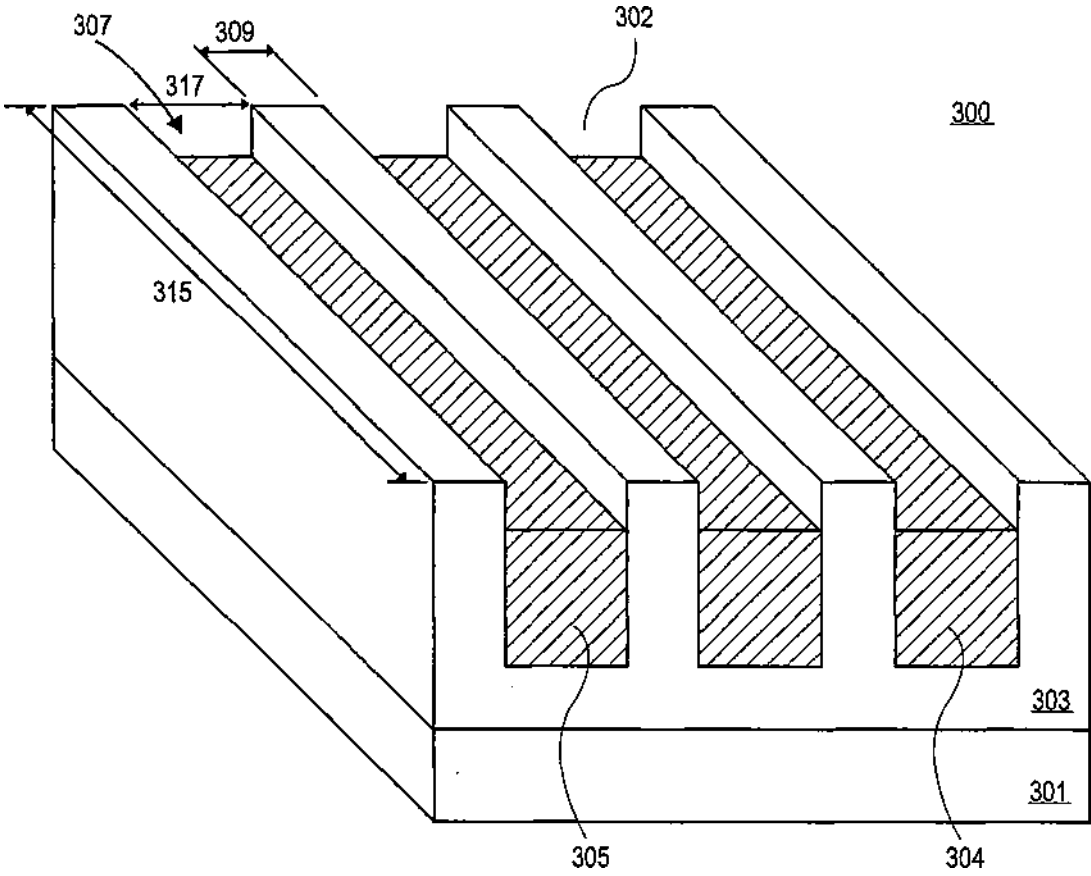


FIG. 3A

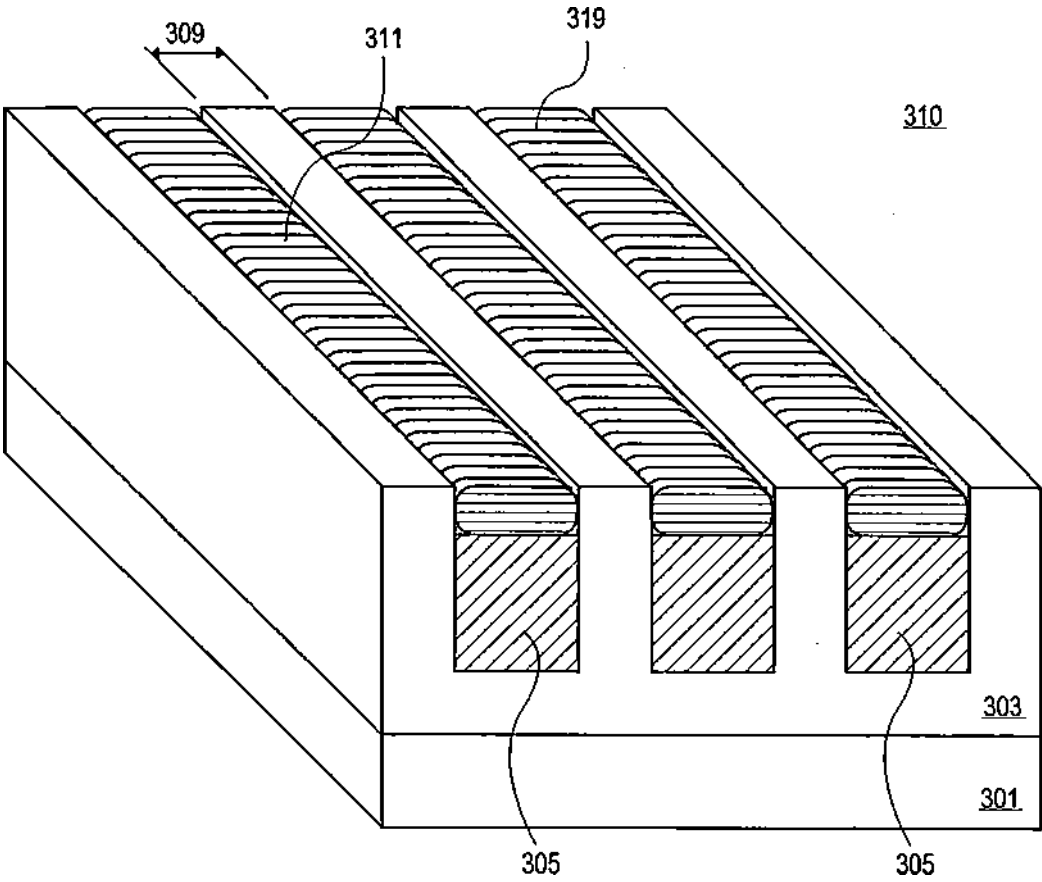


FIG. 3B

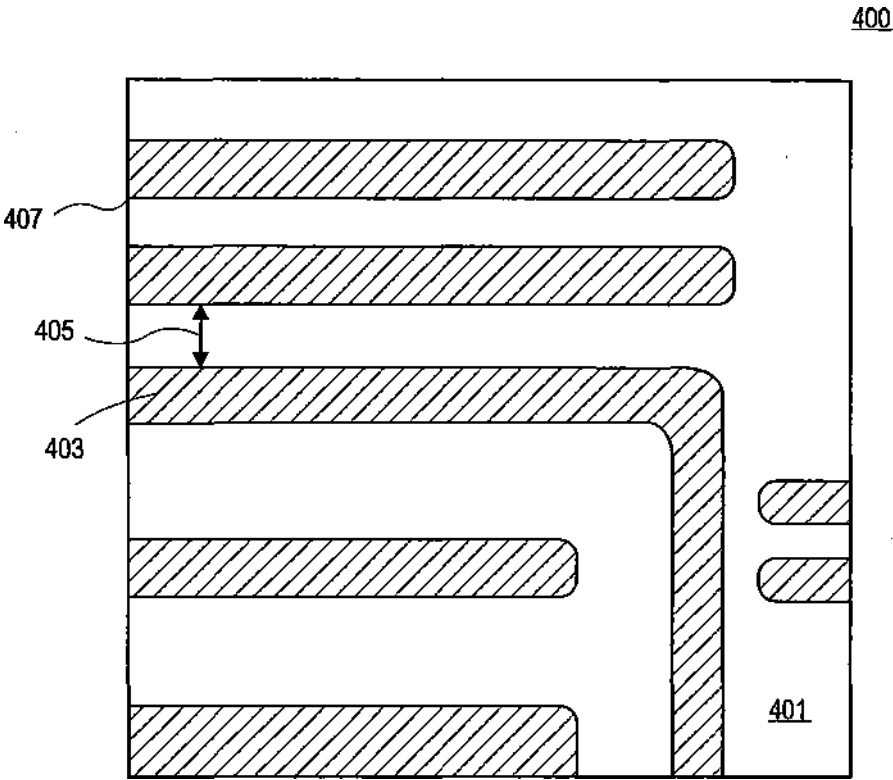


FIG. 4

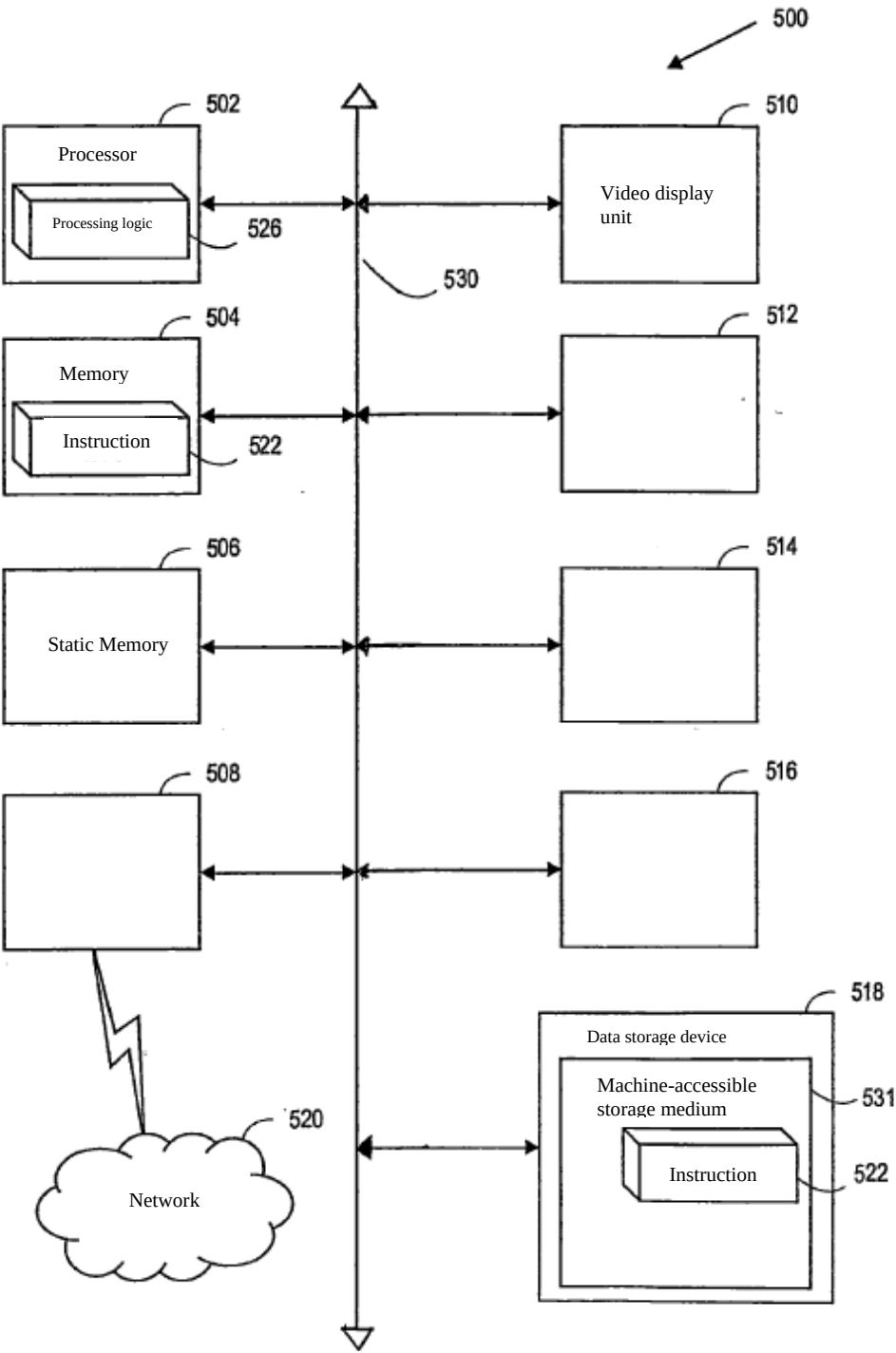


FIG. 5



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(54)名稱

形成自我對準帽之方法與裝置

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

(57)摘要

使一基材之上的一介電層中之至少一導電線凹入，而形成一通道。該通道係自我對準該導電線。可使用一化學劑將該導電線蝕刻到一預定深度，而形成該通道，其中該化學劑包含一抑制劑，用以提供與結晶取向無關的蝕刻之均勻性。在該通道中之該凹入導電線上沈積用來防止電遷移之一覆蓋層。該通道被配置成將該覆蓋層容納在該導電線之寬度內。

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemistry comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A capping layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the capping layer within the width of the conductive line.

指定代表圖：

符號簡單說明：

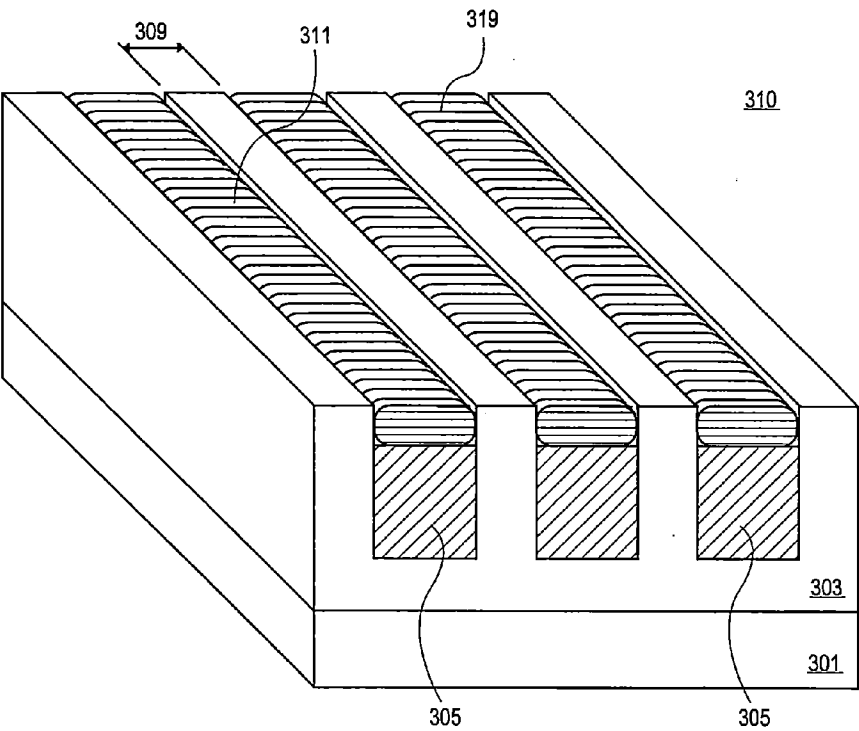
301 . . . 基材

303 . . . 介電層

305 . . . 導電線

309 . . . 間隔

311、319 . . . 覆蓋層



第3B圖

發明摘要

※申請案號：106120928（由101140536分割）

※申請日：101年11月01日

※IPC分類：H01L 21/768 (2006.01)

【發明名稱】(中文/英文)

形成自我對準帽之方法與裝置

Methods and apparatuses to form self-aligned caps

【中文】

使一基材之上的一介電層中之至少一導電線凹入，而形成一通道。該通道係自我對準該導電線。可使用一化學劑將該導電線蝕刻到一預定深度，而形成該通道，其中該化學劑包含一抑制劑，用以提供與結晶取向無關的蝕刻之均勻性。在該通道中之該凹入導電線上沈積用來防止電遷移之一覆蓋層。該通道被配置成將該覆蓋層容納在該導電線之寬度內。

【英文】

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemistry comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A capping layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the capping layer within the width of the conductive line.

【代表圖】

【本案指定代表圖】：第(3B)圖。

【本代表圖之符號簡單說明】：

301：基材

303：介電層

305：導電線

309：間隔

311、319：覆蓋層

【本案若有化學式時，請揭示最能顯示發明特徵的化學式】：無

發明專利說明書

(本說明書格式、順序，請勿任意更動)

【發明名稱】(中文/英文)

形成自我對準帽之方法與裝置

Methods and apparatuses to form self-aligned caps

【技術領域】

本發明之實施例係有關電子裝置製造之領域，尤係有關互連結構之形成。

【先前技術】

由於電子裝置的特徵尺寸 (feature size) 縮小，所以互連的可靠性對積體電路性能變得極為重要。一般而言，電遷移 (electromigration) 述及導體中由於導電電子與擴散金屬原子間之動量轉移 (momentum transfer) 產生的離子移動而造成之材料遷移。此種效應在使用高電流密度的應用中 (例如，在涉及邏輯裝置的微電子結構中) 尤其重要。通常將金屬覆蓋技術用來防止電遷移。

第 1A 圖是具有金屬電遷移帽的一典型互連結構之一橫斷面圖。如第 1A 圖所示，在一介電基材 101 上形成之諸如線 103 及 104 等的金屬互連線原本被一線間隔 105 間隔開。可使用無電鍍 (electroless plating) 而在該基材的一平面之上的各別互連線上生長諸如帽 111-113 等的電遷移帽。一般而言，該等互連線上的該等電遷移帽之生長是

等向性的 (isotropic)。可在該基材之上而以垂直及橫向之方式在互連金屬線上生長該電遷移帽。該金屬電遷移帽的橫向生長可產生凸出基材 101 且超出該等互連線的寬度之諸如一外緣凸出 109 等的外伸結構。如第 1A 圖所示，該等金屬帽之橫向生長使線至線間隔自間隔 105 減少到間隔 107。

外緣凸出 109 之尺寸通常為帽厚度的大約 50%。例如，如果兩個相鄰金屬帽有大約 10 奈米 ("nm") 的厚度，則其外緣凸出的總尺寸可以在大約 2x5 奈米。因此，線至線間隔可減少了諸如二分之一，而自大約 20 奈米減少到大約 10 奈米。

第 1B 圖是一典型互連結構之一上視圖，該互連結構具有在有諸如互連線 123 等的一些互連線之基材 121 的一平面之上以無電方式生長的一些金屬電遷移帽。如第 1B 圖所示，該基材之上的該等金屬帽之橫向生長增加了線邊緣粗糙程度 (Line Edge Roughness; 簡稱 LER)，且減少了線至線間隔。如第 1B 圖所示，諸如線至線間隔 125 等的線至線間隔不受控制地改變。增加的 LER 及減少的線至線間隔都對該等互連結構的可靠性有不利的影響，且增加了可能導致整個積體電路裝置故障的電流短路之風險。

【發明內容】

使一基材之上的一介電層中之至少一導電線凹入，而形成一通道。該通道係自我對準該導電線。可使用一化學

劑將該導電線蝕刻到一預定深度，而形成該通道，其中該化學劑包含一抑制劑，用以提供了與結晶取向（*crystallographic orientation*）無關的蝕刻之均勻性。在該通道中之該凹入導電線上沈積用來防止電遷移之一覆蓋層。該通道被配置成將該覆蓋層容納在該導電線之寬度內。

【圖式簡單說明】

已參照各附圖而以舉例且非限制之方式說明了本發明，在該等附圖中，相像的代號指示類似的元件，其中：

第 1A 圖是具有金屬電遷移帽的一典型互連結構之一橫斷面圖。

第 1B 圖是具有金屬電遷移帽的一典型互連結構之一上視圖。

第 2A 圖示出用來製造根據本發明的一實施例的一互連結構的一基材之一橫斷面圖。

第 2B 圖是根據本發明的一實施例而在該基材之上形成一介電層之後的類似於第 2A 圖之一圖。

第 2C 圖是根據本發明的一實施例而在該介電層之上沈積一光阻層而在該介電層中形成一或多個開口之後的類似於第 2B 圖之一圖。

第 2D 圖是根據本發明的一實施例而在該介電層中形成了一或多個開口之後的類似於第 2C 圖之一圖。

第 2E 圖是根據本發明的一實施例而在該介電層之上

沈積了一導電層之後的類似於第 2D 圖之一圖。

第 2F 圖是根據本發明的一實施例而在自該介電層的上表面去除該導電層及該基部層中之該等開口之外的一些部分而形成有圖案的導電線之後的類似於第 2E 圖之一圖。

第 2G 圖是根據本發明的一實施例而在一基材之上的一介電層中凹入導電線之後的類似於第 2F 圖之一圖。

第 2H 圖是根據本發明的一實施例而在將該等覆蓋層選擇性地沈積到該等通道中之各別被凹入的導電線而防止電遷移之後的類似於第 2G 圖之一圖。

第 3A 圖是根據本發明的一實施例而在凹入一基材之上的一介電層中之該等導電線之後的一互連結構之三維圖 300。

第 3B 圖是根據本發明的一實施例而在將覆蓋層沈積到該等凹入導電線形成的各別通道之後的類似於第 3A 圖之一圖 310。

第 4 圖是根據本發明的一實施例而具有被選擇性地沈積到一基材之上的一介電層中之凹入導電線所形成的通道內之覆蓋層之一互連結構 400 之一上視圖。

第 5 圖示出一資料處理系統的一實施例之一方塊圖。

【實施方式】

在下文之說明中，述及了諸如特定材料或元件尺寸等的許多特定細節，以便提供對本發明的一或多個實施例之

徹底了解。然而，對此項技術具有一般知識者應可了解：可在沒有這些特定細節的情形下實施本發明的該一或多個實施例。在其他的情形中，並未詳述半導體製程、技術、材料、或設備等的習知事項，以避免非必要地模糊了本說明。對此項技術具有一般知識者在參閱所包含的說明之後，將能夠在無須過度實驗之情形下實施適當的功能。

雖然將說明且在各附圖中示出了本發明的某些實施例，但是我們應可了解：這些實施例只是本發明的例示而非限制，且本發明不限於所示及所述的特定結構及配置，這是因為對此項技術具有一般知識者可作出一些修改。

在本說明書中提及"一個實施例"、"另一實施例"、或"一實施例"時，意指以與該實施例有關之方式所述之一特定特徵、結構、或特性被包含在本發明的至少一實施例。因此，在本說明書中各處出現詞語"在一實施例中"或"對於一實施例而言"時，不必然都參照到相同的實施例。此外，可在一或多個實施例中以任何適當的方式結合該等特定特徵、結構、或特性。

此外，本發明的觀點呈現少於所揭示的單一實施例的所有特徵。因此，在實施方式之後的申請專利範圍特此被明確地併入該實施方式，而使每一申請專利範圍獨立對應本發明的一各別之實施例。雖然將參照數個實施例而說明本發明，但是熟悉此項技術者當可了解：本發明不限於所述之該等實施例，而是可在後附的申請專利範圍之精神及範圍內以修改及改變實施本發明。本說明因而將被視為例

示而非限制。

本發明說明了於沈積自我對準金屬帽時控制線邊緣粗糙程度（LER）及線至線間隔之方法及裝置。使至少一導電線凹入，而形成一基材之上的一介電層中之一通道。在該通道中之該凹入導電線上沈積用來防止電遷移之一覆蓋層。該通道係自我對準該導電線。該通道被配置成將該覆蓋層容納在該導電線的寬度內。亦即，使該互連線凹入，而將該帽生長容納在自我對準該互連線之一通道內。如將於下文中進一步詳細說明的，可使用一化學劑將該導電線蝕刻到一預定深度，而形成該通道，其中該化學劑包含一抑制劑，而提供了與結晶取向無關的蝕刻之均勻性。可將本發明所述之方法及裝置用來控制與選擇性沈積之諸如無電鍍鈷帽等的電遷移帽相關聯的 LER 之增加。亦即，可將一無電鍍帽容納在自我對準一互連線的一凹入處內，而防止通常與被選擇性沈積在金屬互連線上的電遷移帽相關聯的 LER 之增加以及線至線間隔之減少。消除 LER 之增加且防止線至線間隔之減少時，可降低故障的風險，且可提高小尺寸的（例如，奈米尺度的）電子裝置之製造良率（manufacturing yield）。該等電子裝置可以是諸如電晶體、記憶體、邏輯裝置等的電腦系統架構裝置、以及任何其他其他的積體電路及微電子裝置。

第2A圖示出用來製造根據本發明的一實施例的一互連結結構的一基材之一橫斷面圖200。在一實施例中，基材201包括一單晶矽。在一實施例中，基材201包括一矽上絕緣

體（Silicon On Insulator；簡稱SOI）。對於替代實施例而言，基材可包含諸如磷化銮、砷化鎵、氮化鎵、矽鍺、及碳化矽等的化合物半導體（compound semiconductor）。在另一實施例中，基材201可包括諸如玻璃及石英。基材201可包含具有諸如電晶體、開關、光電子裝置、電容、電阻、互連（圖中未示出）等的主動及被動裝置的積體電路之一或多個金屬化層（metalization layer）。可以諸如層間介質等的一介電材料（圖中未示出）將基材201的積體電路之該一或多個金屬化層與鄰近的金屬化層隔離。可以通孔（圖中未示出）在電氣上互連該等鄰近的金屬化層。

第2B圖是根據本發明的一實施例而在基材201之上形成一介電層203之後的類似於第2A圖之一圖。在一實施例中，介電層203是一層間介電質（Interlayer Dielectric；簡稱ILD）。在一實施例中，介電層203是諸如二氧化矽、氧化矽、碳摻雜氧化物（Carbon Doped Oxide；簡稱CDO）、或以上各項的任何組合等的一低k值介質。在一實施例中，介電層203包括氮化物、氧化物、聚合物、磷矽玻璃（phosphosilicate glass）、氟矽玻璃（fluorosilicate glass）（SiOF）、有機矽玻璃（organosilicate glass）（SiOCH）、或以上各項的任何組合。在一實施例中，介電層203包括旋塗（spin-on）低k值介電材料。在一實施例中，介電層203是二氧化矽。在另一實施例中，介電層203是氮化矽。可使用任何適當的

沈積技術沈積介電層 203。在一實施例中，可使用諸如化學氣相沈積（Chemical Vapor Deposition；簡稱 CVD）、濺鍍（sputtering）、旋塗、或另一薄膜沈積技術等的毯覆式沈積（blanket deposition）技術沈積介電層 203。在一實施例中，介電層 203 被沈積到範圍大約為 50 奈米至 2 微米之厚度。

第 2C 圖是根據本發明的一實施例而在介電層 203 之上沈積一光阻層 204 而在介電層 203 中形成一或多個開口之後的類似於第 2B 圖之一圖。在一實施例中，如第 2C 圖所示，在介電層 203 上形成的一硬遮罩層 202 上沈積光阻層 204。在另一實施例中，光阻層 204 被直接沈積到介電層 203 上。如第 2C 圖所示，光阻層 204 及硬遮罩層 202 被產生圖案且被蝕刻，而形成諸如開口 220 等的一些開口。光阻及硬遮罩的圖案產生及蝕刻是對微電子裝置製造技術具有一般知識者所習知的。可使用對微電子裝置製造技術具有一般知識者習知的技術中之一種技術執行光阻的圖案產生及蝕刻。該技術可包含：遮蔽該光阻層；使該被遮蔽層曝光；然後使未被曝光的各部分顯影，以便去除該光阻層中被曝光的該等部分，而在該光阻層中形成一開窗。在一實施例中，可在一電漿反應器中執行曝光及光阻層去除之程序。可使用諸如反應式離子蝕刻（Reactive Ion Etch；簡稱 RIE）等的乾式蝕刻、濕式蝕刻、或以上各項技術的任何組合蝕刻硬遮罩層 202 中之開口，而露出介電層 203 的一部分。

第 2D 圖是根據本發明的一實施例而在介電層 203 中形成了諸如開口 206 等的一或多個開口之後的類似於第 2C 圖之一圖。在一實施例中，經由介電層 203 中之諸如開口 220 等的開口而實施諸如開口 206 等的該等開口。在另一實施例中，經由被直接沈積到介電層 203 上的有圖案之光阻 204 中之該等開口蝕刻該介電層，而形成該等開口。在一實施例中，使用諸如雷射蝕刻等的非等向乾式蝕刻（anisotropic dry etching）形成介電層 203 中之諸如溝槽等的開口。在另一實施例中，使用乾式蝕刻、濕式蝕刻、或對微電子裝置製造技術具有一般知識者習知的技術之一組合形成介電層 203 中之該等開口。在一實施例中，介電層 203 中之該等開口具有範圍大約為 0.005 微米（ μm ）至 $5\mu\text{m}$ 的寬度、以及範圍大約為 $0.005\mu\text{m}$ 至 $10\mu\text{m}$ 的深度。在一實施例中，該製程中稍後在 ILD 203 內形成的導電線之尺寸決定了該等開口之尺寸。

在形成了諸如開口 206 等的該等開口之後，去除該光阻及硬遮罩。自介電層 203 去除該光阻及硬遮罩是對微電子裝置製造技術具有一般知識者所習知的。在一實施例中，可使用一化學技術、機械技術、或以上兩者去除該光阻及硬遮罩。

第 2E 圖是根據本發明的一實施例而在介電層 203 之上沈積了一導電層 205 之後的類似於第 2D 圖之一圖。如第 2E 圖所示，導電層 205 之形成涉及以一導電材料填入介電層 203 中之該一或多個開口，而形成一或多條導電

線。在一實施例中，先在介電層 203 上沈積用來覆蓋該等開口的內部側壁及底部之一基部層（圖中未示出），然後在該基部層上沈積一導電層 205。在一實施例中，該基部層包含在一導電障壁層（conductive barrier layer）（圖中未示出）上沈積之一導電晶種層（seed layer）。該晶種層可包括銅，且該導電障壁層可包括鋁、鈦、鉭、氮化鉭、及類似的材料。該導電障壁層可被用來防止導電材料自諸如銅等的該晶種層擴散到 ILD 203。此外，該導電障壁層可被用來提供該晶種層（例如，銅）之黏著。在一實施例中，爲了形成該基部層，將該導電障壁層沈積到介電層 203，而覆蓋該等開口之側壁及底部，然後在該導電障壁層上沈積該晶種層。在另一實施例中，該導電基部層包含被直接沈積到介電層 203 而覆蓋該等開口之側壁及底部的該晶種層。可使用對半導體製造技術具有一般知識者習知的任何薄膜沈積技術（例如，以濺鍍、毯覆式沈積等的薄膜沈積技術）沈積該導電障壁層及晶種層中之每一層。在一實施例中，該導電障壁層及晶種層中之每一層具有範圍大約爲 1 至 100 奈米之厚度。在一實施例中，該障壁層可以是被蝕刻而建立至下方金屬層的導電性之一薄介電質。在一實施例中，可完全省略該障壁層，且可利用銅線的適當摻雜，而作出一"自我形成之"障壁。

導電層 205 填滿諸如開口 206 等的該等開口，且覆蓋該基部層（圖中未示出）中在介電層 203 的頂部上的該等開口之外的一些部分。在一實施例中，以一電鍍製程將諸

如銅等的導電層 205 沈積到銅基部層之該晶種層。在一實施例中，使用對微電子裝置製造技術具有一般知識者習知的一鑲嵌（damascene）製程將導電層 205 沈積到該等開口。在一實施例中，使用諸如電鍍、無電鍍等的對半導體製造技術具有一般知識者習知的選擇性沈積技術中的一種技術將導電層 205 沈積到該晶種層上。在一實施例中，對導電層 205 的材料之選擇決定了對該晶種層的材料之選擇。例如，如果導電層 205 之材料包含銅，則該晶種層之材料也包含銅。在一實施例中，導電層 205 包括諸如銅（Cu）、鈦（Ru）、鎳（Ni）、鈷（Co）、鉻（Cr）、鐵（Fe）、錳（Mn）、鈦（Ti）、鋁（Al）、鈪（Hf）、鉭（Ta）、鎢（W）、釩（V）、鉬（Mo）、鈀（Pd）、金（Au）、銀（Ag）、鉑（Pt）、或以上各項的任何組合。

第 2F 圖是根據本發明的一實施例而在介電層 203 的上表面去除導電層 205 及該基部層中之該等開口之外的一些部分而形成諸如導電線 208 等的有圖案的導電線之後的類似於第 2E 圖之一圖。可以化學方式（例如，使用蝕刻法）、機械方式（例如，研磨法）、或該等技術的一組合（例如，使用對微電子裝置製造技術具有一般知識者習知的化學機械研磨（Chemical-Mechanical Polishing；簡稱 CMP）技術）去除導電層 205 的一些部分。在一實施例中，使用前文所述之方法在介電層 203 內形成一或多條有圖案的導電線。在另一實施例中，對介電層 203 的上表

面上沈積之導電層執行圖案產生及蝕刻，而形成該等導電線。對介電層 203 的上表面上沈積之導電層執行圖案產生及蝕刻是對微電子裝置製造技術具有一般知識者所習知的。在一實施例中，該導電線之諸如厚度 211 等的厚度是大約在 0.015 微米至 1 微米的範圍。在一實施例中，該導電線之諸如寬度 209 等的寬度是大約在 5 奈米至大約 500 奈米的範圍。在一實施例中，該等導電線間之諸如間隔 207 等的間隔是自大約 5 奈米至大約 500 奈米。在一實施例中，該等導電線間之間隔是自大約 2 奈米至大約 100 奈米。

第 2G 圖是根據本發明的一實施例而在一基材之上的一介電層中凹入諸如導電線 208 等的導電線之後的類似於第 2F 圖之一圖。如第 2G 圖所示，在介電層 203 中形成諸如通道 212 等的通道。如第 2G 圖所示，諸如通道 212 等的通道具有由介電層 203 構成的諸如側壁 214 及 216 等的側壁、以及諸如由導電線 208 構成之底部 218 等的由各別導電線構成之底部。

在一實施例中，該通道具有諸如自大約 5 奈米至大約 50 奈米之深度 213 等的深度。在一實施例中，該通道之深度是自大約 2 奈米至大約 20 奈米。在一實施例中，該通道具有自該導電線的諸如第 2F 圖所示之厚度 211 等的厚度之大約 10%至大約 50%的深度。在一實施例中，如將於下文中進一步詳細說明的，該等導電線被凹入到根據覆蓋層的厚度而決定之深度。

第 3A 圖是根據本發明的一實施例而在凹入一基材 301 之上的一介電層 303 中之諸如一導電線 305 及一導電線 304 等的導電線之後的一互連結構之三維圖 300。基材 301、介電層 303、以及導電線 305 及 304 可以是諸如前文所述之任何各別的基材、介電層、及導電線。如第 3A 圖所示，凹入該等導電線，而在基材 301 之上的一介電層 303 中形成諸如一通道 302 及一通道 307 等的通道。如第 3A 圖所示，該等通道自我對準該等各別的導電線。例如，通道 307 自我對準導電線 305，且通道 302 自我對準導電線 304。如第 3A 圖所示，通道之諸如長度 315 等的長度是沿著導電線之長度，且通道之諸如寬度 317 等的長度是沿著導電線之寬度。在一實施例中，通道之長度實質上大於通道之寬度。在一實施例中，通道之寬度小於 100 奈米，且通道之長度至少為 500 奈米。在一實施例中，通道之寬度是自大約 5 奈米至大約 500 奈米，且通道之長度是自大約幾百奈米至大約幾百微米。如第 3A 圖所示，諸如導電線 305 及 304 等的該等導電線被諸如間隔 309 等的距離隔離。在一實施例中，諸如導電線 305 及 304 等的該等導電線間之間隔是自大約 5 奈米至大約 500 奈米。在一實施例中，諸如導電線 305 及 304 等的該等導電線間之間隔是自大約 2 奈米至大約 100 奈米。

在一實施例中，凹入諸如線 208、線 304 及 305 等的導電線涉及使用含有蝕刻劑、氧化劑、抑制劑、及溶劑的化學劑以與結晶取向無關之方式均勻地濕式蝕刻該等導電

線。亦即，將抑制劑及溶劑加至該蝕刻劑時，可在蝕刻期間在導電材料上形成一鈍化層（passivation layer）（圖中未示出），而以與結晶取向無關之方式均勻地蝕刻該導電材料。含有蝕刻劑、氧化劑、抑制劑、及溶劑的該濕式蝕刻化學劑可控制導電線的蝕刻深度，因而可以只凹入導電線的一部分（例如，5%至50%）。

在一實施例中，用來濕式蝕刻導電線而提供沒有圖案相依性及晶向偏好的通道之該化學劑包含質量佔了大約1%至大約40%的一蝕刻劑、質量佔了大約1%至大約10%的一氧化劑、質量佔了大約0.1%至大約1%的抑制劑、以及質量佔了大約1%至大約60%的一有機溶劑。在一實施例中，用來濕式蝕刻導電線之該化學劑包含質量佔了自大約0.1%至大約70%的一蝕刻劑（取決於該蝕刻劑的蝕刻速率）、質量佔了自大約0.1%至大約10%的一氧化劑（取決於該氧化劑的強度）、質量佔了自大約百萬分之50（50 ppm）至大約1%的一抑制劑、以及質量佔了自大約1%至大約60%的一溶劑。

在一實施例中，用來蝕刻導電線之該化學劑可包含：諸如甘胺酸（glycine）、乙二胺四乙酸（ethylenediaminetetraacetic acid）、 α -胺基酸（alpha-amino acid）、多元羧酸（polycarboxylic acid）、或以上各項的任何組合等的蝕刻劑；諸如過氧化物（peroxide）、臭氧（ozone）、過錳酸鹽（permanganate）、鉻酸鹽（chromate）、過硼酸鹽

(perborate) 、次鹵酸鹽 (hypohalite) 、或以上各項的任何組合等的氧化劑；諸如唑 (azole) 、胺 (amine) 、胺基酸 (amino acid) 、磷酸鹽 (phosphate) 、磷酸鹽 (phosphonate) 、或以上各項的任何組合等的抑制劑；以及溶劑。該溶劑可以是諸如水等的水相系統 (aqueous system) (較佳的) 或有機溶劑。有機溶劑之例子是丙烯碳酸鹽 (propylene carbonate) 、環丁砜 (sulfolane) 、乙二醇醚 (glycol ether) 、及氯化甲烷 (methylene chloride) 的有機溶劑。

例如，關於用來蝕刻銅導電線的化學劑中之蝕刻劑，銅金屬通常處於零氧化態 (zero oxidation state) 。爲了蝕刻銅，需要將銅氧化爲 $0+n$ 氧化態，其中 n 可以是任何 1、2、3、或 4。第一氧化態及第二氧化態通常是銅的較常見之氧化態。對於被用來作爲蝕刻劑的任何分子而言，該分子必須能夠結合處於氧化態 1、2、3、或 4 中之任一氧化態的銅。通常利用一分子中之 15 族 (氮族) 、16 族 (氧族) 、或 17 族 (鹵素族) 原子進行該結合。在一實施例中，用來蝕刻銅導電線的蝕刻劑是諸如任何甘胺酸、乙二胺四乙酸、 α -胺基酸、多元羧酸 (例如，係爲三羧酸 (tricarboxylic acid) 之檸檬酸 (citric acid)) 、草酸 (oxalic acid) 、及丙二酸 (malonic acid) 等的有機蝕刻劑。

例如，用來蝕刻銅導電線的該化學劑中之氧化劑被用來將銅氧化態自不溶性銅金屬改變爲可溶性銅離子。可自

諸如任何過氧化物（例如，過氧化氫（hydrogen peroxide））、臭氧、過錳酸鹽、鉻酸鹽、過硼酸鹽、及次鹵酸鹽等的任何氧化劑中選擇該氧化劑。

例如，爲了以均勻且無結晶取向之方式蝕刻構成電流承載線的銅，重要的是將一抑制劑加入該化學劑。抑制劑的作用是形成一鈍化層（自該抑制劑的分子形成的高分子化合物（polymeric compound），用來以一種特定且週期性之方式結合銅）。在銅的受控制蝕刻期間的該鈍化層之形成對於確保蝕刻的均勻性且防止沿著結晶邊界（例如，晶界（grain boundary）的蝕刻侵襲（例如，形成孔洞（void））是極爲重要的。例如，在被選擇的氧化劑及蝕刻劑中不會分解的任何抑制劑都可被用於蝕刻銅導電線之該化學劑。抑制劑的類別是對子裝置製造技術具有一般知識者所習知的。例如，其中包括唑、胺、胺基酸、磷酸鹽、及磷酸鹽的任何有機抑制劑用於蝕刻銅導電線之該化學劑。

在另一實施例中，使用其中包含檸檬酸及過氧化物的化學劑進行濕式蝕刻，而凹入該等銅導電線。然而，包含檸檬酸及過氧化物的化學劑通常有可能難以控制的高蝕刻速率。此外，包含檸檬酸及過氧化物的化學劑之蝕刻速率取決於可能產生粗糙蝕刻表面的結晶取向。將諸如苯并噻唑（benzothiazole）（BTA）等的腐蝕抑制劑加入該化學劑時，有機溶劑中之檸檬酸及過氧化物的稀釋可大幅減緩蝕刻速率，且消除該蝕刻的結晶本質，例如，消除蝕刻

出沿著晶界的銅中之孔洞，而產生平滑的表面。

在一實施例中，以其中包括將該蝕刻化學劑噴灑或傾注到該等導電線之濕式蝕刻法凹入該等導電線。在一實施例中，以其中包括將該等導電線浸泡在該蝕刻化學劑溶液之濕式蝕刻法凹入該等導電線。在一實施例中，在自大約攝氏 15 度至大約攝氏 50 度的溫度下進行濕式蝕刻一段預定時間，而凹入該等導電線。在至少某些實施例中，以諸如電漿蝕刻等的乾式蝕刻法凹入該等導電線。

第 2H 圖是根據本發明的一實施例而在將該等覆蓋層選擇性地沈積到該等通道中之各別被凹入的導電線而防止電遷移之後的類似於第 2G 圖之一圖。使用前文所述的化學劑蝕刻出的該等導電線具有可黏著該覆蓋層之平滑且均勻的上表面。如第 2H 圖所示，覆蓋層 215 被沈積到通道 212 內之凹入的導電線 208 上。在一實施例中，諸如通道 212 等的通道被配置成將一覆蓋層容納在該覆蓋層之諸如第 2F 圖所示的寬度 209 等的寬度內。亦即，該凹入的導電線產生了將該覆蓋層的生長容納在通道內之通道，因而減輕了線至線間隔之減少及 LER 之增加。如第 2H 圖所示，覆蓋層 215 被設置在通道 212 的該等側壁內之導電線 208 上。在一實施例中，以無電鍍（例如，鍍製）、化學氣相沈積（CVD）、物理氣相沈積（Physical Vapor Deposition；簡稱 PVD）、或對電子裝置製造技術具有一般知識者習知的任何其他的選擇性沈積技術將該覆蓋層沈積到該凹入導電線上。在一實施例中，諸如線 208 等的導

電線包含一第一金屬，且該覆蓋層包含與該第一金屬不同的一第二金屬，而該第二金屬被用來防止來自該導電線的該第一金屬之電遷移。在一實施例中，用於該覆蓋層之金屬比用於該導電線之金屬重，以便防止電遷移。

例如，可由其中包括銅、鋁之任何金屬製成該導電線。在一實施例中，係由鈷（Co）、諸如硼磷化鈷（CoBP）、鎢硼磷化鈷（CoWBP）、鎢磷化鈷（CoWP）、鎢硼化鈷（CoWB）、鎢磷化鈷（CoWP）等的無電鍍鈷合金、或以上各項的任何組合製成諸如覆蓋層 215 等的該覆蓋層。在另一實施例中，係由鎳（Ni）、諸如硼磷化鎳（NiBP）、鎢硼磷化鎳（NiWBP）、鎢磷化鎳（NiWP）、鎢硼化鎳（NiWB）、鎢磷化鎳（NiWP）等的無電鍍鎳合金、或以上各項的任何組合製成諸如覆蓋層 215 等的該覆蓋層。在另一實施例中，係由形式為純元素之諸如鉑（Pt）、鈀（Pd）、釕（Ru）、銥（Ir）、銱（Rh）等的鉑（Pt）族金屬或合金製成諸如覆蓋層 215 等的該覆蓋層。用於鉑（Pt）族金屬的典型合金元素是鎢（W）、硼（B）、磷（P）。在又一實施例中，係由諸如鉭（Ta）、鎢（W）、鉬（Mo）、或以上各項的組合等的耐火金屬（refractory metal）製成諸如覆蓋層 215 等的該覆蓋層。

在一實施例中，將鈷覆蓋層沈積到該凹入銅導電層上的一通道內。在一實施例中，將鎳覆蓋層沈積到該凹入銅導電層上的一通道內。在一實施例中，將耐火金屬覆蓋層

沈積到該凹入銅導電層上的一通道內。

在一實施例中，使用無電沈積及諸如化學氣相沈積（CVD）等的氣相沈積中之任一沈積技術將包含鉑（Pt）族金屬、鈷、鎳、或以上各項的組合之該等覆蓋層沈積到諸如銅、鋁等的該等導電層上。在一實施例中，在一實施例中，使用對電子裝置製造技術具有一般知識者習知的CVD及PVD技術中之任何技術將其中包括耐火金屬之該等覆蓋層沈積到諸如銅、鋁等的該等導電層上。在一實施例中，該覆蓋層的諸如厚度221等的厚度是自大約2奈米至大約50奈米。在一實施例中，該覆蓋層之厚度足以防止來自下方的導電層之電遷移。在一實施例中，該覆蓋層具有不大於該覆蓋層被沈積在其內的通道的深度之厚度。

第3B圖是根據本發明的一實施例而在將覆蓋層沈積到該等凹入導電線形成的各別通道之後的類似於第3A圖之一圖310。如第3B圖所示，諸如覆蓋層311及319等的覆蓋層被以前文所述之方式選擇性地沈積到諸如通道302及通道307等的各別通道。如第3A圖所示，該等覆蓋層被容納在其各別的通道內。如第3B圖所示，間隔309將覆蓋層319與覆蓋層311隔離。在一實施例中，導電線305與304間之間隔以及覆蓋層319與311間之間隔是相同的。

第4圖是根據本發明的一實施例而具有被選擇性地沈積到一基材之上的一介電層401中之凹入導電線所形成的通道內之覆蓋層之一互連結構400之一上視圖。如第4圖

所示，諸如互連線 403 等的該等互連線之 LER 實質上減少了，該等互連線之邊緣是平滑的，且諸如線至線間隔 405 等的線至線間隔稱加了且被保持在該等線之間。在一實施例中，該線至線間隔增加了 2 倍的帽厚度。因而可導致電場及介電崩潰（dielectric breakdown）時間的大幅減少，尤其對於具有 20 奈米的線及 20 奈米的間隔的未來技術節點（technology node）更是如此。目前已知可行的最小帽厚度是 5 奈米。此即意指：在傳統的方法下，遮罩上繪製的線至線間隔將是 10 奈米，而不是 20 奈米。此外，外緣凸出的尺寸目前往往是帽厚度的大約 50%。對於 5-10 奈米的典型帽厚度而言，使用前文所述之方法時，LER 可減少 3-5 奈米，且與線寬無關。對於未來的 20 奈米技術節點而言，LER 減少 3-5 奈米時，可導致互連結構的線至線間隔之 15-20% 增加。

第 5 圖示出一資料處理系統 500 的一實施例之一方塊圖，該資料處理系統 500 具有諸如電晶體、記憶體 504 及記憶體 518 等的記憶體、諸如處理邏輯裝置 526 等的處理邏輯裝置、以及使用前文所述之方法而建造之任何其他的積體電路及微電子裝置。如第 5 圖所示，資料處理系統 500 包含一處理器 502，該處理器 502 具有處理邏輯 526。在至少某些實施例中，處理邏輯 526 包含：一基材之上的一介電層中之至少一導電線；該介電層中且在該導電線之上的一通道；以及該通道中之該至少一導電線上的一覆蓋層，該覆蓋層以前文所述之方式防止電遷移。在至

少某些實施例中，記憶體 504 及 518 中之每一記憶體包含：一基材之上的一介電層中之至少一導電線；該介電層中且在該導電線之上的一通道；以及該通道中之該至少一導電線上的一覆蓋層，該覆蓋層以前文所述之方式防止電遷移。

在替代實施例中，該資料處理系統可被連接到（例如，被連線到）一區域網路（Local Area Network；簡稱 LAN）、一企業內部網路（intranet）、一企業間網路（extranet）、或網際網路中之其他機器。該資料處理系統可在一主從式網路環境中以一伺服器或一用戶端機器之身分操作，或在一同級間網路（peer-to-peer network）（或分散式網路（distributed network））環境中以一同級機器之方式操作。該資料處理系統可以是個人電腦（Personal Computer；簡稱 PC）、平板個人電腦、機上盒（Set-Top Box；簡稱 STB）、個人數位助理（Personal Digital Assistant；簡稱 PDA）、行動電話、網路設備、伺服器、網路路由器、交換器或橋接器、或能夠執行可指定將被該資料處理系統接受的行動的一組指令（循序的或其他形式的）之任何機器。此外，雖然只示出單一資料處理系統，但是術語"資料處理系統"也將被理解為包括個別地或聯合地執行用來執行本發明所述的該等方法中之任何一或多種方法的一組（或多組）指令之任何群組的資料處理系統。

該例示資料處理系統 500 包含經由一匯流排 530 而相

互通訊之一處理器 502、一主記憶體 504（例如，唯讀記憶體（Read Only Memory；簡稱 ROM）、快閃記憶體、諸如同步動態隨機存取記憶體（Synchronous DRAM；簡稱 SDRAM）或 Rambus 動態隨機存取記憶體（Rambus DRAM；簡稱 RDRAM）等的動態隨機存取記憶體（Dynamic Random Access Memory；簡稱 DRAM）、靜態記憶體 506（例如，快閃記憶體、靜態隨機存取記憶體（Static Random Access Memory；簡稱 SRAM）等的靜態記憶體）、以及一輔助記憶體 518（例如，一資料儲存裝置）。

處理器 502 代表諸如微處理器或中央處理單元等的一或多個一般用途處理裝置。更具體而言，處理器 502 可以是複雜指令集計算（Complex Instruction Set Computing；簡稱 CISC）微處理器、精簡指令集計算（Reduced Instruction Set Computing；簡稱 RISC）微處理器、極長指令集（Very Long Instruction Word；簡稱 VLIW）微處理器、實施其他指令集的處理器、或實施一些指令集的組合之處理器。處理器 502 也可以是諸如特定應用積體電路（Application Specific Integrated Circuit；簡稱 ASIC）、現場可程式閘陣列（Field-Programmable Gate Array；簡稱 FPGA）、數位信號處理器（Digital Signal Processor；簡稱 DSP）、或網路處理器等的一或多個特殊用途處理裝置。處理器 502 被配置成處理邏輯 526，以便執行本發明所述之操作。

電腦系統 500 可進一步包含一網路介面裝置 508。電腦系統 500 亦可包含一視訊顯示單元 510（例如，一液晶顯示器（Liquid Crystal Display；簡稱 LCD）、發光二極體顯示器（Light Emitting Diode Display；簡稱 LED）、或一陰極射線管（Cathode Ray Tube；簡稱 CRT）、一文數字輸入裝置 512（例如，一鍵盤）、一游標控制裝置 514（例如一滑鼠）、及一信號產生裝置 516（例如，一喇叭）。

輔助記憶體 518 可包含一機器可存取的儲存媒體（或尤指一電腦可讀取的儲存媒體）531，該機器可存取的媒體中儲存了用來實施本發明所述的該等方法或功能中之任何一或多種方法或功能之一或多組指令（例如，軟體 522）。在電腦系統 500 執行軟體 522 期間，可將軟體 522 完全地或至少部分地儲存在主記憶體 504 及／或處理器 502 內，其中主記憶體 504 及處理器 502 也構成機器可讀取的儲存媒體。可進一步經由網路介面裝置 508 及一網路 520 而傳輸或接收軟體 522。

雖然機器可存取的儲存媒體 531 在一實施例中被示為一單一媒體，但是術語"機器可讀取的儲存媒體"應被理解為包括用來儲存該一或多組指令之一單一媒體或多個媒體（例如，集中式或分散式資料庫及／或相關聯的快取記憶體及伺服器）。術語"機器可讀取的儲存媒體"也應被理解為包括能夠儲存或編碼一組指令以供機器執行且使該機器執行本發明的該等方法中之任何一或多種方法之任何媒

體。術語"機器可讀取的儲存媒體"因而應被理解為包括（但不限於）固態記憶體、光學媒體、及磁性媒體。

在替代實施例中，第 5 圖示出一計算裝置 500。計算裝置 500 設有一板 530。該板可包含其中包括（但不限於）一處理器 502 及至少一通訊晶片 508 之一些組件。處理器 502 在實體上及電氣上被耦合到板 530。在某些實施例中，至少一通訊晶片也在實體上及電氣上被耦合到板 530。在進一步的實施例中，通訊晶片 508 被整合在處理器 502 內。

計算裝置 500 可根據其應用而包含可以在或可以不在實體上及電氣上被耦合到板 530 之其他組件。這些其他組件包括（但不限於）揮發性記憶體（例如，DRAM）、非揮發性記憶體（例如，ROM）、快閃記憶體、圖形處理器、數位信號處理器、密碼處理器、晶片組、天線、顯示器、觸控式螢幕控制器、電池、音訊編碼解碼器、視訊編碼解碼器、功率放大器、全球衛星定位系統（Global Positioning System；簡稱 GPS）裝置、羅盤、加速度計、陀螺儀、喇叭、相機、及大量儲存裝置（諸如硬碟機、固態硬碟、光碟機、及數位多功能光碟（Digital Versatile Disk；簡稱 DVD）機等的組件。

通訊晶片 508 能夠執行無線通訊，以便將資料傳輸進及出計算裝置 500。術語"無線"及其衍生物可被用來描述可利用通過非固體介質的被調變之電磁輻射而傳送資料之電路、裝置、系統、方法、技術、或通訊通道等的項目。

該術語並不意味著相關聯的裝置不包含任何導線，但是該等裝置在某些實施例中可能不包含任何導線。通訊晶片 508 可實施其中包括（但不限於）Wi-Fi（IEEE 802.11 系列）、WiMAX（IEEE 802.16 系列）、IEEE 802.20、長程演進計畫（Long Term Evolution；簡稱 LTE）、演進資料最佳化（Ev-DO）、增強型高速封包接取網路（HSPA+）、增強型高速下行封包存取（HSDPA+）、增強型高速上行封包存取（HSUPA+）、增強型資料 GSM 環境（EDGE）、全球行動通訊系統（GSM）、通用封包無線電服務（GPRS）、劃碼多向近接（CDMA）、分時多向近接（TDMA）、數位增強無線通訊（DECT）、藍牙（Bluetooth）、上述各項的衍生標準或協定、以及被稱為第三代（3G）、第四代（4G）、第五代（5G）、及未來各世代之任何其他無線協定的一些無線標準或協定中之任何無線標準或協定。計算裝置 500 可包含複數個通訊晶片 508。例如，一第一通訊晶片 508 可被專用於諸如 Wi-Fi 及藍牙等的較短距離之無線通訊，且一第二通訊晶片 1006 可被專用於諸如 GPS、EDGE、GPRS、CDMA、WiMAX、LTE、Ev-DO、及其他無線通訊等的較長距離之無線通訊。

計算裝置 500 之處理器 502 包含被封裝在處理器 502 內之一積體電路晶粒。在本發明的某些實施例中，該處理器之該積體電路晶粒包含諸如電晶體或金屬互連等的一或多個裝置，其中係使用可以本發明所述之方式控制沈積自

我對準的金屬帽時的線邊緣粗糙程度及線至線間隔之方法及設備而形成該一或多個裝置。術語"處理器"可參照到用來處理來自暫存器及／或記憶體的電子資料且將該電子資料轉換為可被儲存在暫存器及／或記憶體的其他電子資料的任何裝置或裝置的一部分。

通訊晶片 508 也包括被封裝在通訊晶片 508 內之一積體電路晶粒。根據本發明的另一實施例，該通訊晶片之該積體電路晶粒包含諸如電晶體或金屬互連等的一或多個裝置，其中係使用可以本發明所述之方式控制沈積自我對準的金屬帽時的線邊緣粗糙程度及線至線間隔之方法及設備而形成該一或多個裝置。

在進一步的實施例中，計算裝置 500 內所設有之另外組件可包含一積體電路晶粒，該積體電路晶粒包含諸如電晶體或金屬互連等的一或多個裝置，其中係使用可以本發明所述之方式控制沈積自我對準的金屬帽時的線邊緣粗糙程度及線至線間隔之方法及設備而形成該一或多個裝置。

在各實施例中，該計算裝置 500 可以是膝上型電腦、簡易筆記本電腦、筆記型電腦、超輕薄筆記型電腦、智慧型手機、平板電腦、個人數位助理（PDA）、超級行動個人電腦、行動電話、桌上型電腦、伺服器、印表機、掃描器、監視器、機上盒、娛樂控制單元、數位相機、可攜式音樂播放器、或數位錄影機。在進一步的實施例中，計算裝置 500 可以用來處理資料的任何其他電子裝置。

在前文之說明書中，已參照本發明的一些特定實施例

而說明了本發明的實施例。顯然可在不脫離後附的申請專利範圍述及的本發明實施例之較寬廣的精神及範圍下對本發明的實施例作出各種修改。因此，本說明書及各圖式將被視為例示性而非限制性。

【符號說明】

101：介電基材

103、104：線

105、107：線間隔

111-113：帽

109：外緣凸出

121、201、301：基材

123、403：互連線

125、405：線至線間隔

203、303、401：介電層

204：光阻層

202：硬遮罩層

206、220：開口

205：導電層

208、304、305：導電線

211、221：厚度

209、317：寬度

207、309：間隔

212、302、307：通道

214、216：側壁
 213：深度
 315：長度
 215、311、319：覆蓋層
 400：互連結構
 500：資料處理系統
 504：記憶體
 526：處理邏輯
 502：處理器
 506：靜態記憶體
 518：輔助記憶體
 530：匯流排
 508：網路介面裝置
 510：視訊顯示單元
 512：文數字輸入裝置
 514：游標控制裝置
 516：信號產生裝置
 531：機器可存取的儲存媒體
 522：軟體
 520：網路
 530：板
 1006：通訊晶片

申請專利範圍

1.一種積體電路結構，包含：

具有上表面的介電層，該介電層包含矽、氧及碳；以及

在該介電層中的導電結構，該導電結構包含：

包含銅的第一導電材料，該第一導電材料具有上表面，該第一導電材料之該上表面的一部份在該介電層之該上表面的一部份下方；以及

在該第一導電材料之該上表面上的第二導電材料，該第二導電材料包含鈷，其中該第一導電材料與該第二導電材料於該第一導電材料及該第二導電材料交會之位置具有相同寬度，其中該第二導電材料具有上表面，該上表面具有一部份為實質上與該介電層之該上表面的一部份共平面，且其中該第二導電材料之該上表面具有彎曲角於該介電層之該上表面的該部份下方；以及

部分地圍繞該導電結構的障壁層，該障壁層包含鉭。

2.如申請專利範圍第 1 項之積體電路結構，其中該障壁層更包含氮。

3.如申請專利範圍第 1 項之積體電路結構，其中該第二導電材料更包含硼。

4.如申請專利範圍第 3 項之積體電路結構，其中該第二導電材料更包含磷。

5.如申請專利範圍第 3 項之積體電路結構，其中該第二導電材料更包含鎢。

6.如申請專利範圍第 3 項之積體電路結構，其中該第二導電材料更包含鎢及磷。

7.如申請專利範圍第 1 項之積體電路結構，其中該第二導電材料更包含磷。

8.如申請專利範圍第 7 項之積體電路結構，其中該第二導電材料更包含鎢。

9.一種製造積體電路結構的方法，該方法包含下列步驟：

形成包含有矽、氧及碳的介電層；

形成溝槽於該介電層中；

形成障壁層於該溝槽中，該障壁層包含鋁；

形成第一導電材料於該障壁層中，該第一導電材料包含銅；

使該第一導電材料凹入至該介電層之上表面的一部份的下方；以及

形成第二導電材料在該凹入第一導電材料之該上表面上，該第二導電材料包含鈷，其中該第一導電材料與該第二導電材料於該第一導電材料及該第二導電材料交會之位置具有相同寬度，且其中該第二導電材料之該上表面具有彎曲角於該介電層之該上表面的該部份下方。

10.如申請專利範圍第 9 項之方法，其中使該第一導電材料凹入至該介電層之該上表面的該部份的下方之步驟包含使用濕式蝕刻程序。

11.如申請專利範圍第 9 項之方法，其中該障壁層更

包含氮。

12.如申請專利範圍第 9 項之方法，其中該第二導電材料更包含硼。

13.如申請專利範圍第 12 項之方法，其中該第二導電材料更包含磷。

14.如申請專利範圍第 12 項之方法，其中該第二導電材料更包含鎢。

15.如申請專利範圍第 12 項之方法，其中該第二導電材料更包含鎢及磷。

16.如申請專利範圍第 9 項之方法，其中該第二導電材料更包含磷。

17.如申請專利範圍第 16 項之方法，其中該第二導電材料更包含鎢。

18.一種防止電遷移之裝置，包含：
 基材；
 該基材之上的介電層；
 在該介電層中的至少一溝槽，該溝槽具有介電側壁；
 在該至少一溝槽中的導電材料，該導電材料包含銅及鈷，

在該導電材料及在位於該導電材料之上的所述介電側壁的部份上的覆蓋區域，其中該覆蓋區域包含面向該導電材料的圓形角部位。

19.如申請專利範圍第 18 項之裝置，其中鄰近該介電層的該覆蓋區域的頂部不高於鄰近該覆蓋區域的該介電層

的頂部邊界。

20.如申請專利範圍第 18 項之裝置，其中該導電材料不高於位於鄰近該導電材料位置之該介電層的頂部邊界。

21.如申請專利範圍第 18 項之裝置，更包含：

障壁層，介於該導電材料與該至少一溝槽之所述介電側壁間。

22.如申請專利範圍第 18 項之裝置，其中該覆蓋區域包含鈷。

23.如申請專利範圍第 18 項之裝置，其中該介電層包含低 k 值材料。

24.如申請專利範圍第 18 項之裝置，其中該介電層包含矽、氧及碳。

25.如申請專利範圍第 18 項之裝置，其中該基材包含半導體材料。

26.如申請專利範圍第 18 項之裝置，其中該導電材料為互連之一部分。

27.如申請專利範圍第 18 項之裝置，其中該介電層包含碳摻雜矽氧化物。

28.一種資料處理系統，包含

晶片，包括有包含基材的電子裝置；

該基材之上的介電層；

在該介電層中的至少一溝槽，該溝槽具有介電側壁；

在該至少一溝槽中的導電材料，該導電材料包含銅及鈷；以及

在該導電材料及在位於該導電材料之上的所述介電側壁的部份上的覆蓋區域，其中該覆蓋區域包含面向該導電材料的圓形角部位。

29.如申請專利範圍第 28 項之資料處理系統，其中鄰近該介電層的該覆蓋區域的頂部不高於鄰近該覆蓋區域的該介電層的頂部邊界。

30.如申請專利範圍第 28 項之資料處理系統，其中該導電材料不高於位於鄰近該導電材料位置之該介電層的頂部邊界。

31.如申請專利範圍第 28 項之資料處理系統，其中該電子裝置更包含介於該導電材料與該至少一溝槽之所述介電側壁間的障壁層。

32.如申請專利範圍第 28 項之資料處理系統，其中該覆蓋區域包含鈷。

33.如申請專利範圍第 28 項之資料處理系統，其中該介電層包含低 k 值材料。

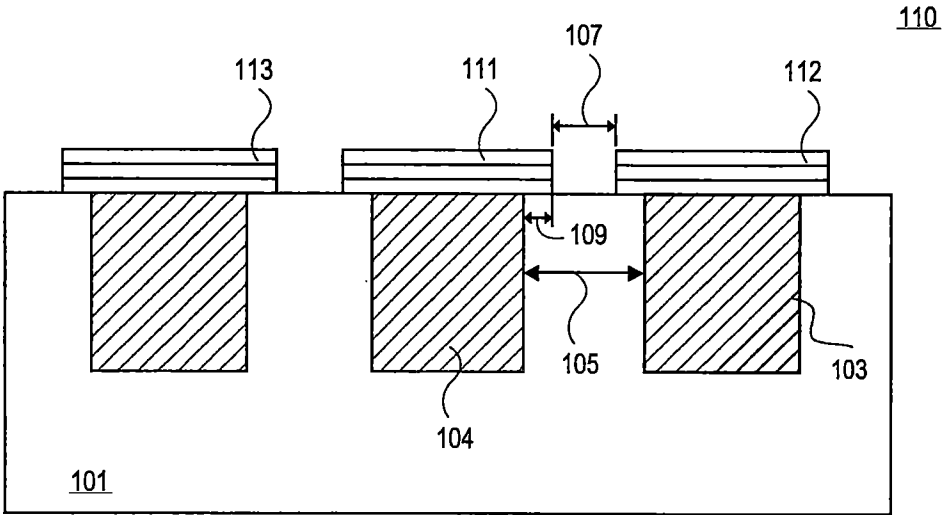
34.如申請專利範圍第 28 項之資料處理系統，其中該介電層包含矽、氧及碳。

35.如申請專利範圍第 28 項之資料處理系統，其中該基材包含半導體材料。

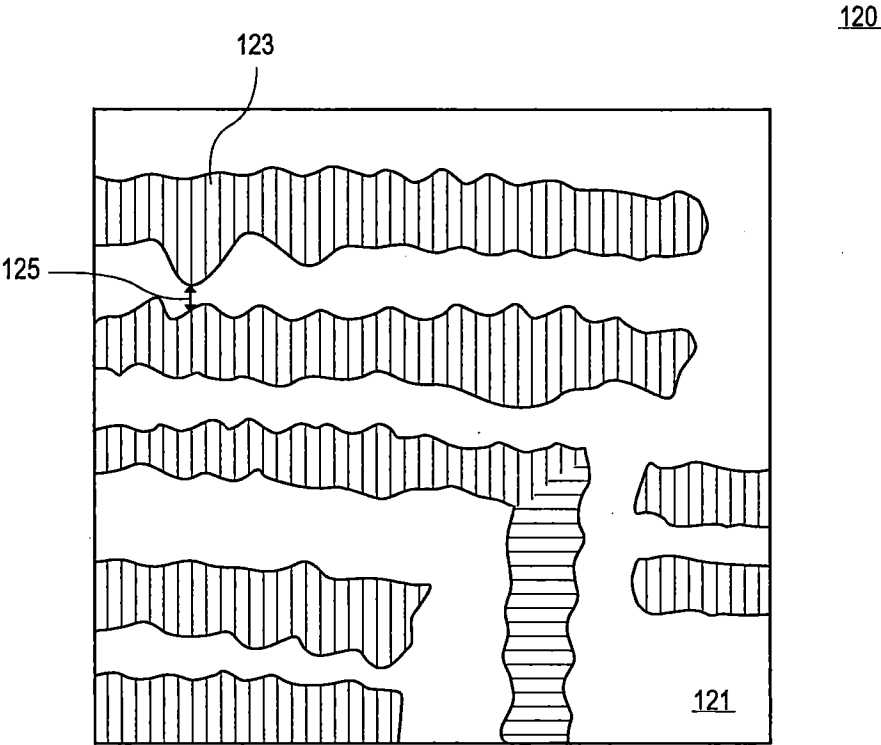
36.如申請專利範圍第 28 項之資料處理系統，其中該導電材料為互連之一部分。

37.如申請專利範圍第 28 項之資料處理系統，其中該介電層包含碳摻雜矽氧化物。

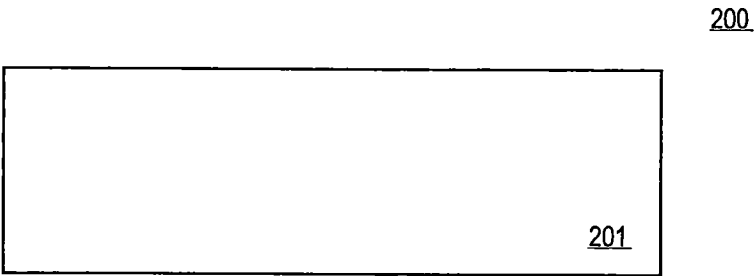
圖 式



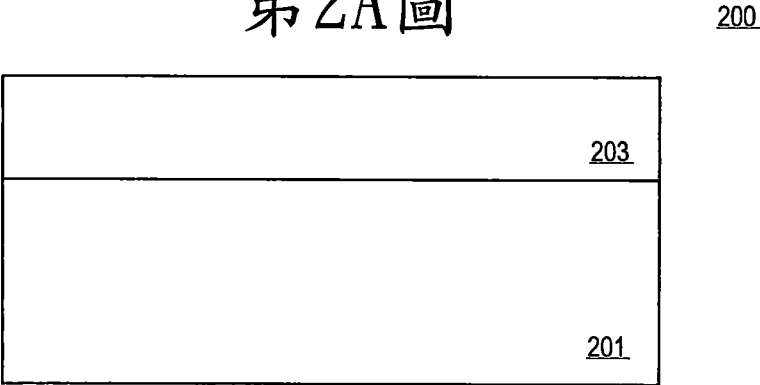
第1A圖
(先前技術)



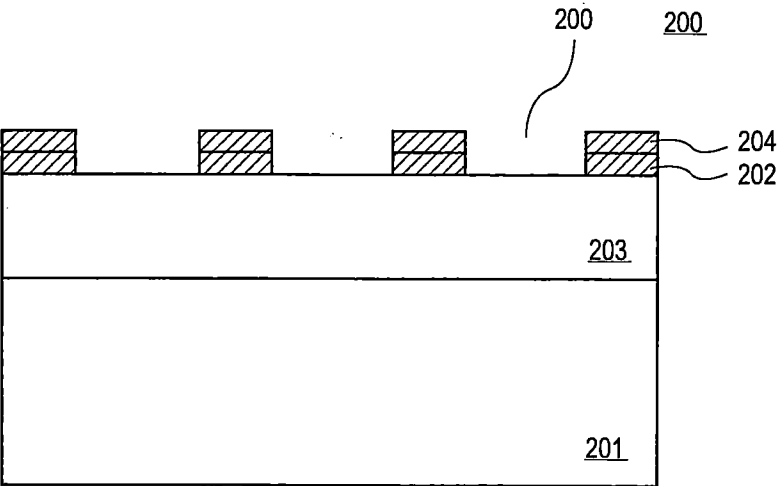
第1B圖
(先前技術)



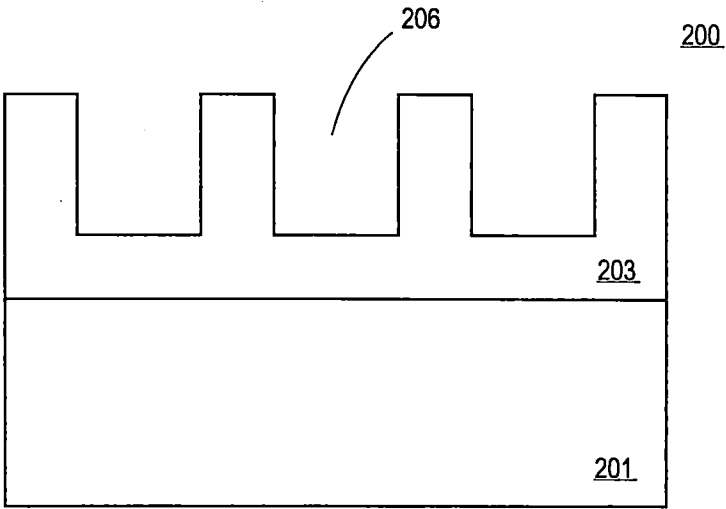
第2A圖



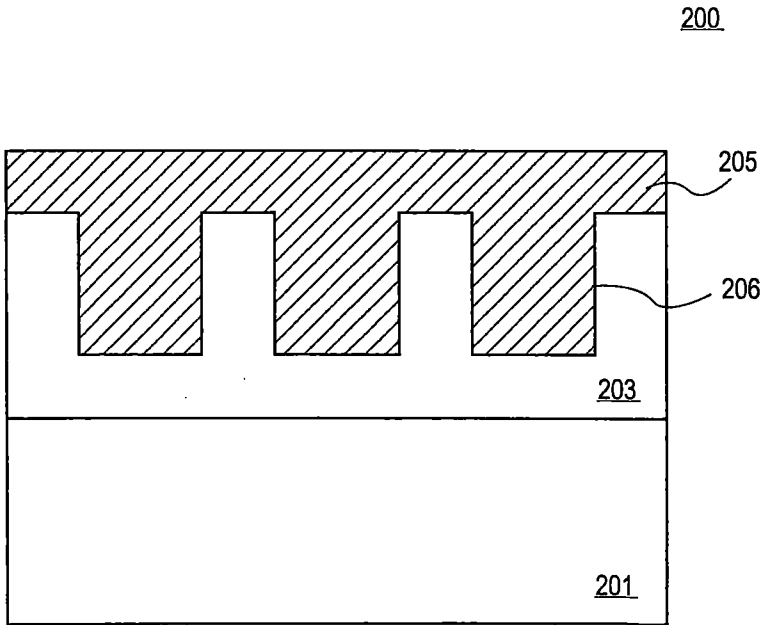
第2B圖



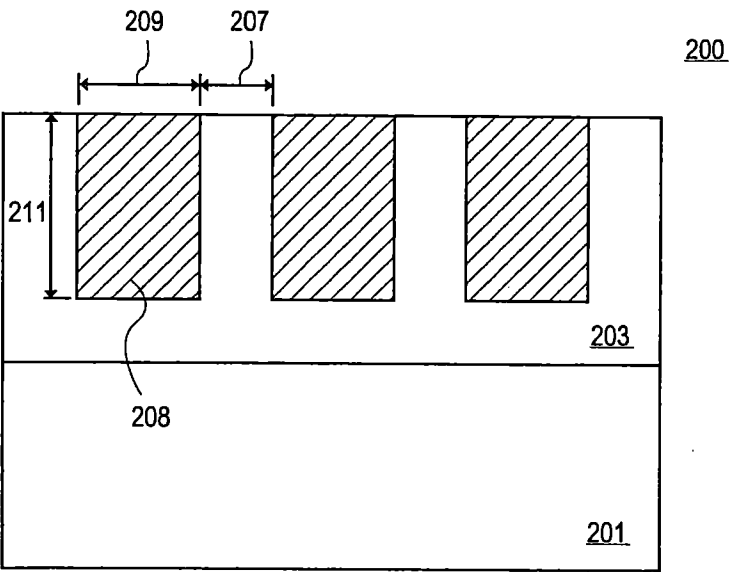
第2C圖



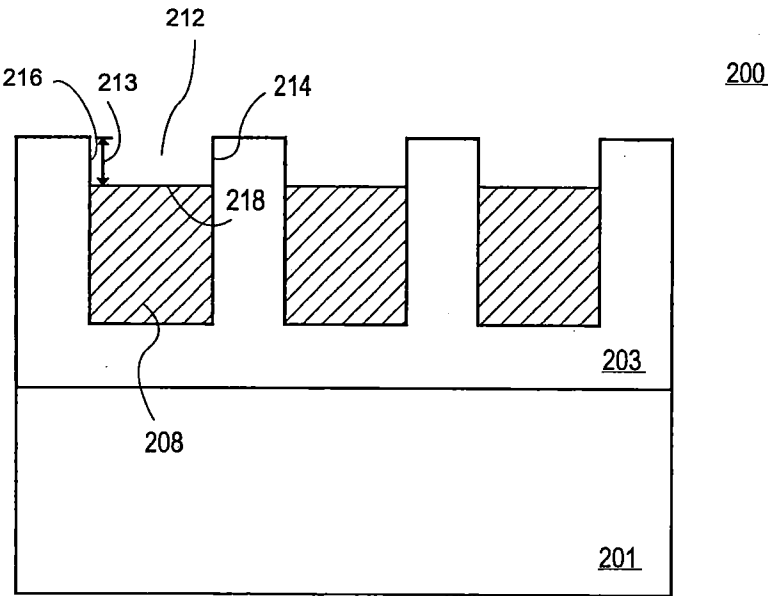
第2D圖



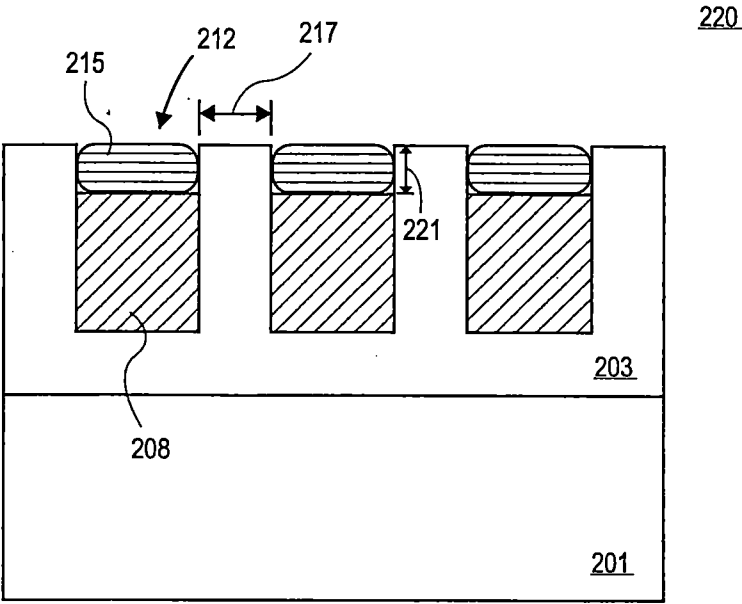
第2E圖



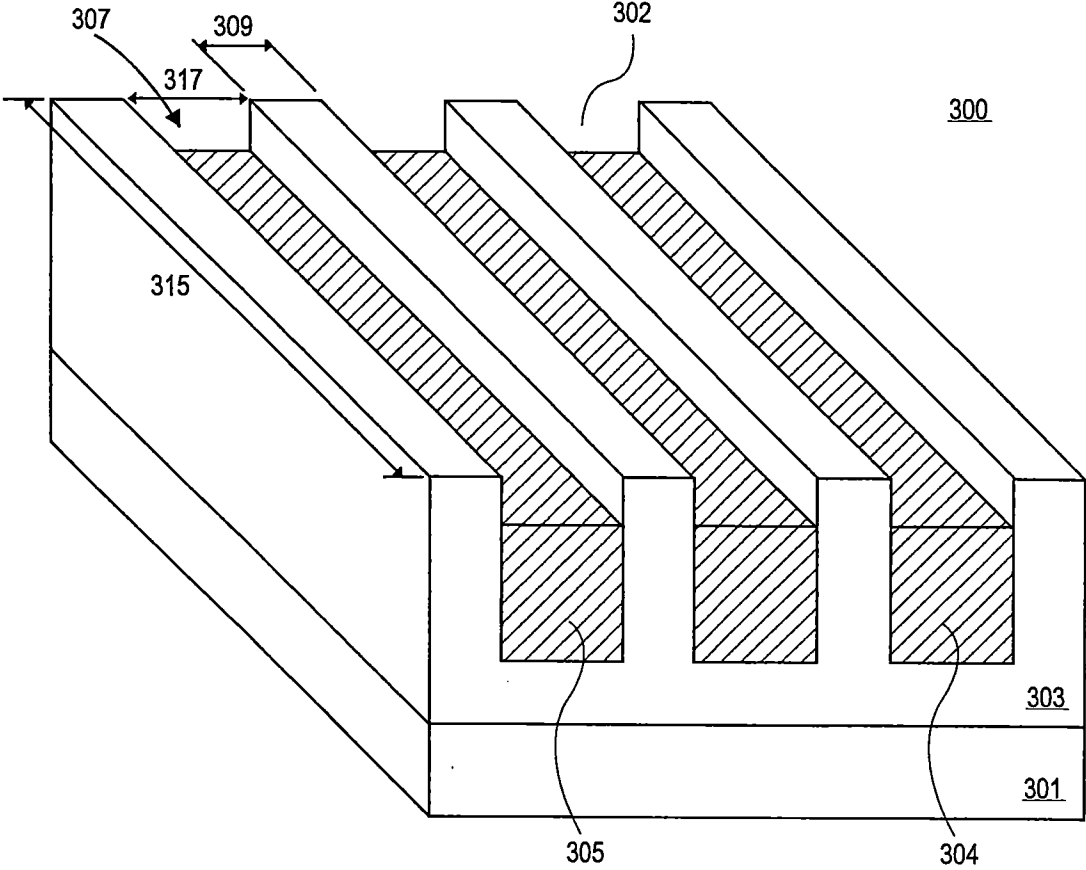
第2F圖



第2G圖

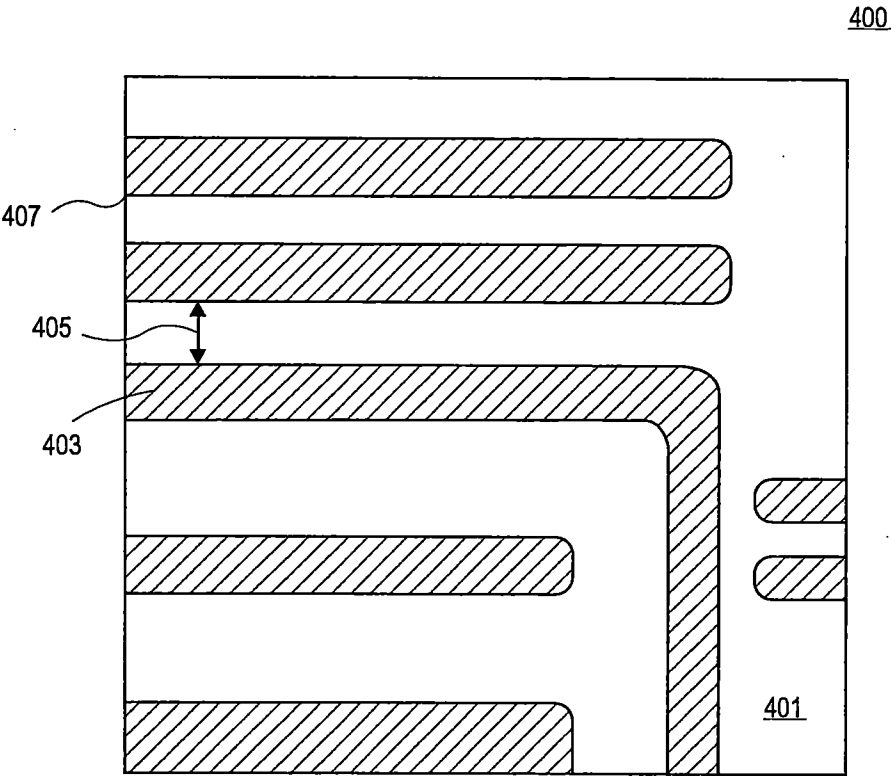


第2H圖

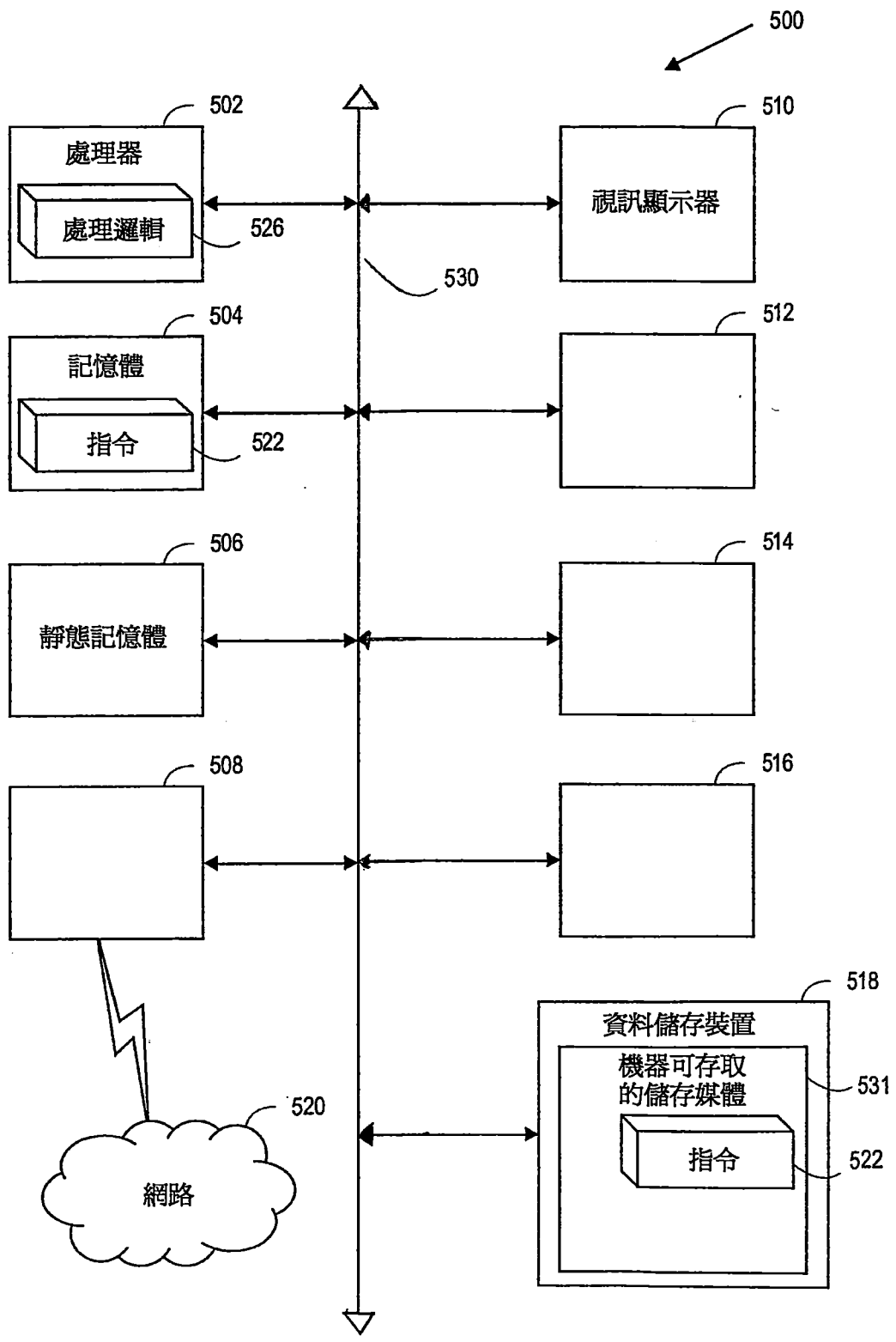


第3A圖





第4圖



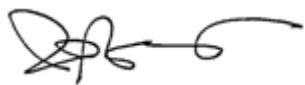
第5圖

I, Jian Zhang, declare as follows:

1. I am a native speaker of Chinese and am well versed in both the Chinese and English languages and have over 20 years of experience translating Chinese technical documents into English.
2. The following translation of the corresponding source text from Chinese into English is accurate and complete to the best of my knowledge.

I declare under penalty of perjury of the laws of the United States of America that the foregoing information is true and accurate to the best of my knowledge. Statements made herein are to the best of my knowledge true and are based on information that I believe to be true and further these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the patent application in the United States of America or any patent issuing thereon.

Executed on: November 28, 2022, at 6076 S. Paris St., Greenwood Village, CO 80111



Signed by Jian Zhang