UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293

CONFIRMATION NO. 2892

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

POWER OF ATTORNEY NOTICE

OC000000131237689

Date Mailed: 01/21/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/14/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tmwilliams/

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/477,506	04/03/2017	Boyan Boyanov	D0480-PA-13290-US-03

CONFIRMATION NO. 2892

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

POA ACCEPTANCE LETTER

OC000000131237709

Date Mailed: 01/21/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/14/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/tmwilliams/

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	15/477,506
Filing Date	April 3, 2017
First Named Inventor	Boyan Boyanov
Title	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
Art Unit	2898
Examiner Name	Joseph M. Galvin, III
Attorney Docket Number	D0480-PA-13290-US-03

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	January 14, 2022
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
15/477,506	April 3, 2017

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	
Name	Lisa Hopkinson		
Title	Administrator of Patents		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☑ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	44748743
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	14-JAN-2022
Filing Date:	03-APR-2017
Time Stamp:	13:09:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2022-01-14_POA_D0480-PA-13290-US-03.pdf	1255628 3452739b566ccfe2e15c8e49c6804a5c00d73bdc	no	2

Warnings:

Information:	
Total Files Size (in bytes):	1255628

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	10/15/2019	10446493	P38794USDC 111548-227293	2892

31817 7590 09/25/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 142 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Boyan Boyanov, Portland, OR;
INTEL CORPORATION, Santa Clara, CA;
Kanwal Jit Singh, Hilsboro, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	FORTICH, RODOLFO D
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

Change(s) applied to document, /K.W./ 8/2/2019

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 7,396,757	07-08-2008	~~IBM CORP~~ Yang	
		US6,908,847	06-21-2005	SAITO, TATSUYUKI, ET AL.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		KR-1020090085066	08-06-2009	IBM		X
		CN-101490825A	07-22-2009	IBM		X
		CN-1420560	05-28-2003	HITACHI LTD		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		4th Non-Final Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) mailed September 12, 2017, 7 pgs., with English translation.	X
		1st Non-Final Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CND) mailed August 28, 2017, 10 pgs., with English translation.	X
		Final Office Action for Korean Patent Application 10-2016-7033745 (Attorney Docket No. P38794KRD2) mailed July 18, 2017, 5 pgs., with English translation.	x

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

Based on PTO/SB/08A(08-08) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

PTO/SB/47 (03-09)
Approved for use through 03/31/2012. OMB 0651-0016
U.S. Patent and Trademark Office; U. S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

- OR -

Fax to:
571-273-6500

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below**: If you have a Customer Number to represent the fee address. **When to check the second box below**: If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:

☑ Customer Number: 000197

OR

☐ The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	15/477,506

Completed by (check one):

☐ Applicant/Inventor

☑ Attorney or Agent of record 35934 (Reg. No.)

☐ Assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☐ Assignee recorded at Reel _____ Frame_____

/Michael A. Bernadicou/
Signature

Michael A. Bernadicou
Typed or printed name

503-222-9981
Requester's telephone number

9/4/2019
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more that one signature is required, see below*.

☑ * **Total of** 1 **forms are submitted.**

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1. 11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313- 1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.
SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	15477506
Filing Date:	03-Apr-2017
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Attorney Docket Number:	P38794USDC 111548-227293

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1000**

Electronic Acknowledgement Receipt	
EFS ID:	37060351
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	04-SEP-2019
Filing Date:	03-APR-2017
Time Stamp:	19:56:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1000
RAM confirmation Number	E201994J57146279
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	P38794USDC_Issue_Fee_09-04-19.pdf	97319 5ca58baab0eefc2e6b2bd7fe4b1ef15ef03f4df3	no	1
Warnings:					
Information:					
2	Maintenance Fee Address Change	P38794USDC_Maintenance_Fees.pdf	312404 9cb874981c7702bcf13d89d64ea22a621ef1510c	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30448 efad5d77e47e6d007b5cc3252e117a077c04866f	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	440171		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 06/12/2019
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Lisa Puccinelli	(Typed or printed name)
/Lisa Puccinelli/	(Signature)
September 4, 2019	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293	2892

TITLE OF INVENTION: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	09/12/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
GALVIN III, JOSEPH M	2898	257-773000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
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1 Schwabe, Williamson & Wyatt, P.C.
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

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Intel Corporation	Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

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5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
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NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Michael A. Bernadicou/ Date September 4, 2019

Typed or printed name Michael A. Bernadicou Registration No. 35934

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293	2892

31817 7590 08/07/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
GALVIN III, JOSEPH M	

ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
08/07/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

(corrected) ***Notice of Allowability***	**Application No.** 15/477,506	**Applicant(s)** Boyanov et al.	
	Examiner JOSEPH M GALVIN III	**Art Unit** 2898	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to IDS filed 06/27/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-7 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☑ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 06/27/2019.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/JOSEPH M GALVIN III/
Primary Examiner, Art Unit 2898

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		CN 101064295	10/31/2007	Zhang Gong Chen et al.		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		Office Action from Chinese Patent Application No. 201711404006.5 (Attorney Docket No. P38794CN-D-D1) mailed June 4, 2019, 10 pages.	
		Office Action from Korean Patent Application No. 10-2019-7002805 (Attorney Docket No. P38794KR-D2-D2-D1) mailed March 27, 2019, 3 pgs.	

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	08/01/2019

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
		CN 101064295	10/31/2007	Zhang Gong Chen et al.		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
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EXAMINER **DATE CONSIDERED**

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Bibliographic data: CN101064295 (A) — 2007-10-31

Semiconductor device and its making method

Inventor(s): ZHANG GONG CHEN [CN] ± (GONG,CHEN ZHANG, ; ZHANG GONG, ; CHEN YUWEN, ; BEI DUOHUI, ; SUN ZHIJIANG)

Applicant(s): SEMICONDUCTOR MFG INT SHANGHAI [CN] ± (SEMICONDUCTOR MANUFACTURING INTERNATIONAL (SHANGHAI) CORPORATION)

Classification: **- international:** ***H01L21/768; H01L23/522***
- cooperative:

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Priority number(s): CN20061026326 20060430

Also published as: CN100468718 (C)

Abstract of CN101064295 (A)

The invention provides semiconductor component and preparing method. The semiconductor component possesses a top metal layer and a lower metal layer which is electric connected with the top metal layer via the middle medium layer. The method firstly covers etch stopping layer on the underlay which possesses metal pattern, its thickness is 100-300 angstrom, covering the blocking layer whose thickness is two times of etch stopping layer on the etch stopping layer, covering middle medium layer on the blocking layer and etching the groove and through hole which are needed by depositing top metal, thereinto existence of the blocking layer avoids peeling off of the etch stopping layer and the middle medium layer.

[19] 中华人民共和国国家知识产权局

[51] Int. Cl.
H01L 23/522 (2006.01)
H01L 21/768 (2006.01)

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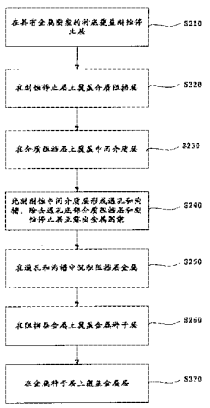
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代理人 逯长明
权利要求书 2 页 说明书 7 页 附图 6 页

[54] 发明名称

半导体器件及其制造方法

[57] 摘要

本发明提供一种半导体器件及其制造方法。该半导体器件具有一个顶层的金属层以及一个通过中间介质层通孔电连接至顶层金属层的下层金属层。本发明的制造方法为先在具有金属图案的衬底上覆盖刻蚀停止层，其厚度为 100～300 埃，在刻蚀停止层上覆盖厚度约为刻蚀停止层 2 倍的阻挡层，在阻挡层上覆盖中间介质层并通过光刻刻蚀出沉积顶层金属所需的沟槽和通孔，其中阻挡层的存在避免了刻蚀停止层与中间介质层剥离现象的发生。



1、一种半导体器件，其特征在于包括：

衬底；在衬底上形成的介质层和形成于所述介质层中的金属图案层；

在所述介质层和金属图案层上形成的刻蚀停止层；

在所述刻蚀停止层上形成的阻挡层；

在所述阻挡层上形成的中间介质层；所述中间介质层上具有沟槽和通孔，在所述沟槽和通孔中依次填充有金属阻挡层，金属种子层和互连金属层。

2、如权利要求 1 所述的半导体器件，其特征在于：所述的刻蚀停止层的厚度为 100 埃～300 埃。

3、如权利要求 1 所述的半导体器件，其特征在于：所述的阻挡层的厚度为 200 埃～600 埃。

4、如权利要求 2 所述的半导体器件，其特征在于：所述的刻蚀停止层至少为氧化硅、碳化硅（SiC）、氮化硅（SiN）、碳氮氧化合物（SiOC）、掺氮碳化硅中的一种或其组合。

5、如权利要求 3 所述的半导体器件，其特征在于：所述的阻挡层至少为氧化硅、碳化硅（SiC）、氮化硅（SiN）、碳氮氧化合物（SiOC）、掺氮碳化硅中的一种或其组合。

6、如权利要求 1 所述的半导体器件，其特征在于：所述的中间介质层至少为氟硅玻璃（FSG）、磷硅玻璃(PSG)、硼硅玻璃（BSG）、硼磷硅玻璃（BPSG）、氧化硅、氮化硅（SiN）、碳化硅（SiC）中的一种或其组合。

7、如权利要求 1 所述的半导体器件，其特征在于：所述的中间介质层上的沟槽的深度小于通孔的深度。

8、如权利要求 1 所述的半导体器件，其特征在于：所述的金属阻挡层为钛（Ti）、钨（W）、钽（Ta）、钼（Mo）、钴（Co）、铂（Pt）、钛钨（TiW）、氮化钛（TiN）、氮化钽（TaN）中的一种或其组合。

9、如权利要求 1 所述的半导体器件，其特征在于：所述的金属种子层为铜、铝、钨、金或银。

10、如权利要求 1 所述的半导体器件，其特征在于：所述的互连金属层包括铜或铝。

11、如权利要求 1 所述的半导体器件，其特征在于：所述的通孔位于金属图案上方相对应的位置。

12、如权利要求 1 所述的半导体器件，其特征在于：所述的通孔中的互连金属层通过所述的金属种子层和金属阻挡层与所述的衬底上的所述的金属图案电连接。

13、一种半导体器件的制造方法，其特征在于包括：

提供一半导体衬底，在衬底上形成介质层和金属图案层；

在所述介质层和金属图案层上形成刻蚀停止层；

在所述刻蚀停止层上形成一个阻挡层；

在所述阻挡层上形成中间介质层；

刻蚀所述中间介质层、阻挡层和刻蚀停止层形成通孔以露出所述金属图案，并在所述中间介质层形成沟槽；

在所述沟槽和通孔中依次填充金属种子层、金属阻挡层和互连金属层。

14、如权利要求 13 所述的半导体器件的制造方法，其特征在于：所述刻蚀停止层和阻挡层的形成方法包括物理气相沉积（PVD）或化学气相沉积(CVD)。

15、如权利要求 13 所述的半导体器件的制造方法，其特征在于：所述化学气相沉积包括常压化学气相沉积（APCVD)、低压化学气相沉积(LPCVD)、离子体增强化学气相沉积（PE CVD)、高密度等离子体化学气相沉积(HDPCVD)。

16、如权利要求 13 所述的半导体器件的制造方法，其特征在于：所述刻蚀停止层的厚度为 100 埃～300 埃。

17、如权利要求 13 所述的半导体器件的制造方法，其特征在于：所述阻挡层的厚度为 200 埃～600 埃。

18、如权利要求 13 所述的半导体器件的制造方法，其特征在于：所述中间介质层的形成方法包括物理气相沉积，化学气相沉积。

19、如权利要求 13 所述的半导体器件的制造方法，其特征在于：所述金属阻挡层利用物理气相沉积或电镀方法形成。

半导体器件及其制造方法

技术领域

本发明涉及半导体制造技术领域，特别涉及一种半导体器件及其制造方法。

背景技术

半导体技术发展要求越来越高集成度的同时，对线宽及工艺的要求也越来越苛刻。在向小线宽技术节点迈进的同时，IC 业界选用铜和低K材料作为减小 0.13um及其以下技术节点的互连电阻电容（RC） 延迟的关键解决方法，相对于铝金属工艺中蚀刻去除铝的过程,铜具有易扩散、难刻蚀等特点，业界引入了双镶嵌工艺（Dual Damascene），其特点就是先在带有器件的衬底上形成中间介质层并刻蚀出沟槽和通孔，然后淀积铜进入刻蚀好的图形中，并应用平坦化方法除去多余的铜。

通常情况下在半导体器件后段顶层金属制作中，其工艺步骤一般为在形成带有金属图形的衬底上，淀积刻蚀停止层，中间介质层，铜扩散阻止层，铜淀积层，然后化学机械研磨。因此，相应的开发与双镶嵌工艺兼容的介质材料如刻蚀停止层，中间介质层材料就成为迫切需要。铜和低K材料的工艺整合是具有挑战性的。

相对于介电常数比较大的SIN(K~7.8) 和SION（K～7），现有技术中一般采用介电常数小的SIC（K~5）作为刻蚀停止层，采用化学气相淀积方法淀积氟硅玻璃(FSG) 作为中间介质层并在工艺中用高浓度的氟来减小其介电常数。但是高浓度的氟常常是不稳定的，会向两边的介质层或金属层扩散从而破坏其交界面的粘附性。专利申请号为99110641的中国专利公开了一种通过在FSG 上表面形成防止氟物质穿过其中的氧氮化硅的方法来解决FSG扩散至上层金属表面腐蚀金属并破坏FSG与金属的交界面粘附的问题，但是，高浓度氟对下层刻蚀停止层的破坏导致FSG与刻蚀停止层的粘附性变差并在顶层金属沉积后产生剥离的问题成为工艺人员关注的问题。

图1为现有技术中刻蚀停止层上直接覆盖中间介质层的示意图。如图1所示，在有金属图案110的衬底100上覆盖有刻蚀停止层120和中间介质层130，沟槽150和通孔140形成于中间介质层130上并在沟槽150和通孔140中填有金

属，例如铜。图2为现有技术中刻蚀停止层和其上层的中间介质层剥离的示意图。如图2所示，在铜制程中，非导电介质材料和其金属层与其它辅助介电层的粘附不免会有问题，由于中间介质层130和刻蚀停止层120粘附性不好产生剥离现象发生，剥离现象可发生在该器件生产过程中或器件生产完成后在对钝化层与外引线 (packaging wire bonding)粘附强度可靠性测试的时候。在生产过程中产生剥离，会导致后层金属层翘起，影响其电连接并最终导致器件电性失败；如果在生产过程中没有剥离，也会由于其粘附性能差而导致器件的寿命变短。

发明内容

因此，本发明的目的在于提供一种半导体器件及其制造方法，以解决顶层金属中间介质层与其下层刻蚀停止层粘附性差并产生剥离的问题。

为达到上述目的，本发明提供一种半导体器件，包括：

衬底；在衬底上形成的介质层和形成于所述介质层中的金属图案层；

在所述介质层和金属图案层上形成的刻蚀停止层；

在所述刻蚀停止层上形成的阻挡层；

在所述阻挡层上形成的中间介质层；所述中间介质层上具有沟槽和通孔，在所述沟槽和通孔中依次填充有金属阻挡层，金属种子层和互连金属层。

所述的刻蚀停止层的厚度为 100 埃～300 埃。

所述的阻挡层的厚度为 200 埃－600 埃。

所述的刻蚀停止层至少为氧化硅、碳化硅（SiC）、氮化硅（SiN）、碳氮氧化合物（SiOC）、掺氮碳化硅中的一种或其组合。

所述的阻挡层至少为氧化硅、碳化硅（SiC）、氮化硅（SiN）、碳氮氧化合物（SiOC）、掺氮碳化硅中的一种或其组合。

所述的中间介质层至少为氟硅玻璃（FSG）、磷硅玻璃(PSG)、硼硅玻璃（BSG）、硼磷硅玻璃（BPSG）、氧化硅、氮化硅（SiN）、碳化硅（SiC）中的一种或其组合。

所述的中间介质层上的沟槽的深度小于通孔的深度。

所述的金属阻挡层为钛（Ti）、钨（W）、钽（Ta）、钼（Mo）、钴（Co）、铂（Pt）、钛钨（TiW）、氮化钛（TiN）、氮化钽（TaN）中的一种或其组合。

所述的金属种子层为铜、铝、钨、金或银。

所述的互连金属层包括铜或铝。

所述的通孔位于金属图案上方相对应的位置。

所述的通孔中的互连金属层通过所述的金属种子层和金属阻挡层与所述的衬底上的所述的金属图案电连接。

相应地，本发明提供了一种半导体器件的制造方法，包括：

提供一半导体衬底，在衬底上形成介质层和金属图案层；

在所述介质层和金属图案层上形成刻蚀停止层；

在所述刻蚀停止层上形成一个阻挡层；

在所述阻挡层上形成中间介质层；

刻蚀所述中间介质层、阻挡层和刻蚀停止层形成通孔以露出所述金属图案，并在所述中间介质层形成沟槽；

在所述沟槽和通孔中依次填充金属种子层、金属阻挡层和互连金属层。

所述刻蚀停止层和阻挡层的形成方法包括物理气相沉积（PVD）或化学气相沉积(CVD)。

所述化学气相沉积包括常压化学气相沉积（APCVD)、低压化学气相沉积(LPCVD)、离子体增强化学气相沉积（PE CVD)、高密度等离子体化学气相沉积(HDPCVD)。

所述刻蚀停止层的厚度为 100 埃～300 埃。

所述阻挡层的厚度为 200 埃～600 埃。

所述中间介质层的形成方法包括物理气相沉积，化学气相沉积。

所述金属阻挡层利用物理气相沉积或电镀方法形成。

与现有技术相比，本发明具有以下优点：本发明通过在刻蚀停止层和中间介质层之间插入阻挡层，阻止了中间介质层中的氟向刻蚀停止层与中间介质层的扩散，从而减少了由于自由的氟扩散带来了对两层交界面的腐蚀和破坏，有助于增加上下两层在交界面的粘附；

另外，由于沉积过程中离子轰击对化学键的破坏和重组，会在沉积的介质膜中产生很高的应力，高的膜应力会导致开裂和分层，阻挡层 SiN 由于离子轰击破坏 Si-N 键，因而会有高的压应力，因而有助于平衡中间介质层材料氟硅玻璃(FSG)的张应力，从而减小了由于应力对于层与层之间的粘附的影响，增加了其粘附力。

附图说明

图 1 为现有技术中刻蚀停止层上直接覆盖中间介质层的示意图；

图 2 为现有技术中刻蚀停止层和其上层的中间介质层剥离的示意图；

图 3 为本发明半导体器件的结构剖面图；

图 4 为本发明半导体器件制造方法的工艺流程图；

图 5 至图 10 为说明本发明半导体器件制造方法的剖面图。

具体实施方式

为使本发明的上述目的、特征和优点能够更加明显易懂，下面结合附图对本发明的具体实施方式做详细的说明。

图 3 为本发明半导体器件的结构剖面图。如图 3 所示，本发明的半导体器件包括一个衬底 100 和形成于所述衬底 100 上介质层 105 中的金属图案层 110，金属图案层 110 通过在介质层 105 上旋涂光致抗蚀剂（Photoresist）曝光显影并刻蚀而形成。在所述介质层 105 和金属图案层 110 上形成有刻蚀停止层 120，厚度为 100 埃～300 埃，其材料可以是氧化硅，碳化硅（SiC），氮化硅（SiN），碳氮氧化合物（SiOC），掺氮碳化硅中的一个或其组合。刻蚀停止层的作用是为了防止在刻蚀本层材料时不会破坏其下层图形。刻蚀停止层 120 作为其上层的材料刻蚀的终点停止层，能够保护其下层的金属图案 110 不会被刻蚀而形成缺陷。本发明的半导体器件在刻蚀停止层 120 上覆盖有厚度为 200 埃～600 埃阻挡层 125，选用的材料可以是氧化硅、碳化硅（SiC），氮化硅（SiN），碳氮氧化合物（SiOC），掺氮碳化硅中的一个或其组合。在阻挡层 125 上沉积有低介电常数材料的中间介质层 130，与互连金属如铜匹配减小其寄生电容和互联金属电阻造成的电阻电容（RC）延迟，可选的材料包括氟硅玻璃（FSG），磷硅玻璃(PSG)，硼硅玻璃（BSG），硼磷硅玻璃（BPSG）。

中间介质层 130 上有通过涂布光致抗蚀剂，曝光显影把掩模板的图形转移到中间介质层 130 上而形成的通孔 140 和沟槽 150，沟槽 150 的深度小于通孔 140 的深度，两者是否连接取决于器件决定的电连接的需要。在通孔 140 和沟槽 150 中依次覆盖有金属阻挡层 160，金属种子层 170，互连金属层 180，金属阻挡层包括钛（Ti），钨（W），钽（Ta），钼（Mo），钴（Co），铂（Pt），钛钨（TiW），氮化钛（TiN），氮化钽（TaN）中的一种或其组合，金属种子层包括铜、铝、钨、金、或银，互连金属层包括铜或铝。通孔 140 底部与衬底

100 上的金属图案 110 相连。

沉积的阻挡层 125 可以增加中间介质层 130 和刻蚀停止层 120 的粘附性，例如，阻挡层 125 材料为 SiN，中间介质层 130 材料对于顶层金属一般选用氟硅玻璃（FSG），FSG 中的氟具有很强的扩散效应，由于为了减小介质层材料介电常数从而减小其寄生电容与互连金属电阻的电阻电容（RC）延迟，在沉积 FSG 是往往选用高浓度的氟，高浓度的氟是不稳定的，其会向上下层扩散，氟对交界面的腐蚀会减小其粘附性，会造成层与层的剥离，SiN 是很好的氟的阻挡层，N 的含量越高，氟的扩散越少发生，引入阻挡层材料可以有效阻挡其扩散，减小其对表面的腐蚀，增加了粘附性能。

另外，沉积的低介电常数材料 FSG 会有张应力，介质膜中的高的应力会导致分层，沉积阻挡层材料 SiN 采用等离子体增强化学气相沉积，沉积过程中高速离子对 SiN 中离子键的破坏会使沉积的 SiN 膜有很高的压应力（Compressive stress），有助于平衡 FSG 中的张应力对其下层膜的影响从而减小应力带来的分层现象。

图 4 为本发明半导体器件制造方法的工艺流程图。如图 4 所示，本发明的半导体器件的制造方法。首先，在具有金属图案 110 的衬底 100 上覆盖刻蚀停止层 120（S210）；然后，在刻蚀停止层 120 上通过气相沉积淀积阻挡层 125（S220）；接着，在阻挡层 125 上覆盖中间介质层 130（S230）；通过光刻、刻蚀在中间介质层 130 上形成通孔 140 和沟槽 150，并打开通孔 140 底部的阻挡层 125 和刻蚀停止层 120，使通孔 140 底部露出衬底 100 上的金属图案 110(S240)；最后，在通孔 140 和沟槽 150 中覆盖金属阻挡层 160（S250）；在金属阻挡层 160 上覆盖金属种子层 170（S260）；在金属种子层 170 上填充互连金属层 180（S270）。

图 5 至图 10 为说明本发明半导体器件制造方法的剖面图。下面结合图 5 至图 10 详细描述实现该方法的工艺步骤。如图 5 所示，本发明在衬底 100 首先形成一个介质层 105 和通过光刻、刻蚀并沉积金属，例如铜，形成的金属图案 110。

接着，如图 6 所示，在衬底 100 和金属图案 110 上沉积一刻蚀停止层 120，沉积的方法可以是等离子体增强化学气相沉积。优选的，沉积的厚度为 100 埃至 300 埃，沉积的材料可以是掺氮碳化硅，硅的氧化物，碳化硅（SiC），

氮化硅（SiN），碳氮氧化合物（SiOC）中的一个或其组合。该刻蚀停止层 120 作为保护下层金属图案 110 在上层刻蚀时不受损伤的阻挡材料并可以作为下层金属的扩散阻挡层，以阻挡下层金属图案中的金属如铜不会扩散至上层中。如本领域的技术人员所知铜作为后段的互连金属具有很强的扩散效应，因而刻蚀停止层也有作为阻挡下层金属扩散的作用。本发明的半导体器件制造方法在刻蚀停止层 120 上不是直接积淀上层介质层来完成对非导电介电层的沉积，而是在沉积刻蚀停止层 120 后，在刻蚀停止层 120 上通过物理气相淀积（PVD）或化学气相淀积沉积一层阻挡层 125，该阻挡层 125 的厚度为 200 埃～600 埃，该阻挡层的材料可以是高密度和高应力的氮化硅（SiN）或其他有机材料、无机材料、金属，或者至少包括硅的氧化物、碳化硅（SiC），碳氮氧化合物（SiOC）中的一个或其组合。在完成阻挡层 125 的沉积后，在其上沉积中间介质层 130，由于中间介质层需选用介电常数小的材料，本实施例中优选的使用化学气相沉积的方法淀积氟硅玻璃(FSG)，其中，通常氟的浓度高，其介电常数会小，本实施例中使其介电常数约为 3.7。其它可选的材料包括氟硅玻璃（FSG），磷硅玻璃(PSG)，硼硅玻璃（BSG）或硼磷硅玻璃（BPSG）。沉积的阻挡层 125 可阻止中间介质层 130 中氟的扩散并减小 FSG 的张应力影响，增加了刻蚀停止层 120 和中间介质层 130 的粘附性能，减小了两层之间分层、剥离等缺陷。

完成在带有金属图案的衬底上沉积刻蚀停止层 120、阻挡层 125 和中间介质层 130 后，如图 7 所示，在中间介质层上涂布光致抗蚀剂 135 通过曝光显影形成图案 136，定义连接孔，露出下层的中间介质层 130，图案 136 的位置与衬底 100 上金属图案 110 的位置相对应。然后，如图 8 所示，刻蚀该中间介质层 130，在刻蚀过程中光致抗蚀剂作为刻蚀的阻挡层保护其下层的中间介质层 130 的被光致抗蚀剂覆盖位置，中间介质层 130 连接孔位置由于露出所以会被刻蚀，通过干法或湿法刻蚀，在中间介质层 130 上形成通孔 140。刻蚀在露出中间介质层 130 下层阻挡层 125 时停止，可以看出，阻挡层 125 也作为中间介质层 130 的刻蚀停止层。通过灰化(Ashing)和清洗（strip）去除光致抗蚀剂 135，就形成了在中间介质层 130 上的通孔 140。如图 9 所示，用和上述相同的方法在中间介质层 130 上形成沟槽 150，沟槽 150 的深度小于通孔 140 的深度，也即沟槽 150 的底部不会露出中间介质层 130 下层的阻挡层 125，

沟槽 150 是否跟通孔 140 相连取决于沟槽 150 和通孔 140 沉积的金属的电连接需要。然后继续刻蚀并清洗除去通孔 140 下面阻挡层 130 和刻蚀停止层 125，使衬底上的金属图案 110 可以通过通孔 140 露出。

如图 10 所示，在形成的沟槽 150 和通孔 140 中填入金属，如铜，由于铜离子的扩散效应，如果不对其进行相应的处理，填入到通孔 140 和沟槽 150 中的铜就会扩散至其相邻的介质层如中间介质层 130，就会改变介质层的绝缘效果并引入其他的寄生效应，影响器件的性能。因而有必要对其进行适当的处理，通常会先淀积扩散阻挡层（Diffusion Barrier），在所述的通孔 140 和沟槽 150 种通过合适的方法如物理气相沉积或化学气相沉积淀积一层金属阻挡层 160，其材料可以是氮化钛（TiN），钛（Ti），钨（W），钽（Ta），钼（Mo），钴（Co），铂（Pt），钛钨（TiW），氮化钽（TiN）中的一种或其组合。加入金属阻挡层 160 可以很好的阻止金属铜对介质层的扩散，并可增强金属铜和其介质层的粘附性。在金属阻挡层 160 上积淀金属种子层（Metal seed）170 和互连金属层 180，其淀积可以是物理气相沉积、化学气相沉积或电镀。淀积的金属层的厚度至少填满整个通孔 140 和沟槽 150。

本发明虽然以较佳实施例公开如上，但其并不是用来限定本发明，任何本领域技术人员在不脱离本发明的精神和范围内，都可以做出可能的变动和修改，因此本发明的保护范围应当以本发明权利要求所界定的范围为准。

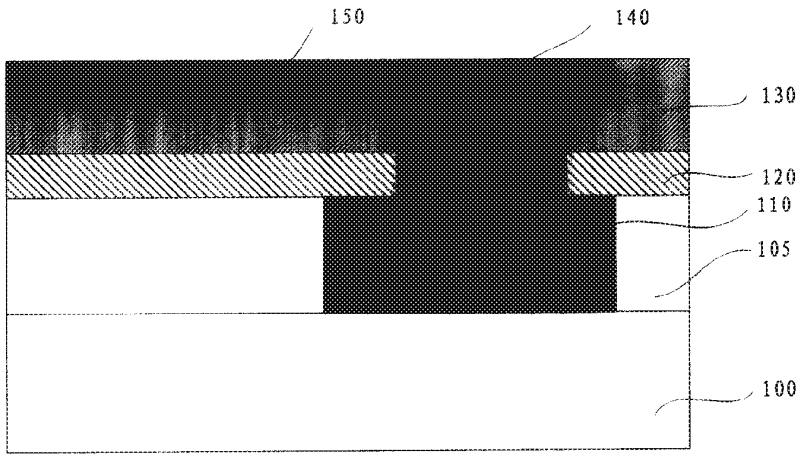


图 1

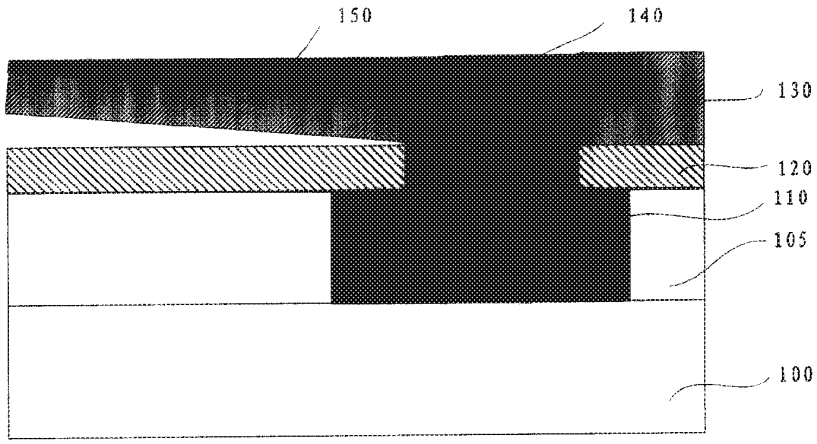


图 2

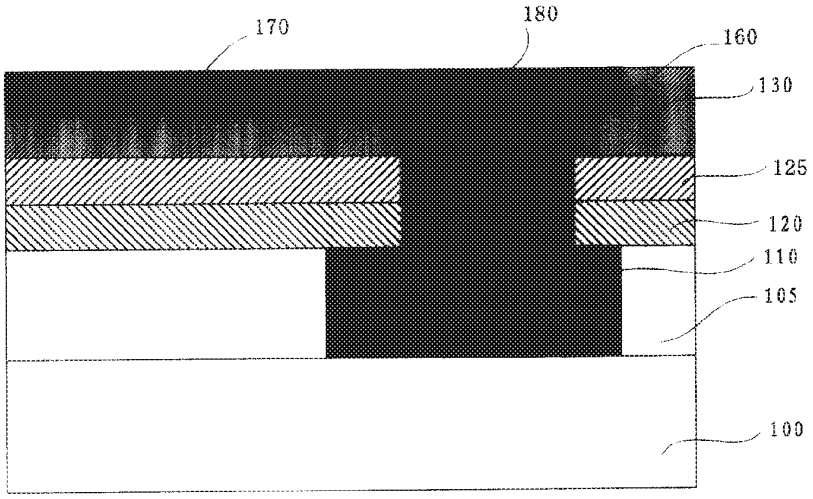


图 3

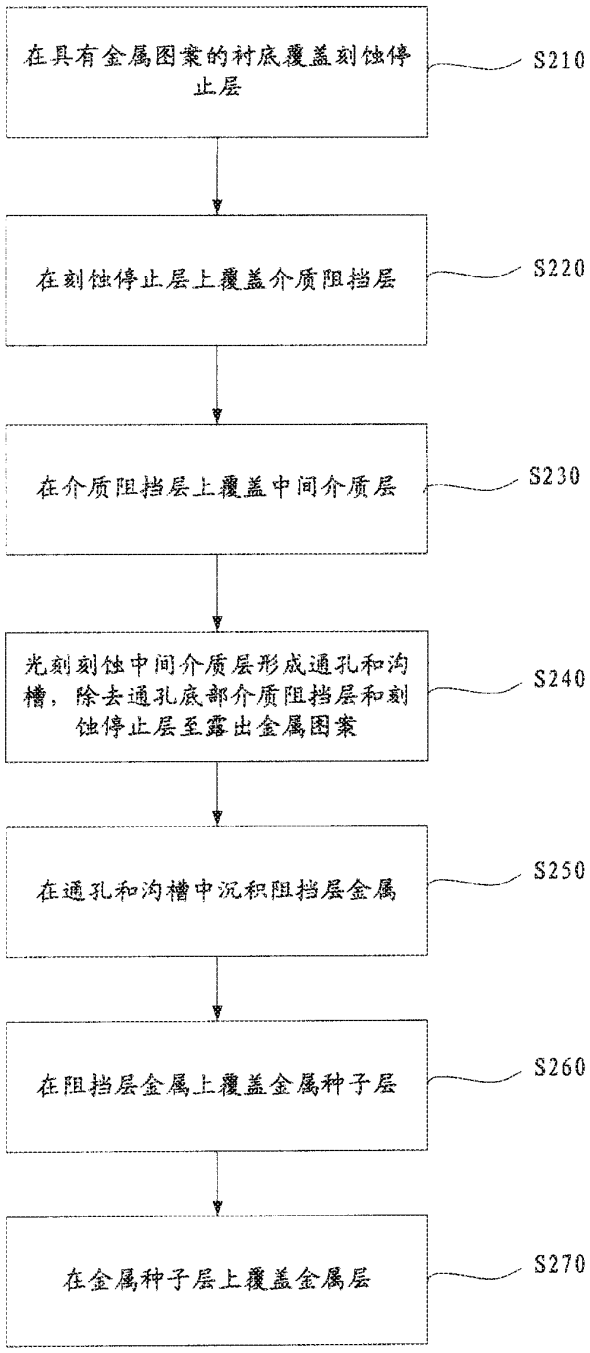

在具有金属图案的衬底覆盖刻蚀停止层
S210
在刻蚀停止层上覆盖介质阻挡层
S220
在介质阻挡层上覆盖中间介质层
S230
光刻刻蚀中间介质层形成通孔和沟槽，除去通孔底部介质阻挡层和刻蚀停止层至露出金属图案
S240
在通孔和沟槽中沉积阻挡层金属
S250
在阻挡层金属上覆盖金属种子层
S260
在金属种子层上覆盖金属层
S270

图 4

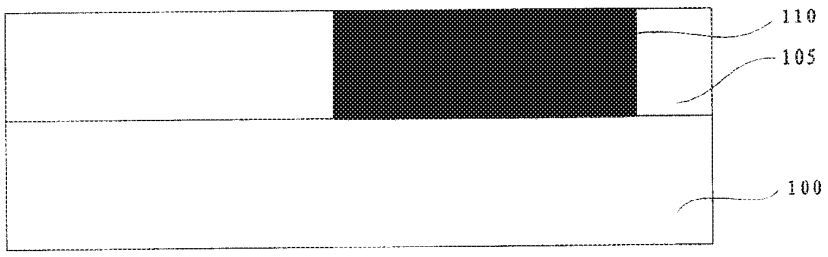


图 5

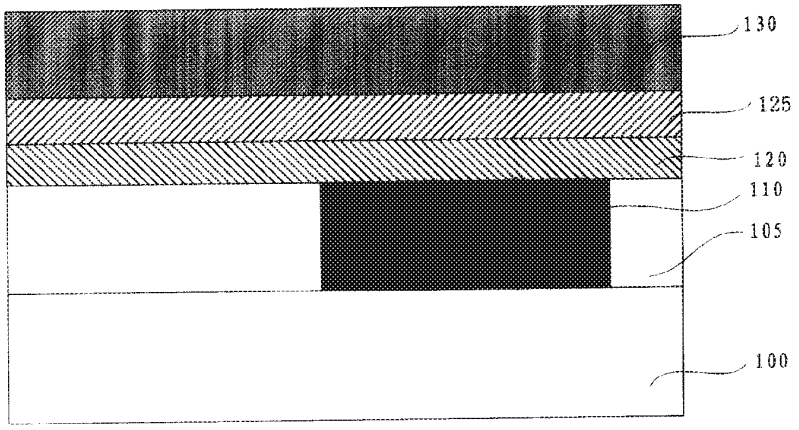


图 6

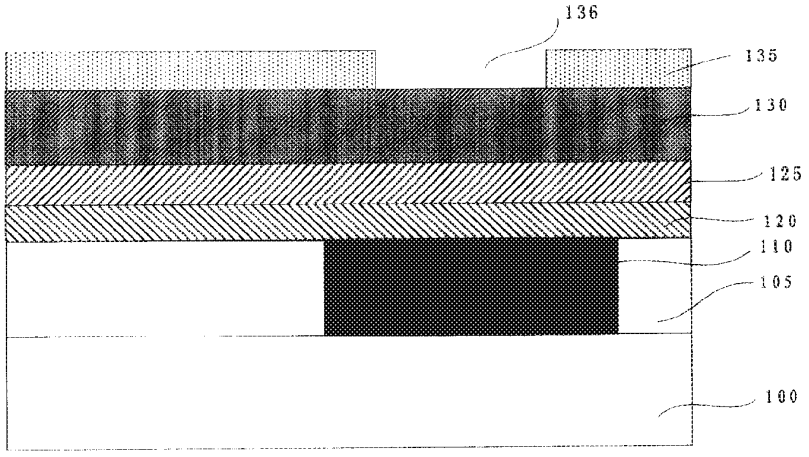


图 7

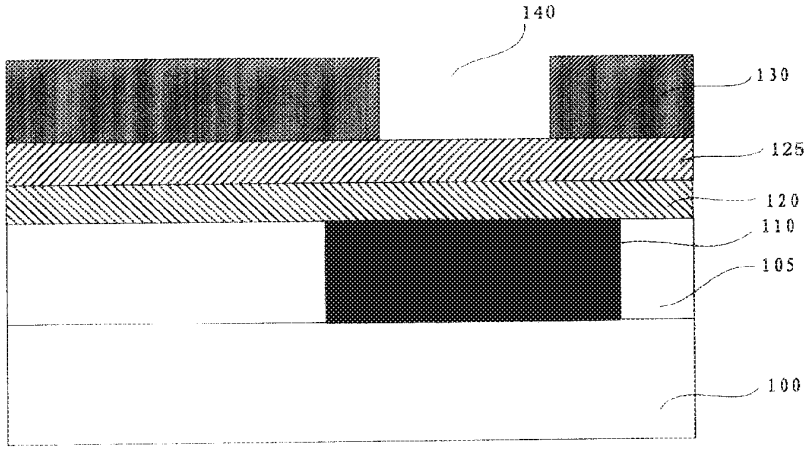


图 8

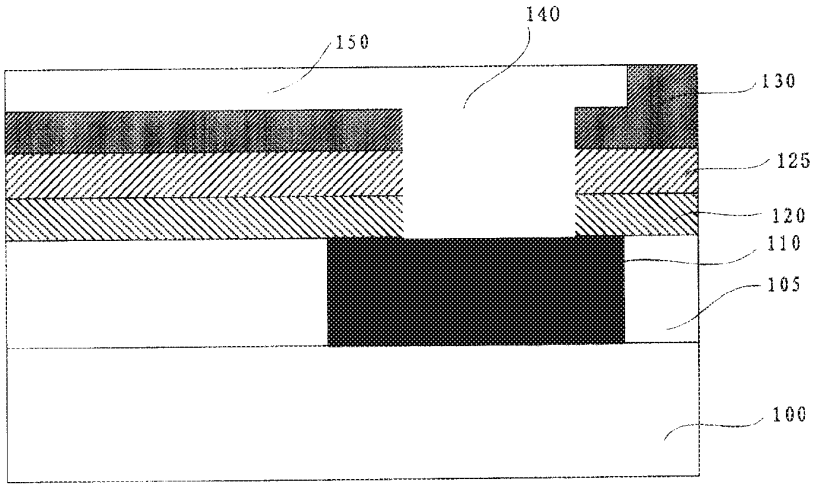

140
150
130
125
120
110
105
100

图 9

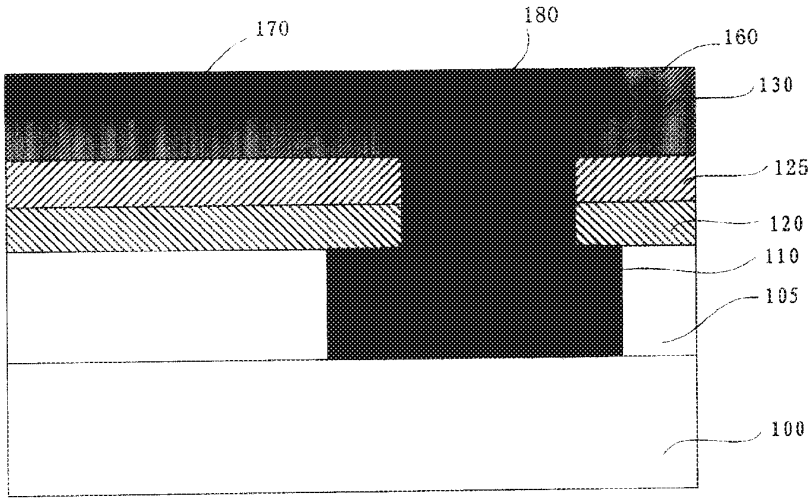

180
170
160
130
125
120
110
105
100

图 10

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DESCRIPTION CN101064295

The present invention provides a semiconductor device and a method of fabricating the same. The semiconductor device has a top metal layer and an underlying metal layer electrically connected to the top metal layer through vias of the intermediate dielectric layer. The manufacturing method of the present invention first covers an etch stop layer on a substrate having a metal pattern, and has a thickness of 100 to 300 angstroms, and covers a etch stop layer having a barrier layer twice as thick as the etch stop layer. The barrier layer is covered with an intermediate dielectric layer and is etched by photolithography to remove trenches and vias required for depositing the top layer metal, wherein the presence of the barrier layer avoids the occurrence of peeling of the etch stop layer and the intermediate dielectric layer.

Semiconductor device and method of manufacturing same

Technical field

The present invention relates to the field of semiconductor manufacturing technology, and in particular to a semiconductor device and a method of fabricating the same.

Background technique

The development of semiconductor technology requires more and more integration, and the requirements for line width and process are becoming more and more demanding. While moving toward the small linewidth technology node, the IC industry has chosen copper and low-k materials as a key solution to reduce the interconnect resistance and capacitance (RC) delay of 0.13um and below technology nodes, compared to

etching in aluminum metal processes. In the process of removing aluminum, copper is easy to diffuse and difficult to etch. The industry has introduced Dual Damascene, which is characterized by forming an intermediate dielectric layer on the substrate with the device and etching the trench and Through holes are then deposited into the etched pattern and planarization is used to remove excess copper.

Generally, in the fabrication of the top layer metal in the latter part of the semiconductor device, the process step is generally to deposit an etch stop layer, an intermediate dielectric layer, a copper diffusion preventing layer, and a copper deposition layer on the substrate with the metal pattern. Then chemical mechanical grinding. Therefore, the corresponding development of a dielectric material compatible with the dual damascene process, such as an etch stop layer, an intermediate dielectric layer material has become an urgent need. Process integration of copper and low-k materials is challenging.

Compared with SIN (K ~ 7.8) and SIO N (K ~ 7), which have relatively large dielectric constants, SIC (K ~ 5) with a small dielectric constant is generally used as an etch stop layer in the prior art, and chemical vapor deposition is used. The method deposits fluorosilicate glass (FSG) as an intermediate dielectric layer and uses a high concentration of fluorine in the process to reduce its dielectric constant. However, high concentrations of fluorine are often unstable and diffuse to the dielectric or metal layers on both sides to disrupt the adhesion of the interface. The Chinese patent No. 99110641 discloses a method for preventing the diffusion of FSG to the upper metal surface and destroying the interface adhesion between the FSG and the metal by forming a surface on the upper surface of the FSG to prevent the fluorine material from passing through the silicon oxynitride. The problem attached, however, that the destruction of the underlying etch stop layer by the high concentration of fluorine causes the adhesion of the FSG to the etch stop layer to deteriorate and the problem of peeling after the top metal deposition becomes a problem of the process personnel.

FIG. 1 is a schematic view of a prior art directly covering an intermediate dielectric layer on an etch stop layer. As shown in FIG. 1, the substrate 100 having the metal pattern 110 is covered with an etch stop layer 120 and an intermediate dielectric layer 130. The trench 150 and the via 140 are formed on the intermediate dielectric layer 130 and pass through the trench 150. The holes 140 are filled with a metal such as copper. Fig. 2 is a schematic view showing the peeling of the intermediate layer of the etching stop layer and the upper layer thereof in the prior art. As shown in FIG. 2, in the copper process, the adhesion of the non-conductive dielectric material and the metal layer thereof to the other auxiliary dielectric layer is inevitably problematic, because the adhesion of the intermediate dielectric layer 130 and the etch stop layer 120 is not good. The peeling phenomenon occurs, and the peeling phenomenon may occur during the production process of the device or after the device is produced, when the adhesion strength test of the passivation layer and the outer wire (packaging wire bonding) is tested. Peeling in the production process will cause the back metal layer to lift up, affecting its electrical connection and eventually causing the device to fail. If there is no peeling during the production process, the life of the device will be changed due to poor adhesion. short.

Summary of the invention

SUMMARY OF THE INVENTION Accordingly, it is an object of the present invention to provide a semiconductor device and a method of fabricating the same that solve the problem of poor adhesion of the top metal intermediate dielectric layer to its underlying etch stop layer and peeling

To achieve the above object, the present invention provides a semiconductor device comprising

a substrate; a dielectric layer formed on the substrate; and a metal pattern layer formed in the dielectric layer;

An etch stop layer formed on the dielectric layer and the metal pattern layer;

a barrier layer formed on the etch stop layer;

An intermediate dielectric layer formed on the barrier layer; the intermediate dielectric layer has a trench and a via hole therein, and the trench and the via hole are sequentially filled with a metal barrier layer, a metal seed layer and an interconnect metal layer.

The etch stop layer has a thickness of 100 angstroms to 300 angstroms.

The barrier layer has a thickness of 200 angstroms to 600 angstroms.

The etch stop layer is at least one of silicon oxide, silicon carbide (SiC), silicon nitride (SiN), carbon oxynitride (SiOC), nitrogen- doped silicon carbide, or a combination thereof.

The barrier layer is at least one of silicon oxide, silicon carbide (SiC), silicon nitride (SiN), carbon oxynitride (SiOC), nitrogen- doped silicon carbide, or a combination thereof.

The intermediate dielectric layer is at least fluorosilicate glass (FSG), phosphosilicate glass (PSG), borosilicate

glass (BSG), borophosphosilicate glass (BPSG), silicon oxide, silicon nitride (SiN), silicon carbide (One or a combination of SiC).

The depth of the trench on the intermediate dielectric layer is less than the depth of the via.

The metal barrier layer is titanium (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo), cobalt (Co), platinum (Pt), titanium tungsten (TiW), titanium nitride (TiN), One or a combination of tantalum nitride (TaN).

The metal seed layer is copper, aluminum, tungsten, gold or silver.

The interconnect metal layer comprises copper or aluminum.

The through holes are located at corresponding positions above the metal pattern.

The interconnect metal layer in the via is electrically connected to the metal pattern on the substrate through the metal seed layer and the metal barrier layer.

Accordingly, the present invention provides a method of fabricating a semiconductor device, comprising

Providing a semiconductor substrate, forming a dielectric layer and a metal pattern layer on the substrate;

Forming an etch stop layer on the dielectric layer and the metal pattern layer;

Forming a barrier layer on the etch stop layer;

Forming an intermediate dielectric layer on the barrier layer;

Etching the intermediate dielectric layer, the barrier layer and the etch stop layer to form via holes to expose the metal pattern and forming trenches in the intermediate dielectric layer;

A metal seed layer, a metal barrier layer, and an interconnect metal layer are sequentially filled in the trench and the via.

The method of forming the etch stop layer and the barrier layer includes physical vapor deposition (PVD) or chemical vapor deposition (CVD).

The chemical vapor deposition includes atmospheric pressure chemical vapor deposition (APCVD), low pressure chemical vapor deposition (LPCVD), ion enhanced chemical vapor deposition (PECVD), and high density plasma chemical vapor deposition (HDPCVD).

The etch stop layer has a thickness of 100 angstroms to 300 angstroms.

The barrier layer has a thickness of 200 angstroms to 600 angstroms.

The method of forming the intermediate dielectric layer includes physical vapor deposition, chemical vapor deposition.

The metal barrier layer is formed using a physical vapor deposition or electroplating method.

Compared with the prior art, the present invention has the following advantages: the present invention prevents diffusion of fluorine in the intermediate dielectric layer to the etch stop layer and the intermediate dielectric layer by inserting a barrier layer between the etch stop layer and the intermediate dielectric layer. , thereby reducing the corrosion and destruction of the interface between the two layers due to the free diffusion of fluorine, which helps to increase the adhesion of the upper and lower layers at the interface;

In addition, due to the destruction and recombination of chemical bonds by ion bombardment during deposition, high stress is generated in the deposited dielectric film, high film stress causes cracking and delamination, and barrier SiN destroys Si-N bond due to ion bombardment. Therefore, there is a high compressive stress, which helps to balance the tensile stress of the intermediate dielectric layer material fluorosilicate glass (FSG), thereby reducing the influence of stress on the adhesion between the layers, and increasing its viscosity. Attached to force.

DRAWINGS

1 is a schematic view of a prior art directly covering an intermediate dielectric layer on an etch stop layer;

2 is a schematic view showing the peeling of the etch stop layer and the intermediate medium layer of the upper layer thereof in the prior art;

Figure 3 is a cross- sectional view showing the structure of a semiconductor device of the present invention;

4 is a process flow diagram of a method of fabricating a semiconductor device of the present invention;

5 to 10 are cross- sectional views illustrating a method of fabricating a semiconductor device of the present invention.

Detailed ways

The above described objects, features, and advantages of the present invention will be more apparent from the aspects of the invention.

Figure 3 is a cross- sectional view showing the structure of a semiconductor device of the present invention. As shown in FIG. 3, the semiconductor device of the present invention includes a substrate 100 and a metal pattern layer 110 formed in the dielectric layer 105 on the substrate 100. The metal pattern layer 110 is spin- coated on the dielectric layer 105. Photoresist is formed by exposure development and etching. An etch stop layer 120 is formed on the dielectric layer 105 and the metal pattern layer 110, and has a thickness of 100 angstroms to 300 angstroms. The material thereof may be silicon oxide, silicon carbide (SiC), silicon nitride (SiN), carbon nitrogen. One or a combination of an oxygen compound (SiOC), nitrogen- doped silicon carbide. The function of the etch stop layer is to prevent the underlying pattern from being destroyed when etching the underlying material. The etch stop layer 120 serves as an end stop layer for etching the material of the upper layer, and can protect the underlying metal pattern 110 from being etched to form defects. The semiconductor device of the present invention is covered on the etch stop layer 120 with a barrier layer 125 having a thickness of 200 angstroms to 600 angstroms. The selected material may be silicon oxide, silicon carbide (SiC), silicon nitride

(SiN), carbon oxynitride (SiOC), one or a combination of nitrogen-doped silicon carbide. An intermediate dielectric layer 130 having a low dielectric constant material deposited on the barrier layer 125 is matched to an interconnect metal such as copper to reduce the resistive capacitance (RC) delay caused by its parasitic capacitance and interconnect metal resistance. The optional material includes fluorosilicon. Glass (FSG), phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG).

The intermediate dielectric layer 130 has a via hole 140 and a trench 150 formed by applying a photoresist, and exposing and developing the pattern of the mask to the intermediate dielectric layer 130. The depth of the trench 150 is smaller than that of the via 140. Depth, whether or not the two are connected depends on the electrical connection determined by the device. The via hole 140 and the trench 150 are sequentially covered with a metal barrier layer 160, a metal seed layer 170, and an interconnect metal layer 180. The metal barrier layer includes titanium (Ti), tungsten (W), tantalum (Ta), and molybdenum (Mo).), one or a combination of cobalt (Co), platinum (Pt), titanium tungsten (TiW), titanium nitride (TiN), tantalum nitride (TaN), and the metal seed layer includes copper, aluminum, tungsten, gold Or silver, the interconnect metal layer comprises copper or aluminum. The bottom of the via 140 is connected to the metal pattern 110 on the substrate 100.

The deposited barrier layer 125 may increase the adhesion of the intermediate dielectric layer 130 and the etch stop layer 120. For example, the barrier layer 125 is made of SiN, and the intermediate dielectric layer 130 is generally made of fluorosilicate glass (FSG) for the top metal, in the FSG. Fluorine has a strong diffusion effect. In order to reduce the dielectric constant of the dielectric layer material and reduce the resistance capacitance (RC) delay of its parasitic capacitance and interconnect metal resistance, it is often preferred to use a high concentration of fluorine in the deposition of FSG. The concentration of fluorine is unstable, and it will diffuse up and down. The corrosion of fluorine at the interface will reduce its adhesion, which will cause the layer to peel off. SiN is a good barrier layer of fluorine. The content of N is more. High, the less diffusion of fluorine occurs, the barrier material is introduced to effectively block its diffusion, reduce its corrosion to the surface, and increase the adhesion performance.

In addition, the deposited low dielectric constant material FSG will have tensile stress, high stress in the dielectric film will lead to delamination, deposition of barrier material SiN using plasma enhanced chemical vapor deposition, high-speed ion-pairing of ionic bonds in SiN during deposition The damage will cause the deposited SiN film to have a high compressive stress, which will help balance the tensile stress in the FSG to the underlying film and reduce the delamination caused by the stress.

4 is a process flow diagram of a method of fabricating a semiconductor device of the present invention. As shown in Fig. 4, a method of manufacturing a semiconductor device of the present invention. First, the etch stop layer 120 is overlaid on the substrate 100 having the metal pattern 110 (S210); then, the barrier layer 125 is deposited by vapor deposition on the etch stop layer 120 (S220); then, on the barrier layer 125 The intermediate dielectric

layer 130 is covered (S230); the via hole 140 and the trench 150 are formed on the intermediate dielectric layer 130 by photolithography and etching, and the barrier layer 125 and the etch stop layer 120 at the bottom of the via hole 140 are opened to make the via hole The bottom of the 140 exposes the metal pattern 110 on the substrate 100 (S240); finally, the metal barrier layer 160 is covered in the via 140 and the trench 150 (S250); the metal barrier layer 170 is covered on the metal barrier layer 160 (S260); An interconnect metal layer 180 is filled on the metal seed layer 170 (S270).

5 to 10 are cross-sectional views illustrating a method of fabricating a semiconductor device of the present invention. The process steps for implementing the method are described in detail below with reference to FIGS. 5 through 10. As shown in Fig. 5, the present invention first forms a dielectric layer 105 on the substrate 100 and a metal pattern 110 formed by photolithography, etching, and deposition of a metal such as copper.

Next, as shown in FIG. 6, an etch stop layer 120 is deposited on the substrate 100 and the metal pattern 110, and the deposition may be plasma enhanced chemical vapor deposition. Preferably, the deposited material has a thickness of 100 angstroms to 300 angstroms, and the deposited material may be nitrogen-doped silicon carbide, silicon oxide, silicon carbide (SiC), silicon nitride (SiN), carbon oxynitride (SiOC). One or a combination thereof. The etch stop layer 120 serves as a barrier material for protecting the underlying metal pattern 110 from damage during etching of the upper layer and as a diffusion barrier for the underlying metal to prevent metal such as copper in the underlying metal pattern from diffusing into the upper layer. As is known to those skilled in the art, copper as a late-stage interconnect metal has a strong diffusion effect, and thus the etch stop layer also functions to block diffusion of the underlying metal. The semiconductor device manufacturing method of the present invention does not directly deposit an upper dielectric layer on the etch stop layer 120 to complete deposition of the non-conductive dielectric layer, but passes through the etch stop layer 120 after depositing the etch stop layer 120. A vapor barrier layer 125 is deposited by physical vapor deposition (PVD) or chemical vapor deposition. The barrier layer 125 has a thickness of 200 angstroms to 600 angstroms. The material of the barrier layer may be high density and high stress silicon nitride (SiN). Or other organic material, inorganic material, metal, or at least one of silicon oxide, silicon carbide (SiC), carbon oxynitride (SiOC), or a combination thereof. After the deposition of the barrier layer 125 is completed, the intermediate dielectric layer 130 is deposited thereon. Since the intermediate dielectric layer needs to select a material having a small dielectric constant, the preferred method of depositing fluorosilicate glass (FSG) by chemical vapor deposition in this embodiment is used. In general, the concentration of fluorine is high, and the dielectric constant thereof is small. In this embodiment, the dielectric constant is about 3.7. Other optional materials include fluorosilicate glass (FSG), phosphosilicate glass (PSG), borosilicate glass (BSG) or borophosphosilicate glass (BPSG). The deposited barrier layer 125 can prevent the diffusion of fluorine in the intermediate dielectric layer 130 and reduce the tensile stress effect of the FSG, increase the adhesion property of the etch stop layer 120 and the intermediate dielectric layer 130, and reduce the delamination between the two layers. Defects such as peeling

After depositing the etch stop layer 120, the barrier layer 125 and the intermediate dielectric layer 130 on the

substrate with the metal pattern, as shown in FIG. 7, the photoresist 135 is coated on the intermediate dielectric layer to form by exposure and development. The pattern 136 defines a connection hole exposing the lower intermediate dielectric layer 130, and the position of the pattern 136 corresponds to the position of the metal pattern 110 on the substrate 100. Then, as shown in FIG. 8, the intermediate dielectric layer 130 is etched, and the photoresist serves as a barrier layer for etching to protect the photoresist covering position of the lower intermediate dielectric layer 130 during the etching process. The position of the connection hole of the intermediate dielectric layer 130 is etched due to exposure, and the via hole 140 is formed on the intermediate dielectric layer 130 by dry or wet etching. The etch stops when the lower barrier layer 125 of the intermediate dielectric layer 130 is exposed. It can be seen that the barrier layer 125 also serves as an etch stop layer for the intermediate dielectric layer 130. The vias 140 are formed on the intermediate dielectric layer 130 by removing the photoresist 135 by ashing and stripping. As shown in FIG. 9, a trench 150 is formed on the intermediate dielectric layer 130 in the same manner as described above, and the depth of the trench 150 is smaller than the depth of the via hole 140, that is, the bottom of the trench 150 does not expose the lower layer of the intermediate dielectric layer 130. The barrier layer 125, whether the trench 150 is connected to the via 140 depends on the electrical connection of the trench 150 and the metal deposited by the via 140. Then, etching and cleaning are performed to remove the barrier layer 130 and the etch stop layer 125 under the via hole 140, so that the metal pattern 110 on the substrate can be exposed through the via hole 140.

As shown in FIG. 10, the formed trenches 150 and vias 140 are filled with a metal such as copper. Due to the diffusion effect of the copper ions, if they are not treated correspondingly, they are filled into the via holes 140 and the trenches 150. The copper will diffuse to its adjacent dielectric layer, such as the intermediate dielectric layer 130, which will change the dielectric layer's insulating effect and introduce other parasitic effects that affect device performance. Therefore, it is necessary to properly treat it, usually by first depositing a diffusion barrier (Diffusion Barrier), and depositing a through hole 140 and a trench 150 by a suitable method such as physical vapor deposition or chemical vapor deposition. The metal barrier layer 160 may be made of titanium nitride (TiN), titanium (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo), cobalt (Co), platinum (Pt), titanium tungsten (TiW), one of or a combination of tantalum nitride (TiN). The addition of the metal barrier layer 160 can well prevent the diffusion of metallic copper to the dielectric layer and enhance the adhesion of the metallic copper to its dielectric layer. A metal seed layer 170 and an interconnect metal layer 180 are deposited on the metal barrier layer 160, and the deposition may be physical vapor deposition, chemical vapor deposition, or electroplating. The thickness of the deposited metal layer fills at least the entire via 140 and the trench 150.

The present invention is disclosed in the above preferred embodiments, but it is not intended to limit the present invention, and any one skilled in the art can make possible variations and modifications without departing from the spirit and scope of the invention. The scope of protection should be determined by the scope defined by the claims of the present invention.

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CLAIMS CN101064295

1、
A semiconductor device characterized by comprising

a substrate; a dielectric layer formed on the substrate; and a metal pattern layer formed in the dielectric layer;

An etch stop layer formed on the dielectric layer and the metal pattern layer;

a barrier layer formed on the etch stop layer;

An intermediate dielectric layer formed on the barrier layer; the intermediate dielectric layer has a trench and a via hole therein, and the trench and the via hole are sequentially filled with a metal barrier layer, a metal seed layer and an interconnect metal layer.

2、
The semiconductor device according to claim 1, wherein said etch stop layer has a thickness of from 100 to 300 .

3、
A semiconductor device according to claim 1, wherein said barrier layer has a thickness of from 200 to 600 .

4、
The semiconductor device according to claim 2, wherein said etch stop layer is at least silicon oxide, silicon carbide (SiC), silicon nitride (SiN), carbon oxynitride (SiO C), nitrogen- doped carbonization O ne or a combination of silicon.

5、
The semiconductor device according to claim 3, wherein said barrier layer is at least silicon oxide, silicon carbide (SiC), silicon nitride (SiN), carbon oxynitride (SiO C), and nitrogen- doped silicon carbide. O ne or a combination thereof.

6、
A semiconductor device according to claim 1, wherein said intermediate dielectric layer is at least fluorosilicate glass (FSG), phosphosilicate glass (PSG), borosilicate glass (BSG), borophosphosilicate glass (BPSG). O ne of silicon oxide, silicon nitride (SiN), silicon carbide (SiC), or a combination thereof.

7、
A semiconductor device according to claim 1, wherein the depth of the trench on said intermediate dielectric layer is smaller than the depth of the via hole.

8、
A semiconductor device according to claim 1, wherein said metal barrier layer is titanium (Ti), tungsten (W), tantalum (Ta), molybdenum (Mo), cobalt (C o), platinum (Pt). O ne or a combination of titanium tungsten (TiW), titanium nitride (TiN), tantalum nitride (TaN).

9、
The semiconductor device according to claim 1, wherein said metal seed layer is copper, aluminum, tungsten, gold or silver.

10、
The semiconductor device of claim 1 wherein said interconnect metal layer comprises copper or aluminum.

11、
A semiconductor device according to claim 1, wherein said through hole is located at a corresponding position above the metal pattern.

12、
The semiconductor device according to claim 1, wherein said interconnect metal layer in said via hole is electrically connected to said metal pattern on said substrate through said metal seed layer and said metal barrier layer connection.

13、
A method of fabricating a semiconductor device, comprising

Providing a semiconductor substrate, forming a dielectric layer and a metal pattern layer on the substrate;

Forming an etch stop layer on the dielectric layer and the metal pattern layer;

Forming a barrier layer on the etch stop layer;

Forming an intermediate dielectric layer on the barrier layer;

Etching the intermediate dielectric layer, the barrier layer and the etch stop layer to form via holes to expose the metal pattern and forming trenches in the intermediate dielectric layer;

A metal seed layer, a metal barrier layer, and an interconnect metal layer are sequentially filled in the trench and the via.

14、
A method of fabricating a semiconductor device according to claim 13, wherein the etching stop layer and the barrier layer are formed by physical vapor deposition (PVD) or chemical vapor deposition (CVD).

15、

A method of fabricating a semiconductor device according to claim 13, wherein said chemical vapor deposition comprises atmospheric pressure chemical vapor deposition (APCVD), low pressure chemical vapor deposition (LPCVD), and ion enhanced chemical vapor deposition (PECVD). High-density plasma chemical vapor deposition (HDPCVD).

16、
The method of fabricating a semiconductor device according to claim 13, wherein the etching stop layer has a thickness of 100 to 300 .

17、
A method of manufacturing a semiconductor device according to claim 13, wherein said barrier layer has a thickness of from 200 to 600 .

18、
A method of fabricating a semiconductor device according to claim 13, wherein the method of forming the intermediate dielectric layer comprises physical vapor deposition, chemical vapor deposition.

19、
A method of manufacturing a semiconductor device according to claim 13, wherein said metal barrier layer is formed by a physical vapor deposition or plating method.

Electronic Patent Application Fee Transmittal					
Application Number:	15477506				
Filing Date:	03-Apr-2017				
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS				
First Named Inventor/Applicant Name:	Boyan Boyanov				
Filer:	Michael A. Bernadicou/Lisa Puccinelli				
Attorney Docket Number:	P38794USDC 111548-227293				
Filed as Large Entity					
Filing Fees for Utility under 35 USC 111(a)					
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Basic Filing:					
Pages:					
Claims:					
Miscellaneous-Filing:					
Petition:					
Patent-Appeals-and-Interference:					
Post-Allowance-and-Post-Issuance:					
Extension-of-Time:					

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	36430549
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	27-JUN-2019
Filing Date:	03-APR-2017
Time Stamp:	21:38:05
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Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	062819INTEFSW00006837500393
Deposit Account	500393
Authorized User	Lisa Puccinelli
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37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

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	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Foreign Reference	Ref_CN_101064295.pdf	2547688 a3a35657d4972428ddcce002c351a35f8f0a487b	no	30
Warnings:					
Information:					
3	Other Reference-Patent/App/Search documents	Ref_P38794CN-D-D1_OA_06-04-19.pdf	11089739 650e71e8036fdce15eeb0db6e7403578efb9f5c2	no	10
Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	Ref_P38794KR-D2-D2-D1_OA_03-27-19.pdf	1481914 d4e9e1b30dad8c1e056a674e818f362e6a92b71e	no	3
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyan Boyanov, et al.
Art Unit	2898
Examiner Name	Galvin III, Joseph M.
Attorney Docket No.	P38794USDC Conf. No. 2892

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted after Allowance but prior to payment of the Issue Fee. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☒ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	06-27-2019
Name/Print	Michael A. Bernadicou	Registration Number	35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 06-27-2019

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

31817 7590 06/12/2019
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
GALVIN III, JOSEPH M	
ART UNIT	PAPER NUMBER
2898	

DATE MAILED: 06/12/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293	2892

TITLE OF INVENTION: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	09/12/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

31817 7590 06/12/2019
SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293	2892

TITLE OF INVENTION: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	09/12/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
GALVIN III, JOSEPH M	2898	257-773000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC ~~111548-227293~~	2892

31817 7590 06/12/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
GALVIN III, JOSEPH M	
ART UNIT	**PAPER NUMBER**
2898	

DATE MAILED: 06/12/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/477,506	Applicant(s) Boyanov et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to AFCP 2.0 filed 06/03/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-7 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☑ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☑ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☑ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 05/16/2019.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☑ Other PTO-2323.

/JOSEPH M GALVIN III/
Primary Examiner, Art Unit 2898

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Response to Amendment

The amendment, filed 06/03/2019, has been entered.

Response to Arguments

Applicant's arguments, see pages 4-5, filed 06/03/2019, with respect to the capping layer directly on the dielectric have been fully considered and are persuasive. The 35 USC 103 rejection of claim 1 has been withdrawn.

Allowable Subject Matter

Claims 1-7 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 1, the prior art of record teaches the apparatus as claimed in claim 1, but fails to teach or reasonably suggest a motivation for wherein the first capping layer, made of cobalt, is directly on the sidewall of the dielectric layer to prevent electromigration and wherein a top of the first capping layer is not higher than the top boundary.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH M GALVIN III whose telephone number is (571)272-0559. The examiner can normally be reached on M-F: 8:30AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 5712721864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOSEPH M GALVIN III/
Primary Examiner, Art Unit 2898

Notice of References Cited	Application/Control No. 15/477,506	Applicant(s)/Patent Under Reexamination Boyanov et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090200668-A1	08-2009	Yang; Chih-Chao	H01L21/76834	257/751
*	B	US-20100171219-A1	07-2010	Moreau; David	H01L21/76834	257/751
*	C	US-20060205204-A1	09-2006	Beck; Michael	H01L21/7684	438/628
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

AFCP 2.0 Decision	Application No.	Applicant(s)	
	15/477,506	Boyanov et al.	
	Examiner	Art Unit	AIA (FITF) Status
	JOSEPH M GALVIN III	2898	No

This is in response to the After Final Consideration Pilot request filed 03 June 2019.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other: _____

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☑ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action . See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☐ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other: _____

   Examiner Note: Please attach an interview summary when necessary as described above.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	Art Unit
	JOSEPH M GALVIN III	2898

CPC - Searched*		
Symbol	Date	Examiner
H01L21/76802,7684,76849,7685,76879,76883	11/26/2018	JG
H01L23/485,5226,528,53209,53238,53295	11/26/2018	JG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EASTsearch	11/26/2018	JG
updated EAST search	03/29/2019	JG
updated EAST search	06/09/2019	JG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	21/76802,7684,76849,7685,76879,76883	06/09/2019	JG
H01L	23/485,5226,528,53209,53238,53295	06/09/2019	JG
	See EAST search history	06/09/2019	JG

/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	Art Unit
	JOSEPH M GALVIN III	2898

CPC								
Symbol							Type	Version
H01L	/	23	/	53238			F	2013-01-01
H01L	/	21	/	7685			I	2013-01-01
H01L	/	23	/	485			I	2013-01-01
H01L	/	21	/	76883			I	2013-01-01
H01L	/	21	/	76849			I	2013-01-01
H01L	/	23	/	528			I	2013-01-01
H01L	/	23	/	53209			I	2013-01-01
H01L	/	23	/	53295			I	2013-01-01
H01L	/	21	/	76802			I	2013-01-01
H01L	/	21	/	7684			I	2013-01-01
H01L	/	21	/	76879			I	2013-01-01
H01L	/	23	/	5226			I	2013-01-01
H01L	/	2924	/	0002			A	2013-01-01

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
H01L	/	2924	/	0002	A	1	1	2013-01-01
H01L	/	2924	/	00	A	1	2	2013-01-01

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	7	
/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	09 June 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3B

U.S. Patent and Trademark Office — Part of Paper No.: 20190609

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	**Art Unit**
	JOSEPH M GALVIN III	2898

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L23/532	/	23	/	532

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	7	
/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	09 June 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3B

U.S. Patent and Trademark Office — Part of Paper No.: 20190609

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	**Art Unit**
	JOSEPH M GALVIN III	2898

☑ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	7	
/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	09 June 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	3B

U.S. Patent and Trademark Office — Part of Paper No.: 20190609

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L10	3	"20090283499"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:39
L11	161	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
L12	38405	((("INTEL") near3 ("CORPORATION"))).AS,AANM.	USPAT	OR	OFF	2019/06/09 14:42
L13	57250	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
L14	18240	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
L15	10205	L14 and cap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
L16	2332	L15 and L13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
L17	426	L16 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
L18	243	(CuCo copper near2 cobalt) with interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/06/09 14:42
S1	1	"15477506"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:31
S2	53238	(H01L21/76802 OR H01L21/7684 OR	US-PGPUB;	OR	OFF	2018/11/26

		H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	USPAT; USOCR; EPO; JPO; DERWENT			08:54
S3	158	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:54
S4	36636	(("INTEL") near3 ("CORPORATION"))).AS,AANM.	USPAT	OR	OFF	2018/11/26 08:54
S5	20	("8043958" "6348731" "6114238" "6046108" "7396757" "6908847" "5470789").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:57
S6	3	"20080027677"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:00
S11	3	"20070049008"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/26 09:03
S12	2	"20090200668"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:05
S13	193	(CuCo copper near2 cobalt) with interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:22
S14	17544	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:24
S15	9779	S14 and cap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:25
S17	2228	S15 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:25
S18	391	S17 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:59
S19	160	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46

S20	55664	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S21	17972	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S22	10028	S21 and cap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S23	2289	S22 and S20	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S24	406	S23 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
S25	160	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 16:03

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L19	153	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:47
L20	37244	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:47
L21	3679	((cobalt Co) near5 cap$4).clm.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:47
L22	420	20 and 21	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:48
L24	281	22 and (copper Cu).clm.	US-PGPUB; USPAT	OR	OFF	2019/06/09 14:48

6/9/2019 2:55:57 PM
C:\Users\jgalvin\Documents\EAST\Workspaces\15477506.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Boyan Boyanov	Examiner: Galvin III, Joseph M.
Application No.: 15/477,506	Art Unit: 2898
Filed: April 3, 2017	Confirmation No.: 2892
For: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.116

AND

REQUEST FOR AFTER-FINAL CONSIDERATION PILOT (AFCP 2.0) REVIEW

Dear Examiner:

This is in response to the Final Office Action mailed April 3, 2019. Applicant respectfully requests the Examiner to enter this Amendment and consider the following remarks. Applicant also requests the Examiner to consider the arguments under the After-Final Consideration Pilot (AFCP 2.0) review program initiated by the USPTO.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

OK TO ENTER: /J.M.G/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed February, 19, 2019, 18 pgs.	X

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	06/09/2019

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Boyan Boyanov	Examiner: Galvin III, Joseph M.
Application No.: 15/477,506	Art Unit: 2898
Filed: April 3, 2017	Confirmation No.: 2892
For: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT UNDER 37 CFR §1.116

AND

REQUEST FOR AFTER-FINAL CONSIDERATION PILOT (AFCP 2.0) REVIEW

Dear Examiner:

This is in response to the Final Office Action mailed April 3, 2019. Applicant respectfully requests the Examiner to enter this Amendment and consider the following remarks. Applicant also requests the Examiner to consider the arguments under the After-Final Consideration Pilot (AFCP 2.0) review program initiated by the USPTO.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
P38794USDC	15/477,506	April 3, 2017
First Named Inventor:	**Title:**	
Boyan Boyanov	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:

- Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
- The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
  - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
  - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
    - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
    - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/Michael A. Bernadicou/	June 3, 2019
Name (Print/Typed) Michael A. Bernadicou	**Practitioner Registration No.** 35934

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

[✓] * Total of 1 forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	36188448
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	03-JUN-2019
Filing Date:	03-APR-2017
Time Stamp:	19:30:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Intel_P38794USDC_RFOA_06_03_19.pdf	159541 a1135f4f174c2c80615886301fa06f6ebb5efb9d	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Applicant Arguments/Remarks Made in an Amendment	4	7
	Claims	2	3
	Response After Final Action	1	1

Warnings:					
Information:					
2	After Final Consideration Program Request	P38794USDC_Certification_Form_After_Final_2-0.pdf	285110 98f938a89bb0fea9fe31c1c9210ae60610f45785	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	444651		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang et al.* (US 2009/0200668) in view of *Moreau et al.* (US 2010/0171219) Claims 4-5 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang et al.* in view of *Moreau et al.* further in view of *Beck* (US 2006/0205204).

Applicant herein amends independent claim 1, from which claims 2-7 depend, and respectfully request reconsideration of claims 1-7 in view of the amendments and the following arguments.

Amended independent claim 1 is directed to an apparatus, including the features, "*at least one first conductive line in a dielectric layer over a substrate, the dielectric layer having a top boundary*," "*a channel in the dielectric layer on the at least one first conductive line, the channel comprising a sidewall of the dielectric layer between the at least one first conductive line and the top boundary,* ***and a first capping layer comprising cobalt*** *deposited in the channel* ***on the at least one first conductive line comprising copper*** *and cobalt,* ***the first capping layer directly on the sidewall of the dielectric layer*** *to prevent electromigration, wherein a top of the first capping layer is not higher than the top boundary*." (Emphasis added.)

That is, Applicant teaches, and claims in claims 1-7, an apparatus including a capping layer comprising cobalt on a conductive line comprising copper, the capping layer comprising cobalt directly on a sidewall of a dielectric layer. Applicant does not understand the cited references of record as disclosing at least this feature of Applicant's claims 1-7.

Applicant understands Yang as disclosing an interconnect structure

formed in a dielectric material 52. The interconnect structure includes a diffusion barrier 58, a conductive material 60, and a metallic layer 62'. The metallic layer 62' may include cobalt. (*See* Yang, e.g., Paragraph 0073, and Figure 2F, shown below.)

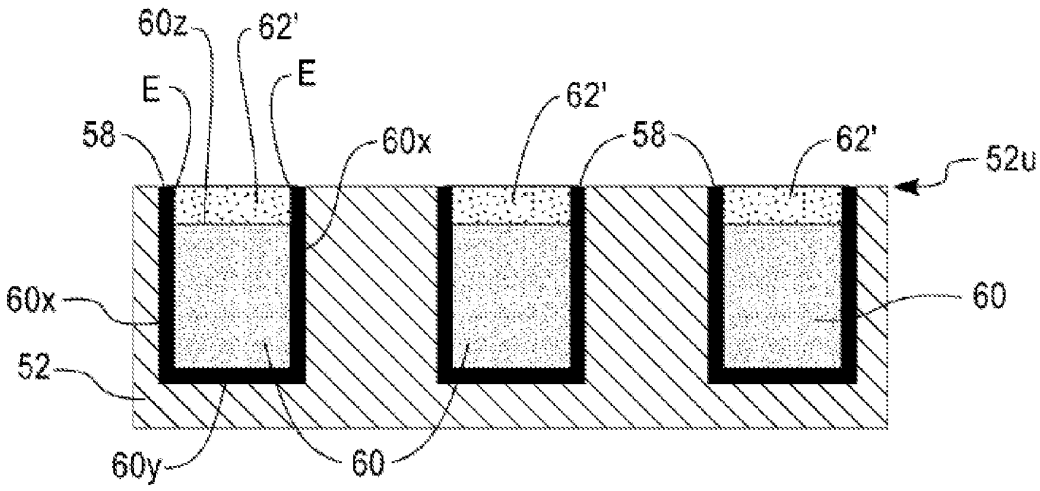


FIG. 2F

Figure 2F of Yang.

However, Applicant understands the metallic layer 62' as being on a sidewall of diffusion barrier 58 of Yang. That is, Applicant does not understand metallic layer 62' as being directly on a sidewall of dielectric layer 52 of Yang, as is required by Applicant's claims 1-7.

Furthermore, with respect to amended independent claim 1, Applicant does not understand the other cited references of record as curing the above noted deficiencies of Yang. Accordingly, Applicant respectfully requests that the Examiner remove the rejections of claims 1-7.

Request for After-Final Consideration Pilot (AFCP 2.0) Review

Applicant respectfully requests the Examiner to consider the arguments under the After-Final Consideration Pilot (AFCP 2.0) review program initiated by the USPTO to bring this matter to a condition for allowance without undue prosecution and RCE because the Examiner appears to have done a substantial search.

CONCLUSION

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 50-0393.

Respectfully submitted,

SCHWABE WILLIAMSON & WYATT

June 3, 2019	/Michael A. Bernadicou/
Date	Michael A. Bernadicou Reg. No. 35,934

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Portland, OR 97204
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Facsimile: 503.796.9200

Listing of Claims:

1. (Currently Amended) An apparatus, comprising:

at least one first conductive line in a dielectric layer over a substrate, the dielectric layer having a top boundary;

a channel in the dielectric layer on the at least one first conductive line, the channel comprising a sidewall of the dielectric layer between the at least one first conductive line and the top boundary, and

a first capping layer comprising cobalt deposited in the channel on the at least one first conductive line comprising copper and cobalt, the first capping layer directly on the sidewall of the dielectric layer to prevent electromigration, wherein a top of the first capping layer is not higher than the top boundary.

2. (Original) The apparatus of claim 1, wherein the first capping layer is self-aligned to the first conductive line.

3. (Previously Presented) The apparatus of claim 1, further comprising

a second capping layer selectively deposited on a second conductive line within second sidewalls of the dielectric layer, the second conductive line being at a first spacing from the at least one first conductive line, and wherein the second capping layer is at the first spacing from the first capping layer.

4. (Original) The apparatus of claim 1, wherein the at least first conductive line is at a depth from 5 nanometers to 50 nanometers from a top surface of the dielectric layer.

5. (Original) The apparatus of claim 1, wherein the first conductive line is at a depth from a top surface of the dielectric layer that is from 10% to 50% of the thickness of the first conductive line.

6. (Original) The apparatus of claim 1, wherein the at least one first conductive line is an interconnect incorporated into a data processing system.

7. (Original) The apparatus of claim 1, wherein a spacing between the at least one first conductive line and a second conductive line in the dielectric layer is from 5 nm to 500 nm.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/477,506	Filing Date 04/03/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	06/03/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 7	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/THERESA D DAWKINS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed February, 19, 2019, 18 pgs.	X

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyan Boyanov, et al.
Art Unit	2898
Examiner Name	Galvin III, Joseph M.
Attorney Docket No.	P38794USDC Conf. No. 2892

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted after Final Office Action but prior to Notice of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☒ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	05-16-2019
Name/Print	Michael A. Bernadicou	Registration Number	35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 05-16-19

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Electronic Patent Application Fee Transmittal	
Application Number:	15477506
Filing Date:	03-Apr-2017
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Filer:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Filed as Large Entity	
Filing Fees for Utility under 35 USC 111(a)	

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	36033803
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	16-MAY-2019
Filing Date:	03-APR-2017
Time Stamp:	18:53:17
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$240
RAM confirmation Number	051719INTEFSW00017978500393
Deposit Account	500393
Authorized User	Lisa Puccinelli
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794USDC_IDS_05-16-19.pdf	250249 3c19b50b60a8af70911f436532492d84d40de0e0	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
	Transmittal Letter		1	1	
Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	Ref_CN-D_OA_02-19-19.pdf	693594 8ba3572346c45a7f9c661437360e3291819b8597	no	18
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30494 a5346556719a704f0873e23dc82c32445554c9c8	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	974337		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293	2892

31817 7590 04/03/2019

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
GALVIN III, JOSEPH M	

ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
04/03/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 15/477,506	Applicant(s) Boyanov et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 03/01/2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-7 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-7 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/03/2017 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☑ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 12/28/2018 01/29/2019.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Response to Amendment

The amendment, filed 03/01/2019, has been entered. Claims 1-7 are pending in this application.

Response to Arguments

Applicant's arguments filed 03/01/2019 have been fully considered but they are not persuasive.

Applicants argue, on page 5, that they do not understand metallic layer (62') as being on a sidewall of dielectric layer (52) of Yang.

Applicant's arguments are not persuasive, for the metallic layer (62') is on the diffusion barrier layer (58), which is on the sidewall of the dielectric layer (52), and therefore the metallic layer (62') is on the dielectric layer (52). Stated more clearly, the metallic layer (62') is indirectly on the dielectric layer (52). This rationale flows from the same notion that a drinking glass, resting on a coaster which is on a table, is still on a table. Therefore, the metallic layer (62') of Yang, is on the dielectric sidewall (52).

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject

matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yang et al (US 2009/0200668 hereinafter Yang) in view of Moreau et al (US 2010/0171219 hereinafter Moreau).

With respect to claim 1, Yang (Figs. 2A-2G) teaches an apparatus, comprising:

at least one first conductive line (60 Left) in a dielectric layer (52) over a substrate (not shown), the dielectric layer (52) having a top boundary; (Fig. 2G, [0053-0054] the dielectric layer is formed over a substrate, [0070] the conductive line)

a channel in the dielectric layer (52) on the at least one first conductive line (60 Left), the channel comprising a sidewall of the dielectric layer between the at least one first conductive line (60 Left) and the top boundary, (Fig. 2D [0070-71] the channel in the dielectric layer (52) is formed above the first conductive line and comprises a sidewall of the dielectric layer) and

a first capping layer (62' Left) comprising cobalt deposited in the channel on the at least one first conductive line (60 Left) comprising copper and the first capping layer (62' left) on the sidewall of the dielectric to prevent electromigration, wherein a top of the first capping layer (62') is not higher than the top boundary (52). (Figs. 2F-2G [0070-0077] the capping layer (62') comprises cobalt, and is formed on the first conductive line comprising copper or a Cu alloy and is not higher than the top boundary of the dielectric (52) and is formed indirectly on the sidewall of the dielectric.

Yang teaches wherein the first conductive line comprises copper or a copper alloy, but fails to explicitly disclose wherein the first conductive line comprises copper and cobalt.

Moreau, in a related art application, teaches a copper interconnect formed of copper of a copper alloy, and teaches copper cobalt (CuCo) is a well-known copper alloy that can be used as the material for a copper interconnect. ([0074])

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to utilize the CuCo alloy of Moreau as the copper alloy of Yang, as this is a well-known copper alloy for use as an interconnect in the semiconductor art that can provide similar and improved performance. ([0074]) See MPEP 2143 (B) Simple substitution of one known element for another to obtain predictable results

With respect to claim 2, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, wherein the first capping layer (62' Left) is self-aligned to the first conductive line (60 Left). (Figs. 2F-2G, [0074-0075])

With respect to claim 3, Yang (Figs. 2A-2G) in view of Moreau teaches The apparatus of claim 1, further comprising a second capping layer (62' Middle) selectively deposited on the second conductive line (60 Middle) within second sidewalls of the dielectric layer (52), the second conductive line (60 Middle) being at a first spacing from the at least one first conductive line (60 Left), and wherein the second capping layer (62' Middle) is at the first spacing from the first capping layer (62' Left). (Figs. 2F-2G [0070-0077] the second conductive line and capping layer have the same spacing form the first conductive line and capping layer.)

With respect to claim 6, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, wherein the at least one first conductive line is an interconnect

incorporated into a data processing system. ([0002-0008] the interconnect is part of a data processing system)

Claims 4-5 and 7 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yang in view of Moreau further in view of Beck (US 2006/0205204 hereinafter Beck).

With respect to claim 4, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, wherein the dielectric layer is between 50 to 1000nm and the openings may extend completely through the dielectric, ([0062-0063]) and further recessing the conductive line (60) from a top surface of the dielectric layer (52) so that the capping layer (62') is not above the dielectric. (Figs. 2C-2F)

Yang in view of Moreau fails to explicitly disclose wherein the at least first conductive line is at a depth from 5 nanometers to 50 nanometers from a top surface of the dielectric layer.

Beck (Figs. 3-10), in a related art application, teaches wherein the first conductive line (116) is at a depth from 5-20 nanometers from a top surface of the dielectric layer (106). (Fig. 10 [0046-61]) See MPEP 2144.05 In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to form the conductive line of Yang in view of Moreau to be at a depth between 5-50 nanometers from a top surface of the dielectric layer, as Beck teaches this is a well-known thickness for a cobalt capping layer in the semiconductor

art, which is readily applied to the conductive line with similar dimensions of Yang in view of Moreau. ([0046-0061]) See MPEP 2143 (C) Use of known technique to improve similar devices (methods, or products) in the same way

With respect to claim 5, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, but fails to explicitly disclose wherein the first conductive line is at a depth from a top surface of the dielectric layer that is from 10% to 50% of the thickness of the first conductive line. (Though one of ordinary skill in the art could arrive at this limitation based on the relationship between Fig. 2G and the thicknesses given in [0060-0077] through routine experimentation)

Beck (Figs. 3-10), in a related art application, teaches wherein the first conductive line (116) is at a depth from a top surface of the dielectric layer (106) that is from 10% to 50% of the thickness of the first conductive line (116). ([0040] the first conductive line is a depth of 100nm from the top surface of the dielectric layer (106), [0046-0061] the first conductive layer is recessed to a depth of between 5-20nm for the formation of the capping layer. Therefore the first conductive line is from 5% to 20% is at a depth from a top surface of the dielectric layer.) See MPEP 2144.05 In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to form the conductive line of Yang in view of Moreau to be at a depth between 10% to 50% of the thickness of the conductive line from a top surface of the dielectric layer, as Beck teaches this is a well-known thickness for a cobalt

capping layer in the semiconductor art, which is readily applied to the conductive line with similar dimensions of Yang in view of Moreau. ([0046-0061]) See MPEP 2143 (C) Use of known technique to improve similar devices (methods, or products) in the same way

With respect to claim 7, Yang (Figs. 2A-2G) in view of Moreau teaches The apparatus of claim 1, but fails to explicitly disclose wherein a spacing between the at least one first conductive line and a second conductive line in the dielectric layer is from 5 nm to 500 nm.

Beck, in a related art application, teaches it is well-known in the art to form interconnects as close as possible to one another to maximize connections, which is typically 90 to 100nm or 65-70nm. ([0062]) See MPEP 2144.05 In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to form the first and second conductive lines to be between 5nm and 500nm apart, as these are well-known distances for metal line spacing in the semiconductor art, which allows for the maximum number of interconnects. ([0062]) See MPEP 2143 (C) Use of known technique to improve similar devices (methods, or products) in the same way

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH M GALVIN III whose telephone number is (571)272-0559. The examiner can normally be reached on M-F: 8:30AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 5712721864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOSEPH M GALVIN III/
Primary Examiner, Art Unit 2898

Notice of References Cited	Application/Control No. 15/477,506	Applicant(s)/Patent Under Reexamination Boyanov et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090200668-A1	08-2009	Yang; Chih-Chao	H01L21/76834	257/751
*	B	US-20100171219-A1	07-2010	Moreau; David	H01L21/76834	257/751
*	C	US-20060205204-A1	09-2006	Beck; Michael	H01L21/7684	438/628
	D					
	E					
	F					
	G					
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	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	Art Unit
	JOSEPH M GALVIN III	2898

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/26/2018	03/29/2019							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	Art Unit
	JOSEPH M GALVIN III	2898

CPC - Searched*		
Symbol	Date	Examiner
H01L21/76802,7684,76849,7685,76879,76883	11/26/2018	JG
H01L23/485,5226,528,53209,53238,53295	11/26/2018	JG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EASTsearch	11/26/2018	JG
updated EAST search	03/29/2019	JG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	160	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
L2	55664	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
L3	17972	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
L4	10028	L3 and cap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
L5	2289	L4 and L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
L6	406	L5 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 15:46
L10	160	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2019/03/29 16:03
S1	1	"15477506"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:31
S2	53238	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:54
S3	158	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/11/26 08:54

			EPO; JPO; DERWENT			
S4	36636	((("INTEL") near3 ("CORPORATION"))).AS,AANM.	USPAT	OR	OFF	2018/11/26 08:54
S5	20	("8043958" "6348731" "6114238" "6046108" "7396757" "6908847" "5470789").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:57
S6	3	"20080027677"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:00
S11	3	"20070049008"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/26 09:03
S12	2	"20090200668"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:05
S13	193	(CuCo copper near2 cobalt) with interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:22
S14	17544	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:24
S15	9779	S14 and cap$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:25
S17	2228	S15 and S2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:25
S18	391	S17 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:59

EAST Search History (Interference)

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3/ 29/ 2019 4:19:24 PM
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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2892
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed November 1, 2018, 7 pages.	X
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed December 27, 2018, 5 pages.	x

EXAMINER /JOSEPH M GALVIN III/ **DATE CONSIDERED** 03/29/2019

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boiyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed September 28, 2018, 40 pages.	X

EXAMINER /JOSEPH M GALVIN III/ **DATE CONSIDERED** 03/29/2019

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	
Boyan Boyanov	Examiner: Galvin III, Joseph M.
Application No.: 15/477,506	Art Unit: 2898
Filed: April 3, 2017	Confirmation No.: 2892
For: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Dear Sir:

This is in response to the Office Action mailed December 4, 2018. Applicant respectfully requests the Examiner to enter the following amendments and consider the following remarks.

The Listing of Claims begins on page 2 of this paper.

Remarks/Arguments begin on page 4 of this paper.

Listing of Claims:

1. (Currently Amended) An apparatus, comprising:

at least one first conductive line in a dielectric layer over a substrate, the dielectric layer having a top boundary;

a channel in the dielectric layer on the at least one first conductive line, the channel comprising a sidewall of the dielectric layer between the at least one first conductive line and the top boundary, and

a first capping layer comprising cobalt deposited in the channel on the at least one first conductive line comprising copper and cobalt, the first capping layer [[and]] on the sidewall of the dielectric layer to prevent electromigration, wherein a top of the first capping layer is not higher than the top boundary.

2. (Original) The apparatus of claim 1, wherein the first capping layer is self-aligned to the first conductive line.

3. (Currently Amended) The apparatus of claim 1, further comprising

a second capping layer selectively deposited on [[the]] a second conductive line within second sidewalls of the dielectric layer, the second conductive line being at a first spacing from the at least one first conductive line, and wherein the second capping layer is at the first spacing from the first capping layer.

4. (Original) The apparatus of claim 1, wherein the at least first conductive line is at a depth from 5 nanometers to 50 nanometers from a top surface of the dielectric layer.

5. (Original) The apparatus of claim 1, wherein the first conductive line is at a depth from a top surface of the dielectric layer that is from 10% to 50% of the thickness of the first conductive line.

6. (Original) The apparatus of claim 1, wherein the at least one first conductive line is an interconnect incorporated into a data processing system.

7. (Original) The apparatus of claim 1, wherein a spacing between the at least one first conductive line and a second conductive line in the dielectric layer is from 5 nm to 500 nm.

REMARKS

Claim Rejections - 35 USC § 112

Claim 3 recites the limitation "the second conductive line" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Applicant herein amends claim 3, and respectfully requests that the Examiner remove the rejection of claim 3 in view of the amendments.

Claim Rejections – 35 U.S.C. § 103

Claims 1-3 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang et al.* (US 2009/0200668) in view of *Moreau et al.* (US 2010/0171219) Claims 4-5 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Yang et al.* in view of *Moreau et al.* further in view of *Beck* (US 2006/0205204).

Applicant herein amends independent claim 1, from which claims 2-7 depend, and respectfully request reconsideration of claims 1-7 in view of the amendments and the following arguments.

Amended independent claim 1 is directed to an apparatus, including the features, "*at least one first conductive line in a dielectric layer over a substrate, the dielectric layer having a top boundary*," "*a channel in the dielectric layer on the at least one first conductive line, the channel comprising a sidewall of the dielectric layer between the at least one first conductive line and the top boundary,* ***and a first capping layer comprising cobalt*** *deposited in the channel* ***on the at least one first conductive line comprising copper*** *and cobalt,* ***the first capping layer on the sidewall of the dielectric layer*** *to prevent electromigration, wherein a top of the first capping layer is not higher than the top boundary*." (Emphasis added.)

That is, Applicant teaches, and claims in claims 1-7, an apparatus including a capping layer comprising cobalt on a conductive line comprising copper, the capping layer comprising cobalt on a sidewall of a dielectric layer. Applicant does not understand the cited references of record as disclosing at least this feature of Applicant's claims 1-7.

Applicant understands Yang as disclosing an interconnect structure formed in a dielectric material 52. The interconnect structure includes a diffusion barrier 58, a conductive material 60, and a metallic layer 62'. The metallic layer 62' may include cobalt. (*See* Yang, e.g., Paragraph 0073, and Figure 2F, shown below.)

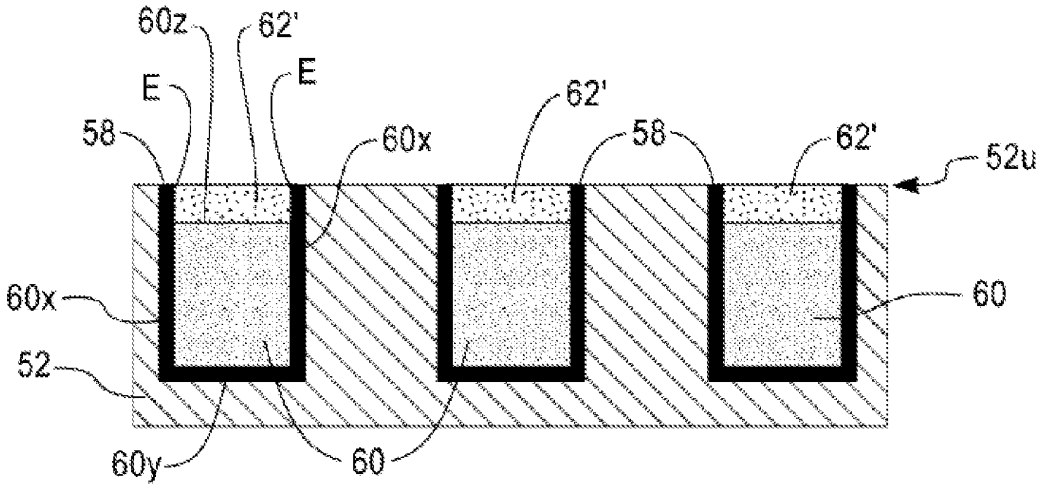


FIG. 2F

Figure 2F of Yang.

However, Applicant understands the metallic layer 62' as being on a sidewall of diffusion barrier 58 of Yang. That is, Applicant does not understand metallic layer 62' as being on a sidewall of dielectric layer 52 of Yang, as is required by Applicant's claims 1-7.

Furthermore, with respect to amended independent claim 1, Applicant does not understand the other cited references of record as curing the above noted deficiencies of Yang. Accordingly, Applicant respectfully requests that the Examiner remove the rejections of claims 1-7.

CONCLUSION

The Examiner is respectfully requested to contact the undersigned by telephone if it is believed that such contact would further the examination of the present application.

Pursuant to 37 C.F.R. 1.136(a)(3), the Applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 50-0393.

Respectfully submitted,

SCHWABE WILLIAMSON & WYATT

March 1, 2019	/Michael A. Bernadicou/
Date	Michael A. Bernadicou Reg. No. 35,934

1211 SW 5th, Ste. 1900
Portland, OR 97204
Telephone: 503.222.9981
Facsimile: 503.796.9200

Electronic Acknowledgement Receipt	
EFS ID:	35302935
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	01-MAR-2019
Filing Date:	03-APR-2017
Time Stamp:	19:05:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Intel_P38794USDC_ROA_03_01_19.pdf	155934 8fc43d0f82bffa311189fa2d87ed63c96f7ebf4c	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	3
	Applicant Arguments/Remarks Made in an Amendment	4	7
Warnings:			
Information:			
	Total Files Size (in bytes):	155934	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/477,506	Filing Date 04/03/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	03/01/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 7	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/ROBERT J TALBERT/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2892
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed November 1, 2018, 7 pages.	X
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed December 27, 2018, 5 pages.	x

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	34998008
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	29-JAN-2019
Filing Date:	03-APR-2017
Time Stamp:	17:49:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794USDC_IDS_01-29-19.pdf	295382 3683b2d3a63f470321818bbbd3a10ec00590d058	yes	2

	Multipart Description/PDF files in .zip description			
	Document Description	**Start**	**End**	
	Transmittal Letter	1	1	
	Information Disclosure Statement (IDS) Form (SB08)	2	2	
Warnings:				
Information:				
2	Other Reference-Patent/App/Search documents	Ref_KR-D2-D2_OA_11-01-18.pdf	2952726 6401ae7f3f8d8b09d6d8f5425a8078e1d863eae6	no	7
Warnings:				
Information:				
3	Other Reference-Patent/App/Search documents	Ref_KR-D2-D2_OA_12-27-18.pdf	546406 1b38156d4af44a02a04915c2e1d888e87c416d79	no	5
Warnings:				
Information:				
		Total Files Size (in bytes):	3794514	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyanov, et al.
Art Unit	2898
Examiner Name	Galvin III, Joseph M.
Attorney Docket No.	P38794USDC Conf. No. 2892

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of a final Office Action or Notice of Allowance. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☐ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	01-29-2019
Name/Print	Michael A. Bernadicou	Registration Number	35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 01-29-19

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boiyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed September 28, 2018, 40 pages.	X

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	34716063
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	28-DEC-2018
Filing Date:	03-APR-2017
Time Stamp:	16:49:56
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794US_IDS_12-28-18.pdf	239323 f3d1ee05b6c745e8550035fcb96e2b34509c078c	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Transmittal Letter	1	1
	Information Disclosure Statement (IDS) Form (SB08)	2	2

Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	Ref_P38794CN-D_OA_09-28-18.pdf	18625171 2b5abcef7894fd9d76a52e0dd684e078ec195300	no	40
Warnings:					
Information:					
		Total Files Size (in bytes):	18864494		

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New International Application Filed with the USPTO as a Receiving Office

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyanov, et al.
Art Unit	2898
Examiner Name	Galvin III, Joseph M.
Attorney Docket No.	P38794USDC Conf. No. 2892

DUTY OF DISCLOSURE STATEMENT

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OR

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OR

☐ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	12-28-2018
Name/Print	Michael A. Bernadicou	Registration Number	35934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 12-28-2018

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/477,506	04/03/2017	Boyan Boyanov	P38794USDC 111548-227293	2892

31817 7590 12/04/2018

SCHWABE, WILLIAMSON & WYATT, P.C.
1211 SW 5th Avenue, Suite 1600
Portland, OR 97204

EXAMINER	
GALVIN III, JOSEPH M	

ART UNIT	PAPER NUMBER
2898	

NOTIFICATION DATE	DELIVERY MODE
12/04/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

IPDocketing@SCHWABE.com
intelparalegal@schwabe.com

PTOL-90A (Rev. 04/07)

Office Action Summary	Application No. 15/477,506	Applicant(s) Boyanov et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/03/2017.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-7 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-7 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/03/2017 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☑ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☑ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☑ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date See Continuation Sheet.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Continuation of Attachment(s) 2) Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date: 04/03/2017, 04/17/2017, 05/25/2017, 12/12/2017, 03/05/2018, 06/08/2018, 06/15/2018, 10/05/2018

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 3 recites the limitation "the second conductive line" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yang et al (US 2009/0200668 hereinafter Yang) in view of Moreau et al (US 2010/0171219 hereinafter Moreau).

With respect to claim 1, Yang (Figs. 2A-2G) teaches an apparatus, comprising:

at least one first conductive line (60 Left) in a dielectric layer (52) over a substrate (not shown), the dielectric layer (52) having a top boundary; (Fig. 2G, [0053-0054] the dielectric layer is formed over a substrate, [0070] the conductive line)

a channel in the dielectric layer (52) on the at least one first conductive line (60 Left), the channel comprising a sidewall between the at least one first conductive line (60 Left) and the top boundary, (Fig. 2D [0070-71] the channel in the dielectric layer (52) is formed above the first conductive line) and

a first capping layer (62' Left) comprising cobalt deposited in the channel on the at least one first conductive line (60 Left) comprising copper and on the sidewall to prevent electromigration, wherein a top of the first capping layer (62') is not higher than the top boundary (52). (Figs. 2F-2G [0070-0077] the capping layer (62') comprises cobalt, and is formed on the first conductive line comprising copper or a Cu alloy and is not higher than the top boundary of the dielectric (52).

Yang teaches wherein the first conductive line comprises copper or a copper alloy, but fails to explicitly disclose wherein the first conductive line comprises copper and cobalt.

Moreau, in a related art application, teaches a copper interconnect formed of copper of a copper alloy, and teaches copper cobalt (CuCo) is a well-known copper alloy that can be used as the material for a copper interconnect. ([0074])

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to utilize the CuCo alloy of Moreau as the copper alloy of Yang, as this is a well-known copper alloy for use as an interconnect in the semiconductor art that can provide similar and improved performance. ([0074]) See

MPEP 2143 (B) Simple substitution of one known element for another to obtain predictable results

With respect to claim 2, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, wherein the first capping layer (62' Left) is self-aligned to the first conductive line (60 Left). (Figs. 2F-2G, [0074-0075])

With respect to claim 3, Yang (Figs. 2A-2G) in view of Moreau teaches The apparatus of claim 1, further comprising a second capping layer (62' Middle) selectively deposited on the second conductive line (60 Middle) within second sidewalls of the dielectric layer (52), the second conductive line (60 Middle) being at a first spacing from the at least one first conductive line (60 Left), and wherein the second capping layer (62' Middle) is at the first spacing from the first capping layer (62' Left). (Figs. 2F-2G [0070-0077] the second conductive line and capping layer have the same spacing form the first conductive line and capping layer.)

With respect to claim 6, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, wherein the at least one first conductive line is an interconnect incorporated into a data processing system. ([0002-0008] the interconnect is part of a data processing system)

Claims 4-5 and 7 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Yang in view of Moreau further in view of Beck (US 2006/0205204 hereinafter Beck).

With respect to claim 4, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, wherein the dielectric layer is between 50 to 1000nm and the openings may extend completely through the dielectric, ([0062-0063]) and further

recessing the conductive line (60) from a top surface of the dielectric layer (52) so that the capping layer (62') is not above the dielectric. (Figs. 2C-2F)

Yang in view of Moreau fails to explicitly disclose wherein the at least first conductive line is at a depth from 5 nanometers to 50 nanometers from a top surface of the dielectric layer.

Beck (Figs. 3-10), in a related art application, teaches wherein the first conductive line (116) is at a depth from 5-20 nanometers from a top surface of the dielectric layer (106). (Fig. 10 [0046-61]) See MPEP 2144.05 In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to form the conductive line of Yang in view of Moreau to be at a depth between 5-50 nanometers from a top surface of the dielectric layer, as Beck teaches this is a well-known thickness for a cobalt capping layer in the semiconductor art, which is readily applied to the conductive line with similar dimensions of Yang in view of Moreau. ([0046-0061]) See MPEP 2143 (C) Use of known technique to improve similar devices (methods, or products) in the same way

With respect to claim 5, Yang (Figs. 2A-2G) in view of Moreau teaches the apparatus of claim 1, but fails to explicitly disclose wherein the first conductive line is at a depth from a top surface of the dielectric layer that is from 10% to 50% of the thickness of the first conductive line. (Though one of ordinary skill in the art could arrive

at this limitation based on the relationship between Fig. 2G and the thicknesses given in [0060-0077] through routine experimentation)

Beck (Figs. 3-10), in a related art application, teaches wherein the first conductive line (116) is at a depth from a top surface of the dielectric layer (106) that is from 10% to 50% of the thickness of the first conductive line (116). ([0040] the first conductive line is a depth of 100nm from the top surface of the dielectric layer (106), [0046-0061] the first conductive layer is recessed to a depth of between 5-20nm for the formation of the capping layer. Therefore the first conductive line is from 5% to 20% is at a depth from a top surface of the dielectric layer.) See MPEP 2144.05 In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to form the conductive line of Yang in view of Moreau to be at a depth between 10% to 50% of the thickness of the conductive line from a top surface of the dielectric layer, as Beck teaches this is a well-known thickness for a cobalt capping layer in the semiconductor art, which is readily applied to the conductive line with similar dimensions of Yang in view of Moreau. ([0046-0061]) See MPEP 2143 (C) Use of known technique to improve similar devices (methods, or products) in the same way

With respect to claim 7, Yang (Figs. 2A-2G) in view of Moreau teaches The apparatus of claim 1, but fails to explicitly disclose wherein a spacing between the at

least one first conductive line and a second conductive line in the dielectric layer is from 5 nm to 500 nm.

Beck, in a related art application, teaches it is well-known in the art to form interconnects as close as possible to one another to maximize connections, which is typically 90 to 100nm or 65-70nm. ([0062]) See MPEP 2144.05 In the case where the claimed ranges "overlap or lie inside ranges disclosed by the prior art" a prima facie case of obviousness exists. In re Wertheim, 541 F.2d 257, 191 USPQ 90 (CCPA 1976); In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990)

It would have been obvious to one of ordinary skill in the art prior to the effective filing date of the invention to form the first and second conductive lines to be between 5nm and 500nm apart, as these are well-known distances for metal line spacing in the semiconductor art, which allows for the maximum number of interconnects. ([0062]) See MPEP 2143 (C) Use of known technique to improve similar devices (methods, or products) in the same way

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOSEPH M GALVIN III whose telephone number is (571)272-0559. The examiner can normally be reached on M-F: 8:30AM-5PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Julio Maldonado can be reached on 5712721864. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JOSEPH M GALVIN III/
Primary Examiner, Art Unit 2898

Notice of References Cited	Application/Control No. 15/477,506	Applicant(s)/Patent Under Reexamination Boyanov et al.	
	Examiner JOSEPH M GALVIN III	Art Unit 2898	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20090200668-A1	08-2009	Yang; Chih-Chao	H01L21/76834	257/751
*	B	US-20100171219-A1	07-2010	Moreau; David	H01L21/76834	257/751
*	C	US-20060205204-A1	09-2006	Beck; Michael	H01L21/7684	438/628
	D					
	E					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	Art Unit
	JOSEPH M GALVIN III	2898

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/26/2018								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/477,506	Boyanov et al.
	Examiner	Art Unit
	JOSEPH M GALVIN III	2898

CPC - Searched*		
Symbol	Date	Examiner
H01L21/76802,7684,76849,7685,76879,76883	11/26/2018	JG
H01L23/485,5226,528,53209,53238,53295	11/26/2018	JG

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EASTsearch	11/26/2018	JG

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/JOSEPH M GALVIN III/ Primary Examiner, Art Unit 2898	

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov
	Group Art Unit	2898
	Examiner Name	Not yet assigned
Sheet 1 of 1	Attorney Docket No: 42P38794DC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		KR 1020100109932	10-11-2010	International Business Machines Corporation		X
		WO 2009098120A1	08-13-2009	International Business Machines Corporation		
		JP 2009506536A	02-12-2009	Freescale Semiconductor		X
		WO 2007024470A2	03-01-2007	Freescale Semiconductor		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Application Number	Not yet assigned
				Filing Date	April 3, 2017
				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	1	of	5	Attorney Docket Number	42P38794DC

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number: Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	5,470,789	11-28-1995	Misawa	
		US-				
		US-				

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	Not yet assigned
				Filing Date	April 3, 2017
				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	2	of	5	Attorney Docket Number	42P38794DC

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-	7,338,908	03-04-2008	Koos et al.	
		US-	7,396,759 B1	07-08-2008	Van Schravendijk Bart et al.	
		US-	2005-0001325	01-06-2005	Andricacos et al.	
		US-	2006/0128144 A1	06-15-2006	Hyun-Mog Park et al.	
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NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		OTA, Takashi, et al., "Experimental Evaluation of Out-of-Plane Distortion of Electrostatically Chucked EUV Reticle," Proc. Of SPIE Vol. 6921, 69213S, (2008)	
		M.M ANTONIJEVIC et al., "Copper Corrosion Inhibitors. A review", Int. J. Electrochem Sci., Vol. 3, 2008, 28 pages.	
		T. SAITO et al., 'A Robust, Deep-Submicron Copper Interconnect Structure using Self-Aligned Metal Capping Method", IEEE, 2004, 3 pages.	
		PCT International Search Report and Written Opinion for PCT/US2011/059453, mailed July 16, 2012 (14 pp.).	
		Taiwan Patent Application No. 101140536, Office Action and Taiwan IPO Search Report (with English translation), dated November 27, 2014, (15 pages) [P38794TW].	
		International Preliminary Report on Patentability (Chapter 1 of the Patent Cooperation Treaty) for PCT/US2011/059453, mailed May 6, 2014 (8 pages).	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	Not yet assigned
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				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	3	of	5	Attorney Docket Number	42P38794DC

U.S. PATENT DOCUMENTS

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		US-			
		US-			
		US-			
		US-			

NON PATENT LITERATURE DOCUMENTS

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	NPL1	Chih-Kai Hsu "Electromigration Study on Sn capped Air-gap Cu Damascenes Structure", 2006.	
	NPL2	Korean Patent Application No. 10-2014-7015212, Office Action (with English translation), dated August 3, 2015 (14 pages) [P38794KR].	
	NPL3	Taiwan (R.O.C.) Patent Application No. 101140536, Office Action (with English translation), dated August 13, 2015, (17 pages) [P38794TW].	
	NPL4	China Patent Application No. 201180074611.5, Office Action (with English translation), dated November 16, 2015, (20 pages) [P38794CN].	

Examiner Signature	/JOSEPH M GALVIN III/	Date Considered	11/26/2018

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Substitute for Form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(use as many sheets as necessary)*				Application Number	Not yet assigned
				Filing Date	April 3, 2017
				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	4	of	5	Attorney Docket Number	42P38794DC

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number / Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

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	NPL1	Korea Patent Application No. 10-2014-7016212, Notice of Allowance (Allowed Claims in English) mailed March 2, 2016, 4 pages [Atty Docket: P38794KR]	
	NPL2	Korea Patent Application No. 10-2016-7003215, Notice of Preliminary Rejection (Office and Claims in English) mailed April 1, 2016, 7 pages [Atty Docket: P38794KR-D]	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known	
Application Number	Not yet assigned
Filing Date	April 3, 2017
First Named Inventor:	Boyan BOYANOV
Art Unit	Not yet assigned
Examiner Name	Not yet assigned
Attorney Docket Number	42P38794DC

Sheet	5	of	5

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,470,789	11-1995	Misawa	
		US- 2009/0283499	11-2009	Mayer et al.	
		US- 2010/0081276 A1	04-2010	Ishizaka	
		US- 2009/0283499 A1	11-2009	Mayer	
		US 2010/0081276 A1	04-2010	Mishizaka	
		US 2009/0283499 A1	11-2009	Mayer	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T*
		WO 2002/045142 A2	06/06/2002	Christopher THOMAS, et al.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
	NPL1	Korean Patent Application No. 10-2016-7003215, Office Action (with English translation), dated April 1, 2016 (5 pages) [P38794KR-D].	
	NPL2	Taiwan (R.O.C.) Patent Application No. 101140536, Office Action (with English translation), dated April 19, 2016, (14 pages) [P38794TW].	

Examiner Signature	/JOSEPH M GALVIN III/	Date Considered	11/26/2018

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Base ADF REFERENCES CONSIDERED by EXAMINER, WHERE FILED IN IFW on 11/26/2018.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"15477506"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:31
L2	53238	(H01L21/76802 OR H01L21/7684 OR H01L21/76849 OR H01L21/7685 OR H01L21/76879 OR H01L21/76883 OR H01L23/485 OR H01L23/5226 OR H01L23/528 OR H01L23/53209 OR H01L23/53238 OR H01L23/53295).CPC.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:54
L3	158	((("BOYANOV") near3 ("Boyan")) OR (("SINGH") near3 ("Kanwal"))).INV.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:54
L4	36636	((("INTEL") near3 ("CORPORATION"))).AS,AANM.	USPAT	OR	OFF	2018/11/26 08:54
L5	20	("8043958" "6348731" "6114238" "6046108" "7396757" "6908847" "5470789").pn.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 08:57
L6	3	"20080027677"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:00
L11	3	"20070049008"	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/26 09:03
L12	2	"20090200668"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:05
L13	193	(CuCo copper near2 cobalt) with interconnect	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:22
L14	17544	copper with line and dielectric and substrate	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:24
L15	9779	14 and cap$4	US-PGPUB; USPAT; USOCR;	OR	OFF	2018/11/26 09:25

			EPO; JPO; DERWENT			
L17	2228	15 and 2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:25
L18	391	17 and spacing	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	OFF	2018/11/26 09:59

EAST Search History (Interference)

< This search history is empty>

11/ 26/ 2018 11:11:27 AM
C:\ Users\ jgalvin\ Documents\ EAST\ Workspaces\ 15477506.wsp

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	FORTICH, RODOLFO D
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 7,396,757	07-08-2008	IBM CORP	
		US6,908,847	06-21-2005	SAITO, TATSUYUKI, ET AL.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		KR-1020090085066	08-06-2009	IBM		X
		CN-101490825A	07-22-2009	IBM		X
		CN-1420560	05-28-2003	HITACHI LTD		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		4th Non-Final Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) mailed September 12, 2017, 7 pgs., with English translation.	X
		1st Non-Final Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CND) mailed August 28, 2017, 10 pgs., with English translation.	X
		Final Office Action for Korean Patent Application 10-2016-7033745 (Attorney Docket No. P38794KRD2) mailed July 18, 2017, 5 pgs., with English translation.	x

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional) [2] Applicant is to place a check mark here if English language Translation is attached

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US-8,043,958	10/25/2011	Jonathan D. Reid, et al.	
		US-6,348,731	02/19/2002	Leon Ashley, et al.	
		US-6,114,238	09/05/2000	Kuan-Yang Liao	
		US-6,046,108	04/04/2000	Chung-Shi Liu, et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		Office Action from Taiwan Patent Application No. 106120928 (Attorney Docket No. P38794TW-D1), mailed July 7, 2018, 15 pages, with English Translation..	X
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. P38794KR-D2-D1), mailed September 27, 2018, 6 pages, with English Translation.	X

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.M.G/

Bibliographic Data

Application No: 15/477,506

Foreign Priority claimed: (•) Yes ( ) No

35 USC 119 (a-d) conditions met: [✓] Yes [ ] No [ ] Met After Allowance

Verified and Acknowledged: /JOSEPH M GALVIN III/ Examiner's Signature [ ] Initials

Title: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/03/2017	257	2898	P38794USDC 111548-227293
RULE			

APPLICANTS

INTEL CORPORATION, Santa Clara, CA,

INVENTORS

Boyan Boyanov Portland, OR, UNITED STATES

Kanwal Jit Singh Hilsboro, OR, UNITED STATES

CONTINUING DATA

This application is a CON of 14675613 03/31/2015 PAT 9627321

14675613 is a DIV of 13991899 06/05/2013 PAT 9373584

13991899 is a 371 of PCT/US2011/059453 11/04/2011

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

04/12/2017

STATE OR COUNTRY

UNITED STATES

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Portland, OR 97204

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	FORTICH, RODOLFO D
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

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		2nd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed July 1, 2016, 21 pgs., with English translation.	X
		3rd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed December 20, 2016, 11 pgs., with English translation.	X
		Notice of Final Rejection for Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2) Mailed December 5, 2017, 6 pgs., with English translation.	X

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Fortich, Rodolfo D.
Sheet 1 of 2	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		JP 6-275612A	9/30/1994	Misawa, Nobuhiro		
		CN 1364311A	8/14/2002	Kun, Hu Chao et al.		
		CN 1921102A	2/28/2007	Shih, Chien-Hsueh		
		JP 3326698	9/24/2002	Misawa Nobuhiro		

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Fortich, Rodolfo D.
Sheet 2 of 2	Attorney Docket No: P38794USDC	

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	**Cite No [1]**	**Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.**	**T[2]**
		Notice of Allowance from Korean Patent Application No. 10-2016-7003215 (Attorney Docket No. P38794KR-D), mailed September 2, 2016, 2 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed March 2, 2017, 9 pages.	
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. P38794KR-D2-D1), mailed April 23, 2018, 10 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed March 15, 2018 6 pages.	
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed May 1, 2018, 13 pages.	
		Office Action from Korean Patent Application No.10-2014-7015212 (Attorney Docket No. P38794KR), mailed January 7, 2016, 8 pages.	
		Office Action from Taiwan Patent Application No. 101140536 (Attorney Docket No. P38794TW), mailed March 22, 2017, 4 pages.	
		Office Action from Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN), mailed April 25, 2017, 19 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed February 20, 2018, 8 pages.	
		Notice of Allowance from Taiwan Patent Application No. 101140536 (Attorney Docket No. P38794TW), mailed June 29, 2017, 2 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed April 10, 2015, 7 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed April 10, 2015, 7 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed November 3, 2014, 7 pages.	
		Office Action from US Patent Application No. 14/675,613 (Attorney Docket No. P38794USD) mailed July 5, 2016, 6 pages.	
		Office Action from US Patent Application No. 14/675,613 (Attorney Docket No. P38794USD) mailed January 29, 2016, 8 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed June 28, 2017.	

EXAMINER	/JOSEPH M GALVIN III/	**DATE CONSIDERED**	11/30/2018

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
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Substitute for form 1449A/PTO	*Complete if Known*	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov
	Group Art Unit	2898
	Examiner Name	Not yet assigned
Sheet 1 of 1	Attorney Docket No: 42P38794DC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]
		CN 1575508A	02-02-2005	Christopher Thomas et al.		*

*= Machine Translation in English

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Fortich, Rodolfo D.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

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		Office Action for Chinese Patent Application 201180074611.5 (Attorney Docket No. P38794CN), mailed March 9, 2018, 7 pages.	X

EXAMINER	/JOSEPH M GALVIN III/	DATE CONSIDERED	11/26/2018

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	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Galvin III, Joseph M.
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

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		US-8,043,958	10/25/2011	Jonathan D. Reid, et al.	
		US-6,348,731	02/19/2002	Leon Ashley, et al.	
		US-6,114,238	09/05/2000	Kuan-Yang Liao	
		US-6,046,108	04/04/2000	Chung-Shi Liu, et al.	

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Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

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		Office Action from Taiwan Patent Application No. 106120928 (Attorney Docket No. P38794TW-D1), mailed July 7, 2018, 15 pages, with English Translation..	X
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. P38794KR-D2-D1), mailed September 27, 2018, 6 pages, with English Translation.	X

EXAMINER **DATE CONSIDERED**

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	33936399
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Justin K. Brask/Sheri Villarreal
Filer Authorized By:	Justin K. Brask
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	05-OCT-2018
Filing Date:	03-APR-2017
Time Stamp:	18:49:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794USDC_IDS_10_05_18.pdf	347135 dd926771605384967a5e272dc5940a2a11431986	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Non Patent Literature	P38794KR-D2-D1_OA_09_27_18.pdf	382952 6c4ad29116da3650425a54dd869c644ad17699e5	no	6
Warnings:					
Information:					
3	Non Patent Literature	P38794TW-D1_OA_07_06_18.pdf	2779861 e81f233633911e053bdd6a8137660d790eca39fc	no	15
Warnings:					
Information:					
		Total Files Size (in bytes):	3509948		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyan Boyanov, et al.
Art Unit	2898
Examiner Name	Galvin III, Joseph M.
Attorney Docket No.	P38794USDC 111548-227293

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has bee n made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☐ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	10-05-2018
Name/Print	Justin K. Brask	Registration Number	61080

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	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Fortich, Rodolfo D.
Sheet 1 of 2	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS					
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		JP 6-275612A	9/30/1994	Misawa, Nobuhiro		
		CN 1364311A	8/14/2002	Kun, Hu Chao et al.		
		CN 1921102A	2/28/2007	Shih, Chien-Hsueh		
		JP 3326698	9/24/2002	Misawa Nobuhiro		

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		Notice of Allowance from Korean Patent Application No. 10-2016-7003215 (Attorney Docket No. P38794KR-D), mailed September 2, 2016, 2 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed March 2, 2017, 9 pages.	
		Office Action from Korean Patent Application No. 10-2018-7003480 (Attorney Docket No. P38794KR-D2-D1), mailed April 23, 2018, 10 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed March 15, 2018 6 pages.	
		Office Action from Korean Patent Application No. 10-2018-7008361 (Attorney Docket No. P38794KR-D2-D2), mailed May 1, 2018, 13 pages.	
		Office Action from Korean Patent Application No.10-2014-7015212 (Attorney Docket No. P38794KR), mailed January 7, 2016, 8 pages.	
		Office Action from Taiwan Patent Application No. 101140536 (Attorney Docket No. P38794TW), mailed March 22, 2017, 4 pages.	
		Office Action from Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN), mailed April 25, 2017, 19 pages.	
		Office Action from Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2), mailed February 20, 2018, 8 pages.	
		Notice of Allowance from Taiwan Patent Application No. 101140536 (Attorney Docket No. P38794TW), mailed June 29, 2017, 2 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed April 10, 2015, 7 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed April 10, 2015, 7 pages.	
		Office Action from US Patent Application No. 13/991,899 (Attorney Docket No. P38794US) mailed November 3, 2014, 7 pages.	
		Office Action from US Patent Application No. 14/675,613 (Attorney Docket No. P38794USD) mailed July 5, 2016, 6 pages.	
		Office Action from US Patent Application No. 14/675,613 (Attorney Docket No. P38794USD) mailed January 29, 2016, 8 pages.	
		Office Action from Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CN-D), mailed June 28, 2017.	

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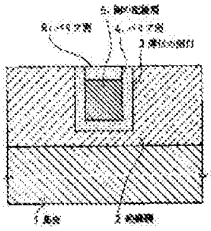
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Legal Status

(11)Publication number	06-275612
(43)Date of publication of application	30.09.1994
(51)Int.Cl.	H01L 21/3205 H01L 21/28 H01L 21/90 H05K 3/02
(21)Application number	05-059889
(22)Date of filing	19.03.1993
(71)Applicant	FUJITSU LTD
(72)Inventor	MISAWA NOBUHIRO



(54)MANUFACTURE OF INTEGRATED CIRCUIT DEVICE

(57)Abstract
PURPOSE: To provide a method for realizing the flattening of a copper wiring layer containing a barrier layer or of a contact without vaporizing copper compound by etching, regarding the manufacturing method of an integrated circuit device.
CONSTITUTION: A trench type aperture 3 is formed in an insulating film 2 formed on a substrate 1; a thin barrier material layer is deposited on the substrate 1 containing the aperture 3; a copper layer is deposited on the barrier material layer; the copper deposition layer and the barrier material deposition layer formed on the insulating film 2 are eliminated; the copper deposited in the trench type aperture 3 is so eliminated that a step-difference is formed whose surface is lower than the surface of the insulating film 2; thus a copper wiring layer 51 and a barrier layer 41 are formed. A barrier material layer is deposited on the substrate 1 containing the copper wiring layer 51 in the trench type aperture 3, and the barrier material deposition layer is flattened and polished, thereby forming a barrier layer 61 in a self-alignment manner on the copper wiring layer 51 in the aperture. By the similar process, a contact can be formed on the wiring substrate.

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CLAIMS

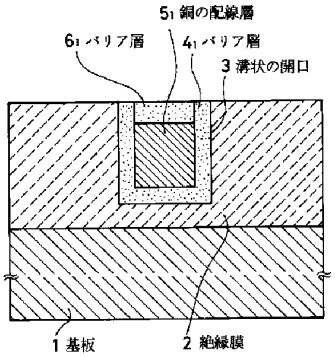
[Claim(s)]
[Claim 1]A manufacturing method of an integrated circuit device characterized by comprising the following.
A process of forming an opening in an insulator layer formed on a substrate.
A process of depositing copper sedimentary layers on the substrate containing the opening.
A process of removing copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer while removing sedimentary layers of copper deposited on the insulator layer.
A process of depositing sedimentary layers of a barrier material on a substrate containing copper in the opening.
A process of forming a barrier layer in a top surface of copper in the opening by a self aryne by carrying out flattening polish of the sedimentary layers of the barrier material.

[Claim 2]A manufacturing method of an integrated circuit device characterized by comprising the following.
A process of forming an opening in an insulator layer formed on a circuit board.
A process of depositing sedimentary layers of a barrier material on the circuit board containing the opening.
A process of depositing copper sedimentary layers on sedimentary layers of the barrier material.
A process of removing copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer while removing sedimentary layers of a barrier material and copper sedimentary layers which were deposited on the insulator layer.
A process of depositing sedimentary layers of a barrier material on a substrate containing copper in the opening.
A process of forming a barrier layer in a top surface of copper in the opening by a self aryne by carrying out flattening polish of the sedimentary layers of the barrier material.

[Claim 3]While removing sedimentary layers of copper deposited on an insulator layer by carrying out buffing using an aqueous solution and an abradant of a potassium iodide or potassium chloride, A manufacturing method of an integrated circuit device described in Claim 1 or Claim 2 removing copper deposited into an opening so that it may have a level difference whose surface is lower than the surface of the insulator layer.
[Claim 4]A manufacturing method of an integrated circuit device described in any 1 item from Claim 1 to which an opening formed in an insulator layer is a grooved opening, and is characterized by forming a wiring layer with copper deposited into the grooved opening to Claim 3.
[Claim 5]A manufacturing method of an integrated circuit device described in any 1 item from Claim 1 which an opening formed in an insulator layer is a contact hole which reaches a substrate, and is characterized by forming contact to the circuit board with copper deposited all over the contact hole to Claim 3.
[Claim 6]A manufacturing method of an integrated circuit device described in any 1 item from Claim 1, wherein material of a barrier layer is TiN to Claim 5.
[Claim 7]A manufacturing method of an integrated circuit device described in any 1 item from Claim 1, wherein material of a barrier layer is an insulating material which does not contain oxygen to Claim 4.

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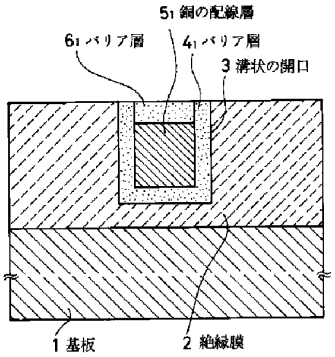
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]The present invention relates to the manufacturing method of the integrated circuit device which has the characteristics in the method of forming the wiring layer or contact which used copper. In recent years, high integration of the integrated circuit device using an Al wiring layer follows on proceeding, and increase of the contact resistance by the reduction of a contact area and increase of resistance by micronization of wiring size, and electromigration resistance degradation have been a problem. For this reason, electromigration resistance is high and the technology which forms fine wiring and minute contact using the material of low resistance is needed. Copper attracts attention as such a metallic material for wiring.
[0002]
[Description of the Prior Art]Conventionally, as a method of forming a wiring layer with copper, after depositing a copper thin film on an entire substrate with a sputtering method or a vapor deposition method, the method of using a chemical reaction and molding into desired wiring formation by RIE was tried.
[0003]
[Problem to be solved by the invention]However, in the usual method, there was a defect whose form after patterning of wiring an etch rate is slow since the steam pressure of copper halide occurred by an etching step is very low, and is not clear.
[0004]It had become an obstacle, when the coating membrane for preventing copper oxidation was formed after forming a copper wiring layer, unevenness of a wiring layer enlarged and the surface was flattened by forming coating membrane. An object of the present invention is to provide the method of realizing a copper wiring layer or flattening of contact including a barrier layer, without evaporating a copper compound by etching, in order to correspond to the above-mentioned problem.
[0005]
[Means for solving problem]In the manufacturing method of the integrated circuit device concerning the present invention, In order to achieve the above-mentioned object, while removing the sedimentary layers of the process of forming an opening in the insulator layer formed on the substrate, the process of depositing copper sedimentary layers on the substrate containing the opening, and copper deposited, on the insulator layer, The process of removing copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer, The process of depositing the sedimentary layers of a barrier material on the substrate containing copper in the opening, and the process of forming a barrier layer in the top surface of copper in the opening by a self aryne by carrying out flattening polish of the sedimentary layers of the barrier material were adopted.
[0006]The process of forming an opening in the insulator layer formed on the circuit board and the process of depositing the sedimentary layers of a barrier material on the circuit board containing the opening, While removing the sedimentary layers of the process of depositing copper sedimentary layers on the sedimentary layers of the barrier material, and the barrier material deposited, on the insulator layer, and copper sedimentary layers, The process of removing copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer, The process of depositing the sedimentary layers of a barrier material on the substrate containing copper in the opening, and the process of forming a barrier layer in the top surface of copper in the opening by a self aryne by carrying out flattening polish of the sedimentary layers of the barrier material were adopted.
[0007]In this case, while removing the sedimentary layers of the copper deposited on the insulator layer by carrying out buffing using the aqueous solution and abradant of a potassium iodide or potassium chloride, the process of removing copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer is employable.
[0008]The opening formed in the insulator layer in this case can be used as a grooved opening, and a wiring layer can be formed with copper deposited into the grooved opening, Or the opening formed in the insulator layer can be made into the contact hole which reaches a substrate, and the contact to the circuit board can be formed with copper deposited all over the contact hole.
[0009]And material of a barrier layer can be made into the insulating material which does not contain TiN or oxygen in this case again, a wiring layer can be formed, material of a barrier layer can be set to TiN and contact can be formed.
[0010]
[Function]Fig.1 is a composition explanatory view of the integrated circuit device manufactured by the present invention. As for a substrate, an insulator layer and the opening of a groove [2 / 3], and 4_1, in this figure, a copper wiring layer and 6_1 of a barrier layer and 5_1 are barrier layers 1.
[0011]In this composition explanatory view, the summary of the manufacturing method of the integrated circuit device which has the characteristics in the formation method of a wiring layer is described.
[0012]The grooved opening 3 is formed in the insulator layers 2, such as SiO_2 formed on the substrate 1, with photolithography technology, Barrier materials, such as TiN, are deposited

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Representative drawing

Representative drawing | 1 | 2 | 3 | 4 | 5

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by a sputtering method etc. all over the insulator layer 2 including the inside of this grooved opening 3, barrier material sedimentary layers are formed, copper is deposited with a CVD method etc. on these barrier material sedimentary layers, and the sedimentary layers of the copper which embeds the grooved opening 3 completely are formed.
[0013]Carry out buffing of the sedimentary layers of this copper using a potassium iodide (KI)+ iodine (I_2) aqueous solution (5%) and abrasive soap, and it removes the copper sedimentary layers and barrier material sedimentary layers which are formed in insulator layer 2 top surface, By barrier layer 4 $_1$, the three way type of a bottom surface and a side surface is surrounded, and wiring layer 5 $_1$ of copper lower than the top surface of the insulator layer 2 is formed.
[0014]And form barrier material sedimentary layers again all over the insulator layer 2 including the wiring layer 5 $_1$ top of copper lower than the top surface of the insulator layer 2, perform a flattening polish, and it leaves barrier layer 6 $_1$ only to the top surface of copper wiring layer 5 $_1$, The four quarters are surrounded by barrier layer 4 $_1$ and barrier layer 6 $_1$, and copper wiring layer 5 $_1$ which has a top surface of the insulator layer 2 and a top surface which corresponds is formed.
[0015]Since according to the present invention a copper wiring layer can be formed and the surroundings of a copper wiring layer can be further covered by a barrier layer, without using the process of etching a copper layer and leaving a wiring layer like before, Copper oxidation and diffusion are prevented and the flattening wiring layer of low resistance strong against electromigration can be formed.
[0016]
[Working example]Hereinafter, the Example of the manufacturing method of the integrated circuit device of the present invention is described.
(The 1st Example) Fig.2 and Fig.3 are the work flow illustrative drawings of the manufacturing method of the integrated circuit device of the 1st Example, and (A) - (E) shows each process. in this figure -- 1 -- barrier material sedimentary layers and 4 $_1$ are [barrier material sedimentary layers and 6 $_1$ of copper sedimentary layers and 5 $_1$] barrier layers a copper wiring layer and 6 a barrier layer and 5 a substrate, an insulator layer and the opening of a groove [2 / 3], and 4.
[0017]By this work flow illustrative drawing, the manufacturing method of the integrated circuit device which has the characteristics in the formation method of a wiring layer is described.
[0018]1st process (refer to Fig.2 (A))
The grooved opening 3 for forming a copper wiring layer in the insulator layers 2, such as SiO_2 formed on the substrate 1, is formed with photolithography technology. This substrate 1 may be an insulating substrate for supporting the semiconductor substrate of an integrated circuit device, and a wiring layer, a layer insulation body film of a multilayer interconnection layer, etc.
[0019]2nd process (refer to Fig.2 (B))
All over the insulator layer 2 including the inside of the grooved opening 3, TiN is deposited by a sputtering method and the barrier material sedimentary layers 4 are formed. On these barrier material sedimentary layers 4, copper is deposited with a CVD method, and the sedimentary layers 5 of the copper which embeds the grooved opening 3 completely are formed. As source gas of the sedimentary layers (CVD-Cu) 5 of copper by this CVD method, Membranes are formed by the substrate temperature of 200 degrees C, and growing pressure 1Torr using Cu(HFA) tmvs (Cu(1)-hexafluoroacetylacetonato-trimethylvinylsilyl).
[0020]3rd process (refer to Fig.2 (C))
Buffing of the sedimentary layers 5 of this copper is carried out using a potassium iodide (KI)+ iodine (I_2) aqueous solution (5%) and abrasive soap (trade name Balkalox 0.1CR), The copper sedimentary layers 5 and the barrier material sedimentary layers 4 which consists of TiN which are formed in insulator layer 2 top surface are removed, by barrier layer 4 $_1$, the three way type of a bottom surface and a side surface is surrounded, and wiring layer 5 $_1$ of copper lower than the top surface of the insulator layer 2 is formed.
[0021]4th process (refer to Fig.3 (D))
TiN is again deposited by a sputtering method all over the insulator layer 2 including the wiring layer 5 $_1$ top of copper lower than the top surface of the insulator layer 2, and the barrier material sedimentary layers 6 are formed.
[0022]5th process (refer to Fig.3 (E))
Carry out the flattening polish of these barrier material sedimentary layers 6, and it leaves barrier layer 6 $_1$ only to the top surface of copper wiring layer 5 $_1$, Barrier layer 4 $_1$ and barrier layer 6 $_1$ surround the four quarters completely, and it forms copper wiring layer 5 $_1$ which has a top surface of the insulator layer 2, and a plane which corresponds. On wiring layer 5 $_1$ of this flat insulator layer 2 and copper, other wiring layers can be formed succeedingly.
[0023]In the above-mentioned Example, although the example using TiN as a barrier material was described, When the insulating material which replaces with TiN and does not contain oxygen, such as an SiN film, in the surroundings of copper wiring layer 5 $_1$ is formed, The portion in which copper wiring layer 5 $_1$ carries out direct contact to an oxide film can be lost, and copper wiring layer 5 $_1$ can be prevented from oxidizing, and it can prevent copper of copper wiring layer 5 $_1$ diffusing to the insulator layer 2 conversely, and degrading the characteristic.
[0024](The 2nd Example) Fig.4 and Fig.5 are the work flow illustrative drawings of the manufacturing method of the integrated circuit device of the 2nd Example, and (A) - (E) shows each process. in this figure -- 11 -- a circuit board and 12 -- an insulator layer and 13 -- barrier material sedimentary layers and 14 $_1$ are [barrier material sedimentary layers and 16 $_1$ of copper sedimentary layers and 15 $_1$] barrier layers copper contact and 16 a barrier layer and 15 a contact hole and 14.
[0025]By this work flow illustrative drawing, the manufacturing method of the integrated circuit device which has the characteristics in the formation method of contact is described. Since the formation process of contact of this Example is the same as the formation process of the wiring layer of the 1st Example substantially, it omits a detailed description.
[0026]1st process (refer to Fig.4 (A))
The contact hole 13 for forming copper contact in the insulator layer 12 formed on the circuit board 11 is formed with photolithography technology.
[0027]2nd process (refer to Fig.4 (B))
All over the insulator layer 12 including the inside of the contact hole 13, the barrier material sedimentary layers 14 are formed by a sputtering method. On these barrier material sedimentary layers 14, copper is deposited with a CVD method, and the sedimentary layers 15 of the copper which embeds the contact hole 13 completely are formed.
[0028]3rd process (refer to Fig.4 (C))
Carry out buffing of the sedimentary layers 15 of this copper using a potassium iodide (KI)+ iodine (I_2) aqueous solution (5%) and abrasive soap, and it removes the copper sedimentary layers 15 and the barrier material sedimentary layers 14 which are formed in the top surface of the insulator layer 12, Barrier layer 14 $_1$ surrounds the circumference and it forms contact 15 $_1$ of copper lower than the top surface of the insulator layer 12.
[0029]4th process (refer to Fig.5 (D))
The barrier material sedimentary layers 16 are again formed all over the insulator layer 12 including the contact 15 $_1$ top of copper lower than the top surface of the insulator layer 12.
[0030]5th process (refer to Fig.5 (E))
Carry out the flattening polish of these barrier material sedimentary layers 16, and it leaves barrier layer 16 $_1$ only to the top surface of copper contact 15 $_1$, The whole surface is surrounded by barrier layer 14 $_1$ and barrier layer 16 $_1$, and copper contact 15 $_1$ which has a top surface of the insulator layer 12 and a plane which corresponds is formed.
[0031]In this Example, the barrier metal or alloy which has conductivity, such as TiN, is used as a barrier material, On contact 15 $_1$ of the flat insulator layer 12 and copper, other wiring layers can be formed succeedingly, and between other wiring layers can electrically

be connected with copper contact 15 $_1$ via conductive barrier layer 16 $_1$.
[0032]In each of above-mentioned Examples, although the surroundings of copper wiring layer 5 $_1$ or contact are covered by the barrier layer, When the material of an insulator layer has a property equivalent to a barrier material, the object of this invention can be attained by forming a barrier layer in the upper chisel of copper wiring layer 5 $_1$ or contact.
[0033]
[Effect of the Invention]Since a copper wiring layer can be formed and all the surroundings of a copper wiring layer are further covered in the layer of a barrier material, without using the conventional process of etching a copper layer and leaving a wiring layer according to the present invention as described above. The place which copper oxidation and diffusion are prevented, can form the flattening wiring layer of low resistance strong against electromigration, and contributes to high integration of an integrated circuit device is large.

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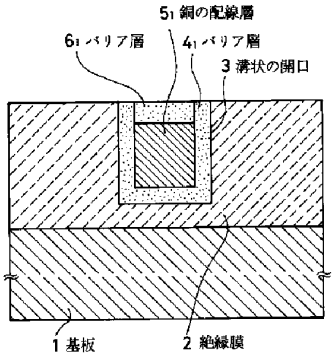
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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
A [FIG. 1] It is a composition explanatory view of the integrated circuit device manufactured by the present invention.
A [FIG. 2] By the work flow illustrative drawing (1) of the manufacturing method of the integrated circuit device of the 1st Example, (A) - (C) shows each process.
A [FIG. 3] By the work flow illustrative drawing (2) of the manufacturing method of the integrated circuit device of the 1st Example, (D) and (E) show each process.
A [FIG. 4] By the work flow illustrative drawing (1) of the manufacturing method of the integrated circuit device of the 2nd Example, (A) - (C) shows each process.
A [FIG. 5] By the work flow illustrative drawing (2) of the manufacturing method of the integrated circuit device of the 2nd Example, (D) and (E) show each process.
[Explanations of letters or numerals]
1 Substrate
2 Insulator layer
3 A grooved opening
4 Barrier material sedimentary layers
4 $_1$ barrier layer
5 Copper sedimentary layers
The wiring layer of 5 $_1$ copper
6 Barrier material sedimentary layers
6 $_1$ barrier layer
11 Circuit board
12 Insulator layer
13 Contact hole
14 Barrier material sedimentary layers
14 $_1$ barrier layer
15 Copper sedimentary layers
Contact of 15 $_1$ copper
16 Barrier material sedimentary layers
16 $_1$ barrier layer

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JP,06-275612,A

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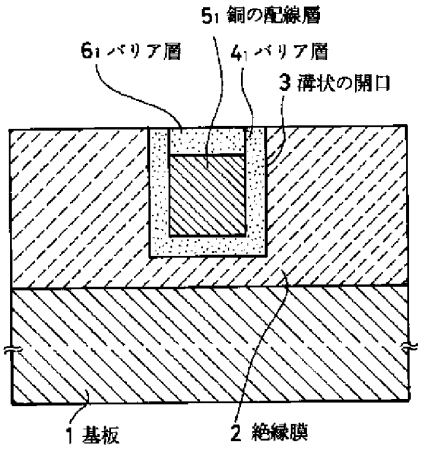
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DRAWINGS

A [FIG. 1]

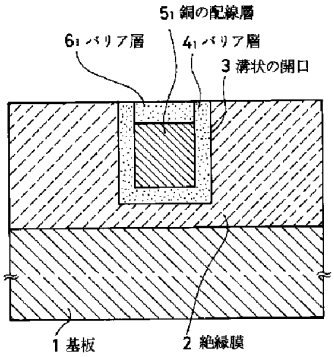
本発明によって製造された集積回路装置の構成説明図



A [FIG. 2]

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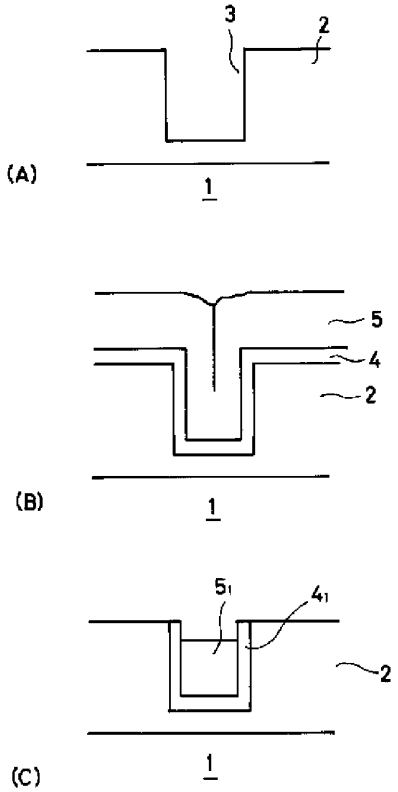


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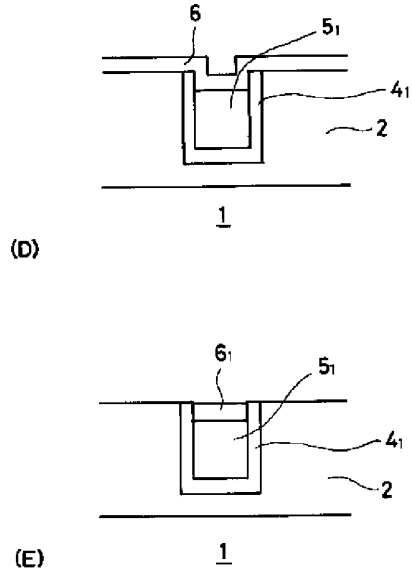
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第１実施例の集積回路装置の製造方法の工程説明図（１）



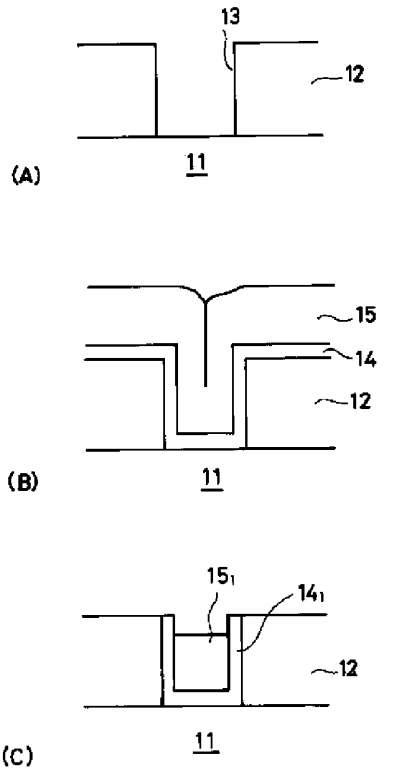
A [FIG. 3]

第１実施例の集積回路装置の製造方法の工程説明図（２）



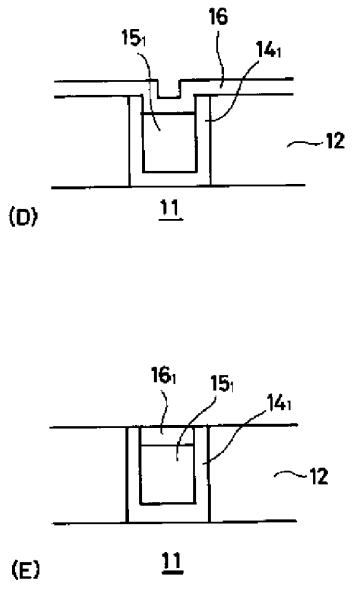
A [FIG. 4]

第２実施例の集積回路装置の製造方法の工程説明図（１）



A [FIG. 5]

第２実施例の集積回路装置の製造方法の工程説明図（２）



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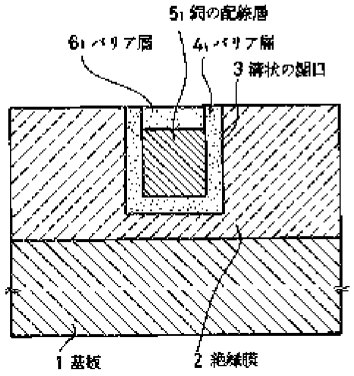
(54)【発明の名称】　集積回路装置の製造方法

(57)【要約】

【目的】　集積回路装置の製造方法に関し、エッチングによって銅の化合物を気化することなく、バリア層を含めた銅の配線層あるいはコンタクトの平坦化を実現する方法を提供する。

【構成】　基板１の上に形成された絶縁膜２に溝状の開口３を形成し、この開口３を含む基板１の上に薄いバリア材料の堆積層を堆積し、その上に銅の堆積層を堆積した後、絶縁膜２の上に形成された銅の堆積層とバリア材料の堆積層を除去するとともに、溝状の開口３の中に堆積された銅を表面が絶縁膜２の表面より低い段差を有するように除去して銅の配線層５，とバリア層４，を形成し、この溝状の開口３の中の銅の配線層５，を含む基板１の上にバリア材料の堆積層を堆積し、このバリア材料の堆積層を平坦化研磨して開口中の銅の配線層５，の上にセルフアラインでバリア層６，を形成する。同様の工程によって配線基板上にコンタクトを形成することができる。

本発明によって製造された集積回路装置の構成説明図



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【特許請求の範囲】

【請求項１】　基板上に形成された絶縁膜に開口を形成する工程と、該開口を含む該基板の上に銅の堆積層を堆積する工程と、該絶縁膜の上に堆積された銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去する工程と、該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程とを含むことを特徴とする集積回路装置の製造方法。

【請求項２】　回路基板上に形成された絶縁膜に開口を形成する工程と、該開口を含む該回路基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層の上に銅の堆積層を堆積する工程と、該絶縁膜の上に堆積されたバリア材料の堆積層と銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去する工程と、該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程とを含むことを特徴とする集積回路装置の製造方法。

【請求項３】　沃化カリウムまたは塩化カリウムの水溶液と研磨材を用いてバフ研磨することによって、絶縁膜の上に堆積された銅の堆積層を除去するとともに、開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去することを特徴とする請求項１または請求項２に記載された集積回路装置の製造方法。

【請求項４】　絶縁膜に形成された開口が、溝状開口であり、該溝状開口中に堆積した銅によって配線層を形成することを特徴とする請求項１から請求項３までのいずれか１項に記載された集積回路装置の製造方法。

【請求項５】　絶縁膜に形成された開口が、基板に達するコンタクトホールであり、該コンタクトホール中に堆積した銅によって該回路基板に対するコンタクトを形成することを特徴とする請求項１から請求項３までのいずれか１項に記載された集積回路装置の製造方法。

【請求項６】　バリア層の材料がＴｉＮであることを特徴とする請求項１から請求項５までのいずれか１項に記載された集積回路装置の製造方法。

【請求項７】　バリア層の材料が酸素を含まない絶縁材料であることを特徴とする請求項１から請求項４までのいずれか１項に記載された集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、銅を用いた配線層またはコンタクトを形成する方法に特徴を有する集積回路装置の製造方法に関する。近年、Ａｌ配線層を用いた集積回路装置の高集積化が進むに伴い、コンタクト面積の縮

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小化によるコンタクト抵抗の増大、および、配線サイズの微細化による抵抗の増大やエレクトロマイグレーション耐性の劣化が問題になっている。このため、エレクトロマイグレーション耐性が高く、かつ、低抵抗の材料を用いて微細配線や微細なコンタクトを形成する技術が必要になっている。このような配線用金属材料として銅が注目されている。

【０００２】

【従来の技術】従来、銅で配線層を形成する方法としては、スパッタ法あるいは蒸着法により基板全面に銅の薄膜を堆積した後に、化学反応を利用しＲＩＥによって所望の配線形成に成形する方法が試みられていた。

【０００３】

【発明が解決しようとする課題】ところが、通常の方法では、エッチング工程で生じるハロゲン化銅の蒸気圧が極めて低いためエッチング速度が遅く、配線のパターニング後の形状が鮮明でない等の欠点があった。

【０００４】また、銅の配線層を形成した後に銅の酸化を防止するための被覆膜を形成すると、被覆膜を形成することによって配線層の凹凸が大きくなり、表面を平坦化する上で障害となっていた。本発明は、上記の問題に対応するため、エッチングにより銅の化合物を気化することなく、バリア層を含めた銅の配線層あるいはコンタクトの平坦化を実現する方法を提供することを目的とする。

【０００５】

【課題を解決するための手段】本発明にかかる集積回路装置の製造方法においては、上記の目的を達成するために、基板上に形成された絶縁膜に開口を形成する工程と、該開口を含む該基板の上に銅の堆積層を堆積する工程と、該絶縁膜の上に堆積された銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去する工程と、該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程を採用した。

【０００６】また、回路基板上に形成された絶縁膜に開口を形成する工程と、該開口を含む該回路基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層の上に銅の堆積層を堆積する工程と、該絶縁膜の上に堆積されたバリア材料の堆積層と銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去する工程と、該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程を採用した。

【０００７】この場合、沃化カリウムまたは塩化カリウムの水溶液と研磨材を用いてバフ研磨することによっ

て．絶縁膜の上に堆積された銅の堆積層を除去するとともに．開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去する工程を採用することができる。

【０００８】またこの場合．絶縁膜に形成された開口を溝状開口にして．該溝状開口中に堆積した銅によって配線層を形成することができ．あるいは．絶縁膜に形成された開口を基板に達するコンタクトホールにして．該コンタクトホール中に堆積した銅によって該回路基板に対するコンタクトを形成することができる。

【０００９】そしてまた．この場合．バリア層の材料をＴｉＮまたは酸素を含まない絶縁材料にして配線層を形成することができ、バリア層の材料をＴｉＮにしてコンタクトを形成することができる。

【００１０】

【作用】図１は．本発明によって製造された集積回路装置の構成説明図である。この図において、１は基板、２は絶縁膜、３は溝状の開口．４，はバリア層、５，は銅の配線層、６，はバリア層である。

【００１１】この構成説明図によって．配線層の形成方法に特徴を有する集積回路装置の製造方法の概要を説明する。

【００１２】基板１の上に形成されたＳｉＯ２等の絶縁膜２に溝状の開口３をフォトリソグラフィー技術によって形成し、この溝状の開口３の中を含む絶縁膜２の全面にＴｉＮ等のバリア材料をスパッタ法等によって堆積してバリア材料堆積層を形成し、このバリア材料堆積層の上に．銅をＣＶＤ法等によって堆積して、溝状の開口３を完全に埋め込む銅の堆積層を形成する。

【００１３】この銅の堆積層を、沃化カリウム（ＫＩ）＋沃素（Ｉ２）水溶液（５％）と研磨剤を用いてバフ研磨し．絶縁膜２上面に形成されている銅の堆積層とバリア材料堆積層を除去して．バリア層４，によって底面と側面の三方を囲まれ、絶縁膜２の上面より低い銅の配線層５，を形成する。

【００１４】そして、絶縁膜２の上面より低い銅の配線層５，の上を含む絶縁膜２の全面に再びバリア材料堆積層を形成し、平坦化ポリッシュを行って、銅の配線層５，の上面のみにバリア層６，を残して．バリア層４，とバリア層６，によって四方を囲まれ．絶縁膜２の上面と一致する上面を有する銅の配線層５，を形成する。

【００１５】本発明によると、従来のように、銅層をエッチングして配線層を残す工程を用いることなく銅の配線層を形成することができ．さらに銅の配線層の周りをバリア層によって覆うことができるため、銅の酸化、拡散が防止され．エレクトロマイグレーションに強い低抵抗の平坦化配線層を形成することができる。

【００１６】

【実施例】以下．本発明の集積回路装置の製造方法の実施例を説明する。

（第１実施例）図２、図３は、第１実施例の集積回路装置の製造方法の工程説明図で、（Ａ）～（Ｅ）は各工程を示している。この図において、１は基板、２は絶縁膜．３は溝状の開口、４はバリア材料堆積層、４，はバリア層、５は銅の堆積層．５，は銅の配線層、６はバリア材料堆積層．６，はバリア層である。

【００１７】この工程説明図によって．配線層の形成方法に特徴を有する集積回路装置の製造方法を説明する。

【００１８】第１工程（図２（Ａ）参照）

基板１の上に形成されたＳｉＯ２等の絶縁膜２に．銅の配線層を形成するための溝状の開口３をフォトリソグラフィー技術によって形成する。この基板１は、集積回路装置の半導体基板、配線層を担持するための絶縁基板、多層配線層の層間絶縁体膜等であり得る。

【００１９】第２工程（図２（Ｂ）参照）

溝状の開口３の中を含む絶縁膜２の全面に、ＴｉＮをスパッタ法によって堆積してバリア材料堆積層４を形成する。このバリア材料堆積層４の上に．銅をＣＶＤ法によって堆積して．溝状の開口３を完全に埋め込む銅の堆積層５を形成する。このＣＶＤ法による銅の堆積層（ＣＶＤ－Ｃｕ）５のソースガスとして、Ｃｕ（ＨＦＡ）ｔｍｖｓ（Ｃｕ（ｌ）－ｈｅｘａｆｌｕｏｒｏａｃｅｔｙｌａｃｅｔｏｎａｔｏ－ｔｒｉｍｅｔｈｙｌｖｉｎｙｌｓｉｌｙｌ）を用い、基板温度２００℃．成長圧力１Ｔｏｒｒで成膜する。

【００２０】第３工程（図２（Ｃ）参照）

この銅の堆積層５を、沃化カリウム（ＫＩ）＋沃素（Ｉ２）水溶液（５％）および研磨剤（商品名Ｂａｌｋａｌｏｘ　０．１ＣＲ）を用いてバフ研磨し、絶縁膜２上面に形成されている銅の堆積層５とＴｉＮからなるバリア材料堆積層４を除去して．バリア層４，によって底面と側面の三方を囲まれ、絶縁膜２の上面より低い銅の配線層５，を形成する。

【００２１】第４工程（図３（Ｄ）参照）

絶縁膜２の上面より低い銅の配線層５，の上を含む絶縁膜２の全面に再びＴｉＮをスパッタ法により堆積して、バリア材料堆積層６を形成する。

【００２２】第５工程（図３（Ｅ）参照）

このバリア材料堆積層６を平坦化ポリッシュして．銅の配線層５，の上面のみにバリア層６，を残して．バリア層４，とバリア層６，によって四方を完全に囲まれ、絶縁膜２の上面と一致する平面を有する銅の配線層５，を形成する。この平坦な絶縁膜２と銅の配線層５，の上に．他の配線層を引き続いて形成することができる。

【００２３】上記の実施例においては．バリア材料としてＴｉＮを用いた例を説明したが、ＴｉＮに代えて銅の配線層５，の周りにＳｉＮ膜等の酸素を含まない絶縁材料を形成した場合は、銅の配線層５，が酸化膜と直接接触する部分がなくなり、銅の配線層５，が酸化されるのを防止することができ、また逆に銅の配線層５，の銅が

絶縁膜２に拡散して特性を劣化させることを防止することができる。

【００２４】（第２実施例）図４，図５は，第２実施例の集積回路装置の製造方法の工程説明図で，（Ａ）～（Ｅ）は各工程を示している。この図において，１１は回路基板，１２は絶縁膜，１３はコンタクトホール，１４はバリア材料堆積層，１４，はバリア層，１５は銅の堆積層，１５$_1$は銅のコンタクト，１６はバリア材料堆積層，１６，はバリア層である。

【００２５】この工程説明図によって，コンタクトの形成方法に特徴を有する集積回路装置の製造方法を説明する。この実施例のコンタクトの形成工程は第１実施例の配線層の形成工程とほぼ同様であるから，詳細な説明を省略する。

【００２６】第１工程（図４（Ａ）参照）

回路基板１１の上に形成された絶縁膜１２に，銅のコンタクトを形成するためのコンタクトホール１３をフォトリソグラフィー技術によって形成する。

【００２７】第２工程（図４（Ｂ）参照）

コンタクトホール１３の中を含む絶縁膜１２の全面に，スパッタ法によってバリア材料堆積層１４を形成する。このバリア材料堆積層１４の上に，銅をＣＶＤ法によって堆積して，コンタクトホール１３を完全に埋め込む銅の堆積層１５を形成する。

【００２８】第３工程（図４（Ｃ）参照）

この銅の堆積層１５を，沃化カリウム（ＫＩ）＋沃素（I_2）水溶液（５％）と研磨剤を用いてバフ研磨し，絶縁膜１２の上面に形成されている銅の堆積層１５とバリア材料堆積層１４を除去して，周囲をバリア層１４，によって囲まれ，絶縁膜１２の上面より低い銅のコンタクト１５，を形成する。

【００２９】第４工程（図５（Ｄ）参照）

絶縁膜１２の上面より低い銅のコンタクト１５$_1$の上を含む絶縁膜１２の全面に再びバリア材料堆積層１６を形成する。

【００３０】第５工程（図５（Ｅ）参照）

このバリア材料堆積層１６を平坦化ポリッシュして，銅のコンタクト１５，の上面のみにバリア層１６$_1$を残して，バリア層１４，とバリア層１６$_1$によって全面を囲まれ，絶縁膜１２の上面と一致する平面を有する銅のコンタクト１５$_1$を形成する。

【００３１】この実施例においては，バリア材料としてＴｉＮ等の導電性を有するバリアメタルあるいは合金を用い，平坦な絶縁膜１２と銅のコンタクト１５$_1$の上に，他の配線層を引き続いて形成し，導電性のバリア層１６$_1$を介して銅のコンタクト１５$_1$と他の配線層の間を電気的に接続することができる。

【００３２】上記の各実施例においては，銅の配線層５，あるいはコンタクトの周りをバリア層で覆っているが，絶縁膜の材料がバリア材料と同等の性質を有する場合は，銅の配線層５，あるいはコンタクトの上部のみにバリア層を形成することによって，本発明の目的を達成することができる。

【００３３】

【発明の効果】以上説明したように，本発明によると，銅層をエッチングして配線層を残す従来の工程を用いることなく，銅の配線層を形成することができ，さらに銅の配線層の周りは全てバリア材料の層で覆われるため，銅の酸化，拡散が防止され，エレクトロマイグレーションに強い低抵抗の平坦化配線層を形成することができ，集積回路装置の高集積化に寄与するところが大きい。

【図面の簡単な説明】

【図１】本発明によって製造された集積回路装置の構成説明図である。

【図２】第１実施例の集積回路装置の製造方法の工程説明図（１）で，（Ａ）～（Ｃ）は各工程を示している。

【図３】第１実施例の集積回路装置の製造方法の工程説明図（２）で，（Ｄ），（Ｅ）は各工程を示している。

【図４】第２実施例の集積回路装置の製造方法の工程説明図（１）で，（Ａ）～（Ｃ）は各工程を示している。

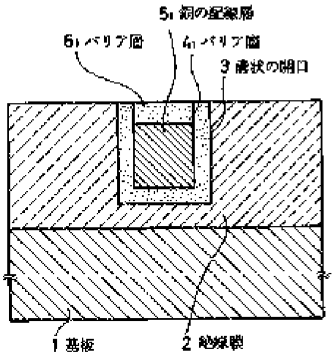
【図５】第２実施例の集積回路装置の製造方法の工程説明図（２）で，（Ｄ），（Ｅ）は各工程を示している。

【符号の説明】

１　基板
２　絶縁膜
３　溝状の開口
４　バリア材料堆積層
４$_1$　バリア層
５　銅の堆積層
５$_1$　銅の配線層
６　バリア材料堆積層
６$_1$　バリア層
１１　回路基板
１２　絶縁膜
１３　コンタクトホール
１４　バリア材料堆積層
１４$_1$　バリア層
１５　銅の堆積層
１５$_1$　銅のコンタクト
１６　バリア材料堆積層
１６$_1$　バリア層

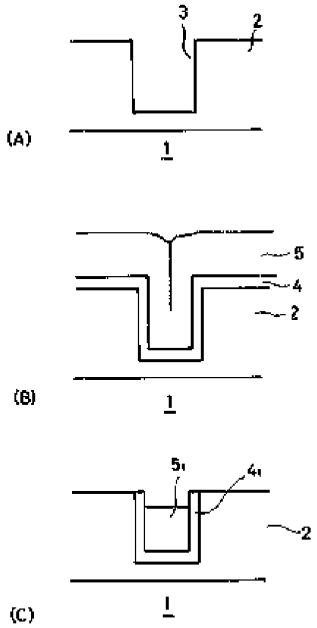
【図１】

本発明によって製造された集積回路装置の構成説明図



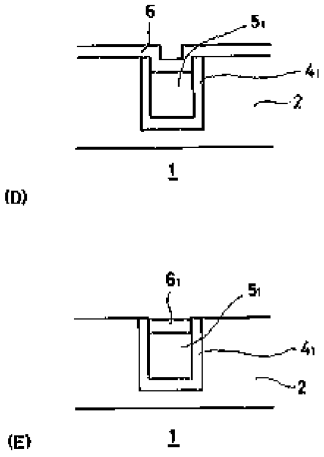
【図２】

第１実施例の集積回路装置の製造方法の工程説明図（１）



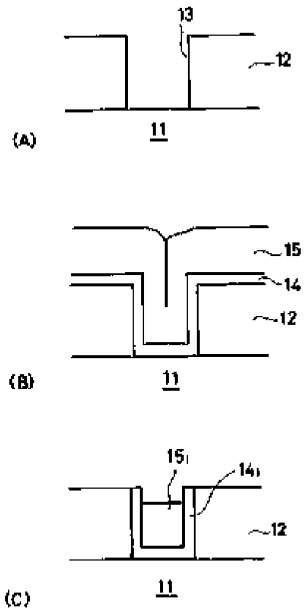
【図３】

第１実施例の集積回路装置の製造方法の工程説明図（２）



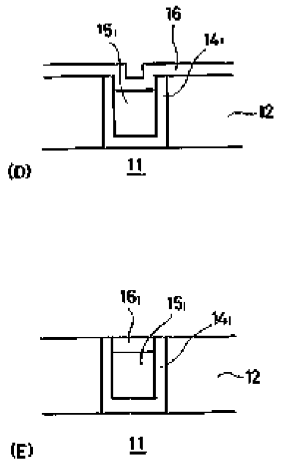
【図４】

第２実施例の集積回路装置の製造方法の工程説明図（１）



【図５】

第２実施例の集積回路装置の製造方法の工程説明図（２



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Reduced electromigration and stress induced migration of Cu wires by surface coating

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Applicant(s): IBM [US] ± (IBM CORP)

Classification: **- international:** ***C23C18/16; H01L21/28; H01L21/288; H01L21/3205; H01L21/44; H01L21/4763; H01L21/768; H01L23/52; H01L23/532;*** (IPC1-7): H01L21/288; H01L21/768; H01L23/532

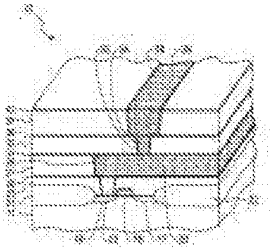
- cooperative: **H01L21/288**; **H01L21/76843**; **H01L21/76849**; **H01L21/76864**; **H01L23/53228**; **H01L23/53238**; **H01L23/5329**; H01L2924/0002 more

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Abstract not available for CN1364311 (A)
Abstract of corresponding document: WO0108213 (A1)



The idea of the invention is to coat the free surface of patterned Cu conducting lines (60, 70) in on-chip interconnections (BEOL) wiring by a 1-20 nm thick metal layer (63, 74) prior to deposition of the interlevel dielectric. This coating is sufficiently thin so as to obviate the need for additional planarization by polishing, while providing protection against oxidation and surface, or interface, diffusion of Cu which has been identified by the inventors as the leading contributor to metal line failure by electromigration and thermal stress voiding. Also, the metal layer (63, 74) increases the adhesion strength between the Cu (60, 70) and dielectric (66) so as to further increase lifetime and facilitate process yield. The free surface is a direct result of the CMP (chemical mechanical polishing) in a damascene process or in a dry etching process by which Cu wiring is patterned. It is proposed that the metal capping layer (63, 74) be deposited by a selective process

onto the Cu to minimize further processing. We have used electroless metal coatings, such as CoWP, CoSnP and Pd, to illustrate significant reliability benefits, although chemical vapor deposition (CVD) of metals or metal forming compounds can be employed.

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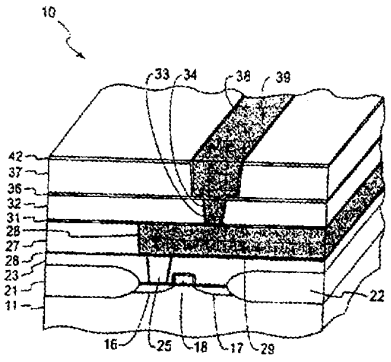
[74]专利代理机构 中国国际贸易促进委员会专利商标事务所
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权利要求书5页 说明书7页 附图页数5页

[54]发明名称 用表面涂敷方法降低铜布线的电迁移和应力引起的迁移

[57]摘要

本发明的想法是在淀积层间介质之前，用1－20nm厚的金属层(63，74)涂敷芯片上互连(BEOL)布线中的被图形化的铜导线(60,70)的自由表面。这一涂层要足够薄，以便免除对抛光额外整平的需要，同时提供抗氧化、抗铜的表面或界面扩散的保护，本发明人已经证实铜的表面和界面扩散是电迁移和热应力空洞造成金属线条失效的首要原因。金属层(63,74)还提高了铜(60,70)与介质(66)之间的粘附强度，从而进一步提高了寿命和工艺成品率。自由表面是镶嵌工艺或干法腐蚀工艺中用以对铜布线进行图形化的CMP(化学机械抛光)的直接结果。提出了用选择性工艺将金属覆盖层(63,74)淀积到铜上以便尽量减少进一步处理。虽然能够使用金属或金属形成的化合物来进行化学汽相淀积(CVD)，但我们已经使用诸如CoWP、CoSnP和Pd之类的无电金属涂敷方法来演示明显的可靠性好处。



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权 利 要 求 书

1.具有高抗电迁移性的导体的制作方法，它包含下列步骤：在衬底上制作介质层，在所述介质层中制作至少一个沟槽，在所述沟槽中形成金属衬里，在所述金属衬里上形成导体来填充所述沟槽，形成与所述介质层上表面共平面的所述导体的被整平的上表面，以及在所述导体的所述上表面上形成导电膜，所述导电膜形成金属对金属的金属键。

2. 权利要求 1 的方法，其特征在于，所述形成导电膜的步骤包括用无电淀积方法制作所述导电膜的步骤，从而所述导体的所述上表面被防止了氧化和腐蚀，并提供了高的抗电迁移性和高的抗热应力空洞性。

3. 权利要求 2 的方法，其特征在于，所述无电淀积膜的厚度为 1-20nm。

4. 权利要求 2 的方法，其特征在于，所述无电淀积膜的厚度为 1-10nm。

5. 权利要求 2 的方法，其特征在于，所述无电淀积步骤包括下列步骤：

首先将所述衬底浸入金属离子溶液，从而在所述导体的所述上表面上形成一个金属纳米粒子层，

然后将所述衬底再次浸入金属离子和次磷酸盐离子的无电络合物溶液，从而在所述导体的所述上表面上形成一个金属磷化物导电膜，以及

在惰性或还原气氛中，于至少 300℃的温度下，对所述衬底退火至少 2 小时，从而在所述导体与所述金属磷化物导电膜之间得到优异的粘附性。

6. 权利要求 5 的方法，其特征在于，略去所述再次浸入步骤。

7. 权利要求 5 的方法，其特征在于，所述导电膜选自 CoWP、CoSnP、CoP、Pd、In 和 W 构成的组，且厚度为 1-20nm。

8. 权利要求 2 的方法，其特征在于，所述无电淀积步骤包括下列

步骤:

首先将所述衬底浸入金属离子溶液，从而在所述导体的表面上形成一个金属纳米粒子层，

然后将所述衬底再次浸入金属离子和二甲氨基硼烷的无电络合物溶液，从而在所述导体的所述上表面上形成一个金属-硼的导电膜层，以及

在惰性或还原气氛中，于至少 300℃的温度下，对所述衬底退火至少 2 小时，从而在所述导体与所述金属硼导电膜之间得到优异的粘附性。

9. 权利要求 1 的方法，其特征在于，用诸如化学汽相淀积（CVD）、物理汽相淀积（PVD）、蒸发、溅射、以及金属热互扩散之类的物理方法，将所述导电膜涂敷在所述导体的表面上。

10. 权利要求 9 的方法，其特征在于，所述导电膜选自 Pd、In、W、及其混合物构成的组。

11. 一种结构，它包含:

衬底上的介质层，

制作在所述衬底上的所述介质中的至少一个沟槽，

制作在所述沟槽中的金属衬里，

填充所述沟槽的所述衬里上的导体，

具有所述介质层的上表面的所述导体的被整平了的上表面，以及

所述导体所述上表面上的导电膜，所述导电膜形成金属对金属的化学键和金属键。

12. 权利要求 11 的结构，其特征在于，所述导电膜选自 CoWP、CoSnP、CoP、Pd、CoB、CoSnB、CoWB、In、NiB 和 W 构成的组，从而防止所述导体的所述上表面被氧化和腐蚀。

13. 权利要求 12 的结构，其特征在于，所述导电膜的厚度为 1-20nm。

14. 权利要求 12 的结构，还包括所述导体和所述介质层上所述导电膜上的绝缘介质覆盖层。

15. 权利要求 14 的结构，其特征在于，所述绝缘介质覆盖层选自氮化硅、氧化硅、介电常数小于 3.2 的 SICOH 的绝缘化合物、类金刚石碳、氟化类金刚石碳、和聚亚芳基醚构成的组。

16. 权利要求 11 的结构，其特征在于，所述导体选自铜和铜合金构成的组。

17. 权利要求 11 的结构，其特征在于，所述衬底选自硅、硅锗、SOI 和砷化镓构成的组。

18.具有高抗电迁移性的导体的制作方法，它包含下列步骤:

在衬底上形成图形化的导体，

在所述导体的所述表面上形成导电膜，所述导电膜形成金属对金属的金属键。

19. 权利要求 18 的方法，其特征在于，所述形成导电膜的步骤包括用无电淀积方法制作所述导电膜的步骤，从而所述导体的所述表面被防止了氧化和腐蚀，并提供了高的抗电迁移性和高的抗热应力空洞性。

20. 权利要求 19 的方法，其特征在于，所述无电淀积膜的厚度为 1-20nm。

21. 权利要求 19 的方法，其特征在于，所述无电淀积膜的厚度为 1-10nm。

22. 权利要求 19 的方法，其特征在于，所述无电淀积步骤包括下列步骤:

首先将所述衬底浸入金属离子溶液，从而在所述导体的所述表面上形成一个金属纳米粒子层，

然后将所述衬底再次浸入金属离子和次磷酸盐离子的无电络合物溶液，从而在所述导体的所述表面上形成一个金属磷化物导电膜，以及

在惰性或还原气氛中，于至少 300℃的温度下，对所述衬底退火至少 2 小时，从而在所述导体与所述金属磷化物导电膜之间得到优异的粘附性。

23. 权利要求 22 的方法，其特征在于，略去所述再次浸入步骤。

24. 权利要求 22 的方法，其特征在于，所述导电膜选自 CoWP、CoSnP、CoP、Pd、In 和 W 构成的组，且厚度为 1-20nm。

25. 权利要求 19 的方法，其特征在于，所述无电淀积步骤包括下列步骤:

首先将所述衬底浸入金属离子溶液，从而在所述导体的表面上形成一个金属纳米粒子层，

然后将所述衬底再次浸入金属离子和二甲氨基硼烷的无电络合物溶液，从而在所述导体的所述表面上形成一个金属-硼的导电膜，以及

在惰性或还原气氛中，于至少 300℃的温度下，对所述衬底退火至少 2 小时，从而在所述导体与所述金属硼导电膜之间得到优异的粘附性。

26. 权利要求 18 的方法，其特征在于，用诸如化学汽相淀积（CVD）、物理汽相淀积（PVD）、蒸发、溅射、以及金属热互扩散之类的物理方法，将所述导电膜涂敷在所述导体的表面上。

27. 权利要求 26 的方法，其特征在于，所述导电膜选自 Pd、In、W、及其混合物构成的组。

28. 一种结构，它包含:

衬底上的图形化导体，

所述衬底表面上的导电膜，所述导电膜形成金属对金属的金属键。

29. 权利要求 28 的结构，其特征在于，所述导电膜选自 CoWP、CoSnP、CoP、Pd、CoB、CoSnB、CoWB、In、NiB 和 W 构成的组，从而防止所述导体的所述上表面被氧化和腐蚀。

30. 权利要求 29 的结构，其特征在于，所述导电膜的厚度为 1-20nm。

31. 权利要求 29 的结构，还包括所述导体的所述导电膜上的绝缘介质覆盖层。

32. 权利要求 31 的结构，其特征在于，所述绝缘介质覆盖层选自氮化硅、氧化硅、介电常数小于 3.2 的 SICOH 的绝缘化合物、类金刚

石碳、氟化类金刚石碳、和聚亚芳基醚构成的组。

33. 权利要求 29 的结构，其特征在于，所述导体选自铜和铜合金构成的组。

34. 权利要求 29 的结构，其特征在于，所述衬底选自硅、硅锗、SOI 和砷化镓构成的组。

35. 权利要求 8 的方法，其特征在于，所述导电膜选自 CoB、CoSnB、CoWB 和 NiB 构成的组。

36. 权利要求 25 的方法，其特征在于，所述导电膜选自 CoB、CoSnB、CoWB 和 NiB 构成的组。

02.01.24

说　　明　　书

用表面涂敷方法降低铜布线的电迁移和应力引起的迁移

技术领域

本发明涉及到半导体芯片上的金属互连，更确切地说是涉及到一种表面涂敷或处理，用来防止电子流使导体表面原子向下运动即所谓电迁移现象和/或防止倾向于释放应力的应力梯度使导体表面原子移动即所谓应力引起的迁移。

背景技术

微电子电路越来越高的密度和速度，已经使金属化系统从 Al(Cu) 转向到了 Cu，以便降低导体的电阻。同时，对更高的电流密度的要求已经暴露出 Al(Cu)线由于电迁移而失效，限制了电路设计者能够提高性能的范围。铜的更高的熔点被期望能够改进导体的电流承载能力，延长电迁移寿命。但我们从所得到的测试结果已经发现，电迁移寿命主要依赖于诸如铜/介质界面处的原子输运之类的原子行为，而不依赖于铜晶格、晶粒边界或铜/衬里界面原子输运的本征特性。于是证明铜导体承受电流的特性并不明显地优越于 Al(Cu)。

制造铜导体图形的基本工艺是采用镶嵌方法，其中，在介质层中制作沟槽，在沟槽中形成衬里，然后用铜填充沟槽，并对其进行化学机械抛光（CMP），终止于与介质层共平面的洁净铜顶面。铜/金属衬里界面被形成在铜导体的其他 3 个表面上。电迁移寿命是线条厚度、宽度和截面积的函数。测得的数据表明，仅仅顶部表面对具有竹状和接近竹状的晶粒结构的铜导体的质量输运有贡献，而边界与表面的组合对更宽的线条的质量输运有贡献。同一个关系被发现而与铜的淀积方法无关，亦即，不管是用物理汽相淀积（PVD）、化学汽相淀积（CVD）、或电镀来进行淀积，都出现此问题。除了电迁移寿命失效之外，还发现铜导体图形对热循环应力下的原子空洞很敏感，发现空洞总是开始于原子迁移率最高的铜/介质界面处。由于铜迁移速率即漂

移速度是迁移率（D/kT）与驱动力（F）的乘积，其中 D 是铜的扩散率，T 是绝对温度，k 是波耳兹曼常数。对于电迁移和应力引起的迁移力，驱动力 F 分别是 Z*eE 和(Ds/Dx)W，其中 Z*是有效电荷数目，e 是电子电荷，E 是电场，(Ds/Dx)是应力梯度，而 W 是原子体积。目前不可避免的是，能够实现最高性能和可靠性的铜导体技术的成就要求改变或修正覆盖层的铜/介质界面以降低铜输运和原子空洞。

铜导体表面的修正可以在 CMP 之后进行。此工艺则应该对铜有选择性，并在铜导体表面上提供一个薄层，以便基本上保持与包含沟槽的介质或绝缘体共平面。此工艺必须导致铜导体与层上随后制作的介质之间更好的粘附性和铜导体中铜原子更好的抗氧化性以及降低了的铜导体原子输运，以便提供最高的可靠性。

发明内容

根据本发明，借助于在诸如 CMP 整平或干法腐蚀工艺之后在铜表面上提供一个 1-20nm 的金属薄层，改变了铜导体的暴露铜表面，以便在后续的芯片处理和/或芯片利用过程中降低对电迁移、氧化、腐蚀、应力空洞和剥层的敏感性，从而改善可靠性和成品率。本发明提出了无电金属淀积方法作为在铜导体上形成金属薄层的方法，用来提高电迁移寿命和抗应力引起的迁移。

此选择性淀积工艺包含下列步骤。

a. 用 Pd 离子催化剂选择性地激活铜表面，如方程 1 所示。

$Cu + Pd^{++}$ ------ á$Cu^{++} + Pd$ （1）

这一步骤在铜线表面上留下多个 Pd 纳米粒子，用作下一步骤的催化剂。

b. 用无电还原方法选择性地淀积金属或合金，如方程 2 所示。

还原剂+Me^{n+} +Cu ------á Cu/Me +被氧化的还原剂 （2）

其中 Me^{n+}是金属离子，例如 Co^{2+}。

例如，使用次磷酸盐作为还原剂，钴离子作为覆盖金属，则有方程 3 所示的化学反应。

$2H_2PO_2^- + Co^{2+} + H_2O$…((..Cu..)) -----á$Co + 2HPO_3^{2-} + H_2 + 4H^+$ （3）

在本发明中，我们使用了上述的次磷酸盐系统，并将金属钯、钴、钴钨、磷化钴钨、钴锡、磷化钴锡、磷化钴和钴的其它合金淀积到铜导体的表面上。还可以理解的是，能够使用其它的还原剂，例如能够淀积诸如 Co-B 或 Ni-B 之类的其它类型合金的二甲氨基硼烷。

上述步骤 a 和 b 的结果是，铜导体的暴露表面被由金属化合物或合金组成的厚度最好为 1-10nm 的薄膜涂敷，该薄膜通过化学键和/或金属键牢固地粘附于铜表面上或铜表面中的铜原子。

在用来制作集成电路芯片上的铜互连的镶嵌工艺中，下列重要发现对于本发明来说是至关重要的。

1. 铜表面上的涂敷膜的厚度必须薄：由于镶嵌工艺的考虑，最大厚度为 20nm，最好是 1-10nm。以这种方式获得至少 3 个主要性质：a）铜线的电阻率不受影响或增加不大于 20%，b）各个铜导体之间搭桥可能造成的漏电被消除，以及 c）铜导体或铜线不需要进一步整平。为了提供后续形成在其上的介质层的平整的顶部表面而不必整平后续的介质层的顶部表面，要求对铜导体/介质表面进行整平或基本的整平。一个表面上的台阶特征通过下一层被转移到该表面，特别是用 CVD 方法制作的表面。

2. 涂敷膜的优选组分可以是 Co-Sn-P、Co-W-P、Co-P 或 Pd.

3. 具有涂敷膜的晶片在 300℃下被退火 2 小时，以便进一步改善与铜表面的化学键合或金属键合，并减慢铜导体/介质界面处铜原子沿铜表面的扩散以及铜原子沿晶粒边界的扩散。铜导体/介质界面位于铜导体与形成在铜导体上的介质层之间。镶嵌工艺中的铜导体位于具有用铜导体填充沟槽之前制作在沟槽中的金属衬里的介质层中的沟槽中。

4. 金属的选择性 CVD 或其它的淀积工艺也可以被用来在具有化学键合和/或金属键合的铜导体的表面上淀积金属膜，以便获得铜导体的更高的抗电迁移性。

附图说明

当结合附图考虑本发明的下列详细描述时，本发明的这些和其它

的特点、目的、和优点将变得明显，其中:

图 1 是本发明一个实施方案的剖面图。

图 2A-2D 是本发明第二实施方案的各个制造阶段的剖面图。

图 3A-3E 是第三实施方案的各个制造阶段的剖面图。

图 4 是三层电迁移测试结构的剖面图。

图 5 曲线示出了顶部表面上具有和不具有金属薄膜的介质层沟槽中的铜导体和衬里的欧姆电阻对时间的关系。

具体实施方式

现参照附图，图 1 是含有用单镶嵌工艺制作的铜线和通孔的集成电路芯片 10 上的铜后端线（BEOL）结构例子的剖面图。

在图 1 中，集成电路芯片 10 具有衬底 11，可以是例如 Si、SiGe、Ge、SOI 和 GaAs. 衬底 11 中可以制作典型 FET 晶体管 19 的源区 16 和漏区 17 以及栅 18. 在源区 16 和漏区 17 的二侧是衬底 11 上凹陷的氧化物区 21 和 22. 氧化物层 23 被制作在氧化物区 21 和 22 以及 FET 晶体管 19 上. 在层 23 中形成源接触窗口，并用金属 25 通常是钨填充. 层 23 和金属 25 被化学机械抛光（CMP）整平. 例如由氮化硅组成的覆盖层 26 被制作在层 23 的上表面上. 介质层 27 被制作在层 26 上，并在其中形成沟槽. 衬里 28 被形成在沟槽的底部和侧壁上，然后用铜填充以形成线条 29. 用 CMP 对层 27 和线条 29 进行整平. 在层 27 和线条 29 的上表面上制作覆盖层 31. 在覆盖层 31 上形成介质层 32. 在层 31 和 32 中形成通孔窗口，随之以在窗口中形成金属衬里 33 和诸如铜的金属以形成通孔 34. 用 CMP 方法整平层 32 和通孔 34. 在层 32 和通孔 34 上制作覆盖层 36. 在覆盖层 36 上制作介质层 37. 在层 37 和覆盖层 36 中形成沟槽或窗口. 在层 37 和覆盖层 36 的沟槽中形成衬里 38. 用金属铜填充沟槽以形成线条 39. 用 CMP 方法整平层 37 和线条 39. 在层 37 和线条 39 上制作覆盖层 42. 覆盖层 26、31 和 36 是由不同于层 23、27、32 和 37 的介质组成的，可以是二氧化硅、类金刚石碳（DLC）、氟化 DLC、聚亚芳基醚、SiCOH 等. 在 1998 年 6 月 29 日提出的 No.09/107567 中，描述了 SiCOH，此处被列为参考来

显示低 k（介电常数）介质的一个例子．注意，BEOL 是用单镶嵌铜工艺制造的，亦即，各个铜层被单独地加工，且线条 31 和 39 的顶部与介质 8 形成界面。

图 2A-2D 示出了用来制造单镶嵌铜线条的工艺顺序，说明了用无电镀方法选择性淀积形成金属覆盖层．在此工艺顺序中，如图 2A 所示，淀积介质层 55-57 和 58．如图 2B 所示，用光刻工艺将图形转移到介质层 56 和 57 中．然后淀积衬里金属 59，随之以淀积厚度大于图形深度的铜导体 60．如图 2C 所示，用 CMP 清除过量的铜导体 60 和衬里 59，以形成平整的表面。如图 2D 所示，薄的无电金属涂层 63 被选择性地淀积到铜导体 60 上。图 2A-2D 所示的工艺可以对下一个铜导体互连层重复。

图 3 是双重镶嵌工艺的工艺顺序，其中的铜线条和通孔被同时淀积。从图 3A 所示的平整的介质层 65-67 开始，通孔 71 的图形通过图 3B 所示的介质层 67 被转移，线条或通孔图形然后如图 3C 所示被转移到层 67 中，其间通孔 71 的通孔腐蚀继续通过介质层 66 和 67 直到下面先前形成的铜线（未示出）．作为变通，线条 70 的图形窗口可以首先通过介质层 67 被转移，然后可以将通孔图形转移到层 67 中以提供图 3C 所示的窗口．然后淀积衬里金属 69，通常用电镀方法将铜淀积到二个图形中，并用 CMP 进行整平，以提供图 3D 所示的线条 70 和通孔 71 的结构。然后如图 3E 所示，在线条 70 的顶部表面上形成无电金属涂层 74．结构继续到下一层时，要求重复图 3E 所示的制作平整介质层 66'和 67'的步骤．无电涂层 74 现在将线条 70 的铜表面分隔于制作在其上的平整介质 66'．层 23、27、32 和 37 所用的材料可以被用于图 2A-2D 中的层 55 和 57 以及图 3A-3E 中的层 65 和 67．层 26、31、36 和 42 所用的材料可以被用于图 2A-2D 中的层 56 以及图 3A-3E 中的层 66.

在图 2 和 3 所示的单镶嵌工艺和双重镶嵌工艺二者中，借助于用金属层 59、63、69 和 74 整个包围铜导体，提供了可靠性方面的至关重要的改善。目前主要厂家的铜 BEOL 工艺仅仅提供图 1 所示的由衬

里 38 形成的三面覆盖，而导体 39 的第四表面即顶部表面被示为与介质接触，此介质通常是覆盖介质层 42，其界面是铜原子输运和原子空洞的根源。

图 4 所示的测试结构 75 被用于电迁移寿命测量。图 4 示出了具有 SiNx/SiO2 介质的三层镶嵌互连的剖面图。介质层 67 具有通过 W 通孔 77 连接到衬里 69 下表面和铜导体 70 第一端的下 W 线条 76。铜导体 70 在三个表面上具有衬里 69，且宽度为 0.28μm。铜导体 70 被电镀。铜导体 70 的第二端通过衬里 79 被连接到铜导体 80 的下表面。电子流从 W 线条 76 流到铜导体 80。用 CMP 整平铜导体 70 和介质层 67 的上表面。然后在铜导体 70 的上表面上制作金属膜 74。氮化硅组成的介质层 66'被制作在层 67 和铜导体 70 上。介质层 67'被制作在层 66'上。在介质层 67'中形成沟槽和通孔，并在沟槽和通孔中制作衬里，随之以用铜导体 80 进行填充。用 CMP 对层 67'和铜导体 80 进行整平。铜导体 80 被选择成宽而短，以防止铜导体 80 中的电迁移损伤。氮化硅组成的层 82 被制作在层 67'和铜导体 80 上。介质层 84 被制作在层 82 上。具有各种各样无电淀积的金属涂层 74 的以及图 1 所示的无涂层的测试结构 75，在 294℃和 25mA/mm^2 下被测量电迁移。

图 5 示出了在 294℃下的电迁移测试，说明了三面具有金属衬里 69 并在铜导体 70 的顶部表面上涂敷有金属层 74 的铜线的优异的寿命。在图 5 中，纵坐标表示 R/R_0，而横坐标表示时间，单位为小时。注意，作为监视着迁移速率的时间的函数的电阻变化，在图 5 中未曾达到 1.2 的正常失效水平，表示甚至在未被涂敷的铜线的 20 倍失效时间之后，被涂敷的样品的电阻改变 20%。图 5 示出了金属涂层 74 明显地改善了电迁移寿命。测试结构 75 中的铜导体 70 的电阻变化被监测为跟踪正在发生的铜原子迁移的程度的手段，电阻随时间改变得越多，铜原子输运就越多，且铜导体寿命就越短。如图 5 所示，在曲线 91-94 所示的未被涂敷的样品中，电阻急剧地增大，而在所有被金属膜 74 涂敷的样品中，如曲线 97-99 所示，电阻变化很慢。在此测试中，正常寿命被定义为相对于其原来电阻 R_0 变化 20%，且直至至少 2200 小时之

后仍然没有达到，而顶部表面无涂层的铜线在 100 小时之内就失效。发现曲线 97 所示的采用 CoWP 涂层 74 的变化速率最低，但曲线 98 所示的 CoSnP 以及曲线 99 所示的 Pd 的所有涂层 74 同样提供长的寿命。可望此改善外推到使用温度 100℃会给出二个数量级以上的电迁移和应力迁移寿命增加，这意味着电路设计者有极大的灵活性，并有效地消除了作为使用电流限制因素的电迁移。还发现，在标准的未被涂敷的样品中产生空洞的热循环条件下，在同一组被涂敷的样品中未观察到原子应力空洞。这一测试结果进一步支持了未被介质涂敷的铜的表面或界面是电迁移因而是可靠性退化的主要根源的假说。

虽然已经描述了借助于在铜导体上表面上形成具有金属对金属的化学键合和金属键合的导电膜来改善铜导体中的抗电迁移性和降低应力引起的迁移的结构和方法，但对于本技术的熟练人员来说，显然可以作出各种修正和变化而不偏离仅仅被所附权利要求的范围所限制的本发明的宽广范围。

说 明 书 附 图

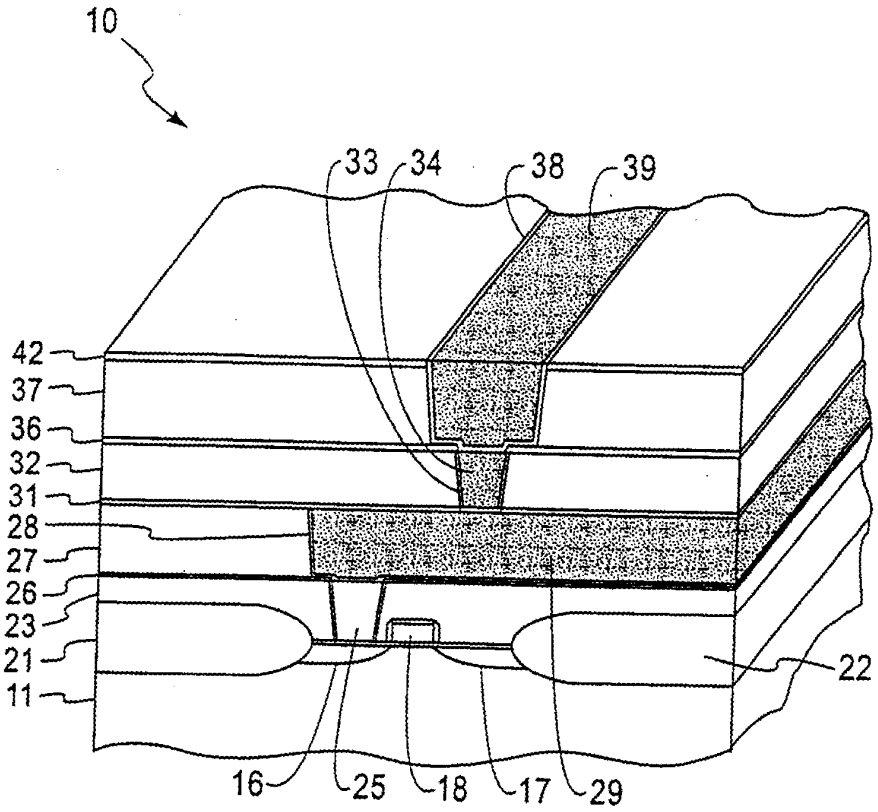


图 1

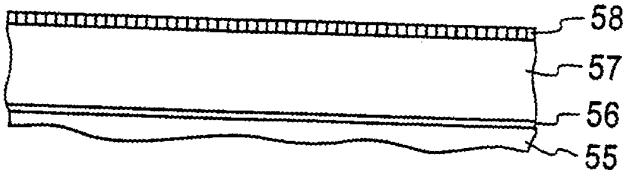


图 2A

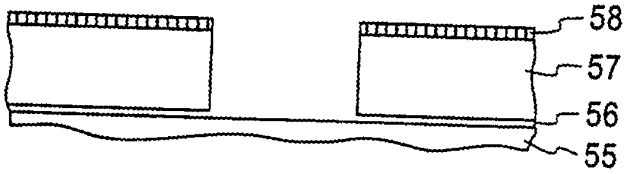


图 2B

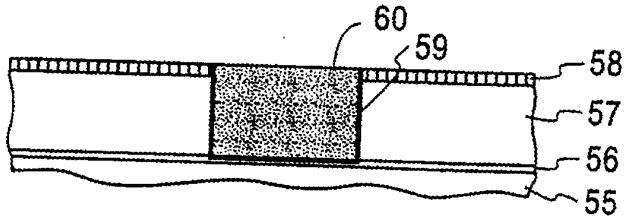


图 2C

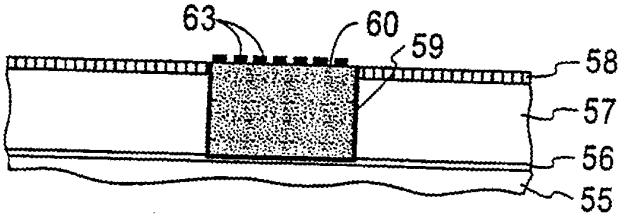


图 2D

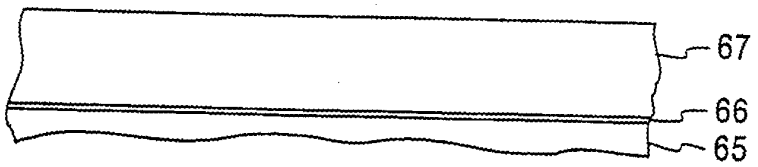


图 3A

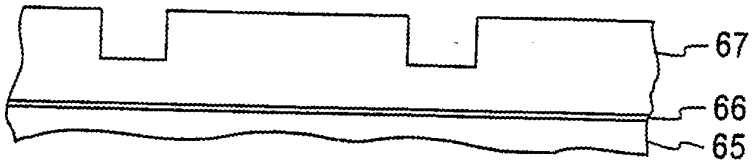


图 3B

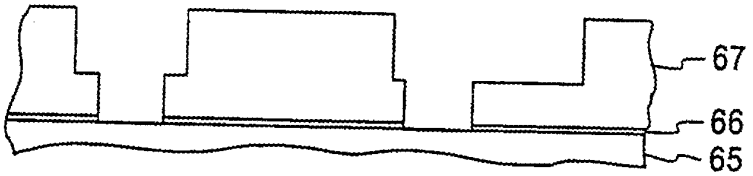


图 3C

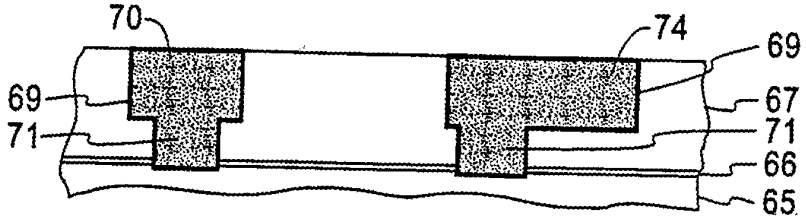


图 3D

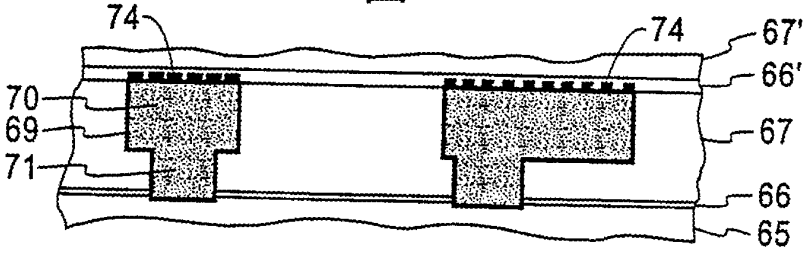


图 3E

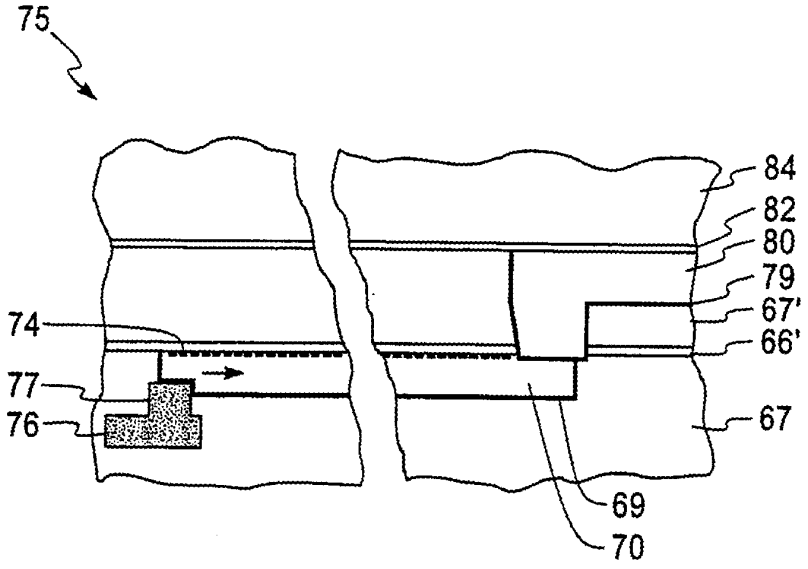


图 4

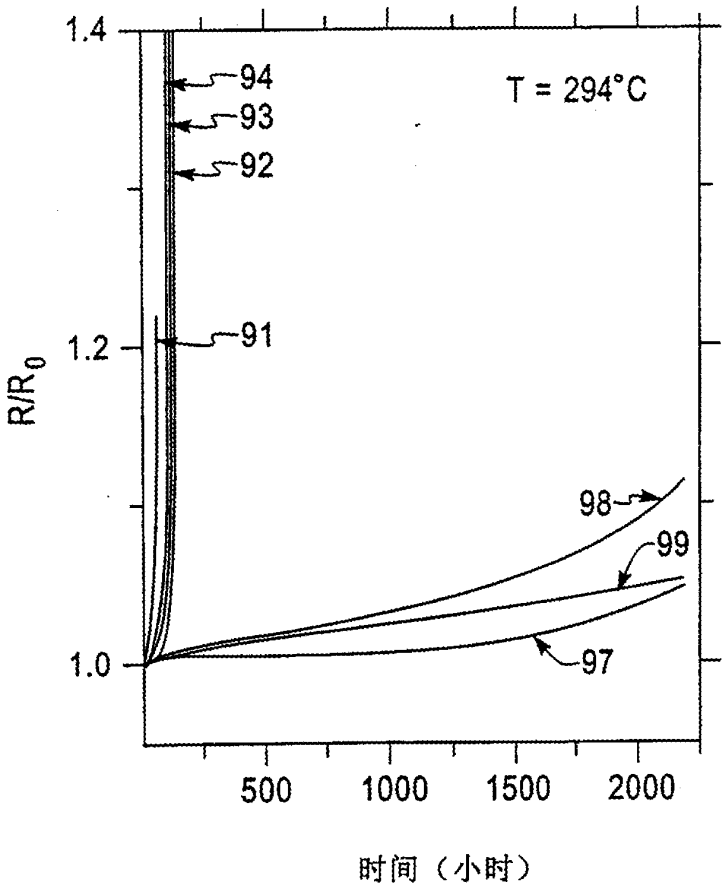


图 5

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DESCRIPTION CN1364311

Surface coating method to reduce electromigration and stress induced migration of copper wiring

Technical field

The present invention relates to metal interconnections on semiconductor chips, and more particularly relates to a surface coating or treatment for preventing the downward movement of atoms of a conductor surface by an electron current, i.e. the so-called electromigration phenomenon and/or prevention of a tendency The stress gradient that releases the stress causes the surface of the conductor to move, that is, the so-called stress-induced migration.

Background technique

The ever-increasing density and speed of microelectronics have shifted the metallization system from Al(Cu) to Cu in order to reduce the resistance of the conductor. At the same time, the requirement for higher current densities has exposed the Al(Cu) wire as a result of electromigration failure, limiting the range of performance that circuit designers can improve. The higher melting point of copper is expected to improve the current carrying capacity of the conductor and extend the electromigration life. However, we have found from the test results that the electromigration lifetime mainly depends on the atomic behavior such as the atomic transport at the copper/dielectric interface, and does not depend on the copper lattice, grain boundaries, or copper/liner interfacial atoms The intrinsic properties of transport. Thus, it was confirmed that the copper conductor's current-carrying characteristics are not significantly superior to Al(Cu).

The basic process for fabricating a copper conductor pattern is to use a damascene method in which a trench is formed in a dielectric layer, a liner is formed in the trench, the trench is then filled with copper, and chemical mechanical polishing (CMP) is performed on the trench to terminate it. Dielectric layer coplanar clean copper top surface. The copper/metal liner interface is formed on the other three surfaces of the copper conductor. Electromigration lifetime is a function of line thickness, width, and cross-sectional area. The measured data show that only the top surface contributes to the mass transport of copper conductors having a bamboo-like and near-bamboo grain structure, while the combination of the boundary and the surface contributes to the mass transport of the wider lines. The same relationship was found to be independent of the copper deposition method, i.e., this problem occurs regardless of whether deposition is performed by physical vapor deposition (PVD), chemical vapor deposition (CVD), or electroplating. In addition to the electromigration lifetime failure, it has also been found that the copper conductor pattern is sensitive to the atomic voids under thermal cycling stress and it was found that the voids always start at the copper/medium interface with the highest atomic mobility. Since the copper migration rate, i.e., the drift speed, is the product of the mobility (D/kT) and the driving force (F), where D is the diffusion rate of copper, T is the absolute temperature, and k is the Boltzmann constant. For electromigration and stress-induced migration forces, the driving forces F are respectively Z<*>eE and (Ds/Dx) W, where Z<*> is the number of effective charges, e is the electronic charge, and E is the electric field, (Ds/ Dx) is the stress gradient and W is the atomic volume. It is unavoidable that achievement of copper conductor technology that can achieve the highest performance and reliability requires changing or correcting the copper/media interface of the overlay to reduce copper transport and atomic voiding.

The modification of the copper conductor surface can be performed after CMP. This process should be selective for copper and provide a thin layer on the surface of the copper conductor so as to remain substantially coplanar with the dielectric or insulator containing the trench. This process must result in better adhesion between the copper conductor and the subsequently fabricated media on the layer and better oxidation resistance of the copper atoms in the copper conductor and reduced transport of the copper conductor atoms in order to provide the highest reliability.

Summary of the Invention

According to the present invention, the exposed copper surface of the copper conductor is changed by providing a 1-20 nm metal thin layer on the copper surface after a process such as CMP leveling or dry etching for subsequent chip processing and/or chip During use, sensitivity to electromigration, oxidation, corrosion, stress voids, and delamination is reduced, thereby improving reliability and yield. The present invention proposes an electroless metal deposition method as a method of forming a thin metal layer on a copper conductor for improving electromigration lifetime and stress-induced migration.

This selective deposition process includes the following steps.

a. The copper surface was selectively activated with a Pd ion catalyst as shown in Equation 1.

[chemical formula] (1)

This step leaves a plurality of Pd nanoparticles on the surface of the copper wire and is used as a catalyst for the next step.

b. A metal or alloy is selectively deposited by an electroless reduction method as shown in Equation 2.

[chemical formula] (2)

Where Me<n+> is a metal ion, such as Co<2+>.

For example, using a hypophosphite as a reducing agent and a cobalt ion as a covering metal, there is a chemical reaction represented by Equation 3. [chemical formula] (3)

In the present invention, we use the above hypophosphite system and deposit metallic palladium, cobalt, cobalt tungsten, cobalt tungsten phosphide, cobalt tin, cobalt tin phosphide, cobalt phosphide and other alloys of cobalt onto copper. On the surface of the conductor. It will also be understood that other reducing agents can be used, for example dimethylaminoborane capable of depositing other types of alloys such as Co-B or Ni-B.

As a result of the above steps a and b, the exposed surface of the copper conductor is coated with a thin film of a metal compound or alloy preferably having a thickness of 1 to 10 nm. The film is strongly adhered to the copper surface by chemical bonds and/or metal bonds. Copper atoms in or on copper surfaces.

In the damascene process used to fabricate copper interconnects on integrated circuit chips, the following important findings are critical to the present invention.

1.

The thickness of the coating film on the copper surface must be thin: the maximum thickness is 20 nm, preferably 1-10 nm, due to the damascene process. In this way, at least 3 main properties are obtained: a) The resistivity of the copper wire is not influenced or increased by more than 20%, b) The leakage that may be caused by the bridging between the respective copper conductors is eliminated, and c) The copper conductor or copper The line does not need to be leveled further. In order to provide a flat top surface of the dielectric layer subsequently formed thereon without having to level the top surface of the subsequent dielectric layer, a leveling or substantially leveling of the copper conductor/media surface is required. A surface step feature is transferred to the surface by the next layer, especially the surface made by the CVD method.

2.

The preferred component of the coating film may be Co-Sn-P, Co-W-P, Co-P or Pd.

3.

Wafers with a coated film are annealed at 300° C. for 2 hours to further improve the chemical or metal bonding with the copper surface and slow the diffusion of copper atoms along the copper surface at the copper conductor/dielectric interface and along the copper atoms Grain boundary diffusion.

The copper conductor/dielectric interface is between the copper conductor and the dielectric layer formed on the copper conductor. The copper conductors in the damascene process are located in the trenches in the metal liner of the metal liner that is made in the trench prior to filling the trench with the copper conductor.

4.

Metal selective CVD or other deposition processes can also be used to deposit a metal film on a surface of a chemically and/or metalically bonded copper conductor in order to obtain a higher electromigration resistance of the copper conductor.

Description of the drawings

These and other features, objects, and advantages of the present invention will become apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings, in which:

FIG. 1 is a sectional view of an embodiment of the present invention.

2A-2D are cross-sectional views of various stages of manufacture of a second embodiment of the present invention.

3A-3E are cross-sectional views of various stages of manufacture of the third embodiment.

FIG. 4 is a cross-sectional view of a three-layer electromigration test structure.

The graph of Figure 5 shows the ohmic resistance versus time of the copper conductors and linings in the dielectric layer trenches with and without the metal thin film on the top surface.

detailed description

Referring now to the drawings, Fig. 1 is a cross-sectional view of an example of a copper back end (BEOL) structure on an integrated circuit chip 10 containing copper lines and vias made using a single damascene process.

In FIG. 1, the integrated circuit chip 10 has a substrate 11, which may be, for example, Si, SiGe, Ge, SOI, and GaAs.

The source region 16 and the drain region 17 and the gate 18 of a typical FET transistor 19 can be made in the substrate 11. On both sides of the source region 16 and the drain region 17 are oxide regions 21 and 22 recessed on the substrate 11. An oxide layer 23 is formed on the oxide regions 21 and 22 and the FET transistor 19. A source contact window is formed in layer 23 and filled with metal 25, typically tungsten. Layer 23 and metal 25 are planarized by chemical mechanical polishing (CMP). A cover layer 26 made of, for example, silicon nitride is formed on the upper surface of the layer 23. A dielectric layer 27 is formed on layer 26 and forms a trench therein. Liners 28 are formed on the bottom and side walls of the trench and then filled with copper to form lines 29. Layer 27 and line 29 are leveled with CMP. A cover layer 31 is formed on the upper surface of the layer 27 and the line 29. A dielectric layer 32 is formed on the cover layer 31. A via window is formed in layers 31 and 32, followed by the formation of metal liner 33 and metal such as copper in the window to form via 34. The layer 32

and the through hole 34 are leveled by the CMP method. A cover layer 36 is formed on the layer 32 and the through hole 34. A dielectric layer 37 is formed on the cover layer 36. Grooves or windows are formed in layer 37 and cover layer 36. A liner 38 is formed in the grooves of layer 37 and cover layer 36. The trenches are filled with metal copper to form lines 39. The layer 37 and the line 39 are leveled by the CMP method. A cover layer 42 is formed on the layer 37 and the lines 39. The cover layers 26, 31, and 36 are composed of different media than layers 23, 27, 32, and 37 and may be silica, diamond-like carbon (DLC), fluorinated DLC, polyarylene ether, SiCOH, and the like. In No. 09/107,567, filed June 29, 1998, SiCOH is described, which is hereby incorporated by reference to show an example of a low k (dielectric constant) medium. Note that BEOL is manufactured using a single damascene copper process, i.e., each copper layer is separately processed, and the tops of lines 31 and 39 form an interface with the dielectric 8.

Figures 2A-2D illustrate the process sequence used to fabricate single damascene copper lines illustrating selective deposition of a metal cap layer by electroless plating. In this process sequence, as shown in FIG. 2A, dielectric layers 55-57 and 58 are deposited. As shown in FIG. 2B, the pattern is transferred into dielectric layers 56 and 57 using a photolithography process. A liner metal 59 is then deposited, followed by deposition of a copper conductor 60 having a thickness greater than the depth of the pattern. As shown in Fig. 2C, excess copper conductor 60 and liner 59 are removed by CMP to form a flat surface. As shown in FIG. 2D, a thin electroless metal coating 63 is selectively deposited on the copper conductor 60. The process shown in FIGS. 2A-2D can be repeated for the next copper conductor interconnect layer.

Fig. 3 is a process sequence of a dual damascene process in which copper lines and through holes are simultaneously deposited. Starting from the flat dielectric layers 65-67 shown in FIG. 3A, the pattern of vias 71 is transferred through the dielectric layer 67 shown in FIG. 3B, and the line or via pattern is then transferred to layer 67 as shown in FIG. 3C. Through-hole etching of vias 71 continues through the dielectric layers 66 and 67 until the previously formed copper wire (not shown). Alternately, the graphic window of line 70 may be first transferred through dielectric layer 67 and then the via pattern may be transferred into layer 67 to provide the window shown in Figure 3C. A liner metal 69 is then deposited. Copper is generally deposited in two patterns by electroplating and planarized by CMP to provide the structure of lines 70 and vias 71 shown in FIG. 3D. Then, as shown in Fig. 3E, an electroless metal coating 74 is formed on the top surface of the line bar 70. As the structure continues to the next layer, it is required to repeat the steps of making flat media layers 66' and 67' shown in FIG. 3E. The electroless coating 74 now separates the copper surface of the line 70 from the planarized media 66' The materials used for layers 23, 27, 32 and 37 may be used for layers 55 and 57 in Figures 2A-2D and layers 65 and 67 in Figures 3A-3E. The materials used for layers 26, 31, 36, and 42 may be used for layer 56 in FIGS. 2A-2D and layer 66 in FIGS. 3A-3E.

In both the single damascene process and the dual damascene process shown in Figs. 2 and 3, by enveloping the copper conductor entirely with the metal layers 59, 63, 69 and 74, a very important improvement in reliability is provided. Currently, the main manufacturer's copper BEOL process only provides the three-sided cover formed

by the liner 38 shown in FIG. 1, and the fourth surface of the conductor 39, ie, the top surface, is shown in contact with the medium, which is usually the cover dielectric layer 42, and the interface thereof. It is the source of copper atom transport and atom cavity.

The test structure 75 shown in FIG. 4 is used for electromigration life measurement. Figure 4 shows a cross-sectional view of a three-layer damascene interconnect with SiNx/Si02 dielectric. The dielectric layer 67 has lower W lines 76 connected to the lower surface of the liner 69 and the first end of the copper conductor 70 through the W-vias 77. The copper conductor 70 has a liner 69 on three surfaces and has a width of 0.28 μm. The copper conductor 70 is plated. The second end of the copper conductor 70 is connected to the lower surface of the copper conductor 80 through the liner 79. The electron flow flows from the W line 76 to the copper conductor 80. The upper surface of copper conductor 70 and dielectric layer 67 is leveled with CMP. Then, a metal film 74 is formed on the upper surface of the copper conductor 70. A dielectric layer 66' composed of silicon nitride is formed on the layer 67 and the copper conductor 70. Dielectric layer 67' is formed on layer 66'. Grooves and through holes are formed in the dielectric layer 67', and linings are formed in the grooves and through holes, followed by filling with the copper conductor 80. Layer 67' and copper conductor 80 are leveled by CMP. The copper conductor 80 is selected to be wide and short to prevent electromigration damage in the copper conductor 80. A layer 82 of silicon nitride is formed on the layer 67' and the copper conductor 80. Dielectric layer 84 is formed on layer 82. The test structures 75 with various electrolessly deposited metal coatings 74 and without the coatings shown in Figure 1 were electromigrated at 294C and 25 mA/mm<2>.

FIG. 5 shows an electromigration test at 294° C. illustrating the excellent lifetime of a copper wire with a metal liner 69 on three sides and a metal layer 74 coated on the top surface of the copper conductor 70. In FIG. 5, the ordinate represents R/R0 and the abscissa represents time in hours. Note that as a function of the change in resistance as a function of the monitoring rate of the migration rate, a normal failure level of 1.2 was not reached in FIG. 5, indicating that even after 20 times the time of failure of the uncoated copper wire, the sample was coated. Change the resistance by 20%. Figure 5 shows that the metal coating 74 significantly improves the electromigration lifetime. The change in resistance of the copper conductor 70 in the test structure 75 is monitored as a means to track the extent of the copper atom migration that is occurring. The more the resistance changes over time, the more copper atoms are transported and the shorter the copper conductor life is. As shown in FIG. 5, in the uncoated samples shown in curves 91-94, the resistance increases sharply, and in all the samples coated by the metal film 74, as shown by curves 97-99, the resistance The change is slow. In this test, the normal life is defined as a 20% change from its original resistance R0, and it is still not reached after at least 2200 hours, and the uncoated copper wire on the top surface fails within 100 hours. The curve 97 shows the lowest rate of change with the CoWP coating 74, but all the CoSnP shown by the curve 98 and the Pd shown by the curve 99 all provide longevity as well. Expecting this improvement to be extrapolated to the operating temperature of 100° C will give an electromigration and stress migration lifetime increase of more than two orders of magnitude, which means that the circuit designer has great flexibility and effectively eliminates the use of current limiting The electromigration of factors. It has also been found that no atomic stress voids are observed in the same set of coated samples under thermal cycling conditions that produce voids in a standard, uncoated sample.

This test result further supports the hypothesis that the surface or interface of the copper that is not coated with the media is electromigration and thus a major source of reliability degradation.

Although structures and methods for improving electromigration resistance in copper conductors and reducing stress induced migration by forming a conductive film having metal-to-metal chemical bonding and metal bonding on an upper surface of a copper conductor have been described, It will be apparent to those skilled in the art that various modifications and variations can be made without departing from the broad scope of the invention, which is limited only by the scope of the appended claims.

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CLAIMS CN1364311

1.

A method for fabricating a conductor having high resistance to electromigration, comprising the steps of: forming a dielectric layer on a substrate, forming at least one trench in the dielectric layer, forming a metal liner in the trench, A conductor is formed on the metal liner to fill the trench, a flattened upper surface of the conductor coplanar with the upper surface of the dielectric layer is formed, and a conductive film is formed on the upper surface of the conductor. The conductive film forms a metal-to-metal metal bond.

2.

The method of claim 1, characterized in that said step of forming a conductive film includes the step of forming said conductive film by an electroless deposition method so that said upper surface of said conductor is prevented from oxidation and corrosion and provided High resistance to electromigration and high resistance to thermal stress cavitation.

3.

The method according to claim 2, wherein the electroless deposited film has a thickness of 1 to 20 nm.

4.

The method according to claim 2, wherein the electroless deposited film has a thickness of 1 to 10 nm.

5.

The method of claim 2, wherein said electroless deposition step includes the following steps:

The substrate is first immersed in a solution of a metal ion to form a metallic nanoparticle layer on the upper surface of the conductor.

The substrate is then immersed again in an electroless complex solution of metal ions and hypophosphite ions to form a metal phosphide conductive film on the upper surface of the conductor, and

The substrate is annealed for at least 2 hours at a temperature of at least 300° C in an inert or reducing atmosphere to obtain excellent adhesion between the conductor and the metal phosphide conductive film.

6.
The method of claim 5, wherein the re-immersion step is omitted.

7.
The method of claim 5, wherein the conductive film is selected from the group consisting of CoWP, CoSnP, CoP, Pd, In, and W, and has a thickness of 1-20 nm.

8.
The method of claim 2, wherein said electroless deposition step includes the following steps:

The substrate is first immersed in a metal ion solution to form a metal nanoparticle layer on the surface of the conductor.

The substrate is then immersed again in an electroless complex solution of metal ions and dimethylaminoborane to form a metal-boron conductive film layer on the upper surface of the conductor, and

The substrate is annealed for at least 2 hours at a temperature of at least 300° C in an inert or reducing atmosphere to obtain excellent adhesion between the conductor and the metal boron conductive film.

9.
The method of claim 1, characterized in that said conducting is performed by a physical method such as

chemical vapor deposition (CVD), physical vapor deposition (PVD), evaporation, sputtering, and metal thermal interdiffusion. A film is coated on the surface of the conductor.

10.
The method of claim 9, wherein the conductive film is selected from the group consisting of Pd, In, W, and mixtures thereof.

11.
A structure that contains:

The dielectric layer on the substrate,

Fabricating at least one groove in the medium on the substrate,

Making a metal lining in the groove,

The conductor on the lining filling the trench,

The flattened upper surface of the conductor with the upper surface of the dielectric layer, and

The conductor is a conductive film on the upper surface, and the conductive film forms a metal-to-metal chemical bond and a metal bond.

12.
The structure of claim 11, characterized in that said conductive film is selected from the group consisting of CoWP, CoSnP, CoP, Pd, CoB, CoSnB, CoWB, In, NiB and W so as to prevent said upper surface of said conductor from being Oxidation and corrosion.

13.
The structure of claim 12, wherein the conductive film has a thickness of 1 to 20 nm.

14.
The structure of claim 12 further comprising an insulating dielectric coating on said conductive film and said dielectric layer on said dielectric layer.

15.
The structure of claim 14, characterized in that said insulating dielectric coating is selected from the group consisting of silicon nitride, silicon oxide, an insulating compound having a dielectric constant of less than 3.2, SICOH, diamond-like carbon, fluorinated diamond-like carbon, and polyarylene Group of ethers.

16.
The structure of claim 11 wherein said conductor is selected from the group consisting of copper and copper alloys.

17.
The structure of claim 11 wherein the substrate is selected from the group consisting of silicon, silicon germanium, SOI, and gallium arsenide.

18.
A method for manufacturing a conductor having high resistance to electromigration, which includes the following steps:

Forming a patterned conductor on the substrate

A conductive film is formed on the surface of the conductor, and the conductive film forms a metal-to-metal metal bond.

19.
The method of claim 18, wherein said step of forming a conductive film includes the step of forming said conductive film by an electroless deposition method so that said surface of said conductor is prevented from oxidation and corrosion and provided High resistance to electromigration and high thermal stress cavitation.

20.

The method of claim 19, wherein the electroless deposited film has a thickness of 1-20 nm.

21.
The method of claim 19, wherein the electroless deposited film has a thickness of 1 to 10 nm.

22.
The method of claim 19, wherein said electroless deposition step comprises the following steps:

The substrate is first immersed in a solution of a metal ion to form a metallic nanoparticle layer on the surface of the conductor.

The substrate is then immersed again in an electroless complex solution of metal ions and hypophosphite ions to form a metal phosphide conductive film on the surface of the conductor, and

The substrate is annealed for at least 2 hours at a temperature of at least 300° C in an inert or reducing atmosphere to obtain excellent adhesion between the conductor and the metal phosphide conductive film.

23.
The method of claim 22, wherein the re-immersion step is omitted.

24.
The method of claim 22, wherein the conductive film is selected from the group consisting of CoWP, CoSnP, CoP, Pd, In, and W, and has a thickness of 1 to 20 nm.

25.
The method of claim 19, wherein said electroless deposition step comprises the following steps:

The substrate is first immersed in a metal ion solution to form a metal nanoparticle layer on the surface of the conductor.

The substrate is then immersed again in an electroless complex solution of metal ions and dimethylaminoborane

to form a metal-boron conductive film on the surface of the conductor, and

The substrate is annealed for at least 2 hours at a temperature of at least 300° C in an inert or reducing atmosphere to obtain excellent adhesion between the conductor and the metal boron conductive film.

26.
The method of claim 18, characterized in that said conducting is performed by a physical method such as chemical vapor deposition (CVD), physical vapor deposition (PVD), evaporation, sputtering, and metal thermal interdiffusion. A film is coated on the surface of the conductor.

27.
The method of claim 26, wherein the conductive film is selected from the group consisting of Pd, In, W, and mixtures thereof.

28.
A structure that contains:

Patterned conductor on the substrate,

A conductive film on the surface of the substrate, the conductive film forming a metal-to-metal metal bond.

29.
The structure of claim 28, wherein said conductive film is selected from the group consisting of CoWP, CoSnP, CoP, Pd, CoB, CoSnB, CoWB, In, NiB, and W so as to prevent said upper surface of said conductor from being Oxidation and corrosion.

30.
The structure of claim 29, wherein the conductive film has a thickness of 1 to 20 nm.

31.
The structure of claim 29, further comprising an insulating dielectric coating on said conductive film of said conductor.

32.
The structure of claim 31, characterized in that said insulating dielectric coating is selected from the group consisting of silicon nitride, silicon oxide, an insulating compound having a dielectric constant of less than 3.2 SICOH, diamond-like carbon, fluorinated diamond-like carbon, and polyarylene Group of ethers.

33.
The structure of claim 29, wherein the conductor is selected from the group consisting of copper and a copper alloy.

34.
The structure of claim 29, wherein the substrate is selected from the group consisting of silicon, silicon germanium, SOI, and gallium arsenide.

35.
The method of claim 8, wherein the conductive film is selected from the group consisting of CoB, CoSnB, CoWB, and NiB.

36.
The method of claim 25, wherein the conductive film is selected from the group consisting of CoB, CoSnB, CoWB, and NiB.

Espacenet

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Copper interconnect structures and fabrication method thereof, semiconductor device

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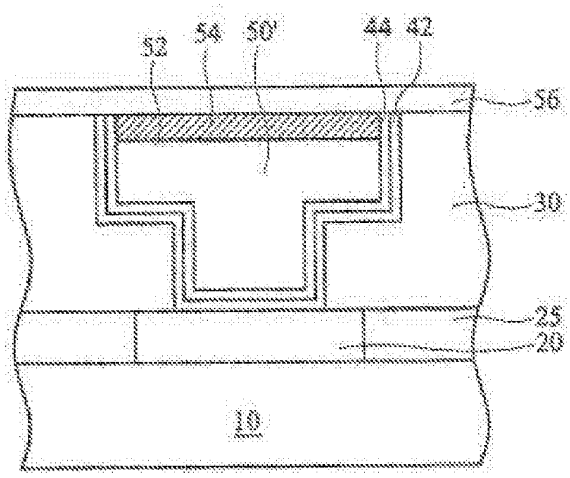
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The interconnect structure has a damascene structure with a via (32) or trench (34) in a dielectric layer (30). A conductor whose top surface is lower than the top surface of the dielectric layer, is filled the via or trench. A cobalt-comprising cap having metal cobalt (Co), cobalt tungsten (CoW), cobalt tungsten phosphide (CoWP) or cobalt tungsten boride (CoWB), on the conductor. An independent claim is included for method for fabricating interconnect structure.



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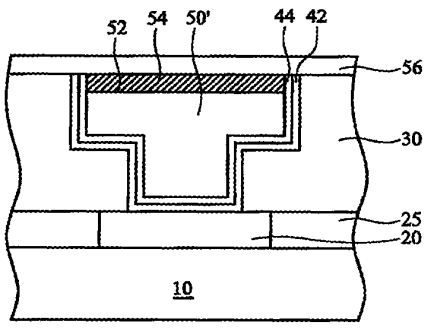
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[54] 发明名称

内连线结构及其制造方法、半导体装置

[57] 摘要

本发明提供一种铜内连线结构以做为内连线。上述内连线结构具有铜凹陷，其位于以铜填入位于介电层中的介层孔/沟槽的镶嵌结构中。另外，上述内连线结构也可以具有金属覆盖层，填入上述铜凹陷中。由于本发明的内连线结构包括铜凹陷，以选择性成长方式在上述铜凹陷上形成的金属覆盖层可受到良好的控制。



1. 一种内连线结构，包括：

镶嵌结构，包括介电层，以及位于该介电层中的介层孔和/或沟槽；

导体，填入该介层孔和/或该沟槽中，其中该导体的顶面低于该介电层的顶面；以及

含钴覆盖层，位于该导体上。

2. 如权利要求 1 所述的内连线结构，其中该导体的该顶面与该介电层的该顶面之间的距离为 20Å 至 200Å。

3. 如权利要求 1 所述的内连线结构，其中该导体上的该含钴覆盖层的顶面与该介电层的该顶面大体上为共平面。

4. 如权利要求 3 所述的内连线结构，其中该含钴覆盖层包括钴、钨化钴、磷钨化钴或硼钨化钴。

5. 如权利要求 1 所述的内连线结构，其中该导体包括铜或铜合金。

6. 如权利要求 1 所述的内连线结构，还包括蚀刻停止层，位于该含钴覆盖层以及该介电层上。

7. 一种内连线结构的制造方法，包括：

在介电层中形成镶嵌结构；

在该镶嵌结构中填入导电材料以形成导体；

凹陷该导体的表面，使其低于该介电层的顶面；以及

在凹陷的该导体上形成含钴覆盖层。

8. 如权利要求 7 所述的内连线结构的制造方法，其中该导体的凹陷工艺为化学机械抛光工艺。

9. 如权利要求 8 所述的内连线结构的制造方法，其中该化学机械抛光工艺以过氧化氢、硝酸、次氯酸、铬酸、氨水或铵盐为氧化剂，以及以研浆为研磨剂进行。

10. 如权利要求 7 所述的内连线结构的制造方法，还包括：

填入该导电材料之前，形成导电阻挡层和/或种子层衬于该镶嵌结构上；

进行化学机械抛光工艺使该导体的该表面大体上与位于该介电层上的该导电阻挡层和/或该种子层的顶面共平面；以及

凹陷该导体的该表面之前，移除位于该介电层上的该导电阻挡层和/或该

种子层。

11. 如权利要求 7 所述的内连线结构的制造方法，其中该含钴覆盖层形成于凹陷的该导体上，且该含钴覆盖层未延伸至该介电层的该顶面上。

12. 如权利要求 7 所述的内连线结构的制造方法，其中该含钴覆盖层包括钴、钨化钴、磷钨化钴或硼钨化钴。

13. 如权利要求 7 所述的内连线结构的制造方法，其中该含钴覆盖层以选择性成长方式形成。

14. 如权利要求 7 所述的内连线结构的制造方法，其中形成该含钴覆盖层之前，进行清洁工艺以凹陷该导体。

15. 如权利要求 14 所述的内连线结构的制造方法，其中该清洁工艺是在含酸环境进行，其中该酸包括硝酸、次氯酸或铬酸。

16. 如权利要求 7 所述的内连线结构的制造方法，其中该导体包括铜或铜合金。

17. 如权利要求 7 所述的内连线结构的制造方法，还包括形成蚀刻停止层，覆盖于该含钴覆盖层以及该介电层上。

内连线结构及其制造方法、半导体装置

技术领域

本发明关于一种铜内连线结构的制造方法，特别关于形成铜凹陷于镶嵌结构中。

背景技术

芯片制造业者持续不断地试图改进工艺以达到更高的芯片操作速率。在半导体工艺技术也同时发展的情形下，多层内连线的电阻/电容时间延迟(RC delay)效应会妨碍芯片操作速率。多层内连线电阻以及多层内连线间电容的增加，产生了电阻/电容时间延迟效应。由于铜的电阻低，所以铜为多层内连线材料中的最佳选择的一。

在公知的铜内连线工艺中，在铜的化学机械抛光工艺(chemical mechanical polishing, CMP)后会形成例如氮化物层的介电停止层(dielectric stop layer)。铜与停止层之间的界面不良是元件可靠度的主要阻碍。所以例如钨(W)、钴(Co)、磷钨化钴(CoWP)或硼钨化钴(CoWB)的金属覆盖层被提供以改善铜与停止层之间的界面。如此，上述的金属覆盖层通常以选择性成长方式形成，但此种形成方式却难以控制且会导致金属覆盖层往横向成长。因为金属覆盖层的横向成长而引起的漏电是重大的问题。

发明内容

有鉴于此，本发明的主要目的是提供一种铜内连线结构的制造方法，形成铜凹陷于镶嵌结构中，以改善上述公知技术的问题。

本发明提供一种内连线结构，包括：

镶嵌结构，包括介电层，以及位于该介电层中的介层孔和/或沟槽；

导体，填入该介层孔和/或该沟槽中，其中该导体的顶面低于该介电层的顶面；以及

含钴覆盖层，位于该导体上。

根据所述的内连线结构，其中该导体的该顶面与该介电层的该顶面之间的距离为 20Å 至 200Å。

根据所述的内连线结构，其中该导体上的该含钴覆盖层的顶面与该介电层的该顶面大体上为共平面。

根据所述的内连线结构，其中该含钴覆盖层包括钴、钨化钴、磷钨化钴或硼钨化钴。

根据所述的内连线结构，其中该导体包括铜或铜合金。

根据所述的内连线结构，还包括蚀刻停止层，位于该含钴覆盖层以及该介电层上。

本发明还提供一种内连线结构的制造方法，包括：

在介电层中形成镶嵌结构；

在该镶嵌结构中填入导电材料以形成导体；

凹陷该导体的表面，使其低于该介电层的顶面；以及

在凹陷的该导体上形成含钴覆盖层。

根据所述的内连线结构的制造方法，其中该导体的凹陷工艺为化学机械抛光工艺。

根据所述的内连线结构的制造方法，其中该化学机械抛光工艺以过氧化氢、硝酸、次氯酸、铬酸、氨水或铵盐为氧化剂，以及以研浆为研磨剂进行。

根据所述的内连线结构的制造方法，还包括：

填入该导电材料之前，形成导电阻挡层和/或种子层衬于该镶嵌结构上；

进行化学机械抛光工艺使该导体的该表面大体上与位于该介电层上的该导电阻挡层和/或该种子层的顶面共平面；以及

凹陷该导体的该表面之前，移除位于该介电层上的该导电阻挡层和/或该种子层。

根据所述的内连线结构的制造方法，其中该含钴覆盖层形成于凹陷的该导体上，且该含钴覆盖层未延伸至该介电层的该顶面上。

根据所述的内连线结构的制造方法，其中该含钴覆盖层包括钴、钨化钴、磷钨化钴或硼钨化钴。

根据所述的内连线结构的制造方法，其中该含钴覆盖层以选择性成长方式形成。

根据所述的内连线结构的制造方法，其中形成该含钴覆盖层之前，进行清洁工艺以凹陷该导体。

根据所述的内连线结构的制造方法，其中该清洁工艺是在含酸环境进行，其中该酸包括硝酸、次氯酸或铬酸。

根据所述的内连线结构的制造方法，其中该导体包括铜或铜合金。

根据所述的内连线结构的制造方法，还包括形成蚀刻停止层，覆盖于该含钴覆盖层以及该介电层上。

本发明实施例提供一种内连线结构的制造方法，包括：镶嵌结构以及铜导体，上述铜导体位于上述镶嵌结构中。上述镶嵌结构包括介层孔和/或沟槽，其位于介电层中。上述导体的顶面低于上述介电层的顶面；以及形成导体凹陷。

此外，本发明实施例提供另一种内连线结构。上述内连线结构包括导体凹陷，其位于镶嵌结构中；以及导电覆盖层，位于上述导体凹陷上，且上述导电覆盖层未延伸至上述介电层的上述顶面上。

本发明实施例还提供一种内连线结构的制造方法，包括：形成介层孔/沟槽于介电层中。填入铜导体于上述介层孔/沟槽中，且大体上超过上述介电层的表面。之后，进行铜移除工艺，使上述导体的顶面低于上述介电层的顶面，以形成铜凹陷。

由于内连线结构包括铜凹陷，以选择性成长方式在上述铜凹陷上形成的金属覆盖层可受到良好的控制。上述金属覆盖层不会往横向成长而导致短路或漏电问题的发生。

附图说明

图 1A-1H 为剖面图，显示本发明实施例的内连线结构的制造方法。

其中，附图标记说明如下：

10 衬底

20 金属内连线；

25 絶缘层

30 介电层；

32 介层孔部位

34 沟槽部位
42 导电阻挡层
44 种子层；
50、50' 导体
52 凹陷
54 覆盖层
56 蚀刻停止层
60 双镶嵌结构

具体实施方式

以下利用工艺剖面图，以更详细地说明本发明优选实施例的内连线结构及其制造方法。在本发明各实施例中，相同的符号表示相同的元件。

如图 1A 所示，提供半导体衬底 10。如图 1A 所示，在例如氧化硅的絶缘层 25 内部图案化金属内连线 20。另外，沉积介电层 30，并图案化此介电层 30 使其具有介层孔部位 32 以及沟槽部位 34，借以形成包含介层孔部位 32 以及沟槽部位 34 的双镶嵌结构 60。虽然双镶嵌结构已显示在图 1A 至图 1H，但非限于此双镶嵌结构，其它类型的内连线图案也是使用此典型的技术金属化。

如图 1B 所示，沉积导电阻挡层 42 于介电层 30 的顶面上以及衬于介层孔部位 32 以及沟槽部位 34 的表面，导电阻挡层 42 优选包括钽(Ta)或氮化钽(TaN)。接着，如图 1B 所示，顺应性地沉积例如铜种子层的种子层 44 于导电阻挡层 42 上。

如图 1C 所示，例如铜或铜合金的导体 50，利用例如非电镀法或电镀法的镀膜工艺，填入于介层孔部位 32 以及沟槽部位 34 中且超过此两者的表面。借此，铜导体 50 经由导电阻挡层 42 电性连接至位于下方的金属内连线 20。

接着，如图 1D 所示，进行化学机械抛光工艺以移除一部分铜导体 50 以及使其顶面平坦化，使得残留的铜导体 50'大体上与位于介电层 30 上的导电阻挡层 42 共平面(或种子层 44，假使仅存在种子层 44 时)。的后，如第 1E 图所示，以蚀刻或其它化学机械抛光工艺，移除位于介电层 30 上的种子层 44 以及导电阻挡层 42。如此，残留的铜导体 50'的顶面会稍微高于介电层 30

的顶面。

如图 1F 所示，形成铜导体 50'的凹陷 52，其深度为 20Å 至 200Å。可用化学机械抛光工艺形成铜凹陷 52。化学机械抛光工艺优选以过氧化氢(hydrogen peroxide, H_2O_2)、硝酸(nitric acid)、次氯酸(hypochlorous acid)、铬酸(chromic acid)、氨水(ammonia)或铵盐(ammonium salt)为氧化剂；以及以例如氧化铝(alumina, Al_2O_3)的研浆为研磨剂；和加入苯并三唑(Benzotriazole, BTA)的去离子水(Deionized Water, DI water)进行。

也可以用移除位于介电层 30 上的导电阻挡层 42 之后的清洁工艺形成导体的凹陷 52。清洁工艺是在含酸环境进行，其中上述酸包括硝酸、次氯酸、铬酸或者类似的酸。

还或者，如图 1G 所示，形成导电覆盖层 54 以填充导体的凹陷 52。典型地，导电覆盖层 54 以选择性成长方式形成，以致于导电材料只会形成于铜导体 50'的表面上以及其凹陷中。在优选实施例中，导电覆盖层 54 的顶面与介电层 30 的顶面大体上为共平面(两者具有相同表面)。优选地，导电覆盖层 54 的顶面不超过介电层 30 的顶面。导电覆盖层 54 的材质可为任何适合的导电材料，例如以化学气相沉积法(CVD)形成的钨层。优选的导电覆盖层 54 为含钴覆盖层。含钴覆盖层可为钴(Co)、钨化钴(CoW)、磷钨化钴(CoWP)或硼钨化钴(CoWB)。假使移除位于介电层 30 上的导电阻挡层 42 之后，并无清洁工艺或额外的化学机械抛光工艺形成铜凹陷 52，则铜凹陷 52 可以经由形成覆盖层前的预清洁工艺(pre-cap clean procss)。形成覆盖层前的预清洁工艺可在含酸环境进行，其中上述酸包括硝酸、次氯酸、铬酸或者类似的酸。

由于铜连线结构包括铜凹陷，以选择性成长方式在铜凹陷上形成的导电覆盖层可受到良好的控制。导电覆盖层不会往横向成长而导致短路或漏电问题的发生。如图 1H 所示，在优选实施例中，可形成蚀刻停止层 56 覆盖于导电覆盖层 54 以及介电层 30 上。而含钴覆盖层 54 也可改善铜导体 50'以及其上的蚀刻停止层 56 之间的界面。

虽然本发明已以优选实施例揭示如上，然其并非用以限定本发明，任何本领域的技术人员，在不脱离本发明的精神和范围内，当可做些许更动与润饰，因此本发明的保护范围当视后附的权利要求所界定的为准。

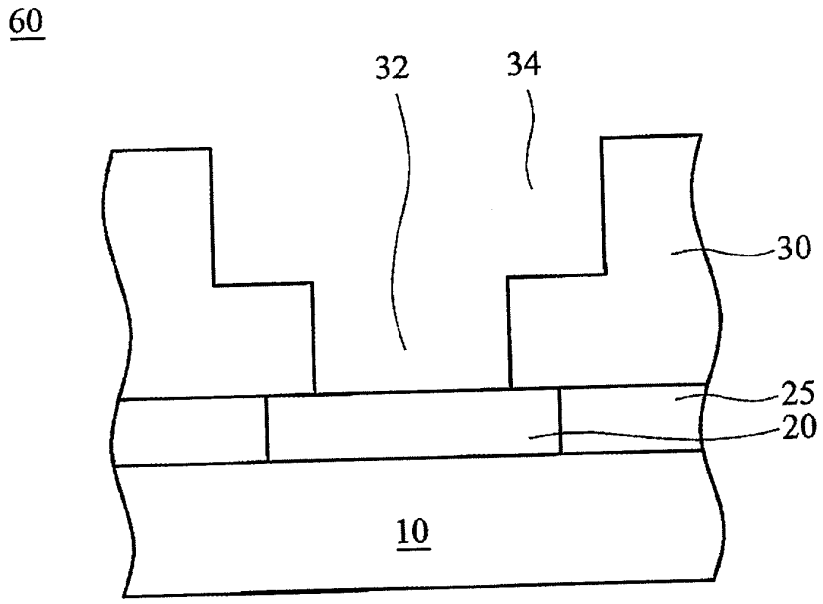


图 1A

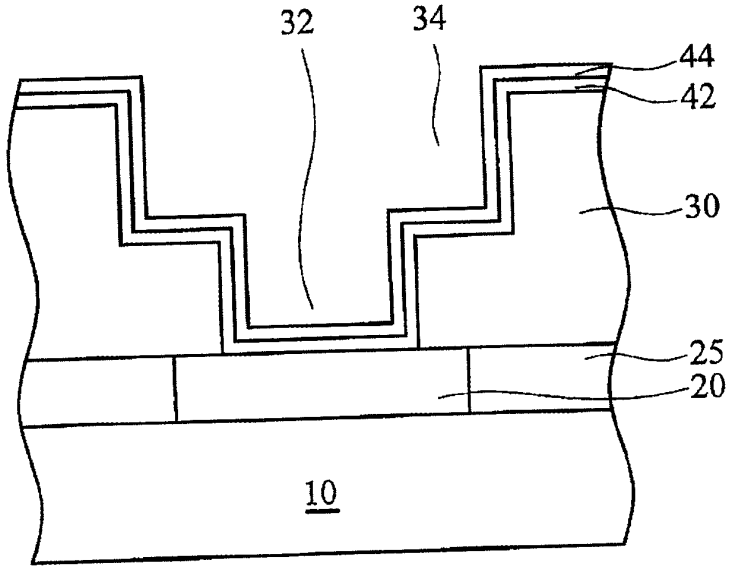


图 1B

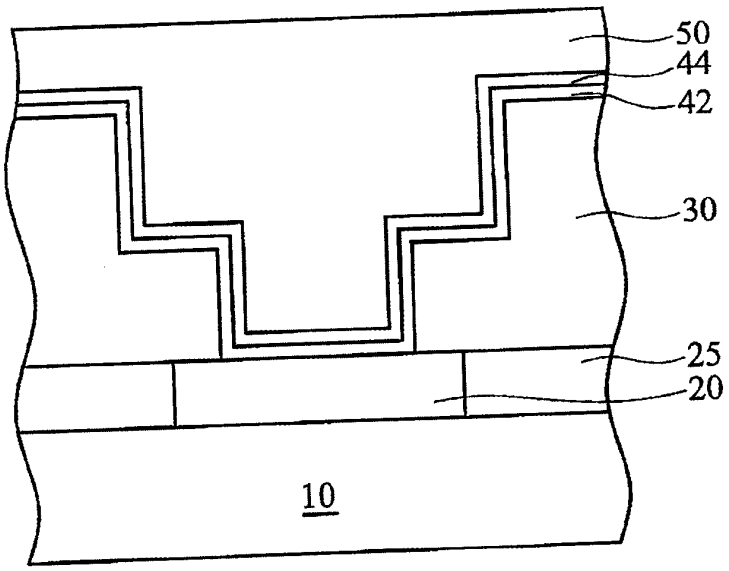


图 1C

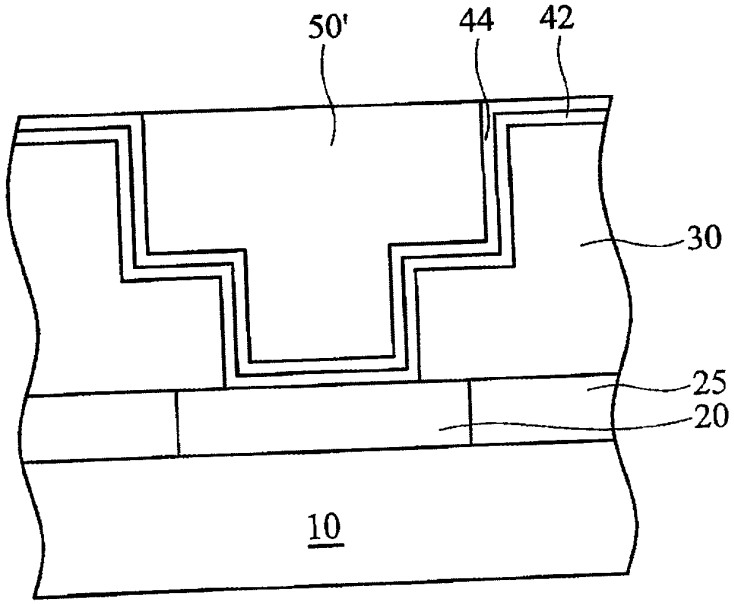


图 1D

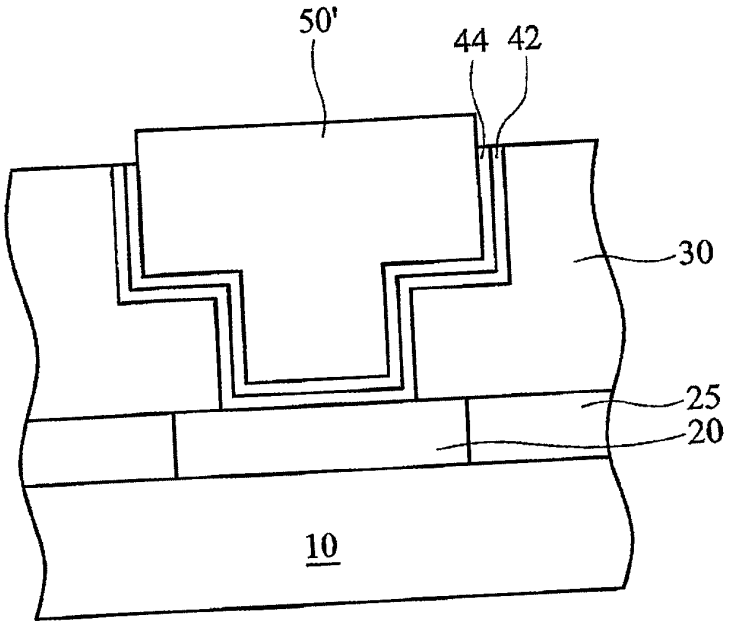


图 1E

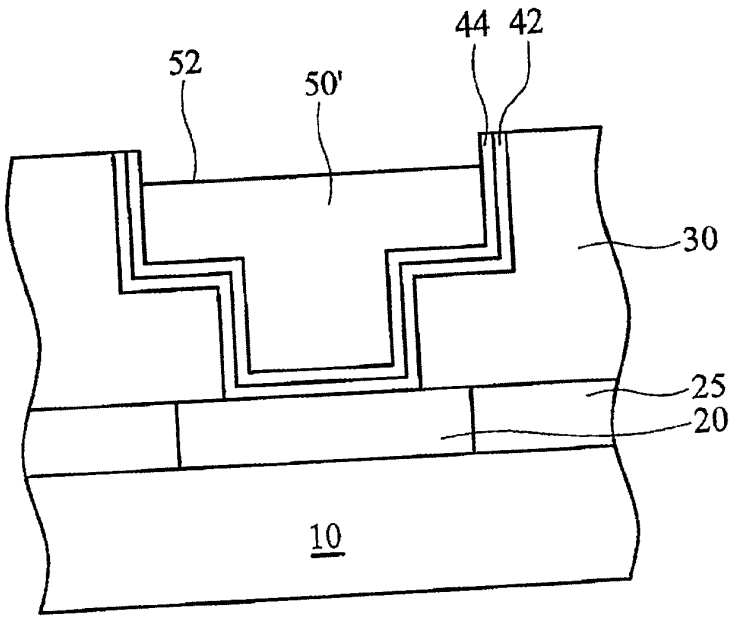


图 1F

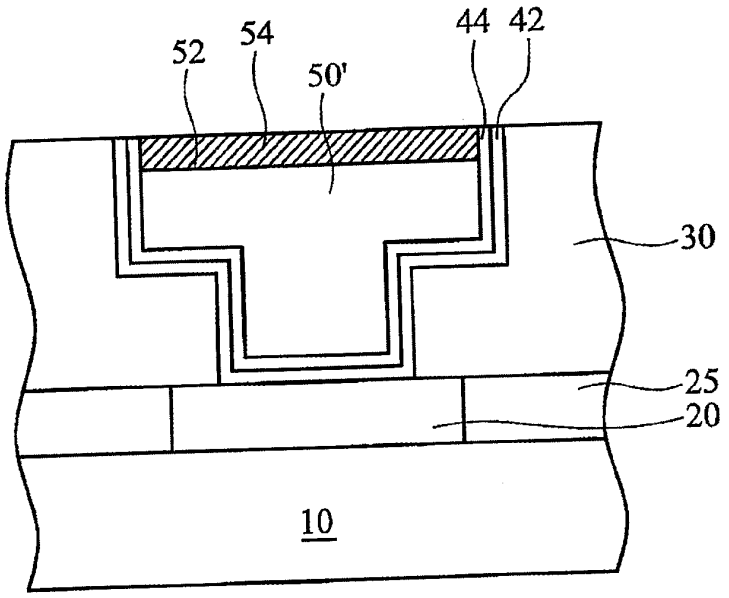


图 1G

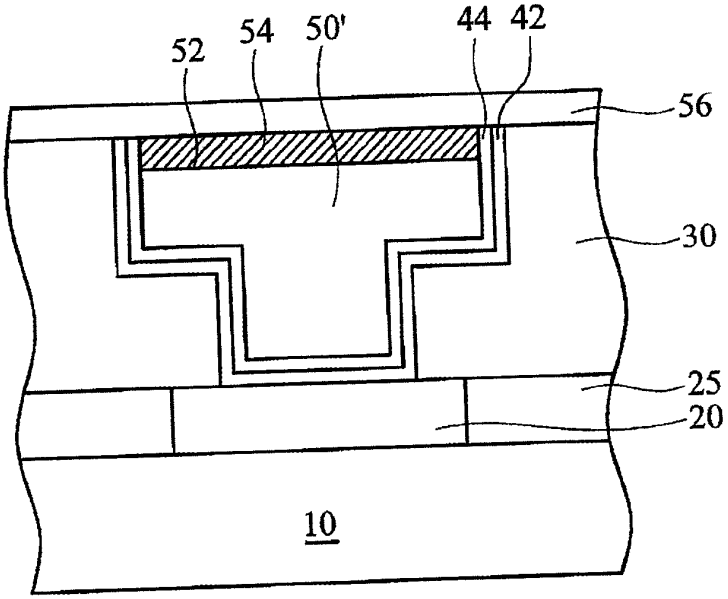


图 1H

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DESCRIPTION CN1921102

The present invention provides a copper interconnect structure as an interconnect. The interconnect structure described above has a copper recess that is located in a damascene structure filled with copper in the via/trench located in the dielectric layer. In addition, the interconnect structure described above may also have a metal capping layer and fill in the copper recess. Since the interconnect structure of the present invention includes copper recesses, the metal cap layer formed on the copper recesses in a selective growth manner can be well controlled.

Interconnect structure and its manufacturing method, semiconductor device

Technical field

The present invention relates to a method of manufacturing a copper interconnect structure, and more particularly to forming a copper recess in a damascene structure.

Background technique

Chip manufacturers continue to try to improve the process to achieve higher chip operating speeds. In the same time that the semiconductor process technology is also developed, the RC delay effect of the multilayer interconnect blocks the chip operation rate. The increase in multilayer interconnect resistance and capacitance between multilayer interconnections creates a resistive/capacitive time delay effect. Due to the low resistance of copper, copper is the best choice among multilayer interconnect materials.

In the known copper interconnect process, a dielectric stop layer such as a nitride layer is formed after chemical mechanical polishing (CMP) of copper. The poor interface between copper and the stop layer is a major obstacle to component reliability. So metal coatings such as tungsten (W), cobalt (Co), cobalt phosphotungstenide (CoWP) or cobalt tungsten boride (CoWB) are provided to improve the interface between copper and the stop layer. As such, the above-described metal capping layer is usually formed in a selective growth manner, but such a forming manner is difficult to control and causes the metal capping layer to grow laterally. Leakage due to lateral growth of the metal cap is a significant problem.

Summary of the Invention

In view of this, the main object of the present invention is to provide a method of manufacturing a copper interconnect structure that forms copper recesses in a damascene structure to improve the above-mentioned problems of the known technology.

The present invention provides an interconnect structure including:

A damascene structure, including a dielectric layer, and vias and/or trenches in the dielectric layer;

a conductor filled in the via hole and/or the trench, wherein a top surface of the conductor is lower than a top surface of the dielectric layer; and

Cobalt-containing coating on the conductor.

According to the interconnect structure described above, the distance between the top surface of the conductor and the top surface of the dielectric layer is 20 to 200 .

According to the interconnect structure, the top surface of the cobalt-containing capping layer on the conductor is substantially coplanar with the top surface of the dielectric layer.

According to the interconnect structure, wherein the cobalt-containing cap layer includes cobalt, cobalt tungsten, cobalt phosphotungstate, or cobalt tungsten borocarbide.

According to the interconnect structure, wherein the conductor comprises copper or a copper alloy.

According to the interconnect structure, an etch stop layer is further included on the cobalt-containing cap layer and the dielectric layer.

The invention also provides a method for manufacturing an interconnect structure, comprising:

Forming a damascene structure in the dielectric layer;

Filling the conductive material in the damascene structure to form a conductor;

Dent the surface of the conductor below the top surface of the dielectric layer; and

A cobalt-containing cap layer is formed on the recessed conductor.

According to the manufacturing method of the interconnect structure described above, the recess process of the conductor is a chemical mechanical polishing process.

According to the manufacturing method of the interconnect structure described above, the chemical mechanical polishing process is performed using hydrogen peroxide, nitric acid, hypochlorous acid, chromic acid, ammonia or ammonium salt as an oxidant, and slurry as an abrasive.

According to the method for manufacturing an interconnect structure, the method further includes:

Before filling in the conductive material, a conductive barrier layer and/or a seed layer are formed on the damascene structure;

Performing a chemical mechanical polishing process such that the surface of the conductor is substantially

coplanar with the top surface of the conductive barrier layer and/or the seed layer on the dielectric layer; and

Before the surface of the conductor is recessed, the conductive barrier layer and/or the seed layer on the dielectric layer are removed.

According to the method of fabricating the interconnect structure, wherein the cobalt-containing capping layer is formed on the recessed conductor, and the cobalt-containing capping layer does not extend to the top surface of the dielectric layer.

According to the method for fabricating the interconnect structure, wherein the cobalt-containing cap layer includes cobalt, cobalt tungsten, cobalt tungstotungsten, or cobalt tungsten boride.

According to the manufacturing method of the interconnect structure described above, the cobalt-containing capping layer is formed in a selective growth manner.

According to the manufacturing method of the interconnect structure described above, before the cobalt-containing cap layer is formed, a cleaning process is performed to recess the conductor.

According to the manufacturing method of the interconnection structure described above, wherein the cleaning process is performed in an acid-containing environment, the acid includes nitric acid, hypochlorous acid or chromic acid.

According to the above described method of fabricating an interconnect structure, wherein the conductor includes copper or a copper alloy.

According to the method of fabricating the interconnect structure, an etching stop layer is further formed to cover the cobalt-containing cap layer and the dielectric layer.

An embodiment of the present invention provides a method for manufacturing an interconnect structure, including: a damascene structure and a copper conductor, wherein the copper conductor is located in the above-mentioned mosaic structure. The damascene structure described above includes vias and/or trenches in the dielectric layer. The top surface of the conductor is lower than the top surface of the dielectric layer; and the

conductor recess is formed.

In addition, an embodiment of the present invention provides another interconnect structure. The interconnect structure includes a conductor recess in the damascene structure; and a conductive cover layer on the conductor recess, and the conductive cover layer does not extend to the top surface of the dielectric layer.

An embodiment of the present invention further provides a method for manufacturing an interconnect structure, including: forming a via hole/trench in a dielectric layer. A copper conductor is filled in the vias/trenches and substantially exceeds the surface of the dielectric layer. Thereafter, a copper removal process is performed so that the top surface of the conductor is lower than the top surface of the dielectric layer to form a copper recess.

Since the interconnect structure includes copper recesses, the metal cap layer formed on the copper recesses in a selective growth manner can be well controlled. The above-mentioned metal cap layer does not grow in the horizontal direction, resulting in the occurrence of a short-circuit or leakage problem.

Description of the drawings

FIGS. 1A-1H are cross-sectional views illustrating a method of fabricating an interconnect structure according to an embodiment of the present invention.

Among them, the reference numerals are as follows:

10	Substrate
20	Metal interconnect
25	Insulation
30	Dielectric layer

32 Via hole

34 Groove area

42 Conductive barrier

44 Seed layer

50、50'conductor

52 陷

54 Overlay

56 Etch stop layer

60 Dual damascene structure

detailed description

The interconnect structure and its manufacturing method according to the preferred embodiment of the present invention will be described in more detail using the process cross-sectional diagram below. In the various embodiments of the present invention, the same symbols denote the same elements.

As shown in FIG. 1A, a semiconductor substrate 10 is provided. As shown in Fig. 1A, the metal interconnect 20 is patterned inside the insulating layer 25 such as silicon oxide. In addition, the dielectric layer 30 is deposited, and the dielectric layer 30 is patterned to have the via hole portions 32 and the trench portions 34, thereby forming a dual damascene structure 60 including the via hole portions 32 and the trench portions 34. Although the dual damascene structure has been shown in FIGS. 1A to 1H, it is not limited to this dual damascene structure, and other types of interconnect patterns are also metallized using this typical technique.

As shown in FIG. 1B, a conductive barrier layer 42 is deposited on the top surface of the dielectric layer 30 and on the surfaces of the via holes 32 and the trenches 34. The conductive barrier layer 42 preferably includes tantalum (Ta) or tantalum nitride. (TaN). Next, as shown in FIG. 1B, a seed layer 44 such as a copper seed layer is compliantly deposited on the conductive barrier layer 42.

As shown in Fig. 1C, a conductor 50 such as copper or a copper alloy is filled in the via hole portion 32 and the groove portion 34 and over both surfaces by a plating process such as electroless plating or plating. As a result, the copper conductor 50 is electrically connected to the underlying metal interconnect 20 via the conductive barrier layer 42 .

Next, as shown in FIG. 1D, a chemical mechanical polishing process is performed to remove a portion of the copper conductor 50 and planarize its top surface so that the remaining copper conductor 50 ′ is substantially common with the conductive barrier layer 42 on the dielectric layer 30. Plane (or seed layer 44, if only seed layer 44 is present). After that, as shown in FIG. 1E, the seed layer 44 and the conductive barrier layer 42 on the dielectric layer 30 are removed by etching or other chemical mechanical polishing process. As such, the top surface of the remaining copper conductor 50' will be slightly higher than the top surface of the dielectric layer 30. FIG.

As shown in Fig. 1F, the recess 52 of the copper conductor 50' is formed to a depth of 20 to 200 Å. Copper recess 52 may be formed by a chemical mechanical polishing process. The chemical mechanical polishing process preferably uses hydrogen peroxide (H2O2), nitric acid, hypochlorous acid, chromic acid, ammonia, or ammonium salt as an oxidizing agent. And with a slurry such as alumina (Al2O3) as the abrasive; and deionized water (Deionized Water, DI water) added with benzotriazole (BTA).

The recess 52 of the conductor may also be formed by a cleaning process after the conductive barrier layer 42 on the dielectric layer 30 is removed. The cleaning process is performed in an acid-containing environment, wherein the above-mentioned acid includes nitric acid, hypochlorous acid, chromic acid, or the like.

Still alternatively, as shown in FIG. 1G, a conductive overlay 54 is formed to fill the recess 52 of the conductor. Typically, the conductive cover layer 54 is formed in a selective growth manner so that the conductive material is formed only on the surface of the copper conductor 50' and its recesses. In a preferred embodiment, the top surface of conductive overlay 54 is substantially coplanar with the top surface of dielectric layer 30 (both having the same surface). Preferably, the top surface of the conductive overlay 54 does not exceed the top surface of the dielectric layer 30 . The material of the conductive cap 54 may be any suitable conductive material such as a

tungsten layer formed by chemical vapor deposition (CVD). The preferred conductive overlay 54 is a cobalt containing overlay. The cobalt-containing cap layer may be cobalt (Co), cobalt tungsten (CoW), cobalt tungstophosphor (CoWP), or cobalt borocarbide (CoWB). After removing the conductive barrier layer 42 on the dielectric layer 30 and no copper cleaning recesses 52 are formed by a cleaning process or an additional chemical mechanical polishing process, the copper recesses 52 may be pre-capped via a pre-cap formation process. Clean procss). The pre-cleaning process prior to the formation of the cover layer can be performed in an acid-containing environment, wherein the above-mentioned acid includes nitric acid, hypochlorous acid, chromic acid or the like.

Since the copper wiring structure includes copper recesses, the conductive coating formed on the copper recesses in a selective growth manner can be well controlled. Conductive coatings do not grow in the horizontal direction and cause short circuit or leakage problems. As shown in FIG. 1H, in a preferred embodiment, an etch stop layer 56 may be formed to cover the conductive cap layer 54 and the dielectric layer 30. The cobalt-containing cap layer 54 also improves the interface between the copper conductor 50' and the etch stop layer 56 thereon.

Although the present invention has been disclosed in the preferred embodiments as above, it is not intended to limit the present invention. Any person skilled in the art can make some changes and modifications without departing from the spirit and scope of the present invention. Therefore, the present invention The scope of protection is subject to the definition in the appended claims.

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CLAIMS CN1921102

1.
An interconnect structure including:

A damascene structure, including a dielectric layer, and vias and/or trenches in the dielectric layer;

a conductor filled in the via hole and/or the trench, wherein a top surface of the conductor is lower than a top surface of the dielectric layer; and

Cobalt-containing coating on the conductor.

2.
The interconnect structure of claim 1, wherein a distance between the top surface of the conductor and the top surface of the dielectric layer is 20 to 200.

3.
The interconnect structure of claim 1, wherein a top surface of the cobalt-containing capping layer on the conductor is substantially coplanar with the top surface of the dielectric layer.

4.

The interconnect structure of claim 3, wherein the cobalt-containing cap layer includes cobalt, cobalt tungsten, cobalt phosphotungsten, or cobalt tungsten boride.

5.
The interconnect structure of claim 1, wherein the conductor comprises copper or a copper alloy.

6.
The interconnect structure of claim 1 further comprising an etch stop layer on the cobalt containing layer and the dielectric layer.

7.
A method for manufacturing an interconnect structure includes:

Forming a damascene structure in the dielectric layer;

Filling the conductive material in the damascene structure to form a conductor;

Dent the surface of the conductor below the top surface of the dielectric layer; and

A cobalt-containing cap layer is formed on the recessed conductor.

8.
The method for fabricating an interconnect structure according to claim 7, wherein the recessing process of the conductor is a chemical mechanical polishing process.

9.
The method for manufacturing an interconnect structure according to claim 8, wherein the chemical mechanical polishing process uses hydrogen peroxide, nitric acid, hypochlorous acid, chromic acid, ammonia or ammonium salt as an oxidant, and slurry as an abrasive agent. .

10.

The method of manufacturing an interconnect structure according to claim 7, further comprising:

Before filling in the conductive material, a conductive barrier layer and/or a seed layer are formed on the damascene structure;

Performing a chemical mechanical polishing process such that the surface of the conductor is substantially coplanar with the top surface of the conductive barrier layer and/or the seed layer on the dielectric layer; and

Before the surface of the conductor is recessed, the conductive barrier layer and/or the seed layer on the dielectric layer are removed.

11.
The method of fabricating an interconnect structure of claim 7, wherein the cobalt-containing capping layer is formed on the recessed conductor, and the cobalt-containing capping layer does not extend to the top surface of the dielectric layer.

12.
The method of fabricating an interconnect structure according to claim 7, wherein the cobalt-containing overcoat layer comprises cobalt, cobalt tungsten, cobalt phosphotungstate, or cobalt tungsten boronitride.

13.
The method of fabricating an interconnect structure according to claim 7, wherein the cobalt-containing cap layer is formed in a selective growth manner.

14.
The method of fabricating an interconnect structure according to claim 7, wherein a cleaning process is performed to recess the conductor before forming the cobalt-containing cap layer.

15.
The method of manufacturing an interconnect structure according to claim 14, wherein the cleaning process is performed in an acid-containing environment, wherein the acid comprises nitric acid, hypochlorous acid or chromic acid.

16.

The method of fabricating an interconnect structure according to claim 7, wherein the conductor comprises copper or a copper alloy.

17.

The method of fabricating an interconnect structure of claim 7, further comprising forming an etch stop layer over the cobalt-containing cap layer and the dielectric layer.

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最終頁に続く

(54)【発明の名称】　集積回路装置の製造方法

1

(57)【特許請求の範囲】
【請求項１】基板上に形成された絶縁膜に開口を形成する工程と、
該開口を含む該基板の上に銅の堆積層を堆積する工程と、
研磨により、該絶縁膜の上に堆積された銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように研磨除去する工程と、
該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、
該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する程とを含んでなることを特徴とする集積回路装置の製造方法。

2

【請求項２】回路基板上に形成された絶縁膜に開口を形成する工程と、
該開口を含む該回路基板の上にバリア材料の堆積層を堆積する工程と、
該バリア材料の堆積層の上に銅の堆積層を堆積する工程と、
研磨に依り、該絶縁膜の上に堆積されたバリア材料の堆積層と銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように研磨除去する工程と、
該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、
該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程とを含んでなることを特徴とする集積回路装置の

製造方法。

【請求項３】沃化カリウムまたは塩化カリウムの水溶液と研磨剤を用いてバフ研磨することによって、絶縁膜の上に堆積された銅の堆積層を除去するとともに、開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去することを特徴とする請求項１或いは請求項２記載の集積回路の製造方法。

【請求項４】絶縁膜に形成された開口が、溝状開口であり、該溝状開口中に堆積した銅によって配線層を形成することを特徴とする請求項１乃至請求項３の何れか１記載の集積回路装置の製造方法。

【請求項５】絶縁膜に形成された開口が、基板に達するコンタクトホールであり、該コンタクトホール中に堆積した銅によって該回路基板に対するコンタクトを形成することを特徴とする請求項１乃至請求項３の何れか１記載の集積回路装置の製造方法。

【請求項６】バリア層の材料がＴｉＮであることを特徴とする請求項１乃至請求項５の何れか１記載の集積回路装置の製造方法。

【請求項７】バリヤ層の材料が酸素を含まない絶縁材料であることを特徴とする請求項１乃至請求項４の何れか１記載の集積回路装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、銅を用いた配線層またはコンタクトをもつ集積回路装置の製造方法に関する。近年、ＡｌＣｕ配線層を用いた集積回路装置の高集積化が進むに伴い、コンタクト面積の縮小化によるコンタクト抵抗の増大、および、配線サイズの微細化による抵抗の増大やエレクトロマイグレーション耐性の劣化が問題になっている。このため、エレクトロマイグレーション耐性が高く、かつ、低抵抗の材料を用いて微細配線や微細なコンタクトを形成する技術が必要になっている。このような配線用金属材料として銅が注目されている。

【０００２】

【従来の技術】従来、銅で配線層を形成する方法としては、スパッタ法あるいは蒸着法により基板全面に銅の薄膜を堆積した後に、化学反応を利用したＲＩＥによって所望の配線形成に成形する方法が試みられていた。

【０００３】

【発明が解決しようとする課題】ところが、通常の方法では、エッチング工程で生じるハロゲン化銅の蒸気圧が極めて低いためエッチング速度が遅く、配線のパターニング後の形状が鮮明でない等の欠点があった。

【０００４】また、銅の配線層を形成した後に銅の酸化を防止するための被覆膜を形成すると、被覆膜を形成することによって配線層の凹凸が大きくなり、表面を平坦化する上で障害となっていた。本発明は、上記の問題に対応するため、エッチングにより銅の化合物を気化することなく、バリア層を含めた銅の配線層あるいはコンタクトの平坦化を実現する手段を提供することを目的とする。

【０００５】

【問題点を解決するための手段】本発明に依る集積回路装置の製造方法に於いては、

（１）

基板上に形成された絶縁膜に開口を形成する工程と、該開口を含む該基板の上に銅の堆積層を堆積する工程と、研磨により、該絶縁膜の上に堆積された銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように研磨除去する工程と、該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程とを含んでなることを特徴とするか、又は、

【０００６】（２）

回路基板上に形成された絶縁膜に開口を形成する工程と、該開口を含む該回路基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層の上に銅の堆積層を堆積する工程と、研磨に依り、該絶縁膜の上に堆積されたバリア材料の堆積層と銅の堆積層を除去するとともに、該開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように研磨除去する工程と、該開口中の銅を含む基板の上にバリア材料の堆積層を堆積する工程と、該バリア材料の堆積層を平坦化研磨することによって該開口中の銅の上面にセルフアラインでバリア層を形成する工程とを含んでなることを特徴とするか、又は、

【０００７】（３）

前記（１）或いは（２）に於いて、沃化カリウムまたは塩化カリウムの水溶液と研磨剤を用いてバフ研磨することによって、絶縁膜の上に堆積された銅の堆積層を除去するとともに、開口中に堆積された銅を表面が該絶縁膜の表面より低い段差を有するように除去することを特徴とするか、又は

【０００８】（４）

前記（１）乃至（３）の何れか１に於いて、絶縁膜に形成された開口が、溝状開口であり、該溝状開口中に堆積した銅によって配線層を形成することを特徴とするか、又は、

（５）

前記（１）乃至（３）の何れか１に於いて、絶縁膜に形成された開口が、基板に達するコンタクトホールであり、該コンタクトホール中に堆積した銅によって該回路基板に対するコンタクトを形成することを特徴とするか、又は、

【０００９】（６）

前記（１）乃至（５）の何れか１に於いて、バリア層の材料がＴｉＮであることを特徴とするか、又は、

（７）
前記（１）乃至（４）の何れか１に於いて、バリヤ層の材料が酸素を含まない絶縁材料であることを特徴とする。

【００１０】
【作用】図１は、本発明によって製造された集積回路装置の構成説明図である。この図において、１は基板、２は絶縁膜、３は溝状の開口、４，はバリア層、５，は銅の配線層、６，はバリア層である。

【００１１】この構成説明図によって、配線層の形成方法に特徴を有する集積回路装置の製造方法の概要を説明する。

【００１２】基板１の上に形成されたＳｉＯ２等の絶縁膜２に溝状の開口３をフォトリソグラフィー技術によって形成し、この溝状の開口３の中を含む絶縁膜２の全面にＴｉＮ等のバリア材料をスパッタ法等によって堆積してバリア材料堆積層を形成し、このバリア材料堆積層の上に、銅をＣＶＤ法等によって堆積して、溝状の開口３を完全に埋め込む銅の堆積層を形成する。

【００１３】この銅の堆積層を、沃化カリウム（ＫＩ）＋沃素（Ｉ２）水溶液（５％）と研磨剤を用いてバフ研磨し、絶縁膜２上面に形成されている銅の堆積層とバリア材料堆積層を除去して、バリア層４，によって底面と側面の三方を囲まれ、絶縁膜２の上面より低い銅の配線層５，を形成する。

【００１４】そして、絶縁膜２の上面より低い銅の配線層５，の上を含む絶縁膜２の全面に再びバリア材料堆積層を形成し、平坦化ポリッシュを行って、銅の配線層５，の上面のみにバリア層６，を残して、バリア層４，とバリア層６，によって四方を囲まれ、絶縁膜２の上面と一致する上面を有する銅の配線層５，を形成する。

【００１５】本発明によると、従来のように、銅層をエッチングして配線層を残す工程を用いることなく銅の配線層を形成することができ、さらに銅の配線層の周りをバリア層によって覆うことができるため、銅の酸化、拡散が防止され、エレクトロマイグレーションに強い低抵抗の平坦化配線層を形成することができる。

【００１６】
【実施例】以下、本発明の集積回路装置の製造方法の実施例を説明する。

（第１実施例）図２、図３は、第１実施例の集積回路装置の製造方法の工程説明図で、（Ａ）～（Ｅ）は各工程を示している。この図において、１は基板、２は絶縁膜、３は溝状の開口、４はバリア材料堆積層、４，はバリア層、５は銅の堆積層、５，は銅の配線層、６はバリア材料堆積層、６，はバリア層である。

【００１７】この工程説明図によって、配線層の形成方法に特徴を有する集積回路装置の製造方法を説明する。

【００１８】第１工程（図２（Ａ）参照）
基板１の上に形成されたＳｉＯ２等の絶縁膜２に、銅の配線層を形成するための溝状の開口３をフォトリソグラフィー技術によって形成する。この基板１は、集積回路装置の半導体基板、配線層を担持するための絶縁基板、多層配線層の層間絶縁体膜等であり得る。

【００１９】第２工程（図２（Ｂ）参照）
溝状の開口３の中を含む絶縁膜２の全面に、ＴｉＮをスパッタ法によって堆積してバリア材料堆積層４を形成する。このバリア材料堆積層４の上に、銅をＣＶＤ法によって堆積して、溝状の開口３を完全に埋め込む銅の堆積層５を形成する。このＣＶＤ法による銅の堆積層（ＣＶＤ－Ｃｕ）５のソースガスとして、Ｃｕ（ＨＦＡ）ｔｍｖｓ（Ｃｕ（ｌ）－ｈｅｘａｆｌｕｏｒｏａｃｅｔｙｌａｃｅｔｏｎａｔｏ－ｔｒｉｍｅｔｈｙｌｖｉｎｙｌｓｉｌｙｌ）を用い、基板温度２００℃、成長圧力１Ｔｏｒｒで成膜する。

【００２０】第３工程（図２（Ｃ）参照）
この銅の堆積層５を、沃化カリウム（ＫＩ）＋沃素（Ｉ２）水溶液（５％）および研磨剤（商品名Ｂａｌｋａｌｏｘ　０．１ＣＲ）を用いてバフ研磨し、絶縁膜２上面に形成されている銅の堆積層５とＴｉＮからなるバリア材料堆積層４を除去して、バリア層４，によって底面と側面の三方を囲まれ、絶縁膜２の上面より低い銅の配線層５，を形成する。

【００２１】第４工程（図３（Ｄ）参照）
絶縁膜２の上面より低い銅の配線層５，の上を含む絶縁膜２の全面に再びＴｉＮをスパッタ法により堆積して、バリア材料堆積層６を形成する。

【００２２】第５工程（図３（Ｅ）参照）
このバリア材料堆積層６を平坦化ポリッシュして、銅の配線層５，の上面のみにバリア層６，を残して、バリア層４，とバリア層６，によって四方を完全に囲まれ、絶縁膜２の上面と一致する平面を有する銅の配線層５，を形成する。この平坦な絶縁膜２と銅の配線層５，の上に、他の配線層を引き続いて形成することができる。

【００２３】上記の実施例においては、バリア材料としてＴｉＮを用いた例を説明したが、ＴｉＮに代えて銅の配線層５，の周りにＳｉＮ膜等の酸素を含まない絶縁材料を形成した場合は、銅の配線層５，が酸化膜と直接接触する部分がなくなり、銅の配線層５，が酸化されるのを防止することができ、また逆に銅の配線層５，の銅が絶縁膜２に拡散して特性を劣化させることを防止することができる。

【００２４】（第２実施例）図４、図５は、第２実施例の集積回路装置の製造方法の工程説明図で、（Ａ）～（Ｅ）は各工程を示している。この図において、１１は回路基板、１２は絶縁膜、１３はコンタクトホール、１４はバリア材料堆積層、１４，はバリア層、１５は銅の堆積層、１５，は銅のコンタクト、１６はバリア材料堆積層、１６，はバリア層である。

【００２５】この工程説明図によって、コンタクトの形

成方法に特徴を有する集積回路装置の製造方法を説明する。この実施例のコンタクトの形成工程は第１実施例の配線層の形成工程とほぼ同様であるから、詳細な説明を省略する。

【００２６】第１工程（図４（Ａ）参照）

回路基板１１の上に形成された絶縁膜１２に、銅のコンタクトを形成するためのコンタクトホール１３をフォトリソグラフィー技術によって形成する。

【００２７】第２工程（図４（Ｂ）参照）

コンタクトホール１３の中を含む絶縁膜１２の全面に、スパッタ法によってバリア材料堆積層１４を形成する。このバリア材料堆積層１４の上に、銅をＣＶＤ法によって堆積して、コンタクトホール１３を完全に埋め込む銅の堆積層１５を形成する。

【００２８】第３工程（図４（Ｃ）参照）

この銅の堆積層１５を、沃化カリウム（ＫＩ）＋沃素（I_2）水溶液（５％）と研磨剤を用いてバフ研磨し、絶縁膜１２の上面に形成されている銅の堆積層１５とバリア材料堆積層１４を除去して、周囲をバリア層14_1によって囲まれ、絶縁膜１２の上面より低い銅のコンタクト15_1を形成する。

【００２９】第４工程（図５（Ｄ）参照）

絶縁膜１２の上面より低い銅のコンタクト15_1の上を含む絶縁膜１２の全面に再びバリア材料堆積層１６を形成する。

【００３０】第５工程（図５（Ｅ）参照）

このバリア材料堆積層１６を平坦化ポリッシュして、銅のコンタクト15_1の上面のみにバリア層16_1を残して、バリア層14_1とバリア層16_1によって全面を囲まれ、絶縁膜１２の上面と一致する平面を有する銅のコンタクト15_1を形成する。

【００３１】この実施例においては、バリア材料としてＴｉＮ等の導電性を有するバリアメタルあるいは合金を用い、平坦な絶縁膜１２と銅のコンタクト15_1の上に、他の配線層を引き続いて形成し、導電性のバリア層16_1を介して銅のコンタクト15_1と他の配線層の間を電気的に接続することができる。

【００３２】上記の各実施例においては、銅の配線層５，あるいはコンタクトの周りをバリア層で覆っているが、絶縁膜の材料がバリア材料と同等の性質を有する場合は、銅の配線層５，あるいはコンタクトの上部のみにバリア層を形成することによって、本発明の目的を達成することができる。

【００３３】

【発明の効果】以上説明したように、本発明によると、銅層をエッチングして配線層を残す従来の工程を用いることなく、銅の配線層を形成することができ、さらに銅の配線層の周りは全てバリア材料の層で覆われるため、銅の酸化、拡散が防止され、エレクトロマイグレーションに強い低抵抗の平坦化配線層を形成することができ、集積回路装置の高集積化に寄与するところが大きい。

【図面の簡単な説明】

【図１】本発明によって製造された集積回路装置の構成説明図である。

【図２】第１実施例の集積回路装置の製造方法の工程説明図（１）で、（Ａ）～（Ｃ）は各工程を示している。

【図３】第１実施例の集積回路装置の製造方法の工程説明図（２）で、（Ｄ），（Ｅ）は各工程を示している。

【図４】第２実施例の集積回路装置の製造方法の工程説明図（１）で、（Ａ）～（Ｃ）は各工程を示している。

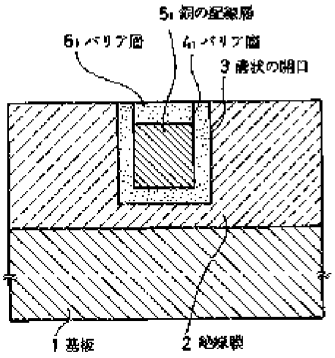
【図５】第２実施例の集積回路装置の製造方法の工程説明図（２）で、（Ｄ），（Ｅ）は各工程を示している。

【符号の説明】

１　基板
２　絶縁膜
３　溝状の開口
４　バリア材料堆積層
4_1　バリア層
５　銅の堆積層
5_1　銅の配線層
６　バリア材料堆積層
6_1　バリア層
１１　回路基板
１２　絶縁膜
１３　コンタクトホール
１４　バリア材料堆積層
14_1　バリア層
１５　銅の堆積層
15_1　銅のコンタクト
１６　バリア材料堆積層
16_1　バリア層

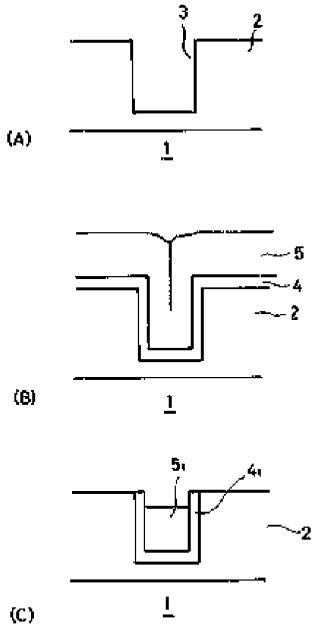
【図１】

本発明によって製造された集積回路装置の構成説明図



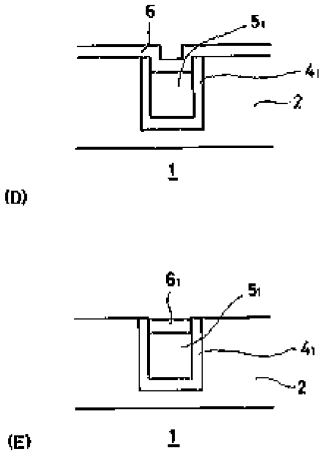
【図２】

第１実施例の集積回路装置の製造方法の工程説明図（１）



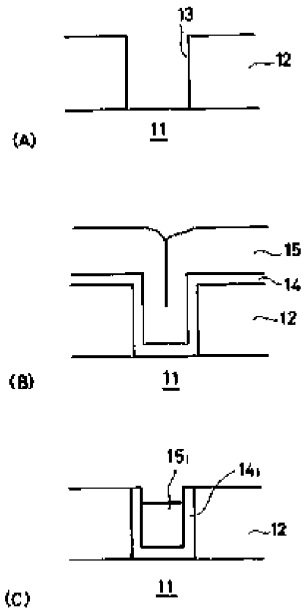
【図３】

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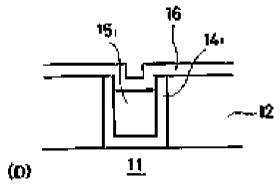
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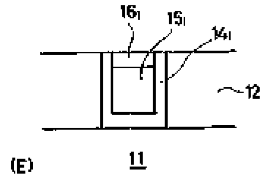
第２実施例の集積回路装置の製造方法の工程説明図（１）



【図５】

第２実施例の集積回路装置の製造方法の工程説明図（２





フロントページの続き

(58)調査した分野(Int.Cl.', ＤＢ名)

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H01L 21/3205 - 21/3213
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CLAIMS

(57)[Claim(s)]

[Claim 1]While a process of forming an opening in an insulator layer formed on a substrate, a process of depositing copper sedimentary layers on the substrate containing the opening, and polish remove sedimentary layers of copper deposited on the insulator layer, A process of carrying out polish removal of the copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer, A manufacturing method of an integrated circuit device which contains, so that a barrier layer is formed in a top surface of copper in the opening by a self aryne by carrying out flattening polish of a process of depositing sedimentary layers of a barrier material on a substrate containing copper in the opening, and the sedimentary layers of the barrier material, and is characterized by things.

[Claim 2]A manufacturing method of an integrated circuit device characterized by comprising the following.
A process of forming an opening in an insulator layer formed on a circuit board.
A process of depositing sedimentary layers of a barrier material on the circuit board containing the opening.
A process of depositing copper sedimentary layers on sedimentary layers of the barrier material.
A process of carrying out polish removal of the copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer while removing sedimentary layers of a barrier material and copper sedimentary layers which depended on polish and were deposited on the insulator layer.
A process of depositing sedimentary layers of a barrier material on a substrate containing copper in the opening.
A process of forming a barrier layer in a top surface of copper in the opening by a self aryne by carrying out flattening polish of the sedimentary layers of the barrier material.

[Claim 3]While removing sedimentary layers of copper deposited on an insulator layer by carrying out buffing using an aqueous solution and abrasive soap of a potassium iodide or potassium chloride, Claim 1 removing copper deposited into an opening so that it may have a level difference whose surface is lower than the surface of the insulator layer, or a manufacturing method of the integrated circuit according to claim 2.

[Claim 4]A manufacturing method of an integrated circuit device of any 1 description of Claim 3 to Claim 1 with which an opening formed in an insulator layer is a grooved opening, and is characterized by forming a wiring layer with copper deposited into the grooved opening.

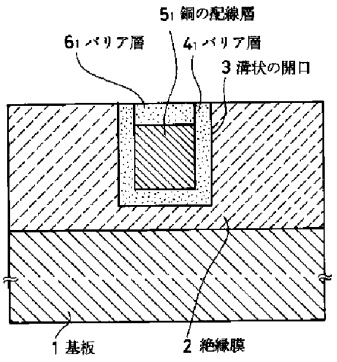
[Claim 5]A manufacturing method of an integrated circuit device of any 1 description of Claim 3 to Claim 1 which an opening formed in an insulator layer is a contact hole which reaches a substrate, and is characterized by forming contact to the circuit board with copper deposited all over the contact hole.

[Claim 6]A manufacturing method of an integrated circuit device of any 1 description of Claim 5 to Claim 1, wherein material of a barrier layer is TiN.

[Claim 7]A manufacturing method of an integrated circuit device of any 1 description of Claim 4 to Claim 1, wherein material of a barrier layer is an insulating material which does not contain oxygen.

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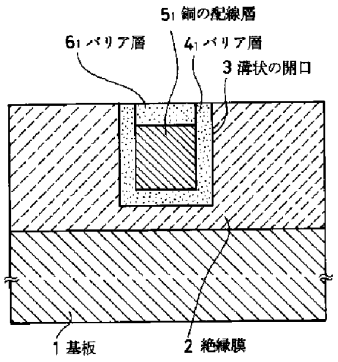
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]The present invention relates to the manufacturing method of an integrated circuit device with the wiring layer or contact which used copper. In recent years, high integration of the integrated circuit device using an Al wiring layer follows on proceeding, and increase of the contact resistance by the reduction of a contact area and increase of resistance by micronization of wiring size, and electromigration resistance degradation have been a problem. For this reason, electromigration resistance is high and the technology which forms fine wiring and minute contact using the material of low resistance is needed. Copper attracts attention as such a metallic material for wiring.
[0002]
[Description of the Prior Art]Conventionally, as a method of forming a wiring layer with copper, after depositing a copper thin film on an entire substrate with a sputtering method or a vapor deposition method, the method of using a chemical reaction and molding into desired wiring formation by RIE was tried.
[0003]
[Problem to be solved by the invention]However, in the usual method, there was a defect whose form after patterning of wiring an etch rate is slow since the steam pressure of copper halide occurred by an etching step is very low, and is not clear.
[0004]It had become an obstacle, when the coating membrane for preventing copper oxidation was formed after forming a copper wiring layer, unevenness of a wiring layer enlarged and the surface was flattened by forming coating membrane. An object of the present invention is to provide a means to realize a copper wiring layer or flattening of contact including a barrier layer, without evaporating a copper compound by etching, in order to correspond to the above-mentioned problem.
[0005]
[Means for Solving the Problem]In a manufacturing method (1) of an integrated circuit device which depends on the present invention,
While a process of forming an opening in an insulator layer formed on a substrate, a process of depositing copper sedimentary layers on the substrate containing the opening, and polish remove sedimentary layers of copper deposited on the insulator layer, A process of carrying out polish removal of the copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer, or [that a process of forming a barrier layer in a top surface of copper in the opening by a self aryne is included, and it is characterized by things by carrying out flattening polish of a process of depositing sedimentary layers of a barrier material on a substrate containing copper in the opening, and the sedimentary layers of the barrier material] -- or [0006](2)
A process of forming an opening in an insulator layer formed on a circuit board, and a process of depositing sedimentary layers of a barrier material on the circuit board containing the opening, While removing sedimentary layers of a process of depositing copper sedimentary layers on sedimentary layers of the barrier material, and a barrier material which depended on polish and was deposited on the insulator layer, and copper sedimentary layers, A process of carrying out polish removal of the copper deposited into the opening so that it may have a level difference whose surface is lower than the surface of the insulator layer, or [that a process of forming a barrier layer in a top surface of copper in the opening by a self aryne is included, and it is characterized by things by carrying out flattening polish of a process of depositing sedimentary layers of a barrier material on a substrate containing copper in the opening, and the sedimentary layers of the barrier material] -- or [0007](3)
While removing sedimentary layers of copper deposited on an insulator layer in the above (1) or (2) by carrying out buffing using an aqueous solution and abrasive soap of a potassium iodide or potassium chloride, or [that it is characterized by removing copper deposited into an opening so that it may have a level difference whose surface is lower than the surface of the insulator layer] -- or[0008](4) or [that it is characterized by forming a wiring layer with copper which an opening formed in an insulator layer is a grooved opening, and deposited into the grooved opening in any 1 of the (3) to the above (1)] -- or (5)
or [that an opening formed in an insulator layer in any 1 of the (3) to the above (1) is a contact hole which reaches a substrate, and it is characterized by forming contact to the circuit board with copper deposited all over the contact hole] -- or[0009](6) In any 1 of the (5) to the above (1), it is an insulating material which is characterized by material of a barrier layer being TiN or in which material of a barrier layer does not contain oxygen in any 1 of the (4) to (7) above (1). [0010]
[Function]Fig.1 is a composition explanatory view of the integrated circuit device manufactured by the present invention. As for a substrate, an insulator layer and the opening of a groove [2 / 3], and 4_1, in this figure, a copper wiring layer and 6_1 of a barrier layer and 5_1 are barrier layers 1.
[0011]In this composition explanatory view, the summary of the manufacturing method of the integrated circuit device which has the characteristics in the formation method of a wiring layer is described.
[0012]The grooved opening 3 is formed in the insulator layers 2, such as SiO_2 formed on the substrate 1, with photolithography technology, Barrier materials, such as TiN, are deposited by a sputtering method etc. all over the insulator layer 2 including the inside of this grooved opening 3, barrier material sedimentary layers are formed, copper is deposited with a CVD

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method etc. on these barrier material sedimentary layers, and the sedimentary layers of the copper which embeds the grooved opening 3 completely are formed.
[0013]Carry out buffing of the sedimentary layers of this copper using a potassium iodide (KI)+ iodine (I_2) aqueous solution (5%) and abrasive soap, and it removes the copper sedimentary layers and barrier material sedimentary layers which are formed in insulator layer 2 top surface, By barrier layer 4 $_1$, the three way type of a bottom surface and a side surface is surrounded, and wiring layer 5 $_1$ of copper lower than the top surface of the insulator layer 2 is formed.
[0014]And form barrier material sedimentary layers again all over the insulator layer 2 including the wiring layer 5 $_1$ top of copper lower than the top surface of the insulator layer 2, perform a flattening polish, and it leaves barrier layer 6 $_1$ only to the top surface of copper wiring layer 5 $_1$, The four quarters are surrounded by barrier layer 4 $_1$ and barrier layer 6 $_1$, and copper wiring layer 5 $_1$ which has a top surface of the insulator layer 2 and a top surface which corresponds is formed.
[0015]Since according to the present invention a copper wiring layer can be formed and the surroundings of a copper wiring layer can be further covered by a barrier layer, without using the process of etching a copper layer and leaving a wiring layer like before, Copper oxidation and diffusion are prevented and the flattening wiring layer of low resistance strong against electromigration can be formed.
[0016]
[Working example]Hereinafter, the Example of the manufacturing method of the integrated circuit device of the present invention is described.
(The 1st Example) Fig.2 and Fig.3 are the work flow illustrative drawings of the manufacturing method of the integrated circuit device of the 1st Example, and (A) - (E) shows each process. in this figure -- 1 -- barrier material sedimentary layers and 4 $_1$ are [barrier material sedimentary layers and 6 $_1$ of copper sedimentary layers and 5 $_1$] barrier layers a copper wiring layer and 6 a barrier layer and 5 a substrate, an insulator layer and the opening of a groove [2 / 3], and 4.
[0017]By this work flow illustrative drawing, the manufacturing method of the integrated circuit device which has the characteristics in the formation method of a wiring layer is described.
[0018]1st process (refer to Fig.2 (A))
The grooved opening 3 for forming a copper wiring layer in the insulator layers 2, such as SiO_2 formed on the substrate 1, is formed with photolithography technology. This substrate 1 may be an insulating substrate for supporting the semiconductor substrate of an integrated circuit device, and a wiring layer, a layer insulation body film of a multilayer interconnection layer, etc.
[0019]2nd process (refer to Fig.2 (B))
All over the insulator layer 2 including the inside of the grooved opening 3, TiN is deposited by a sputtering method and the barrier material sedimentary layers 4 are formed. On these barrier material sedimentary layers 4, copper is deposited with a CVD method, and the sedimentary layers 5 of the copper which embeds the grooved opening 3 completely are formed. As source gas of the sedimentary layers (CVD-Cu) 5 of copper by this CVD method, Membranes are formed by the substrate temperature of 200 degrees C, and growing pressure 1Torr using Cu(HFA) tmvs (Cu(1)-hexafluoroacetylacetonato-trimethylvinylsilyl).
[0020]3rd process (refer to Fig.2 (C))
Buffing of the sedimentary layers 5 of this copper is carried out using a potassium iodide (KI)+ iodine (I_2) aqueous solution (5%) and abrasive soap (trade name Balkalox 0.1CR), The copper sedimentary layers 5 and the barrier material sedimentary layers 4 which consists of TiN which are formed in insulator layer 2 top surface are removed, by barrier layer 4 $_1$, the three way type of a bottom surface and a side surface is surrounded, and wiring layer 5 $_1$ of copper lower than the top surface of the insulator layer 2 is formed.
[0021]4th process (refer to Fig.3 (D))
TiN is again deposited by a sputtering method all over the insulator layer 2 including the wiring layer 5 $_1$ top of copper lower than the top surface of the insulator layer 2, and the barrier material sedimentary layers 6 are formed.
[0022]5th process (refer to Fig.3 (E))
Carry out the flattening polish of these barrier material sedimentary layers 6, and it leaves barrier layer 6 $_1$ only to the top surface of copper wiring layer 5 $_1$, Barrier layer 4 $_1$ and barrier layer 6 $_1$ surround the four quarters completely, and it forms copper wiring layer 5 $_1$ which has a top surface of the insulator layer 2, and a plane which corresponds. On wiring layer 5 $_1$ of this flat insulator layer 2 and copper, other wiring layers can be formed succeedingly.
[0023]In the above-mentioned Example, although the example using TiN as a barrier material was described, When the insulating material which replaces with TiN and does not contain oxygen, such as an SiN film, in the surroundings of copper wiring layer 5 $_1$ is formed, The portion in which copper wiring layer 5 $_1$ carries out direct contact to an oxide film can be lost, and copper wiring layer 5 $_1$ can be prevented from oxidizing, and it can prevent copper of copper wiring layer 5 $_1$ diffusing to the insulator layer 2 conversely, and degrading the characteristic.
[0024](The 2nd Example) Fig.4 and Fig.5 are the work flow illustrative drawings of the manufacturing method of the integrated circuit device of the 2nd Example, and (A) - (E) shows each process. in this figure -- 11 -- a circuit board and 12 -- an insulator layer and 13 -- barrier material sedimentary layers and 14 $_1$ are [barrier material sedimentary layers and 16 $_1$ of copper sedimentary layers and 15 $_1$] barrier layers copper contact and 16 a barrier layer and 15 a contact hole and 14.
[0025]By this work flow illustrative drawing, the manufacturing method of the integrated circuit device which has the characteristics in the formation method of contact is described. Since the formation process of contact of this Example is the same as the formation process of the wiring layer of the 1st Example substantially, it omits a detailed description.
[0026]1st process (refer to Fig.4 (A))
The contact hole 13 for forming copper contact in the insulator layer 12 formed on the circuit board 11 is formed with photolithography technology.
[0027]2nd process (refer to Fig.4 (B))
All over the insulator layer 12 including the inside of the contact hole 13, the barrier material sedimentary layers 14 are formed by a sputtering method. On these barrier material sedimentary layers 14, copper is deposited with a CVD method, and the sedimentary layers 15 of the copper which embeds the contact hole 13 completely are formed.
[0028]3rd process (refer to Fig.4 (C))
Carry out buffing of the sedimentary layers 15 of this copper using a potassium iodide (KI)+ iodine (I_2) aqueous solution (5%) and abrasive soap, and it removes the copper sedimentary layers 15 and the barrier material sedimentary layers 14 which are formed in the top surface of the insulator layer 12, Barrier layer 14 $_1$ surrounds the circumference and it forms contact 15 $_1$ of copper lower than the top surface of the insulator layer 12.
[0029]4th process (refer to Fig.5 (D))
The barrier material sedimentary layers 16 are again formed all over the insulator layer 12 including the contact 15 $_1$ top of copper lower than the top surface of the insulator layer 12.
[0030]5th process (refer to Fig.5 (E))
Carry out the flattening polish of these barrier material sedimentary layers 16, and it leaves barrier layer 16 $_1$ only to the top surface of copper contact 15 $_1$, The whole surface is surrounded by barrier layer 14 $_1$ and barrier layer 16 $_1$, and copper contact 15 $_1$ which has a top surface of the insulator layer 12 and a plane which corresponds is formed.
[0031]In this Example, the barrier metal or alloy which has conductivity, such as TiN, is used as a barrier material, On contact 15 $_1$ of the flat insulator layer 12 and copper, other wiring layers can be formed succeedingly, and between other wiring layers can electrically be connected with copper contact 15 $_1$ via conductive barrier layer 16 $_1$.
[0032]In each of above-mentioned Examples, although the surroundings of copper wiring

layer 5 $_1$ or contact are covered by the barrier layer, When the material of an insulator layer has a property equivalent to a barrier material, the object of this invention can be attained by forming a barrier layer in the upper chisel of copper wiring layer 5 $_1$ or contact.
[0033]
[Effect of the Invention]Since a copper wiring layer can be formed and all the surroundings of a copper wiring layer are further covered in the layer of a barrier material, without using the conventional process of etching a copper layer and leaving a wiring layer according to the present invention as described above. The place which copper oxidation and diffusion are prevented, can form the flattening wiring layer of low resistance strong against electromigration, and contributes to high integration of an integrated circuit device is large.

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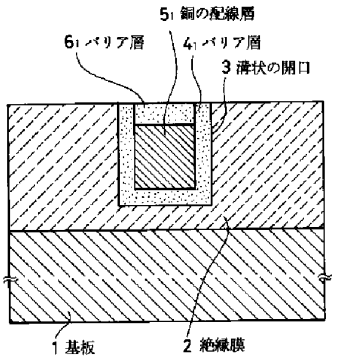
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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
A [FIG. 1] It is a composition explanatory view of the integrated circuit device manufactured by the present invention.
A [FIG. 2] By the work flow illustrative drawing (1) of the manufacturing method of the integrated circuit device of the 1st Example, (A) - (C) shows each process.
A [FIG. 3] By the work flow illustrative drawing (2) of the manufacturing method of the integrated circuit device of the 1st Example, (D) and (E) show each process.
A [FIG. 4] By the work flow illustrative drawing (1) of the manufacturing method of the integrated circuit device of the 2nd Example, (A) - (C) shows each process.
A [FIG. 5] By the work flow illustrative drawing (2) of the manufacturing method of the integrated circuit device of the 2nd Example, (D) and (E) show each process.
[Explanations of letters or numerals]
1 Substrate
2 Insulator layer
3 A grooved opening
4 Barrier material sedimentary layers
4 $_1$ barrier layer
5 Copper sedimentary layers
The wiring layer of 5 $_1$ copper
6 Barrier material sedimentary layers
6 $_1$ barrier layer
11 Circuit board
12 Insulator layer
13 Contact hole
14 Barrier material sedimentary layers
14 $_1$ barrier layer
15 Copper sedimentary layers
Contact of 15 $_1$ copper
16 Barrier material sedimentary layers
16 $_1$ barrier layer

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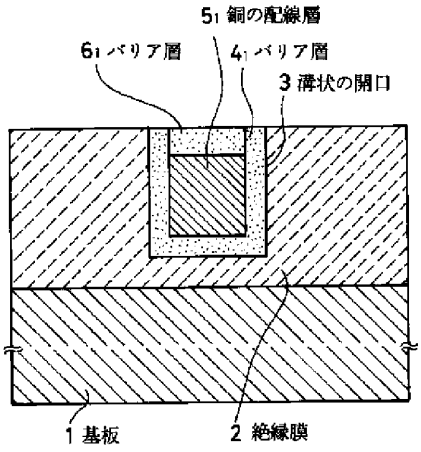
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A [FIG. 1]

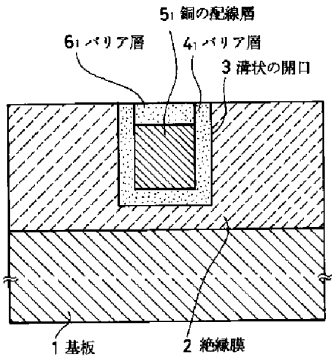
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A [FIG. 2]

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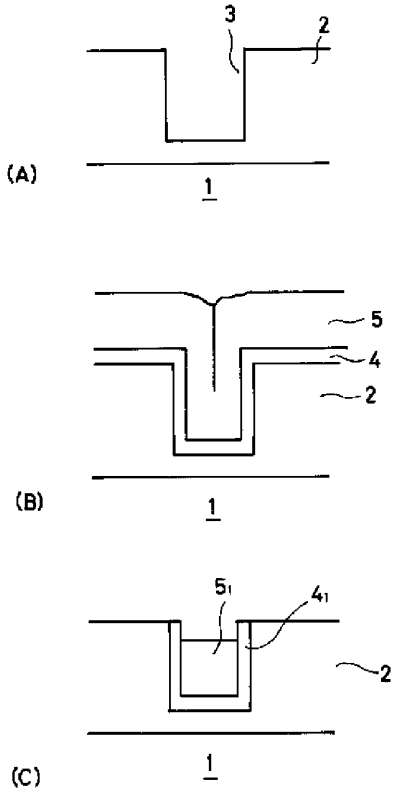


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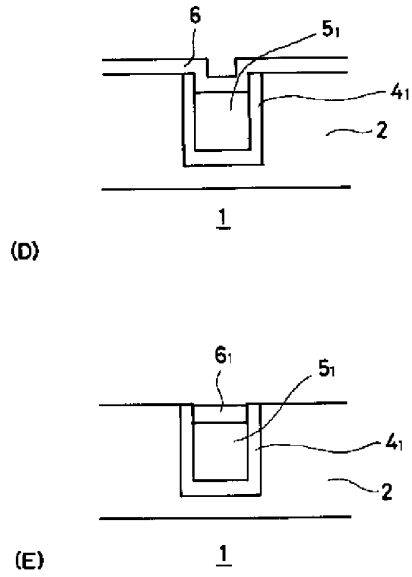
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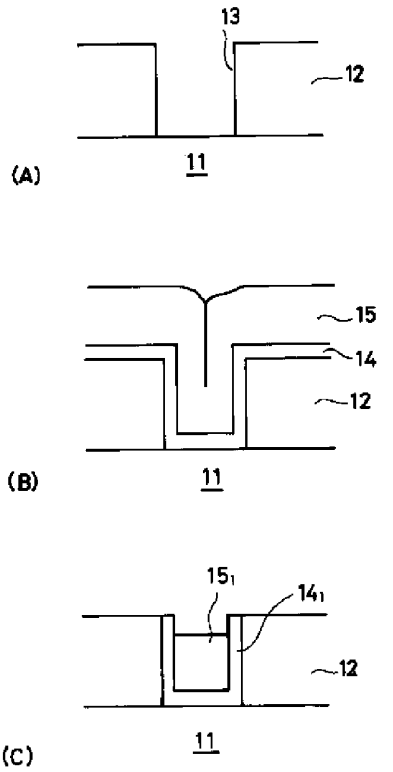
A [FIG. 3]

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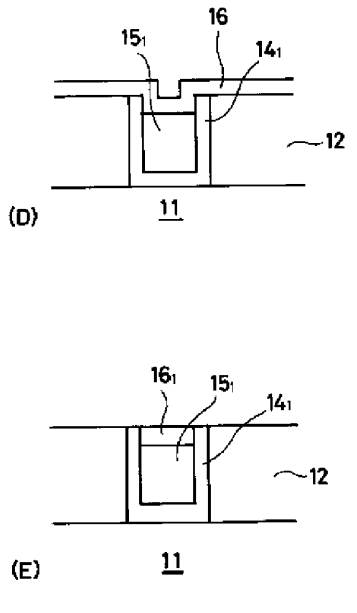
A [FIG. 4]

第２実施例の集積回路装置の製造方法の工程説明図（１）



A [FIG. 5]

第２実施例の集積回路装置の製造方法の工程説明図（２）



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First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
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Warnings:					
Information:					
2	Other Reference-Patent/App/Search documents	1_Ref_P38794KR-D_NOA_09-02-16.pdf	1776167 988cbe4ed5814d18a16ed9a6a7471cf880fd9bb6	no	2
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Information:					
3	Other Reference-Patent/App/Search documents	2_Ref_P38794KR-D2_OA_03-02-17.pdf	2601347 72797e16c59aeddb173fa874da06b5994114cf25	no	9
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5	Other Reference-Patent/App/Search documents	4_Ref_P38794CN_OA_03-15-18.pdf	820993 595afbbb1e70cc4b28f277b8d285b1ac37456d80	no	20
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Information:					
6	Other Reference-Patent/App/Search documents	5_Ref_P38794KR-D2-D2_OA_05-01-18.pdf	3588963 6a434e84ed6fa335678ecaabe604fe87dafe9f73	no	13
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Information:					
7	Other Reference-Patent/App/Search documents	6_Ref_P38794KR_OA_01-07-16.pdf	1244170 c57e3df900e30375c7f9e84238ece511c94f2539	no	8
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Information:					
8	Other Reference-Patent/App/Search documents	9_Ref_P38794KR-D2_02-20-18.pdf	2500769 47043c4f5925243be80df3e49564e47827960bca	no	8
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Information:					
9	Other Reference-Patent/App/Search documents	11_Ref_P38794US_OA_04-10-15.pdf	290806 bf55b612fbd2d635a1c268b778a742a66695bd09	no	7
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Information:					
10	Other Reference-Patent/App/Search documents	12_Ref_P38794US_OA_08-28-15.pdf	271243 645f723f8b3024aa1b9d36bb3600240422b30872	no	6
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Information:					
11	Other Reference-Patent/App/Search documents	13_Ref_P38794US_OA_11-03-14.pdf	255333 4ae9127e0ef4779b8af2a60f2a0211a642dd4437	no	7
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Information:					
12	Other Reference-Patent/App/Search documents	14_Ref_P38794USD_07-05-16.pdf	258738 abf1a65ec629be3fdaafa622991d42c47d9c201b	no	6
Warnings:					
Information:					
13	Other Reference-Patent/App/Search documents	15_Ref_P38794USD_OA_01-29-16.pdf	373652 206f76f9e649ae4e727e00e259c705e708475ed0	no	8
Warnings:					
Information:					
14	Other Reference-Patent/App/Search documents	16_Ref_P38794CN-D-OA1-06-28-17.pdf	210890 5f426188a4ce31540edeb59a5caa2109fdecb402	no	6
Warnings:					
Information:					

15	Foreign Reference	A_Ref_JP_06-275612.pdf	455852 71e7aff190fa430f053ef692bbc45069a04a5e3b	no	16
Warnings:					
Information:					
16	Foreign Reference	B_Ref_CN1364311.pdf	9133440 016d24b0bd5d4d1372d6d311b7302e50732a7c5f	no	35
Warnings:					
Information:					
17	Foreign Reference	C_Ref_CN1921102.pdf	1790519 2a219058a3d0b1790ef32e7e8ec824b36e1dec61	no	25
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18	Foreign Reference	D_JP_3326698.pdf	429339 f9fad0e00535877b7c24aa51f3fd176b8c58a765	no	15
Warnings:					
Information:					
19	Other Reference-Patent/App/Search documents	-8_Ref_P38794CN-OA_04-25-17.pdf	10401209 af84eebc186477369c56097b92c1af17a45c34fa	no	19
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Information:					
20	Other Reference-Patent/App/Search documents	-7_Ref_P38794TW_OA_03-22-17_.pdf	1892822 955a66a871533ce86cb778529e4a53aadbdf8f3a	no	4
Warnings:					
Information:					
21	Other Reference-Patent/App/Search documents	-10_Ref_TW_NOA_06-29-17.pdf	924964 72eac898414e3045dd8fad08d4e78ed9d1019a11	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	42700298		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyanov et al.
Art Unit	2898
Examiner Name	Fortich, Rodolofo D.
Attorney Docket No.	P38794USDC

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

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CERTIFICATION STATEMENT

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OR

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OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Justin K. Brask/	Date (MM-DD-YYYY)	06-15-2018
Name/Print	Justin K. Brask	Registration Number	61080

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 06-15-18

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	Fortich, Rodolfo D.
Sheet 1 of 1	Attorney Docket No: P38794USDC	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		Office Action for Chinese Patent Application 201180074611.5 (Attorney Docket No. P38794CN), mailed March 9, 2018, 7 pages.	X

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	32845304
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Lisa Puccinelli
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	08-JUN-2018
Filing Date:	03-APR-2017
Time Stamp:	17:51:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Other Reference-Patent/App/Search documents	P38794CN_OA_03-09-18_w_Translation.pdf	1695337 8fe146394c2b43278e5376addfbbbafd988aa856	no	7

Warnings:

Information:					
2		P38794USDC_IDS_06-08-18.pdf	607462 5fbaebc753c9c423f6d0529177410 4f6a9f78e6c	yes	2
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
		Total Files Size (in bytes):	2302799		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyanov et al.
Art Unit	2898
Examiner Name	Fortich, Rodolofo D.
Attorney Docket No.	P38794USDC

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OR

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OR

☒ None

☐ The IDS Filing Fee in the amount of $240.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	06-08-2018
Name/Print	Michael A. Bernadicou	Registration Number	35,934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Lisa Puccinelli */Lisa Puccinelli/* *Date* 06-08-18

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	FORTICH, RODOLFO D
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

US PATENT DOCUMENTS

Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No [1]	Foreign Patent Document — Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T [2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T [2]
		2nd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed July 1, 2016, 21 pgs., with English translation.	X
		3rd Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) Mailed December 20, 2016, 11 pgs., with English translation.	X
		Notice of Final Rejection for Korean Patent Application No. 10-2016-7033745 (Attorney Docket No. P38794KR-D2) Mailed December 5, 2017, 6 pgs., with English translation.	X

EXAMINER **DATE CONSIDERED**

Based on PTO/SB/08A(08-06) - Substitute Disclosure Statement Form (PTO-1449)

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

Electronic Acknowledgement Receipt	
EFS ID:	31964793
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Sheri Villarreal
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	05-MAR-2018
Filing Date:	03-APR-2017
Time Stamp:	22:12:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794USDC_IDS_03_05_18.pdf	320297 d1f31c9cccf976b25780c7c158f6c00a22a0b8a2	yes	2

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Non Patent Literature	P38794CN_OA2_English_translation_07_01_16.pdf	5109288 624880b6525bfce4466e0e98d2ef9f4c1129fe6d	no	21
Warnings:					
Information:					
3	Non Patent Literature	P38794CN_OA3_English_Translation_12_20_16.pdf	4110468 a6c82f1d73f4f0955a198bd0a31ee9f5833f6edf	no	11
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Information:					
4	Non Patent Literature	P38794KR-D2_FOA_English_Translation_12_05_17.pdf	396208 ac6fb55ccf8faeabcb0f17631a831ca5b6769822	no	6
Warnings:					
Information:					
		Total Files Size (in bytes):	9936261		

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No.	15/477,506
Filing Date	April 3, 2017
First Inventor	Boyan Boyanov, et al.
Art Unit	2898
Examiner Name	FORTICH, RODOLFO D
Attorney Docket No.	P38794USDC 111548-227293 Con. No. 2892

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SIGNATURE

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Signature	/Michael A. Bernadicou/	Date (MM-DD-YYYY)	03-05-2018
Name/Print	Michael A. Bernadicou	Registration Number	35,934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal /Sheri Villarreal/ Date 03-05-18

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Substitute for form 1449A/PTO	Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*	**Application Number**	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov, et al.
	Group Art Unit	2898
	Examiner Name	FORTICH, RODOLFO D
Sheet 1 of 1	Attorney Docket No: P38794USDC 111548-227293	

US PATENT DOCUMENTS					
Examiner Initial *	Cite No [1]	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 7,396,757	07-08-2008	IBM CORP	
		US6,908,847	06-21-2005	SAITO, TATSUYUKI, ET AL.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No [1]	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[2]
		KR-1020090085066	08-06-2009	IBM		X
		CN-101490825A	07-22-2009	IBM		X
		CN-1420560	05-28-2003	HITACHI LTD		X

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		4th Non-Final Office Action for Chinese Patent Application No. 201180074611.5 (Attorney Docket No. P38794CN) mailed September 12, 2017, 7 pgs., with English translation.	X
		1st Non-Final Office Action for Chinese Patent Application No. 201510203055.7 (Attorney Docket No. P38794CND) mailed August 28, 2017, 10 pgs., with English translation.	X
		Final Office Action for Korean Patent Application 10-2016-7033745 (Attorney Docket No. P38794KRD2) mailed July 18, 2017, 5 pgs., with English translation.	x

EXAMINER **DATE CONSIDERED**

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Semiconductor device and mfg. method thereof

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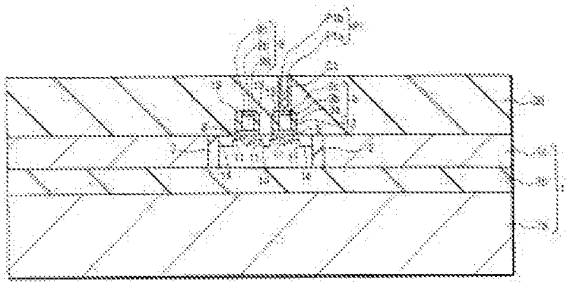
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Provided is a semiconductor device comprising a first interlayer insulating film formed over a semiconductor substrate and having a wiring trench; a wiring portion which has a first barrier metal layer formed over the side walls and bottom surface of said wiring trench, a first conductor layer formed over said first barrier metal layer so as to embed said wiring trench with said first conductor layer, and a capping barrier metal film formed over the surface of said first conductor layer; a second interlayer insulating film formed over said first interlayer insulating film and having a connecting hole; and a



connecting portion which has a second barrier metal layer formed over the side walls and bottom surface of said connecting hole, and a second conductor layer formed over said second barrier metal layer so as to embed said connecting hole with said second conductor layer;; wherein at a joint between said connecting portion and said wiring portion, at least either one of said second barrier metal layer or said capping barrier metal film on the bottom surface of said connecting hole is removed. According to the present invention, contact resistance between the first-level interconnect and plug can be reduced and electromigration resistance can be improved.

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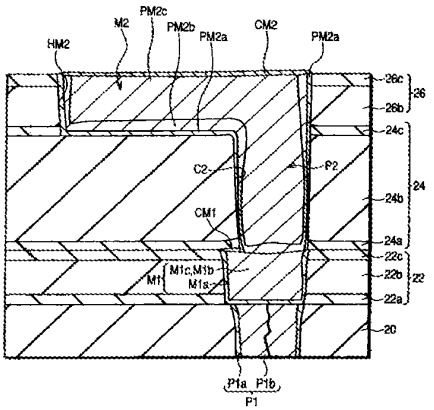
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[54] 发明名称 半导体器件及其制造方法

[57] 摘要

提供了一种半导体器件，包括：制作在半导体衬底上并具有布线沟槽的第一层间绝缘膜；布线部分，它具有制作在所述布线沟槽侧壁和底部表面上的第一阻挡金属层、制作在所述第一阻挡金属层上用以掩埋所述布线沟槽的第一导体层、以及制作在所述第一导体层表面上的帽层阻挡金属膜；制作在所述第一层间绝缘膜上并具有连接孔的第二层间绝缘膜；以及连接部分，它具有制作在所述连接孔的侧壁和底部表面上的第二阻挡金属层，以及制作在所述第二阻挡金属层上用以掩埋所述连接孔的第二导体层；其中，在所述连接部分与所述布线部分之间的连接处，至少清除所述连接孔底部表面上的所述第二阻挡金属层或所述帽层阻挡金属膜中的任何一个。 根据本发明，能够减小第一层互连与栓塞之间的接触电阻，并能够改善电迁移阻力。



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1．一种半导体器件，包括：

制作在半导体衬底上并具有布线沟槽的第一层间绝缘膜；

布线部分，它具有制作在所述布线沟槽侧壁和底部表面上的第一阻挡金属层、制作在所述第一阻挡金属层上以便掩埋所述布线沟槽的第一导体层、以及制作在所述第一导体层表面上的帽层阻挡金属膜；

制作在所述第一层间绝缘膜上并具有连接孔的第二层间绝缘膜；以及

连接部分，它具有制作在所述连接孔的侧壁和底部表面上的第二阻挡金属层，以及制作在所述第二阻挡金属层上以便掩埋所述连接孔的第二导体层；

其中，在所述连接部分与所述布线部分之间的连接处，至少清除所述连接孔底部表面上的所述第二阻挡金属层或所述帽层阻挡金属膜中的任何一个。

2．一种半导体器件，包括布线部分和连接部分，

所述布线部分具有第一导体层和制作在所述第一导体层侧面和底部表面上从而环绕所述第一导体层的第一阻挡金属层，且

所述连接部分制作在所述布线部分上并具有第二导体层和制作在所述第二导体层侧面上从而环绕所述第二导体层的第二阻挡金属层，

其中，在所述连接部分与所述布线部分之间的连接处，所述第二阻挡金属层被制作成所述第二导体层底部表面上的不连续膜。

3．一种半导体器件，包括布线部分和制作在层间绝缘膜中的连接部分，

所述布线部分具有第一导体层、制作在所述第一导体层侧面和底部表面上从而环绕所述第一导体层的第一阻挡金属层、以及制作在所述第一导体层表面上的帽层阻挡金属膜，

所述连接部分具有第二导体层以及制作在所述第二导体层的侧

面和底部表面中至少侧面上从而环绕所述第二导体层的第二阻挡金属层，

其中，在所述连接部分与所述布线部分之间的连接处，所述第二阻挡金属层或所述帽层阻挡金属膜都不被制作，或被制作成所述第二导体层底部表面上的不连续膜。

4．根据权利要求 1 的半导体器件，

其中在所述布线部分与所述连接部分之间的连接处，前者被制作成面积大于后者。

5．根据权利要求 1 的半导体器件，

其中所述帽层阻挡金属膜不仅仅制作在所述连接部分与所述布线部分之间的连接处。

6．根据权利要求 1 的半导体器件，

其中从所述连接孔的底部表面清除所述第二阻挡金属层。

7．根据权利要求 1 的半导体器件，

其中在所述第二导体层的底部表面上不制作所述第二阻挡金属层。

8．一种半导体器件的制造方法，包括下列步骤：

在半导体衬底上制作第一层间绝缘膜；

在所述第一层间绝缘膜中制作布线沟槽；

在所述布线沟槽的侧壁和底部表面上制作第一阻挡金属层；

在所述第一阻挡金属层上制作第一导体层，以便用所述第一导体层掩埋所述布线沟槽；

在所述第一导体层的表面上制作帽层阻挡金属膜；

在所述第一层间绝缘膜上制作第二层间绝缘膜；

在所述第二层间绝缘膜中制作连接孔；

在所述连接孔的侧壁和底部表面上制作第二阻挡金属层；以及

在所述第二阻挡金属层上制作第二导体层，以便用所述第二导体层掩埋所述连接孔，

其中，在制作所述连接孔的步骤中，仅仅在所述连接孔与所述布

线沟槽的重叠部分处清除所述帽层阻挡金属膜。

9. 根据权利要求 8 的制造方法，

其中，在所述布线沟槽与所述连接孔的重叠部分处，所述布线沟槽被制作成面积大于所述连接孔。

10. 根据权利要求 8 的制造方法，还包括，在制作所述第二导体层之前，从所述连接孔的底部表面清除所述第二阻挡金属层。

11. 一种半导体器件，包括第一布线结构和第二布线结构，

所述第一布线结构具有第一布线部分和制作在其上的第一连接部分，

所述第一布线部分具有第一导体层、制作在所述第一导体层侧面和底部表面上从而环绕所述第一导体层的第一阻挡金属层、以及制作在所述第一导体层表面上的第一帽层阻挡金属膜，

所述第一连接部分制作在所述第一布线部分上并具有第二导体层，第二阻挡金属层制作在所述第二导体层侧面和底部表面上从而环绕所述第二导体层，且

所述第二布线结构制作在所述第一布线结构上并具有第二布线部分和制作在其上的第二连接部分，

所述第二布线部分具有第三导体层、制作在所述第三导体层侧面和底部表面上从而环绕所述第三导体层的第三阻挡金属层、以及制作在所述第三导体层表面上的第二帽层阻挡金属膜，且

所述第二连接部分制作在所述第二布线部分上并具有第四导体层，第四阻挡金属层制作在所述第四导体层侧面和底部表面上从而环绕所述第四导体层，

其中，所述第一和第二阻挡金属层以及所述第一帽层阻挡金属膜的结构分别不同于所述第三和第四阻挡金属层以及所述第二帽层阻挡金属膜。

12. 根据权利要求 11 的半导体器件，

其中所述第二帽层阻挡金属膜制作成比所述第一帽层阻挡金属膜更薄，或所述第一帽层阻挡金属膜被制作成比所述第二帽层阻挡金

属膜更薄。

13. 根据权利要求 11 的半导体器件，

其中从所述第四导体层的底部表面清除所述第四阻挡金属层或所述第二帽层阻挡金属膜中的任何一个，且

其中从所述第二导体层的底部表面清除所述第二阻挡金属层或所述第一帽层阻挡金属膜中的任何一个。

14. 根据权利要求 11 的半导体器件，

其中保留所述第四阻挡金属层和所述第二帽层阻挡金属膜，而不从所述第四导体层的底部表面清除，且

其中从所述第二导体层的底部表面清除所述第二阻挡金属层或所述第一帽层阻挡金属膜中的任何一个。

15. 根据权利要求 11 的半导体器件，

其中所述第二布线结构的所述第二连接部分的直径大于所述第一布线结构的所述第一连接部分，或所述第二布线结构的所述第二布线部分的宽度大于所述第一布线结构的所述第一布线部分。

16. 根据权利要求 11 的半导体器件，还包括经由所述第二连接部分与所述第二布线部分连接的布线，

其中保留所述第四阻挡金属层和所述第二帽层阻挡金属膜不被清除。

17. 一种半导体器件，包括：

制作在半导体衬底上的第一绝缘膜；

制作在所述第一绝缘膜上的第二绝缘膜；

借助于选择性地清除所述第一绝缘膜和所述第二绝缘膜而制作的布线沟槽；

布线部分，它具有制作在所述布线沟槽的侧壁和底部表面上的第一阻挡金属层、制作在所述第一阻挡金属层上以掩埋所述布线沟槽的第一导体层、以及制作在所述第一导体层表面上的帽层阻挡金属膜；

制作在所述第二绝缘膜上并具有连接孔的第三绝缘膜；以及

连接部分，它具有制作在所述连接孔侧壁和底部表面中至少侧壁

上的第二阻挡金属层以及制作在所述第二阻挡金属层上以掩埋所述连接孔的第二导体层，

其中，所述第二绝缘膜具有阻挡绝缘膜的功能。

18. 根据权利要求 17 的半导体器件，

其中具有阻挡绝缘膜功能的第四绝缘膜制作在所述帽层阻挡金属膜上。

19. 根据权利要求 17 的半导体器件，

其中所述第二绝缘膜是由介电常数比氮化硅膜低的或介电常数不大于 5.5 的材料组成的低介电常数膜。

20. 根据权利要求 19 的半导体器件，

其中所述低介电常数膜具有 Si 和 C，Si 和 N，Si、C 和 N，Si、O 和 N，Si、O 和 C，或 Si、O、C 和 N，或是利用 CVD 方法用 TMS（三甲氧基硅烷）和 N_2O 形成的膜。

21. 根据权利要求 17 的半导体器件，

其中所述第二绝缘膜在制作所述连接孔时具有腐蚀停止层的功能。

22. 根据权利要求 18 的半导体器件，

其中所述第四绝缘膜在制作所述连接孔时具有腐蚀停止层的功能。

23. 根据权利要求 17 的半导体器件，

其中所述第二阻挡金属层从所述连接孔的底部表面被清除。

24. 根据权利要求 17 的半导体器件，

其中所述第一和第三绝缘膜包括由介电常数低于氧化硅膜或介电常数为 3.7 或以下的材料组成的低介电常数膜。

25. 根据权利要求 24 的半导体器件，

其中所述低介电常数膜具有 Si 和 C，Si、C 和 O，Si、O 和 F，C 和 H，或 Si、O、C 和 H，或还是多孔的。

26. 一种半导体器件的制造方法，包括下列步骤：

在半导体衬底上制作第一绝缘膜；

在所述第一绝缘膜上制作第二绝缘膜;

借助于选择性地清除所述第一绝缘膜和所述第二绝缘膜而制作布线沟槽;

在所述布线沟槽的侧壁和底部表面上制作第一阻挡金属层;

在所述第一阻挡金属层上制作第一导体层以便用所述第一导体层掩埋所述布线沟槽;

在所述第一导体层表面上制作帽层阻挡金属膜;

在所述第二绝缘膜上制作第三绝缘膜;

在所述第三绝缘膜中制作连接孔;

在所述连接孔侧壁和底部表面中的至少侧壁上制作第二阻挡金属层;以及

在所述第二阻挡金属层上制作第二导体层以便用所述第二导体层掩埋所述连接孔,

其中,所述第二绝缘膜用作阻挡绝缘膜。

27. 根据权利要求 26 的制造方法,还包括在所述帽层阻挡金属膜上制作具有阻挡绝缘膜功能的第四绝缘膜的步骤。

28. 根据权利要求 26 的制造方法,

其中所述第二绝缘膜是由介电常数比氮化硅膜低的或介电常数不大于 5.5 的材料组成的低介电常数膜。

29. 根据权利要求 28 的制造方法,

其中所述低介电常数膜利用 CVD 方法,用 Si 和 C,Si 和 N,Si、C 和 N,Si、O 和 N,Si、O 和 C,Si、O、C 和 N,或 TMS 和 N_2O 形成。

30. 根据权利要求 26 的制造方法,

其中所述第二绝缘膜在制作所述连接孔时具有腐蚀停止层的功能。

31. 根据权利要求 27 的制造方法,

其中所述第四绝缘膜在制作所述连接孔时具有腐蚀停止层的功能。

32. 根据权利要求 26 的制造方法还包括,在制作所述第二导体

层之前，从所述连接孔的底部表面清除所述第二阻挡金属层。

33. 根据权利要求 26 的制造方法，还包括下列步骤：

在所述连接孔的制作步骤中，仅仅从所述连接孔与所述布线沟槽的重叠部分清除所述帽层阻挡金属膜；以及

在所述第二导体层的制作步骤之前，从所述连接孔的底部表面清除所述第二阻挡金属层。

34. 根据权利要求 26 的制造方法，

其中所述第一和第三绝缘膜包括由介电常数低于氧化硅膜或介电常数为 3.7 或以下的材料组成的低介电常数膜。

35. 根据权利要求 34 的制造方法，

其中所述低介电常数膜具有 Si 和 C，Si、C 和 O，Si、O 和 F，C 和 H，或 Si、O、C 和 H，或还是多孔的。

36. 根据权利要求 1 的半导体器件，

其中所述阻挡金属层由 Ta、TaN、TaSiN、W、WN、WSiN、Ti、TiN、TiSiN 的任何一种的单层膜或通过将 Ta、TaN、TaSiN、W、WN、WSiN、Ti、TiN、TiSiN 的任何二种或更多种层叠而得到的叠层膜组成。

37. 根据权利要求 1 的半导体器件，

其中所述帽层阻挡金属膜由主要包括 W、WN、WSiN 和 W 的金属层，主要包括 CoWP、CoWB 或 Co 的金属层，TiN、TiSiN、Ta、TaN、TaSiN 的任何一种的单层膜或所述金属层和单层膜的任何二种的叠层膜组成。

38. 根据权利要求 1 的半导体器件，

其中所述导体层由 Cu、主要包括 Cu 和 Al 的金属层、主要包括 Al 和 Ag 的金属层、主要包括 Ag 的金属层中的任何一种组成。

39. 根据权利要求 8 的制造方法，

其中所述阻挡金属层由 Ta、TaN、TaSiN、W、WN、WSiN、Ti、TiN、TiSiN 的任何一种的单层膜或借助于将 Ta、TaN、TaSiN、W、WN、WSiN、Ti、TiN、TiSiN 的任何二种或更多种层叠而得到的叠层膜组成。

40. 根据权利要求 8 的制造方法，

其中所述帽层阻挡金属膜由主要包括 W、WN、WSiN 和 W 的金属层，主要包括 CoWP、CoWB 或 Co 的金属层，TiN、TiSiN、Ta、TaN、TaSiN 的任何一种的单层膜，或借助于将所述金属层和单层膜的任何二种层叠而得到的叠层膜组成。

41. 根据权利要求 8 的制造方法，

其中所述导体层由 Cu、主要包括 Cu 和 Al 的金属层、主要包括 Al 和 Ag 的金属层、主要包括 Ag 的金属层中的任何一种组成。

42. 一种半导体器件的制造方法，包括下列步骤：

（a）在半导体衬底上的第一绝缘膜中制作第一导体层；

（b）在所述第一导体层的表面上制作帽层阻挡金属膜；

（c）在所述帽层阻挡金属膜和第一绝缘膜上制作第二绝缘膜，然后在所述第二绝缘膜上制作第三绝缘膜；

（d）选择性地清除所述第二和第三绝缘膜以形成存在于所述第二绝缘膜和第三绝缘膜二者中并从所述布线沟槽向所述帽层阻挡金属膜延伸的连接孔；

（e）在所述布线沟槽的侧壁和底部以及所述连接孔的侧壁和底部上，制作阻挡金属膜；

（f）从所述连接孔的底部清除所述阻挡金属膜；以及

（g）在所述布线沟槽和连接孔中制作第二导体层。

43. 根据权利要求 42 的制造方法，

其中在所述阻挡金属制作步骤中，所述阻挡金属膜被制作成在所述布线沟槽底部处的厚度大于在所述连接孔底部处的厚度。

44. 根据权利要求 43 的制造方法，

其中在所述步骤（f）中，各向异性腐蚀被用来从所述连接孔底部清除所述阻挡金属膜。

45. 根据权利要求 42 的制造方法还包括，在所述步骤(d)和(e)之间，清除从所述连接孔底部暴露的所述帽层阻挡金属膜。

46. 一种半导体器件，包括：

（a）制作在半导体衬底上第一绝缘膜中的第一导体层；

（b）制作在所述第一绝缘膜和所述第一导体层上的第二绝缘膜；

（c）制作在所述第二绝缘膜上的第三绝缘膜；

（d）制作在所述第三绝缘膜中的布线沟槽；

（e）制作在所述第二绝缘膜中并从所述布线沟槽底部延伸到所述第一导体层的连接孔；

（f）制作在所述布线沟槽侧壁和底部以及所述连接孔侧壁上的阻挡金属层；

（g）制作在所述布线沟槽和连接孔中的第二导体层；以及

（h）制作在所述第一导体层与所述第二绝缘膜之间的帽层阻挡金属膜，

其中在所述第一导体层与所述第二导体层之间，既不制作所述帽层阻挡金属膜也不制作所述阻挡金属层。

47．一种半导体器件，包括：

（a）制作在半导体衬底上第一绝缘膜中的第一导体层；

（b）制作在所述第一绝缘膜和第一导体层上的第二绝缘膜；

（c）制作在所述第二绝缘膜上的第三绝缘膜；

（d）制作在所述第三绝缘膜中的布线沟槽；

（e）制作在所述第二绝缘膜中并从所述布线沟槽底部延伸到所述第一导体层的连接孔；

（f）制作在所述布线沟槽侧壁和底部以及所述连接孔侧壁和底部上的阻挡金属膜；

（g）制作在所述布线沟槽和连接孔中的第二导体层；以及

（h）制作在所述第一导体层与所述第二绝缘膜之间的帽层阻挡金属膜，

其中在所述第一导体层与所述第二导体层之间，不制作所述帽层阻挡金属膜。

48．一种半导体器件，包括：

（a）制作在半导体衬底上第一绝缘膜中的第一导体层；

（b）制作在所述第一导体层上的阻挡金属层；

（c）制作在所述第一绝缘膜和阻挡金属层上的第二绝缘膜；

（d）制作在所述第二绝缘膜上的第三绝缘膜；

（e）制作在所述第三绝缘膜中的布线沟槽；

（f）制作在所述第二绝缘膜中并从所述布线沟槽底部延伸到所述阻挡金属层的连接孔；

（g）制作在所述布线沟槽侧壁和底部以及所述连接孔侧壁上的阻挡金属膜；

（h）制作在所述布线沟槽和连接孔中的第二导体层，

其中在所述第一导体层与所述第二导体层之间，不制作所述阻挡金属层。

49. 根据权利要求 8 的制造方法，还包括至少下列步骤之一：

在制作所述连接孔的步骤之后，在含氢或氨的气氛中，对所述第一导体层的暴露表面进行热处理；

在含氢或氨以及稀有气体中任何一种的气氛中，产生等离子体，从而用等离子体辐照所述第一导体层暴露的所述表面；以及

用稀有气体溅射腐蚀所述第一导体层暴露的所述表面。

50. 根据权利要求 10 的制造方法，还包括至少下列步骤之一：

在清除所述第二阻挡金属层的步骤之后，在含氢或氨的气氛中，对所述第一导体层暴露的表面进行热处理；

在含氢或氨以及稀有气体中任何一种的气氛中，产生等离子体，从而用等离子体辐照所述第一导体层暴露的所述表面；以及

用含氢氟酸的溶液清洗所述第一导体层暴露的所述表面。

半导体器件及其制造方法

技术领域

本发明涉及到半导体集成电路器件，更确切地说是涉及到能够用于各个互连之间连接部分的技术。

背景技术

近年来，由于半导体集成电路器件（半导体器件）倾向于小型化和多层化，对于用来在绝缘膜中形成沟槽，并以导电膜将其埋置，从而形成互连的所谓镶嵌技术，已经进行了研究。

这一镶嵌技术可以被粗略地分成单一镶嵌技术和双重镶嵌技术。在单一镶嵌技术中，布线沟槽和用来连接各个互连的沟槽，用不同的步骤来埋置，而在双重镶嵌技术中，布线沟槽和连接沟槽被同时埋置。

铜膜之类被用作待要填充在这种沟槽中的导电膜。

为了（1）防止构成待要埋置的导电膜的金属（当导电膜是铜膜时，此金属是铜）在绝缘膜中扩散，或（2）当绝缘膜由诸如氧化硅膜之类的氧化物组成时，防止否则会由于氧化硅膜与导电膜的接触而发生的导电膜氧化，制作了具有阻挡性质的导电膜。

在待要埋置在沟槽中的导电膜（例如铜膜）上，制作诸如氮化硅膜之类的具有阻挡性质的绝缘膜，以便防止金属扩散进入待要制作在导电膜上的绝缘膜中，或用绝缘膜防止其氧化。

发明内容

然而，氮化硅膜具有大的介电常数，致使互连的RC时间常数变大，从而干扰器件的高速运行。

构成导电膜的金属的扩散（转移）引起电迁移。作为对铜的扩散率的研究结果，铜-阻挡膜界面上的扩散激活能被认为大于铜-氮化硅膜

界面上的扩散激活能（铜以更大的扩散率扩散）。因此，电迁移寿命受到铜-氮化硅膜界面上铜扩散的激活能的限制。

若电迁移在各个互连之间的连接部分的底部表面上引起空洞，则连接部分与下方互连之间的接触面积变小，导致互连寿命更快地降低。

本发明人研究了诸如具有阻挡性质的钨（W）膜之类的导电膜在互连上的形成。

例如，在美国专利 6147402 中，公开了在由 Al-Cu 合金（AlnCuy 合金）组成的互连上形成由 W 组成的帽层（WCAP）的技术。

在美国专利 6114243 中，公开的是一种在所谓镶嵌结构中，在铜层（24）上形成导电帽层（26），在其上形成通孔或双重镶嵌窗口（35），然后形成阻挡层（36）和铜层（38）的技术。括号中的参考号是专利公报中所述的参考号。

然而，互连上诸如具有阻挡性质的钨（W）膜之类的导电膜（以下称为“帽层阻挡金属层”）的形成，导致这样一种结构，其中，构成互连的金属膜、帽层阻挡金属层、阻挡金属层、以及构成连接部分的金属层，已经被按此顺序层叠在互连与连接部分之间。在这种结构中，这些膜之间的接触电阻不可避免地增大。

当金属原子由于电迁移而在这种结构中发生转移时，连接部分与互连之间的帽层阻挡金属层和阻挡金属层的存在就干扰金属在连接部分与互连之间的转移。

结果，空洞的产生频率增大，且引起断路的可能性增大。与电迁移造成的断路一样，由于界面上阻挡金属和铜之间的应力诱导剥离或应力诱导空洞形成亦即应力迁移，也可能产生相似的断路。

本发明的目的是减小互连与连接部分之间的接触电阻。

本发明的另一目的是改善可靠性，更确切地说是降低电迁移造成的空洞或断路的产生频率，或降低应力迁移造成的断路的产生频率。

本发明的再一目的是改善半导体器件的特性。

借助于此处的描述和附图，本发明的上述目的和新颖特点将显而易见。

以下简要地概述一下本说明书公开的本发明的典型发明。

（1）一种根据本发明的半导体器件，包括：

制作在半导体衬底上并具有布线沟槽的第一层间绝缘膜；

布线部分，它具有：制作在布线沟槽侧壁和底部表面上的第一阻挡金属层，制作在第一阻挡金属层上用以掩埋布线沟槽的第一导体层，以及制作在第一导体层表面上的帽层阻挡金属膜；

制作在第一层间绝缘膜上并具有连接孔的第二层间绝缘膜；以及

连接部分，它具有：制作在连接孔的侧壁和底部表面上的第二阻挡金属层，以及制作在第二阻挡金属层上用以掩埋连接孔的第二导体层；

其中，在连接部分与布线部分之间的连接处，至少清除连接孔底部表面上的第二阻挡金属层或帽层阻挡金属膜中的任何一个。

（2）根据本发明的半导体器件的制造方法，包括：

在半导体衬底上制作第一层间绝缘膜，

在第一层间绝缘膜中制作布线沟槽，

在布线沟槽的侧壁和底部表面上制作第一阻挡金属层，

在第一阻挡金属层上制作第一导体层，以便用第一导体层掩埋布线沟槽，

在第一导体层的表面上制作帽层阻挡金属膜，

在第一层间绝缘膜上制作第二层间绝缘膜，

在第二层间绝缘膜中制作连接孔，

在连接孔的侧壁和底部表面上制作第二阻挡金属层，以及

在第二阻挡金属层上制作第二导体层，以便用第二导体层掩埋连接孔；

其中，在制作连接孔的步骤中，仅仅从连接孔与布线沟槽的重叠部分清除帽层阻挡金属膜。

（3）一种根据本发明的半导体器件，包括第一布线结构和第二布线结构，第一布线结构具有制作在其上的第一布线部分和第一连接部分；

第一布线部分具有第一导体层、制作在第一导体层侧壁和底部表面上以便环绕第一导体层的第一阻挡金属层、以及制作在第一导体层表面上的第一帽层阻挡金属膜；且

第一连接部分制作在第一布线部分上并具有第二导体层以及制作在第二导体层侧面和底部表面上以便环绕第二导体层的第二阻挡金属层；且

第二布线结构制作在第一布线结构上并具有制作在其上的第二布线部分和第二连接部分；

第二布线部分具有第三导体层、制作在第三导体层侧壁和底部表面上以便环绕第三导体层的第三阻挡金属层、以及制作在第三导体层表面上的第二帽层阻挡金属膜；且

第二连接部分制作在第二布线部分上并具有第四导体层和制作在第四导体层侧面和底部表面上以便环绕第四导体层的第四阻挡金属层；

其中，第一和第二阻挡金属层以及第一帽层阻挡金属膜的结构分别不同于第三和第四阻挡金属层和第二帽层阻挡金属膜。

（4）一种根据本发明的半导体器件，包括：

制作在半导体衬底上的第一绝缘膜；

制作在第一绝缘膜上的第二绝缘膜；

借助于选择性地清除第一绝缘膜和第二绝缘膜而制作的布线沟槽；

布线部分，它具有制作在布线沟槽侧壁和底部表面上的第一阻挡金属层、制作在第一阻挡金属层上以便掩埋布线沟槽的第一导体层、以及制作在第一导体层表面上的帽层阻挡金属膜；

制作在第二绝缘膜上并具有连接孔的第三绝缘膜；以及

连接部分，它具有制作在连接孔侧壁和底部表面的至少侧壁上的第二阻挡金属层以及制作在第二阻挡金属层上以便掩埋连接孔的第二导体层；

其中，第二绝缘膜具有阻挡绝缘膜的功能。

（5）一种根据本发明的半导体器件的制造方法，包括：

在半导体衬底上制作第一绝缘膜，

在第一绝缘膜上制作第二绝缘膜，

借助于选择性地清除第一绝缘膜和第二绝缘膜而制作布线沟槽，

在布线沟槽的侧壁和底部表面上制作第一阻挡金属层，

在第一阻挡金属层上制作第一导体层以便将其掩埋在布线沟槽中，

在第一导体层表面上制作帽层阻挡金属膜，

在第二绝缘膜上制作第三绝缘膜，

在第三绝缘膜中制作连接孔，

在连接孔侧壁和底部表面中的至少侧壁上制作第二阻挡金属层，以及

在第二阻挡金属层上制作第二导体层以便将其掩埋在连接孔中；

其中，第二绝缘膜用作阻挡绝缘膜。

附图说明

图 1 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 2 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 3 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 4 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 5 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 6 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 7 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 8 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 9 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 10 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 11 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 12 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 13 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 14 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 15 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 16 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 17 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 18 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 19 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 20 是衬底的局部剖面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 21 是衬底的局部平面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 22 是衬底的局部平面图，说明了根据本发明实施方案 1 的半导

体器件的制造方法；

图 23 是衬底的局部平面图，说明了根据本发明实施方案 1 的半导体器件的制造方法；

图 24 是衬底的局部剖面图，说明了根据本发明实施方案 2 的半导体器件的制造方法；

图 25 是衬底的局部剖面图，说明了根据本发明实施方案 2 的半导体器件的制造方法；

图 26 是衬底的局部剖面图，说明了根据本发明实施方案 3 的半导体器件的制造方法；

图 27 是衬底的局部剖面图，说明了根据本发明实施方案 4 的半导体器件的制造方法；

图 28 是衬底的局部剖面图，说明了根据本发明实施方案 5 的半导体器件的制造方法；

图 29 是衬底的局部剖面图，说明了根据本发明实施方案 6 的半导体器件的制造方法；

图 30 是衬底的局部剖面图，说明了根据本发明实施方案 6 的半导体器件的制造方法；

图 31 是衬底的局部剖面图，说明了根据本发明实施方案 7 的半导体器件的制造方法；

图 32 是衬底的局部剖面图，说明了根据本发明实施方案 8 的半导体器件的制造方法；

图 33 是衬底的局部平面图，说明了根据本发明实施方案的半导体器件的制造方法；

图 34 是衬底的局部剖面图，说明了根据本发明实施方案的半导体器件的制造方法；

图 35 是衬底的局部平面图，说明了根据本发明实施方案 9 的半导体器件的制造方法；

图 36 是衬底的局部剖面图，说明了根据本发明实施方案 9 的半导体器件的制造方法；

图 37 是衬底的局部剖面图，说明了根据本发明实施方案 6 的半导体器件的制造方法；

图 38 是衬底的局部剖面图，说明了根据本发明实施方案 7 的半导体器件的制造方法；

具体实施方式

下面将根据附图来详细描述本发明的各个实施方案。在所有用来描述下述各个实施方案的附图中，用相似的参考号来表示具有相似功能的元件，且重复的描述从略。

（实施方案 1）

以下按其制造步骤的顺序来描述根据本发明实施方案的半导体器件。图 1-23 是衬底的局部剖面图或局部平面图，说明了根据本发明实施方案 1 的半导体器件的制造方法。

如图 1 所示，作为半导体元件的一个例子，在半导体衬底的主表面上制作 n 沟道型 MISFET（金属绝缘体半导体场效应晶体管）Qn。

下面是 MISFET 制作工艺的一个例子。

首先制备的是半导体衬底 1，即所谓 SOI（绝缘体上硅）衬底，它具有绝缘膜，例如制作在半导体区 1a 上的氧化硅膜 1b 以及制作在绝缘膜上的 p 型半导体区 1c。此半导体衬底的各个元件形成区（半导体区 1c）被元件隔离区 2 隔离。利用半导体区 1c 的热氧化或借助于将氧化硅膜掩埋在半导体区 1c 中形成的沟槽中，能够形成这些元件隔离区 2。利用其中已经形成了元件隔离区 2 的这些区域，来确定其中待要制作诸如 MISFET 之类的半导体元件的有源区。

利用半导体衬底（以下简称为“衬底”）1 的热氧化，在其表面上形成清洁的栅绝缘膜 8。

在栅绝缘膜 8 上相继淀积低阻多晶硅膜 9a、薄的 WN（氮化钨）膜 9b、以及 W（钨）膜 9c 作为导电膜。

然后，利用例如干法腐蚀技术，对 W 膜 9c、WN 膜 9b、以及多晶硅膜 9a 进行腐蚀，从而形成具有多晶硅膜 9a、WN 膜 9b、以及 W 膜 9c 的

栅电极。

借助于对栅电极 9 二侧上的衬底 1 进行 n 型杂质磷(P)或砷(As)的离子注入，形成 n^-型半导体区 11。

在衬底 1 上淀积氮化硅膜作为绝缘膜之后，进行各向异性腐蚀，以便在栅电极 9 的侧壁上形成侧壁间隔 13。

然后，对栅电极 9 二侧上的衬底 1 进行 n 型杂质的离子注入，以便形成杂质浓度高于 n^-型半导体区 11 的 n^+型半导体区 14(源，漏)。

利用上述各个步骤，就形成了具有 LDD(轻掺杂的漏)结构并配备有源和漏的 n 沟道型 MISFET Qn。除了用于制作的杂质具有相反的导电性之外，可以用相似的方法来制作 p 沟道型 MISFET Qp。

然后形成用来电连接 n 沟道型 MISFET Qn 或其它未示出的元件的互连。下面将描述其制作步骤。

如图 1 所示，在用 CVD(化学气相淀积)方法在 n 沟道型 MISFET Qn 上形成氧化硅膜 20 作为绝缘膜之后，用化学机械抛光(CMP)方法对氧化硅膜 20 的表面进行抛光，以便整平表面。

在氧化硅膜 20 上形成光抗蚀剂膜(未示出，以下简称为“抗蚀剂膜”)。用此抗蚀剂膜作为掩模，对氧化硅膜 20 进行腐蚀，以便在 n 沟道型 MISFET Qn 的栅电极 9 上形成接触孔 C1。

用 CVD 或溅射方法，在接触孔 C1 中的氧化硅膜 20 上，形成薄的氮化钛(TiN)膜 P1a 作为阻挡金属层，随之以用 CVD 方法形成钨(W)膜 P1b 作为导电膜。用 CMP 方法清除接触孔 C1 外面的 TiN 膜 P1a 和 W 膜 P1b，以形成栓塞 P1。钛(Ti)膜与 TiN 膜的叠层可以被用作阻挡金属层。

如图 2 所示，利用原硅酸四乙酯作为源材料，用 CVD 方法在氧化硅膜 20 和栓塞 P1 上形成氧化硅膜 22a 作为绝缘膜。这一氧化硅膜 22a 以下将被称为“TEOS 膜 22”。图 2 是局部放大图，示出了图 1 所示栓塞 1 的周围。栓塞 P1(P1b)中的线是淀积钨膜时出现的裂缝。

然后在 TEOS 膜 22a 上形成低介电常数绝缘膜 22b。借助于涂敷芳香族聚合物材料，随之以热处理，能够形成此低介电常数绝缘膜。作为

变通，有机二氧化硅玻璃可以被用作低介电常数绝缘膜。在此情况下，材料涂敷也随之以热处理。此有机二氧化硅玻璃主要由 SiOCH 或 SiOH 组成。可以采用其它的有机聚合物材料或其中引入孔隙的上述材料。

涂敷这种膜作为低介电常数绝缘膜，使得能够整平衬底表面上的不平整性。衬底表面上的不平整性来自于下方层的不平整图形或 CMP 时的侵蚀或凹陷。

作为变通，可以用 CVD 方法来制作低介电常数绝缘膜。三甲基硅烷或四甲基硅烷被用作源材料来进行制作。在此情况下，膜主要由 SiOC 组成。此处可以使用的低介电常数绝缘膜的例子包括主要由 SiOF 组成的膜、主要由 SiC 组成的膜、以及具有芳香族碳氢化合物结构的有机聚合物膜（含有 C 和 H 的膜）。在上述膜或 SiO_2（氧化硅）膜中引入孔隙（成多孔状），能够减小介电常数。可以用 CVD 方法来制作这些膜。

这种低介电常数绝缘膜的介电常数(3.7 或以下)低于氧化硅膜(例如 TEOS 膜）的介电常数，致使有可能减小各个互连（包括栅电极）之间的寄生电容，从而提高半导体器件的工作速度。

可以采用 CVD 方法制作的上述低介电常数绝缘膜（SiOC、SiOF、SiOC、或 SiO_2 的多孔材料）来代替 TEOS 膜 22a。

在低介电常数绝缘膜 22b 上，制作 TEOS 膜 22c。用相似于 TEOS 膜 22a 的方法来制作 TEOS 膜 22c。

低介电常数绝缘膜 22b 被夹在 TEOS 膜 22a 与 22c 之间，以便保持其叠层的机械强度。在构成绝缘膜（22）的 3 个层中，亦即在 TEOS 膜 22a 与 22c 以及低介电常数绝缘膜 22b 中，制作布线沟槽。

然后，如图 3 所示，借助于用光刻和干法腐蚀方法从待要形成第一层互连的区域清除绝缘膜 22(22a、22b、22c)，而制作布线沟槽 HM1。布线沟槽 HM1 的厚度为例如 0.25μm，宽度为 0.18μm。若低介电常数绝缘膜 22b 与 TEOS 膜 22a 之间的腐蚀选择性被用于上述腐蚀，用 TEOS 膜 22a 作为腐蚀停止膜，则能够制作具有良好可控性的这一布线沟槽 HM1。

如图 4 所示，借助于用溅射方法在包括布线沟槽 HM1 内部的绝缘膜 22 上进行淀积，形成依次层叠有氮化钽（TaN）膜和钽（Ta）膜的阻

挡膜 M1a。可以用 CVD 方法或作为溅射中的一种的离子化溅射方法来制作这一阻挡膜 M1a。在这种离子化溅射中，构成阻挡膜的金属被离子化，并借助于对衬底进行偏置而将方向性赋予金属离子。这使得即使在微小的沟槽中也有可能淀积覆盖性良好的膜。阻挡膜 M1a 被制作成在布线沟槽 HM1 侧壁上的厚度约为 5nm，而在其底部约为 30nm。

阻挡膜不局限于上述 TaN 和 Ta 的层叠膜。可以用作阻挡膜的膜的例子包括由 Ta、TaN、TaSiN、W、氮化钨(WN)、WSiN、Ti、TiN、或 TiSiN 组成的单层膜；Ti、TiN 和 Ti 的三层膜；Ti 和 TiN 的双层膜；TiSiN 和 Ta 的双层膜；Ta、TaN、Ta 的三层膜；以及 Ta 和 TaN 的双层膜。可以采用借助于层叠任何二个或更多个这种单层膜而得到的叠层膜。

用例如电镀方法，在阻挡膜 M1a 上形成诸如铜膜之类的导电膜。首先用例如离子化溅射方法形成薄的铜膜 M1b 作为电镀的籽晶膜。在这一离子化溅射中，铜被离子化，然后衬底被偏置，以便将方向性赋予得到的铜离子。在形成铜膜 M1b 的淀积时，靶与衬底之间的距离保持为大约 300nm，并将衬底温度调节到 25℃或以下。在成膜的开始阶段，比较小的 DC 或 RF 偏压被施加到衬底。在衬底上淀积一定厚度的铜膜之后，施加到衬底的偏压被相对提高。借助于提高偏压，离子被注入到衬底表面，且已经淀积在其上的铜膜被溅射腐蚀。此时，离子被基本上垂直于衬底注入，致使平面零件（绝缘膜 22 和布线沟槽 HM1 的底部）被择优腐蚀。已经散射的铜被重新淀积在布线沟槽 HM1 的侧壁上，从而改善了布线沟槽 HM1 侧壁和底部的台阶覆盖。用低压长距离溅射代替离子化溅射来制作膜。

用电镀方法，利用例如含硫酸铜的溶液作为电镀液，在铜膜 M1b 上制作铜膜 M1c。制作此铜膜 M1c 以便以此掩埋布线沟槽 HM1。

在减压气氛下，衬底 1 被退火(热处理)。如图 5 所示，例如用 CMP 或回腐蚀（etchback）方法，清除布线沟槽 HM1 外面的铜膜 M1c 和 M1b 以及阻挡膜 M1a，以便形成由铜膜 M1b 和 M1c 以及阻挡膜 M1a 组成的第一层互连 M1。然后进一步在减压气氛下对衬底进行退火（热处理）。

如图 6 所示，借助于在其上引起钨(W)的选择性生长或择优生长，

在第一层互连 M1 上形成厚度约为 2-20nm 的钨膜 CM1。例如借助于在下列条件下处理 1.5 分钟来形成钨膜 CM1：0.3 Torr（0.3×1.33322×10^2Pa），衬底托温度设定为 460℃（实际衬底温度为 430℃），六氟化钨（WF_6）流速为 5cc，氢（H_2）流速为 500cc。

利用上述处理，钨仅仅选择性地生长在第一层互连 M1 上，或择优生长在第一层互连 M1 到 TEOS 膜 22 上。在优先考虑钨的生长速率的情况下，此处理在比较高的温度下进行，但可以将温度设定为大约 300℃。于是，可以利用选择性生长或择优生长来方便地制作帽层导电膜。虽然 1）钨膜在形成在整个衬底表面上之后，可以用光刻或干法腐蚀方法来进行图形化；或 2）可以在 CMP 或回腐蚀时，用过抛光或过腐蚀方法形成帽层导电膜，从而使铜膜表面凹陷，并将钨膜埋置在此凹陷中（这意味着在钨膜形成在整个表面上之后，凹陷外面的钨膜被 CMP 之类清除），但这种方法使制造步骤复杂化。此外，必须控制光刻时的不对准或 CMP 时的凹陷或侵蚀，使得难以形成精确的帽层导电膜。另一方面，若采用选择性生长或择优生长，则制造步骤不会变得复杂化，并能够形成具有良好精度的帽层导电膜。不言自明，形成帽层导电膜的方法不局限于选择性生长或择优生长；而是不仅能够采用 CVD 方法，而且能够采用电镀方法来形成帽层导电膜。

同第一层互连 M1 上的帽层导电膜一样，主要由 W 组成的金属层，或 WN、WSiN、TiN、TiSiN、Ta、TaN 或 TaSiN（氮硅化钽）的单层膜，主要由 Co、CoWP（钴钨磷）、CoWB（钴钨硼）组成的金属层，或借助于层叠其中任何多个膜而得到的叠层（双层膜或三层膜），都可以用作钨膜。钨的电阻为 5-20μΩ，而 TiN 的电阻为 80-150μΩ。Ta 或 TaN 的电阻也高于钨。因此，比之采用其它的膜，用钨作为帽层导电膜能够降低互连的电阻。要指出的是，铜的电阻为 1.7-2.2μΩ。

可以在同一个装置中（原位）进行制作钨膜 CM1 之前的退火以及钨膜 CM1 的制作。当在其中具有成膜装置和退火装置二者的多工作室中进行膜的制作和退火而无须从工作室取出衬底时，可以防止衬底（铜膜 M1c）的表面被沾污，从而改善钨膜的成膜性能和质量。

在形成钨膜 CM1 之前，CMP 之后衬底表面上铜的沾污可以借助于用诸如氢氟酸（HF）之类的清洗液进行清洗而被清除。这种清洗改善了钨膜的选择性。此处，利用氢氟酸进行清洗只是一个例子，清洗液不局限于氢氟酸，只要对从衬底表面暴露的绝缘膜的表面具有腐蚀能力或能够清除附着在表面的铜沾污即可。倘若衬底 1 在形成钨膜 CM1 之前，在例如 3000Pa（例如 150-10000Pa）的压力下被暴露于流速为 500cm^3/min（sccm）（例如 50-3000sccm）的氢（H_2）气氛中 3 分钟，则可以得到相似于上述清洗的效果。借助于消除铜沾污或利用氢处理将铜表面上的氧化物还原成铜，钨膜可以具有改进的选择性，能够防止损失选择性所造成的互连之间的短路，并能够改善制作在互连（铜膜）上的钨膜的厚度均匀性。由于铜的氧化物在电扩散时将用作铜离子的供应源，故这一氧化物的清除使得有可能减少铜离子在绝缘膜中的注入量，并改善半导体器件的可靠性。

当钨膜不可避免地生长在 TEOS 膜 22 上时，可以利用上述铜清洗带来的剥离效应来清除绝缘膜上的钨膜。对清洗液的组成没有限制，只要能够腐蚀从衬底表面暴露的绝缘膜表面或能够清除附着在表面上的钨即可。利用形成钨膜之后的 CMP 或衬底表面的后清洗，也能够清除绝缘膜上不必要的钨膜。清除 TOES 膜 22c 上的导电物质，能够防止各个互连之间的短路。

然后，如图 7 所示，用 CVD 方法，在 TEOS 膜 22c 和钨膜 CM1 上相继淀积 TEOS 膜 24a、SiOC 膜 24b、以及 TEOS 膜 24c 作为绝缘膜。这些膜的表面上具有对应于钨膜 CM1 的不平整性。利用此叠层膜(24)的 TEOS 膜 24a 和 SiOC 膜 24b，第一层互连 M1 被隔离于第二层互连 M2。在这些膜中制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2。可以采用 TMS 膜、SiC 膜、或作为介电常数低于 SiN 膜（氮化硅膜）的阻挡绝缘膜的 SiCN 膜来代替 TEOS 膜 24a 和 24c。可以例如用下列方法来形成这种低介电常数绝缘膜。利用 CVD 方法，用三甲氧基硅烷和一氧化二氮（N_2O）能够形成 TMS 膜。它主要由 SiON 组成（主要由 SiON 组成的膜被称为“TMS 膜”）。 用三甲基硅烷能够形成

SiC膜，而用三甲基硅烷和氨气能够形成SiCN膜。另一种低介电常数膜可以被用来代替TEOS膜24a或24c。SiOF膜可以被用来代替SiOC膜24b。

然后，如图8所示，在TEOS膜24上，相继制作采用诸如芳香族聚合物材料之类的涂敷材料的低介电常数绝缘膜26b和TEOS膜26c作为绝缘膜。以相似于用来形成低介电常数绝缘膜22b和TEOS膜22c的方法来形成这些膜（26b，26c）。由于涂敷的膜被用作低介电常数绝缘膜，故能够整平衬底表面的不平整性。此外，低介电常数绝缘膜26b被夹在TEOS膜26c与24c之间，致使能够保持这些膜组成的叠层膜（26）的机械强度。在绝缘膜（26）和上述TEOS膜24c中，形成待要被第二层互连M2掩埋的布线沟槽HM2。

如图9所示，硬掩模MK被淀积在TEOS膜26c上，随之以用光刻和干法腐蚀方法从第二层互连形成区清除硬掩模MK。氮化硅膜之类可以被用作硬掩模MK。

如图10所示，在硬掩模MK上形成抗蚀剂膜R1。然后，用光刻方法，从第一层互连与第二层互连的连接区清除抗蚀剂膜R1。

用此抗蚀剂膜R1作为掩模，例如用干法腐蚀方法，清除绝缘膜26（26b和26c）与绝缘膜24中的TEOS膜24c和SiOC膜24b，以形成接触孔C2。TEOS膜24a于是留在第一层互连M1上，以便防止否则在稍后要进行的用来清除抗蚀剂的烧蚀时会出现的被暴露的铜的氧化，并防止铜在干法腐蚀时散射。但由于铜膜M1C被作为帽层导电膜的钨膜CM1覆盖，故不一定要使TEOS膜24留在第一层互连M1上。

如图11所示，在清除抗蚀剂膜R1之后，借助于例如用硬掩模MK作为掩模，用干法腐蚀方法清除绝缘膜26(26b和26c)和TEOS膜24c，形成布线沟槽HM2。此时，保留在接触孔C2底部上的TEOS膜24a也被清除。

此布线沟槽HM2的厚度约为0.25μm，而宽度约为0.18μm。接触孔C2离布线沟槽HM2底部的深度约为0.35μm。而其直径约为0.18μm。

此处，在制作接触孔C2之后形成布线沟槽HM2。作为变通，也可

以在形成布线沟槽 HM2 之后制作接触孔 C2，然后将抗蚀剂膜等掩埋在此沟槽中，以便整平衬底表面。

如图 12 所示，例如用干法腐蚀方法，清除从接触孔 C2 底部暴露的钨膜 CM1，以便暴露铜膜 M1c。虽然没有特别的限制，但可以借助于改变所使用的腐蚀气体种类而连续地进行布线沟槽HM2的制作以及用来清除钨膜 CM1 的干法腐蚀。

由于能够利用形成接触孔C2和布线沟槽HM2的步骤来清除从接触孔 C2 底部暴露的钨膜 CM1，故能够选择性地清除而无须增加步骤来制作另一个掩模。然后清除硬掩模MK。

然后，单独或组合利用下列处理来清除从接触孔底部暴露的铜膜M1c上的氧化物：在含氢或氨的气氛中热处理，将衬底表面暴露于含氢、氨、或者氢或氨之一与 Ar 之类的稀有气体的混合物中的任何一种的气氛中产生的等离子体，以及用 Ar 之类的稀有气体对衬底表面进行溅射腐蚀。然后，如图 13 所示，例如用低压长距离溅射方法，在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26 上淀积例如依次层叠有氮化钽（TaN）膜和钽（Ta）膜的阻挡膜 PM2a。可以用 CVD 方法，或用在铜膜 M1b 的制作步骤中具体描述了的离子化溅射方法，来制作阻挡膜 PM2a。如上所述，离子化溅射能够赋予被淀积的金属离子方向性。在成膜的后期，当淀积在布线沟槽上或接触孔底部的金属在大的偏压下被溅射腐蚀时，这样散射的金属能够被重新淀积在其侧壁上，从而能够改善侧壁和底部的台阶覆盖。

此处，布线沟槽 HM2 侧壁上阻挡膜 PM2a 的厚度被调节为大约 5nm，在布线沟槽 HM2 底部上为大约 30nm，在接触孔 C2 侧壁上为大约 3nm，而在接触孔 C2 底部上为大约 20nm。借助于控制布线沟槽 HM2 底部上的阻挡膜 PM2a 的厚度大于接触孔 C2 底部上的厚度，即使阻挡膜 PM2a 稍后从接触孔 C2 底部被溅射腐蚀清除，阻挡膜 PM2a 也能够留在布线沟槽 HM2 的底部上。而且，借助于在将起始成膜条件设定成允许高的各向异性（方向性）的情况下制作阻挡膜 PM2a，有可能防止布线沟槽 HM2 底部或侧壁上或接触孔 C2 侧壁上的阻挡膜 PM2a 过多地增厚。

如图 14 所示，从接触孔 C2 底部清除阻挡膜 PM2a，随之以在阻挡膜 PM2a 和暴露的铜膜 M1c 上形成铜膜 PM2b。可以例如用上述的离子化溅射方法来进行阻挡膜 PM2a 的清除和铜膜 PM2b 的形成。

当靶与衬底之间的距离被设定为大约 300mm 而衬底温度被调整为 25℃或更低时，借助于在起始阶段对衬底施加大的 DC 或 RF 偏压，接触孔 C2 底部上的阻挡膜 PM2a 被溅射腐蚀，从而将气氛中所含的铜离子和氩（Ar）注入到衬底表面。此时，这些离子基本上垂直入射到衬底，致使平面部分（布线沟槽 HM2 的底部和接触孔 C2 的底部）被择优腐蚀。如上所述，布线沟槽 HM2 底部上的阻挡膜 PM2a 被制作成比接触孔 C2 底部上的更厚，致使当清除接触孔 C2 底部上的阻挡膜 PM2a 时，有可能在布线沟槽 HM2 底部上留下阻挡膜 PM2a。

借助于适当地选择腐蚀条件，从而将被散射的阻挡膜 PM2a 重新淀积在布线沟槽 HM1 或接触孔 C2 的侧壁和底部上，能够改善这些侧壁或底部的台阶覆盖。借助于将已经在布线沟槽 HM2 或接触孔 C2 的侧壁的上部（角落）上淀积得很厚的阻挡膜 PM2a 重新淀积，还有可能匀平布线沟槽 HM2 或接触孔 C2 侧壁上的阻挡膜 PM2a 的厚度。

如图 15 所示，借助于减小偏压或停止施加偏压，在布线沟槽 HM2 和接触孔 C2 中淀积薄的铜膜 PM2b 作为电镀的籽晶膜。此时，如上所述，借助于在衬底上淀积一定厚度的铜膜之后将偏压提高到相对高的水平，有可能改善布线沟槽 HM2 或接触孔 C2 侧壁和底部上的铜膜 PM2b 的台阶覆盖。

结果，在布线沟槽 HM2 的侧壁和底部以及接触孔 C2 的侧壁上，通过阻挡膜 PM2a 形成铜膜 PM2b，而在从接触孔 C2 底部暴露的铜膜 M1c 上，铜膜 PM2b 被直接形成，其间不插入阻挡膜 PM2a。阻挡膜 PM2a 在布线沟槽 HM2 侧壁和底部上的厚度约为 5nm，在接触孔 C2 侧壁上约为 3nm，而铜膜 PM2b 的厚度约为 10nm。

若在一个装置中进行从接触孔 C2 底部清除阻挡膜 PM2a 以及形成布线沟槽 HM2 和接触孔 C2 内部的铜膜 PM2b，则能够防止阻挡膜 PM2a 的氧化或外来物质附着到其上，从而能够改善阻挡膜 PM2a 和铜膜 PM2b

的质量。在诸如偏压按需要被改变的条件下，当从接触孔 C2 底部清除阻挡膜 PM2a 时，也有可能在其它位置（布线沟槽 HM2 内部或接触孔 C2 侧壁上）形成铜膜 PM2b。

可以在分立的装置中进行从接触孔 C2 底部清除阻挡膜 PM2a 以及形成布线沟槽 HM2 和接触孔 C2 内部的铜膜 PM2b。例如，在用各向异性腐蚀方法从接触孔 C2 底部清除阻挡膜 PM2a 之后，可以用溅射方法形成布线沟槽 HM2 和接触孔 C2 内部的铜膜 PM2b。在此情况下，可以在含氢或氨的减压气氛中进行热处理或等离子体处理，或用诸如氢氟酸（HF）之类的清洗液进行清洗，以便清除被各向异性腐蚀暴露的阻挡膜 PM2a 和铜膜 M1c 表面上的氧化物或外来物质。

然后，利用电镀方法，用含硫酸铜的溶液作为电镀液，在铜膜 PM2b 上形成铜膜 PM2c。此铜膜 PM2c 被制作用以掩埋布线沟槽 HM2 和接触孔 C2。

在减压气氛中对衬底 1 进行退火（热处理）之后，用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而如图 16 所示形成各由铜膜 PM2b 和 PM2c 以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 与第二层互连的栓塞（连接部分）P2。此处，第二层互连 M2 意味着埋置在布线沟槽 HM2 中的铜膜 PM2b 和 PM2c 以及阻挡膜 PM2a，而栓塞 P2 意味着从布线沟槽 HM2 延伸的埋置在接触孔 C2 中的铜膜 PM2b 和 PM2c 以及阻挡膜 PM2a。

在减压气氛中，衬底 1 被进一步退火（热处理）。

如上所述，本实施方案由于清除了第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 和阻挡膜 PM2a，第一层互连 M1 因而与作为构成栓塞 P2 的主要金属的铜直接接触，从而减小了电阻。而且，本实施方案使得铜原子能够在第一层互连 M1 与栓塞 P2 之间运动，这就使得有可能减小第一层互连 M1 与栓塞 P2 之间界面处的空洞产生率，从而改善电迁移阻力。

具体地说，阻挡膜 PM2a 或钨膜 CM1 都不形成在接触孔 C2 的底部，亦即不形成在第一层互连 M1 与栓塞（连接部分）P2 之间的接合处。由于阻挡膜 PM2a 和钨膜 CM1 二者被从接触孔 C2 底部清除，故第一层互连

M1 与作为构成栓塞 P2 的主要金属的铜直接接触。在阻挡金属与铜之间不存在界面，致使能够防止栓塞附近由应力迁移造成的断路。

由于钨膜 CM1 和阻挡膜 PM2a 成一整体（这些膜不不连续地覆盖着铜膜），故其内部铜膜的整个表面被阻挡金属膜覆盖。粘附性比较低的铜与绝缘膜之间的界面可以从结构中消除，这就改善了铜表面上的粘附性。结果，能够抑制空洞的产生并能够改善电迁移阻力。

虽然钨膜 CM1 和阻挡膜 PM2a 都不存在于钨膜 CM1 与阻挡膜 PM2a 之间，但第一层互连 M1 与栓塞 P2 的其它部分被钨膜 CM1 或阻挡膜 PM2a 覆盖。这种结构使得有可能：1）防止构成待要埋置的导电膜的金属（在铜膜的情况下是铜）扩散进入绝缘膜，以及 2）防止导电膜由于氧化硅膜与导电膜接触而氧化。

由于铜在铜-阻挡膜界面上比在铜-氮化硅膜界面上更不容易扩散，故比之使用诸如氮化硅膜之类的绝缘膜作为帽层膜，采用钨膜作为帽层导电膜使得有可能改善电迁移阻力。

此外，由于诸如氮化硅膜之类的绝缘膜不被用作帽层导电膜，故能够减小存在于各个互连之间的绝缘膜的有效介电常数。结果，能够改善信号经由互连的传输速度，从而能够实现半导体器件的高速工作。氮化硅膜的介电常数约为 6-8，而 TEOS 膜的介电常数为 4。

第一层互连 M1 与栓塞 P2 被硬钨膜 CM1 或阻挡膜 PM2a 覆盖，能够防止应力迁移造成的互连断路。例如由于热处理时施加的热应力而出现这种应力。确切地说，在本实施方案中，由于采用了硬度低的低介电常数绝缘膜，故对第一层互连 M1 与栓塞 P2 的保护是有效的。

由于钨膜被用作帽层导电膜，故能够掩埋如果有的话出现在下方铜膜表面上的缺陷，导致互连可靠性和产品成品率的改善。铜膜表面上的缺陷是破裂、收缩或刮伤引起的。例如，用 CMP 抛光铜膜时就出现破裂或刮伤。热处理或铜膜埋置不充分也产生破裂或刮伤。

若这种缺陷在铜膜中或在铜膜与阻挡膜之间的界面处引起空隙，则互连电阻增大。这种空隙成为电迁移的起点，从而降低电迁移阻力。制作在这种空隙上的栓塞不可避免地要增大连接电阻。

另一方面，采用钨膜作为帽层导电膜，能够借助于在其中埋置钨膜而修复空隙，从而改善电迁移阻力、得到的半导体器件的可靠性、以及产品的成品率。

然后，如图 17 所示，借助于在第二层互连 M2 上选择性地生长或择优生长钨（W）而在第二层互连 M2（PM2c）上形成厚度约为 2-20nm 的钨膜 CM2。例如用下列条件下的 1.5 分钟的处理来形成这一钨膜 CM2：0.3 Torr（$0.3 \times 1.33322 \times 10^2$ Pa），衬底托设定温度为 460℃（实际衬底温度为 430℃），六氟化钨（WF_6）流速为 5scc，氢（H_2）流速为 500scc。

上述处理仅仅在第二层互连 M2 上引起钨的选择性生长或与 TEOS 膜 26c 上的生长相比的钨在第二层互连 M2 上的择优生长。在优先考虑钨的生长速率的情况下，上述处理在相对高的温度下进行，但此温度可以被设定为大约 300℃。

不仅可以采用钨作为帽层导电膜，而且可以采用 WN、WSiN、CoWP、CoWB、TiN、TiSiN、Ta、TaN 或 TaSiN 的单层膜或借助于层叠这些膜中的任何二个或更多个而得到的叠层膜（双层膜、三层膜等）作为帽层导电膜。

如上所述，可以在一个装置中（原位）进行紧临钨膜 CM2 形成之前的退火以及钨膜 CM2 的形成。

在形成钨膜 CM2 之前，例如借助于用诸如氢氟酸（HF）之类的清洗液进行清洗，或在 3000 Pa 的压力下，在流速为 500cm^3/min（sccm）的氢（H_2）气氛中处理 3 分钟，可以清除 CMP 之后衬底表面上的铜沾污。

可以利用上述铜清洗带来的剥离效应来清除已经生长在 TEOS 膜 26c 上的钨膜。在形成钨膜之后，借助于衬底表面的 CMP，也可以清除 TEOS 膜 26c 上的钨膜。以这种方式清除 TEOS 膜 26c 上的导电物质，能够防止各个互连之间的短路。

如图 18 所示，用 CVD 方法，在 TEOS 膜 26c 和钨膜 CM2 上相继淀积 TEOS 膜 28a、SiOC 膜 28b、以及另一个 TEOS 膜 28c。这些膜的制作方法相似于用来制作 TEOS 膜 24a 和 24c 以及 SiOC 膜 24b 的方法。在 TEOS 膜 28c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜

30b 和 TEOS 膜（未示出）作为绝缘膜。这些膜的制作方法相似于用来制作低介电常数绝缘膜 22b 和 TEOS 膜 22c 的方法。

在得到的 5 层绝缘膜中，以相似于用于布线沟槽 HM2 和接触孔 C2 的方法制作布线沟槽和接触孔。其制作步骤未示出。

以这种方式重复形成绝缘膜、布线沟槽、接触孔、阻挡膜、铜膜、以及钨膜，从而形成具有多层互连的半导体器件。

图 19 和 20 示出了 5 层互连（M1-M5）的一个例子。图 21-23 是图 19 和 20 所示半导体器件的局部平面图，其中图 19 对应于 A-A'剖面，而图 20 对应于 B-B'剖面。图 21 是平面图，清楚地示出了第一层互连 M1 至第五层互连 M5 的淀积。为了便于其理解，图 22 示出了第一层互连 M1 至第三层互连 M3 的淀积，而图 23 示出了第三层互连 M3 至第五层互连 M5 的淀积。

如图 19-23 所示，可以用相似于用于第二层互连 M2 及位于其下方的栓塞 2 的方法来形成第三层互连 M3 及位于其下方的栓塞 P3。

具体地说，在绝缘膜（28 和 30）中形成布线沟槽（HM3）和接触孔（C3）之后，阻挡膜（PM3a）和铜膜（PM3b 和 PM3c）被相继制作在包括布线沟槽（HM3）和接触孔（C3）内部的绝缘膜上。在接触孔 C3 中，形成栓塞 P3。

在制作接触孔（C3）时，形成在位于接触孔下方的互连的表面上的钨膜（CM2）被预先清除。在形成铜膜（PM3b）之前，从接触孔（C3）底部清除阻挡膜（PM3a）。也可以在形成铜膜（PM3b）时，从接触孔（C3）底部清除阻挡膜（PM3a）。

结果，可以获得如上所述的诸如降低互连（M3）与栓塞（P3）之间接触电阻以及改善电迁移阻力之类的效果。

如图 19 和 20 所示，第三层互连 M3 经由阻挡膜 PM4a 和钨膜 CM3，被连接到第四层互连 M4，而第四层互连 M4 经由阻挡膜 PM5a 和钨膜 CM4，被连接到第五层互连 M5。如图 21 和 23 所示，第三互连 M3 至第五互连 M5 中各个的宽度大，致使能够确保大的连接区（栓塞 4 或 5 的直径）。即使存在阻挡膜（PM4a，PM5a）和钨膜（CM3，CM4），也能够将接触电

阻抑制到比较小的水平。由于省略了从连接区清除这些膜的步骤，故能够简化步骤。构成第五层互连 M5 的阻挡膜 PM5a 是例如 TiN 膜、由 Ti 和 TiN 组成的双层膜、或由 Ti、TiN、Ti 组成的三层膜; PM5b 是铝（Al）或 Al 合金膜; 而其上的 PM5c 是 TiN 膜或由 Ti 和 TiN 组成的双层膜。在第五层互连 M5 上，由氧化硅膜和氮化硅膜组成的叠层膜 38 被形成作为保护膜。

如图 19 和 20 所示，第五层互连 M5 上的钨膜 CM5 可以被形成得比第四层互连 M4 上的钨膜 CM4 更薄。借助于将第五互连上的钨膜（第二帽层阻挡金属膜）调节成比第四层互连上的钨膜（第一帽层阻挡金属膜）更薄，能够减小与上层互连的连接电阻。借助于将下层钨膜制作得比上层钨膜更厚，能够保持可靠性裕度。

相反，关于第四层互连 M4 和第五层互连 M5 上的钨膜 CM4 和 CM5，钨膜 CM4 可以被制作得比钨膜 CM5 更薄。形成在上层互连上的接触孔的直径通常大，致使上层互连上的钨膜（第二帽层阻挡金属膜）的厚度增加不影响连接电阻。借助于在不影响连接电阻的范围内加厚上层互连上的钨膜，能够保持可靠性裕度。由于上层互连的布局规则不那么严格，故能够减小由于加厚钨膜而可能出现的短路可能性。减薄下层互连上的钨膜（第一帽层阻挡金属膜）使得有可能减小互连表面上的不平整性，从而减小各个互连之间短路的可能性。当待要层叠的层数增加时，这种不平整性就占主导。若互连表面变得显著地不规则，则可以用涂敷膜作为互连上的绝缘膜来整平。迄今描述了第四层互连 M4 和第五层互连 M5 上的钨膜 CM4 和 CM5，这同样适用于第三层互连 M3 和第四层互连 M4 上的钨膜 CM3 和 CM4，或第二层互连 M2 和第三层互连 M3 上的钨膜 CM2 和 CM3。

在形成叠层膜 38 之后，对衬底表面进行 NH_3 等离子体处理。这一处理引起: 1）构成形成在衬底上的互连（M1-M4）的铜膜的表面还原，2）铜膜表面氮化，3）形成在衬底上的诸如 TEOS 膜之类的绝缘膜表面清洗，4）绝缘膜表面损伤恢复，或 5）绝缘膜表面氮化。结果，能够抑制构成互连的铜的离子化。此外，能够防止铜离子在绝缘膜中扩散，从

而能够改善绝缘膜的特性。

（实施方案 2）

在本实施方案中，将描述其中待要形成布线沟槽和接触孔的绝缘膜的叠层结构的例子。

（1）在实施方案 1 中，布线沟槽 HM2 和接触孔 C2 制作在五层绝缘膜（24a、24b、24c、26b、26c）中（参见图 12），但这些膜中的 24a 可以被省略。图 24 是衬底的局部剖面图，示出了根据本发明实施方案 2 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤，相似于参照图 1-6 描述了的实施方案 1 的步骤，不再赘述。

然后，如图 24 所示，用 CVD 方法，在 TEOS 膜 22c 和钨膜 CM1 上，相继淀积 SiOC 膜 24b 和 TEOS 膜 24c 作为绝缘膜。在 TEOS 膜 24c 上，，相继形成采用诸如芳香族聚合物材料之类的涂敷材料的低介电常数绝缘膜 26b 和 TEOS 膜 26c 作为绝缘膜。这 4 个膜（24b、24c、26b、26c）的性质和形状如实施方案 1 详细所述。

在这这 4 个膜（24b、24c、26b、26c）中的 SiOC 膜 24b 中，制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2，同时在 TEOS 膜 24c、低介电常数绝缘膜 26b 和 TEOS 膜 26c 中制作布线沟槽 HM2。

如在实施方案 1 中那样，在 TEOS 膜 26 上形成第二层互连形成区中具有窗口的硬掩模（未示出），随之以形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜（未示出）。

用此抗蚀剂膜作为掩模，清除绝缘膜膜 26 和 24，以便形成接触孔 C2。在清除抗蚀剂膜之后，用硬掩模作为掩模，清除绝缘膜 26 和 TEOS 膜 24，以便形成布线沟槽 HM2。可以在形成布线沟槽 HM2 之后制作接触孔 C2。

例如用干法腐蚀方法清除从接触孔 C2 底部暴露的钨膜 CM1，以便暴露铜膜 M1c。

制作第二层互连 M2 和栓塞(连接部分)P2 的步骤以及之后的步骤，相似于实施方案 1 中的步骤，因此，下面仅仅描述其概况。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26 上形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，从接触孔 C2 底部清除阻挡膜 PM2a。在淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。

然后，如图 24 所示，用 CVD 方法在 TEOS 膜 26c 和钨膜 CM2 上相继淀积 SiOC 膜 28b 和 TEOS 膜 28c。这些膜相似于 SiOC 膜 24b 和 TEOS 膜 24c 被形成。在 TEOS 膜 28c 上，相继形成采用诸如芳香族聚合物材料之类的涂敷材料的低介电常数绝缘膜 30b 和 TEOS 膜（未示出）作为绝缘膜。这些膜的制作相似于低介电常数绝缘膜 22b 和 TEOS 膜 22c。

在上述的 4 层绝缘膜中，布线沟槽和接触孔的制作相似于布线沟槽 HM2 和接触孔 C2 的制作，但未示出此步骤。

根据本实施方案，布线沟槽 HM2 和接触孔 C2 制作在 4 层绝缘膜（24b、24c、26b、26c）中，致使其制作步骤比实施方案 1 更简单。

由于第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 和阻挡膜 PM2a 被清除，故能够减小第一层互连 M1 与栓塞 P2 之间的接触电阻，并能够改善电迁移阻力。于是可获得实施方案 1 所述的效果。

（2）在实施方案 1 中，布线沟槽 HM2 和接触孔 C2 制作在 5 层绝

的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，从接触孔 C2 底部清除阻挡膜 PM2a。在淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。

然后，如图 25 所示，用 CVD 方法，在低介电常数绝缘膜 26b 和钨膜 CM2 上相继淀积 TEOS 膜 28a、SiOC 膜 28b 和另一个 TEOS 膜 28c 作为绝缘膜。这些膜相似于 TEOS 膜 24a 和 24c 以及 SiOC 膜 24b 被形成。在 TEOS 膜 28c 上，用诸如芳香族聚合物材料之类的涂敷材料，形成低介电常数绝缘膜 30b 作为绝缘膜。此膜的制作相似于低介电常数绝缘膜 22b。

在上述 4 层绝缘膜中，以相似于用来制作布线沟槽 HM2 和接触孔 C2 的方法来制作布线沟槽和接触孔，但未示出此步骤。

根据本实施方案，布线沟槽 HM2 和接触孔 C2 制作在 4 层绝缘膜（24a、24b、24c、26b）中，致使其制作步骤比实施方案 1 更简单。其中要形成第一层互连的绝缘膜，可以由 TEOS 膜 22a 和低介电常数绝缘膜 22b 构成，而实施方案 1 所示的 TEOS 膜 22c 可以省略。图 25 示出了 22c 被省略的情况。

由于第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 和阻挡膜 PM2a 被清除，故能够减小第一层互连 M1 与栓塞 P2 之间的接触电阻，并能够改善电迁移阻力。于是可获得实施方案 1 所述的相似效果。

（实施方案 3）

缘膜（24a、24b、24c、26b、26c）中，但绝缘膜 26c 可以从这 5 个绝缘膜中省略。图 25 是衬底的局部剖面图，示出了根据本发明实施方案 2 的半导体器件的制造方法。

下面根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤，相似于上面参照图 1-6 在实施方案 1 中所述的步骤，故不再赘述。

如图 25 所示，用 CVD 方法，在衬底 1（第一层互连 M1）上相继淀积 TEOS 膜 24a、SiOC 膜 24b、另一个 TEOS 膜 24c 作为绝缘膜。然后，在 TEOS 膜 24c 上，用诸如芳香族聚合物材料之类的涂敷材料形成低介电常数绝缘膜 26b 作为绝缘膜。这 4 个膜（24a、24b、24c、26b）的性质和形状如实施方案 1 详细所述。

在这 4 个膜（24a、24b、24c、26b）中的 SiOC 膜 24b 和 TEOS 膜 24a 中，制作接触孔 C2，用来形成连接第一层互连 M1 与第二层互连 M2 的栓塞（连接部分）P2，同时在 TEOS 膜 24c 和低介电常数绝缘膜 26b 中，形成沟槽 HM2。

如在实施方案 1 中那样，在低介电常数绝缘膜 26b 上形成第二层互连形成区中具有窗口的硬掩模（未示出），随之以形成第一层互连与第二层互连的连接区中具有窗口的抗蚀剂膜（未示出）。

以此抗蚀剂膜作为掩模，清除低介电常数绝缘膜 26b、TEOS 膜 24c、SiOC 膜 24b，以形成接触孔 C2，随之以清除抗蚀剂膜。用硬掩模作为掩模，清除低介电常数绝缘膜 26b 和 TEOS 膜 24c，以形成布线沟槽 HM2，并从接触孔 C2 底部清除 TEOS 膜 24a。可以在制作布线沟槽 HM2 之后来形成接触孔 C2。

例如用干法腐蚀方法，清除从接触孔 C2 底部暴露的钨膜 CM1，以便暴露铜膜 M1c（第一层互连 M1）。

制作第二层互连 M2 和栓塞（连接部分）P2 的步骤以及之后的步骤，相似于实施方案 1 中的步骤，因此，下面仅仅描述其概况。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和接触孔 C2 内部的低介电常数绝缘膜 26b 上形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上

在实施方案 1 中，其中埋置第二层互连 M2 的布线沟槽 HM2 制作在绝缘膜 26 和 TEOS 膜 24c 中。此布线沟槽 HM2 可以制作在绝缘膜 26 中。图 26 是衬底的局部剖面图，示出了根据本发明实施方案 3 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤，相似于上面参照图 1-6 在实施方案 1 中所示的步骤，不再赘述。

如图 26 所示，用 CVD 方法，在 TEOS 膜 22c 和钨膜 CM1 上，相继淀积 TEOS 膜 24a、SiOC 膜 24b 和另一个 TEOS 膜 24c 作为绝缘膜。然后，在 TEOS 膜 24c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜 26b 和 TEOS 膜 26c 作为绝缘膜。这 5 个膜（24a、24b、24c、26b、26c）的性质和形状如实施方案 1 中详细所述。

在这 5 个膜（24a、24b、24c、26b、26c）中的 TEOS 膜 24a 和 24c 以及 SiOC 膜 24b 中，制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2，同时在低介电常数绝缘膜 26b 和 TEOS 膜 26c 中制作布线沟槽 HM2。

如在实施方案 1 中那样，在 TEOS 膜 26c 上形成第二层互连形成区中具有窗口的硬掩模（未示出），随之以在硬掩模上形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜（未示出）。

用此抗蚀剂膜作为掩模，清除绝缘膜 26（26b，26c）、TEOS 膜 24c 以及 SiOC 膜 24b，以便形成接触孔 C2，随之以清除抗蚀剂膜。用硬掩模作为掩模，清除绝缘膜 26（26b，26c），以便形成布线沟槽 HM2，并从接触孔 C2 底部清除 TEOS 膜 24a。可以在形成布线沟槽 HM2 之后制作接触孔 C2。

例如用干法腐蚀方法，清除从接触孔 C2 底部暴露的钨膜 CM1，以便暴露铜膜 M1c。

制作第二层互连 M2 和栓塞（连接部分）P2 的步骤以及之后的步骤，相似于实施方案 1 中的步骤，因此，下面仅仅描述其概况。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和接触孔 C2 内部的

TEOS 膜 26c 上形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，从接触孔 C2 底部清除阻挡膜 PM2a。在淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。

然后，如图 26 所示，用 CVD 方法，在 TEOS 膜 26c 和钨膜 CM2 上相继淀积 TEOS 28a、SiOC 膜 28b 和另一个 TEOS 膜 28c 作为绝缘膜。这些膜相似于 SiOC 膜 24b 以及 TEOS 膜 24a 和 24c 被形成。在 TEOS 膜 28c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜 30b 和 TEOS 膜（未示出）作为绝缘膜。这些膜的制作相似于低介电常数绝缘膜 22b 和 TEOS 膜 22c。

在上述的 5 层绝缘膜中，以相似于用于布线沟槽 HM2 和接触孔 C2 的方法制作布线沟槽和接触孔，但未示出此步骤。

于是能够在绝缘膜（26）中形成布线沟槽 HM2。

同样在此实施方案中，由于第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 和阻挡膜 PM2a 被清除，故能够减小第一层互连 M1 与栓塞 P2 之间的接触电阻，并能够改善电迁移阻力。于是可获得实施方案 1 所述的相似效果。

（实施方案 4）

在实施方案 2 中，借助于在互连 M1 和 M2 上形成钨膜 CM1 和 CM2，防止了构成互连的铜扩散进入绝缘膜中以及氧化硅膜与铜膜之间的接

触造成的氧化物的形成。借助于在这些钨膜上形成薄的氮化硅膜，可以加强对铜扩散或氧化的防止。图 27 是衬底的局部剖面图，示出了根据本发明实施方案 4 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤，相似于上面参照图 1-6 在实施方案 1 中所述的步骤，不再赘述。

如图 27 所示，用 CVD 方法，淀积氮化硅膜 401 作为铜扩散防止膜或抗氧化膜。此氮化硅膜被制作成厚度为 20nm 或以下，由于如实施方案具体所述那样，存在于各个互连之间的绝缘膜的有效介电常数借助于减薄而尽可能地减小，故氮化硅膜具有大的介电常数。

然后，在氮化硅膜 401 上，用 CVD 方法相继淀积 SiOC 膜 24b 和 TEOS 膜 24c 作为绝缘膜。在 TEOS 膜 24c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜 26b 和另一个 TEOS 膜 26c 作为绝缘膜。这 4 个膜（24b、24c、26b、26c）的性质和形状如实施方案 1 中详细所述。

在这 4 个膜（24b、24c、26b、26c）中的 SiOC 膜 24b 以及氮化硅膜 401 中，制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2，同时在 TEOS 膜 24c、低介电常数绝缘膜 26b、以及 TEOS 膜 26c 中，制作布线沟槽 HM2。

如在实施方案 1 中那样，在 TEOS 膜 26c 上形成第二层互连形成区中具有窗口的硬掩模（未示出），随之以形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜（未示出）。

用此抗蚀剂膜作为掩模，清除绝缘膜膜 26 和绝缘膜 24 中的 TEOS 膜 24c 和 SiOC 膜 24b，以便形成接触孔 C2。在清除抗蚀剂膜之后，用硬掩模作为掩模，清除绝缘膜 26（26b，26c）以及 TEOS 膜 24c，以便形成布线沟槽 HM2。可以在形成布线沟槽 HM2 之后制作接触孔 C2。

例如用干法腐蚀方法，清除从接触孔 C2 底部暴露的氮化硅膜 401 以及下方的钨膜 CM1，以便暴露铜膜 M1c。

制作第二层互连 M2 和栓塞（连接部分）P2 的步骤以及之后的步骤，相似于实施方案 1 中的步骤，因此，下面仅仅描述其概况。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26c 上形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，从接触孔 C2 底部清除阻挡膜 PM2a。在淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。然后，用 CVD 方法，在钨膜 CM2 上淀积氮化硅膜 402 作为铜扩散防止膜或抗氧化膜。此氮化硅膜被制作成厚度为 20nm 或以下。

然后，如图 27 所示，用 CVD 方法在氮化硅膜 402 上相继淀积 SiOC 膜 28b 和 TEOS 膜 28c 作为绝缘膜。这些膜相似于 SiOC 膜 24b 和 TEOS 膜 24c 被形成。在 TEOS 膜 28c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜 30b 和 TEOS 膜（未示出）作为绝缘膜。这些膜的制作相似于低介电常数绝缘膜 22b 和 TEOS 膜 22c。

在这些绝缘膜中，以相似于用于布线沟槽 HM2 和接触孔 C2 的方法，制作布线沟槽和接触孔，但未示出此步骤。

根据本实施方案，由于薄的氮化硅膜 401 和 402 被形成在钨膜 CM1 和 CM2 上，故能够加强对铜扩散或氧化的防止。借助于将这些氮化硅膜 401 和 402 的厚度调节为 20nm 或以下，能够减小存在于各个互连之间的绝缘膜的有效介电常数。

由于第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 和阻挡膜 PM2a 被清除，故能够减小第一层互连 M1 与栓塞 P2 之间的接触电阻，并能够改善

如在实施方案 1 中那样，在阻挡绝缘膜 502 上形成第二层互连形成区中具有窗口的硬掩模（未示出），随之以形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜（未示出）。

用此抗蚀剂膜作为掩模，清除绝缘膜膜 26（502，26b）、TEOS 膜 24c 以及 SiOC 膜 24b，以便形成接触孔 C2，随之以清除抗蚀剂膜。用硬掩模作为掩模，清除绝缘膜 26（502，26b）和 TEOS 膜 24c，以便形成布线沟槽 HM2，并从接触孔 C2 底部清除 TEOS 膜 24a。可以在形成布线沟槽 HM2 之后制作接触孔 C2。

然后，例如用干法腐蚀方法清除从接触孔 C2 底部暴露的钨膜 CM1，以便暴露铜膜 M1c。

制作第二层互连 M2 和栓塞(连接部分)P2 的步骤以及之后的步骤，相似于实施方案 1 中的步骤，因此，下面仅仅描述其概况。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和接触孔 C2 内部的诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜之类的阻挡膜 502 上，形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，从接触孔 C2 底部清除阻挡膜 PM2a。在淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。

然后，如图 28 所示，用 CVD 方法，在阻挡绝缘膜 502 和钨膜 CM2 上相继淀积 TEOS 膜 28a、SiOC 膜 28b、和 TEOS 膜 28c 作为绝缘膜。这

电迁移阻力。于是可获得实施方案 1 所述的相似效果。

（实施方案 5）

在实施方案 1 中，被互连 M1 和 M2 填充的最上面的绝缘膜是 TEOS 膜 22c 和 26c，可以用氮化硅膜代替。作为变通，可以采用介电常数低于氮化硅膜的作为阻挡绝缘膜的 TMS 膜、SiC 膜、或 SiCN 膜。可以用 CVD 方法，例如用三甲氧基硅烷和一氧化二氮（N_2O）来形成这种低介电常数绝缘膜。此膜主要由 SiON 组成（以下将此膜称为“TMS 膜”）。作为变通，可以用三乙基硅烷来形成 SiC 膜，或可以用三乙基硅烷和氨来形成 SiCN 膜。

总之，在实施方案 5 中，实施方案 1 中的 TEOS 膜 22c 和 26c 被诸如氮化硅膜、SiO 膜、TMS 膜、SiC 膜、或 SiCN 膜之类的阻挡绝缘膜 501 和 502 代替。

图 28 是衬底的局部剖面图，示出了根据本发明实施方案 5 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成氧化硅膜 20 和埋置在此膜中的栓塞 P1 的各个步骤，相似于上面参照图 1 在实施方案 1 中所述的步骤，不再赘述。

如图 28 所示，如在实施方案 1 中那样，在氧化硅膜 20 和栓塞 1 上形成 TEOS 膜 22a 作为绝缘膜。然后，借助于对 TEOS 膜 22a 进行涂敷，随之以热处理而形成低介电常数绝缘膜 22b。也可以用 CVD 方法来形成这一低介电常数绝缘膜。

在低介电常数绝缘膜 22b 上，形成诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、或 SiCN 膜之类的阻挡绝缘膜 501 作为铜扩散防止膜或抗氧化膜。

低介电常数绝缘膜 22b 被夹在用 CVD 方法形成的膜（22a 和 501）之间，以便保持其叠层膜的机械强度。在由 TEOS 膜 22a、低介电常数绝缘膜 22b、和诸如氮化硅膜之类的阻挡绝缘膜 501 组成的 3 层绝缘膜（22）中，制作布线沟槽 HM1。

用光刻和干法腐蚀方法，形成其中要形成第一层互连的绝缘膜 22

（22a、22b、501），从而形成布线沟槽 HM1。此布线沟槽 HM1 的厚度约为 0.25μm，而宽度为 0.18μm。

如在实施方案 1 中那样，例如用溅射方法，在包括布线沟槽 HM1 内部的绝缘膜 22 上，淀积阻挡膜 M1a，随之以用离子化溅射方法在阻挡膜 M1a 上形成薄的铜膜 M1b 作为电镀的籽晶膜。然后例如用电镀方法，在铜 M1b 上形成铜膜 M1c。此铜膜 M1c 被形成为埋置在布线沟槽 HM1 中。

在减压气氛中，对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM1 外面的铜膜 M1c 和 M1b 以及阻挡膜 M1a，从而形成由铜膜 M1c 和 M1b 以及阻挡膜 M1a 组成的第一层互连 M1。此时，在第一层互连 M1 形成区外面的区域中，诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜之类的阻挡膜 501 被暴露。然后，在减压气氛中对衬底 1 进行退火（热处理）。

如在实施方案 1 中那样，在第一层互连 M1 上进行钨（W）的选择性生长或择优生长作为帽层导电膜，从而在第一层互连 M1 上形成约 2-20nm 的钨膜 CM1。在形成钨膜 CM1 之前，可以进行清洗或氢处理。或者，可以在形成钨膜 CM1 之后进行清洗。

在诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜之类的阻挡绝缘膜 501 和钨膜 CM1 上，用 CVD 方法相继淀积 TEOS 膜 24a、SiOC 膜 24b、以及另一个 TEOS 膜 24c 作为绝缘膜。然后，在 TEOS 膜 24c 上，用芳香族聚合物材料形成低介电常数绝缘膜 26b 作为绝缘膜，随之以用相似于用来形成诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜之类的阻挡绝缘膜 501 的方法，形成诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜之类的阻挡绝缘膜 502。这些膜 24a、24b、24c、26b 的性质和形状如实施方案 1 中详细所述。

在这 5 个膜（24a、24b、24c、26b、502）中的 TEOS 膜 24a 和 SiOC 膜 24b 中，制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2，同时在 TEOS 膜 24c、低介电常数绝缘膜 26b 和氮化硅膜 502 中，制作布线沟槽 HM2。

些膜相似于 SiOC 膜 24b 以及 TEOS 膜 24a 和 24c 被形成。在 TEOS 膜 28c 上，相继形成使用芳香族聚合物材料的低介电常数绝缘膜 30b 以及氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜（未示出）作为绝缘膜。这些膜的制作相似于低介电常数绝缘膜 22b 或诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、或 SiCN 膜之类的阻挡绝缘膜 502。

在上述的 5 层绝缘膜中，以相似于用于布线沟槽 HM2 和接触孔 C2 的方法制作布线沟槽和接触孔，但未示出此步骤。

在此实施方案中，诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、SiOC 膜、SiOCN 膜、以及 SiCN 膜之类的阻挡绝缘膜 501 和 502 被用作其中要埋置互连 M1 和 M2 的最上层绝缘膜。这样，即使在制作接触孔 C2 时出现掩模不对准，致使接触孔 C2（栓塞 P2）的图形侵入第一层互连 M1，甚至达及氮化硅膜 501，此阻挡绝缘膜 501 也防止了来自构成栓塞 P2 的铜膜的铜扩散，而且能够防止由铜膜与氧化硅膜（低介电常数绝缘膜 22b）之间的接触造成的铜膜氧化。为了减小存在于各个互连之间的绝缘膜的有效介电常数，阻挡绝缘膜的厚度最好尽可能薄。

如图 28 所示，当为了提高互连的密度和集成度而将第一层互连 M1 的互连宽度和接触孔 C2 的直径设计成相等时，在第一层互连 M1 与接触孔 C2 之间就出现裕度范围造成的掩模不对准。即使发生这样的不对准，形成在接触孔 C2 底部上的阻挡绝缘膜 501 也能够防止铜从构成栓塞 P2 的铜膜经由接触孔 C2 底部向绝缘膜 22b 扩散。

如上所述，即使出现不对准，也能够在接触孔 C2 底部保持对铜扩散的阻挡性能，致使第一层互连 M1 的互连宽度和接触孔 C2 的直径能够被设计成相等，从而能够提高互连的密度和集成度而不损失互连可靠性。

由于第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 和阻挡膜 PM2a 被清除，故可获得实施方案 1 所述的诸如减小第一层互连 M1 与栓塞 P2 之间的接触电阻以及改善电迁移阻力之类的效果。

（实施方案 6）

以在接触孔底部留下不连续的钨膜。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26c 上，形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，在阻挡膜 PM2a 上淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。

然后，如图 29 所示，在 TEOS 膜 26c 和钨膜 CM2 上，淀积诸如 TEOS 膜 28a 的绝缘膜。

在作为第一层互连 M1 和栓塞（连接部分）P2 的连接部分的接触孔 C2 的底部上，阻挡膜 PM2a 未被从接触孔 C2 的底部清除。这意味着比之实施方案 1，能够减少制造步骤数目，因为仅仅需要从接触孔 C2 的底部清除铜膜 CM1 而从接触孔 C2 底部清除阻挡膜 PM2a 的步骤可以省略。

在此实施方案中，第一层互连 M1 与栓塞 P2 之间的钨膜 CM1 被清除，致使能够减小其间的接触电阻。由于第一层互连 M1 与栓塞 P2 之间存在阻挡膜 PM2a，故这一减少效应可能稍微小一些，但可获得诸如改善电迁移阻力之类的实施方案 1 所述的效果。可以利用其表面的腐蚀，在阻挡膜 PM2a 被减薄之后来淀积铜膜 PM2b。

图 37 描述了此实施方案 6 应用于为提高互连密度和集成度而将第一层互连 M1 的互连宽度和接触孔 C2 的直径设计成相等的情况的例子。如图 37 所示，当第一层互连 M1 的互连宽度和接触孔 C2 的直径被设计成相等时，在制作接触孔 C2 时出现掩模不对准，接触孔 C2 的图形被形

在实施方案 1 中，在从接触孔 C2 底部清除阻挡膜 PM2a 之后，制作了铜膜 PM2b 和 PM2c。阻挡膜 PM2a 可以留在第二层互连 M2 与栓塞 P2 之间而无须从接触孔 C2 底部清除。图 29 和 30 是衬底的局部剖面图，用来说明根据本发明实施方案 6 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤，相似于上面参照图 1-6 在实施方案 1 中所述的步骤，不再赘述。在图 29 中，氧化硅膜 20 中的栓塞 P1 被省略（这同样适用于图 30-32）。

如图 29 所示，用 CVD 方法，在衬底 1（钨膜 CM1）上相继淀积 TEOS 膜 24a、SiOC 膜 24b、以及另一个 TEOS 膜 24c 作为绝缘膜。然后，在 TEOS 膜 24c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜 26b 以及 TEOS 膜 26c 作为绝缘膜。这 5 个膜（24a、24b、24c、26b、26c）的性质或形状如实施方案 1 中详细所述。

在这 5 个膜（24a、24b、24c、26b、26c ）中的 SiOC 膜 24b 和 TEOS 膜 24a 中，制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2，同时在 TEOS 膜 24c 和 26c、以及低介电常数绝缘膜 26b 中，制作布线沟槽 HM2。

如在实施方案 1 中那样，在 TEOS 膜 26c 上形成第二层互连形成区中具有窗口的硬掩模（相似于图 9 所示的），随之以在硬掩模上形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜（相似于图 10 所示的）。

用此抗蚀剂膜作为掩模，清除 TEOS 膜 26c 中的 TEOS 膜 24c 和 24a 以及 SiOC 膜 24b、低介电常数绝缘膜膜 26b、以及绝缘膜 24，以便形成接触孔 C2（相似于图 10 中的）。在清除抗蚀剂膜之后，用硬掩模作为掩模，清除 TEOS 膜 26c 和 24c 以及低介电常数绝缘膜 26b，以便形成布线沟槽 HM2（相似于图 11 中的）。可以在形成布线沟槽 HM2 之后制作接触孔 C2。

例如用干法腐蚀方法，清除从接触孔 C2 底部暴露的钨膜 CM1，以便暴露铜膜 M1c（相似于图 12 中的）。可以完全地清除钨膜 CM1，或可

成为侵入第一层互连 M1，甚至延伸到低介电常数绝缘膜 22c。即使在这种情况下，由于阻挡膜 PM2a 被形成在接触孔 C2 侧壁和底部上，故也能够在接触孔 C2 底部上防止铜从构成栓塞 P2 的铜膜向绝缘膜 22c 扩散。而且能够防止由铜膜与氧化硅膜（TEOS 膜 22c）之间的接触造成的铜膜氧化。

这样，即使出现不对准，也能够在接触孔 C2 底部保持对铜扩散的阻挡性能，致使第一层互连 M1 的互连宽度和接触孔 C2 的直径能够被设计成相等，从而能够提高互连的密度和集成度而不损失互连可靠性。此外能够省略从接触孔 C2 底部清除阻挡膜 PM2a 的步骤，致使比之实施方案 1 能够减少制造步骤数目。

如图 30 所示，第一层互连 M1 与栓塞 P2 之间的阻挡膜 PM2a 可以被形成为不连续的膜。

在这种情况下，阻挡膜 PM2a 不被均匀地形成在接触孔 C2 的整个底部上，而是被局部地形成。这是一种不连续的膜，它允许铜膜 M1c 和 M1b 与铜膜 PM2b 和 PM2c 在未形成阻挡膜 PM2a 的部分处直接接触。

在作为第一层互连 M1 与栓塞（连接部分）P2 之间的连接的接触孔 C2 的底部上，用来防止铜扩散的阻挡材料被形成为不连续膜。

例如借助于在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26c 上形成阻挡膜 PM2a，同时控制成膜条件，使接触孔 C2 底部上的阻挡膜显著地薄，能够形成这种不连续的膜。

作为变通，可以用下列方法来形成这种不连续的膜。在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26c 上淀积阻挡膜 PM2a 到布线沟槽 HM2 侧壁上的厚度约为 5nm，布线沟槽 HM2 底部上的厚度约为 30nm，接触孔 C2 侧壁上的厚度约为 3nm，而接触孔 C2 底部上的厚度约为 20nm 之后，从接触孔 C2 底部清除阻挡膜 PM2a。在清除时，腐蚀条件被控制成不完全清除阻挡膜。

如上所述，若存在于第一层互连 M1 与栓塞 P2 之间的阻挡膜 PM2a 被形成为不连续的膜，则能够减小其间的接触电阻。此外，它使铜能够经由阻挡膜 PM2a 的不连续部分进行转移，从而可获得实施方案 1 所述

的诸如改善电迁移阻力之类的效果。

（实施方案 7）

在实施方案 1 中，在从接触孔 C2 底部清除钨膜 CM1 之后，制作了铜膜 PM2b 和 PM2c。作为变通，钨膜 CM1 可以留在第二层互连 M2 与栓塞 P2 之间而无须从接触孔 C2 底部清除。图 31 是衬底的局部剖面图，用来说明根据本发明实施方案 7 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤，相似于参照图 1-6 所述的实施方案 1 的步骤，不再赘述。

然后，如图 31 所示，用 CVD 方法，在衬底 1（钨膜 CM1）上相继淀积诸如 TEOS 膜 24a、SiOC 膜 24b、以及另一个 TEOS 膜 24c 之类的绝缘膜。在 TEOS 膜 24c 上，相继形成采用芳香族聚合物材料的低介电常数绝缘膜 26b 以及 TEOS 膜 26c 作为绝缘膜。这 5 个膜（24a、24b、24c、26b、26c）的性质或形状如实施方案 1 中详细所述。

在这 5 个膜（24a、24b、24c、26b、26c ）中的 SiOC 膜 24b 和 TEOS 膜 24a 中，制作接触孔 C2，用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞（连接部分）P2，同时在 TEOS 膜 24c 和 26c、以及低介电常数绝缘膜 26b 中，制作布线沟槽 HM2。

如在实施方案 1 中那样，在 TEOS 膜 26c 上形成第二层互连形成区中具有窗口的硬掩模（相似于图 9 中的），随之以形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜（相似于图 10 中的）。

用此抗蚀剂膜作为掩模，清除 TEOS 膜 26c、低介电常数绝缘膜膜 26b、TEOS 膜 24c 和 24a、以及 SiOC 膜 24b，以便形成接触孔 C2（相似于图 10 中的）。在清除抗蚀剂膜之后，用硬掩模作为掩模，清除 TEOS 膜 26c 和 24c 以及低介电常数绝缘膜 26b，以便形成布线沟槽 HM2。可以在形成布线沟槽 HM2 之后制作接触孔 C2（相似于图 11 中的）。然后清除硬掩模。接着形成第二层互连 M2 和栓塞（连接部分）P2，同时从接触孔 C2 底部暴露钨膜 CM1。形成第二层互连 M2 和栓塞 P2 的步骤以及之后的步骤相似于实施方案 1 中的步骤，故下面仅仅描述其概况。

如在实施方案 1 中那样，在包括布线沟槽 HM2 和从中暴露钨膜 CM1 的接触孔 C2 内部的 TEOS 膜 26c 上，形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm，布线沟槽 HM2 底部上的厚度被淀积为大约 30nm，接触孔 C2 侧壁上的厚度被淀积为大约 3nm，而接触孔 C2 底部上的厚度被淀积为大约 20nm。

如在实施方案 1 中那样，从接触孔 C2 底部清除阻挡膜 PM2a。在淀积薄的铜膜 PM2b 作为电镀籽晶膜之后，用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火（热处理），随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a，从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞（连接部分）P2。

如在实施方案 1 中那样，在第二层互连 M2 上进行钨（W）的选择性生长或择优生长，从而形成钨膜 CM2。

然后，如图 31 所示，在 TEOS 膜 26c 和钨膜 CM2 上，淀积 TEOS 膜 28a 作为绝缘膜。

在此实施方案中，第一层互连 M1 与栓塞 P2 之间的阻挡膜 PM2a 被清除。致使能够减小其间的接触电阻。由于第一层互连 M1 与栓塞 P2 之间存在钨膜 CM1，故这一减少效应可能稍微小一些，但可获得实施方案 1 所述的诸如电迁移阻力改善的效果。

在作为第一层互连 M1 和栓塞（连接部分）P2 的连接部分的接触孔 C2 的底部上，存在着钨膜 CM1，但阻挡膜 PM2a 未被形成在接触孔 C2 的底部上。这意味着比之实施方案 1，能够减少制造步骤数目，因为仅仅需要从接触孔 C2 的底部清除阻挡膜 PM2a，而从接触孔 C2 底部清除铜膜 CM1 的步骤可以省略。

图 38 描述了此实施方案 7 应用于为提高互连密度和集成度而将第一层互连 M1 的互连宽度和接触孔 C2 的直径设计成相等的情况的例子。如图 38 所示，绝缘膜 22 的组成相似于实施方案 5 的。具体地说，如图 38 所示，在氧化硅膜 20 和栓塞 P1 上形成诸如实施方案 5 中那样的 TEOS