

膜 22a 之类的绝缘膜之后,借助于涂敷到 TEOS 膜 22a 上,随之以热处理,形成低介电常数绝缘膜 22b。作为变通,可以用 CVD 方法来形成此低介电常数绝缘膜。

然后,用 CVD 方法,在低介电常数绝缘膜 22b 上,形成诸如氮化硅膜、SiON 膜、TMS 膜、SiC 膜、或 SiCN 膜之类的阻挡绝缘膜 501 作为铜扩散防止膜或抗氧化膜。

上述步骤及其以后的步骤相似于上面参照图 31 所述的实施方案 7 的步骤,故不再赘述。

在此实施方案中,阻挡绝缘膜 501 被用作其中要埋置互连 M1 的最上层绝缘膜。这样,即使在制作接触孔 C2 时出现掩模不对准且接触孔 C2 的图形侵入第一层互连 M1,甚至达及阻挡绝缘膜 501,接触孔 C2 底部上的这一阻挡绝缘膜 501 也能够防止铜从构成栓塞 P2 的铜膜向绝缘膜 22b 扩散,而且能够防止由铜膜与氧化硅膜(低介电常数绝缘膜 22b)之间的接触造成的铜膜氧化。为了减小存在于各个互连之间的绝缘膜的有效介电常数,阻挡绝缘膜的厚度最好尽可能薄。

这样,即使出现不对准,也能够接触孔 C2 的底部上保持对铜扩散的阻挡性能,致使第一层互连 M1 的互连宽度和接触孔 C2 的直径能够被设计成相等,从而能够提高互连的密度和集成度而不损失互连可靠性。此外能够省略从接触孔 C2 底部清除钨膜 CM1 的步骤,致使比之实施方案 1 能够减少制造步骤数目。

(实施方案 8)

在实施方案 1 中,在互连 M1 和 M2 上形成单层钨膜 CM1 和 CM2 作为帽层导电膜。此帽层导电膜可以由叠层膜代替。图 32 是衬底的局部剖面图,用来说明根据本发明实施方案 8 的半导体器件的制造方法。

下面将根据其制造方法来描述本发明这一实施方案的半导体器件。直至形成第一层互连 M1 及其上的钨膜 CM1 的各个步骤,相似于上面参照图 1-6 在实施方案 1 中所述的步骤,不再赘述。

然后,如图 32 所示,借助于在氮气气氛中进行处理,钨膜 CM1 被转变为氮化钨膜 CM1a,随之以如实施方案 1 那样在氮化钨膜 CM1a 上选

择性生长或择优生长钨(W),从而形成钨膜 CM1b。得到的氮化钨膜 CM1a 和钨膜 CM1b 构成帽层导电膜 801。

用 CVD 方法,在衬底(钨膜 CM1b)上相继淀积 TEOS 膜 24a、SiOC 膜 24b、以及另一个 TEOS 膜 24c 作为绝缘膜。然后在 TEOS 膜 24c 上,
5 相继形成采用芳香族聚合物材料的低介电常数绝缘膜 26b 以及 TEOS 膜 26c 作为绝缘膜。这 5 个膜(24a、24b、24c、26b、26c)的性质或形状如实施方案 1 中详细所述。

在这 5 个膜(24a、24b、24c、26b、26c)中的 SiOC 膜 24b 和 TEOS 膜 24a 中,制作接触孔 C2,用来形成连接第一层互连 M1 和第二层互连 M2 的栓塞(连接部分)P2,同时在 TEOS 膜 24c 和 26c、以及低介
10 电常数绝缘膜 26b 中,制作布线沟槽 HM2。

如在实施方案 1 中那样,在 TEOS 膜 26c 上形成第二层互连形成区中具有窗口的硬掩模(未示出),随之以在硬掩模上形成第一层互连与第二层互连连接区中具有窗口的抗蚀剂膜(未示出)。

用此抗蚀剂膜作为掩模,清除 TEOS 膜 26c、低介电常数绝缘膜膜 26b、TEOS 膜 24c 和 24a、以及 SiOC 膜 24b,以便形成接触孔 C2。在清除抗蚀剂膜之后,用硬掩模作为掩模,清除 TEOS 膜 26c 和 24c 以及低介电常数绝缘膜 26b,从而形成布线沟槽 HM2。可以在形成布线沟槽 HM2 之后制作接触孔 C2。
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例如用干法腐蚀方法,清除从接触孔 C2 底部暴露钨膜 CM1b 以及位于其下方的氮化钨膜 CM1a,以便暴露铜膜 M1c。
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形成第二层互连 M2 和栓塞(连接部分)P2 的步骤以及之后的步骤相似于实施方案 1 中的步骤,故下面仅仅描述其概况。

如在实施方案 1 中那样,在包括布线沟槽 HM2 和接触孔 C2 内部的 TEOS 膜 26c 上,形成阻挡膜 PM2a。它在布线沟槽 HM2 侧壁上的厚度被淀积为大约 5nm,布线沟槽 HM2 底部上的厚度被淀积为大约 30nm,接触孔 C2 侧壁上的厚度被淀积为大约 3nm,而接触孔 C2 底部上的厚度被淀积为大约 20nm。
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如在实施方案 1 中那样,从接触孔 C2 底部清除阻挡膜 PM2a。在淀

积薄的铜膜 PM2b 作为电镀籽晶膜之后,用电镀方法在铜膜 PM2b 上形成铜膜 PM2c。在减压气氛中对衬底 1 进行退火(热处理),随之以用 CMP 或回腐蚀方法清除布线沟槽 HM2 和接触孔 C2 外面的铜膜 PM2c 和 PM2b 以及阻挡膜 PM2a,从而形成各由铜膜 PM2b、PM2c、以及阻挡膜 PM2a 组成的第二层互连 M2 以及用来连接第一层互连 M1 和第二层互连的栓塞(连接部分) P2。

如在实施方案 1 中那样,用相似于用来形成氮化钨膜 CM1a 和钨膜 CM1b 的方法,在第二层互连 M2 上形成氮化钨膜 CM2 和钨膜 CM2b。

然后,如图 32 所示,用 CVD 方法,在 TEOS 膜 26c 和钨膜 CM2b 上,相继淀积 TEOS 膜 28a、SiOC 膜 28b、以及 TEOS 膜 28c 作为绝缘膜。在 TEOS 膜 28c 上,相继形成采用芳香族聚合物材料的低介电常数绝缘膜 30b 以及 TEOS (未示出) 作为绝缘膜。

在上述 5 层绝缘膜中,用相似于用来制作布线沟槽 HM2 和接触孔 C2 的方法,制作布线沟槽和接触孔,但未示出此步骤。

以上述方式,互连上的帽层导电膜 801 和 802 可以被制作成叠层膜。

同样,在此实施方案中,由于第一层互连 M1 与栓塞 P2 之间的钨膜 CM1a、钨膜 CM1b、以及阻挡膜 PM2a 被清除,故能够减小其间的接触电阻。此外,可获得实施方案 1 所述的诸如电迁移阻力改善的效果。

(实施方案 9)

在实施方案 1 中,接触孔的直径被制作成基本上等于位于其下方的互连的宽度。接触孔下方的互连的宽度可以被制作成大于接触孔的直径,或可以在互连中局部安排直径大于接触孔的连接区。

例如,如图 22 所示,在实施方案 1 中,接触孔(例如 C2)的直径几乎等于其下方的互连的宽度(例如 M1 的宽度)。图 33 示出了第一层互连 M1、第二层互连 M2、以及用来连接它们的栓塞 P2 的图形。图 34 是沿图 33 中 C-C'线的剖面图。如图 34 所示,阻挡膜 PM2a 被形成在其中要制作栓塞 P2 的接触孔(C2)和其中要形成第二层互连的布线沟槽(HM2)的侧壁或底部上。虽然在图 34 的剖面中未示出,但钨膜 CM1 被

形成在第一层互连 M1 的表面上作为帽层导电膜。栓塞 P2 与互连 M1 之间的阻挡膜 PM2a 和钨膜 CM1 被清除,致使能够减小其间的接触电阻,并可获得实施方案 1 所述的诸如改善电迁移阻力的效果。

如图 35 所示,连接区 M901 可以被排列在第一层互连 M1 的末端。
5 此连接区 M901 被制作成宽度大于第一层互连 M1。连接区 M902 被排列在第二层互连 M2 的末端处。图 35 示出了第一层互连 M1、第二层互连 M2、以及用来连接它们的栓塞 P2 的图形。图 36 是沿图 35 中 C-C'线的剖面图。如图 36 所示,阻挡膜 PM2a 被形成在其中要制作栓塞 P2 的接触孔 (C2) 和其中要形成第二层互连的布线沟槽 (HM2) 的侧壁或底部
10 上。钨膜 CM1 被形成在第一层互连 M1 的表面上作为帽层导电膜。在连接区 M901 的外围表面上,钨膜 CM1 仍然作为帽层导电膜。

同样在此情况下,栓塞 P2 与互连 M1 之间的阻挡膜 PM2a 和钨膜 CM1 被清除,致使能够减小其间的接触电阻,并可获得实施方案 1 所述的诸如改善电迁移阻力的效果。

15 于是,当在互连中排列宽的连接区 M901 和 M902 时,就能够保持栓塞或待要形成在其上的互连图形的对准裕度。

至此就根据各个实施方案详细描述了本发明人提出的本发明。但应该记住的是,本发明不局限于此即不受此限制。在不超越本发明范围的程度内可以被修正。

20 确切地说,在实施方案 1-9 中,用双重镶嵌方法形成了第二层互连 M2 和连接部分 (栓塞) P2。也可以用单一镶嵌方法在分立的各个步骤中加以形成。在此情况下,借助于清除位于栓塞 P2 下方的第一层互连 M1 表面上的帽层导电膜以及栓塞 P2 底部上的阻挡膜,能够减小接触电阻,并能够改善电迁移阻力。

25 实施方案 5 所示的具有阻挡绝缘膜 501 的绝缘膜 22,可以被应用于实施方案 2-4 和 6-9。即使出现不对准,也能够在接触孔 C2 的底部上保持对铜扩散的阻挡性能,使得有可能将第一层互连 M1 的宽度设计成等于接触孔 C2 的直径,从而提高互连的密度和集成度,同时保持互连的可靠性。

实施方案 2-4 所示的绝缘膜 22、24、26，可以被应用于实施方案 6-9。

在实施方案 1 等之中，MISFET Qn 被作为半导体元件的例子，但不仅可以制作 MISFET，还可以制作诸如双极晶体管之类的其它元件。

5 在实施方案 6 中，阻挡膜 PM2a 被公开为阻挡材料，在作为第一层互连 M1 与栓塞（连接部分）P2 之间的连接部分的接触孔的底部上形成不连续的膜。不仅可以由上述阻挡膜 PM2a，而且还可以由钨膜 CM1 或阻挡膜 PM2a 与钨膜 CM1 二者，来形成不连续的阻挡材料膜。

在实施方案 1 等之中，利用涂敷型材料来获得层间绝缘膜的整平，
10 但也可以用 CMP 来代替。在实施方案 1 等之中，在加工沟槽时，利用了层叠的各个层间绝缘膜的腐蚀选择性比率之间的差别。作为变通，借助于控制干法腐蚀时间或监视腐蚀深度，可以在达及层间绝缘膜底部之前终止沟槽加工。

下面简要描述一下从本说明书公开的本发明的典型发明可获得的
15 优点。

在具有其表面上有帽层阻挡金属膜的布线部分和其上形成的连接部分并具有作为其外围的被阻挡金属膜覆盖的导体层的半导体器件中，阻挡金属层或帽层阻挡金属膜中的至少一个，从布线部分与连接部分之间的连接处被清除，致使能够减小其间的接触电阻。此外，能够降低电
20 迁移造成的空洞或断路的产生率。而且能够改善半导体器件的特性。

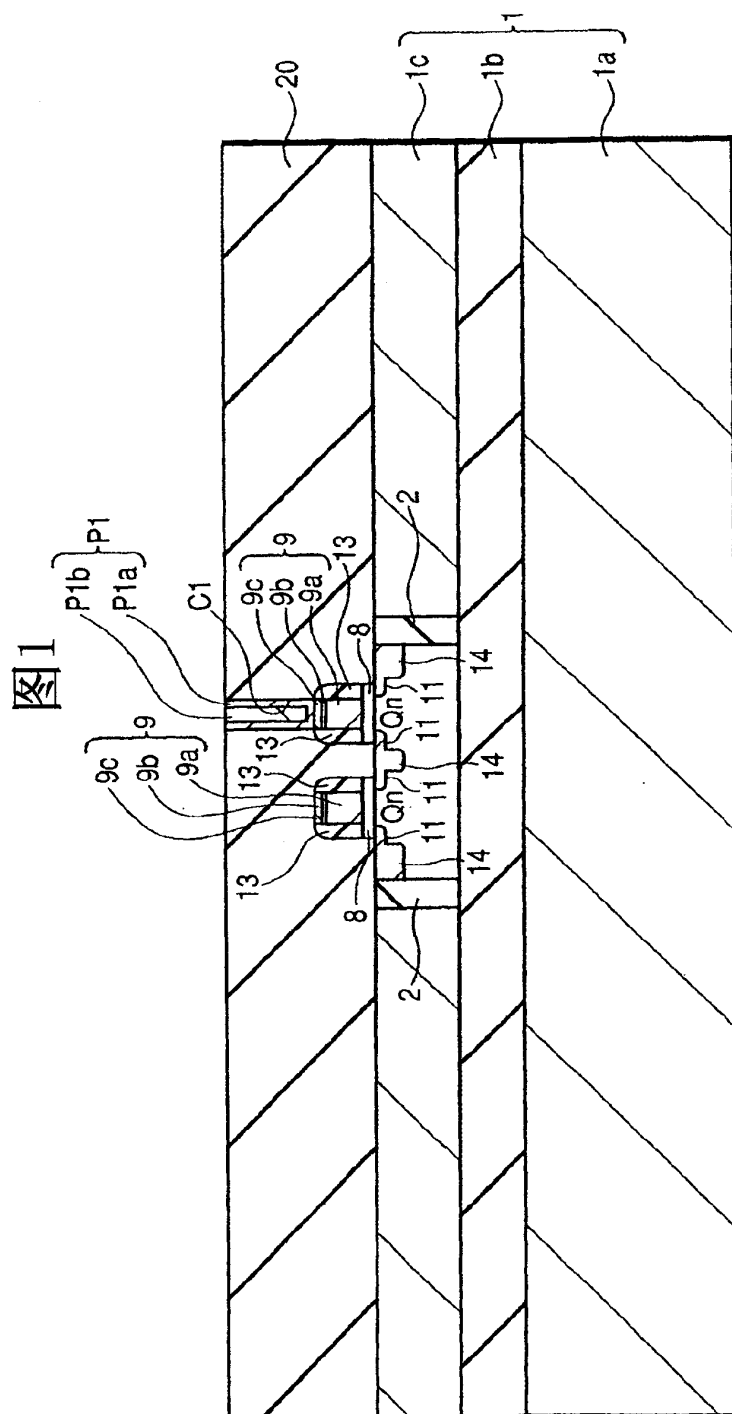


图4

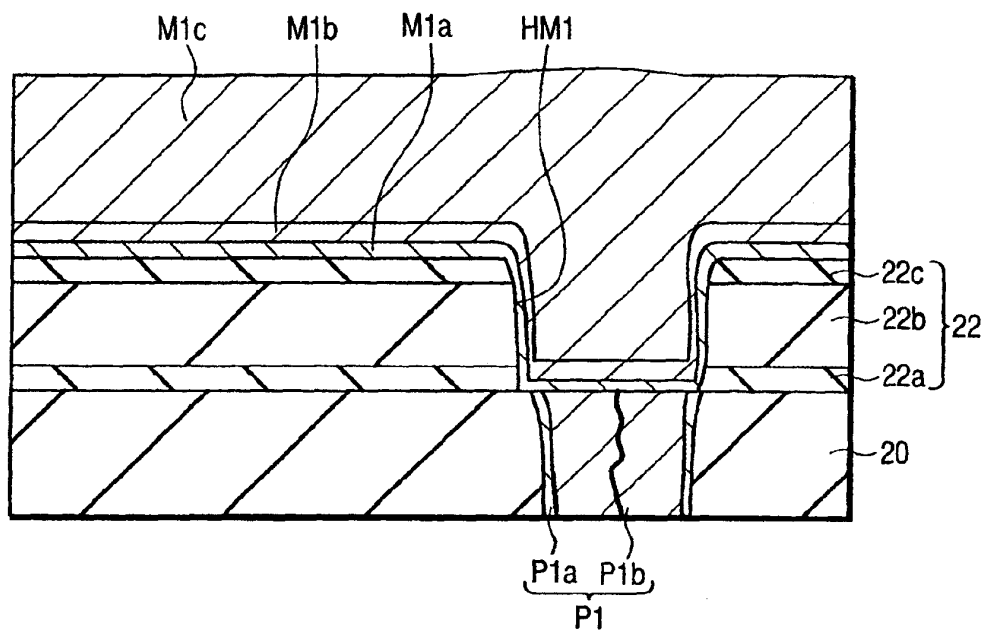


图5

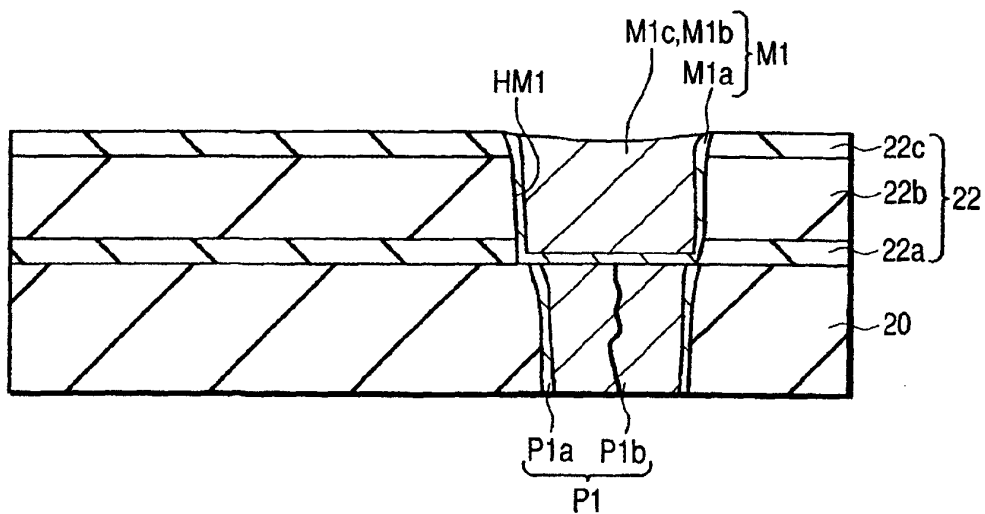


图2

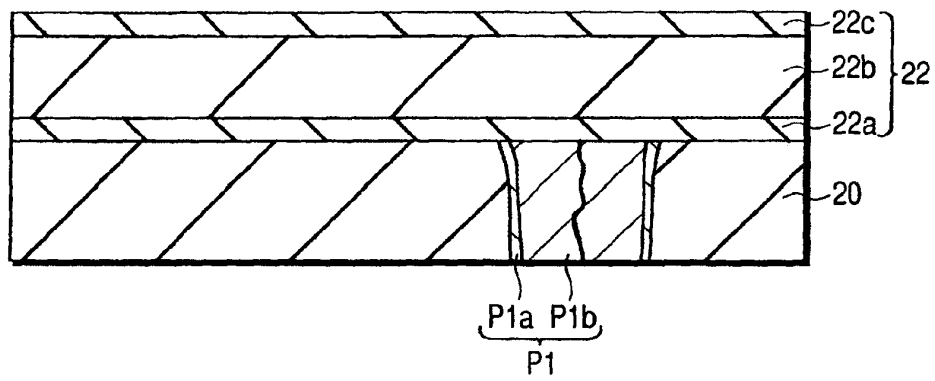


图3

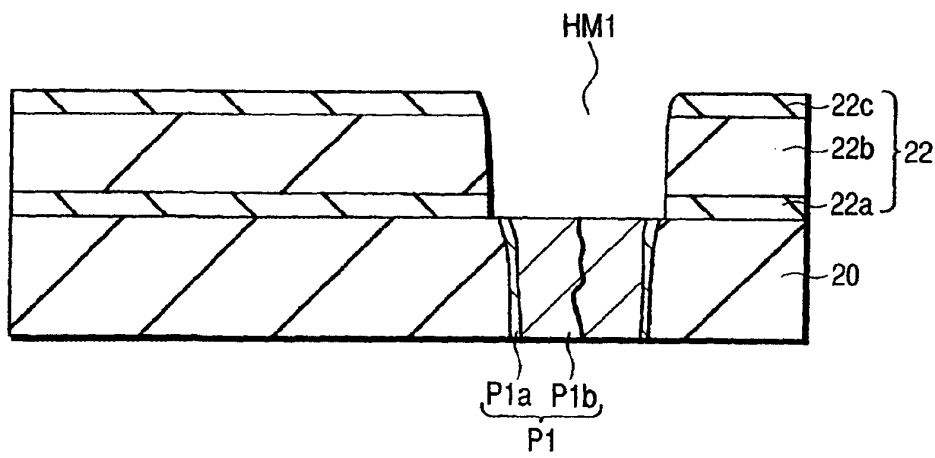


图6

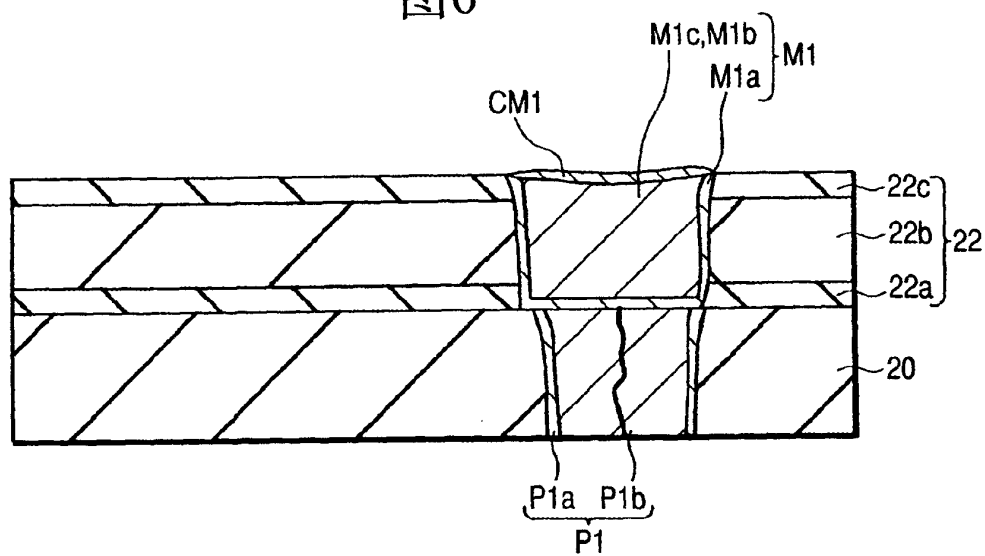


图7

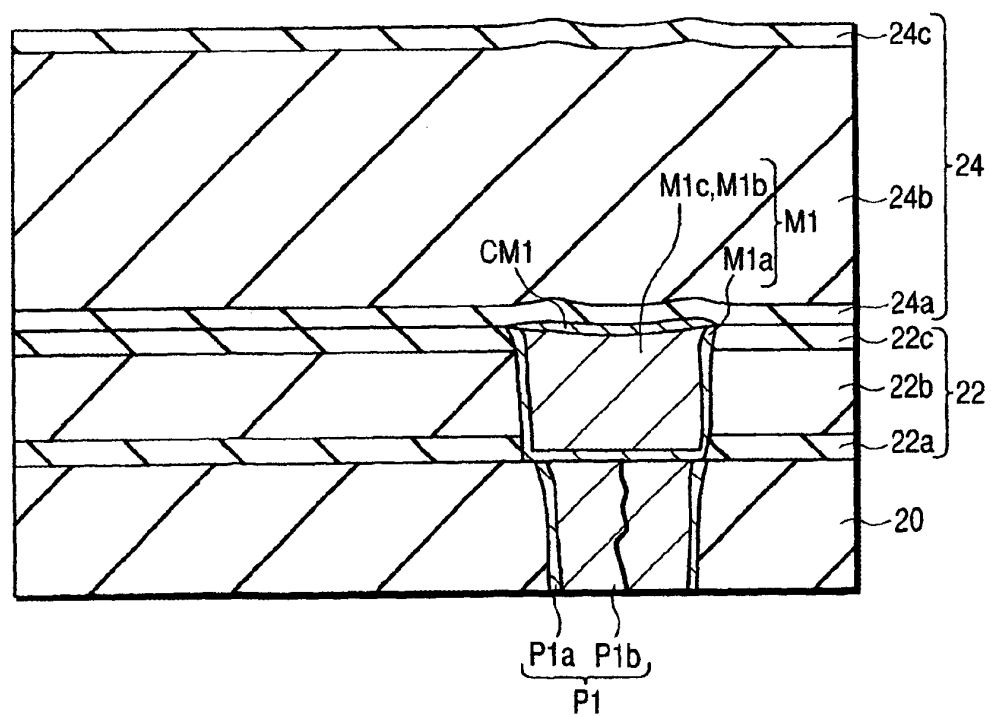


图8

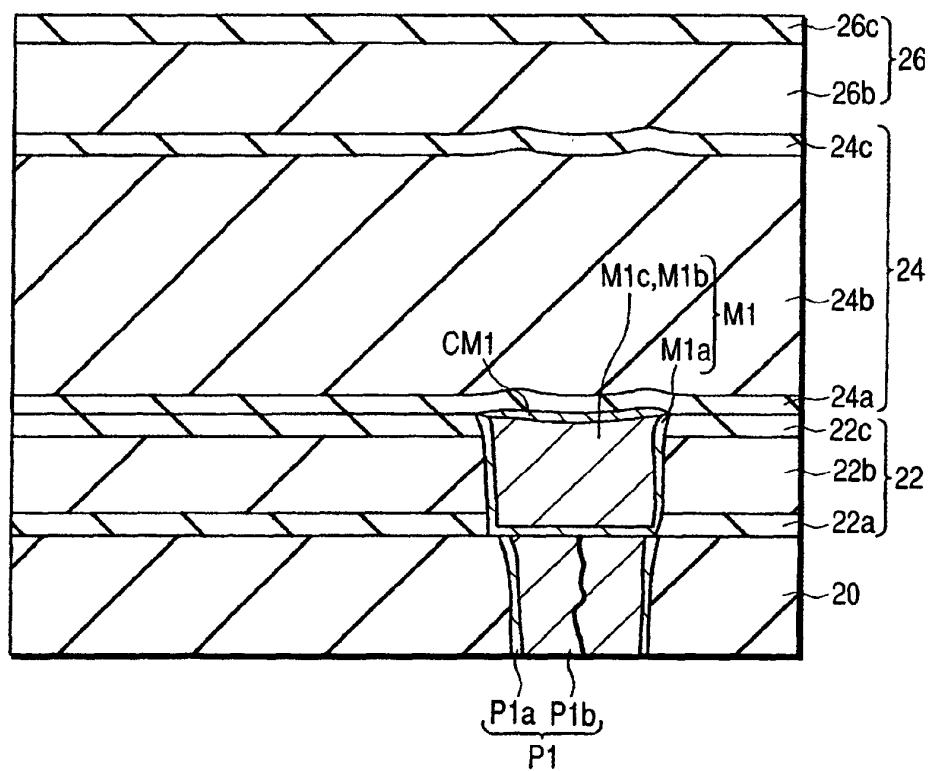


图9

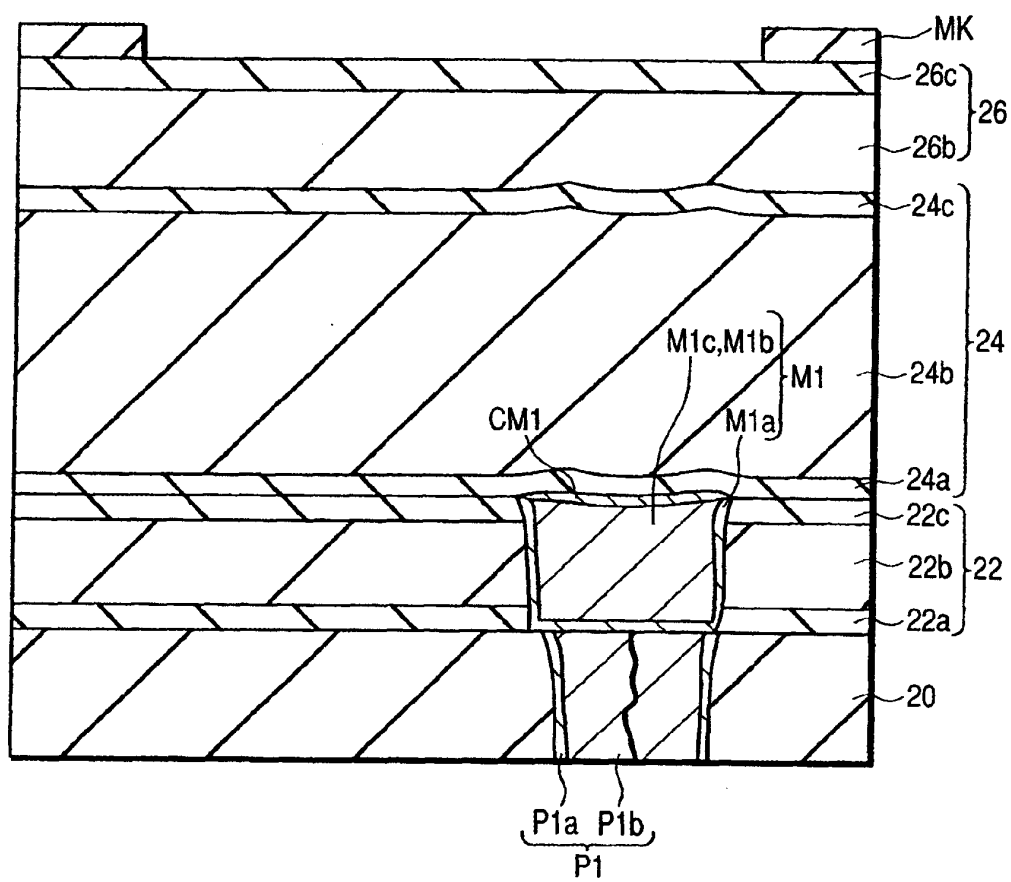


图12

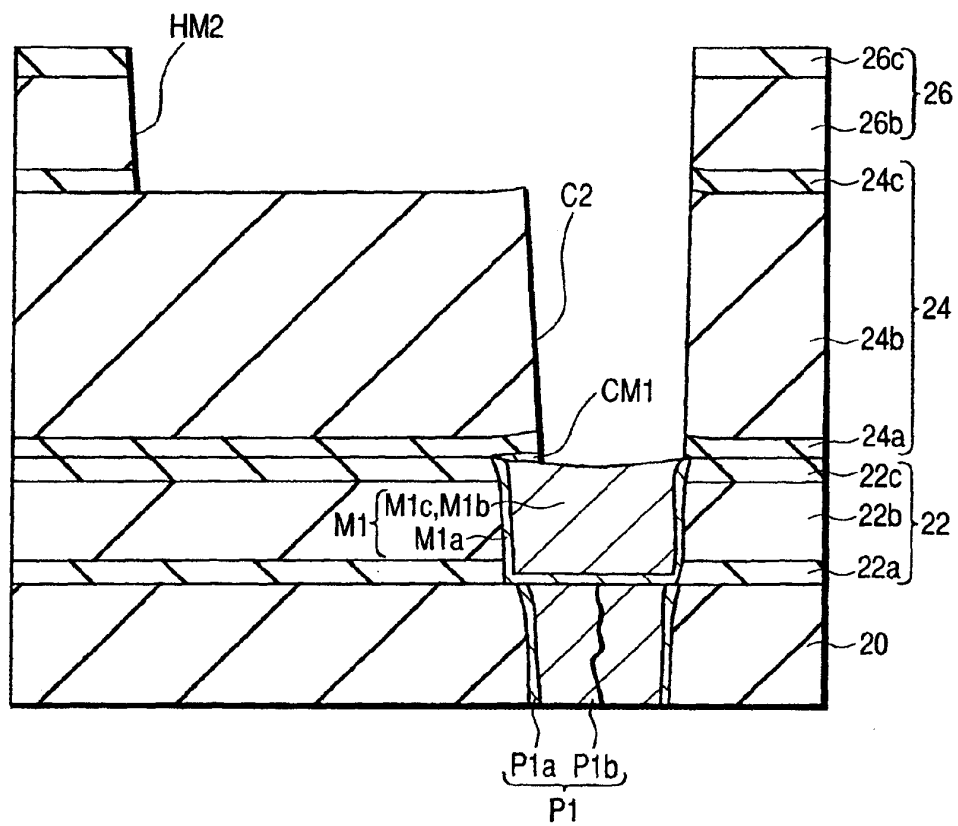


图 11

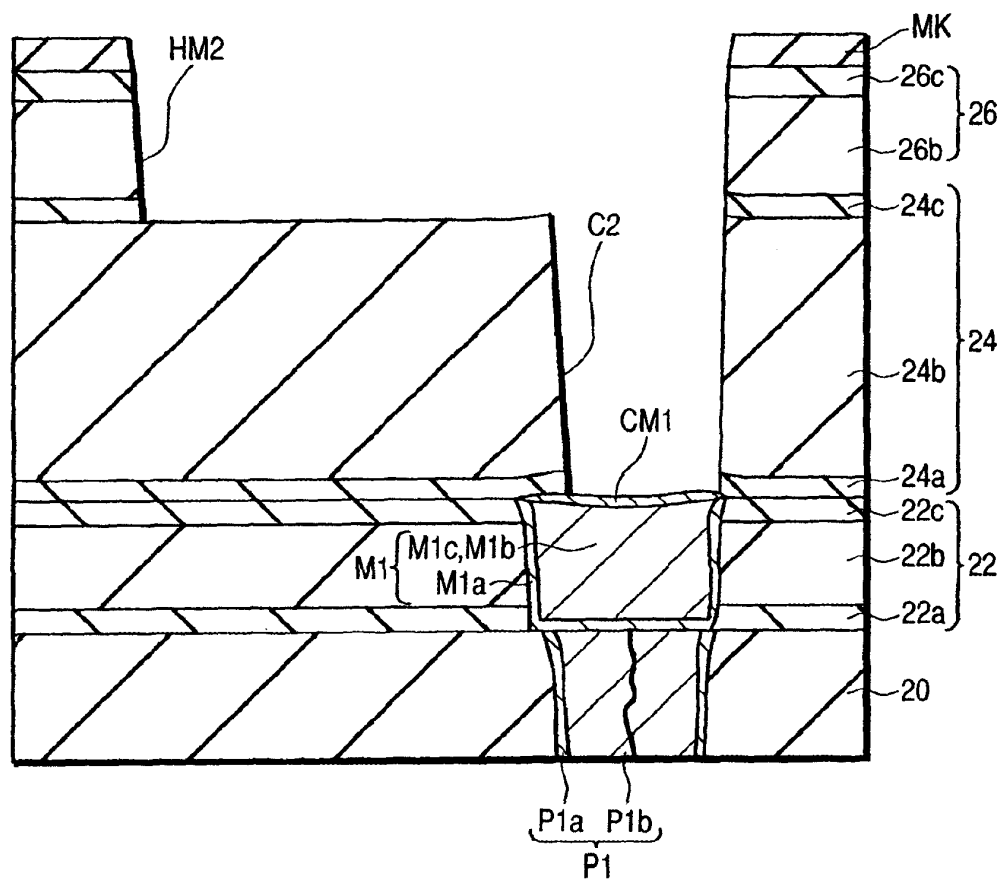


图 13

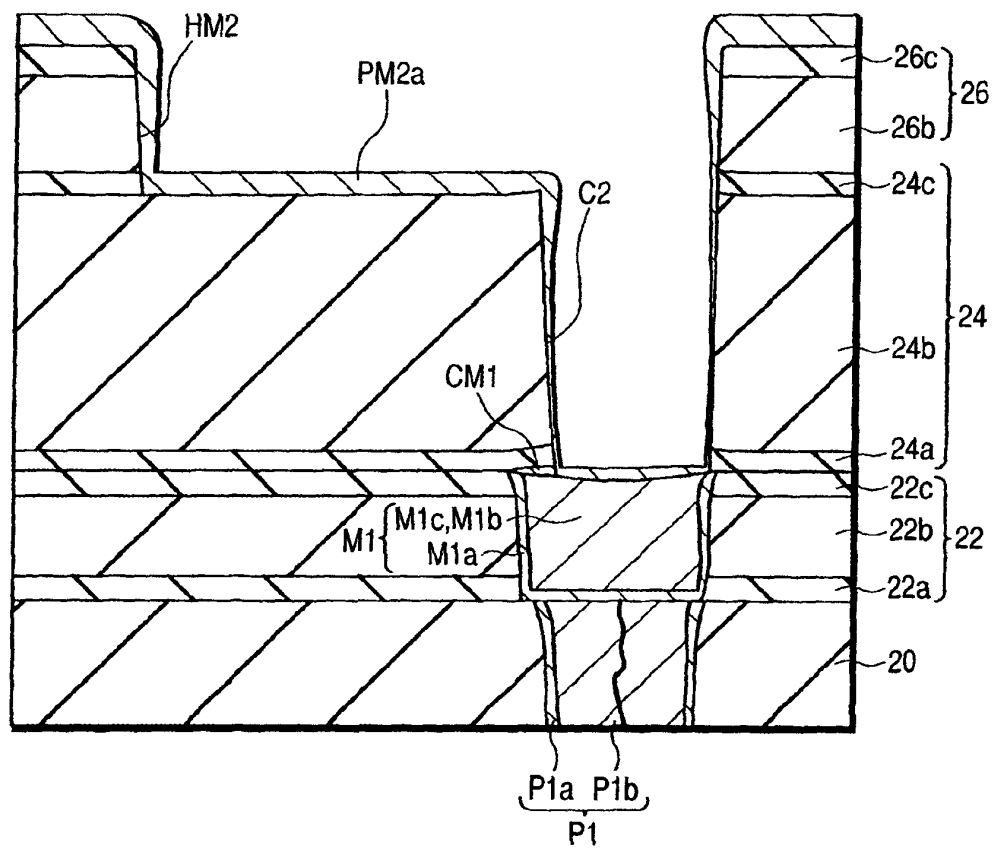


图14

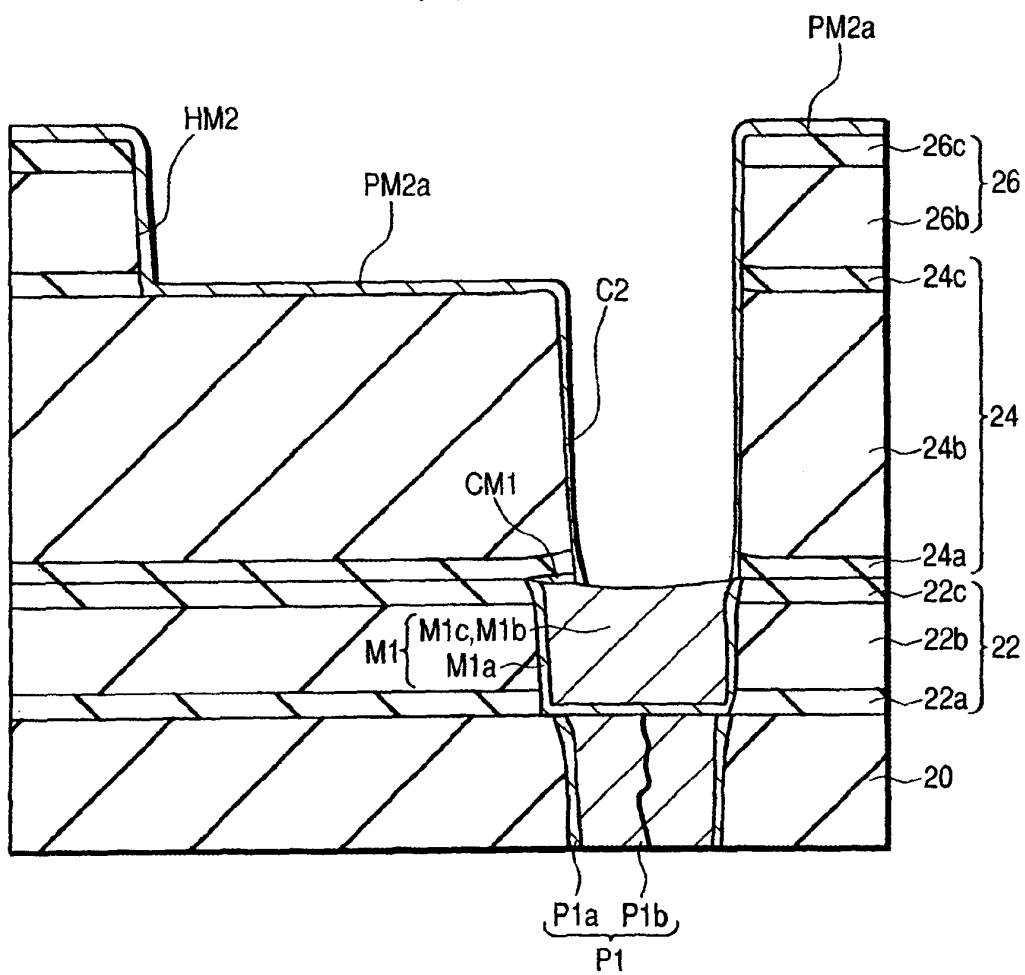


图15

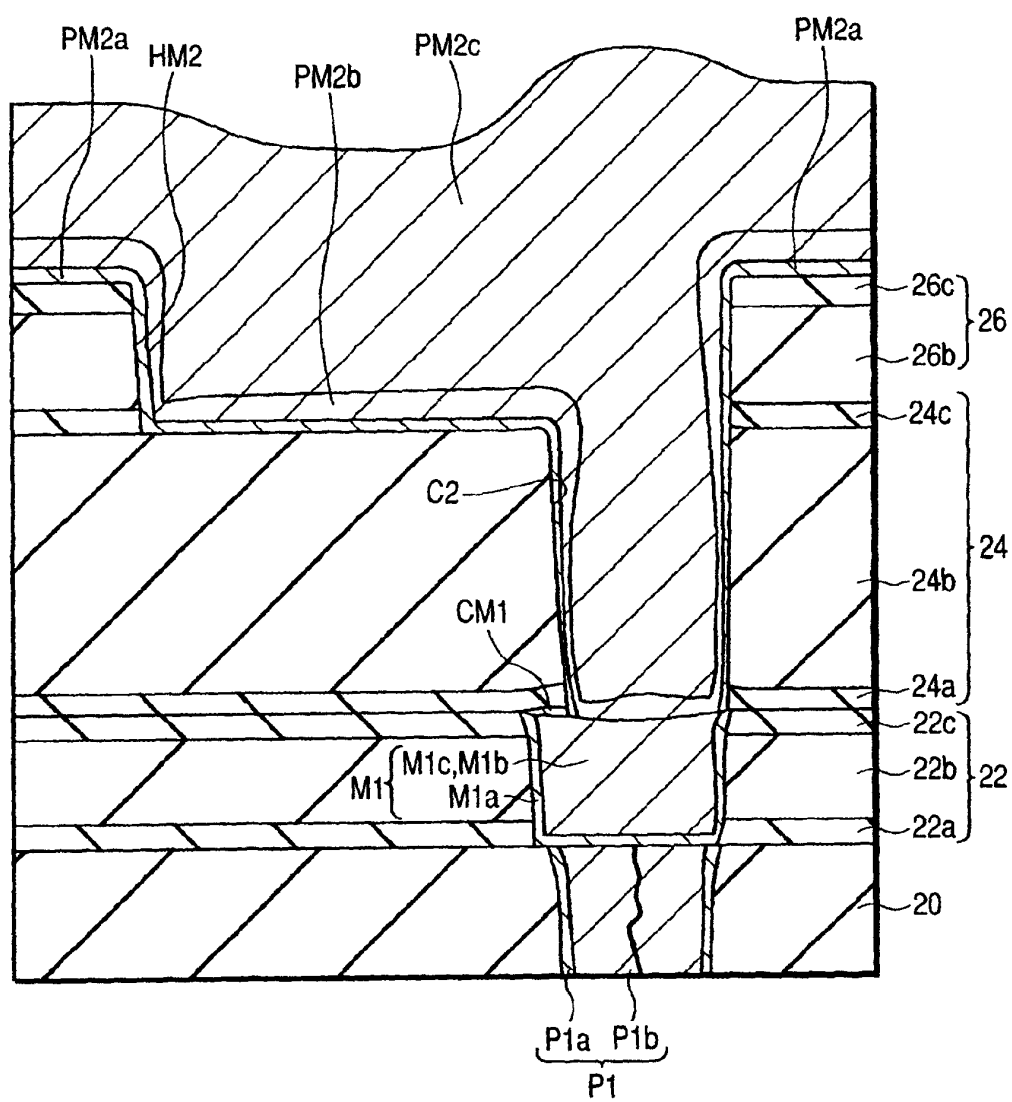


图16

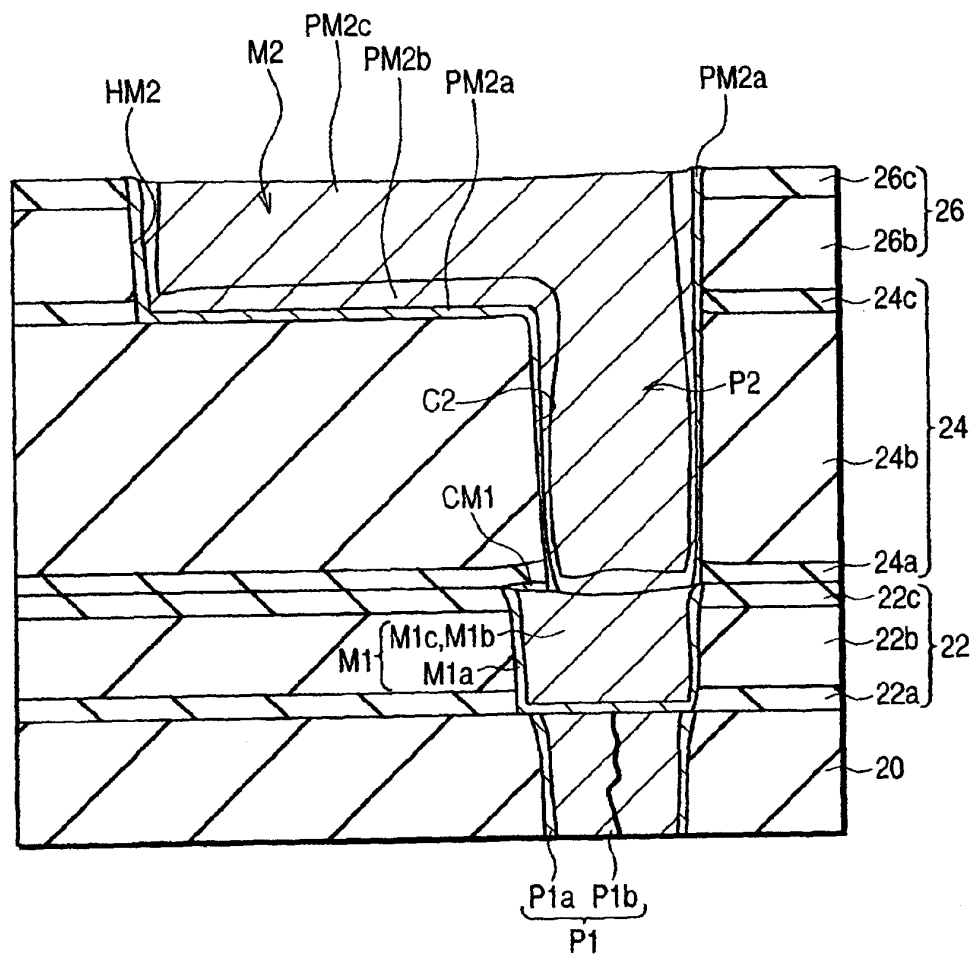


图18

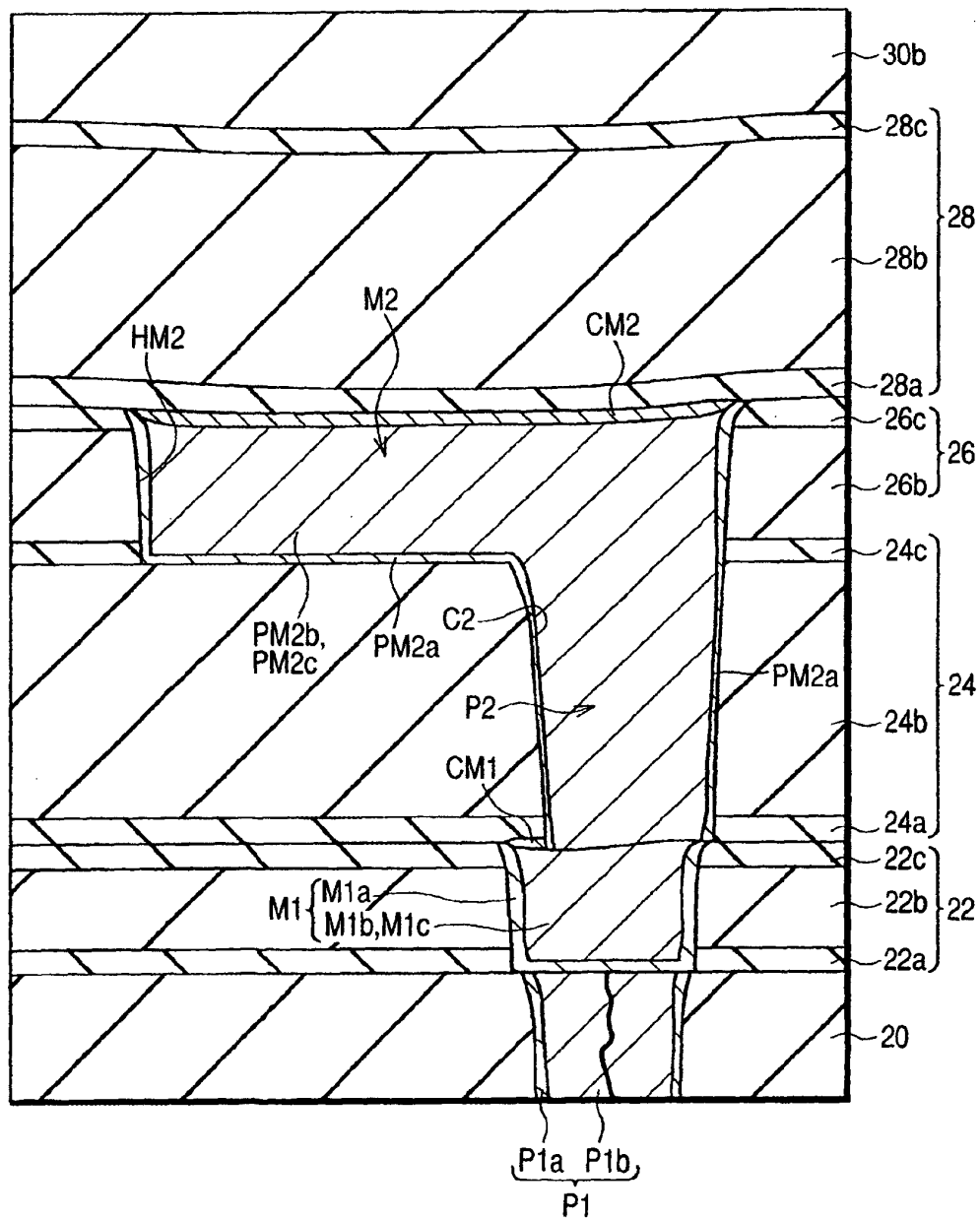


图17

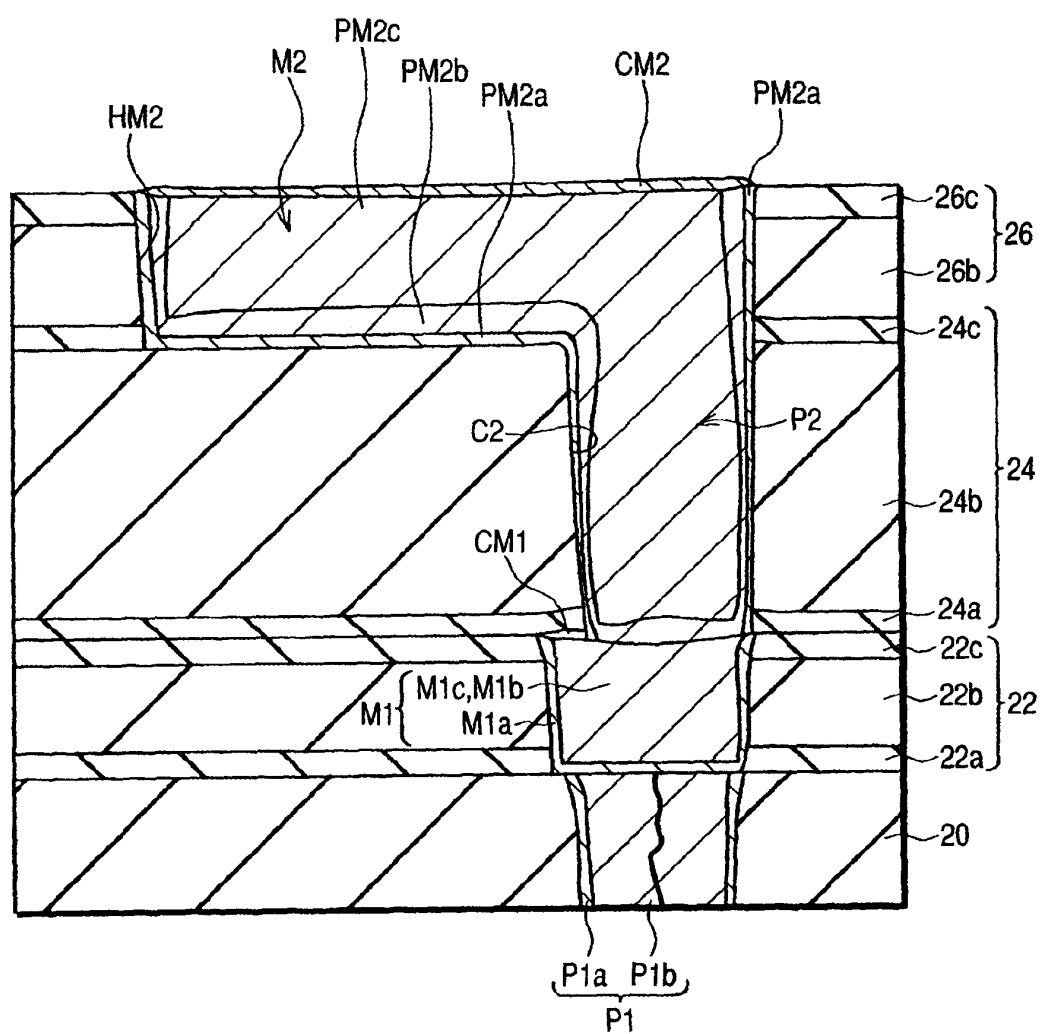


图19

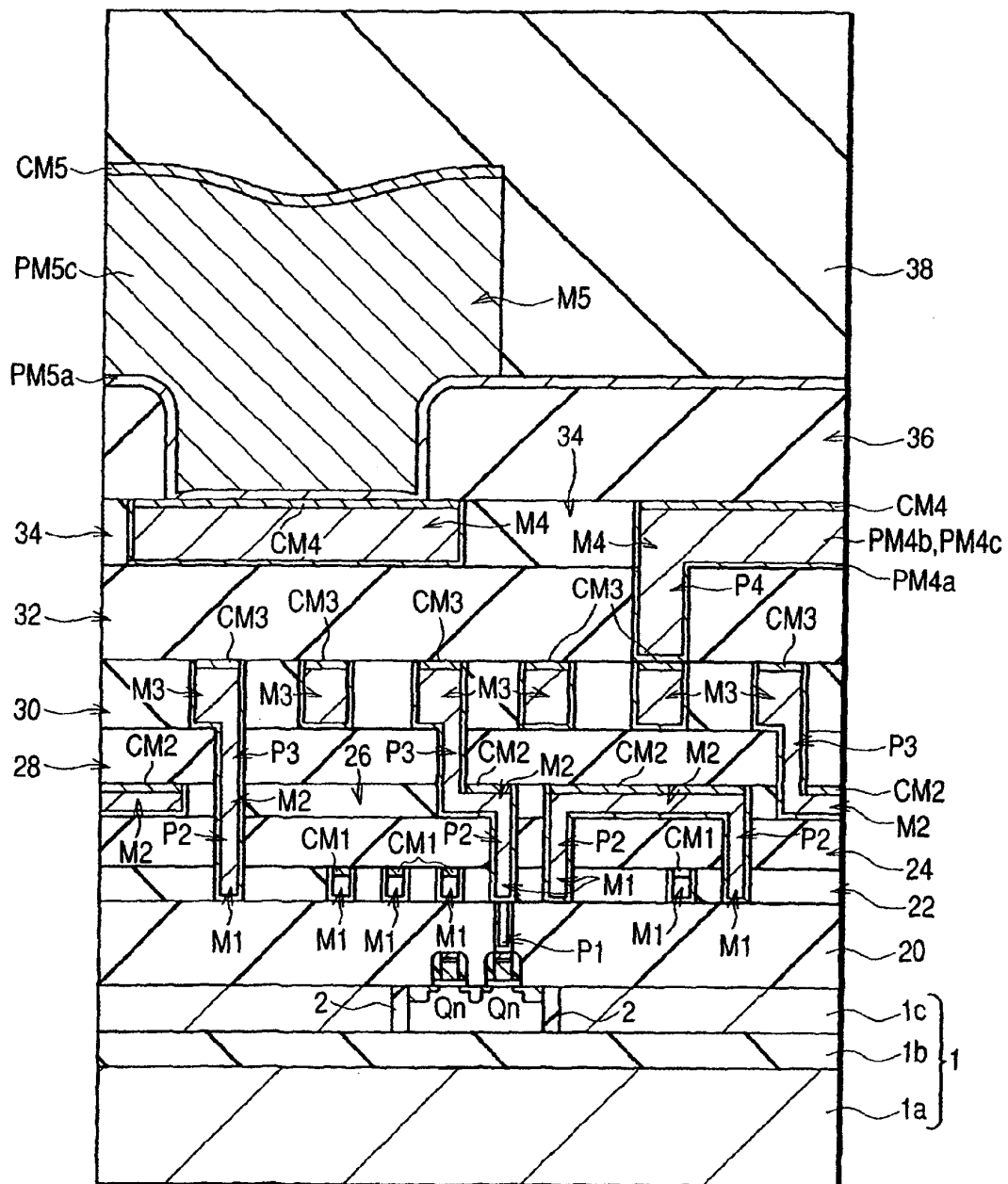


图20

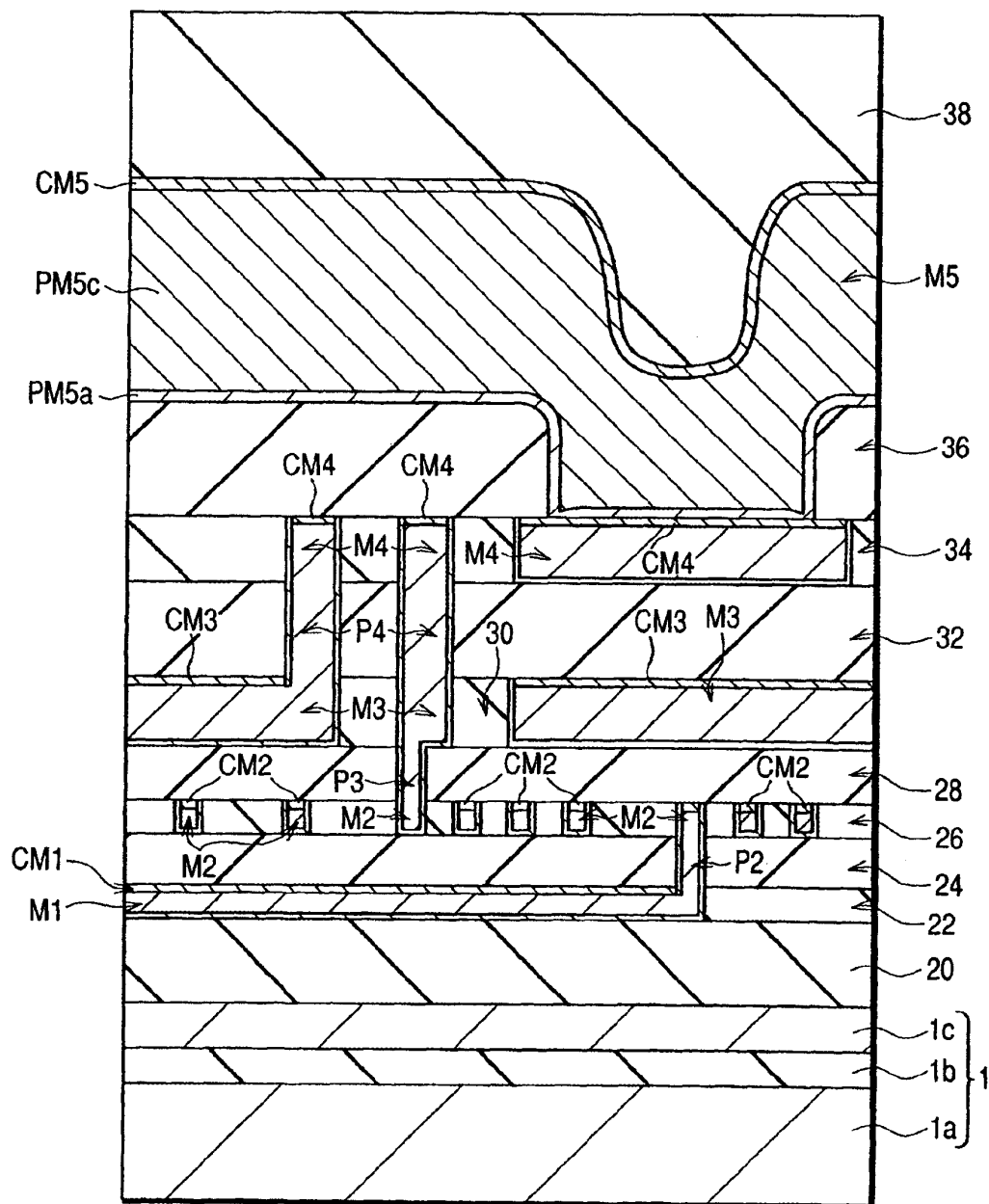
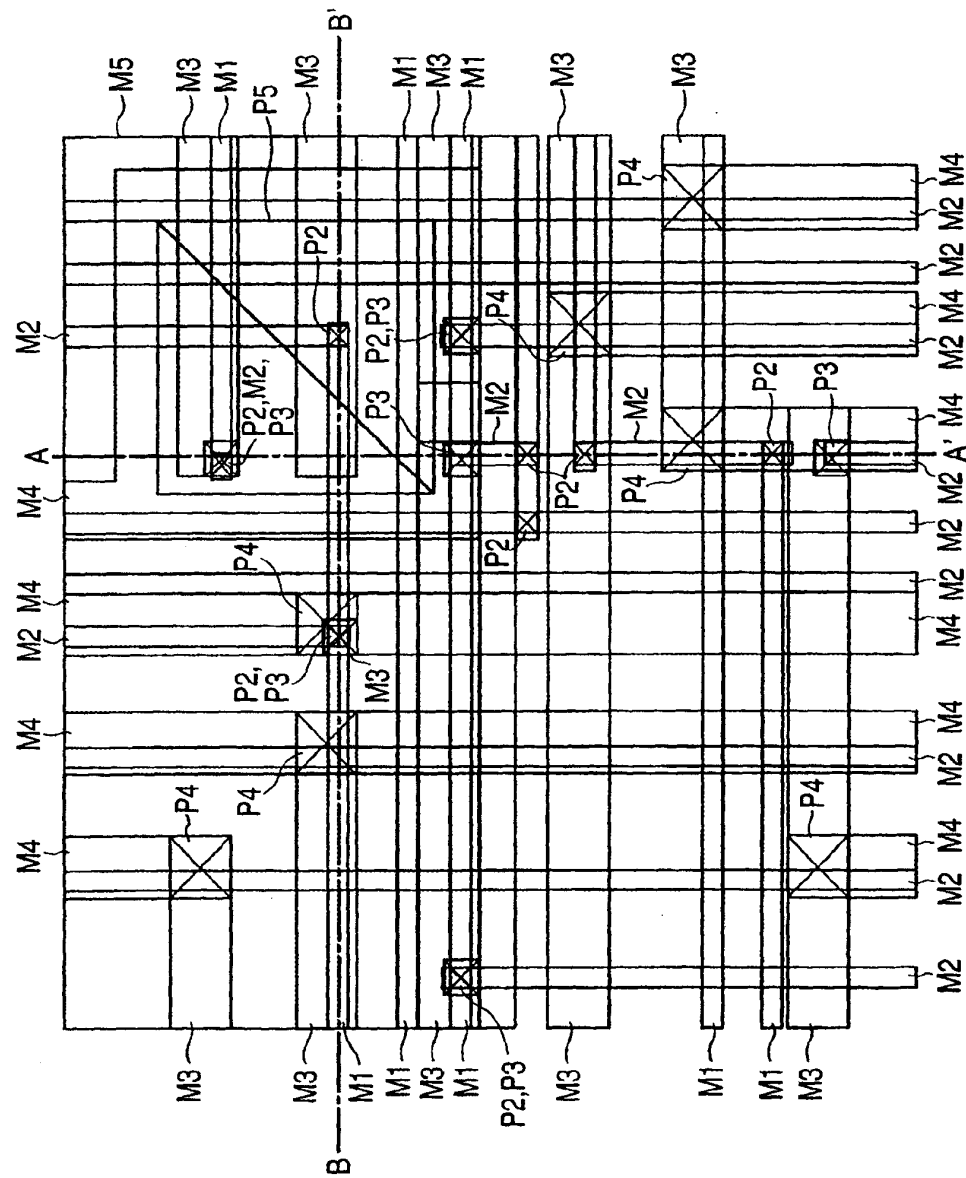


图21



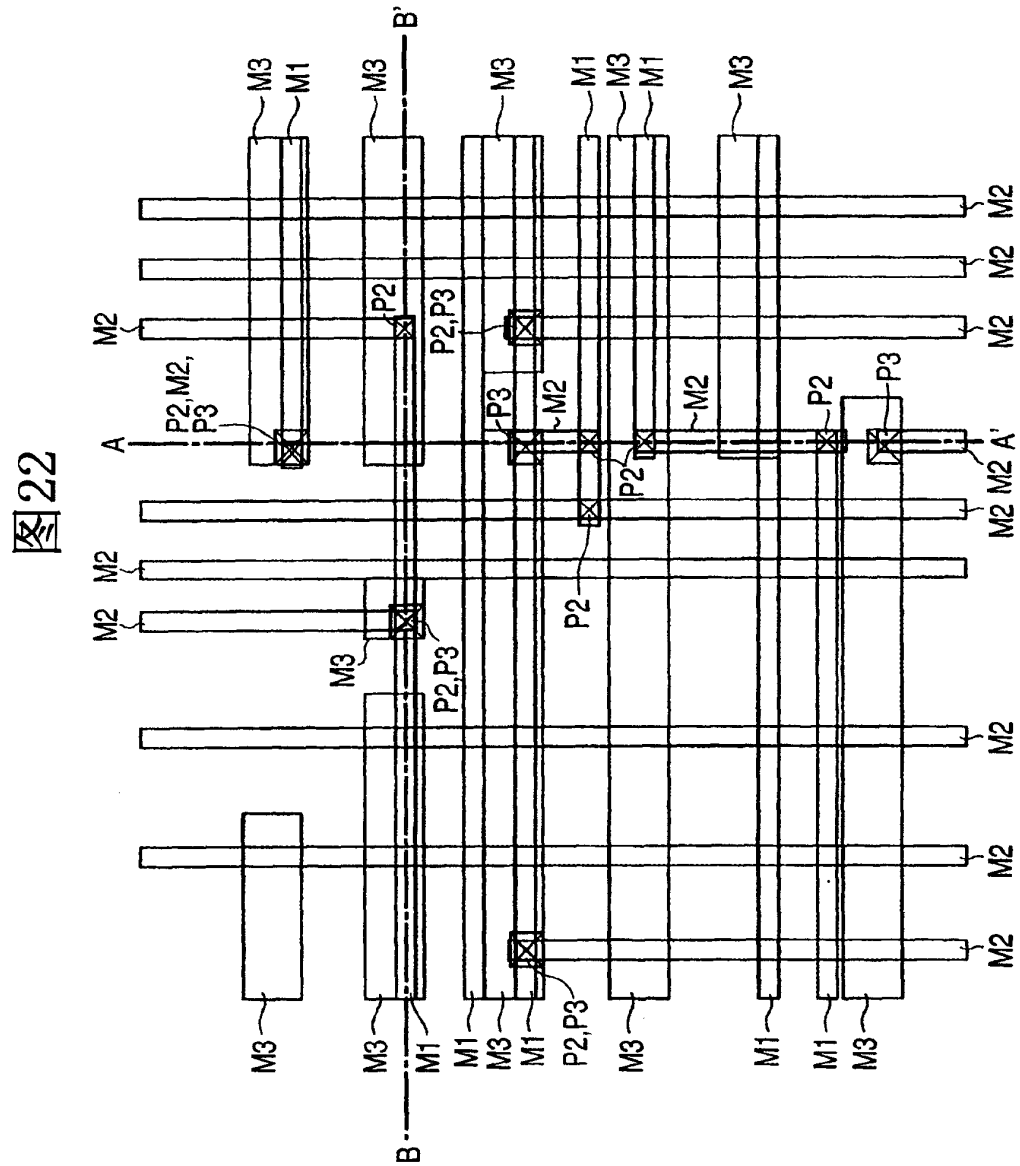


图 23

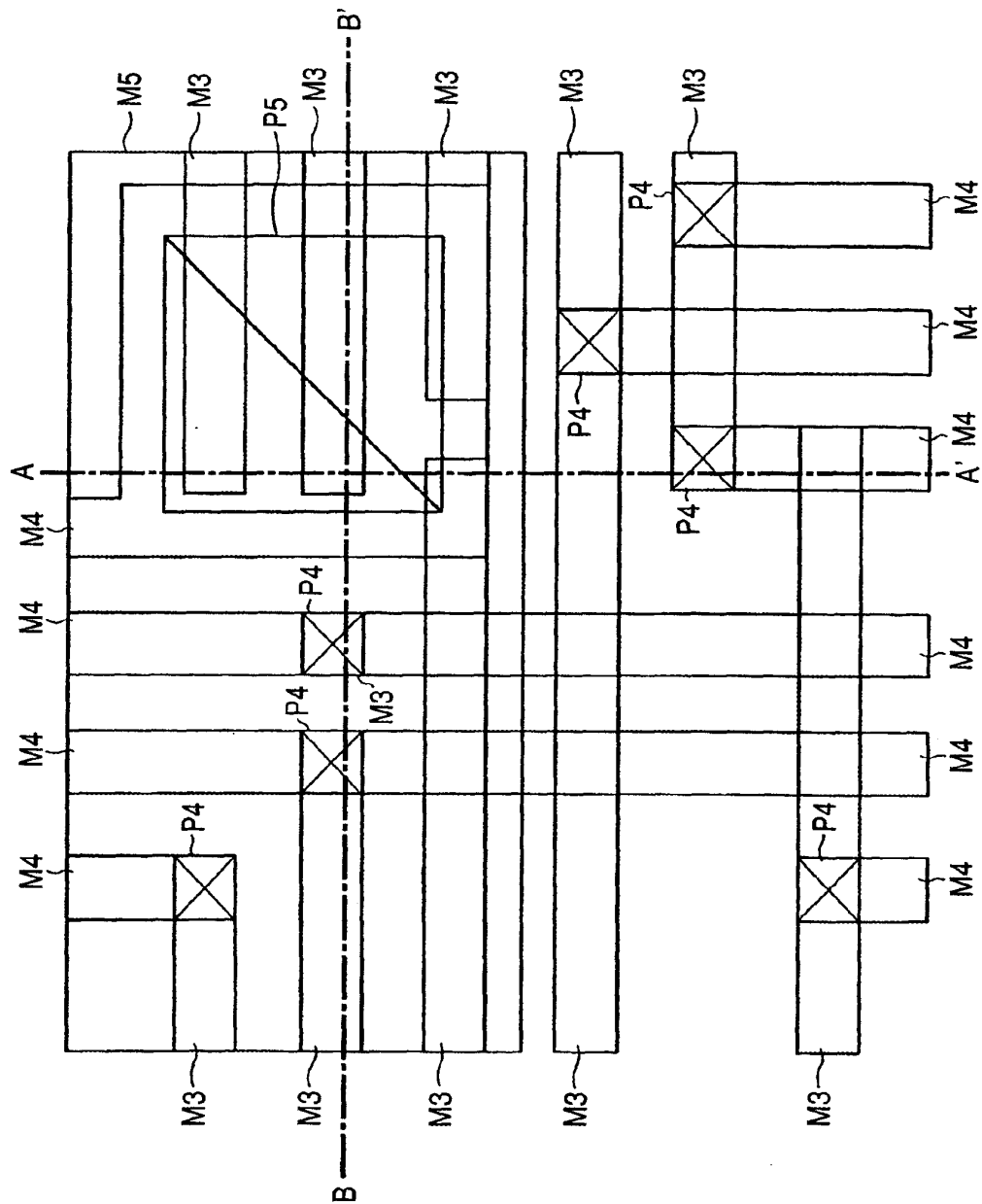


图24

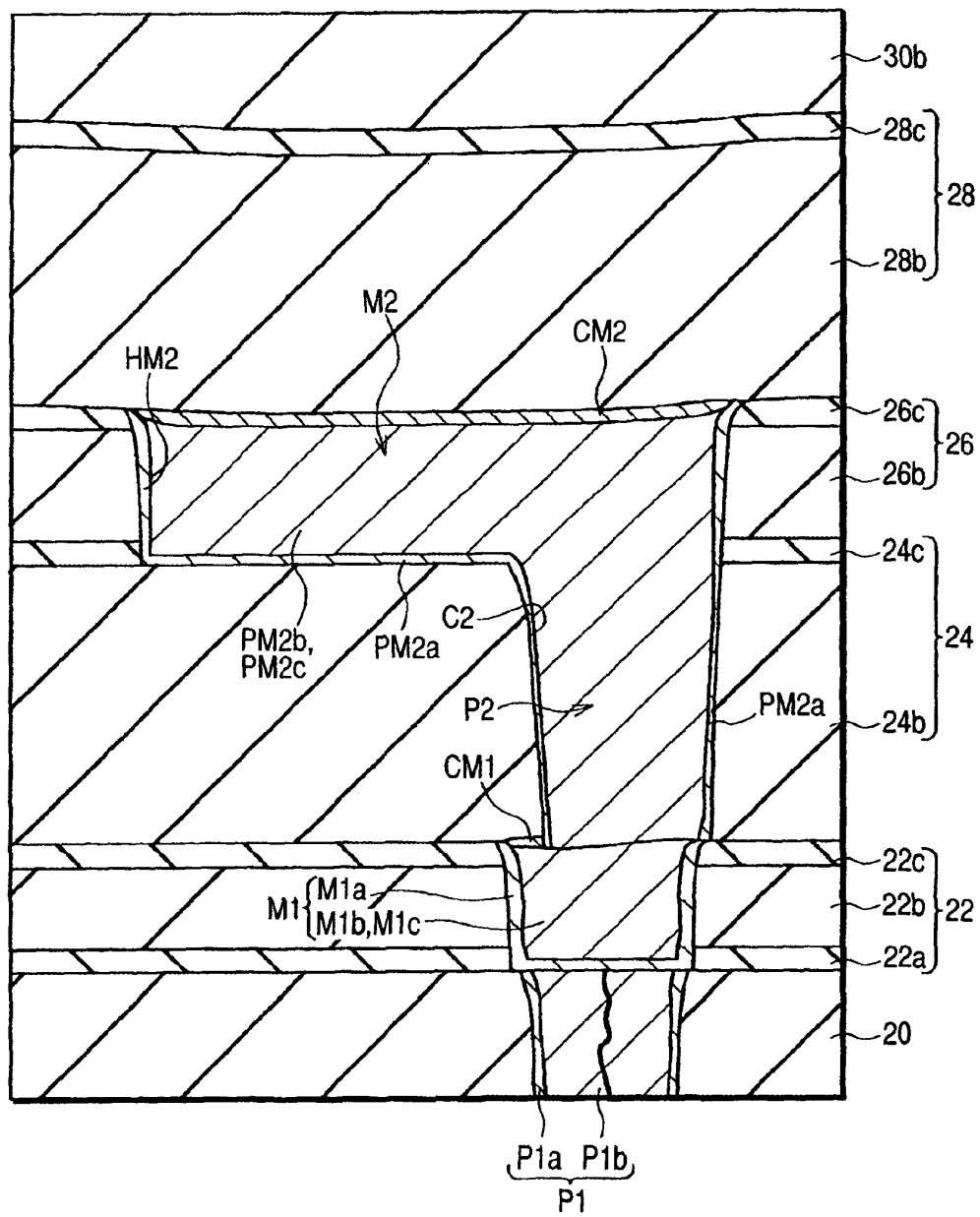


图25

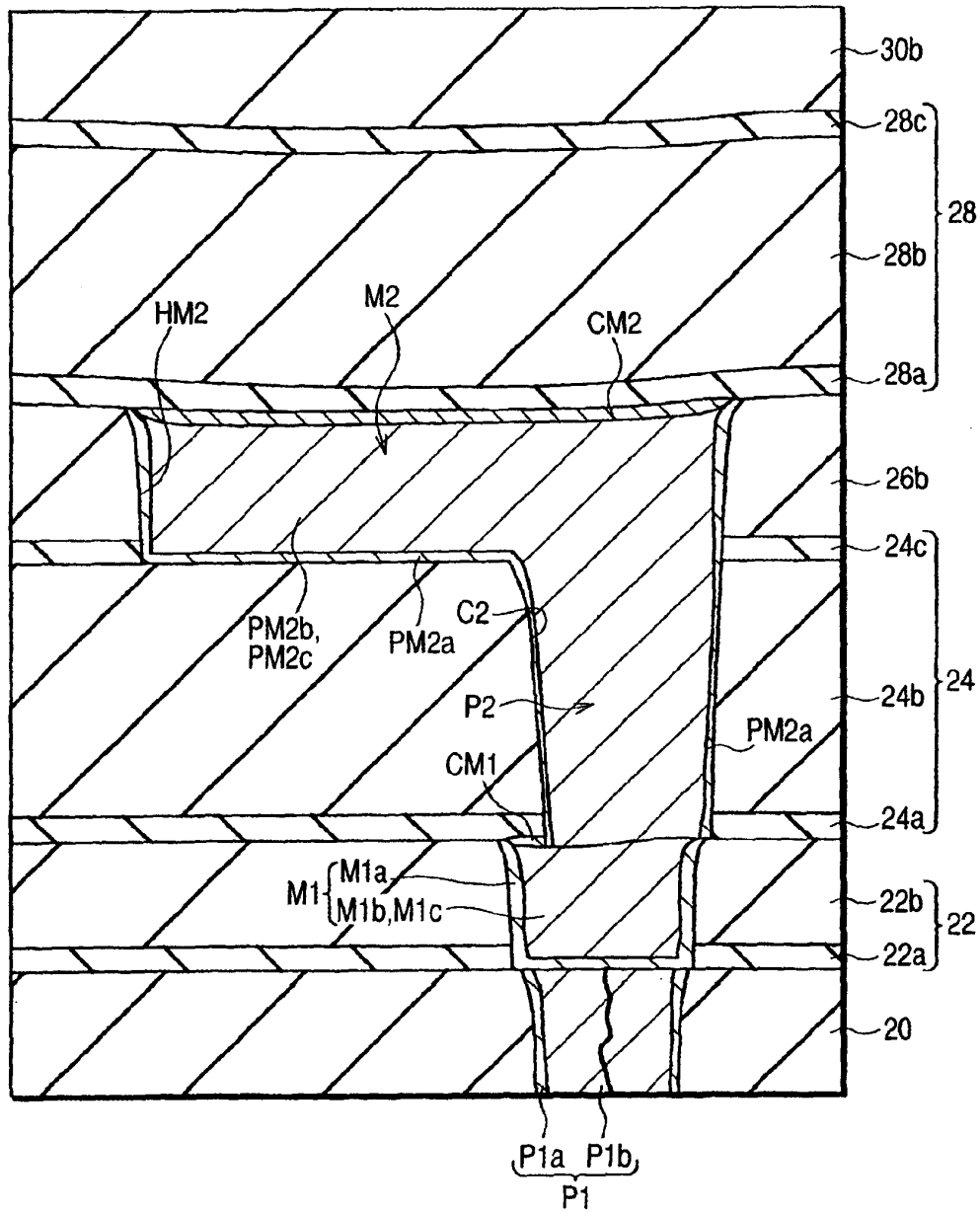


图26

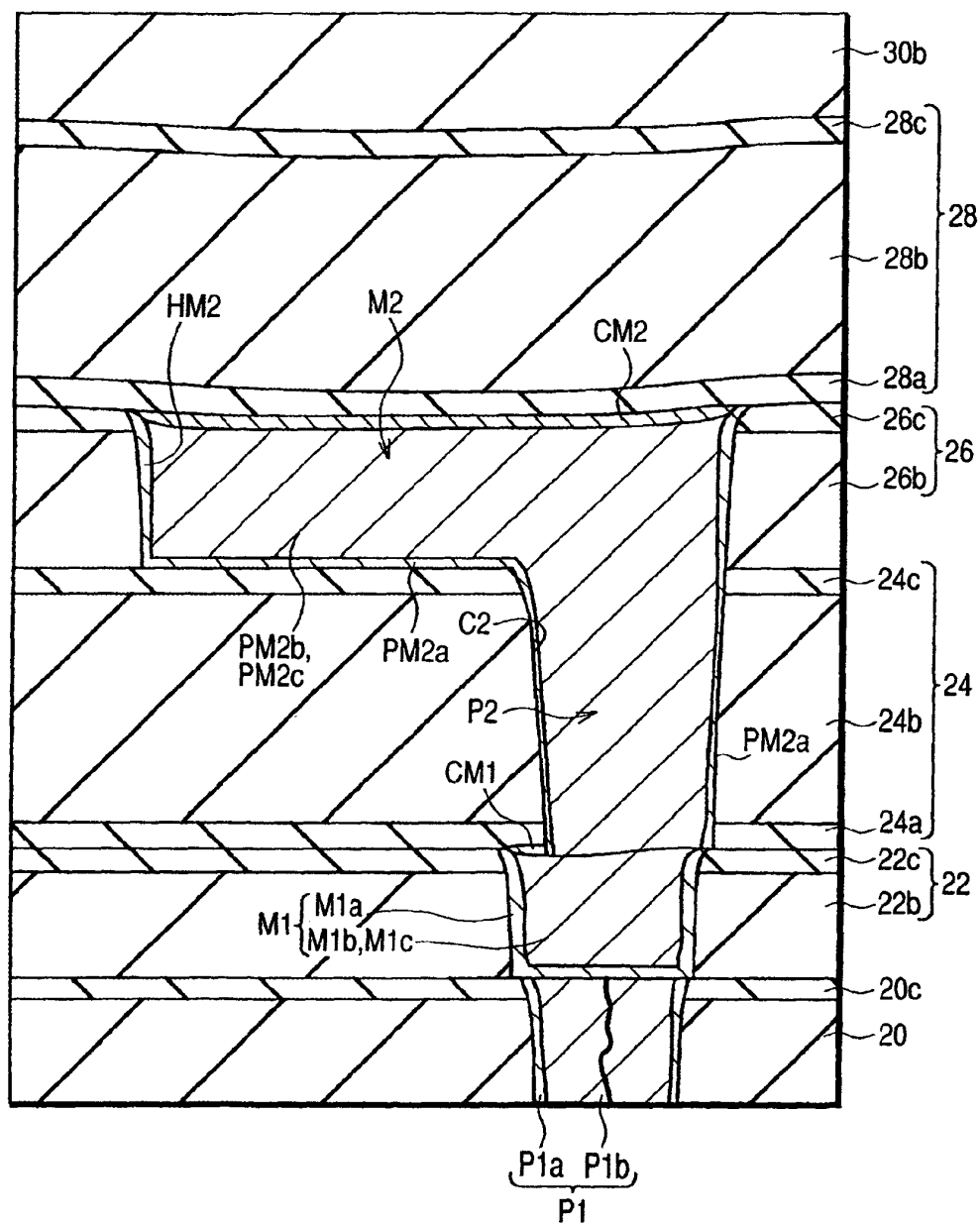


图27

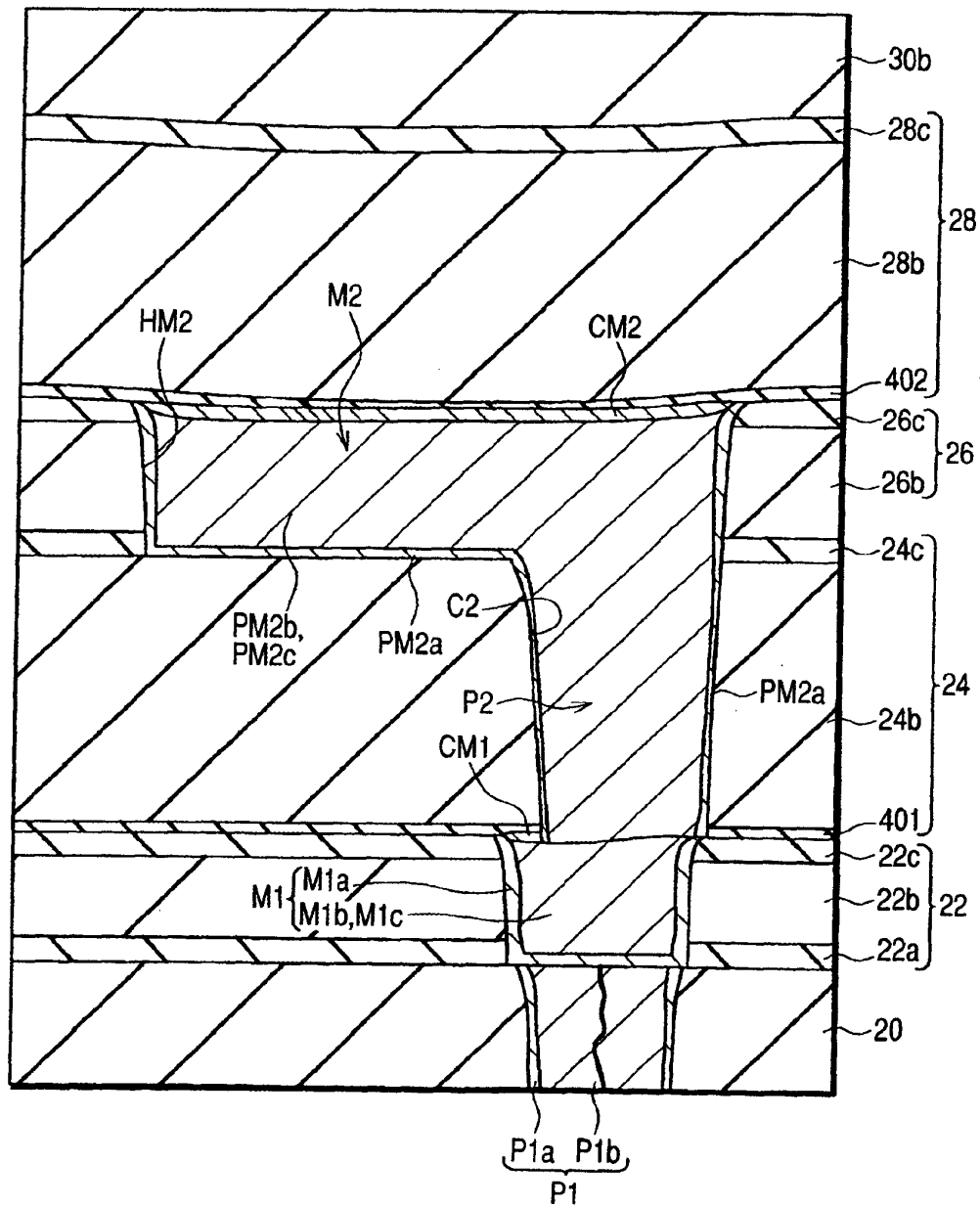


图28

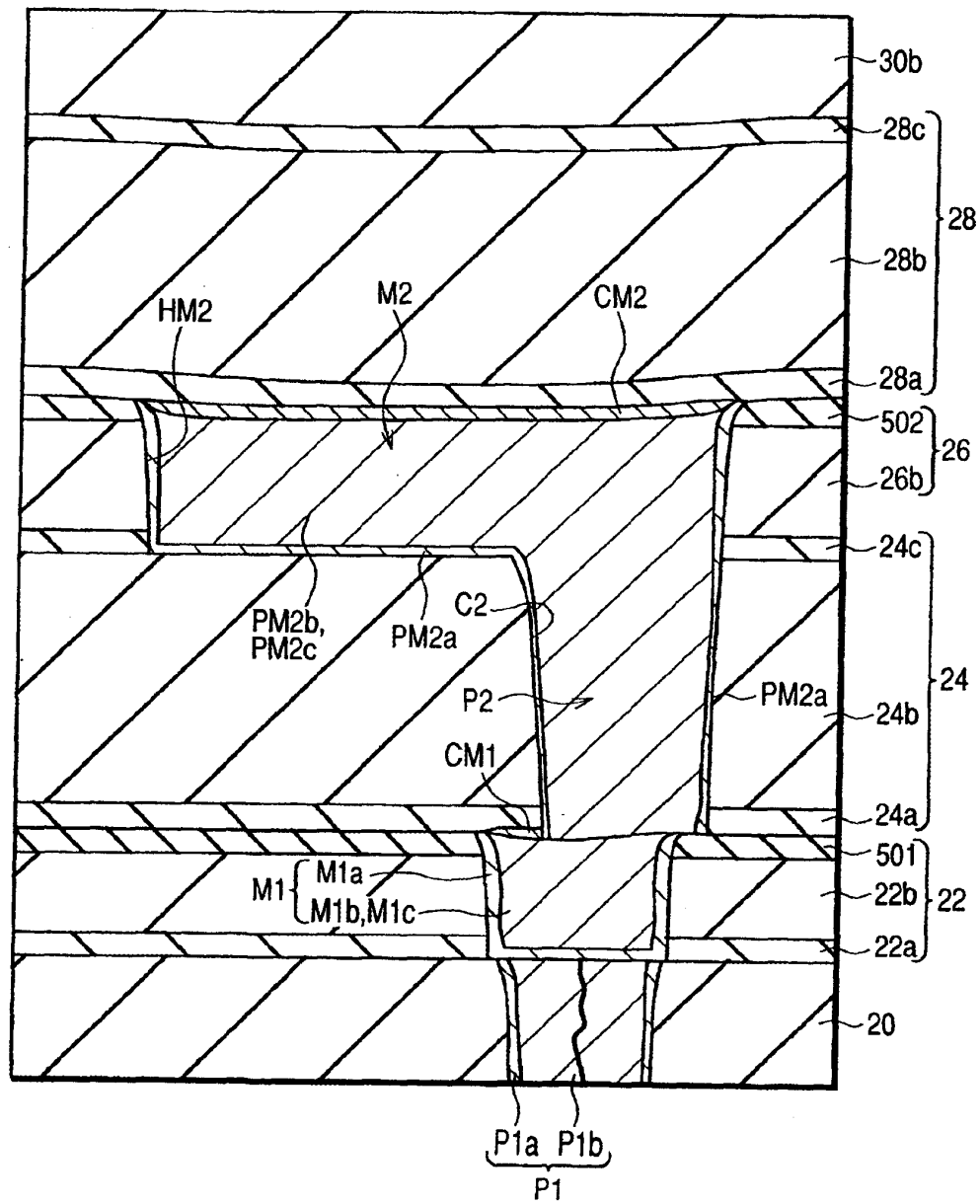


图29

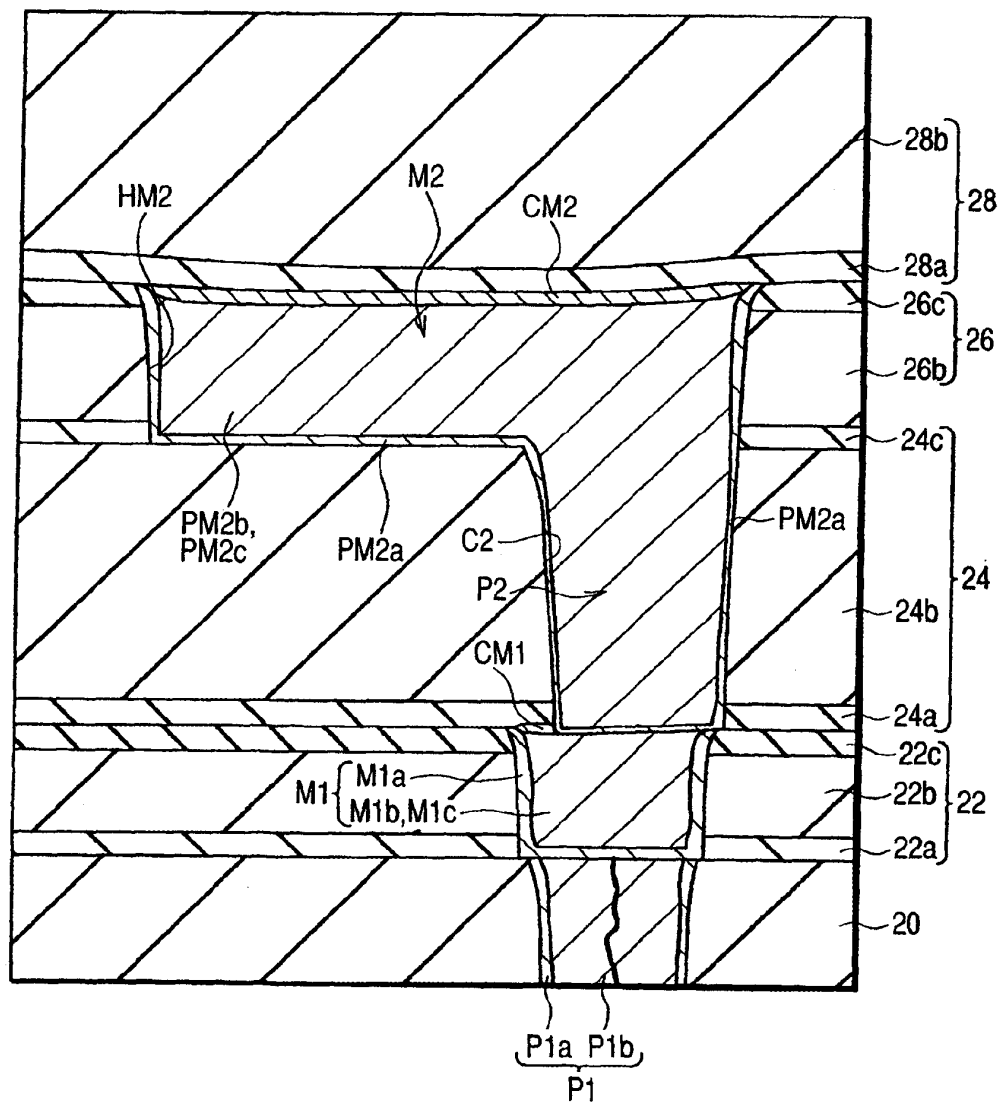


图31

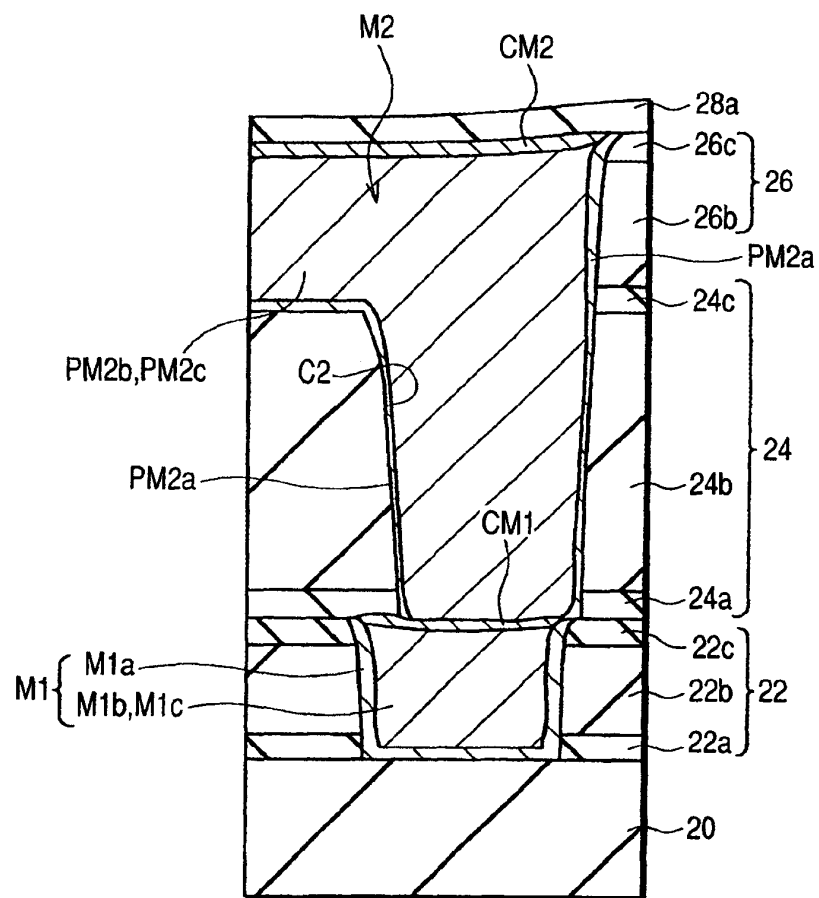


图32

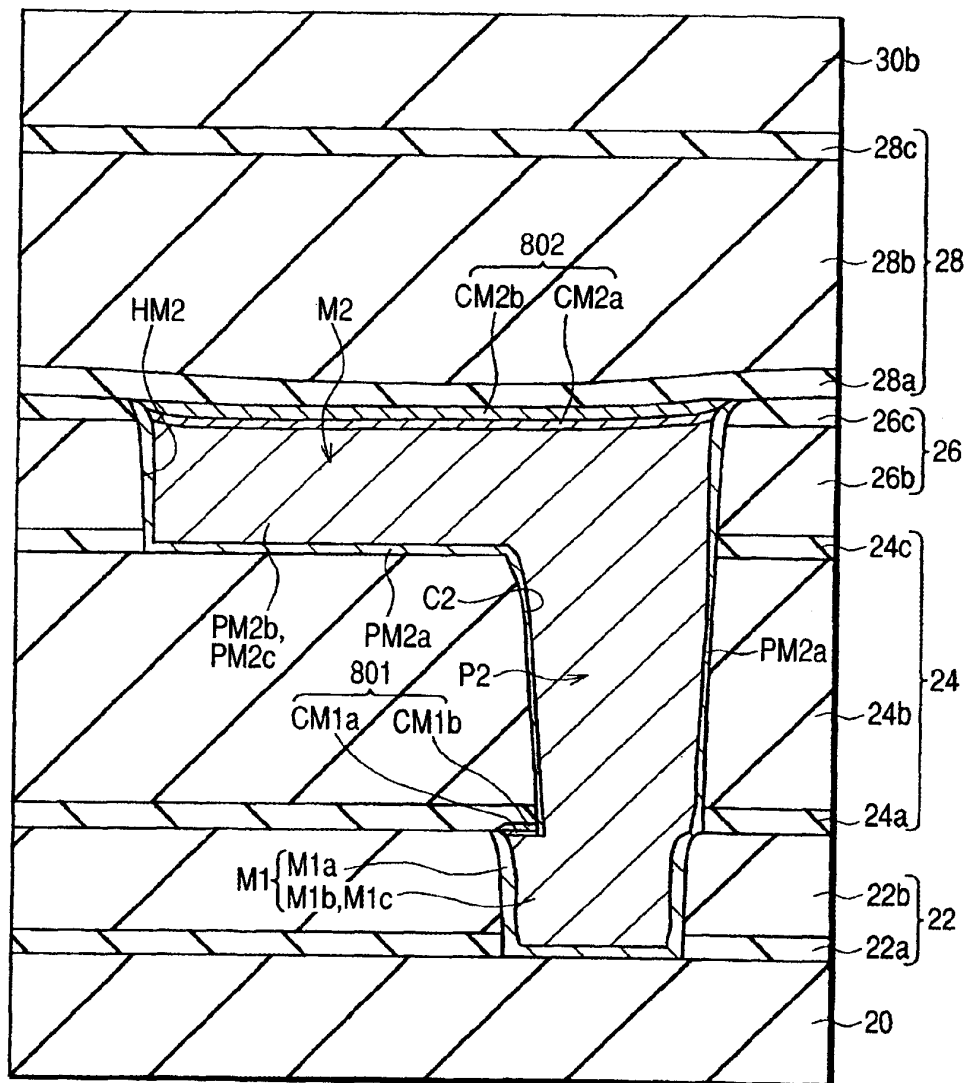


图30

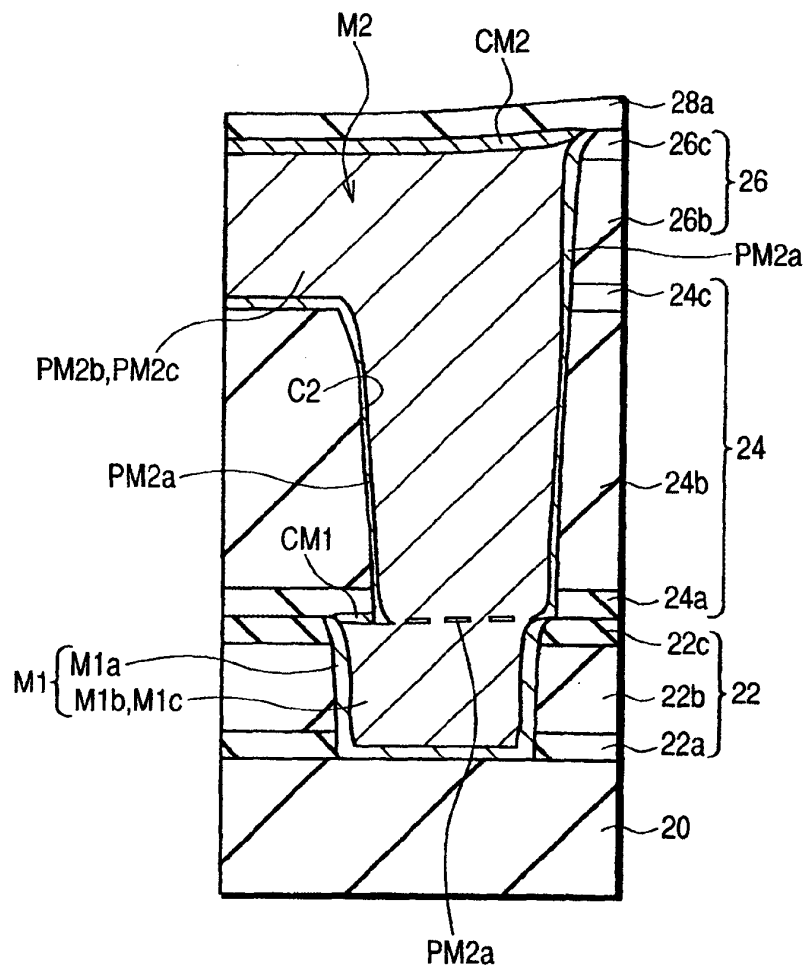


图33

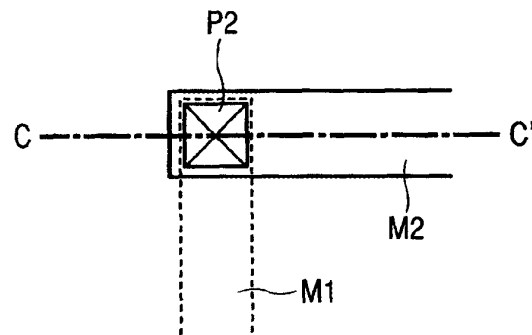


图34

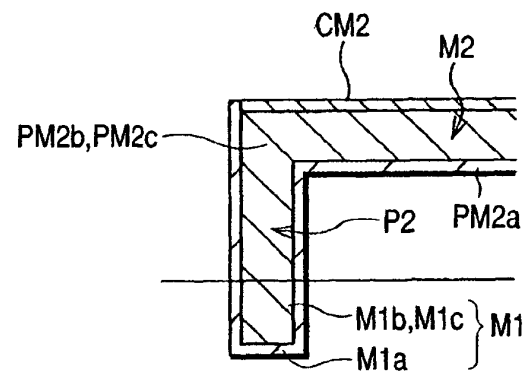


图35

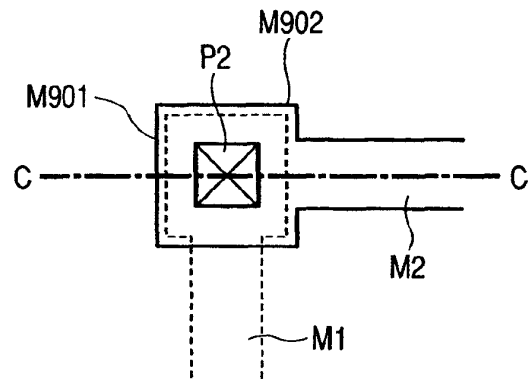


图36

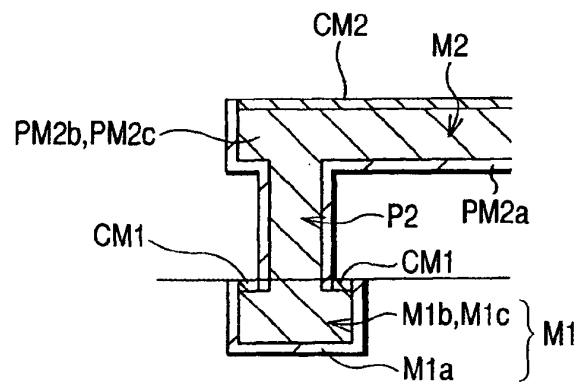


图37

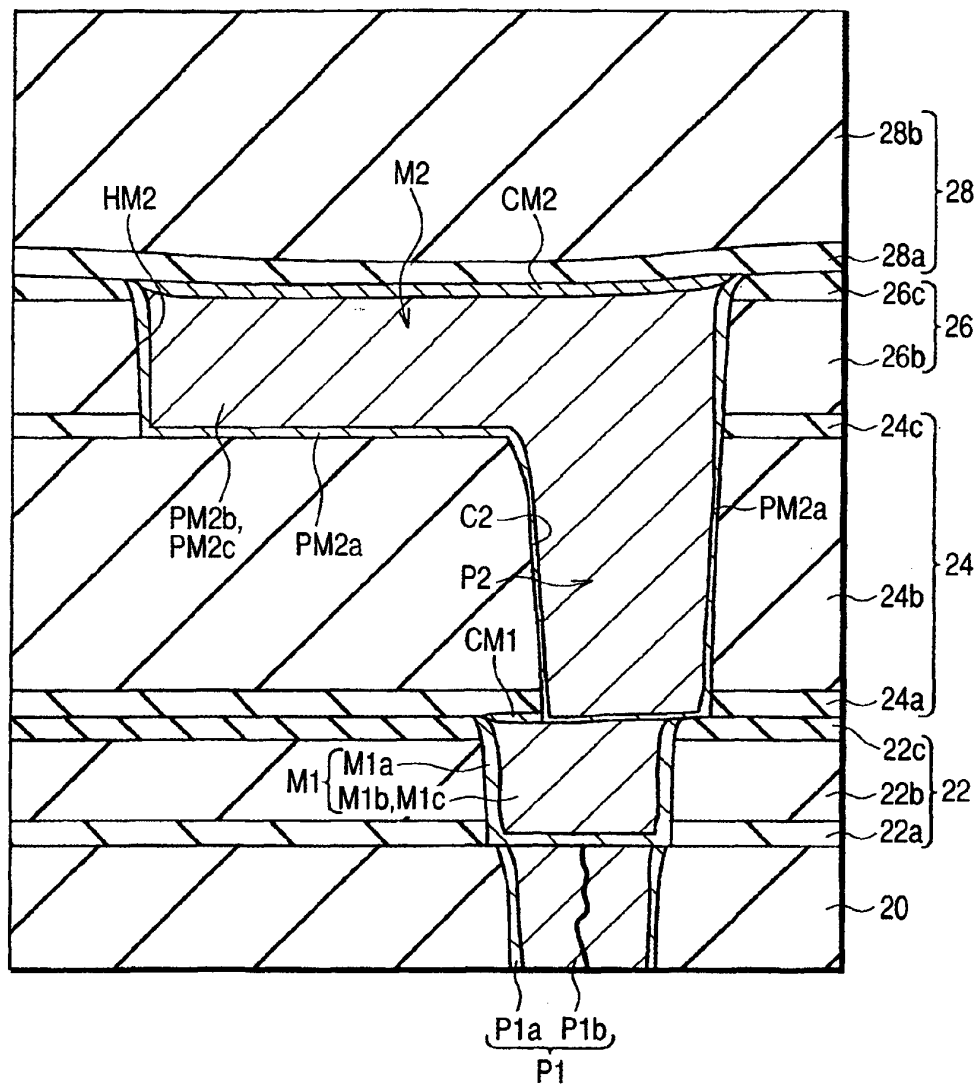
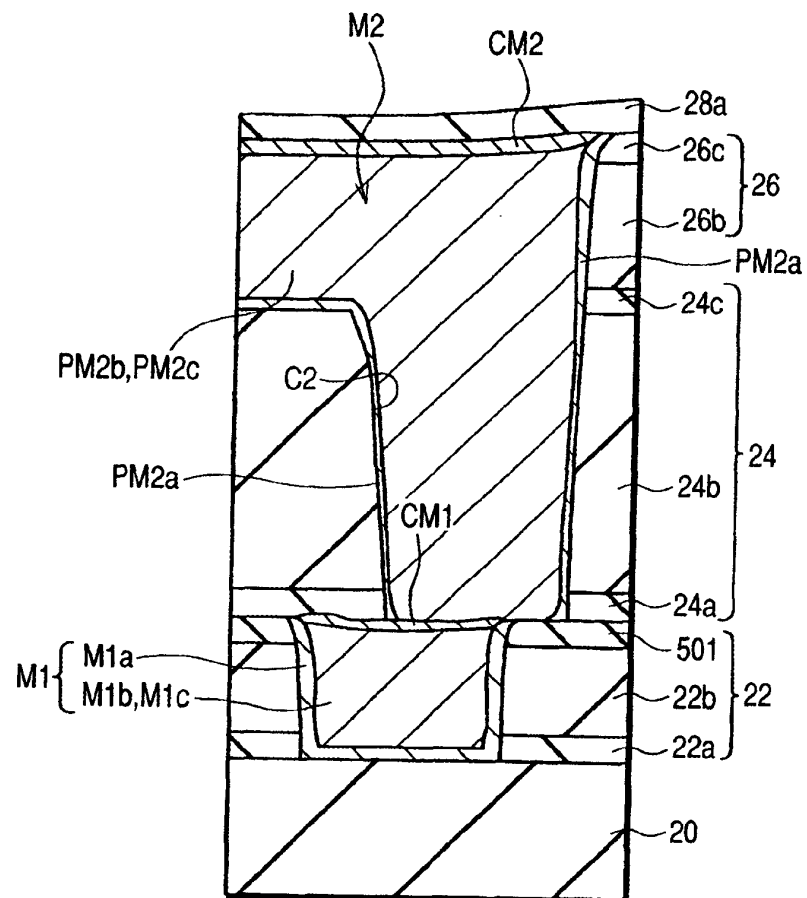


图38





Espacenet

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An interconnect structure with dielectric air gaps

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US7595554 (B2) WO2008008758 (A2) WO2008008758 (A3) less

Abstract of CN101490825 (A)

The invention relates to an interconnect structure with improved performance and capacitance by providing air gaps inside the dielectric layer by use of a multi-phase photoresist material. The interconnect features are embedded in a dielectric layer having a columnar air gap structure in a portion of the dielectric layer surrounding the interconnect features. The interconnect features may also be embedded in a dielectric layer having two or more phases with a different dielectric constant created. The interconnect structure is compatible with current back end of line processing.

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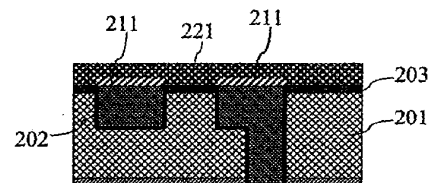
[74] 专利代理机构 北京市柳沈律师事务所
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权利要求书 3 页 说明书 6 页 附图 4 页

[54] 发明名称
具有电介质气隙的互连结构

[57] 摘要

一种通过利用多相光致抗蚀剂材料在电介质层内提供气隙而具有改善的性能和电容的互连结构。互连特征嵌入在电介质层中，该电介质层在围绕互连特征的部分中具有柱形气隙结构。互连特征也可以嵌入在具有产生不同介电常数的两相或更多相的电介质层中。该互连结构与现有的后段处理兼容。



1. 一种形成互连结构的方法, 包括:

形成嵌在第一电介质层(201)中的互连特征(202), 所述第一电介质层(201)沉积在衬底上, 所述互连特征(202)具有图案化的暴露的互连区域(204);

在所述第一电介质层(201)的围绕所述暴露的互连区域(204)的部分上形成第二层材料(203);

在所述暴露的互连区域(204)上形成帽层(211);

在所述第二层材料(203)和所述帽层(211)上沉积多相光致抗蚀剂(221); 及

将所述多相光致抗蚀剂(221)的与所述第二层材料(203)邻接的部分分离成不同相的材料的图案。

2. 如权利要求1的方法, 还包括:

在所述第一电介质层(201)的围绕所述暴露的互连区域(204)的所述部分中形成柱状气隙(240)并利用 RIE 工艺去除所述多相光致抗蚀剂(221)和所述第二层材料(203)。

3. 如权利要求2的方法, 还包括:

在所述不同相的材料的图案和所述帽层(211)上沉积第二电介质材料(251)。

4. 如权利要求1的方法, 其中所述第二层材料(203)具有亲水表面。

5. 如权利要求1的方法, 其中所述第二层材料(203)具有约 20Å 至约 800Å 的厚度。

6. 如权利要求1的方法, 其中所述第二层材料(203)是电介质。

7. 如权利要求1的方法, 其中所述第二层材料(203)是绝缘体。

8. 如权利要求1的方法, 其中所述第二层材料(203)是半导体。

9. 如权利要求1的方法, 其中所述互连特征(202)包括选自 Cu、Al、AlCu 和 W 构成的组的材料。

10. 如权利要求1的方法, 其中所述第一电介质层(201)是低介电常数材料。

11. 如权利要求1的方法, 其中所述第一电介质层(201)具有约 500Å

至约 10000Å 的厚度。

12. 如权利要求 1 的方法, 其中所述帽层 (211) 是具有选自包括 W、P、B、Sn 和 Pd 的组的材料的 Co 合金。

13. 如权利要求 12 的方法, 其中所述帽层 (211) 具有约 50Å 到约 300Å 的厚度。

14. 如权利要求 1 的方法, 其中所述帽层 (211) 的材料选自包括 CoSnP、Pd 和 Ru 的组。

15. 如权利要求 1 的方法, 其中所述帽层 (211) 具有疏水表面。

16. 如权利要求 1 的方法, 其中所述多相光致抗蚀剂 (221) 是具有第一相 (A) 光致抗蚀剂 (231) 和第二相 (B) 光致抗蚀剂 (232) 的两相光致抗蚀剂。

17. 如权利要求 16 的方法, 其中所述两相光致抗蚀剂 (221) 具有约 50Å 至约 1000Å 的厚度。

18. 如权利要求 16 的方法, 其中所述第一相 (A) 光致抗蚀剂 (231) 包括硅石、有机硅烷和选自包括胺、酰胺、醛和 hydrosy 的组的材料, 所述第二相 (B) 光致抗蚀剂 (232) 是聚合物。

19. 如权利要求 16 的方法, 其中所述第二相 (B) 光致抗蚀剂 (232) 比所述第一相 (A) 光致抗蚀剂 (231) 具有更高的耐蚀刻性。

20. 如权利要求 16 的方法, 还包括去除所述第一相 (A) 光致抗蚀剂 (231) 的步骤。

21. 如权利要求 3 的方法, 其中所述第二电介质材料 (251) 是低介电常数材料。

22. 一种互连结构, 包括:

嵌在第一电介质层 (201) 中的互连特征 (202), 所述互连特征 (202) 具有图案化的暴露的互连区域 (204);

在所述暴露的互连区域 (204) 上的帽层 (211);

在所述第一电介质层 (201) 的围绕所述暴露的互连区域 (204) 的部分中的柱状气隙结构 (240); 及

在所述柱状气隙结构 (240) 和帽层 (211) 上的第二电介质材料 (251)。

23. 一种互连结构, 包括:

嵌在第一电介质层 (201) 中的互连特征 (202), 所述互连特征 (202)

具有图案化的暴露的互连区域 (204);
在所述暴露的互连区域 (204) 上的帽层 (211);
在所述第一电介质层 (201) 的围绕所述暴露的互连区域 (204) 的部分
中的双 k 电介质材料 (241) 结构; 及
在所述柱状气隙结构 (240) 和帽层 (211) 上的第二电介质材料 (251)。

具有电介质气隙的互连结构

技术领域

本发明总地涉及半导体器件的制造，更具体而言，涉及在电介质层中实现气隙（air gap）的方法和结构。

背景技术

随着半导体器件持续缩小，互连线宽的相应减小增加了线电阻。互连之间减小的间距还产生了更多的寄生电容。这导致电路信号延迟和较低的芯片速度及性能。

为了减少电路延迟的 BEOL（后段：back end of line）互连部分，传统的二氧化硅电介质（大约 4.0 的 k 值）被大约 3.0 的 k 值的致密低 k 膜取代。为了进一步改善性能，对于高级器件而言需要更佳的电容率（k 小于 2.5）。

可以用新的多孔低 k 电介质改善电容，然而，与致密电介质相比，多数多孔材料具有相对弱的机械特性。对于当前的 BEOL 工艺而言，将这些材料与其它模块工艺集成也是一个严重的挑战。例如，常规 CMP（化学机械抛光）工艺难以抛光低机械模量多孔电介质，常规 PVD（等离子体气相沉积）扩散阻挡沉积技术不能在多孔电介质的表面上提供良好的覆盖。

通过降低介电常数改善电容的另一技术是在导线之间产生气隙。虽然二氧化硅具有大约 4.0 和更大的介电常数，但空气的介电常数大约为 1。

美国专利 No. 5949143 (Bang) 在相邻的两个互连之间形成气隙。该气隙被扩散阻挡层覆盖且然后被绝缘层覆盖，从而允许与上面的互连层面集成。

美国专利 No. 6440839 (Partovi) 通过在层间电介质 (interlevel dielectric) 上使用“润湿性的 (tenon-wetting)”侧壁间隔物来抑制金属的沉积，以在相邻的两个互连之间形成小的气隙。该技术限于在两个宽间距的互连之间形成小的气隙。

美国专利 No. 6861332 (Park) 公开了使用排气孔在电介质中形成气隙。

美国专利 No. 6780753 (Latchford) 这样形成气隙：在导体之间沉积电介质材料，在导体和电介质之上沉积多孔层，然后通过多孔层从导体之间的

空间剥离电介质材料，在导体之间留下气隙。

美国公开 No. 2005/0062165 (Saengar) 形成封闭的气隙互连结构。

美国公开 No. 2006/0019482 (Su) 在多个虚设柱 (stake) 和多个金属线之间形成气隙。

因此，需要这样的结构，其提高互连的可靠性，与现有 BEOL 处理相容。

本发明的一个目的是通过在致密电介质材料中产生气隙来提供性能和电容的改善。

本发明的另一个目的是以与现有的 BEOL 处理相容的方式提供这些改善而没有使用新的或特别的多孔电介质材料。

发明内容

本发明提供一种互连结构，包括：嵌在第一电介质层中的互连特征，所述互连特征具有图案化的暴露的互连区域；所述暴露的互连区域上的帽层；所述第一电介质层的围绕所述暴露的互连区域的部分中的柱状气隙结构；及所述柱状气隙结构和帽层上的第二电介质材料。

在另一实施例中，提供一种互连结构，包括：嵌在第一电介质层中的互连特征，所述互连特征具有图案化的暴露的互连区域；所述暴露的互连区域上的帽层；所述第一电介质层的围绕所述暴露的互连区域的部分中的双 k 电介质材料结构；以及所述柱状气隙结构和帽层上的第二电介质材料。

在本发明的另一实施例中，提供一种形成互连结构的方法，包括：形成嵌在第一电介质层中的互连特征，所述第一电介质层沉积在衬底上，所述互连特征具有图案化的暴露的互连区域；在所述第一电介质层的围绕所述暴露的互连区域的部分上形成第二层材料；在所述暴露的互连区域上形成帽层；在所述第二层材料和所述帽层上沉积多相光致抗蚀剂；以及将所述多相光致抗蚀剂的与所述第二层材料邻接的部分分离成不同相的材料的图案。

该方法还包括在所述第一电介质层的围绕所述暴露的互连区域的所述部分中形成柱状气隙，并利用 RIE 工艺去除所述多相光致抗蚀剂和所述第二层材料。该方法还包括在所述不同相的材料的图案和所述帽层上沉积第二电介质材料。

所述第二层材料优选具有亲水表面。所述第二层材料优选具有约 20Å 至约 800Å 的厚度。所述第二层材料优选是电介质、绝缘体或半导体。

所述互连特征优选包括选自 Cu、Al、AlCu 和 W 构成的组的材料。所述第一电介质层优选是低介电常数材料，且优选具有约 500Å 至约 10000Å 的厚度。

所述帽层优选是 Co 合金，具有 Co 和选自包括 W、P、B、Sn 和 Pd 的组的材料。所述帽层优选具有约 50Å 到约 300Å 的厚度。在优选实施例中，帽层材料选自包括 CoSnP、CoWP、Pd 和 Ru 的组。所述帽层优选具有疏水表面。

在优选实施例中，所述多相光致抗蚀剂是具有第一相 (A) 光致抗蚀剂和第二相 (B) 光致抗蚀剂的两相光致抗蚀剂。所述两相光致抗蚀剂优选具有约 50Å 至约 1000Å 的厚度。

所述第一相 (A) 光致抗蚀剂优选包括硅石、有机硅烷和选自包括胺、酰胺、醛和 hydrosy 的组的材料，所述第二相 (B) 光致抗蚀剂优选是聚合物。在优选实施例中，所述第二相 (B) 光致抗蚀剂比所述第一相 (A) 光致抗蚀剂具有更高的耐蚀刻性。

该方法还可包括去除所述第一相 (A) 光致抗蚀剂的步骤。所述第二电介质材料优选是低介电常数材料。

附图说明

相信本发明的特征是新颖的，且本发明的基本特性具体阐述于所附权利要求中。图仅用于说明，且不是按比例。然而，发明本身，无论是结构还是操作方法，通过参照下面结合附图的详细说明可被更好地理解。附图中：

图 1A-1D 是示意性剖视图，示出具有气隙的常规镶嵌结构；

图 2A-2E 是示意性剖视图，示出根据本发明在镶嵌结构中形成气隙的方法；

图 2F(a)和 2F(b)是示意性剖视图，示出根据本发明的优选气隙结构。

具体实施方式

本发明通过在电介质材料内产生气隙而提供具有改善的性能和电容的互连结构。

本发明通过在层间电介质内提供气隙结构 (通过多相光致抗蚀剂材料产生) 改善了互连器件的电容。本发明与现有的 BEOL 工艺流程兼容，不需要

开发新的模块用于产生蚀刻轮廓 (etching profile)、更好的阻挡层覆盖、处理 CMP 工艺。

参照图 1A-1D, 示出用于在镶嵌结构中产生气隙的常规方法的示意图。图 1A 示出在嵌入于电介质中的互连上的选择性帽沉积。图 1B 示出硬掩模层的沉积。图 1C 示出沉积阻挡掩模 (block mask) 用于图案化和蚀刻。图 1D 示出去除围绕互连的电介质且由此形成气隙。

该工艺需要额外的掩模, 导致增加的成本和工艺时间, 以及与将阻挡掩模对准到图案化的互连特征相关的增大的产率损失。

根据本发明, 气隙结构由在 RIE (反应离子蚀刻) 处理期间具有不同蚀刻选择性的多相光致抗蚀剂材料例如 Diblock 产生。本发明提供这样的优点, 即与现有的 Cu 双镶嵌工艺兼容地产生气隙而没有额外的掩模工艺。本发明的工艺成本因而低于现有的方法。本发明还具有更好的技术扩展性, 因为其不限于任何特定的电介质材料。

参照图 2A-2F 描述本发明提出的制造气隙互连结构的详细方法。现在参照图 2A, 导电互连 202 嵌在绝缘体层 201 例如低介电常数材料和第二层材料 203 中。第二层材料 203 优选地具有“亲水表面”以用于后来的局部选择性相分离。嵌入的导电互连 202 还具有未嵌入在绝缘体 201 中的暴露表面 204。

第二层材料 203 的厚度优选地在 $20\text{\AA}$ 至 $800\text{\AA}$ 之间。第二层材料 203 可以是电介质、绝缘体或半导体。导电互连材料 202 优选地是 Cu、Al、Al(Cu) 或 W。优选地, 绝缘体层 201 是厚度在 500 至 $10000\text{\AA}$ 之间的低 k 材料。

现在参照图 2B, 互连导体 202 的暴露表面 204 被选择性地盖以帽层 211。帽层 211 优选地为 CoWP, 其既用作钝化层又用作扩散阻挡层。优选地, 帽层 211 的层厚在 50 至 $200\text{\AA}$ 之间。除了 CoWP 之外, 其它材料如 CoSnP、Pd 和 Ru 也是用于此功能的良好候选。优选地帽层材料 211 具有“疏水”表面以用于后来的随机相形成。该选择性帽沉积还将产生局部形貌 (topography) 以及提供两种不同的表面, 即疏水的金属性帽表面 211 和亲水的电介质硬掩模表面 203。

现在参照图 2C, 多相光致抗蚀剂材料 221 沉积在硬掩模 203 和帽层 211 的表面上。在优选实施例中, 多相光致抗蚀剂材料 221 是两相光致抗蚀剂例如 Diblock。两相光致抗蚀剂层 221 优选地具有 50 至 $1000\text{\AA}$ 之间的厚度。第

一相 (A) 优选地包括硅石、有机硅烷和胺、酰胺 (amide)、醛 (aldehyde) 或 hydrosy。第二相 (B) 优选地是常规的聚合物光致抗蚀剂。

现在参照图 2D, 其通过顶视图 2D (a) 和剖视图 2D (b) 示出了两相光致抗蚀剂材料 221 相分离成第一相 (A) 231 和第二相 (B) 232。两相光致抗蚀剂材料的相分离通过 UV 固化或热烘焙进行。UV 固化可在常规的 UV 固化设备中进行且该结构然后在约 100℃ 至约 400℃ 的基板温度经历 UV 曝光步骤。

可在环境气体例如不活泼气体和形成气体存在的情况下进行 UV 曝光, 所述不活泼气体包括例如 He、Ar、Xe、N₂、或它们的混合物, 所述形成气体例如为 N₂/O₂。可选地, 化学活性气体可加入到不活泼气体中。化学活性气体的示例包括: H₂、CH₄、三甲基硅烷 (trimethylsilane)、乙烯或具有化学式 HSiRR₁R₂ 的硅烷衍生物, 其中 R、R₁ 和 R₂ 可以相同或不同且选自甲基、乙基、丙基、乙烯基、丙烯基、甲氧基和乙氧基构成的组。

所述两种不同相的材料优选地具有不同的蚀刻选择性。在优选实施例中, 第二相 (B) 232 比第一相 (A) 231 具有更高的耐蚀刻性 (etching-resistance)。如图 2D (b) 所示, 相分离仅局部地发生于具有亲水表面的第二层材料 203 上方。该局部相分离也由形貌特征导致, 该形貌特征归因于帽层 211 和第二层材料 203 之间的高度差。

该局部相分离也由两相光致抗蚀剂 221 与第二层材料 203 (相分离发生处) 之间和两相光致抗蚀剂 221 与帽层 211 (不发生相分离处) 之间不同的界面特性引起。为了提高后面的蚀刻选择性, 可选地在下一处理步骤之前从表面去除第一相 (A) 231。去除步骤可以是湿法、等离子体或其它化学相关工艺。可以使用的湿法化学剥离工艺的示例是使用氢氧化四甲基铵 (TMAH) 作为化学蚀刻剂的工艺。

现在参照图 2E, 示出通过 RIE 工艺从围绕帽层 211 的分离的两相光致抗蚀剂到下面的绝缘体 201 的图案转移。该 RIE 蚀刻导致在两相分离的光致抗蚀剂下面的绝缘材料 201 中形成柱形气隙结构 240。帽层 211 下面的绝缘材料 201 不受影响。可选地以不同取向重复上述抗蚀剂沉积、相分离以及 RIE 工艺以产生网状气隙结构, 从而进一步减小最终的电容率 (dielectric capacitance)。由于第二相材料 (B) 232 比第一相材料 (A) 231 具有更高的蚀刻选择性, 所以第一相材料 (A) 231 将在 RIE 期间蚀刻掉, 因而留下散

布在第二相材料 (B) 232 中的柱形气隙。

现在参照图 2F, 第二绝缘体材料 251 然后沉积在柱形气隙结构 240 和帽层 211 的表面上以用于进一步处理。优选地, 第二绝缘体层 251 是低 k 材料。在图 2F(a) 所示的实施例中, 所沉积的第二绝缘体材料 251 填充柱形间隙从而产生双 k 电介质材料 (two-k dielectric material) 241。在这种情况下, 第二绝缘体 251 的介电常数小于第一绝缘体 201 的介电常数从而得到总体上较低的 k 值。

在图 2F(b) 所示的优选实施例中, 所沉积的第二绝缘体 252 不填充柱形气隙, 留下气隙在最终结构 240 中。

对于本领域技术人员而言显然的是, 在不偏离本发明精神的情况下, 可以超出这里具体描述的实施例而对本发明进行其它修改。因此, 这些修改也落在所附权利要求完全限定的本发明的范围内。

工业适用性

本发明可应用于制造半导体器件期间在电介质层中产生气隙。

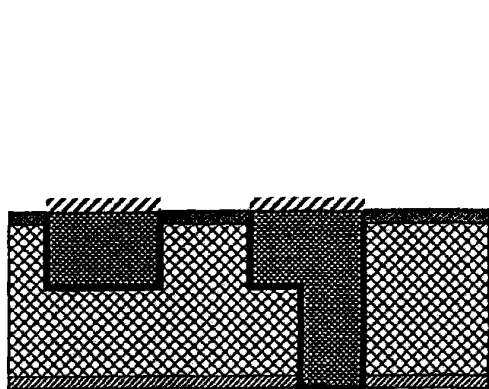


图 1A
现有技术

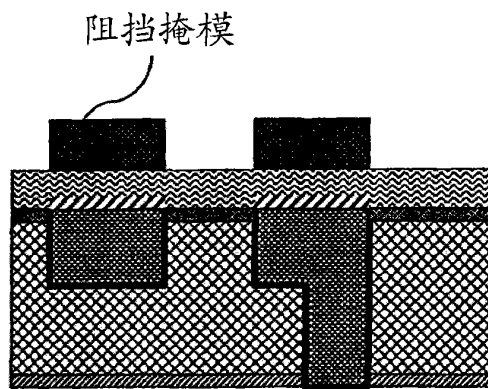


图 1C

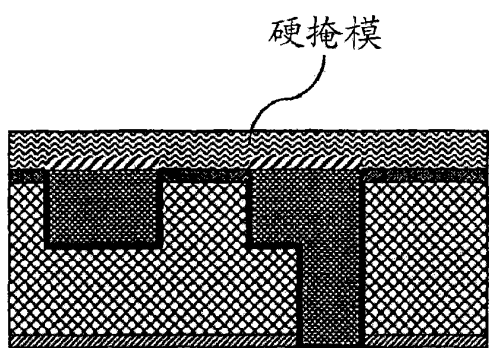


图 1B

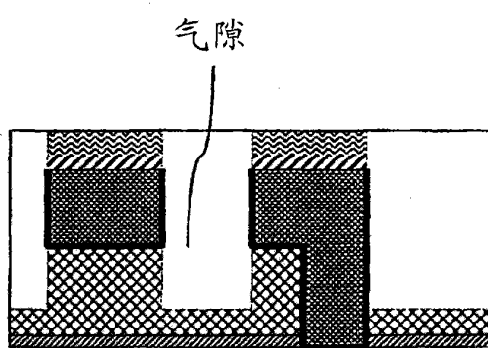


图 1D

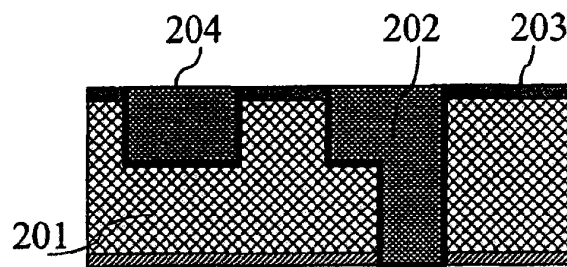


图 2A

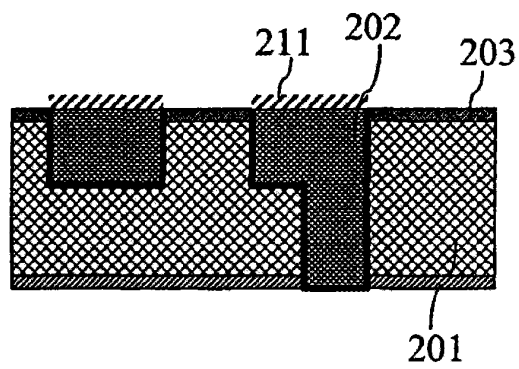


图 2B

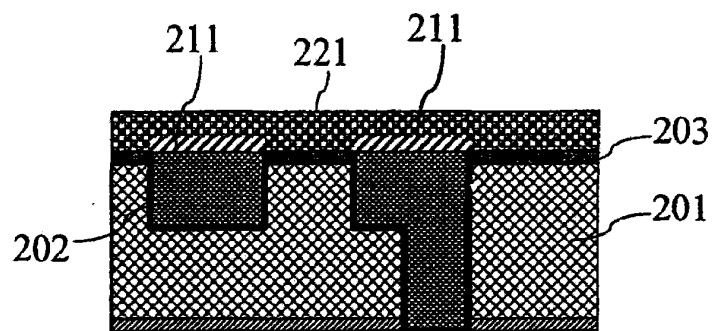


图 2C

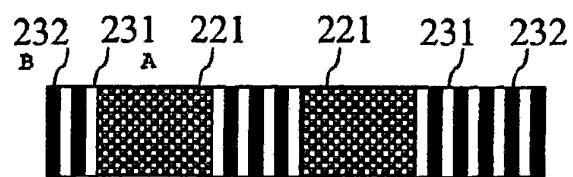


图 2D(a)

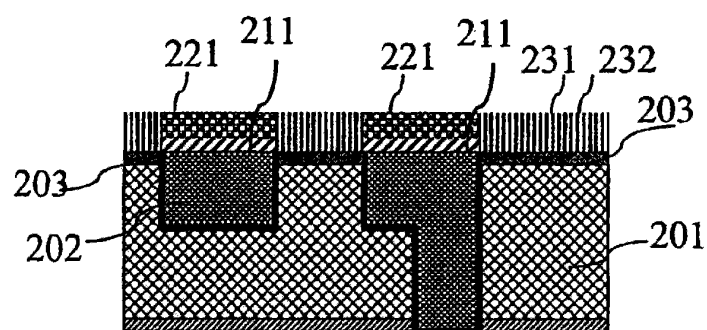


图 2D(b)

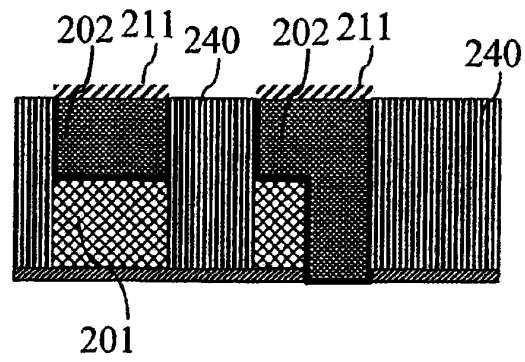


图 2E

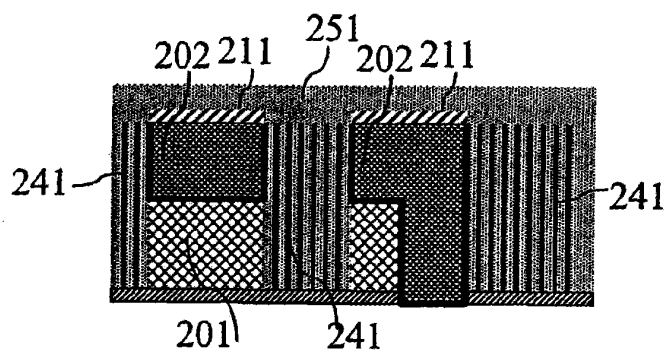


图 2F(a)

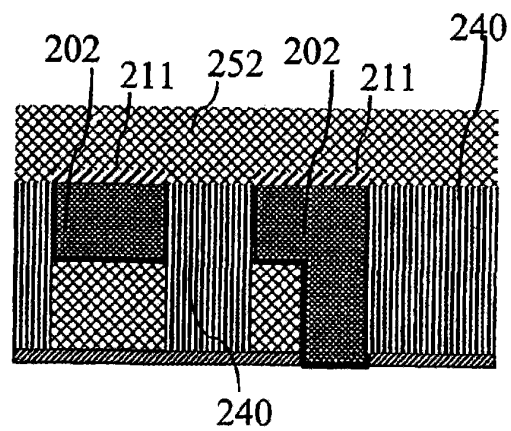


图 2F(b)

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Applicant	INTERNATIONAL BUSINESS MACHINES CORPORATION.
Rightholder	INTERNATIONAL BUSINESS MACHINES CORPORATION.

발명의 명칭

이중 라이너 캡핑층 상호접속 구조물

Title of Invention

DUAL LINER CAPPING LAYER INTERCONNECT STRUCTURE

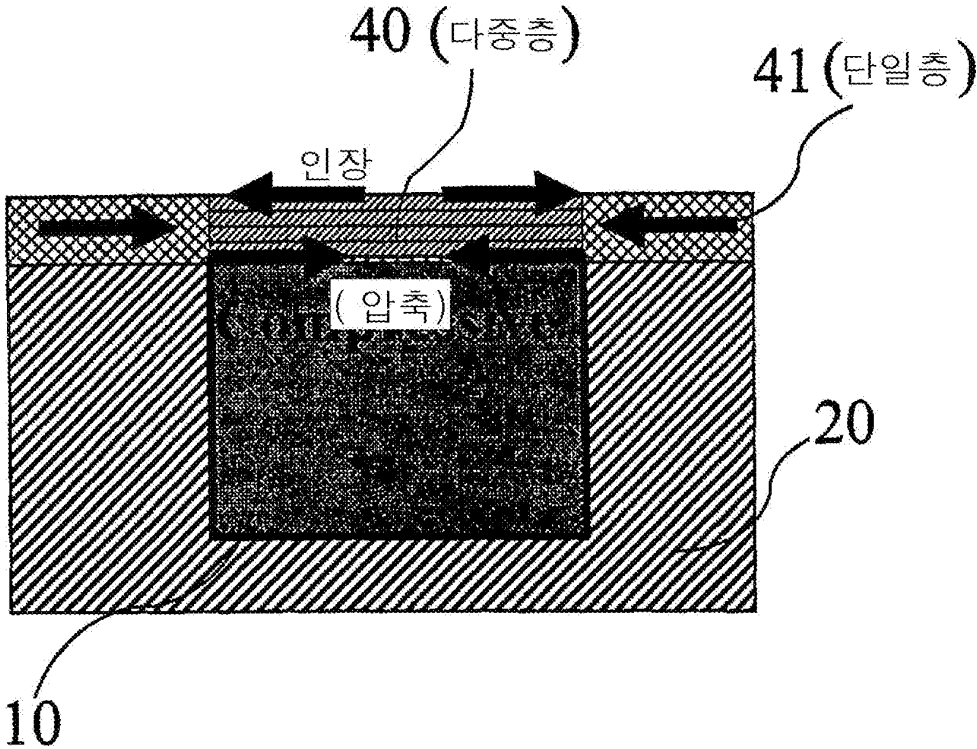
요약

본 발명은 Cu/유전체 계면에서 Cu 수송 및 원자 튕을 감소시키기 위하여 Cu 상호접속 상에 있는 고 인장 스트레스 캡핑층에 관한 것이다. 상기 고 인장 유전체 필름은 얇은 유전체 물질의 다중층을 증착하는 것으로 형성되고, 각각의 층은 대략 50 Å (5 nm) 이하의 두께이다. 각각의 유전체 층은 유전체 캡이 내부 인장 스트레스를 갖도록 각각의 후속 유전체층을 증착하기 전에 플라즈마 처리된다.
유전체, 인장, 구리 상호접속

Abstract

The present invention relates to the high tensile stress capping layer which has on the Cu interconnection it reduces the Cu transportation and atom gap in the Cu / dielectric interface. It is formed that the multi layer of a dielectric material in which the high elasticity dielectric film is thin is deposited and each layer is approximately, the thickness less than 50 Å (5nm). Before each dielectric layer deposits each following dielectric layer so that the dielectric material cap has the inside tensile stress it is plasma processed.
The dielectric, the extension, and the copper interconnect .

대표도면 (Representative drawing)



청구의 범위

청구 1항:

반도체 소자에 있어서, 적어도 하나의 전도성 상호접속이 부분적으로 내재된 유전체층; 상기 적어도 하나의 전도성 상호접속과 접촉하는 다중 증착 인장 캡핑층; 및 상기 유전체층과 접촉하고 상기 인장 캡핑층과 동일 평면 상에 있는 압축성 캡핑층을 포함하는 반도체 소자.

청구 2항:

제1항에 있어서, 상기 적어도 하나의 전도성 상호접속을 부분적으로 둘러싸는 확산장벽층을 더 포함하는 반도체 소자

청구 3항:

제1항에 있어서, 상기 인장 캡핑층은 순차적으로 증착된 층들로 구성되는 것인 반도체 소자.

청구 4항:

제1항에 있어서, 상기 인장 캡핑층은 이산화규소(SiO_2), 질화규소(Si_3N_4), 및 $\text{SiC}_x\text{N}_y\text{H}_z$ 의 규소 화합물(여기서, x, y 및 z는 가변적인 백분율이다)로 이루어진 군에서 선택된 물질로 구성되는 것인 반도체 소자.

Scope of Claims

Claim 1:

The semiconductor device including the dielectric layer, the multiple deposition extension capping layer contacting at least one conductive phase call connected, and the compressibility capping layer contacting the dielectric layer and has on the same plane as the extension capping layer as to the semiconductor device, and as to the dielectric layer, at least one conductive phase call connected is partly input.

Claim 2:

As for claim 1, the semiconductor device which further includes the diffusion barrier layer surrounding at least one conductive phase call connected

Claim 3:

As for claim 1, the semiconductor device consisting of layers in which the successively the extension capping layer is deposited.

Claim 4:

As for claim 1, the semiconductor device in which the extension capping layer consists of silicon dioxide (SiO_2), silicon nitride (Si_3N_4), and the material selected from the group consisting of silicide (the here the x, and the y and z are the variable percentage) of the $\text{SiC}_x\text{N}_y\text{H}_z$ and silicon nitride ($\text{Si}(\text{SB})_3/(\text{SB})\text{N}(\text{SB})_4/(\text{SB})$).

청구 5항:

제1항에 있어서, 상기 적어도 하나의 전도성 상호접속은 알루미늄, 구리, 텅스텐, 실버, 골드, 알루미늄-구리 및 니켈로 이루어진 군에서 선택된 물질로 구성되는 반도체 소자.

청구 6항:

반도체 소자의 제조방법에 있어서, 적어도 하나의 전도성 상호접속이 부분적으로 내재된 유전체층을 제공하는 단계 — 상기 적어도 하나의 전도성 상호접속의 상부 표면은 상기 유전체층의 표면과 실질적으로 동일 평면임 — ; 상기 유전체층 및 상기 적어도 하나의 전도성 상호접속 상에 인장 캠핑층을 증착하는 단계 — 상기 인장 캠핑층은 상기 적어도 하나의 전도성 상호접속과 접촉함 — ; 상기 인장 캠핑층 상에 플라스마 처리를 수행하는 단계; 상기 유전체층 상에 상기 인장 캠핑층의 일부를 제거하는 단계 — 상기 인장 캠핑층은 상기 적어도 하나의 전도성 상호접속과 접촉하여 남아 있음 — ; 상기 인장 캠핑층 및 유전체층 상에 압축성 캠핑층을 증착하는 단계; 및 상기 압축성 캠핑층을 상기 인장 캠핑층으로부터 제거하는 단계 — 상기 압축성 캠핑층은 상기 유전체층 상에 형성되고 상기 인장 캠핑층 근처에 있음 — 를 포함하고, 상기 인장 캠핑층은 상기 유전체층 및 상기 적어도 하나의 전도성 상호접속 상에 적어도 2번의 순차적 증착 및 플라스마 처리 단계에 의해 증착된 다중 증착 캠핑층이고, 상기 인장 캠핑층은 상기 전도성 상호접속의 표면에서 압축성 스트레스를 가하는 반도체 소자의 제조방법.

청구 7항:

반도체 소자의 제조방법에 있어서, 적어도 하나의 전도성 상호접속이 부분적으로 내재된 유전체층을 제공하는 단계; 상기 유전체층 및 상기 적어도 하나의 전도성 상호접속 상에 압축성 캠핑층을 증착하는 단계; 상기 적어도 하나의 전도성 상호접속 상에서 상기 압축성 캠핑층의 일부를 제거하는 단계; 상기 압축성 캠핑층 및 상기 적어도 하나의 전도성 상호접속 상에 인장 캠핑층을 증착하는 단계; 및 상기 인장 캠핑층을 상기 압축성 캠핑층으로부터 제거하는 단계를 포함하고, 여기서, 상기 인장 캠핑층은 상기 압축성 캠핑층 및 상기 적어도 하나의 전도성 상호접속 상에 적어도 2번의 순차적 증착 및 플라스마 처리 단계에 의해 증착된 다중 증착 캠핑층인 반도체 소자의 제조방법.

청구 8항:

제6항 또는 제7항에 있어서, 상기 인장 캠핑층은 7 Torr(933 Pa)의 압력, 400℃의 온도, 및 600 Watts의 고주파 파워 및 0

Claim 5:

As for claim 1, the semiconductor device consisting of the material in which at least one conductive phase call connected is selected from the group consisting of the aluminum, copper, tungsten, silver, gold, aluminum-copper and nickel.

Claim 6:

As to the semiconductor element manufacturing method, the step and the step — compressibility capping layer removing the compressibility capping layer from the extension capping layer are formed on the dielectric layer and it remains in contact with at least one conductive phase call connected that the step: step — extension capping layer removing the part of the extension capping layer on the dielectric layer deposits the compressibility capping layer on — : extension capping layer and dielectric layer the step — extension capping layer in which it is the coplanar the top surface of the conductive phase call connected of the step — at least one providing the dielectric layer in which at least one conductive phase call connected is partly input substantially deposits the extension capping layer with the surface of the dielectric layer on — : dielectric layer and at least one conductive phase call connected contacts at least one conductive phase call connected of performing the plasma processing on — : extension capping layer it is in the extension capping layer vicinity it includes ; and the extension capping layer is the multiple deposition capping layer deposited on the dielectric layer and at least one conductive phase call connected with the sequential vapor deposition and plasma processing step of at least two times. The semiconductor element manufacturing method in which the extension capping layer adds the compressive stress on the surface of the conductive phase call connected.

Claim 7:

The semiconductor element manufacturing method in which it includes the step of providing the dielectric layer, the step of depositing the compressibility capping layer on the dielectric layer and at least one conductive phase call connected, the step of removing the part of the compressibility capping layer on at least one conductive phase call connected, the step of depositing the extension capping layer on the compressibility capping layer and at least one conductive phase call connected, and the step of removing the extension capping layer from the compressibility capping layer as to the semiconductor element manufacturing method ; and here the extension capping layer is the multiple deposition capping layer deposited on the compressibility capping layer and at least one conductive phase call connected with the sequential vapor deposition and plasma processing step of at least two times, and as to the step of, at least one conductive phase call connected is partly input.

Claim 8:

As for claim 6 or 7, the semiconductor element manufacturing method in which the extension capping l

Watts의 저주파 파워에서 화학 증기 증착법에 의해 증착되는 반도체 소자의 제조방법.

청구 9항:

제6항 또는 제7항에 있어서, 상기 인장 캡핑층은 이산화규소, 질화규소 및 $\text{SiC}_x\text{N}_y\text{H}_z$ 형태의 규소, 탄소, 질소 및 수소의 화합물(여기서, x , y 및 z 는 가변 백분율이다)로 이루어진 군에서 선택된 유전체 물질인 반도체 소자의 제조방법.

청구 10항:

제6항에 있어서, 상기 플라즈마 처리는 5 Torr(667 Pa)의 압력, 400℃의 온도, 및 500 Watts의 고주파 파워 및 0 Watts의 저주파 파워에서 처리되는 반도체 소자의 제조방법.

기술분야

본 발명은 반도체 집적 회로(IC#39#s)에 관한 것이며, 보다 상세하게는 백-엔드-오브-더-라인(BEOL) 상호접속 구조에 관한 것이다.

배경기술

구리 상호접속에서 계속적으로 보다 작은 크기로의 감소 및 저-k-유전체의 도입은 공정의 복잡성을 증가시키는 것에 부가하여 더 큰 관심을 받는 신뢰성 문제의 원인이 된다. 반도체 상호접속 구조물에서, 전기적 이동(Electromigration, EM)은 금속 파손 메카니즘(metal failure mechanism)으로 동일시되고 있다. EM은 매우 큰 규모의 집적(VLSI) 회로에 대한 심각한 신뢰성 문제이다.

Cu/유전체 계면을 따라 발생하는 전기적 이동 파손은 VLSI 회로 응용에서 주된 신뢰성 문제로서 동일시되고 있다. Cu 라인에서 대량 수송에 따라 금속 라인에서의 텅이 유전체, 예를 들면 Si_3N_4 , SiC 및 $\text{SiC}(\text{N},\text{H})$, 캡핑층 및 Cu의 계면을 따라 발생하는 것이 관찰되었다. Cu/유전체 계면에서 Cu 수송 및 원자 텅(atomic voiding)을 감소시키는 것은 신뢰성을 강화시키기 위한 반도체 산업에서 주된 목적이다.

도 1은 통상적인 상호접속 구조물의 단면도이다. 구리 상호접속(10)은 인터 레벨 유전체(inter level dielectric, ILD) 물질(20)로 형성된다. 이어서, 압축력이 있는 캡핑층(30)은 상호접속 구조물(10)과 ILD(20)의 노출된 표면 위에 형성된다. 도

ayer is deposited in the pressure of 7 Torr (933 Pa), and the low frequency power of the radio frequency power of the temperature of 400℃ and 600 Watts and 0 Watts with the chemical vapor deposition.

Claim 9:

As for claim 6 or 7, the semiconductor element manufacturing method which is a dielectric material in which the extension capping layer is selected from the group consisting of the silicon dioxide, the silicon of the $\text{SiC}_x\text{N}_y\text{H}_z$ form and silicon nitride, carbon, and compound (the here the x , and the y and z are the variable percentage) of hydrogen and nitrogen.

Claim 10:

As for claim 6, the semiconductor element manufacturing method in which the plasma processing is processed at the pressure of 5 Torr (667 Pa), and the low frequency power of the radio frequency power of the temperature of 400℃ and 500 Watts and 0 Watts.

Technical Field

The present invention relates to the semiconductor IC (integrated circuit) (IC's). And more specifically, it is about the back-end - of -, more, - line (BEOL) interconnect structure.

Background Art

The introduction of the reduction to the small size and low-K - dielectric in the copper interconnect is caused by the reliability problem it adds to increase the complexity of the process and of receiving the greater concern. In the semiconductor interconnect structure, the electromigration (Electromigration, EM) is regarded to the metal failure mechanism. EM is the serious reliability problem toward the integrated (VLSI) circuit of the large scale.

It is regarded as the reliability problem that the electromigration damage generated according to the Cu / dielectric interface is principal in the VLSI circuit application. In the Cu line, it was observed that the gap at the metal line was generated according to the bulk transportation according to the dielectric, for example, the Si_3N_4 , the SiC and $\text{SiC}(\text{N},\text{H})$, and the interface of the Cu and capping layer. In the Cu / dielectric interface, it is the purpose of being principal in the semiconductor industry for strengthening the reliability to reduce the Cu transportation and atom gap (atomic voiding).

Figure 1 is a cross-sectional view of the normal interconnect structure. The copper interconnect (10) is formed with the interlevel dielectric (inter level dielectric, ILD) material (20). Subsequently, the capping layer

1에서 보여지는 통상적인 상호접속 구조물에서, 단일 압축성 캡핑층(30)은 단일 CVD 증착 단계로 제공된다. 압축성 캡핑층은 대략 250 Å (25nm)의 전형적인 두께로 증착된다. 이 경우에서, 압축성 캡핑층은 Cu 상호접속 내에 인장 스트레스(tensile stress)를 초래한다. CVD 증착 파라미터는 전형적으로 대략 2.4 Torr(320 Pa)의 압력, 대략 400°C의 온도, 및 대략 1,170 Watts의 HF 파워, 대략 130 Watts의 LF 파워이다. 가스 조성 및 유속은 전형적으로 SiH₄ 대략 250 분당 스탠다드 큐빅 센티미터(sccm), N₂ 대략 19,000 sccm, 및 NH₃ 대략 1,300 sccm이다.

Cu/계면에서의 Cu 수송 및 원자 틈을 감소시키는 것은 Cu 상호접속에서 압축성 스트레스를 창출하는 것으로 본 발명에 개시된다. 인장 스트레스를 갖는 종래 기술에서의 Cu 상호접속에 비하여, 높은 압축성 스트레스를 갖는 Cu 상호접속은 보다 우수한 전기적 이동 저항 효과를 초래한다. Cu 상호접속의 상부에 인장 필름을 증착하고/하거나 Cu 상호접속 주변에 압축성 필름을 증착하는 것은 Cu 상호접속에서 높은 압축성 스트레스를 발생시키고, 이것은 Cu 상호접속에서 EM 저항을 개선시키는 데 이롭다는 것이 본 명세서에 또한 개시된다.

따라서, 본 발명의 목적은 Cu/유전체 계면에서 Cu 수송 및 원자 틈을 감소시키기 위하여 Cu 상호접속의 상부에 높은 인장 스트레스 캡핑층을 제공하는 것이다. 높은 인장 유전체 필름은 다층의 얇은 유전체 물질을 증착하는 것으로 형성되고, 각각의 층은 대략 50 Å (5nm) 이하의 두께이다. 각각의 유전체 층은 유전체 캡이 내부 인장 스트레스를 갖도록 각각의 어어지는 유전체층을 증착하기 전에 플라즈마 처리된다.

상세설명

본 발명은 전도성 상호접속이 부분적으로 내재된 유전체층; 및 전도성 상호접속과 접촉하는 인장 캡핑층을 포함하는 반도체 소자를 제공한다. 본 발명은 유전체층과 접촉하는 압축성 캡핑층을 더 포함한다. 반도체 소자는 전도성 상호접속을 부분적으로 둘러싸는 확산장벽층(diffusion barrier layer)을 더 포함할 수도 있다. 인장 캡핑층은 순차적으로 증착된 층들로 구성되는 것이 바람직하다.

인장 캡핑층은 이산화규소(SiO₂), 질화규소(Si₃N₄), 및 규소 화합물, 예를 들면, SiC_xN_yH_z (여기서, x, y 및 z는 가변적인 백분율이다)로 이루어진 군에서 선택된 물질로 구성되는 것이 바람직하다. 전도성 상호접속은 알루미늄, 구리, 텅스텐, 실

r (30) in which it has the compressive force is formed on the exposed surface of the ILD (20) and interconnect structure (10). In the normal interconnect structure which is seen in fig. 1, the single compressibility capping layer (30) is provided to the single CVD deposition step. The compressibility capping layer is deposited to approximately, the typical thickness of 250 Å (25nm). In this case, the compressibility capping layer causes the tensile stress within the Cu interconnection. The typically the CVD deposition parameter is approximately, the pressure of 2.4 Torr (320 Pa), approximately, the temperature of 400°C, approximately, the HF power of 1,170 Watts, approximately, the LF power of 130 Watts. The typically the gas melting and flux are the SiH₄, approximately, 250 per-minute standard cubic centimeter (sccm), and N₂, approximately, 19,000 sccm and NH₃, approximately, 1,300 sccm.

In the Cu interconnection the Cu transportation at the Cu / interface and atom gap is reduced, with the compressive stress is created it is disclosed in the invention. The electromigration resistance effect excellent than the Cu interconnection having the high compressive stress is caused in comparison with the Cu interconnection at the prior art having the tensile stress. The high compressive stress is generated in the Cu interconnection to deposit the extension film on the upper portion of the Cu interconnection and do or deposit the compressibility film on the Cu interconnection around and it is moreover disclosed in this specification to this improve the EM resistant in the Cu interconnection but beneficial.

Therefore, in the object of the present invention is the Cu / dielectric interface, in order to reduce the Cu transportation and atom gap the tensile stress capping layer high toward the upper portion of the Cu interconnection is provided. It is formed that the high extension dielectric film deposits thin a dielectric material of the multi layer and each layer is approximately, the thickness less than 50 Å (5nm). Before each dielectric layer deposits the connected dielectric layer so that the dielectric material cap has the inside tensile stress it is plasma processed.

Detailed Description

The invention provides the semiconductor device comprising the dielectric layer in which the conductive phase call connected is partly input and the extension capping layer contacting the conductive phase call connected. The compressibility capping layer in which the invention contacts the dielectric layer further is included. The diffusion barrier layer in which the semiconductor device partly surrounds the conductive phase call connected further can be included. It is the be desirable to consist of layers in which the successively the extension capping layer is deposited.

It is the be desirable that the extension capping layer consists of silicon dioxide (SiO₂(SB)₂(/SB)), the silicon nitride (Si(SB)₃(/SB)N(SB)₄(/SB)) and silicide, and the material selected from the group consisting of for example

바, 골드, 알루미늄-구리 및 니켈로 이루어진 군에서 선택된 물질로 구성되는 것이 바람직하다. 확산장벽층은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W, 및 WN으로 이루어진 군에서 선택된 물질로 구성되는 것이 바람직하다.

본 발명은 또한 전도성 상호접속이 부분적으로 내재된 유전체층을 제공하는 단계; 상기 유전체층 및 상기 전도성 상호접속 상에 인장 캡핑층을 증착하는 단계; 상기 인장 캡핑층 상에 플라즈마 처리를 수행하는 단계; 상기 유전체층 상에 상기 인장 캡핑층의 일부를 제거하는 단계; 상기 인장 캡핑층 및 상기 유전체층 상에 압축성 캡핑층을 증착하는 단계; 및 상기 압축성 캡핑층을 상기 인장 캡핑층으로부터 제거하는 단계를 포함하는 반도체 소자의 제조방법을 제공한다.

인장 캡핑층은 대략 7 Torr(933 Pa)의 압력, 대략 400℃의 온도, 및 대략 600 Watts의 고주파 파워 및 대략 0 Watts의 저주파 파워에서 화학 증기 증착법에 의해 증착되는 것이 바람직하다. 상기 화학 증기 증착법은 대략 150sccm의 SiH₄, 대략 8,000 sccm의 N₂, 및 대략 2,500 sccm의 NH₃의 가스 조성 및 유속을 포함한다.

상기 인장 캡핑층은 이산화규소, 질화규소 및 SiC_xN_yH_z 형태의 규소, 탄소, 질소 및 수소의 화합물(여기서, x, y 및 z는 가변 백분율이다)로 이루어진 군에서 선택된 유전체 물질이 바람직하다.

상기 플라즈마 처리는 대략 5 Torr(667 Pa)의 압력, 대략 400℃의 온도, 및 대략 500 Watts의 고주파 파워 및 대략 0 Watts의 저주파 파워에서이다. 상기 플라즈마 처리는 대략 40 초 동안 대략 8,000 sccm의 N₂의 가스 조성 및 유속을 포함한다. 상기 인장 캡핑층과 플라즈마 처리는 제자리(in situ)에서 수행되는 것이 바람직하다.

상기 압축성 캡핑층은 상기 인장 캡핑층으로부터 화학기계적 폴리싱으로 제거되는 것이 바람직하다. 상기 인장 캡핑층은 상기 유전체층과 상기 전도성 상호접속 상에 2이상의 후속 증착 및 플라즈마 처리 단계에 의한 증착된 다중 증착 캡핑층인 것이 바람직하다.

본 발명은 또한 전도성 상호접속이 부분적으로 내재된 유전체층을 제공하는 단계; 상기 유전체층 및 상기 전도성 상호접속 상에 압축성 캡핑층을 증착하는 단계; 상기 전도성 상호접속 상에서 상기 압축성 캡핑층의 일부를 제거하는 단계; 상기 압축성 캡핑층 및 상기 상호접속 상에 인장 캡핑층을 증착하는 단

e, SiC_xN_yH_z (the here the x, and the y and z are the variable percentage). It is the be desirable to consist of the material in which the conductive phase call connected is selected from the group consisting of the aluminum, copper, tungsten, silver, gold, aluminum-copper and nickel. It is the be desirable to consist of the material in which the diffusion barrier layer is selected from the group consisting of the ta, taN, ti, tiN, ru, ruN, ruTa, ruTaN, W and WN.

The invention further provides the semiconductor element manufacturing method comprising the step of providing the dielectric layer, the step of depositing the extension capping layer on the dielectric layer and conductive phase call connected, the step of performing the plasma processing on the extension capping layer, the step of removing the part of the extension capping layer on the dielectric layer, the step of depositing the compressibility capping layer on the extension capping layer and dielectric layer, and the step of removing the compressibility capping layer from the extension capping layer, and as to the step of, the conductive phase call connected is partly input.

It is the be desirable that the extension capping layer is deposited in approximately, the pressure of 7 Torr (933 Pa), approximately, the temperature of 400℃, approximately, the radio frequency power of 600 Watts, approximately, the low frequency power of 0 Watts with the chemical vapor deposition. The chemical vapor deposition comprises approximately, the SiH₄ of 150sccm, approximately, N₂ of 8,000 sccm, approximately, the gas melting of the NH₃ of 2,500 sccm, and the flux.

A dielectric material in which the extension capping layer is selected from the group consisting of the silicon dioxide, the silicon of the SiC_xN_yH_z form and silicon nitride, carbon, and compound (the here the x, and the y and z are the variable percentage) of hydrogen and nitrogen is the be desirable.

The plasma processing is in approximately, the pressure of 5 Torr (667 Pa), approximately, the temperature of 400℃, approximately, the radio frequency power of 500 Watts, approximately, the low frequency power of 0 Watts. The plasma processing includes approximately, 40 second, approximately, the gas melting of N₂ of 8,000 sccm and the flux. It is the be desirable that the extension capping layer and plasma processing are performed in the proper place (in situ).

It is the be desirable that the compressibility capping layer is removed from the extension capping layer to the chemical mechanical polish. The extension capping layer is the be desirable on the dielectric layer and conductive phase call connected the deposited multiple deposition capping layer by the succession deposition more than 2 and plasma processing step.

The invention further provides the semiconductor element manufacturing method comprising the step of providing the dielectric layer, the step of depositing the compressibility capping layer on the dielectric layer and conductive phase call connected, the step of remov

계; 및 상기 인장 캡핑층을 상기 압축성 캡핑층으로부터 제거하는 단계를 포함하는 반도체 소자의 제조방법을 제공한다.

상기 인장 캡핑층은 대략 7 Torr(933 Pa)의 압력, 대략 400℃의 온도, 및 대략 600 Watts의 고주파 파워 및 대략 0 Watts의 저주파 파워에서 화학 증기 증착법에 의해 증착되는 것이 바람직하다. 상기 화학 증기 증착법은 대략 150sccm의 SiH₄, 대략 8,000 sccm의 N₂, 및 대략 2,500 sccm의 NH₃의 가스 조성 및 유속을 포함한다.

상기 인장 캡핑층은 이산화규소, 질화규소 및 SiC_xN_yH_z 형태의 규소, 탄소, 질소 및 수소의 화합물(여기서, x, y 및 z는 가변 백분율이다)로 이루어진 군에서 선택된 유전체 물질이 바람직하다. 상기 플라즈마 처리는 대략 5 Torr(667 Pa)의 압력, 대략 400℃의 온도, 및 대략 500 Watts의 고주파 파워 및 대략 0 Watts의 저주파 파워에서이다. 상기 플라즈마 처리는 대략 40 초 동안 대략 8,000 sccm의 N₂의 가스 조성 및 유속을 포함한다. 상기 인장 캡핑층과 상기 플라즈마 처리는 제자리(in situ)에서 수행되는 것이 바람직하다.

상기 압축성 캡핑층은 상기 인장 캡핑층으로부터 화학기계적 폴리싱으로 제거되는 것이 바람직하다. 상기 인장 캡핑층은 상기 유전체층과 상기 전도성 상호접속 상에 2이상의 후속 증착 및 플라즈마 처리 단계에 의한 증착된 다중 증착 캡핑층인 것이 바람직하다.

도면에 대한 간단한 설명

본 발명은 첨부하는 도면을 예시로서만 참조하여 더욱 상세히 설명된다.

도 1은 통상적인 상호접속 구조를 보여주는 개략적인 단면도이다.

도 2는 본 발명의 바람직한 구현예를 보여주는 개략적인 단면도이다.

도 3 내지 12는 본 발명에 따른 바람직한 구조를 보여주는 개략적인 단면도이다.

실시예

이어지는 설명에서, 다양한 특정 항목, 예를 들면, 특정 구조, 성분, 물질, 크기, 공정 단계 및 기술이 본 발명의 철저한 이해를 제공하기 위해 설명된다. 그러나, 당업자들에게 의해 이들 특정 항목 없이 본 발명을 실시할 수 있다고 이해될 것이다. 다른 예에서, 잘 알려진 구조 또는 공정 단계는 발명을 애매하게 하는 것을 피하기 위하여 상세히 설명되지 않는다.

ing the part of the compressibility capping layer on the conductive phase call connected, the step of depositing the extension capping layer on the compressibility capping layer and interconnection, and the step of removing the extension capping layer from the compressibility capping layer, and as to the step of, the conductive phase call connected is partly input.

It is the be desirable that the extension capping layer is deposited in approximately, the pressure of 7 Torr (933 Pa), approximately, the temperature of 400℃, approximately, the radio frequency power of 600 Watts, approximately, the low frequency power of 0 Watts with the chemical vapor deposition. The chemical vapor deposition comprises approximately, the SiH₄ of 150sccm, approximately, N₂ of 8,000 sccm, approximately, the gas melting of the NH₃ of 2,500 sccm, and the flux.

A dielectric material in which the extension capping layer is selected from the group consisting of the silicon dioxide, the silicon of the SiC_xN_yH_z form and silicon nitride, carbon, and compound (the here the x, and the y and z are the variable percentage) of hydrogen and nitrogen is the be desirable. The plasma processing is in approximately, the pressure of 5 Torr (667 Pa), approximately, the temperature of 400℃, approximately, the radio frequency power of 500 Watts, approximately, the low frequency power of 0 Watts. The plasma processing includes approximately, 40 second, approximately, the gas melting of N₂ of 8,000 sccm and the flux. It is the be desirable that the extension capping layer and plasma processing are performed in the proper place (in situ).

It is the be desirable that the compressibility capping layer is removed from the extension capping layer to the chemical mechanical polish. The extension capping layer is the be desirable on the dielectric layer and conductive phase call connected the deposited multiple deposition capping layer by the succession deposition more than 2 and plasma processing step.

Brief explanation of the drawing

The invention relates to the example drawing attached. And it refers and it is more particularly explained.

Figure 1 is a summary cross-sectional view showing the interconnect structure of being normal.

Figure 2 is a summary cross-sectional view showing the implementation doing with the desirable of the invention.

Figures 3 through 12 are the summary cross-sectional view showing the structure of doing with the desirable according to the present invention.

Example(s)

In the connected description, the various particular item, for example, the specific scheme, component, material, size, processing stage and technology are explained in order to provide the understanding of being thorough of the invention. But person skilled in the arts will make out because of performing the invention without these particular items. In the dissimilar example, so tha

t the well known structure or the processing stage avoid making the invention confusing it is not explained.

층, 영역 또는 기판과 같은 부재가 다른 부재 #34#상(on) #34# 또는 #34#위(over) #34#로 언급되는 경우, 이것은 다른 부재상에 직접적으로 있을 수 있거나 또는 개재 부재(intervening elements)가 존재할 수도 있다고 이해되어질 것이다. 반면에, 부재가 다른 부재 #34#상에 직접적으로(directly on) #34# 또는 #34#위에 직접적으로(directly over) #34#로 언급되는 경우, 개재 부재가 존재하지 않는다. 또한, 부재가 다른 부재 #34#밑(beneath) #34# 또는 #34#아래(under) #34#로 언급되는 경우, 이것은 다른 부재 밑에 또는 아래에 직접적으로 있을 수 있거나 또는 개재 부재가 존재할 수 있다고 이해되어질 것이다. 반면에서, 부재가 다른 부재 #34#밑에 직접적으로(directly beneath) #34# 또는 #34#아래에 직접적으로(directly under) #34#로 언급되는 경우, 개재 부재가 존재하지 않는다.

It directly can have on the case of being mentioned in the member " phase (on) in which the layer, and the member such as the domain and substrate are different in the " (over) with 34, and the member in which this is different or because the interposing member (intervening elements) can be existent it is understood. On the other hand, the case of being mentioned in the member " phase in which the member is different to the direct (directly on) in the " the upper part to the direct (directly over) with 34, and the interposing member are nonexistent. Moreover, the of being mentioned in the member " bottom (beneath) in which the member is different to the #34 # (under) " with 34 case directly can have or because the interposing member can be existent or it is understood under the case, and the member in which this is different. In the other side, the case of being mentioned in the member " bottom in which the member is different to the direct (directly beneath) in the " lower part to the direct (directly under) with 34, and the interposing member are nonexistent.

본 발명의 바람직한 구현에는 도 2에 나타내어진다. 다중 증착 인장 캠핑층(40)은 구리 상호접속(10) 상에만 형성된다. 단일 증착 압축성 캠핑층(41)은 ILD(20) 표면에서만 형성된다. 본 발명에서, 특정적으로 맞추어진 CVD 증착 파라미터는 상호접속 상에 인장 스트레스 캠핑 층을 제공하기 위해 캠핑층 증착 사이에 후반 증착 표면 처리와 조합해서 사용된다. 바람직한 구현예에서, 단일 증착은 대략 50 Å(5nm) 미만으로 증착될 것이다. 바람직한 구현예에서, 다중층 인장 캠핑층(40)은 3번 이상의 후속적으로 증착되고 처리된 층들로 구성된다.

The implementation doing with desirable of the invention is shown in fig. 2. The multiple deposition extension capping layer (40) is formed on the copper interconnect (10). The single deposition compressibility capping layer (41) is formed at the ILD (20) surface. In the present invention, so that the characteristically adjusted CVD deposition parameter provide the tensile stress capping layer on the interconnection, it assembles between the capping layer deposition with the latter half deposition surface processing and the interconnection is used. In the implementation doing with desirable, the single deposition will be deposited to approximately, 50 Å (5nm) under. In the implementation doing with desirable, the multi layer extension capping layer (40) consists of the layer which is deposited to the subsequently and is processed more than three times.

도 3을 참조하여, 본 발명의 바람직한 구현예를 보다 상세히 설명한다. 도 3은 다수의 금속 상호접속이 패턴화된 개구부에 형성된 전도성 상호접속 물질(101)에 의해 제공되는 미소전자(microelectronic) 부재 또는 칩의 일부의 개략적인 단면도이다. 도 3은 인터레벨(interlevel) 유전체층 또는 #34#ILD#34#(102)가 형성되고 있는 제작 단계를 보여준다.

Referring to Figure 3, the implementation doing with desirable of the invention is more particularly illustrated. Figure 3 is a summary cross-sectional view of the microelectronic member or the chip it is provided by the conductivity interconnect material (101) formed in the opening part in which multiple metal interconnects are patterned. Figure 3 shows the manufacture process that at the interlevel dielectric layer or the "ILD#34 # (102) is formed.

상기 ILD(102) 물질은 SiCOH 또는 SiLK와 같은 저-k 물질이 바람직하다. 상기 ILD(102) 물질은 전형적으로 대략 4.0 또는 그 미만의 유전 상수, 보다 전형적으로 대략 2.8 또는 그 미만의 유전 상수를 갖는다. 본 명세서에서 언급된 모든 유전 상수는 다르게 표시되지 않는 이상 진공에 관한 것이다. 이들 유전체들은 일반적으로 4.0 이상의 높은 유전 상수를 갖는 유전체 물질과 비교하여 보다 낮은 기생 크로스 토크(lower parasitic cross talk)를 갖는다.

The low-K material such as the SiCOH and SiLK the ILD (102) material is the be desirable. The ILD (102) material typically more typically has approximately, the dielectric constant of 2.8 or less than the with approximately, the dielectric constant of 4.0 or less than the . All dielectric constants mentioned by this specification relates to the vacuum it is not differently indicated. These dielectrics has a dielectric material generally having the high dielectric constant more than 4.0 and the low parasitism cross-talk (lower parasitic cross talk) comparing but.

ILD(102) 내에, 다수의 패턴화된 개구부가 전형적으로 유전체층(102)의 상부 표면에 의해 한정된 주표면(105)의 방향으로

It is provided within the ILD (102) in the form of the line pattern which it horizontally extends in such surface

수직으로 연장하는 또는 이런 표면에 수평으로 연장하는 라인 패턴의 형태로 제공된다. 각각의 패턴화된 개구부 내에, 확산 장벽 물질(103)이 각각의 개구부의 벽과 바닥을 따라서 증착되고, 이 후에 전도성 상호접속 물질(101)이 각각의 개구부 내의 남겨진 공간을 채우기 위해 증착된다. 이들 단계는 전형적으로 평면화 공정, 예를 들면, 화학기계적 폴리싱(#34#CMP#34#) 공정으로 이어지고, 이것은 패턴화된 개구부의 ILD(102) 외부면의 노출된 상부 표면(105)를 접촉하는 임의의 과량의 금속을 제거한다.

유전체층(102)에서 각각의 개구부를 채우는 전도성 상호접속 물질(101)은 바람직하게 금속, 예를 들면, 파괴-부식(destructive corrosion)이 잘되지 않고 우수한 전도성 특성을 갖는 귀금속이다. 그러나, 몇몇의 금속과 금속 합금은 집적된 회로 또는 칩의 BEOL 제작에서 전도성 상호접속 라인을 형성하기에 특히 적합한 것으로 두드러진다. 이런 금속은 알루미늄, 구리, 텅스텐, 실버, 골드, 알루미늄-구리 및 니켈을 포함한다. 특정 구현예에서, 유전체층(102)에서 패턴화된 개구부를 채우는 전도성 상호접속 물질(101)은 필수적으로 구리로 구성된다.

전도성 상호접속 물질(101)이 유전체 물질을 통해 확산하기 쉬운 구리 또는 다른 금속을 포함하는 경우, 즉, 금속이 #34#높은 확산계수#34#를 갖는 경우, 전도성 상호접속 물질(101)은 확산 장벽체로서 기능하는 금속 또는 금속 화합물의 층 위에 형성되는 것이 바람직하다. 확산 장벽 물질(103)은 구리가 전도성 상호접속 물질(101)로부터 금속 라인의 벽 및 바닥에 근접한 ILD(102)로 확산하는 것을 방지한다.

확산 장벽 물질(103)은 바람직하게 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W, WN 및 전도성 물질이 그것을 통과해 확산하는 것을 방지하는 장벽으로서 제공할 수 있는 임의의 다른 물질이다. 상기 확산 장벽 물질(103)은 장벽층(103)이 전도성 상호접속 물질(101)의 전도성 특성에 영향을 미치지 않거나, 또는 그의 유전체 특성에 영향을 미치는 ILD(102)의 유전체 물질과 상호작용하도록 전도성 상호접속 물질(101)과 상호작용하지 않는다. 증착은 증착 방법, 예를 들면, 원자층 증착법(ALD), 화학 증착법(CVD), 플라즈마 강화된 화학 증착법(P-ECVD), 스퍼터링, 화학적 용액 증착 또는 플레이팅(plating)으로 형성된다.

미도시된 기판은 반도체성 물질, 절연성 물질, 전도성 물질 또는 이들의 임의의 조합을 포함할 수도 있다. 기판이 반도체성 물질로 구성되는 경우, 임의의 반도체, 예를 들면, Si, SiGe, SiGeC, SiC, Ge 합금, GaAs, InAs, InP 및 기타 III/V 또는 I

e which it perpendicularly extends as the direction of the major surface (105) in which multiple patterned opening parts are typically restricted by the top surface of the dielectric layer (102). Under barrier metal (103) is deposited within the patterned opening part according to wall and bottom surface of each opening part and so that the conductivity interconnect material (101) fill up the space remaining within each opening part it is deposited to the then. These steps are typically connected to the planarization step, for example, the chemical mechanical polish ("CMP") process and the metal of the arbitrary excess of quantity contacting the exposed top surface (105) of the ILD (102) external side of the opening part in which this is patterned is removed.

In the dielectric layer (102), it is the precious metal in which preferably the conductivity interconnect material (101) filling up each opening part the metal, for example, the break down - corrosion (destructive corrosion) does not go well and having the conductive property of being excellent. But in the BEOL manufacture of the several metal and the circuit in which the metal alloy is integrated or the chip, it is prominent that it is especially suitable because of forming the conductivity interconnect lines. Such metal comprises aluminum, the copper, tungsten, silver, gold, the aluminum-copper, and nickel. In the specific implementation example, the obligatorily the conductivity interconnect material (101) filling the patterned opening part in the dielectric layer (102) consists of the copper.

The copper easy the conductivity interconnect material (101) diffuses through a dielectric material or the case, of including the dissimilar metal in other words, the metal is the "are in that case, it has the diffusion coefficient", and the conductivity interconnect material (101) are the be desirable it is formed on the layer of the metal functioning as the diffusion barrier or the metal compound. Under barrier metal (103) prevents the copper from diffusing from the conductivity interconnect material (101) to the ILD (102) near to wall and bottom surface of the metal line.

Under barrier metal (103) is the dissimilar material can provide as the obstacle which prevents preferably the Ta, the TaN, the Ti, the TiN, the Ru, the RuN, the RuTa, the RuTaN, W, WN and conductive material passing that and diffusing. Under barrier metal (103) the barrier (103) does not affect the conductive property of the conductivity interconnect material (101) or it or does not interact with the conductivity interconnect material (101) in order to interact with a dielectric material of the ILD (102) affecting its dielectric property. The deposition is formed with ***, for example, the atomic layer deposition (ALD), the chemical vapor deposition technique (CVD), the chemical vapor deposition technique (P-ECVD), which plasma is enhanced the sputtering, and the chemical solution deposition or the plating.

The substrate which is not shown comprises the semiconductor type material, the insulating material, the conductive material, or their arbitrary combination. The case where the substrate is made up of the semico

I/VI 화합물 반도체가 사용될 수 있다. 이들 나열된 유형의 반도체성 물질 이외에도, 본 발명은 반도체 기판이 층을 이룬 반도체, 예를 들면, Si/SiGe, Si/SiC, 실리콘-온-인슐레이터(SOIs) 또는 실리콘 게르마늄-온-인슐레이터(SGOIs)인 경우도 포함한다.

기판이 절연 물질인 경우, 절연 물질은 유기 절연체, 무기 절연체 또는 이들의 다층을 포함하는 조합물이 될 수 있다. 기판이 전도성 물질인 경우, 기판은 예를 들면, 폴리Si, 원소 금속, 원소 금속들의 합금, 금속 규화물, 금속 질화물 이들의 다층을 포함하는 조합물을 포함할 수 있다. 기판이 반도체성 물질을 포함하는 경우, 하나 이상의 반도체 소자, 예를 들면, 상보성 금속 산화물 반도체(CMOS) 소자가 그 위에 제작될 수 있다. 기판이 절연체 물질과 전도성 물질의 조합물을 포함하는 경우, 기판은 다층을 이룬 상호접속 구조의 보다 낮은 상호접속 레벨을 나타낼 수 있다.

도 4를 참조하여 제 1 유전체 캡핑층(215)의 증착을 설명한다. 바람직한 구현예에서, CVD 증착 파라미터는 대략 7 Torr(933 Pa)의 압력, 대략 400℃의 온도, 및 대략 600 Watts의 HF 파워 및 대략 0 Watts의 LF 파워이다. 가스 조성과 유속 대략 150sccm의 SiH₄, 대략 8,000 sccm의 N₂, 및 대략 2,500 sccm의 NH₃이다.

제 1 유전체 캡핑층(215)는 금속 채워진 라인 패턴에 상대적인 스트레스를 유지할 수 있는 임의의 유전체 물질 또는 유전체 물질의 조합물을 포함할 수 있다. 바람직하게, 제 1 유전체 캡핑층(215)는 일종 이상의 유전체 물질 또는 이산화규소(SiO₂), 질화규소(Si₃N₄), 다른 유전체 규소 화합물, 예를 들면, SiC_xY_yN_z(여기서, x, y 및 z는 가변적인 백분율이다)로 이루어진 군에서 선택된 유전체 물질들의 조합물로 필수적으로 구성된다.

증착 후, 제 1 유전체 캡핑층(215)은 연장된 시간, 고온 및 고주파 플라즈마 처리를 바람직하게 암모니아 및 질소 종(NH₃ 및 N₂) 또는 선택적으로 수소(H₂)를 사용하여 겪게 된다. 바람직한 구현예에서, 플라즈마 처리 파라미터는 대략 5 Torr(667 Pa)의 압력, 대략 400℃의 온도, 및 대략 500 Watts의 HF 파워 및 대략 0 Watts의 LF 파워이다. 상기 가스 조성과 유속은 대략 8,000 sccm의 N₂이다. 상기 플라즈마 처리는 대략 40초 동안이다.

유전체 캡 증착 및 후속 플라즈마 처리는 제자리에서, 즉 동일

ductor type material, and the arbitrary semiconductor, for example, the Si, the SiGe, the SiGeC, the SiC, the Ge alloy, the GaAs, the InAs, the InP and the other II / V or the II / VI compound semiconductor can be used. Even in case the invention is the semiconductor, in which the semiconductor substrate is comprised the layer for example, the Si / SiGe, the Si / SiC, and the silicon-on-insulator (SOIs) or the silicon germanium on insulator (SGOIs) it includes besides the semiconductor type material enumerated with these of the type.

In case the substrate is the insulation material it can become the combination in which the insulation material includes organic insulator, and the inorganic insulator or their multi layer. The substrate may include the combination in which in case it is the conductive material the substrate includes for example, the poly Si, the elemental metal, the alloy of the elemental metals, the metal silicide, and the metal-nitride their multi layer. At least one semiconductor device, for example, the complementary metal oxide semiconductor (CMOS) device of the substrate can be the semiconductor type material manufactured in case the includes in the upper part. The substrate can show the lower interconnect level of the interconnect structure where the substrate is comprised the multi layer the combination of the conductive material and insulation material in case the includes.

The deposition of the first dielectric capping layer (215) is illustrated with reference to fig. 4. In the implementation doing with desirable, the CVD deposition parameter is approximately, the pressure of 7 Torr (933 Pa), approximately, the temperature of 400℃, approximately, the HF power of 600 Watts, approximately, the LF power of 0 Watts. It is the gas melting and flux, approximately, the SiH₄ of 150sccm, approximately, N₂ of 8,000 sccm, approximately, the NH₃ of 2,500 sccm.

The combination of the arbitrary a dielectric material maintaining the relative stress even the line pattern in which the first dielectric capping layer (215) is filled with metal or the dielectric material is include might. Preferably, the obligatorily the first dielectric capping layer (215) consists of the combination of a dielectric material selected from the group consisting of a dielectric material more than the kind or the silicon dioxide (SiO₂(S B)2(/SB)), the silicon nitride (Si(SB)3(/SB)N(SB)4(/SB)), and the dissimilar dielectric silicide, for example, SiC_xY_yN_z (the here the x, and the y and z are the variable percentage).

Preferably the time when the first dielectric capping layer (215) is extended, and the high temperature and radio frequency plasma processing are selectively undergone after the deposition as ammonia and nitrogen species (the NH₃ and N₂) using the hydrogen (H(SB)2(/SB)). In the implementation doing with desirable, the plasma processing parameter is approximately, the pressure of 5 Torr (667 Pa), approximately, the temperature of 400℃, approximately, the HF power of 500 Watts, approximately, the LF power of 0 Watts. The gas melting and flux are approximately, N₂ of 8,000 sccm. The plasma processing is for approximately, 40 second.

In the dielectric material cap deposition and after

한 공정 챔버에서 또는 하나 이상의 연결된 챔버들을 갖는 동일한 툴 안에서 수행되는 것이 바람직하다. 이런 방식에서, ILD의 표면을 플라즈마 처리 후에 유전체 캡을 증착하기 위해 챔버로부터 기판을 수동적으로 제거할 필요없이 수행된다. 바람직한 구현예에서, 제 1 유전체 캡 층(215)은 ILD(102)의 노출된 상부 표면 및 전도성 상호접속을 덮기 위해 대략 50 Å (5nm) 미만의 두께로 증착된다. 증착후, 제 1 절연체 캡 층(215)의 노출된 상부 표면(225)은 제 2 플라즈마 처리를 겪는다. 제 2 플라즈마 처리는 인장 스트레스를 제 1 유전체 캡 층(215)에 나누어주는 효과를 갖는다.

plasma treatment is the proper place, or it that is is the e be desirable in the same processing chamber to be p erformed in the same tool having connected chambers. In such mode, it is the surface of ILD performed without the need to manually remove the substrate from the chamber in order to deposit the dielectric material cap after the plasma processing. In the implementation doing with desirable, so that the first dielectric cap layer (215) cover the top surface and the exposed conductive phase call connected of the ILD (102) it is deposited to approximately, the thickness less than 50 Å (5nm). The exposed top surface (225) of the first insulator cap layer (215) undergoes the second plasma processing after the deposition. It has the effect that the second plasma processing distributes the tensile stress to the first dielectric cap layer (215).

도 5(a) 내지 도 5(b)를 참조하면, 제 2 유전체 캡핑 층(226)은 제 1 유전체 캡핑층(215)의 노출된 상부 표면(225)을 덮기 위해 증착된다. 제 1 유전체 캡핑층(215)과 마찬가지로, 제 2 유전체 캡핑층(226)은 바람직하게 약 50 Å (5nm) 미만의 두께로 증착된다. 제 1 유전체 캡핑층(215)과 마찬가지로, 제 2 유전체 캡핑층(226)은 스트레스를 유지할 수 있는 임의의 유전체 물질 또는 유전체 물질들의 조합물을 포함할 수 있다. 바람직하게, 제 2 유전체 캡핑층(226)은 일종 이상의 유전체 물질 또는 이산화규소, 질화규소 및 SiC_xN_yH_z의 형태로 규소, 탄소, 질소 및 수소의 화합물(여기서, x, y 및 z는 가변적인 백분율이다)로 이루어진 군에서 선택된 물질들의 조합물로 필수적으로 구성된다.

So that the second dielectric capping layer (226) cover the exposed top surface (225) of the first dielectric capping layer (215), Figure 5(a) is deposited with reference to 5 (b). The second dielectric capping layer (226) is deposited to the preferably like the first dielectric capping layer (215) to the thickness less than about 50 Å (5nm). The combination of the arbitrary a dielectric material in which the second dielectric capping layer (226) can maintain the stress or the dielectric materials is include might like the first dielectric capping layer (215). Preferably, the obligatorily the second dielectric capping layer (226) consists of the combination of the materials selected in the form of a dielectric material more than the kind or the silicon dioxide, and the silicon nitride and SiC_x N_y H_z from the group consisting of silicon, carbon, and compound (the here the x, and the y and z are the variable percentage) of hydrogen and nitrogen.

바람직하게, 제 2 유전체 캡핑층(226)은 제 1 유전체 캡 층과 동일한 유전체 물질로 필수적으로 구성된다. 제 1 유전체 캡핑 층(215)과 마찬가지로, 제 2 유전체 캡핑층(226)의 노출된 상부 표면(230)은 또한 증착 후에 바람직하게 제 1 유전체 캡핑 층(215)의 플라즈마 처리 동안 사용된 동일한 파라미터와 종(species)을 사용하여 증착된 제 2 유전체 캡핑층(226)의 인장 스트레스를 제어하기 위해 플라즈마 처리가 진행된다. 예를 들면, 플라즈마 처리는 반응성 종으로써 암모니아와 질소의 혼합물 또는 선택적으로 수소를 포함할 수 있다. 제 1 유전체 캡핑 층(215)의 경우에서와 같이, 이들 증착 및 플라즈마 처리 공정은 제자리에서 수행되는 것이 바람직하다.

Preferably, the obligatorily the second dielectric capping layer (226) consists of the same dielectric material as the first dielectric cap layer. In order to control the tensile stress of the second dielectric capping layer (226) deposited using the kind (species) and the same parameter in which preferably the exposed top surface (230) of the second dielectric capping layer (226) is used after moreover, the deposition for the plasma processing of the first dielectric capping layer (215), the plasma processing is progressed like the first dielectric capping layer (215). For example, the plasma processing comprises ammonia with the reactive species and the mixture of the nitrogen, selectively, hydrogen. In case of the first dielectric capping layer (215), it is the be desirable that these deposition and plasma treatment processes are together performed in the proper place.

추가로, 도 5(a) 내지 도 5(b)에 관하여, 제 2 유전체 캡핑 층(226)의 증착 및 플라즈마 처리에 이어서, 제 3 유전체 캡핑 층(236)이 제 2 유전체 캡핑층(226)의 노출된 상부 표면(230)을 덮기 위해 증착된다. 제 1 유전체 캡핑층(215) 및 제 2 유

Additionally, so that the third dielectric capping layer (236) cover the exposed top surface (230) of the second dielectric capping layer (226), Figure 5(a) is deposited about 5 (b) following the deposition and plasma pro

전체 캡핑층(226)과 마찬가지로, 제 3 유전체 캡핑층(236)은 약 50 Å 미만의 두께로 형성된다. 제 1 및 제 2 유전체 캡핑층(215, 226)과 마찬가지로, 제 3 유전체 캡핑층(236)은 스트레스를 유지할 수 있는 임의의 유전체 물질 또는 유전체 물질들의 조합물을 포함할 수 있다. 바람직하게, 제 3 유전체 캡핑층(236)은 하나 이상의 유전체 물질들 또는 이산화규소, 질화규소 및 SiC_xN_yH_z의 형태로 규소, 탄소, 질소 및 수소의 화합물로 이루어진 군에서 선택된 물질들의 조합물로 필수적으로 구성된다.

바람직하게, 제 3 유전체 캡핑층(236)은 제 1 및 제 2 유전체 캡핑층과 동일한 유전체 물질로 필수적으로 구성된다. 제 1 및 제 2 유전체 캡핑층에 수행된 플라즈마 처리에서와 같이, 제 3 유전체 캡핑층(236)의 노출된 상부 표면(240)은 증착 후에, 제 3 유전체 캡핑층(236)에서 인장 스트레스를 제어 또는 생성하기 위하여, 바람직하게 제 1 및 제 2 유전체 캡핑층의 플라즈마 처리 동안에 사용된 동일한 파라미터와 종들을 사용하여 플라즈마 처리가 진행된다. 예를 들어, 플라즈마 처리는 반응성 증으로써 암모니아 및 질소의 혼합물 또는 선택적으로 수소를 포함할 수 있다. 제 1 및 제 2 유전체 캡핑층의 경우에서와 같이, 이들 증착 및 플라즈마 처리 공정은 제자리에서 수행되는 것이 바람직하다.

유전체 캡핑층의 연속적인 증착 및 플라즈마 처리의 목적은 내부 인장 스트레스를 갖는 인장 유전체 캡핑층(200)을 얻기 위해서이다. 내부적으로 인장 스트레스된 유전체 캡핑층(200)은 이것과 접촉하는 전도성 상호접속 물질(101)의 표면에 압축성 스트레스를 작용한다. 결과적으로, 전도성 상호접속 물질(101), 예를 들면, 구리는 상기 설명된 문제가 될 수 있는 이것과 접촉하는 금속 피쳐(features) 상에 인장 스트레스를 덜 작용시키는 경향이 있다.

사용된 유전체 캡핑층의 수와 이들의 제작과 관련된 다른 파라미터는 주된 중요성을 갖지 않는다. 오히려, 유전체 캡핑층의 내부 인장 스트레스의 크기 및 안정성이 보다 더 중요하다. 따라서, 유전체 캡핑 물질의 단일층이 요구된 크기와 특성의 요구된 내부 인장 스트레스를 갖도록 증착되는 경우, 단일 유전체 캡핑층은 충분하다. 선택적으로 세개 이상의 이런 유전체 캡핑층이 이들 특성을 얻기 위해 요구되어 진다면, 세개 이상의 유전체 캡핑층이 상기 설명된 방법에 따라서 증착되고 플라즈마 처리될 필요가 있다. 도 5(a) 및 도 5(b)에서 설명된 바람직한 구현예에서, 인장층(200)은 세번 연속적으로 증착되고 플라즈마 처리가 수행된 층으로 구성된다.

cessing of the second dielectric capping layer (226). The third dielectric capping layer (236) is formed with the thickness less than about 50 Å like the first dielectric capping layer (215) and the second dielectric capping layer (226). The combination of the arbitrary a dielectric material in which the third dielectric capping layer (236) can maintain the stress or the dielectric materials is include might like first and second dielectric capping layers (215, 226). Preferably, the obligatorily the third dielectric capping layer (236) consists of the combination of the materials selected in the form of at least one a dielectric materials or the silicon dioxide, and the silicon nitride and SiC_xN_yH_z from the group consisting of silicon, carbon, and the compound of hydrogen and nitrogen.

Preferably, the obligatorily the third dielectric capping layer (236) consists of the same dielectric material as first and second dielectric capping layer. In the third dielectric capping layer (236) after the exposed top surface (240) silver deposition, of the plasma processing, performed in first and second dielectric capping layer the third dielectric capping layer (236), in order that the tensile stress is controlled or it produces preferably the plasma processing is progressed for the plasma processing of first and second dielectric capping layer using the parameter and the used same kinds. For example, the plasma processing comprises ammonia with the reactive species and the mixture of the nitrogen, selectively, hydrogen. In case of first and second dielectric capping layer, it is the be desirable that these deposition and plasma treatment processes are together performed in the proper place.

The extension dielectric capping layer (200) in which the object of the deposition and the successive plasma processing of the dielectric capping layer have the inside tensile stress is to be obtained. Internally, the dielectric capping layer (200) stressed with extension acts the compressive stress on the surface of the conductivity interconnect material (101) contacting this. Consequently, the tensile stress tends to be less operated on the metal feature (features) contacting this in which it can become the problem that the conductivity interconnect material (101), for example, the copper is above-mentioned.

It does not have the significance in which the dissimilar parameter associated with the number of used dielectric capping layers and their manufacture are principal. Rather, much more, the size of the inside tensile stress of the dielectric capping layer and stability are important. Therefore, the size and the case, and the single genetic entity capping layer of being deposited in order to have the required inside tensile stress of property are sufficient the monolayer of the dielectric capping material is required. Selectively, if it is required so that such dielectric capping layer more than the force obtain these properties it need to be deposited according to the method in which the dielectric capping layer described in the above is three times above-mentioned and it be plasma processed. In the implementation doing with desirable explained in Figure 5(a) and Figure 5(b), it consists of the layer in which the tensile layer (200) is deposited to the consecutively and the plasma processing is

도 6을 참조하여 통상적인 리소그래피 및 식각 공정에 의해 ILD(102) 표면에 인장 캡핑층(200)의 일부가 제거되는 것을 보여준다. 상기 리소그래피 공정은 포토레지스트를 적용하는 단계, 포토레지스트를 요구된 패턴으로 방사 노출시키는 단계 및 노출된 레지스트를 통상적인 레지스트 현상제로 현상시키는 단계를 포함한다. 상기 식각 단계는 건조 식각 공정, 습식 화학 식각 공정 또는 이들의 조합을 포함할 수 있다. #34#건조 식각 #34#의 용어는 본 명세서에서 반응성 이온 식각, 이온 빔 식각, 플라즈마 식각 또는 레이저 제거(laser ablation)와 같은 식각 기술을 나타낸다.

도 7을 참조하여, 통상적인 공정에 의한 단일 압축성 유전체층(416)의 증착을 보여준다. 블랭킷(blanket) 증착은 인장 유전체 캡핑층(200) 및 ILD(102)의 재-노출된 상부 표면(105) 위에 압축성 유전체층(416)을 증착한다.

도 8을 참조하여, CMP 후의 구조를 설명한다. 인장층(200) 상에 증착된 압축성 층 물질의 제거는 전도성 상호접속 물질(101) 상에만 형성된 다중 증착 인장 캡핑층(200)을 초래한다. 단일 증착 압축성 유전체층(416)은 ILD(102) 표면에만 형성된다. 바람직한 본 구현예에서, 다중 증착 인장 캡핑층(200)은 세번의 연속적으로 증착 및 처리된 층으로 구성된다.

도 9를 참조하여, 본 발명의 다른 구현예를 설명한다. 상기 설명된 바와 같이, 전도성 상호접속 물질(101)은 인터 레벨 유전체(ILD) 물질(102)로 형성된다. 전도성 상호접속 물질(101)과 ILD(102) 사이에 또한 확산 장벽 물질(103)이 있을 것이다. 증착된 단일 압축성 유전체층(416)이 있다.

도 10을 참조하여, 통상적인 리소그래피 및 식각 공정에 의한 전도성 상호접속 물질(101) 표면 상에 단일 압축성 유전체층(416)의 일부의 제거를 설명한다.

도 11을 참조하여, 인장 유전체 캡핑층(200)의 증착을 설명한다. 블랭킷 증착은 압축성 유전체층(416) 및 전도성 상호접속 물질(101) 위에 인장 유전체 층(200)을 증착할 것이다. 바람직한 본 구현예에서, 인장층(200)은 종래 구현예에서 설명되고 및 도 4와 5에서 설명된 바와 같이 다중의 연속적으로 증착되고 플라즈마 처리가 수반된 층으로 구성된다.

도 12를 참조하여, CMP 후의 구조를 설명한다. 압축성 층(416) 상에 증착된 인장층 물질의 제거는 전도성 상호접속 물질(101) 상에만 형성된 다중 증착 인장 캡핑층(200)을 초래한다. 단일 증착 압축성 유전체층(416)은 ILD(102) 표면에만 형

performed.

Referring to Figure 6, it shows that lithography and the etching process of being normal get rid of the part of the extension capping layer (200) in the ILD (102) surface. The lithographic process comprises the step of developing with the normal resist developer the step of applying the photoresist, and the step of exposing the photoresist radiation to the required pattern and the exposed resist. The equation angular step may include the dry etching process, and the wet chemical etch process or their combination. In the term of the "dry etching" is this specification, the reactive ion etching, the ion beam etch, and the etching such as the plasma etching process and laser ablation are shown.

Referring to Figure 7, the deposition of the single compressibility dielectric layer (416) by the process of being normal is shown. The blanket deposition deposits the compressibility dielectric layer (416) on the top surface (105) exposed with material - of the ILD (102) and extension dielectric capping layer (200).

Referring to Figure 8, the structure after CMP is illustrated. The one of the compressibility layer material deposited on the tensile layer (200) causes the formed multiple deposition extension capping layer (200) on the conductivity interconnect material (101). The single deposition compressibility dielectric layer (416) is formed in the ILD (102) surface. In this implementation doing with desirable, the multiple deposition extension capping layer (200) consists of the layer which the consecutively is processed with the deposition of the Severn.

The dissimilar implementation of the invention is illustrated with reference to fig. 9. As shown in it is above-mentioned the conductivity interconnect material (101) is formed with the interlevel dielectric (ILD) material (102). It will have moreover, under barrier metal (103) between the conductivity interconnect material (101) and ILD (102). It has the deposited single compressibility dielectric layer (416).

Referring to Figure 10, the partial the one of the single compressibility dielectric layer (416) is illustrated on the conductivity interconnect material (101) surface by the normal lithography and etching process.

Referring to Figure 11, the deposition of the extension dielectric capping layer (200) is illustrated. The blanket deposition will deposit the extension dielectric layer (200) on the compressibility dielectric layer (416) and conductivity interconnect material (101). It is deposited to the consecutively of multiple and it as described in detail in the drawing 4 and 5 the tensile layer (200) is explained in this implementation done with desirable in the conventional embodiment example consists of the layer in which the plasma processing is accompanied.

The structure after CMP is illustrated with reference to fig. 12. The one of the tensile layer material deposited on the compressibility layer (416) causes the formed multiple deposition extension capping layer (200) on the

성된다.

conductivity interconnect material (101). The single deposition compressibility dielectric layer (416) is formed in the ILD (102) surface.

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Electronic Acknowledgement Receipt	
EFS ID:	31200619
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	31817
Filer:	Michael A. Bernadicou/Sheri Villarreal
Filer Authorized By:	Michael A. Bernadicou
Attorney Docket Number:	P38794USDC 111548-227293
Receipt Date:	12-DEC-2017
Filing Date:	03-APR-2017
Time Stamp:	14:32:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P38794USDC_IDS_12_12_17.pdf	494677	yes	2
			f9068d77a9cf36a0f364ef41ef765208477ed18f		

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Form (SB08)		2	2	
Warnings:					
Information:					
2	Foreign Reference	CN1420560A_w_Abstract.pdf	10891807	no	89
			89266f1a5be265735ca892f12daa60340223dd94		
Warnings:					
Information:					
3	Foreign Reference	CN101490825A_w_abstract.pdf	1882845	no	15
			247d1b2863823c2637dba40655dae99c58368504		
Warnings:					
Information:					
4	Foreign Reference	KR1020090085066_w_English_translation.pdf	8694606	no	14
			6b200986cf239b8e54b3efabacbc0259232328c7		
Warnings:					
Information:					
5	Non Patent Literature	P38794CN_OA4_09_12_17.pdf	2480652	no	7
			958459a44388886e379da9c0672f7db758d5831		
Warnings:					
Information:					
6	Non Patent Literature	P38794CND_OA1_08_12_17.pdf	5171091	no	10
			42b5bc718da6f51668ec5c087983cf1d3c58e819		
Warnings:					
Information:					
7	Non Patent Literature	P38794KR-D2_FOA_07_18_17.pdf	193270	no	5
			dc9ec0b1e876de7e0ae56f714c6f921d8ace7a49		
Warnings:					

Information:	
Total Files Size (in bytes):	29808948
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application No. 15/477,506

Filing Date April 3, 2017

First Inventor Boyan Boyanov, et al.

Art Unit 2898

Examiner FORTICH, RODOLFO D

Attorney Docket No. P38794USDC 111548-227293

DUTY OF DISCLOSURE STATEMENT

In accordance with the duty of disclosure, enclosed is a copy of an Information Disclosure Statement (IDS) Citation Form PTO/SB/08 or PTO-1449, together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). This IDS and IDS Citation Form are being submitted before the mailing of the first Office Action on the merits. It is respectfully requested that the cited references be considered and that the enclosed copy of PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

The submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made in the subject application and is not to be construed as an admission that the information cited in this statement is material to patentability.

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

OR

☒ None

☐ The IDS Filing Fee in the amount of \$180.00 as set forth in 37 CFR 1.17(p) has been submitted herewith.

☒ It is requested that any requisite fees be debited from Deposit Account 50-0393.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of signature.

Signature /Michael A. Bernadicou/

Date (MM-DD-YYYY) 12-12-2017

Name/Print Michael A. Bernadicou

Registration Number 35,934

I hereby certify that this correspondence is being submitted electronically via EFS Web on the date shown below.

Sheri Villarreal /Sheri Villarreal/

Date 12-12-17

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to be (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 5450, Alexandria, VA 22315-5450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/477,506	04/03/2017	Boyan Boyanov	42P38794DC

CONFIRMATION NO. 2892

PUBLICATION NOTICE

31817

SCHWABE, WILLIAMSON & WYATT, P.C.

c/o CPA GLOBAL

900 2nd Avenue South, Suite 600

MINNEAPOLIS, MN 55402



OC00000092912555

Title:METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

Publication No.US-2017-0207120-A1

Publication Date:07/20/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/477,506	04/03/2017	Boyan Boyanov	42P38794DC

45209
BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

CONFIRMATION NO. 2892
POWER OF ATTORNEY NOTICE



Date Mailed: 07/17/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/12/2017.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/mabebe/



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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/477,506	04/03/2017	Boyan Boyanov	42P38794DC

CONFIRMATION NO. 2892

POA ACCEPTANCE LETTER

31817
SCHWABE, WILLIAMSON & WYATT, P.C.
c/o CPA GLOBAL
900 2nd Avenue South, Suite 600
MINNEAPOLIS, MN 55402



Date Mailed: 07/17/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/12/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/mabebe/

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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:



Practitioners associated with the Customer Number:

31817

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:



The address associated with Customer Number:

31817

OR



Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

Assignee Name and Address:

Intel Corporation
2200 Mission College Boulevard
Santa Clara, California 95054**A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.****SIGNATURE of Assignee of Record**

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	24 June 2016
Name	Lisa Hopkinson	Telephone	480.715.9827
Title	Administrator of Patents		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Intel Corporation
Application No./Patent No.: 15/477,506 Filed/Issue Date: 04/03/2017
Titled: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
Intel Corporation, a corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: BOYAN BOYANOV ET AL. To: INTEL CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 027334, Frame 0408, or for which a copy thereof is attached.

2. From: BOYAN BOYANOV ET AL. To: INTEL CORPORATION

The document was recorded in the United States Patent and Trademark Office at
Reel 031022, Frame 0160, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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 Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Nathan R. Maki/

07/12/2017

Signature

Date

Nathan R. Maki

Reg. No. 51,110

Printed or Typed Name

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	29767628
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	45209
Filer:	Nathan Robert Maki/Aileen Lee
Filer Authorized By:	Nathan Robert Maki
Attorney Docket Number:	42P38794DC
Receipt Date:	12-JUL-2017
Filing Date:	03-APR-2017
Time Stamp:	20:57:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	P38794USDC_POA.pdf	291283	no	1
			b44d4b465c228ecc8c76323aa21b1be9bff2a89c		
Warnings:					

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	P38794USDC_373c.pdf	120399	no	3
			58f3f61da771970ab212e82ed77027b1db7afcd1		
Warnings:					
Information:					
Total Files Size (in bytes):				411682	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov
	Group Art Unit	2898
	Examiner Name	Not yet assigned
Sheet 1 of 1		Attorney Docket No: 42P38794DC

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		CN 1575508A	02-02-2005	Christopher Thomas et al.		*

*= Machine Translation in English

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

EXAMINER

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Copper alloy interconnections for integrated circuits and methods of making same

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ABSTRACT translated from Chinese

Preparation of copper alloy interconnects on integrated circuits, including copper plated onto the seed layer, the copper, the concentration of doping element can be controlled, so that the core part of the copper interconnect lines in low concentration doping element and a higher concentration of doping element surface of the copper interconnects in. Copper alloy at different current densities are plated to provide rich interface elements doped. Thus, the surface portion of the interconnect element has a higher doping concentration, which can improve electromigration resistance, and at the same time, maintaining the internal interconnect a much lower concentration of doping elements, which will interconnect the ideal Low resistance remained.

DESCRIPTION translated from Chinese

Copper alloy interconnects for integrated circuits and manufacturing method thereof

Technical Field

The present invention relates generally to the field of integrated circuit fabrication, and more particularly relates to a copper alloy and its preparing interconnects (interconnection).

Background

Advances in semiconductor manufacturing technology have led to the development of multi-layer interconnection lines of integrated circuits. In such an integrated circuit, the conductive material between the patterned and patterned interconnect layer of conductive material on the other one interconnect layer, such as silica or the like by a thin film of electrically insulating material is maintained. Such conductive materials are typically metal or metal alloy. The interconnection between the different conductive material layer, and to provide an opening through the conductive structure is formed in the insulating layer and to be connected so that the conductive material is located between different patterned interconnect layer on the electrical connection can be maintained. Such conductive structure generally refers to contacts or micro-channel (via).

Other developments in semiconductor manufacturing technology, resulting in the integration of millions of transistors, each of which is capable of high-speed switching transistor. The so many fast switching transistors can be integrated into an integrated circuit consequence is that the increase in energy consumption during operation. One capable of reducing power consumption while increasing the speed of the technique is that the traditional aluminum and aluminum alloys for an integrated circuit interconnects, replaced with smaller resistance metal, such as copper. Electrical skilled in the art that, by reducing the

resistance, the electrical signal path through the interconnect on an integrated circuit spread faster. Further, since the resistance of copper is much smaller than the resistance of aluminum, and therefore, as compared with the aluminum interconnection line, the cross sectional area of the copper interconnects can be smaller, without causing resistance based interconnects generated increased signal propagation delay. Further, since the electrical capacitance between the two nodes is a direct function of the area between the nodes, and therefore, the use of smaller copper interconnects would reduce parasitic capacitance. Thus, the aluminum-based interconnects replace the copper-based interconnects, depending on the choice of the size, provide less resistance, smaller capacitor or both.

As mentioned earlier, copper has some advantages on electricity, such as lower unit cross-sectional area of resistance, the ability to provide a smaller parasitic capacitance, and greater resistance to electromigration. For all these reasons, IC manufacturers have found that the copper included in their products is ideal.

When used in integrated circuit interconnects, although copper and aluminum have an advantage compared to some of the electricity, but copper interconnects may still produce some of the defects and electromigration.

Therefore, a need to provide a stronger resistance to electromigration of the copper-based integrated circuit interconnects.

Brief Description

Figure 1 is a plating embedded structure (damascene structure) is a cross-sectional schematic view, according to one interpretation of indirect parcel of the present invention (encapsulaton) scheme in which the dopant concentrated on the surface of the metal film.

Figure 2 is a cross-sectional schematic view plated embedded structure, according to one interpretation of indirect parcel of the present invention, which has been fully dopant diffusion, so that it remains on the surface of the metal film.

Figure 3 is a cross-sectional schematic view plated embedded structure, according to one interpretation of indirect parcel of the present invention, showing the aggregation of dopants in the Cu interface.

Figure 4 is a cross-sectional schematic view of the structure of the plating embedded explained according to an aspect of the present invention is directly wrapped, wherein the dopant metal film is focused on the bottom surface, side surfaces and an upper surface.

Figure 5 is a cross-sectional structure of a plating embedded diagram explains the parcel in accordance with a direct aspect of the present invention, which has been fully dopant diffusion, so that it remains on the surface of the metal film.

Figure 6 is a cross-sectional structure of a plating embedded diagram explains the parcel in accordance with a direct aspect of the present invention, showing the enrichment of the dopant in the Cu interface.

Figure 7 is a cross-sectional schematic view of an interconnect structure, elemental copper alloy is preferably formed at the interface portion of the interconnect structure.

Figure 8 is a cross-sectional schematic view of an interconnect structure, alloying elements Cu is preferably formed on the upper surface of the interconnect structure.

Figure 9 is a flow chart showing a process according to the invention in operation.

FIG. 10 is a flowchart showing a process according to the invention in operation.

DETAILED DESCRIPTION

We have demonstrated that by adding a small amount of copper to second metal interconnect lines can be greatly improved electromigration lifetime copper interconnects. However, after the introduction of such a second metal, a common consequence is that compared to copper, conductivity decreases.

In one embodiment of the present invention, a Cu-Sn-based sulfonic acid plating bath, such that in the electrodeposition process control in real time the percentage of Cu in Sn becomes possible. In this manner, a second metal, e.g., Sn, may be placed in those areas (e.g., the surface of copper interconnect lines) are more likely to occur is known electromigration, while only a few are placed interconnecting lines Sn those who do not wish to decrease the area of its conductive (e.g., metal trench (trench) inside). Such electroplating process according to the present invention, enabling the deposited copper body (bulk) in precise, very small amount (e.g., horizontal ppm) of Sn (or other doping element). At room temperature after annealing or after grain growth, Sn primarily accumulated in the grain boundaries. Sn in the copper grain boundaries suppresses grain boundary diffusion of Cu and electromigration activation energy is increased to about 1.3ev. In addition to Sn, the doping elements other available include, but are not limited to, In, Cd, Zn, Bi, Sb, Mn, Mg, Co, Cr, Ni, Pb, Re, Ru, Rh, Pd, Pt, Os, W, S, C.

According to the present invention, a schematic of the plating bath, comprising a low concentration of sulfuric acid and sulfonic acids, the doping element to the copper ion-containing doping elements plating solution "super fill (superfill)" and deposited. Sulfonic acid aids in adding carbon to the coating. Since the solubility of carbon in copper is low, followed by annealing operation can be driven to the interface area. Moreover, according to the present invention, the plating process by real-time changes in current density, while the alloy doping element concentration to be regulated. That is to say, can be made of copper interconnects, the inner body doping concentration of <0.5%, while the doping concentration in the interface or the surface portion of the interconnect line may be > 0.5%. The current density can be varied by varying the applied voltage. For example, if the substrate is made of negatively charged more, then it will be more strongly attracted to the positively charged ions to the substrate.

Terms Term chips, integrated circuits, monolithic devices, semiconductor devices or components, microelectronic devices or components and similar terms and expressions, in the art are often used interchangeably. All terms described above may be applied to the present invention, because in this field, they are generally able to be understood.

The term metal wire, trace (trace), wires (wire), wire, signaling and signal media are all related. The above terminology generally interchangeable, in accordance with the specific to the general order of appearance. In this area, the wire is sometimes called traces, wires, lines, interconnect, or simply referred to as metal.

The term "contact" and "micro-channel" refers to electrical connection between the conductor of the different interconnection layers. In the art, these terms are sometimes used to describe the insulator can be formed in the above-described structure in which an opening can also be used to describe the structure itself is formed. For the present invention disclosure, contacts and micro-channel refers to the structure formed.

NHE refers to the standard hydrogen electrode.

The acronym refers to the millionth ppm.

Substrate, the wafer may also be referred to as (wafer). The wafer may be a semiconductor material, a non-semiconductor material, or a semiconductor material and the non-binding made of semiconductor material. It may have a multi-layer film formed of different materials on a silicon wafer. Other materials may be a wafer, e.g., GaAs, silicon (silicon-on-sapphire) sapphire, or a silicon on insulator (silicon-on-insulator, SOI).

As used herein, the terms vertical, refers to the surface of the substrate substantially at right angles.

Embodiments of the present invention there is provided a plating bath, Cu alloy may be deposited onto the Cu or Cu alloy seed layer (seed layer) on. Cu alloy plating include, but are not limited to, CuSn, CuC, CuS, CuIn, CuCd, CuCr, CuZn, CuBi, CuSb, CuPb, CuMn, CuMg, CuCo, CuNi, CuRe, CuRu, CuW, CuPt, CuPd, CuRh, CuOs . Cu alloy seed layer include, but are not limited to, CuSn, CuMg, CuAl, CuTi, CuTa, CuW, CuIn, CuSb, CuZn, CuPd, CuMn, CuCr, CuNi, CuRu, CuRh, CuAu, CuBi, CuCd, CuPt, CuIr , CuOs, CuRe, CuMo, CuZr, CuW.

For purposes of the present invention is considered, the seed layer, either Cu or Cu alloy, can be by physical vapor deposition (PVD), chemical vapor deposition (CVD), atomic layer deposition (ALD), or any other suitable for forming seed crystals It is deposited in layers. Cu alloy seed layer with or without the case blocking layer may be used. Copper diffusion blocking layer includes, but not limited to, Ta, TaN, TaSiN, W, WN, WSiN, Ti, TiN, TiSiN, Co. Blocking layer may be deposited by PVD, CVD or ALD.

Embodiments of the present invention comprises a plating deposition process. The plating bath according to the present invention, an exemplary embodiment can be combined together to form the following materials: a concentration in the range of 5-100g / l of Cu ions; concentration in the range of 1-50g / l (in the plating bath, by weight meter less than 10% sulfuric acid); the concentration range of 10-100mg / l of Cl ion; one or more acid; and Sn (II) ions. One or more elements may be co-doped with copper deposition, including Sn, In, Cd, Cr, Zn, Bi, Sb, Pb, Mn, Mg, Co, Ni, Re, W, Ru, Pt, Rh, Pd, C, S, Os. Selected doping element is included in the plating bath. In addition, organic additives include, but are not limited to, an anti-inhibitors, e.g., an alkyl sulfonic acid thiol esters; one inhibitor, such as polyether (e.g., polyethylene glycol (PEG), polypropylene glycol (PPG)); and a levelers, such as polyimide or polyamide, can also be used in the plating bath. Complexing agents, such as but not limited to, citric acid (ester), tartaric acid (ester), ethylenediaminetetraacetic acid (EDTA) and acetates, may also be included in the plating bath, the copper that is deposited to provide a more negative potential, which will help those co-deposited with the electrode potential of Cu (NHE + 0.34V) large difference in the occurrence of elements Cu, such elements as Cr, Mg, Mn (NHE-1.18V), Co (NHE- 0.8V), Zn (NHE-0.76V), In (NHE- 0.35V), Ni (NHE-0.25V). Complexing agents can also be used to provide a more negative electrode potential of a noble metal, such as Pd (NHE + 0.99V), Rh (NHE + 0.8V) and Pt (NHE + 0.73V).

In the above-described exemplary plating bath, Cu ions can be provided starting materials include, but are not limited to, copper sulfate, copper nitrate, copper chloride, copper methanesulfonate, copper ethanesulfonate, copper propanesulfonic acid, benzene acid copper and copper triflate. Cl ions can provide a starting material including, but not limited to, HCl. Sulfonic acids including, but not limited to, methanesulfonic acid (MSA), ethanesulfonic acid (ESA), propionic acid (PSA), benzenesulfonic acid (BSA) and trifluoromethanesulfonic acid (triflic acid-TFA), available concentration range of 0.005mol / l- 2.5mol / l. May be provided Sn (II) ions starting materials include, but are not limited to, tin sulfate (II), tin acetate (II), tin bromide (II), tin chloride (II), tin fluoride (II), iodide, tin (II) oxide and tin (II), the concentration range of 0.1-200g / l.

Producing an alloy structure in the illustrative embodiment of the present invention, the plating current density is in the process of change, because change in accordance with the present invention, the current density in the plating bath, can control the concentration of copper deposition occurred doping elements. Thus, it can be on a specific area interconnect structure to form enriched in one or more doping elements Cu alloys. Specifically, to create a kind of copper-based interconnects, and an alloy in the outer region of the interconnect or interface.

In the initial stage and the end of the deposition stage, said current density may be greater (e.g. 30-100mA / cm² within the range), so that Cu can be doped with a higher concentration of elements (e.g., by weight, > 0.5%) occurred deposition. Conversely, the smaller the deposition current density (e.g. 0.5-30mA / cm²) enables Cu doped with a low concentration of elements (e.g., by weight <0.5%) deposition occurred. In the same plating tool, it can quickly annealing operation or immediately after the deposition, to form and fixed Cu alloy microstructures. The annealing operation may be driven to the doping element

interface and grain boundaries. Annealing temperatures can be varied within a certain range: when the first operation, the annealing temperature is low, below 250 °C, to increase the grain size of the copper and impurities driven to the interface; while in the second operation, higher annealing temperatures (> 250 °C), so that the interface is preferably Cu alloy.

In another embodiment of the present invention, the chemical mechanical polishing (CMP) after annealing is performed so that the doping element can diffuse to the interface and form a wrap-around structure. In this annealing operation after CMP can at (low and high) of different temperature for annealing chamber plating tool in the comprehensive, independent furnace or rapid thermal processing (RTP) equipment. Annealing operation carried out at the CMP after to be in the etching stop / ILD deposition during or before.

On its surface with Cu interconnects Cu alloy was prepared according to the following embodiments of the interconnect structure in accordance with one embodiment of the present invention: the use of high current density at the end stage of the deposition operation, such that one or more Species doping element preferably co-deposited with Cu; and deposited mostly in the relatively smaller current density in order to make Cu can be deposited with a lower concentration of one or more doping element (<0.5%) occurred . After completion of the plating deposition annealing operation, so that one or more doping elements Cu can diffuse to the top of the filled trench, while the low concentration of Sn (i.e., <100ppm) remains in the body of the crystal grains of copper on the border.

Figure 1-3 A more detailed explanation of the structure and processes. Figure 1 shows a partially cross-sectional view of the wafer processing to a part. More specifically, FIG. 1 shows an interlayer dielectric (ILD) 102, which has ILD102 patterned to form trenches 101 in which the passage 103 and micro. Partially processed wafer is placed in a plating bath containing Cu ions and one or more elements doped ions. Then, on the ILD 102 copper plating layer 104, so that the grooves 101 and 103 are filled with micro-channel, and the upper surface ILD102 also covered with a layer of copper 104. When copper is also used in the plating bath 104, the current density is increased, so that the plating bath is present in one or more elements doped with copper ions codeposition occurs, the copper alloy layer 106 is formed. Current density is the result of choice, so that the amount of the copper layer 104 doping atoms in less than 0.5% by weight, and the copper alloy layer 106 doping atoms in an amount greater than 0.5% by weight.

Referring to Figure 2, the operation is completed after annealing, FIG. 1 shows the structure of it. In this embodiment, an annealing operation at a temperature below 450 °C in the 0.5 to 180 minutes of time, N₂, Ar, or N₂ + H₂ (i.e. forming gas) environment completed. Embodiment, the annealing operation carried out in two steps in another embodiment: First, at a temperature of 100 °C to 250 °C in the 0.5 to 180 minutes of time, N₂, Ar, or N₂ + H₂ (i.e. forming gas) environment first annealing is performed once; and then, at a temperature of 250 °C to 450 °C in the 0.5 to 180 minutes of time, N₂, Ar, or N₂ + H₂ (i.e. forming gas) a second annealing environment. This annealing operation adulterated element 104 through the top of the copper layer driven out from the copper alloy layer 106. Some dopant atoms have been

driven to move the interface to the copper layer 104, the copper alloy layer 108 is formed, as shown in Fig.

Figure 3 shows a block diagram of complete chemical mechanical polishing (CMP) after 2. The CMP operation removes ILD102 covered on the metal surface, resulting in a single interconnect, which interconnects portions 104 having a copper and copper alloy portion 108 as shown in FIG. Shaped copper alloy part is located on the surface of the interconnection structure is close to the vertical sides of the trench areas is generally thin, but closer to the middle of the thicker interconnect structure.

Cu interconnect structure consists of Cu alloys wrapped in one embodiment of the present invention, as described below was prepared based on copper interconnect structures: Let copper and one or more doping elements there were deposited, and then plating Copper - situ annealing dopant material, one or more low solubility doping element driven to interface portion interconnect structures. Such an interconnect structure may also be prepared by the following method: using a larger current density in the initial stage of deposition ($> 30\text{mA} / \text{cm}^2$), with the higher concentrations of copper doping element happened plating (co-plating); Then the current density is small ($< 30\text{mA} / \text{cm}^2$) under copper, such that the interior of the main body portion of the interconnect structure, a relatively low concentration of doping element; and then, at higher current densities ($> 30\text{mA} / \text{cm}^2$) Under copper, so that the top of the interconnect structure (that is, the post-deposition portion) in a relatively high concentration of doping elements.

After the plating operation completed, the annealing operation to doping elements can spread to the top of the copper filled trench.

Figure 4-6 A more detailed explanation of this structure and process. Figure 4 shows a cross-sectional view of a portion of the partially processed wafer. More specifically, Figure 4 shows an interlayer dielectric (ILD) 402, which ILD402 been patterned and formed a trench in which the micro-channel 401 and 403. Partially processed wafer is placed in a plating bath containing Cu ions and one or more elements doped ions. Then, on ILD402 copper alloy plated layer 404, so that the surface grooves 401 and micro channel 403 are covered, and the upper surface ILD402 also covered with a layer of copper alloy 404. In the embodiment illustrated, Sn co-deposited with copper to form a copper alloy 404, the thickness of the deposited layer is about 100 to 500 angstroms. By one or more doping elements and copper deposition from the plating bath CPC prepared copper alloy 404. When still in the used copper alloy plating bath 404, the current density decreases, so that the presence in the plating bath doping elements are not co-deposition of copper occurs to form a copper layer 406. 4, the copper layer 406 filling the portion not occupied and the copper alloy layer 404 of the trench 401 that the micro-passage 403. Current density is the result of choice, making the copper alloy layer 404 doping atoms in an amount greater than 0.5% by weight, and the amount of the copper layer 406 doping atoms of less than 0.5% by weight. After layer 406 is formed, the current density increases, so that one or more doping element atoms from the copper plating bath again CCP deposition, thereby forming a copper alloy layer 408.

Referring to Figure 5, the operation is completed after annealing, FIG. 4 shows the structure of it. In this embodiment, an annealing operation at a temperature below 450 °C in the 0.5 to 180 minutes of time, N₂, Ar, or N₂ + H₂ (i.e. forming gas) environment completed. Embodiment, the annealing operation carried out in two steps in another embodiment: First, at a temperature of 100 °C to 250 °C in the 0.5 to 180 minutes of time, N₂, Ar, or N₂ + H₂ (i.e. forming gas) environment first annealing is performed once; and then, at a temperature of 250 °C to 450 °C in the 0.5 to 180 minutes of time, N₂, Ar, or N₂ + H₂ (i.e. forming gas) a second annealing environment. This annealing operation will be part of the copper layer by doping element 406 driven out from the copper alloy layer 406, as shown in FIG. By driving these doping atoms to the interface surface of the copper layer 406, a self-wrapped copper area is formed. That is, after annealing copper 406 is surrounded by a copper alloy 410.

Figure 6 shows a complete diagram of the chemical mechanical polishing (CMP) after the operation of the structure 5. The CMP operation removes ILD402 covered on the metal surface, resulting in a single interconnect, which interconnects portions 406 having a copper and copper alloys portion 410 as shown in Fig. Shaped copper alloy part is located on the surface of the interconnection structure is close to the vertical sides of the trench areas is generally thin, but closer to the middle of the thicker interconnect structure.

In another embodiment of the present invention, after the excess metal removed by CMP annealed. In this annealing operation after CMP can at (low and high) of different temperature for annealing chamber plating tool in the comprehensive, independent furnace or rapid thermal processing (RTP) equipment. And in accordance with the present invention, this annealing operation can be carried out during the deposition process or the ILD etch stop layer, or before.

Figure 7 shows a cross-sectional portion of the wafer, the wafer having a copper layer surrounded by ILD interconnects and micro-passage. More specifically, copper interconnects and micro passage has since wrapping layer surrounding the core of their region. These self-wrapping layer is composed of a copper alloy. Copper alloy according to the above can only be used to improve the electromigration properties, but also in the copper alloy, it does not require a separate copper diffusion blocking layer is formed, and the copper diffusion blocking layer is present in conventional copper interconnection lines. Figure 8 is similar to FIG. 7, but the present invention is explained an embodiment wherein the copper alloy layer is formed on top of the copper interconnects.

Figure 9 illustrates a method according to the invention. As represented by block 902, at a first current density, the copper plating from the plating bath to the substrate, the plating bath containing sulfuric acid, a sulfonic acid, copper ions, and ion doping. Then, as shown in block 904, the current density is changed to the second value, the copper plating in the plating bath from the same alloy has been previously deposited onto the copper.

10 explains an embodiment of the present invention, which wrapped up the formation of a copper interconnect structure. Parcel mean, the core of the copper interconnect or internal structure is

surrounded by a copper alloy region. The block shown in FIG. 10 1002, at a first current density, copper alloy plating from the plating bath to the substrate, the plating bath containing sulfuric acid, a sulfonic acid, copper ions, and ion doping. The current density is the result of choice, so that there is in the plating bath doping elements can be co-deposited with copper occur. This copper alloy layer is usually formed previously been prepared on a good seed layer. As represented by block 1004, in the second smaller current density, in the same electrolytic copper plating bath from the plating has been previously deposited onto a copper alloy. As shown in block 1006, another from the same copper alloy plating bath is plated onto the copper layer. The copper alloy is deposited at a current density of third down, third current density which is greater than the second current density. The first and the third current density may be equal to, but is not required to be equal. As shown in block 1008, the substrate is annealed so that the copper alloy region doping atoms are driven into the copper layer portion, including the interface portion, thereby forming a self-wrapped around the core area of the copper interconnect structure.

Conclusion embodiment of the present invention provides a composition of copper-based interconnect structure, and methods for their preparation and chemistry. More specifically, by using a plating bath prepared based interconnects embedded copper plating bath which contains a mixture of a low concentration of sulfuric acid (<50g / l) and consisting of a sulfonic acid, can be doped elements "Super fill" and co-plating. The concentration of doping elements can be by varying the current density in the plating process is adjusted, thereby forming a higher doping concentration of the element in the interface region of the interconnect structure, so as to not significantly lower resistivity undoped sacrificial Cu line case, to improve the electromigration resistance. Between the two without any significant delay, the annealing after plating by, for example, in an integrated annealing chamber having a plating tool annealing, doping elements can be diffused to make the interface region, thereby forming an alloy at the interface. Annealing temperature may be low (e.g., <250 °C) to high (> 250 °C) vary so as to preferably form an alloy at the interface. Prepared according to the copper-based interconnect of the present invention can be obtained by doping element alloys wrapped interconnects. Preparation of Cu line is Re, Ru or W wrapped, you can get a built-in blocking layer. In other words, by preparing a Re, Ru or W copper, may be external (i.e., interfacial area) to give doping interconnect element alloy which serve to reduce or prevent copper atoms into the surrounding dielectric layer diffused effect. Cu interconnect structure in accordance with the present invention are prepared to be at the interface or the bottom of the screen contains a copper alloy.

About CuSn electroplating, combination, such as: (a) having a substantially uniform average, in a metal plating film of Sn content is very low, Sn mainly at grain boundaries; bottom (b) and the micro-line passage has a higher CuSn concentration; top (c) online and micro CuSn path has a higher concentration; the top and bottom (d) online and micro CuSn path has a higher concentration. It should also be noted that the annealing may be performed after Cu plating, or copper layer is deposited after the CMP, or after the Cu plating and CMP have been completed.

An advantage of some embodiments of the present invention is that the adsorption of copper interconnect silicon nitride improves.

An advantage of some embodiments of the present invention does not require silicon nitride etch stop layer.

An advantage of some embodiments of the present invention is to improve the wear resistance of copper-based interconnects.

An advantage of some embodiments of the present invention is to hillock formation during annealing operation is reduced.

An advantage of some embodiments of the present invention, relative to pure copper adsorption and blocking layers, the adsorption of copper alloy and blocking layer improved, because the copper alloy in the adulterated ingredient may be blocking layer (e.g., Sn-based copper alloy of Ta blocking layer) is formed an intermetallic compound.

An advantage of some embodiments of the present invention is made of a copper alloy coated copper interconnect provides mechanical support to support copper. When inter-SiO₂-based layer of dielectric material is replaced by a rigid worse and ultra low -k -k dielectric material, which is particularly useful.

For those skilled in the art, in the material after reading this disclosure, other modifications for the apparatus described herein clear, cleaning solutions and processes carried out will be apparent. Thus, as described in the appended claims all such modifications and changes will be considered to fall within the spirit and scope of the present invention.

CLAIMS(22) translated from Chinese

1. An electroplating bath comprising a mixture formed by the following materials: sulfuric acid, sulfonic acid, copper-containing compounds, chlorine-containing compound and at least one doping element.
2. The plating bath according to claim 1, wherein said copper-containing compound selected from the group consisting of the following compounds consisting of: copper sulfate, copper nitrate, copper chloride, copper methanesulfonate, copper ethanesulfonate, propanesulfonic acid copper, and copper triflate benzene copper.
3. The plating bath according to claim 2, further comprising at least one organic additive.
At least one organic additive compound selected from the group consisting of a plating bath according to claim 3, wherein said: alkyl sulfonic acid thiol esters, polyethers, polyimides and polyamides.
5. The electroplating bath of claim 4, further comprising at least one complexing agent.

6. The electroplating bath according to claim 5, wherein said at least one complexing agent selected from the group consisting of the following compounds consisting of: acetate, citrate, tartrate, and EDTA.
7. A plating bath according to claim 2, wherein the acid is selected from the group of compounds consisting of: methanesulfonic acid, ethanesulfonic acid, propanesulfonic acid, benzenesulfonic acid and trifluoromethanesulfonic acid; and the said sulfonic acid in a concentration range of 0.005 mol / l to 2.5 mol / liter between.
8. A plating bath according to claim 1, wherein said at least one doping element selected from the group consisting of the following elements: Sn, In, Cd, Cr, Zn, Bi, Sb, Pb, Mn, Mg, Co, Ni, Re, W, Ru, Pt, Rh, Pd, C, S, Os.
9. The range of concentration of the plating bath of claim 8, wherein the sulfuric acid is between 1-50g / l; and, wherein the concentration of said chlorine-containing compound from the Cl ions in the 10-100mg / l of Room.
10. A plating bath according to claim 3, wherein the sulfuric acid in the plating bath less than 10% by weight.
11. A plating bath according to claim 6, wherein said at least one doping element is Sn; Sn plating baths as a source of material selected from the group consisting of the following materials consisting of: tin sulfate (II), acetate, tin (II) bromide, tin (II), tin chloride (II), tin fluoride (II), iodide, tin (II) oxide and tin (II).
12. A plating bath according to claim 6, wherein said chlorine-containing compound is HCl.
- 13. A method of preparing an integrated circuit on a copper-based interconnect, comprising: a substrate preparation having a dielectric layer thereon, said dielectric layer having a trench into the trench in the dielectric layer and above the groove having a seed layer; the substrate in the plating bath mixture formed by the following materials: sulfuric acid, a sulfonic acid, copper-containing compounds, chlorine-containing compound and at least one doping element; the seed layer a copper layer is formed, said doping element in uneven distribution among a copper layer; annealing of the substrate; and by chemical mechanical polishing, the top of the copper layer is removed.**
14. A method according to claim 13, wherein, wherein said copper layer is formed comprising: applying a first voltage to the wafer to facilitate a first current density; and the second voltage is applied to the wafer to facilitate a second current density.
15. A method according to claim according to claim 14, wherein said first current density is less than 30mA / cm².
16. A method according to claim according to claim 14, wherein said second current density is greater than 30mA / cm².
17. A method according to claim 14, wherein wherein said doping element selected from the group consisting of the following elements: Sn, In, Cd, Cr, Zn, Bi, Sb, Pb, Mn, Mg, Co, Ni, Re, W, Ru, Pt, Rh, Pd, C, S, Os.
18. A method according to claim 14 or claim, wherein said doping element is Sn, the first current density is less than 30mA / cm², and a second current density is greater than 30mA / cm².
19. A method according to claim 13, wherein, wherein said copper layer is formed comprising: applying a first voltage to the wafer to facilitate a first current density; a second voltage is applied to the wafer to

facilitate a second current density; and is applied to the wafer The third voltage to facilitate third current density.

20. A method according to claim according to claim 19, wherein said second current density is less than the first current density, the current density is less than the third and the second current density.

21. An integrated circuit interconnect structure, comprising: a groove having at least one inter-layer dielectric layer, said trenches having vertical sidewalls spaced apart; disposed in said at least one groove metal conductors therein; wherein said internal metal conductor comprises copper, the copper contains less than 0.5% by weight of the doping element, the top metal conductor, comprising an upper surface, comprising copper, said Copper doping element contains more than 0.5% by weight, and the thickness of the top according to the distance between the vertical side walls of the trench varies.

22. The interconnect structure of claim 21, wherein said top is a CuSn alloy, and the thickness of the intermediate position in the top of said vertical sidewall of said at least one groove between the maximum.

REFERENCED BY

Citing Patent	Filing date	Publication date	Applicant	Title
CN100431106C	Sep 26, 2005	Nov 5, 2008	财团法人工业技术研究院	Method for forming interconnected electroplating lead wire of nano-carbon tube and metal composite material
CN100517684C	Feb 14, 2007	Jul 22, 2009	恩益禧电子股份有限公司	Semiconductor device and method for manufacturing same
CN102683270A *	Mar 15, 2012	Sep 19, 2012	瑞萨电子株式会社	Semiconductor device manufacturing method and semiconductor device
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Citing Patent	Filing date	Publication date	Applicant	Title
CN102956541B *	Aug 19, 2011	Nov 25, 2015	中芯国际集成电路制造(上海)有限公司	一种形成铜互连的方法
CN103839920A *	Oct 9, 2013	Jun 4, 2014	意法半导体公司	Copper seed layer for an interconnect structure having a doping concentration level gradient
US9640434	Aug 25, 2014	May 2, 2017	Shanghai Ic R&D Center Co., Ltd	Method for processing an electroplated copper film in copper interconnect process
WO2015165179A1 *	Aug 25, 2014	Nov 5, 2015	上海集成电路研发中心有限公司	Electroplated copper film treatment method for use in semiconductor-copper interconnect process

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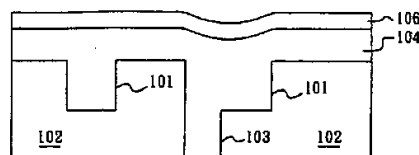
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权利要求书 3 页 说明书 11 页 附图 5 页

[54] 发明名称 用于集成电路的铜合金互连线及其制造方法

[57] 摘要

集成电路上的铜合金互连线的制备,包括将铜镀到种层上,所述的铜中,掺杂元素的浓度可以控制,从而使得铜互连线的核心部分中掺杂元素的浓度较低,而铜互连线的表面部分中掺杂元素的浓度更高。铜合金在不同的电流密度下被镀上,以提供富含掺杂元素的界面。这样,在互连线的表面部分具有较高的掺杂元素浓度,从而可以改善电迁移抗性,而同时,互连线的内部保持低得多的掺杂元素浓度,从而将互连线的理想的低电阻保留了下来。



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1. 一种电镀浴，包含由下列物质形成的混合物：
硫酸、磺酸、含铜化合物、含氯化合物以及至少一种掺杂元素。
- 5 2. 按照权利要求 1 所述的电镀浴，其中所述的含铜化合物选自由下列化合物构成的组：硫酸铜、硝酸铜、氯化铜、甲磺酸铜、乙磺酸铜、丙磺酸铜、苯磺酸铜以及三氟甲磺酸铜。
3. 按照权利要求 2 所述的电镀浴，还包含至少一种有机添加剂。
4. 按照权利要求 3 所述的电镀浴，其中所述的至少一种有机添加剂选自由下列化合物构成的组：烷基磺酸硫羟基酯、聚醚、聚酰亚胺及聚酰胺。
- 10 5. 按照权利要求 4 所述的电镀浴，还包含至少一种络合剂。
6. 按照权利要求 5 所述的电镀浴，其中所述的至少一种络合剂选自由下列化合物构成的组：乙酸酯、柠檬酸酯、酒石酸酯及 EDTA。
- 15 7. 按照权利要求 2 所述的电镀浴，其中所述的磺酸选自由下列化合物构成的组：甲磺酸、乙磺酸、丙磺酸、苯磺酸及三氟甲磺酸；并且所述磺酸的浓度范围在 0.005 摩尔/升到 2.5 摩尔/升之间。
8. 按照权利要求 1 所述的电镀浴，其中所述的至少一种掺杂元素选自由下列元素构成的组：Sn, In、Cd、Cr、Zn、Bi、Sb、Pb、Mn、Mg、
- 20 Co、Ni、Re、W、Ru、Pt、Rh、Pd、C、S、Os。
9. 按照权利要求 8 所述的电镀浴，其中所述硫酸的浓度范围在 1—50 g/l 之间；并且，其中来自所述含氯化合物的 Cl 离子的浓度范围在 10—100 mg/l 之间。
10. 按照权利要求 3 所述的电镀浴，其中所述的硫酸在电镀浴中按重量
- 25 计少于 10%。
11. 按照权利要求 6 所述的电镀浴，其中所述的至少一种掺杂元素是 Sn；电镀浴中作为 Sn 源的材料选自由下列物质构成的组：硫酸锡(II)、乙酸锡(II)、溴化锡(II)、氯化锡(II)、氟化锡(II)、碘化锡(II)及氧化锡(II)。
12. 按照权利要求 6 所述的电镀浴，其中所述的含氯化合物为 HCl。

13.一种制备集成电路上的基于铜的互连线的方法，包括：

预备一种在其上具有电介质层的基片，所述电介质层之中具有沟槽，
在所述电介质层和沟槽之上具有种层；

将所述基片置于由下列物质形成的电镀浴混合物中：硫酸、一种磺
5 酸、含铜化合物、含氯化合物以及至少一种掺杂元素；

在所述种层上形成一个铜层，在所述的铜层之中掺杂元素的分布不均
一；

对基片进行退火；及

通过化学机械抛光，将铜层的顶部除去。

10 14.按照权利要求 13 所述的方法，其中所述的形成铜层包括：

对晶片施加第一电压以促成第一电流密度；及

对晶片施加第二电压以促成第二电流密度。

15 15.按照权利要求 14 所述的方法，其中所述的第一电流密度小于 30
mA/cm²。

16.按照权利要求 14 所述的方法，其中所述的第二电流密度大于 30
mA/cm²。

17.按照权利要求 14 所述的方法，其中所述的掺杂元素选自由下列元
素构成的组：Sn、In、Cd、Cr、Zn、Bi、Sb、Pb、Mn、Mg、Co、Ni、
Re、W、Ru、Pt、Rh、Pd、C、S、Os。

20 18.按照权利要求 14 所述的方法，其中所述的掺杂元素是 Sn，所述的
第一电流密度小于 30 mA/cm²，并且第二电流密度大于 30 mA/cm²。

19.按照权利要求 13 所述的方法，其中所述的形成铜层包括：

对晶片施加第一电压以促成第一电流密度；

对晶片施加第二电压以促成第二电流密度；及

25 对晶片施加第三电压以促成第三电流密度。

20.按照权利要求 19 所述的方法，其中所述的第二电流密度小于第一
电流密度，并且第二电流密度小于第三电流密度。

21.一种集成电路中的互连结构，包括：

一个其中具有至少一个沟槽的层间电介质层，所述的沟槽具有彼此隔

开的垂直侧壁；

放置在所述的至少一个沟槽内的金属导体；

其中所述金属导体的内部包含铜，所述的铜里含有按重量计少于 0.5 %的掺杂元素，所述金属导体的顶部，包括其上表面，包含铜，所述的铜
5 里含有按重量计大于 0.5%的掺杂元素，并且，所述顶部的厚度按照与沟槽垂直侧壁之间的距离而变化。

22.按照权利要求 21 所述的互连结构，其中所述的顶部是 CuSn 合金，并且，所述的顶部在所述的至少一个沟槽的垂直侧壁之间的中间位置厚度最大。

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用于集成电路的铜合金互连线及其制造方法

5 技术领域

本发明一般地涉及集成电路制造领域，更具体地说，涉及铜合金互连线（interconnection）及其制备。

背景技术

- 10 半导体制造技术的进展，导致了具有多层互连线的集成电路的发展。在此类集成电路中，一个互连层上的图形化导电材料与另一个互连层上的图形化导电材料之间，通过诸如二氧化硅之类的材料的薄膜而保持电绝缘。这类导电材料通常是金属或金属合金。不同的互连层上的导电材料之间，通过在绝缘层中形成开口并提供导电结构而加以连接，从而使得位于
- 15 不同互连层上的图形化导电材料之间能够保持电连接。这类导电结构通常是指触点或微通路（via）。

- 半导体制造技术的其他进展，导致了数以百万计的晶体管的集成，其中的每一个晶体管都能够高速开关。将如此之多的能够快速开关的晶体管整合到一个集成电路中的后果是，操作过程中的能耗增加。一项能够在降低能耗的同时提高速度的技术是，将传统的用于集成电路的铝和铝合金互
- 20 连线，替换为电阻更小的金属，例如铜。电气领域的熟练技术人员都知道，通过降低电阻，电信号会通过集成电路上的互连通路传播得更快。而且，由于铜的电阻要比铝的电阻小很多，因此，与铝互连线相比，铜互连线的横截面积可以更小一些，而不会导致基于互连线的电阻而产生的信号
- 25 传播延迟的上升。此外，由于两个电节点之间的电容是节点之间正对面积的函数，因此，使用更小的铜互连线会使寄生电容减小。这样，将基于铝的互连线替换为基于铜的互连线，依赖于所选择的尺寸，提供了更小的电阻、更小的电容或两者均有。

如前所述，铜具有一些电学上的优点，例如更低的单位横截面积的电

阻,提供更小的寄生电容的能力,以及更强的对电迁移的抗性。由于所有这些原因,集成电路制造商们发现,把铜包括在他们的产品中是很理想的。

在用于集成电路的互连线时,虽然铜与铝相比具有一些电学上的优势,但纯铜互连线仍然可能会产生一些与电迁移有关的缺陷。

因此,需要提供具有更强的电迁移抗性的基于铜的集成电路互连线。

附图说明

图 1 是一个电镀的嵌入式结构(damascene structure)的横截面示意图,解释了按照本发明的一个间接包裹(encapsulation)方案,其中掺杂剂集中于金属膜的上表面。

图 2 是一个电镀的嵌入式结构的横截面示意图,解释了按照本发明的一个间接包裹方案,其中掺杂剂已经充分扩散,使得它保留在金属膜的上表面。

图 3 是一个电镀的嵌入式结构的横截面示意图,解释了按照本发明的一个间接包裹方案,显示了在 Cu 界面上掺杂剂的聚集。

图 4 是一个电镀的嵌入式结构的横截面示意图,解释了按照本发明的一个直接包裹方案,其中掺杂剂集中于金属膜的底面、侧面和上表面。

图 5 是一个电镀的嵌入式结构的横截面示意图,解释了按照本发明的一个直接包裹方案,其中掺杂剂已经充分扩散,使得它保留在金属膜的上表面。

图 6 是一个电镀的嵌入式结构的横截面示意图,解释了按照本发明的一个直接包裹方案,显示了在 Cu 界面上掺杂剂的富集。

图 7 是一个互连结构的横截面示意图,铜合金元素优选地在该互连结构的界面部分上形成。

图 8 是一个互连结构的横截面示意图, Cu 合金元素优选地在该互连结构的上表面上形成。

图 9 是一个流程图,显示了按照本发明的一个过程中的操作。

图 10 是一个流程图,显示了按照本发明的一个过程中的操作。

具体实施方式

已经证明，通过向铜互连线中添加少量的第二种金属，可以大大地提高铜互连线的电迁移寿命。但是，引入这样的第二种金属之后，一个常见的后果是，与纯铜相比，其导电性降低。

在本发明的一个实施例中，一种基于苯磺酸的 Cu-Sn 电镀浴，使得在电沉积过程中以实时方式控制 Cu 中 Sn 的百分比成为可能。以这种方式，第二种金属，例如 Sn，可以被置于那些已知更容易发生电迁移的区域（例如铜互连线的表面），而同时只有很少的 Sn 被置于互连线的那些不希望其导电性下降的区域（例如金属沟槽（trench）内部）。按照本发明所述的此类电镀过程，使得能够在铜主体(bulk)中沉积下来精确的、很少量（例如 ppm 水平）的 Sn（或其他掺杂元素）。在退火后或室温晶粒生长后，Sn 主要在晶粒边界处积累。在铜晶粒边界上的 Sn，抑制了 Cu 晶粒边界的扩散，并将电迁移活化能提高到约 1.3 eV。除了 Sn 以外，其他可用的掺杂元素包括，但不限于，In, Cd, Zn, Bi, Sb, Mn, Mg, Co, Cr, Ni, Pb, Re, Ru, Rh, Pd, Pt, Os, W, S, C。

按照本发明所述的一种示意性电镀浴，包括低浓度的硫酸和磺酸，以便将掺杂元素从含有掺杂元素离子的铜电镀溶液中“超级填充(superfill)”和沉积出来。磺酸的使用有助于将碳加入到镀层中。由于碳在铜中的溶解度低，可以随后通过退火操作将其驱赶到界面区域。而且，按照本发明，可以通过对电镀过程中的电流密度进行实时改变，而对合金中掺杂元素的浓度加以调控。也就是说，可以用铜制造互连线，其内部主体的掺杂浓度 < 0.5%，而互连线的界面或表面部分的掺杂浓度可以 > 0.5%。电流密度可以通过改变外加电压而加以改变。例如，如果制成的基片带负电更多，那么它就会更强烈地将带正电的离子吸引到基片上。

术语

术语芯片、集成电路、单片器件、半导体器件或元件、微电子器件或元件以及类似的术语和表达方式，在本领域中通常可以互换使用。可以将

上述的全部术语应用于本发明，因为在本领域中，它们一般都能被理解。

术语金属线、迹线（trace）、电线（wire）、导线、信号通路和信号媒介都是相关的。上述的相关术语一般来说是可以互换的，是按照由具体到一般的顺序出现的。在这个领域里，金属线有时被称为迹线、电线、

5 线、互连线，或简单地称为金属。

术语“触点”和“微通路”均指不同互连层之间的导体的电连接结构。在本领域中，这些术语有时可以用于描述在其中形成上述结构的绝缘体中的开口，也可以用于描述所形成的结构本身。对于本发明所公开的内容，触点和微通路是指形成的结构。

10 NHE 是指标准氢电极。

缩写 ppm 是指百万分之一。

基片，也可以称为晶片（wafer）。晶片，可以由半导体材料、非半导体材料、或者半导体材料与非半导体材料结合而制成。硅晶片上可以有多层由不同材料形成的薄膜。可以用其他材料制造晶片，例如 GaAs，蓝宝石上的硅（silicon-on-sapphire），或者绝缘体上的硅（silicon-on-insulator, SOI）。

此处所使用的术语垂直，是指与基片表面基本成直角。

本发明的实施例提供了一种电镀浴，可以将 Cu 合金沉积到 Cu 或 Cu 合金种晶层（seed layer）上。电镀 Cu 合金包括，但不限于，CuSn、CuC、CuS、CuIn、CuCd、CuCr、CuZn、CuBi、CuSb、CuPb、CuMn、CuMg、CuCo、CuNi、CuRe、CuRu、CuW、CuPt、CuPd、CuRh、CuOs。Cu 合金种晶层包括，但不限于，CuSn、CuMg、CuAl、CuTi、CuTa、CuW、CuIn、CuSb、CuZn、CuPd、CuMn、CuCr、CuNi、CuRu、CuRh、CuAu、CuBi、CuCd、CuPt、CuIr、CuOs、CuRe、CuMo、CuZr、CuW。

基于本发明的目的考虑，种晶层，不论是 Cu 还是 Cu 合金，都可以通过物理气相沉积（PVD）、化学气相沉积（CVD）、原子层沉积（ALD）或任何其他适合于形成种晶层的方式加以沉积。Cu 合金种晶层在有或没有阻断层的情况下均可使用。铜扩散阻断层包括，但不限于，Ta、TaN、

TaSiN、W、WN、WSiN、Ti、TiN、TiSiN、Co。阻断层可以通过 PVD、CVD 或 ALD 加以沉积。

本发明的实施例包括一个电镀沉积过程。按照本发明的电镀浴的一个示意性实施例可以通过将下列物质组合在一起而形成：浓度范围为 5-100 g/l 的 Cu 离子；浓度范围为 1-50 g/l（在电镀浴中按重量计小于 10%）的硫酸；浓度范围为 10-100 mg/l 的 Cl 离子；一种或多种磺酸；以及 Sn (II) 离子。一种或多种掺杂元素可以与铜共沉积，包括 Sn, In、Cd、Cr、Zn、Bi、Sb、Pb、Mn、Mg、Co、Ni、Re、W、Ru、Pt、Rh、Pd、C、S、Os。选出的掺杂元素被包括在电镀浴中。此外，有机添加剂包括，但不限于，一种抗抑制剂，例如烷基磺酸硫羟基酯；一种抑制剂，例如聚醚（例如聚乙二醇（PEG）、聚丙二醇（PPG））；以及一种匀平剂，例如聚酰亚胺或聚酰胺，也可以用于电镀浴中。络合剂，例如但不限于，柠檬酸(酯)、酒石酸(酯)、乙二胺四乙酸（EDTA）及乙酸酯，也可以被包括在电镀浴中，以为铜提供更负的沉积电势，而这将有助于那些与 Cu 的电极电势（NHE +0.34V）相差较大的元素与 Cu 发生共沉积，这类元素如 Cr、Mg、Mn（NHE -1.18V）、Co（NHE -0.8V）、Zn（NHE -0.76V）、In（NHE -0.35V）、Ni（NHE -0.25V）。络合剂也可用于为贵金属提供更负的电极电势，如 Pd（NHE +0.99V）、Rh（NHE +0.8V）以及 Pt（NHE +0.73V）。

在上述的示意性电镀浴中，可以提供 Cu 离子的起始原料包括，但不限于，硫酸铜、硝酸铜、氯化铜、甲基磺酸铜、乙磺酸铜、丙磺酸铜、苯磺酸铜以及三氟甲磺酸铜。可以提供 Cl 离子的起始原料包括，但不限于，HCl。磺酸包括，但不限于，甲磺酸（MSA）、乙磺酸（ESA）、丙磺酸（PSA）、苯磺酸（BSA）及三氟甲磺酸（triflic acid — TFA），可用的浓度范围为 0.005 mol/l—2.5 mol/l。可以提供 Sn (II)离子的起始原料包括，但不限于，硫酸锡(II)、乙酸锡(II)、溴化锡(II)、氯化锡(II)、氟化锡(II)、碘化锡(II)及氧化锡(II)，浓度范围为 0.1—200 g/l。

制造合金结构

在本发明的示意性实施例中，电镀过程中的电流密度是变化的，因为按照本发明改变电镀浴中的电流密度，可以控制与铜一起发生沉积的掺杂元素的浓度。这样，就可以在互连结构的特定区域上，形成富含一种或多种掺杂元素的 Cu 合金。具体地说，制造出了一种基于铜的互连线，并且在互连线的外部或界面区域具有合金。

在沉积的起始阶段和结束阶段，上述的电流密度可以较大（例如在 30-100 mA/cm² 范围内），以便使 Cu 可以与更高浓度的掺杂元素（例如按重量计 >0.5%）发生沉积。相反地，较小的沉积电流密度（例如 0.5-30 mA/cm²）可以使 Cu 与低浓度的掺杂元素（例如按重量计 <0.5%）发生沉积。在同一电镀工具中，可以在沉积结束后很快或立即进行退火操作，以形成并固定 Cu 合金的微观结构。该退火操作也可以将掺杂元素驱赶到界面和晶粒边界处。退火温度可以在一定范围内变化：在第一次操作的时候，退火温度较低，低于 250℃，以提高铜晶粒的尺寸并将杂质驱赶到界面上；而在第二次操作时，退火温度较高（>250℃），以便优选地在界面上形成 Cu 合金。

在本发明的另一个实施例中，在化学机械抛光（CMP）之后进行退火，从而使得掺杂元素能够扩散到界面上并形成包裹式结构。在 CMP 之后的这一退火操作，可以在不同的温度（低和高）下，在电镀工具的综合退火腔、独立熔炉或快速热处理（RTP）设备中进行。在 CMP 之后的这一退火操作，也可以在蚀刻阻止/ILD 沉积的过程中或之前进行。

在其上表面具有 Cu 合金的 Cu 互连线

按下述方法制备了按照本发明的一个实施例所述的互连结构：在沉积操作的结束阶段采用较大的电流密度，使得一种或多种掺杂元素优选地与 Cu 共沉积；而沉积的大部分是在相对更小的电流密度下进行的，以便使 Cu 可以与较低浓度的一种或多种掺杂元素（< 0.5%）发生沉积。在电镀沉积完成后进行退火操作，使得一种或多种掺杂元素可以向充满 Cu 的沟槽的顶部扩散，而同时很低浓度的 Sn（也就是，<100 ppm）仍保留在铜主体的晶粒边界上。

图 1-3 更详细的解释了此结构和过程。图 1 示出部分处理地晶片的一个部分的横截面。更具体地说，图 1 示出层间电介质 (ILD) 102, 该 ILD102 已经图形化以在其中形成沟槽 101 和微通路 103。部分处理晶片被置于含有 Cu 离子以及一种或多种掺杂元素离子的电镀浴中。然后，在 5 ILD 102 上镀一层铜 104，使得沟槽 101 和微通路 103 都被充满，并且 ILD 102 的上表面也覆盖上了一层铜 104。当还处于用来镀铜 104 的电镀浴中时，将电流密度提高，从而使得存在于电镀浴中的一种或多种掺杂元素离子与铜发生共沉积，形成铜合金层 106。电流密度是经过选择的，从而使得铜层 104 中掺杂原子的量按重量计小于 0.5%，并且铜合金层 106 中掺杂原子的量按重量计大于 0.5%。

参见图 2，在退火操作完成后，图 1 的结构显示了出来。在这个实施例中，退火操作是在低于 450°C 的温度下，在 0.5 到 180 分钟的时间内，在 N₂、Ar 或 N₂+H₂（也就是形成气体）环境中完成的。在另一个实施例中，退火操作分两步进行：首先，在 100°C 到 250°C 的温度下，在 0.5 到 15 180 分钟的时间内，在 N₂、Ar 或 N₂+H₂（也就是形成气体）环境中进行第一次退火；然后，在 250°C 到 450°C 的温度下，在 0.5 到 180 分钟的时间内，在 N₂、Ar 或 N₂+H₂（也就是形成气体）环境中进行第二次退火。此退火操作将掺杂元素通过铜层 104 的顶部从铜合金层 106 中驱赶出来。一些掺杂原子也被驱赶着向铜层 104 的界面移动，形成铜合金层 108，如图 20 2 所示。

图 3 示出完成了化学机械抛光 (CMP) 之后的图 2 的结构。该 CMP 操作除去了覆盖于 ILD 102 上表面的金属，从而产生了单个的互连线，这些互连线具有如图 3 所示的铜部分 104 和铜合金部分 108。位于互连结构上表面的铜合金部分的形状是，在靠近沟槽的垂直侧面的地方一般是薄的，而越靠近互连结构的中间则越厚。

由 Cu 合金包裹的 Cu 互连结构

在本发明的一个实施例中，按下述方法制备了一种基于铜的互连结构：令铜与一种或多种掺杂元素发生共沉积，然后对电镀的铜—掺杂剂材

料进行原位退火，将一种或多种低溶解度的掺杂元素驱赶到互连结构的界面部分。这样的互连结构也可以通过下述方法制备：在沉积的初始阶段使用更大的电流密度 ($> 30 \text{ mA/cm}^2$)，使铜与更高浓度的掺杂元素发生共电镀(co-plating)；然后在较小的电流密度 ($< 30 \text{ mA/cm}^2$) 下镀铜，使得在互连结构的内部主体部分中，掺杂元素的浓度相对较低；然后，在较大的电流密度 ($> 30 \text{ mA/cm}^2$) 下镀铜，使得在互连结构的顶部（也就是后沉积的部分）中掺杂元素的浓度相对较高。

在电镀操作完成后，进行退火操作，以便掺杂元素可以向充满铜的沟槽的顶部扩散。

10 图 4-6 更详细的解释了这一结构和过程。图 4 示出部分处理晶片的一个部分的横截面。更具体地说，图 4 示出层间电介质 (ILD) 402，该 ILD402 已经图形化并在其中形成了沟槽 401 和微通路 403。部分处理晶片被置于含有 Cu 离子以及一种或多种掺杂元素离子的电镀浴中。然后，在 ILD 402 上镀一层铜合金 404，使得沟槽 401 和微通路 403 的表面都被覆盖住，并且 ILD 402 的上表面也覆盖上了一层铜合金 404。在图示的实施例中，Sn 与铜共沉积以形成铜合金 404，该层沉积的厚度大约在 100 到 500 埃。通过一种或多种掺杂元素与铜从电镀浴中共沉积而制得铜合金 404。当还处于用来镀铜合金 404 的电镀浴中时，将电流密度减小，从而使得存在于电镀浴中的掺杂元素不与铜发生共沉积，以形成铜层 406。如图 4 所示，铜层 406 填充了沟槽 401 和微通路 403 之中那些没有被铜合金层 404 所占据的部分。电流密度是经过选择的，从而使得铜合金层 404 中掺杂原子的量按重量计大于 0.5%，并且铜层 406 中掺杂原子的量按重量计小于 0.5%。在层 406 形成后，提高电流密度，使得一种或多种掺杂元素原子与铜再次从电镀浴中共沉积，从而形成铜合金层 408。

25 参见图 5，在退火操作完成后，图 4 的结构显示了出来。在这个实施例中，退火操作是在低于 450°C 的温度下，在 0.5 到 180 分钟的时间内，在 N_2 、Ar 或 $\text{N}_2 + \text{H}_2$ （也就是形成气体）环境中完成的。在另一个实施例中，退火操作分两步进行：首先，在 100°C 到 250°C 的温度下，在 0.5 到 180 分钟的时间内，在 N_2 、Ar 或 $\text{N}_2 + \text{H}_2$ （也就是形成气体）环境中进行

第一次退火；然后，在 250℃到 450℃的温度下，在 0.5 到 180 分钟的时间内，在 N₂、Ar 或 N₂+H₂（也就是形成气体）环境中进行第二次退火。此退火操作将掺杂元素通过铜层 406 的一部分从铜合金层 406、408 中驱赶出来，如图 4 所示。通过将 these 掺杂原子向铜层 406 的界面表面驱赶，一个自包裹的铜区域形成了。也就是说，铜 406 被退火后铜合金 410 包围起来了。

图 6 示出完成了化学机械抛光（CMP）操作之后的图 5 的结构。该 CMP 操作除去了覆盖于 ILD 402 上表面的金属，从而产生了单个的互连线，这些互连线具有如图 6 所示的铜部分 406 和铜合金部分 410。位于互连结构上表面的铜合金部分的形状是，在靠近沟槽的垂直侧面的地方一般是薄的，而越靠近互连结构的中间则越厚。

在本发明的另一个实施例中，在多余的金属通过 CMP 除去之后进行退火。在 CMP 之后的这一退火操作，可以在不同的温度（低和高）下，在电镀工具的综合退火腔、独立熔炉或快速热处理（RTP）设备中进行。而且按照本发明，这一退火操作可以在蚀刻阻止或 ILD 层的沉积过程中或之前进行。

图 7 示出晶片的一个部分的横截面，该晶片具有被 ILD 层包围的铜互连线和微通路。更具体地说，铜互连线和微通路具有包围着它们的核心区域的自包裹层。这些自包裹层是由铜合金形成的。铜合金不但可以按照上面所述用于改善电迁移性质，而且在使用铜合金后，就不需要单独形成的铜扩散阻断层，而铜扩散阻断层存在于传统的铜互连线中。图 8 与图 7 相似，但解释了本发明的一个实施例，其中铜合金层形成于铜互连线的顶部。

图 9 解释了按照本发明的一种方法。如框 902 所示，在第一电流密度下，将铜从电镀浴中镀到基片上，该电镀浴中含有硫酸、一种磺酸、铜离子和掺杂离子。然后，如框 904 所示，将电流密度改为第二个值，从同一电镀浴中将铜合金镀到先前已经沉积下来的铜上。

图 10 解释了本发明的一个实施例，其中形成了被包裹起来的铜互连结构。包裹的意思是，铜互连结构的核心部分或内部被铜合金区域所包

围。如图 10 中的框 1002 所示,在第一电流密度下,将铜合金从电镀浴中镀到基片上,该电镀浴中含有硫酸、一种磺酸、铜离子和掺杂离子。该电流密度是经过选择的,使得存在于电镀浴中的掺杂元素可以与铜发生共沉积。此铜合金层通常形成于先前已经制备好的种层上。如框 1004 所示,在第二个较小的电流密度下,从同一电镀浴中将铜镀到先前已经沉积下来的铜合金上。如框 1006 所示,另一层铜合金从同一电镀浴中被镀到铜层上。该铜合金是在第三电流密度下沉积下来的,这第三电流密度要大于第二电流密度。第一和第三电流密度可以相等,但并不要求其相等。如框 1008 所示,对基片进行退火,使得铜合金区域中的掺杂原子被驱赶到铜层部分中,包括界面部分,从而在铜互连结构的核心部分周围形成一个自包裹区域。

结论

本发明的实施例提供了基于铜的互连结构,以及其制备的方法和化学组成。更具体地说,通过使用一种电镀浴,制备了嵌入式的基于铜的互连线,该电镀浴中含有由低浓度的硫酸($< 50 \text{ g/l}$)和磺酸组成的混合物,可以对掺杂元素进行“超级填充”和共镀。掺杂元素的浓度可以通过改变电镀过程中的电流密度而加以调节,从而在互连结构的界面区域形成更高的掺杂元素浓度,以便在没有显著牺牲未掺杂 Cu 线的电阻率的情况下,改善电迁移抗性。在两者之间没有任何显著延时的情况下,通过在电镀后进行退火,例如在一个具有综合退火腔的电镀工具中进行退火,可以令掺杂元素扩散至界面区域,从而在界面上形成合金。退火温度可以由低(例如 $< 250^\circ\text{C}$)到高($> 250^\circ\text{C}$)进行变化,以便优选地在界面处形成合金。制备按照本发明的基于铜的互连线,可以得到被掺杂元素合金所包裹的互连线。制备被 Re、Ru 或 W 所包裹的 Cu 线,可以得到一个内嵌的阻断层。换句话说,通过制备具有 Re、Ru 或 W 的铜线,可以在互连线的外部(也就是界面区域)得到掺杂元素合金,该合金起到了减少或阻止铜原子向周围的电介质层扩散的作用。按照本发明制备的 Cu 互连结构,也可以在上界面或底部界面含有铜合金。

关于 CuSn 电镀，组合，例如：（a）具有基本均一的平均值，在电镀金属膜中 Sn 的含量很低，Sn 主要在晶粒边界处；（b）在线和微通路的底部具有更高的 CuSn 浓度；（c）在线和微通路的顶部具有更高的 CuSn 浓度；（d）在线和微通路的顶部和底部具有更高的 CuSn 浓度。也应当注意，退火可以在 Cu 电镀之后、或在对沉积的铜层进行 CMP 之后、或在 Cu 电镀和 CMP 都完成之后进行。

本发明一些实施例的一个优点是，氮化硅对铜互连线的吸附改善了。

本发明一些实施例的一个优点是，不需要氮化硅蚀刻阻止层。

本发明一些实施例的一个优点是，基于铜的互连线的耐磨性提高。

10 本发明一些实施例的一个优点是，在退火操作过程中形成的小丘减少了。

本发明一些实施例的一个优点是，相对于纯铜和阻断层之间的吸附而言，铜合金和阻断层之间的吸附改善了，因为铜合金里的掺杂成分可以与阻断层（例如，铜的 Sn 合金与基于 Ta 的阻断层）形成一个金属互化物。

15 本发明一些实施例的一个优点是，由铜合金包裹的铜互连线提供了机械支架，以支持铜线。当基于 SiO₂ 的层间电介质材料被刚性更差的低-k 和超低-k 电介质材料所取代时，这一点尤其有用。

对于本领域的熟练技术人员而言，在阅读本公开材料之后，针对此处所清晰描述的装置、清洁方案和过程而进行的其他修改将会是显而易见的。因此，正如所附的权利要求所描述的，所有的此类修改和改变将会被认为落入了本发明的精神和范围之中。

20

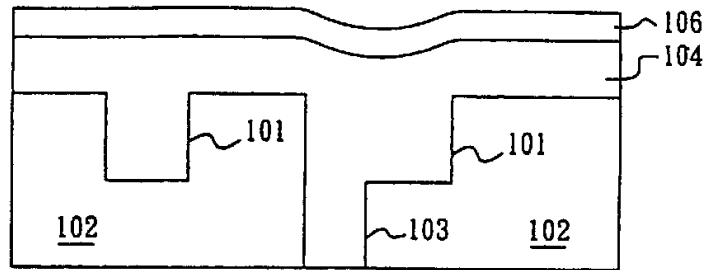


图1

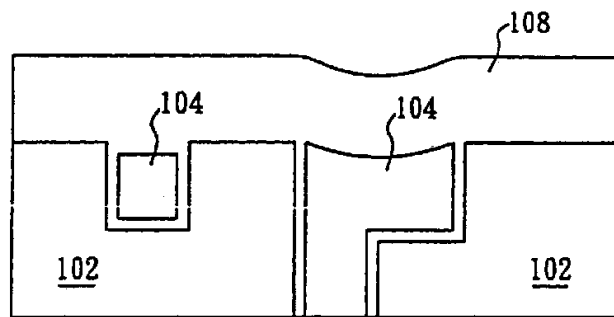


图2

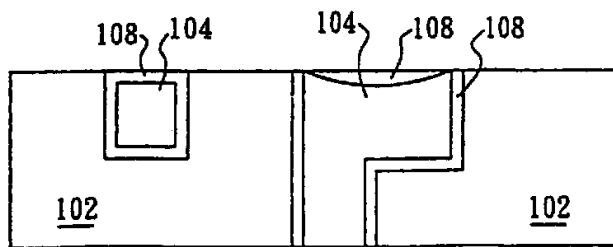


图3

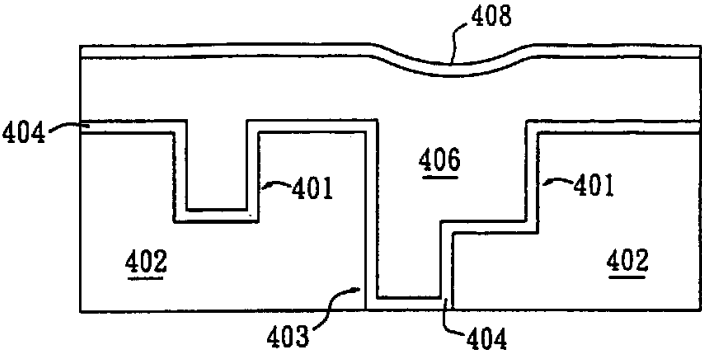


图4

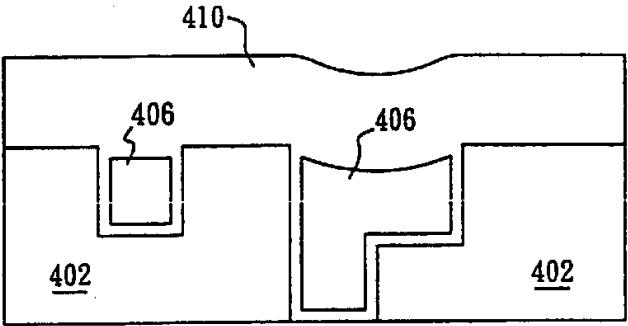


图5

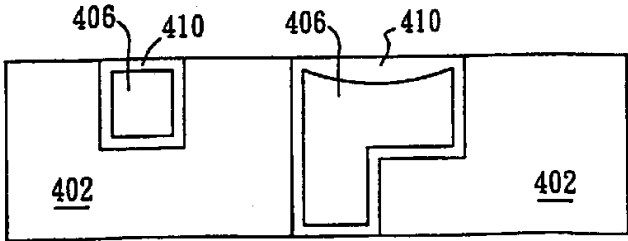


图6

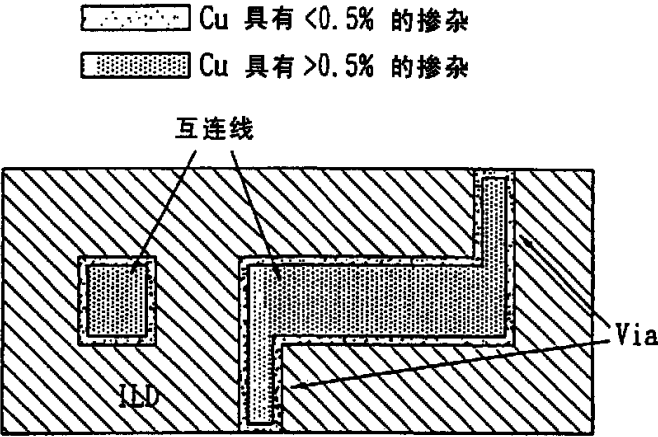


图7

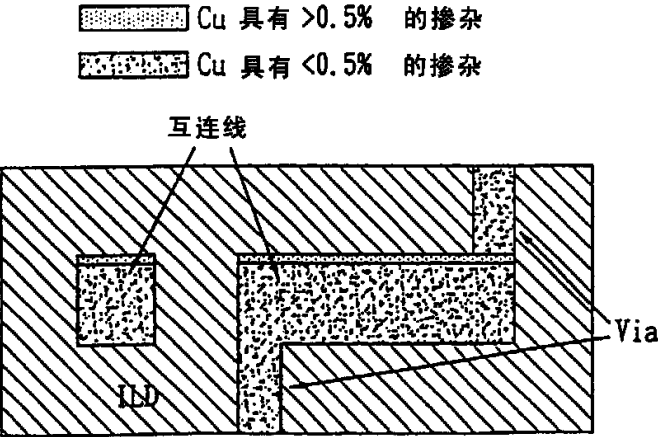


图8

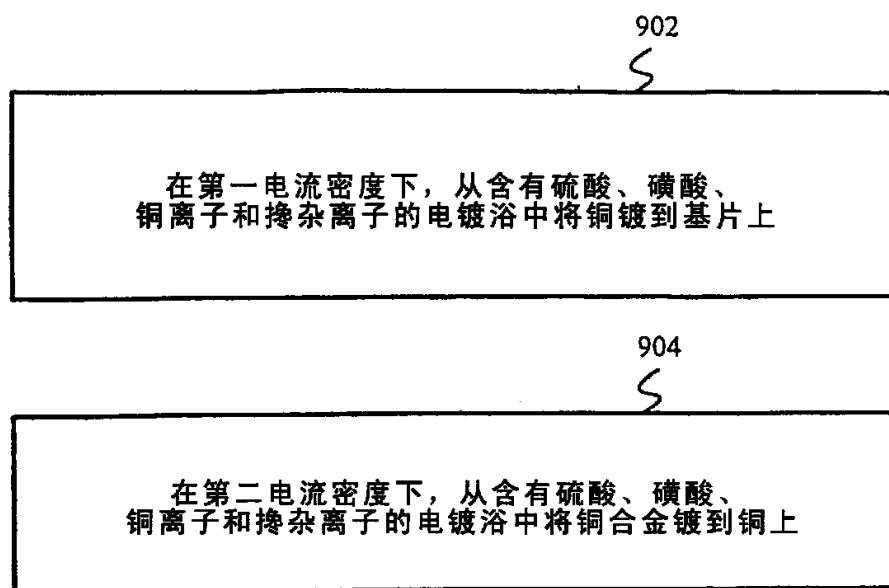


图9

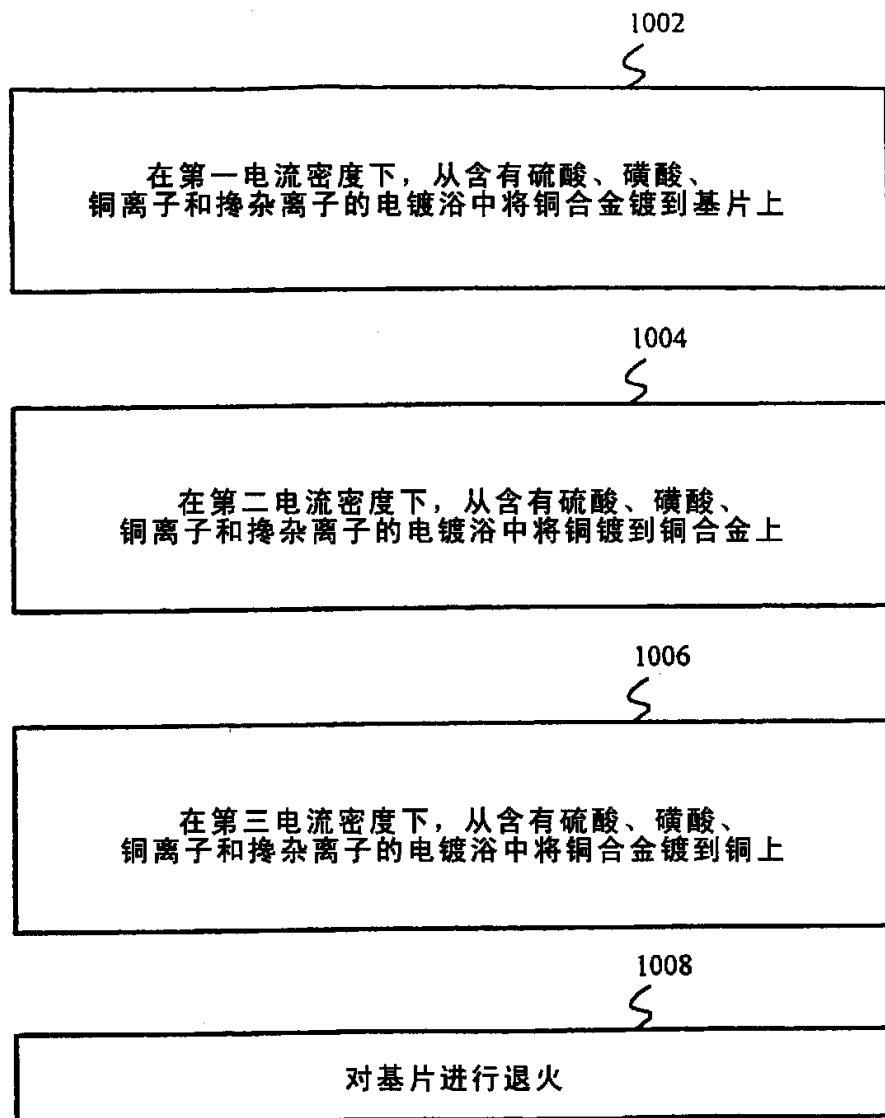


图10

Electronic Acknowledgement Receipt	
EFS ID:	29318353
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	45209
Filer:	Tatiana Rossin/Juanita Briscoe
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Attorney Docket Number:	42P38794DC
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Application Type:	Utility under 35 USC 111(a)

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	P38794DC_IDS.pdf	25159	no	2
			4745c91e2bb0de07e0fe8599bdb25377eeff5f5		
Warnings:					

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	P38794DC_1449.pdf	28307	no	1
			49fde068169163be6dfbed12188132d33b ee08c		
Warnings:					
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3	Foreign Reference	CN1575508A_English.pdf	128235	no	15
			95e755bbc0c00e628f4e3d6ce09fe092b32e 5c9d		
Warnings:					
Information:					
4	Foreign Reference	CN1575508A.pdf	932239	no	20
			063fc3500191afc59da3bedd4784a5218bb 7a8b7		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Boyan Boyanov et al.

Application No.: 15/477,506

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INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

- X 37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
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- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
- (2) Charge Deposit Account No. 02-2666 \$180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: May 25, 2017

/Tatiana Rossin/
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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>	<i>Complete if Known</i>	
	Application Number	15/477,506
	Filing Date	April 3, 2017
	First Named Inventor	Boyan Boyanov
	Group Art Unit	2898
	Examiner Name	Not yet assigned
Sheet 1 of 1		Attorney Docket No: 42P38794DC

US PATENT DOCUMENTS					
Examiner Initial *	Cite No ¹	USP Document Number	Publication or Issue Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No ¹	Foreign Patent Document Country Code/Number/Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		KR 1020100109932	10-11-2010	International Business Machines Corporation		X
		WO 2009098120A1	08-13-2009	International Business Machines Corporation		
		JP 2009506536A	02-12-2009	Freescale Semiconductor		X
		WO 2007024470A2	03-01-2007	Freescale Semiconductor		

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

EXAMINER	DATE CONSIDERED
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Based on PTO/SB/08A(09-06) - Substitute Disclosure Statement Form (PTO-1449) as modified by BSTZ 03/26/07
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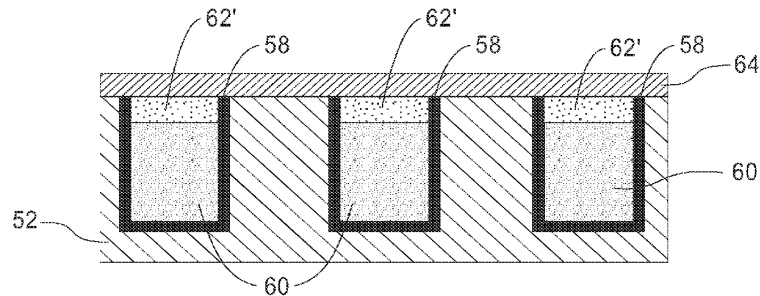
전체 청구항 수 : 총 10 항

(54) 높은 누설 저항을 갖는 상호연결 구조체

(57) 요약

도전성 피쳐(즉, 도전 물질)가 유전 물질의 상부 표면과 동일 평면이 아니고, 대신에 도전 물질이 유전 물질의 상부 표면 아래에 리세스되는 상호연결 구조체가 제공된다. 유전 물질의 상부 표면 아래에 리세스되는 것뿐만 아니라, 본 발명에 따른 상호연결 구조체의 도전 물질은 모든 표면(즉, 측벽 표면들, 상부 표면 및 바닥 표면)이 확산 장벽 물질에 의해 둘러싸인다. 종래 기술의 상호연결 구조체들과는 달리, 리세스된 도전 물질의 상부 표면 위에 위치하는 장벽 물질은 리세스된 도전 물질을 포함하는 개구와 함께 위치한다.

도 2g



특허청구의 범위

청구항 1

대략 4.0 이하의 유전 상수를 갖는 유전 물질;

상기 유전 물질 내에 매립(embedded)되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 도전 물질 - 상기 도전 물질의 상기 상부 표면은 상기 유전 물질의 상부 표면 아래에 위치함 - ;

상기 도전 물질의 상기 측벽 표면들 및 상기 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽(U-shaped diffusion barrier); 및

상기 도전 물질의 상기 상부 표면 상에 위치하고, 적어도 상기 U-형 장벽의 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성(diffusion barrier properties)을 갖는 절연층 또는 금속층

을 포함하는, 상호연결 구조체.

청구항 2

제1항에 있어서,

상기 유전 물질의 상기 상부 표면 및 확산 장벽 속성을 갖는 상기 절연층 또는 금속층의 상부 표면 상에 위치하는 유전 캐핑층(dielectric capping layer)을 더 포함하는, 상호연결 구조체.

청구항 3

제2항에 있어서,

상기 유전 캐핑층은 SiC, Si₃N₄, SiO₂, 탄소 도핑된 산화물 및 질소와 수소 도핑된 탄화 규소 SiC(N,H) 중 하나를 포함하는, 상호연결 구조체.

청구항 4

제1항 내지 제3항 중 어느 한 항에 있어서,

상기 유전 물질은 SiO₂, 실세스퀴옥산(silsesquioxane), Si, C, O 및 H의 원자들을 포함하는 C 도핑된 산화물 및 열경화성 폴리아릴렌 에테르(thermosetting polyarylene ether) 중의 하나를 포함하는, 상호연결 구조체.

청구항 5

제1항 내지 제4항 중 어느 한 항에 있어서,

상기 U-형 확산 장벽은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa₂, W 또는 WN을 포함하는, 상호연결 구조체.

청구항 6

제1항 내지 제5항 중 어느 한 항에 있어서,

상기 도전 물질과 상기 U-형 확산 장벽 사이에 위치하는 U-형 도금 시드층을 더 포함하고, 상기 U-형 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru 또는 Ru 합금을 포함하는, 상호연결 구조체.

청구항 7

제1항 내지 제6항 중 어느 한 항에 있어서,

상기 도전 물질은 순수형 또는 합금형 Cu, W 또는 Al을 포함하는, 상호연결 구조체.

청구항 8

제1항 내지 제7항 중 어느 한 항에 있어서,

확산 장벽 속성을 갖는 상기 절연층 또는 금속층은 탄화 규소, 질화 규소, 질소와 수소 도핑된 탄화규소 및 순

수형, 합금형 또는 질화형 Ta, Ru, Ir, W, Co, Ti 및 Rh로부터 선택되는 금속 물질 중 하나를 포함하는, 상호연결 구조체.

청구항 9

대략 4.0 이하의 유전 상수를 갖는 유전 물질;

상기 유전 물질 내에 매립되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 구리 함유 도전 물질 - 상기 구리 함유 도전 물질의 상기 상부 표면은 상기 유전 물질의 상부 표면 아래에 위치함 - ;

상기 구리 함유 도전 물질의 상기 측벽 표면들 및 상기 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽; 및

상기 도전 물질의 상기 상부 표면 상에 위치하고, 적어도 상기 U-형 장벽의 적어도 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성을 갖는 절연층 또는 금속층

을 포함하는, 상호연결 구조체.

청구항 10

상호연결 구조체를 형성하는 방법으로서,

약 4.0 이하의 유전 상수를 갖는 유전 물질 내로 적어도 하나의 개구를 형성하는 단계 - 상기 유전 물질은 상기 유전 물질의 상부 표면 상에 위치하는 패터닝된 하드 마스크를 가짐 - ;

상기 적어도 하나의 개구와 상기 패터닝된 하드 마스크를 확산 장벽으로 라이닝(lining)하는 단계;

상기 적어도 하나의 개구를 도전 물질로 부분적으로 채우는 단계 - 상기 도전 물질은 상기 유전 물질의 상부 표면 아래에 위치하는 상부 표면을 가짐 - ;

상기 적어도 하나의 개구 내와 상기 도전 물질의 상기 상부 표면 상뿐만 아니라 상기 패터닝된 하드 마스크를 라이닝하는 상기 확산 장벽의 위에 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질을 형성하는 단계; 및

상기 적어도 하나의 개구 내에 확산 장벽 속성을 갖는 상기 절연 물질 또는 금속 물질의 또 다른 부분을 유지하고 상기 적어도 하나의 개구 내에 U-형 확산 장벽을 형성하고, 상기 유전 물질의 상기 상부 표면 위에 위치하는 상기 패터닝된 하드 마스크와 상기 확산 장벽 및 상기 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 일부분을 제거하는 단계를 포함하고,

확산 장벽 속성을 갖는 상기 절연 물질 또는 금속 물질의 상기 또 다른 부분은 상기 유전 물질의 상기 상부 표면과 동일 평면 상의(coplanar) 상부 표면을 갖고, 상기 도전 물질은 상기 도전 물질의 측벽 표면들 및 바닥 표면 상에 위치한 상기 U-형 확산 장벽에 의해 완전히 둘러싸이며, 확산 장벽 속성을 갖는 상기 절연 물질의 상기 또 다른 부분은 상기 도전 물질의 상기 상부 표면 상에 위치하는, 상호연결 구조체 형성 방법.

명세서

기술분야

[0001] 본 발명은 반도체 구조체와 이의 제조 방법에 관한 것이다. 본 발명은 더 구체적으로는 상호연결 유전체(interconnect dielectric)의 상부 표면에 높은 누설 저항을 가질뿐만 아니라, 금속성 잔류물들(metallic residues)(예를 들어, 결함들)이 없는 반도체의 상호연결 구조체와 이의 제조 방법에 관한 것이다. 상호연결 유전체의 상부 표면에서 금속성 잔류물(예를 들어, 결함들)이 형성되는 것을 피하면서, 상호연결 구조체 내의 누설저항이 개선된다.

배경기술

[0002] 일반적으로 반도체 장치들은 반도체 기판 상에 제조되는 집적회로(IC)를 형성하는 복수의 회로를 포함된다. 신호 경로들의 복합 네트워크는 일반적으로 기판의 표면 상에 분포된 회로 소자들을 연결하기 위해 라우팅된다. 장치에 걸쳐서 이러한 신호들의 효율적인 라우팅은 예를 들어 싱글 또는 듀얼 다마신 배선 구조(damascene wiring structures)와 같은 멀티레벨 또는 다층(multilayered) 기법들의 형성을 요구한다. 배선 구조는 일반적

으로 구리, Cu 또는 Cu 합금을 포함하는데, 이는 Cu 기반 상호연결체들이 알루미늄, Al 기반 상호연결체들과 비교했을 때 복합 반도체 칩 상의 많은 수의 트랜지스터들 사이의 더 높은 속도의 신호 전송을 제공하기 때문이다.

[0003] 일반적인 상호연결 구조체 내에서, 금속 비아들(vias)은 반도체 기판에 수직하게 배열되고 금속 선들은 반도체 기판에 평행하게 배열된다. 오늘날의 IC 제품 칩들은 4.0 미만의 유전 상수를 갖는 유전 물질에 금속 선들과 금속 비아들(예를 들어, 도전성 피쳐들(conductive features))을 매립(embedding)함으로써, 신호 속도의 추가적인 향상과 인접하는 금속 선들의 신호("크로스토크(crosstalk)"로 알려짐)의 감소를 달성하였다.

[0004] 현재의 반도체 상호연결 구조체들에서는, TDDB(time-dependent-dielectric-breakdown)가 Cu 기반 금속층(metallurgy)과 낮은 k 유전 물질(low K dielectric materials)을 포함하는 미래의 상호연결 구조체들에 대한 주요 신뢰성 문제들 중의 하나로 파악된다. "TDDB"는 상호연결 구조체의 유전 물질이 시간이 경과함에 따라 손상이 생기기 시작한다는 것을 의미한다. 유전 물질의 손상은 상호연결 구조체를 준비하는 동안 상호연결 유전 물질의 표면 상에 형성되는 진성 수단(intrinsic means) 또는 결함들에 의해 유발될 수 있다.

[0005] 상호연결 유전체 표면을 따라서 나타나는 금속 이온, 특히 Cu 이온의 누설이 TDDB에 기여하는 주요 진성 손상 메커니즘으로 파악된다. 도 1a는 이러한 진성 누설 현상을 나타내는 선행 기술의 상호연결 구조체(10)이다. 구체적으로, 선행 기술의 상호연결 구조체는 Cu 피쳐(14)가 매립된 유전 물질(12)을 포함한다. Cu 피쳐(14)는 일반적으로 확산 장벽(diffusion barrier; 16)에 의해 유전 물질(14)로부터 분리된다. 유전 캐핑 층(dielectric capping layer; 18)은 유전 물질(14), 확산 장벽(16) 및 Cu 피쳐(14)의 표면 상에 존재한다. 도 1a에서 화살표들은 도시된 바와 같이 상호연결 구조체의 상부 표면을 따라 발생하는 도전성 피쳐(14)로부터의 Cu 이온들의 누설(확산)을 표시한다. 시간이 경과함에 따라, 이러한 Cu 이온들의 누설은 TDDB뿐만 아니라 상호연결 구조체 내의 장치들의 손상을 발생시킨다.

[0006] 도 1b에 도시된 바와 같이, TDDB에 대한 또 다른 기여 인자는 결함과 연관되어 있다. 구체적으로, 도 1b는 Cu 잔류물(20)(예를 들어, 결함)이 유전 물질(12)의 상부 표면과 유전 캐핑 층(18) 사이의 인터페이스에 존재하는 도 1a에 도시된 컴포넌트들을 포함하는 또 다른 선행 기술의 상호연결 구조체(10')이다. Cu 잔류물(20)은 Cu 피쳐(14)(즉, 유전 물질(12) 내로 형성되는 개구 내의 Cu의 피착(deposition) 및 연마(planarization))가 형성되는 동안 형성된다. 유전 물질의 표면에 결함을 제공하는 포스트 연마 Cu 잔류물들은 TDDB 손상의 주요 원인들 중 하나이다.

[0007] 위에서 Cu가 선행 기술의 상호연결 구조체들과 관련하여 구체적으로 설명되었지만, 전술한 누설과 결함 문제들은, 예를 들어 Al 및 W와 같은 다른 유형의 도전성 금속들에서도 (상당한 속도 및 정도로) 일어난다는 것을 유의해야 한다.

[0008] 도 1a에 도시된 누설 문제와 도 1b에 도시된 잔류물 문제에 비추어 볼 때, 금속 누설, 특히 Cu 이온 확산과 금속성 잔류물, 특히 Cu 잔류물 모두가 상호연결 구조체로부터 감소되거나 또는 완전하게 제거될 수 있는 상호연결 구조체를 제공해야 할 계속적인 필요성이 있다.

발명의 내용

[0009] 본 발명은 높은 누설 저항을 갖고 상호연결 구조체의 특정 상호연결 레벨의 상부 유전체 표면에서 금속성 잔류물이 없는 상호연결 구조체를 제공한다. 이와 같은 본 발명의 상호연결 구조체는 선행 기술의 상호연결 구조체들과 비교하여 개선된 TDDB를 나타낸다.

[0010] 본 발명의 상호연결 구조체에서, 도전성 피쳐(예를 들어, 도전 물질)는 유전 물질의 상부 표면과 동일 평면 상에 있지 않지만, 대신에 도전 물질은 유전 물질의 상부 표면 아래에 리세스(recess)된다. 유전 물질의 상부 표면 아래에 리세스되는 것뿐만 아니라, 본 발명의 상호연결 구조체의 도전 물질은 모든 면(예를 들어, 측벽의 표면들, 상부 표면 및 하부 표면)이 확산 장벽 물질에 의해 둘러싸인다. 리세스된 도전 물질의 측벽 표면들과 바닥 표면은 U-형 확산 장벽으로 라이닝된다(lined). 리세스된 도전 물질의 상부 표면은 절연층 또는 금속층으로 라이닝된다. 도전 물질의 상부 표면을 라이닝하는 절연층 또는 금속층의 예지 부분들은 U-형 확산 장벽의 상부 측벽 표면들과 접하거나 또는 도금 시드 층(plating seed layer)이 존재한다면 선택적인 도금 시드 층과 접한다. 리세스된 도전 물질의 상부 표면을 라이닝하는 절연층 또는 금속층 모두는 확산 장벽 속성(diffusion barrier properties)을 갖는다. 리세스된 도전 물질이 확산 장벽 물질에 의해서 완전히 둘러싸이므로, 유전 물질의 표면에서의 금속 이온의 누설은 완전히 또는 현저하게 제거된다.

- [0011] 선행 기술의 상호연결 구조체들과는 달리, 리세싱된 도전 물질의 상부 표면상에 위치한 장벽 물질은 본 발명의 상호연결 구조체의 리세싱된 도전 물질을 포함하는 개구와 함께 위치한다. 선행 기술의 상호연결 구조체에서는, 도전성 피처(즉, 도전 물질)의 위에(atop) 형성된 임의의 장벽층이, 예를 들어 스패닝(spanning)과 같은 개구의 위에 존재하고 본 발명의 상호연결 구조체의 경우와 같이 도전 물질을 포함하는 개구 내에 존재하지 않는다.
- [0012] 본 발명의 상호연결 구조체에서는, 리세싱된 도전 물질과 유전 물질 사이에 직접적인 접촉이 있지 않고 유전 물질의 표면 상에 연장되는 도전 물질의 연마가 사용되지 않아서, 선행 기술의 상호연결 구조체들의 경우처럼 상호연결 유전 물질의 상부 표면에서 도전성 잔류물들이 형성되지 않는다는 것을 또한 유의해야 한다. 상기 태양은 유전체 표면 상의 도전성 금속 잔류물(예를 들어, 결합)을 상당히 감소시키거나 또는 심지어 제거시키는데 현저한 효과를 가진다. 이와 같이, 본 발명은 높은 체적에서 제조될 수 있는, 신뢰성 있고 기술적으로 확장 가능한 상호연결 구조체를 제공한다.
- [0013] 일반적인 용어로, 본 발명의 상호연결 구조체는,
- [0014] 약 4.0 이하의 유전 상수를 갖는 유전 물질;
- [0015] 유전 물질 내에 매립되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 도전 물질(도전 물질의 상부 표면은 유전 물질의 상부 표면 아래에 위치함);
- [0016] 도전 물질의 측벽 표면들 및 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽; 및
- [0017] 도전 물질의 상부 표면 상에 위치하고, 적어도 U-형 장벽의 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성을 갖는 절연층 또는 금속층을 포함한다.
- [0018] 본 발명의 상호연결 구조체의 일부 실시예에서, 유전 캐핑층이 또한 제공되며, 유전 캐핑층은 유전 물질의 상부 표면 및 확산 장벽 속성을 갖는 절연층 또는 금속층의 상부 표면 상에 위치한다. 이러한 실시예에서, 유전 캐핑층은 SiC, Si₃N₄, SiO₂, 탄소 도핑된 산화물 및 질소와 수소 도핑된 탄화 규소 SiC(N,H) 중 하나를 포함할 수 있다.
- [0019] 본 발명의 상호연결 구조체의 다른 실시예에서, 다공성(porous) 또는 비다공성(non-porous)일 수 있는 유전 물질은 SiO₂, 실세스퀴옥산(silsesquioxane), Si, C, O 및 H의 원자들을 포함하는 C 도핑된 산화물 및 열경화성 폴리아릴렌 에테르(thermosetting polyarylene ether) 중의 하나를 포함할 수 있다.
- [0020] 본 발명의 또 다른 실시예에서, 본 발명의 상호연결 구조체 내의 U-형 확산 장벽은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W 또는 WN을 포함할 수 있다.
- [0021] 본 발명의 상호연결 구조체의 또 다른 실시예에서, U-형 도금 시드층이 또한 제공되며 U-형 도금 시드층은 적어도 하나의 도전 물질과 U-형 확산 장벽 사이에 위치한다. 이러한 경우에, 절연층 또는 금속층의 에지 부분들은 U-형 도금 시드층의 상부 측벽 표면과 직접적으로 접한다. U-형 도금 시드층은 도전 물질이 도금 프로세스에 의해 형성될 때 사용된다. U-형 도금 시드층이 존재할 때, U-형 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru 또는 Ru 합금을 포함할 수 있다.
- [0022] 본 발명의 상호연결 구조체의 또 다른 실시예에서, 적어도 하나의 도전 물질은 순수형 또는 합금형 Cu,W 또는 Al을 포함할 수 있다.
- [0023] 본 발명의 바람직한 실시예에서, 상호연결 구조체가 제공되며, 상호연결 구조체는 약 4.0 이하의 유전 상수를 갖는 유전 물질; 유전 물질 내에 매립되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 구리 함유 도전 물질(구리 함유 도전 물질의 상부 표면은 유전 물질의 상부 표면 아래에 위치함); 구리 함유 도전 물질의 측벽 표면들 및 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽; 및 도전 물질의 상부 표면 상에 위치하고, 적어도 U-형 장벽의 적어도 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성을 갖는 절연층 또는 금속층을 포함한다.
- [0024] 본 발명의 바람직한 상호연결 구조체의 일부 실시예에서, 유전 캐핑층이 또한 제공되며, 유전 캐핑층은 유전 물질의 상부 표면 및 확산 장벽 속성을 갖는 절연층 또는 금속층의 상부 표면 상에 존재한다. 이러한 실시예에서, 유전 캐핑층은 SiC, Si₃N₄, SiO₂, 탄소 도핑된 산화물 및 질소와 수소 도핑된 탄화 규소 SiC(N,H) 중 하나를 포함할 수 있다.

- [0025] 본 발명의 상호연결 구조체의 다른 실시예에서, 다공성 또는 비다공성일 수 있는 유전 물질은 SiO_2 , 실세스퀴옥산, Si, C, O 및 H의 원자들을 포함하는 C 도핑된 산화물 및 열경화성 폴리아릴렌 에테르 중 하나를 포함할 수 있다.
- [0026] 바람직한 상호연결 구조체의 또 다른 실시예에서, 본 발명의 상호연결 구조체 내의 U-형 확산 장벽은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W 또는 WN을 포함할 수 있다.
- [0027] 바람직한 상호연결 구조체의 또 다른 실시예에서, U-형 도금 시드층이 또한 제공되며 U-형 도금 시드층은 도전 물질과 U-형 확산 장벽 사이에 위치한다. 이 경우에, 절연층 또는 금속층의 에지 부분들은 U-형 도금 시드층의 상부 측벽 표면과 직접적으로 접한다. U-형 도금 시드층은 구리 함유 도전 물질이 도금 프로세스에 의해 형성될 때 사용된다. U-형 도금 시드층이 존재할 때, U-형 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru 또는 Ru 합금을 포함할 수 있다.
- [0028] 전술한 상호연결 구조체와 더불어, 본 발명은 또한 상호연결 구조체의 제조 방법도 제공한다.
- [0029] 본 방법은,
- [0030] 약 4.0 이하의 유전 상수를 갖는 유전 물질 내로 적어도 하나의 개구를 형성하는 단계(유전 물질은 유전 물질의 상부 표면 상에 위치하는 패터닝된 하드 마스크를 가짐);
- [0031] 적어도 하나의 개구와 패터닝된 하드 마스크를 확산 장벽으로 라이닝하는 단계;
- [0032] 적어도 하나의 개구를 도전 물질로 부분적으로 채우는 단계(도전 물질은 유전 물질 상부 표면 아래에 위치하는 상부 표면을 가짐);
- [0033] 적어도 하나의 개구 내와 도전 물질의 상부 표면 상뿐만 아니라 패터닝된 하드 마스크를 라이닝하는 확산 장벽의 위에 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질을 형성하는 단계; 및
- [0034] 유전 물질의 상부 표면 위에 위치하는 패터닝된 하드 마스크와 확산 장벽 및 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 일부분을 제거하는 반면에, 적어도 하나의 개구 내에 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 또 다른 부분을 유지하고, 적어도 하나의 개구 내에 U-형 확산 장벽을 형성하는 단계를 포함하고,
- [0035] 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 또 다른 부분은 유전 물질의 상부 표면과 동일 평면 상의 상부 표면을 갖고, 도전 물질은 도전 물질의 측벽 표면들 및 바닥 표면 상에 위치한 U-형 확산 장벽에 의해 완전히 둘러싸이며, 확산 장벽 속성을 갖는 유전 물질의 또 다른 부분은 도전 물질의 상부 표면 상에 위치한다.
- [0036] 본 방법의 일 실시예에서, 유전 캐핑층이 유전 물질의 상부 표면 및 적어도 하나의 개구에 남아 있는 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 또 다른 부분의 상부 표면 상에 형성된다. 유전 캐핑층이 존재할 때, 유전 캐핑층은 SiC, Si_3N_4 , SiO_2 , 탄소 도핑된 산화물 및 질소와 수소가 도핑된 탄화 규소 SiC(N,H) 중 하나를 포함할 수 있다.
- [0037] 본 방법의 또 다른 실시예에서, 확산 장벽은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W 또는 WN을 포함할 수 있고, 화학 기상 피착, 플라즈마 강화 화학 기상 피착, 원자층 피착, 물리 기상 피착, 스퍼터링, 화학 용액 피착 및 도금에 의해 형성된다.
- [0038] 본 방법의 또 다른 실시예에서, 도금 시드층이 도전 물질과 확산 장벽 사이에 형성되고, 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru 또는 Ru 합금을 포함할 수 있다. 실시예에서, 도금 시드층이 사용되며, 도금 시드층은 화학 기상 피착, 플라즈마 강화 화학 기상 피착, 원자층 피착 또는 물리 기상 피착에 의해 형성된다.
- [0039] 본 방법의 다른 실시예에서, 도전 물질은 순수형 또는 합금형의 Cu, W 또는 Al을 포함할 수 있다.
- [0040] 본 방법의 또 다른 실시예에서, 적어도 하나의 개구를 도전 물질로 부분적으로 채우는 단계는 화학 기상 피착, 스퍼터링, 화학 용액 피착 및 도금으로부터 선택된 피착 프로세스를 포함한다.
- [0041] 본 발명의 또 다른 실시예에서, 적어도 하나의 개구를 도전 물질로 부분적으로 채우는 단계는 적어도 하나의 개구를 도전 물질 및 리세싱으로 완전히 채우는 것을 포함한다.
- [0042] 본 방법의 또 다른 실시예에서, 제거하는 단계는 화학 기계적 폴리싱을 포함한다.

도면의 간단한 설명

- [0043] 본 발명의 실시예는 첨부된 도면을 참조하여 오직 예시적인 방법으로 기술된다.
- 도 1a-1b는 (단면도를 통해) 선행기술의 상호연결 구조체를 도시하는 도식적 도면. 도 1a는 Cu 누설을 도시하며, 도 1b는 Cu 잔류물을 도시함.
- 도 2a-2g는 (단면도를 통해) 높은 누설 저항을 가지며 유전 물질의 표면에서 금속성 잔류물이 존재하지 않는 매우 신뢰성 있고 기술적으로 확장가능한 상호연결 구조체를 제조하는 본 발명에 사용되는 기본 프로세스 단계를 도시하는 도식적 도면.
- 발명을 실시하기 위한 구체적인 내용*
- [0044] 높은 누설 저항을 갖고 유전 물질의 표면에 존재하는 금속성 잔류물이 없는 상호연결 구조체 및 상호연결 구조체를 제조하는 방법을 제공하는 본 발명은 본 출원에 첨부되는 다음의 설명 및 도면을 참조함으로써 더 자세히 기술될 것이다. 본 출원의 도면은 오직 예시적인 목적을 위해 제공되며, 도면은 축척에 맞게 도시되지 않았음을 주의해야 한다.
- [0045] 다음의 설명에서, 특정 구조, 컴포넌트, 물질, 치수, 프로세스 단계 및 기술과 같은 수많은 구체적인 세부사항이 본 발명의 전체적인 이해를 제공하기 위해 제공된다. 그러나, 본 발명은 이러한 구체적인 세부사항 없이 실시될 수 있다는 것이 본 기술분야의 당업자에게 명백할 것이다. 또 다른 예에서, 잘 알려진 구조 또는 프로세스 단계는 본 발명을 모호하게 만드는 것을 피하기 위해 상세히 기술되지 않는다.
- [0046] 층, 영역 또는 기관과 같은 요소가 또 다른 요소 "상에" 또는 "위에" 위치한다고 지칭될 때, 다른 요소 바로 위에 있을 수 있거나, 또는 개입 요소가 또한 존재할 수 있다. 반대로, 요소가 또 다른 요소 "바로 위" 또는 "바로 상부에" 위치한다고 지칭될 때, 개입 요소는 존재하지 않는다. 요소가 또 다른 요소에 "연결된다" 또는 "결합된다"고 지칭될 때, 다른 요소에 직접 연결되거나 결합될 수 있거나, 또는 개입 요소가 존재할 수 있다. 반대로, 요소가 또 다른 요소에 "직접 연결된다" 또는 "직접 결합된다"고 지칭될 때, 개입 요소는 존재하지 않는다.
- [0047] 전술한 바와 같이, 본 발명은 높은 누설 저항을 갖고 유전 물질의 표면에 존재하는 금속성 잔류물이 없는 상호연결 구조체 및 상호연결 구조체를 제조하는 방법을 제공한다. 본 발명의 상호연결 구조체는 선행 기술 발명의 구조체보다 개선된 TDDb를 나타낸다.
- [0048] 본 발명의 상호연결 구조체에서, 도전성 피처(즉, 도전 물질)는 유전 물질의 상부 표면과 동일 평면에 있지 않지만, 대신에 도전 물질은 유전 물질의 상부 표면 아래에 리세스된다. 유전 물질의 상부 표면 아래에 리세스될 뿐만 아니라, 본 발명의 상호연결 구조체의 도전 물질은 모든 면(예를 들어, 측벽 표면, 상부 표면, 및 바닥 표면)이 확산 장벽 물질에 의해 둘러싸여진다. 개구 내의 리세스된 도전 물질의 측벽 표면 및 바닥 표면이 U-형 확산 장벽으로 라이닝된다. 리세스된 도전 물질의 상부 표면은 절연층 또는 금속층으로 라이닝되고, 이들 모두는 확산 장벽 속성을 갖는다. 도전 물질의 상부 표면을 라이닝하는 절연층 또는 금속층의 에지 부분은 U-형 확산 장벽의 상부 측벽 표면, 또는 U-형 도금 시드층이 존재한다면 선택적인 U-형 도금 시드층과 접한다.
- [0049] 본 출원에서 리세스된 도전 물질과 유전 물질 사이에 직접적인 접촉이 없고, 선행 기술 상호연결 구조체에서의 경우와 같이 이러한 도전성 잔류물이 상호연결 구조체의 상부 표면에 형성되지 않으므로 상호연결 유전체의 표면 상에서 연장되는 도전 물질의 연마(planarization)는 사용되지 않는다는 것을 또한 유의해야 한다. 상기 태양은 유전체 표면 상의 도전성 금속 잔류물(예를 들어, 결합)을 감소시키는 데 현저한 효과를 가진다.
- [0050] 도 2a-2g를 참조하면, 도 2a-2g는 본 발명의 반도체 상호연결 구조체를 형성하는 데 사용되는 기본 프로세스 단계를 도시한다. 도 2a는 유전 물질(52) 및 유전 물질(52)의 표면 상에 위치하는 하드 마스크(54)를 포함하는 초기 구조체(50)를 도시한다.
- [0051] 초기 구조체(50), 즉, 유전 물질(52)은 (본 출원의 도면에 도시되지 않은) 기관 상에 위치할 수 있다. 도시되지 않은 기관은 반도체 물질, 절연 물질, 도전 물질 또는 이들의 임의의 조합을 포함할 수 있다. 기관이 반도체 물질로 구성될 때, Si, SiGe, SiGeC, SiC, Ge 합금, GaAs, InAs, InP 및 다른 III/V 또는 II/VI 화합물 반도체와 같은 임의의 반도체가 사용될 수 있다. 이러한 나열된 유형의 반도체 물질뿐만 아니라, 본 발명은 또한 반도체 기관이, 예를 들어 Si/SiGe, Si/SiC, SOI(silicon-on-insulator) 또는 SGOI(silicon germanium-on-insulator)와 같은 계층화된 반도체인 경우도 고려한다.
- [0052] 기관이 절연 물질일 때, 절연 물질은 유기 절연체, 무기 절연체 또는 복수층을 포함하는 이들의 조합일 수

있다. 기판이 도전 물질일 때, 기판은 예를 들어 다결정 규소(PolySi), 원소 금속(elemental metal), 원소 금속의 합금, 금속 규화물, 금속 질화물 또는 복수층을 포함하는 이들의 조합을 포함할 수 있다. 기판이 반도체 물질을 포함할 때, 예를 들어 CMOS(complementary metal oxide semiconductor) 장치와 같은 하나 이상의 반도체 장치가 그 위에 제조될 수 있다. 기판이 절연 물질 및 도전 물질의 조합을 포함할 때, 기판은 다층 상호연결 구조체(multilayered interconnect structure)의 제1 상호연결 레벨을 나타낼 수 있다.

[0053] 유전 물질(52)은 무기 유전체 또는 유기 유전체를 포함하는 임의의 인터레벨(interlevel) 또는 인트라레벨(intralevel) 유전체를 포함한다. 유전 물질(52)은 다공성이거나 비-다공성일 수 있다. 유전 물질(52)로서 사용될 수 있는 적절한 유전체의 소정의 예는 SiO_2 , 실세스퀴옥산, Si, C, O 및 H의 원자를 포함하는 C 도핑된 산화물(즉, 올가노실리케이트(organosilicates)), 열경화성 폴리아릴렌 에테르 또는 그들의 복수층을 포함하지만, 이에 한정되는 것은 아니다. "폴리아릴렌"이라는 용어는 본 출원에서 결합(bonds), 축합 고리(fused ring) 또는 예를 들어, 산소, 유황, 술폰(sulfone), 술폭시화물(sulfoxide), 카르보닐기(carbonyl) 등과 같은 비활성 결합 그룹(inert linking groups)에 의해 함께 결합된 아릴 잔기(aryl moieties) 또는 비활성 대체 아릴 잔기(inertly substitute aryl moieties)를 표현하기 위해 사용된다.

[0054] 유전 물질(52)은 일반적으로 약 4.0 이하의 유전 상수를 가지며, 유전 상수는 약 2.8 이하인 것이 더 일반적이다. 본 명세서에 언급된 모든 유전 상수는 특별히 다르게 언급되지 않는 한 진공에 관한 수치이다. 이러한 유전체들은 4.0 보다 더 높은 유전 상수를 가지는 유전 물질과 비교할 때 일반적으로 더 낮은 기생 크로스 토크(parasitic cross talk)를 가진다. 유전 물질(52)의 두께는 사용되는 유전 물질뿐만 아니라 유전 물질(52) 내의 유전층의 정확한 개수에 따라 변할 수 있다. 일반적으로, 일반적인 상호연결 구조체에 대하여, 유전 물질(52)은 약 50nm에서 약 1000nm의 두께를 가진다.

[0055] 전술한 바와 같이, 초기 구조체(50)는 또한 유전 물질(52)의 상부 표면 상에 위치한 하드 마스크(54)를 포함한다. 하드 마스크(54)는 산화물, 질화물, 산화질화물 또는 이들의 임의의 다층 조합을 포함한다. 일 실시예에서, 하드 마스크(54)는 이산화 규소(silicon dioxide)와 같은 산화물인 반면, 또 다른 실시예에서 하드 마스크(54)는 질화 규소와 같은 질화물이다.

[0056] 하드 마스크(54)는 예를 들어, 화학 기상 피착(Chemical Vapor Deposition; CVD), 플라즈마 강화 화학 기상 피착(Plasma Enhanced Chemical Vapor Deposition; PECVD), 화학 용액 피착(chemical solution deposition), 증착(evaporation) 및 물리 기상 피착(Physical Vapor Deposition; PVD)을 포함하는 종래의 피착 프로세스를 사용하여 형성된다. 대안적으로, 하드 마스크(54)는 열산화(thermal oxidation) 및 열질화(thermal nitridation) 중 하나에 의해 형성될 수 있다.

[0057] 본 발명에 사용되는 하드 마스크(54)의 두께는 하드 마스크 자체의 물질뿐만 아니라 이를 형성하는데 사용되는 기술에 따라 변할 수 있다. 일반적으로, 하드 마스크(54)는 약 5nm에서 약 100nm의 두께를 가지며, 약 10nm에서 약 80nm의 두께가 더 일반적이다.

[0058] 다음으로, 도 2b에 도시된 바와 같이, 적어도 하나의 개구(56)가 리소그래피 및 에칭을 사용하여 하드 마스크(54)와 유전 물질(52) 내로 형성된다. 리소그래피 프로세스는 하드 마스크(54) 위에 포토레지스트(photoresist)(도시되지 않음)를 형성하는 단계, 포토레지스트를 원하는 패턴의 방식에 노출하는 단계 및 종래의 레지스트 현상액(resist developer)을 사용하여 노출된 포토레지스트를 현상하는 단계를 포함한다. 에칭 프로세스는 드라이 에칭 프로세스(예를 들어, 반응성 이온 에칭(reactive ion etching), 이온 빔 에칭(ion beam etching), 플라즈마 에칭 또는 레이저 어블레이션(laser ablation)) 및/또는 습식 화학 에칭 프로세스(wet chemical etching process)를 포함한다. 일반적으로, 반응성 이온 에칭은 적어도 하나의 개구(56)를 제공하는 데 사용된다. 일반적으로, 에칭 프로세스는 포토레지스트에 제공되는 패턴이 하드 마스크(54)로 전사(transferred)되는 제1 패턴 전사 단계(first pattern transfer step)를 포함하며, 패턴링된 포토레지스트는 이후에 애싱(ashing) 단계에 의해 제거되며, 그 다음에 제2 패턴 전사 단계가 패턴링된 하드 마스크로부터의 패턴을 아래의 유전 물질 내로 전사하기 위해 사용된다.

[0059] 유전 물질(54) 내로 형성된 적어도 하나의 개구(56)의 깊이(유전 물질의 상부 표면에서부터 개구의 바닥 벽까지 측정됨)는 변할 수 있으며 본 출원에 있어서 중요하지 않다. 일부 실시예에서, 적어도 하나의 개구(56)는 유전 물질을 완전히 통과해서 연장될 수 있다. 또 다른 실시예에서, 적어도 하나의 개구(56)는 유전 물질(52) 자체 내에서 멈춘다. 또 다른 실시예에서, 상이한 깊이의 개구가 형성될 수 있다.

[0060] 적어도 하나의 개구(56)는 비아 개구(via opening), 선 개구(line opening) 및/또는 결합된 비아/선 개구

(combined via/line opening)일 수 있다. 도 2b에서, 예를 들어 각각의 개구는 선 개구로서 도시된다.

- [0061] 다음으로, 도 2c에서 도시된 바와 같이, 확산 장벽(58)은 그 안에 적어도 하나의 개구를 포함하는 도 2b에 도시된 구조체의 모든 노출된 표면 상에서 (즉, 각각의 개구의 측벽 및 바닥 벽 상에서) 남아있는 하드 마스크(54)의 상부 표면을 따라 형성된다.
- [0062] 확산 장벽(58)은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W, WN 또는 도전 물질이 그곳을 통과하여 확산되는 것을 방지하는 장벽으로서 기능할 수 있는 임의의 다른 물질을 포함한다. 확산 장벽(58)의 두께는 사용되는 피착 프로세스뿐만 아니라 사용되는 물질에 따라 변할 수 있다. 일반적으로, 확산 장벽(58)은 약 2nm에서 약 50nm의 두께를 가지며, 약 5nm에서 약 20nm의 두께가 더 일반적이다.
- [0063] 확산 장벽(58)은 예를 들어, 화학 기상 피착(CVD), 플라즈마 강화 화학 기상 피착(PECVD), 원자층 피착(ALD), 물리 기상 피착(PVD), 스퍼터링, 화학 용액 피착 및 도금을 포함하는 피착 프로세스에 의해 형성된다.
- [0064] 일부 실시예에 있어서, 선택적인 도금 시드층(도 2c 내에 구체적으로 도시되지 않음)은 확산 장벽(58)의 표면 상에서 형성될 수 있다. 확산 장벽(58) 상에서 연속적이고 직접적으로 형성되는 도전 물질의 경우에 있어서는, 선택적인 도금 시드층이 필요하지 않다. 선택적인 도금 시드층은 사전 선택된 도전 금속 또는 금속 합금의 연속적인 전기 도금(electroplating)을 선택적으로 촉진하기 위해 사용된다. 선택적인 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru, Ru 합금(예를 들어, TaRu 합금) 또는 낮은 금속 도금 과전압(overpotential)을 가지는 임의의 다른 적절한 귀금속(noble metal) 또는 귀금속 합금을 포함할 수 있다. Cu 금속이 개구(56) 내에서 연속적으로 형성되는 경우, 일반적으로 Cu 또는 Cu 합금 도금 시드층이 사용된다.
- [0065] 선택적인 시드층의 두께는 선택적인 도금 시드층의 물질뿐만 아니라 이를 형성하는데 사용되는 기술에 따라 변할 수 있다. 일반적으로, 선택적인 도금 시드층은 약 2nm에서 약 80nm의 두께를 가진다.
- [0066] 선택적인 도금 시드층은, 예를 들어 CVD, PECVD, ALD 및 PVD를 포함하는 종래의 피착 프로세스에 의해 형성될 수 있다.
- [0067] (유전 물질(52) 내에서 도전 피처를 형성하는) 도전 물질(60)은, 예를 들어 도 2d에 도시된 구조체를 제공하는 적어도 확산 장벽으로 라이닝된 적어도 하나의 개구(56) 내에서 부분적으로 형성된다. 부분적으로 형성된 구조체를 생성하기 위해 시간 제어 프로세스가 수행된다. 도전 물질(60)은 다결정 규소, SiGe, 도전 금속, 적어도 하나의 도전 금속을 포함하는 합금, 도전 금속 규화물 또는 이들의 조합을 포함할 수 있다. 바람직하게는, 도전 물질(60)은 Cu, W, 또는 Al과 같은 도전 금속이며, Cu 또는 Cu 합금(예를 들어, AlCu)이 본 발명에 있어 보다 바람직하다.
- [0068] 도전 물질(60)은 적어도 하나의 개구(56)를 부분적으로 채우거나 또는 적어도 하나의 개구(56)를 전체적으로 채운 후, 도전 물질(60)을 유전 물질(52)의 상부 표면 아래 레벨로 리세싱함으로써 형성될 수 있다. 화학 기상 피착(CVD), 플라즈마 강화 화학 기상 피착(PECVD), 스퍼터링, 화학 용액 피착 또는 도금을 포함하는, 적어도 하나의 개구를 바닥에서부터 위로 채우는 임의의 종래의 피착 프로세스가 사용될 수 있다. 바람직하게는, 상향식(bottom-up) 도금 프로세스가 사용된다.
- [0069] 리세싱 단계가 사용되는 경우, 도전 물질(60)의 부분을 선택적으로 제거하는 에칭 프로세스가 유전 물질(52) 내의 적어도 하나의 개구(56)를 부분적으로 채우기 위해 사용된다.
- [0070] 다음으로, 연마 정지층(planarization stop layer; 62)이 적어도 하나의 개구(56)의 남은 부분 내에서뿐만 아니라, 적어도 하나의 개구(56)의 외부로 연장되는 확산 장벽(58)(또는 선택적인 금속 시드층)의 위에서 형성된다. 연마 정지층(62)을 포함하는 결과 구조체(resultant structure)가, 예를 들어 도 2e에 도시된다. 연마 정지층(62)은, 예를 들어 탄화 규소, 질화 규소 및/또는 질소와 수소 도핑된 탄화규소와 같은 임의의 절연 물질 또는, 예를 들어 확산 장벽 속성을 갖는 순수형, 합금형 또는 질화형 Ta, Ru, Ir, W, Co, Ti 및/또는 Rh와 같은 임의의 금속 물질을 포함한다. 이와 같이, 연마 정지층(62)은 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질로서 지칭될 수 있다.
- [0071] 연마 정지층(62)은, 이에 한정되는 것은 아니지만 CVD, PECVD, 증착, 화학 용액 피착, 스퍼터링 및 물리 기상 피착(PVD)을 포함하는 종래의 피착 프로세스에 의해 형성된다.
- [0072] 다음으로, 도 2f에 도시된 바와 같이, 예를 들어 화학 기계적 연마(chemical mechanical polishing; CMP) 및/또는 그라인딩(grinding)과 같은 연마 프로세스는 적어도 하나의 개구(56)의 입구 위로 연장되는 연마 정지층(62)의 부분을 제거하는데 사용된다. 연마 단계 동안, 확산 장벽 및 하드 마스크는 유전 물질(52)의 상부, 수

평 표면의 위로부터 제거된다. 이와 같이, 연마 프로세스는 (측벽 표면 및 바닥 표면 상의) U-형 확산 장벽과, 본 발명의 이 단계 동안 제거되지 않는 연마 정치층(62')의 나머지 부분에 의해 완벽하게 둘러싸인 도전 물질(60)을 제공한다. 연마 장벽의 나머지 부분은 적어도 하나의 개구 내에 위치하며, 유전 물질(52)의 상부 표면과 동일 평면 상의 상부 표면을 가진다.

[0073] 도 2f는 본 발명의 상호연결체를 도시한다. 도시된 바와 같이, 본 발명의 상호연결 구조체는 약 4.0 이하의 유전 상수를 갖는 유전 물질(52); 및 유전 물질(52) 내에 매립되는 측벽 표면들(60X), 바닥 표면(60Y) 및 상부 표면(60Z)을 갖는 도전 물질(60)을 포함하고, 도전 물질(60)의 상부 표면(60Z)은 유전 물질(52)의 상부 표면(52U) 아래에 위치한다. 본 발명의 상호연결 구조체는 또한 도전 물질(60)의 측벽 표면들(60X) 및 바닥 표면(60Y) 상에 위치하는 적어도 하나의 U-형 확산 장벽(58)을 포함한다. 본 발명의 상호연결 구조체는 또한 도전 물질(60)의 상부 표면(60Z) 상에 위치하는 확산 장벽 속성(62')을 가지는 절연층 또는 금속층을 포함하며, 이러한 절연층 또는 금속층은 적어도 U-형 장벽의 상부 측벽 표면들과 접하는 에지 부분들(E)을 갖는, 확산 장벽 속성(62')을 갖는다.

[0074] 도 2g는 유전 캐핑층(64)이 도 2f에 도시된 구조체의 노출된 표면 상에서 형성되는 선택적인 실시예를 도시한다. 유전 캐핑층(64)은, 예를 들어, SiC, Si₃N₄, SiO₂, 탄소 도핑된 산화물, 질소와 수소 도핑된 탄화규소 SiC(N,H) 또는 이들의 복수층과 같은 임의의 적절한 유전 캐핑 물질을 포함한다. 예를 들어, 화학 기상 피착, 플라즈마 강화 화학 기상 피착, 화학 용액 피착, 증착 및 원자층 피착과 같은 임의의 종래의 피착 프로세스가 선택적인 유전 캐핑층(64)을 형성하는데 사용될 수 있다. 유전 캐핑층(64)의 두께는 이를 형성하는데 사용되는 기술뿐만 아니라 층의 구성 물질에 따라 변할 수 있다. 일반적으로, 유전 캐핑층(64)은 약 15nm에서 약 100nm의 두께를 가지며, 약 25nm에서 약 45nm의 두께가 더 일반적이다.

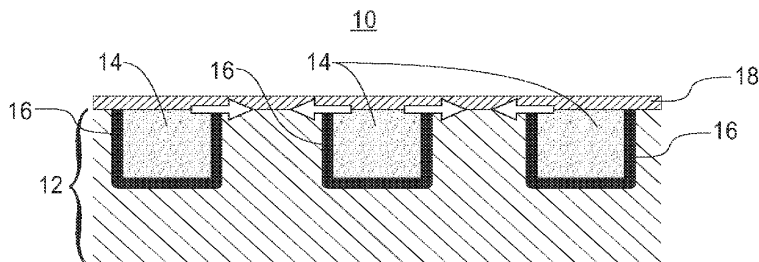
[0075] 본 발명의 방법 동안, 도전 물질(60)과 유전 물질(52) 간에 직접적인 접촉은 없으며, 유전체의 표면 상에서 연장되는 도전 물질의 연마가 사용되지 않으므로, 도전성 잔류물이 형성되지 않는다. 상기 태양은 유전체 표면 상에 도전성 금속 잔여물(예를 들어, 결함)을 감소시키는데 현저한 효과를 가진다. 따라서, 본 발명의 방법은 대량으로 제조될 수 있는 신뢰성 있고 기술적으로 확장가능한 상호연결 구조체를 제공한다.

[0076] 본 발명이 바람직한 실시예에 대해 구체적으로 도시되고 기술되었으나, 본 기술 분야의 당업자는 형태 및 세부 사항에 대해 전술한 것의 변형 및 다른 변형이 본 발명의 사상과 범위를 벗어나지 않고 이루어질 수 있다는 것을 이해할 수 있다. 따라서, 본 발명은 기술되고 도시된 정확한 형태 및 세부사항에 한정되지 않으며 첨부된 특허청구범위의 범위 안에 포함된다.

도면

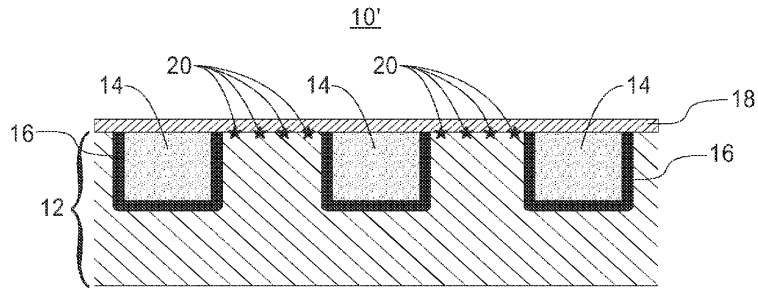
도면1a

(종래 기술)

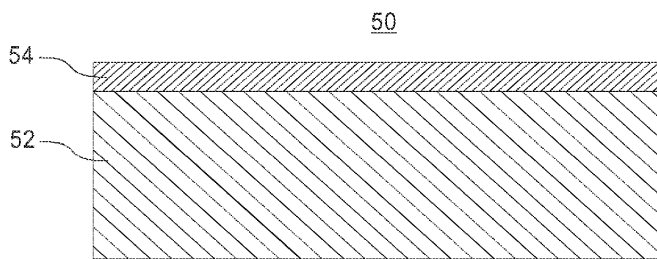


도면 1b

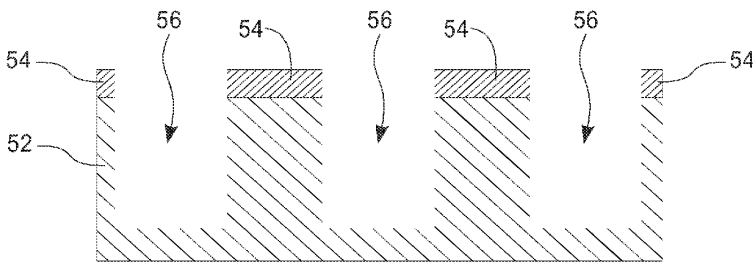
(종래 기술)



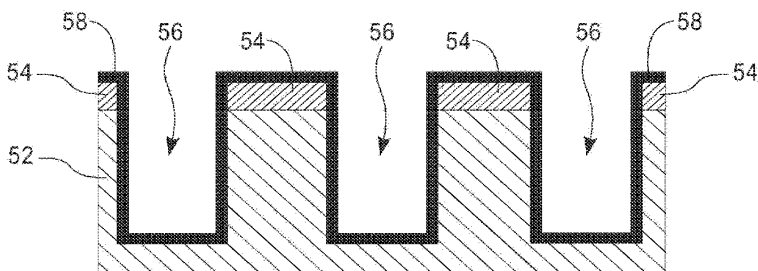
도면 2a



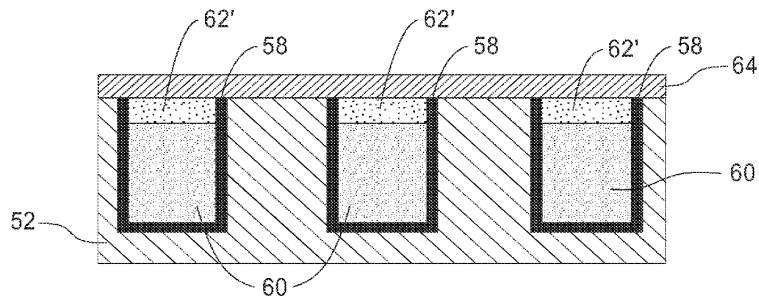
도면 2b



도면 2c



도 2g





Unexamined Patent Publication(A)

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Agent.	CHANG, Soo Kil YANG, Young June
Inventor	YANG, Chih-Chao NITTA, Satyanarayana, Venkata
Applicant	INTERNATIONAL BUSINESS MACHINES CORPORATION.

발명의 명칭

높은 누설 저항을 갖는 상호연결 구조체

Title of Invention

The mutual linking structure having the high leak resistance.

요약

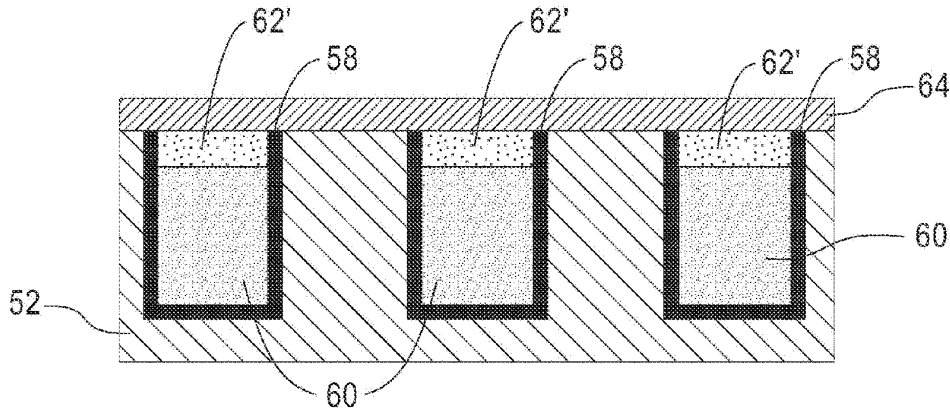
도전성 피쳐(즉, 도전 물질)가 유전 물질의 상부 표면과 동일 평면이 아니고, 대신에 도전 물질이 유전 물질의 상부 표면 아래에 리세스되는 상호연결 구조체가 제공된다. 유전 물질의 상부 표면 아래에 리세스되는 것뿐만 아니라, 본 발명에 따른 상호연결 구조체의 도전 물질은 모든 표면(즉, 측벽 표면들, 상부 표면 및 바닥 표면)이 확산 장벽 물질에 의해 둘러싸인다. 종래 기술의 상호연결 구조체들과는 달리, 리세스된 도전 물질의 상부 표면 위에 위치하는 장벽 물질은 리세스된 도전 물질을 포함하는 개구와 함께 위치한다.

Abstract

It is not conducting feature (in other words, the conducting material) the same plane as the top surface of the dielectric material and the mutual linking structure in which the conducting material is instead of recessed under the top surface of the dielectric material is provided. The conducting material of the mutual linking structure according to the present invention all surface (in other words, the side wall surface the top surface and bottom surface) are surrounded with under barrier metal it is recessed under the top surface of the dielectric material. It is positioned with the opening including the conducting material in which the barrier material positioned on the top surface of the conducting material

recessed to the mutual linking structures of the prior art is recessed.

대표도면(Representative drawing)



청구의 범위

청구 1항:

대략 4.0 이하의 유전 상수를 갖는 유전 물질;

상기 유전 물질 내에 매립(embedded)되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 도전 물질 - 상기 도전 물질의 상기 상부 표면은 상기 유전 물질의 상부 표면 아래에 위치함 - ;

상기 도전 물질의 상기 측벽 표면들 및 상기 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽(U-shaped diffusion barrier); 및

상기 도전 물질의 상기 상부 표면 상에 위치하고, 적어도 상기 U-형 장벽의 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성(diffusion barrier properties)을 갖는 절연층 또는 금속층

을 포함하는, 상호연결 구조체.

청구 1항:

Scope of Claims

Claim 1:

Approximately, the mutual linking structure which comprises side wall surfaces that become within the dielectric material :

dielectric material having the dielectric constant less than 4.0 with the padding (embedded), the bottom surface, and the insulating layer or the metallic layer

having the diffusion barrier attribute (diffusion barrier properties) which has edge areas contacting with upper sidewall surfaces of at least U- type obstacle it is located on surface the top surface of the conducting material and at least one U- type diffusion barrier (U-shaped diffusion barrier) :

located on surface side wall surfaces and bottom surface of - :

conducting material the top surface of the conducting material - conducting material having the top surface is positioned under the top surface of the dielectric material.

Claim 1:

대략 4.0 이하의 유전 상수를 갖는 유전 물질;

상기 유전 물질 내에 매립(embedded)되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 도전 물질 - 상기 도전 물질의 상기 상부 표면은 상기 유전 물질의 상부 표면 아래에 위치함 - ;

상기 도전 물질의 상기 측벽 표면들 및 상기 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽(U-shaped diffusion barrier); 및

상기 도전 물질의 상기 상부 표면 상에 위치하고, 적어도 상기 U-형 장벽의 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성(diffusion barrier properties)을 갖는 절연층 또는 금속층

을 포함하는, 상호연결 구조체.

Approximately, the mutual linking structure which comprises side wall surfaces that become within the dielectric material :

dielectric material having the dielectric constant less than 4.0 with the padding (embedded), the bottom surface, and the insulating layer or the metallic layer

having the diffusion barrier attribute (diffusion barrier properties) which has edge areas contacting with upper sidewall surfaces of at least U- type obstacle it is located on surface the top surface of the conducting material and at least one U- type diffusion barrier (U-shaped diffusion barrier) :

located on surface side wall surfaces and bottom surface of - :

conducting material the top surface of the conducting material - conducting material having the top surface is positioned under the top surface of the dielectric material.

청구 2항:

제1항에 있어서,

상기 유전 물질의 상기 상부 표면 및 확산 장벽 속성을 갖는 상기 절연층 또는 금속층의 상부 표면 상에 위치하는 유전 캐핑층(dielectric capping layer)을 더 포함하는, 상호연결 구조체.

청구 2항:

제1항에 있어서,

상기 유전 물질의 상기 상부 표면 및 확산 장벽 속성을 갖는 상기 절연층 또는 금속층의 상부 표면 상에 위치하는 유전 캐핑층(dielectric capping layer)을 더 포함하는, 상호연결 구조체.

청구 3항:

제2항에 있어서,

Claim 2:

As for claim 1, the mutual linking structure which further includes the heredity capping layer (dielectric capping layer) located on surface the top surface of the insulating layer having the top surface and diffusion barrier attribute of

dielectric material or the metallic layer.

Claim 2:

As for claim 1, the mutual linking structure which further includes the heredity capping layer (dielectric capping layer) located on surface the top surface of the insulating layer having the top surface and diffusion barrier attribute of

dielectric material or the metallic layer.

Claim 3:

The mutual linking structure of claim 2, w herein

상기 유전 캐핑층은 SiC, Si₄NH₃, SiO₂, 탄소 도핑된 산화물 및 질소와 수소 도핑된 탄화 규소 SiC(N,H) 중 하나를 포함하는, 상호연결 구조체.

청구 3항:

제2항에 있어서,

상기 유전 캐핑층은 SiC, Si₄NH₃, SiO₂, 탄소 도핑된 산화물 및 질소와 수소 도핑된 탄화 규소 SiC(N,H) 중 하나를 포함하는, 상호연결 구조체.

청구 4항:

제1항 내지 제3항 중 어느 한 항에 있어서,

상기 유전 물질은 SiO₂, 실세스퀴옥산(silsesquioxane), Si, C, O 및 H의 원자들을 포함하는 C 도핑된 산화물 및 열경화성 폴리아릴렌 에테르(thermosetting polyarylene ether) 중의 하나를 포함하는, 상호연결 구조체.

청구 4항:

제1항 내지 제3항 중 어느 한 항에 있어서,

상기 유전 물질은 SiO₂, 실세스퀴옥산(silsesquioxane), Si, C, O 및 H의 원자들을 포함하는 C 도핑된 산화물 및 열경화성 폴리아릴렌 에테르(thermosetting polyarylene ether) 중의 하나를 포함하는, 상호연결 구조체.

청구 5항:

제1항 내지 제4항 중 어느 한 항에 있어서,

상기 U-형 확산 장벽은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa₂N, W 또는 WN을 포함하는, 상호연결 구조체.

청구 5항:

heredity capping layer comprises the SiC, the Si₄NH₃, the SiO₂, and the oxide which is carbon doped and one among the A-doped silicon carbide SiC (N,H) nitrogen and hydrogen.

Claim 3:

The mutual linking structure of claim 2, wherein

heredity capping layer comprises the SiC, the Si₄NH₃, the SiO₂, and the oxide which is carbon doped and one among the A-doped silicon carbide SiC (N,H) nitrogen and hydrogen.

Claim 4:

As for any one of claim 1 through claim 3, the mutual linking structure including one of oxide and the A-doped thermosetting property polyarylene ether (thermosetting polyarylene ether) Cs wherein

dielectric material includes the atoms of H and SiO₂, the silsesquioxane, the Si, C, O.

Claim 4:

As for any one of claim 1 through claim 3, the mutual linking structure including one of oxide and the A-doped thermosetting property polyarylene ether (thermosetting polyarylene ether) Cs wherein

dielectric material includes the atoms of H and SiO₂, the silsesquioxane, the Si, C, O.

Claim 5:

As for any one of claim 1 through claim 4, the mutual linking structure wherein

U-type diffusion barrier includes the Ta, the TaN, the Ti, the TiN, the Ru, the RuN, the RuTa, the RuTa₂N, W or WN.

Claim 5:

제1항 내지 제4항 중 어느 한 항에 있어서,

상기 U-형 확산 장벽은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa_N, W 또는 WN을 포함하는, 상호연결 구조체.

청구 6항:

제1항 내지 제5항 중 어느 한 항에 있어서,

상기 도전 물질과 상기 U-형 확산 장벽 사이에 위치하는 U-형 도금 시드층을 더 포함하고, 상기 U-형 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru 또는 Ru 합금을 포함하는, 상호연결 구조체.

청구 6항:

제1항 내지 제5항 중 어느 한 항에 있어서,

상기 도전 물질과 상기 U-형 확산 장벽 사이에 위치하는 U-형 도금 시드층을 더 포함하고, 상기 U-형 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru 또는 Ru 합금을 포함하는, 상호연결 구조체.

청구 7항:

제1항 내지 제6항 중 어느 한 항에 있어서,

상기 도전 물질은 순수형 또는 합금형 Cu, W 또는 Al을 포함하는, 상호연결 구조체.

청구 7항:

제1항 내지 제6항 중 어느 한 항에 있어서,

상기 도전 물질은 순수형 또는 합금형 Cu, W 또는 Al을 포함하는, 상호연결 구조체.

청구 8항:

제1항 내지 제7항 중 어느 한 항에 있어서,

확산 장벽 속성을 갖는 상기 절연층 또는 금속층은 탄화 규소, 질화 규소, 질소와 수소 도핑

As for any one of claim 1 through claim 4, the mutual linking structure wherein

U- type diffusion barrier includes the Ta, the TaN, the Ti, the TiN, the Ru, the RuN, the RuTa, the RuTa_N, W or WN.

Claim 6:

As for any one of claim 1 through claim 5, the mutual linking structure wherein the U- type plated seed layer the U- type plated seed layer positioned between

conducting material and U- type diffusion barrier further is included includes the Cu, the Cu alloy, the Ir, the Ir alloy, the Ru or the Ru alloy.

Claim 6:

As for any one of claim 1 through claim 5, the mutual linking structure wherein the U- type plated seed layer the U- type plated seed layer positioned between

conducting material and U- type diffusion barrier further is included includes the Cu, the Cu alloy, the Ir, the Ir alloy, the Ru or the Ru alloy.

Claim 7:

As for any one of claim 1 through claim 6, the mutual linking structure wherein

conducting material includes the pure form or the alloy type Cu, and W or the Al.

Claim 7:

As for any one of claim 1 through claim 6, the mutual linking structure wherein

conducting material includes the pure form or the alloy type Cu, and W or the Al.

Claim 8:

As for any one of claim 1 through claim 7, the mutual linking structure wherein the insulating layer or the metallic layer having

된 탄화규소 및 순수형, 합금형 또는 질화형 Ta, Ru, Ir, W, Co, Ti 및 Rh로부터 선택되는 금속 물질 중 하나를 포함하는, 상호연결 구조체.

청구 8항:

제1항 내지 제7항 중 어느 한 항에 있어서,

확산 장벽 속성을 갖는 상기 절연층 또는 금속층은 탄화 규소, 질화 규소, 질소와 수소 도핑된 탄화규소 및 순수형, 합금형 또는 질화형 Ta, Ru, Ir, W, Co, Ti 및 Rh로부터 선택되는 금속 물질 중 하나를 포함하는, 상호연결 구조체.

청구 9항:

대략 4.0 이하의 유전 상수를 갖는 유전 물질;

상기 유전 물질 내에 매립되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 구리 함유 도전 물질 - 상기 구리 함유 도전 물질의 상기 상부 표면은 상기 유전 물질의 상부 표면 아래에 위치함 - ;

상기 구리 함유 도전 물질의 상기 측벽 표면들 및 상기 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽; 및

상기 도전 물질의 상기 상부 표면 상에 위치하고, 적어도 상기 U-형 장벽의 적어도 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성을 갖는 절연층 또는 금속층

을 포함하는, 상호연결 구조체.

청구 9항:

diffusion barrier attribute includes one among the metal material selected from the silicon carbide and the A -doped napiform the silicon carbide, the silicon nitride, and nitrogen and hydrogen, and the alloy type or the nitride type Ta, the Ru, the Ir, W, the Co, the Ti and Rh.

Claim 8:

As for any one of claim 1 through claim 7, the mutual linking structure wherein the insulating layer or the metallic layer having

diffusion barrier attribute includes one among the metal material selected from the silicon carbide and the A -doped napiform the silicon carbide, the silicon nitride, and nitrogen and hydrogen, and the alloy type or the nitride type Ta, the Ru, the Ir, W, the Co, the Ti and Rh.

Claim 9:

Approximately, the mutual linking structure which comprises side wall surfaces reclaimed within the dielectric material :

dielectric material having the dielectric constant less than 4.0, the bottom surface, and the insulating layer or the metallic layer

having the diffusion barrier attribute which has edge areas contacting with at least upper sidewall surfaces of at least U- type obstacle it is located on surface the top surface of the conducting material and at least one U- type diffusion barrier :

located on surface side wall surfaces and bottom surface of - :

copper-containing conducting material the top surface of the copper-containing conducting material - copper-containing conducting material having the top surface is positioned under the top surface of the dielectric material.

Claim 9:

대략 4.0 이하의 유전 상수를 갖는 유전 물질; Approximately, the mutual linking structure which comprises side wall surfaces reclaimed within the dielectric material :

상기 유전 물질 내에 매립되는 측벽 표면들, 바닥 표면 및 상부 표면을 갖는 구리 함유 도전 물질 - 상기 구리 함유 도전 물질의 상기 상부 표면은 상기 유전 물질의 상부 표면 아래에 위치함 - ;

dielectric material having the dielectric constant less than 4.0, the bottom surface, and the insulating layer or the metallic layer

상기 구리 함유 도전 물질의 상기 측벽 표면들 및 상기 바닥 표면 상에 위치하는 적어도 하나의 U-형 확산 장벽; 및

having the diffusion barrier attribute which has edge areas contacting with at least upper sidewall surfaces of at least U-type obstacle it is located on surface the top surface of the conducting material and at least one U-type diffusion barrier :

상기 도전 물질의 상기 상부 표면 상에 위치하고, 적어도 상기 U-형 장벽의 적어도 상부 측벽 표면들과 접하는 에지 부분들을 갖는, 확산 장벽 속성을 갖는 절연층 또는 금속층

located on surface side wall surfaces and bottom surface of - :

을 포함하는, 상호연결 구조체.

copper-containing conducting material the top surface of the copper-containing conducting material - copper-containing conducting material having the top surface is positioned under the top surface of the dielectric material.

청구 10항:

상호연결 구조체를 형성하는 방법으로서,

약 4.0 이하의 유전 상수를 갖는 유전 물질 내로 적어도 하나의 개구를 형성하는 단계 - 상기 유전 물질은 상기 유전 물질의 상부 표면 상에 위치하는 패턴닝된 하드 마스크를 가짐 - ;

Claim 10:

As the method for forming the mutual linking structure, another part of the insulation material which has the top surface in which the step - conducting material which partly fills in the opening of the step :

상기 적어도 하나의 개구와 상기 패턴닝된 하드 마스크를 확산 장벽으로 라이닝(lining)하는 단계;

at least one which has the patterned hard mask in which the step - dielectric material forming at least one opening within the dielectric material having the dielectric constant less than

상기 적어도 하나의 개구를 도전 물질로 부분적으로 채우는 단계 - 상기 도전 물질은 상기 유전 물질의 상부 표면 아래에 위치하는 상부 표면을 가짐 - ;

about 4.0 is located on surface the top surface of the dielectric material has the opening and above-mentioned patterned hard mask of - :

상기 적어도 하나의 개구 내와 상기 도전 물질의 상기 상부 표면 상뿐만 아니라 상기 패턴닝된 하드 마스크를 라이닝하는 상기 확산 장벽의 위에 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질을 형성하는 단계; 및

at least one as the diffusion barrier with the lining (lining) with the conducting material is positioned under the top surface of the dielectric material has the diffusion barrier attribute on the upper part of not only the top surface phase of inside of the opening of - :

상기 적어도 하나의 개구 내에 확산 장벽 속성을 갖는 상기 절연 물질 또는 금속 물질의 또 다른 부분을 유지하고 상기 적어도 하나의 개구 내에 U-형 확산 장벽을 형성하고, 상기 유전 물질의 상기 상부 표면 위에 위치하는 상기 패턴닝된 하드 마스크와 상기 확산 장벽 및 상기 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 일부분을 제거하는 단계를 포함하고,

확산 장벽 속성을 갖는 상기 절연 물질 또는 금속 물질의 상기 또 다른 부분은 상기 유전 물질의 상기 상부 표면과 동일 평면 상의(coplanar) 상부 표면을 갖고, 상기 도전 물질은 상기 도전 물질의 측벽 표면들 및 바닥 표면 상에 위치한 상기 U-형 확산 장벽에 의해 완전히 둘러싸이며, 확산 장벽 속성을 갖는 상기 절연 물질의 상기 또 다른 부분은 상기 도전 물질의 상기 상부 표면 상에 위치하는, 상호연결 구조체 형성 방법.

at least one and conducting material but also the diffusion barrier doing lining the above-mentioned patterned hard mask or the insulation material having the diffusion barrier attribute within the step :

of forming the metal material and at least one opening or the metal material is maintained and the U- type diffusion barrier is formed within at least one opening. A mutual linking structure formation method comprising the steps of: the step of removing one part of the above-mentioned hard mask which being patterned positioned on the top surface of the dielectric material and diffusion barrier and the insulation material having the diffusion barrier attribute or the metal material is included; another part of the insulation material or the metal material having

diffusion barrier attribute has the same plane top cloth (coplanar) top surface as the top surface of the dielectric material; completely surrounding with the U- type diffusion barrier in which the conducting material is located on surface the side wall surfaces and bottom surface of the conducting material; and another part of the insulation material having the diffusion barrier attribute is located on surface the top surface of the conducting material.

청구 10항:

상호연결 구조체를 형성하는 방법으로서,

약 4.0 이하의 유전 상수를 갖는 유전 물질 내로 적어도 하나의 개구를 형성하는 단계 - 상기 유전 물질은 상기 유전 물질의 상부 표면 상에 위치하는 패턴닝된 하드 마스크를 가짐 - ;

상기 적어도 하나의 개구와 상기 패턴닝된 하드 마스크를 확산 장벽으로 라이닝(lining)하는 단계;

상기 적어도 하나의 개구를 도전 물질로 부분적으로 채우는 단계 - 상기 도전 물질은 상기

Claim 10:

As the method for forming the mutual linking structure, another part of the insulation material which has the top surface in which the step - conducting material which partly fills in the opening of the step :

at least one which has the patterned hard mask in which the step - dielectric material forming at least one opening within the dielectric material having the dielectric constant less than

about 4.0 is located on surface the top surface of the dielectric material has the opening and above-mentioned patterned ha

유전 물질의 상부 표면 아래에 위치하는 상부 rd mask of - :
표면을 가짐 - ;

상기 적어도 하나의 개구 내와 상기 도전 물질의 상기 상부 표면 상뿐만 아니라 상기 패턴닝된 하드 마스크를 라이닝하는 상기 확산 장벽의 위에 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질을 형성하는 단계; 및

상기 적어도 하나의 개구 내에 확산 장벽 속성을 갖는 상기 절연 물질 또는 금속 물질의 또 다른 부분을 유지하고 상기 적어도 하나의 개구 내에 U-형 확산 장벽을 형성하고, 상기 유전 물질의 상기 상부 표면 위에 위치하는 상기 패턴닝된 하드 마스크와 상기 확산 장벽 및 상기 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질의 일부분을 제거하는 단계를 포함하고,

확산 장벽 속성을 갖는 상기 절연 물질 또는 금속 물질의 상기 또 다른 부분은 상기 유전 물질의 상기 상부 표면과 동일 평면 상의(coplanar) 상부 표면을 갖고, 상기 도전 물질은 상기 도전 물질의 측벽 표면들 및 바닥 표면 상에 위치한 상기 U-형 확산 장벽에 의해 완전히 둘러싸이며, 확산 장벽 속성을 갖는 상기 절연 물질의 상기 또 다른 부분은 상기 도전 물질의 상기 상부 표면 상에 위치하는, 상호연결 구조체 형성 방법.

at least one as the diffusion barrier with the lining (lining) with the conducting material is positioned under the top surface of the dielectric material has the diffusion barrier attribute on the upper part of not only the top surface phase of inside of the opening of - :

at least one and conducting material but also the diffusion barrier doing lining the above-mentioned patterned hard mask or the insulation material having the diffusion barrier attribute within the step :

of forming the metal material and at least one opening or the metal material is maintained and the U- type diffusion barrier is formed within at least one opening. A mutual linking structure formation method comprising the steps of: the step of removing one part of the above-mentioned hard mask which being patterned positioned on the top surface of the dielectric material and diffusion barrier and the insulation material having the diffusion barrier attribute or the metal material is included; another part of the insulation material or the metal material having

diffusion barrier attribute has the same plane top cloth (coplanar) top surface as the top surface of the dielectric material; completely surrounding with the U- type diffusion barrier in which the conducting material is located on surface the side wall surfaces and bottom surface of the conducting material; and another part of the insulation material having the diffusion barrier attribute is located on surface the top surface of the conducting material.

기술분야

본 발명은 반도체 구조체와 이의 제조 방법에 관한 것이다. 본 발명은 더 구체적으로는 상호연결 유전체(interconnect dielectric)의 상부 표면에 높은 누설 저항을 가질뿐만 아니라, 금

Technical Field

The invention relates to the semiconductor structure and manufacturing method thereof. The invention relates to the mutual linking structure of the semiconductor with

속성 잔류물들(metallic residues)(예를 들어, 결함들)이 없는 반도체의 상호연결 구조체와 이의 제조 방법에 관한 것이다. 상호연결 유전체의 상부 표면에서 금속성 잔류물(예를 들어, 결함들)이 형성되는 것을 피하면서, 상호연결 구조체 내의 누설저항이 개선된다.

hout the metallic residue (metallic residues) (for example, deformities) more specifically, it has the high leak resistance on the top surface of the interconnection dielectric (interconnect dielectric) and manufacturing method thereof. In the top surface of the interconnection dielectric, while it avoids that the metallic residue (for example, deformities) is formed the leak resistance within the mutual linking structure is improved.

배경기술

일반적으로 반도체 장치들은 반도체 기판 상에 제조되는 집적회로(IC)를 형성하는 복수의 회로를 포함된다. 신호 경로들의 복합 네트워크는 일반적으로 기판의 표면 상에 분포된 회로 소자들을 연결하기 위해 라우팅된다. 장치에 걸쳐서 이러한 신호들의 효율적인 라우팅은 예를 들어 싱글 또는 듀얼 다마신 배선 구조(damascene wiring structures)와 같은 멀티레벨 또는 다층(multilayered) 기법들의 형성을 요구한다. 배선 구조는 일반적으로 구리, Cu 또는 Cu 합금을 포함하는데, 이는 Cu 기반 상호연결체들이 알루미늄, Al 기반 상호연결체들과 비교했을 때 복합 반도체 칩 상의 많은 수의 트랜지스터들 사이의 더 높은 속도의 신호 전송을 제공하기 때문이다.

일반적인 상호연결 구조체 내에서, 금속 비아들(vias)은 반도체 기판에 수직하게 배열되고 금속 선들은 반도체 기판에 평행하게 배열된다. 오늘날의 IC 제품 칩들은 4.0 미만의 유전 상수를 갖는 유전 물질에 금속 선들과 금속 비아들(예를 들어, 도전성 피쳐들(conductive features))을 매립(embedding)함으로써, 신호 속도의 추가적인 향상과 인접하는 금속 선들의 신호(#34#크로스토크(crosstalk)#34#로 알려짐)의 감소를 달성하였다.

Background Art

Generally, it is multiple circuits in which semiconductor devices form the manufactured integrated circuit (IC) on the semiconductor substrate included. It is routed circuit devices in which the generally the complex network of the signaling paths is distributed on the surface of the substrate are connected. Such efficient routing of the signals demands for example, the formation of the multi-level like single or the dual damascene interconnection structure (damascene wiring structures) or multilayer (multilayered) techniques through the apparatus. The wiring structure many signal transmission of the speed of being much higher between the transistors of the number on the complex semiconductor chip is due to be provided compared to this, Cu base interconnects aluminum, and Al base interconnects generally, the copper, and the Cu or the Cu alloy are included.

The metal via (vias) is perpendicularly arranged in the semiconductor substrate and metal lines are arranged in the general mutual linking structure parallel to the semiconductor substrate. IC device chip of the today achieved the reduction of the signal (it is known by the "cross-talk (crosstalk)") adjacent to the additional improvement of the signal speed of metal lines metal lines and metal via (for example, the conducting feature (conductive features)) in the dielectric material having the dielectric constant less than 4.0 as the padding (embedding) box.

현재의 반도체 상호연결 구조체들에서는, TDDDB(time-dependent-dielectric-breakdown)가 Cu 기반 금속층(metallurgy)과 낮은 k 유전 물질(low K dielectric materials)을 포함하는 미래의 상호연결 구조체들에 대한 주요 신뢰성 문제들 중의 하나로 파악된다. #34#TDDDB#34#는 상호연결 구조체의 유전 물질이 시간이 경과함에 따라 손상이 생기기 시작한다는 것을 의미한다. 유전 물질의 손상은 상호연결 구조체를 준비하는 동안 상호연결 유전 물질의 표면 상에 형성되는 진성 수단(intrinsic means) 또는 결함들에 의해 유발될 수 있다.

상호연결 유전체 표면을 따라서 나타나는 금속 이온, 특히 Cu 이온의 누설이 TDDDB에 기여하는 주요 진성 손상 메커니즘으로 파악된다. 도 1a는 이러한 진성 누설 현상을 나타내는 선행 기술의 상호연결 구조체(10)이다. 구체적으로, 선행 기술의 상호연결 구조체는 Cu 피쳐(14)가 매립된 유전 물질(12)을 포함한다. Cu 피쳐(14)는 일반적으로 확산 장벽(diffusion barrier; 16)에 의해 유전 물질(12)로부터 분리된다. 유전 캐핑 층(dielectric capping layer; 18)은 유전 물질(12), 확산 장벽(16) 및 Cu 피쳐(14)의 표면 상에 존재한다. 도 1a에서 화살표들은 도시된 바와 같이 상호연결 구조체의 상부 표면을 따라 발생하는 도전성 피쳐(14)로부터의 Cu 이온들의 누설(확산)을 표시한다. 시간이 경과함에 따라, 이러한 Cu 이온들의 누설은 TDDDB뿐만 아니라 상호연결 구조체 내의 장치들의 손상을 발생시킨다.

도 1b에 도시된 바와 같이, TDDDB에 대한 또 다른 기여 인자는 결함과 연관되어 있다. 구체적으로, 도 1b는 Cu 잔류물(20)(예를 들어, 결함)이 유전 물질(12)의 상부 표면과 유전 캐핑 층(18) 사이의 인터페이스에 존재하는 도 1a에 도시된 컴포넌트들을 포함하는 또 다른 선행 기술의 상호연결 구조체(10#39#)이다.

In current semiconductor mutual linking structures, the TDDDB (time-dependent-dielectric-breakdown) is the Cu base metallic layer (metallurgy) and low k dielectric material (low K dielectric materials) grasped due to one of major reliability problems toward the mutual linking structures of the future included. It means that the damage begins to happen as the dielectric material of the mutual linking structure of time as to the "TDDDB", passes. While preparing for the mutual linking structure the damage of the dielectric material can be caused by the intrinsic means or the deformities formed on the surface of the interconnection dielectric material.

The metal ion, showing up according to the interconnection dielectric surface especially, the leakage of the Cu ion is perceived due to the major intrinsic damage mechanism contributing to TDDDB. Figure 1a is a mutual linking structure (10) of the prior art showing such intrinsic leakage phenomenon. Specifically, the mutual linking structure of the prior art includes the dielectric material (12) in which the Cu feature (14) is reclaimed. Generally the Cu feature (14) is separated from the dielectric material (12) by the diffusion barrier (diffusion barrier: 16). The hereditary capping layer (dielectric capping layer: 18) resides above the dielectric material (12), and the surface of the Cu feature (14) and diffusion barrier (16). In the drawing 1a, arrows indicate the leakage (diffusion) of Cu ions from the conducting feature (14) which as shown in the figure, is generated according to the top surface of the mutual linking structure. As time passes the leakage of such Cu ions generates the damage of the apparatuses within not only TDDDB but also the mutual linking structure.

As shown in FIG. 1b, another contributing factors about TDDDB is related to the deformity. Specifically, figure 1b is a mutual linking structure (10') of another prior art including the components illustrated in Figure 1a the Cu residue (20) (for example, the deformity) existing in the interface between the top surface of the dielectric ma

Cu 잔류물(20)은 Cu 피쳐(14)(즉, 유전 물질(12) 내로 형성되는 개구 내의 Cu의 피착(deposition) 및 연마(planarization))가 형성되는 동안 형성된다. 유전 물질의 표면에 결함을 제공하는 포스트 연마 Cu 잔류물들은 TDDB 손상의 주요 원인들 중 하나이다.

위에서 Cu가 선행 기술의 상호연결 구조체들과 관련하여 구체적으로 설명되었지만, 전술한 누설과 결함 문제들은, 예를 들어 Al 및 W와 같은 다른 유형의 도전성 금속들에서도 (상이한 속도 및 정도로) 일어난다는 것을 유의해야 한다.

도 1a에 도시된 누설 문제와 도 1b에 도시된 잔류물 문제에 비추어 볼 때, 금속 누설, 특히 Cu 이온 확산과 금속성 잔류물, 특히 Cu 잔류물 모두가 상호연결 구조체로부터 감소되거나 또는 완전하게 제거될 수 있는 상호연결 구조체를 제공해야 할 계속적인 필요성이 있다.

terial (12) and the heredity capping layer (18). While the Cu residue (20) Cu feature (14) (the deposition of the Cu within the opening formed within in other words, the dielectric material (12) and grinding (planarization)) are formed it is formed. Post grinding Cu residues providing the deformity on the surface of the dielectric material are one among the main causes of the TDDB damage.

In the upper part, specifically the Cu was explained in connection with the mutual linking structures of the prior art. However the above-described leakage and the defect problems have to note occurring in for example, the dissimilar conductive metals of the type such as the Al and W.

When it lights to the leakage problem illustrated in Figure 1a and residue problem illustrated in Figure 1b, the metal leakage, especially, the Cu ion diffusion and metallic residue, especially, the Cu residue everyone are on the decrease from the mutual linking structure or it has the continuous necessity to provide the mutual linking structure which perfects can be removed.

발명을 실시하기 위한 구체적인 내용

높은 누설 저항을 갖고 유전 물질의 표면에 존재하는 금속성 잔류물이 없는 상호연결 구조체 및 상호연결 구조체를 제조하는 방법을 제공하는 본 발명은 본 출원에 첨부되는 다음의 설명 및 도면을 참조함으로써 더 자세히 기술될 것이다. 본 출원의 도면은 오직 예시적인 목적을 위해 제공되며, 도면은 축척에 맞게 도시되지 않았음을 주의해야 한다.

다음의 설명에서, 특정 구조, 컴포넌트, 물질, 치수, 프로세스 단계 및 기술과 같은 수많은 구체적인 세부사항이 본 발명의 전체적인 이해를 제공하기 위해 제공된다. 그러나, 본 발명은 이러한 구체적인 세부사항 없이 실시될 수 있다는 것이 본 기술분야의 당업자에게 명백할

Description of Embodiments

By referring to the following description and drawing attached to the application which the invention providing the mutual linking structure without the metallic residue having the high leak resistance and exists on the surface of the dielectric material and the method for manufacturing the mutual linking structure looks it will be more described in detail. The drawing of this application is only provided for the purpose of being illustrative and it has to note that drawing was not illustrated according to accumulation.

In the following description, so that the numerous detailed detail article like the specific scheme, component, material, dimension, process step and technology provide the understanding of being whole of the invention technology is provided. But it will be clear to the person skilled in the art

것이다. 또 다른 예에서, 잘 알려진 구조 또는 프로세스 단계는 본 발명을 모호하게 만드는 것을 피하기 위해 상세히 기술되지 않는다.

층, 영역 또는 기판과 같은 요소가 또 다른 요소 #34#상에#34# 또는 #34#위에#34# 위치한다고 지칭될 때, 다른 요소 바로 위에 있을 수 있거나, 또는 개입 요소가 또한 존재할 수 있다. 반대로, 요소가 또 다른 요소 #34#바로 위#34# 또는 #34#바로 상부에#34# 위치한다고 지칭될 때, 개입 요소는 존재하지 않는다. 요소가 또 다른 요소에 #34#연결된다#34# 또는 #34#결합된다#34#고 지칭될 때, 다른 요소에 직접 연결되거나 결합될 수 있거나, 또는 개입 요소가 존재할 수 있다. 반대로, 요소가 또 다른 요소에 #34#직접 연결된다#34# 또는 #34#직접 결합된다#34#고 지칭될 때, 개입 요소는 존재하지 않는다.

전술한 바와 같이, 본 발명은 높은 누설 저항을 갖고 유전 물질의 표면에 존재하는 금속성 잔류물이 없는 상호연결 구조체 및 상호연결 구조체를 제조하는 방법을 제공한다. 본 발명의 상호연결 구조체는 선행 기술 발명의 구조체보다 개선된 TDDb를 나타낸다.

본 발명의 상호연결 구조체에서, 도전성 피쳐(즉, 도전 물질)는 유전 물질의 상부 표면과 동일 평면에 있지 않지만, 대신에 도전 물질은 유전 물질의 상부 표면 아래에 리세스된다. 유전 물질의 상부 표면 아래에 리세스될뿐만 아니라, 본 발명의 상호연결 구조체의 도전 물질은 모든 면(예를 들어, 측벽 표면, 상부 표면, 및 바닥 표면)이 확산 장벽 물질에 의해 둘러싸여진다. 개구 내의 리세스된 도전 물질의 측벽 표면 및 바닥 표면이 U-형 확산 장벽으로

t of this technical field that the invention can be performed without such detailed detail article. In another example, in order to avoid that the well known structure or the process step ambiguously makes the invention it is not described.

When the layer, and the element such as the domain and substrate are called in another element " phase to be positioned at the " the upper part with 34 , it can be in the dissimilar element, immediately, the upper part or the intervention element moreover can exist. On the contrary, when it is called that the element is positioned with another element " , immediately, the " or the " , immediately, on top " , the intervention element is nonexistent. When the element is connected to another element with " the element is combined with 34 it is with 34 and it is called , it is connected directly to the dissimilar element or the element can be combined or the intervention element can exist. On the contrary, when the element is connected directly to another element with " the element is directly combined with 34 it is with 34 and it is called , the intervention element is nonexistent.

As described above, the present invention is to provide the mutual linking structure without the metallic residue which exists on the surface of the dielectric material it has the high leak resistance and the method for manufacturing the mutual linking structure. TDDb in which the mutual linking structure of the invention is improved than the structure of the prior art invention is shown.

In the mutual linking structure of the invention, the conducting feature (in other words, the conducting material) is not in the same plane as the top surface of the dielectric material. However the conducting material is instead of recessed under the top surface of the dielectric material. It is recessed under the top surface of the dielectric material. In addition the conducting material of the mutual linking structure of the invention every respect (for example,

라이닝된다. 리세싱된 도전 물질의 상부 표면은 절연층 또는 금속층으로 라이닝되고, 이들 모두는 확산 장벽 속성을 갖는다. 도전 물질의 상부 표면을 라이닝하는 절연층 또는 금속층의 에지 부분은 U-형 확산 장벽의 상부 측벽 표면, 또는 U-형 도금 시드층이 존재한다면 선택적인 U-형 도금 시드층과 접한다.

the side wall surface, and the top surface and bottom surface) surround with under barrier metal. The side wall surface of the recessed conducting material within the opening and bottom surface are lined to the U- type diffusion barrier. The recessed top surface of the conducting material is lined to the insulating layer or the metallic layer and all of them has the diffusion barrier attribute. If the upper sidewall surface or the U- type plated seed layer of the U- type diffusion barrier exists the edge area of the insulating layer or the metallic layer doing lining the top surface of the conducting material contacts with the selective U- type plated seed layer.

본 출원에서 리세싱된 도전 물질과 유전 물질 사이에 직접적인 접촉이 없고, 선행 기술 상호연결 구조체에서의 경우와 같이 이러한 도전성 잔류물이 상호연결 구조체의 상부 표면에 형성되지 않으므로 상호연결 유전체의 표면 상에서 연장되는 도전 물질의 연마(planarization)는 사용되지 않는다는 것을 또한 유의해야 한다. 상기 태양은 유전체 표면 상의 도전성 금속 잔류물(예를 들어, 결함)을 감소시키는 데 현저한 효과를 가진다.

There is no direct contact between the conducting material and the dielectric material recessed in this application and it moreover has to note that the extended grinding (planarization) of the conducting material is not used on the surface of the interconnection dielectric since such conductive stringer is not formed in the top surface of the mutual linking structure like the case at the prior art mutual linking structure. The conductive metal residue (for example, the deformity) on the dielectric surface is reduced but still has the notable effect.

도 2a-2g를 참조하면, 도 2a-2g는 본 발명의 반도체 상호연결 구조체를 형성하는 데 사용되는 기본 프로세스 단계를 도시한다. 도 2a는 유전 물질(52) 및 유전 물질(52)의 표면 상에 위치하는 하드 마스크(54)를 포함하는 초기 구조체(50)를 도시한다.

Referring to Figure 2a-2g, figure 2a-2g shows the basic process step of being used to form the semiconductor mutual linking structure of the invention. Figure 2a shows the initial configuration (50) including the hard mask (54) located on surface the surface of the dielectric material (52) and dielectric material (52).

초기 구조체(50), 즉, 유전 물질(52)은 (본 출원의 도면에 도시되지 않은) 기판 상에 위치할 수 있다. 도시되지 않은 기판은 반도체 물질, 절연 물질, 도전 물질 또는 이들의 임의의 조합을 포함할 수 있다. 기판이 반도체 물질로 구성될 때, Si, SiGe, SiGeC, SiC, Ge 합금, GaAs, InAs, InP 및 다른 III/V 또는 II/VI 화합물 반도체와 같은 임의의 반도체가 사용될 수 있다. 이러한 나열된 유형의 반도체 물질뿐만 아니라, 본 발명은 또한 반도체 기판이, 예

The initial configuration (50), in other words, the dielectric material (52) can be located on surface (is not illustrated in the drawing of this application) substrate. The substrate which is not illustrated may include the semiconductor material, the insulation material, and the conducting material or their arbitrary combination. When the substrate is made up of the semiconductor material the arbitrary semiconductor like the si, siGe, siGeC, siC, ge alloy, gaAs,

를 들어 Si/SiGe, Si/SiC, SOI(silicon-on-insulator) 또는 SGOI(silicon germanium-on-insulator)와 같은 계층화된 반도체인 경우도 고려한다.

기판이 절연 물질일 때, 절연 물질은 유기 절연체, 무기 절연체 또는 복수층을 포함하는 이들의 조합일 수 있다. 기판이 도전 물질일 때, 기판은 예를 들어 다결정 규소(PolySi), 원소 금속(elemental metal), 원소 금속의 합금, 금속 규화물, 금속 질화물 또는 복수층을 포함하는 이들의 조합을 포함할 수 있다. 기판이 반도체 물질을 포함할 때, 예를 들어 CMOS(complementary metal oxide semiconductor) 장치와 같은 하나 이상의 반도체 장치가 그 위에 제조될 수 있다. 기판이 절연 물질 및 도전 물질의 조합을 포함할 때, 기판은 다층 상호연결 구조체(multilayered interconnect structure)의 제1 상호연결 레벨을 나타낼 수 있다.

유전 물질(52)은 무기 유전체 또는 유기 유전체를 포함하는 임의의 인터레벨(interlevel) 또는 인트라레벨(intralevel) 유전체를 포함한다. 유전 물질(52)은 다공성이거나 비-다공성일 수 있다. 유전 물질(52)로서 사용될 수 있는 적절한 유전체의 소정의 예는 SiO₂, 실세스퀴옥산, Si, C, O 및 H의 원자를 포함하는 C 도핑된 산화물(즉, 올가노실리케이트(organo silicates)), 열경화성 폴리아릴렌 에테르 또는 그들의 복수층을 포함하지만, 이에 한정되는 것은 아니다. #34#폴리아릴렌#34#이라는 용어는 본 출원에서 결합(bonds), 축합 고리(fused ring) 또는 예를 들어, 산소, 유황, 술폰(sulfone), 술폭시화물(sulfoxide), 카르보닐기(carbonyl) 등과 같은 비활성 결합 그룹(inert linking groups)에 의해 함께 결합된 아

inAs, inP and the other III / V or the II / VI compound semiconductor can be used. Even in case moreover, the semiconductor substrate is for example, the Si / SiGe, the Si / SiC, and the layered semiconductor such as the SOI (silicon-on-insulator) and SGOI (silicon germanium-on-insulator) the enumerated invention not only the semiconductor material of the type considers.

When the substrate is the insulation material it can be their combination in which the insulation material includes organic insulator, and the inorganic insulator or the multi-layer. The substrate the substrate is the conducting material, for example, can comprise their combination including the polycrystalline silicon (PolySi), the elemental metal, the alloy of the elemental metal, the metal silicide, and the metal-nitride or the multi-layer. When the substrate includes the semiconductor material for example, at least one semiconductor device like the CMOS (complementary metal oxide semiconductor) apparatus can be manufactured for the upper part. When the substrate includes the combination of the conducting material and insulation material the substrate can show the first interconnect level of the multi layer mutual linking structure (multilayered interconnect structure).

The dielectric material (52) is used in order to express the aryl residue (aryl moieties) which includes the A -doped oxide (in other words, the organo silicate (organosilicates)) C, and the thermosetting property polyarylene ether or their multi-layers and however it is not thus restricted is coupled together in the application which the term called the " polyarylene " this looks with the combination (bonds), and the condensed cycle (fused ring), for example, the deactivation bonding group (inert linking groups) like the oxygen, sulfur, the sulfone, the sulfoxy cargo (sulfoxide), the carbonyl radical etc. Or the deactivation, substitution, the aryl residue (inertly substitute aryl moieties) including the predetermined example of the arbitrary interlevel

릴 잔기(aryl moieties) 또는 비활성 대체 아릴 잔기(inertly substitute aryl moieties)를 표현하기 위해 사용된다.

유전 물질(52)은 일반적으로 약 4.0 이하의 유전 상수를 가지며, 유전 상수는 약 2.8 이하인 것이 더 일반적이다. 본 명세서에 언급된 모든 유전 상수는 특별히 다르게 언급되지 않는 한 진공에 관한 수치이다. 이러한 유전체들은 4.0 보다 더 높은 유전 상수를 가지는 유전 물질과 비교할 때 일반적으로 더 낮은 기생 크로스 토크(parasitic cross talk)를 가진다. 유전 물질(52)의 두께는 사용되는 유전 물질뿐만 아니라 유전 물질(52) 내의 유전층의 정확한 개수에 따라 변할 수 있다. 일반적으로, 일반적인 상호연결 구조체에 대하여, 유전 물질(52)은 약 50nm에서 약 1000nm의 두께를 가진다.

전술한 바와 같이, 초기 구조체(50)는 또한 유전 물질(52)의 상부 표면 상에 위치한 하드 마스크(54)를 포함한다. 하드 마스크(54)는 산화물, 질화물, 산화질화물 또는 이들의 임의의 다층 조합을 포함한다. 일 실시예에서, 하드 마스크(54)는 이산화 규소(silicon dioxide)과 같은 산화물인 반면, 또 다른 실시예에서 하드 마스크(54)는 질화 규소과 같은 질화물이다.

하드 마스크(54)는 예를 들어, 화학 기상 피착(Cheical Vapor Deposition; CVD), 플라즈마 강화 화학 기상 피착(Plasma Enhanced Chemical Vapor Deposition; PECVD), 화학 용액 피착(chemical solution deposition), 증착(evaporation) 및 물리 기상 피착(Physical Vapor Deposition; PVD)을 포함하는 종래의 피착 프로세스를 사용하여 형성된다.

including the inorganic dielectric or the organic dielectric substance or the proper dielectric which can be used as the dielectric material (52) it can be the non-porous the dielectric material (52) is the porosity it includes the intralevel dielectric is the SiO_2 , the silsesquioxane, the Si, C, O, and the atom of H.

Generally the dielectric material (52) has the dielectric constant less than about 4.0 and the dielectric constant is more general about 2.8 or less. As long as all dielectric constants mentioned in this specification are not specially differently mentioned it is the value about the vacuum. Such dielectrics generally it has the lower parasitic cross-talk (parasitic cross talk) compared to the dielectric material having the dielectric constant which is much higher than 4.0. It can change according to the correct number of the dielectric layer within not only the dielectric material in which the thickness of the dielectric material (52) is used but also the dielectric material (52). Generally, in the dielectric material (52) about the general mutual linking structure, is about 50nm, it has the thickness of about 1000nm.

As described above, the hard mask (54) in which the initial configuration (50) is located on surface moreover, the top surface of the dielectric material (52) is included. The hard mask (54) comprises the oxide, the nitride, the oxynitride, or their arbitrary multi layer combination. In one embodiment, whereas the hard mask (54) is the oxide like the silicon dioxide it is the nitride such as the hard mask (54) is the silicon nitride in another preferred embodiment.

The hard mask (54) is formed using the conventional deposition process including for example, the chemical vapor deposition (Chemical Vapor Deposition: CVD), the plasma enhanced chemical vapor deposition (Plasma Enhanced Chemical Vapor Deposition: PECVD), the chemical solution deposition, deposition (evaporation) and physical vapor sticking (Physical Vapor De

대안적으로, 하드 마스크(54)는 열산화(thermal oxidation) 및 열질화(thermal nitridation) 중 하나에 의해 형성될 수 있다.

본 발명에 사용되는 하드 마스크(54)의 두께는 하드 마스크 자체의 물질뿐만 아니라 이를 형성하는데 사용되는 기술에 따라 변할 수 있다. 일반적으로, 하드 마스크(54)는 약 5nm에서 약 100nm의 두께를 가지며, 약 10nm에서 약 80nm의 두께가 더 일반적이다.

다음으로, 도 2b에 도시된 바와 같이, 적어도 하나의 개구(56)가 리소그래피 및 에칭을 사용하여 하드 마스크(54)와 유전 물질(52) 내로 형성된다. 리소그래픽 프로세스는 하드 마스크(54) 위에 포토레지스트(photoresist) (도시되지 않음)를 형성하는 단계, 포토레지스트를 원하는 패턴의 방사에 노출하는 단계 및 종래의 레지스트 현상액(resist developer)을 사용하여 노출된 포토레지스트를 현상하는 단계를 포함한다. 에칭 프로세스는 드라이 에칭 프로세스(예를 들어, 반응성 이온 에칭(reactive ion etching), 이온 빔 에칭(ion beam etching), 플라즈마 에칭 또는 레이저 어블레이션(laser ablation)) 및/또는 습식 화학 에칭 프로세스(wet chemical etching process)를 포함한다. 일반적으로, 반응성 이온 에칭은 적어도 하나의 개구(56)를 제공하는데 사용된다. 일반적으로, 에칭 프로세스는 포토레지스트에 제공되는 패턴이 하드 마스크(54)로 전사(transferred)되는 제1 패턴 전사 단계(first pattern transfer step)를 포함하며, 패턴닝된 포토레지스트는 이후에 애싱(ashing) 단계에 의해 제거되며, 그 다음에 제2 패턴 전사 단계가 패턴닝된 하드 마스크로부터의 패턴을 아래의 유전 물질 내로 전사하기 위해 사용된다.

유전 물질(54) 내로 형성된 적어도 하나의 개구(56)의 깊이(유전 물질의 상부 표면에서부터 개구의 바닥 벽까지 측정됨)는 변할 수 있으며 본 출원에 있어서 중요하지 않다. 일부 실시예에서, 적어도 하나의 개구(56)는 유전 물질을 완전히 통과해서 연장될 수 있다. 또 다른 실시예에서, 적어도 하나의 개구(56)는

position: PVD). Alternatively, the hard mask (54) is formed by one among the thermal oxidation and heat-nitriding (thermal nitridation).

The thickness of the hard mask (54) possible to be used in the present invention can change according to not only the material of the hard mask itself but also the technology which is used to form this. Generally, in the hard mask (54) is about 5nm, it has the thickness of about 100nm and the thickness of about 80nm is more general in about 10nm.

Next, as shown in FIG. 2b, at least one opening (56) is formed using lithography and etching within the hard mask (54) and dielectric material (52). The lithographic process comprises the step of developing the step of forming the photoresist (photoresist) (not shown) on the hard mask (54), and the step of exposing the photoresist to the radiation of the desired pattern and the photoresist exposed using the conventional resist developer. The etching process includes dry etching process (for example, the reactive ion etch (reactive ion etching), the ion beam etching, and the plasma etching or the laser ablation) and/or the wet chemical etching process. Generally, the reactive ion etch is used when at least one opening (56) is provided. Generally, the first pattern transfer step in which the pattern in which the etching process is provided to the photoresist consists of the hard mask (54) with the imprint (transferred) is included and thereafter the patterned photoresist is removed using the ashing step and it is used in order to transfer the pattern from the hard mask in which and then, the second pattern transfer step is patterned within the following dielectric material.

The non-critical as to the application which it looks at while the depth (in the top surface of the dielectric material, it is measured to the bottom wall of the opening) of at least one opening (56) formed within the dielectric material (54) can change. In some embodiments, at least one opening

유전 물질(52) 자체 내에서 멈춘다. 또 다른 실시예에서, 상이한 깊이의 개구가 형성될 수 있다.

적어도 하나의 개구(56)는 비아 개구(via opening), 선 개구(line opening) 및/또는 결합된 비아/선 개구(combined via/line opening)일 수 있다. 도 2b에서, 예를 들어 각각의 개구는 선 개구로서 도시된다.

다음으로, 도 2c에서 도시된 바와 같이, 확산 장벽(58)은 그 안에 적어도 하나의 개구를 포함하는 도 2b에 도시된 구조체의 모든 노출된 표면 상에서 (즉, 각각의 개구의 측벽 및 바닥 상에서) 남아있는 하드 마스크(54)의 상부 표면을 따라 형성된다.

확산 장벽(58)은 Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa_N, W, WN 또는 도전 물질이 그곳을 통과하여 확산되는 것을 방지하는 장벽으로서 기능할 수 있는 임의의 다른 물질을 포함한다. 확산 장벽(58)의 두께는 사용되는 피착 프로세스뿐만 아니라 사용되는 물질에 따라 변할 수 있다. 일반적으로, 확산 장벽(58)은 약 2nm에서 약 50nm의 두께를 가지며, 약 5nm에서 약 20nm의 두께가 더 일반적이다.

확산 장벽(58)은 예를 들어, 화학 기상 피착(CVD), 플라즈마 강화 화학 기상 피착(PECVD), 원자층 피착(ALD), 물리 기상 피착(PVD), 스퍼터링, 화학 용액 피착 및 도금을 포함하는 피착 프로세스에 의해 형성된다.

일부 실시예에 있어서, 선택적인 도금 시드층(도 2c 내에 구체적으로 도시되지 않음)은 확산 장벽(58)의 표면 상에서 형성될 수 있다. 확산 장벽(58) 상에서 연속적이고 직접적으로 형성되는 도전 물질의 경우에 있어서는, 선택적인 도금 시드층이 필요하지 않다. 선택적인

ng (56) completely passes the dielectric material and it can be extended. In another preferred embodiment, at least one opening (56) stops in the dielectric material (52) itself. Another operation ornamental seal characters, and the opening of the different depth can be formed.

At least one opening (56) may be the via aperture (via opening), and the line opening and/or the combined via / line opening (combined via/line opening). In the drawing 2b, each opening is for example illustrated as the line opening.

Next, as shown in Figure 2c, it is formed on exposed surfaces of the structure illustrated in Figure 2b in which the diffusion barrier (58) includes at least one opening in the inside according to the top surface of the hard mask (54) remaining.

The diffusion barrier (58) comprises the Ta, the TaN, the Ti, the TiN, the Ru, the RuN, the RuTa, the RuTa_N, W, WN, or the dissimilar material functioning as the obstacle which prevents it is diffused the conducting material passes through that place. It can change according to not only the deposition process where the thickness of the diffusion barrier (58) is used but also the used material. Generally, in the diffusion barrier (58) is about 2nm, it has the thickness of about 50nm and the thickness of about 20nm is more general in about 5nm.

The diffusion barrier (58) is formed by the deposition process including for example, the chemical vapor deposition (CVD), the plasma enhanced chemical vapor deposition (PECVD), the atomic layer deposition (ALD), the physical vapor sticking (PVD), the sputtering, the chemical solution deposition and plating.

As to the some embodiment, the selective plated seed layer (the drawing 2c, specifically, not shown) can be formed on the surface of the diffusion barrier (58). It has in case of the conducting material successive and which is directly formed on the diffusion barrier (58) and the selective pl

도금 시드층은 사전 선택된 도전 금속 또는 금속 합금의 연속적인 전기 도금(electroplating)을 선택적으로 촉진하기 위해 사용된다. 선택적인 도금 시드층은 Cu, Cu 합금, Ir, Ir 합금, Ru, Ru 합금(예를 들어, TaRu 합금) 또는 낮은 금속 도금 과전압(overpotential)을 가지는 임의의 다른 적절한 귀금속(noble metal) 또는 귀금속 합금을 포함할 수 있다. Cu 금속이 개구(56) 내에서 연속적으로 형성되는 경우, 일반적으로 Cu 또는 Cu 합금 도금 시드층이 사용된다.

선택적인 시드층의 두께는 선택적인 도금 시드층의 물질뿐만 아니라 이를 형성하는데 사용되는 기술에 따라 변할 수 있다. 일반적으로, 선택적인 도금 시드층은 약 2nm에서 약 80nm의 두께를 가진다.

선택적인 도금 시드층은, 예를 들어 CVD, PE CVD, ALD 및 PVD를 포함하는 종래의 피착 프로세스에 의해 형성될 수 있다.

(유전 물질(52) 내에서 도전 피처를 형성하는) 도전 물질(60)은, 예를 들어 도 2d에 도시된 구조체를 제공하는 적어도 확산 장벽으로 라이닝된 적어도 하나의 개구(56) 내에서 부분적으로 형성된다. 부분적으로 형성된 구조체를 생성하기 위해 시간 제어 프로세스가 수행된다. 도전 물질(60)은 다결정 규소, SiGe, 도전 금속, 적어도 하나의 도전 금속을 포함하는 합금, 도전 금속 규화물 또는 이들의 조합을 포함할 수 있다. 바람직하게는, 도전 물질(60)은 Cu, W, 또는 Al과 같은 도전 금속이며, Cu 또는 Cu 합금(예를 들어, AlCu)이 본 발명에 있어 보다 바람직하다.

도전 물질(60)은 적어도 하나의 개구(56)를 부분적으로 채우거나 또는 적어도 하나의 개구(56)를 전체적으로 채운 후, 도전 물질(60)을 유전 물질(52)의 상부 표면 아래 레벨로 리세

ated seed layer is not necessary. It is used the successive electroplating of the conductive metal in which the selective plated seed layer is pre-selected or the metal alloy is selectively promoted. The precious metal (noble metal) or the dissimilar proper noble metal alloy in which the selective plated seed layer has the Cu, the Cu alloy, the Ir, the Ir alloy, the Ru, the Ru alloy (for example, the TaRu alloy) or the low metal plating overvoltage (overpotential) is include might. Generally the Cu or the Cu alloy plated seed layer of the Cu metal is used in the opening (56) with case of being consecutively formed.

It can change according to not only the material of the plated seed layer in which the thickness of the selective seed layer is selective but also the technology which is used to form this. Generally, the selective plated seed layer has the thickness of about 80nm in about 2nm.

The selective plated seed layer is formed by the conventional deposition process including for example, CVD, PECVD, and ALD and PVD.

(The conductive feature is formed in the dielectric material (52)) The conducting material (60) is partly formed in at least one opening (56) lined to at least diffusion barrier providing the structure illustrated in Figure 2d for example. In order to produce the formed structure the time control process is partly performed. The conducting material (60) may include the alloy including the polycrystalline silicon, the SiGe, the conductive metal, at least one conductive metal, and the electric conduction metal silicide or their combination. Preferably, the conducting material (60) is Cu, and the conductive metal such as W and Al and the Cu or the Cu alloy (for example, the AlCu) is the be desirable than the invention.

After the conducting material (60) partly fills up at least one opening (56) or on the whole, at least one opening (56) is filled up it can be formed by recessing the conducting material (60) to the top surface

싱함으로써 형성될 수 있다. 화학 기상 피착(CVD), 플라즈마 강화 화학 기상 피착(PECVD), 스퍼터링, 화학 용액 피착 또는 도금을 포함하는, 적어도 하나의 개구를 바닥에서부터 위로 채우는 임의의 종래의 피착 프로세스가 사용될 수 있다. 바람직하게는, 상향식(bottom-up) 도금 프로세스가 사용된다.

리세싱 단계가 사용되는 경우, 도전 물질(60)의 부분을 선택적으로 제거하는 에칭 프로세스가 유전 물질(52) 내의 적어도 하나의 개구(56)를 부분적으로 채우기 위해 사용된다.

다음으로, 연마 정지층(planarization stop layer; 62)이 적어도 하나의 개구(56)의 남은 부분 내에서뿐만 아니라, 적어도 하나의 개구(56)의 외부로 연장되는 확산 장벽(58)(또는 선택적인 금속 시드층)의 위에서 형성된다. 연마 정지층(62)을 포함하는 결과 구조체(resultant structure)가, 예를 들어 도 2e에 도시된다. 연마 정지층(62)은, 예를 들어 탄화 규소, 질화 규소 및/또는 질소와 수소 도핑된 탄화규소와 같은 임의의 절연 물질 또는, 예를 들어 확산 장벽 속성을 갖는 순수형, 합금형 또는 질화형 Ta, Ru, Ir, W, Co, Ti 및/또는 Rh와 같은 임의의 금속 물질을 포함한다. 이와 같이, 연마 정지층(62)은 확산 장벽 속성을 갖는 절연 물질 또는 금속 물질로서 지칭될 수 있다.

연마 정지층(62)은, 이에 한정되는 것은 아니지만 CVD, PECVD, 증착, 화학 용액 피착, 스퍼터링 및 물리 기상 피착(PVD)을 포함하는 종래의 피착 프로세스에 의해 형성된다.

다음으로, 도 2f에 도시된 바와 같이, 예를 들어 화학 기계적 연마(chemical mechanical polishing; CMP) 및/또는 그라인딩(grinding)과 같은 연마 프로세스는 적어도 하나의 개

lower level of the dielectric material (52). The arbitrary conventional deposition process filled up can be at least one opening including the chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), sputtering, chemical solution deposition or plating used in the bottom surface. Preferably, the bottom-up plating process is used.

So that the etching process which selectively removes the case where the recessing step is used, and the part of the conducting material (60) partly fill up at least one opening (56) within the dielectric material (52) it is used.

Next, the polish stop layer (planarization stop layer: 62) is formed at the upper part of the diffusion barrier (58) (the metal seed layer which is or selective) in which it is extended to the outside of at least one opening (56) inside of the part of at least one opening (56) remains. The structure (resultant structure) is illustrated in for example, the drawing 2e as a result of including the polish stop layer (62). The polish stop layer (62) comprises for example, the silicon carbide, the arbitrary insulation material, like the A-doped silicon carbide the silicon nitride and/or nitrogen and hydrogen or the napiform having for example, the diffusion barrier attribute, the alloy type, or the arbitrary metal material like the nitride type Ta, the Ru, the Ir, W, the Co, the Ti and/or the Rh. In this way, it can be called as the insulation material or the metal material in which the polish stop layer (62) has the diffusion barrier attribute.

The polish stop layer (62) is formed by the conventional deposition process which is not thus restricted but includes the CVD, PECVD, the deposition, the chemical solution deposition, the sputtering and physical vapor sticking (PVD).

Next, as shown in FIG. 2f, for example, the grinding process like the chemical mechanical polishing (chemical mechanical polishing: CMP) and/or the grinding is used when the part of the polish stop layer (6

구(56)의 입구 위로 연장되는 연마 정지층(62)의 부분을 제거하는데 사용된다. 연마 단계 동안, 확산 장벽 및 하드 마스크는 유전 물질(52)의 상부, 수평 표면의 위로부터 제거된다. 이와 같이, 연마 프로세스는 (측벽 표면 및 바닥 표면 상의) U-형 확산 장벽과, 본 발명의 이 단계 동안 제거되지 않는 연마 정지층(62#39#)의 나머지 부분에 의해 완벽하게 둘러싸인 도전 물질(60)을 제공한다. 연마 장벽의 나머지 부분은 적어도 하나의 개구 내에 위치하며, 유전 물질(52)의 상부 표면과 동일 평면 상의 상부 표면을 가진다.

도 2f는 본 발명의 상호연결체를 도시한다. 도시된 바와 같이, 본 발명의 상호연결 구조체는 약 4.0 이하의 유전 상수를 갖는 유전 물질(52); 및 유전 물질(52) 내에 매립되는 측벽 표면들(60X), 바닥 표면(60Y) 및 상부 표면(60Z)을 갖는 도전 물질(60)을 포함하고, 도전 물질(60)의 상부 표면(60Z)은 유전 물질(52)의 상부 표면(52U) 아래에 위치한다. 본 발명의 상호연결 구조체는 또한 도전 물질(60)의 측벽 표면들(60X) 및 바닥 표면(60Y) 상에 위치하는 적어도 하나의 U-형 확산 장벽(58)을 포함한다. 본 발명의 상호연결 구조체는 또한 도전 물질(60)의 상부 표면(60Z) 상에 위치하는 확산 장벽 속성(62#39#)을 가지는 절연층 또는 금속층을 포함하며, 이러한 절연층 또는 금속층은 적어도 U-형 장벽의 상부 측벽 표면들과 접하는 에지 부분들(E)을 갖는, 확산 장벽 속성(62#39#)을 갖는다.

도 2g는 유전 캐핑층(64)이 도 2f에 도시된 구조체의 노출된 표면 상에서 형성되는 선택적인 실시예를 도시한다. 유전 캐핑층(64)은, 예

2) upwardly extended with the entrance of at least one opening (56) is removed. It first of all, the upper portion of the dielectric material (52), and the consolidation of the horizontal surface gets rid of the diffusion barrier and hard mask for the polishing step. In this way, the conducting material (60) in which the grinding process is completely surrounded with the remaining part of (on the side wall surface and bottom surface) U- type diffusion barrier, and the polishing stopping layer (62') which is not removed for the two-step of the invention is provided. The remaining part of the abrasive barrier has the top surface of the dielectric material (52) it is positioned within at least one opening and the same top surface on plane.

Figure 2f shows the interconnect of the invention. As shown in the figure, the mutual linking structure of the invention includes the dielectric material (52) having the dielectric constant less than about 4.0, and the conducting material (60) having the side wall surface (60X) reclaimed within the dielectric material (52), and the bottom surface (60Y) and top surface (60Z) and the top surface (60Z) of the conducting material (60) is positioned under the top surface (52U) of the dielectric material (52). The mutual linking structure of the invention includes moreover, the side wall surface (60X) of the conducting material (60) and at least one U- type diffusion barrier (58) located on surface the bottom surface (60Y). The mutual linking structure of the invention has such insulating layer or the metallic layer is upper sidewall surfaces of at least U- type obstacle the insulating layer or the metallic layer having the phase obstacle attribute (62') located on surface the top surface (60Z) of the conducting material (60) the moreover is included and the diffusion barrier attribute (62') having the edge area (E) contacting.

Figure 2g shows the selective embodiment which is formed on the exposed surface of the structure in which the heredity capping layer (64) Lee is illustrated in 2f. Th

를 들어, SiC, Si₄NH₃, SiO₂, 탄소 도핑된 산화물, 질소와 수소 도핑된 탄화 규소 SiC(N, H) 또는 이들의 복수층과 같은 임의의 적절한 유전 캐핑 물질을 포함한다. 예를 들어, 화학 기상 피착, 플라즈마 강화 화학 기상 피착, 화학 용액 피착, 증착 및 원자층 피착과 같은 임의의 종래의 피착 프로세스가 선택적인 유전 캐핑층(64)을 형성하는데 사용될 수 있다. 유전 캐핑층(64)의 두께는 이를 형성하는데 사용되는 기술뿐만 아니라 층의 구성 물질에 따라 변할 수 있다. 일반적으로, 유전 캐핑층(64)은 약 15nm에서 약 100nm의 두께를 가지며, 약 25nm에서 약 45nm의 두께가 더 일반적이다.

본 발명의 방법 동안, 도전 물질(60)과 유전 물질(52) 간에 직접적인 접촉은 없으며, 유전체의 표면 상에서 연장되는 도전 물질의 연마가 사용되지 않으므로, 도전성 잔류물이 형성되지 않는다. 상기 태양은 유전체 표면 상에 도전성 금속 잔여물(예를 들어, 결함)을 감소시키는데 현저한 효과를 가진다. 따라서, 본 발명의 방법은 대량으로 제조될 수 있는 신뢰성 있고 기술적으로 확장가능한 상호연결 구조체를 제공한다.

본 발명이 바람직한 실시예에 대해 구체적으로 도시되고 기술되었으나, 본 기술 분야의 당업자는 형태 및 세부사항에 대해 전술한 것의 변형 및 다른 변형이 본 발명의 사상과 범위를 벗어나지 않고 이루어질 수 있다는 것을 이해할 수 있다. 따라서, 본 발명은 기술되고 도시된 정확한 형태 및 세부사항에 한정되지 않으며 첨부된 특허청구범위의 범위 안에 포함된다.

the heredity capping layer (64) comprises for example, the SiC, the Si₄NH₃, the A-doped silicon carbide SiC(N,H) the SiO₂, the oxide which is carbon doped, and nitrogen and hydrogen, or the proper heredity capping agent like their multi-layer. For example, it can be used to form the heredity capping layer (64) in which the arbitrary conventional deposition process like the chemical vapor deposition, the plasma enhanced chemical vapor deposition, the chemical solution deposition, the deposition and atomic layer deposition is selective. It can change according to the configuration element of not only the technology which is used to the thickness of the heredity capping layer (64) form this but also the layer. Generally, in the heredity capping layer (64) is about 15nm, it has the thickness of about 100nm and the thickness of about 45nm is more general in about 25nm.

The direct contact does not have for the method of the invention between the conducting material (60) and dielectric material (52) and the grinding of the extended conducting material is not used on the surface of the dielectric. Therefore the conductive stringer is not formed. The conductive metal residue (for example, the deformity) is reduced on the dielectric surface but sun has the notable effect. Therefore, the mutual linking structure having with reliability and the method of the invention can be massively manufactured is technologically expandable is provided.

Was specifically illustrated and the invention was described about the preferred embodiment. But it can understand that deformation and the other deformation of in which the person skilled in the art of this technical field states above about the form and detail article can not deviate from thought and range of the present invention and deformation can be made. Therefore, it is included in the range of the patent claim which is attached while not being restricted to the correct form and the detail article in which the invention is describe

d and which is illustrated.

도면에 대한 간단한 설명

본 발명의 실시예는 첨부된 도면을 참조하여 오직 예시적인 방법으로 기술된다.

도 1a-1b는 (단면도를 통해) 선행기술의 상호 연결 구조체를 도시하는 도식적 도면. 도 1a는 Cu 누설을 도시하며, 도 1b는 Cu 잔류물을 도시함.

도 2a-2g는 (단면도를 통해) 높은 누설 저항을 가지며 유전 물질의 표면에서 금속성 잔류물이 존재하지 않는 매우 신뢰성 있고 기술적으로 확장가능한 상호연결 구조체를 제조하는 본 발명에 사용되는 기본 프로세스 단계를 도시하는 도식적 도면.

Brief explanation of the drawing

Referring to the figure, it is only described to the illustrative method the embodiment of the invention is attached.

Figure 1a-1b is a diagrammatic drawing showing the mutual linking structure of (through the cross-sectional view) prior art. The drawing 1a shows the Cu leakage and the drawing 1b shows the Cu residue.

Figure 2a-2g is a diagrammatic drawing showing the basis process step possible to be used in the present invention of manufacturing the mutual linking structure having with the reliability and the metallic residue is nonexistent on the surface of the dielectric material is technologically expandable while having the leak resistance high with (through the cross-sectional view).

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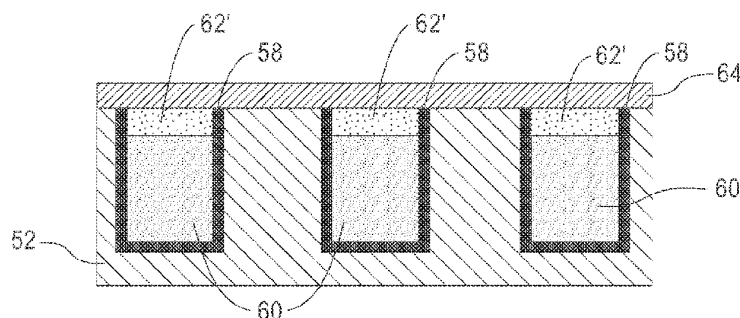


FIG. 2G

(57) Abstract: An interconnect structure is provided in which the conductive feature (i.e., conductive material) is not coplanar with the upper surface of the dielectric material, but instead the conductive material is recessed below an upper surface of the dielectric material. In addition to being recessed below the upper surface of the dielectric material, the conductive material of the interconnect structure is surrounded on all sides (i.e., sidewall surfaces, upper surface and bottom surface) by a diffusion barrier material. Unlike prior art interconnect structures, the barrier material located on the upper surface of the recessed conductive material is located with an opening including the recessed conductive material.

INTERCONNECT STRUCTURE WITH HIGH LEAKAGE RESISTANCE

Field of the Invention

5 The present invention relates to a semiconductor structure, and a method of fabricating the same. More particularly, the present invention relates to a semiconductor interconnect structure, and a method of fabricating the same, having a high leakage resistance as well as no metallic residues (e.g., defects) present at the upper surface of the interconnect dielectric.

10 The leakage resistance within an interconnect structure is improved, while avoiding the formation of metallic residues (e.g., defects) at the upper surface of the interconnect dielectric.

Background of the Invention

15 Generally, semiconductor devices include a plurality of circuits that form an integrated circuit (IC) fabricated on a semiconductor substrate. A complex network of signal paths will normally be routed to connect the circuit elements distributed on the surface of the substrate. Efficient routing of these signals across the device requires formation of multilevel or multilayered schemes, such as, for example, single or dual damascene wiring structures. The

20 wiring structure typically includes copper, Cu, or a Cu alloy since Cu-based interconnects provide higher speed signal transmission between large numbers of transistors on a complex semiconductor chip as compared with aluminum, Al,-based interconnects.

25 Within a typical interconnect structure, metal vias run perpendicular to the semiconductor substrate and metal lines run parallel to the semiconductor substrate. Further enhancement of the signal speed and reduction of signals in adjacent metal lines (known as "crosstalk") are achieved in today's IC product chips by embedding the metal lines and metal vias (e.g., conductive features) in a dielectric material having a dielectric constant of less than 4.0.

30 In current semiconductor interconnect structures, time-dependent-dielectric-breakdown (TDDB) has been identified as one of the major reliability concerns for future interconnect structures that include Cu-based metallurgy and low k dielectric materials. By "TDDB" it is

meant, that over time the dielectric material of the interconnect structure begins to fail. The failure of the dielectric material may be caused by intrinsic means or by defects that are formed on the surface of the interconnect dielectric material during the course of preparing the interconnect structure.

5

Leakage of metallic ions, particularly Cu ions, along the interconnect dielectric surface has been identified as the major intrinsic failure mechanism that attributes to TDDB. FIG. 1A is a prior art interconnect structure 10 which illustrates this intrinsic leakage phenomenon. Specifically, the prior art interconnect structure includes a dielectric material 12 having a Cu feature 14 embedded therein. The Cu feature 14 is typically separated from the dielectric material 14 by a diffusion barrier 16. A dielectric capping layer 18 is present on the surface of the dielectric material 14, the diffusion barrier 16 and the Cu feature 14. In FIG. 1A, the arrows designate the leakage (diffusion) of Cu ions from the conductive feature 14 which occurs along the upper surface of the interconnect structure as shown. Over time, this leakage of Cu ions results in TDDB as well as failure of the devices within the interconnect structure.

Another contributor to TDDB, which is illustrated in FIG. 1B, is defect related. Specifically, FIG. 1B is another prior art interconnect structure 10' including the components as shown in FIG. 1A in which Cu residues (e.g., defects) 20 are present at the interface between the upper surface of the dielectric material 12 and the dielectric capping layer 18. The Cu residues 20 are formed during the formation of the Cu features 14 (i.e., deposition and planarization of Cu within an opening formed into the dielectric material 12). Post planarization Cu residues, which provide defects at the surface of the dielectric material, are one of the root causes of time-dependent-dielectric-breakdown (TDDB) failure.

It is noted that although Cu is specifically mentioned with respect to the prior art interconnect structures mentioned above, the above leakage and defect problems occur (although at different rates and extents) with other types of conductive metals such as, for example Al and W.

30

In view of leakage problem illustrated in FIG. 1A, and the residues problem illustrated in FIG. 1B, there is a continued need for providing an interconnect structure in which metallic leakage, particularly, Cu ion diffusion, and metallic residues, particularly Cu residues, can both be reduced or completely eliminated from an interconnect structure.

5

Summary of the Invention

The present invention provides an interconnect structure that has high leakage resistance and no metallic residues present at the upper dielectric surface of a particular interconnect level of an interconnect structure. As such, the inventive interconnect structure exhibits an improved time-dependent-dielectric-breakdown (TDDB) as compared to prior art interconnect structures.

In the inventive interconnect structure, the conductive feature (i.e., conductive material) is not coplanar with the upper surface of the dielectric material, but instead the conductive material is recessed below an upper surface of the dielectric material. In addition to being recessed below the upper surface of the dielectric material, the conductive material of the inventive interconnect structure is surrounded on all sides (i.e., sidewall surfaces, upper surface and bottom surface) by a diffusion barrier material. The sidewall surfaces and the bottom surface of the recessed conductive material are lined with a U-shaped diffusion barrier. The upper surface of the recessed conductive material is lined with an insulating or metallic layer. Edge portions of the insulating or metallic layer lining the upper surface of the conductive material are in contact with upper sidewall surfaces of the U-shaped diffusion barrier or, if present, an optional plating seed layer. The insulating or metallic layer lining the upper surface of the recessed conductive material both have diffusion barrier properties. Since the recessed conductive material is completely surrounded by a diffusion barrier material, leakage of metallic ions at the surface of the dielectric material is substantially, if not completely, eliminated.

Unlike prior art interconnect structures, the barrier material located on the upper surface of the recessed conductive material is located with an opening including the recessed conductive material in the present inventive interconnect structure. In prior art interconnect

structures, any barrier layer formed atop the conductive feature (i.e. conductive material) is present atop, e.g., spanning, the opening, not within the opening containing the conductive material as is the case in the inventive interconnect structure.

5 It is further noted that in the present interconnect structure there is no direct contact between the recessed conductive material and the dielectric material and no planarization of the conductive material extending on the surface of the dielectric material is employed as such no conductive residues are formed at the upper surface of the interconnect dielectric material as is the case with prior art interconnect structures. The above features have a significant
10 benefit on substantially reducing or even eliminating conductive metal residues (e.g., defects) on the dielectric surface. As such, the present invention provides a reliable and technology extendible interconnect structure that can be fabricated in high volumes.

In general terms, the interconnect structure of the present invention comprises:

15 a dielectric material having a dielectric constant of about 4.0 or less;

a conductive material having sidewall surfaces, a bottom surface and an upper surface
20 embedded within said dielectric material, wherein said upper surface of said conductive material is located beneath an upper surface of the dielectric material;

at least a U-shaped diffusion barrier located on said sidewall surfaces and said bottom surface of said conductive material; and

25 an insulating or metallic layer having diffusion barrier properties located on said upper surface of said conductive material, said insulating or metallic layer having diffusion barrier properties having edge portions that are in contact with upper sidewall surfaces of at least said U-shaped barrier.

30 In some embodiments of the interconnect structure of the present invention, a dielectric capping layer is also present and is located on the upper surface of the dielectric material and an upper surface of the insulating or metallic layer having diffusion barrier properties. In

such an embodiment, the dielectric capping layer may comprise one of SiC, Si₃N₄, SiO₂, a carbon doped oxide, and a nitrogen and hydrogen doped silicon carbide SiC(N,H).

5 In a further embodiment of the inventive interconnect structure, the dielectric material, which may be porous or non-porous, may comprise one of SiO₂, a silsesquioxane, a C doped oxide including atoms of Si, C, O and H, and a thermosetting polyarylene ether.

10 In a yet further embodiment of the present invention, the U-shaped diffusion barrier within the inventive interconnect structure may comprise Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa₂N, W or WN.

15 In another embodiment of the inventive interconnect structure, a U-shaped plating seed layer is also present and is located between the at least one conductive material and the U-shaped diffusion barrier. In this instance, the edge portions of the insulating or metallic layer are in direct contact with the upper sidewall surface of the U-shaped plating seed layer. The U-shaped plating seed layer is used when the conductive material is formed by a plating process. When present, the U-shaped plating seed layer may comprise Cu, a Cu alloy, Ir, an Ir alloy, Ru or a Ru alloy.

20 In still another embodiment of the inventive interconnect structure, the at least one conductive material may comprises Cu, W or Al in pure or alloyed form.

In a preferred embodiment of the invention, an interconnect structure is provided that comprises:

25 a dielectric material having a dielectric constant of about 4.0 or less;

30 a copper-containing conductive material having sidewall surfaces, a bottom surface and an upper surface embedded within said dielectric material, wherein said upper surface of said copper-containing conductive material is located beneath an upper surface of the dielectric material;

at least a U-shaped diffusion barrier located on said sidewall surfaces and said bottom surface of said copper-containing conductive material; and

5 an insulating or metallic layer having diffusion barrier properties located on said upper surface of said conductive material, said insulating or metallic layer having diffusion barrier properties having edge portions that are in contact with at least upper sidewall surfaces of at least said U-shaped barrier.

10 In some embodiments of the preferred interconnect structure of the present invention, a dielectric capping layer is also present and is located on the upper surface of the dielectric material and an upper surface of the insulating or metallic layer having diffusion barrier properties. In such an embodiment, the dielectric capping layer may comprise one of SiC, Si₃NH₃, SiO₂, a carbon doped oxide, and a nitrogen and hydrogen doped silicon carbide SiC(N,H).

15 In a further embodiment of the preferred interconnect structure, the dielectric material, which may be porous or non-porous, may comprise one of SiO₂, a silsesquioxane, a C doped oxide including atoms of Si, C, O and H, and a thermosetting polyarylene ether.

20 In a yet further embodiment of the preferred interconnect structure, the U-shaped diffusion barrier within the inventive interconnect structure may comprise Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa₂N, W or WN.

25 In another embodiment of the preferred interconnect structure, a U-shaped plating seed layer is also present and is located between the conductive material and the U-shaped diffusion barrier. In this instance, the edge portions of the insulating or metallic layer are in direct contact with the upper sidewall surface of the U-shaped plating seed layer. The U-shaped plating seed layer is used when the copper-containing conductive material is formed by a plating process. When present the U-shaped plating seed layer may comprise Cu, a Cu
30 alloy, Ir, an Ir alloy, Ru or a Ru alloy.

In addition to the interconnect structures mentioned above, the present invention also provides a method of fabricating the same.

5 forming at least one opening into a dielectric material having a dielectric constant of about 4.0 or less, said dielectric material having a patterned hard mask located on an upper surface thereof;

lining the at least one opening and the patterned hard mask with a diffusion barrier;

10 partially filling the at least one opening with a conductive material, said conductive material having an upper surface that is located beneath an upper surface of said dielectric material;

15 forming an insulating or metallic material having diffusion barrier properties within the at least one opening and on the upper surface of said conductive material as well as atop the diffusion barrier lining the patterned hard mask; and

20 removing a portion of the insulating or metallic material having diffusion barrier properties and the diffusion barrier and the patterned hard mask that lay above the upper surface of the dielectric material, while maintaining another portion of the insulating or metallic material having diffusion barrier properties within said at least one opening and forming a U-shaped diffusion barrier within said at least one opening, wherein said another portion of the insulating or metallic material having diffusion barrier properties has an upper surface that is coplanar with the upper surface of the dielectric material, and said conductive material is completely surrounded by the U-shaped diffusion barrier located on sidewall surfaces and a
25 bottom surface of said conductive material, and said another portion of the insulating material having diffusion barrier properties located on the upper surface of the conductive material.

30 In one embodiment of the inventive method, a dielectric capping layer is formed on the upper surface of the dielectric material and on an upper surface of the another portion of the insulating or metallic material having diffusion barrier properties that remains in the at least

one opening. When present, the dielectric capping layer may comprise one of SiC, Si₃NH₃, SiO₂, a carbon doped oxide, and a nitrogen and hydrogen doped silicon carbide SiC(N,H).

5 In another embodiment of the inventive method, the diffusion barrier may comprises Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTa₂N, W or WN, and is formed by chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, physical vapor deposition, sputtering, chemical solution deposition and plating.

10 In yet another embodiment of the inventive method, a plating seed layer is formed between the conductive material and the diffusion barrier, and the plating seed layer may comprise Cu, a Cu alloy, Ir, an Ir alloy, Ru or a Ru alloy. In embodiments wherein a plating seed layer is employed, the plating seed layer is formed by chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition or physical vapor deposition.

15 In a further embodiment of the inventive method, the conductive material may comprise Cu, W or Al in pure or alloyed form.

20 In a still further embodiment of the inventive method, the partially filing the at least one opening with the conductive material comprises a deposition process selected from chemical vapor deposition, sputtering, chemical solution deposition and plating.

25 In an even further embodiment of the present invention, the partially filing the at least one opening with the conductive material comprises completely filling the at least one opening with the conductive material and recessing.

In still an even further embodiment of the inventive method, the removing step comprises chemical mechanical polishing.

Brief Description of the Drawings

30 Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings in which:

FIGS. 1A-1B are pictorial representations (through cross sectional views) depicting prior art interconnect structures. FIG. 1A shows Cu leakage, while FIG. 1B shows Cu residues; and

FIGS. 2A-2G are pictorial representations (through cross sectional views) depicting the basic process steps that are employed in the present invention in fabricating a highly reliable and technology extendible interconnect structure having a high leakage resistance and no metallic residues present at the surface of the dielectric material.

Detailed Description of the Invention

The present invention, which provides an interconnect structure having high leakage resistance and no metallic residues present at the surface of the dielectric material and a method of fabricating the same, will now be described in greater detail by referring to the following discussion and drawings that accompany the present application. It is noted that the drawings of the present application are provided for illustrative purposes only and, as such, the drawings are not drawn to scale.

In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to provide a thorough understanding of the present invention. However, it will be appreciated by one of ordinary skill in the art that the invention may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the invention.

It will be understood that when an element as a layer, region or substrate is referred to as being "on" or "over" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" or "directly over" another element, there are no intervening elements present. It will also be understood that when an element is referred to as being "connected" or "coupled" to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly

connected” or “directly coupled” to another element, there are no intervening elements present.

As stated above, the present invention provides an interconnect structure having high
5 leakage resistance and no metallic residues present at the surface of the dielectric material and a method of fabricating the same. The inventive interconnect structure exhibits improved TDDb than prior art invention structures.

In the inventive interconnect structure, the conductive feature (i.e., conductive material) is
10 not coplanar with the upper surface of the dielectric material, but instead the conductive material is recessed below an upper surface of the dielectric material. In addition to being recessed below the upper surface of the dielectric material, the conductive material of the inventive interconnect structure is surrounded on all sides (i.e., sidewall surfaces, upper
15 surface and bottom surface) by a diffusion barrier material. The sidewall surfaces and the bottom surface of the recessed conductive material within the opening are lined with a U-shaped diffusion barrier. The upper surface of the recessed conductive material is lined with an insulating or metallic layer, both of which have diffusion barrier properties. Edge
20 portions of the insulating or metallic layer lining the upper surface of the conductive material are in contact with upper sidewall surfaces of the U-shaped diffusion barrier or, if present, an optional U-shaped plating seed layer.

It is further noted that in the present application there is no direct contact between the recessed conductive material and the dielectric material and no planarization of the
25 conductive material extending on the surface of the interconnect dielectric is employed as such no conductive residues are formed at the upper surface of the interconnect structure as is the case with prior art interconnect structures. The above features have a significant benefit on reducing conductive metal residues (e.g., defects) on the dielectric surface.

Reference is now made to FIGS. 2A-2G which illustrate the basic processing steps that are
30 used in forming the semiconductor interconnect structure of the present invention. FIG. 2A illustrates an initial structure 50 that comprises a dielectric material 52 and a hard mask 54 located on a surface of the dielectric material 52.

The initial structure 50, i.e., the dielectric material 52, may be located upon a substrate (not shown in the drawings of the present application). The substrate, which is not shown, may comprise a semiconducting material, an insulating material, a conductive material or any combination thereof. When the substrate is comprised of a semiconducting material, any semiconductor such as Si, SiGe, SiGeC, SiC, Ge alloys, GaAs, InAs, InP and other III/V or II/VI compound semiconductors may be used. In addition to these listed types of semiconducting materials, the present invention also contemplates cases in which the semiconductor substrate is a layered semiconductor such as, for example, Si/SiGe, Si/SiC, silicon-on-insulators (SOIs) or silicon germanium-on-insulators (SGOIs).

When the substrate is an insulating material, the insulating material can be an organic insulator, an inorganic insulator or a combination thereof including multilayers. When the substrate is a conducting material, the substrate may include, for example, polySi, an elemental metal, alloys of elemental metals, a metal silicide, a metal nitride or combinations thereof including multilayers. When the substrate comprises a semiconducting material, one or more semiconductor devices such as, for example, complementary metal oxide semiconductor (CMOS) devices can be fabricated thereon. When the substrate comprises a combination of an insulating material and a conductive material, the substrate may represent a first interconnect level of a multilayered interconnect structure.

The dielectric material 52 comprises any interlevel or intralevel dielectric including inorganic dielectrics or organic dielectrics. The dielectric material 52 may be porous or non-porous. Some examples of suitable dielectrics that can be used as the dielectric material 52 include, but are not limited to: SiO₂, silsesquioxanes, C doped oxides (i.e., organosilicates) that include atoms of Si, C, O and H, thermosetting polyarylene ethers, or multilayers thereof. The term "polyarylene" is used in this application to denote aryl moieties or inertly substituted aryl moieties which are linked together by bonds, fused rings, or inert linking groups such as, for example, oxygen, sulfur, sulfone, sulfoxide, carbonyl and the like.

The dielectric material 52 typically has a dielectric constant that is about 4.0 or less, with a dielectric constant of about 2.8 or less being even more typical. All dielectric constants mentioned herein are relative to a vacuum, unless otherwise noted. These dielectrics

generally have a lower parasitic cross talk as compared with dielectric materials that have a higher dielectric constant than 4.0. The thickness of the dielectric material 52 may vary depending upon the dielectric material used as well as the exact number of dielectrics layers within the dielectric material 52. Typically, and for normal interconnect structures, the dielectric material 52 has a thickness from about 50 to about 1000 nm.

As mentioned above, the initial structure 50 also includes a hard mask 54 located on an upper surface of dielectric material 52. The hard mask 54 comprises an oxide, a nitride, an oxynitride or any multilayered combination thereof. In one embodiment, the hard mask 54 is an oxide such as silicon dioxide, while in another embodiment the hard mask 54 is a nitride such as silicon nitride.

The hard mask 54 is formed utilizing a conventional deposition process including, for example, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), chemical solution deposition, evaporation, and physical vapor deposition (PVD). Alternatively, the hard mask 54 may be formed by one of thermal oxidation, and thermal nitridation.

The thickness of the hard mask 54 employed in the present invention may vary depending on the material of the hard mask itself as well as the techniques used in forming the same. Typically, the hard mask 54 has a thickness from about 5 to about 100 nm, with a thickness from about 10 to about 80 nm being even more typical.

Next, and as shown in FIG. 2B, at least one opening 56 is formed into the hard mask 54 and the dielectric material 54 utilizing lithography and etching. The lithographic process includes forming a photoresist (not shown) atop the hard mask 54, exposing the photoresist to a desired pattern of radiation and developing the exposed photoresist utilizing a conventional resist developer. The etching process includes a dry etching process (such as, for example, reactive ion etching, ion beam etching, plasma etching or laser ablation), and/or a wet chemical etching process. Typically, reactive ion etching is used in providing the at least one opening 56. Typically, the etching process includes a first pattern transfer step in which the pattern provided to the photoresist is transferred to the hard mask 54, the patterned

photoresist is then removed by an ashing step, and thereafter, a second pattern transfer step is used to transfer the pattern from the patterned hard mask into the underlying dielectric material.

5 The depth of the at least one opening 56 that is formed into the dielectric material 54 (measured from the upper surface of the dielectric material to the bottom wall of the opening) may vary and it not critical to the present application. In some embodiments, the at least one opening 56 may extend entirely through the dielectric material. In yet other
10 embodiments, the at least one opening 56 stops within the dielectric material 52 itself. In yet further embodiments, different depth openings can be formed.

It is further observed that the at least one opening 56 may be a via opening, a line opening, and/or combined via/line opening. In FIG. 2B, and by way of an example, each of the openings is shown as line openings.

15

Next, as shown in FIG. 2C, a diffusion barrier 58 is formed on all exposed surfaces of the structure shown in FIG. 2B including within the at least one opening (i.e., on sidewalls and the bottom wall of each of the openings) and along the upper surface of remaining hard mask 54.

20

The diffusion barrier 58 comprises Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W, WN or any other material that can serve as a barrier to prevent a conductive material from diffusing there through. The thickness of the diffusion barrier 58 may vary depending on the deposition process used as well as the material employed. Typically, the diffusion barrier 58
25 has a thickness from about 2 to about 50 nm, with a thickness from about 5 to about 20 nm being more typical.

The diffusion barrier 58 is formed by a deposition process including, for example, chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), atomic
30 layer deposition (ALD), physical vapor deposition (PVD), sputtering, chemical solution deposition and plating.

In some embodiments, an optional plating seed layer (not specifically shown within FIG. 2C) can be formed on the surface of the diffusion barrier 58. In cases in which the conductive material to be subsequently and directly formed on the diffusion barrier 58, the optional plating seed layer is not needed. The optional plating seed layer is employed to selectively promote subsequent electroplating of a pre-selected conductive metal or metal alloy. The optional plating seed layer may comprise Cu, a Cu alloy, Ir, an Ir alloy, Ru, a Ru alloy (e.g., TaRu alloy) or any other suitable noble metal or noble metal alloy having a low metal-plating overpotential. Typically, Cu or a Cu alloy plating seed layer is employed, when a Cu metal is to be subsequently formed within the openings 56.

The thickness of the optional seed layer may vary depending on the material of the optional plating seed layer as well as the technique used in forming the same. Typically, the optional plating seed layer has a thickness from about 2 to about 80 nm.

The optional plating seed layer can be formed by a conventional deposition process including, for example, CVD, PECVD, ALD, and PVD.

A conductive material 60 (forming a conductive feature within the dielectric material 52) is partially formed within the at least one opening 56 that is now lined with at least diffusion barrier providing the structure shown, for example, in FIG. 2D. A time-controlled process is performed to result in the partially formed structure. The conductive material 60 may comprise polySi, SiGe, a conductive metal, an alloy comprising at least one conductive metal, a conductive metal silicide or combinations thereof. Preferably, the conductive material 60 is a conductive metal such as Cu, W or Al, with Cu or a Cu alloy (such as AlCu) being highly preferred in the present invention.

The conductive material 60 may be formed by partially filling the at least one opening 56 or by fully filling the at least one opening 56 and then recessing the conductive material 60 to a level below the upper surface of the dielectric material 52. Any conventional deposition process including chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), sputtering, chemical solution deposition or plating that fills the at least

one opening from the bottom upwards can be used. Preferably, a bottom-up plating process is employed.

5 When a recess step is employed, an etching process that selectively removes portions of the conductive material 60 is used to provide partial filling of the at least one opening 56 in the dielectric material 52.

10 Next, a planarization stop layer 62 is formed within the remaining portion of the at least one opening 56 as well as atop the diffusion barrier 58 (or optional metal seed layer) that extends outside of the at least one opening 56. The resultant structure including the planarization stop layer 62 is shown, for example, in FIG. 2E. The planarization stop layer 62 comprises any insulating material such as, for example, silicon carbide, silicon nitride, and/or a nitrogen and hydrogen doped silicon carbide or any metallic material such as, for example, Ta, Ru, Ir, W, Co, Ti and/or Rh in pure, alloyed or nitrided forms which have diffusion
15 barrier properties. As such, the planarization stop layer 62 may be referred to as an insulating or metallic material having diffusion barrier properties.

The planarization stop layer 62 is formed by a conventional deposition process including, but not limited to CVD, PECVD, evaporation, chemical solution deposition, sputtering, and
20 physical vapor deposition (PVD).

Next, and as is illustrated in FIG. 2F, a planarization process such as, for example, chemical mechanical polishing (CMP) and/or grinding, is employed to remove portions of the planarization stop layer 62 that extend above the mouth of the at least one opening 56. It is
25 noted that during the planarization step the diffusion barrier and the hard mask are removed from atop the upper, horizontal surface of the dielectric material 52. As such, the planarization process provides a conductive material 60 that is completely surrounded by a U-shaped diffusion barrier (on the sidewall surfaces and bottom surface) and by the remaining portion of planarization stop layer 62' that was not removed during this step of the
30 present invention. The remaining portion of the planarization stop layer is located within the at least one opening and it has an upper surface that is coplanar with the upper surface of the dielectric material 52.

It is emphasized that FIG. 2F illustrates the inventive interconnect of the present invention. As shown, the inventive interconnect structure includes dielectric material 52 having a dielectric constant of about 4.0 or less; and a conductive material 60 having sidewall surfaces 60X, a bottom surface 60Y and an upper surface 60Z embedded within dielectric material 52, wherein the upper surface 60Z of the conductive material 60 is located beneath the upper surface 52U of the dielectric material 52. The inventive interconnect structure also includes at least a U-shaped diffusion barrier 58 located on said sidewall surfaces 60X and said bottom surface 60Y of the conductive material 60. The inventive interconnect structure also includes an insulating or metallic layer having diffusion barrier properties 62' located on the upper surface 60Z of the conductive material 60, said insulating or metallic layer having diffusion barrier properties 62' having edge portions E that are in contact with upper sidewall surfaces of at least said U-shaped barrier.

FIG. 2G illustrates an optional embodiment in which a dielectric capping layer 64 is formed on the exposed surfaces of the structure shown in FIG. 2F. The dielectric capping layer 64 comprises any suitable dielectric capping material such as, for example, SiC, Si₃NH₃, SiO₂, a carbon doped oxide, a nitrogen and hydrogen doped silicon carbide SiC(N,H) or multilayers thereof. Any conventional deposition process such as, for example, chemical vapor deposition, plasma enhanced chemical vapor deposition, chemical solution deposition, evaporation, and atomic layer deposition may be used in forming the optional dielectric capping layer 64. The thickness of the dielectric capping layer 64 may vary depending on the technique used to form the same as well as the material make-up of the layer. Typically, the dielectric capping layer 64 has a thickness from about 15 to about 100 nm, with a thickness from about 25 to about 45 nm being more typical.

It is noted that during the method of the invention, no direct contact between the conductive material 60 and the dielectric material 52 is made and no planarization of a conductive material extending on the surface of the dielectric is employed as such no conductive residues are formed. The above features have a significant benefit on reducing conductive metal residues (e.g., defects) on the dielectric surface. As such, the inventive method provides a reliable and technology extendible interconnect structure that can be fabricated in high volumes.

While the present invention has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present invention. It is therefore intended that the present invention
5 not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

CLAIMS

1. An interconnect structure comprising:
 - a dielectric material having a dielectric constant of about 4.0 or less;
 - 5 a conductive material having sidewall surfaces, a bottom surface and an upper surface embedded within said dielectric material, wherein said upper surface of said conductive material is located beneath an upper surface of the dielectric material;
 - at least a U-shaped diffusion barrier located on said sidewall surfaces and said bottom surface of said conductive material; and
 - 10 an insulating or metallic layer having diffusion barrier properties located on said upper surface of said conductive material, said insulating or metallic layer having diffusion barrier properties having edge portions that are in contact with upper sidewall surfaces of at least said U-shaped barrier.
- 15 2. The interconnect structure of Claim 1 further comprising a dielectric capping layer located on said upper surface of said dielectric material and an upper surface of said insulating or metallic layer having diffusion barrier properties.
- 20 3. The interconnect structure of Claim 2 wherein said dielectric capping layer comprises one of SiC, Si₃NH₃, SiO₂, a carbon doped oxide, and a nitrogen and hydrogen doped silicon carbide SiC(N,H).
- 25 4. The interconnect structure of any preceding Claims wherein said dielectric material comprises one of SiO₂, a silsesquioxane, a C doped oxide including atoms of Si, C, O and H, and a thermosetting polyarylene ether.
5. The interconnect structure of any preceding Claims wherein said U-shaped diffusion barrier comprises Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W or WN.
- 30 6. The interconnect structure of any preceding Claims further comprises a U-shaped plating seed layer located between said conductive material and said U-shaped diffusion

barrier, said U-shaped plating seed layer comprises Cu, a Cu alloy, Ir, an Ir alloy, Ru or a Ru alloy.

7. The interconnect structure of any preceding Claims wherein said conductive material
5 comprises Cu, W or Al in pure or alloyed form.

8. The interconnect structure of any preceding Claims wherein said insulating or
metallic material having diffusion barrier properties comprises one of silicon carbide, silicon
nitride, a nitrogen and hydrogen doped silicon carbide, and a metallic material selected from
10 Ta, Ru, Ir, W, Co, Ti and Rh in pure, alloyed or nitrided forms.

9. An interconnect structure comprising:
a dielectric material having a dielectric constant of about 4.0 or less;
a copper-containing conductive material having sidewall surfaces, a bottom surface
15 and an upper surface embedded within said dielectric material, wherein said upper surface of
said copper-containing conductive material is located beneath an upper surface of the
dielectric material;
at least a U-shaped diffusion barrier located on said sidewall surfaces and said
bottom surface of said copper-containing conductive material; and
20 an insulating or metallic layer having diffusion barrier properties located on said
upper surface of said conductive material, said insulating or metallic layer having diffusion
barrier properties having edge portions that are in contact with at least upper sidewall
surfaces of at least said U-shaped barrier.

10. The interconnect structure of Claim 9 further comprising a dielectric capping layer
25 located on said upper surface of said dielectric material and an upper surface of said
insulating or metallic layer having diffusion barrier properties.

11. The interconnect structure of Claim 10 wherein said dielectric capping layer
30 comprises one of SiC, Si₃N₄, SiO₂, a carbon doped oxide, and a nitrogen and hydrogen
doped silicon carbide SiC(N,H).

12. The interconnect structure of any Claims 9 to 11 wherein said dielectric material comprises one of SiO₂, a silsesquioxane, a C doped oxide including atoms of Si, C, O and H, and a thermosetting polyarylene ether.

5 13. The interconnect structure of any of Claims 9 to 12 wherein said U-shaped diffusion barrier comprises Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W or WN.

10 14. The interconnect structure of any of Claims 9 to 13 further comprises a U-shaped plating seed layer located between said conductive material and said U-shaped diffusion barrier, said U-shaped plating seed layer comprises Cu, A Cu alloy, Ir, an Ir alloy, Ru or a Ru alloy.

15 15. The interconnect structure of any of Claims 9 to 14 wherein said insulating or metallic material having diffusion barrier properties comprises one of silicon carbide, silicon nitride, a nitrogen and hydrogen doped silicon carbide and a metallic material selected from Ta, Ru, Ir, W, Co, Ti and Rh in pure, alloyed or nitrided forms.

20 16. A method of forming an interconnect structure comprising:
forming at least one opening into a dielectric material having a dielectric constant of about 4.0 or less, said dielectric material having a patterned hard mask located on an upper surface thereof;

25 lining the at least one opening and the patterned hard mask with a diffusion barrier;
partially filling the at least one opening with a conductive material, said conductive material having an upper surface that is located beneath an upper surface of said dielectric material;

forming an insulating or metallic material having diffusion barrier properties within the at least one opening and on the upper surface of said conductive material as well as atop the diffusion barrier lining the patterned hard mask; and

30 removing a portion of the insulating or metallic material having diffusion barrier properties and the diffusion barrier and the patterned hard mask that lay above the upper surface of the dielectric material, while maintaining another portion of the insulating or metallic material having diffusion barrier properties within said at least one opening and

forming a U-shaped diffusion barrier within said at least one opening, wherein said another portion of the insulating or metallic material having diffusion barrier properties has an upper surface that is coplanar with the upper surface of the dielectric material, and said conductive material is completely surrounded by the U-shaped diffusion barrier located on sidewall surfaces and a bottom surface of said conductive material, and said another portion of the insulating material having diffusion barrier properties located on the upper surface of the conductive material.

17. The method of Claim 16 further comprising forming a dielectric capping layer on said upper surface of said dielectric material and on an upper surface of the another portion of the insulating or metallic material having diffusion barrier properties that remains in said at least one opening.

18. The method of Claim 16 or Claim 17 wherein said diffusion barrier comprises Ta, TaN, Ti, TiN, Ru, RuN, RuTa, RuTaN, W or WN.

19. The method of any of Claims 16 to 18 wherein said diffusion barrier is formed by chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition, physical vapor deposition, sputtering, chemical solution deposition and plating.

20. The method of any of Claims 16 to 19 further comprises a forming a plating seed layer located between said conductive material and said diffusion barrier, said plating seed layer comprises Cu, A Cu alloy, Ir, an Ir alloy, Ru or a Ru alloy.

21. The method of Claim 20 wherein said plating seed layer is formed by chemical vapor deposition, plasma enhanced chemical vapor deposition, atomic layer deposition or physical vapor deposition.

22. The method of any of Claims 16 to 21 wherein said conductive material comprises Cu, W or Al in pure or alloyed form.

23. The method of any of Claims 16 to 22 wherein said partially filing the at least one opening with the conductive material comprises a deposition process selected from chemical vapor deposition, sputtering, chemical solution deposition and plating.

5 24. The method of any of Claims 16 to 23 wherein said partially filing the at least one opening with the conductive material comprises completely filling the at least one opening with said conductive material and recessing.

10 25. The method of Claim 16 to 24 wherein said insulating or metallic material having diffusion barrier properties comprises one of silicon carbide, silicon nitride, a nitrogen and hydrogen doped silicon carbide and a metallic material selected from Ta, Ru, Ir, W, Co, Ti and Rh in pure, alloyed or nitrated forms.

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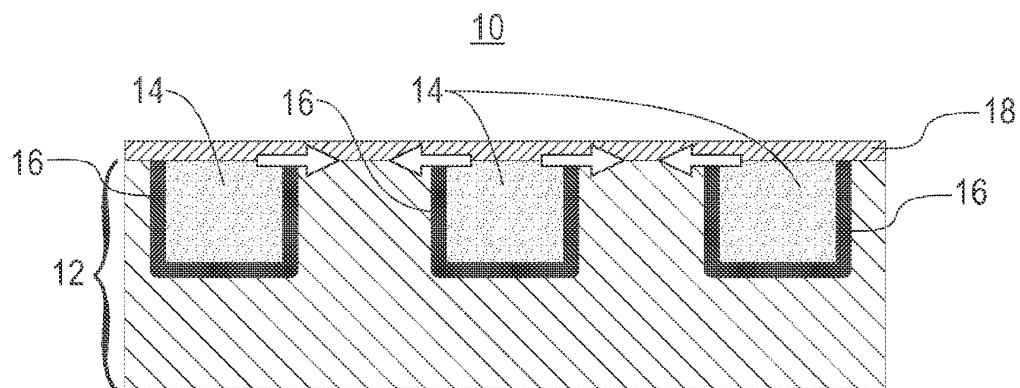


FIG. 1A
Prior Art

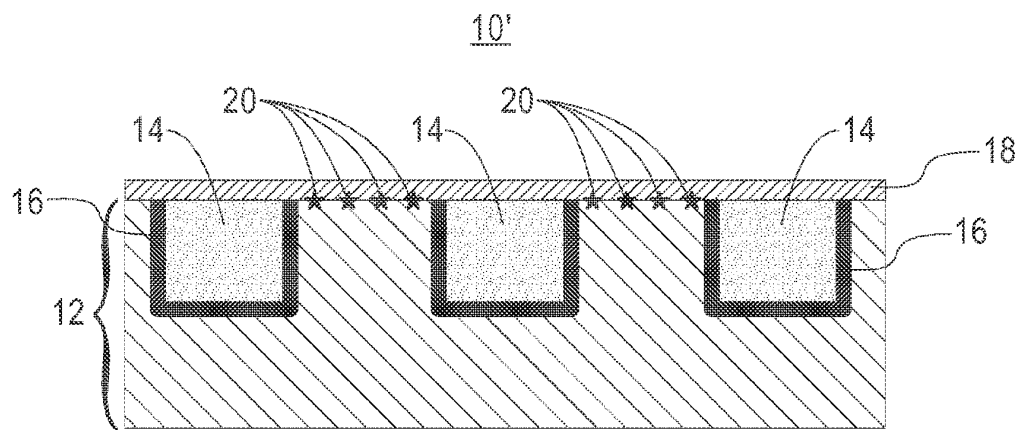


FIG. 1B
Prior Art

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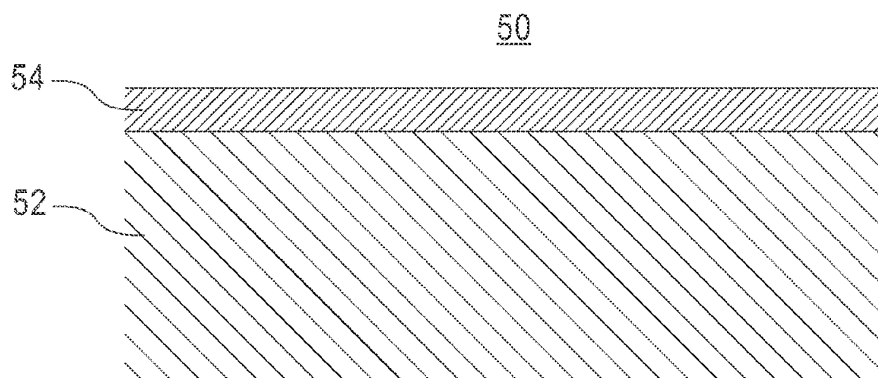


FIG. 2A

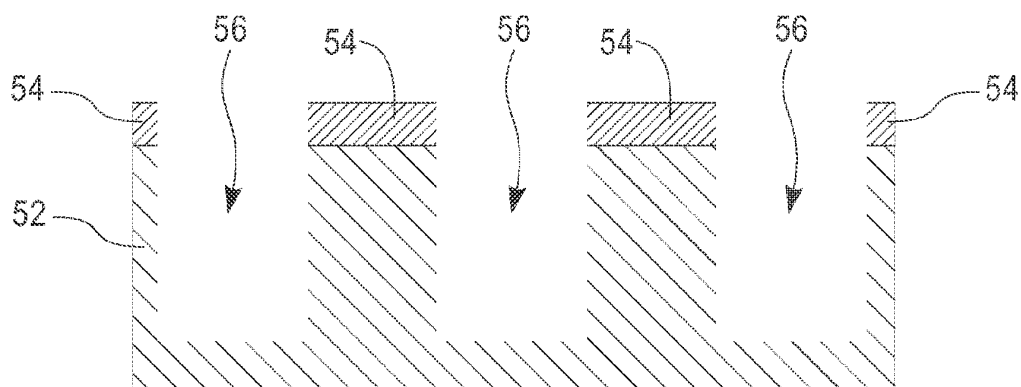


FIG. 2B

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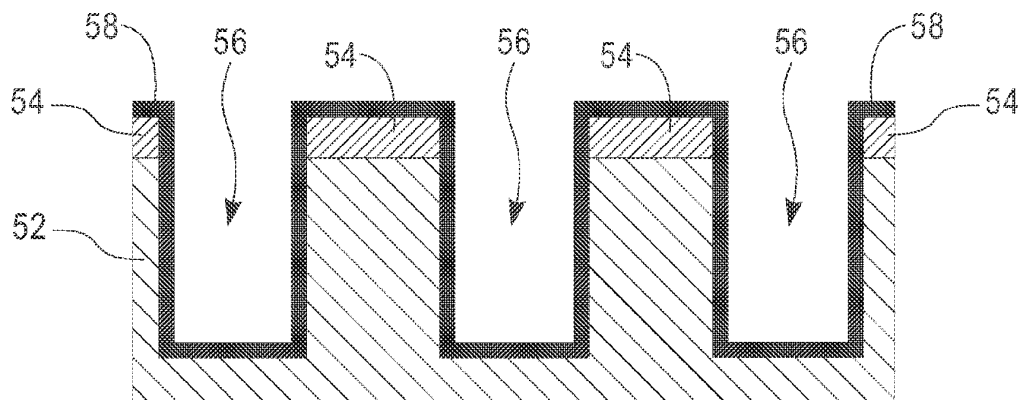


FIG. 2C

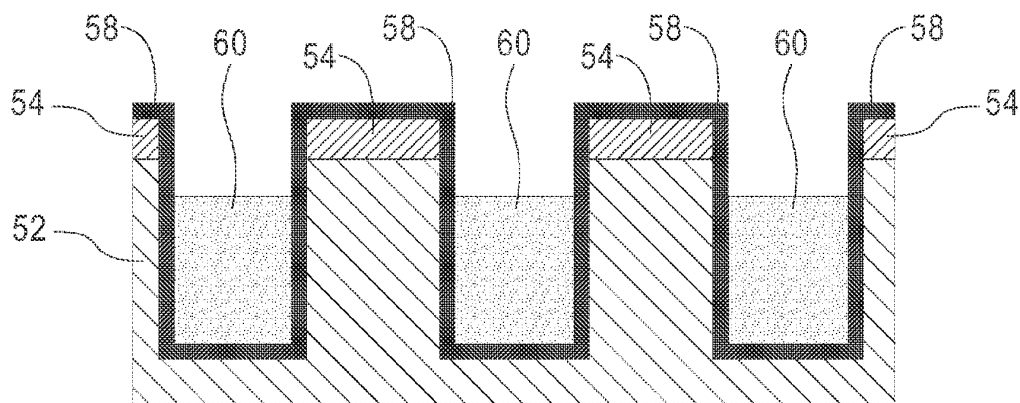


FIG. 2D

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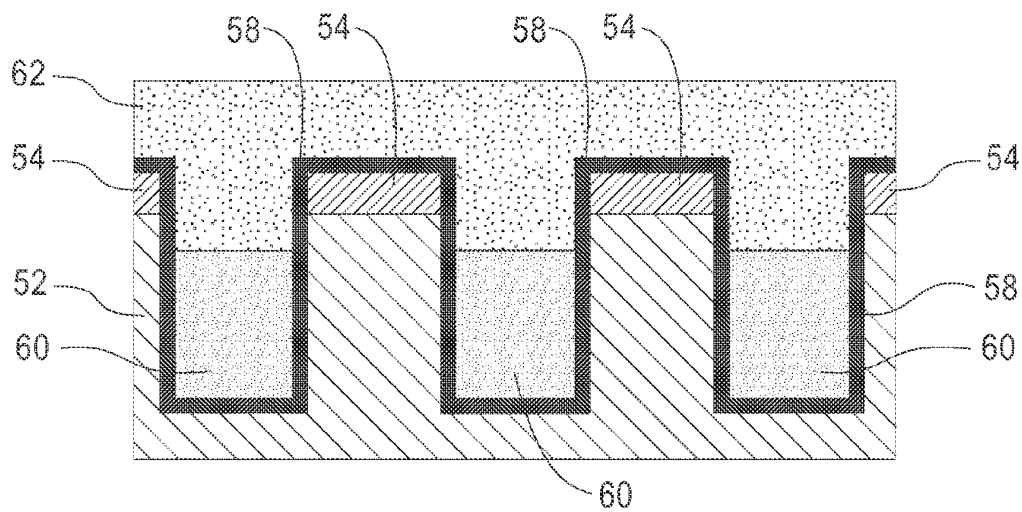


FIG. 2E

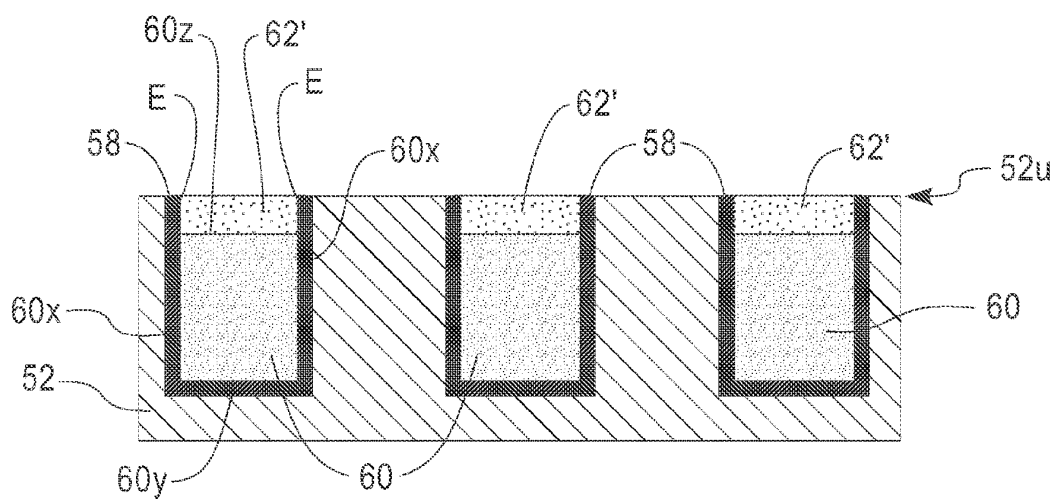


FIG. 2F

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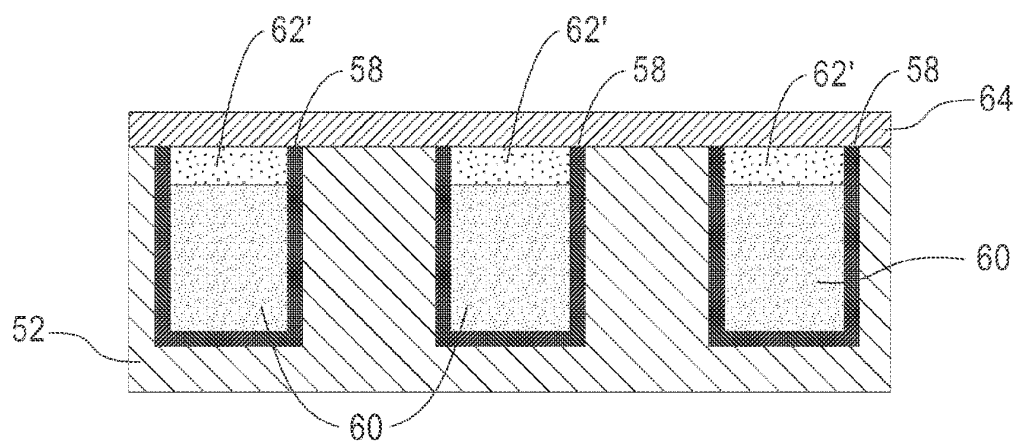


FIG. 2G

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2009/050627

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/768 H01L23/532

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/023917 A1 (YAMADA MASAKI [JP]) 1 February 2007 (2007-02-01) the whole document	1-3, 5-11, 13, 15-19, 22-25
X	WO 2006/112202 A (SHARP KK [JP]; KAMIKUBO NORITAKA) 26 October 2006 (2006-10-26) the whole document	1, 4-9, 12-16, 19-25
X	KR 100 752 195 B1 (DONGBU ELECTRONICS CO LTD [KR]) 20 August 2007 (2007-08-20) the whole document	1, 4, 5, 7-9, 12, 13, 15, 16, 19, 22-25

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:

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- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

- *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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- *8* document member of the same patent family

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INTERNATIONAL SEARCH REPORT

International application No
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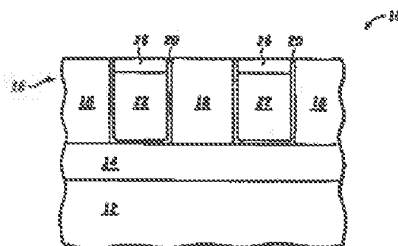
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最終頁に続く

(54) 【発明の名称】 キャップ層を半導体素子の上に形成するための方法



[0001] 本発明は、概して半導体に関し、特にキャップ層を半導体素子の上に形成する方法に関する。

[0002] 集積回路では、誘電体層を使用してチップの相互接続配線の周りの絶縁を行なう。銅配線のような高導電化を可能にする相互接続材料によって信号をチップの中を効率的に伝送することができるのと同様に、絶縁材料の容量値を小さくすることによっても、複数の信号を相互接続を通してより効率的に伝送することができる。これは、これらの信号が互いに干渉することが少なくなるからである。最も普及している誘電体材料は二酸化シリコンである。しかしながら、半導体業界では特に、低誘電率材料又は低k材料と一般的に表記される商業的に有用な低容量の誘電体材料の開発が行なわれている。

- [0003] 相互接続を形成する場合、誘電体層をバターンニングしてトレンチ、ビア開口などのような空洞を形成する。次に、空洞に銅のような導電性材料を充填する。エレクトロマイグレーション又は拡散を防止するために、非常に薄いバリア層を誘電体の上に形成し、そして銅をバリア層の上に形成する。バリア層は通常、 Ta （タンタル）により形成される。化学的機械研磨（CMP）プロセスを使用して銅及びバリア層を誘電体層の上から除去する。銅の不要部分を取り除いて銅を空洞に埋め込み、そしてタンダステン（W）、モリブデン（Mo）、レニウム（Ru）などのような元素が添加された従来のコバルト（Co）膜を銅の上に形成して銅が周囲の誘電体材料に拡散する現象を防止する。この処理によって、銅を低 k 材料を使用して高密度に形成することができる。また、銅をこれらのタイプの材料でキャップすることにより、エレクトロマイグレーション耐性を高めて信頼性を高めることができる。信頼性の高い半導体を実現するためには、これらの銅を、非常に高い選択性を利用した増幅プロセスで増幅させる必要がある。また、キャップ層の形成は、銅表面の状態によって大きく変わる。
- [0004] 通常、コバルト膜は銅の上に無電解メッキにより増幅させる。メッキプロセスによって、キノコ型形状を有するコバルト膜が形成される。キノコ型構造は誘電体の表面の上に延出し、そしてキノコ型構造によって複数の導体の間に許容できないリーク電流が発生する。更に、メッキプロセスによってコバルト膜の表面が非常に粗くなる。
- [0005] 従って、平滑なキャップ層を銅の上に形成し、複数の導体の間のリーク電流を最小に抑える方法が必要になる。
- [0006] 簡括すると、本発明は、半導体素子の相互接続部において、キャップ層をビア開口又はトレンチのような空洞に充填される導電金属層の上部に形成する方法を提供するものである。キャップ層は、導電金属が後続の工程で素子内に形成される相互接続部に拡散する現象を防止するために設けられる。
- [0007] 絶縁回路層を基板の上に形成する。相互接続部は絶縁回路層の上部の上に、誘電体層を増幅させ、そして誘電体層をバターンニングして、ビア開口、トレンチなどとしてすることができる空洞を形成することにより形成される。タンタル又は窒化タンタルのような拡散バリア層をバターンニング済み誘電体層の上に増幅させて、空洞と、そしてバターンニング済み誘電体層の上部と、を拡散バリア層で裏打ちする。銅のような導電金属を拡散バリア層の上に増幅させて、空洞に金属を充填し、そしてブランケット膜をバターンニング済み誘電体層の上に形成する。拡散バリア層は、導電金属が誘電体層に拡散する現象を防止するように機能する。導電金属から成るブランケット膜を化学的機械研磨法（CMP）又は他の平坦化方法により除去し、そして導電金属を空洞に残留させる。拡散バリア層は導電金属から成るブランケット膜とともに除去されるということがほとんどない。又は別の平坦化工程においてブランケット膜とともに除去されるということがほとんどなく、そしてバターンニング済み誘電体の表面に残留する。この残留拡散バリア層が、誘電体層をCMPのような更に別の処理によるダメージを覚えることがないように保護するように機能する。次に、空洞に残留する導電金属の不要部分を、選択性化学エッチングにより取り除いて、又はCMP又は他の平坦化プロセスによる低ディッシングの研磨により取り除いて導電金属を空洞に埋め込む。次に、コバルト、又は他の導電性元素を添加したコバルトから成るキャップ層を無電解メッキ又は他の増幅プロセスによって増幅させて、キャップ層が導電金属上の後述の導体に連続的に充填されるようにする。空洞よりも上に延び、かつバターンニング済み誘電体層の上部の上に延在する部分のキャップ層を、単一のCMPプロセス又は他の平坦化プロセスによって除去する。キャップ層の表面粗さをこの平坦化プロセスによって低減してリーク電流を小さくする。
- [0008] 導電金属層を除去した後、拡散バリア層をバターンニング済み誘電体層の上部の上に残留させることにより、誘電体表面は、キャップ層を増幅させている際に露出することがない。又はキャップ層の平坦化、及び拡散バリア層の除去を同時にこなしている際のほとんどの時間の間露出することがない。誘電体層がキャップ層の増幅プロセスにおいて露出することがないようにすることにより、キャップ層の増幅プロセスにおいて使用される材料の拡散が極めて小さくなる。キャップ層を無電解メッキ処理で増幅させる場合、残留拡散バリア層は、誘電体層への金属イオンの拡散をほとんど阻止するように作用して、導電性材料が満足されることによって発生するリーク電流を低減する。残留拡散バリア層は更に、キャップ層の平坦化、及び拡散バリア層の大部分の除去を同時にこなしている際の機械的強度を更に高めるように作用して、誘電体層へのダメージを低減する。機械的ダメージを低減し、かつ誘電体層への汚染物質の拡散を低減する利点は、誘電体層が低誘電率材料である場合に一層顕著になる。更に、キャップ層を形成する方法は、キャップ層を平坦化する処理、及び誘電体層上に残留する拡散バリア層を除去する処理を、別々の工程においてではなく、一つのプロセス工程において行なうことにより簡易化される。
- [0009] 図1は、半導体ウェハ10の一部分の断面図を示している。半導体ウェハを処理して、集積回路を構築した半導体装置を形成する。半導体ウェハ10は基板12と、そして絶縁回路層14と、を含み、絶縁回路層は、トランジスタ、ダイオード、抵抗体、及び他の回路要素のような複数の構造を含む。トランジスタは、例えば特許型金属酸化物半導体（CMOS）トランジスタとすることができる。基板12は、シリコン、シリコンオンインシュレータ、シリコンゲルマニウム、又は他の半導体材料とすることができる。相互接続層16は回路層14の表面に形成する。相互接続層16は誘電体層18から成り、この誘電体層をバターンニングして空洞16及び残留構造構造を、従来のフォトリソグラフィ及びエッチングプロセスを使用して形成する。空洞16はビア開口、トレンチなどとしてすることができる。一の実施形態では、誘電体層18は炭素含有シリコンであるが、二酸化シリコン、不純物含

有ニ酸化シリコン、又は多孔質低誘電率材料とすることができる。拡散バリア層20を誘電体層18の上に堆積させ、そして拡散バリア層20でパターニング済み誘電体層18の上部、及び空間16の側壁及び底面を裏打ちする。拡散バリア層20は物理気相成長法(PVD)、化学気相成長法(CVD)、又は他の成る堆積法によって堆積させる。一の実施形態では、拡散バリア層はタンタル(Ta)とすることができるが、窒化タンタル(TaN)、窒化チタン(TiN)、又は他の誘電性材料とすることができる。誘電金属層22を拡散バリア層20の上に堆積させると、誘電金属層22で空間16が充填され、続いて誘電金属層22がパターニング済み誘電体層18及び拡散バリア層20を覆うブラケット層を形成するようになる。誘電金属層22は銅又は他の誘電金属とすることができ、そして電解メッキ、PVD法、又は他の堆積法、或いはこれらの方法の組み合わせにより堆積させる。一の実施形態では、誘電金属層22は、銅シード層をPVD法によって形成し(図示せず)、次に銅をシード層の上部の上に電解メッキにより堆積させることができる。

[0010] 図2は、誘電金属層22の一部分を従来の化学的銅めっき(CMP)プロセス、又は電気化学的銅めっき(eCMP)のような別の平坦化方法を使用して除去した後の図1の半導体素子10の断面図を示している。図2に示すように、空間16に充填される金属の部分を除いて、誘電金属層22の全てを除去する。拡散バリア層20はCMPプロセスでほとんど除去されることがない。拡散バリア層20の内、パターニング済み誘電体層18の上の全ての部分、又はほとんど部分を残すことにより、パターニング済み誘電体層18を後続の処理工程の影響を受けないように保護することができる。

[0011] 図3は、空間16に残留する誘電金属層22の一部分を除去して後退領域24を形成して残留誘電金属層22の上部表面がパターニング済み誘電体層18の上部表面の下方に位置するようにした後の、図2の半導体素子10の一部分の断面図を示している。金属層22の中の後退領域24は、選択的化學エッチングにより、又はCMP、eCMP、又は他の平坦化プロセスによる低ディッシングの原理により形成することができる。ここで、拡散バリア層20はこの処理時点で除去されないことに注目されたい。拡散バリア層20は、誘電体層18が後続の処理工程によって発生し得る汚染物質及びダメージの影響を受けることがないように誘電体層18を保護する。

[0012] 図4は、キャップ層26を選択的に堆積させた後の図3の半導体素子10の断面図を示している。一の実施形態では、キャップ層26は無電解メッキによって堆積させるが、他の選択的堆積技術を使用することができる。キャップ層26は、コバルト(Co)のような誘電金属であり、キャップ層26にはタングステン(W)又はボロン(B)のような他の元素を添加することができる。一の実施形態では、キャップ層26は、コバルト(Co)、タングステン(W)、及びボロン(B)を含む。図示の実施形態では、キャップ層26を堆積させる処理では、ボロン、稀酸コバルト、及びタングステン酸ナトリウム又はタングステン酸を含む溶液を塗布する。また、キャップ層26には、ニッケル(Ni)、モリブデン(Mo)、シリウム(Ru)、及びパリン(P)のような元素を添加することができる。理想的話は、キャップ層26を後退領域24への充填が完了するまで堆積させてから、キャップ層の堆積を停止する。しかしながら、コバルト、タングステン、及びボロンを含むキャップ層を堆積させる処理は容易かつ正確に制御することができないので、必要とされる材料よりも多くの材料を堆積させて、確率の後退領域が十分に充填されるようにする。これによって、キャップ層26が図4に示すキノコ型構造を有するようになる。キャップ層26は、銅が後の工程で形成される相互接続層に於いて拡散することがないように機能する。また、キャップ層はエレクトロマイグレーションを低減するように機能することができる。

[0013] 図5は、キャップ層26の一部分、及びパターニング済み誘電体層18の上の拡散バリア層20を、従来のCMP、eCMP、又は他の平坦化方法によって1回の工程で除去して、誘電体層18及びキャップ層26の上部表面全体が平坦になるようにした後の図4の半導体素子10の一部分の断面図を示している。また、キャップ層26の表面粗さを、1回の平坦化工程によって低減して、リーク電流を減らす。更に、CMP装置のブラザン(巨錠定数)を1台だけ使用して、キャップ層26及び拡散バリア層20の両方を1回のCMP処理工程で除去する。これにより製造コストを、半導体素子を形成するために必要なCMP工程の数を減らすことにより下げる。また、拡散バリア層20を、図2に示す銅層22をCMPによって除去した後に堆積させることにより、拡散バリア層20が図5に示すように除去されるまで、誘電体層18を後続の処理工程の影響を受けることがないように保護する。拡散バリア層20による保護を行わない場合には、後続の処理工程によって汚染又はダメージが誘電体層18に発生する恐れがある。バリア層を残留させることにより、誘電体層18は、バリア層/キャップ層を除去するための図6のCMP工程の最後の段階で露出するだけである。

[0014] 本発明について好適な実施形態を参照しながら説明してきたが、この技術分野の当業者であれば、本発明は多くの方法により変更することができる。更に、特定の形で開示し、そして上に説明した実施形態以外の多くの実施形態を探り得ることが理解できるであろう。従って、添付の請求項が、本発明の真の技術範囲に含まれる本発明の全ての変形を含むものと考えらる。

[0015] 効果、他の利点、及び技術的課題に対する解決法について、特定の実施形態に関して上に記載してきた。しかしながら、効果、利点、問題解決法、及び凡そこれらの効果、利点、又は問題解決法をもたらし、又はさらに顕著にし

得る全ての要素（群）が、いずれかの請求項又は全ての請求項の必須の、必要な、又は基本的な特徴又は要素であると解読されるべきではない。

【請求項 1】

能動回路によって半導体素子が覆われるように半導体基板を露ける工程と、

空洞を有するバタ—ニング済み誘電体を能動回路の上方に形成する工程と、

拡散バリアをバタ—ニング済み誘電体の上方に形成して、空洞が拡散バリアで塞打ちされ、かつバタ—ニング済み誘電体の上部表面が拡散バリアで被覆されるようにする工程と、

導電層を拡散バリアの上方に、導電層が空洞に充填されるように形成する工程と、

導電層をエッチングして導電層を拡散バリアの上部表面から、拡散バリアのほとんどの部分を除去することなく除去する工程と、

後送領域を空洞内の導電層に、後送領域がバタ—ニング済み誘電体の上部表面の下方に位置するように形成する工程と、

後送領域にキャップ層を充填する工程と、

バタ—ニング済み誘電体の上部表面の上の拡散バリア、及びキャップ層の一部分を除去して、拡散バリアがバタ—ニング済み誘電体の上部表面の上から除去され、及び平坦な表面がバタ—ニング済み誘電体の上部表面とキャップ層の上部表面との間に形成されるようにする工程とを備える、半導体素子の製造方法。

【請求項 2】

導電層をエッチングする前記工程は、

化学的機械研磨（CMP）を実施する工程と、

CMPを実施した後に、拡散バリアと導電層との間で選択性を示す化学エッチャントを用いたエッチングを行なう工程とを備える、請求項1記載の方法。

【請求項 3】

バタ—ニング済み誘電体の上部表面の上の拡散バリア、及びキャップ層の一部分を除去する工程では、拡散バリア、及びキャップ層の一部分を化学的機械研磨（CMP）処理工程の間に除去する、請求項1記載の方法。

【請求項 4】

前記バタ—ニング済み誘電体は低k誘電体からなり、前記導電層は銅からなり、前記拡散バリアはタンタルからなり、前記キャップ層はシリコンからなる、請求項1記載の方法。

【請求項 5】

キャップ層は更にタングステン及びボロンを含む、請求項4記載の方法。

【請求項 6】

導電層をエッチングする工程では、CMPを実施して、バタ—ニング済み誘電体の上部表面の上の導電層を除去し、そして導電層の一部分を空洞の中に埋め込んで後送領域を形成する、請求項1記載の方法。

【請求項 7】

後述領域に充填する工程では、コバルト／タングステン／ボロンを選択的に堆積させる、請求項 1 記載の方法。

【請求項 8】

選択的に堆積させる工程では、ボロン、ニオブコバルト、及びタングステン酸ナトリウム又はタングステン酸を含む溶液を塗布する、請求項 7 記載の方法。

【請求項 9】

導電層を形成する工程では、銅を電解メッキする、請求項 1 記載の方法。

【請求項 10】

導電層をエッチングする前記工程では

CMP によって、パターンング済み誘電体の上部表面の上の導電層のほぼ全てを除去し、

CMP によって、導電層をパターンング済み誘電体の上部表面の上から完全に除去し、そして拡散バリアの少なくとも一部分を、パターンング済み誘電体の上部表面の上方に残留させ、及び

空洞の中の導電層をエッチバックして後述領域を形成する、請求項 1 記載の方法。

【請求項 11】

除去する工程では、CMP を実施する、請求項 1 記載の方法。

【請求項 12】

半導体基板を、絶縁層によって半導体基板が覆われるように塗ける工程と、

空洞を有するパターンング済み誘電体を絶縁層の上方に形成する工程と、

拡散バリアをパターンング済み誘電体の上方に形成して、空洞が拡散バリアで裏打ちされ、かつパターンング済み誘電体の上部表面が拡散バリアで被覆されるようにする工程と、

メッキによって導電層を拡散バリアの上方に形成して、導電層が空洞に充填されるようにする工程と、

パターンング済み誘電体の上部表面の上の導電層を除去する工程を実施して、拡散バリアの少なくとも一部分をパターンング済み誘電体の上部表面の上方に残留させ、そして空洞の中の導電層の一部分を除去して、後述領域をパターンング済み誘電体の上部表面の下方に形成する工程と、

後述領域にキャップ層を選択堆積法により充填して、キャップ層の上部表面がパターンング済み誘電体の上部表面よりも高くなるようにする工程と、

パターンング済み誘電体の上部表面の上の拡散バリアを除去する工程を実施して、キャップ層の一部分を除去し、そしてほぼ平坦な表面をパターンング済み誘電体の上部表面とキャップ層の上部表面との間に形成する工程とを備える、半導体素子の製造方法。

【請求項 13】

拡散バリアを除去する工程では、CMP を実施する、請求項 1 2 記載の方法。

【請求項 14】

導電層を除去する工程では、CMP を実施する、請求項 1 2 記載の方法。

【請求項 15】

導電層を除去する工程では更に、導電層と拡散バリアとの間で選択性を示すエッチャントを用いたエッチングを行なって後述領域を形成する。請求項 14 記載の方法。

【請求項 16】

前記導電層は銅からなり、前記キャップ層はコバルトからなる。請求項 12 記載の方法。

【請求項 17】

前記拡散バリアはタンタルからなる。請求項 16 記載の方法。

【請求項 18】

半導体基板上、絶縁回路によって半導体基板が覆われるように設ける工程と、

空間を有するパターンニング済み誘電体を絶縁回路の上に形成する工程と、

拡散バリアをパターンニング済み誘電体の上に形成して、空間が拡散バリアで塞がれ、かつパターンニング済み誘電体の上部表面が拡散バリアで被覆されるようにする工程と、

導電層を拡散バリアの上方に、導電層が空間に充填されるように形成する工程と、

導電層を平坦化することにより拡散バリアを露出させる工程と、

後述領域を空間に、後述領域がパターンニング済み誘電体の上部表面の下方に位置するように形成する工程と、

後述領域にキャップ層を充填する工程と、

パターンニング済み誘電体及びキャップ層の上部表面を平坦化することにより、パターンニング済み誘電体の上部表面の上の拡散バリアを除去する工程とを備える。半導体素子の製造方法。

【請求項 19】

前記導電層は銅からなり、前記拡散バリアはタンタルからなり、キャップ層はコバルトからなる。請求項 18 記載の方法。

【請求項 20】

上部表面を平坦化する工程、及び導電層を平坦化する工程は CMP により行なわれる。請求項 18 記載の方法。

(57) 【要約】

半導体素子形成する方法は、複数の空間 (16) を有するパターンニング済み誘電体 (18) を絶縁回路の上に形成する工程を含む。拡散バリア (20) をパターンニング済み誘電体 (18) の上に形成する。導電層 (22) を複数の空間の中の拡散バリアの上に形成する。導電層を、導電層が誘電体の上部表面の下方に位置するようにエッチバックして、後述領域 (24) を、複数の空間の中の導電層の上に形成する。次に、後述領域にキャップ層 (26) を充填する。キャップ層及び拡散バリアを除去すると、非平坦な平滑な平坦化表面が得られる。非平坦な平滑な平坦化表面を形成することにより、複数の導体の間のリーク電流を低減する。

[0001]

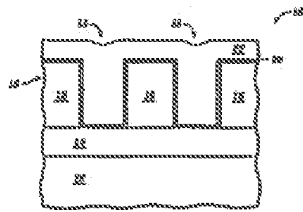


FIG. 1

[0002]

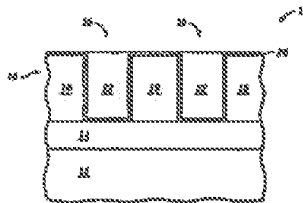


FIG. 2

[0003]

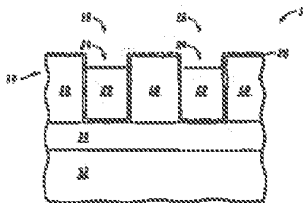


FIG. 3

[0004]

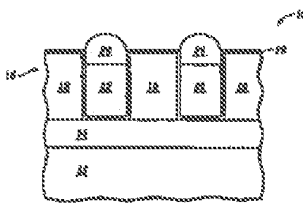


FIG. 4

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(FIG. 5)

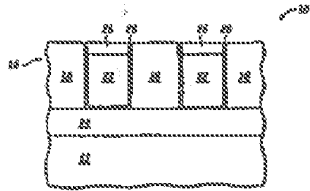


FIG. 6

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 98/02822

A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - H04L 81/4788 (2007.01) USPC - 438/622; 438/627; 438/678 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELD SEARCHED 3-Section descriptive search (classification system followed by classification symbols) USPC - 438/622; 438/627; 438/678 Documents searched after this abstract documents to the extent that each document are located in the fields searched (USPC - 438/622; 438/627; 438/678 (not search, see limits below)) Electronic data base consulted during the international search (names of data base and, where practicable, search terms used) FAST/EST/USPT/JP/EP/AS/JPAT/Dialog/ProQuest/Engineering; Google Scholar Search Terms: coding layer, countermeasure, channel or channel coding, stream, code		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2004/019891 A1 (Covenger et al.) 17 June 2004 (17.06.2004), entire document, especially page [0018], [0020], [0028]	1-6, 8, 9-13, 15, 20 4-6, 7-8, 13, 17, 19
Y	US 2003/019130 A1 (Fang et al.) 29 July 2003 (29.07.2003), page [0040], [0046] (20-47)	4-6, 7-8, 13, 17, 19
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Date of the actual completion of the international search 22 April 2007 (24.04.2007)		Date of mailing of the international search report 10 JUL 2007
Name and mailing address of the ISA/LA Mail Stop PCT, 4800 USA/15, Christchurch for Patents P.O. Box 1405, Alexandria, Virginia 22315-1405 Washington DC 20541-4051		Authorized officer: Lee W. Young PCT telephone 571-273-6000 PCT fax 571-273-7710

Form PCT/ISA/210 (second sheet) (April 2004)

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(81)指定国 AP(BW, CH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), EA(AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), EP(AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OA(BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TO), AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KN, KP, KR, KZ, LA, L C, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW

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CLAIMS

[Claim(s)]

[Claim 1]

A process of providing a semiconductor substrate so that a semiconductor substrate may be covered with an active circuit,
A process of forming a patterned dielectric which has a cavity above the active circuit,
A process at which a diffusion barrier is formed above a patterned dielectric, and a cavity is backed with a diffusion barrier, and the upper surface of a patterned dielectric is covered by diffusion barrier,
A process of forming a conductive layer above a diffusion barrier so that a conductive layer may be filled up by cavity,
A process of removing a conductive layer from the upper surface of a diffusion barrier by etching a conductive layer without removing almost all portions of a diffusion barrier,
A process of forming a retreating region so that a retreating region may be placed at a conductive layer in a cavity down the upper surface of a patterned dielectric,
A process of filling up a retreating region with a cap layer,
A diffusion barrier on the upper surface of a patterned dielectric and a part of cap layer are removed, A manufacturing method of a semiconductor device with which a diffusion barrier is removed from on the upper surface of a patterned dielectric, and the substantially flat surface is provided with a process formed between the upper surface of a patterned dielectric, and the upper surface of a cap layer.

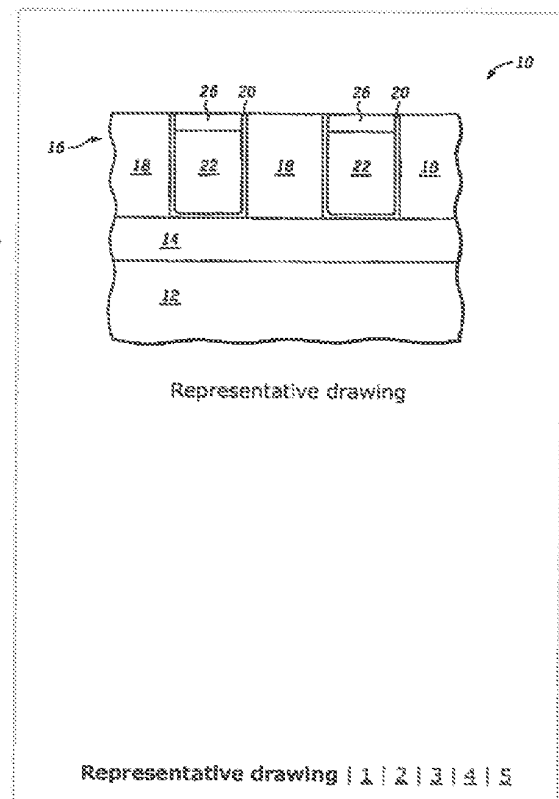
[Claim 2]

The aforementioned process of etching a conductive layer,
A process of carrying out chemical mechanical polishing (CMP),
A method according to claim 1 provided with a process of performing

etching using a chemical etchant which shows selectivity between a diffusion barrier and a conductive layer after carrying out CMP.

[Claim 3]

A method according to claim 1 of removing a diffusion barrier and a part of cap layer between chemical mechanical-polishing (CMP) down stream



processing in a process of removing a diffusion barrier on the upper surface of a patterned dielectric, and a part of cap layer.

[Claim 4]

A way according to claim 1 the aforementioned patterned dielectric consists of a low k dielectric, the aforementioned conductive layer consists of copper, the aforementioned diffusion barrier consists of tantalum, and the aforementioned cap layer consists of cobalt.

[Claim 5]

A way according to claim 4 a cap layer contains tungsten and boron further.

[Claim 6]

A method according to claim 1 of hollowing a part of conductive layer in a cavity, and forming a retreating region by carrying out CMP and removing a conductive layer on the upper surface of a patterned dielectric in a process of etching a conductive layer.

[Claim 7]

A method according to claim 1 of making cobalt / tungsten / boron deposit selectively in a process with which a retreating region is filled up.

[Claim 8]

A method according to claim 7 of applying a solution containing borane, cobalt sulfate and sodium tungstate, or tungstic acid in a process made to deposit selectively.

[Claim 9]

A method according to claim 1 of carrying out electrolytic plating of the copper in a process of forming a conductive layer.

[Claim 10]

At the aforementioned process of etching a conductive layer,
CMP -- a conductive layer on the upper surface of a patterned dielectric -- removing all substantially

By CMP, remove a conductive layer from on the upper surface of a patterned dielectric completely, and at least 1 portion of a diffusion barrier is made to remain above the upper surface of a patterned dielectric, and it reaches. A method according to claim 1 of carrying out etchback of the conductive layer in a cavity, and forming a retreating region.

[Claim 11]

A method according to claim 1 of carrying out CMP in a process to remove.

[Claim 12]

A process of providing a semiconductor substrate so that a semiconductor substrate may be covered with an active circuit,

A process of forming a patterned dielectric which has a cavity above the active circuit,

A process at which a diffusion barrier is formed above a patterned dielectric, and a cavity is backed with a diffusion barrier, and the upper surface of a patterned dielectric is covered by diffusion barrier,

A process which forms a conductive layer above a diffusion barrier and with which a conductive layer is filled up into a cavity by plating,

A process of removing a conductive layer on the upper surface of a patterned dielectric is carried out, It is the residual process of carrying out, and removing a part of conductive layer in a cavity, and forming a retreating region down the upper surface of a patterned dielectric, above the upper surface of a patterned dielectric about at least 1 portion of a diffusion barrier,

A process of filling up a retreating region with a cap layer by the selection depositing method, and making it the upper surface of a cap layer become higher than the upper surface of a patterned dielectric,

A manufacturing method of a semiconductor device which comprises a process of forming the substantially flat surface between the upper surface of a patterned dielectric, and the upper surface of a cap layer, by carrying out a process of removing a diffusion barrier on the upper surface of a patterned dielectric, and removing a part of cap layer.

[Claim 13]

A method according to claim 12 of carrying out CMP in a process of removing a diffusion barrier.

[Claim 14]

A method according to claim 12 of carrying out CMP in a process of removing a conductive layer.

[Claim 15]

A method according to claim 14 of performing etching using etchant which shows selectivity between a conductive layer and a diffusion barrier; and forming a retreating region further, at a process of removing a conductive layer.

[Claim 16]

A way according to claim 12 the aforementioned conductive layer consists of copper and the aforementioned cap layer consists of cobalt.

[Claim 17]

A way according to claim 16 the aforementioned diffusion barrier consists of tantalum.

[Claim 18]

A process of providing a semiconductor substrate so that a semiconductor substrate may be covered with an active circuit,

A process of forming a patterned dielectric which has a cavity above the active circuit,

A process at which a diffusion barrier is formed above a patterned dielectric, and a cavity is backed with a diffusion barrier, and the upper surface of a patterned dielectric is covered by diffusion barrier,

A process of forming a conductive layer above a diffusion barrier so that a conductive layer may be filled up by cavity,

A process at which a diffusion barrier is exposed by flattening a conductive layer,

A process of forming a retreating region so that a retreating region may be placed at a cavity down the upper surface of a patterned dielectric,

A process of filling up a retreating region with a cap layer,

A manufacturing method of a semiconductor device provided with a process of removing a diffusion barrier on the upper surface of a patterned dielectric by flattening the upper surface of a patterned dielectric and a cap layer.

[Claim 19]

A way according to claim 18 the aforementioned conductive layer consists of copper, the aforementioned diffusion barrier consists of tantalum, and a cap layer consists of cobalt.

[Claim 20]

A method according to claim 18 by which a process of flattening the upper surface, and a process of flattening a conductive layer are performed by CMP.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[Field of the Invention]

[0001]

The present invention relates to a semiconductor generally and relates to the method of forming especially a cap layer on a semiconductor device.

[Background of the Invention]

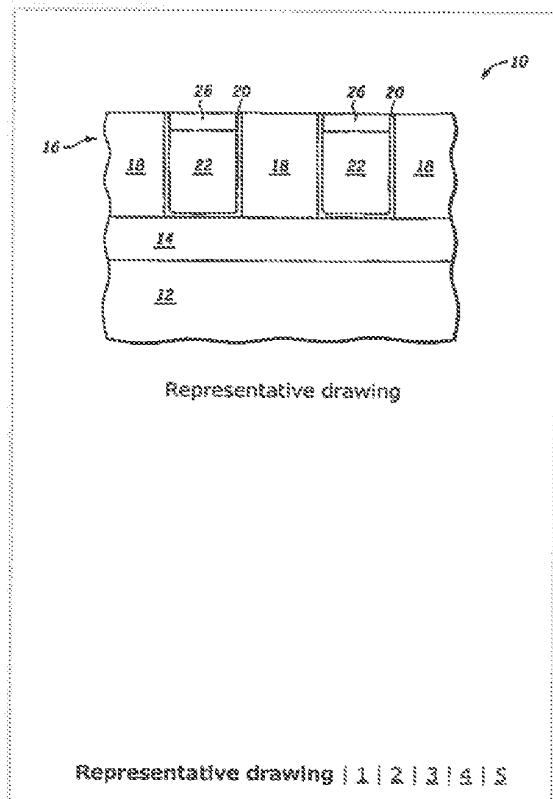
[0002]

In an integrated circuit, a surrounding insulation of the interconnecting wiring of a chip is performed using a dielectric layer. Although a plurality of signals can be transmitted more to a high speed through interconnection also by making capacity value of an insulating material small exactly the same with the ability of the inside of a chip to be transmitted for a signal at high speed with the interconnection material which enables improvement in the speed like a copper wiring, This is because that these signals interfere each other decreases. Most diffused dielectric materials are silicon dioxide. However, in the semiconductor industry, development of the dielectric materials of the commercially useful low capacity always written as a low dielectric constant material or low k material generally is performed.

[0003]

When forming interconnection, a dielectric layer is patterned and cavities, such as a trench and a beer opening, are formed. Next, a cavity is filled up with a conductive material like copper. In order to prevent electromigration or diffusion, a very thin barrier layer is formed on a dielectric, and copper is formed on a barrier layer. A barrier layer is usually formed by Ta (tantalum). Copper and a barrier layer are removed from on a dielectric layer using a chemical mechanical-polishing (CMP) process. Cobalt (Co) film of the former which removes a copper garbage and embeds copper in a cavity and by which elements, such as tungsten (W), molybdenum (Mo), and a rhenium

(Re), were added is formed on copper, and copper prevents the phenomenon which diffuses to the surrounding dielectric materials. By this processing, copper can be formed with high density using low k material. By capping copper with these types of material, electromigration resistance can be improved and reliability can be improved. In order to realize a reliable



semiconductor, it is necessary to make these films deposit in the deposition process using very high selectivity. Formation of a cap layer changes largely according to the state of a copper surface.

[0004]

Usually, a cobalt film is made to deposit by electroless deposition on copper. The cobalt film which has a mushroom mold configuration is formed by the plating process. Mushroom mold structure extends on the surface of a dielectric, and leakage current nonpermissible among a plurality of conductors according to mushroom mold structure generates it. The surface of a cobalt film becomes very coarse by a plating process.

[Description of the Invention]

[Problem to be solved by the invention]

[0005]

Therefore, a smooth cap layer is formed on copper and the method of suppressing the leakage current between a plurality of conductors to the minimum is needed.

[Means for solving problem]

[0006]

If summarizing it, the present invention provides the method of forming in the upper part of the electric conduction metal layer filled up with a cap layer by a beer opening or cavity like a trench in the interconnection layer of a semiconductor device. A cap layer is provided in order that electric conduction metal may prevent the phenomenon which diffuses to the interconnection layer formed in an element at a following process.

[Best Mode of Carrying Out the Invention]

[0007]

An active circuit layer is formed on a substrate. An interconnection layer makes a dielectric layer deposit on the upper part of an active circuit layer, and patterns a dielectric layer, and is formed by forming the cavity which can be used as a beer opening, a trench, etc. A diffusion barrier layer like tantalum or tantalum nitride is made to deposit on a patterned dielectric layer, and the upper part of a cavity and a patterned dielectric layer is backed with a diffusion barrier layer. Electric conduction metal like copper is made to deposit on a diffusion barrier layer, and a cavity is filled up with metal, and a blanket film is formed on a patterned dielectric layer. A diffusion barrier layer functions as electric conduction metal preventing the phenomenon which diffuses to a dielectric layer. The blanket film which comprises electric conduction metal is removed with a chemical mechanical-polishing method (CMP) or other flattening methods, and electric conduction metal is made to remain in a cavity. A diffusion barrier layer does not almost have it hardly being removed with the blanket film which comprises electric conduction metal, or being removed with a blanket film in another flattening process, and remains on the surface of a patterned dielectric. This residual diffusion barrier layer functions as protecting so that the damage according a dielectric layer to another processing like CMP may not be received. Next, the garbage of the residual electric conduction metal to carry out is removed by selectivity chemical etching in a cavity, or is removed by polish of low dishing by CMP or other planarizing processes in it, and electric conduction metal is embedded in a cavity. Next, the cap layer which comprises cobalt or the cobalt which added other conductive elements is made to deposit according to electroless deposition or other deposition processes, and the retreating region on electric conduction metal is excessively filled up with a cap layer. A single CMP process or other planarizing processes remove the cap layer of the portion which extends above a cavity and extends on the upper part of a patterned dielectric layer. The surface roughness of a cap layer is reduced according to this planarizing process, and leakage current is made small.

[0008]

After removing an electric conduction metal layer, a diffusion barrier layer by [residual] carrying out on the upper part of a patterned dielectric layer a dielectric surface. While making the cap layer deposit, it does not expose, or it does not expose between almost all the time at the time of performing

simultaneously flattening of a cap layer, and removal of the diffusion barrier layer. When keeping a dielectric layer from being exposed in the deposition process of a cap layer, diffusion of the material used in the deposition process of a cap layer becomes very small. When making a cap layer deposit in an electroless plating process, a residual diffusion barrier layer acts so that most diffusion of the metal ion to a dielectric layer may be prevented, and reduces the leakage current which occurs by catching a conductive material. A residual diffusion barrier layer acts so that the mechanical strength at the time of removing flattening of a cap layer and most diffusion barrier layers simultaneously may further be raised, and it reduces the damage to a dielectric film. The advantage which reduces a mechanical damage and reduces diffusion of the pollutant to a dielectric layer becomes much more remarkable, when a dielectric layer is a low dielectric constant material. The method of forming a cap layer is simplified by performing [in / in a separate process, there is nothing then and / one process process] processing which flattens a cap layer, and processing which removes the residual diffusion barrier layer to carry out on a dielectric layer.

[0009]

Fig.1 shows some cross sectional views of the semiconductor wafer 10. A semiconductor wafer is processed and the semiconductor device which mounted the integrated circuit is formed. The semiconductor wafer 10 includes a plurality of structures [like a transistor, a diode, a resistor, and other circuit elements] whose active circuit layer is including the substrate 12 and the active circuit layer 14. A transistor can be used as a complementary-type metal oxide semiconductor (CMOS) transistor, for example. The substrate 12 can be used as silicon, a silicon on insulator, silicon germanium, or other semiconductor materials. The interconnection layer 16 is formed in the surface of the circuitry layer 14. The interconnection layer 16 comprises the dielectric layer 18, patterns this dielectric layer, and forms the cavity 15 and a residual vertical structure using a conventional photolithography and etching process. The cavity 15 can be used as a beer opening, a trench, etc. According to the embodiment of 1, although the dielectric layer 18 is carbon content silicon oxide, it can be used as silicon dioxide, impurity content silicon dioxide, or a porous low dielectric constant material. The diffusion barrier layer 20 is made to deposit on the dielectric layer 18, and the side wall and bottom surface of the upper part of the patterned dielectric layer 18 and the cavity 15 are backed with the diffusion barrier layer 20. A diffusion barrier is made to deposit by physical vapor growth (PVD), a chemical-vapor-deposition method (CVD), or other depositing methods of a certain. According to the embodiment of 1, although a diffusion barrier layer can be made into tantalum (Ta), it can be used as tantalum nitride (Ta₃N₅), titanium nitride (TiN), or other conductive materials. If the electric conduction metal layer 22 is made to deposit on the diffusion barrier layer 20, the cavity 15 will be filled up with the electric conduction metal layer 22, and it will come to form the blanket layer in which the electric conduction metal layer 22 covers the patterned dielectric layer 18 and the diffusion barrier 20 continuously. The electric conduction metal layer 22 can be used as copper or other electric conduction metal, and is made to deposit with the combination of electrolytic plating, a PVD method, other depositing methods, or these methods. The electric conduction metal layer 22 can form a copper seed layer with a PVD method (not shown), and, next, can make copper deposit by electrolytic plating on the upper part of a seed layer in the embodiment of 1.

[0010]

Fig.2 shows the cross sectional view of the semiconductor device 10 of the Fig.1 after removing a part of electric conduction metal layer 22 using the conventional chemical mechanical-polishing (CMP) process or another flattening method like electrochemistry mechanical polishing (eCMP). As shown in Fig.2, except for the portion of the metal with which the cavity 15 is filled up, all the electric conduction metal layers 22 are removed. The diffusion barrier layer 20 is hardly removed in a CMP process. By leaving all

the portions on the patterned dielectric layer 18 among the diffusion barrier layers 20, or almost all portions, it can protect so that it may not be subject to the influence of down stream processing of succession to the patterned dielectric layer 18.

[0011]

Fig.3 shows some cross sectional views of the semiconductor wafer 10 of Fig.2 after removing a part of residual electric conduction metal layer 22 to carry out in the cavity 15, forming the retreating region 24 in it and making it the upper surface of the residual electric conduction metal layer 22 be placed at it down the upper surface of the patterned dielectric layer 18. The retreating region 24 in the metal layer 22 can be formed by alternative chemical etching or polish of low dishing by CMP, eCMP, or other planarizing processes. Here, please note that are the diffusion barrier layer 20 at this processing time, and it is not removed. The diffusion barrier layer 20 protects the dielectric layer 18 so that it may not be subject to the influence of the pollutant and damage which the dielectric layer 18 may generate by following down stream processing.

[0012]

Fig.4 shows the cross sectional view of the semiconductor wafer 10 of the Fig.3 after making the cap layer 26 deposit selectively. According to the embodiment of 1, although the cap layer 26 is made to deposit by electroless deposition, it can use other selection deposition technology. The cap layer 26 is electric conduction metal like cobalt (Co), and can add other elements like tungsten (W) or boron (B) to the cap layer 26. According to the embodiment of 1, the cap layer 26 contains cobalt (Co), tungsten (W), and boron (B). At an illustrated embodiment, the solution containing borane, cobalt sulfate and sodium tungstate, or tungstic acid is applied by the processing on which the cap layer 26 is made to deposit. To the cap layer 26, nickel (nickel), molybdenum (Mo), a rhenium (Re), and an element like a phosphorus (P) can be added. After making it deposit ideally until the filling to the retreating region 24 completes the cap layer 26, deposition of a cap layer is stopped. However, since it cannot say that the processing on which the cap layer containing cobalt, tungsten, and boron is made to deposit is controlled easily and correctly, rather than the material needed, much material is made to deposit and it fills up with a retreating region sufficiently reliably. By this, the cap layer 26 comes to have the mushroom mold structure shown in Fig.4. The cap layer 26 functions as copper never diffusing to the interconnection layer formed at a next process. The cap layer can function as reducing electromigration.

[0013]

Fig.5 removes a part of cap layer 26 and the diffusion barrier layer 20 on the patterned dielectric layer 18 at 1 time of a process with the conventional CMP, eCMP, or other flattening methods. Some cross sectional views of the semiconductor wafer 10 of the Fig.4 after making it the whole upper surface of the dielectric layer 18 and the cap layer 26 become flat are shown. The surface roughness of the cap layer 26 is reduced by 1 time of a flattening process, and leakage current is reduced. Platen (rotary surface plate) of a CMP device Only one set is used and both the cap layer 26 and the diffusion barrier layer 20 are removed at 1 time of a CMP treatment process. It can lower by this reducing the number of CMP processes required in order to form a semiconductor device for a manufacturing cost. It protects so that it may not be subject to the influence of down stream processing of succession to the dielectric layer 18, until it is removed as the diffusion barrier layer 20 shows Fig.5 by [residual] carrying out after CMP removes the copper layer 22 which shows the diffusion barrier layer 20 to Fig.2. In not performing protection by the diffusion barrier layer 20, there is a possibility that contamination or a damage may occur in the dielectric layer 18 by following down stream processing. By [residual] carrying out, the dielectric layer 18 only exposes a barrier layer in the stage of the last of the CMP process of the Fig.5 for removing a barrier layer/cap layer.

[0014]

While referring to an embodiment suitable about the present invention, it has described, but if it is a person skilled in the art of this technical field, it

will be able to understand that many embodiments other than the embodiment which could change the present invention by many methods, and was disclosed in the still more specific form, and was described upwards can be taken. Therefore, an attached claim thinks that all the deformation of the present invention contained in true technical scope of the present invention is included.

[0015]

It has described upwards about a specific embodiment about the solution over an effect, other advantages, and a technical problem. however, no elements (group) which bring about an effect, an advantage, a problem-solving method, one of effects, an advantage, or a problem-solving method, or can be made still more remarkable should be interpreted as it being the required or fundamental characteristics or an element with one of claims, or all the indispensable claims.

[Brief Description of the Drawings]

[0016]

[Drawing 1]Some cross sectional views of the semiconductor wafer after forming an interconnection layer.

[Drawing 2]Some cross sectional views of the semiconductor wafer of the Fig.1 after removing a part of metal layer.

[Drawing 3]Some cross sectional views of the semiconductor wafer of the Fig.2 after removing another portion of a metal layer.

[Drawing 4]Some cross sectional views of the semiconductor wafer of the Fig.3 after forming a cap layer.

[Drawing 5]Some cross sectional views of the semiconductor wafer of the Fig.4 after removing a part of cap layer.

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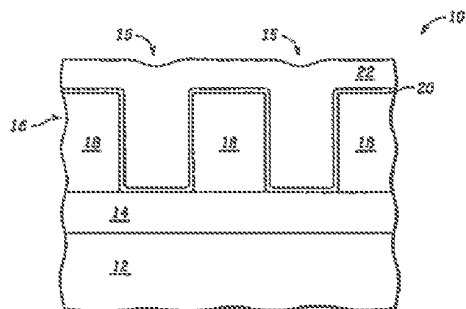
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CLAIMS DETAILED DESCRIPTION**DRAWINGS***** NOTICES ***

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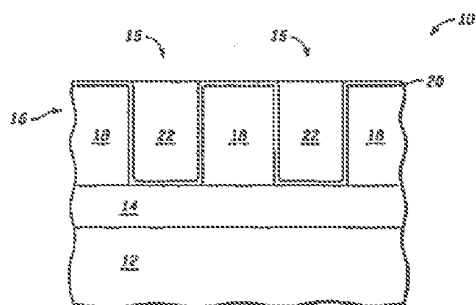
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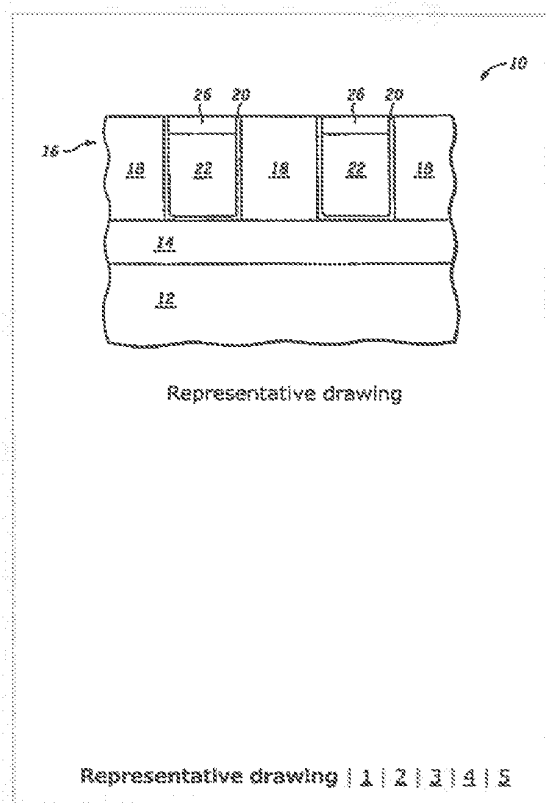
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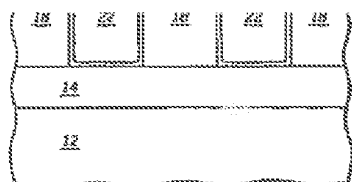
DRAWINGS**FIG. 1**

[Drawing 1]

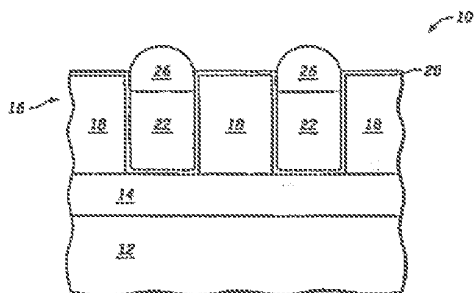
**FIG. 2**

[Drawing 2]

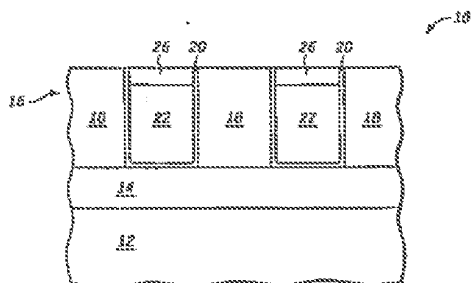


*FIG. 3*

[Drawing 3]

*FIG. 4*

[Drawing 4]

*FIG. 5*

[Drawing 5]

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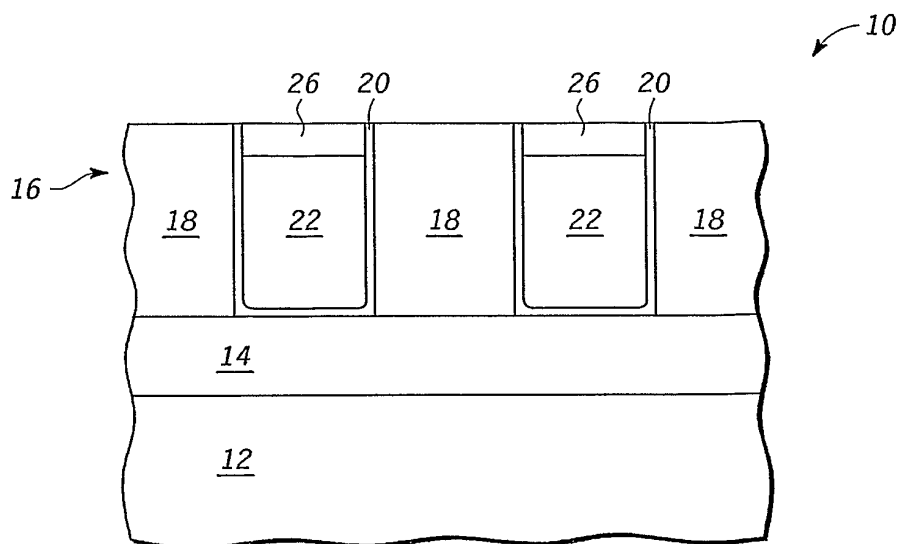
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ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR FORMING A CAPPING LAYER ON A SEMICONDUCTOR DEVICE



(57) Abstract: A method for making a semiconductor device includes forming a patterned dielectric (18) overlying active circuitry, the patterned dielectric having a plurality of cavities (15). A diffusion barrier (20) is formed over the patterned dielectric (18). A conductive layer (22) is formed over the diffusion barrier in the plurality of cavities. The conductive layer is etched back to be below a top surface of the dielectric, forming recessed areas (24) over the conductive layers in the plurality of cavities. The recessed areas are then filled with a capping film (26). The capping film and the diffusion barrier are removed to provide a relatively smooth planarized surface. Providing a relatively smooth planarized surface reduces leakage currents between conductors.

METHOD FOR FORMING A CAPPING LAYER ON A SEMICONDUCTOR DEVICE

5 FIELD OF THE INVENTION

The present invention relates generally to semiconductors, and more particularly, to a method for forming a capping layer on a semiconductor device.

10 BACKGROUND OF THE INVENTION

In integrated circuits, a dielectric layer is used to provide insulation around the interconnect wiring of the chip. Just as faster interconnect materials such as copper allow a signal to move faster through the chip, decreasing the capacitance factor of the insulating material also allows signals to travel across the interconnect faster because they have less interference with each other. The most common dielectric material is silicon dioxide. However, the semiconductor industry is constantly searching for commercially useful, lower capacitance dielectric materials, commonly referred to as low dielectric constant or low k materials.

20 When forming interconnects, the dielectric layer is patterned to form cavities such as trenches, vias, and the like. The cavities are then filled with a conductive material such as copper. To prevent electro-migration or diffusion, a relatively thin barrier layer is formed on the dielectric and the copper is formed on the barrier layer. The barrier layer is typically formed from Ta (tantalum). A chemical mechanical polishing (CMP) process is used to remove the copper and barrier layer from over the dielectric. The copper is recessed in the cavities and a conventional cobalt (Co) film doped with elements like tungsten (W), molybdenum (Mo), rhenium (Re), etc. are formed over the copper to prevent diffusion of copper into the surrounding dielectric material. This can enable integration of copper with low k materials. Also capping copper with these types of materials can enhance reliability by increasing electro-migration resistance. In order to be successful a very selective deposition of these films is required. Also, formation of the capping layer is highly dependent on the condition of the copper surface.

Typically, the cobalt films are deposited on the copper by electroless plating. The plating process may produce a cobalt film having a mushroom shaped profile. The mushroom shape extends above the surface of the dielectric and may cause unacceptable

leakage between conductors. In addition, the plating process results in cobalt film with a relatively rough surface.

Therefore, there is a need for a method to form a smooth capping film over copper that minimizes leakage currents between conductors.

5

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross-sectional view of a portion of a semiconductor wafer after formation of an interconnect level.

10 FIG. 2 illustrates a cross-sectional view of a portion of a semiconductor wafer of FIG. 1 after a portion of a metal layer has been removed.

FIG. 3 illustrates a cross-sectional view of a portion of a semiconductor wafer of FIG. 2 after a further portion of a metal layer has been removed.

15 FIG. 4 illustrates a cross-sectional view of a portion of the semiconductor wafer of FIG. 3 after formation of a capping layer.

FIG. 5 illustrates a cross-sectional view of a portion of the semiconductor wafer of FIG. 4 after removal of a portion of the capping layer.

DETAILED DESCRIPTION

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Generally, the present invention provides a method for forming a capping layer on top of a conductive metal layer that fills a cavity, such as a via or trench in an interconnect level of a semiconductor device. A purpose of the capping layer is to prevent diffusion of the conductive metal into subsequent interconnect levels within the device.

25 An active circuitry layer is formed on a substrate. The interconnect level is formed on top of the active circuitry level by depositing a dielectric layer and patterning the dielectric layer to form cavities, which can be vias, trenches, and the like. A diffusion barrier layer, such as tantalum or tantalum nitride, is deposited over the patterned dielectric layer such that the cavities and the top of the patterned dielectric layer are lined with the diffusion barrier
30 layer. A conductive metal, such as copper, is deposited over the diffusion barrier layer, filling the cavities and forming a blanket film over the patterned dielectric layer. The diffusion barrier layer prevents diffusion of the conductive metal into the dielectric layer. The blanket film of the conductive metal is removed by chemical mechanical polishing

(CMP) or other planarization method and the conductive metal remains in the cavities. The diffusion barrier layer is not substantially removed with the blanket film of the conductive metal, or in a separate planarization step, and remains on the surface of the patterned dielectric. This remaining diffusion barrier layer protects the dielectric layer from damage
5 from further processing, such as CMP. The conductive metal remaining in the cavities is then recessed through selective chemical etching or deliberate dishing through CMP or other planarization process. The capping layer of cobalt or cobalt doped with other conductive elements is then deposited through electroless plating or other deposition process such that it overfills the recessed area above the conductive metal. The capping layer extending above
10 the cavity and the barrier layer on top of the patterned dielectric layer is removed by a single CMP process or other planarization process. The surface roughness of the capping layer is reduced through this planarization process resulting in reduced leakage.

By leaving the diffusion barrier layer on top of the patterned dielectric layer after the conductive metal layer is removed, the dielectric surface is not exposed during the deposition
15 of the capping layer or during a substantial portion of the simultaneous planarization of the capping layer and removal of the diffusion barrier layer. By not exposing the dielectric layer to the capping layer deposition process, diffusion of materials used in the capping layer deposition process is significantly reduced. In the case of electroless deposition of the capping layer, the remaining diffusion barrier layer substantially prevents the diffusion of
20 metal ions into the dielectric layer resulting in reduced leakage caused by trapping of conductive materials. The remaining diffusion barrier layer also provides additional mechanical strength during the simultaneous planarization of the capping layer and substantial removal of the diffusion barrier layer resulting in reduced damage of the dielectric film. The benefits of reduced mechanical damage and reduced diffusion of contaminants into
25 the dielectric layer are greater when the dielectric layer is a lower dielectric constant material. Furthermore, the method of forming the capping layer is simplified by planarizing the capping layer and removing the diffusion barrier layer remaining on the dielectric layer in one process step rather than in separate steps.

30 FIG. 1 illustrates a cross-sectional view of a portion of a semiconductor wafer 10. The semiconductor wafer is processed to produce semiconductor devices having integrated circuits implemented thereon. Semiconductor wafer 10 includes a substrate 12 and an active circuitry layer 14 containing a plurality of structures such as transistors, diodes, resistors and

other circuit elements. The transistors may be, for example, complementary metal-oxide semiconductor (CMOS) transistors. Substrate 12 can be silicon, silicon-on-insulator, silicon germanium, or other semiconductor material. An interconnect level 16 is formed on a surface of the circuitry layer 14. The interconnect layer 16 consists of a dielectric layer 18 which is
5 patterned to form cavities 15 and remaining vertical structures using conventional photolithography and etch processes. The cavities 15 can be vias, trenches and the like. In one embodiment, the dielectric layer 18 is a carbon-containing silicon oxide but it can be silicon dioxide, doped silicon dioxide, or a porous low dielectric constant material. A diffusion barrier layer 20 is deposited on the dielectric layer 18 and lines the top of the
10 patterned dielectric layer 18 and the sidewalls and bottoms of the cavities 15. The diffusion barrier is deposited by physical vapor deposition (PVD), chemical vapor deposition (CVD) or some other deposition method. In one embodiment, the diffusion barrier layer is tantalum (Ta) but can be tantalum nitride (Ta_N), titanium nitride (TiN) or other conductive material. A conductive metal layer 22 is deposited on the diffusion barrier layer 20 which fills the
15 cavities 15 and subsequently forms a blanket layer atop the patterned dielectric layer 18 and the diffusion barrier 20. The conductive metal layer 22 can be copper or other conductive metal and is deposited by electroplating, PVD or other deposition technique or combination thereof. In one embodiment, the conductive metal layer 22 can be deposited by forming a seed layer of copper by PVD (not shown) then electroplating copper on top of the seed layer.

20

FIG. 2 illustrates a cross-sectional view of the semiconductor device 10 of FIG. 1 after a portion of the conductive metal layer 22 has been removed using a conventional chemical mechanical polishing (CMP) process or another planarization method such as electrochemical mechanical polishing (eCMP). As illustrated in FIG. 2, all of conductive
25 metal layer 22 is removed except for the metal filling the cavities 15. The diffusion barrier layer 20 is not substantially removed in the CMP process. By leaving all or a substantial portion of the diffusion layer 20 atop the patterned dielectric layer 18, the patterned dielectric layer 18 is protected from subsequent processing steps.

30

FIG. 3 illustrates a cross-sectional view of the portion of the semiconductor wafer 10 of FIG. 2 after removal of a portion of the conductive metal layer 22 remaining in the cavities 15 to form recessed regions 24 such that the top surface of the remaining conductive metal layer 22 is below the top surface of the patterned dielectric layer 18. The recessed regions 24

in metal layer 22 can be formed by selective chemical etching or deliberate dishing through CMP, eCMP or other planarization process. Note that diffusion layer 20 is not removed at this time. Diffusion layer 20 protects dielectric layer 18 from contaminants and damage that may be caused by subsequent processing steps.

5

FIG. 4 illustrates a cross-sectional view of the semiconductor wafer 10 of FIG. 3 after selective deposition of capping layer 26. In one embodiment the capping layer 26 is deposited by electroless plating but other selective deposition techniques may be used. The capping layer 26 is a conductive material such as cobalt (Co) and can be doped with other elements such as tungsten (W) or boron (B). In one embodiment the capping layer 26 comprises cobalt (Co), tungsten (W) and boron (B). In the illustrated embodiment, the deposition of the capping layer 26 comprises applying a solution comprising borane, cobalt sulfate, and sodium tungstate or tungstic acid. Also, the capping layer 26 can be doped with elements like nickel (Ni), molybdenum (Mo), rhenium (Re), and phosphorus (P). Ideally, the capping layer 26 would be deposited until completely filling the recessed regions 24 and then stopped. But because deposition of a capping layer comprising cobalt, tungsten and boron may not be easily accurately controllable, more material than needed will be deposited to ensure the recesses are adequately filled. This results in the capping layer 26 having the mushroom shape illustrated in FIG. 4. The capping layer 26 functions to prevent copper from diffusing into any subsequent interconnect level. Also, the capping layer may function to reduce electro-migration.

FIG. 5 illustrates a cross-sectional view of the portion of the semiconductor wafer 10 of FIG. 4 after a portion of capping layer 26 and the diffusion barrier layer 20 on the patterned dielectric layer 18 are removed by conventional CMP, eCMP or other planarization method in one step such that the entire top surface of the dielectric layer 18 and the capping layer 26 are planar. Also, the surface roughness of capping layer 26 is reduced by the one planarization step resulting in reduced leakage. In addition, only one platen of a CMP tool is used to remove both the capping layer 26 and the diffusion barrier layer 20 in one CMP process step. This may reduce manufacturing costs by reducing the number of CMP steps required to manufacture the device. Also, by leaving the diffusion barrier layer 20 on after the CMP removal of copper layer 22 illustrated in FIG. 2, the dielectric layer 18 is protected from subsequent processing steps until it is removed as illustrated in FIG. 5. Without the

protection provided by diffusion barrier layer 20, the subsequent processing steps may cause contamination or damage to the dielectric layer 18. By leaving the barrier layer on, the dielectric layer 18 is only exposed at the end of the barrier layer/capping layer CMP step of FIG. 5.

5

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above. Accordingly, it is intended by the appended claims to cover all

10 modifications of the invention which fall within the true scope of the invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element

15 of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

20

CLAIMS

What is claimed is:

5

1. A method for making a semiconductor device, comprising:

providing a semiconductor substrate having overlying active circuitry;

forming a patterned dielectric over the active circuitry, wherein the patterned dielectric has a cavity;

10

forming a diffusion barrier over the patterned dielectric wherein the cavity is lined with the diffusion barrier and a top surface of the patterned dielectric is coated with the diffusion barrier;

forming a conductive layer over the diffusion barrier wherein the conductive layer fills the cavity;

15

etching the conductive layer to remove the conductive layer from over the top surface of the diffusion barrier, without removing a substantial portion of the diffusion barrier;

forming a recessed region in the conductive layer in the cavity, wherein the recessed region is below the top surface of the patterned dielectric layer;

20

filling the recessed region with a capping layer; and

removing the diffusion barrier from over the top surface of the patterned dielectric and a portion of the capping layer, wherein the diffusion barrier is removed over the top surface of the patterned dielectric and a substantially planar surface is formed between the top surface of the patterned dielectric layer and a top surface of the capping layer.

25

2. The method of claim 1 wherein the etching the conductive layer, comprises:

performing chemical mechanical polishing (CMP); and

30

after the performing the CMP, applying a chemical etchant that is selective between the diffusion barrier and the conductive layer.

3. The method of claim 1, wherein removing the diffusion barrier from over the top surface of the patterned dielectric and a portion of the capping layer comprises removing the diffusion barrier and the portion of the capping layer during one chemical mechanical polishing (CMP) process step.

5

4. The method of claim 1, wherein the patterned dielectric comprises a low k dielectric, the conductor layer comprises copper, the diffusion barrier comprises tantalum, and the capping layer comprises cobalt.

10 5. The method of claim 4, wherein the capping layer further comprises tungsten and boron.

6. The method of claim 1, wherein the etching the conductive layer comprises performing CMP to remove the conductive layer over the top surface of the patterned
15 dielectric layer and dish out a portion of the conductive layer in the cavity to form the recessed region.

7. The method of claim 1, wherein the filling the recessed region comprises performing selective deposition of cobalt tungsten boron.

20

8. The method of claim 7, wherein the performing the selective deposition comprises:
applying a solution comprising borane, cobalt sulfate, and sodium tungstate or
tungstic acid.

25 9. The method of claim 1, wherein the forming the conductive layer comprises electroplating copper.

10. The method of claim 1 wherein the etching the conductive layer comprises:
removing by CMP substantially all of the conductive layer over the top surface
30 of the patterned dielectric;
completely removing by CMP the conductive layer from over the top surface
of the patterned dielectric and leaving at least a portion of the diffusion
barrier over the top surface of the patterned dielectric; and

etching back the conductive layer in the cavity to form the recessed region.

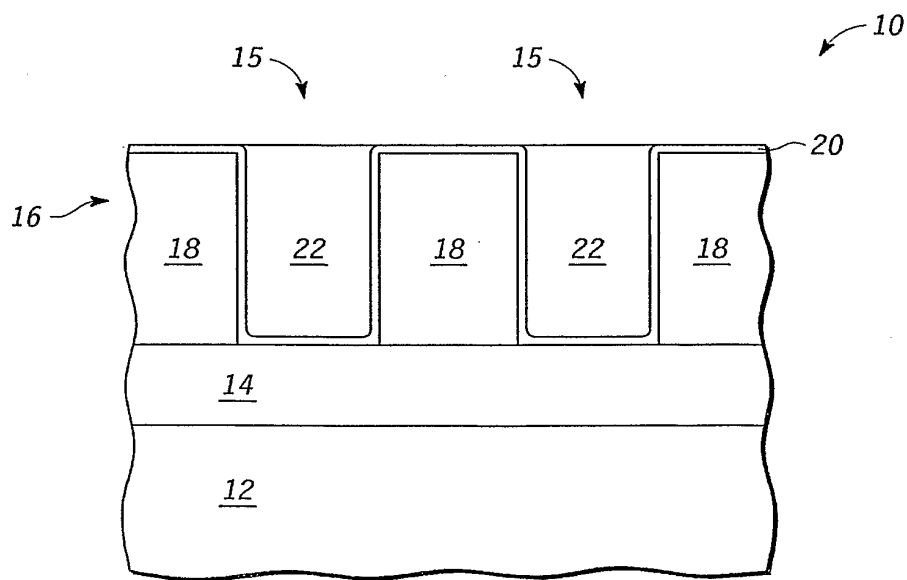
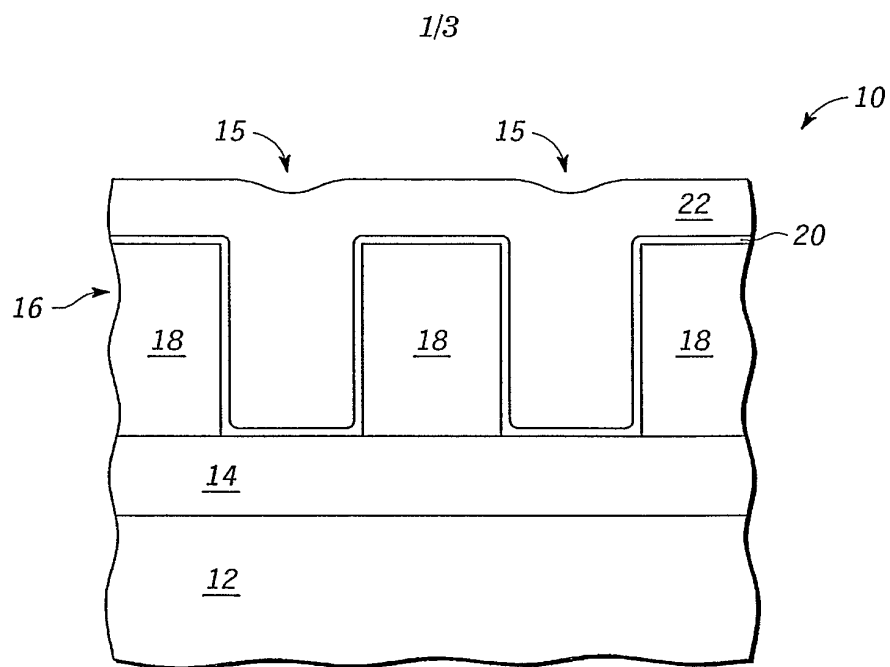
11. The method of claim 1, wherein the removing comprises performing CMP.

5 12. A method of forming a semiconductor device, comprising:
providing a semiconductor substrate having overlying active circuitry;
forming a patterned dielectric over the active circuitry, wherein the patterned
dielectric has a cavity;
forming a diffusion barrier over the patterned dielectric wherein the cavity is
10 lined with the diffusion barrier and a top surface of the patterned
dielectric is coated with the diffusion barrier;
by plating, forming a conductive layer over the diffusion barrier wherein the
conductive layer fills the cavity;
performing a step for removing the conductive layer over the top surface of
15 the patterned dielectric, leaving at least a portion of the diffusion
barrier over the top surface of the patterned dielectric, and removing a
portion of the conductive layer in the cavity to form a recessed region
below the top surface of the patterned dielectric layer;
filling the recessed region with a capping layer by selective deposition,
20 wherein a top surface of the capping layer is higher than the top
surface of the patterned dielectric layer; and
performing a step for removing the diffusion barrier over the top surface of the
patterned dielectric, removing a portion of the capping layer, and
forming a substantially planar surface between the top surface of the
25 patterned dielectric layer and a top surface of the capping layer.

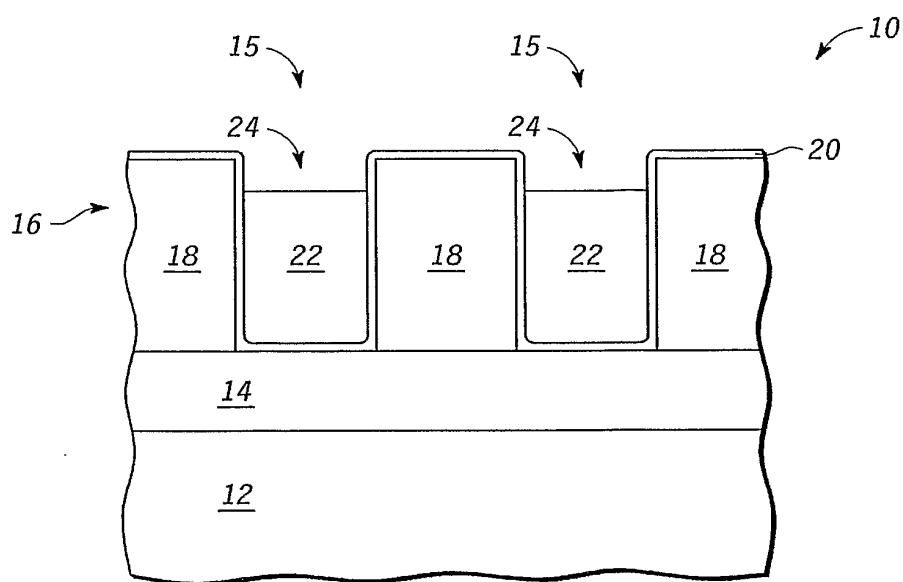
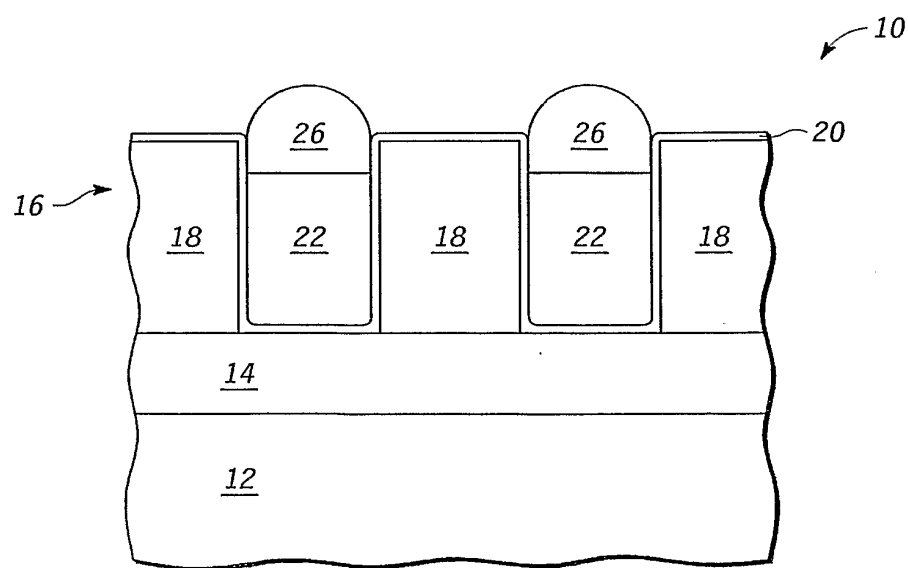
13. The method of claim 12, wherein the step for removing the diffusion barrier
comprises performing CMP.

30 14. The method of claim 12, wherein the step for removing the conductive layer
comprises performing CMP.

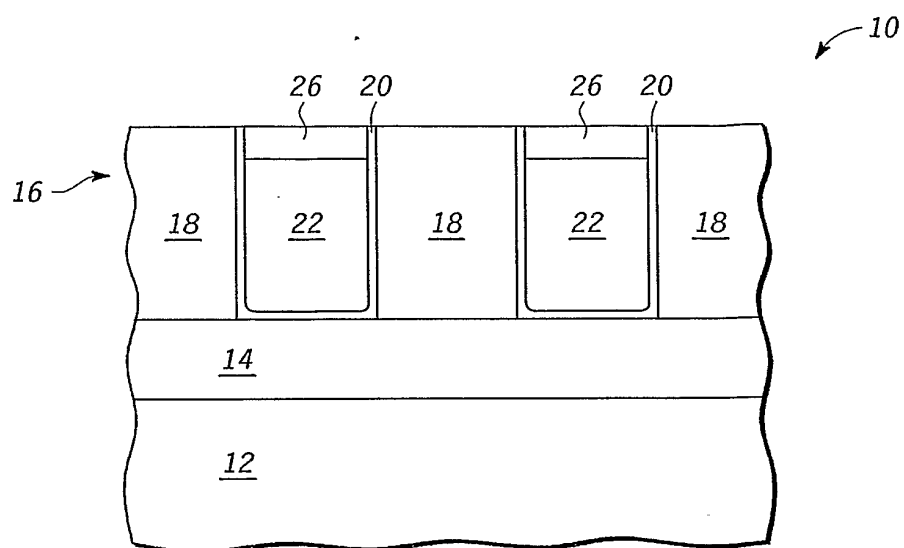
15. The method of claim 14 wherein the step for removing the conductive layer further comprises applying an etchant that is selective between the conductive layer and the diffusion barrier to form the recessed region.
- 5 16. The method of claim 12, wherein the conductive layer comprises copper and the capping layer comprises cobalt.
17. The method of claim 16, wherein the diffusion barrier comprises tantalum.
- 10 18. A method for making a semiconductor device, comprising:
providing a semiconductor substrate having overlying active circuitry;
forming a patterned dielectric over the active circuitry, wherein the patterned
dielectric has a cavity;
forming a diffusion barrier over the patterned dielectric wherein the cavity is
15 lined with the diffusion barrier and a top surface of the patterned
dielectric is coated with the diffusion barrier;
forming a conductive layer over the diffusion barrier wherein the conductive
layer fills the cavity;
planarizing the conductive layer and thereby exposing the diffusion barrier;
20 forming a recessed region in the cavity below the top surface of the patterned
dielectric layer;
filling the recessed region with a capping layer; and
planarizing top surfaces of the patterned dielectric and the capping layer and
thereby removing the diffusion barrier over the top surface of the
25 patterned dielectric.
19. The method of claim 18, wherein the conductive layer comprises copper, the diffusion barrier comprises tantalum, and the capping layer comprises cobalt.
- 30 20. The method of claim 18, wherein the planarizing the top surfaces and the planarizing the conductive layer are performed by CMP.



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*FIG. 3**FIG. 4*

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*FIG. 5*

Electronic Acknowledgement Receipt	
EFS ID:	28943430
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	45209
Filer:	Tatiana Rossin/Juanita Briscoe
Filer Authorized By:	Tatiana Rossin
Attorney Docket Number:	42P38794DC
Receipt Date:	17-APR-2017
Filing Date:	03-APR-2017
Time Stamp:	15:05:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	P38794DC_IDS_041717.pdf	25065	no	2
			808caa3fa114afb9aac9f0eeb77981c6a686c239		
Warnings:					

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	P38794DC_1449_041717.pdf	28341	no	1
			fca123ce7d10a5a939f55f2b9ff1b06f3991b467		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	KR1020100109932.pdf	794905	no	13
			d4aa533ce44eda56bb411f4925658799abdbd7cfe		
Warnings:					
Information:					
4	Foreign Reference	KR1020100109932_English_Translation.pdf	8198501	no	24
			6f5f487e57c0129ec3d490255c08e6e16feeaf7d		
Warnings:					
Information:					
5	Foreign Reference	WO2009098120A1.pdf	3286239	no	31
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Warnings:					
Information:					
6	Foreign Reference	JP2009506536.pdf	285431	no	10
			bfb2a1c544ab784a3ee96fc1b98d319f70ec7463		
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7	Foreign Reference	JP2009506536_English_Translation.pdf	310176	no	10
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8	Foreign Reference	WO2007024470A2.pdf	618548	no	14
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Warnings:					
Information:					
Total Files Size (in bytes):				13547206	
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:

Boyan Boyanov et al.

Application No.: 15/477,506

Filed: April 3, 2017

Art unit: 2898

Examiner: Not yet assigned

For: METHODS AND APPARATUSES TO
FORM SELF-ALIGNED CAPS

Confirmation No.: 2892

CERTIFICATE OF ELECTRONIC FILING
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April 17, 2017
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Juanita Briscoe
Name of Person Filing Correspondence
/Juanita Briscoe/ April 17, 2017
Signature Date

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed). It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

- X 37 C.F.R. §1.97(b).
- 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:
- A statement pursuant to 37 C.F.R. §1.97(e) or
- Charge Deposit Account No. 02-2666 \$180.00 for the fee under 37 C.F.R. § 1.17(p).
- 37 C.F.R. §1.97(d). If so, then enclosed with this Information Disclosure Statement are the following:
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- (2) Charge Deposit Account No. 02-2666 \$180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 17, 2017 /Tatiana Rossin/
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
15/477,506	04/03/2017	2668	1600	42P38794DC	7	1

CONFIRMATION NO. 2892

FILING RECEIPT



0000000090572901

45209

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
1279 Oakmead Parkway
Sunnyvale, CA 94085-4040

Date Mailed: 04/13/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Boyan Boyanov, Portland, OR;
Kanwal Jit Singh, Hillsboro, OR;

Applicant(s)

INTEL CORPORATION, Santa Clara, CA;

Power of Attorney: The patent practitioners associated with Customer Number 45209

Domestic Priority data as claimed by applicant

This application is a CON of 14/675,613 03/31/2015 PAT 9627321
which is a DIV of 13/991,899 06/05/2013 PAT 9373584
which is a 371 of PCT/US2011/059453 11/04/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

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Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 04/12/2017

page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/477,506**

Projected Publication Date: 07/20/2017

Non-Publication Request: No

Early Publication Request: No
Title

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

Preliminary Class

382

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 15/477,506			
APPLICATION AS FILED - PART I									
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY			
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)		
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280		
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600		
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720		
TOTAL CLAIMS (37 CFR 1.16(i))	7	minus 20 = *				x 80 =	0.00		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 420 =	0.00		
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00		
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00		
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600		
APPLICATION AS AMENDED - PART II									
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
			TOTAL ADD'L FEE			TOTAL ADD'L FEE			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)	
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =		
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =		
	Application Size Fee (37 CFR 1.16(s))								
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
			TOTAL ADD'L FEE			TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.									

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No. 42P38794DC
(maximum 12 characters)First Named Inventor Boyan BoyanovTitle: METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPSFiled by EFS-WEB on: April 3, 2017ADDRESS TO: **Commissioner for Patents**
P.O. Box 1450
Alexandria, Virginia 22313-1450**APPLICATION ELEMENTS**

See MPEP chapter 600 concerning utility patent application contents.

1. **Fee Transmittal Form (e.g., PTO/SB/17)**
(Submit an original and a duplicate for fee processing)
2. **Applicant Claims Small Entity Status. (37 CFR 1.27)**
3. X **Specification (Total Pages 25)**
(preferred arrangement set forth below)
 - Descriptive Title of the Invention
 - Cross Reference to Related Applications
 - Statement Regarding Fed sponsored R & D
 - Reference sequence listing, a table,
or a computer program listing appendix
 - Background of the Invention
 - Brief Summary of the Invention
 - Brief Description of the Drawings (if filed)
 - Detailed Description
 - Claim(s)
 - Abstract of the Disclosure
4. X **Drawings(s) (35 USC 113) (Total Sheets 10)**
5. X **Oath or Declaration (Total Pages 3)**
 - a. Newly Executed (Original or Copy)
 - b. X Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 18 completed)
 - i. DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
 - c. Unsigned.
6. X Application Data Sheet. (37 CFR 1.76)
7. CD-ROM or CD-R in duplicate, large table or Computer Program (Appendix)
8. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
 - a. Computer Readable Form (CRF)
 - b. Specification Sequence Listing on:
 - i. CD-ROM or CD-R (2 copies); or
 - ii. paper
 - c. Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS	
9.	☐ Assignment Papers (cover sheet & documents(s))
10.	☒ a. Separate 37 CFR 3.73(b) Statement (where there is an assignee)
	☒ b. Power of Attorney
11.	☐ English Translation Document (if applicable)
12.	☒ a. Information Disclosure Statement (IDS)/PTO-1449
	☐ b. Copies of IDS Citations
13.	☐ Preliminary Amendment
14.	☐ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
15.	☐ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16.	☐ Nonpublication Request under 35 U.S.C. 122(b)(2)(B)(i). <u>Applicant must attach form PTO/SB/35 or its equivalent.</u>
17A.	☐ Claim for Foreign Priority
17B.	☒ Other: <u>Transmittal For Power Of Attorney To One Or More Registered Practitioners</u>
17C. ☒ Pursuant to 37 C.F.R. 1.136(a)(3), applicant(s) hereby request and authorize the U.S. Patent and Trademark Office to (1) treat any concurrent or future reply that requires a petition for extension of time as incorporating a petition for extension of time for the appropriate length of time and (2) charge all required fees, including extension of time fees and fees under 37 C.F.R. 1.16 and 1.17, to Deposit Account No. 02-2666.	
18. If a CONTINUING APPLICATION , check appropriate box, and supply the requisite information below <u>and in the first sentence of the specification following the title (e.g., by way of preliminary amendment)</u> , or in an Application Data Sheet Under 37 C.F.R. 1.76:	
☒ Continuation	☐ Divisional
☐ Continuation-in-part (CIP)	☐ Group Art Unit
Of Prior Application No.: <u>14/675,613</u>	Examiner <u>Fortich, Rodolfo D.</u>
Which is a divisional of prior application no. 13/991,899 filed June 5, 2013, now issued as U.S. Patent No. 9,373,584 issued June 21, 2016, which is a national stage entry of PCT/US2011/059453 filed November 4, 2011..	
Applicant(s): Also include a Preliminary Amendment to amend the specification to claim priority. For CONTINUATION AND DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation <u>can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.</u>	
19.	Correspondence Address
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	FAX <u>(408) 720-8383</u>
Name (PRINT/TYPE): <u>Tatiana Rossin</u> Registration No.: <u>56,833</u>	
Signature: <u>/Tatiana Rossin/</u> Date: <u>April 3, 2017</u>	

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
First Named Inventor/Applicant Name:		Boyan Boyanov		
Filer:		Tatiana Rossin/Juanita Briscoe		
Attorney Docket Number:		42P38794DC		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	28815387
Application Number:	15477506
International Application Number:	
Confirmation Number:	2892
Title of Invention:	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
First Named Inventor/Applicant Name:	Boyan Boyanov
Customer Number:	45209
Filer:	Tatiana Rossin/Juanita Briscoe
Filer Authorized By:	Tatiana Rossin
Attorney Docket Number:	42P38794DC
Receipt Date:	03-APR-2017
Filing Date:	
Time Stamp:	15:00:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1600
RAM confirmation Number	040417INTEFSW00001563504238
Deposit Account	
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	P38794DC_ADS.pdf	111610	no	9
			fb8cf68d25194ec9b03c721442e47b4c554548f8		
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
2		P38794DC_Application.pdf	140535	yes	25
			f590821351bfe9aa1b4c0f865e18b24b4b8587d8		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Abstract		25	25	
	Claims		23	24	
	Specification		1	22	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P38794D_Figures.pdf	143856	no	10
			8771bd039dc1ff97e9e0937caa04e4410830bb9c		
Warnings:					
Information:					
4	Oath or Declaration filed	P38794DC_Declaration.pdf	357722	no	3
			67558cbc8869bdf767fd62876acc64b6f99baa7		
Warnings:					
Information:					

5	Power of Attorney	P38794DC_POA.pdf	261885	no	2
			8def335236e7b70cbd1be7dfd0367b4edbd51445		
Warnings:					
Information:					
6	Transmittal Letter	P38794DC_IDS.pdf	17747	no	2
			39364b6d914e3496a2998365fa86c243fc204b61		
Warnings:					
Information:					
7	Information Disclosure Statement (IDS) Form (SB08)	P38794DC_1449.pdf	161851	no	5
			30fef2a1f5ae1c1a3c4557c88a6a2588211f2190		
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8	Transmittal of New Application	42P38794DC_Utility_Transmittal.pdf	35992	no	2
			2f59487aa275cfd6b4a16a63c56ceb4f510b49e8		
Warnings:					
Information:					
9	Fee Worksheet (SB06)	fee-info.pdf	34956	no	2
			9696407a5be0df421e2c79969db00b7dceeade6		
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Total Files Size (in bytes):			1266154		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--------------------------	---

Inventor Information:

Inventor 1					Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Boyan		Boyanov			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	Portland	State/Province	OR	Country of Residence	US	
Mailing Address of Inventor:						
Address 1		15760 NW Rondos Drive				
Address 2						
City	Portland	State/Province	OR			
Postal Code	97229	Country	US			
Inventor 2					Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Kanwal	Jit	Singh			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	Hillsboro	State/Province	OR	Country of Residence	US	
Mailing Address of Inventor:						
Address 1		1055 NE Creeksedge Drive				
Address 2						
City	Hillsboro	State/Province	OR			
Postal Code	97124	Country	US			
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add	

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).
--

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

☐ An Address is being provided for the correspondence information of this application.			
Customer Number	45209		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
Attorney Docket Number	42P38794DC	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	45209		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
	Continuation of	14675613	2015-03-31		
Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14675613	Division of	13991899	2013-06-05	9373584	2016-06-21
Prior Application Status	Pending		Remove		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)		
13991899	a 371 of international	PCT/US2011/059453	2011-11-04		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Remove
			Access Code ⁱ (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
Clear			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	INTEL CORPORATION		
Mailing Address Information For Applicant:			
Address 1	2200 Mission College Blvd.		
Address 2			
City	Santa Clara	State/Province	CA
Country	US	Postal Code	95052
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	Given Name	Middle Name	Family Name	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		State/Province	
Country ⁱ		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Tatiana Rossin/		Date (YYYY-MM-DD)	2017-04-03	
First Name	Tatiana	Last Name	Rossin	Registration Number	56,833
Additional Signature may be generated within this form by selecting the Add button.					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	42P38794DC
		Application Number	
Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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ABSTRACT

At least one conductive line in a dielectric layer over a substrate is recessed to form a channel. The channel is self-aligned to the conductive line. The channel can be formed by etching the conductive line to a predetermined depth using a chemistry comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation. A capping layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is configured to contain the capping layer within the width of the conductive line.

CLAIMS

What is claimed is:

1. An apparatus, comprising:
at least one first conductive line in a dielectric layer over a substrate, the dielectric layer having a top boundary;
a channel in the dielectric layer on the at least one first conductive line, the channel comprising a sidewall between the at least one first conductive line and the top boundary,
and
a first capping layer comprising cobalt deposited in the channel on the at least one first conductive line comprising copper and cobalt and on the sidewall to prevent electromigration, wherein a top of the first capping layer is not higher than the top boundary .
2. The apparatus of claim 1, wherein the first capping layer is self-aligned to the first conductive line.
3. The apparatus of claim 1, further comprising
a second capping layer selectively deposited on the second conductive line within second sidewalls of the dielectric layer, the second conductive line being at a first spacing from the at least one first conductive line, and wherein the second capping layer is at the first spacing from the first capping layer.
4. The apparatus of claim 1, wherein the at least first conductive line is at a depth from 5 nanometers to 50 nanometers from a top surface of the dielectric layer.
5. The apparatus of claim 1, wherein the first conductive line is at a depth from a top surface of the dielectric layer that is from 10% to 50% of the thickness of the first conductive line.
6. The apparatus of claim 1, wherein the at least one first conductive line is an interconnect incorporated into a data processing system.

P38794DC

7. The apparatus of claim 1, wherein a spacing between the at least one first conductive line and a second conductive line in the dielectric layer is from 5 nm to 500 nm.

METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS

CROSS REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of co-pending U.S. Patent Application No. 14/675,613 filed on March 31, 2015, which is a divisional application of U.S. Patent Application No. 13/991,899 filed June 5, 2013, now issued as U.S. Patent No. 9,373,584, which is a U.S. National Phase application under 35 U.S.C. § 371 of International Application No. PCT/US2011/059453, filed November 4, 2011, entitled “METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS” and claims the priority benefit thereof.

FIELD

[0002] Embodiments of the present invention relate to the field of electronic device manufacturing, and in particular, to forming interconnect structures.

BACKGROUND

[0003] As the feature size of electronic devices shrinks, reliability of interconnects becomes critical to integrated circuit performance. Generally, electromigration refers to the transport of material caused by the movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms. The effect is especially important in applications where high current densities are used, for example, in microelectronics structures involving logic devices. Typically, a metal capping technology is used to prevent electromigration.

[0004] Figure 1A is a cross-sectional view of a typical interconnect structure having metal electromigration caps. As shown in Figure 1A, metal interconnect lines, for example lines 103 and 104, formed on a dielectric substrate 101 are originally spaced apart at a line spacing 105. The electromigration caps, for example, caps 111-113, can be grown on the respective interconnect lines above a flat surface of the substrate using electroless plating. Generally, the growth of the electromigration caps on the interconnect lines is isotropic. The electromigration

cap can grow on the interconnect metal line vertically as well as laterally above the substrate. The lateral growth of the metal electromigration caps may generate overhang structures, for example, an overhang 109 that protrude over the substrate 101 outside the width of the interconnect lines. As shown in Figure 1A, the lateral growth of the metal caps reduces a line-to-line spacing from spacing 105 to spacing 107.

[0005] Typically, the size of the overhang 109, is about 50% of the cap thickness. For example, if the two neighboring metal caps have the thickness of about 10 nanometers (“nm”), the total size of their overhangs can be about 2x5nm. As such, the line-to-line spacing can be reduced, for example, by a factor of two from about 20 (nm) to about 10 nm.

[0006] Figure 1B is a top view of a typical interconnect structure having metal electromigration caps electrolessly grown over a flat surface of substrate 121 having interconnect lines, such as an interconnect line 123. As shown in Figure 1B, the lateral growth of the metal caps above the substrate increases the line edge roughness (“LER”) and reduces line-to-line spacing. As shown in Figure 1B, the line-to-line spacing, for example, a line-to-line spacing 125, varies uncontrollably. Both the increased LER and reduced line-to-line spacing negatively impact on the reliability of the interconnect structures, increase the risk of current shorting that may lead to the failure of the entire integrated circuit device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements, in which:

[0008] Figure 1A is a cross-sectional view of a typical interconnect structure having metal electromigration caps.

[0009] Figure 1B is a top view of a typical interconnect structure having metal electromigration caps.

[0010] Figure 2A shows a cross-sectional view of a substrate to fabricate an interconnect structure according to one embodiment of the invention.

[0011] Figure 2B is a view similar to Figure 2A, after a dielectric layer is formed over the substrate according to one embodiment of the invention.

[0012] Figure 2C is a view similar to Figure 2B, after a photoresist layer is deposited over the dielectric layer to form one or more openings in the dielectric layer according to one embodiment of the invention.

[0013] Figure 2D is a view similar to Figure 2C, after one or more openings are formed in the dielectric layer according to one embodiment of the invention.

[0014] Figure 2E is a view similar to Figure 2D, after a conductive layer is deposited over the dielectric layer according to one embodiment of the invention.

[0015] Figure 2F is a view similar to Figure 2E, after portions of conductive layer and the base layer are removed from the top surface of the dielectric layer outside the openings to form patterned conductive lines according to one embodiment of the invention.

[0016] Figure 2G is a view similar to Figure 2F, after conductive lines in a dielectric layer over a substrate are recessed according to one embodiment of the invention.

[0017] Figure 2H is a view similar to Figure 2G, after capping layers are selectively deposited onto the respective recessed conductive lines in the channels to prevent electromigration according to one embodiment of the invention.

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[0018] Figure 3A is a three-dimensional view 300 of an interconnect structure after recessing the conductive lines in a dielectric layer over a substrate according to one embodiment of the invention.

[0019] Figure 3B is a view 310 similar to Figure 3A, after capping layers are deposited into the respective channels formed by the recessed conductive lines according to one embodiment of the invention.

[0020] Figure 4 is a top view of an interconnect structure 400 having capping layers selectively deposited within channels formed by the recessed conductive lines in a dielectric layer over a substrate according to one embodiment of the invention.

[0021] Figure 5 shows a block diagram of an exemplary embodiment of a data processing system 500 having one or more electronic devices, e.g., transistors, memories, such as a memory 504, and a memory 518, processing logic devices, such a processing logic device 526, and any other integrated circuit and microelectronic devices that are built using methods described herein.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0022] In the following description, numerous specific details, such as specific materials, dimensions of the elements, etc. are set forth in order to provide thorough understanding of one or more of the embodiments of the present invention. It will be apparent, however, to one of ordinary skill in the art that the one or more embodiments of the present invention may be practiced without these specific details. In other instances, semiconductor fabrication processes, techniques, materials, equipment, etc., have not been described in great details to avoid unnecessarily obscuring of this description. Those of ordinary skill in the art, with the included description, will be able to implement appropriate functionality without undue experimentation.

[0023] While certain exemplary embodiments of the invention are described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described because modifications may occur to those ordinarily skilled in the art.

[0024] Reference throughout the specification to “one embodiment”, “another embodiment”, or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearance of the phrases “in one embodiment” or “for an embodiment” in various places throughout the specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0025] Moreover, inventive aspects lie in less than all the features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of this invention. While the invention has been described in terms of several embodiments, those skilled in the art will recognize that the invention is not limited to the

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embodiments described, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative rather than limiting.

[0026] Methods and apparatuses to control a line edge roughness (“LER”) and line-to-line spacing in deposition of self-aligned metal caps are described herein. At least one conductive line is recessed to form a channel in a dielectric layer over a substrate. A capping layer to prevent electromigration is deposited on the recessed conductive line in the channel. The channel is self-aligned to the conductive line. The channel is configured to contain the capping layer within the width of the conductive line. That is, the interconnect line is recessed to contain the cap growth within a channel self aligned to the interconnect line. The channel can be formed by etching the conductive line to a predetermined depth using a chemistry comprising an inhibitor to provide uniformity of etching independent of a crystallographic orientation, as described in further detail below. Methods and apparatuses described herein can be used to control the increase in LER associated with selectively deposited electromigration caps, for example, electroless cobalt caps. That is, an increase in LER and reduction in line-to-line spacing typically associated with the electromigration caps selectively deposited on the metal interconnect lines can be prevented by containing an electroless cap within a recess that is self-aligned to an interconnect line. Eliminating an increase in LER and preventing from reducing of the line-to-line spacing can decrease the risk of failure and increase the manufacturing yield of the electronic devices having reduced (e.g., nanometer scale) dimensions. The electronic devices can be, for example, computer system architecture devices, e.g., transistors, memories, logic devices, and any other integrated circuit and microelectronic devices.

[0027] Figure 2A shows a cross-sectional view 200 of a substrate to fabricate an interconnect structure according to one embodiment of the invention. In one embodiment, substrate 201 includes a monocrystalline silicon. In one embodiment, substrate 201 includes a silicon-on-insulator (“SOI”). For alternate embodiments, substrate may comprise compound

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semiconductors, e.g., indium phosphide, gallium arsenide, gallium nitride, silicon germanium, and silicon carbide. In another embodiment, substrate 201 may include e.g., glass, and quartz. Substrate 201 may include one or more metallization layers of integrated circuits having active and passive devices, e.g., transistors, switches, optoelectronic devices, capacitors, resistors, interconnects (not shown). The one or more metallization layers of integrated circuits of substrate 201 may be separated from adjacent metallization layers by a dielectric material (not shown), e.g., interlayer dielectric. The adjacent metallization layers may be electrically interconnected by vias (not shown).

[0028] Figure 2B is a view similar to Figure 2A, after a dielectric layer 203 is formed over the substrate 201 according to one embodiment of the invention. In one embodiment, dielectric layer 203 is an interlayer dielectric (“ILD”). In one embodiment, dielectric layer 203 is a low-k dielectric, e.g., silicon dioxide, silicon oxide, and carbon doped oxide (“CDO”), or any combination thereof. In one embodiment, Dielectric layer 203 includes a nitride, oxide, a polymer, phosphosilicate glass, fluorosilicate (“SiOF”) glass, organosilicate glass (“SiOCH”), or any combination thereof. In one embodiment, dielectric layer 203 includes a spin-on low-k dielectric material. In one embodiment, dielectric layer 203 is silicon dioxide. In another embodiment, dielectric layer 203 is silicon nitride. dielectric layer 203 may be deposited using any suitable deposition technique. In one embodiment, dielectric layer 203 may be deposited using blanket deposition technique, for example, chemical vapor deposition (“CVD”), sputtering, spin-on, or another thin film deposition technique. In one embodiment, dielectric layer 203 is deposited to the thickness in the approximate range of 50nm to 2μm.

[0029] Figure 2C is a view similar to Figure 2B, after a photoresist layer 204 is deposited over dielectric layer 203 to form one or more openings in dielectric layer 203 according to one embodiment of the invention. In one embodiment, photoresist layer 204 is deposited on a hard mask layer 202 formed on dielectric layer 203, as shown in Figure 2C. In another embodiment, photoresist layer 204 is deposited directly onto dielectric layer 203. As shown in Figure 2C,

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photoresist layer 204 and hard mask layer 202 are patterned and etched to form openings, such as an opening 220. Patterning and etching of the photoresist and hard mask is known to one of ordinary skill in the art of microelectronic device manufacturing. Patterning and etching of the photoresist may be performed using one of the techniques known to one of ordinary skill in the art of microelectronic device manufacturing. The technique may include masking the photoresist layer, exposing the masked layer to light, and then developing the unexposed portions to remove the portions of the photoresist layer that are exposed to light to form a window in the photoresist layer. In one embodiment, the process of exposing to light and removing the photoresist layer may be performed in a plasma reactor. The opening in hard mask 202 may be etched to expose a portion of dielectric layer 203 using a dry etching, e.g., reactive ion etching ("RIE"), wet etching, or any combination thereof techniques.

[0030] Figure 2D is a view similar to Figure 2C, after one or more openings, such as an opening 206, are formed in dielectric layer 203 according to one embodiment of the invention. In one embodiment, the openings are, such as opening 206, is etched through openings in hard mask 202, such as opening 220. In another embodiment, the openings are formed by etching the dielectric layer through the openings in patterned photoresist 204 deposited directly onto dielectric layer 203. In one embodiment, the openings in the dielectric layer 203, for example, trenches, are formed using an anisotropic dry etching, e.g., plasma etching. In another embodiment, the openings in the dielectric layer 203 are formed using dry etching, wet etching, or a combination thereof techniques known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the openings in dielectric layer 203 has the width in the approximate range of 0.005microns ("μm ") to 5 μm, and the depth in the approximate range of 0.005 μm to 10 μm. In one embodiment, the size of openings is determined by the size of a conductive line formed within ILD 203 later on in the process.

[0031] After forming the openings, such as opening 206, the photoresist and hard mask are removed. Removing of the photoresist and the hard mask from dielectric layer 203 is known to

one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the photoresist and hard mask may be removed using a chemical technique, mechanical technique, or both.

[0032] Figure 2E is a view similar to Figure 2D, after a conductive layer 205 is deposited over dielectric layer 203 according to one embodiment of the invention. As shown in Figure 2E, forming of the conductive layer 205 involves filling the one or more openings in dielectric layer 203 with a conductive material to form one or more conductive lines. In one embodiment, a base layer (not shown) is first deposited on dielectric layer 203 covering the internal sidewalls and bottom of the openings, and then a conductive layer 205 is deposited on the base layer. In one embodiment, the base layer includes a conductive seed layer (not shown) deposited on a conductive barrier layer (not shown). The seed layer can include copper, and the conductive barrier layer can include aluminum, titanium, tantalum, tantalum nitride, and the like metals. The conductive barrier layer can be used to prevent diffusion of the conductive material from the seed layer, e.g., copper, into ILD 203. Additionally, the conductive barrier layer can be used to provide adhesion for the seed layer (e.g., copper). In one embodiment, to form the base layer, the conductive barrier layer is deposited onto the dielectric layer 203 covering the sidewalls and bottom of the opening, and then the seed layer is deposited on the conductive barrier layer. In another embodiment, the conductive base layer includes the seed layer that is directly deposited onto dielectric layer 203 covering the sidewalls and bottom of the openings. Each of the conductive barrier layer and seed layer may be deposited using any thin film deposition technique known to one of ordinary skill in the art of semiconductor manufacturing, e.g., by sputtering, blanket deposition, and the like. In one embodiment, each of the conductive barrier layer and the seed layer has the thickness in the approximate range of 1 to 100 nm. In one embodiment, the barrier layer may be a thin dielectric that has been etched to establish conductivity to the metal layer below. In one embodiment, the barrier layer may be omitted

altogether and appropriate doping of the copper line may be used to make a “self-forming barrier”.

[0033] Conductive layer 205 fills the openings, such as an opening 206, and covers portions of the base layer (not shown) outside of the openings that are on top of dielectric layer 203. In one embodiment, conductive layer 205 e.g., copper, is deposited onto the seed layer of base layer of copper, by an electroplating process. In one embodiment, conductive layer 205 is deposited into the openings using a damascene process that is known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, conductive layer 205 is deposited onto the seed layer using one of selective deposition techniques known to one of ordinary skill in the art of semiconductor manufacturing, e.g., electroplating, electroless plating, and the like. In one embodiment, the choice of a material for conductive layer 205 determines the choice of a material for the seed layer. For example, if the material for conductive layer 205 includes copper, the material for the seed layer also includes copper. In one embodiment, conductive layer 205 includes e.g., copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), Vanadium (V), Molybdenum (Mo), palladium (Pd), gold (Au), silver (Au), platinum Pt, or any combination thereof.

[0034] Figure 2F is a view similar to Figure 2E, after portions of conductive layer 205 and the base layer are removed from the top surface of dielectric layer 203 outside the openings to form patterned conductive lines, such as a conductive line 208 according to one embodiment of the invention. Portions of conductive layer 205 may be removed chemically, e.g., using etching, mechanically, e.g., using polishing, or by a combination of thereof techniques, e.g., using a chemical-mechanical polishing (“CMP”) technique known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, one or more patterned conductive lines are formed within dielectric layer 203 using methods described above. In another embodiment, the conductive lines are formed by patterning and etching of the conductive layer

deposited on the top surface of dielectric layer 203. Patterning and etching of the conductive layer deposited on the top surface of the dielectric layer 203 is known to one of ordinary skill in the art of microelectronic device manufacturing. In one embodiment, the thickness of the conductive line, for example, a thickness 211 is in the approximate range of $0.015\mu\text{m}$ to $1\mu\text{m}$. In one embodiment, the width of the conductive line, for example, a width 209 is in the approximate range of 5nm to about 500nm. In one embodiment, the spacing between the conductive lines, for example, a spacing 207, is from about 5nm to about 500nm. In one embodiment, the spacing between the conductive lines is from about 2nm to about 100nm.

[0035] Figure 2G is a view similar to Figure 2F, after the conductive lines, for example, a conductive line 208, in a dielectric layer over a substrate are recessed according to one embodiment of the invention. As shown in Figure 2G, channels, such as a channel 212, are formed in dielectric layer 203. As shown in Figure 2G, channels, such as channel 212, have sidewalls made of dielectric layer 203, such as sidewalls 214 and 216, and a bottom made of a respective conductive line, such as a bottom 218 made of conductive line 208.

[0036] In one embodiment, the channel has depth, such as a depth 213 from about 5 nm to about 50nm. In one embodiment, the depth of the channel is from about 2 nm to about 20nm. In one embodiment, the channel has depth that is from about 10% to about 50% of the thickness of the conductive line, such as a thickness 211 shown in Figure 2F. In one embodiment, the conductive lines are recessed to the depth, which is determined based on the thickness of a capping layer, as described in further detail below.

[0037] Figure 3A is a three-dimensional view 300 of an interconnect structure after recessing the conductive lines, such as a conductive line 305 and a conductive line 304, in a dielectric layer 303 over a substrate 301 according to one embodiment of the invention. Substrate 301, dielectric layer 303, and the conductive lines 305 and 304, can be, for example, any of the respective substrates, dielectric layers, and conductive lines, as described above. As shown in Figure 3A, channels, such as a channel 302 and a channel 307, are formed in a dielectric layer

303 over substrate 301 by recessing the conductive lines. As shown in Figure 3A, the channels are self-aligned to the respective conductive lines. For example, channel 307 is self-aligned to conductive line 305 and channel 302 is self-aligned to conductive line 304. As shown in Figure 3A, the length of the channel, e.g., a length 315 is along the length of the conductive line, and the width of the channel, e.g., a width 307 is along the width of the conductive line. In one embodiment, the length of the channel is substantially longer than the width of the channel. In one embodiment, the width of the channel is less than 100nm, and the length of the channel is at least 500nm. In one embodiment, the width of the channel is from about 5 nm to about 500nm, and the length of the channel is from about a few hundred nanometers to about a few hundred microns. As shown in Figure 3A, the conductive lines, such as conductive lines 305 and 304 are separated by a distance, such as a spacing 309. In one embodiment, the spacing between the conductive lines, such as lines 305 and 304 is from about 5nm to about 500nm. In one embodiment, the spacing between the conductive lines, such as lines 305 and 304 is from about 2nm to about 100nm.

[0038] In one embodiment, recessing the conductive lines, such as line 208, lines 304 and 305, involves wet etching the conductive lines uniformly independent of a crystallographic orientation using a chemistry containing an etchant, an oxidizer, an inhibitor, and a solvent. That is, adding an inhibitor and a solvent to the etchant provides uniform etching of the conductive material independent of a crystallographic orientation, by forming, during etching, a passivation layer (not shown) on the conductive material. The wet etch chemistry containing an etchant, an oxidizer, an inhibitor, and solvent provides control over the depth of the etching of the conductive line, so that only a portion (e.g., 5% to 50%) of the conductive line can be recessed.

[0039] In one embodiment, the chemistry to wet etch the conductive lines to provide a channel that is free from a pattern dependence and a crystallographic preference comprises between about 1% to about 40% by mass of an etchant, between about 1% to about 10% by mass of an

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oxidizer, and between about 0.1% to about 1% by mass of an inhibitor, and between about 1 to about 60% by mass of an organic solvent. In one embodiment, the chemistry to wet etch the conductive lines comprises an etchant from about 0.1% to about 70% by mass (depending on the etch rate of the etchant), an oxidizer from about 0.1% to about 10% by mass (depending on the strength of the oxidizer), an inhibitor from about 50 parts per million (ppm) to about 1% by mass; and a solvent between about 1 to about 60% by mass.

[0040] In one embodiment, the chemistry to etch the conductive lines can include an etchant, for example, a glycine, an ethylenediaminetetraacetic acid, an alpha-amino acid, a polycarboxylic acid, or a combination thereof; the oxidizer, for example, a peroxide, an ozone, a permanganate, a chromate, a perborate, a hypohalite, or a combination thereof, an inhibitor, for example, an azole, an amine, an amino acid, a phosphate, a phosphonate, or a combination thereof, and a solvent. The solvent can be an aqueous system (preferred), e.g., water, or an organic solvent. The examples of an organic solvents are propylene carbonate, sulfolane, glycol ethers, methylene chloride, and the like.

[0041] For example, regarding the etchant in the chemistry to etch copper conductive lines, Cu metal is typically in a zero oxidation state. In order to etch copper, the copper needs to be oxidized into a 0+n oxidation state where 'n' can be any of 1, 2, 3 or 4. Typically, 1st state and 2^d state are more common oxidation states of copper. For any molecule to act as an etchant, it needs to be able to bind copper in one of its oxidation states 1, 2, 3 or 4. This binding typically occurs through the use of group 15 (Nitrogen family), group 16 (Oxygen family) or group 17 (Halogen family) atoms in a molecule. In one embodiment, the etchant to etch copper conductive lines is an organic etchant, for example, any of glycine, ethylenediaminetetraacetic, alpha-amino acids, polycarboxylic acids (for example, citric acid that is a tricarboxylic acid), oxalic and malonic acids.

[0042] For example, an oxidizer in the chemistry to etch copper conductive lines is used to change the copper oxidation state from an insoluble copper metal to a soluble copper ion. The

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oxidizer can be chosen from any of the oxidizers, for example, any of peroxides (e.g., hydrogen peroxide), ozone, permanganates, chromates, perborates and hypohalites, and the like.

[0043] For example, to etch the copper constituting the current carrying line in a uniform and non-crystallographic orientation, it is important to add an inhibitor to the chemistry. The role of an inhibitor is to form a passivation layer (a polymeric compound formed from the molecules of the inhibitor binding copper in a specific and periodic manner). The formation of this passivation layer during the controlled etch of copper is critical to ensure uniformity of etching and preventing etching attacks (e.g., forming voids) along crystallographic (e.g., grain) boundaries. For example, any inhibitor that is not decomposed in the chosen oxidizer and etchant combination may be used in the chemistry to etch copper conductive lines. The classes of inhibitors are known to one of ordinary skill in the art of electronic device manufacturing. For example, any of organic inhibitors including azoles, amines, amino acids, phosphates and phosphonates can be used in the chemistry to etch the copper conductive lines.

[0044] In another embodiment, the conductive copper lines are recessed by wet etching using a chemistry comprising a citric acid and peroxide. A chemistry comprising citric acid and peroxide, however, typically has high etching rate that can be difficult to control. Additionally, an etching rate of the chemistry comprising citric acid and peroxide depends on a crystallographic orientation that may produce rough etched surface. Addition of a corrosion inhibitor, for example, benzotriazole ("BTA") to the chemistry, and dilution of the citric acid and peroxide in organic solvent can slow down the etching rate dramatically and eliminate the crystallographic nature of the etch, such as etching the voids in Cu along the grain boundaries producing a smooth surface.

[0045] In one embodiment, the conductive lines are recessed by wet etching that involves any of spraying, and pouring the etching chemistry onto the conductive lines. In one embodiment, the conductive lines are recessed by wet etching that involves immersing the conductive lines into the etching chemistry solution. In one embodiment, the conductive lines are recessed by wet

etching at a temperature from about 15°C to about 50°C for a predetermined time. In at least some embodiments, the conductive lines are recessed by dry etching, e.g., plasma etching.

[0046] Figure 2H is a view similar to Figure 2G, after the capping layers are selectively deposited onto the respective recessed conductive lines in the channels to prevent electromigration according to one embodiment of the invention. The conductive lines etched using the chemistry as described above, have a smooth uniform top surface to adhere the capping layer. As shown in Figure 2H, a capping layer 215 is deposited onto recessed conductive line 208 within channel 212. In one embodiment, the channel, such as channel 212, is configured to contain a capping layer within the width of the conductive line, e.g., width 209 shown in Figure 2F. That is, the recessed conductive line creates a channel which contains the growth of the capping layer within the channel that mitigates the reduction in line-to-line spacing and increase in LER. As shown in Figure 2H the capping layer 215 is located on the conductive line 208 within the sidewalls of the channel 212. In one embodiment, the capping layer is deposited on the recessed conductive line by an electroless deposition (e.g., plating), a chemical vapor deposition (“CVD”), a physical vapor deposition (“PVD”), or any other selective deposition techniques known to one of ordinary skill in the art of electronic device manufacturing. In one embodiment, a conductive line, such as line 208, comprises a first metal, and the capping layer comprises a second metal other than the first metal to prevent electromigration of the first metal from the conductive line. In one embodiment, the metal for the capping layer is heavier than the metal for the conductive line to prevent electromigration.

[0047] For example, the conductive line can be made of any of the metals including copper, aluminum. In one embodiment, the capping layer, such as capping layer 215, is made of cobalt (“Co”), cobalt electroless alloys, e.g., CoBP, CoWBP, CoWP, CoWB, CoWP, or a combination thereof. In another embodiment, a capping layer, such as capping layer 215, is made of nickel (“Ni”), Ni electroless alloys, e.g., NiBP, NiWBP, NiWP, NiWB, NiWP, or a combination thereof. In another embodiment, a capping layer, such as capping layer 215, is made of platinum

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("Pt") group metals, for example, Pt, Pd, Ru, Ir, Rh as pure elements or alloys. The typical alloy elements for Pt group metals are W, B, P. In yet another embodiment, a capping layer, such as capping layer 215, is made of refractory metals, for example, Ta, W, Mo, or a combination thereof.

[0048] In one embodiment, the Co capping layer is deposited within a channel onto the recessed Cu conductive layer. In one embodiment, Ni capping layer is deposited within a channel onto the recessed Cu conductive layer. In one embodiment, refractory metal capping layer is deposited within a channel onto the recessed Cu conductive layer.

[0049] In one embodiment, the capping layers comprising a Pt group metal, Co, Ni, or a combination thereof, are deposited onto the conductive layers, e.g., copper, aluminum, using any of an electroless deposition, and a vapor phase deposition, e.g., CVD. In one embodiment, the capping layers including refractory metals are deposited onto the conductive layers, e.g., copper, aluminum, using any of a CVD and PVD techniques known to one of ordinary skill in the art of electronic device manufacturing. In one embodiment, the thickness of the capping layer, e.g., a thickness 221, is from about 2 nm to about 50 nm. In one embodiment, the thickness of the capping metal layer is sufficient to prevent electromigration from the underlying conductive layer. In one embodiment, the capping layer has the thickness that is no greater than the depth of the channel within which the capping layer is deposited.

[0050] Figure 3B is a view 310 similar to Figure 3A, after capping layers are deposited into the respective channels formed by the recessed conductive lines according to one embodiment of the invention. As shown in Figure 3B, capping layers, such as a capping layer 311 and 319 are selectively deposited into respective channels, such as channel 302 and channel 307, as described above. As shown in Figure 3A, the capping layers are contained within their respective channels. As shown in Figure 3B, the capping layer 319 is separated from capping layer 311 by spacing 309. In one embodiment, the spacing between conductive lines 305 and 304 and the spacing between the capping layers 319 and 311 is the same.

[0051] Figure 4 is a top view of an interconnect structure 400 having capping layers selectively deposited within channels formed by the recessed conductive lines in a dielectric layer 401 over a substrate according to one embodiment of the invention. As shown in Figure 4, the LER of the interconnect lines, such as an interconnect line 403 is substantially reduced, the edges of the interconnect lines are smooth, and a line-to-line spacing, such as a line-to-line spacing 405 is increased and maintained between the lines. In one embodiment, the line-to-line spacing is increased by 2x cap thickness. This can result in rather dramatic decreases in electric field and time to dielectric breakdown, especially, for a future technology node having 20nm lines and 20nm spaces. The minimum cap thickness known to work today is 5nm. This means that with a conventional approach the line-line space would be 10nm instead of the 20nm drawn on a mask. Furthermore, currently, the size of the protrusions in the overhang tends to be about 50% of the cap thickness. For a typical cap thickness of 5-10nm using methods described above LER can be decreased by 3-5nm independent of line width. For a future 20 nm technology node, decrease in LER by 3-5nm can result in 15-20% increase in line-to-line spacing of an interconnect structure.

[0052] Figure 5 shows a block diagram of an exemplary embodiment of a data processing system 500 having one or more electronic devices, e.g., transistors, memories, such as a memory 504, and a memory 518, processing logic devices, such a processing logic device 526, and any other integrated circuit and microelectronic devices that are built using methods described herein. As shown in Figure 5, data processing system 500 includes a processor 502 having processing logic 526. In at least some embodiments, processing logic 526 contains at least one conductive line in a dielectric layer over a substrate, a channel in the dielectric layer over the one conductive line; and a capping layer on the at least one conductive line in the channel to prevent electromigration, as described herein. In at least some embodiments, each of the memories 504 and 518 contains at least one conductive line in a dielectric layer over a substrate,

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a channel in the dielectric layer over the one conductive line; and a capping layer on the at least one conductive line in the channel to prevent electromigration, as described herein

[0053] In alternative embodiments, the data processing system may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The data processing system may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The data processing system may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that data processing system. Further, while only a single data processing system is illustrated, the term “data processing system” shall also be taken to include any collection of data processing systems that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[0054] The exemplary data processing system 500 includes a processor 502, a main memory 504 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 506 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 518 (e.g., a data storage device), which communicate with each other via a bus 530.

[0055] Processor 502 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 502 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 502 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital

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signal processor (DSP), network processor, or the like. Processor 502 is configured to execute the processing logic 526 for performing the operations described herein.

[0056] The computer system 500 may further include a network interface device 508. The computer system 500 also may include a video display unit 510 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 512 (e.g., a keyboard), a cursor control device 514 (e.g., a mouse), and a signal generation device 516 (e.g., a speaker).

[0057] The secondary memory 518 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 531 on which is stored one or more sets of instructions (e.g., software 522) embodying any one or more of the methodologies or functions described herein. The software 522 may also reside, completely or at least partially, within the main memory 504 and/or within the processor 502 during execution thereof by the computer system 500, the main memory 504 and the processor 502 also constituting machine-readable storage media. The software 522 may further be transmitted or received over a network 520 via the network interface device 508.

[0058] While the machine-accessible storage medium 531 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine-readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state memories, and optical and magnetic media.

[0059] In alternative embodiments, Figure 5 illustrates a computing device 500. The computing device 500 houses a board 530. The board may include a number of components, including but

not limited to a processor 502 and at least one communication chip 508. The processor 502 is physically and electrically coupled to the board 530. In some implementations the at least one communication chip 508 is also physically and electrically coupled to the board 530. In further implementations, the communication chip 508 is integrated within the processor 502.

[0060] Depending on its applications, computing device 500 may include other components that may or may not be physically and electrically coupled to the board 530. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, a solid state drive, a compact disk (CD) drive, a digital versatile disk (DVD) drive, and so forth).

[0061] The communication chip 508 enables wireless communications for the transfer of data to and from the computing device 500. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 508 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 500 may include a plurality of communication chips 508. For instance, a first communication chip 508 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 1006 may be

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dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[0062] The processor 502 of the computing device 500 includes an integrated circuit die packaged within the processor 502. In some implementations of the invention, the integrated circuit die of the processor includes one or more devices, such as transistors or metal interconnects, that are formed using methods and apparatuses to control a line edge roughness and line-to-line spacing in deposition of self-aligned metal caps as described herein. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[0063] The communication chip 508 also includes an integrated circuit die packaged within the communication chip 508. In accordance with another implementation of the invention, the integrated circuit die of the communication chip includes one or more devices, such as transistors or metal interconnects, that are formed using methods and apparatuses to control a line edge roughness and line-to-line spacing in deposition of self-aligned metal caps as described herein.

[0064] In further implementations, another component housed within the computing device 600 may contain an integrated circuit die that includes one or more devices, such as transistors or metal interconnects, that are formed using methods and apparatuses to control a line edge roughness and line-to-line spacing in deposition of self-aligned metal caps as described herein.

[0065] In various implementations, the computing device 500 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 500 may be any other electronic device that processes data.

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[0066] In the foregoing specification, embodiments of the invention have been described with reference to specific exemplary embodiments thereof. It will be evident that various modifications may be made thereto without departing from the broader spirit and scope of embodiments of the invention as set forth in the following claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense.

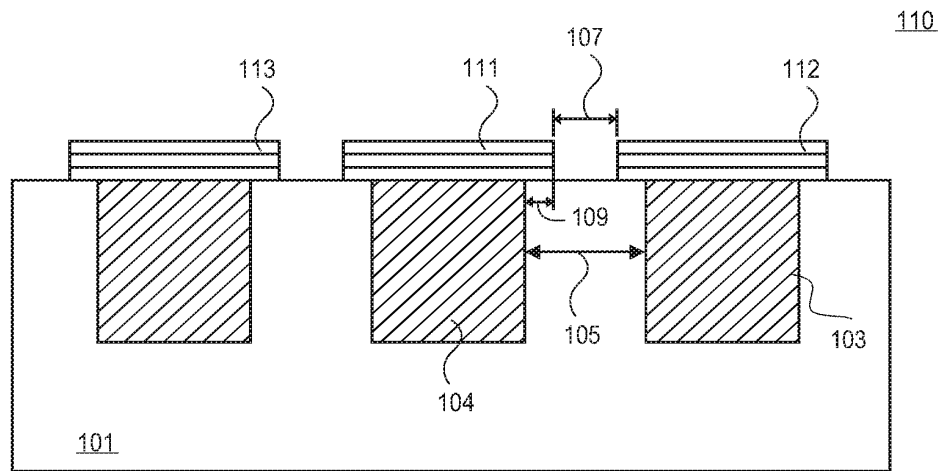


FIG. 1A
(PRIOR ART)

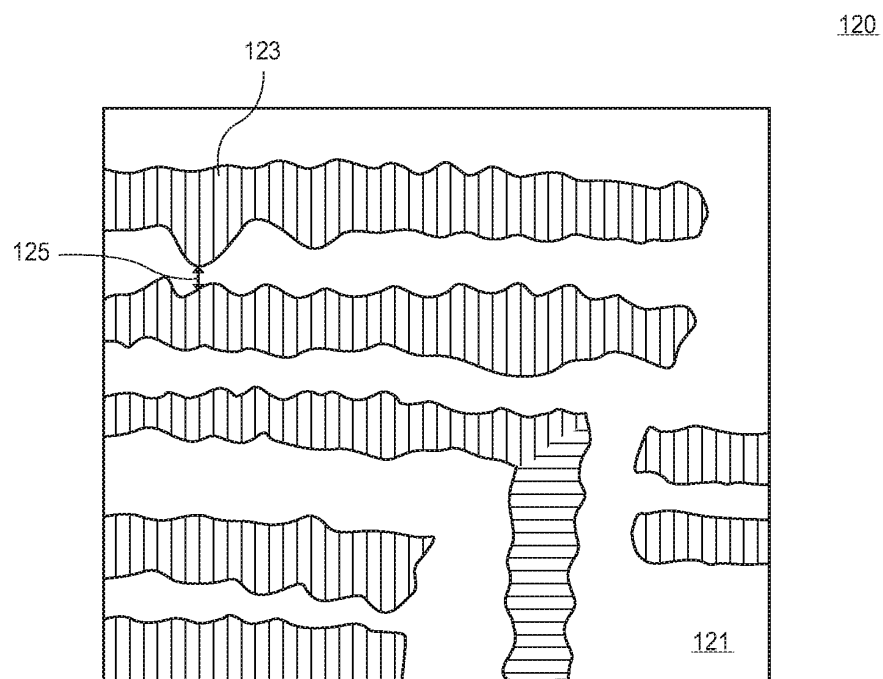


FIG. 1B
(PRIOR ART)

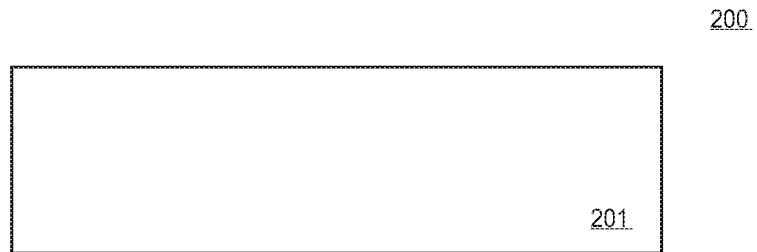


FIG. 2A

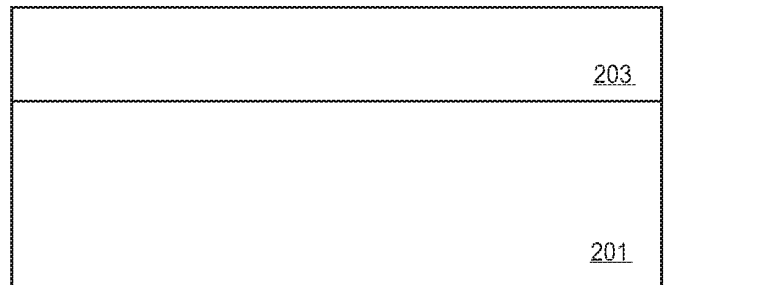


FIG. 2B

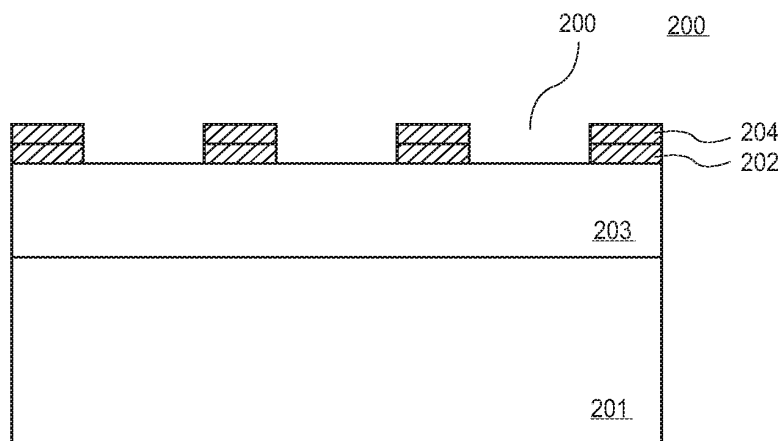


FIG. 2C

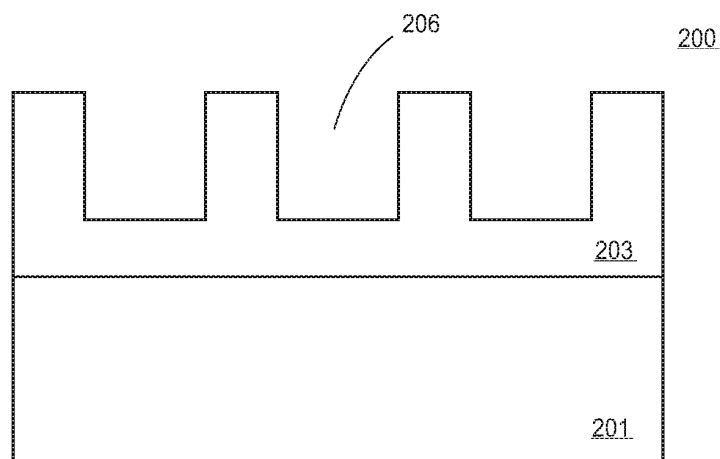


FIG. 2D

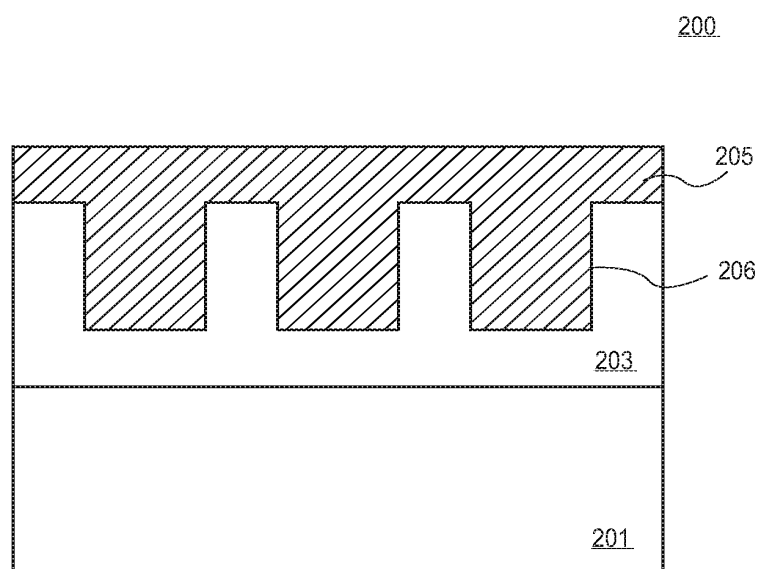


FIG. 2E

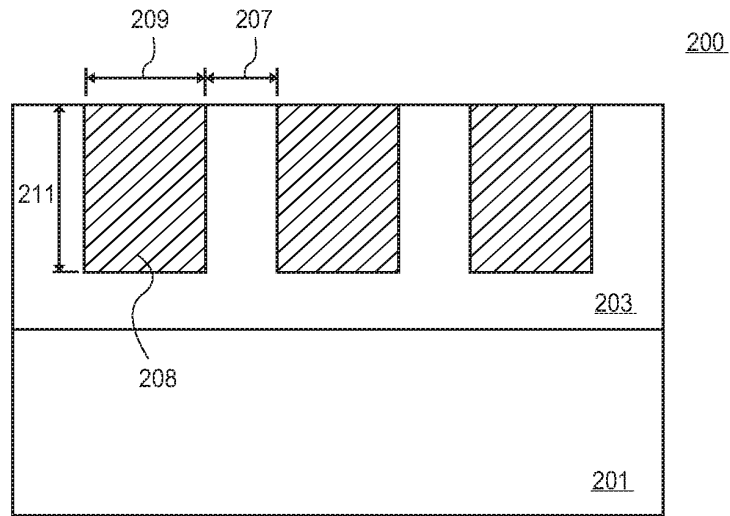


FIG. 2F

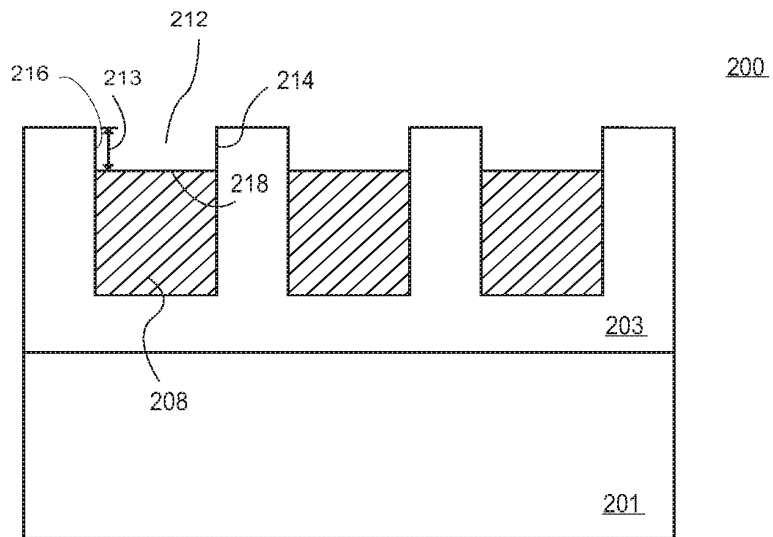


FIG. 2G

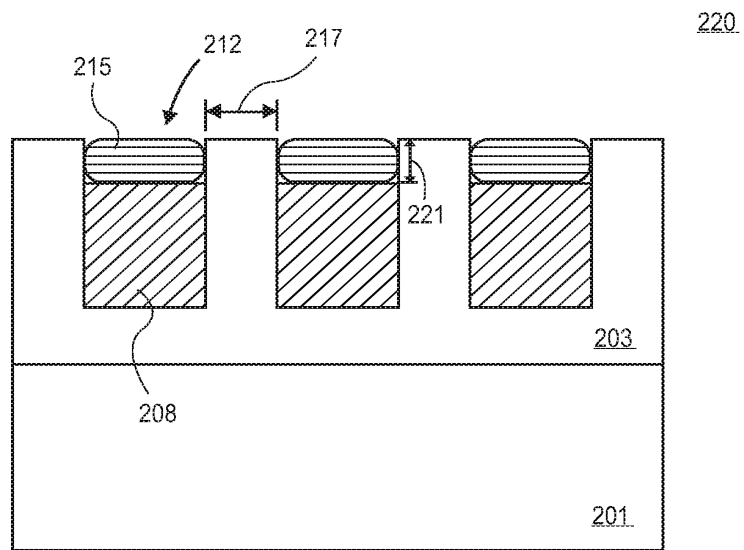
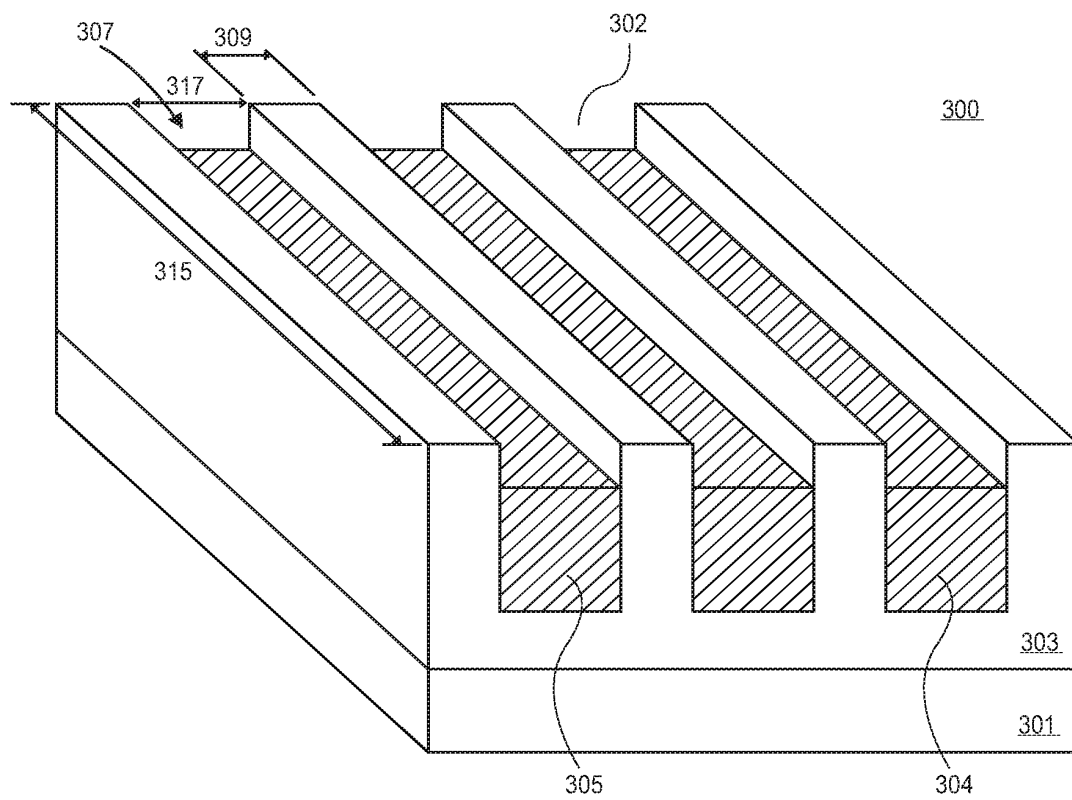


FIG. 2H

**FIG. 3A**

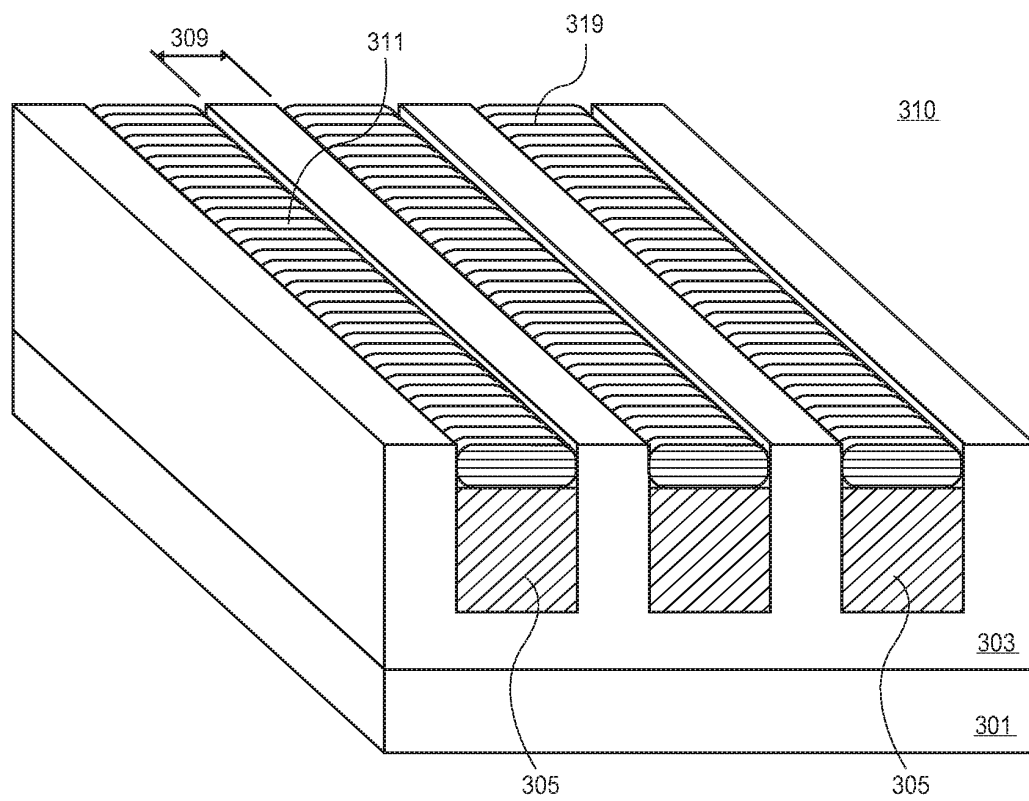


FIG. 3B

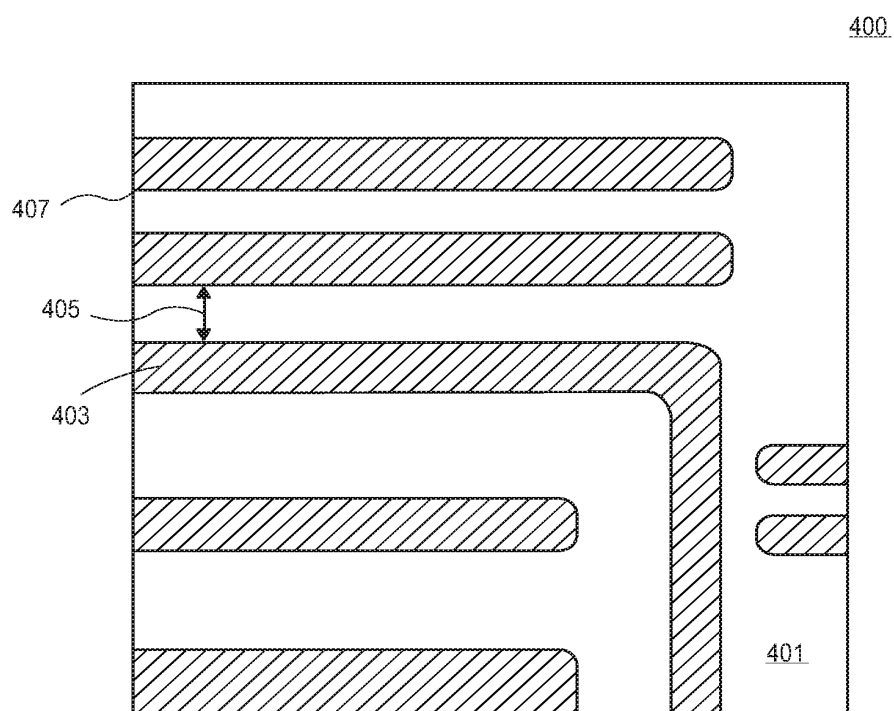
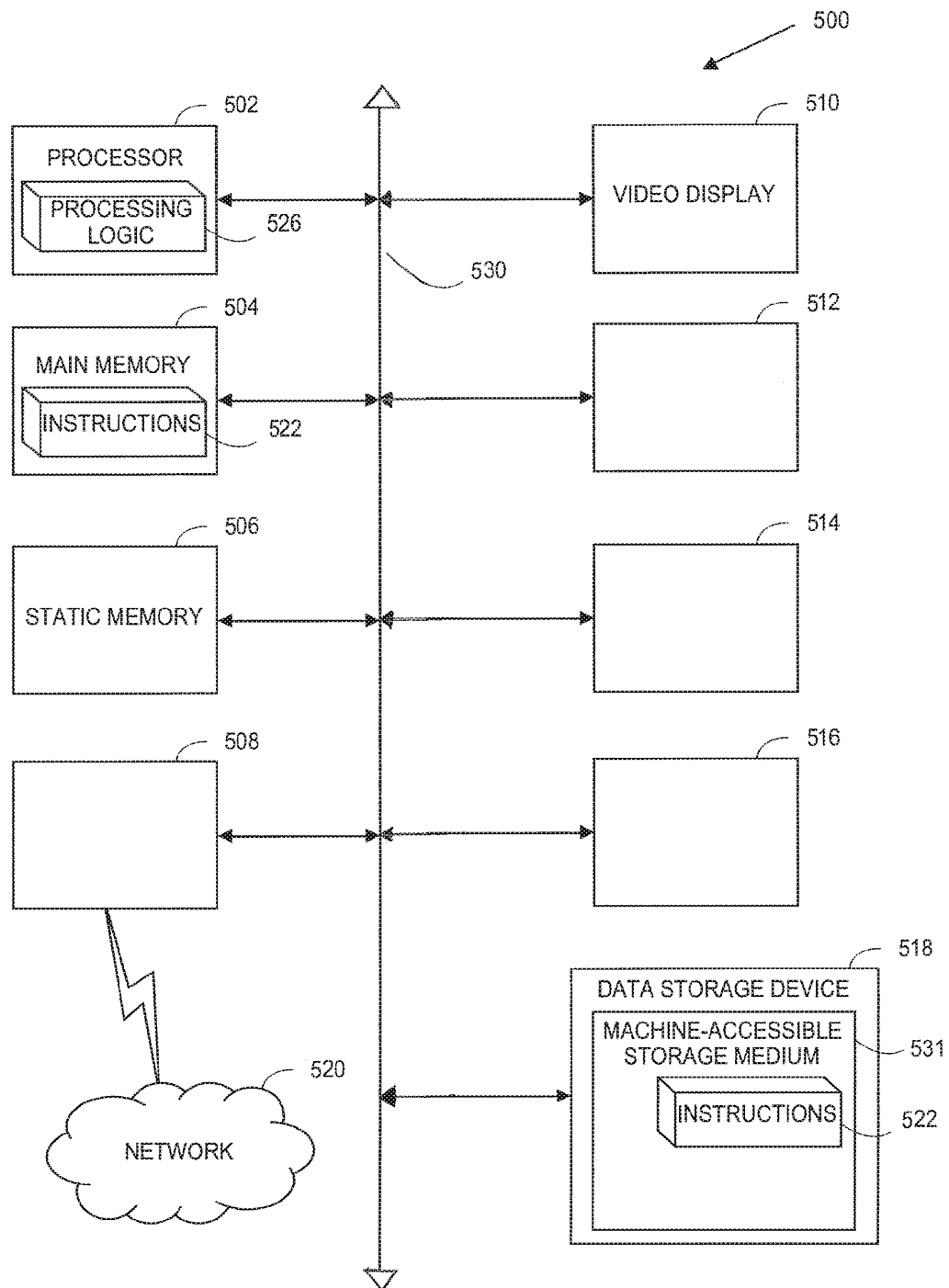
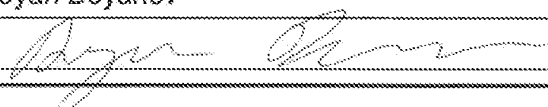


FIG. 4

**FIG. 5**

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>14/675,613</u> filed on <u>March 31, 2015</u> The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR	
Inventor: <u>Boyan Boyanov</u> Date (Optional): <u>7/13/15</u>	
Signature: 	
Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

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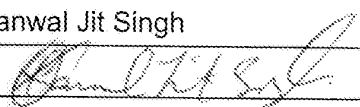
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The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS
As the below named inventor, I hereby declare that: This declaration is directed to: ☐ The attached application, or ☒ United States application or PCT international application number <u>14/675,613</u> filed on <u>March 31, 2015</u>. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: <u>Kanwal Jit Singh</u> Date (Optional): <u>July 13, 2015</u> Signature: <u></u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.	

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				Application Number	Not yet assigned	
				Filing Date	April 3, 2017	
				First Named Inventor:	Boyan BOYANOV	
				Art Unit	Not yet assigned	
				Examiner Name	Not yet assigned	
Sheet	1	of	5	Attorney Docket Number	42P38794DC	
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	5,470,789	11-28-1995	Misawa	
		US-				
		US-				

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				Filing Date	April 3, 2017
				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	2	of	5	Attorney Docket Number	42P38794DC
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Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 7,338,908	03-04-2008	Koos et al.	
		US- 7,396,759 B1	07-08-2008	Van Schravendijk Bart et al.	
		US- 2005-0001325	01-06-2005	Andricacos et al.	
		US- 2006/0128144 A1	06-15-2006	Hyun-Mog Park et al.	
		US- 2009/0127097 A1	05-21-2009	Chen Kei-Wei et al.	
		US- 2009/0283499 A1	11-19-2009	Mayer Steven T. et al.	

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		OTA, Takashi, et al., "Experimental Evaluation of Out-of-Plane Distortion of Electrostatically Chucked EUV Reticle," Proc. Of SPIE Vol. 6921, 69213S, (2008)	
		M.M ANTONIJEVIC et al., "Copper Corrosion Inhibitors. A review", Int. J. Electrochem Sci., Vol. 3, 2008, 28 pages.	
		T. SAITO et al., "A Robust, Deep-Submicron Copper Interconnect Structure using Self-Aligned Metal Capping Method", IEEE, 2004, 3 pages.	
		PCT International Search Report and Written Opinion for PCT/US2011/059453, mailed July 16, 2012 (14 pp.).	
		Taiwan Patent Application No. 101140536, Office Action and Taiwan IPO Search Report (with English translation), dated November 27, 2014, (15 pages) [P38794TW].	
		International Preliminary Report on Patentability (Chapter 1 of the Patent Cooperation Treaty) for PCT/US2011/059453, mailed May 6, 2014 (8 pages).	

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				Application Number	Not yet assigned	
				Filing Date	April 3, 2017	
				First Named Inventor:	Boyan BOYANOV	
				Art Unit	Not yet assigned	
				Examiner Name	Not yet assigned	
Sheet	3	of	5	Attorney Docket Number	42P38794DC	
U.S. PATENT DOCUMENTS						
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		US-				
		US-				
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	NPL1	Chih-Kai Hsu "Electromigration Study on Sn capped Air-gap Cu Damascenes Structure", 2006.	
	NPL2	Korean Patent Application No. 10-2014-7015212, Office Action (with English translation), dated August 3, 2015 (14 pages) [P38794KR].	
	NPL3	Taiwan (R.O.C.) Patent Application No. 101140536, Office Action (with English translation), dated August 13, 2015, (17 pages) [P38794TW].	
	NPL4	China Patent Application No. 201180074611.5, Office Action (with English translation), dated November 16, 2015, (20 pages) [P38794CN].	

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				Application Number	Not yet assigned
				Filing Date	April 3, 2017
				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
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Sheet	4	of	5	Attorney Docket Number	42P38794DC
U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	Korea Patent Application No. 10-2014-7016212, Notice of Allowance (Allowed Claims in English) mailed March 2, 2016, 4 pages [Atty Docket: P38794KR]	
	NPL2	Korea Patent Application No. 10-2016-7003215, Notice of Preliminary Rejection (Office and Claims in English) mailed April 1, 2016, 7 pages [Atty Docket: P38794KR-D]	

Examiner Signature		Date Considered	
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¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	Not yet assigned
				Filing Date	April 3, 2017
				First Named Inventor:	Boyan BOYANOV
				Art Unit	Not yet assigned
				Examiner Name	Not yet assigned
Sheet	5	of	5	Attorney Docket Number	42P38794DC
U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US- 5,470,789	11-1995	Misawa	
		US- 2009/0283499	11-2009	Mayer et al.	
		US- 2010/0081276 A1	04-2010	Ishizaka	
		US- 2009/0283499 A1	11-2009	Mayer	
		US 2010/0081276 A1	04-2010	Mishizaka	
		US 2009/0283499 A1	11-2009	Mayer	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ² Number ³ Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ²
		WO 2002/045142 A2	06/06/2002	Christopher THOMAS, et al.		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
	NPL1	Korean Patent Application No. 10-2016-7003215, Office Action (with English translation), dated April 1, 2016 (5 pages) [P38794KR-D].	
	NPL2	Taiwan (R.O.C.) Patent Application No. 101140536, Office Action (with English translation), dated April 19, 2016, (14 pages) [P38794TW].	

Examiner Signature	Date Considered
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NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	Not yet assigned		
Filing Date	April 3, 2017		
First Named Inventor	Boyan Boyanov		
Title	METHODS AND APPARATUSES TO FORM SELF-ALIGNED CAPS		
Art Unit	Not yet assigned		
Examiner Name	Not yet assigned		
Attorney Docket Number	42P38794DC		
SIGNATURE of Applicant or Patent Practitioner			
Signature	/Tatiana Rossin/	Date (Optional)	April 3, 2017
Name	Tatiana Rossin	Registration Number	56,833
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☒ *Total of <u> 1 </u> forms are submitted.			

SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

- ☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 45209
- OR
- ☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

- ☒ The address associated with the above-mentioned Customer Number

OR

- ☐ The address associated with Customer Number:

OR

Firm or Individual Name				
Address				
City	State	Zip		
Country				
Telephone	Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

INTEL CORPORATION

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	<u>Kerry Tweet</u>	Date (Optional)	<u>August 14, 2014</u>
Name	<u>Kerry Tweet</u>		
Title	<u>Assistant Director of Patents, Intel Corporation</u>		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

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Atty. Docket No: 42P38794DC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	Examiner: Not yet assigned
Boyan Boyanov	)	
	)	Art Unit: Not yet assigned
Application No.: Not yet assigned	)	
	)	
Filing Date: April 3, 2017	)	
	)	
For: METHODS AND	)	
APPARATUSES TO FORM	)	
SELF-ALIGNED CAPS	)	
	)	

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

Applicant hereby requests consideration of the enclosed Information Disclosure Statement pursuant to 37 C.F.R. §1.97(b).

Pursuant to 37 C.F.R. §1.98(d), copies of the references are not being provided herewith since they were previously sent to the Patent and Trademark Office during the prosecution of prior Application No. 14/675,613 filed on March 31, 2015, and prior Application No. 13/991,899 filed on June 5, 2013. These previous applications are relied upon for an earlier filing date under 35 U.S.C. §120. Please consider these cited documents in the currently pending §1.53(b) continuation application filed on April 3, 2017.

CERTIFICATE OF ELECTRONIC FILING

I hereby certify that this correspondence is being deposited with the United States Patent and Trademark Office via electronic filing through the United States Patent and Trademark Electronic Filing System on:

_____ April 3, 2017	Date of Deposit
_____ Juanita Briscoe	Name of Person Filing Correspondence
_____ /Juanita Briscoe/	_____ April 3, 2017
Signature	Date

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: April 3, 2017

/Tatiana Rossin/

Tatiana Rossin

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