

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DAEDALUS PRIME LLC
Patent Owner

Patent No. 10,727,183

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,727,183**

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I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) requests *inter partes* review of claims 1-25 (“the challenged claims”) of U.S. Patent No. 10,727,183 (“the ’183 patent”) (Ex. 1001), which, according to PTO records, is assigned to Daedalus Prime LLC (“Patent Owner” or “PO”). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest

Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters

The ’183 patent is at issue in *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al*, Case No. 2:22-CV-00353.

Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Howard Herr (*pro hac vice* to be filed). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705,

email: PH-Samsung-Daedalus-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '183 patent is available for review and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-25 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-25 are unpatentable under 35 U.S.C. § 102(a)(1) as being anticipated by Taiwanese Patent Application Publication 201804569 to Boyanov et al. ("Boyanov '569") (Ex. 1005).

As discussed below, Boyanov '569 qualifies as prior art and is properly relied upon for showing unpatentability of the '183 patent.

1. Earliest Effective Filing Date of '183 Patent

The '183 patent issued from U.S. Application No. 16/559,086 ("the '086 application") (*see* Ex. 1004), which claims to be a continuation of U.S. Application

No. 15/477,506, (“the ’506 application”) (Ex. 1006) filed April 3, 2017, which claims to be a continuation of U.S. Application No. 14/675,613 (“the ’613 application”) (Ex. 1007) filed March 31, 2015, which claims to be a division of U.S. Application No. 13/991,899 (“the ’899 application”) (Ex. 1008) filed June 5, 2013, which is a national stage entry of International Application PCT/US2011/059453 (“the ’453 PCT application”) filed November 4, 2011. However, the ’183 patent is not entitled to claim priority to the ’506 application, the ’613 application, the ’899 application, or the ’453 PCT application (collectively “the priority applications”), because as explained below, the claims of the ’183 patent are not fully supported by any of the priority applications. (Ex. 1002, ¶¶37-45.) Therefore, the earliest effective filing date for the ’183 patent is September 3, 2019, which is the filing date of ’086 application from which the ’183 patent issued.

In order for a claim in a U.S. application to be entitled to the benefit of the filing date of an earlier filed U.S. or PCT application, the subject matter of the claim must be disclosed in the earlier-filed application in accordance with the written description requirement of Section 112. *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1306 (Fed. Cir. 2008) (subject matter disclosed for first time in a continuation application does not receive benefit of the parent’s filing date); *see also In re Gosteli*, 872 F.2d 1008, 1010–11 (Fed. Cir. 1989). Here, none of the claims of

the '183 patent have adequate disclosure in the priority applications to satisfy the written description requirement, and, hence, none of the claims are entitled to priority to any of the earlier-filed applications. (Ex. 1002, ¶¶37-45.)

To comply with the written description requirement, the specification or earlier-filed application “must describe the invention sufficiently to convey to a person of skill in the art that the patentee had possession of the claimed invention at the time of the application, i.e., that the patentee invented what is claimed.” *LizardTech, Inc. v. Earth Resource Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed Cir. 2005); *see also Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997); *Allergan, Inc. v. Sandoz Inc.*, 796 F.3d 1293, 1308-09 (Fed. Cir. 2015). “The test requires an objective inquiry in to the four corners of the specification from the perspective” of a person of ordinary skill in the art (“POSITA”). *Ariad Parm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). Whether the added subject matter is an obvious variant of the disclosed subject matter is irrelevant. *Lockwood*, 107 F.3d at 1572.

As demonstrated below, all of the claims of the '183 patent include subject matter that lacks written description support in the priority applications, and therefore none of the claims are entitled to an earliest effective filing date any earlier than the September 3, 2019, filing date of '086 application. *PowerOasis, Inc.*, 522

F.3d at 1306; *In re Gosteli*, 872 F.2d at 1010–11. (Ex. 1002, ¶¶37-45.)

The '183 patent includes three independent claims 1, 9, and 18, from which all of the remaining claims depend. Each of independent claims 1, 9, and 18 recites the following limitations:

- (1) “wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet,” and
- (2) “wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer”

(Ex. 1001, 13:35-39, 13:42-45, 14:9-15, 14:49-53, 14:56-59.)

In the '183 patent, the “first conductive material” corresponds to the conductive lines deposited in openings in a dielectric layer overlying the substrate, whereas the “second conductive material” corresponds to the “capping layer” formed on recessed portions of the conductive lines to prevent electromigration. (Ex. 1001, 9:20-33; *see also infra* section VII for an overview of the '183 patent.)

The first and second conductive materials are shown in annotated figure 2H below.

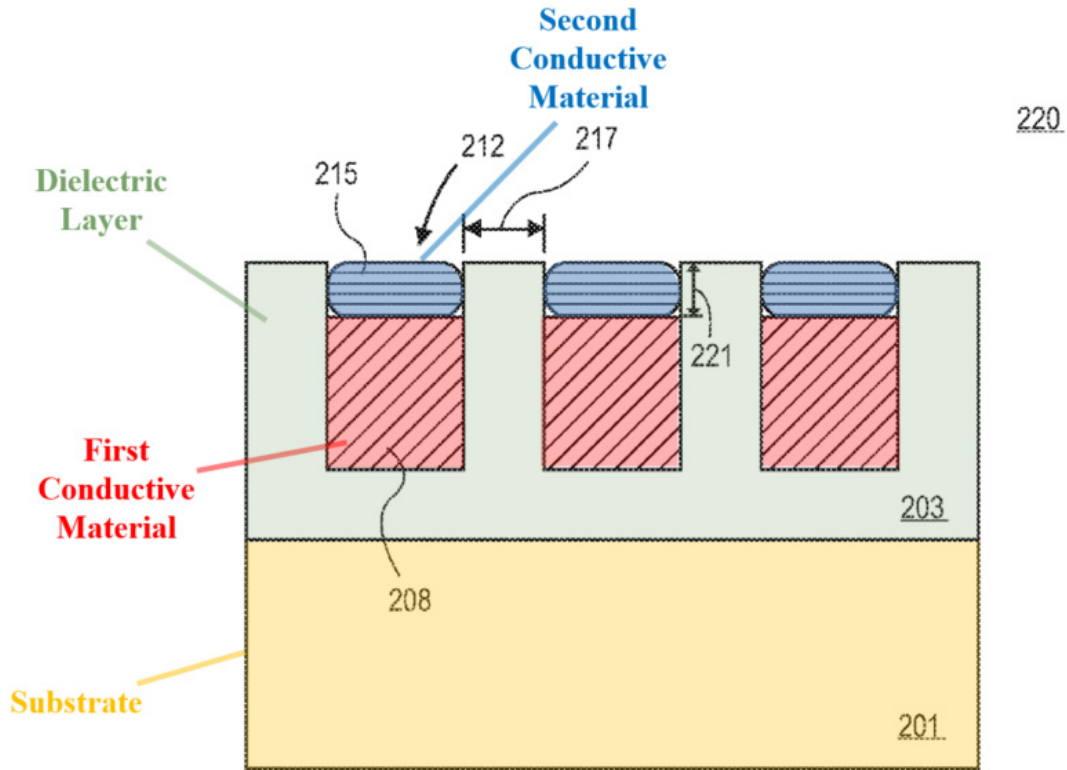


FIG. 2H

(Ex. 1001, FIG. 2H (annotated); Ex. 1002, ¶40.)

None of the priority applications describe, depict, or disclose in any manner that “the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet” as recited in claim limitation (1) above. (See Exs. 1006-1011

generally,¹ Ex. 1002, ¶41.) While the conductive lines corresponding to the first conductive material are described as having “uniform top surface to adhere the capping layer” (Ex. 1006, ¶[0046]), there is no description or depiction of the second conductive material (i.e., the “capping layer”) having a uniform bottom surface or a particular width at the location where the first and second conductive materials meet. (See Ex. 1006 *generally*; see also *id.*, ¶¶[0046]-[0050]; Ex. 1002, ¶41.) Instead, figures 2H and 3B, which are the only figures depicting the intersection of the first and second conductive materials, show that the first and second conductive materials have a different width at the location where they meet. (Ex. 1006, FIGs. 2H, 3B; Ex. 1002, ¶42.) Specifically, figures 2H and 3B depict the bottom surface of the capping layer (“second conductive material”) as having a curved-corner shape just

¹ The specification and drawings for all of the priority applications are the same with respect to disclosure of the relevant features discussed in this section. As such, the exemplary citations to the ’506 application are representative for all of the priority applications. Moreover, as demonstrated by the file histories for the priority applications, neither of claim limitations (1) and (2) was added to any of the priority applications during prosecution.

like the upper surface of the capping layer.

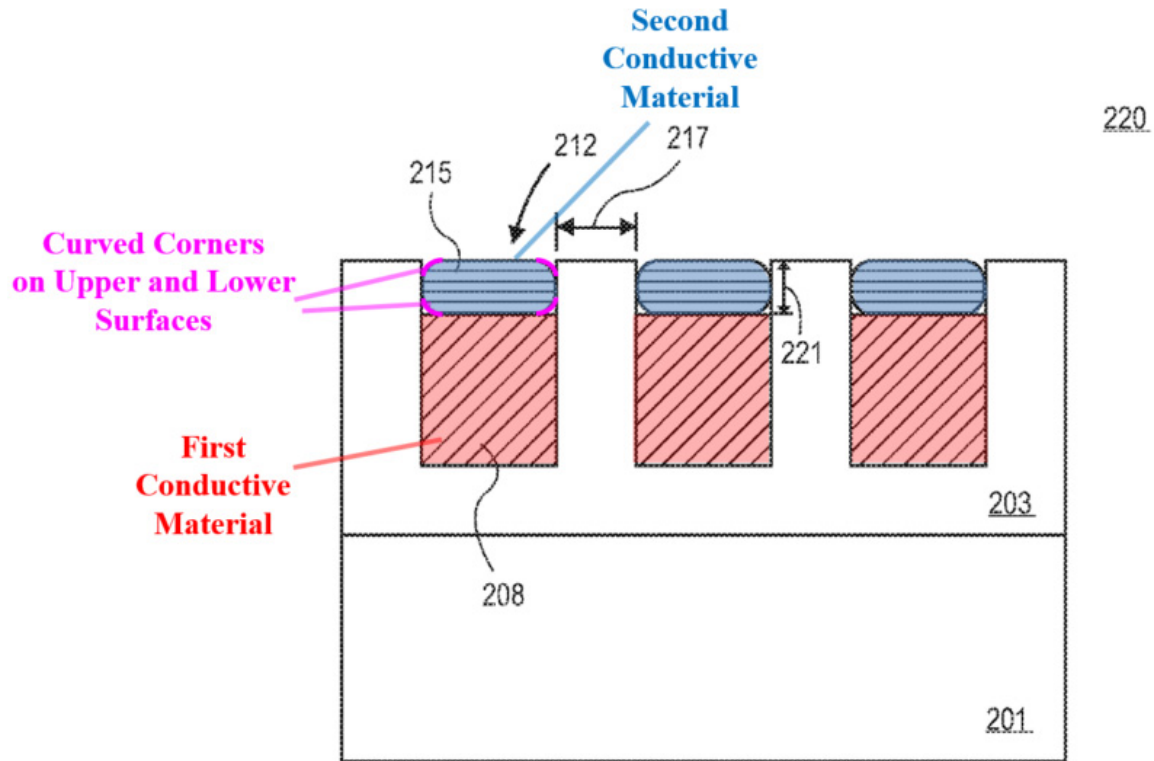


FIG. 2H

(Ex. 1006, FIG. 2H (annotated); Ex. 1002, ¶42.)

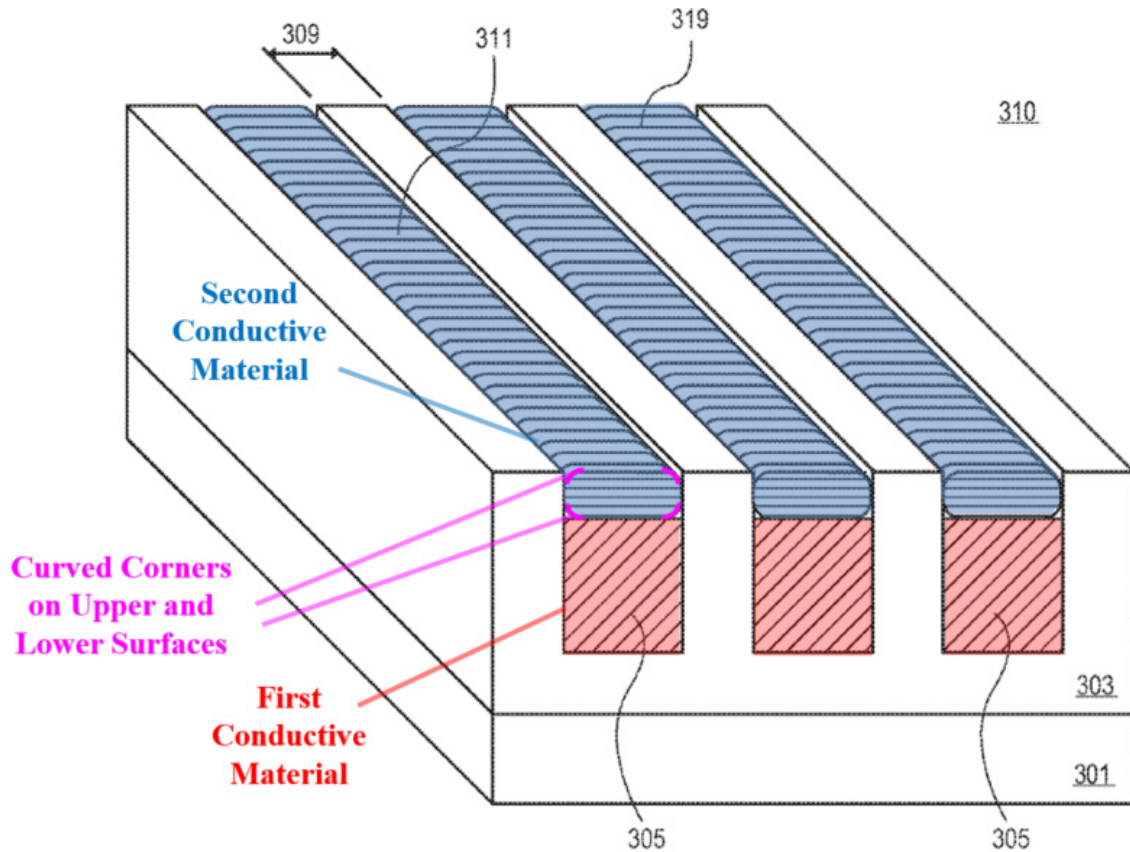
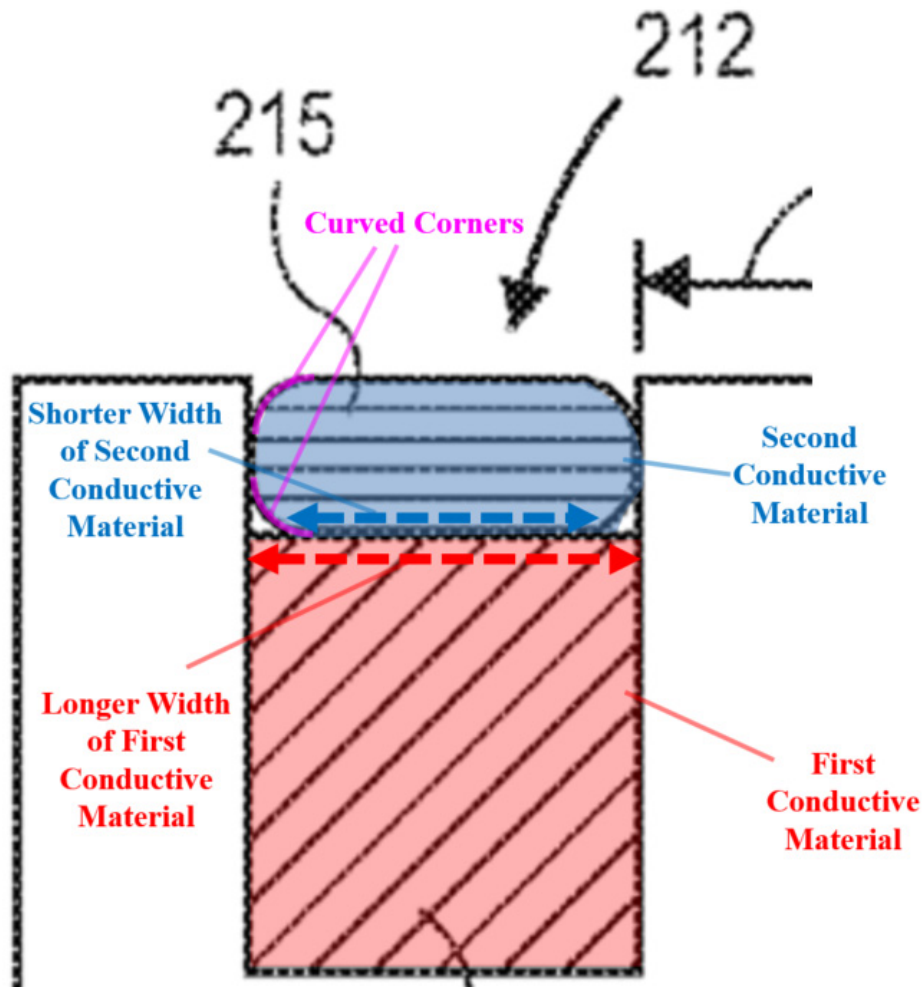


FIG. 3B

(Ex. 1006, FIG. 3B (annotated); Ex. 1002, ¶42.)

Because the second conductive material has curved corners on both the upper and lower surfaces in figures 2H and 3B, the width of the second conductive material is less than the width of the first conductive material where those two materials meet. (Ex. 1006, FIGs. 2H, 3B; Ex. 1002, ¶43.) This is shown in the annotated, enlarged excerpt of figure 2H below.



(Ex. 1006, FIG. 2H (excerpt, annotated); Ex. 1002, ¶43.)

A POSITA would not have understood, based on the disclosures of the priority applications of the '183 patent, that the named inventors possessed an invention that includes the recited “wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet,” as such a limitation is not described or depicted

in any of the priority applications. (Ex. 1002, ¶44.)

To the extent Patent Owner contends that there is inherent disclosure of the “first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet” based on the disclosure regarding formation of the second conductive material, figure 2H demonstrates that there is no such inherency, as figure 2H shows the width of the two conductive materials to be different where they meet.²

For at least these reasons, none of claims 1-25 are entitled to priority to the earlier-filed applications, and the earliest effective filing date for the '183 patent is

² In addition to not disclosing limitation (1) alone, none of the priority applications disclose limitations (1) and (2) together as recited in the claims. The only possible support for the “curved corner” in limitation (2) is figures 2H and 3B, which depict a second conductive material that has curved corners on both the upper and lower surfaces. (Ex. 1001, FIGs. 2H, 3B.) There is no disclosure in any of the priority applications of a second conductive material that has **both** a flat, uniform lower surface where the second conductive material meets the first conductive material, and a top surface that has a curved corner as recited in the claims. (Ex. 1002, ¶45.)

no earlier than the September 3, 2019 filing date of the '086 application.

2. The Boyanov '569 Taiwanese Published Patent Application

Taiwanese Patent Application Publication 201804569 to Boyanov et al. ("Boyanov '569") (Ex. 1005) published February 1, 2018, and therefore qualifies as prior art to the '183 patent under 37 U.S.C. 102(a)(1).³ Boyanov '569 also claims priority to the same '453 PCT application from which the '183 patent is derived. (Ex. 1005, Cover.) Boyanov '569 includes essentially the same written description and drawings as the '183 patent, and also includes claims with features (1) and (2) discussed above and recited in each of claims 1, 9, and 18 of the '183 patent.

Boyanov '569 was not considered as prior art by the Patent Office during prosecution of the '183 patent. (Ex. 1001, Cover ("References Cited" section); *see generally* Ex. 1001.)

³ Because the '183 patent has an earliest-effective filing date of September 3, 2019, the '183 patent is subject to the provisions of the Leahy-Smith America Invents Act (AIA).

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’183 patent would have had a bachelor’s degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. (Ex. 1002, ¶¶16-17.)⁴ More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE ’183 PATENT

The ’183 patent is entitled “Methods and Apparatuses to Form Self-Aligned Caps.” (Ex. 1001, Title.) The ’183 patent discloses formation of conductive lines in a dielectric layer over a substrate, where the conductive lines are recessed in order to allow a capping layer to be formed on each of the conductive lines. (*Id.*, Abstract; Ex. 1002, ¶¶28-35.) The ’183 patent discloses that prior art interconnect structures formed the capping layers over conductive lines that were not recessed, and instead, had an upper surface co-planar with the dielectric layer in which the conductive lines are contained. (Ex. 1001, 1:43-46 (“The electromigration caps, for example, caps

⁴ Petitioner submits the declaration of Dr. Stanley Shanfield (Ex. 1002), an expert in the field of the ’183 patent. (*Id.*, ¶¶5-12; Ex. 1003.)

111-113, can be grown on the respective interconnect lines above a flat surface of the substrate using electroless plating.”) As shown in annotated figure 1A below, because the growth of the caps is isotropic, they grow horizontally and vertically such that they extend beyond the conductive lines onto the surface of the substrate. (*Id.*, 1:46-53.) As a result, the line-to-line spacing is reduced from the spacing 105 between the conductive lines to the spacing 107 between the overhanging caps. (*Id.*, 1:53-55.)

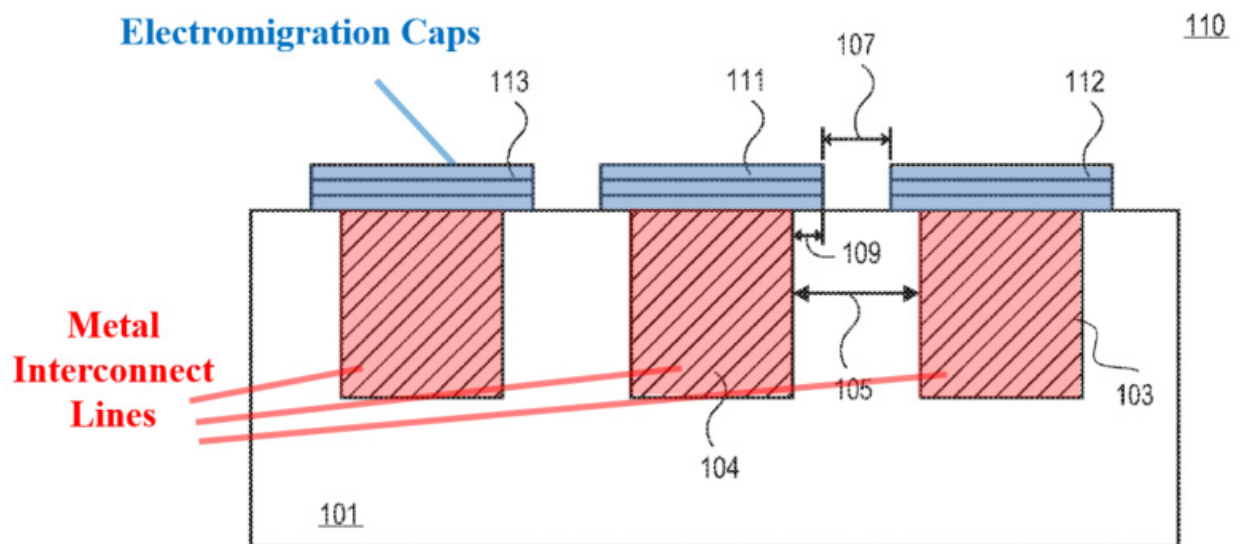


FIG. 1A
(PRIOR ART)

(Ex. 1001, FIG. 1A (annotated); Ex. 1002, ¶28.)

According to the '183 patent, the overhang 109 of the caps is about 50% of the cap thickness. (Ex. 1001, 1:56-57.) Figure 1B of the '183 patent illustrates a top view of an interconnect structure and shows how the lateral growth of the caps above the substrate increased the line edge roughness ("LER") and reduces line-to-line spacing 125. (*Id.*, 1:61-2:2.) The '183 patent further discloses that "[b]oth the increased LER and reduced line-to-line spacing negatively impact on the reliability of the interconnect structures, increase the risk of current shorting that may lead to the failure of the entire integrated circuit device." (*Id.*, 2:3-6; Ex. 1002, ¶29.)

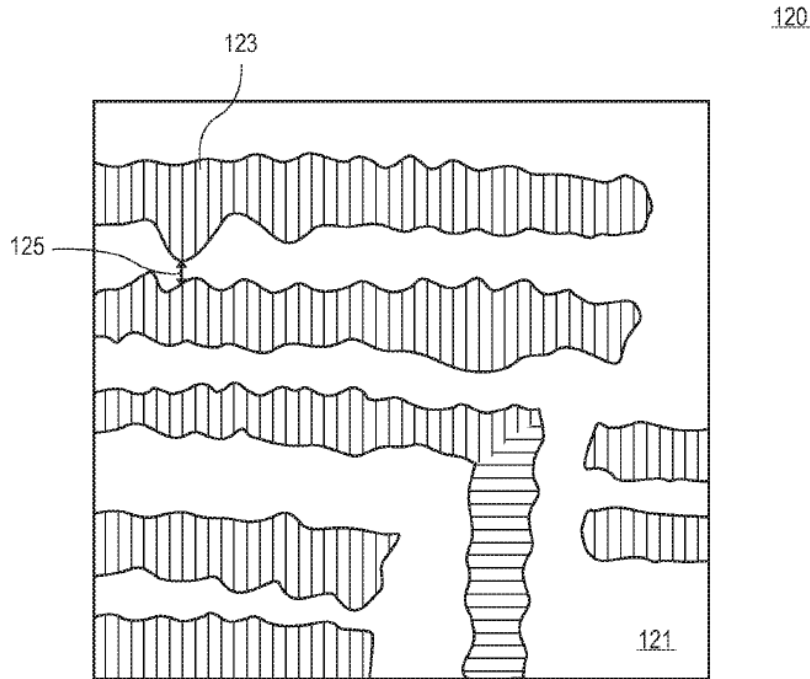


FIG. 1B
(PRIOR ART)

(Ex. 1001, FIG. 1B.)

In an attempt to address these problems, the '183 patent discloses “[m]ethods and apparatuses to control a line edge roughness (“LER”) and line-to-line spacing in deposition of self-aligned metal caps.” (*Id.*, 3:46-48.) The '183 patent discloses the steps for forming such an interconnect structure in conjunction with figures 2A-2H. (*Id.*, 2:19-47, FIGs. 2A-2H.) Figure 2B shows the dielectric layer 203 formed over the substrate 201. (*Id.*, 4:27-29.)

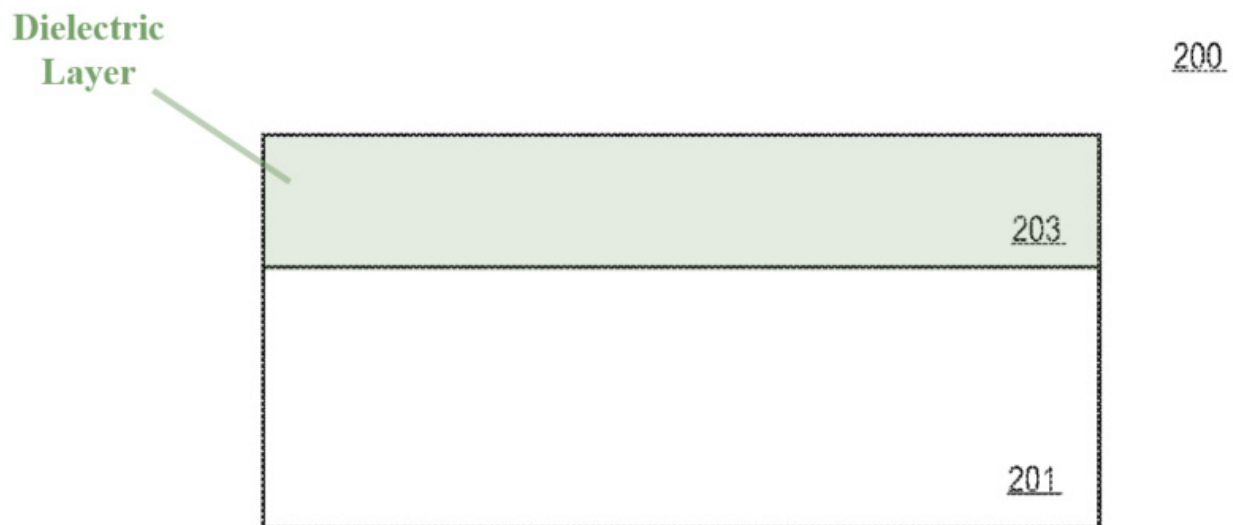


FIG. 2B

(*Id.*, FIG. 2B (annotated); Ex. 1002, ¶30.)

Figure 2D shows openings (“trenches”) 206 formed in the dielectric layer.
(Ex. 1001, 5:6-8.)

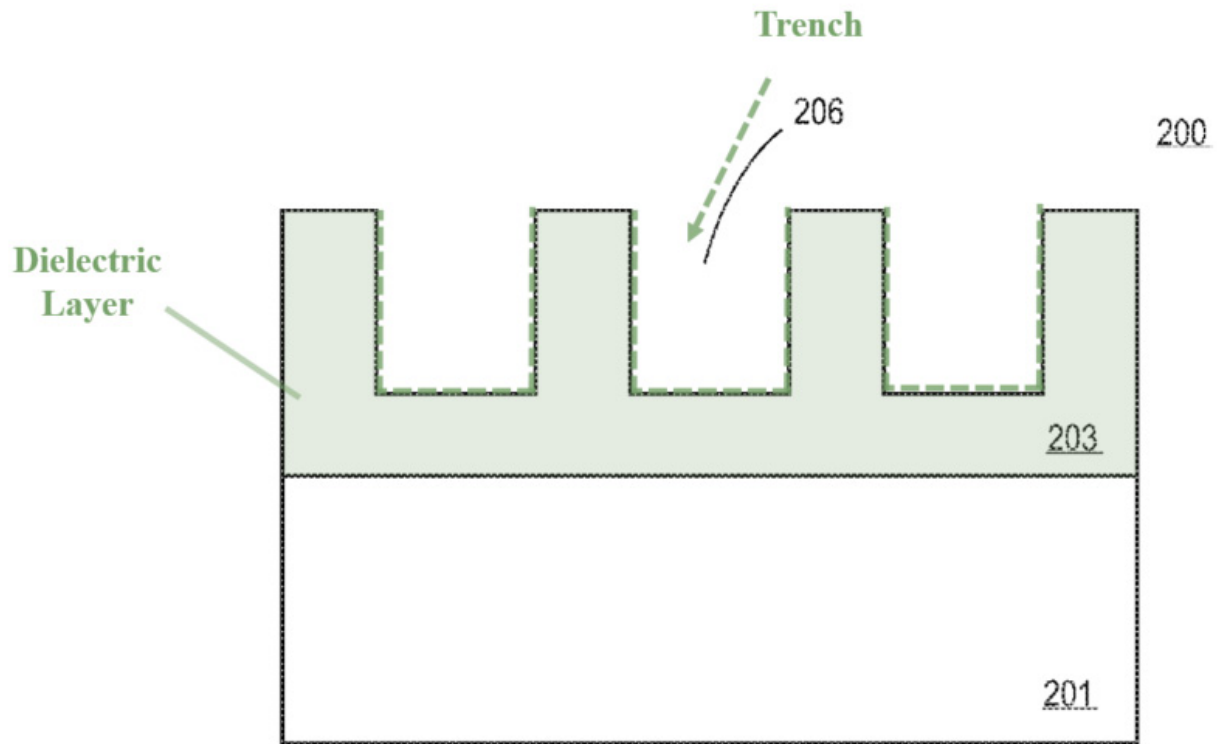


FIG. 2D

(*Id.*, FIG. 2D (annotated); Ex. 1002, ¶31.)

The '183 patent discloses that a base layer than includes a barrier layer (not shown) can be formed on the inner sidewalls and bottom of the trenches. (Ex. 1001, 5:39-48.) Figure 2E shows a conductive layer 205 deposited over the dielectric layer 203, where the conductive layer 205 fills the opening with conductive material to form conductive lines. (*Id.*, 5:34-39.)

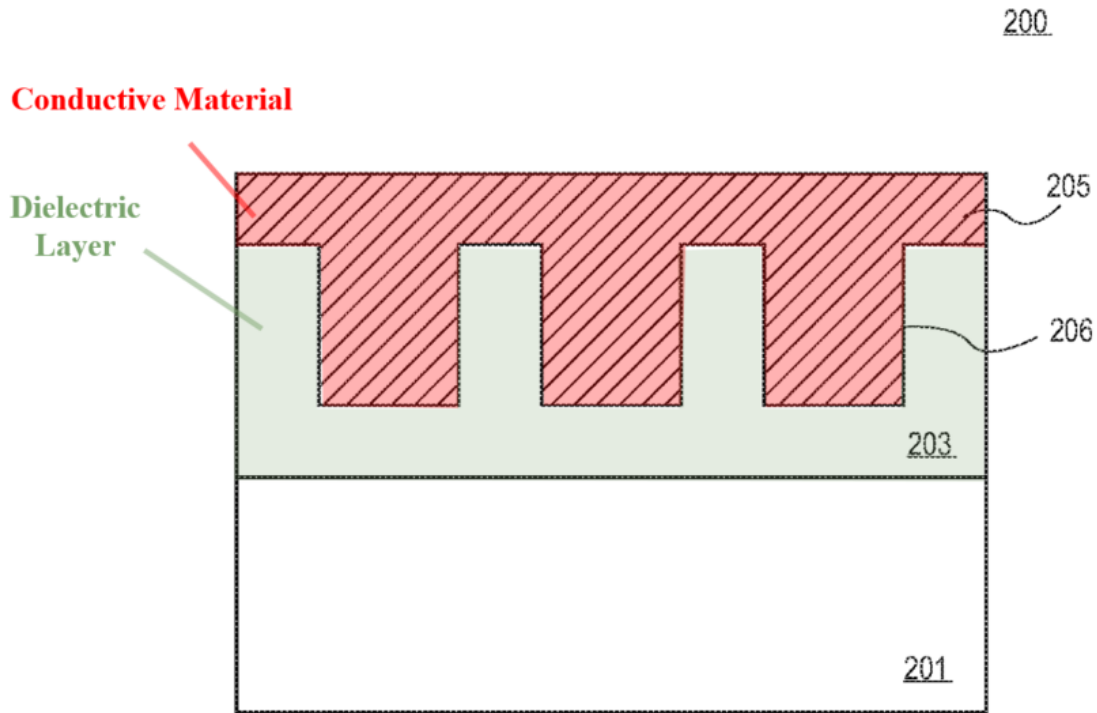


FIG. 2E

(*Id.*, FIG. 2E (annotated); Ex. 1002, ¶32.)

Following deposition of the conductive material in the openings, portions of the conductive layer 205 are removed from the top surface of the dielectric layer outside the opening to form conductive lines 208 shown in figure 2F. (Ex. 1001, 6:29-33.)

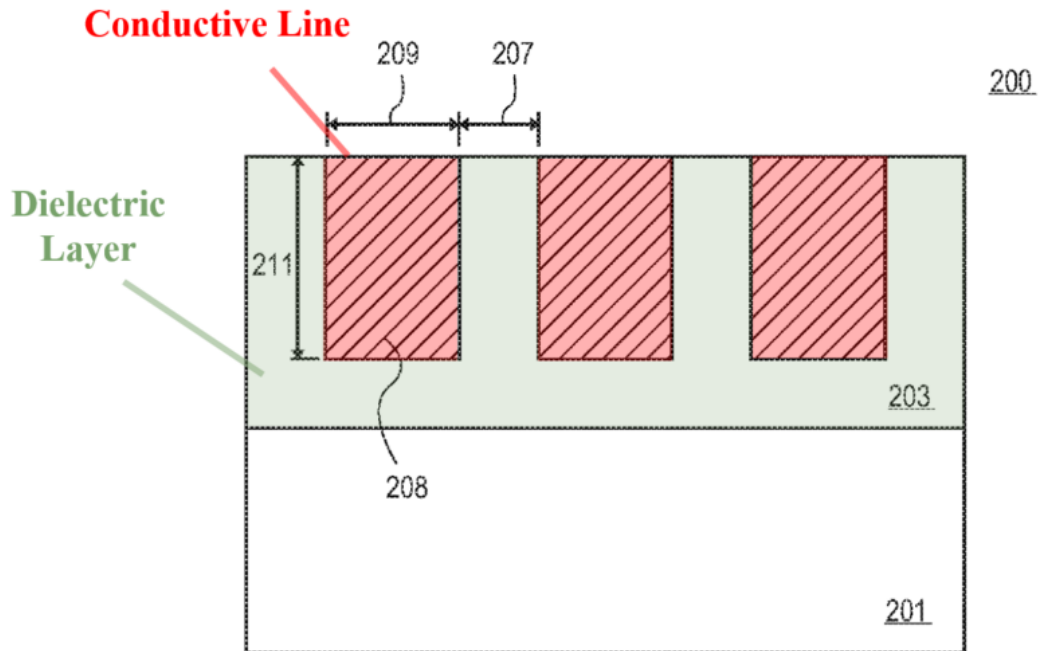


FIG. 2F

(*Id.*, FIG. 2F (annotated); Ex. 1002, ¶33.)

As shown in figure 2G, following removal of the conductive material from the top surface of the dielectric layer, the conductive lines are recessed to form channels 212. (Ex. 1001, 6:56-64.)

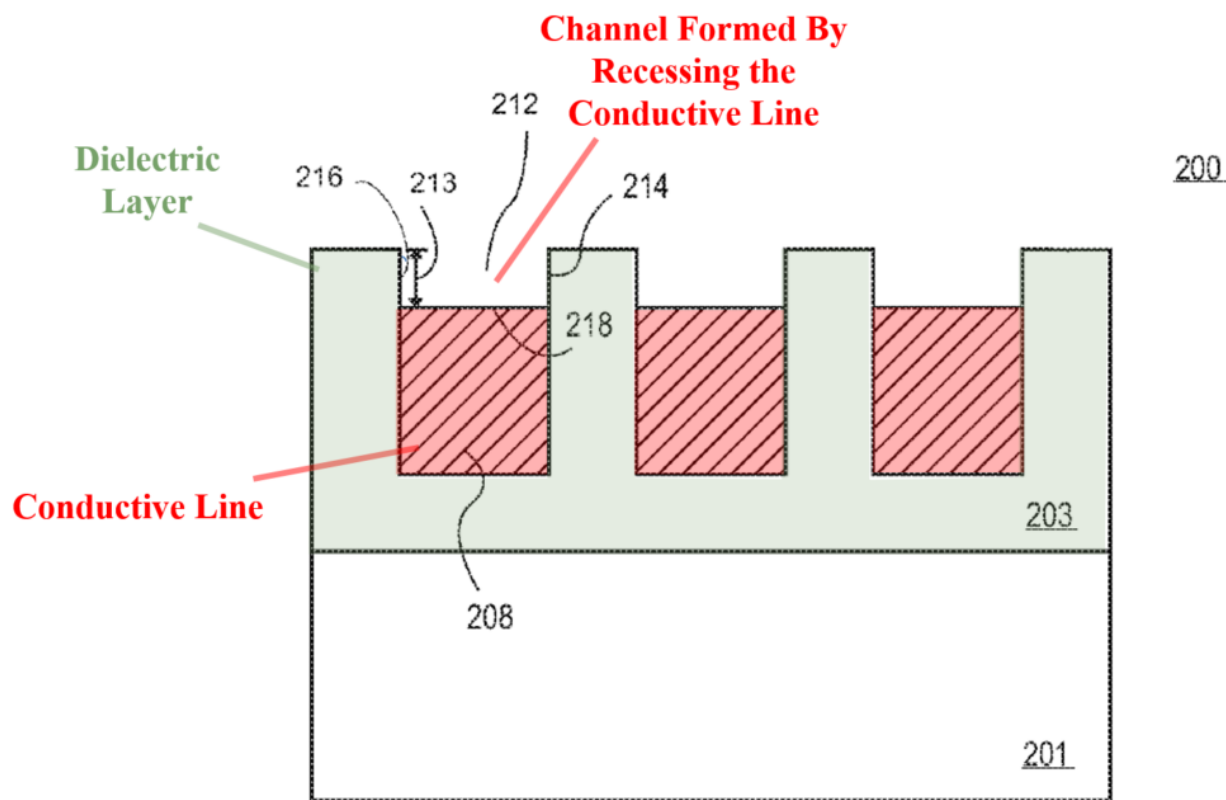


FIG. 2G

(*Id.*, FIG. 2G (annotated); Ex. 1002, ¶34.)

Figure 2H shows the interconnect structure following deposition of the capping layers 215, where the capping layers 215 are deposited on the recessed conductive lines 208 within channels 212. (Ex. 1001, 9:6-27.) The '183 patent further discloses that the conductive material for the conductive lines can be copper or aluminum, whereas the capping layer can include cobalt alloys, nickel alloys, platinum group metals or alloys, or refractory metals. (*Id.*, 9:34-48.)

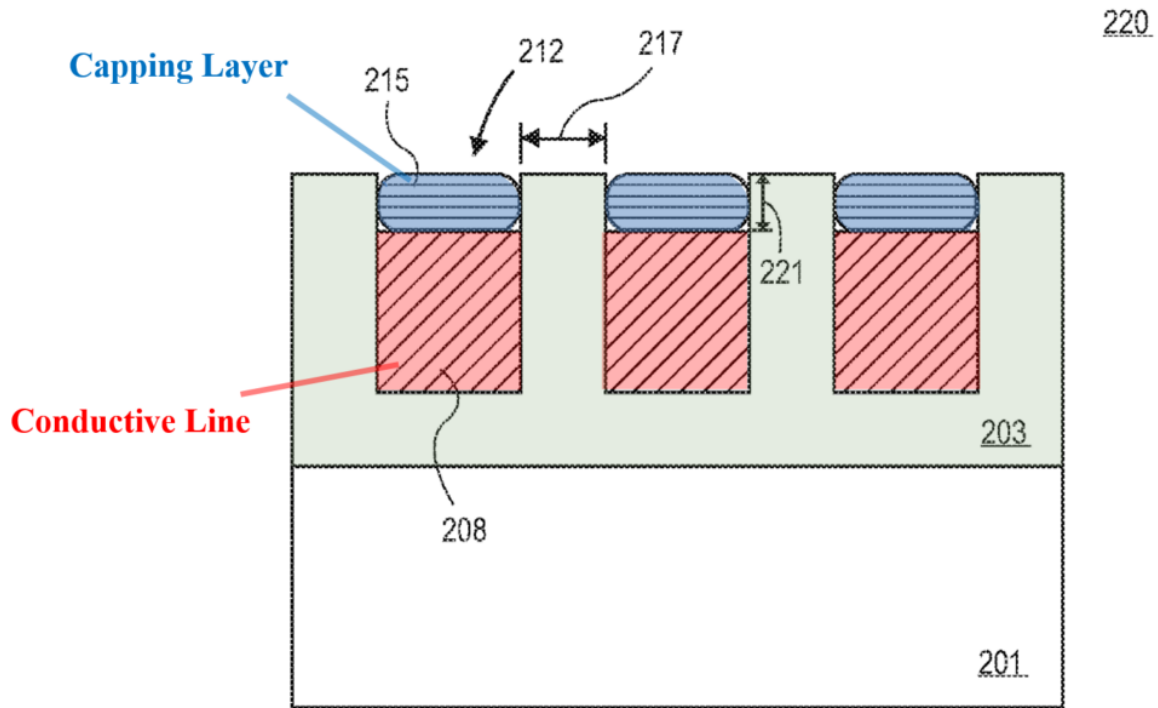


FIG. 2H

(*Id.*, FIG. 2H (annotated); Ex. 1002, ¶35.)

As explained below (*infra* Section IX), the above features were all known in the prior art. (See Ex. 1002, ¶¶46-105; *see also id.*, ¶¶19-27 (describing the state of the art).)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a

POSITA at the time of the invention. *Phillips*, 415 F.3d at 1313; *see also id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶36.)

IX. DETAILED EXPLANATION OF UNPATENTABILITY

A. Ground 1 – Boyanov '569 Anticipates Claims 1-25

As shown in detail below, Boyanov '569, which has essentially the same written description and drawings as the '183 patent, discloses all the features recited in claims 1-25.⁵ Indeed, claims 1-17 of Boyanov '569 are nearly identical to claims

⁵ To the extent that Patent Owner contends that Boyanov '569, which has essentially the same written description, drawings, and claims 1-17 as the '183 patent, does not disclose any of the features of claims 1-25, the claims in the '183 patent including such features would necessarily be invalid for lack of written description under §112. Petitioner reserves the right to raise such invalidity positions in the appropriate venues.

1-17 of the '183 patent, thereby demonstrating that claims 1-17 of the '183 patent are anticipated by Boyanov '569. (*Compare* Ex. 1001, claims 1-17 *with* Ex. 1005, claims 1-17; Ex. 1002, ¶46.)

1. Claim 1

a) “An integrated circuit structure, comprising:”

To the extent the preamble is limiting, Boyanov '569 discloses “an integrated circuit structure.” (Ex. 1002, ¶47.) For example, claim 1 of Boyanov '569 recites “an integrated circuit structure.” (Ex. 1005, claim 1.) Figure 2H of Boyanov '569 below shows an interconnect structure included as a part of an integrated circuit. (*Id.*, 3-4 (describing figures 2A-2H as “a cross-sectional view of a substrate used to fabricate an interconnect structure in accordance with an embodiment of the present invention”), 6 (“The present invention describes methods and apparatus for controlling line edge roughness (LER) and line-to-line spacing when depositing self-aligning metal caps. ... When the increase in LER is eliminated and the line-to-line spacing is prevented from being reduced, the risk of failure can be reduced, and the manufacturing yield of a small-sized (e.g., nano-scale) electronic device can be improved. The **electronic devices can be** computer system architecture devices such as transistors, **memories, logic devices, and the like, as well as any other integrated circuit** and microelectronic device.”) (emphasis added); Ex. 1002, ¶47.)

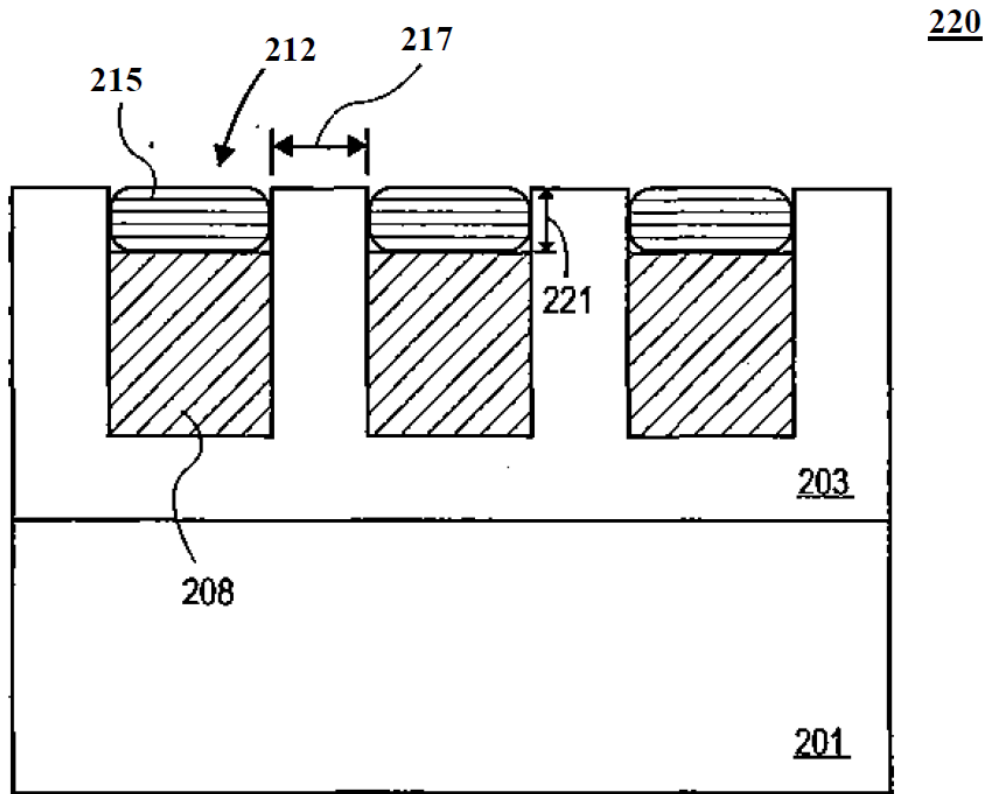


FIG. 2H

(Ex. 1005, FIG. 2H.)

b) “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen and carbon;”

Boyanov ’569 discloses this claim feature. (Ex. 1002, ¶¶48-49.) For example, claim 1 of as Boyanov ’569 recites “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen, and carbon.” (Ex. 1005, claim 1.) As shown in annotated figure 2H below, Boyanov ’569 discloses that the integrated circuit structure includes a dielectric layer having an upper surface. (*Id.*, 3 (“FIG.

2B is a view similar to FIG. 2A after forming a **dielectric layer 203** over the substrate 201 in accordance with an embodiment of the present invention. In one embodiment, the dielectric layer 203 is an interlayer dielectric (ILD).”), 4 (“FIG. 2F is a view similar to FIG. 2E after forming a patterned conductive line, such as conductive line 208, by removing portions other than the conductive layer 205 and the openings in the base layer from **the upper surface of the dielectric layer 203** in accordance with an embodiment of the present invention.”), 11-12 (“In another embodiment, patterning and etching are performed on the conductive layers deposited on **the upper surface of the dielectric layer 203** to form the conductive lines. Patterning and etching of the conductive layer deposited on **the upper surface of dielectric layer 203** is well known to those of ordinary skill in the art of microelectronic device fabrication.”), 12 (“FIG. 2G is a diagram similar to FIG. 2F after recessing a conductive line such as conductive line 208 in a dielectric layer over a substrate in accordance with an embodiment of the present invention.”), 17 (“FIG. 2H is a diagram similar to FIG. 2G after electromigration is prevented by selectively depositing the cover layers into the respective recessed conductive lines in the channels in accordance with an embodiment of the present invention.”); Ex. 1002, ¶48.)

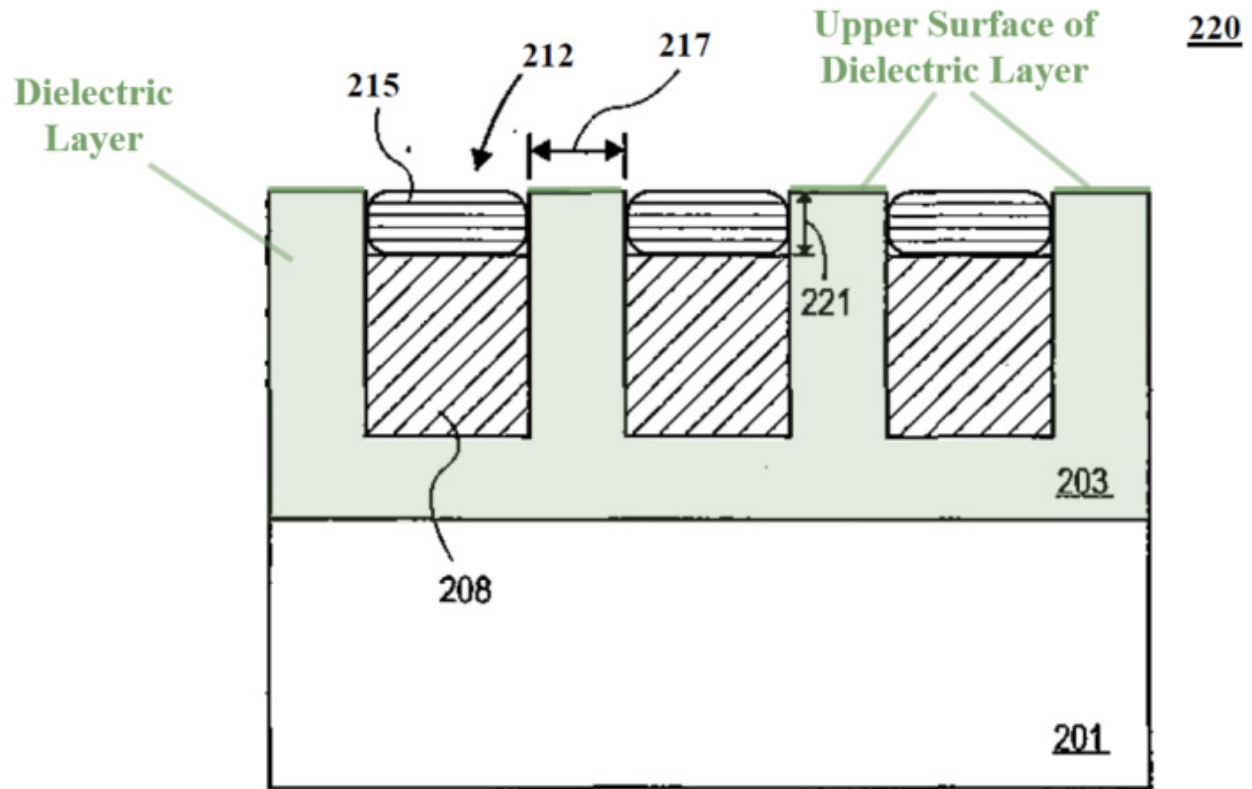


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶48.)

Boyanov '569 further discloses that the dielectric layer includes silicon (Si), oxygen (O), and carbon (C):

In one embodiment, dielectric layer 203 is a low-k dielectric such as silicon dioxide, silicon oxide, **carbon doped oxides (CDO), or any combination of the above.**

In one embodiment, the dielectric layer 203 comprises a nitride, an oxide, a polymer, a phosphosilicate glass, a

fluorosilicate glass (SiOF), an organosilicate glass (SiOCH), or any combination of the above. In an embodiment, the dielectric layer 203 comprises a spin-on low-k dielectric material. In an embodiment, the dielectric layer 203 is silicon oxide.

(Ex. 1005, 7 (emphasis added); Ex. 1002, ¶49.)

c) “a conductive structure in the dielectric layer, the conductive structure comprising:”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶¶50-51.) For example, claim 1 of Boyanov ’569 recites “a conductive structure in the dielectric layer,” where, as discussed below for claim elements 1[d] and 1[e], the conductive structure in claim 1 of Boyanov ’569 is disclosed as including the same features recited in claim 1 of the ’183 patent. (Ex. 1005, claim 1; Ex. 1002, ¶50.) As shown in annotated figure 2H below, Boyanov ’569 discloses a conductive structure in the opening 206 of the dielectric layer 203, where the conductive structure includes conductive layer 205 and covering layer 215, which are made of metal and, therefore, conductive. (Ex. 1005, 10 (“Conductive layer 205 fills the openings, such as openings 206, and covers portions of the base layer (not shown) that are outside of the openings on top of the dielectric layer 203. In one embodiment, a conductive layer 205, such as copper, is deposited onto the seed layer of the copper base layer by an electroplating process.”)),

17 (“FIG. 2H is a diagram similar to FIG. 2G after electromigration is prevented by selectively depositing the cover layers into the respective recessed conductive lines in the channels in accordance with an embodiment of the present invention. ... As shown in FIG. 2H, the cover layer 215 is disposed over the conductive lines 208 in the sidewalls of the channel 212.”), 17-18 (“In one embodiment, the conductive line such as the line 208 comprises a first metal, and the cover layer comprises a second metal different from the first metal, while the second metal is used to prevent electromigration from the first metal of the conductive line.”), 18 (“For example, the conductive line can be made of any metal including copper or aluminum.”); Ex. 1002, ¶51.)

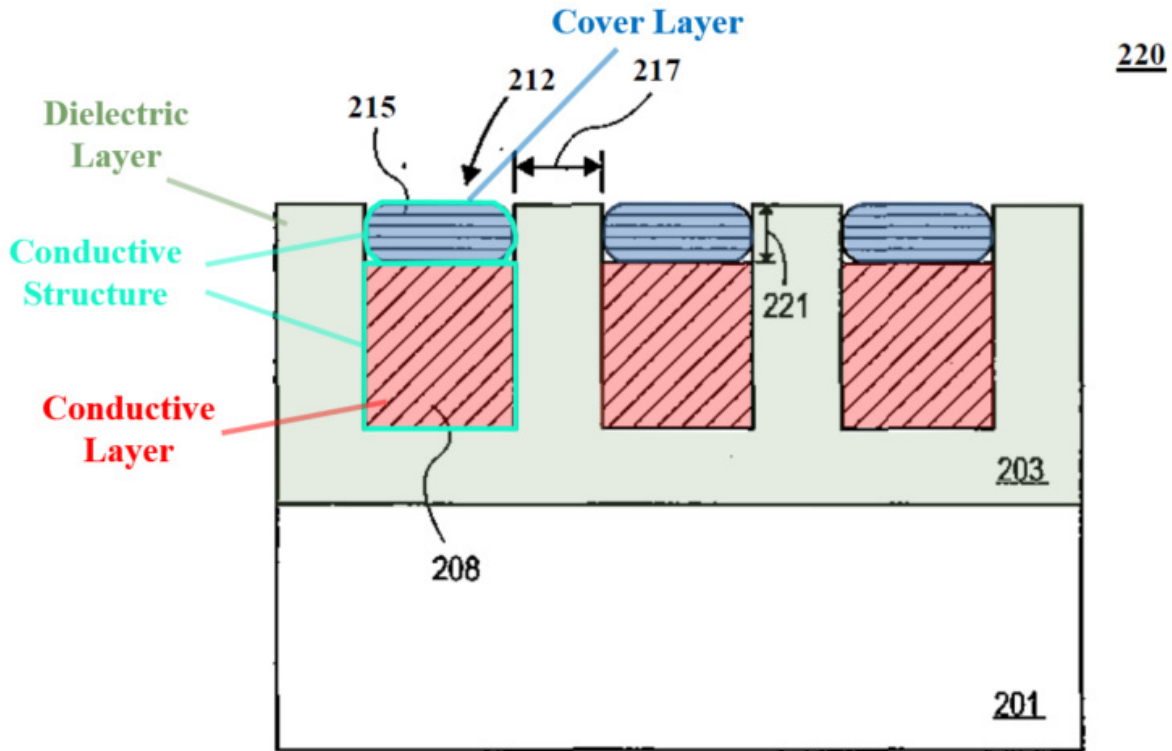


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶51.)

d) “a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”

Boyanov '569 discloses this feature. (Ex. 1002, ¶¶52-54.) For example, claim 1 of Boyanov '569 recites that the conductive structure includes “a first conductive material comprising copper, the first conductive material having an upper surface, and a portion of the upper surface of the first conductive material being below a

portion of the upper surface of the dielectric layer.” (Ex. 1005, claim 1.) As shown in annotated figure 2H below, the conductive layer 208 (“first conductive material”) has an upper surface, where a portion of the upper surface is below a portion of the upper surface of the dielectric layer. (*Id.*, 12 (“FIG. 2G is a diagram similar to FIG. 2F after recessing a conductive line such as conductive line 208 in a dielectric layer over a substrate in accordance with an embodiment of the present invention. As shown in FIG. 2G, a channel such as the channel 212 is formed in the dielectric layer 203.”), 17 (“FIG. 2H is a diagram similar to FIG. 2G after electromigration is prevented by selectively depositing the cover layers into the respective recessed conductive lines in the channels in accordance with an embodiment of the present invention.”); Ex. 1002, ¶52.)

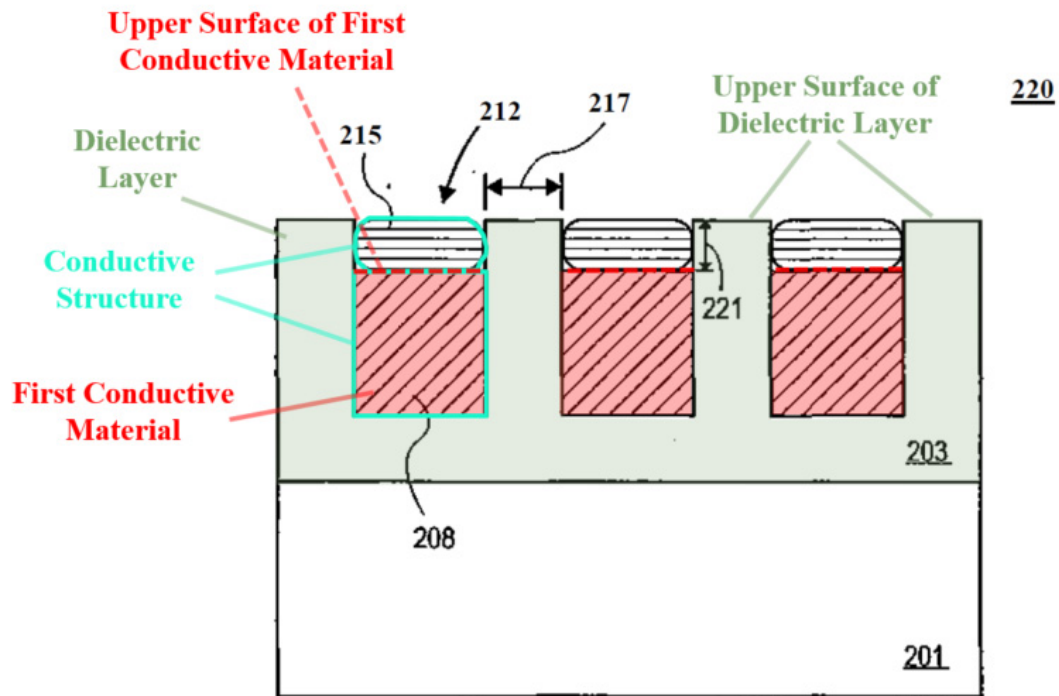


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶52.)

Boyanov '569 discloses that the conductive layer 208 is recessed in order to allow the cover layer 215 to be formed over the conductive layer 208 within the channel 212 in the dielectric layer 203. (Ex. 1005, 12 (“In an embodiment, as will be described in further detail below, the conductive lines are recessed to a depth that is determined according to the thickness of the cover layer.”), 17 (“As shown in FIG. 2H, a cover layer 215 is deposited onto the recessed conductive lines 208 in the channel 212.”).) As such, the upper surface of the recessed conductive layer 208 is

inside the channel 212 and below the upper surface of the dielectric layer 203. (Ex. 1002, ¶53.)

Boyanov '569 further discloses that the conductive layer (“first conductive material”) includes copper. (Ex. 1005, 11 (“For example, if the material of the conductive layer 205 contains copper, the material of the seed layer also contains copper. In an embodiment, the conductive layer 205 includes, for example, copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), vanadium (V), molybdenum (Mo), palladium (Pd), gold (Au), silver (Ag), platinum (Pt), or any combination of the above.”), 15 (“For example, an oxidant in the chemical used to etch copper conductive lines is used to change the copper oxidation state from insoluble copper metal to soluble copper ions.”), 16 (“In another embodiment, the copper conductive lines are recessed by means of wet etching using a chemical comprising citric acid and a peroxide therein.”), 18 (“For example, the conductive line can be made of any metal including copper or aluminum.”).) (Ex. 1002, ¶54.)

e) **“a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”**

Boyanov '569 discloses this feature to the extent it can be understood.⁶ (Ex. 1002, ¶¶55-58.) For example, claim 1 of Boyanov '569 recites that the conductive structure includes “a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have the same width at a position where the first conductive material and the second conductive material

⁶ While the '183 patent does not provide any explanation as to what constitutes a “curved corner below the portion of the upper surface of the dielectric layer,” Petitioner assumes that such a claim feature is met by a structure that has an upper-surface profile similar to that of the capping layer 215 shown in figure 2H of the '183 patent. Petitioner, however, does not concede that claim 1 is not indefinite.

meet, wherein the second conductive material has an upper surface having a portion that is substantially coplanar with a portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer.” (Ex. 1005, claim 1.) As shown in annotated figure 2H below, the cover layer 215 (“second conductive material”) is on the upper surface of the conductive layer (“first conductive material”). (*Id.*, 17 (“As shown in FIG. 2H, a cover layer 215 is deposited onto the recessed conductive lines 208 in the channel 212. ... As shown in FIG. 2H, the cover layer 215 is disposed over the conductive lines 208 in the sidewalls of the channel 212. In one embodiment, the cover layer is deposited onto the recessed conductive line by using electroless plating (e.g., plating), chemical vapor deposition (CVD), physical vapor deposition (PVD), or any other selective deposition technique known to those skilled in the art of electronic device fabrication techniques.”), 18 (“In one embodiment, a cobalt cover layer is deposited into a channel on the recessed copper conductive layer.”); Ex. 1002, ¶55.)

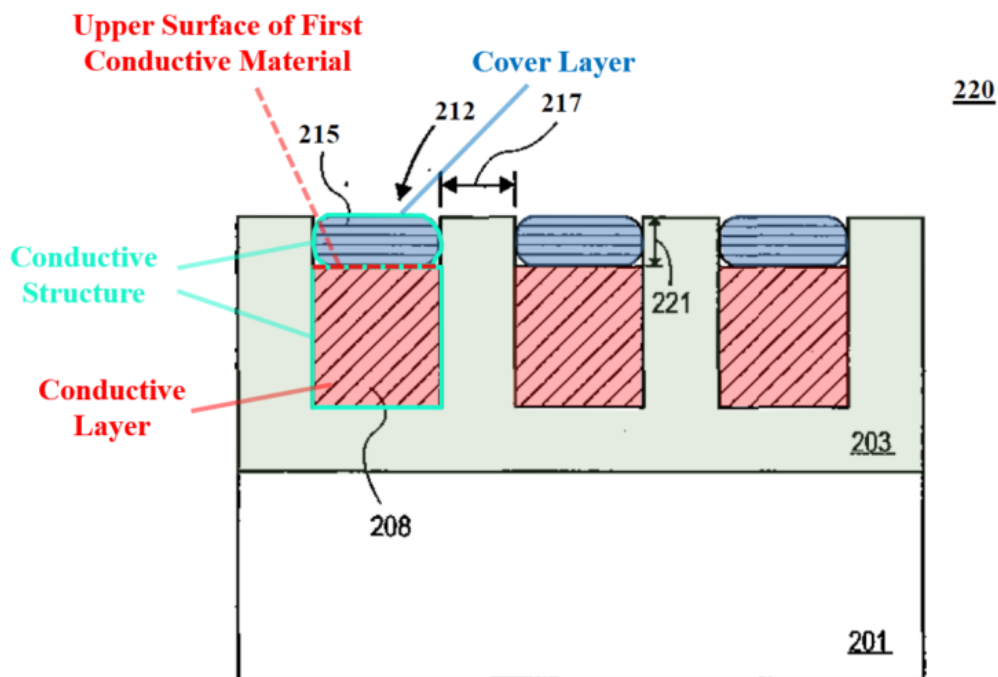


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶55.)

Boyantov '569 further discloses that the cover layer 215 includes cobalt. (Ex. 1005, 18 (“In one embodiment, the **cover layer such as the cover layer 215 is made of cobalt (Co)**, such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.”) For example, Boyantov '569 discloses that “a cobalt cover layer is deposited into a channel on the recessed copper conductive layer.” (Ex. 1005, 18; Ex. 1002, ¶56.)

While not depicted in figure 2H or any other figure, Boyanov '569 also discloses that the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet. (Ex. 1005, claim 1 (“the first conductive material and the second conductive material have the same width at a position where the first conductive material and the second conductive material meet”); Ex. 1002, ¶57.)

Boyanov '569 further discloses that the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer and also has a curved corner below the portion of the upper surface of the dielectric layer. (Ex. 1005, claim 1.) The second conductive material in figure 2H is shown to include a curved cover on the upper surface, where the curved corner is below the upper surface of the dielectric layer. (*Id.*, FIG. 2H; Ex. 1002, ¶58.)

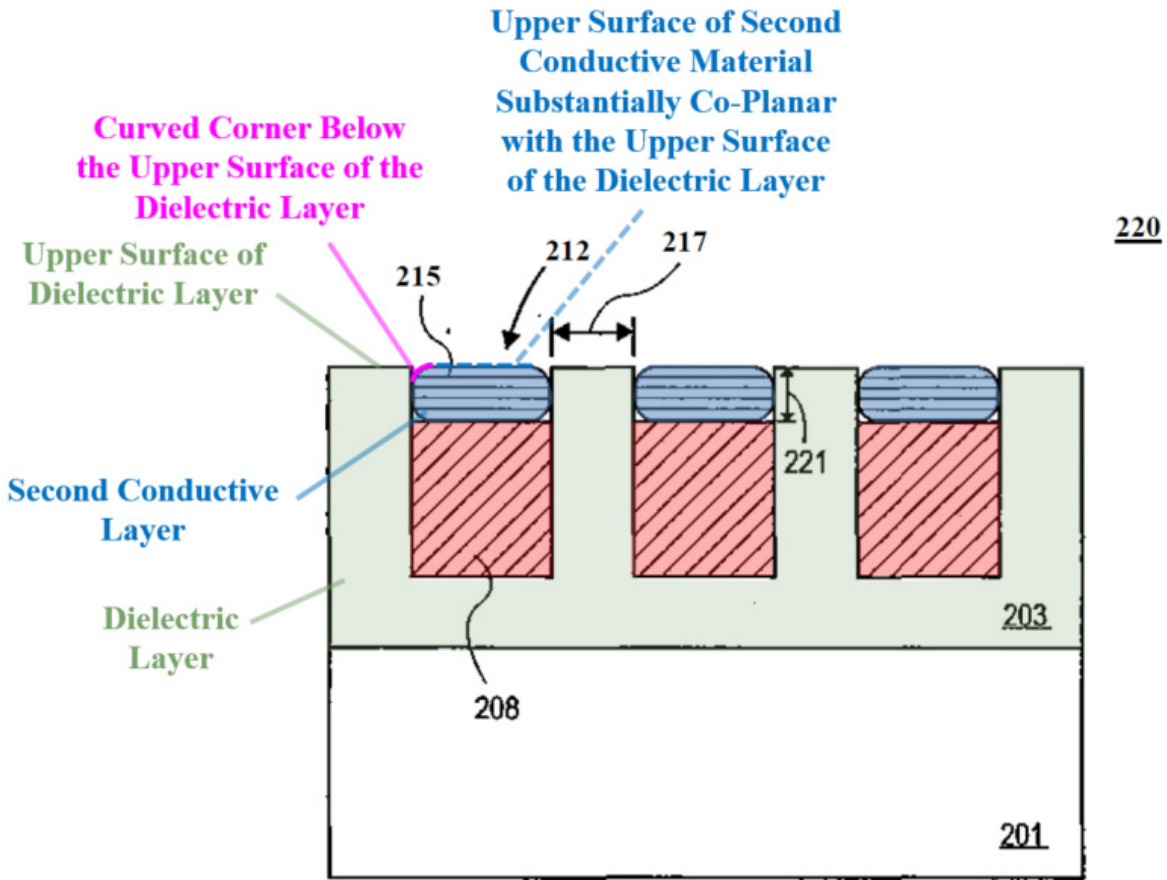


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶58.)

As such, Boyanov '569 discloses claim limitation 1[e], where claim 1 of Boyanov '569 includes all of the features included in claim limitation 1[e].

f) “a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”

Boyanov ’569 discloses this feature to the extent it can be understood.⁷ (Ex. 1002, ¶¶59-60.) For example, claim 1 of Boyanov ’569 recites “a barrier layer partially surrounding the electrically conductive structure, the barrier layer comprising tantalum.” (Ex. 1005, claim 1.) Boyanov ’569 discloses depositing a base layer in the openings of the dielectric layer before filling the openings with the conductive material to form the conductive lines, where the base layer includes a barrier layer comprising tantalum:

FIG. 2E is a view similar to FIG. 2D after deposition of a conductive layer 205 over dielectric layer 203 in accordance with an embodiment of the present invention. As shown in FIG. 2E, the formation of conductive layer 205 involves filling one or more openings in dielectric layer 203 with a conductive material to form one or more conductive lines. In one embodiment, **an inner sidewall**

⁷ While it is unclear what constitutes “partially surrounding,” Petitioner understands that a barrier layer that is in contact with the conductive structure and surrounds the conductive structure on three sides satisfies this limitation. Petitioner, however, does not concede that claim 1 is not indefinite.

and a base layer (not shown) at the bottom for covering the openings are first deposited on the dielectric layer 203, and then a conductive layer 205 is deposited on the base layer. In one embodiment, **the base layer comprises** a conductive seed layer deposited **on a conductive barrier layer (not shown).** The seed layer may comprise copper, and **the conductive barrier layer may comprise** aluminum, titanium, **tantalum, tantalum nitride**, and the like. The conductive barrier layer can be used to prevent the conductive material from diffusing from the seed layer such as copper to the ILD 203. Additionally, the conductive barrier layer can be used to provide adhesion of the seed layer (e.g., copper). In one embodiment, to form the base layer, **the conductive barrier layer is deposited onto the dielectric layer 203 to cover the sidewalls and bottom of the openings**, and then the seed layer is deposited on the conductive barrier layer.

(*Id.*, 9-10 (emphasis added); Ex. 1002, ¶59.)

Because the barrier layer is deposited onto the dielectric layer 203 to cover the sidewalls and bottoms of the openings and then the conductive material corresponding to the conductive layer 205 (“first conductive material”) and conductive material corresponding to the cover layer 215 (“second conductive material”) is later deposited in the openings lined with the barrier layer, the barrier

layer is on three sides of the conductive structure and therefore “partially surrounds” the conductive structure that includes the first and second conductive materials. (Ex. 1002, ¶60.)

2. Claim 2

“The integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶61.) For example, claim 2 of Boyanov ’569 recites “[t]he integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.” (Ex. 1005, claim 2.) Boyanov ’569 further discloses a barrier layer made of tantalum-nitride, which includes tantalum and nitrogen. (*Id.*, 10 (“The seed layer may comprise copper, and **the conductive barrier layer may comprise** aluminum, titanium, tantalum, **tantalum nitride**, and the like.”) (emphasis added); Ex. 1002, ¶61.)

3. Claim 3

“The integrated circuit structure of claim 1, wherein the second conductive material further comprises boron.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶62.) For example, claim 3 of Boyanov ’569 recites “[t]he integrated circuit structure of claim 1, wherein the second conductive material further comprises boron.” (Ex. 1005, claim 3.) Boyanov ’569 further discloses that the cover layer 215 can be made of an alloy that includes

cobalt (Co) (as required by claim 1) as well as boron (B) (as recited in claim 3). (*Id.*, 18 (“In one embodiment, the cover layer such as **the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.**”) (emphasis added); Ex. 1002, ¶62.)

4. Claim 4

“The integrated circuit structure of claim 3, wherein the second conductive material further comprises phosphorus.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶63.) For example, claim 4 of Boyanov ’569 recites “[t]he integrated circuit structure of claim 3, wherein the second conductive material further comprises phosphorus.” (Ex. 1005, claim 4.) Boyanov ’569 further discloses that the cover layer 215 can be made of an alloy that includes cobalt (Co) (as required by claim 1) as well as boron (B) (as recited in claim 3) and phosphorous (P) (as recited in claim 4). (*Id.*, 18 (“In one embodiment, the cover layer such as **the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.**”) (emphasis added); Ex. 1002, ¶63.)

5. Claim 5

“The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶64.) For example, claim 5 of Boyanov '569 recites “[t]he integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten.” (Ex. 1005, claim 5.) Boyanov '569 further discloses that the cover layer 215 can be made of an alloy that includes cobalt (Co) (as required by claim 1) as well as boron (B) (as recited in claim 3) and tungsten (W) (as recited in claim 5). (*Id.*, 18 (“In one embodiment, the cover layer such as **the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.**”) (emphasis added); Ex. 1002, ¶64.)

6. Claim 6

“The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten and phosphorus.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶65.) For example, claim 6 of Boyanov '569 recites “[t]he integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten and phosphorus.” (Ex. 1005,

claim 6.) Boyanov '569 further discloses that the cover layer 215 can be made of an alloy that includes cobalt (Co) (as required by claim 1) as well as boron (B) (as recited in claim 3), tungsten (W) (as recited in claim 6), and phosphorous (P) (as also recited in claim 6). (*Id.*, 18 (“In one embodiment, the cover layer such as **the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.**”) (emphasis added); Ex. 1002, ¶65.)

7. Claim 7

“The integrated circuit structure of claim 1, wherein the second conductive material further comprises phosphorus.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶66.) For example, claim 7 of Boyanov '569 recites “[t]he integrated circuit structure of claim 1, wherein the second conductive material further comprises phosphorus.” (Ex. 1005, claim 7.) Boyanov '569 further discloses that the cover layer 215 can be made of an alloy that includes cobalt (Co) (as required by claim 1) as well as phosphorus (P) (as recited in claim 7). (*Id.*, 18 (“In one embodiment, the cover layer such as **the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt**

tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.” (emphasis added); Ex. 1002, ¶66.)

8. Claim 8

“The integrated circuit structure of claim 7, wherein the second conductive material further comprises tungsten.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶67.) For example, claim 8 of Boyanov ’569 recites “[t]he integrated circuit structure of claim 7, wherein the second conductive material further comprises tungsten.” (Ex. 1005, claim 8.) Boyanov ’569 further discloses that the cover layer 215 can be made of an alloy that includes cobalt (Co) (as required by claim 1) as well as phosphorus (P) (as recited in claim 7) and tungsten (W) (as recited in claim 8). (*Id.*, 18 (“In one embodiment, the cover layer such as **the cover layer 215 is made of cobalt (Co), such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten phosphate (CoWP), or any combination of the above.”**) (emphasis added); Ex. 1002, ¶67.)

9. Claim 9

a) “A method of fabricating an integrated circuit structure, the method comprising:”

To the extent the preamble is limiting, Boyanov ’569 discloses “method of fabricating an integrated circuit structure.” (Ex. 1002, ¶¶68-69.) For example, claim 9 of Boyanov ’569 recites “A method of fabricating an integrated circuit structure,” where the method of claim 9 of Boyanov ’569 includes the same steps as those recited in claim 9 of the ’183 patent.” (*Compare* Ex. 1005, claim 9 *with* Ex. 1001, claim 9; Ex. 1002, ¶68.) Boyanov ’569 is entitled “Methods and Apparatuses to Form Self Aligned Caps” (Ex. 1005, Title), where Boyanov ’569 discloses how to form the interconnect structure shown in figure 2H below that is included as a part of an integrated circuit. (Ex. 1005, 3-4 (describing figures 2A-2H as “a cross-sectional view of a substrate used to fabricate an interconnect structure in accordance with an embodiment of the present invention”), 6 (“The present invention describes methods and apparatus for controlling line edge roughness (LER) and line-to-line spacing when depositing self-aligning metal caps. ... When the increase in LER is eliminated and the line-to-line spacing is prevented from being reduced, the risk of failure can be reduced, and the manufacturing yield of a small-sized (e.g., nano-scale) electronic device can be improved. The **electronic devices can be** computer system architecture devices such as transistors, **memories, logic devices, and the**

like, as well as any other integrated circuit and microelectronic device.”)

(emphasis added); Ex. 1002, ¶69.)

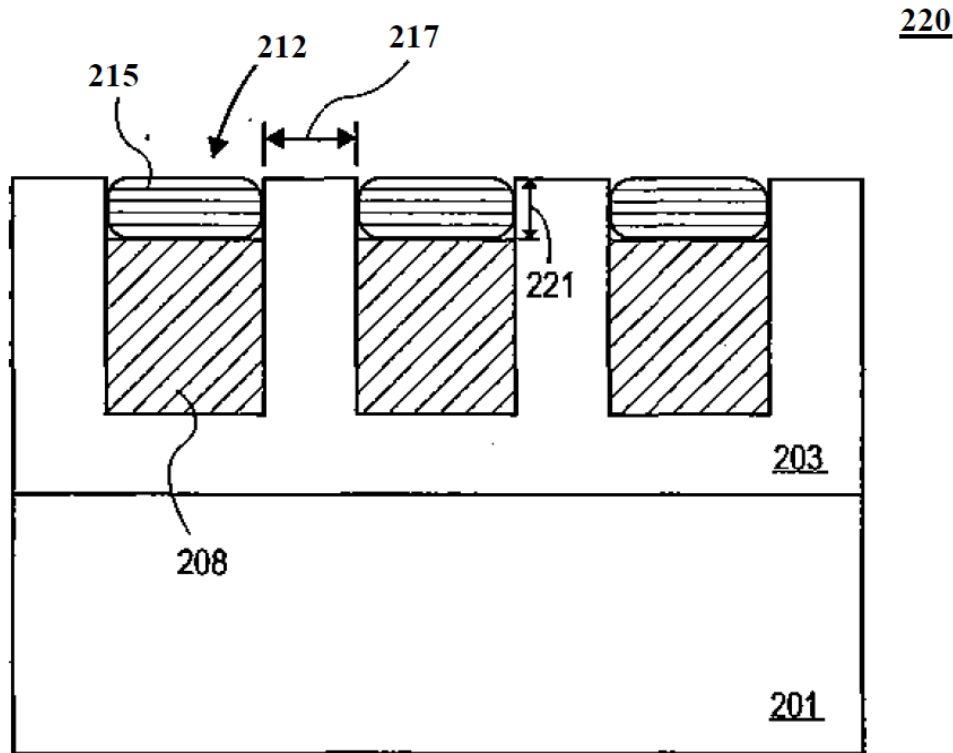


FIG. 2H

(Ex. 1005, FIG. 2H.)

b) “forming a dielectric layer comprising silicon, oxygen and carbon;”

Boyanov ’569 discloses this claim feature. (Ex. 1002, ¶¶70-71.) For example, claim 9 of as Boyanov ’569 recites “forming a dielectric layer comprising silicon, oxygen, and carbon.” (Ex. 1005, claim 1.) As shown in annotated figures 2B and 2H below, Boyanov ’569 discloses forming a dielectric layer as a part of the

integrated circuit structure. (Ex. 1005, 3-4 (describing figures 2A-2H as “a cross-sectional view of a substrate used to fabricate an interconnect structure in accordance with an embodiment of the present invention”), 3 (“FIG. 2B is a view similar to FIG. 2A after **forming a dielectric layer 203** over the substrate 201 in accordance with an embodiment of the present invention. In one embodiment, the dielectric layer 203 is an interlayer dielectric (ILD).”); Ex. 1002, ¶70.)

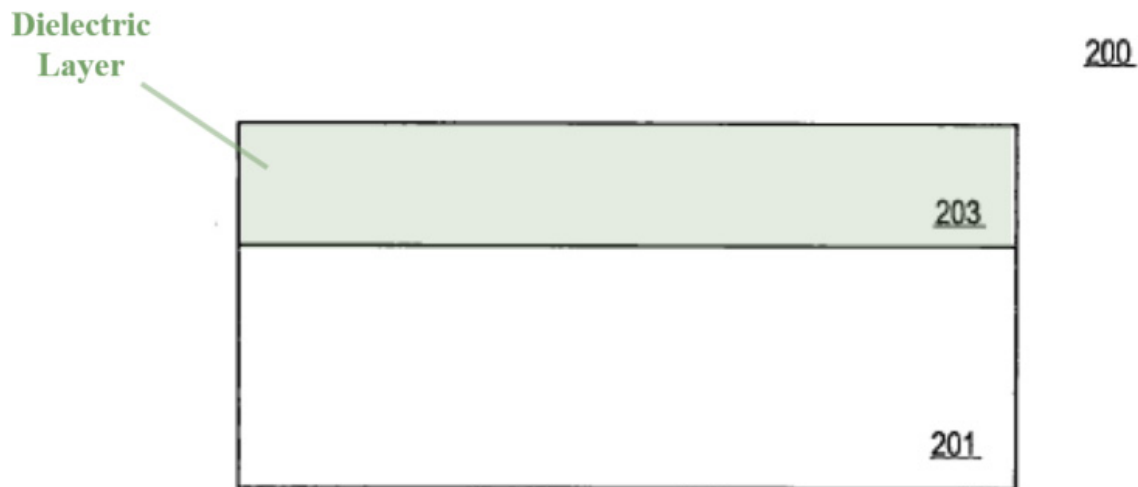


FIG. 2B

(Ex. 1005, FIG. 2B (annotated); Ex. 1002, ¶70.)

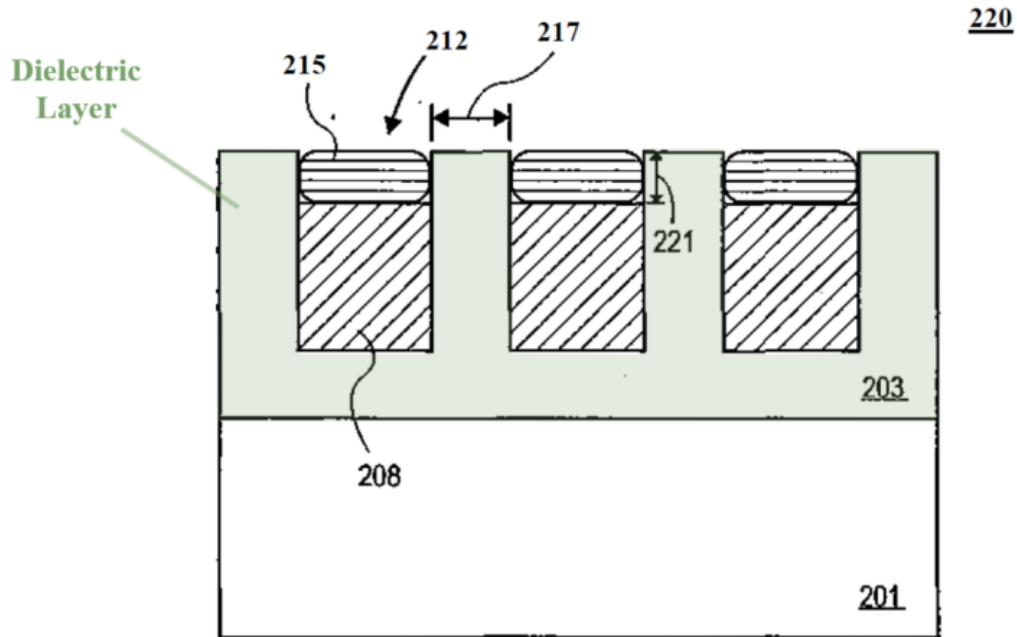


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶70.)

Boyanov '569 further discloses that the dielectric layer includes silicon, oxygen, and carbon. (Ex. 1005, 7 (“In one embodiment, dielectric layer 203 is a low-k dielectric such as silicon dioxide, silicon oxide, **carbon doped oxides (CDO), or any combination of the above.** In one embodiment, the dielectric layer 203 comprises a nitride, an oxide, a polymer, a phosphosilicate glass, a fluorosilicate glass (SiOF), an organosilicate glass (**SiOCH**), or any combination of the above.”) (emphasis added); Ex. 1002, ¶71.)

c) “forming a trench in the dielectric layer;”

Boyanov '569 discloses this feature. (Ex. 1002, ¶¶72-73.) For example, claim 9 of Boyanov '569 recites “forming a trench in the dielectric layer.” (Ex. 1005, claim 9.) Boyanov '569 discloses a forming an opening 206 (“trench”) in the dielectric layer 203:

FIG. 2D is a diagram similar to FIG. 2C after one or more openings, such as openings 206, are formed in dielectric layer 203 in accordance with an embodiment of the present invention. In an embodiment, such openings, such as openings 206, are implemented via openings in dielectric layer 203, such as openings 220. In another embodiment, the openings are formed by etching the dielectric layer through the openings in the patterned photoresist 204 deposited directly onto the dielectric layer 203. In an embodiment, **an opening such as a trench or the like in the dielectric layer 203 is formed** using anisotropic dry etching such as laser etching. In another embodiment, the openings in the dielectric layer 203 are formed using dry etching, wet etching, or a combination of techniques known to those of ordinary skill in the art of microelectronic device fabrication.

(*Id.*, 9 (emphasis added); Ex. 1002, ¶72.)

The opening 206 (“trench”) formed in the dielectric layer is shown in annotated figures 2D and 2H below.

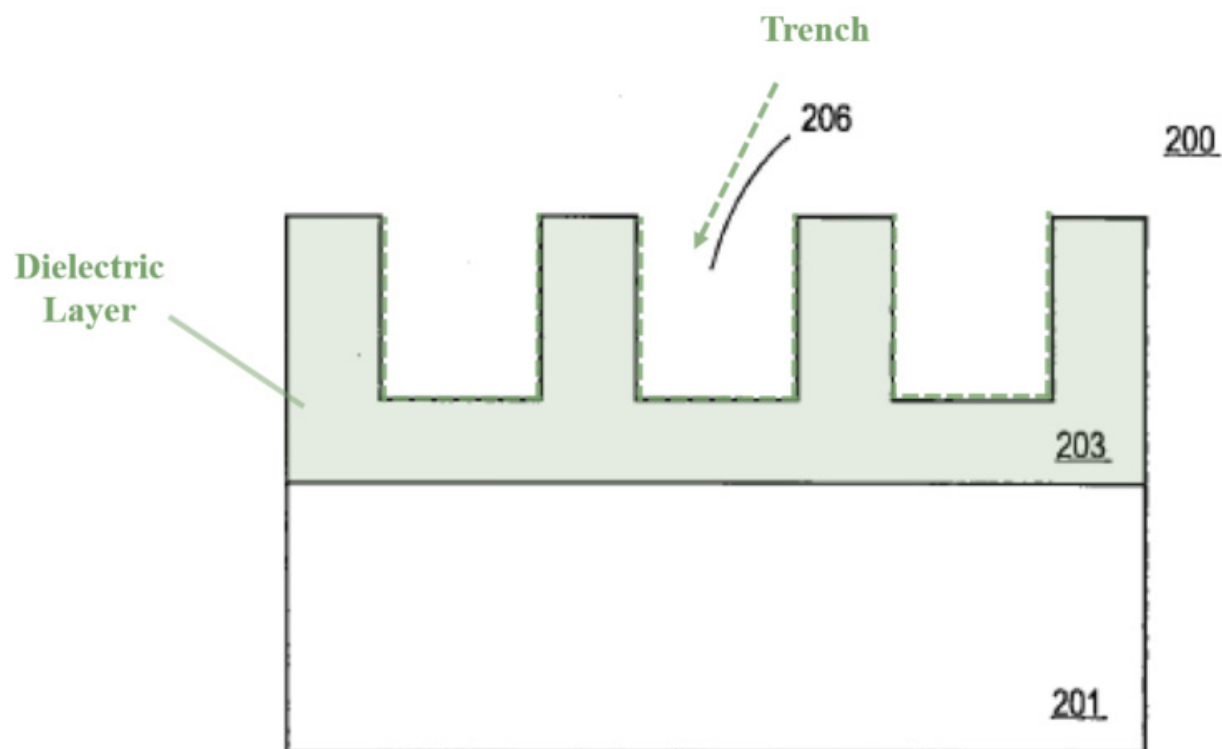


FIG. 2D

(Ex. 1005, FIG. 2D (annotated); Ex. 1002, ¶73.)

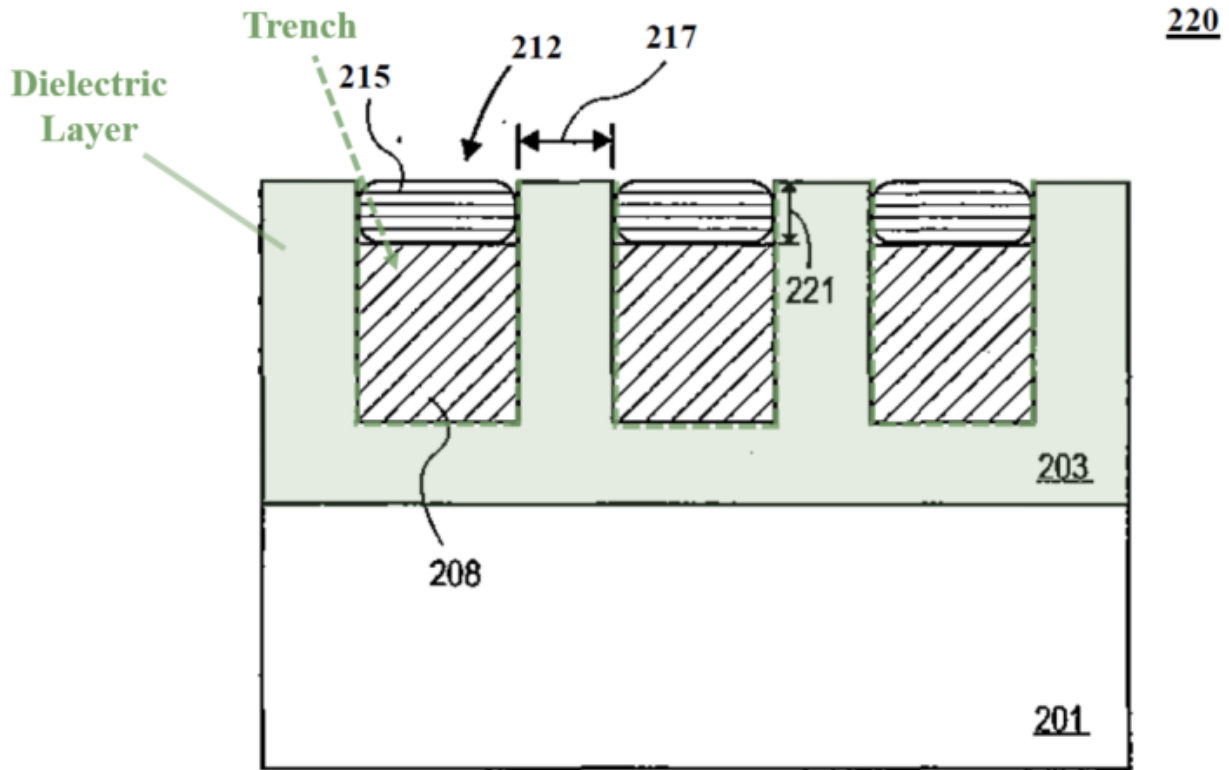


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶73.)

d) “forming a barrier layer in the trench, the barrier layer comprising tantalum;”

Boyanov '569 discloses this feature. (Ex. 1002, ¶74.) For example, claim 9 of Boyanov '569 recites “forming a barrier layer in the trench, the barrier layer comprising tantalum.” (Ex. 1005, claim 9.) Boyanov '569 discloses depositing a base layer in the opening (“trench”) of the dielectric layer before filling the opening

with the conductive material to form the conductive lines, where the base layer includes a barrier layer comprising tantalum:

FIG. 2E is a view similar to FIG. 2D after deposition of a conductive layer 205 over dielectric layer 203 in accordance with an embodiment of the present invention. As shown in FIG. 2E, the formation of conductive layer 205 involves filling one or more openings in dielectric layer 203 with a conductive material to form one or more conductive lines. In one embodiment, **an inner sidewall and a base layer (not shown) at the bottom for covering the openings are first deposited on the dielectric layer 203, and then a conductive layer 205 is deposited on the base layer.** In one embodiment, **the base layer comprises a conductive seed layer deposited on a conductive barrier layer (not shown).** The seed layer may comprise copper, and **the conductive barrier layer may comprise aluminum, titanium, tantalum, tantalum nitride,** and the like. The conductive barrier layer can be used to prevent the conductive material from diffusing from the seed layer such as copper to the ILD 203. Additionally, the conductive barrier layer can be used to provide adhesion of the seed layer (e.g., copper). In one embodiment, to form the base layer, the conductive barrier layer is deposited onto the dielectric layer 203 to cover the

sidewalls and bottom of the openings, and then the seed layer is deposited on the conductive barrier layer.

(*Id.*, 9-10 (emphasis added); Ex. 1002, ¶74.)

e) **“forming a first conductive material within the barrier layer, the first conductive material comprising copper;”**

Boyanov '569 discloses this feature. (Ex. 1002, ¶¶75-78.) For example, claim 9 of Boyanov '569 recites “forming a first conductive material in the barrier layer, the first conductive material comprising copper.” (Ex. 1005, claim 9.) Boyanov '569 discloses forming a conductive layer 205 (“first conductive material”), where, as discussed above for claim element 9[d], the conductive layer 205 is formed following formation of the barrier layer in the trench:

FIG. 2E is a view similar to FIG. 2D **after deposition of a conductive layer 205** over dielectric layer 203 in accordance with an embodiment of the present invention. As shown in FIG. 2E, **the formation of conductive layer 205 involves filling one or more openings in dielectric layer 203 with a conductive material to form one or more conductive lines.** In one embodiment, **an inner sidewall and a base layer (not shown) at the bottom for covering the openings are first deposited on the dielectric layer 203, and then a conductive layer 205 is deposited on the base layer.**

(*Id.*, 9-10 (emphasis added); Ex. 1002, ¶75.)

The conductive layer 205 (“first conductive material”) is shown in annotated figures 2E and 2H below, where, as discussed below for claim limitation 9[f], the conductive layer 205 is recessed in figure 2H, where the recessed conductive layer is shown as conductive layer 208. (Ex. 1002, ¶76.)

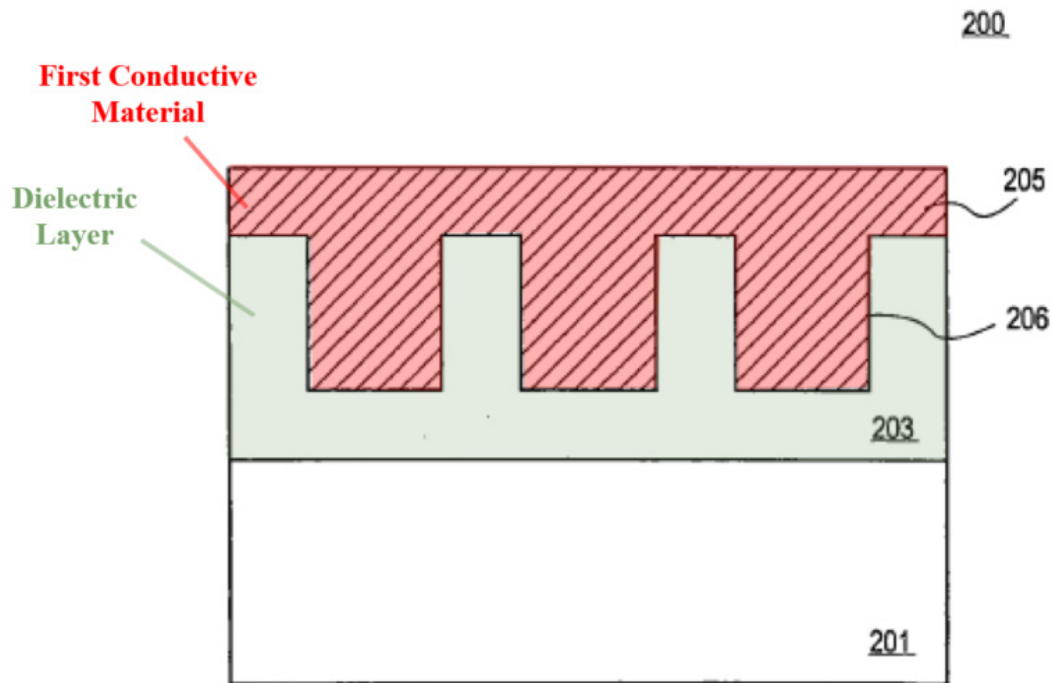
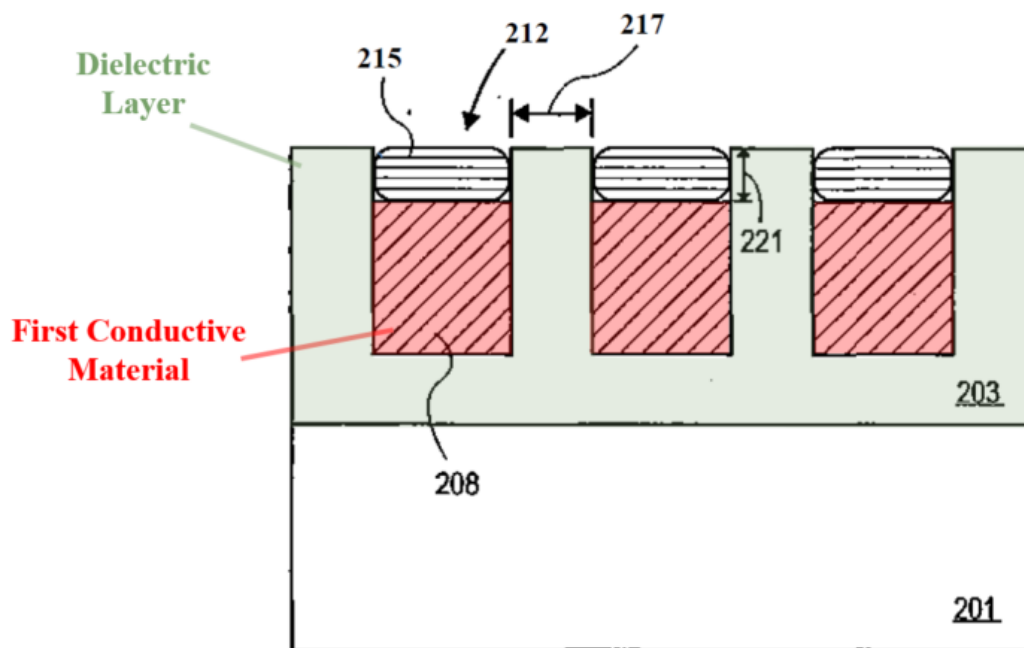


FIG. 2E

(Ex. 1005, FIG. 2E (annotated); Ex. 1002, ¶76.)



(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶76.)

Boyanov '569 discloses that the conductive layer 205 (“first conductive material”) includes copper. (Ex. 1005, 10 (“Conductive layer 205 fills the openings, such as openings 206, and covers portions of the base layer (not shown) that are

outside of the openings on top of the dielectric layer 203. In one embodiment, a conductive layer 205, such as copper, is deposited onto the seed layer of the copper base layer by an electroplating process.”), 11 (“For example, if the material of the conductive layer 205 contains copper, the material of the seed layer also contains copper. In an embodiment, the conductive layer 205 includes, for example, copper (Cu), ruthenium (Ru), nickel (Ni), cobalt (Co), chromium (Cr), iron (Fe), manganese (Mn), titanium (Ti), aluminum (Al), hafnium (Hf), tantalum (Ta), tungsten (W), vanadium (V), molybdenum (Mo), palladium (Pd), gold (Au), silver (Ag), platinum (Pt), or any combination of the above.”); Ex. 1002, ¶78.)

f) “recessing the first conductive material below a portion of an upper surface of the dielectric layer; and”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶¶79-80.) For example, claim 9 of Boyanov ’569 recites “recessing the first conductive material below a portion of an upper surface of the dielectric layer.” (Ex. 1005, claim 9.) Boyanov ’569 discloses recessing the conductive line 208 in the dielectric layer to form a channel below the upper surface of the dielectric layer. (*Id.*, 12 (“FIG. 2G is a diagram similar to FIG. 2F after **recessing a conductive line such as conductive line 208 in a dielectric layer** over a substrate in accordance with an embodiment of the present invention. As shown in FIG. 2G, a channel such as the channel 212 is formed in the

dielectric layer 203.”) As shown in annotated figures 2G and 2H below, the conductive line 208 (“first conductive material”) is recessed below the upper surface of the dielectric layer.

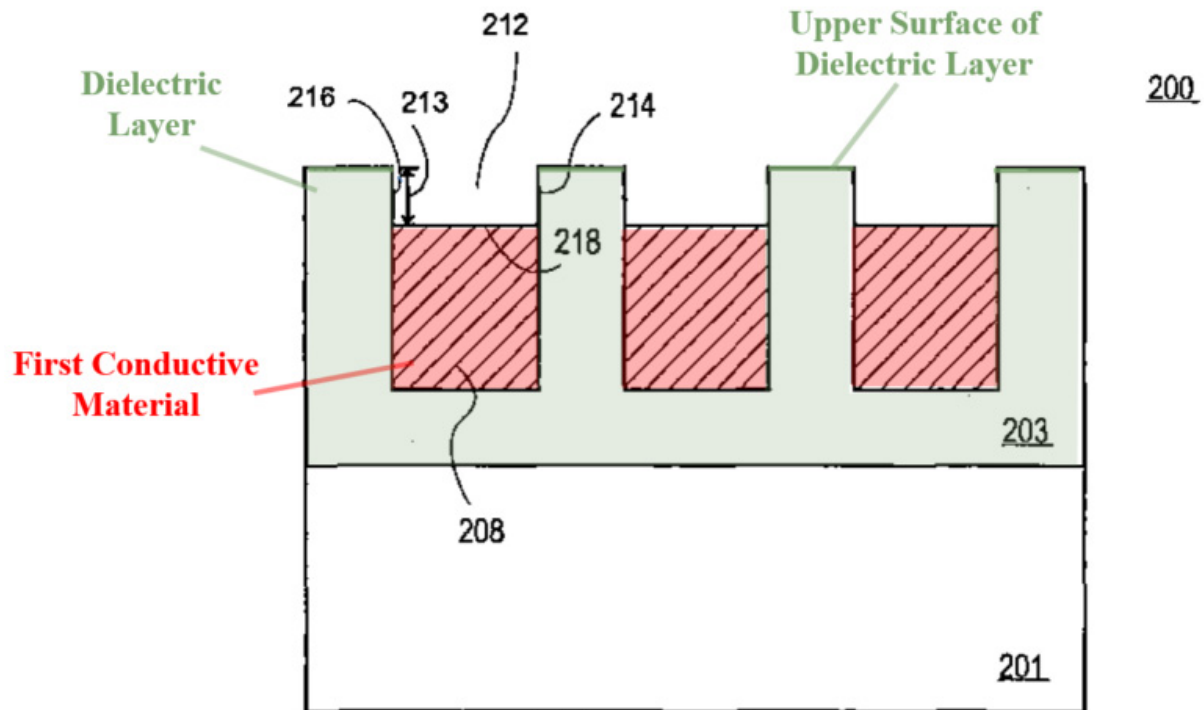


FIG. 2G

(Ex. 1005, FIG. 2G (annotated); Ex. 1002, ¶79.)

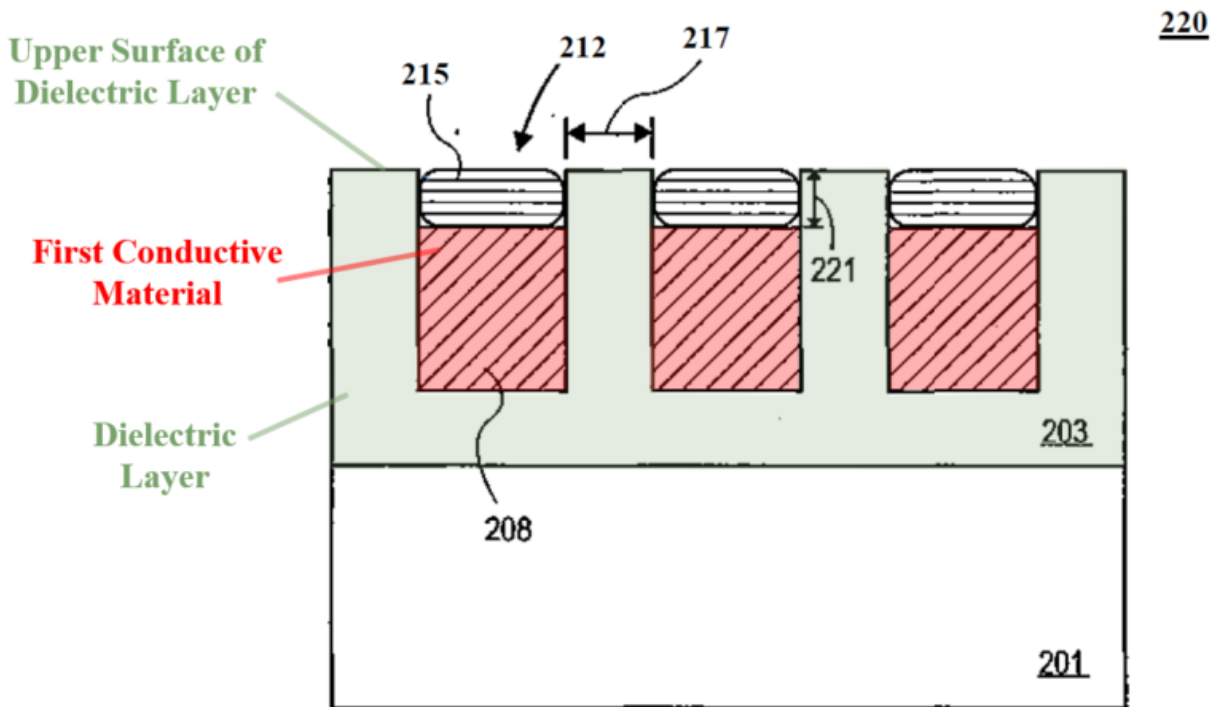


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶79.)

Boyanov '569 discloses that the conductive layer 208 is recessed in order to allow the cover layer 215 to be formed over the conductive layer 208 within the channel 212 in the dielectric layer 203. (Ex. 1005, 12 (“In an embodiment, as will be described in further detail below, the conductive lines are recessed to a depth that is determined according to the thickness of the cover layer.”), 17 (“As shown in FIG. 2H, a cover layer 215 is deposited onto the recessed conductive lines 208 in the channel 212.”); Ex. 1002, ¶80.)

g) “forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a position where the first conductive material and the second conductive material meet, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶¶81-84.) For example, claim 9 of Boyanov '569 recites “forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have the same width at a position where the first conductive material and the second conductive material meet, and wherein the upper surface of the second electrically conductive material has a curved corner below the portion of the upper surface of the dielectric layer.” (Ex. 1005, claim 9.) Boyanov '569 discloses depositing cover layers 215 (“second conductive material”) on the upper surface of the recessed conductive lines in order to prevent electromigration of the conductive layer 208 (“first conductive material”). (*Id.*, 17 (“FIG. 2H is a diagram similar to FIG. 2G after electromigration is prevented by selectively depositing the cover layers into the respective recessed conductive lines in the channels in accordance with an embodiment of the present invention.”); Ex. 1002, ¶81.) As shown in

annotated figure 2H below, the cover layer 215 (“second conductive material”) is on the upper surface of the conductive layer 208 (“first conductive material”).

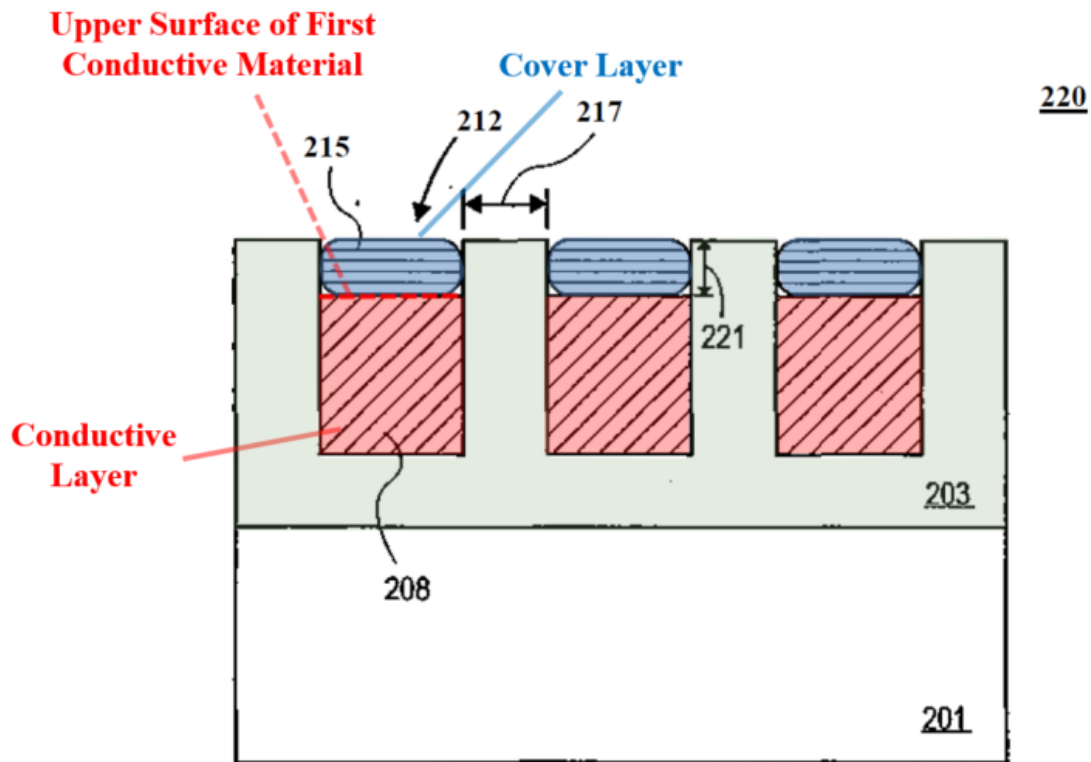


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶81.)

Boyanov '569 further discloses that the cover layer 215 (“second conductive material”) includes cobalt. (Ex. 1005, 18 (“In one embodiment, the **cover layer such as the cover layer 215 is made of cobalt (Co)**, such as electroless cobalt alloys like cobalt borophosphide (CoBP), cobalt tungsten borophosphide (CoWBP), cobalt tungsten phosphide (CoWP), cobalt tungsten boride (CoWB), cobalt tungsten

phosphate (CoWP), or any combination of the above.”) For example, Boyanov ’569 discloses that “a cobalt cover layer is deposited into a channel on the recessed copper conductive layer.”); Ex. 1002, ¶82.)

While not depicted in figure 2H or any other figure, Boyanov ’569 also discloses that the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet. (Ex. 1005, claim 9 (“the first conductive material and the second conductive material have the same width at a position where the first conductive material and the second conductive material meet”); Ex. 1002, ¶83.)

Boyanov ’569 further discloses that the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer and also has a curved corner below the portion of the upper surface of the dielectric layer. (Ex. 1005, claim 9; Ex. 1002, ¶84.) Figure 2H shows that the second conductive material has a portion that is substantially co-planar with the surface of the dielectric layer and also includes a curved corner as recited in claim 9. (Ex. 1005, FIG. 2H; Ex. 1002, ¶84.)

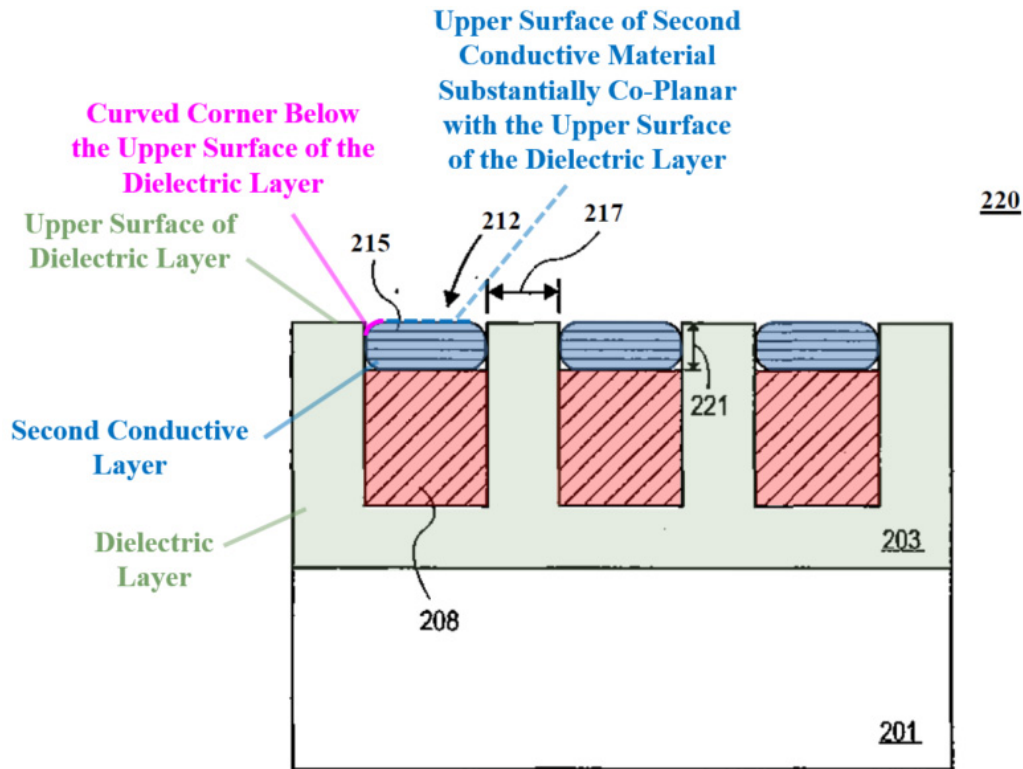


FIG. 2H

(Ex. 1005, FIG. 2H (annotated); Ex. 1002, ¶84.)

As such, Boyanov '569 discloses claim limitation 9[g], where claim 9 of Boyanov '569 includes all of the features included in claim limitation 9[g].

10. Claim 10

“The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶85.) For example, claim 10 of Boyanov '569 recites “[t]he method of claim 9, wherein the step of recessing the first conductive material below the portion of the upper surface of the dielectric layer

comprises using a wet etch process.” (Ex. 1005, claim 10.) Boyanov ’569 discloses using wet etching to recess the conductive lines (“first conductive material”). (Ex. 1005, 13-14 (“In one embodiment, **recessing conductive lines** such as lines 208, lines 304, and 305 **involves uniformly wet etching the conductive lines** using a chemical comprising an etchant, oxidant, an inhibitor, and a solvent in a manner that is independent of crystal orientation.”) (emphasis added); Ex. 1002, ¶85.)

11. Claim 11

“The method of claim 9, wherein the barrier layer further comprises nitrogen.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶86.) For example, claim 11 of Boyanov ’569 recites “[t]he method of claim 9, wherein the barrier layer further comprises nitrogen.” (Ex. 1005, claim 11.) Boyanov ’569 also discloses claim 11 for the same reasons discussed above with respect to claim 2. (*Supra* section IX.A.2.)

12. Claim 12

“The method of claim 9, wherein the second conductive material further comprises boron.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶87.) For example, claim 12 of Boyanov ’569 recites “[t]he method of claim 9, wherein the second conductive material further comprises boron.” (Ex. 1005, claim 12.) Boyanov ’569 also

discloses claim 12 for the same reasons discussed above with respect to claim 3.
(*Supra* section IX.A.3.)

13. Claim 13

“The method of claim 12, wherein the second conductive material further comprises phosphorus.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶88.) For example, claim 13 of Boyanov ’569 recites “[t]he method of claim 12, wherein the second electrically conductive material further comprises phosphorus.” (Ex. 1005, claim 13.) Boyanov ’569 also discloses claim 13 for the same reasons discussed above with respect to claim 4. (*Supra* section IX.A.4.)

14. Claim 14

“The method of claim 12, wherein the second conductive material further comprises tungsten.”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶89.) For example, claim 14 of Boyanov ’569 recites “[t]he method of claim 12, wherein the second conductive material further comprises tungsten.” (Ex. 1005, claim 14.) Boyanov ’569 also discloses claim 14 for the same reasons discussed above with respect to claim 5.
(*Supra* section IX.A.5.)

15. Claim 15

“The method of claim 12, wherein the second conductive material further comprises tungsten and phosphorus.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶90.) For example, claim 15 of Boyanov '569 recites “[t]he method of claim 12, wherein the second conductive material further comprises tungsten and phosphorus.” (Ex. 1005, claim 15.) Boyanov '569 also discloses claim 15 for the same reasons discussed above with respect to claim 6. (*Supra* section IX.A.6.)

16. Claim 16

“The method of claim 9, wherein the second conductive material further comprises phosphorus.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶91.) For example, claim 16 of Boyanov '569 recites “[t]he method of claim 9, wherein the second conductive material further comprises phosphorus.” (Ex. 1005, claim 16.) Boyanov '569 also discloses claim 16 for the same reasons discussed above with respect to claim 7. (*Supra* section IX.A.7.)

17. Claim 17

“The method of claim 16, wherein the second conductive material further comprises tungsten.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶92.) For example, claim 17 of Boyanov '569 recites “[t]he method of claim 16, wherein the second conductive material further comprises tungsten.” (Ex. 1005, claim 17.) Boyanov '569 also

discloses claim 17 for the same reasons discussed above with respect to claim 8.

(*Supra* section IX.A.8.)

18. Claim 18

a) “A computing device, comprising:”

To the extent the preamble is limiting, Boyanov ’569 discloses “a computing device.” (Ex. 1002, ¶93.) For example, figure 5 of Boyanov ’569 below shows a computing device. (Ex. 1005, 24 (“In an alternative embodiment, FIG. 5 illustrates a computing device 500.”); Ex. 1002, ¶93.)

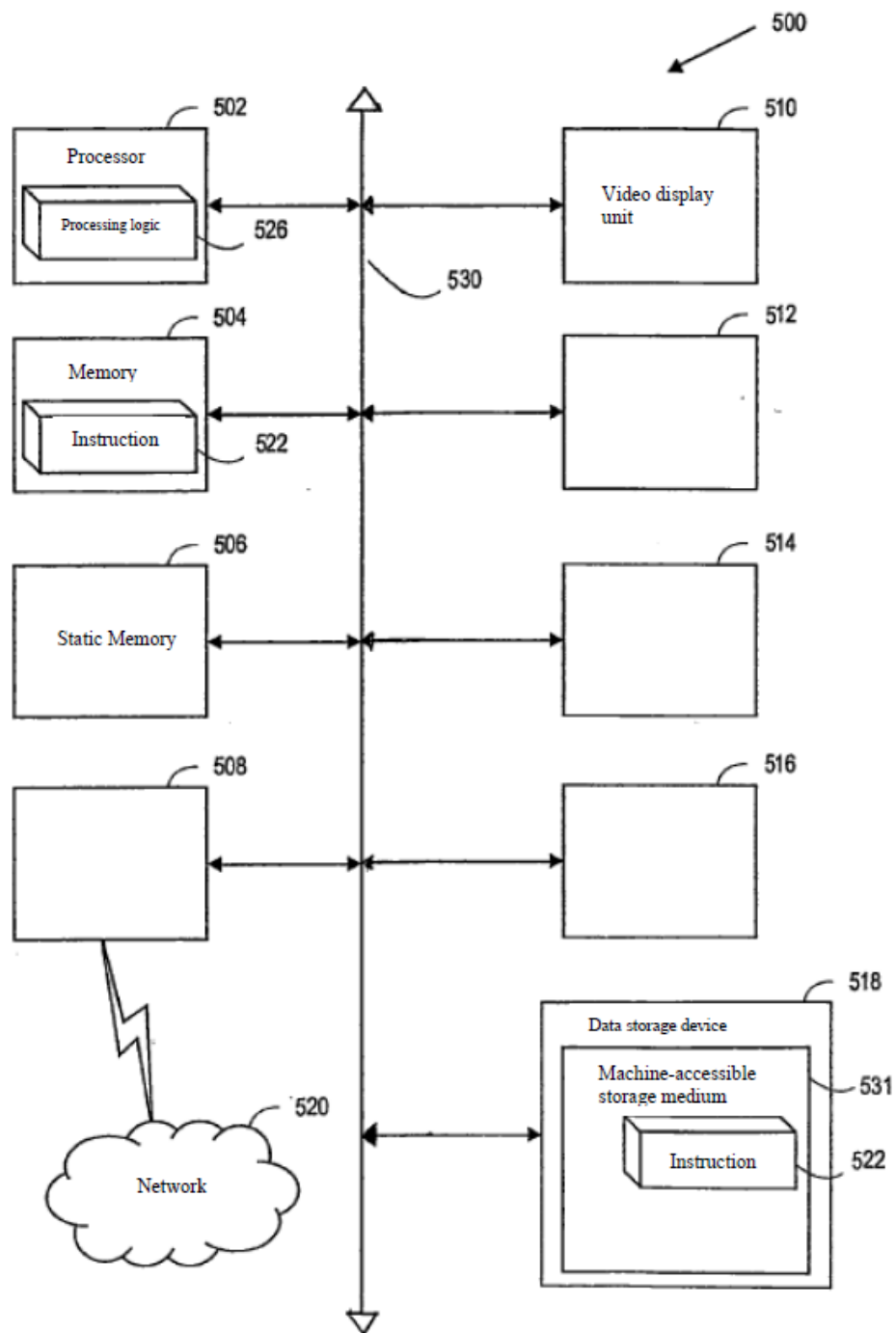


FIG. 5

(Ex. 1005, FIG. 5.)

b) “a board;”

Boyanov ’569 discloses this claim feature. (Ex. 1002, ¶94.) For example, Boyanov ’569 discloses that the computing device shown in figure 5 includes a board 530. ((Ex. 1005, 24 (“The computing device 500 is provided with a board 530.”); Ex. 1002, ¶94.)

c) “a component coupled to the board, the component including an integrated circuit structure, comprising:”

Boyanov ’569 discloses this feature. (Ex. 1002, ¶¶95-96.) For example, Boyanov ’569 discloses a processor 502, a communication chip 508, and additional “components” coupled to the board:

The **board can include some components** including, but not limited to, a processor 502 and at least one communication chip 508. **Processor 502 is physically and electrically coupled to the board 530.** In some embodiments, the **at least one communication chip is also physically and electrically coupled to the board 530.** In a further embodiment, the communication chip 508 is integrated within the processor 502.

(Ex. 1005, 24 (emphasis added); Ex. 1002, ¶95.)

Boyanov ’569 further discloses components coupled to the board that include an integrated circuit die (“integrated circuit structure”). (Ex. 1005, 25 (“Processor

502 of computing device 500 includes an integrated circuit die packaged within processor 502.”); 26 (“The communication chip 508 also includes an integrated circuit die that is packaged within the communication chip 508.”), (“In a further embodiment, additional components disposed within the computing device 500 can include an integrated circuit die”); Ex. 1002, ¶96.)

- d) “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen, and carbon;”**
- e) “a conductive structure in the dielectric layer, the conductive structure comprising:”**
- f) “a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”**
- g) “a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”**
- h) “a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”**

Boyanov '569 discloses these features. (Ex. 1002, ¶¶97-98.) For example Boyanov '569 discloses that the integrated circuit devices of the components included in the computing device discussed above for claim element 18[c] and shown in figure 5 include transistors or interconnect that are formed using “the method and apparatus that control line edge roughness and line-to-line spacing

during the deposition of self aligning metal caps in the manner in accordance with the invention.” (Ex. 1005, 26; *see also id.*, 25-26 (“In some embodiments of the invention, the integrated circuit die of the processor comprises one or more devices, such as a transistor or a metal interconnect, wherein the one or more devices are formed by using the method and apparatus that control line edge roughness and line-to-line spacing during deposition of self-aligning metal caps in the manner in accordance with the invention.”), 26 (“In accordance with another embodiment of the present invention, the integrated circuit die of the communication chip includes one or more devices such as a transistor or a metal interconnect, wherein the one or more devices are formed by using the method and apparatus that control line edge roughness and line-to-line spacing during deposition of self-aligning metal caps in the manner in accordance with the invention.”), 20 (“FIG. 5 illustrates a block diagram of an embodiment of a data processing system 500 having a memory such as a transistor, memory 504 and memory 518, processing logic devices such as processing logic device 526, and any other integrated circuit and microelectronic device constructed using the methods described above. As shown in FIG. 5, the data processing system 500 includes a processor 502 having processing logic 526. In at least some embodiments, processing logic 526 includes: at least one conductive line in a dielectric layer over a substrate; a channel in the dielectric layer and above the

conductive line; and a cover layer on the at least one conductive line in the channel, the cover layer preventing electromigration in the manner previously described.”); Ex. 1002, ¶97.)

The “transistors or interconnect” (“conductive structures”) included in the components of the computing device include the “dielectric layer,” the “first conductive material,” the “conductive structure,” the “second conductive material,” and the “barrier layer” recited in claim elements 18[d]-18[h] for the same reasons discussed above for claim elements 1[b]-1[f]. (*Supra* sections IX.A.1(b)-(f); Ex. 1002, ¶98.)

19. Claim 19

**“The computing device of claim 18, further comprising:
a memory coupled to the board.”**

Boyanov ’569 discloses this feature. (Ex. 1002, ¶99.) For example, Boyanov ’569 discloses that the computing device of figure 5 includes a memory coupled to the board. (Ex. 1005, 20 (“FIG. 5 illustrates a block diagram of an embodiment of a **data processing system 500 having a memory** such as a transistor, memory 504 and memory 518, processing logic devices such as processing logic device 526, and any other integrated circuit and microelectronic device constructed using the methods described above.”) (emphasis added); *see also id.*, 21-22 (“The exemplary

data processing system 500 includes a processor 502, a main memory 504 (e.g., Read Only Memory (ROM), flash memory, and Dynamic Random Access Memory (DRAM) such as Synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM)), a static memory 506 (e.g., flash memory and static random access memory (SRAM)), and an auxiliary memory 518 (for example, a data storage device) that communicate with each other via a bus 530.”), 24 (“Computing device 500 can include other components that may or may not be physically and electrically coupled to board 530 depending on its application. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory”); Ex. 1002, ¶99.)

20. Claim 20

**“The computing device of claim 18, further comprising:
a communication chip coupled to the board.”**

Boyanov ’569 discloses this feature. (Ex. 1002, ¶100.) For example, Boyanov ’569 discloses that the computing device of figure 5 includes a communication chip coupled to the board. (Ex. 1005, 24 (“The **board can include some components including**, but not limited to, a processor 502 and **at least one communication chip 508**. Processor 502 is physically and electrically coupled to the board 530. In some embodiments, **the at least one communication chip is also**

physically and electrically coupled to the board 530.”) (Ex. 1005, 24 (emphasis added); Ex. 1002, ¶100.)

21. Claim 21

**“The computing device of claim 18, further comprising:
a camera coupled to the board.”**

Boyanov ’569 discloses this feature. (Ex. 1002, ¶101.) For example, Boyanov ’569 discloses that the computing device of figure 5 includes a camera coupled to the board. (Ex. 1005, 24 (“Computing device 500 can include other components that may or may not be physically and electrically coupled to board 530 depending on its application. These other components include, ... cameras”); Ex. 1002, ¶101.)

22. Claim 22

**“The computing device of claim 18, further comprising:
a battery coupled to the board.”**

Boyanov ’569 discloses this feature. (Ex. 1002, ¶102.) For example, Boyanov ’569 discloses that the computing device of figure 5 includes a battery coupled to the board. (Ex. 1005, 24 (“Computing device 500 can include other components that may or may not be physically and electrically coupled to board 530 depending on its application. These other components include, ... batteries”); Ex. 1002, ¶102.)

23. Claim 23

**“The computing device of claim 18, further comprising:
an antenna coupled to the board.”**

Boyanov '569 discloses this feature. (Ex. 1002, ¶103.) For example, Boyanov '569 discloses that the computing device of figure 5 includes an antenna coupled to the board. (Ex. 1005, 24 (“Computing device 500 can include other components that may or may not be physically and electrically coupled to board 530 depending on its application. These other components include, ... antennas”); Ex. 1002, ¶103.)

24. Claim 24

**“The computing device of claim 18, wherein the component
is a packaged integrated circuit die.”**

Boyanov '569 discloses this feature. (Ex. 1002, ¶104.) For example, Boyanov '569 discloses that the computing device of figure 5 includes components including a processor 502 and a communication chip 508, each of which is further disclosed to include a packaged integrated circuit die. (Ex. 1005, 25 (“Processor 502 of computing device 500 includes an integrated circuit die packaged within processor 502.”), 26 (“The communication chip 508 also includes an integrated circuit die that is packaged within the communication chip 508.”); Ex. 1002, ¶104.)

25. Claim 25

“The computing device of claim 18, wherein the component is selected from a group consisting of a processor, a communications chip, and a digital signal processor.”

Boyanov '569 discloses this feature. (Ex. 1002, ¶105.) For example, Boyanov '569 discloses that the computing device of figure 5 includes components including a processor 502, a communication chip 508, and a digital signal processor:

In an alternative embodiment, FIG. 5 illustrates a computing device 500. The computing device 500 is provided with a board 530. The **board can include some components including, but not limited to, a processor 502 and at least one communication chip 508.** Processor 502 is physically and electrically coupled to the board 530. In some embodiments, the at least one communication chip is also physically and electrically coupled to the board 530. In a further embodiment, the communication chip 508 is integrated within the processor 502.

Computing device 500 can include other components that may or may not be physically and **electrically coupled to board 530** depending on its application. These **other components include**, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, graphics processors, **digital signal processors**, cryptographic processors,

chipsets , antennas, displays, touch screen controllers, batteries, audio codec, video codec, power amplifiers, Global Positioning System (GPS) devices, compasses, accelerometers, gyroscopes, speakers, cameras, and a large number of storage devices (such as hard disk drives, solid state drives, CD players, and Digital Versatile Disk (DVD) players).

(Ex. 1005, 24 (emphasis added); Ex. 1002, ¶105.)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. The Board Should Not Deny Institution Under *Fintiv*

The merits of Petitioner’s arguments are compelling and the evidence in support is substantial. That “alone demonstrates that the PTAB should not discretionarily deny institution under *Fintiv*.” (Ex. 1012 at 4-5.) But in any event, the six *Fintiv* factors do not justify denying institution.

The **first factor** is neutral because Samsung has not yet moved to stay the district court proceeding. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

The **second factor** weighs against denial. Jury selection is scheduled for May 20, 2024. (Ex. 1013, 1.) However, the median time from the filing of a civil case to trial in the Eastern District of Texas is 24.5 months (Ex. 1014, 37), placing the

expected trial date in the parallel litigation around late September 2024. *See* Ex. 1012 at 8-9 (instructing Board to consider median time-to-trial statistics). Therefore, trial is expected to occur after the FWD in this IPR, which is expected around August 2024. And even if trial proceeds in May 2024, the above timing does not tip in favor of denying the petition in this case. *See also, e.g., Apple Inc. v. Aire Tech. Ltd., IPR2022-01135, Paper 11 at 5-6 (PTAB Jan. 4, 2023).*

The **third factor** weighs strongly against denial. The district court case is in its infancy, and the Parties' have made little investment to date. PO filed its complaint on September 12, 2022, served its initial infringement contentions on November 17, 2022, and just filed an amended complaint on January 24, 2023. Petitioner's diligence in pursuing this petition less than five months after PO's Complaint and shortly after receiving the infringement contentions weighs in favor of institution. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (PTAB April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions).

The **fourth factor** weighs against denial because this Petition challenges claims 3-17, which are not asserted against Petitioner in district court. This IPR petition is thus the only venue in which certain invalidity challenges will be adjudicated, which promotes system efficiency. *See Fintiv*, Paper 11 at 4.

Accordingly, this factor weighs against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14-15 (PTAB April 19, 2021).

Regarding the **fifth factor**, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (April 14, 2021).

The **sixth factor** (other circumstances) weighs heavily against denial given that the disclosure of Boyanov '569 is nearly identical to that of the '183 patent. *See Align Technology, Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan 20, 2021); *see also* Section IX. There is also a significant public interest against “leaving bad patents enforceable,” and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

B. The Board Should Institute This Petition

Petitioner is filing an additional IPR petition challenging the claims of the '183 patent concurrently with the filing of this petition. The other petition does not rely on breaking the priority chain of the '183 patent, relies on prior art references not discussed in the present petition, and is being filed out of an abundance of caution because of the statutory estoppel provisions.

The unpatentability ground presented in this petition differs substantially from those raised in the concurrently filed petition. Accordingly, the Board should

institute review based on the substantially different ground presented in this petition. Indeed, institution of both petitions is particularly justified given that the Board generally discourages follow-on petitions. *See General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper No. 19 at 9 (Sept. 6, 2017). Finally, Petitioner has narrowed the grounds presented in each of the petitions to achieve the goal of “just, speedy, and inexpensive resolution” consistent with 37 C.F.R. § 42.1(b).

XI. CONCLUSION

For the foregoing reasons, Petitioner requests IPR and cancellation of claims 1-25 of the '183 patent.

Respectfully submitted,

Dated: February 3, 2023

By: / Naveen Modi /
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,727,183 contains, as measured by the word processing system used to prepare this paper, 12,085 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: February 3, 2023

By: / Naveen Modi /
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on February 3, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,727,183 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record:

KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

Respectfully submitted,

Dated: February 3, 2023

By: / Naveen Modi /
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner