

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DAEDALUS PRIME LLC
Patent Owner

Patent No. 10,727,183

**DECLARATION OF DR. STANLEY SHANFIELD IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,727,183**

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I, Stanley Shanfield, declare as follows:

I. INTRODUCTION

1. I have been retained by Samsung Electronics Co., Ltd. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 10,727,183 (“the ’183 patent”) (Ex. 1001).¹ I have been asked to consider whether certain references discloses or suggests the features recited in claims 1-25 of the ’183 patent. My opinions are set forth below.

2. I am being compensated at a rate of \$385/hour for my work in this proceeding. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND QUALIFICATIONS

3. I am an independent consultant. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing,

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’183 patent.

developing, and fabricating integrated circuits, including interconnect structures used in such integrated circuits.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. A copy of my current curriculum vitae, which details my education and professional and academic experience, is attached as an addendum with this declaration. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

5. I received a B.S. in Physics from the University of California, Irvine in 1977. I received the University of California Regents Award for Outstanding Research Project for my experimental and theoretical work on rotating relativistic electron beams. Under full ERDA (DOE) scholarship, I received a Ph.D. in Physics from the Massachusetts Institute of Technology in 1981.

6. After receiving my doctorate degree, I worked at Spire Corporation in Bedford, Massachusetts from 1981-1984, where I served as a Staff Scientist, and later, a Senior Staff Scientist. At Spire, I developed new methods for low temperature deposition of plasma-assisted CVD epitaxial silicon. In addition, I built, operated, and characterized an ion-assisted deposition system for making coating for semiconductor and machine tool industries.

7. From 1985-1999, I worked at Raytheon Corporation. As staff and later as section manager, I developed reactive ion etching (RIE) processes for patterning dielectrics (silicon dioxide, silicon nitride, silicon oxynitride, etc.), conductive layers (aluminum-copper, copper-silicon, W-silicide, TaN, doped polysilicon, etc.) and organic layers (photoresist, polyimide, etc.). For example, I developed a low damage, high selectivity process as part of the FET gate formation step. I was responsible for purchasing equipment and developing processes for several plasma systems typical of those used in the semiconductor industry, including load-locked RIE, microwave ECR RIE, barrel etchers, single-wafer elevated temperature RIE systems, etc.

8. In 1996, I became the Manager of Semiconductor Operations at Raytheon. As Manager, I built and led a 300 employee, \$60 million revenue-generating semiconductor development, commercial system design, and electronic module manufacturing operation. I worked directly with engineers in the selection, installation and optimization of several chemo-mechanical polishing systems (CMP), including analysis of operational maintenance and performance monitoring. The manufacturing facility eventually used multiple production CMP systems, and I directly participated in establishing the required metrology (optical thickness monitoring) for maintaining polishing uniformity standards.

9. From 1999-2001, I worked at AXSUN Technologies as part of the founding team, first as the Director of Manufacturing & Wafer Fab Technology, and later, as the Vice President of Operations. As Director of Manufacturing & Wafer Fab Technology, I led device and module manufacturing, creating a wafer fab and circuit board assembly infrastructure; my responsibilities included hiring over 70 individuals and leading production design efforts. In my role as Vice President of Operations, I designed, fabricated, and productized AXSUN's microelectromechanical (MEM) Fabry-Perot optical filter, and I managed a new generation of electronics module design. In addition, I established a process and fabrication facility in Belfast, Northern Ireland for producing thick oxide silicon-on-insulator devices. As a result of my work at AXSUN, I was awarded patents on semiconductor processing and control electronics.

10. I have served since 2003 at the Charles Stark Draper Laboratory ("Draper Laboratory") in Cambridge, Massachusetts, ultimately becoming a Distinguished Member of Technical Staff and Technical Director in Advanced Hardware Development. I led the Advanced Hardware Development Division (approximately 80 staff) in their work on the laboratory's multi-chip integrated circuit module facility. The laboratory has acquired several semiconductor-grade CMP systems for the purpose of fabricating multi-chip modules and for planarization

operations in MEMS devices, and I have been involved in their operation and optimization.

11. I have authored more than 25 journal and conference papers. My publications include numerous papers on topics relating to semiconductor processing, advanced semiconductor devices, electronic circuit design and packaging. I have been invited to give professional talks at various conferences. I am also a co-inventor of several U.S. Patents.

12. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

13. The opinions in this Declaration are based on the documents I reviewed, my knowledge and experience, and professional judgment. In forming my opinions expressed in this Declaration, I have reviewed the following materials: U.S. Patent No. 10,727,183 (Ex. 1001); the prosecution history of U.S. Patent No. 10,727,183 (Ex. 1004); U.S. Patent Publication No. 2005/0282378 to Fukunaga *et al.* (“Fukunaga”) (Ex. 1005); U.S. Patent Publication No. 2006/0128144 to Park *et al.* (“Park”) (Ex. 1006); U.S. Patent Publication No. 2006/0115976 to Chan *et al.* (“Chan”) (Ex. 1007); U.S. Patent Publication No. 2010/0308408 to Song *et al.* (“Song”) (Ex. 1008); U.S. Patent No. 7,863,744 to Kawahara *et al.* (“Kawahara”)

(Ex. 1009); U.S. Patent Publication No. 2003/0064154 to Laxman *et al.* (“Laxman”) (Ex. 1010); U.S. Patent Publication No. 2009/0039512 to Yang *et al.* (“Yang”) (Ex. 1011); U.S. Patent Publication No. 2007/0049008 to Martin *et al.* (“Martin”) (Ex. 1012); U.S. Patent Publication No. 2008/0265416 to Lee *et al.* (“Lee”) (Ex. 1014); , U.S. Patent Publication No. 2009/0152723 to Ou *et al.* (“Ou”) (Ex. 1015); U.S. Patent No. 6,677,253 to Andideh *et al.* (“Andideh”) (Ex. 1016); and any other materials I refer to in this declaration in support of my opinions.

14. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '183 patent at the time of the alleged invention, which I have been asked to initially consider as the early 2010s (including November 4, 2011, the filing date of the '453 PCT application, which I understand is the earliest possible priority date for the '183 patent). My opinions reflect how one of ordinary skill in the art would have understood the '183 patent, the prior art to the patent, and the state of the art at the time of the alleged invention. Notably, even if a later date is assumed as the time of the alleged invention, (e.g. the September, 3, 2019, filing date of the '086 application), my opinions presented in this declaration remain unchanged.

15. Based on my experience and expertise, it is my opinion that certain prior art references disclose or suggest all the features recited in claims 1-25 of the '183 patent, as I discuss in detail below.

IV. LEVEL OF ORDINARY SKILL IN THE ART

16. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the '183 patent as of what I understand is the earliest possible priority date of November 4, 2011, which is the filing date of the '453 PCT application to which the '183 patent claims priority. Specifically, based on my review of the '183 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in the art would have had would have had a bachelor's degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and to become familiar with the prior and current solutions to those problems.

17. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe (early 2010s timeframe). My opinions are the same if a later date of invention is assumed for the '183 patent. For example, my opinions are the same if the alleged date of invention is the September 3, 2019 filing date of '086 application.

V. TECHNICAL BACKGROUND

18. In this section, I present a brief overview of certain aspects of interconnect used in integrated circuits and the manufacture of such interconnect at the time of the alleged invention that will assist in better understanding the '183 patent and the prior art that I discuss in this declaration. The interconnect in such integrated circuits provides the electrical connections between the circuit elements (e.g. transistors, vias, etc.), where, as the density of such components and the speed of operation of such integrated circuits has increased, the structure of such interconnect has evolved to ensure reliable operation of such complex devices at high speed.

A. Interconnect Embedded in Dielectric Layers

19. The various circuit elements (e.g. transistors, logic gates, etc.) on integrated circuit devices are interconnected by metal traces that are formed in different layers on the integrated circuit device. As integrated circuits have become more complex, more layers of metal interconnect are included to provide the needed

connections. For example, as shown in figure 11-30 below, the left image includes three levels of metal interconnect, whereas the image on the right has five.

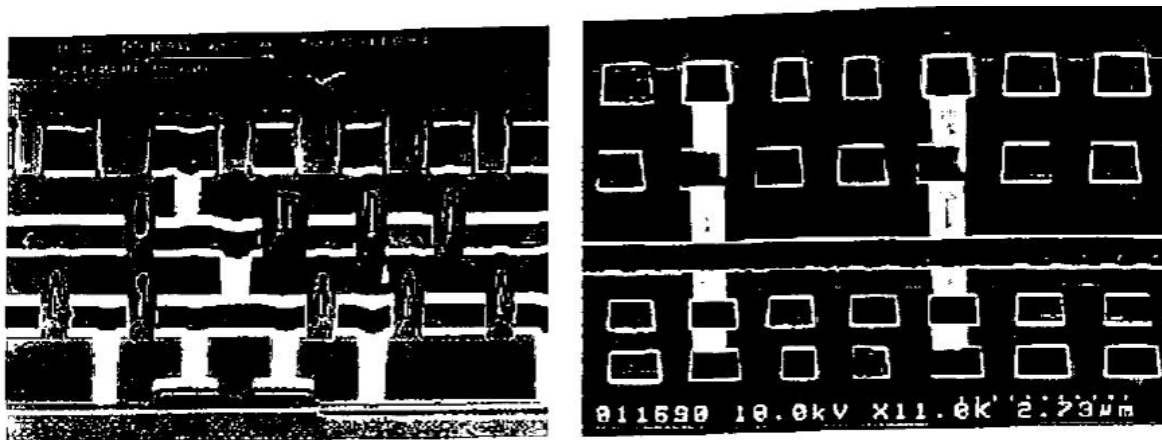


Figure 11-30 Two current back-end structures from VLSI Technology, Inc. The one on the left has three metal levels and uses encapsulated BPSG for the first-level dielectric, and SOG (encapsulated top and bottom with PECVD oxide) and CMP in the intermetal dielectrics. The multilayer metal layers and W plugs are also clearly seen. The SOG regions were deformed during SEM cleaving and erroneously look voidlike. The structure on the right, with five metal levels, uses HDP oxide (with PECVD oxide cap) and CMP in the intermetal dielectrics. Photos courtesy of VLSI Technology, Inc.

(Ex. 1014, 716².)

20. Rather than depositing, patterning, and etching metal layers to create such interconnect, the “damascene” method can be used to form such interconnect. The name “damascene” is derived from the ancient practice of inlaying metal in wood or ceramics for decoration. (*Id.*, 704.) In a damascene process, a blanket

² Citations are to the page numbers of “Silicon VLSI Technology, Fundamentals, Practice, and Modeling” that are on the top of each page.

deposition of metal is used to fill holes corresponding to interconnect layers or vias in a dielectric layer, and then an etchback is done to remove the metal not in the holes. (*Id.*; see also *id.*, 87) While aluminum had been a common metal used for interconnect, copper replaced aluminum in many devices because copper provides lower resistance, which helps reduce interconnect delay, and has much better electromigration resistance than aluminum. (*Id.*, 779.) A basic damascene process involving the formation of a tungsten (W) plug for a contact or via is shown below in figure 11-19.

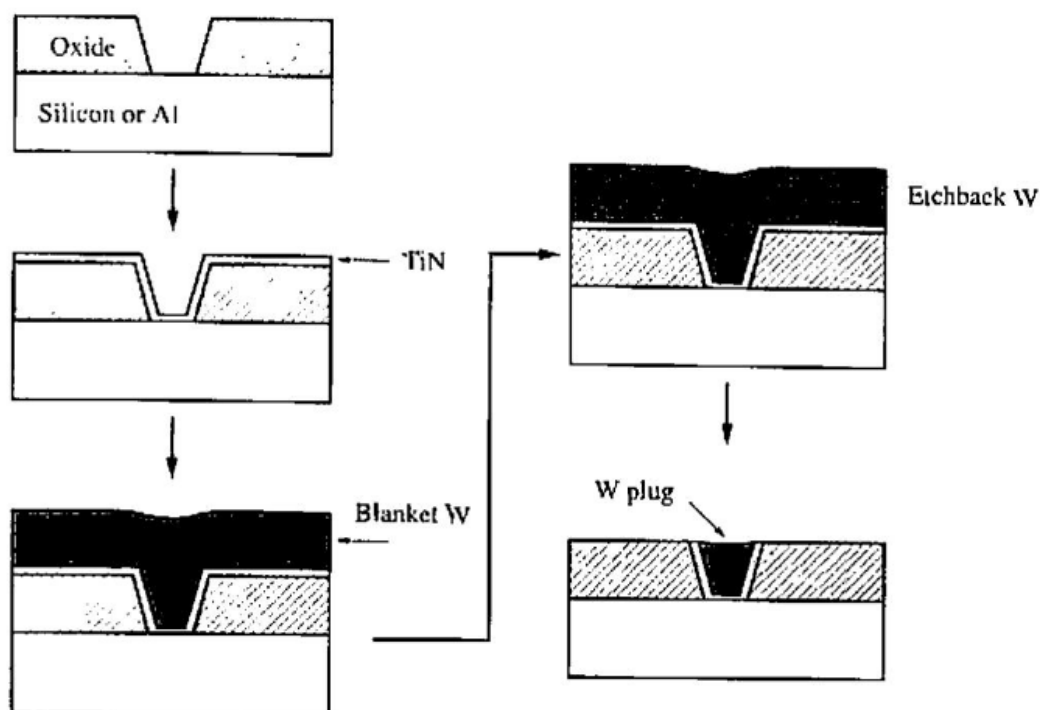


Figure 11-19 Schematic illustration of process to fabricate a W plug for a contact or via. TiN (or a Ti/TiN bilayer) is utilized as an adhesion and barrier layer. An etchback step is done to planarize the W and leave it only in the contact or via hole.

(*Id.*, 705.)

21. The damascene process is especially applicable for copper interconnects. (*Id.*, 570, 724.) As noted above, the damascene process can be used for vias, interconnect, or both. A more advanced version of the damascene process provides both the via and interconnect levels simultaneously. (*Id.*) The steps of forming the interconnect, dielectric layers, and vias that connect the different layers of interconnect are repeated until the required number of metal layers are fabricated. (*Id.*, 725.) After a final layer of passivation is added, packaging of the integrated circuit device finishes the manufacturing process. (*Id.*)

B. Low-K Dielectrics

22. Dielectrics are used to separate and electrically isolate different conducting layers of the integrated circuit from each other. (Ex. 1014, 707.) The dielectric material used for such interlayer dielectrics in integrated circuit devices can impact the interconnect delay for signals propagating on the interconnect lines in such devices. Silicon oxide (SiO_2) was commonly used as an interlayer dielectric material, but it was understood that replacing SiO_2 with lower dielectric constant (“low-k”) materials would “decrease the interconnect delay by decreasing both the line-to-substrate and line-to-line capacitances.” (*Id.*, 779.) It was also recognized that “[d]ecreasing the capacitance also minimizes interconnect cross talk.” (*Id.*) While improving interconnect delay, such low-k dielectrics may not have the same

thermal and mechanical stability of SiO₂. For example, some low-k dielectrics were known to crack easily when subjected to mechanical stress. (*Id.*)

C. Chemical Mechanical Polishing

23. Chemical mechanical polishing (CMP) is used during fabrication of integrated circuits to planarize the surface of a substrate by removing material. (Ex. 1014, 713.) “As its name implies, CMP is a combination of chemical and mechanical polishing or etching.” (*Id.*) Wafers are held face down against a spinning polishing pad and a slurry is kept between the pad and the wafer, where different slurries are used to polish different materials. (*Id.*) Figure 11-27 below shows a cross section of a CMP pad in contact with a top of a wafer.

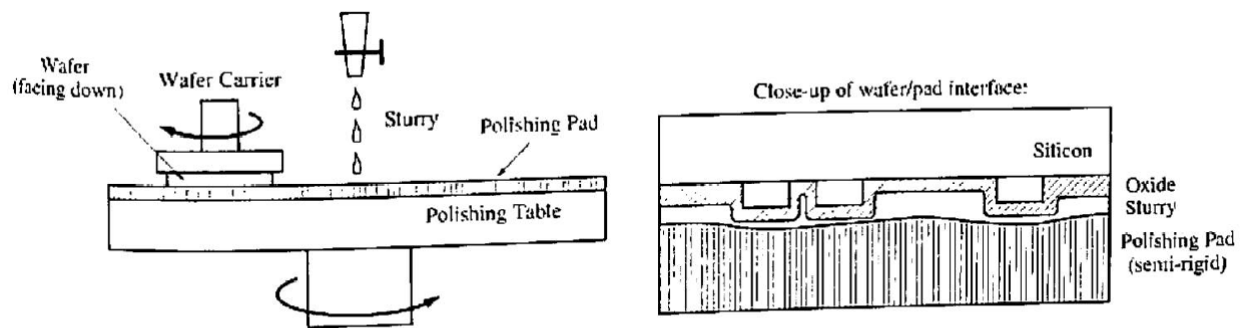


Figure 11-27 Illustration of Chemical-Mechanical Polishing (CMP) system. The right hand figure shows a close-up of wafer/pad interface.

24. CMP is commonly used to remove excess metal deposited as a part of the damascene process. (*Id.*, 87, 570.)

D. Wet Etching

25. Etching can be done in either a wet or dry environment, where wet etching involves the use of liquid etchants such as acids. (Ex. 1014, 609, 612.) In

wet etching the wafer can be immersed in an etchant solution, where the exposed material is removed mostly by chemical processes. (*Id.*) In contrast, dry etching involves the use of gas-phase etchants in a plasma and usually takes place by a combination of chemical and physical processes. (*Id.*)

26. Different materials can be etched at different rates by controlling the selectivity of the etch, where etch selectivity is the ratio of the etch rates for different materials. (*Id.*) “Different materials have different etch rates usually because of the chemical effects involved with etching, as opposed to the physical effects.” (*Id.*, 610.) Chemical reactions can be very selective, whereas physical processes tend to be similar for most materials. (*Id.*)

VI. OVERVIEW OF THE '183 PATENT

27. The '183 patent is entitled “Methods and Apparatuses to Form Self-Aligned Caps.” (Ex. 1001, Title.) The '183 patent discloses formation of conductive lines in a dielectric layer over a substrate, where the conductive lines are recessed in order to allow a capping layer to be formed on each of the conductive lines. (*Id.*, Abstract.) The '183 patent discloses that prior art interconnect structures formed the capping layers over conductive lines that were not recessed, and instead, had an upper surface co-planar with the dielectric layer in which the conductive lines are contained. (*Id.*, 1:43-46 (“The electromigration caps, for example, caps 111-113, can be grown on the respective interconnect lines above a flat surface of the substrate

using electroless plating.”) As shown in annotated figure 1A below, because the growth of the caps is isotropic, the caps grow horizontally and vertically such that they extend beyond the conductive lines onto the surface of the substrate. (*Id.*, 1:46-53.) As a result, the line-to-line spacing is reduced from the spacing 105 between the conductive lines to the spacing 107 between the overhanging caps. (*Id.*, 1:53-55.)

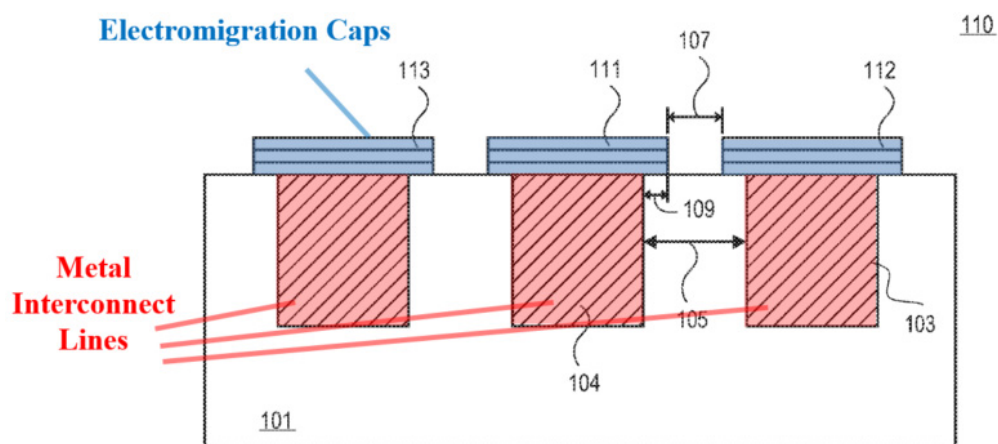


FIG. 1A
(PRIOR ART)

(*Id.*, FIG. 1A (annotated).)

28. According to the '183 patent, the overhang 109 of the caps is about 50% of the cap thickness. (*Id.*, 1:56-57.) Figure 1B of the '183 patent illustrates a top view of an interconnect structure and shows how the lateral growth of the caps above the substrate increases the line edge roughness (“LER”) and reduces line-to-line

spacing 125. (*Id.*, 1:61-2:2.) The '183 patent further discloses that “[b]oth the increased LER and reduced line-to-line spacing negatively impact on the reliability of the interconnect structures, increase the risk of current shorting that may lead to the failure of the entire integrated circuit device.” (*Id.*, 2:3-6.)

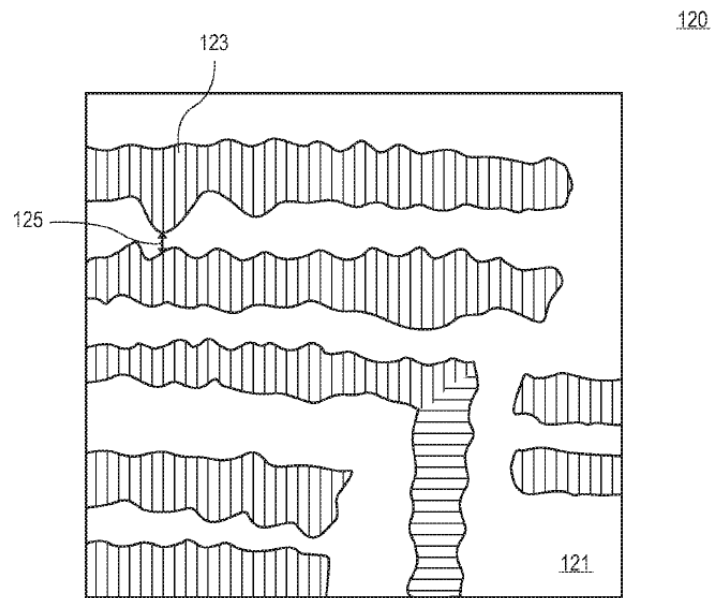


FIG. 1B
(PRIOR ART)

(*Id.*, FIG. 1B.)

29. In an attempt to address these problems, the '183 patent discloses “[m]ethods and apparatuses to control a line edge roughness (‘LER’) and line-to-line spacing in deposition of self-aligned metal caps.” (*Id.*, 3:46-48.) The '183 patent discloses the steps for forming such an interconnect structure in conjunction

with figures 2A-2H. (*Id.*, 2:19-47, FIGs. 2A-2H.) Figure 2B shows the dielectric layer 203 formed over the substrate 201. (*Id.*, 4:27-29.)

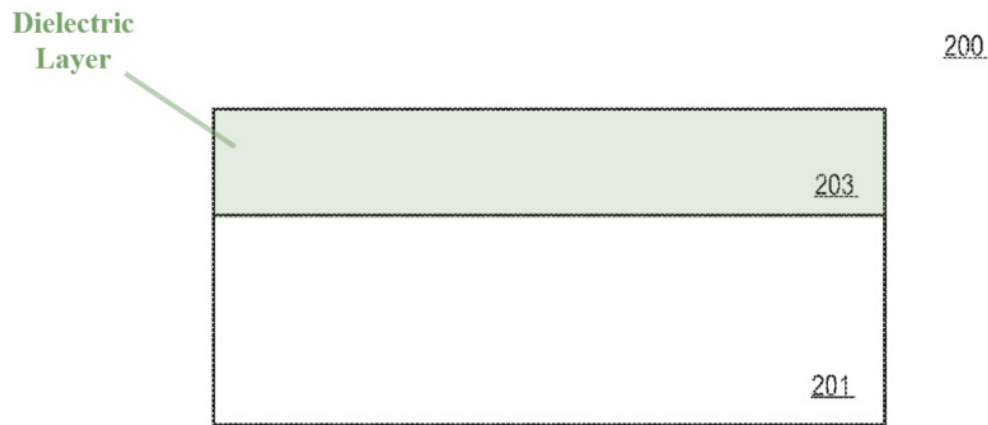


FIG. 2B

(*Id.*, FIG. 2B (annotated).)

30. Figure 2D shows openings (“trenches”) 206 formed in the dielectric layer. (Ex. 1001, 5:6-8.)

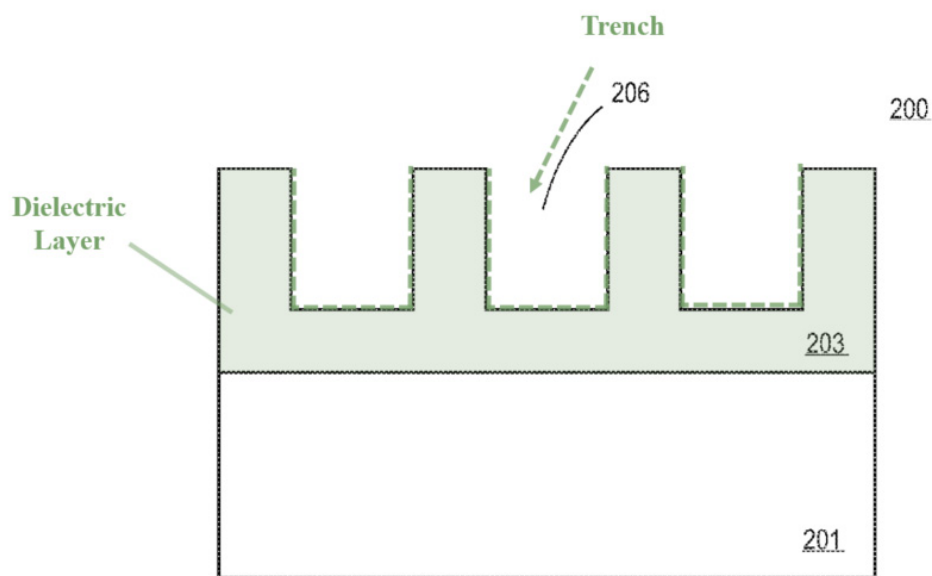


FIG. 2D

(*Id.*, FIG. 2D (annotated).)

31. The '183 patent discloses that a base layer that includes a barrier layer (not shown) can be formed on the inner sidewalls and bottom of the trenches. (Ex. 1001, 5:39-48.) Figure 2E shows a conductive layer 205 deposited over the dielectric layer 203, where the conductive layer 205 fills the opening with conductive material to form conductive lines. (*Id.*, 5:34-39.)

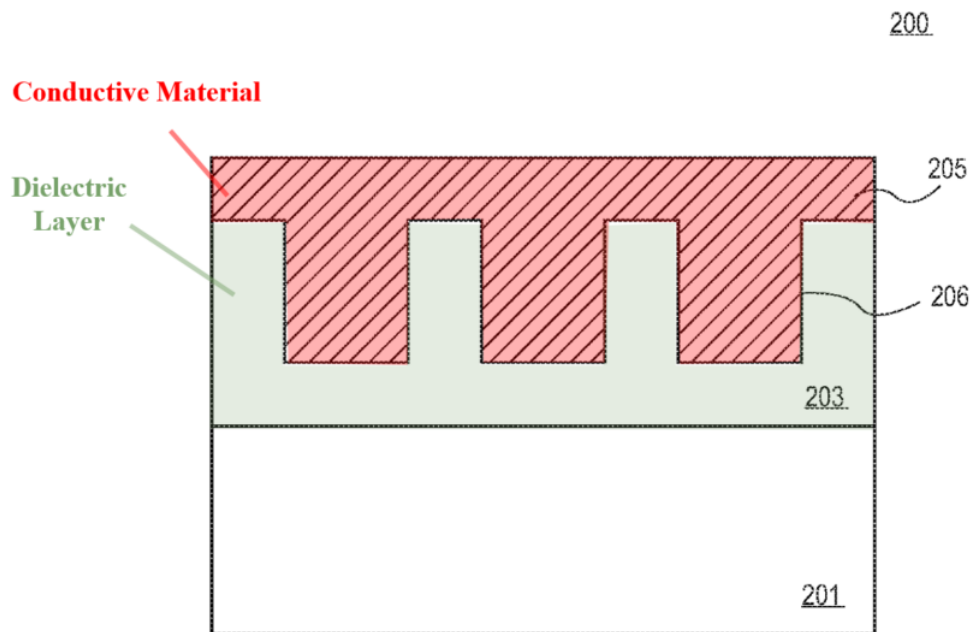


FIG. 2E

(*Id.*, FIG. 2E (annotated).)

32. Following deposition of the conductive material in the openings, portions of the conductive layer 205 are removed from the top surface of the dielectric layer outside the opening to form conductive lines 208 shown in figure 2F.

(*Id.*, 6:29-33.)

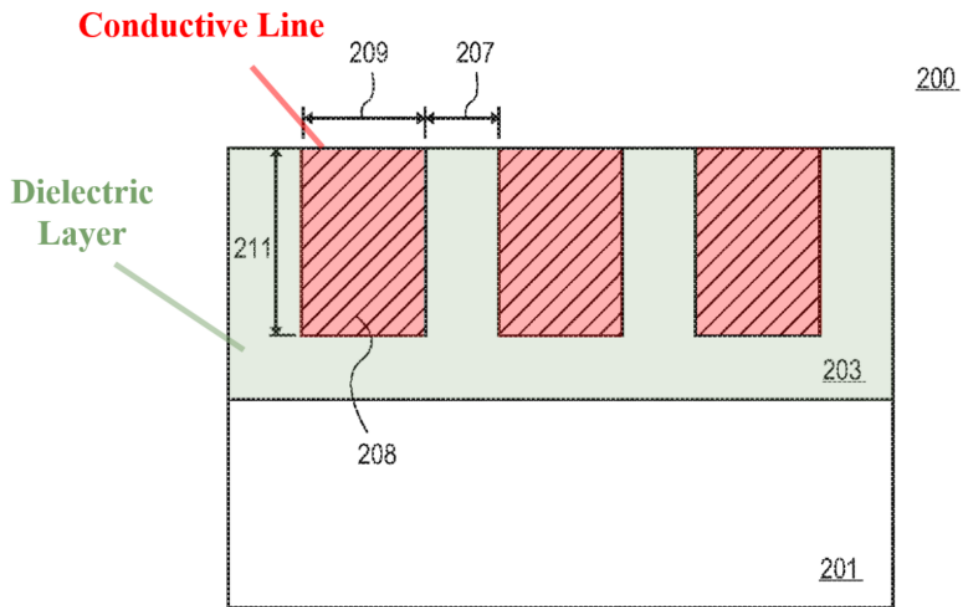


FIG. 2F

(*Id.*, FIG. 2F (annotated).)

33. As shown in figure 2G, following removal of the conductive material from the top surface of the dielectric layer, the conductive lines are recessed to form channels 212. (*Id.*, 6:56-64.)

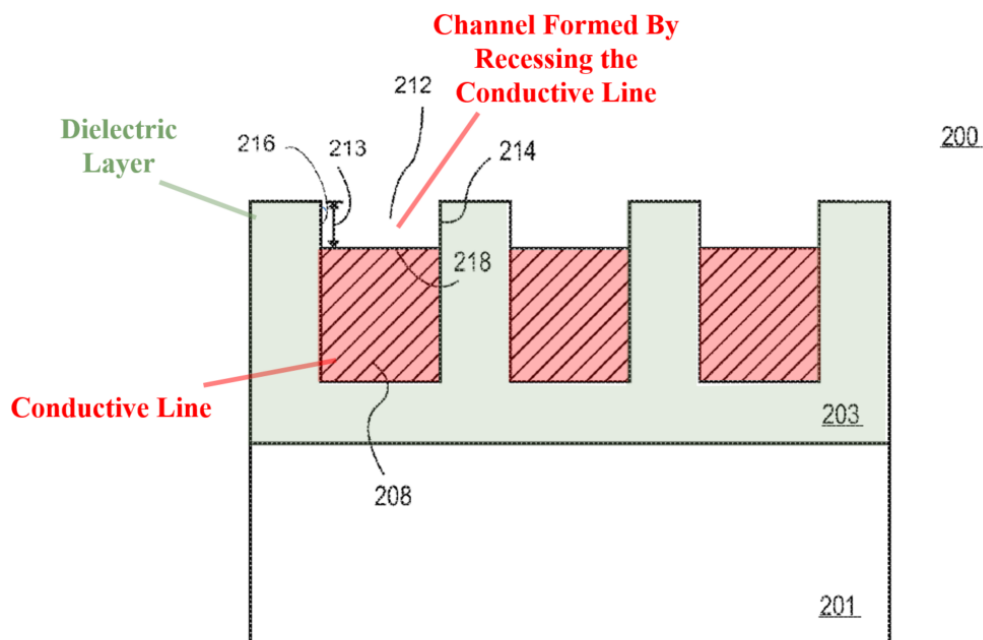


FIG. 2G

(*Id.*, FIG. 2G (annotated).)

34. Figure 2H shows the interconnect structure following deposition of the capping layers 215, where the capping layers 215 are deposited on the recessed conductive lines 208 within channels 212. (*Id.*, 9:6-27.) The '183 patent further discloses that the conductive material for the conductive lines can be copper or aluminum, whereas the capping layer can include cobalt alloys, nickel alloys, platinum group metals or alloys, or refractory metals. (*Id.*, 9:34-48.)

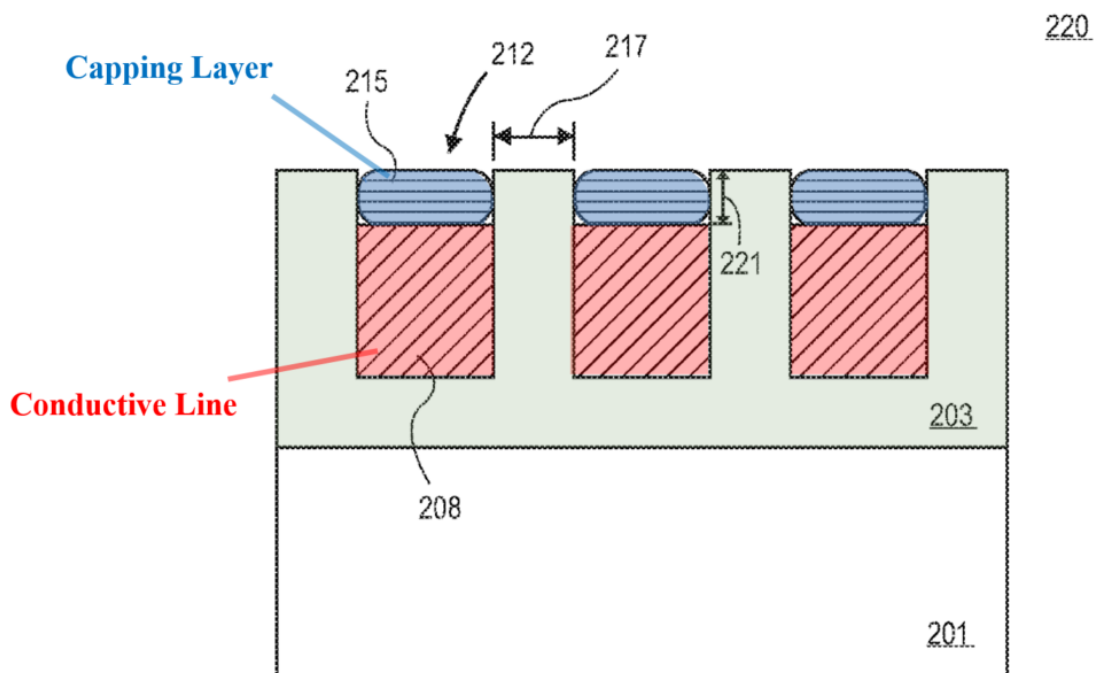


FIG. 2H

(*Id.*, FIG. 2H (annotated).)

VII. CLAIM CONSTRUCTION

35. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is the early 2010s (including November 4, 2011). In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

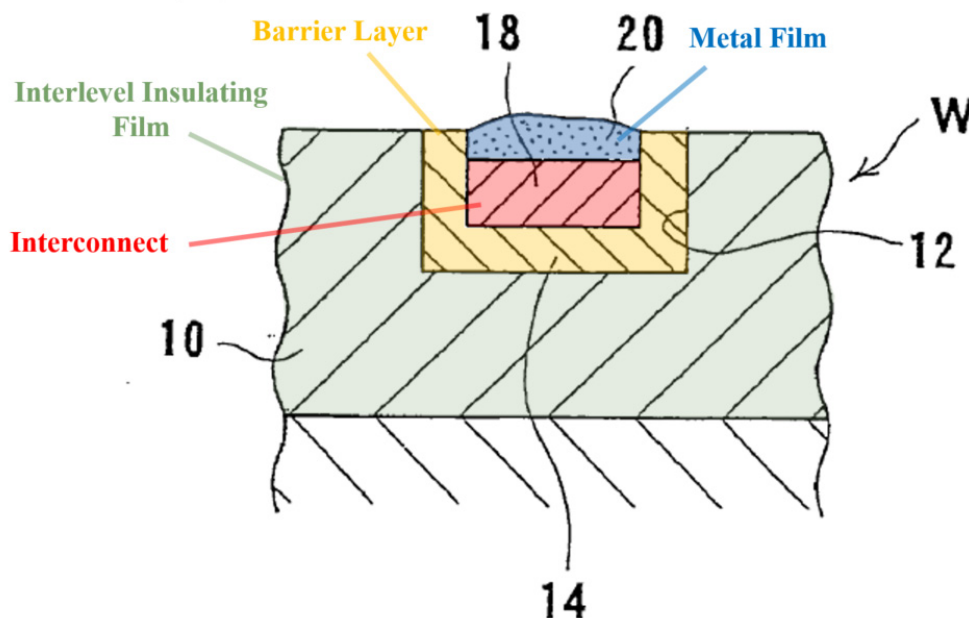
VIII. OVERVIEW OF THE PRIOR ART

A. Fukunaga

36. Fukunaga is entitled “Interconnects Forming Method and Interconnects Forming Apparatus” (Ex. 1005, Title) and discloses “[a]n interconnects forming method and an interconnects forming apparatus are useful for embedding a conductive material (interconnect material), such as copper or silver, into interconnect recesses provided in a surface of a substrate, such as a semiconductor wafer, to thereby form embedded interconnects, and selectively covering the surfaces of embedded interconnects with a metal film (protective film) to provide a multi-level structure” (*id.*, Abstract.).

37. As shown in annotated figure 4C below, Fukunaga discloses an interconnect structure that includes an insulating layer 10 that can be formed of a low-k dielectric material. (*Id.*, ¶[0048] (“an insulating film (interlevel insulating film) 10 of, for example, SiO₂ or a low-k material deposited on a substrate W”), ¶¶[0060], [0075].) A barrier layer 14, which can be Ta or TaN, is formed in recesses (e.g. trenches 12) of the insulating film, where interconnect 18 and metal film 20 are formed within the recesses after the barrier layer such that the barrier layer 14 partially surrounds them. (*Id.*, ¶¶[0013], [0048], [0061].)

FIG. 4C



(*Id.*, FIG. 4C (annotated).)

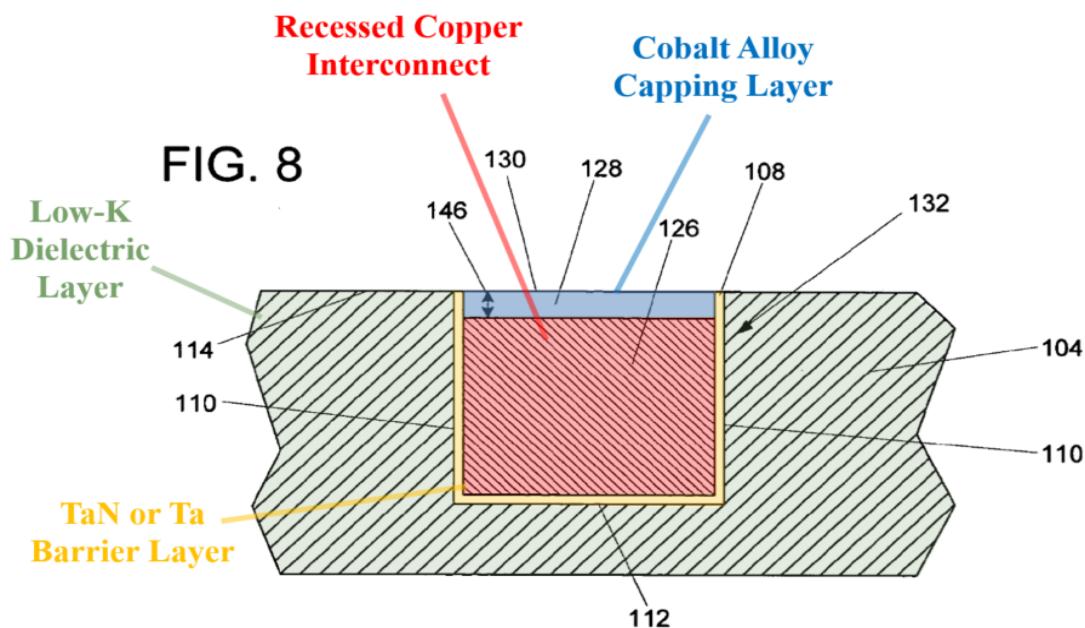
38. Fukunaga further discloses that the interconnect 18 is formed of copper and recessed below the surface of the insulating film. (*Id.*, ¶[0060] (“forming interconnects 18 with the copper 16 embedded in the trenches (interconnect recesses) 12 ... polishing or etching of interconnects 18 is further continued so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.”).) Fukunaga also discloses that the metal film 20, which is a protective “cap” layer (*id.*, [0005]), is formed of cobalt or a cobalt alloy. (*Id.*, ¶[0062] (“Using the barrier layer 14 thus left as a mask, a metal film (protective film) 20 of, for example, a cobalt alloy or a nickel alloy is formed selectively on the surfaces of interconnects 18 in the trenches 12, as shown in FIG.

4B, thereby covering the surfaces of interconnects 18 with the metal film 20 to protect interconnects 18.”.)

B. Park

39. Park is entitled “Interconnects Having a Recessed Capping Layer and Methods of Fabricating the Same.” (Ex. 1006, Title.) As shown in annotated figure 8 below, Park discloses a low-k dielectric layer 104 with an opening lined with barrier layer 108 (e.g. TaN), where a recessed conductive material 126 (e.g., copper) in the opening has an overlying cobalt alloy capping layer 128 that prevents electromigration of the copper interconnect. (*Id.*, ¶¶[0018]-[0019], [0023], [0024].)

40. Park discloses that the low-k dielectric layer 104 can be formed of carbon doped oxide. (*id.*, ¶[0018], ¶[0024]), whereas the capping layer 128 can be formed of cobalt alloys that include one or more of boron (B), phosphorus (P), and tungsten (W) (*id.*, ¶[0027]).



(*Id.*, FIG. 8 (annotated).)

41. Park further discloses that the interconnect structure shown in figure 8 above can be used in, for example, a cell phone or personal digital assistant (PDA) device 210 shown in figure 10 and a computer system 310 shown in figure 11. (*Id.*, ¶¶[0010]-[0011], [0028]-[0029], FIGs. 10, 11.) Park discloses that the PDA, cell phone, and computer system each include a central processing unit (CPU) that includes the interconnect structure like that shown above in figure 8. (*Id.*, ¶¶[0028]-[0029].)

FIG. 10

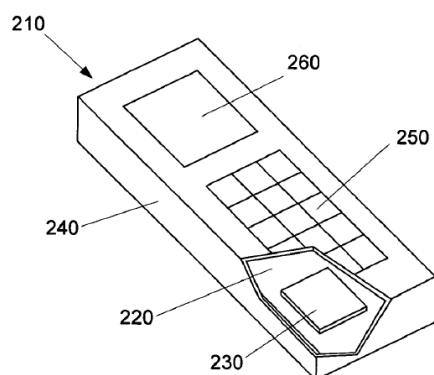
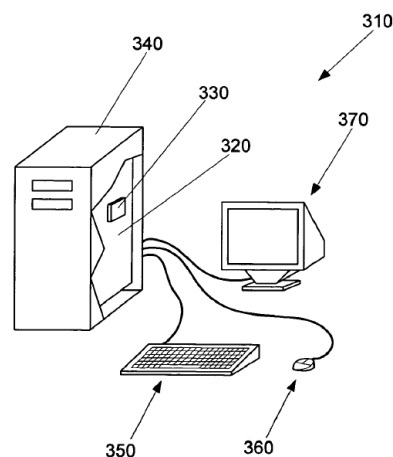


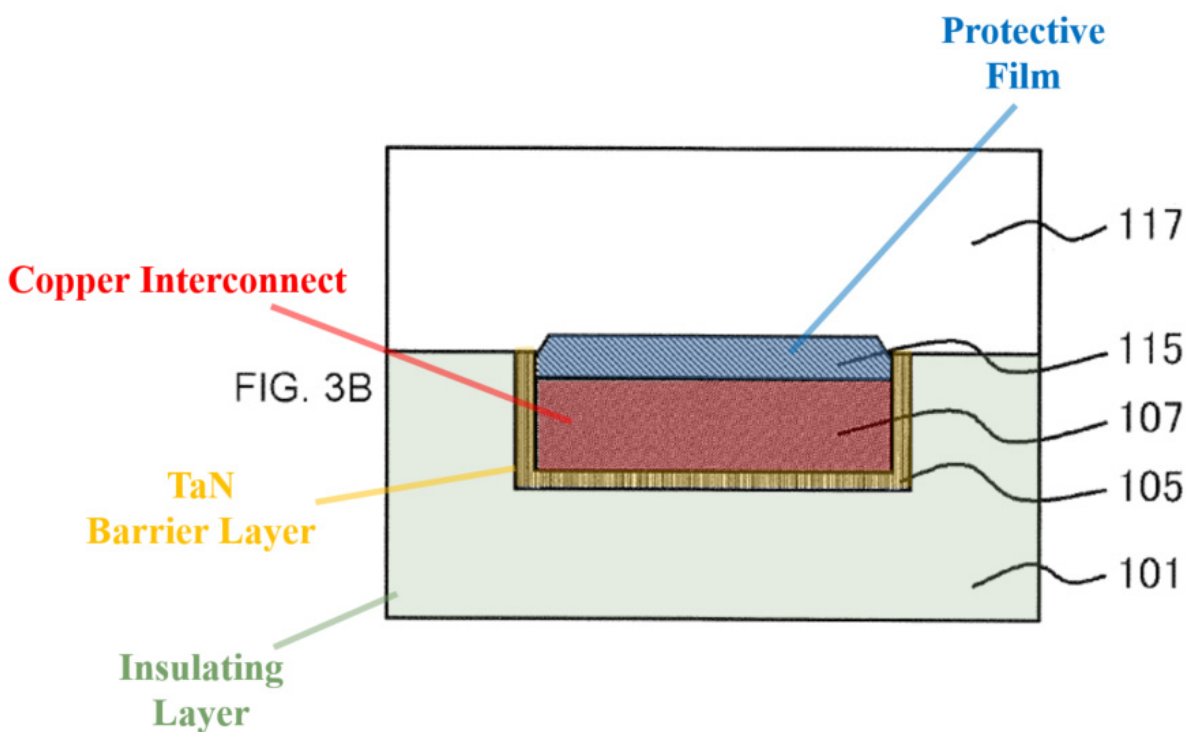
FIG. 11



(*Id.*, FIGs. 10, 11.)

C. Kawahara

42. Kawahara is entitled “Semiconductor Device and Method for Manufacturing Same” (Ex. 1009, Title) and discloses formation of an interconnect structure for semiconductor devices, which are formed on a silicon substrate and include devices such as transistors and via plugs formed on the substrate. (*Id.*, 3:1-3, 6:49-52, 9:32-33). As shown in annotated figure 3B below, Kawahara discloses that the interconnect structure includes an insulating layer 101, a tantalum nitride (TaN) barrier metal film 105, copper interconnect 107, and protective film 115.

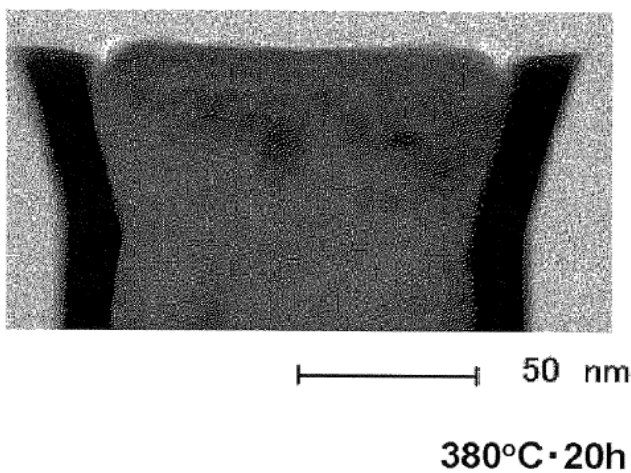


(*Id.*, FIG. 3B (annotated).)

43. Kawahara discloses forming the insulating interlayer 101 as a low dielectric constant insulating film of silicon oxycarbide (SiOC) film that includes silicon (Si), oxygen (O), and carbon (C). (*Id.*, 5:16-22.) Kawahara also discloses that the protective film includes cobalt and can including cobalt alloys that also include one or more of tungsten, phosphorus, and boron. (*Id.*, 5:50-53 (“The protective film 115 and the protective film 129 contain for example, one or more element selected from Co and Ni and one or more element selected from tungsten (W) and phosphorus (P) and boron (B) as constituent element”).)

44. Kawahara discloses that the copper interconnect 107 is recessed in order to allow the cap metal film to be formed on the surface of the interconnect 107 while not extending “from the top of the concave portion 103 beyond the region for forming the barrier metal film 105 considerably exceeding the top of the insulating film 101, or from being considerably swelled to form a mushroom-shape.” (*Id.*, 8:40-52; *see also id.*, 6:64-7:3.) Figure 6B below is a cross-sectional view of a semiconductor device that includes the interconnect structure disclosed by Kawahara. (*Id.*, 9:36-38.)

FIG. 6B



(*Id.*, FIG. 6B.)

IX. THE PRIOR ART DISCLOSES ALL OF THE FEATURES OF THE CHALLENGED CLAIMS

A. Fukunaga in Combination with Park Discloses or Suggests the Features of Claims 1-25

45. In my opinion, Fukunaga in combination with Park discloses or suggests all of the features of claims 1-25 of the '183 patent.

1. Claim 1

a) “An integrated circuit structure, comprising:”

46. I understand that “[a]n integrated circuit structure, comprising” is the preamble to claim 1 of the '183 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Fukunaga discloses this feature. Fukunaga discloses formation of an interconnect structure (“integrated circuit structure”) that can be used in, for example, multi-level interconnect structures overlying a semiconductor base on which semiconductor devices are formed (i.e., an integrated circuit). (Ex. 1005, Abstract, ¶[0002] (“The present invention relates to an interconnects forming method and an interconnects forming apparatus, and more particularly to an interconnects forming method and an interconnects forming apparatus which are useful for embedding a conductive material (interconnect material), such as copper or silver, into interconnect recesses provided in a surface of a substrate, such as a semiconductor wafer, to thereby form embedded interconnects, and selectively covering surfaces of the embedded

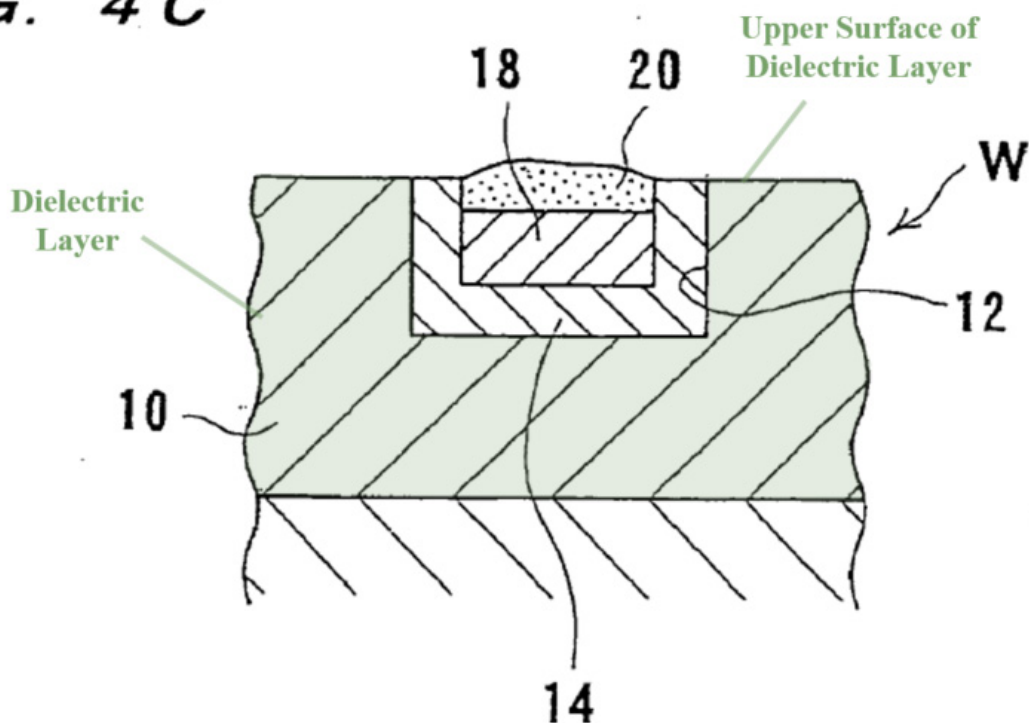
interconnects with a metal film (protective film) to provide a multi-level structure.”), ¶[0005] (“a semiconductor device having a multi-level interconnect structure”), ¶[0007] (“forming copper interconnects in a semiconductor device”), (“a conductive layer 1a formed on a semiconductor base 1 having formed semiconductor devices”), ¶[0074] (“semiconductor wafers”); *see also* my analysis and citations below for the remaining limitations of this claim.)

b) “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen and carbon;”

47. In my opinion, Fukunaga in combination with Park discloses or suggests this claim feature. As shown in annotated figure 4C below, Fukunaga discloses an interconnect structure that includes an insulating layer (“dielectric layer”) that has an upper surface. (Ex. 1005, ¶[0048] (“Figure 2 schematically shows a substrate useable in an interconnects forming method of the present invention. As shown in FIG. 2, trenches 12 as interconnect recesses are formed, for example, by the lithography/etching technique, in an **insulating film (interlevel insulating film) 10 of, for example, SiO₂ or a low-k material** deposited on a substrate W”), ¶[0075] (“A process of forming interconnects on a substrate W, as shown in FIG. 2, by this interconnects forming apparatus will now be described by referring to FIGS. 3A through 3C.”), ¶[0060] (“FIGS. 4A through 4C illustrate, in a sequence of

process steps, an interconnects forming method according to another embodiment of the present invention.”.)

FIG. 4C



(*Id.*, FIG. 4C (annotated).)

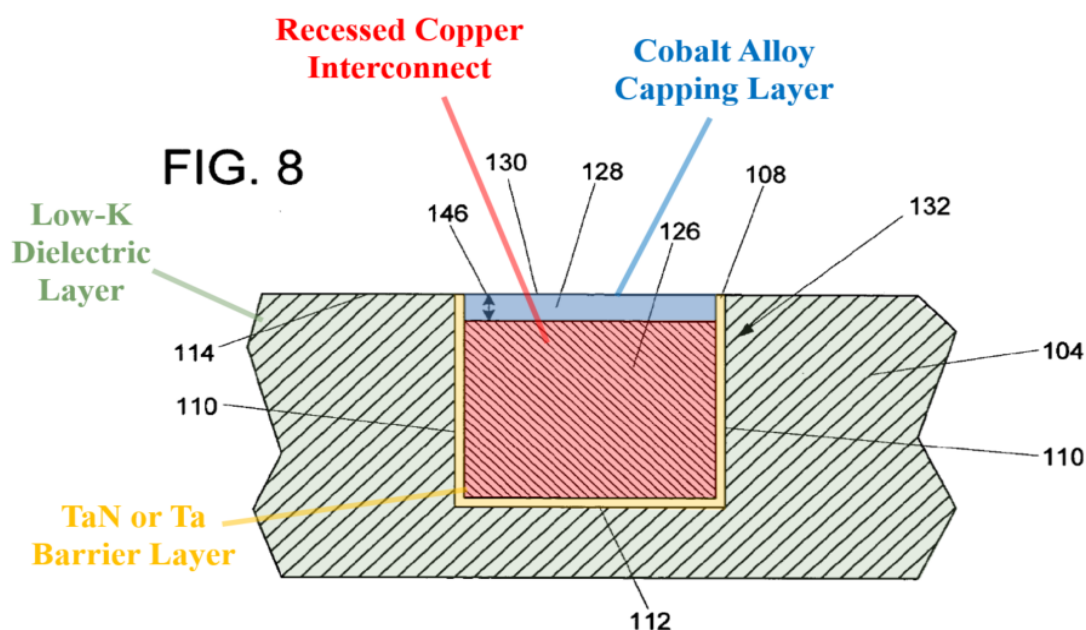
48. Fukunaga discloses that the interlevel insulating film, which may be a low-k material, is a dielectric film. (*Id.*, ¶[0007] (“an insulating film (interlevel **dielectric** film) 10 of, for example, SiO₂ or low-k material”).) A person of ordinary skill in the art would have recognized that “low-k material” refers to “low-k dielectric material” as “low-k” indicates that the material has a low-dielectric constant. (Ex. 1016, 1:57-60 (“Low dielectric constant (k) materials (i.e. ‘low k’

materials), such as fluorinated silica glass (FSG), SiLKTM, and carbon doped oxides (CDO's) have been used to form the ILD, thereby reducing capacitance (C).”).)

49. Fukunaga does not explicitly disclose that the low-k dielectric material includes silicon, oxygen, and carbon. However, as shown by Park and numerous other contemporaneous references, low-k dielectric materials that include silicon (Si), oxygen (O), and carbon (C) were well-known to persons of ordinary skill in the art, and were widely-used in semiconductor devices and interconnect structures like those of Fukunaga. In my opinion, in view of Park and their knowledge of low-k dielectric materials, a person of ordinary skill in the art would have had good reason to form the interconnect structure of Fukunaga such that it includes low-k material that includes silicon (Si), oxygen (O), and carbon (C).

50. Park, like Fukunaga, is directed to copper interconnect structures embedded in low-k materials, where a capping layer overlying recessed copper interconnect is used to prevent electromigration. (Ex. 1006, ¶¶[0018]-[0019], [0023]-[0024], FIG. 8.) Park is entitled “Interconnects Having a Recessed Capping Layer and Methods of Fabricating the Same.” (*Id.*, Title.) As shown and described below, Park discloses an interconnect structure very similar to that disclosed by Fukunaga, including a low-k dielectric layer 104 with an opening lined with barrier layer 108 (e.g. TaN), where a recessed conductive material 126 (e.g., copper) in the opening has an overlying cobalt alloy capping layer 128 that prevents

electromigration of the copper interconnect. (*Id.*, ¶¶[0018]-[0019], ¶[0023] (“As shown in FIG. 8, the recessed conductive material 126 is then capped with a recessed capping layer 128, including, but not limited to, cobalt and alloys thereof. ... The recessed capping layer 128 prevents the electromigration of the conductive material of the interconnect 132”), ¶[0024] (“Referring to FIGS. 1-8, in one embodiment, copper is employed as the conductive material layer 118 deposited over a tantalum/tantalum nitride barrier layer 108 into the opening 106 formed in a low-K dielectric material, such as carbon dope[d] oxide.”), FIG. 8.)



(*Id.*, FIG. 8 (annotated).)

51. Park discloses that the low-k dielectric layer 104 can be formed of carbon doped oxide. (*Id.*, ¶[0018], ¶[0024] (“Referring to FIGS. 1-8, in one embodiment, copper is employed as the conductive material layer 118 deposited

over a tantalum/tantalum nitride barrier layer 108 into the opening 106 formed in a low-K dielectric material, such as carbon dope[d] oxide.”) Carbon doped oxide includes silicon, oxygen, and carbon. (Ex. 1016, 2:44-54 (“In the embodiment shown, the material to be formed on the substrate 100 is Carbon Doped Oxide to act as an ILD. A CDO material is a material that has incorporated silicon (Si), carbon (C), and oxygen (O), providing relatively reduced polarity, density, and conductivity. For example, CDO material can have a dielectric constant (k) that is less than about 3.0. Therefore, CDO materials are generally considered ‘low k’ materials, and useful for lowering capacitance when used as ILD’s as discussed further herein.”))

52. A person of ordinary skill in the art implementing an interconnect structure like that disclosed by Fukunaga would have looked to Park for guidance, particularly because Fukunaga and Park are references in the same field and disclose very similar interconnect structures as shown above. Having looked to Park, such a person of ordinary skill in the art would have had good reason to implement the low-k insulating layer disclosed by Fukunaga such that it includes carbon doped oxide as disclosed by Park.

53. While Fukunaga discloses using a low-k material as the interlevel insulating film 10, Fukunaga does not disclose specific details regarding the chemical makeup of the low-k material in which the interconnect is formed. (Ex.

1005, ¶[0048].) Park, however, discloses a similar low-k material used in a very similar interconnect structure, and Park explicitly discloses using carbon doped oxide for the low-k dielectric. (Ex. 1006, ¶[0018], ¶[0024].) Therefore, a person of ordinary skill in the art would have had good reason to look to Park and would have been motivated to implement the low-k material as disclosed by Fukunaga using carbon doped oxide according to the teachings of Park.

54. Moreover, such a person of ordinary skill in the art would have been motivated to use a carbon doped oxide, which includes silicon, oxygen, and carbon, as the low-k material in an interconnect structure like that disclosed by Fukunaga because the use of such carbon doped oxides in such interconnect structures was known to reduce capacitance and allow for faster signal transmission, reduced power dissipation, and reduced cross-talk. (Ex. 1016, 1:32-37 (“Unfortunately, as capacitance (C) increases so does signal transmission time. Other problems, such as power dissipation and increased cross-talk can also occur. Therefore, reduced capacitance (C) is sought.”), 1:57-60 (“Low dielectric constant (k) materials (i.e. ‘low k’ materials), such as fluorinated silica glass (FSG), SiLK™, and **carbon doped oxides (CDO’s) have been used to form the ILD, thereby reducing capacitance (C).**”) (emphasis added); Ex. 1010, ¶[0004] (“The use of low-k dielectric(K) materials advantageously lowers power consumption, reduces cross talk, and shortens signal delay for closely spaced conductors through reduction of

both nodal and interconnect line capacitances. Dielectric materials, which exhibit low dielectric constants, are critical in the development path toward faster and more power efficient microelectronics.”), ¶[0006] (“**One approach to lowering the dielectric constant of the SiO₂ insulating layer is by incorporation of carbon.**”)

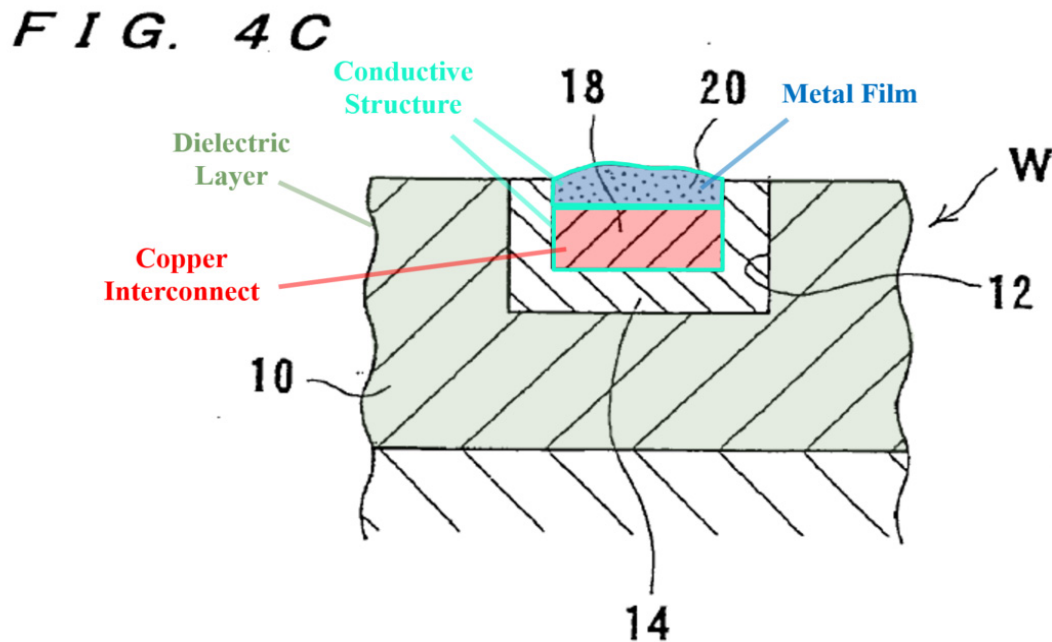
55. Using carbon doped oxides as low-k interlayer dielectrics was well-known and widely-practiced in the art, and a person of ordinary skill in the art would have readily understood that such carbon doped oxides are a viable and preferable low-k dielectric for use in interconnect structures like that disclosed by Fukunaga. (Ex. 1010, ¶[0006] (“In order to produce faster and more power efficient microelectronics with smaller device geometries, insulating materials having dielectric constants of less than 3.0 are necessary. One approach to lowering the dielectric constant of the SiO₂ insulating layer is by incorporation of carbon. Carbon incorporation from between 15-20%, reduces the dielectric constant to as low as 2.7, in part due to the substitution of the high polarized Si—O link by Si—C, (i.e., Nakano, et al., “Effects of Si—C Bond Content on Film Properties of Organic Spin-on Glass” J. Electrochem. Soc., Vol. 142, No 4, Apr. 1995, pp. 1303-1307.”); Ex. 1016, 2:44-54; Ex. 1009 5:20-25 (“Further, the insulating interlayer may be a low dielectric constant insulating film such as silicon oxycarbide (SiOC) film. A specific dielectric constant of the low dielectric constant insulating film may be, for example, equal to or lower than 3.5, and preferable equal to or lower than 3.”; Ex. 1015,

¶[0007] (“The planarized dielectric layer is silicon oxide, carbon doped oxide, SiC_xO_yH_z or a porous dielectric material.”), ¶[0025] (“The dielectric layer 10 can be, for example, any low k or ultra low k material such as, for example, silicon oxide, carbon doped oxide, SiC_xO_yH_z or a porous ILD.”).)

56. As evidenced by the widespread use of carbon doped oxide in similar interconnect structures, a person of ordinary skill in the art would have found it straightforward to use CDO as the low-k material in interconnect structures like those disclosed by Fukunaga. Using CDO as the low-k material in interconnect structures like those disclosed by Fukunaga would have been a straightforward combination of well-known technologies using known methods and would have had predictable results for such a skilled person. Such a person would have known how to use CDO in such a manner and would have had a reasonable expectation of success because, as demonstrated by Park, as well as the numerous contemporaneous references I refer to above, interconnect structures with such carbon doped oxide insulating layers were well known in the art. For at least these reasons, it is my opinion that the Fukunaga-Park combination discloses or suggests claim element 1[b].

c) **“a conductive structure in the dielectric layer, the conductive structure comprising:”**

57. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, as shown in annotated figure 4C below, Fukunaga discloses a conductive structure that includes interconnect 18 and metal film 20 in the trench 12 of the dielectric layer 10, where the interconnect 18 and film 20 are made of metal and, therefore, conductive. (Ex. 1005, ¶[0060] (“First extra copper (interconnect material) 16 formed over the surface of the substrate W is polished and removed by CMP, electrolytic polishing or etching, thereby forming interconnects 18 with the **copper 16 embedded in the trenches** (interconnect recesses) 12”) (emphasis added), ¶[0062] (“Using the barrier layer 14 thus left as a mask, a **metal film (protective film) 20 of, for example, a cobalt alloy** or a nickel alloy is formed selectively on the surfaces of interconnects 18 in the trenches 12, as shown in FIG. 4B, thereby covering the surfaces of interconnects 18 with the metal film 20 to protect interconnects 18.”) (emphasis added), FIGs. 4A-4C).)

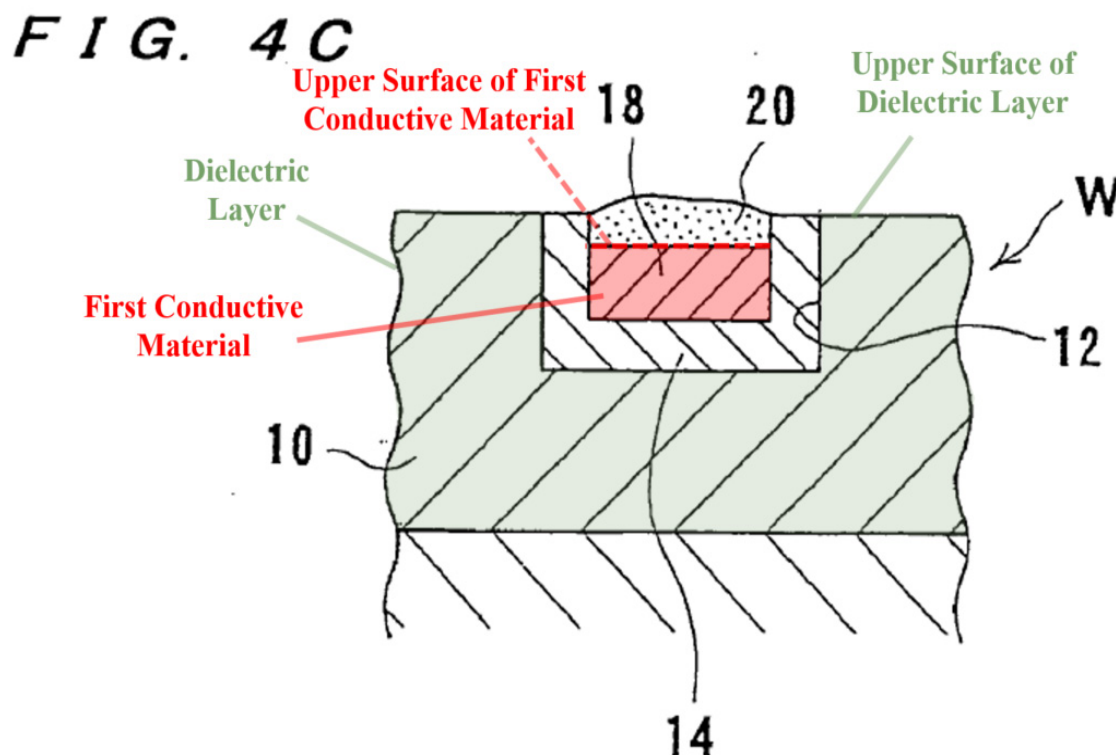


(*Id.*, FIG. 4C (annotated).)

- d) “a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”

58. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, as shown in annotated figure 4C below, the interconnect 18 (“first conductive material”), which is formed of copper, has an upper surface, where a portion of the upper surface is below a portion of the upper surface of the dielectric layer 10. (Ex. 1005, ¶[0060] (“First extra copper (interconnect material) 16 formed over the surface of the substrate **W** is polished and removed by CMP, electrolytic polishing or etching, thereby forming **interconnects 18 with the copper** 16 embedded in the trenches (interconnect recesses) 12 ... polishing or **etching of**

interconnects 18 is further continued so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.”) (emphasis added), ¶[0063] (“By making the distance D between the surface of the barrier layer 14 and the surfaces of the interconnects 18 after the removal of the unnecessary copper almost equal to the sum of the thickness T_1 of the barrier layer 14 and the thickness T_2 of the metal film 20 to be formed on the surfaces of interconnects 18 ($D \approx T_1 + T_2$), as described above, the surface of the substrate W after the removal of the barrier layer 14, which has become unnecessary, can be made flat.”), FIGs. 4A-4C.)



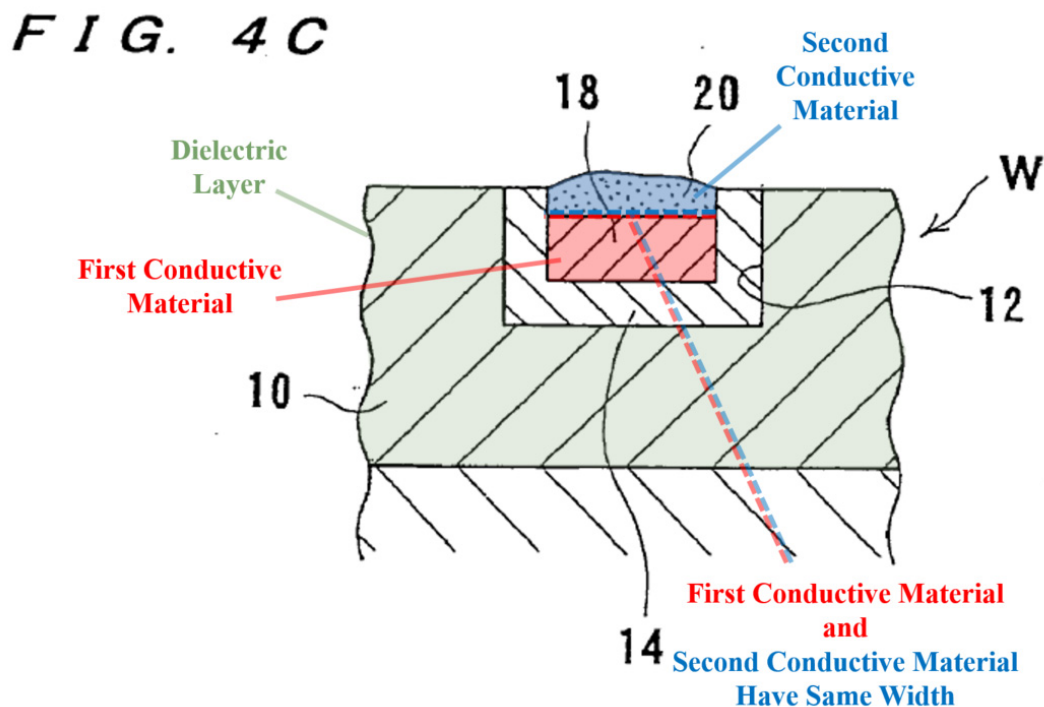
(*Id.* at FIG. 4C (annotated).)

- e) **“a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially coplanar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”**

59. In my opinion, the Fukunaga-Park combination discloses or suggests this feature.³ For example, as shown in annotated figure 4C below, the metal film 20 (“second conductive material”) includes cobalt and is on the upper surface of the interconnect 18 (“first conductive material”). (Ex. 1005, ¶[0062] (“Using the barrier layer 14 thus left as a mask, **a metal film (protective film) 20 of, for example, a cobalt alloy** or a nickel alloy is formed selectively on the surfaces of interconnects 18 in the trenches 12, as shown in FIG. 4B, thereby **covering the surfaces of**

³ While the '183 patent does not provide any explanation as to what constitutes a “curved corner below the portion of the upper surface of the dielectric layer,” I have been asked to assume that such a claim feature is met by a structure that has an upper-surface profile similar to that of the capping layer 215 shown in figure 2H of the '183 patent.

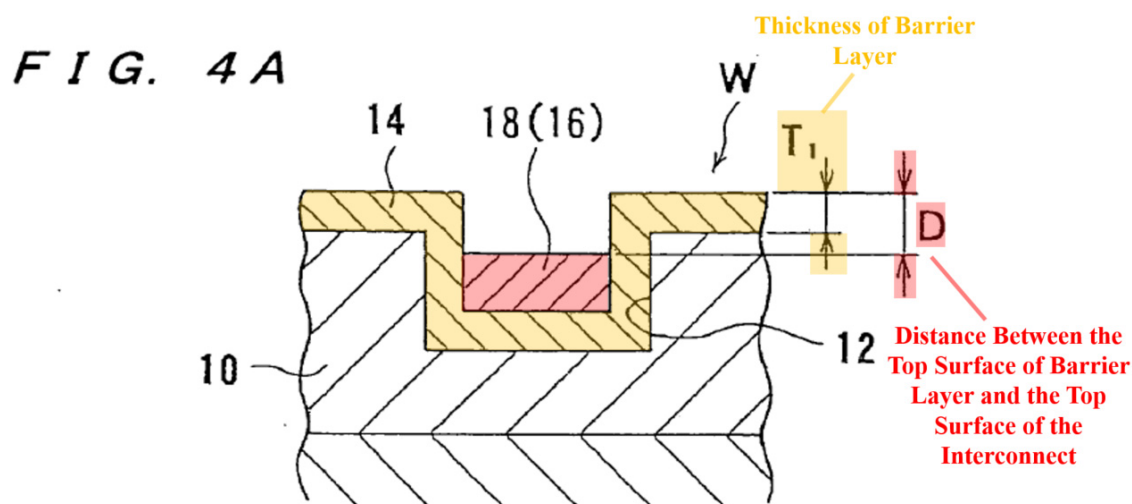
interconnects 18 with the metal film 20 to protect interconnects 18.”) (emphasis added), FIGs. 4B-4C.) Because the metal film 20 (“second conductive material”) is confined by the trench and covers the surface of the interconnect 18 (“first conductive material”), those materials have the same width at the location where they meet. (*Id.*, ¶¶[0062], [0063] (“completing the formation of interconnects 18 of copper whose surfaces are selectively covered and protected with the metal film 20, as shown in FIG. 4C.”), FIGs. 4B-4C.)



(*Id.*, FIG. 4C (annotated).)

60. Fukunaga discloses that the relative positioning of the top surface of the metal film 20 relative to the top surface of the dielectric layer can be adjusted in order to achieve a flat upper surface for the substrate W. (*Id.*, ¶¶[0061], [0063]-

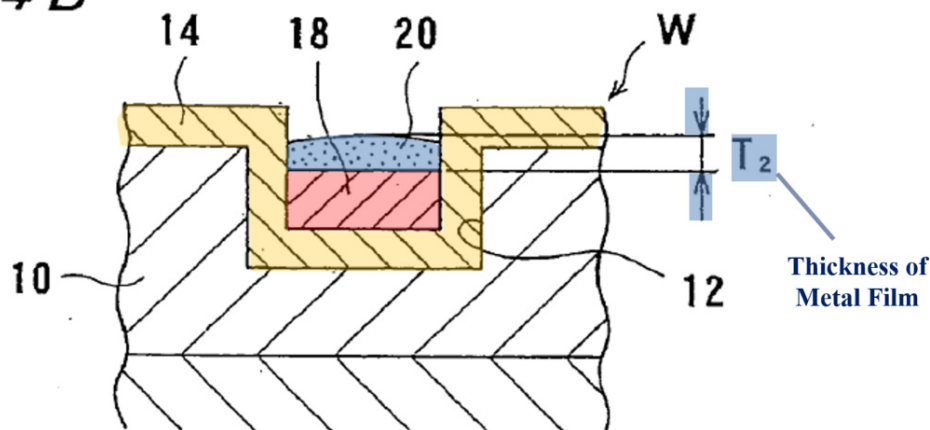
[0065].) For example, Fukunaga discloses that “[t]he distance D between the surface of the barrier layer 14 and the surfaces of the interconnects 18 is determined taking account of the thickness of the barrier layer 14 and the necessary thickness of a metal film 20 to be formed selectively on the surfaces of interconnects 18, as described below.” (*Id.*, ¶[0061].) As shown in annotated figure 4A below, D is the distance between the top surface of the barrier layer 14 and the top surface of the interconnect 18, whereas T_1 is the thickness of the barrier layer 14.



(*Id.*, FIG. 4A (annotated).)

61. The thickness T_2 of the metal film 20 is shown in annotated figure 4B below:

FIG. 4B



(*Id.*, FIG. 4B (annotated).)

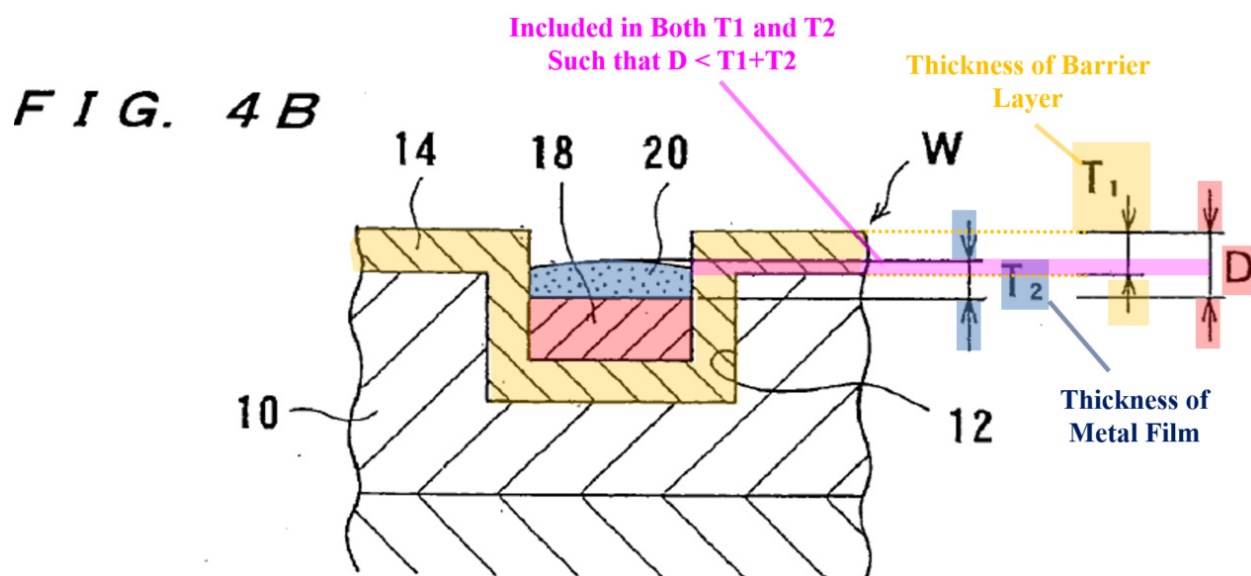
62. Fukunaga further discloses that if the distance D is approximately equal to the sum of the thickness T_1 of the barrier layer 14 and the thickness T_2 of the metal film 20, the result is a flat surface of the substrate:

More preferably, the distance D is made almost equal to the sum of the thickness T_1 of the barrier layer 14 and the thickness T_2 (see FIG. 4B) of the metal film 20 to be formed on the surfaces of the interconnects ($D \approx T_1 + T_2$). For example, when the thickness T_1 of the barrier layer 14 is 10 nm and the necessary thickness T_2 of the metal film 20 is 10 nm, the distance D between the surface of the barrier layer 14 and the surface of the interconnects 18 is made 20 nm. This can **prevent protrusion of the metal film 20 from the surface of the substrate W** after removal of the barrier layer 14 that has become

unnecessary, and can thus **provide the substrate W with a flat surface.**

(*Id.*, ¶[0061] (emphases added).)

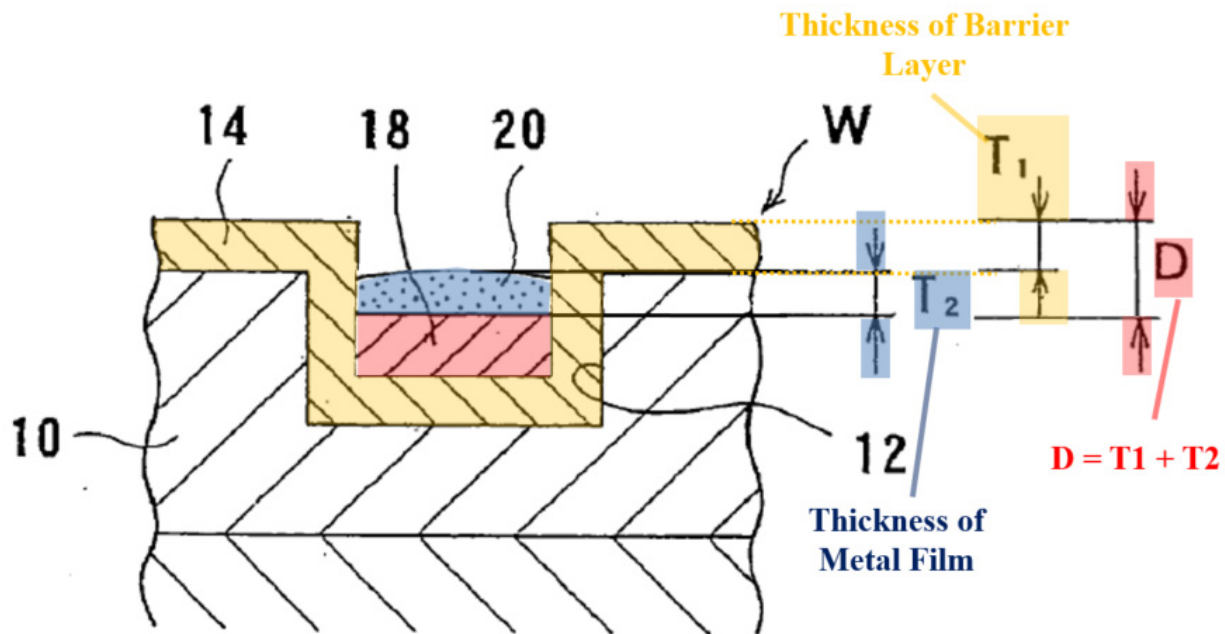
63. The structure shown in figure 4C of Fukunaga results from the removal of the exposed portion of the barrier layer 14 on the insulating film 10 shown in figure 4B, where, as is apparent from the figures, the distance D in the example illustrated in figures 4A-4C is less than the sum of the thicknesses T_1 and T_2 ($D < T_1 + T_2$). This is apparent from figures 4A and 4B, where, as shown in further annotated figure 4B below, both T_1 and T_2 extend over a portion of the barrier layer 14.



(*Id.*, FIG. 4B (annotated).)

64. The demonstrative below is based on figure 4B of Fukunaga, where, as disclosed by Fukunaga, the distance D shown in figure 4B above has been increased

to be approximately equal to the thickness T_1 of the barrier layer 14 plus the thickness T_2 of the metal film 20 structure ($D \approx T_1 + T_2$).



65. Fukunaga further discloses that after formation of the metal film 20, the barrier layer 14 exposed on the top surface of the substrate is removed, where because the distance D is approximately equal to the thickness of the barrier layer 14 and the metal film 20, after removal of the exposed portions of the barrier layer 14, the top surface of the substrate is flat:

Next, only the barrier layer 14 on the insulating film 10, exposed on the surface of the substrate W , is selectively removed by CMP or etching, thereby completing the formation of the interconnects 18 of copper whose surfaces are selectively covered and protected with the metal film 20, as shown in FIG. 4C. **By making the**

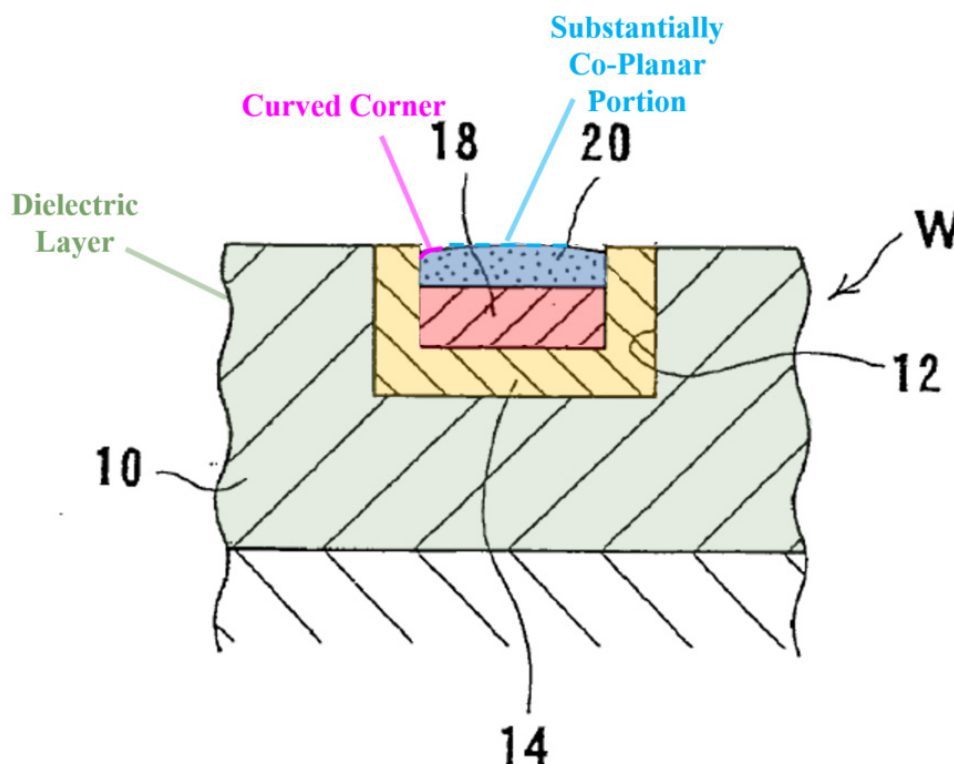
distance D between the surface of the barrier layer 14 and the surfaces of the interconnects 18 after the removal of the unnecessary copper almost equal to the sum of the thickness T_1 of the barrier layer 14 and the thickness T_2 of the metal film 20 to be formed on the surfaces of interconnects 18 ($D \approx T_1 + T_2$), as described above, the surface of the substrate W after the removal of the barrier layer 14, which has become unnecessary, can be made flat.

(*Id.*, ¶[0063] (emphases added).)

66. The demonstrative below is based on the demonstrative above where the distance D is approximately equal to $T_1 + T_2$, and where the exposed portion of the barrier layer 14 has been removed in the same manner disclosed by Fukunaga with respect to the transition between figure 4B and figure 4C. As shown in the demonstrative, the metal film 20 (“second conductive material”) has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer 10, where, as disclosed by Fukunaga, that results in the surface of the substrate W being “flat” where there is no protrusion of the metal film 20 from the surface of the substrate W after removal of the barrier layer 14. (*Id.*, ¶[0017] (“By removing the interconnect material such that the surfaces of the interconnects formed in the interconnect recesses becomes lower than the surface of the insulating film and forming a metal film on the surfaces of interconnects such that the surface

of the metal film becomes substantially flush with the surface of the insulating film, it becomes possible to provide a flat substrate after removing the barrier layer.”),

¶¶[0061], [0063], FIGs. 4A-4C.)



67. Moreover, as also shown in the demonstrative above, and as is consistent with the formation of the metal film 20 by electroless plating as disclosed by Fukunaga, the upper surface of the metal film 20 (“second conductive material”) has a curved corner below the portion of the upper surface of the dielectric layer 10.⁴

⁴ While the '183 patent does not provide any explanation as to what constitutes a “curved corner below the portion of the upper surface of the dielectric layer,” I have

(Ex. 1005, ¶¶[0005] (“Such a protective film of a Co alloy, a Ni alloy, or the like can be produced e.g. by electroless plating.”), [0009] (“Then, as shown in FIG. 1D, electroless plating is performed on a surface of the substrate W to selectively form a protective film 9 of a Co alloy, a Ni alloy, or the like on the surface of interconnects 8, thereby covering and protecting the surfaces of interconnects 8 with the protective film 9.”), [0053] (“The formation of the metal film 20 is carried out, for example, by electroless plating”), FIGs. 1D, 3B, 4B, 5B; Ex. 1012, ¶[0005] (“Typically, the cobalt films are deposited on the copper by electroless plating. The plating process may produce a cobalt film having a mushroom shaped profile.”; Ex. 1009, 7:4-9 (disclosing using electroless plating for forming CoWP cap film), 8:47-52 (mushroom shape can result from formation of the cap film), 7:4-9 (disclosing using electroless plating for forming CoWP cap film in FIG. 6B), FIG. 6B.)

68. The '183 patent does not include any description of a “curved corner” resulting from formation of the capping layer, and the only possible support for such a claimed feature is in figures 2H and 3B. Therefore, a person of ordinary skill in

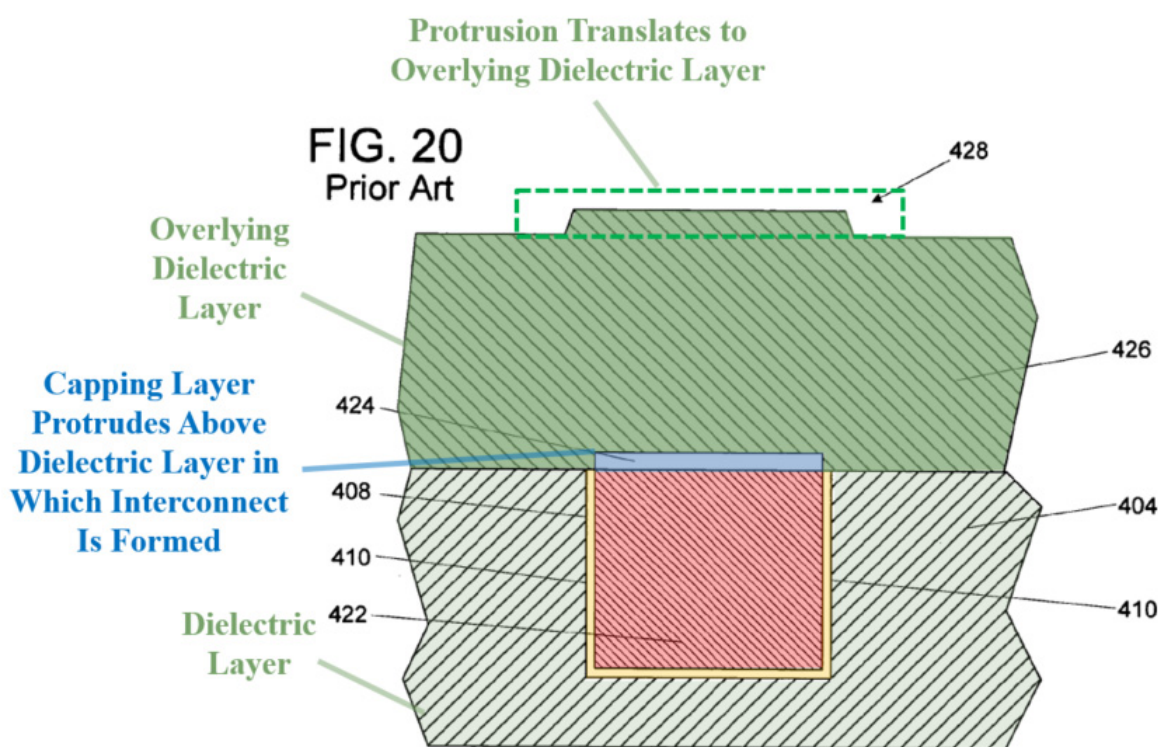
been asked to assume that such a claim feature is met by a structure that has an upper-surface profile similar to that of the capping layer 215 shown in figure 2H of the '183 patent.

the art would have understood that Fukunaga discloses such a “curved corner” in a manner consistent with disclosure of such a feature in the ’183 patent.

69. I have been asked to assume the scenario in which Fukunaga does not explicitly disclose that “the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer.” Under such an assumption, it is my opinion that such a feature would have been disclosed or suggested by the Fukunaga-Park combination.

70. Fukunaga’s metal film 20 is analogous to Park’s capping layer 128, as both are deposited in the dielectric trench to form a cap overlying the recessed conductive material corresponding to the interconnect lines, where the metal film 20 and capping layer 128 are both disclosed as cobalt-alloys that protect the underlying conductive material. (Ex. 1005, ¶[0005] (“In order to prevent thermal diffusion of such interconnects (copper), or to prevent oxidation of such interconnects (copper) e.g. during forming thereon an insulating film (oxide film) under an oxidizing atmosphere later to produce a semiconductor device having a multi-level interconnect structure, it is now under study to selectively cover the exposed surfaces of interconnects with an **protective film (cap material) composed of a Co alloy**, a Ni alloy, or the like so as to prevent thermal diffusion and oxidation of interconnects.”) (emphasis added).) Park discloses that “[t]he recessed capping layer 128 is preferably formed to fill the recess 124 such that a first surface 130 of the

recessed capping layer 128 is substantially planar to the first dielectric material layer first surface 114. (Ex. 1006, ¶[0023] (emphasis added); *see also id.*, claims 1, 4, 10, 18.) Park further discloses that if the capping layer has an elevation difference compared to the dielectric layer such that the capping layer protrudes from the surface of the dielectric layer, then that elevation difference is translated into overlying dielectric layers, which can result in non-planar topography. (*Id.*, ¶¶[0007]-[0008], FIG. 20.)



(*Id.*, FIG. 20 (annotated).)

71. Park further discloses that such topography changes on dielectric layers is undesirable as it interferes with the formation of subsequent layers. (*Id.*, ¶[0008],

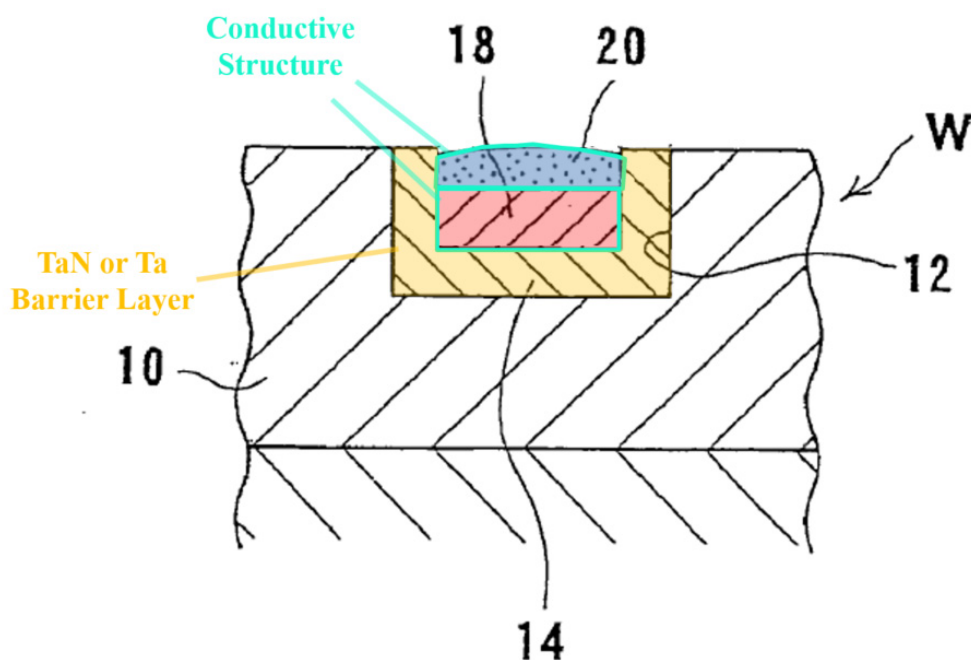
(“Of course, significant topography changes on any dielectric material layer surface is very challenging in lithography due to its limitation of DOF (Depth of Focus), as will be understood by those skilled in the art.”); *see also id.*, Abstract, ¶¶[0002], [0010], [0017].) As such, to the extent not already disclosed or suggested by Fukunaga, in my opinion, a person of ordinary skill in the art would have been motivated to make the top surface of the metal film 20 substantially planar with the top surface of the dielectric layer 10 in order to avoid topographical changes as taught by Park.

f) “a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”

72. In my opinion, the Fukunaga-Park combination discloses or suggests this feature.⁵ For example, Fukunaga discloses forming a barrier layer 14 in the recesses of the insulating film, where the interconnect 18 (“first conductive material”) and metal film 20 (“second conductive material”) included in the conductive structure are formed within the recesses such that the barrier layer 14 partially surrounds the conductive structure. (Ex. 1005, ¶[0013] (“forming a barrier

⁵ While it is unclear what constitutes “partially surrounding,” I have been asked to assume that a barrier layer that is in contact with the conductive structure and surrounds the conductive structure on three sides satisfies this limitation.

layer over a substrate surface having interconnect recesses formed in an insulating film, and then forming a film of an interconnect material in the interconnect recesses and over the substrate surface; . . . and forming a metal film selectively on surfaces of interconnects.”); ¶[0048] (“a barrier layer 14 of TaN, Ta, TiN, WN, or the like is formed by sputtering, ALD (atomic layer deposition), or the like over substantially the entire surface of the insulating film 10.”), (“A film of copper (interconnect material) 16 is formed, for example, by plating, CVD, or the like over the surface of the substrate W, thereby embedding copper in the trenches (interconnect recesses) 12”), ¶[0062] (“Using the barrier layer 14 thus left as a mask, a metal film (protective film) 20 of, for example, a cobalt alloy or nickel alloy is formed selectively on the surfaces of interconnects 18 in the trenches 12 as shown in FIG. 4B”), FIGs. 4A-4C.) As shown in the demonstrative discussed above for claim element 1[e], which is replicated and further annotated below, the barrier layer 14, which Fukunaga discloses is tantalum nitride (TaN) or tantalum (Ta) (Ex. 1005, ¶[0048]), partially surrounds the conductive structure that includes the interconnect 18 and metal film 20, as recited in claim 1.



2. Claim 2

“The integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.”

73. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Fukunaga discloses a barrier layer 14 made of tantalum-nitride, which includes tantalum (Ta) and nitrogen (N). (Ex. 1005, ¶[0048] (“a barrier layer 14 of **TaN**, Ta, TiN, WN, or the like is formed by sputtering, ALD (atomic layer deposition), or the like over substantially the entire surface of the insulating film 10.”) (emphasis added).)

3. Claims 3-8

Claim 3: “The integrated circuit structure of claim 1, wherein the second conductive material further comprises boron.”

Claim 4: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises phosphorus.”

Claim 5: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten.”

Claim 6: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten and phosphorus.”

Claim 7: “The integrated circuit structure of claim 1, wherein the second conductive material further comprises phosphorus.”

74. In my opinion, Fukunaga in view of Park discloses or suggests these features. Claims 3-8 recite various cobalt-containing alloys used for the second conductive material, which corresponds to the metal film 20 that serves as a capping layer in the Fukunaga-Park combination. A person of skill in the art would have known, as demonstrated below, that cobalt containing alloys like those recited in claims 3-8 were well-known and widely-used in the industry as capping layers for copper interconnect like the metal film 20 in Fukunaga and capping layer 128 in Park. Therefore, in my opinion, a person of ordinary skill in the art would have good reason to use such alloys for the metal film 20 in the Fukunaga-Park combination.

75. Fukunaga discloses that the metal film 20 (“second conductive material”) used as the capping layer can be made of a cobalt alloy. (Ex. 1005, ¶[0062] (“Using the barrier layer 14 thus left as a mask, **a metal film (protective**

film) 20 of, for example, **a cobalt alloy** or a nickel alloy is formed selectively on the surfaces of interconnects 18 in the trenches 12, as shown in FIG. 4B, thereby covering the surfaces of interconnects 18 with the metal film 20 to protect interconnects 18.”) (emphasis added).) Fukunaga does not expressly disclose that the “cobalt alloy” metal film 20 includes one or more of boron, phosphorus, or tungsten, but Park discloses using such alloys for a very similar capping layer in a very similar interconnect structure, and a person of ordinary skill in the art would have had good reason to include one or more of boron, phosphorus, and tungsten in the “cobalt alloy” used for the metal film in the interconnect structure disclosed of suggested by the Fukunaga-Park combination that I discuss above for claim 1.

76. As I discuss above for claim element 1[b], Fukunaga and Park are both directed to copper interconnect structures embedded in low-k materials, where there is a protective capping layer (i.e., metal film 20 in Fukunaga and capping layer 128 in Park) overlying the recessed copper interconnect. (See my discussion above in sections IX.A.1(b), (e).) Both Fukunaga and Park disclose that the capping layer can be formed of cobalt alloys. (Ex. 1005, ¶¶[0005], [0062]; Ex. 1006, ¶[0027].) Park further discloses that the capping layer 128 can be formed of cobalt alloys that include one or more of boron (B), phosphorus (P), and tungsten (W) as well as other elements:

The cobalt is deposited by electroless plating to fill the recess 124 (about 10 nm) to form the recessed capping layer 128. **The cobalt may, of course, also be any binary, ternary, or quaternary cobalt alloy containing tungsten, phosphorus, boron, molybdenum, rhenium, or the like.**

(Ex. 1006, ¶[0027] (emphasis added); *see also id.*, claims 16 and 17.)

77. Because Park discloses that the capping layer 128 includes alloys that include, two (binary), three (ternary), or four (quaternary) materials from a list that includes cobalt (Co), tungsten (W), phosphorus (P), and boron (B), Park discloses the capping layer 128 includes Co and B (claim 3), Co, B, and P (claim 4), Co, B, and W (claim 5), Co, B, W, and P (claim 6), Co and P (claim 7), and Co, P, and W (claim 8).

78. A person of ordinary skill in the art implementing an interconnect structure of the Fukunaga-Park combination discussed above for claim 1 would have had good reason to implement the cobalt alloys used for the capping layer such that they include one or more of boron, phosphorus, and tungsten as disclosed by Park. While Fukunaga discloses using “cobalt alloys” as the metal film 20 forming the capping layer, Fukunaga does not specifically disclose the other elements included with cobalt in the cobalt alloys. Park discloses a similar capping layer 128 used in a very similar interconnect structure and explicitly discloses additional elements that

can be included in the cobalt alloys used for such a capping layer. Therefore, a person of ordinary skill in the art would have had good reason to look to Park for specifics as to suitable cobalt alloys and would have had good reason to implement the cobalt alloys as disclosed by Fukunaga according to the teachings of Park. Fukunaga does not disclose the details of the composition of the cobalt alloys in the capping layer, and therefore a person of ordinary skill in the art would have looked to Park, which discloses such details.

79. Such a person of ordinary skill in the art would also have been motivated to use a cobalt alloy that includes boron, phosphorus, and tungsten in the various combinations recited in claims 3-8 because the use of such alloys for capping layers in similar interconnect structures was well-known and widely-practiced in the art. (Ex. 1012, ¶[0018] (“The capping layer 26 is a conductive material such as cobalt (Co) and can be doped with other elements such as tungsten (W) or boron (B). In one embodiment the capping layer 26 comprises cobalt (Co), tungsten (W) and boron (B). ... Also, the capping layer 26 can be doped with elements like nickel (Ni), molybdenum (Mo), rhenium (Re), and phosphorus (P).”); Ex. 1009 5:50-53 (“The protective film 115 and the protective film 129 contain, for example, one or more element selected from Co and Ni and one or more element selected from tungsten (W) and phosphorus (P) and boron (B) as constituent element”); Ex. 1014, ¶[0028] (“FIG. 6A illustrates the formation of metal caps 48 and 50 on copper lines

32 and 34, respectively. Metal caps 48 and 50 preferably comprise materials such as CoP, CoB, CoWP, CoWB ... and combinations thereof. Metal caps 48 and 50 may also be composite layers including more than one layer, wherein each of the layers includes one or more of the above-discussed materials.”); Ex. 1015, ¶[0017] (“The cap layer 28 may be, for example, CoWP or CoWB or other appropriate capping materials designed to prevent copper migration.”).)

80. A person of ordinary skill in the art would have found it straightforward to use cobalt alloys that include one or more of boron, phosphorus, and tungsten as recited in claims 3-8 as the cobalt-containing alloy for the metal film 20 as disclosed by Fukunaga because Park explicitly discloses the use of such alloys as a capping layer in an interconnect structure very similar to that of Fukunaga and because such a person of ordinary skill in the art would have known that such alloys were commonly used for exactly such a purpose in numerous contemporaneous interconnect structures. Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. Moreover, such a skilled person would have had a reasonable expectation of success because, as demonstrated by Park and the numerous contemporaneous references I refer to above that demonstrate the knowledge of such a skilled person, interconnect structures with such cobalt-alloy capping layers were well known in the art.

81. A person of ordinary skill in the art would take note that '183 patent does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the different combinations of materials recited in claims 3-8. Instead, the '183 patent simply provides an extensive list of different materials and combinations of materials that can be included in the second conductive material. (Ex. 1001, 9:35-48.)

82. For at least these reasons, it is my opinion that the Fukunaga-Park combination discloses or suggests that the second conductive material includes cobalt as well as boron, phosphorus, and tungsten in the various combinations recited in claims 3-8.

4. Claim 9

a) “A method of fabricating an integrated circuit structure, the method comprising:”

83. I understand that a “method of fabricating an integrated circuit structure, the method comprising” is the preamble to claim 9 of the '183 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, it is my opinion that Fukunaga discloses this feature. For example, Fukunaga discloses how to form the interconnect structure (“integrated circuit structure”) that I discuss above with respect to claim element 1[e], which is included as a part of an integrated circuit. (See my discussion above for claim elements 1[a], 1[e].) Fukunaga discloses formation of such interconnects that can be used in, for

example, multi-level interconnect structures overlying a semiconductor base on which semiconductor devices are formed. (Ex. 1005, Abstract, ¶[0002] (“The present invention relates to **an interconnects forming method** and an interconnects forming apparatus, and more particularly to **an interconnects forming method** and an interconnects forming apparatus which are useful for embedding a conductive material (interconnect material), such as copper or silver, **into interconnect recesses provided in a surface of a substrate, such as a semiconductor wafer, to thereby form embedded interconnects**, and selectively covering surfaces of the embedded interconnects with a metal film (protective film) to provide a multi-level structure.”), ¶[0005] (“a semiconductor device having a multi-level interconnect structure”), ¶[0007] (“forming copper interconnects in a semiconductor device”), (“a conductive layer 1a formed on a semiconductor base 1 having formed semiconductor devices”), ¶[0074] (“semiconductor wafers”); ¶[0060] (“FIGS. 4A through 4C illustrate, in a sequence of process steps, an interconnects forming method according to another embodiment of the present invention.”); *see also* my analysis and citations below for the remaining limitations of this claim.)

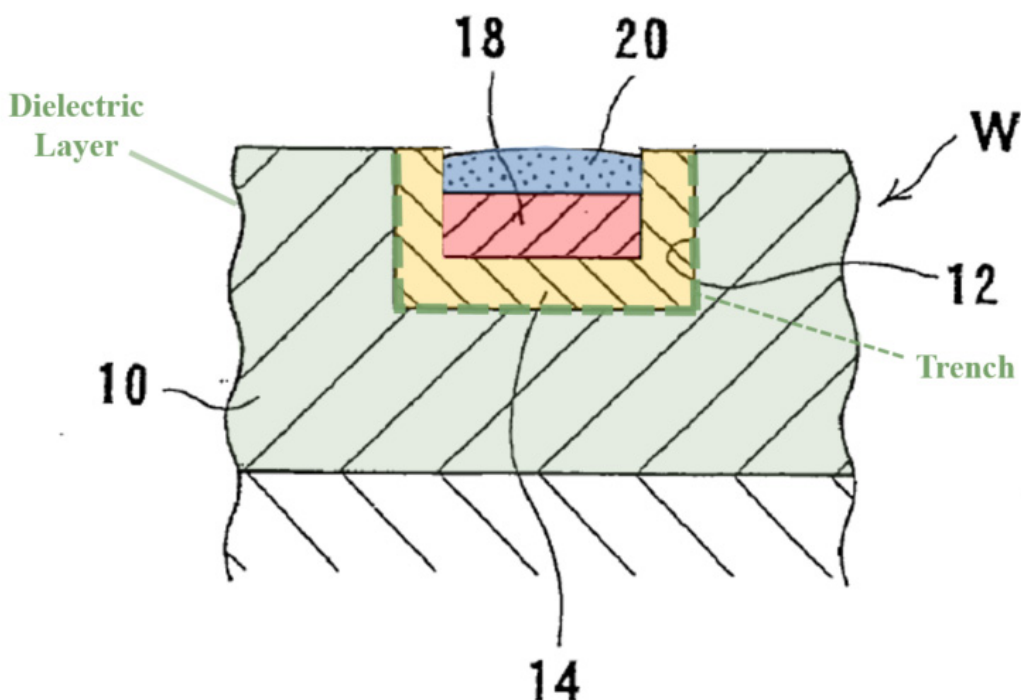
b) “forming a dielectric layer comprising silicon, oxygen and carbon;”

84. In my opinion, the Fukunaga-Park combination discloses or suggests this claim feature. For example, Fukunaga discloses that “[a]s shown in FIG. 2,

trenches 12 as interconnect recesses are formed, for example, by the lithography/etching technique, in **an insulating film (interlevel insulating film) 10** of, for example, SiO₂ or a **low-k material deposited on a substrate W**)". (Ex. 1005, ¶[0048] (emphasis added); *see also id.*, ¶[0007] ("As shown in FIG. 1A, an insulating film (interlevel dielectric film) 2 of , for example, SiO₂ or a low-k material is deposited on a conductive layer 1a formed on a semiconductor base 1 having semiconductor devices.")) As I discuss above for claim element 1[b], the Fukunaga-Park combination discloses or suggests forming the insulating film 10 ("dielectric layer") such that it includes silicon (Si), oxygen (O), and carbon (C). (See my discussion above in section IX.A.1(b).)

c) "forming a trench in the dielectric layer;"

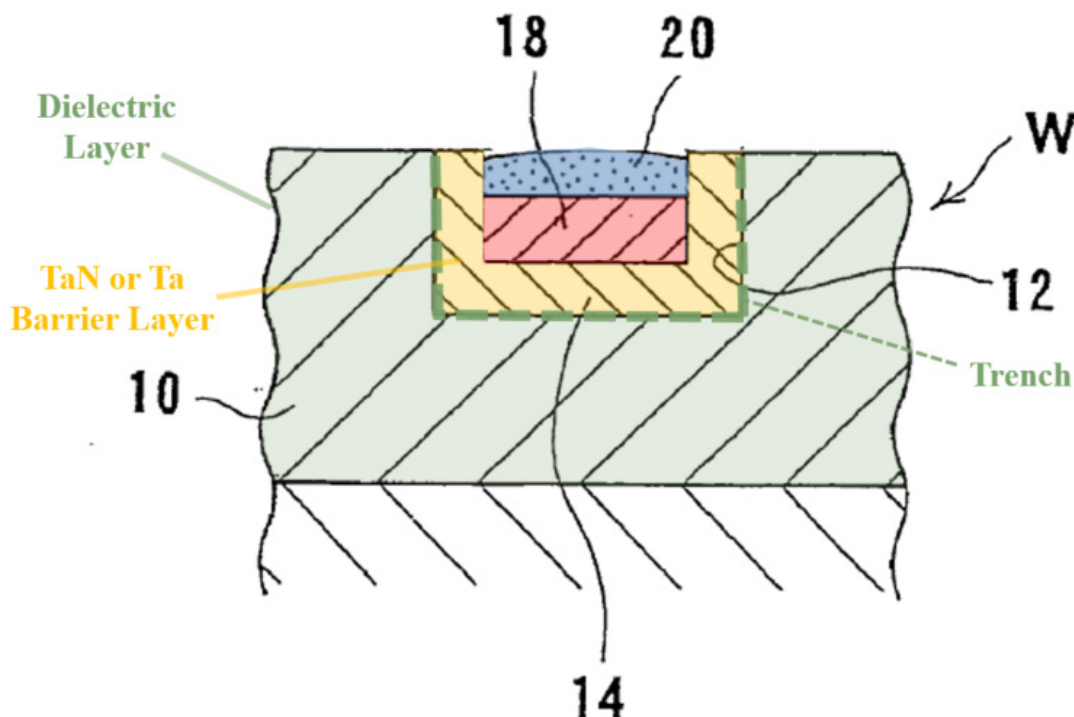
85. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Fukunaga discloses forming trenches 12 in the insulating film 10 ("dielectric layer"). (Ex. 1005, ¶[0048] "As shown in FIG. 2, **trenches 12 as interconnect recesses are formed, for example, by the lithography/etching technique, in an insulating film (interlevel insulating film) 10** of, for example, SiO₂ or a low-k material deposited on a substrate W") (emphasis added).) The trench 12 is shown in the demonstrative below, which corresponds to the embodiment discussed above for claim element 1[e]. (See my discussion above in section IX.A.1(e).)



d) “forming a barrier layer in the trench, the barrier layer comprising tantalum;”

86. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, as I discuss above for claim element 1[f], Fukunaga discloses forming the barrier layer 14 in the recesses (“trench”) of the insulating film, where the barrier layer 14 can be formed of tantalum (Ta) or tantalum nitride (TaN). (Ex. 1005, ¶[0013] (“forming a barrier layer over a substrate surface having interconnect recesses formed in an insulating film, ...”); ¶[0048] (“**a barrier layer 14 of TaN, Ta, TiN, WN, or the like is formed by sputtering, ALD (atomic layer deposition), or the like** over substantially the entire surface of the insulating film 10.”); *see* my discussion above in section IX.A.1(f).) The barrier layer 14 is shown

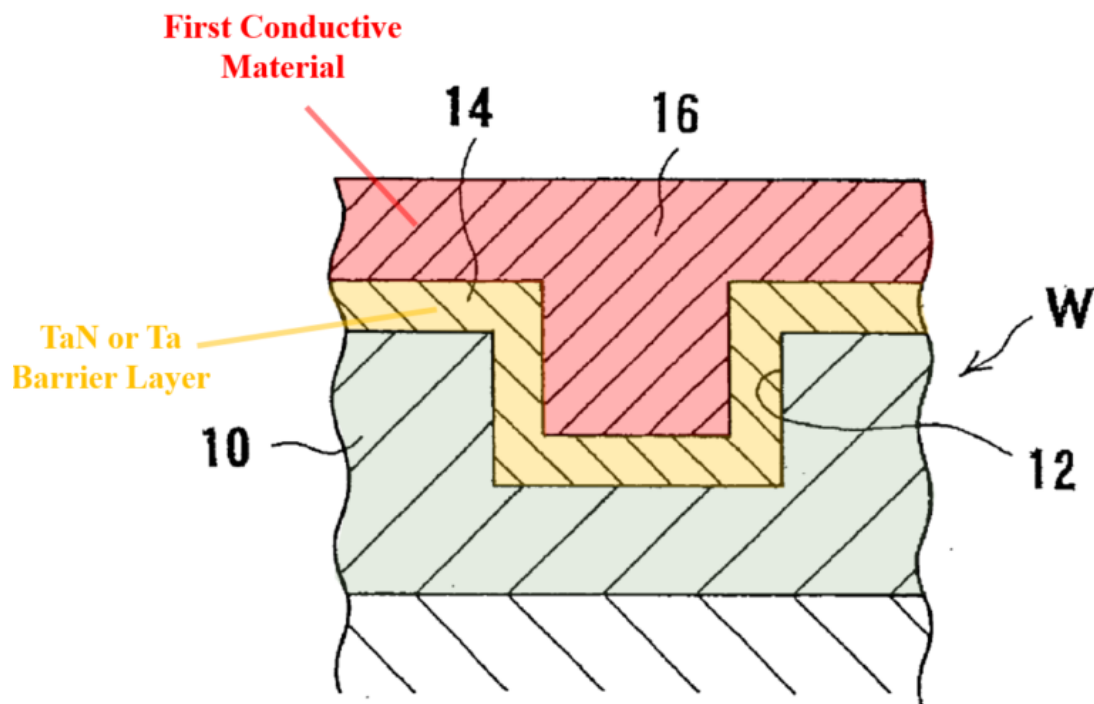
in the demonstrative discussed above for claim element 1[e] above, which is replicated and further annotated below.



- e) **“forming a first conductive material within the barrier layer, the first conductive material comprising copper;”**

87. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Fukunaga discloses that “[a] film of copper (interconnect material) 16 is formed, for example, by plating, CVD, or the like over the surface of the substrate W, thereby embedding copper in the trenches (interconnect recesses) 12.” (Ex. 1005, ¶[0048]; *see also id.*, ¶[0060].) Annotated figure 2 of Fukunaga shows the interconnect 16 after its formation. (*Id.*, ¶¶[0048]-[0049].)

FIG. 2



(*Id.*, FIG. 2 (annotated).)

f) “recessing the first conductive material below a portion of an upper surface of the dielectric layer; and”

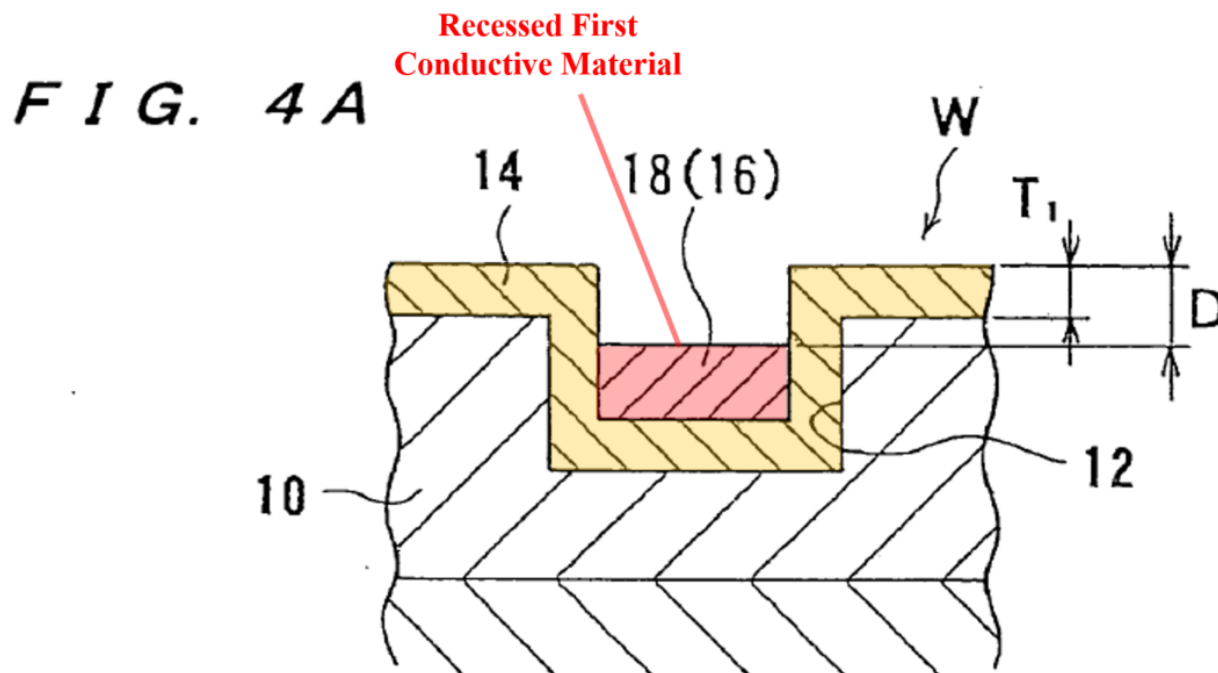
88. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Fukunaga discloses recessing the interconnect material 16 (“first conductive material”) to form a channel below the upper surface of the dielectric layer:

FIGS. 4A through 4C illustrate, in a sequence of process steps, an interconnects forming method according to another embodiment of the present invention. First, extra copper (interconnect material) 16 formed over the surface

of the substrate W is polished and removed by CMP, electrolytic polishing or etching, thereby forming interconnects 18 with the copper 16 embedded in the trenches (interconnect recesses) 12 and making exposed the barrier layer 14 present in the other portion than the interconnect-formed portion, as shown in FIG. 4A. The removal of the extra copper 16 is carried out in such a manner that after the surfaces of the interconnects 18 in the trenches 12 have become substantially flush with the surface of the exposed barrier layer 14, **polishing or etching of interconnects 18 is further continued so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.**

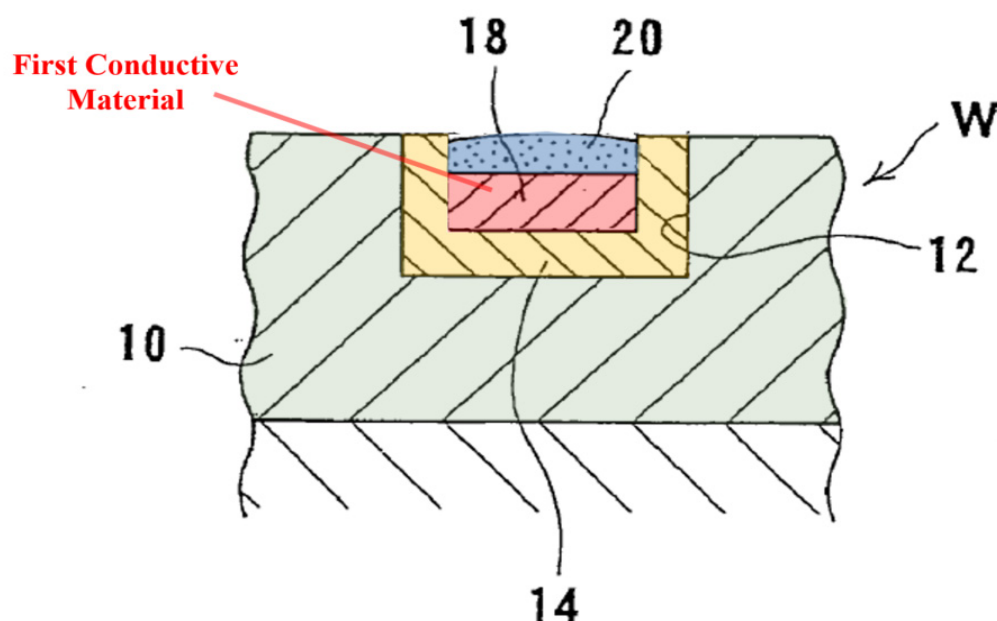
(Ex. 1005, ¶[0060] (emphasis added).)

89. The recessed interconnect material 16 is shown in annotated figure 4A below.



(*Id.*, FIG. 4A (annotated).)

90. As I discuss above for claim element 1[e], Fukunaga discloses the distance D between the top surface of the barrier layer and the top surface of the recessed interconnect 18 is preferably approximately equal to the sum of the thickness of the barrier layer 14 and the thickness of the subsequently deposited metal film 20. (*See* my discussion above in section IX.A.1(e).) The demonstrative below, which corresponds to the embodiment I discuss above for claim element 1[e], shows the interconnect 18 recessed according to such a preferred scenario.



- g) “forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a position where the first conductive material and the second conductive material meet, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer.”

91. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Fukunaga discloses forming the metal film 20 (“second conductive material”), where, as I discuss above for claim element 1[e], the Fukunaga-Park combination discloses or suggests forming the metal film 20 such that (1) the metal film 20 is on the upper surface of the recessed first conductive material, (2) the metal film 20 comprises cobalt, (3) the interconnect 18 and metal film 20 have the same width at a position where they meet, and (4) the upper surface

of the metal film has a curved corner below the portion of the upper surface of the dielectric layer. (*See* my discussion above in section IX.A.1(e).)

5. Claim 10

“The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.”

92. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Fukunaga discloses that, after depositing the copper 16, wet etching is used to remove extra copper 16 (“first conductive material”) above the top surface of the barrier layer 14 so that the surfaces of interconnects 18 in the trenches is flush with the top surface of the barrier layer. (Ex. 1005, ¶[0050], (“[t]he surface of the copper 16 is polished away, leaving the barrier layer 14, so that the surfaces of interconnects 18 in the trenches 12 becomes substantially flush with the surface of the barrier layer 14”), ¶[0051] (“The removal of the extra copper 16 may also be carried out by **etching using an inorganic or organic acid.**”).) A person of ordinary skill in the art would have understood that such etching using acid is “wet etching.” (*See* my discussion above in section V.D.)

93. Fukunaga further discloses that **“etching of interconnects 18 is further continued** so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.” (*Id.*, ¶[0060].) As such, a person of ordinary skill in the art would understand that Fukunaga discloses

or suggests using wet etching to remove the extra copper on the surface of the barrier layer and then continuing that same etching to recess the surface of the interconnects 18. Therefore, in my opinion, the Fukunaga-Park combination discloses or suggests using wet etching to recess the conductive material as recited in claim 10.

94. I have been asked to assume a scenario in which Fukunaga does not disclose using wet etching to recess the conductive material. Under such an assumption, it is still my opinion that the Fukunaga-Park combination discloses or suggests this claim feature. As I noted above, Fukunaga discloses using wet etching to remove the extra copper material outside of the trench. A person of ordinary skill in the art would have understood that using the same acid wet etch to remove both the extra copper outside of the trench as well as the copper in the trench to recess the interconnect would require fewer process steps and simplify manufacturing. Moreover, Fukunaga discloses that wet etching is a preferred form of etching for such material removal as no load is applied to the substrate by such etching, and, in the case where porous low-k dielectric materials are included in the structure, load-applying material removal processes (e.g. chemical mechanic polishing) are less desirable as they can damage the wafer:

In the case of wet etching, no physical force is applied to a substrate. Accordingly, there is no fear of damage to the substrate even when a weak material, such as copper or low-k materials, is present in the substrate. In the case of

a CMP method, on the other hand, processing of a substrate is carried out while applying a load on the substrate, and there is therefore a fear of damage to the substrate. Accordingly, it is necessary with a CMP method to use a slurry having a strong chemical reactivity and carry out polishing at a low pressure and a low speed. As regards electrolytic polishing, as **with wet etching, substantially no load is applied on a substrate, and therefore there is no fear of damage to the substrate.**

(Ex. 1005, ¶[0057] (emphasis added).)

95. Moreover, a person of ordinary skill in the art would have known that wet-etching using an acidic solution, as taught by Fukunaga, was a well-known etching technique for etching recesses in interconnect material like the copper interconnect of Fukunaga. (Ex. 1007, ¶[0038] (“After chemical-mechanical polishing, an acidic solution from source 106 is applied to wafer 80 in FIG. 5C. The acidic solution may take from in HNO₃/H₂O, HCL/KCLO₃/H₂O, or heated HCl/H₂O. Other acidic solutions are contemplated for etching copper interconnects 120. The acidic solution etches the copper interconnects 120, but will not substantially affect the dielectric material 82. Recesses 122 are formed or deepened in the copper interconnects 120 after application of the acidic solution, as shown in FIG. 5D.”); *see also id.*, ¶¶[0007]-[0008]; Ex. 1011, ¶[0066].)

96. Therefore, for these additional reasons, it is my opinion that a person of ordinary skill in the art would have been motivated to perform the etching disclosed by Fukunaga as being used for recessing the interconnect in the trench as wet etching. As noted above, Fukunaga discloses using wet etching to remove excess interconnect material and further discloses using etching to recess the interconnect material below the top surface of the dielectric layer. Based on Fukunaga's teachings regarding wet etching, a person of ordinary skill in the art would have been motivated to use wet etching to recess the interconnect material as it would have been an effective way of removing such material and would not have required the application of a load to the substrate, thereby avoid possible damage to the substrate.

6. Claim 11

“The method of claim 9, wherein the barrier layer further comprises nitrogen.”

97. In my opinion, the Fukunaga-Park combination discloses or suggests this feature for the same reasons I discuss above with respect to claim 2. (*See my discussion above in section IX.A.2.*)

7. Claims 12-17

Claim 12: “The integrated circuit structure of claim 9, wherein the second conductive material further comprises boron.”

Claim 13: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises phosphorus.”

Claim 14: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises tungsten.”

Claim 15: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises tungsten and phosphorus.”

Claim 16: “The integrated circuit structure of claim 9, wherein the second conductive material further comprises phosphorus.”

Claim 17: “The integrated circuit structure of claim 16, wherein the second conductive material further comprises tungsten.”

98. In my opinion, the Fukunaga-Park combination discloses or suggests these features for the same reasons I discuss above with respect to claims 3-8. (*See* my discussion above in section IX.A.3.)

8. Claim 18

a) “A computing device, comprising:”

99. I understand that “[a] computing device, comprising” is the preamble to claim 18 of the ’183 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, the Fukunaga-Park combination discloses or suggests “a computing device.” As I discuss above for claim element 1[b], Fukunaga and Park disclose similar interconnect structures that include a capping layer formed on a recessed interconnect line. (*See* my discussion above in section IX.A.1(b).) While Fukunaga discloses that the interconnect structure can be used in semiconductor devices (Ex. 1005, ¶[0004]), Fukunaga does

not explicitly disclose using the interconnect structure in a “computing device.” Park, however, discloses a very similar interconnect structure used in a computing device, and, in my opinion, a person of ordinary skill in the art would have had good reason to use the interconnect structure of the Fukunaga-Park combination discussed above for claim 1 in a “computing device” as disclosed by Park.

100. Park discloses using the interconnect structure in, for example, a cell phone or personal digital assistant (PDA) device 210 shown in figure 10 and a computer system 310 shown in figure 11. (Ex. 1006, ¶¶[0010]-[0011], ¶[0028] (“The packages formed with the interconnect having recessed capping layer of the present invention may be used in a hand-held device 210, such as a cell phone or a personal data assistant (PDA), as shown in FIG. 10.”), ¶[0029] (“The microelectronic device assemblies formed with the adhesion layer of the present invention may also be used in a computer system 310, as shown in FIG. 11.”)⁶, FIGs. 10, 11.)

⁶ I understand that Park’s reference to “the adhesion layer of the present invention” is a typographical error. Based on the surrounding context and the specification of Park as a whole, a person of ordinary skill in the art would have understood Park to be referring to the “interconnects having recessed capping layer of the present invention” being used in a computer system 310.

FIG. 10

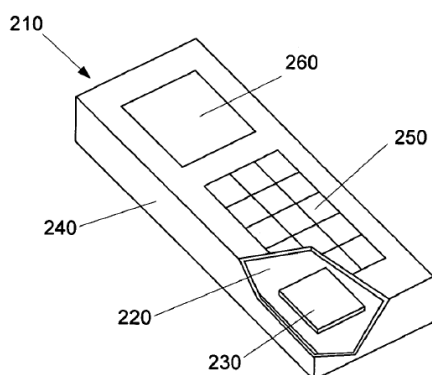
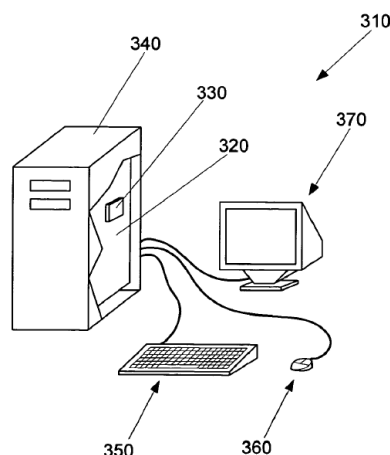


FIG. 11



(*Id.*, FIGs. 10, 11; *see also* my analysis and citations below for the remaining limitations of this claim.)

101. In my opinion, based on Park's disclosure of the use of the interconnect structure in a PDA, cell phone, or computer system, a person of ordinary skill in the art would have had good reason to use the interconnect structure of the Fukunaga-Park combination in a PDA, cell phone, or computer system (each a "computing device"). While Fukunaga does not explicitly disclose the semiconductor devices in which the interconnect structure is used, a person of ordinary skill in the art would have understood that the interconnect structure, which is designed to allow for high-speed propagation of signals on interconnect for semiconductor devices with small-geometry features, is well-suited for use in computing devices like those disclosed by Park. A person of ordinary skill in the art would have been motivated to use the

Fukunaga-Park interconnect structure discussed above for claim 1 in such computing devices as disclosed by Park, as such use would have increased the utility of such an interconnect structure through its implementation in such computing devices and provided the benefit of more reliable operation for the computing devices.

102. Computing devices that include the Fukunaga-Park interconnect structure would have been a predictable combination of known components according to known methods (*e.g.*, applying the teachings of Park regarding using interconnect structures like those of Fukunaga and Park in computing devices), and would have produced the predictable result of a computing device that includes interconnect capping layers on recessed interconnect with the advantages disclosed by Fukunaga and Park.

103. Based on Park's disclosure and their knowledge regarding the use of interconnect structures in computing devices, a person of ordinary skill in the art would have had a reasonable expectation of success in implementing the interconnect structure in such computing devices. Such a skilled person in the art would have understood how to use the interconnect structure to connect different circuit elements within the integrated circuits of the computing devices. Notably, the '183 patent simply identifies various components (*e.g.* processor, memories, etc.) and states that they include "at least one conductive line in a dielectric layer over a substrate, a channel in the dielectric layer over the one conductive line; and a capping

layer on the at least one conductive line in the channel to prevent electromigration, as described herein.” (Ex. 1001, 10:39-52.) The ’183 patent does not provide any more specific implementation details regarding the use of the interconnect in the components, thereby evidencing that a person of ordinary skill in the art would have understood how to, and been able to, successfully incorporate the interconnect structure in such components.

b) “a board;”

104. In my opinion, the Fukunaga-Park combination discloses or suggests this claim feature. For example, Park discloses that each of the PDA, cell phone, and computer system include a substrate or motherboard (“board”) on which integrated circuits are interconnected. (Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an **external substrate 220** with at least one microelectronic device assembly 230, including but not limited to, a central processing units (CPUs), chipsets, memory devices, ASICs, and the like, having at least one recessed capping layer as described above, within a housing 240.”) (emphasis added), ¶[0029] (“The computer system 310 may comprise an **external substrate or motherboard 320** with at least one microelectronic device assembly 330, including but not limited to, a central processing units (CPUs), chipsets, memory devices, ASICs, and the like, having at least one interconnect described above, within a housing or chassis 340.”) (emphasis added).)

FIG. 10

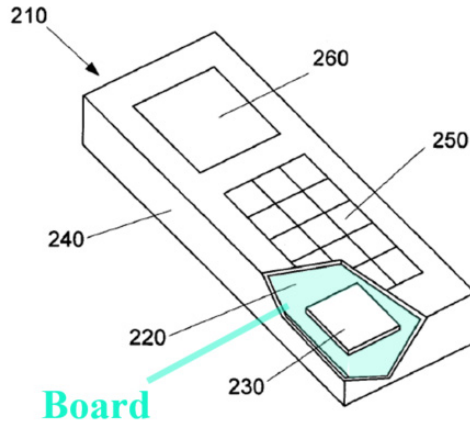
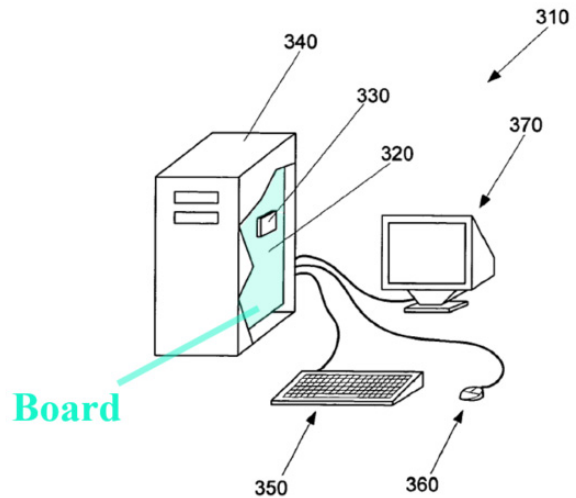


FIG. 11



(*Id.*, FIGs. 10, 11 (annotated).)

- c) “a component coupled to the board, the component including an integrated circuit structure, comprising:”
- d) “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen, and carbon;”
- e) “a conductive structure in the dielectric layer, the conductive structure comprising:”
- f) “a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”
- g) “a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-

planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”

h) “a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”

105. In my opinion, the Fukunaga-Park combination discloses or suggests these features. For example, Park discloses that the boards of the PDA, cell phone, and computer system include a central processing unit (CPU) (“component”), where, as I discuss above in Section IX.8(a), a person of ordinary skill in the art would have been motivated to use the interconnect structure (“integrated circuit structure”) I discuss above for claim 1 in the computing devices disclosed by Park. Therefore, the CPU included in each of the PDA, cell phone, and computer system would include an integrated circuit structure like that discussed above for claim 1. (Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an external substrate 220 with at least one microelectronic device assembly 230, including but not limited to, **a central processing units (CPUs)**, chipsets, memory devices, ASICs, and the like, **having at least one recessed capping layer as described above**, within a housing 240.”) (emphasis added), ¶[0029] (“The computer system 310 may comprise an external substrate or motherboard 320 with at least one microelectronic device assembly 330, including but not limited to, **a central processing units (CPUs)**, chipsets, memory devices, ASICs, and the like, **having at least one interconnect**

described above, within a housing or chassis 340.”) (emphasis added).) The CPU is on the board and therefore “coupled to the board.”

FIG. 10

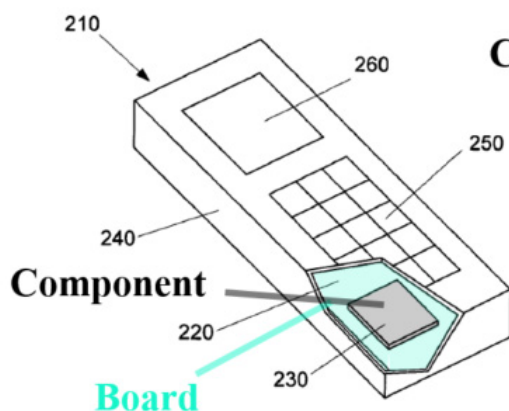
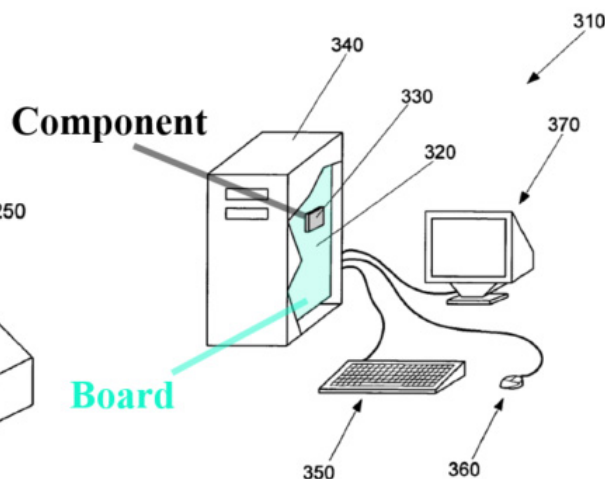


FIG. 11



(*Id.*, FIGs. 10, 11 (annotated).)

106. As I discuss above with respect to claim element 18[a], a person of ordinary skill in the art would have had good reason to use the interconnect structure according to the Fukunaga-Park combination that I discuss above for claim 1 in the integrated circuit structures of the components of the computing devices shown in figures 10 and 11 of Park. (See my discussion above in section IX.A.8(a).) Therefore, the CPU of the computing device, which includes those interconnect structures, includes the “dielectric layer,” the “conductive structure,” the “first conductive material,” the “second conductive material,” and the “barrier layer”

recited in claim elements 18[d]-18[h] for the same reasons I discuss above for claim elements 1[b]-1[f]. (See my discussion above in sections IX.A.1(b)-(f).)

9. Claim 19

“The computing device of claim 18, further comprising:

a memory coupled to the board.”

107. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Park discloses memories coupled to the boards of the computing devices shown in figures 10 and 11. (Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an external substrate 220 with at least one microelectronic device assembly 230, including but not limited to, a central processing units (CPUs), chipsets, **memory devices**, ASICs, and the like, having at least one recessed capping layer as described above, within a housing 240.”) (emphasis added), ¶[0029] (“The computer system 310 may comprise an external substrate or motherboard 320 with at least one microelectronic device assembly 330, including but not limited to, a central processing units (CPUs), chipsets, **memory devices**, ASICs, and the like, having at least one interconnect described above, within a housing or chassis 340.”) (emphasis added).)

10. Claim 20

“The computing device of claim 18, further comprising:

a communication chip coupled to the board.”

108. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, figure 10 of Park shows a “hand-held device 210, such as a cell phone or a personal data assistant (PDA)” that includes multiple components coupled to the substrate 220 (“board”). (Ex. 1006, ¶[0028].) Park does not explicitly disclose that the cell phone or PDA includes a “communication chip” as recited in claim 20, but a person of ordinary skill in the art would have had good reason to include a communication chip in a cell phone or PDA like those disclosed or suggested by the Fukunaga-Park combination. A person of ordinary skill in the art would have known that cell phones and PDAs include communications chips in order to allow the cell phones and PDAs to communicate with other devices that are not physically coupled to the hand held devices. Such devices would use such a communications chip in order to enable Wi-Fi, Bluetooth, and/or cellular radio communications. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in including a communications chip in the Fukunaga-Park device, as the inclusion of such chips on, for example, cell phones was well known and widespread in the industry.

11. Claim 21

“The computing device of claim 18, further comprising:

a camera coupled to the board.”

109. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, figure 10 of Park shows a “hand-held device 210, such as a cell phone or a personal data assistant (PDA)” that includes multiple components coupled to the substrate 220 (“board”). (Ex. 1006, ¶[0028].) Park further discloses that “[t]he external substrate may be attached to various peripheral devices including an input device, such as keypad 250, and a display device, such [as] an LCD display 260.” (*Id.*)

110. Park does not explicitly disclose that the cell phone or PDA includes a “camera” as recited in claim 20, but a person of ordinary skill in the art would have had good reason to include a camera in a cell phone or PDA that includes integrated circuits like those disclosed or suggested by the Fukunaga-Park combination. A person of ordinary skill in the art would have known that cameras were widely used in cell phones long before the earliest possible priority date for the ’183 patent, which is the November 4, 2011 filing date of the ’453 PCT application. Such a skilled person would have been motivated to include a camera on the cell phone disclosed by Park in order to increase the utility of such a cell phone. The camera would have been coupled to the substrate 220 (“board”) of the cell phone in order to allow the

pictures taken by the camera to be stored in memory, viewed on the display, and transferred to other devices from the cell phone. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in including a camera in the Fukunaga-Park device, as the inclusion of such cameras on cell phones was well known and widespread in the industry.

12. Claim 22

“The computing device of claim 18, further comprising:

a battery coupled to the board.”

111. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, figure 10 of Park shows a “hand-held device 210, such as a cell phone or a personal data assistant (PDA)” that includes multiple components coupled to the substrate 220 (“board”). (Ex. 1006, ¶[0028].) Park further discloses that “[t]he external substrate may be attached to various peripheral devices including an input device, such as keypad 250, and a display device, such [as] an LCD display 260.” (*Id.*) Park does not explicitly disclose that the cell phone or PDA includes a “battery” as recited in claim 21, but a person of ordinary skill in the art would have had good reason to include a battery in a cell phone or PDA that includes integrated circuits like those disclosed or suggested by the Fukunaga-Park combination.

112. A person of ordinary skill in the art would have known that batteries were widely used in PDAs and cell phones as they provide power to such devices

that are “hand held” and portable. Thus, a person of ordinary skill in the art would have had a reasonable expectation of success in including a battery in the Fukunaga-Park device. Indeed, a person of ordinary skill in the art would have been motivated to include a battery coupled to the board of the PDAs and cell phones disclosed in Park in order to allow them to operate without being attached to a constant external power source. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in including a battery in the Fukunaga-Park computing device, as the inclusion of such batteries on cell phones was well known and widespread in the industry.

13. Claim 23

“The computing device of claim 18, further comprising:

an antenna coupled to the board.”

113. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, figure 10 of Park shows a “hand-held device 210, such as a cell phone or a personal data assistant (PDA)” that includes multiple components coupled to the substrate 220 (“board”). (Ex. 1006, ¶[0028].) Park further discloses that “[t]he external substrate may be attached to various peripheral devices including an input device, such as keypad 250, and a display device, such [as] an LCD display 260.” (*Id.*) Park does not explicitly disclose that the cell phone or PDA includes an “antenna” as recited in claim 23, but a person of ordinary skill in the art would have

been motivated to include an antenna in a cell phone or PDA that includes integrated circuits like those disclosed or suggested by the Fukunaga-Park combination. A person of ordinary skill in the art would have known that cell phones and PDAs typically include antennas in order to allow the cell phones and PDAs to communicate with other devices that are not physically coupled to the hand held devices. Moreover, a person of ordinary skill in the art would have been motivated to include an antenna in a cell phone or PDA device as disclosed by Park in order to enable Wi-Fi, Bluetooth, and/or cellular radio communications. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in including an antenna in the Fukunaga-Park computing device, as the inclusion of such antennas on cell phones was well known and widespread in the industry.

14. Claim 24

“The computing device of claim 18, wherein the component is a packaged integrated circuit die.

114. In my opinion, the Fukunaga-Park combination discloses or suggests this feature. For example, Park discloses that “[t]he **packages** formed with the interconnects having recessed capping layer of the present invention may be used in a hand-held device 210, such as a cell phone or a personal data assistant (PDA), as shown in FIG. 10.” (Ex. 1006, ¶[0028] (emphasis added); *see also id.*, claim 18 (“at least one **microelectronic device package** attached to said external substrate”) (emphasis added).) A person of ordinary skill in the art would have understood the

CPUs are typically formed on integrated circuit die that are packaged as a part of manufacturing. Therefore, the Fukunaga-Park combination discloses or suggests that the CPU (“component”) coupled to the board of the computing device shown in figure 10 corresponds to a microelectronic device package (“packaged integrated circuit die”). (*Id.*, ¶[0028] (“The hand-held device 210 may comprise an external substrate 220 with at least one microelectronic device assembly 230, including but not limited to, a central processing units (CPUs), chipsets, memory devices, ASICs, and the like, having at least one recessed capping layer as described above, within a housing 240.”).)

15. Claim 25

“The computing device of claim 18, wherein the component is selected from a group consisting of a processor, a communications chip, and a digital signal processor.”

115. In my opinion, the Fukunaga-Park combination discloses or suggests this feature as the “component” I discuss above in claim element 18[c] is a CPU (“processor”). As I discuss above, Park discloses a CPU (“processor”) coupled to the boards of the computing devices shown in figures 10 and 11. (*See* my discussion above in section IX.A.8(c); Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an external substrate 220 with at least one microelectronic device assembly 230, including but not limited to, **a central processing units (CPUs)**, chipsets, memory devices, ASICs, and the like, having at least one recessed capping layer as

described above, within a housing 240.”) (emphasis added), ¶[0029] (“The computer system 310 may comprise an external substrate or motherboard 320 with at least one microelectronic device assembly 330, including but not limited to, **a central processing units (CPUs)**, chipsets, memory devices, ASICs, and the like, having at least one interconnect described above, within a housing or chassis 340.”) (emphasis added).)

B. Fukunaga in Combination with Park and Chan Discloses or Suggests the Features of Claim 10

116. In my opinion, Fukunaga in combination with Park and Chan discloses or suggests all of the features of claim 10 of the ’183 patent.

1. Claim 10

“The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.”

117. As I discuss above in Section IX.A.5, the Fukunaga-Park combination discloses or suggests using a wet etch to recess the interconnects 18 such that their surfaces are lower than the upper surface of the dielectric layer. (*See* my discussion above in section IX.A.5.) I have been asked to assume a scenario in which the Fukunaga-Park combination does not disclose or suggest using a wet etch as recited in claim 10. Under such an assumption, it is my opinion that using such a wet etch

to recess the interconnects 18 in the Fukunaga-Park integrated circuit structure is disclosed or suggested by the Fukunaga-Park combination in further view of Chan.

118. Chan, like Fukunaga and Park, is directed to copper interconnect structures embedded in dielectric material, where a recessed capping layer overlies the copper interconnect. For example, figure 5E of Chan shows copper interconnects 120 formed in trenches of the dielectric layer 82, where cobalt caps 124 cover the top surfaces of the interconnect. (Ex. 1007, ¶[0034] (“FIGS. 5A-5E show cross-sectional views of a portion of wafer 80 during the manufacture of integrated circuits thereon. FIG. 5A shows wafer 80 consisting of a layer of dielectric 82. Trenches 84 are formed in the dielectric 82. The trenches 84 are configured to receive copper interconnects. Although not shown, trenches 84 are lined on the bottom and sides by a thin barrier of metal such as tantalum nitride to prevent copper electromigration.”), ¶[0040] “[T]he cobalt deposited on the exposed surface of the copper interconnects 120 via the electroless plating solution, gradually forms caps 124 shown within FIG. 5E. These caps should cover all exposed surfaces of copper interconnects 120.”)

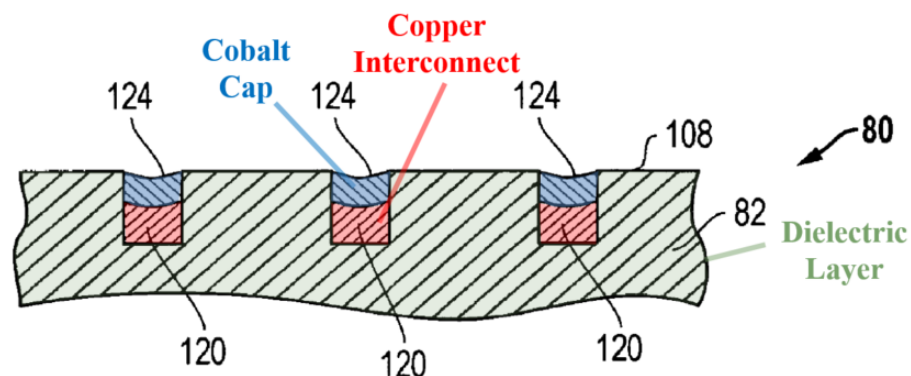


FIG. 5E

(*Id.*, FIG. 5E (annotated).)

119. Like Fukunaga and Park, Chan discloses recessing copper that initially fills the trenches to form recessed interconnects 120 so that the caps are formed in the trench. (*Id.*, ¶¶[0038]-[0039].) Chan discloses that while the copper in the trenches can be recessed by chemical mechanical polishing (CMP), “[t]he recessing effect of chemical-mechanical polishing can vary across the surfaces 22 of copper interconnects 20 as shown in FIG. 1C,” which can result in a dish-like surface. (*Id.*, ¶[0004].) Moreover, Chan also discloses that recesses resulting from CMP are highly dependent on the geometry of the copper interconnects, where the depth of the recess can vary based on pattern density of the interconnect as well as the width of the copper interconnect:

Chemical-mechanical polishing recesses copper interconnects 20 below the surface of dielectric 2 as shown in FIG. 1C. Proper recessing is needed to create effective,

more reliable cobalt caps (e.g., caps 30 in FIG. 1E) on copper interconnects 20. The recesses resulting from chemical-mechanical polishing is highly dependent on the geometry of the copper interconnects. More particularly, the recessing of copper interconnects below the dielectric surface is more dominant in large patterns of copper interconnects than in smaller or more density-packed patterns. In other words, a sufficiently deep recess is created in the copper when the width of the copper interconnect is substantially large and/or when the distance between copper interconnects is substantially large.

The depth of the recess can vary by pattern density. For copper interconnects with small widths or for copper interconnects closely positioned next to each other, the copper interconnect recesses created during chemical-mechanical polishing may not be sufficient.

(*Id.*, ¶¶[0007]-[0008].)

120. Chan further discloses that shallow recesses created by CMP can create problems, including lack of complete coverage for copper interconnects by the overlying cobalt capping layers, which can result in corrosion or other adverse effects. (*Id.*, ¶[0009].) Chan also discloses that using CMP to recess the copper interconnect can also remove portions of the dielectric, which is undesirable. (*Id.*, ¶[0010].)

121. Chan discloses that, rather than using CMP to form or deepen the recesses in the copper interconnects, a wet etch using an acidic solution that does not substantially affect the dielectric layer is used to form or deepen the recesses:

[A]n acidic solution from source 106 is applied to wafer 80 in FIG. 5C. The acidic solution may take from in $\text{HNO}_3/\text{H}_2\text{O}$, $\text{HCL}/\text{KCLO}_3/\text{H}_2\text{O}$, or heated $\text{HCl}/\text{H}_2\text{O}$. Other acidic solutions are contemplated for etching copper interconnects 120. The acidic solution etches the copper interconnects 120, but will not substantially affect the dielectric material 82. Recesses 122 are formed or deepened in the copper interconnects 120 after application of the acidic solution, as shown in FIG. 5D.

(*Id.*, ¶[0038].)

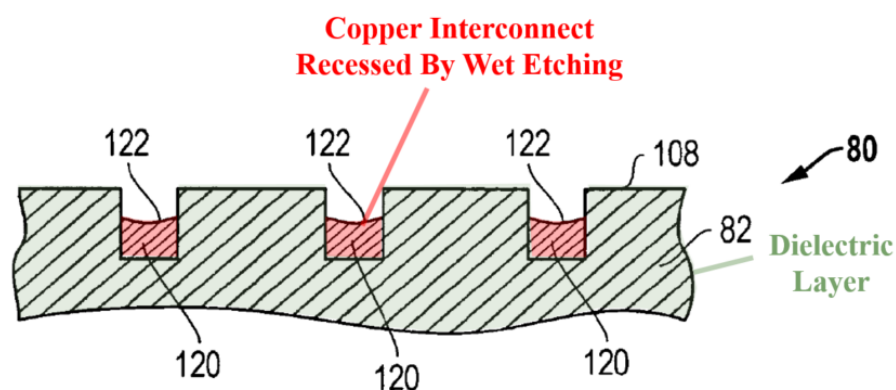


FIG. 5D

(*Id.*, FIG. 5D (annotated).)

122. A person of ordinary skill in the art implementing an interconnect structure like that of the Fukunaga-Park combination would have had good reason

to look to Chan, particularly because all of these references are in the same field and disclose very similar interconnect structures. Having looked to Chan, such a person of ordinary skill in the art would have been motivated to use a wet etch as disclosed by Chan to recess the copper interconnect in the trenches of the Fukunaga-Park combination. As I discuss above, Chan discloses that using wet etching to recess the copper interconnect avoids disadvantages resulting from using CMP for such recessing. Therefore, a person of ordinary skill in the art would have been motivated to use wet etching in the Fukunaga-Park combination to avoid those same disadvantages.

123. Moreover, a person of ordinary skill in the art would have found it straightforward to use wet etching as disclosed by Chan. Such an implementation would have simply been the application of a known method (wet etching to recess the copper interconnect as disclosed by Chan) to a similar device (the interconnect of the Fukunaga-Park combination) and would have produced predictable results (recessed interconnect ready for capping). Moreover, such a skilled person would have had a reasonable expectation of success because Chan discloses using wet etching for a very similar interconnect structure. Therefore, in my opinion, the Fukunaga-Park-Chan combination discloses or suggests claim 10.

C. Fukunaga in Combination with Park and Song Discloses or Suggests the Features of Claims 20-23

124. In my opinion, Fukunaga in combination with Park and Song discloses or suggests all of the features of claims 20-23 of the '183 patent.

1. Claims 20-23

Claim 20: “The computing device of claim 18, further comprising: a communication chip coupled to the board.”

Claim 21: “The computing device of claim 18, further comprising: a camera coupled to the board.”

Claim 22: “The computing device of claim 18, further comprising: a battery coupled to the board.”

Claim 23: “The computing device of claim 18, further comprising: an antenna coupled to the board.”

125. As I discuss above in sections IX.A.10-13, the Fukunaga-Park combination discloses or suggests that the hand-held device (e.g. cell phone or PDA) (“computing device”) includes components coupled to the board (substrate 220), including a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23). (*See* my discussion above sections IX.A.10-13.) I have been asked to assume a scenario in which the Fukunaga-Park combination does not disclose or suggest these features. Under such a scenario, it is my opinion that such features are disclosed or suggested by the Fukunaga-Park combination in further view of Song.

126. Neither Fukunaga nor Park explicitly discloses a cell phone or PDA that includes a communications chip, camera, battery, or antenna, but Song discloses cell phones that include all of the features recited in claims 20-23, and a person of ordinary skill in the art would have had good reasons to implement the cell phone of the Fukunaga-Park combination such that it includes such well-known and widely-used features in further view of Song.

127. For example, Song discloses cell phones that include cameras (claim 21) and batteries (claim 22):

Advances in technology have resulted in smaller and more powerful personal computing devices. For example, there currently exist a variety of portable personal computing devices, including wireless computing devices, such as portable wireless telephones, person digital assistants (PDAs), and paging devices that are small, lightweight, and easily carried by users. More specifically, portable wireless telephones, such as cellular telephones and Internet Protocol (IP) telephones, can communicate voice and data packets over wireless networks. Further, many such wireless telephones include other types of devices that are incorporated therein. For example, a wireless telephone can also include **a digital still camera, a digital video camera**, a digital recorder, and an audio file player. Also, such wireless telephones can process executable instructions, including software applications, such as a

web browser application, that can be used to access the Internet. However, power consumption of such portable devices can quickly deplete a **battery** and diminish a user's experience.

(Ex. 1008, ¶[0002] (emphases added).)

128. Similarly, as shown in annotated figure 7 below, Song discloses a portable device (e.g. cell phone) that includes a wireless controller 740 (“communications chip”) coupled to an antenna 742. (*Id.*, ¶[0016] (“FIG. 7 is a block diagram of a portable device”), ¶[0030] “FIG. 7 also indicates that a wireless controller 740 can be coupled to the digital signal processor 710 and to a wireless antenna.”.) Song further discloses that the wireless controller 740 is included with the other components in box 722 in a “system-in-package” or a “system-on-chip.” Therefore, the wireless controller 740 as a stand-alone chip in the “system-in-package” or the “system-on-chip” that includes the wireless controller 740 is a “communications chip,” as such a chip is coupled to the antenna to support communication using the antenna. (*Id.*, ¶[0030].)

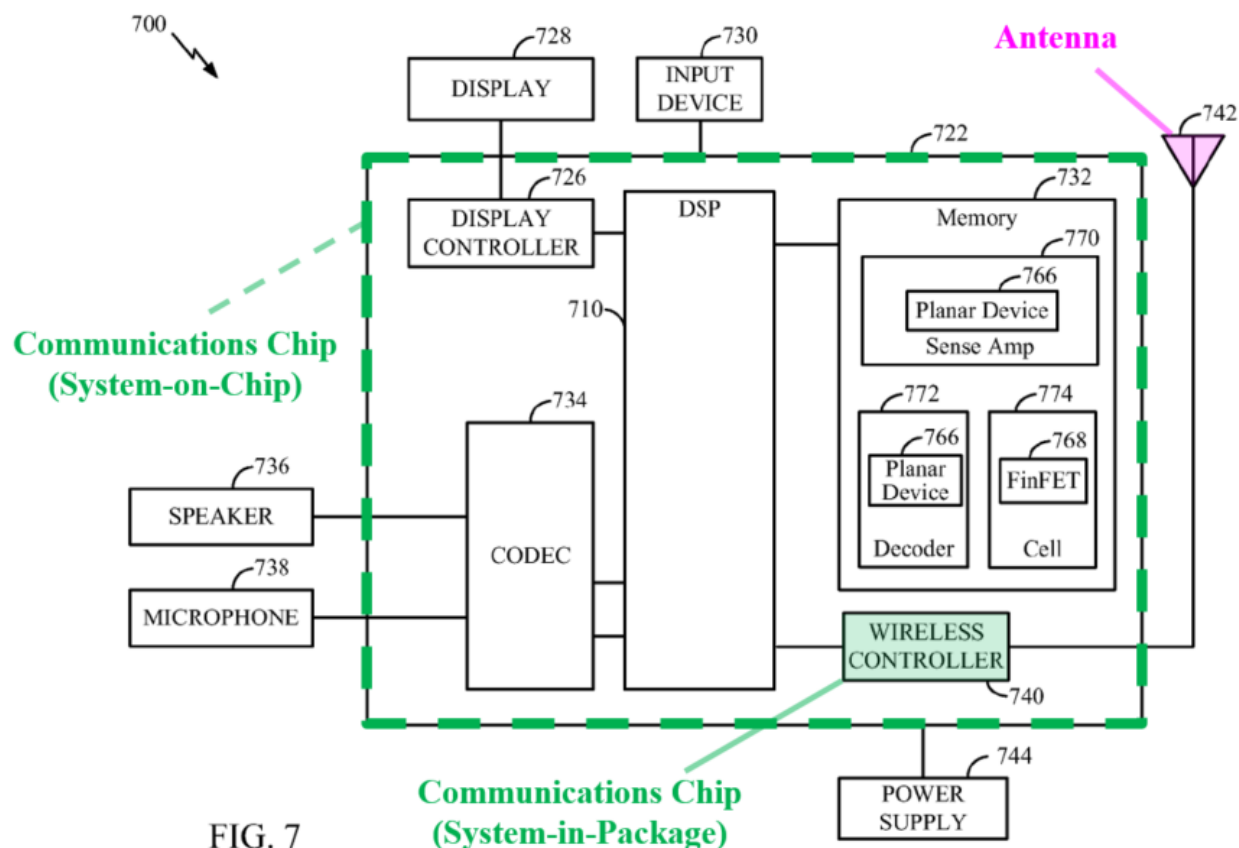


FIG. 7

(*Id.*, FIG. 7 (annotated).)

129. Park does not disclose all of the details regarding the cell phones that incorporate the interconnect structure with capping layer on a recessed conductive line, and therefore a person of ordinary skill in the art would have had good reason to look to Song, which discloses additional details regarding components included in cell phones. In view of Song and their knowledge of state-of-the art cell phone features, such a person of ordinary skill in the art would have been motivated to include a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23) coupled to the board (substrate 220) in the cell phone of

the Fukunaga-Park combination. Such a person of ordinary skill in the art would have been motivated to include such features in order to enable fundamental operational characteristics of the cell phone (communications using the communications chip and antenna powered by the battery) and provide added utility in the form of the ability to take pictures (camera). Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results.

130. As evidenced by Song and the common inclusion of such features in cell phones at the time of the alleged invention, a person of ordinary skill in the art would have had a reasonably likelihood of success in implementing these features in a computing device according to the Fukunaga-Park-Song combination. Notably, the '183 patent does not provide any specific implementation details regarding these components in cell phones, thereby evidencing that a person of ordinary skill in the art would have understood how to, and been able to, successfully incorporate them in a cell phone. For at least these reasons, it is my opinion that the Fukunaga-Park-Song combination discloses or suggests the features of claims 19-23.

D. Kawahara Discloses the Features of Claims 1-9 and 11-17

131. In my opinion, Kawahara discloses all of the features of claims 1-9 and 11-17 of the '183 patent in a manner consistent with Patent Owner's assertions in litigation.

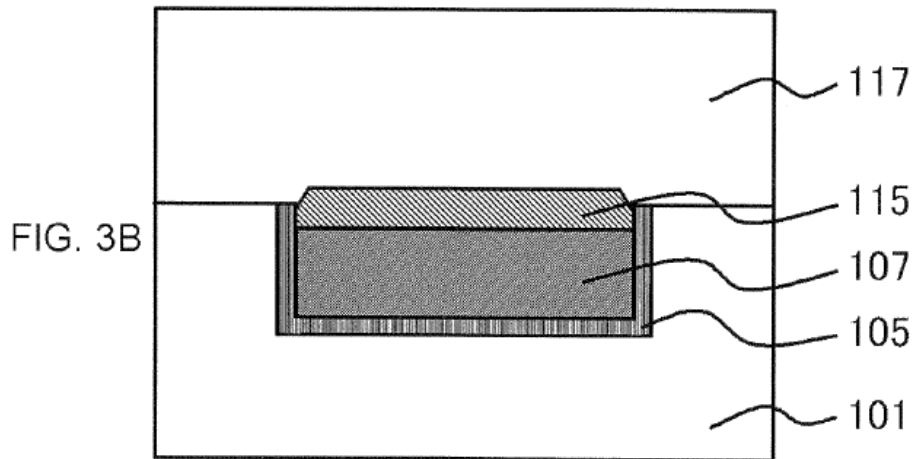
1. Claim 1

a) “An integrated circuit structure, comprising:”

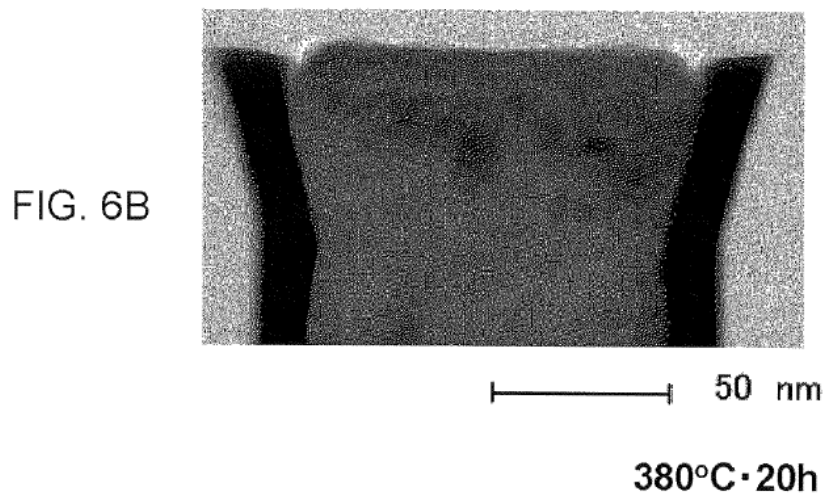
132. I understand that “[a]n integrated circuit structure, comprising” is the preamble to claim 1 of the ’183 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, in my opinion, Kawahara discloses this feature. Kawahara discloses formation of an interconnect structure (“integrated circuit structure”) for semiconductor devices, which are formed on a silicon substrate and include devices such as transistors and via plugs formed on the substrate. (Ex. 1009, 3:1-3 (“According to the present invention, the semiconductor device obtained by employing the above-described method for manufacturing the semiconductor device is presented.”), 6:49-52 (“First of all, as shown in FIG. 2A, the insulating interlayer 101 is formed on the silicon substrate (not shown) having a predetermined device (not shown) such as transistor formed thereon.”), 9:32-33 (“In the present example, a semiconductor device including via plugs and interconnects was manufactured”).)

133. Figures 3B and 6B of Kawahara below show an interconnect structure included as a part of an integrated circuit. (*Id.*, 4:1-3 “FIG. 3A and FIG. 3B are cross-sectional views illustrating a manufacturing process for the semiconductor device shown in FIG. 1.”), 6:45-48 (“FIG. 2A to FIG. 2D, FIG. 3A and FIG. 3B are cross-sectional views, illustrating a manufacturing process for the semiconductor

device 100.”), 9:36-38 (“FIG. 6A and FIG. 6B are cross-sectional views of semiconductor devices, which were obtained in the present example”).)



(*Id.*, FIG. 3B.)

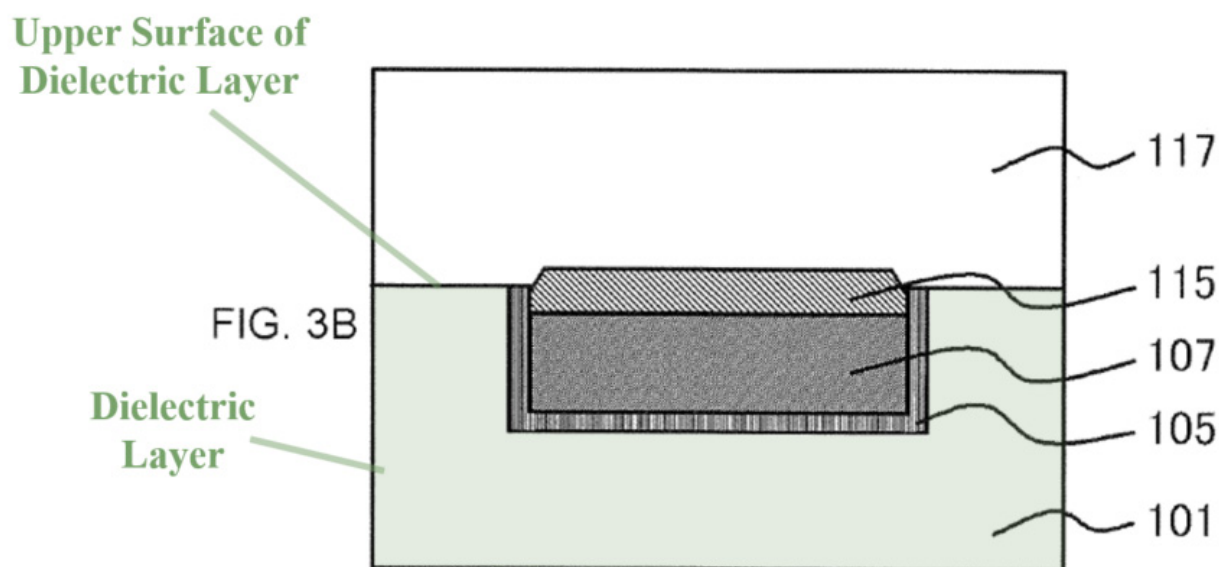


(*Id.*, FIG. 6B.)

- b) “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen and carbon;”

134. In my opinion, Kawahara discloses this claim feature. As shown in annotated figure 3B below, Kawahara discloses that the interconnect structure includes an insulating layer 101 (“dielectric layer”) that has an upper surface. (Ex. 1009, 6:11-17 (“Next a method for manufacturing the semiconductor device 100 will be described. The method for manufacturing the semiconductor device 100 includes, for example, the following process operations: step 11: an insulating film (insulating layer 101) is formed on a substrate such as a semiconductor substrate (not shown);”), 6:49-52 (“First of all, as shown in FIG. 2A, the insulating interlayer 101 is formed on the silicon substrate (not shown) having a predetermined device (not shown) such as transistor formed thereon.”).)

135. Kawahara further discloses forming the insulating interlayer 101 as a low dielectric constant insulating film (“dielectric layer”) of silicon oxycarbide (SiOC) film that includes silicon (Si), oxygen (O), and carbon (C), as claimed. (*Id.*, 5:16-22 (“Each of the insulating interlayer 101, the insulating interlayer 117, the insulating interlayer 123 and the insulating interlayer 131 may be a single layer film or a multiple-layered film. Materials for these insulating interlayers may be, for example, silicon dioxide (SiO₂) film. Further, the insulating interlayer may be a low dielectric constant insulating film such as silicon oxycarbide (SiOC) film.”).)

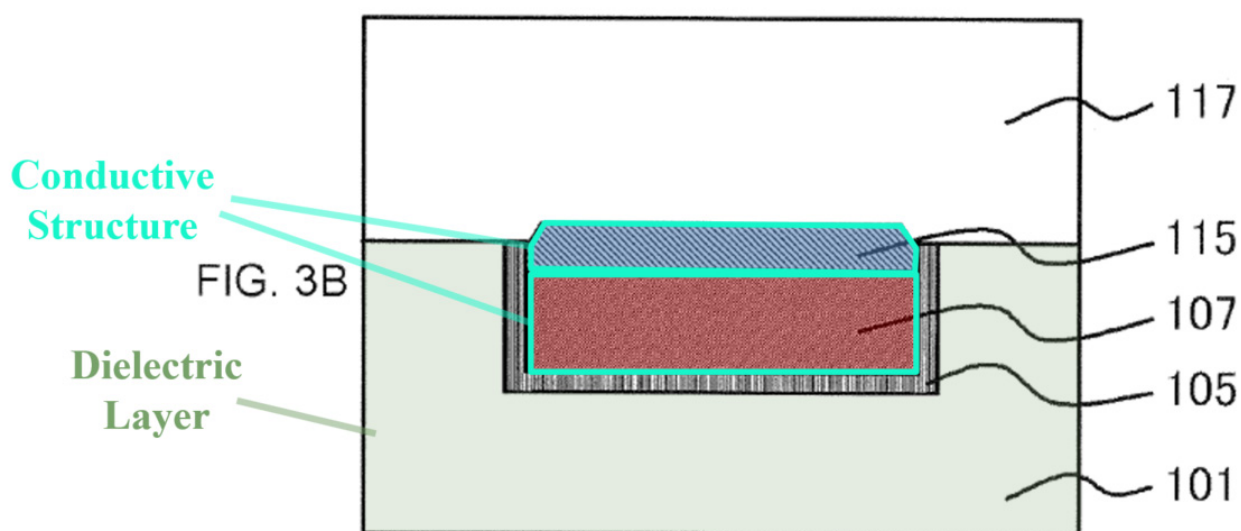


(*Id.*, FIG. 3B (annotated).)

c) **“a conductive structure in the dielectric layer, the conductive structure comprising:”**

136. In my opinion, Kawahara discloses this feature. For example, as shown in annotated figure 3B below, Kawahara discloses a conductive structure in the concave portion of the dielectric layer 101, where the conductive structure includes copper interconnect 107 and electrically conducting protective film 115. (Ex. 1009, 4:43-51 (“a metal film composed of copper (lower layer copper interconnect 107) provided so as to be in contact with the barrier metal film 105 and buried in the interior of the concave portion 103, and an electrically conducting film (protective film 115) provided so as to be in contact with the upper portion of the lower layer copper interconnect 107 and also provided over substantially the entire top surface

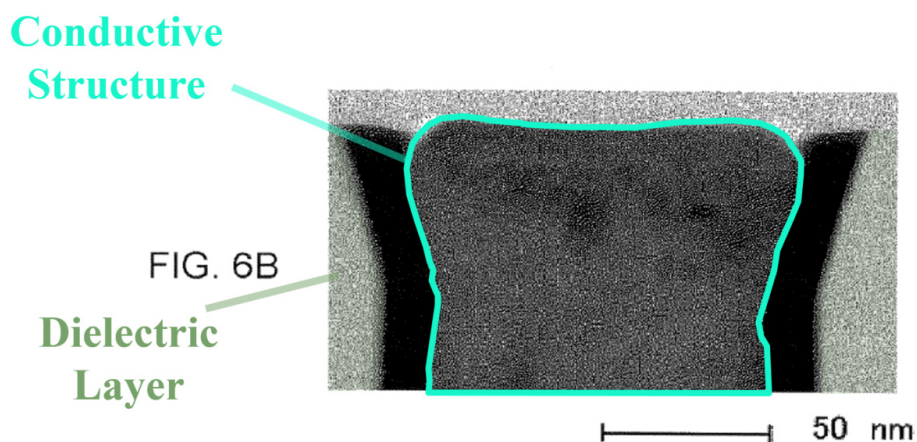
of the lower layer copper interconnect 107.”), 6:62-64 (“selectively forming a lower layer copper interconnect 107 composed of the Cu film 106 within the concave portion 103.”); 7:6-9 (“a COWB film is grown as the cap metal film 111 from the upper surface of the lower layer copper interconnect 107 by a selective plating process such as an electroless plating process and the like.”)⁷.)



(*Id.*, FIG. 3B (annotated).)

137. The conductive structure is also highlighted in annotated figure 6B below.

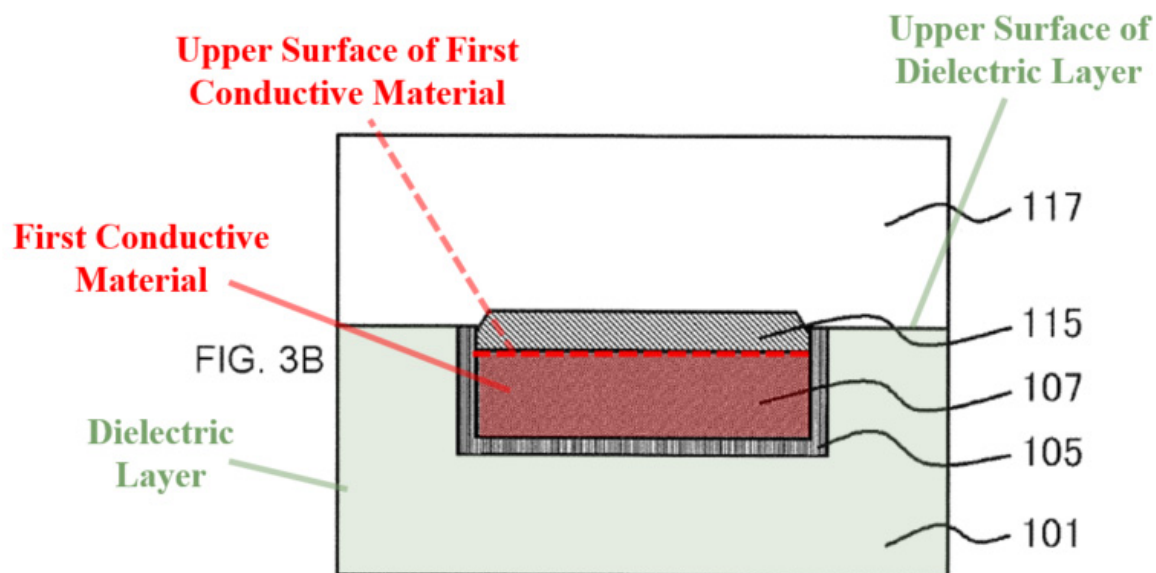
⁷ A person of ordinary skill in the art would have understood that Kawahara's references to COWB film are to cobalt (Co), tungsten (W), boride (B) film (CoWB). (Ex. 1009, 5:55-56.)



(*Id.*, FIG. 6B (annotated).)

- d) **“a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”**

138. Kawahara discloses this feature. For example, as shown in annotated figure 3B below, the lower layer copper interconnect 107 (“first conductive material”) has an upper surface, where a portion of the upper surface is below a portion of the upper surface of the dielectric layer. (Ex. 1009, 4:43-46 (“a metal film composed of copper (lower layer copper interconnect 107) provided so as to be in contact with the barrier metal film 105 and buried in the interior of the concave portion 103”), 6:62-64 (“selectively forming a lower layer copper interconnect 107 composed of the Cu film 106 within the concave portion 103.”).)



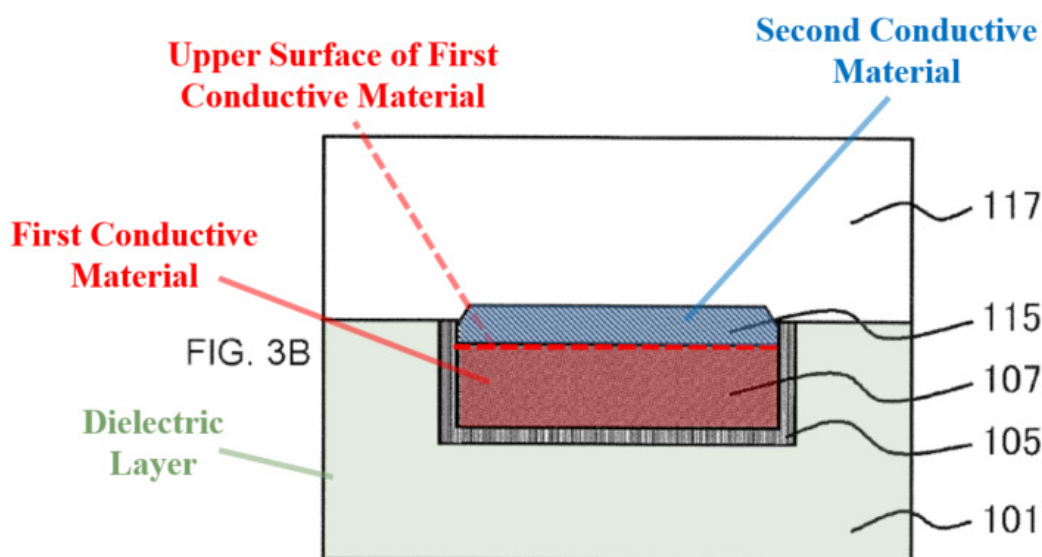
(*Id.* at FIG. 3B (annotated).)

139. Kawahara discloses that the copper interconnect 107 is recessed in order to allow the cap metal film 111 to be formed on the surface of the interconnect 107 (thereby forming the electrically conducting protective film 115) while not extending “from the top of the concave portion 103 beyond the region for forming the barrier metal film 105 considerably exceeding the top of the insulating film 101, or from being considerably swelled to form a mushroom-shape.” (*Id.*, 8:40-52; *see also id.*, 6:64-7:3 (“At this time, the upper surface of the lower layer copper interconnect 107 is retracted to be closer to the substrate than the upper surface of the insulating layer 101 to form a stepper portion 109 (FIG. 2C). A height of the stepper portion 109 may be selected to be sufficiently larger to avoid a formation of the cap metal film 111 outside of the desired region, and may be for example about

70 to 80 nm.”).) Therefore, in my opinion, Kawahara discloses the first conductive material as recited in claim element 1[d]

- e) **“a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially coplanar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”**

140. As shown in annotated figure 3B below, Kawahara discloses forming the protective film 115 (“second conductive material”) on the upper surface of the first conductive material. (Ex. 1009, 7:6-9 (“a COWP film is grown as the cap metal film 111 from the upper surface of the lower layer copper interconnect 107 by a selective plating process such as an electroless plating process and the like.”).)



(*Id.*, FIG. 3B (annotated).)

141. Kawahara further discloses that the protective film 115 (“second conductive material”) includes cobalt:

The protective film 115 and the protective film 129 contain for example, one or more element selected from Co and Ni and one or more element selected from tungsten (W) and phosphorus (P) and boron (B) as constituent element, and more specifically, is composed of one or more electrically conducting films selected from a group consisting of cobalt tungsten phosphide (CoWP) film cobalt tungsten boride (COWB) film, nickel tungsten phosphide (NiWP) film and nickel tungsten boride (NiWB) film.

(*Id.*, 5:50-60; *see also id.*, 7:4-9, 8:1-4.)

142. Kawahara discloses that the protective film 115 (“second conductive material”) covers the “entire upper surface” of the copper interconnect 107 (“first conductive material”), and therefore the first and second conductive materials, which are both contained by the concave portion of the dielectric layer 101, have the same width at the location where they meet:

In order to prevent deterioration in reliability of the metal film composed of copper such as electro-migration (EM), stress induced void (SIV) and the like, it is necessary to ensure the entire surface of the metal film composed of copper to be coated with a cap metal film. For such purpose, it should be designed that the cap metal film covers the metal film composed of copper, even in the inner surface of the barrier metal film, on which the cap metal film is difficult to be formed.

The present inventors therefore have eagerly carried out further investigation based on the above-described scientific knowledge for sufficiently covering the entire upper surface of the metal film composed of copper with a material that composes the cap metal film even if the recessed structure is adopted, and have eventually achieved the present invention.

(*Id.*, 2:1-14.)

Then, as shown in FIG. 3A, the silicon substrate (not shown) having the cap metal film 111 formed thereon is

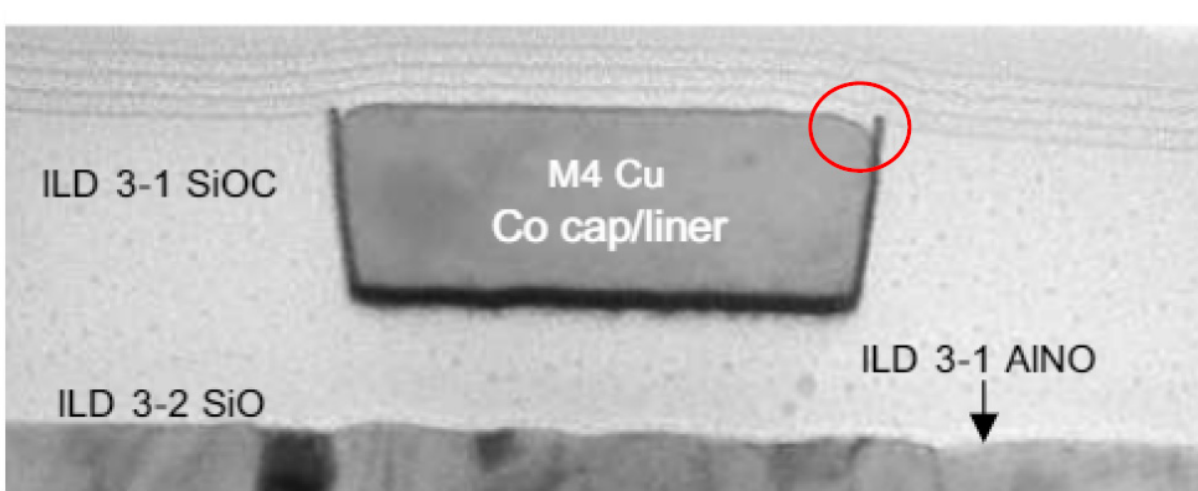
heat-treated at a specific process condition, so that a migration of the constituent material of the cap metal film 111 into the gap 113 is carried out to broaden the cap metal film 111 to the entire upper surface of the lower layer copper interconnect 107, thereby forming the protective film 115.

(*Id.*, 7:15-21.)

Further, since the cap metal film 111 is formed on the lower layer copper interconnect 107 having the stepped portion 109 formed therein by a selective plating process in the present embodiment, the cap metal film 111 is not formed in the vicinity of the side wall of the barrier metal film 105, whereby remaining the gap 113. To solve the problem, after the cap metal film 111 is formed, the constituent material of the cap metal film 111 is migrated to the gap 113 to broaden the cap metal film 111, so that the protective film 115 is formed on the entire upper surface of the lower layer copper interconnect 107. Having this configuration, the upper surface of the lower layer copper interconnect 107 is ensured to be covered with the protective film 115 even if the formation of the cap metal film 111 creates the gap 113 remained therein, so that a generation of electro migration (EM) of copper or a generation of a stress induced void (SIV) in vicinity of the gap 113 can be reduced.

(*Id.*, 8:56-9:5.)

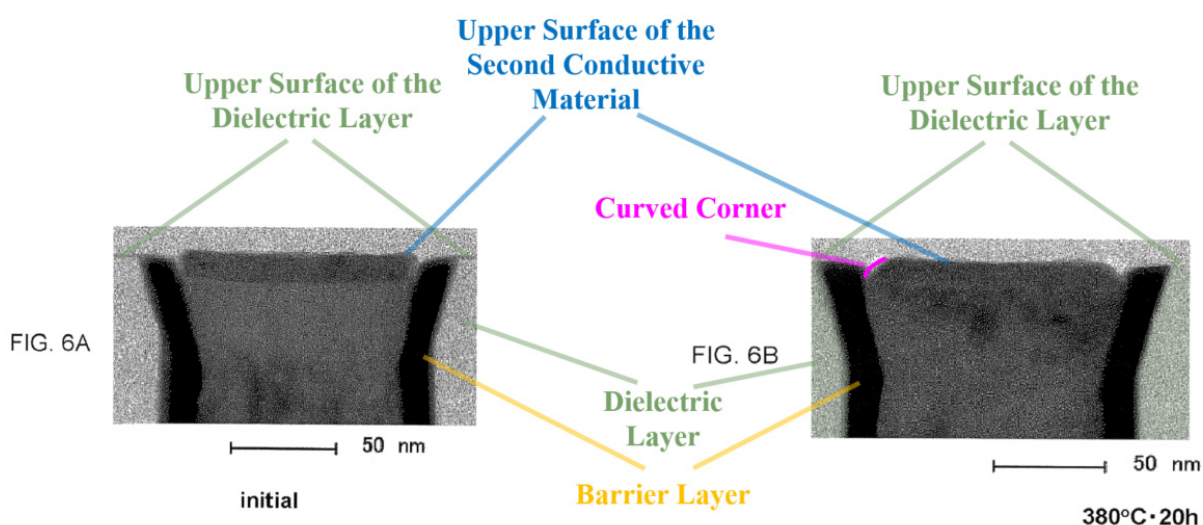
143. I have been informed that, in district court, Patent Owner alleges that a the “the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer” features are met based on the following image depicting interconnect in a certain product. For example, I have been informed that Patent Owner asserts that the divot in the interconnect material within the red circle in the image below forms a “curved corner” as recited in claim 1.



144. I have been asked to apply Patent Owner’s interpretation of the “the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer” terms recited in claim element

1[e] in my analysis herein. It is my opinion that, under Patent Owner's interpretation of this claim element, Kawahara discloses these features.

145. As shown in annotated figures 6A and 6B below, and consistent with what I understand are Patent Owner's assertions in district court, Kawahara discloses that "the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer." Figures 6A and 6B include a divot below the upper surface of the dielectric layer in the same manner as the image of the accused product above such that figures 6A and 6B include a "curved corner" in the same manner as that product.



(Ex. 1009, FIGs. 6A, 6B (annotated).)

146. Kawahara discloses that the copper interconnect 107 is recessed in order to allow the cap metal film 111 to be formed on the surface of the interconnect 107 while not extending “from the top of the concave portion 103 beyond the region for forming the barrier metal film 105 **considerably exceeding the top of the insulating film 101**, or from being considerably swelled to form a mushroom-shape.” (*Id.*, 8:40-52 (emphasis added); *see also id.*, 6:64-7:3 (“At this time, the upper surface of the lower layer copper interconnect 107 is retracted to be closer to the substrate than the upper surface of the insulating layer 101 to form a stepper portion 109 (FIG. 2C). **A height of the stepper portion 109 may be selected to be sufficiently larger to avoid a formation of the cap metal film 111 outside of the desired region**, and may be for example about 70 to 80 nm.”).)⁸

147. Therefore, Kawahara discloses that by recessing the interconnect on which the cap metal film is formed, the cap metal film is formed so that an unwanted extension of the cap metal film can be avoided. (*Id.*, 1:46-56.) For at least these

⁸ While Kawahara discloses an example height of the stepper portion 109 (i.e., the gap left by recessing the interconnect 107) of 80 nm and an example thickness of the protective film 115 of about 120 nm, such thicknesses are only examples presented and a person of ordinary skill in the art would not understand them to be limiting.

reasons, it is my opinion that Kawahara discloses claim element 1[e] in a manner consistent with what I understand to be Patent Owner's assertions in district court.

f) **“a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”**

148. In my opinion, Kawahara discloses this feature. For example, Kawahara discloses forming a tantalum nitride (TaN) barrier metal film 105 (“barrier layer”) covering the inner wall of the concave portion 103, where the copper interconnect 107 (“first conductive material”) and protective film 115 (“second conductive material”) included in the conductive structure are formed within the concave portion 103 such that the barrier layer 105 partially surrounds the conductive structure:

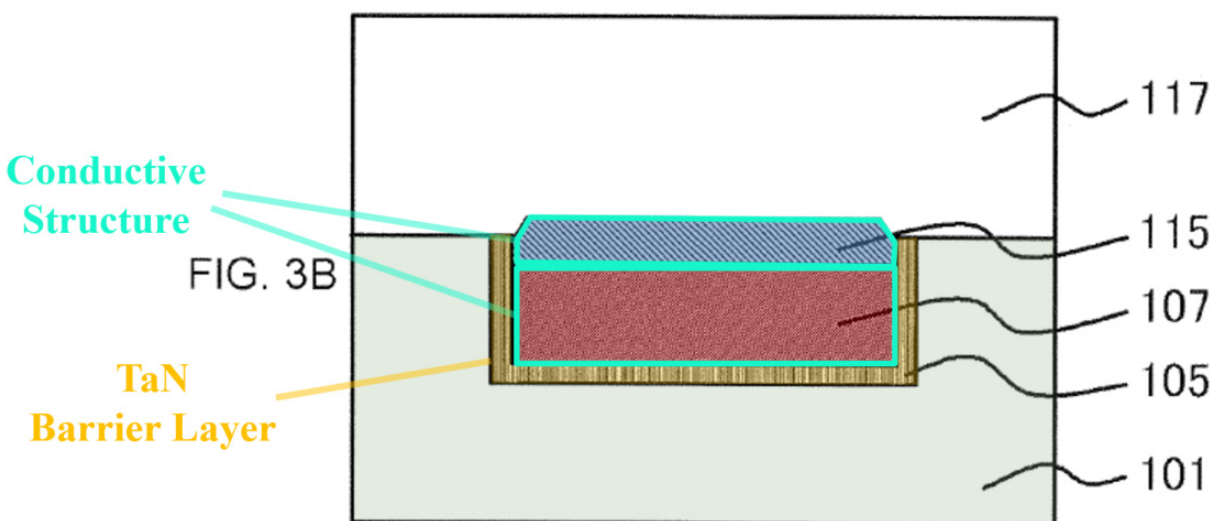
A semiconductor device 100 shown in FIG. 1 includes an insulating film (insulating interlayer 101) formed above a substrate such as a semiconductor substrate, specifically a silicon substrate, and the like (not shown) and provided with a concave portion 103 in a certain location, a barrier metal film 105 covering an inner wall of the concave portion 103, a metal film composed of copper (lower layer copper interconnect 107) provided so as to be in contact with the barrier metal film 105 and buried in the interior of the concave portion 103, and an electrically conducting film (protective film 115) provided so as to be in contact with the upper portion of the lower

layer copper interconnect 107 and also provided over substantially the entire top surface of the lower layer copper interconnect 107.

An upper surface of the lower layer copper interconnect 107 is provided so as to be retracted to be closer to the substrate than an upper end of the **barrier metal film 105 such as tantalum nitride (TaN) film** functioning as a diffusion barrier film for copper (Cu), or in other words than an upper surface of barrier metal film 105 that covers the side wall of the concave portion 103.

(Ex. 1009, 4:38-59.)

149. While what constitutes “partially surrounding” is unclear, I have been asked to assume that a barrier layer that is in contact with the conductive structure and surrounds the conductive structure on three sides satisfies this limitation. As shown in annotated figure 3B below, the TaN barrier layer 105, partially surrounds the conductive structure that includes the interconnect 107 and protective film 115.



(*Id.*, FIG. 3B (annotated).)

2. Claim 2

“The integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.”

150. In my opinion, Kawahara discloses this feature. Kawahara discloses a barrier metal film 105 (“barrier layer”) formed of tantalum nitride (TaN), which includes tantalum and nitrogen. (Ex. 1009, 4:54-55 (“barrier metal film 105 such as tantalum nitride (TaN) film”) (emphasis added).)

3. Claims 3-8

Claim 3: “The integrated circuit structure of claim 1, wherein the second conductive material further comprises boron.”

Claim 4: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises phosphorus.”

Claim 5: “The integrated circuit structure of claim 3,

wherein the second conductive material further comprises tungsten.”

Claim 6: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten and phosphorus.”

Claim 7: “The integrated circuit structure of claim 1, wherein the second conductive material further comprises phosphorus.”

151. In my opinion, Kawahara discloses these features. Claims 3-8 recite various cobalt-containing alloys used for the second conductive material, which corresponds to the protective film 115 that serves as a capping layer in Kawahara. Specifically, claims 3-8 specify that the second conductive material includes cobalt and one or more of boron, phosphorus, and tungsten, and Kawahara discloses such alloys for the protective film 115 (“second conductive material”):

The protective film 115 and the protective film 129 contain for example, **one or more element selected from Co and Ni and one or more element selected from tungsten (W) and phosphorus (P) and boron (B)** as constituent element, and more specifically, is composed of one or more electrically conducting films selected from a group consisting of cobalt tungsten phosphide (CoWP) film cobalt tungsten boride (COWB) film, nickel tungsten phosphide (NiWP) film and nickel tungsten boride (NiWB) film.

(Ex. 1009, 5:50-60.)

152. Because Kawahara discloses that the protective film includes “one or more” of cobalt (Co) and nickel (Ni) as well as “one or more” of tungsten (W), phosphorus (P), and boron (B), Kawahara discloses the second conductive material includes Co and B (claim 3), Co, B, and P (claim 4), Co, B, and W (claim 5), Co, B, W, and P (claim 6), Co and P (claim 7), and Co, P, and W (claim 8). Therefore, Kawahara discloses that the second conductive material includes cobalt as well as boron, phosphorus, and tungsten in the various combinations recited in claims 3-8.

4. Claim 9

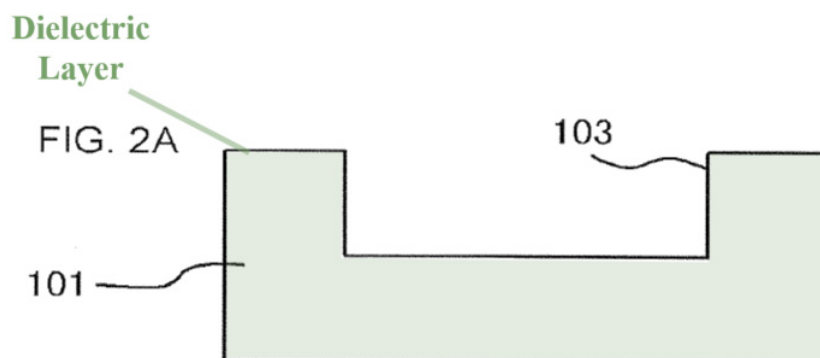
a) “A method of fabricating an integrated circuit structure, the method comprising:”

153. I understand that a “method of fabricating an integrated circuit structure, the method comprising” is the preamble to claim 9 of the '183 patent. I have been asked to assume that the preamble is a claim limitation. Under that assumption, it is my opinion that Kawahara discloses a “method of fabricating an integrated circuit structure.” For example, Kawahara discloses “a method for manufacturing the semiconductor device 100,” where, as I discuss above for claim element 1[a], Kawahara discloses formation of an interconnect structure (“integrated circuit structure”) for semiconductor devices, which are formed on a silicon substrate and include devices such as transistors and via plugs formed on the substrate. (Ex. 1009, 6:11-14, 3:1-3 (“According to the present invention, the semiconductor device

obtained by employing the above-described method for manufacturing the semiconductor device is presented.”); *see* my discussion above in section IX.D.1(a).)

b) “forming a dielectric layer comprising silicon, oxygen and carbon;”

154. In my opinion, Kawahara discloses this claim feature. For example, as shown in annotated figure 2A below, Kawahara discloses “the insulating interlayer 101 is formed on the silicon substrate.”) (Ex. 1009, 6:49-50; *see also id.*, 6:15-16 “an insulting film (insulating layer 101) is formed on a substrate such as a semiconductor substrate.”).)



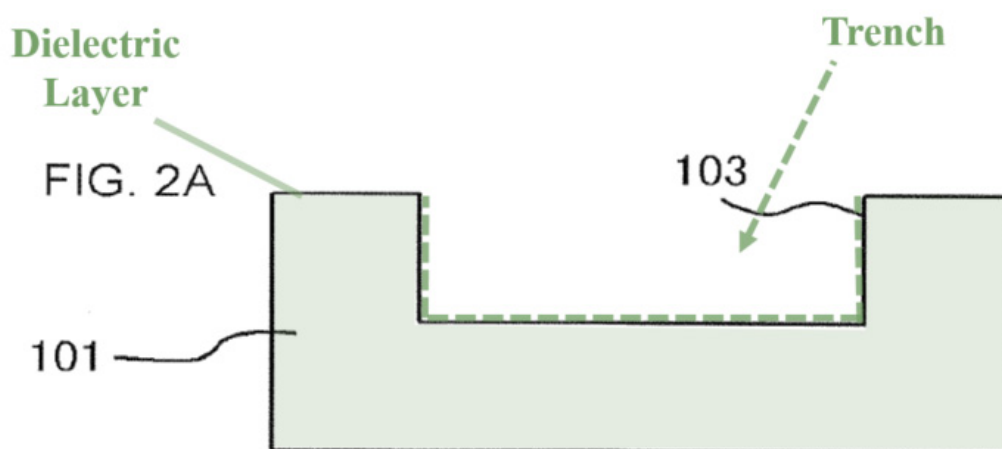
(*Id.*, FIG. 2A (annotated).)

155. Kawhara further discloses forming the insulating interlayer 101 as a low dielectric constant insulating film (“dielectric layer”) of silicon oxycarbide (SiOC) film that includes silicon (Si), oxygen (O), and carbon (C). (*Id.*, 5:16-22 (“Each of the insulating interlayer 101, the insulating interlayer 117, the insulating interlayer 123 and the insulating interlayer 131 may be a single layer film or a

multiple-layered film. Materials for these insulating interlayers may be, for example, silicon dioxide (SiO_2) film. Further, the insulating interlayer may be a low dielectric constant insulating film such as silicon oxycarbide (SiOC) film.”)

c) “forming a trench in the dielectric layer;”

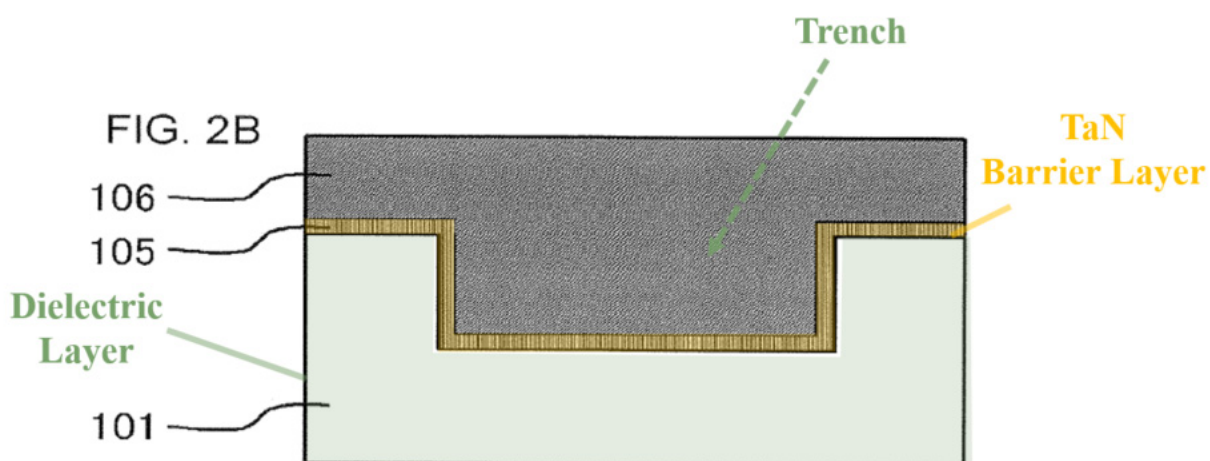
156. In my opinion, Kawahara discloses this claim feature. For example, as shown in annotated figure 2A below, after forming the insulating interlayer 101 (“dielectric layer”), Kawahara discloses etching away portions of the dielectric layer to form a concave portion 103 (“trench”) in that layer. (Ex. 1009, 6:52-54 (“Then, portions of the insulating interlayer 101 in the region for forming the lower layer copper interconnect 107 is selectively etched off to form the concave portion 103.”), 6:18-19 “step 12: the insulating interlayer 101 is selectively removed to form a concave portion 103”).)



(*Id.*, FIG. 2A (annotated).)

d) “forming a barrier layer in the trench, the barrier layer comprising tantalum;”

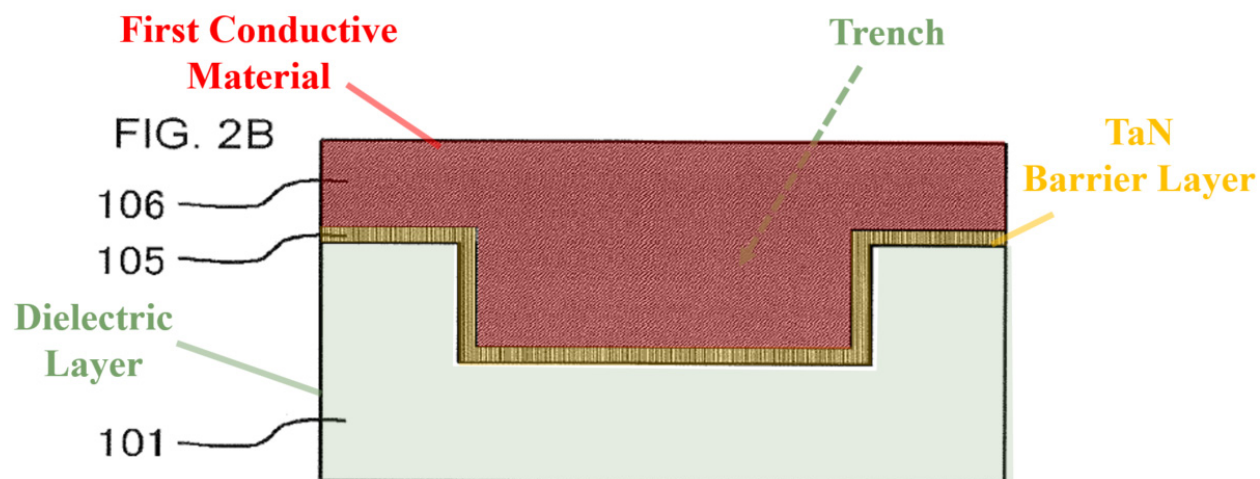
157. In my opinion, Kawahara discloses this claim feature. For example, as shown in annotated figure 2B below, after forming the trench in the insulating interlayer 101 (“dielectric layer”), Kawahara discloses forming barrier metal film 105, which includes tantalum, in the trench. (Ex. 1009, 6:55-56 (“Next, as shown in FIG. 2B, the barrier metal film 105 is deposited on the insulating interlayer 101...”), 6:20-22 “step 13: a barrier metal film 105 that covers an inner wall of the concave portion 103 is formed on the insulating interlayer 101 having the concave portion 103 formed thereon”), 4:54-55 (“barrier metal film 105 such as tantalum nitride (TaN) film”).)



(*Id.*, FIG. 2B (annotated).)

- e) **“forming a first conductive material within the barrier layer, the first conductive material comprising copper;”**

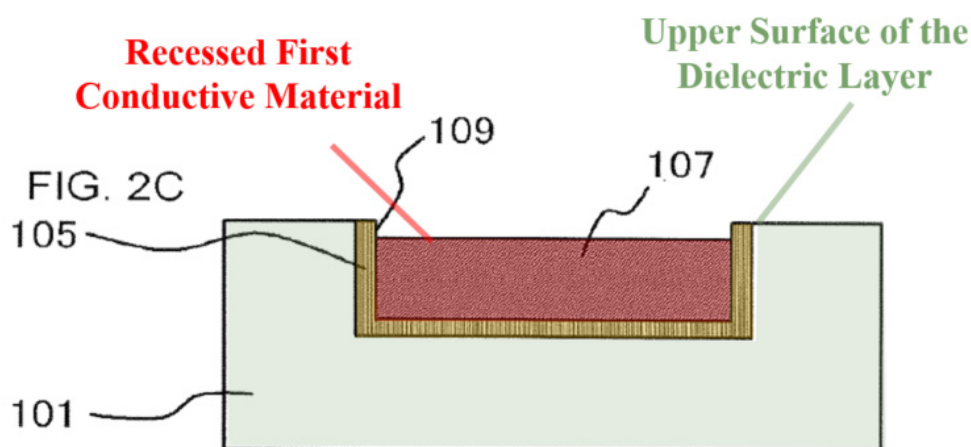
158. In my opinion, Kawahara discloses this claim feature. For example, as shown in annotated figure 2B below, after forming the barrier layer in the trench, Kawahara discloses forming copper film 106 (“first conductive material”) in the lined trench (“within the barrier layer”). (Ex. 1009, 6:56-57 (“[T]hen the Cu film 106 is formed so as to plug the concave portion 103....”), 6:23-26 (“step 14: a metal film composed of copper (Cu film 106 of FIG. 2B) is formed on the insulating interlayer 101 having the barrier metal film 105 formed thereon so as to plug the concave portion 103”).)



(*Id.*, FIG. 2B (annotated).)

f) “recessing the first conductive material below a portion of an upper surface of the dielectric layer; and”

159. In my opinion, Kawahara discloses this claim feature. For example, as shown in annotated figure 2C below, Kawahara discloses that, after removing portions of the barrier layer and copper film using chemical mechanical polishing (CMP), “the upper surface of the lower layer of copper interconnect 107 is retracted [“recessed”] to be closer to the substrate than the upper surface of the insulating interlayer 101 to form a stepper portion 102 (FIG. 2C).” (Ex. 1009, 6:58-67; *see also id.*, 6:27-33 (“Step 15: portions of the Cu film 106 and the barrier metal film 105 formed outside of the concave portion 103 are removed and the upper surface of Cu film 106 is retracted to be closer to the substrate than the upper surface of the barrier metal film 105 on the side wall of the concave portion 103, so as to form a lower layer copper interconnect 107 composed of the Cu film 106”).)



(*Id.*, FIG. 2C (annotated).)

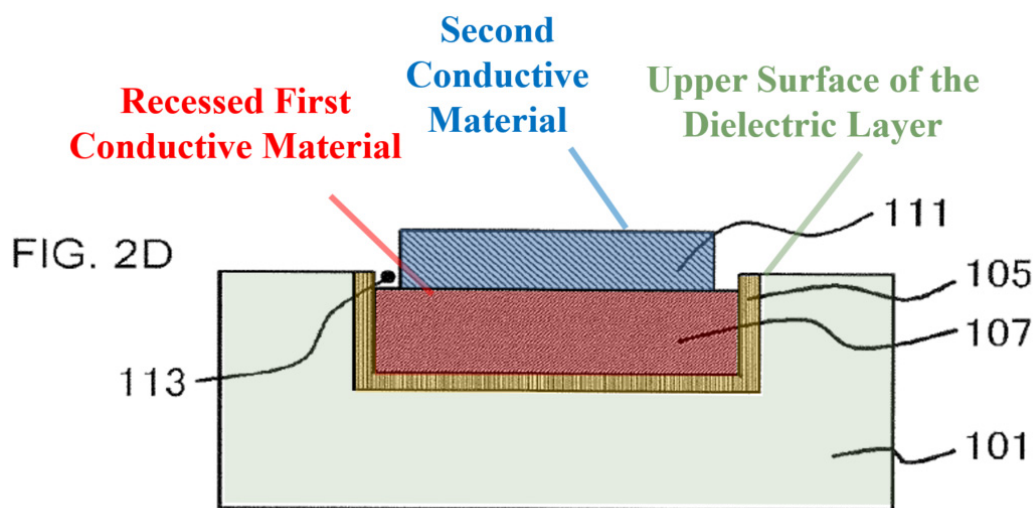
- g) “forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a position where the first conductive material and the second conductive material meet, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer.”**

160. In my opinion, Kawahara discloses this feature in a manner consistent with what I understand to be Patent Owner’s assertions in litigation, for reasons similar to those I discuss above with respect to claim element 1[g]. (See my discussion above in section (IX.D.1(g).) For example, as shown in annotated figure 2D below, Kawahara discloses that, after recessing the interconnect 107 (“first conductive material”), metal film 111 (“second conductive material”) is grown on the surface of the interconnect 107:

Subsequently, as shown in FIG. 2D, a gap 113 is formed between the side wall of the barrier metal film 105 and the cap metal film 111, while a COWP film is grown as the cap metal film 111 from the upper surface of the lower layer copper interconnect 10 by a selective plating process such as an electroless plating process and the like.

(Ex. 1009, 7:4-9; *see also id.*, 6:34-38 (“step 16: after the operation of retracting the Cu film 106 (step 15) a cap metal film 111 is formed on the lower layer copper

interconnect 107 while a spacing (gap 113) is remained on the lower layer copper interconnect 107 in vicinity of the side wall of the barrier metal film 105”).)



(*Id.*, FIG. 2D (annotated).)

161. Kawahara further discloses that after forming the metal film 111, the substrate is heat treated to cause the migration of the metal film into the gap 113 so that the entire upper surface of the lower layer interconnect is covered:

Then, as shown in FIG. 3A, the silicon substrate (not shown) having the cap metal film 111 formed thereon is heat-treated at a specified process condition, so that a migration of the constituent material of the cap metal film 11 into the gap 113 is carried out to broaden the cap metal film 111 to the entire upper surface of the lower layer copper interconnect 107, thereby forming the protective film 115.

(*Id.*, 7:15-21; *see also id.*, 6:39-43 (“step 17: a migration of a constituent material of the cap metal film 111 into the gap 113 is caused to broaden the cap metal film 111, thereby forming an electrically conducting film surface of the lower layer copper interconnect 107.”))

162. As I discuss above for claim element 1[e], Kawahara discloses, in what I understand to be a manner consistent with Patent Owner’s assertions in litigation, that the metal cap metal film 111 (“second conductive material”) (1) is on the upper surface of the recessed first conductive material, (2) comprises cobalt, (3) has the same width at a position where the second conductive material meets the first conductive material, and (4) has a curved corner below the portion of the upper surface of the dielectric layer. (*See my discussion above in section IX.D.1(e).*)

5. Claim 11

“The method of claim 9, wherein the barrier layer further comprises nitrogen.”

163. In my opinion, Kawahara discloses this feature for the same reasons I discuss above with respect to claim 2. (*See my discussion above in section IX.D.2.*)

6. Claims 12-17

Claim 12: “The integrated circuit structure of claim 9, wherein the second conductive material further comprises boron.”

Claim 13: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises phosphorus.”

Claim 14: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises tungsten.”

Claim 15: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises tungsten and phosphorus.”

Claim 16: “The integrated circuit structure of claim 9, wherein the second conductive material further comprises phosphorus.”

Claim 17: “The integrated circuit structure of claim 16, wherein the second conductive material further comprises tungsten.”

164. In my opinion, the Kawahara discloses these features for the same reasons I discuss above with respect to claims 3-8. (*See my discussion above in section IX.D.3.*)

E. Kawahara in Combination with Chan Discloses or Suggests the Features of Claim 10

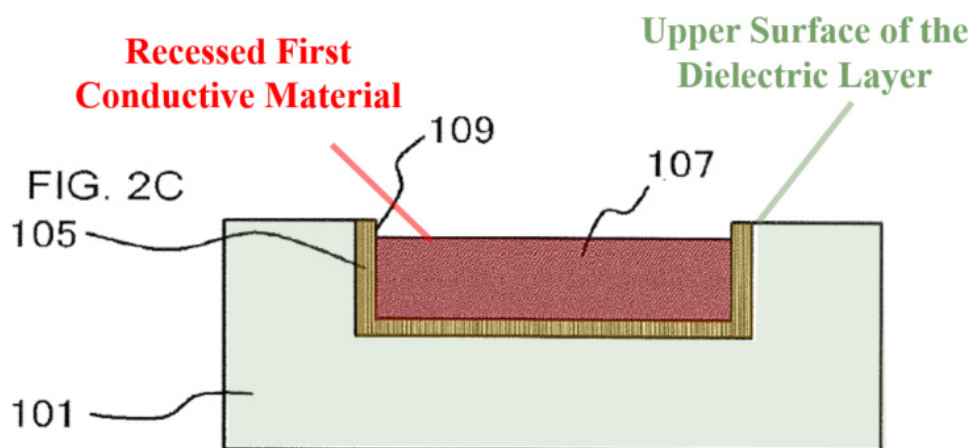
165. In my opinion, Kawahara in view of Chan discloses or suggests all of the features of claim 10 of the '183 patent.

1. Claim 10

“The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.”

166. In my opinion, Kawahara in combination with Chan discloses or suggests this feature. As I discuss above for claim elements 1[d] and 9[f], Kawahara discloses recessing the copper interconnect (“second conductive material”) such that

“the upper surface of the lower layer of copper interconnect 107 is retracted to be closer to the substrate than the upper surface of the insulating interlayer 101.” (See my discussion above in sections IX.D.1(d), IX.D.4(f); Ex. 1009, 6:58-67; *see also id.*, 6:27-33 (“Step 15: portions of the Cu film 106 and the barrier metal film 105 formed outside of the concave portion 103 are removed and the upper surface of Cu film 106 is retracted to be closer to the substrate than the upper surface of the barrier metal film 105 on the side wall of the concave portion 103, so as to form a lower layer copper interconnect 107 composed of the Cu film 106”).)



(*Id.*, FIG. 2C (annotated).)

167. Kawahara does not explicitly disclose using wet etching to recess the copper interconnect layer, but Chan discloses using wet etching for just such a purpose in a similar device, and a person of ordinary skill in the art would have had good reason to use wet etching to remove portions of Kawahara’s copper interconnect in order to provide the recessed area for the overlying capping layer for

reasons similar to those I discussed above with respect to the Fukunaga-Park-Chan combination in Section IX.B. (*See* my discussion above in section IX.B.)

168. Chan, like Kawahara, is directed to copper interconnect structures embedded in dielectric material, where a recessed capping layer overlies the copper interconnect. For example, figure 5E of Chan shows copper interconnects 120 formed in trenches of the dielectric layer 82, where cobalt caps 124 cover the top surfaces of the interconnect. (Ex. 1007, ¶[0034] (“FIGS. 5A-5E show cross-sectional views of a portion of wafer 80 during the manufacture of integrated circuits thereon. FIG. 5A shows wafer 80 consisting of a layer of dielectric 82. Trenches 84 are formed in the dielectric 82. The trenches 84 are configured to receive copper interconnects. Although not shown, trenches 84 are lined on the bottom and sides by a thin barrier of metal such as tantalum nitride to prevent copper electromigration.”), ¶[0040] “[T]he cobalt deposited on the exposed surface of the copper interconnects 120 via the electroless plating solution, gradually forms caps 124 shown within FIG. 5E. These caps should cover all exposed surfaces of copper interconnects 120.”)

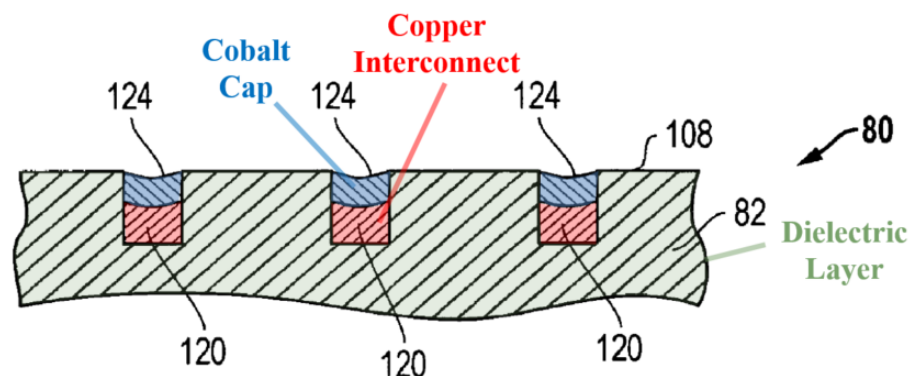


FIG. 5E

(*Id.*, FIG. 5E (annotated).)

169. Like Kawahara, Chan discloses recessing copper that initially fills the trenches to form recessed interconnects 120 so that the caps are formed in the trench. (*Id.*, ¶[0038]-[0039].) Chan discloses that while the copper in the trenches can be recessed by chemical mechanical polishing (CMP), “[t]he recessing effect of chemical-mechanical polishing can vary across the surfaces 22 of copper interconnects 20 as shown in FIG. 1C,” which can result in a dish-like surface. Moreover, Chan also discloses that recesses resulting from CMP are highly dependent on the geometry of the copper interconnects, where the depth of the recess can vary based on pattern density of the interconnect as well as the width of the copper interconnect:

Chemical-mechanical polishing recesses copper interconnects 20 below the surface of dielectric 2 as shown in FIG. 1C. Proper recessing is needed to create effective,

more reliable cobalt caps (e.g., caps 30 in FIG. 1E) on copper interconnects 20. The recesses resulting from chemical-mechanical polishing is highly dependent on the geometry of the copper interconnects. More particularly, the recessing of copper interconnects below the dielectric surface is more dominant in large patterns of copper interconnects than in smaller or more density-packed patterns. In other words, a sufficiently deep recess is created in the copper when the width of the copper interconnect is substantially large and/or when the distance between copper interconnects is substantially large.

The depth of the recess can vary by pattern density. For copper interconnects with small widths or for copper interconnects closely positioned next to each other, the copper interconnect recesses created during chemical-mechanical polishing may not be sufficient.

(*Id.*, ¶¶[0007]-[0008].)

170. Chan further discloses that shallow recesses created by CMP can create problems, including lack of complete coverage for copper interconnects by the overlying cobalt capping layers, which can result in corrosion or other adverse effects. (*Id.*, ¶[0009].) Chan also discloses that using CMP to recess the copper interconnect can also remove portions of the dielectric, which is undesirable. (*Id.*, ¶[0010].)

171. Chan discloses that, rather than using CMP to form or deepen the recesses in the copper interconnects, a wet etch using an acidic solution that does not substantially affect the dielectric layer is used to form or deepen the recesses:

[A]n acidic solution from source 106 is applied to wafer 80 in FIG. 5C. The acidic solution may take from in $\text{HNO}_3/\text{H}_2\text{O}$, $\text{HCL}/\text{KCLO}_3/\text{H}_2\text{O}$, or heated $\text{HCL}/\text{H}_2\text{O}$. Other acidic solutions are contemplated for etching copper interconnects 120. The acidic solution etches the copper interconnects 120, but will not substantially affect the dielectric material 82. Recesses 122 are formed or deepened in the copper interconnects 120 after application of the acidic solution, as shown in FIG. 5D.

(*Id.*, ¶[0038].)

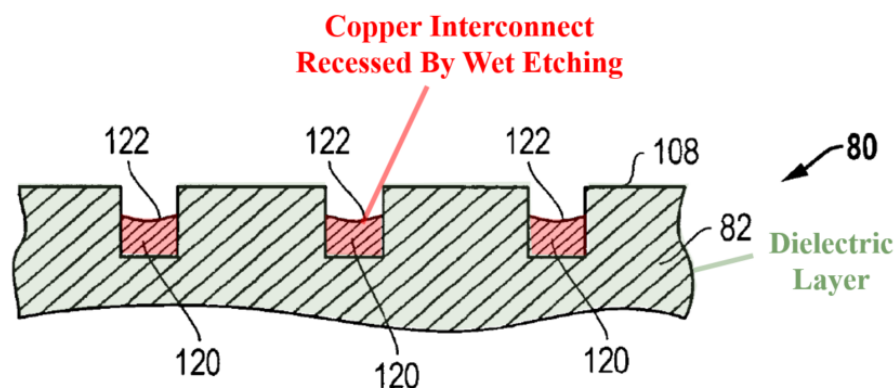


FIG. 5D

(*Id.*, FIG. 5D (annotated).)

172. A person of ordinary skill in the art implementing an interconnect structure like that of Kawahara would have had good reason to look to Chan,

particularly because both of these references are in the same field that very similar interconnect structures. Having looked to Chan, such a person of ordinary skill in the art would have been motivated to use a wet etch as disclosed by Chan to recess the copper interconnect in the trenches of Kawahara. As I discuss above, Chan discloses that using wet etching to recess the copper interconnect avoids disadvantages resulting from using CMP for such recessing. Therefore, a person of ordinary skill in the art would have been motivated to use wet etching with Kawahara's interconnect in order to avoid those same disadvantages. For example, such a person of ordinary skill in the art would have been motivated to use wet etching as opposed to chemical mechanical polishing (CMP) in order to avoid applying a mechanical load to the substrate, which can damage the structure when low-k dielectric materials are used. (Ex. 1005, ¶[0057].)

173. Moreover, a person of ordinary skill in the art would have found it straightforward to use wet etching as disclosed by Chan. Such an implementation would have simply been the application of a known method (wet etching to recess the copper interconnect as disclosed by Chan) to a similar device (the interconnect of Kawahara) and would have produced predictable results (recessed interconnect ready for capping). Moreover, such a skilled person would have had a reasonable expectation of success because Chan discloses using wet etching for a very similar

interconnect structure. Therefore, in my opinion, the Kawahara-Chan combination discloses or suggests claim 10.

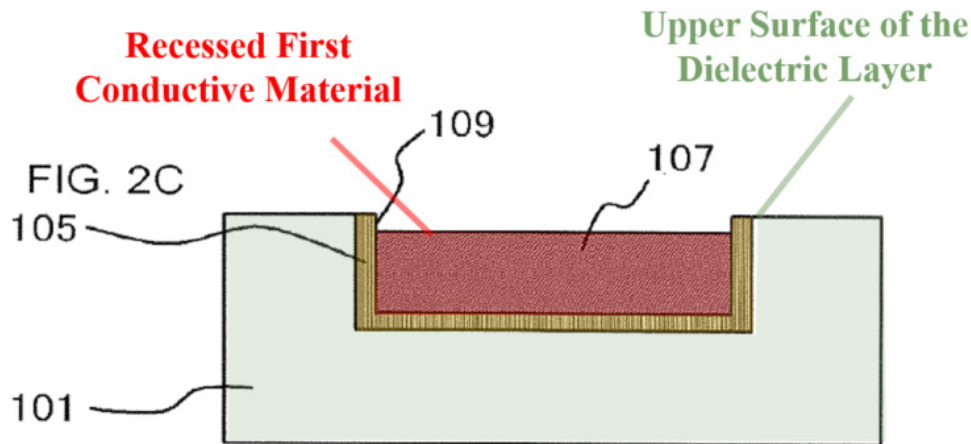
F. Kawahara in Combination with Fukunaga Discloses or Suggests the Features of Claim 10

174. In my opinion, Kawahara in view of Fukunaga discloses or suggests all of the features of claim 10 of the '183 patent.

1. Claim 10

“The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.”

175. In my opinion, Kawahara in combination with Fukunaga discloses or suggests this feature. As I discuss above for claim elements 1[d] and 9[f], Kawahara discloses recessing the copper interconnect (“second conductive material”) such that “the upper surface of the lower layer of copper interconnect 107 is retracted to be closer to the substrate than the upper surface of the insulating interlayer 101.” (Ex. 1009, 6:58-67; *see also id.*, 6:27-33 (“Step 15: portions of the Cu film 106 and the barrier metal film 105 formed outside of the concave portion 103 are removed and the upper surface of Cu film 106 is retracted to be closer to the substrate than the upper surface of the barrier metal film 105 on the side wall of the concave portion 103, so as to form a lower layer copper interconnect 107 composed of the Cu film 106”).)



(*Id.*, FIG. 2C (annotated).)

176. Kawahara does not explicitly disclose using wet etching to recess the copper interconnect layer, but Fukunaga discloses using wet etching for just such a purpose in a similar device, and a person of ordinary skill in the art would have had good reason to use wet etching to remove portions of Kawahara's copper interconnect in order to provide the recessed area for the overlying capping layer.

177. As I discuss above for claim 1 in Section IX.A.1, like Kawahara, Fukunaga is related to forming interconnect for semiconductor devices, where copper interconnect overlies a barrier layer in a trench in a dielectric layer, and a capping layer is formed overlying the copper interconnect within the trench. (*See* my discussion above in section IX.A.1.) Therefore, a person of ordinary skill in the art forming interconnect like that disclosed by Kawahara would have had good reason to look to Fukunaga.

178. Fukunaga discloses that it is beneficial to use wet etching to remove extra copper material, like that shown in figure 2B of Kawahara, as wet etching does not require a mechanical load to be applied to the substrate, which can damage the structure when low-k dielectric materials are used. (Ex. 1005, ¶[0051] (“The removal of the extra copper 16 may also be carried out by etching using an inorganic or organic acid.”), ¶[0060] (“etching of interconnects 18 is further continued so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.”), ¶[0057] (“In the case of wet etching, no physical force is applied to a substrate. Accordingly, there is no fear of damage to the substrate even when a weak material, such as copper or low-k materials, is present in the substrate.”).)

179. Having looked to Fukunaga, a person of ordinary skill in the art would have found been motivated to remove the extra copper interconnect 106 in Kawahara using wet etching in order to avoid possible damage to the semiconductor device. As discussed above for claim element 1[b], Kawahara discloses using a low-k SiOC dielectric material. (See my discussion above in section IX.D.1(b); Ex. 1009, 5:16-22 (“Each of the insulating interlayer 101, the insulating interlayer 117, the insulating interlayer 123 and the insulating interlayer 131 may be a single layer film or a multiple-layered film. Materials for these insulating interlayers may be, for example, silicon dioxide (SiO₂) film. Further, the insulating interlayer may be a low

dielectric constant insulating film such as silicon oxycarbide (SiOC) film.”.) While Kawahara discloses removal of at least a portion of the copper interconnect 106 using CMP, a person of ordinary skill in the art would have been motivated, in view of Fukunaga’s teachings to use wet etching to recess the copper interconnect. Indeed, Fukunaga teaches that CMP can damage the substrate, while wet etching does not raise such a concern:

In the case of a CMP method, on the other hand, processing of a substrate is carried out while applying a load on the substrate, and there is therefore a fear of damage to the substrate. Accordingly, it is necessary with a CMP method to use a slurry having a strong chemical reactivity and carry out polishing at a low pressure and a low speed. As regards electrolytic polishing, as **with wet etching, substantially no load is applied on a substrate, and therefore there is no fear of damage to the substrate.**

(Ex. 1005, ¶[0057].)

180. Moreover, a person of ordinary skill in the art would have known that wet-etching using an acidic solution, as taught by Fukunaga, was a well-known etching technique for etching recesses in interconnect material like the copper interconnect of Kawahara. (Ex. 1007, ¶[0038] (“After chemical-mechanical polishing, an acidic solution from source 106 is applied to wafer 80 in FIG. 5C. The

acidic solution may take from in $\text{HNO}_3/\text{H}_2\text{O}$, $\text{HCL}/\text{KCLO}_3/\text{H}_2\text{O}$, or heated $\text{HCl}/\text{H}_2\text{O}$. Other acidic solutions are contemplated for etching copper interconnects 120. The acidic solution etches the copper interconnects 120, but will not substantially affect the dielectric material 82. Recesses 122 are formed or deepened in the copper interconnects 120 after application of the acidic solution, as shown in FIG. 5D.”); *see also id.*, ¶¶[0007]-[0008]; Ex. 1011, ¶[0066].)

181. Based on Fukunaga’s teachings regarding wet etching, a person of ordinary skill in the art would have been motivated to use wet etching to recess the interconnect as disclosed by Kawahara as it would have been an effective way of removing such material and would not have required the application of a load to the substrate, thereby avoiding possible damage to the substrate. Using wet etching as disclosed by Fukunaga for recessing the copper interconnect in an interconnect structure as disclosed by Kawahara would have been straightforward for a person of ordinary skill in the art to implement, because Fukunaga discloses how to use wet etching to remove excess copper material and such a person of ordinary skill in the art would have known that such wet etching was commonly used for such a purpose. Using wet etching would have been the application of a known technique (wet etching to remove copper interconnect as disclosed by Fukunaga) to a similar device (Kawahara’s interconnect structure), and would have been produced the predictable

result of a recessed copper interconnect ready for capping. Therefore, in my opinion, the Kawahara-Fukunaga combination discloses or suggests claim 10.

G. Kawahara in Combination with Park Discloses or Suggests the Features of Claims 18-25

182. In my opinion, Kawahara in view of Park discloses or suggests all of the features of claims 18-25 of the '183 patent.

1. Claims 18-25

183. As I discuss below, Kawahara in view of Park discloses or suggests all of the features of claims 18-25. Park, like Kawahara and Fukunaga, is directed to copper interconnect structures embedded in low-k materials, where a recessed capping layer overlying the copper interconnect is used to prevent electromigration. (See my discussion above in section IX.A.1(b) showing the similarities between Park and Fukunaga.) Because Park discloses an interconnect structure very similar to that of Kawahara, a person of ordinary skill in the art implementing interconnect like that disclosed by Kawahara would have reason to look to Park.

184. While Kawahara discloses that the interconnect structure can be used in semiconductor devices (Ex. 1009, 3:1-3, 6:49-52, 9:32-33), Kawahara does not explicitly disclose using the interconnect structure in a “computing device.” As discussed above in Sections IX.A.8-15, Park discloses a very similar interconnect structure used in a computing device and, in combination with Fukunaga, discloses or suggests the features of claims 18-25. (See my discussion above in sections

IX.A.8-15.) For example, Park discloses using the interconnect structure in a cell phone or computer (“computing device”) that includes a CPU (“component”) coupled to a board as recited in claim 18. Park also discloses or suggests that such a computing device includes memory (claim 19), a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23). (See my discussion above in sections IX.A.8-13.) Park further discloses or suggests that the CPU (“component”) is a “packaged integrated circuit die” (claim 24) that is a “processor” (claim 25).

FIG. 10

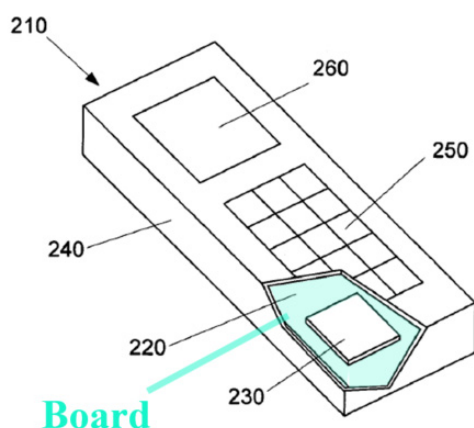
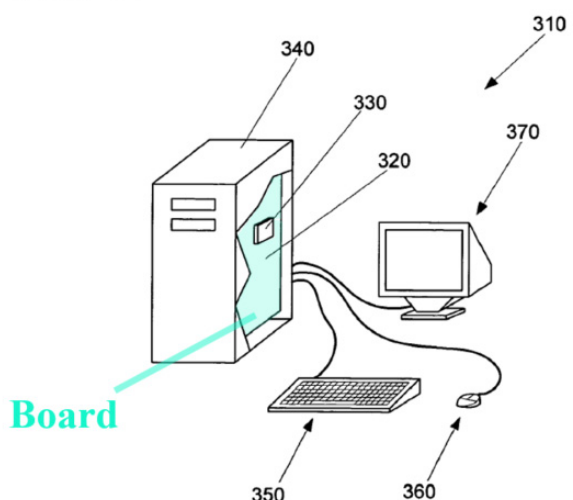


FIG. 11



(Ex. 1006, FIGs. 10, 11 (annotated).)

185. For the same reasons presented above for the Fukunaga-Park combination, a person of ordinary skill in the art would have had good reason to use Kawahara’s interconnect structure discussed above for claim 1 in a semiconductor

device that is a “computing device,” where the features recited in claims 18-25 are disclosed or suggested by the Kawahara-Park combination for the same reasons presented above for the Fukunaga-Park combination.

186. A person of ordinary skill in the art would have understood that using the Kawahara interconnect structure discussed above for claim 1 in computing devices as disclosed by Park, would have been a predictable combination of known components according to known methods to achieve a predictable result. The use of Kawahara’s interconnect structure in Park’s computing devices would have increased the utility of such an interconnect structure through its implementation in such computing devices and, based on the teachings of Kawahara and Park, provided the benefit of more reliable operation for the computing devices. Moreover, a person of ordinary skill in the art would have had a reasonable expectation of success in such a Kawahara-Park combination as Park discloses the use of a similar interconnect structure in computing devices, and the ’183 patent indicates that a person of ordinary skill in the art would be capable using similar interconnect in computing devices. (*Id.*)

187. The inclusion of Kawahara’s interconnect structure, instead of the Fukunaga-Park interconnect, in computing devices as disclosed or suggested by Park does not impact the disclosure or suggestion of the remaining features of claims 18-25.

H. Kawahara in Combination with Park and Song Discloses or Suggests the Features of Claims 20-23

188. In my opinion, Kawahara in view of Park and Song discloses or suggests all of the features of claims 20-23 of the '183 patent.

1. Claims 20-23

189. As I discuss above in Section IX.G, the Kawahara-Park combination discloses or suggests all of the features of claims 20-23 for the similar reasons to those I discuss for the Fukunaga-Park combination in Sections IX.A.10-13. (*See my discussion above in sections IX.G, IX.A.10-13.*) I have been asked to assume a scenario in which the Kawahara-Park combination does not disclose or suggest these features. Under such a scenario, it is my opinion that, in further view of Song, a person of ordinary skill in the art would have been motivated to include such features in the cell phone of the Kawahara-Park combination for the same reasons I discuss above in Section IX.C for the Fukunaga-Park-Song combination.

190. Park does not disclose all of the details regarding the cell phones that incorporate the interconnect structure, and therefore a person of ordinary skill in the art would have had good reason to look to Song, which discloses additional details regarding components included in cell phones. In view of Song and their knowledge of common features in cell phones at the relevant time, a person of ordinary skill in the art would have been motivated to include a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23) as disclosed by

Song in a cell phone of the Kawahara-Park-Song combination for the same reasons I discuss above for the Fukunaga-Park-Song combination. (*See* my discussion above in sections IX.C.1.) Such a person of ordinary skill in the art would have been motivated to include such features in order to enable fundamental operational characteristics of the cell phone (communications using the communications chip and antenna powered by the battery) and provide added utility in the form of the ability to take pictures (camera). Moreover, a person of ordinary skill in the art would have found such an implementation to have been a straightforward combination of well-known technologies using known methods to produce predictable results.

191. In my opinion, a person of ordinary skill in the art would have had a reasonable likelihood of success in implementing such features as they were well-known and widely-implemented features of cell phones. The inclusion of Kawahara's interconnect structure, instead of the Fukunaga-Park interconnect, in computing devices as disclosed or suggested by Park and Song does not impact the disclosure or suggestion of the remaining features of claims 20-23.

X. CONCLUSION

192. In summary, it is my opinion that all of the features recited in claims 1-25 of the '183 patent are disclosed or suggested by the prior art.

193. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.



Dated: February 3, 2023

Stanley Shanfield