

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.
Petitioner

v.

DAEDALUS PRIME LLC
Patent Owner

Patent No. 10,727,183

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,727,183**

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Ex. 1006	U.S. Patent Publication No. 2006/0128144 to Park <i>et al.</i> (“Park”)
Ex. 1007	U.S. Patent Publication No. 2006/0115976 to Chan <i>et al.</i> (“Chan”)
Ex. 1008	U.S. Patent Publication No. 2010/0308408 to Song <i>et al.</i> (“Song”)
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Ex. 1018	Memorandum from Director Vidal (dated June 21, 2022)

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I. INTRODUCTION

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) requests *inter partes* review of claims 1-25 (“the challenged claims”) of U.S. Patent No. 10,727,183 (“the ’183 patent”) (Ex. 1001), which, according to PTO records, is assigned to Daedalus Prime LLC (“Patent Owner” or “PO”). For the reasons discussed below, the challenged claims should be found unpatentable and canceled.

II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

Real Parties-in-Interest

Petitioner identifies the following as the real parties-in-interest: Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Samsung Semiconductor, Inc.

Related Matters

The ’183 patent is at issue in *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al*, Case No. 2:22-CV-00353.

Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Howard Herr (*pro hac vice* to be filed). Service information is Paul Hastings LLP, 2050 M St., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705,

email: PH-Samsung-Daedalus-IPR@paulhastings.com. Petitioner consents to electronic service.

III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge any fees due during this proceeding to Deposit Account No. 50-2613.

IV. GROUNDS FOR STANDING

Petitioner certifies that the '183 patent is available for review and Petitioner is not barred/estopped from requesting review on the grounds identified herein.

V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

Claims 1-25 should be canceled as unpatentable based on the following grounds:

Ground 1: Claims 1-25 are obvious under pre-AIA 35 U.S.C. § 103(a) based on U.S. Patent Publication No. 2005/0282378 to Fukunaga *et al.* (“Fukunaga”) (Ex. 1005) in view of U.S. Patent Publication No. 2006/0128144 to Park *et al.* (“Park”) (Ex. 1006);

Ground 2: Claim 10 is obvious under pre-AIA 35 U.S.C. § 103(a) based on Fukunaga, Park, and U.S. Patent Publication No. 2006/0115976 to Chan *et al.* (“Chan”) (Ex. 1007);

Ground 3: Claims 20-23 are obvious under pre-AIA 35 U.S.C. § 103(a) based

on Fukunaga, Park, and U.S. Patent Publication No. 2010/0308408 to Song *et al.* (“Song”) (Ex. 1008);

Ground 4: Claims 1-9 and 11-17 are anticipated under pre-AIA 35 U.S.C. § 102(a) and 102(e) based on U.S. Patent No. 7,863,744 to Kawahara *et al.* (“Kawahara”) (Ex. 1009);

Ground 5: Claim 10 is obvious under pre-AIA 35 U.S.C. § 103(a) based on Kawahara in view of Chan;

Ground 6: Claim 10 is obvious under pre-AIA 35 U.S.C. § 103(a) based on Kawahara in view of Fukunaga;

Ground 7: Claims 18-25 are obvious under pre-AIA 35 U.S.C. § 103(a) based on Kawahara in view of Park; and

Ground 8: Claims 20-23 are obvious under pre-AIA 35 U.S.C. § 103(a) based on Kawahara, Park, and Song.¹

The ’183 patent issued July 28, 2020, from U.S. App. No. 16/559,086 (“the ’086 application”), filed September 3, 2019. The ’183 patent claims priority back to

¹ Other references discussed herein are provided to show the state of the art at the time of the alleged invention of the ’183 patent.

International Application PCT/US2011/059453 (“the ’453 PCT application”) filed November 4, 2011. As demonstrated in the co-pending IPR petition that challenges the priority chain of the ’183 patent, the earliest effective filing date for the ’183 patent is the September 3, 2019 filing date of the ’086 application. However, all of the references relied on in the present petition are prior art to the ’183 patent even if the ’183 patent were to be entitled to the November 4, 2011 filing date of the ’453 PCT application.

Fukunaga published December 22, 2005. Park published June 15, 2006. Chan published June 1, 2006. Song published December 9, 2010, based on an application filed June 3, 2009. Kawahara issued January 4, 2011, based on an application filed January 4, 2008. Therefore, even if the ’183 patent is entitled to its earliest possible priority date of November 4, 2011, Fukunaga, Park, and Chan are prior art under at least pre-AIA 35 U.S.C. § 102(b), whereas Song and Kawahara are prior art under at least pre-AIA 35 U.S.C. §§ 102(a) and 102(e).

Other than Park, none of these references were considered during prosecution. (*See generally* Ex. 1004.) Park was cited by the Examiner in allowing the claims during prosecution. (Ex. 1004, 32-35.) However, as discussed below in Section X.C., inclusion of Park as a reference applied in Grounds 1-3 and 7-8 does not warrant discretionary denial because Petitioner presents Park in a new light as a

secondary reference in combination with each of Fukunaga and Kawahara, which are references not previously considered by the Patent Office. (Section X.C.)

VI. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) at the time of the alleged invention of the ’183 patent would have had a bachelor’s degree in a field relating to the semiconductor manufacturing process like materials science, physics, electrical engineering, or other related subjects, and at least two to three years of experience with fabrication of integrated circuits. (Ex. 1002, ¶¶16-17.)² More education can supplement practical experience and vice versa. (*Id.*)

VII. OVERVIEW OF THE ’183 PATENT

The ’183 patent discloses formation of an interconnect structure that includes conductive lines in a dielectric layer over a substrate, where the conductive lines are recessed in order to allow a capping layer to be formed on each of the conductive lines. (*Id.*, Abstract; Ex. 1002, ¶¶27-34.) Figure 2H shows the interconnect structure, which includes capping layers 215 deposited on the recessed conductive lines 208 within channels 212. (Ex. 1001, 9:6-27.)

² Petitioner submits the declaration of Dr. Stanley Shanfield (Ex. 1002), an expert in the field of the ’183 patent. (*Id.*, ¶¶5-12; Ex. 1003.)

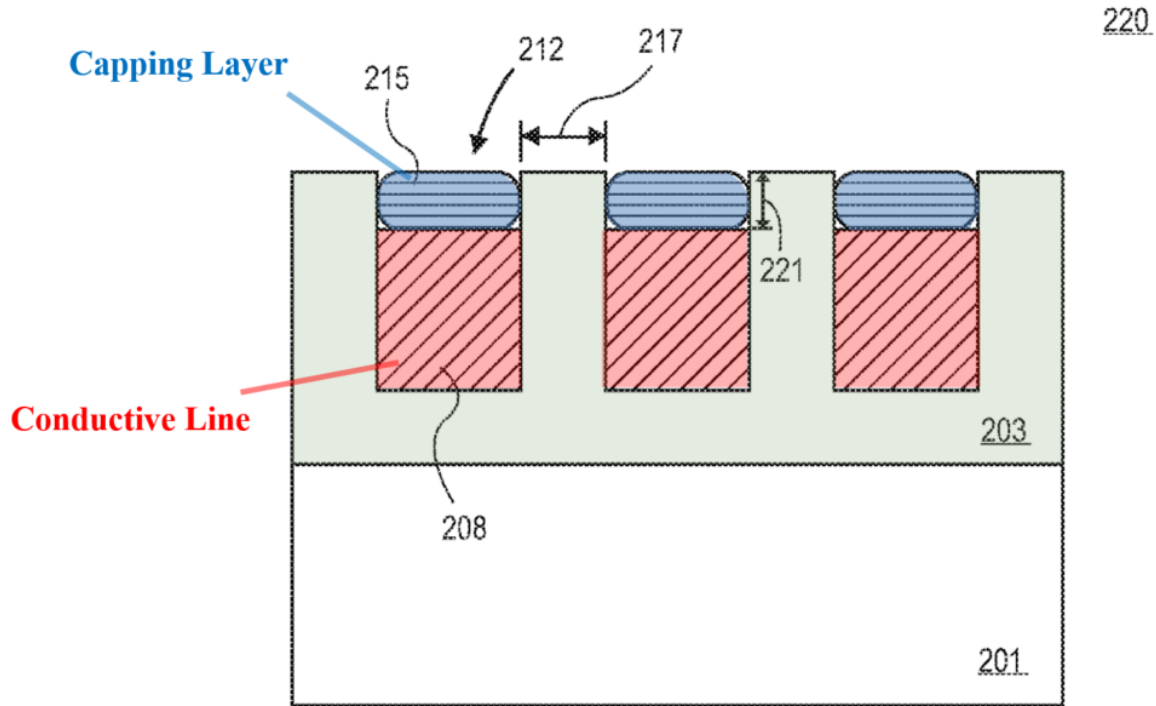


FIG. 2H

(*Id.*, FIG. 2H (annotated); Ex. 1002, ¶34.)

As explained below (*infra* Section IX), the above features were all known in the prior art. (See Ex. 1002, ¶¶45-191; see also *id.*, ¶¶18-26, 36-44 (describing the state of the art).)

VIII. CLAIM CONSTRUCTION

For IPR proceedings, the Board applies the claim construction standard according to *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). See 83 Fed. Reg. 51,340-59 (Oct. 11, 2018). Under *Phillips*, claim terms are typically given their ordinary and customary meanings, as would have been understood by a

POSITA at the time of the invention. *Phillips*, 415 F.3d at 1313; *see also id.*, 1312-16. The Board, however, only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems, Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015) (citing *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)). Petitioner believes that no express constructions of the claims are necessary to assess whether the prior art reads on the challenged claims. (Ex. 1002, ¶35.)

IX. DETAILED EXPLANATION OF UNPATENTABILITY

A. Ground 1 – Fukunaga in View of Park Renders Claims 1-25 Obvious

As shown in detail below, Fukunaga in combination with Park discloses or suggests all the features recited in claims 1-25. (Ex. 1002, ¶¶45-115.)

1. Claim 1

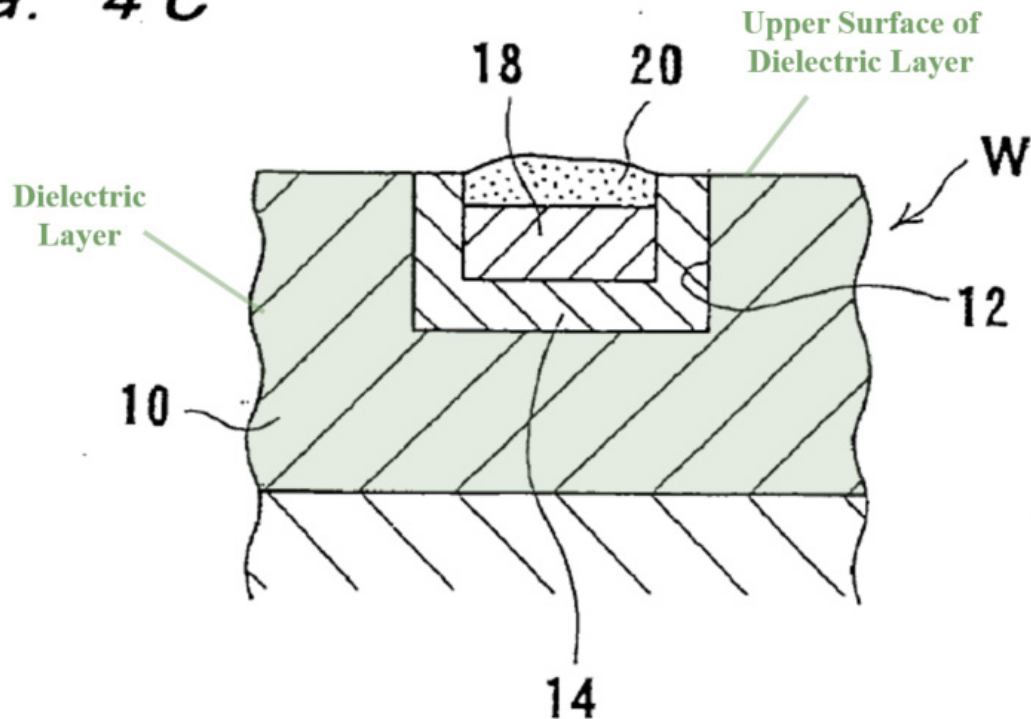
a) “An integrated circuit structure, comprising:”

To the extent the preamble is limiting, Fukunaga discloses “an integrated circuit structure.” (Ex. 1002, ¶46.) Fukunaga discloses an interconnect structure (“integrated circuit structure”) for use in multi-level interconnect structures overlying a semiconductor base that includes semiconductor devices (i.e., an integrated circuit). (Ex. 1005, Abstract, ¶¶[0002], [0005], [0007] (“forming copper interconnects in a semiconductor device”), ¶[0074]; Ex. 1002, ¶46.)

b) “a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen and carbon;”

Fukunaga and Park disclose or suggest this claim feature. (Ex. 1002, ¶¶47-56.) As shown in annotated figure 4C below, Fukunaga’s interconnect structure includes an insulating film 10 (“dielectric layer”) with an upper surface. (Ex. 1005, ¶[0048] (“insulating film (interlevel insulating film) 10 of, for example, SiO₂ or a low-k material deposited on a substrate W . . .”), ¶¶[0075], [0060]; Ex. 1002, ¶47.)

FIG. 4C



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶47.)

Fukunaga discloses that the interlevel insulating film, which may be a low-k material, is a dielectric film. (Ex. 1005, ¶[0007] (“an insulating film (interlevel

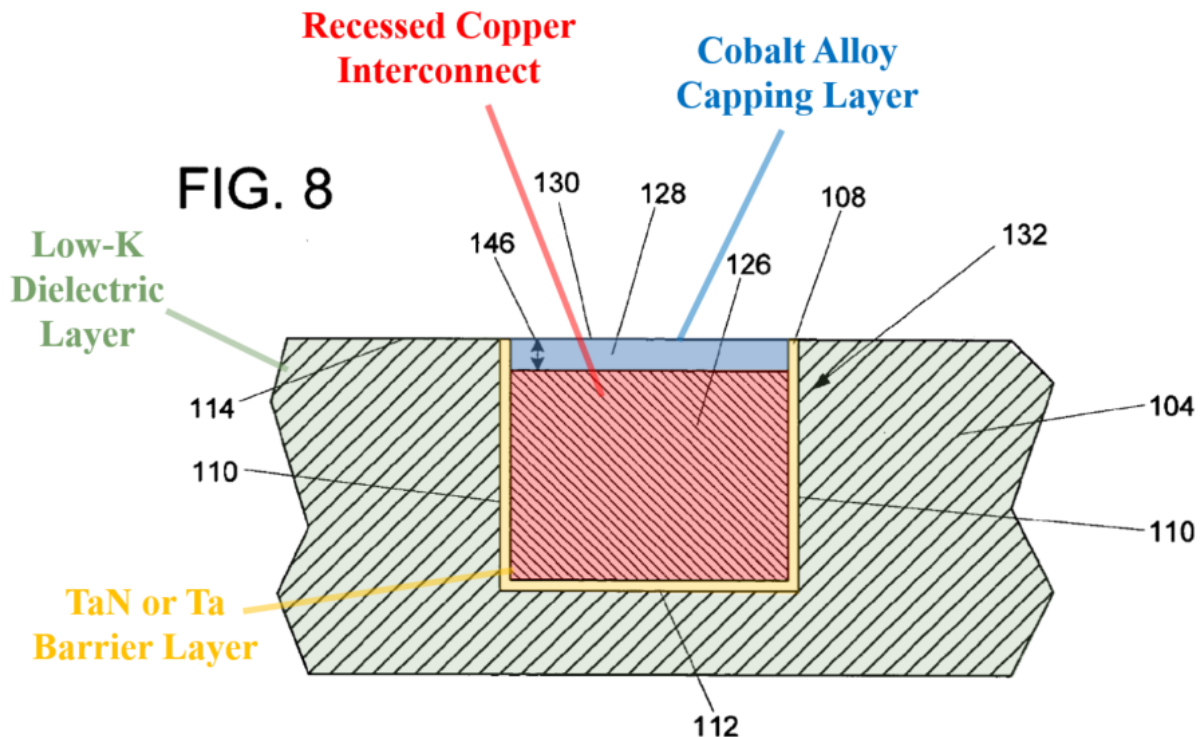
dielectric film) 10 of, for example, SiO₂ or low-k material”)³.) A POSITA would have recognized that “low-k material” refers to “low-k dielectric material.” (Ex. 1002, ¶48.)

Fukunaga does not explicitly disclose that the low-k dielectric material includes silicon, oxygen, and carbon. However, as disclosed by Park and numerous contemporaneous references that evidence the knowledge of a POSITA, low-k dielectric materials that include silicon (Si), oxygen (O), and carbon (C) were well-known and widely-used in semiconductor devices and interconnect structures like those of Fukunaga. (Ex. 1002, ¶49.) As demonstrated below, in view of Park and their knowledge of low-k dielectric materials, a POSITA would have found it obvious to form the interconnect structure of Fukunaga such that it includes low-k material that includes silicon (Si), oxygen (O), and carbon (C). (Ex. 1002, ¶49.)

Park, like Fukunaga, is directed to copper interconnect structures embedded in low-k materials, where a capping layer overlying recessed copper interconnect is used to prevent electromigration. (Ex. 1006, ¶¶[0018]-[0019], [0023]-[0024], FIG. 8; Ex. 1002, ¶50.) Park is entitled “Interconnects Having a Recessed Capping Layer

³ Emphasis added unless otherwise noted.

and Methods of Fabricating the Same” (Ex. 1006, Title) and discloses an interconnect structure very similar to that disclosed by Fukunaga, including a low-k dielectric layer 104, an opening lined with barrier layer 108 (e.g. TaN), a recessed conductive material 126 (e.g., copper) in the opening, and an overlying cobalt alloy capping layer 128. (Ex. 1006, ¶¶[0018]-[0019], [0023]-[0024], FIG. 8; Ex. 1002, ¶50.)



(Ex. 1006, FIG. 8 (annotated); Ex. 1002, ¶50.)

Park discloses that the low-k dielectric layer 104 can be formed of carbon doped oxide (Ex. 1006, ¶[0018], ¶[0024]), which includes silicon, oxygen, and carbon. (Ex. 1016, 2:44-54; Ex. 1002, ¶51.)

A POSITA implementing an interconnect structure like that disclosed by Fukunaga would have looked to Park for guidance, particularly because Fukunaga and Park are references in the same field and disclose very similar interconnect structures. (Ex. 1002, ¶52.) Having looked to Park, a POSITA would have found it obvious to implement the low-k insulating layer disclosed by Fukunaga using carbon doped oxide as disclosed by Park. (*Id.*)

While Fukunaga discloses using low-k material as the interlevel insulating film 10, Fukunaga does not disclose specific details regarding the low-k material. (Ex. 1005, ¶[0048].) Park, however, discloses using carbon doped oxide for the low-k dielectric in a very similar interconnect structure. (Ex. 1006, ¶¶[0018], [0024].) Therefore, a POSITA would have had good reason to look to Park and would have found it obvious to implement the low-k material as disclosed by Fukunaga using carbon doped oxide according to Park. (Ex. 1002, ¶53.)

Moreover, such a POSITA would have been motivated to use a carbon doped oxide, which includes silicon, oxygen, and carbon, as the low-k material in an interconnect structure like that disclosed by Fukunaga because the use of such carbon doped oxides in such interconnect structures was known to reduce capacitance and allow for faster signal transmission, reduced power dissipation, and

reduced cross-talk. (Ex. 1016, 1:32-37, 1:57-60; Ex. 1010, ¶[0004], ¶[0006]; Ex. 1002, ¶54.)

Using carbon doped oxides as low-k interlayer dielectrics was well-known and widely-practiced in the art, and a POSITA would have readily understood that such carbon doped oxides are a viable and preferable low-k dielectric for use in interconnect structures like those of Fukunaga. (Ex. 1010, ¶[0006]; Ex. 1016, 2:44-54; Ex. 1009, 5:20-25; Ex. 1015, ¶¶[0007], ¶[0025]; Ex. 1002, ¶55.)

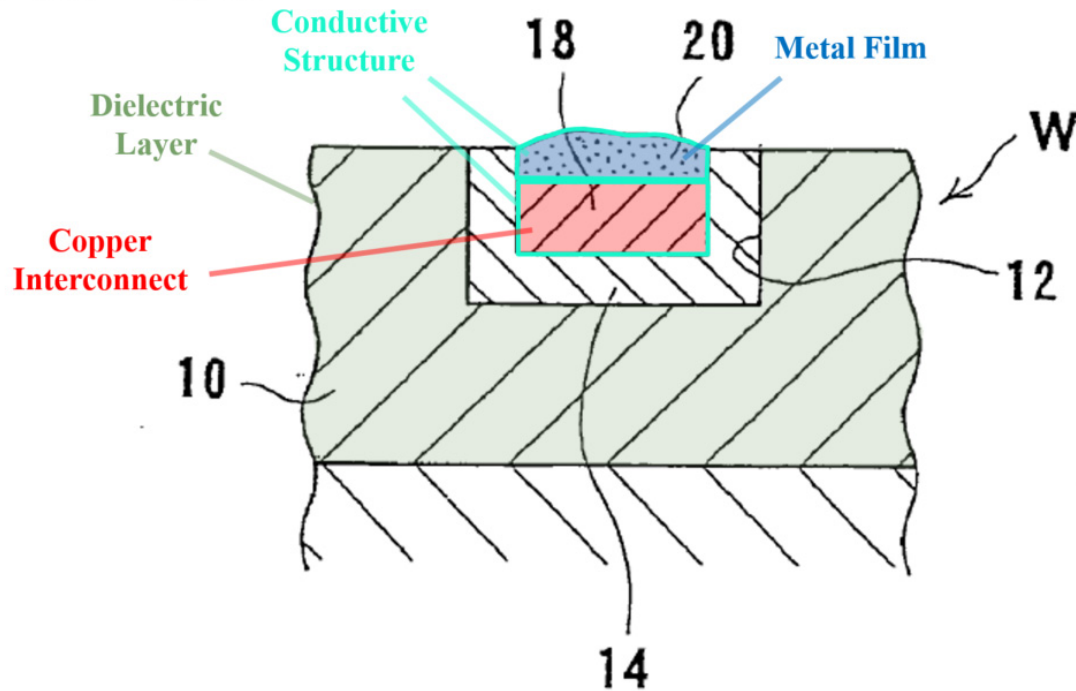
As evidenced by its widespread use in similar interconnect structures, a POSITA would have found it straightforward to use carbon doped oxide as the low-k material in interconnect structures like those disclosed by Fukunaga. (Ex. 1002, ¶56.) Such an implementation would have simply been a combination of well-known technologies using known methods and would have had predictable results. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416-18 (2007). Moreover, a skilled person would have had a reasonable expectation of success because, as demonstrated by Park and other contemporaneous references, interconnect structures with such carbon doped oxide insulating layers were well known in the art. *See Pfizer, Inc. v. Apotex, Inc.*, 480 F.3d 1348, 1364 (Fed. Cir. 2007) (“only a reasonable expectation of success, not a guarantee, is needed” in an obviousness analysis). (Ex. 1002, ¶56.)

Therefore, the Fukunaga-Park combination discloses or suggests claim element 1[b]. (*Id.*)

c) “a conductive structure in the dielectric layer, the conductive structure comprising:”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶57.) For example, as shown in annotated figure 4C below, Fukunaga discloses a conductive structure that includes interconnect 18 and metal film 20 in the trench 12, where the interconnect 18 and film 20 are made of metal and conductive. (Ex. 1005, ¶[0060] (“copper 16 embedded in the trenches (interconnect recesses) 12”), ¶[0062] (“metal film (protective film) 20 of, for example, a cobalt alloy or a nickel alloy is formed selectively on the surfaces of interconnects 18 in the trenches 12”), FIGs. 4A-4C; Ex. 1002, ¶57.)

FIG. 4C

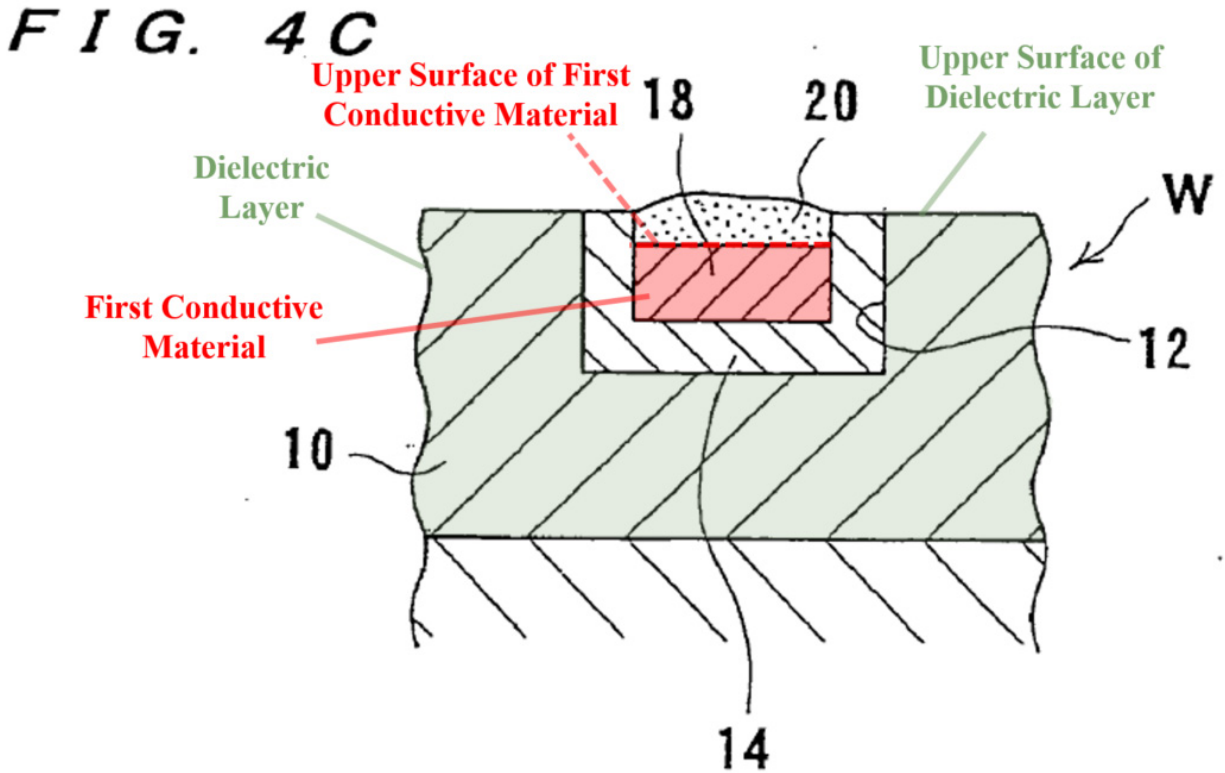


(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶57.)

d) “a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶58.) For example, as shown in annotated figure 4C below, the copper interconnect 18 (“first conductive material”) has an upper surface, where a portion of the upper surface is below a portion of the upper surface of the dielectric layer 10. (Ex. 1005, ¶[0060] (“forming interconnects 18 with the copper 16 embedded in the trenches”) (“polishing or etching of interconnects 18 is further continued so that the surfaces of

interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.”), ¶[0063], FIGs. 4A-4C; Ex. 1002, ¶58.)



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶58.)

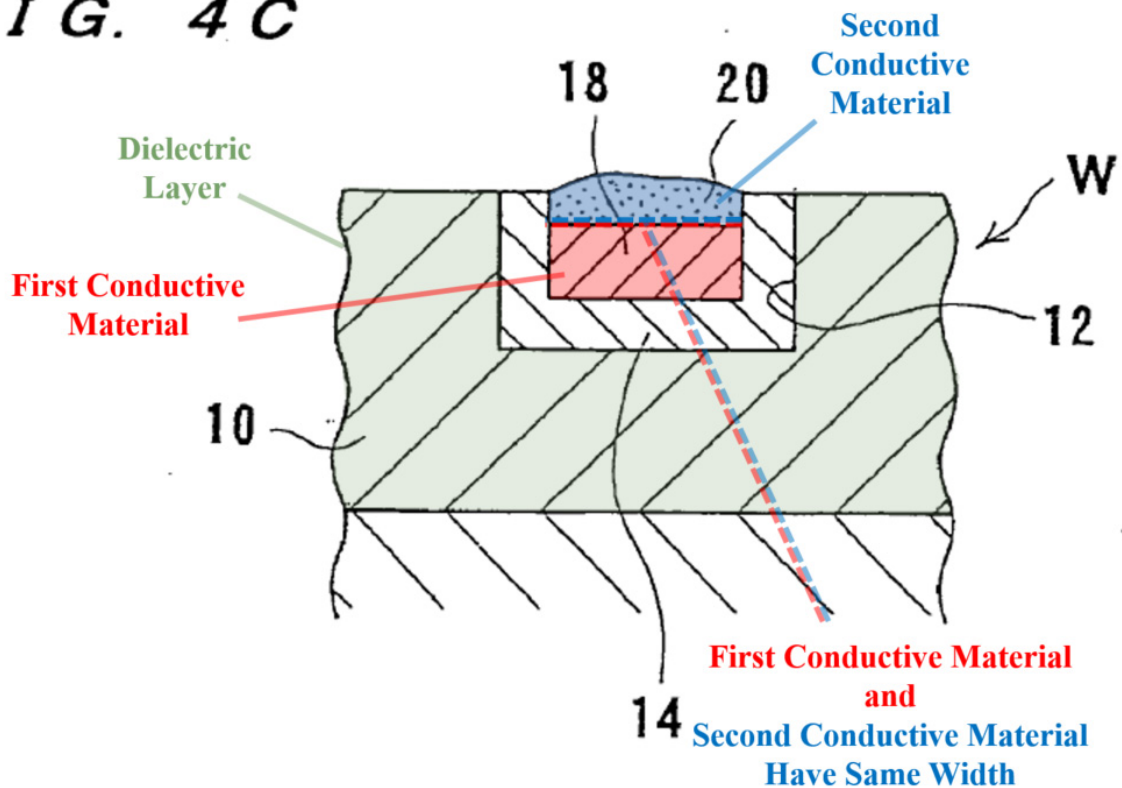
e) **“a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”**

The Fukunaga-Park combination discloses or suggests this feature to the extent it can be understood.⁴ (Ex. 1002, ¶¶59-71.) Metal film 20 (“second conductive material”) includes cobalt and, as shown in annotated figure 4C below, is on the upper surface of the interconnect 18 (“first conductive material”). (Ex. 1005, ¶[0062] (“**a metal film (protective film) 20 of, for example, a cobalt alloy ... is formed selectively on the surfaces of interconnects 18 in the trenches 12, as**

⁴ While the '183 patent does not provide any explanation as to what constitutes a “curved corner below the portion of the upper surface of the dielectric layer,” Petitioner assumes that such a claim feature is met by a structure that has an upper-surface profile similar to that of the capping layer 215 shown in figure 2H of the '183 patent. Petitioner, however, does not concede that claim 1 is not indefinite.

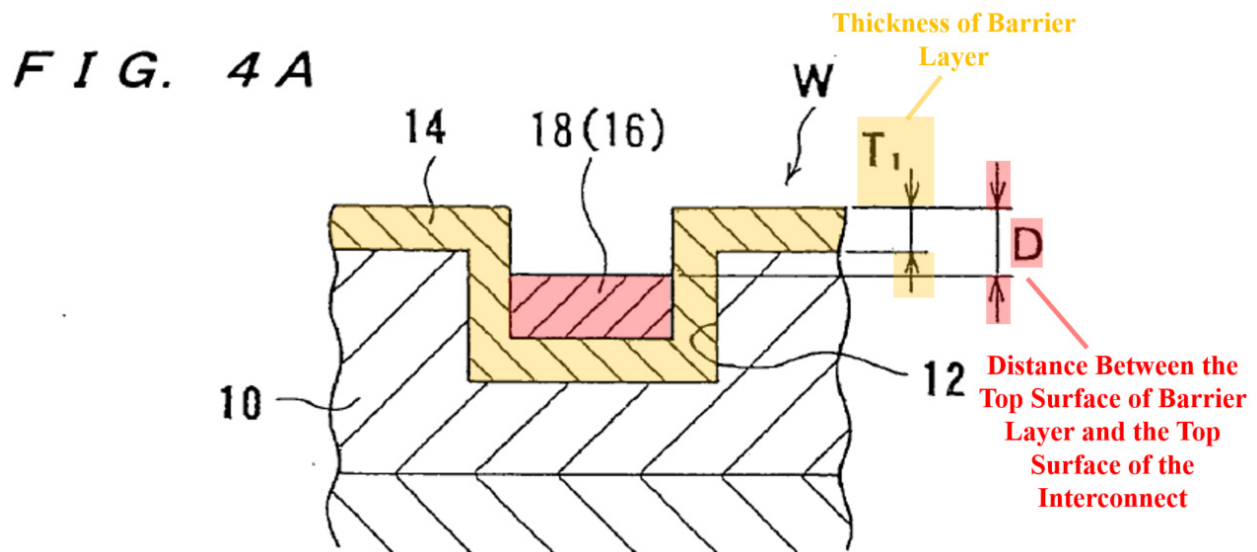
shown in FIG. 4B, thereby **covering the surfaces of interconnects 18 with the metal film 20 to protect interconnects 18.**”), FIGs. 4B-4C; Ex. 1002, ¶59.) Because the metal film 20 (“second conductive material”) is confined by the trench and covers the surface of the interconnect 18 (“first conductive material”), those materials have the same width at the location where they meet. (Ex. 1005, ¶¶[0062]-[0063], FIGs. 4B-4C; Ex. 1002, ¶59.)

FIG. 4C



(Ex. 1005, FIG. 4C (annotated); Ex. 1002, ¶59.)

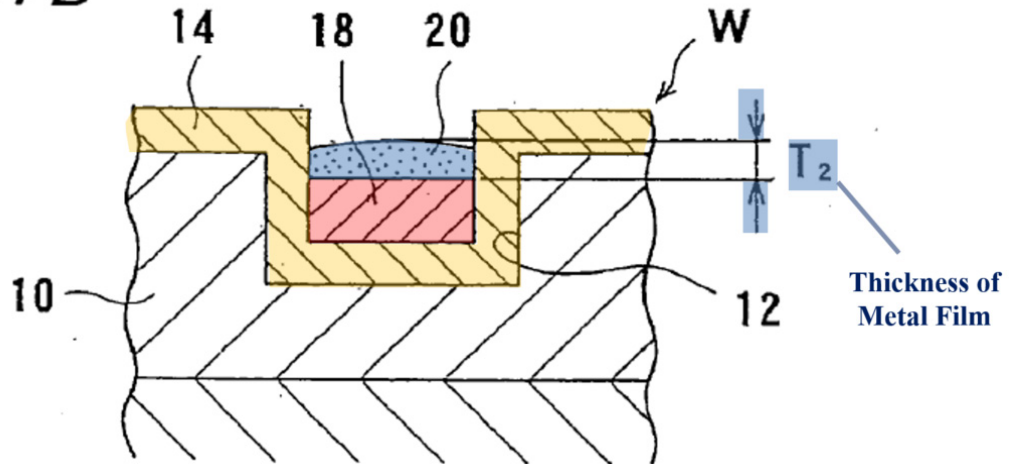
Fukunaga discloses that the relative positioning of the top surface of the metal film 20 relative to the top surface of the dielectric layer can be adjusted in order to achieve a flat upper surface for the substrate W. (Ex. 1005, ¶¶[0061], [0063]-[0065]; Ex. 1002, ¶60.) For example, Fukunaga discloses that “[t]he distance D between the surface of the barrier layer 14 and the surfaces of the interconnects 18 is determined taking account of the thickness of the barrier layer 14 and the necessary thickness of a metal film 20 to be formed selectively on the surfaces of interconnects 18, as described below.” (Ex. 1005, ¶[0061].) As shown in annotated figure 4A below, D is the distance between the top surface of barrier layer 14 and the top surface of interconnect 18, whereas T_1 is the thickness of barrier layer 14.



(Ex. 1005, FIG. 4A (annotated); Ex. 1002, ¶60.)

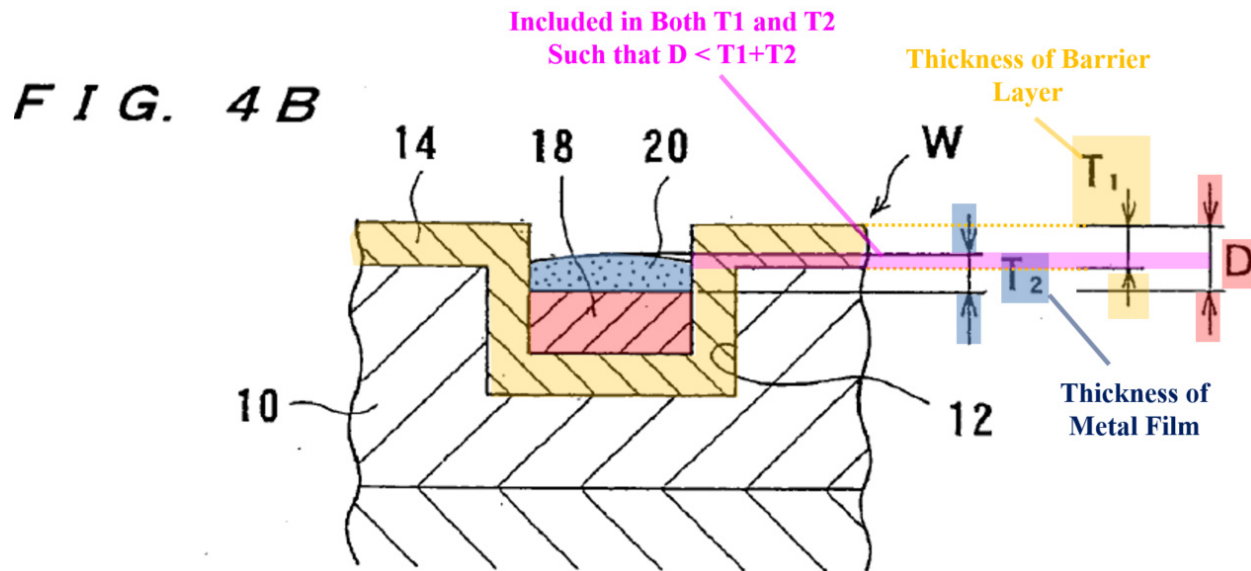
The thickness T_2 of metal film 20 is shown in annotated figure 4B below.

FIG. 4B



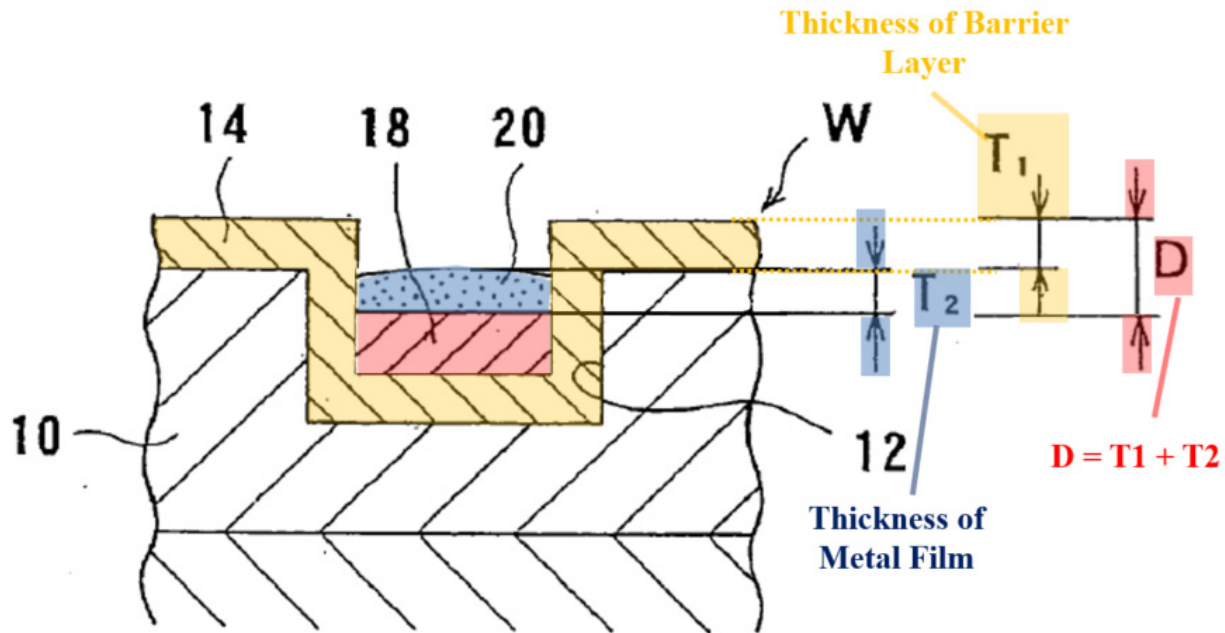
(Ex. 1005, FIG. 4B (annotated); Ex. 1002, ¶61.)

Fukunaga further discloses that if the distance D is approximately equal to the sum of the thickness T_1 of the barrier layer 14 and the thickness T_2 of the metal film 20, the result is a flat surface of the substrate. (Ex. 1005, ¶[0061]; Ex. 1002, ¶62.) The structure shown in figure 4C of Fukunaga results from removing the exposed portion of the barrier layer 14 on the insulating film 10 shown in figure 4B, where the distance D in the example illustrated in figures 4A-4C is less than the sum of the thicknesses T_1 and T_2 ($D < T_1 + T_2$). (Ex. 1002, ¶63.) This is apparent from figures 4A and 4B, where, as shown in further annotated figure 4B below, both T_1 and T_2 extend over a portion of the barrier layer 14. (*Id.*)



(Ex. 1005, FIG. 4B (annotated); Ex. 1002, ¶63.)

The demonstrative below is based on figure 4B of Fukunaga, where, as disclosed by Fukunaga, the distance D shown in figure 4B above has been increased to be approximately equal to the thickness T_1 of barrier layer 14 plus the thickness T_2 of metal film 20 ($D \approx T_1 + T_2$). (Ex. 1002, ¶64.)

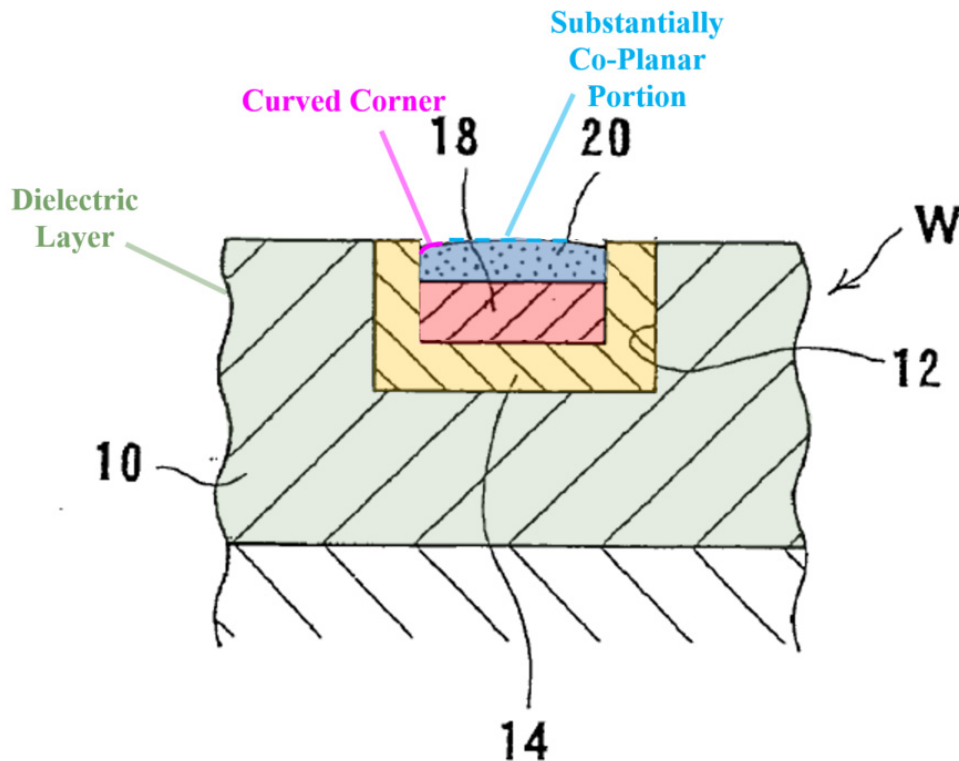


(Id.)

Fukunaga further discloses that after formation of the metal film 20, the barrier layer 14 exposed on the top surface of the substrate is removed, where because the distance D is approximately equal to the thickness of the barrier layer 14 and the metal film 20, after removal of the exposed portions of the barrier layer 14, the top surface of the substrate is flat. (Ex. 1005, ¶[0063]; Ex. 1002, ¶65.)

The demonstrative below is based on the demonstrative above where the distance D is approximately equal to $T_1 + T_2$, and where the exposed portion of the barrier layer 14 has been removed in the same manner disclosed by Fukunaga with respect to the transition between figure 4B and figure 4C. (Ex. 1002, ¶66.) As

shown, the metal film 20 (“second conductive material”) has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer 10, where, as disclosed by Fukunaga, that results in the surface of the substrate W being “flat” where there is no protrusion of the metal film 20 after removal of the barrier layer 14. (Ex. 1005, ¶¶[0017], [0061], [0063], FIGs. 4A-4C; Ex. 1002, ¶66.)



(Ex. 1002, ¶66.)

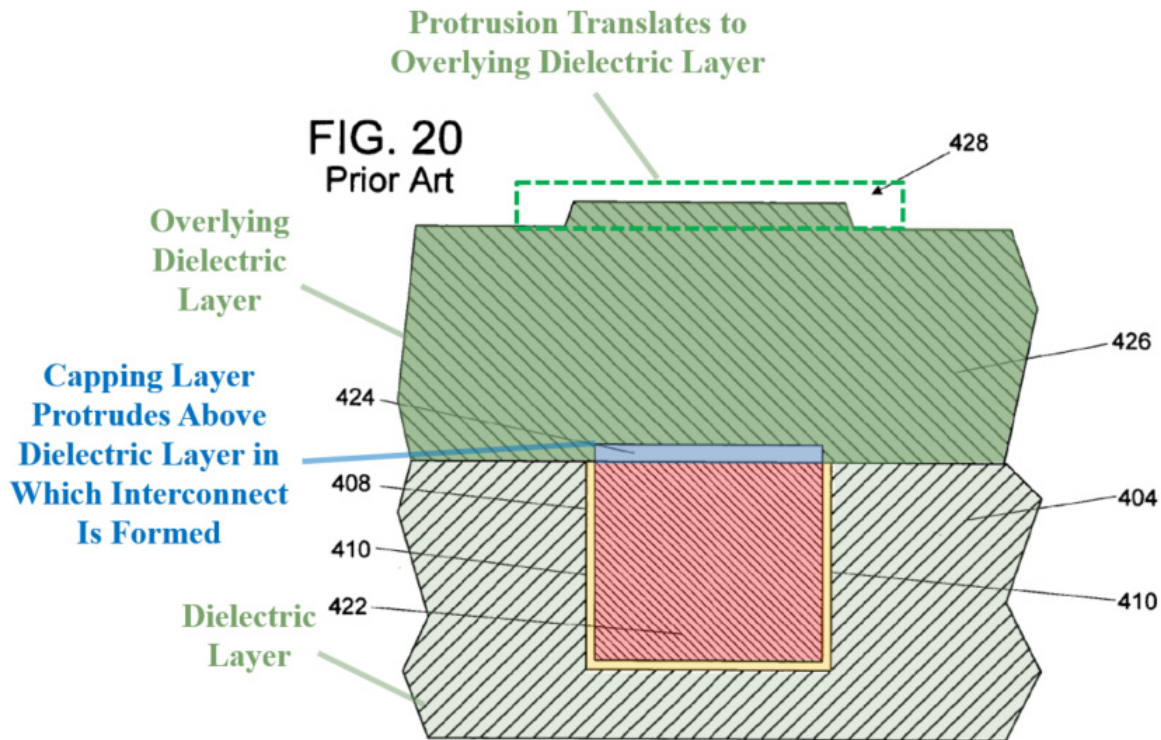
Moreover, as is consistent with the formation of the metal film 20 by electroless plating as disclosed by Fukunaga, the upper surface of the metal film 20

(“second conductive material”) has a curved corner below the portion of the upper surface of the dielectric layer 10.⁵ (Ex. 1005, ¶¶[0005], [0009], [0053], FIGs. 1D, 3B, 4B, 5B; Ex. 1012, ¶[0005] (“Typically, the cobalt films are deposited on the copper by electroless plating. The plating process may produce a cobalt film having a mushroom shaped profile.”); Ex. 1009, 7:4-9, 8:47-52, 9:35-36, FIG. 6B; Ex. 1002, ¶67.)

To the extent that PO argues that Fukunaga does not explicitly disclose that “the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer,” such a feature would have been obvious in view of the knowledge of a POSITA and Park. (Ex. 1002, ¶69.) Fukunaga’s metal film 20 is analogous to Park’s capping layer 128, as both are deposited in the dielectric trench to form a cap overlying the recessed interconnect lines, where metal film 20 and capping layer 128 are cobalt-alloys that protect the underlying lines. (Ex. 1005, ¶[0005]; Ex. 1002, ¶70.) Park discloses

⁵ The ’183 patent does not include any description of a “curved corner” resulting from formation of the capping layer, and the only possible support is in figures 2H and 3B. (Ex. 1002, ¶68.)

that “[t]he recessed capping layer 128 is preferably formed to fill the recess 124 such that a first surface 130 of the **recessed capping layer 128 is substantially planar to the first dielectric material layer first surface 114**. (Ex. 1006, ¶[0023]; *see also id.*, claims 1, 4, 10, 18.) Park further discloses that if the capping layer has an elevation difference compared to the dielectric layer and protrudes above it, that elevation difference is translated into overlying layers, resulting in non-planar topography. (*Id.*, ¶¶[0007]-[0008], FIG. 20; Ex. 1002, ¶70.)



(Ex. 1006, FIG. 20 (annotated); Ex. 1002, ¶70.)

Park further discloses that such topography changes are undesirable and interfere with the formation of subsequent layers. (Ex. 1006, ¶[0008]; *see also id.*, Abstract, ¶¶[0002], [0010], [0017]; Ex. 1002, ¶71.) Therefore, to the extent not already disclosed or suggested by Fukunaga, a POSITA would have found it obvious to make the top surface of the metal film 20 substantially planar with the top surface of the dielectric layer 10 in order to avoid topographical changes as taught by Park. (Ex. 1002, ¶71.)

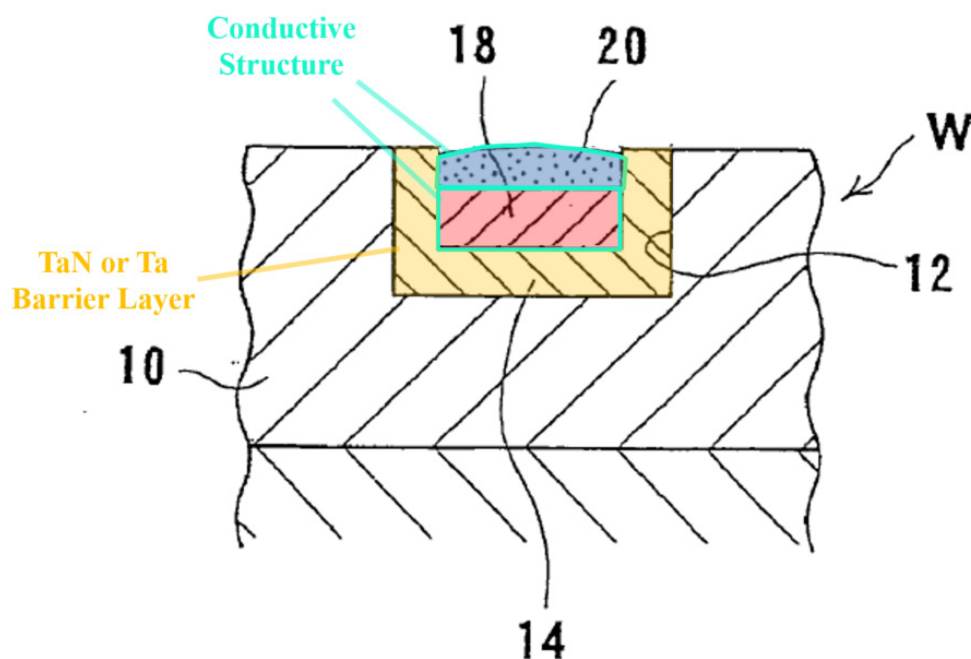
Therefore, the Fukunaga-Park combination discloses or suggests claim element 1[e].

f) “a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”

The Fukunaga-Park combination discloses or suggests this feature to the extent it can be understood.⁶ (Ex. 1002, ¶72.) For example, Fukunaga discloses forming a barrier layer 14 in the recesses of the insulating film, where interconnect

⁶ While it is unclear what constitutes “partially surrounding,” Petitioner understands that a barrier layer that is in contact with the conductive structure and surrounds the conductive structure on three sides satisfies this limitation. Petitioner, however, does not concede that claim 1 is not indefinite.

18 (“first conductive material”) and metal film 20 (“second conductive material”) of the conductive structure are formed within the recesses such that barrier layer 14 partially surrounds the conductive structure. (Ex. 1005, ¶¶[0013], [0048], [0062], FIGs. 4A-4C; Ex. 1002, ¶72.) As shown in the demonstrative discussed above for claim element 1[e], which is replicated and further annotated below, the barrier layer 14, which Fukunaga discloses is tantalum nitride (TaN) or tantalum (Ta) (Ex. 1005, ¶[0048]), partially surrounds the conductive structure.



(Ex. 1002, ¶72.)

2. Claim 2

“The integrated circuit structure of claim 1, wherein the barrier layer further comprises nitrogen.”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶73.) Fukunaga discloses a barrier layer 14 made of tantalum-nitride, which includes tantalum (Ta) and nitrogen (N). (Ex. 1005, ¶[0048]; Ex. 1002, ¶73.)

3. Claims 3-8

Claim 3: “The integrated circuit structure of claim 1, wherein the second conductive material further comprises boron.”

Claim 4: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises phosphorus.”

Claim 5: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten.”

Claim 6: “The integrated circuit structure of claim 3, wherein the second conductive material further comprises tungsten and phosphorus.”

Claim 7: “The integrated circuit structure of claim 1, wherein the second conductive material further comprises phosphorus.”

Claim 8: “The integrated circuit structure of claim 7, wherein the second conductive material further comprises tungsten.”

Fukunaga in view of Park discloses or suggests these features. (Ex. 1002, ¶¶74-82.) Claims 3-8 recite various cobalt-containing alloys used for the second conductive material, which corresponds to metal film 20 that serves as a capping layer in the Fukunaga-Park combination. Cobalt containing alloys like those recited in claims 3-8 were well-known and widely-used in the industry as capping layers for copper interconnect like the metal film 20 in Fukunaga and capping layer 128 in Park, and a POSITA would have found it obvious to use such alloys for metal film 20. (*Id.*, ¶74.)

Fukunaga discloses that metal film 20 (“second conductive material”) can be made of a cobalt alloy. (Ex. 1005, ¶[0062] (“a metal film (protective film) 20 of, for example, a cobalt alloy”).) Fukunaga does not expressly disclose that the cobalt-alloy metal film 20 includes one or more of boron, phosphorus, or tungsten, but Park discloses using such alloys for a very similar capping layer in a very similar interconnect structure, and a POSITA would have found it obvious to include one or more of boron, phosphorus, and tungsten in the cobalt alloy used for the metal film in the Fukunaga-Park combination discussed above for claim 1. (Ex. 1002, ¶75.)

As discussed above for claim element 1[b], Fukunaga and Park are both directed to copper interconnect structures embedded in low-k materials, where a protective capping layer (i.e., metal film 20 in Fukunaga and capping layer 128 in

Park) overlies recessed copper interconnect. (*Supra* sections IX.A.1(b), (e).) Both Fukunaga and Park disclose that the capping layer can be formed of cobalt alloys. (Ex. 1005, ¶¶[0005], [0062]; Ex. 1006, ¶[0027]; Ex. 1002, ¶76.) Park further discloses that the capping layer can be formed of cobalt alloys that include one or more of boron (B), phosphorus (P), and tungsten (W):

The cobalt is deposited by electroless plating to fill the recess 124 (about 10 nm) to form the recessed capping layer 128. The **cobalt may, of course, also be any binary, ternary, or quaternary cobalt alloy containing tungsten, phosphorus, boron,** molybdenum, rhenium, or the like.

(Ex. 1006, ¶[0027]; *see also id.*, claims 16 and 17; Ex. 1002, ¶¶76-77.)

A POSITA implementing the interconnect structure of the Fukunaga-Park combination discussed above for claim 1 would have found it obvious to implement the cobalt-alloy capping layer to include one or more of boron, phosphorus, and tungsten as disclosed by Park. (Ex. 1002, ¶78.) While Fukunaga discloses using “cobalt alloys” as the metal film 20 forming the capping layer, Fukunaga does not specifically disclose the other elements included with cobalt in the cobalt alloys. Park discloses a similar capping layer 128 used in a very similar interconnect structure and explicitly discloses additional elements that can be included in the

cobalt alloys used for such a capping layer. Therefore, a POSITA would have had good reason to look to Park for specifics as to suitable cobalt alloys and would have found it obvious to implement the cobalt alloys as disclosed by Fukunaga according to the teachings of Park. (*Id.*)

Such a POSITA would also have been motivated to use a cobalt alloy that includes boron, phosphorus, and tungsten in the various combinations recited in claims 3-8 because the use of such alloys for capping layers in similar interconnect structures was well-known and widely-practiced in the art. (Ex. 1012, ¶[0018]; Ex. 1009, 5:50-53; Ex. 1014, ¶[0028]; Ex. 1015, ¶[0017]; Ex. 1002, ¶79.)

A POSITA would have found it straightforward to use, and had a reasonable expectation of success in using, cobalt alloys that include one or more of boron, phosphorus, and tungsten as recited in claims 3-8 as the cobalt-containing alloy for the metal film in the Fukunaga-Park combination as because Park explicitly discloses the use of such alloys and they were in common use. (Ex. 1002, ¶80.) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. (*Id.*) See *KSR* at 416-18.

Notably, the '183 patent simply provides an extensive list of different materials and combinations of materials that can be included in the second

conductive material and does not provide any specific disclosure regarding any advantages, criticality, or unexpected results related to the different combinations of materials recited in claims 3-8. (Ex. 1001, 9:35-48; Ex. 1002, ¶81.)

Therefore, the Fukunaga-Park combination discloses or suggests that the second conductive material includes cobalt as well as boron, phosphorus, and tungsten in the various combinations recited in claims 3-8. (Ex. 1002, ¶82.)

4. Claim 9

a) “A method of fabricating an integrated circuit structure, the method comprising:”

To the extent the preamble is limiting, Fukunaga discloses a “method of fabricating an integrated circuit structure.” (Ex. 1002, ¶83.) For example, Fukunaga discloses how to form the interconnect structure (“integrated circuit structure”) discussed above with respect to claim element 1[e]. (*Supra* claim elements 1[a], 1[e]; Ex. 1005, Abstract, ¶¶ [0002], [0005] [0007], [0060], [0074]; Ex. 1002, ¶83.)

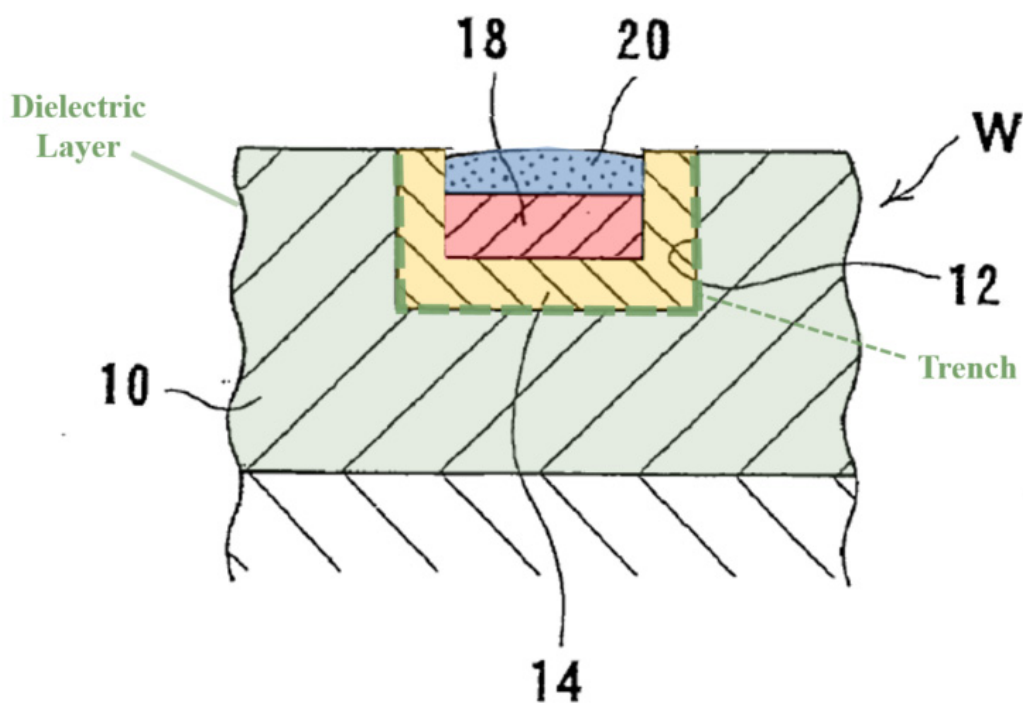
b) “forming a dielectric layer comprising silicon, oxygen and carbon;”

Fukunaga in view of Park discloses or suggests this claim feature. (Ex. 1002, ¶84.) As discussed above for claim element 1[b], Fukunaga discloses forming insulating film 10 (“dielectric layer”) such that it includes silicon (Si), oxygen (O),

and carbon (C). (Ex. 1005, ¶¶[0007], [0048]; *supra* section IX.A.1(b); Ex. 1002, ¶84.)

c) “forming a trench in the dielectric layer;”

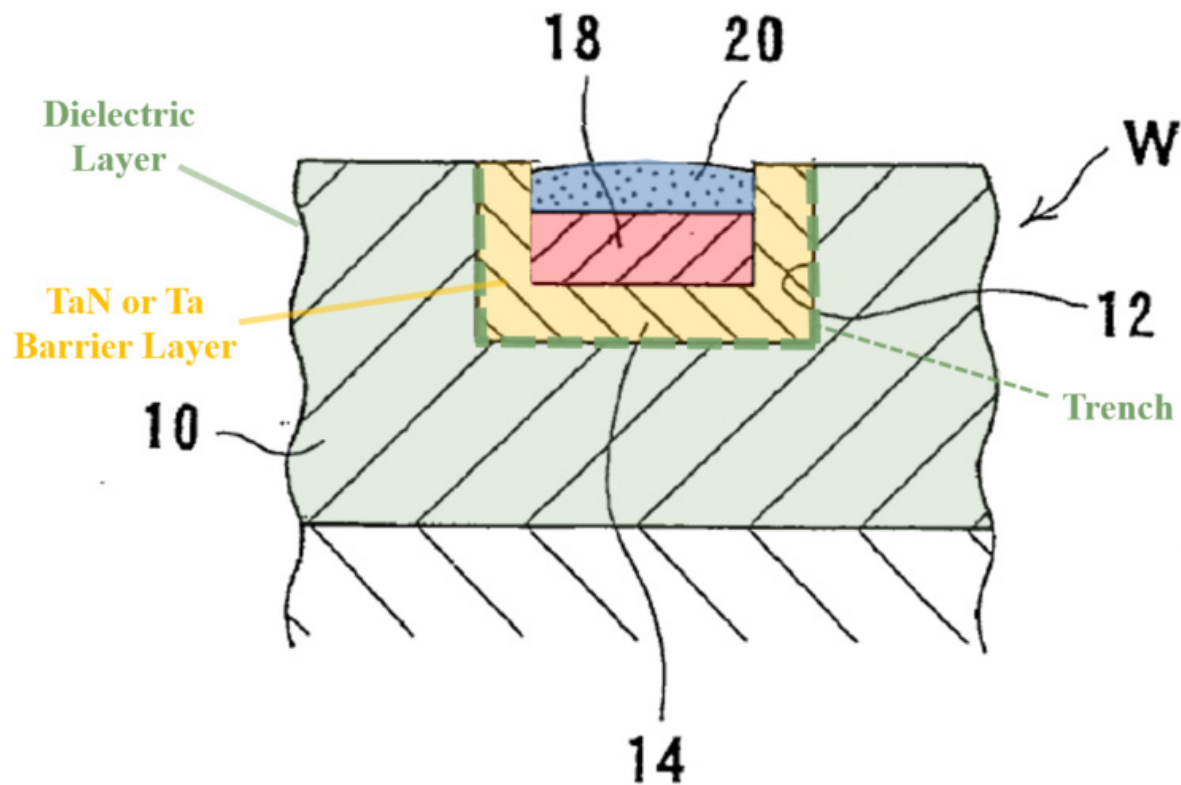
The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶85.) As shown in the demonstrative below corresponding to the embodiment discussed above for claim element 1[e], Fukunaga discloses forming a trench 12 in the insulating film 10 (“dielectric layer”). (Ex. 1005, ¶[0048]; *Supra* section IX.A.1(e).)



(Ex. 1002, ¶85.)

d) “forming a barrier layer in the trench, the barrier layer comprising tantalum;”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶86.) As discussed above for claim element 1[f] and shown in the demonstrative below, Fukunaga discloses forming a tantalum (Ta) or tantalum nitride (TaN) barrier layer 14 in the recesses (“trench”) of the insulating film. (Ex. 1005, ¶¶[0013], [0048]; *supra* section IX.A.1(f).)

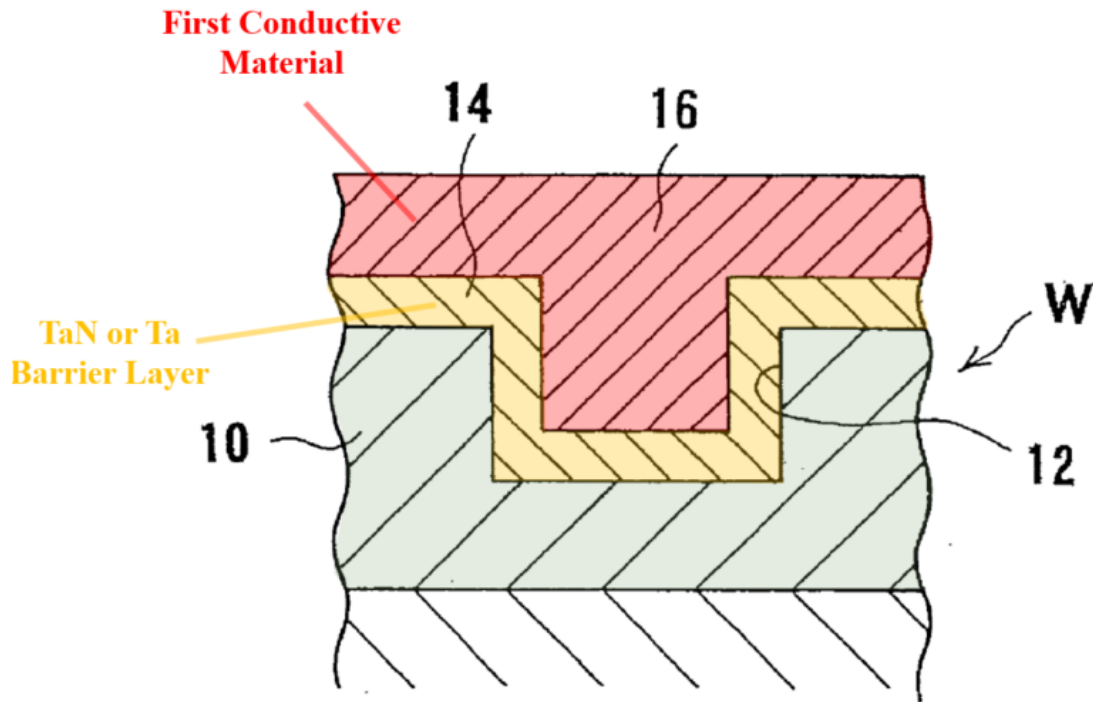


(Ex. 1002, ¶86.)

- e) “forming a first conductive material within the barrier layer, the first conductive material comprising copper;”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶87.) Fukunaga discloses that “[a] film of copper (interconnect material) 16 is formed ... over the surface of the substrate W, thereby embedding copper in the trenches (interconnect recesses) 12.” (Ex. 1005, ¶[0048]; *see also id.*, ¶¶[0049], [0060], FIG. 2.)

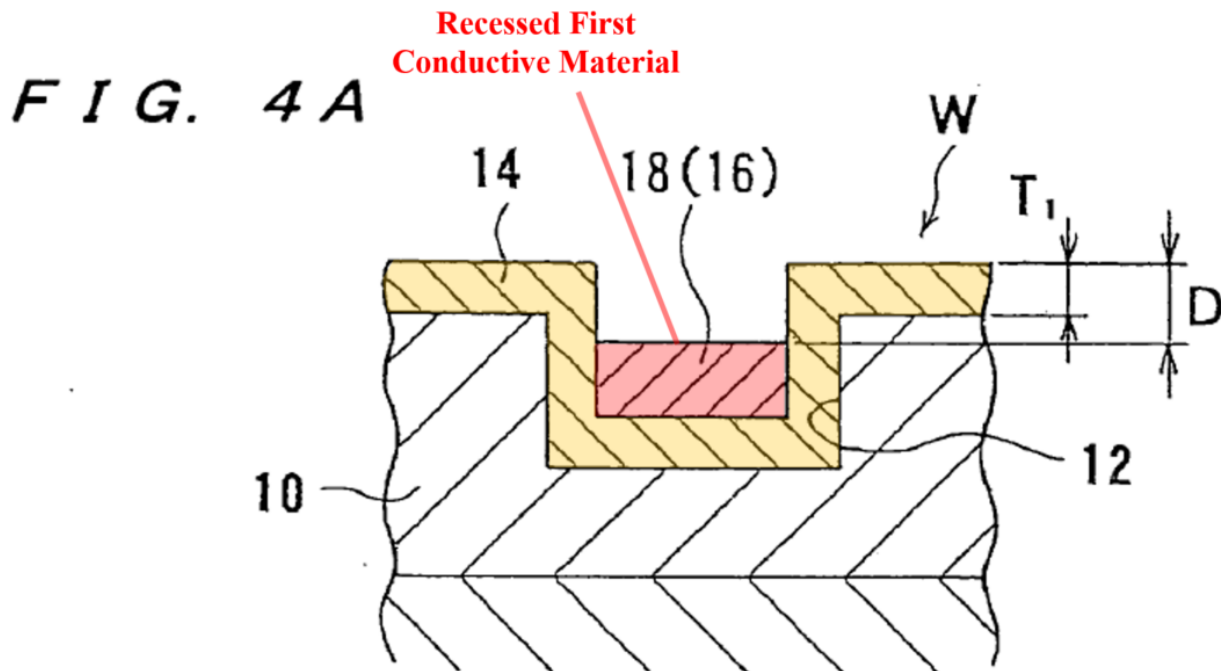
FIG. 2



(*Id.*, FIG. 2 (annotated); Ex. 1002, ¶87.)

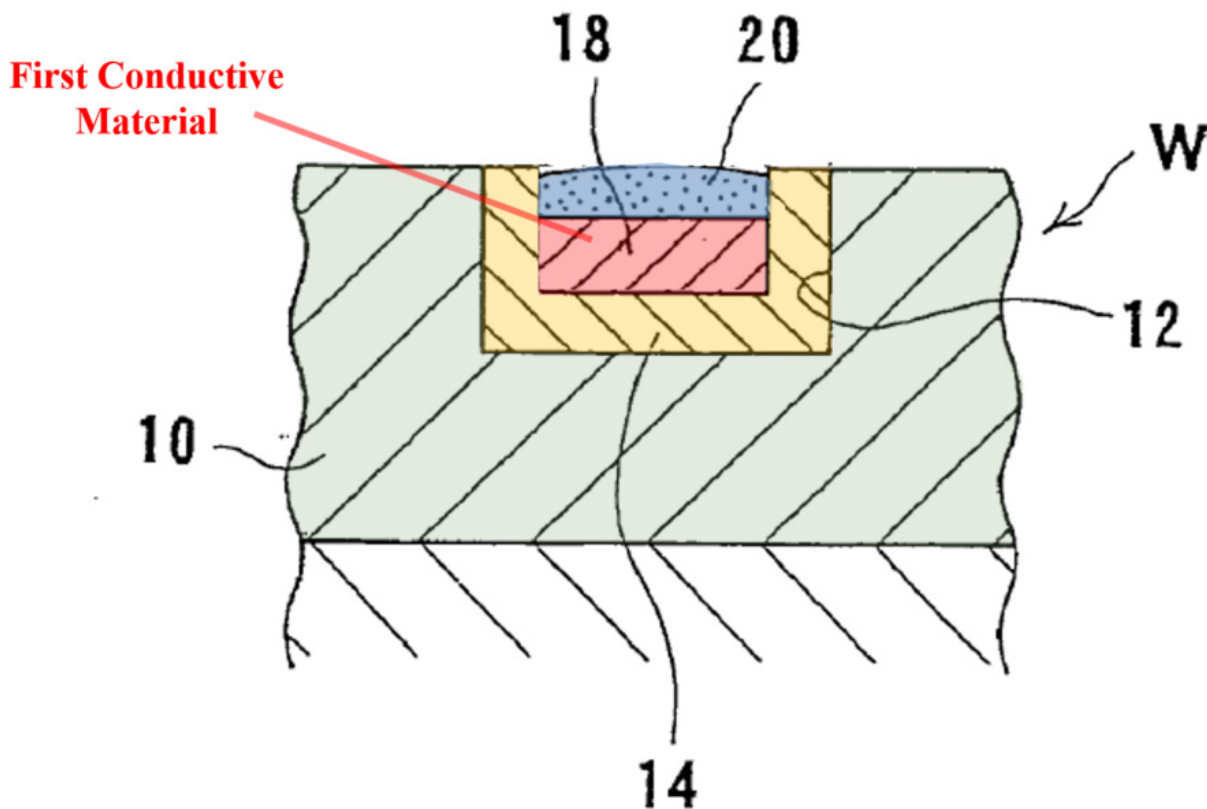
f) “recessing the first conductive material below a portion of an upper surface of the dielectric layer; and”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶¶88-90.) As shown in annotated figure 4A below, Fukunaga discloses recessing interconnect material 16 (“first conductive material”) to form a channel below the upper surface of the dielectric layer. (Ex. 1005, ¶[0060] (“polishing or etching of interconnects 18 is further continued so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.”); Ex. 1002, ¶88.)



(Ex. 1005, FIG. 4A (annotated); Ex. 1002, ¶89.)

As discussed above for claim element 1[e], Fukunaga discloses the distance D between the top surface of the barrier layer and the top surface of the recessed interconnect 18 is preferably approximately equal to the sum of the thickness of the barrier layer 14 and the thickness of the subsequently deposited metal film 20. (*Supra* section IX.A.1(e).) The demonstrative below, which corresponds to the embodiment discussed above for claim element 1[e], shows the interconnect 18 recessed according to such a preferred scenario. (Ex. 1002, ¶90.)

 $(Id.)$

g) “forming a second conductive material on the upper surface of the recessed first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a position where the first conductive material and the second conductive material meet, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer.”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶91.) For example, Fukunaga discloses forming metal film 20 (“second conductive material”), where, as discussed above for claim element 1[e], the Fukunaga-Park combination discloses or suggests forming the metal film 20 such that (1) the metal film 20 is on the upper surface of the recessed first conductive material, (2) the metal film 20 comprises cobalt, (3) the interconnect 18 and metal film 20 have the same width at a position where they meet, and (4) the upper surface of the metal film has a curved corner below the portion of the upper surface of the dielectric layer. (*Supra* section IX.A.1(e); Ex. 1002, ¶91.)

5. Claim 10

“The method of claim 9, wherein recessing the first conductive material below the portion of the upper surface of the dielectric layer comprises using a wet etch process.”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶¶92-96.) Fukunaga discloses that, after depositing the copper 16, wet etching is

used to remove extra copper 16 (“first conductive material”) above the top surface of the barrier layer 14 so that the surfaces of interconnects 18 in the trenches is flush with the top surface of the barrier layer. (Ex. 1005, ¶[0050], ¶[0051] (“The removal of the extra copper 16 may also be carried out by etching using an inorganic or organic acid.”); Ex. 1002, ¶92.) A POSITA would have understood that etching using acid is “wet etching.” (Ex. 1002, ¶92.)

Fukunaga further discloses that “**etching of interconnects 18 is further continued** so that the surfaces of interconnects 18 formed in the trenches 12 become lower than the surface of the exposed barrier layer 14.” (Ex. 1005, ¶[0060].) As such, a POSITA would understand that Fukunaga discloses or suggests using wet etching to remove the extra copper on the surface of the barrier layer and then continuing that same etching to recess the surface of the interconnects 18. (Ex. 1002, ¶93.) Therefore, the Fukunaga-Park combination discloses or suggests claim 10. (*Id.*)

To the extent PO argues that Fukunaga does not explicitly disclose that wet etching is used to further etch and recess interconnects 18, using wet etching to continue etching of the interconnects would have been obvious. (Ex. 1002, ¶94.) A POSITA would have understood that using the same acid wet etch to remove both

the extra copper outside of the trench as well as the copper in the trench to recess the interconnect would require fewer process steps and simplify manufacturing. (*Id.*)

Moreover, Fukunaga discloses that wet etching is a preferred form of etching for such material removal as no load is applied to the substrate by such etching, and, in the case where porous low-k dielectric materials are included in the structure, load-applying material removal processes (e.g. chemical mechanic polishing) are less desirable as they can damage the wafer. (Ex. 1005, ¶[0057]; Ex. 1002, ¶94.) A POSITA would also have known that wet-etching, as taught by Fukunaga, was a well-known etching technique for etching recesses in interconnect material like the copper interconnect of Fukunaga. (Ex. 1007, ¶[0038]; *see also id.*, ¶¶[0007]-[0008]; Ex. 1011, ¶[0066]; Ex. 1002, ¶95.) Therefore, for these additional reasons, a POSITA would have found it obvious to perform the etching disclosed by Fukunaga as wet etching. (Ex. 1002, ¶96.)

6. Claim 11

“The method of claim 9, wherein the barrier layer further comprises nitrogen.”

The Fukunaga-Park combination discloses or suggests this feature for the same reasons discussed above with respect to claim 2. (*Supra* section IX.A.2; Ex. 1002, ¶97.)

7. Claims 12-17

Claim 12: “The integrated circuit structure of claim 9, wherein the second conductive material further comprises boron.”

Claim 13: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises phosphorus.”

Claim 14: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises tungsten.”

Claim 15: “The integrated circuit structure of claim 12, wherein the second conductive material further comprises tungsten and phosphorus.”

Claim 16: “The integrated circuit structure of claim 9, wherein the second conductive material further comprises phosphorus.”

Claim 17: “The integrated circuit structure of claim 16, wherein the second conductive material further comprises tungsten.”

The Fukunaga-Park combination discloses or suggests these features for the same reasons discussed above with respect to claims 3-8. (*Supra* section IX.A.3; Ex. 1002, ¶¶98.)

8. Claim 18

a) “A computing device, comprising:”

To the extent the preamble is limiting, the Fukunaga-Park combination discloses or suggests “a computing device.” (Ex. 1002, ¶¶99-103.) As discussed

above for claim element 1[b], Fukunaga and Park disclose similar interconnect structures that include a capping layer formed on a recessed interconnect line. (*Supra* section IX.A.1(b).) While Fukunaga discloses that the interconnect structure can be used in semiconductor devices (Ex. 1005, ¶[0004]), Fukunaga does not explicitly disclose using the interconnect structure in a “computing device.” Park, however, discloses a very similar interconnect structure used in a computing device, and a POSITA would have found it obvious to use the interconnect structure of the Fukunaga-Park combination discussed above for claim 1 in a “computing device” as disclosed by Park. (Ex. 1002, ¶99.)

Park discloses using the interconnect structure in, for example, a cell phone 210 shown in figure 10 and a computer system 310 shown in figure 11. (Ex. 1006, ¶¶[0010]-[0011], ¶[0028] (“The packages formed with the interconnect having recessed capping layer of the present invention may be used in a hand-held device 210, such as a cell phone or a personal data assistant (PDA), as shown in FIG. 10.”), ¶[0029], FIGs. 10, 11; Ex. 1002, ¶100.)

FIG. 10

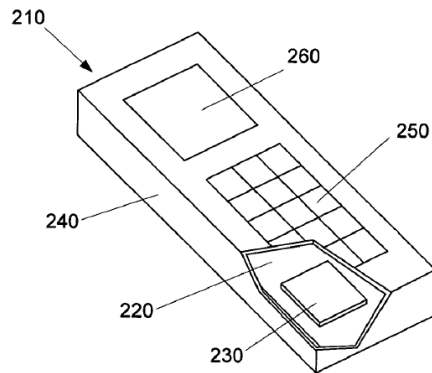
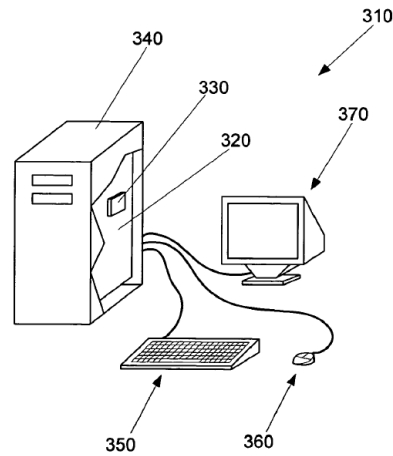


FIG. 11



(Ex. 1006, FIGs. 10, 11.)

Based on Park's disclosure of the use of the interconnect structure in cell phone or computer system, a POSITA would have found it obvious to use the interconnect structure of the Fukunaga-Park combination in a cell phone or computer system (each a "computing device"). (Ex. 1002, ¶101.) While Fukunaga does not explicitly disclose the semiconductor devices in which the interconnect structure is used, a POSITA would have understood that the interconnect structure, which is designed to allow for high-speed propagation of signals on interconnect for semiconductor devices with small-geometry features, is well-suited for use in computing devices like those disclosed by Park. (*Id.*) A POSITA would have found it obvious to use the Fukunaga-Park interconnect structure discussed above for claim 1 in such computing devices as disclosed by Park, as such use would have increased

the utility of such an interconnect structure through its implementation in such computing devices and provided the benefit of more reliable operation for the computing devices. (*Id.*)

Computing devices that include the Fukunaga-Park interconnect structure would have been a predictable combination of known components according to known methods (*e.g.*, applying the teachings of Park regarding using interconnect structures like those of Fukunaga and Park in computing devices), and would have produced the predictable result of a computing device that includes interconnect capping layers on recessed interconnect with the advantages disclosed by Fukunaga and Park. (*Id.*, ¶102.) *See KSR*, 416.

Based on Park's disclosure and their knowledge, a POSITA would have had a reasonable expectation of success in implementing the interconnect structure in such computing devices, as they would have understood how to use the interconnect structure to connect different circuit elements within the integrated circuits of the computing devices. (Ex. 1002, ¶103.) Indeed, the '183 patent simply identifies various components (*e.g.* processor, memories, etc.) and states that they include "at least one conductive line in a dielectric layer over a substrate, a channel in the dielectric layer over the one conductive line; and a capping layer on the at least one conductive line in the channel to prevent electromigration, as described herein."

(Ex. 1001, 10:39-52.) The '183 patent does not provide any more specific implementation details regarding the use of the interconnect in the components, thereby evidencing that a POSITA would have understood how to, and been able to, successfully incorporate the interconnect structure in such components. (Ex. 1002, ¶103.)

b) “a board;”

The Fukunaga-Park combination discloses or suggests this claim feature. (Ex. 1002, ¶104.) For example, Park discloses that the cell phone and computer system include a substrate or motherboard (“board”) on which integrated circuits are interconnected. (Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an **external substrate 220** with at least one microelectronic device assembly 230, including but not limited to, a central processing units (CPUs), chipsets, memory devices, ASICs, and the like, having at least one recessed capping layer as described above, within a housing 240.”), ¶[0029]; Ex. 1002, ¶104.)

FIG. 10

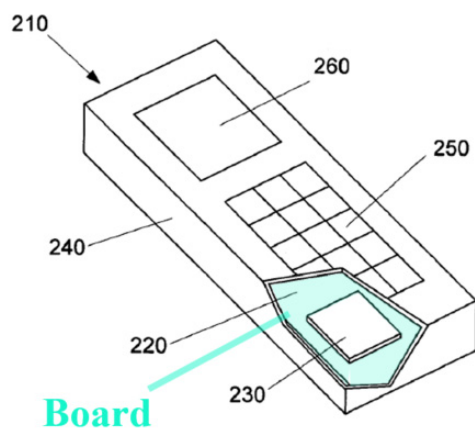
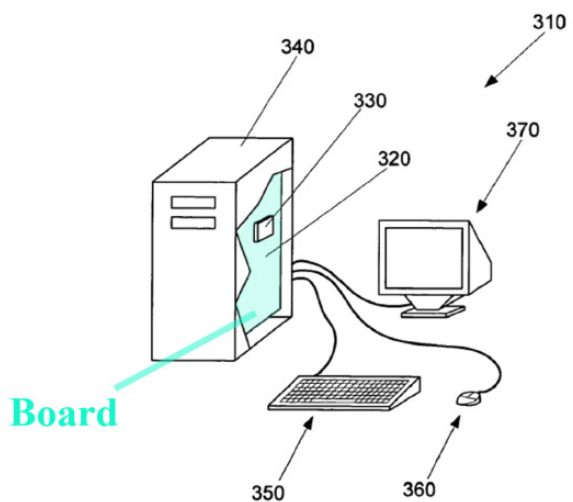


FIG. 11



(Ex. 1006, FIGs. 10, 11 (annotated); Ex. 1002, ¶104.)

- c) **“a component coupled to the board, the component including an integrated circuit structure, comprising:”**
- d) **“a dielectric layer having an upper surface, the dielectric layer comprising silicon, oxygen, and carbon;”**
- e) **“a conductive structure in the dielectric layer, the conductive structure comprising:”**
- f) **“a first conductive material comprising copper, the first conductive material having an upper surface, with a portion of the upper surface of the first conductive material below a portion of the upper surface of the dielectric layer; and”**
- g) **“a second conductive material on the upper surface of the first conductive material, the second conductive material comprising cobalt, wherein the first conductive material and the second conductive material have a same width at a location where the first conductive material and the second conductive material meet, wherein the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer; and”**
- h) **“a barrier layer partially surrounding the conductive structure, the barrier layer comprising tantalum.”**

The Fukunaga-Park combination discloses or suggests these features. (Ex. 1002, ¶¶105-106.) For example, Park discloses that the boards of the cell phone and computer system include a central processing unit (CPU) (“component”). (Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an external substrate 220 with at

least one microelectronic device assembly 230, including ... **a central processing units (CPUs) ... having at least one recessed capping layer as described above**”), ¶[0029]; Ex. 1002, ¶105.) The CPU is on the board and therefore “coupled to the board.” (Ex. 1002, ¶105.)

FIG. 10

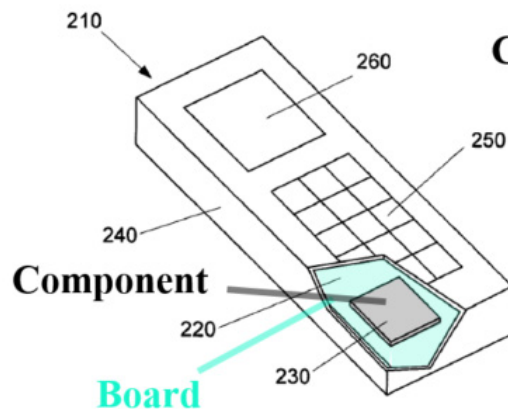
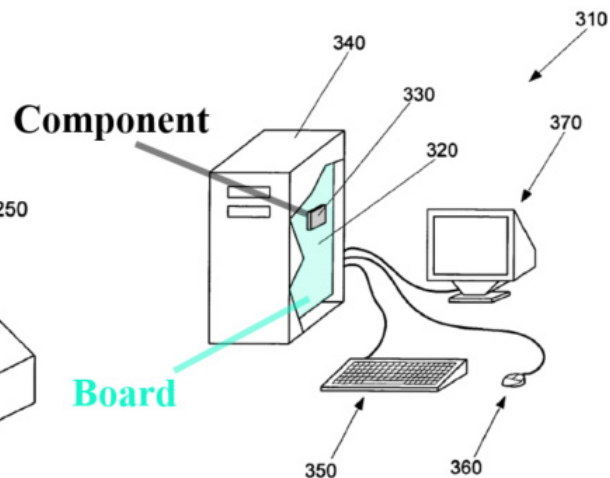


FIG. 11



(Ex. 1006, FIGs. 10, 11 (annotated); Ex. 1002, ¶105.)

As discussed above with respect to claim element 18[a], it would have been obvious to use the interconnect structure according to the Fukunaga-Park combination discussed above for claim 1 in the components of the computing devices shown in figures 10 and 11 of Park. (*Supra* section IX.A.8(a).) Therefore, the CPU of the computing device (“component”), which includes those interconnect structures, includes the “dielectric layer,” the “conductive structure,” the “first

conductive material,” the “second conductive material,” and the “barrier layer” recited in claim elements 18[d]-18[h] for the same reasons discussed above for claim elements 1[b]-1[f]. (*Supra* sections IX.A.1(b)-(f); Ex. 1002, ¶106.)

9. Claim 19

**“The computing device of claim 18, further comprising:
a memory coupled to the board.”**

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶107.) For example, Park discloses memories coupled to the boards of the computing devices shown in figures 10 and 11. (Ex. 1006, ¶[0028] (“The hand-held device 210 may comprise an external substrate 220 with at least one microelectronic device assembly 230, including but not limited to ... memory devices”, ¶[0029]; Ex. 1002, ¶107.)

10. Claim 20

**“The computing device of claim 18, further comprising:
a communication chip coupled to the board.”**

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶108.) For example, figure 10 of Park shows a “hand-held device 210, such as a cell phone” that includes multiple components coupled to the substrate 220 (“board”). (Ex. 1006, ¶[0028].) Park does not explicitly disclose that the cell phone includes a “communication chip,” but a POSITA would have found it obvious to include a

communication chip in a cell phone as disclosed or suggested by the Fukunaga-Park combination. (Ex. 1002, ¶108.) A POSITA would have known that cell phones include communications chips in order to communicate with other devices (e.g., to enable Wi-Fi, Bluetooth, and/or cellular radio communications). (*Id.*) Moreover, a POSITA would have had a reasonable expectation of success in including a communications chip in the Fukunaga-Park device. (*Id.*)

11. Claim 21

**“The computing device of claim 18, further comprising:
a camera coupled to the board.”**

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶¶109-110.) For example, Park discloses “hand-held device 210, such as a cell phone” that includes substrate 220 (“board”) attached to “various peripheral devices.” (Ex. 1006, ¶[0028]; Ex. 1002, ¶109.) Park does not explicitly disclose that the cell phone includes a camera, but a POSITA would have found it obvious to include, and would have had a reasonable expectation of success in including, a camera coupled to the board in a cell phone of the Fukunaga-Park combination because cameras were widely used in cell phones at the relevant time and would have increased the utility of the cell phone. (Ex. 1002, ¶110.)

12. Claim 22

**“The computing device of claim 18, further comprising:
a battery coupled to the board.”**

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶¶111-112.) Park discloses a cell phone that includes peripheral devices coupled to the board (*supra* section IX.A.11), but does not explicitly disclose a battery. (Ex. 1002, ¶111.) However, a POSITA would have found it obvious to include, and had a reasonable expectation of success in including, a battery in the Fukunaga-Park cell phone because batteries were widely used in cell phones to provide power to such portable devices and support mobile use. (*Id.*, ¶¶111-112.)

13. Claim 23

**“The computing device of claim 18, further comprising:
an antenna coupled to the board.”**

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶113.) Park discloses a cell phone that includes peripheral devices coupled to the board (*supra* section IX.A.11), but does not explicitly disclose an antenna. However, a POSITA would have found it obvious to include, and had a reasonable expectation of success in including, an antenna in the Fukunaga-Park cell phone because cell phones typically include antennas to allow for communication with other devices. (Ex. 1002, ¶113.)

14. Claim 24

“The computing device of claim 18, wherein the component is a packaged integrated circuit die.”

The Fukunaga-Park combination discloses or suggests this feature. (Ex. 1002, ¶114.) For example, Park discloses that “[t]he **packages** formed with the interconnects having recessed capping layer of the present invention may be used in a hand-held device 210, such as a cell phone.” (Ex. 1006, ¶[0028]; *see also id.*, claim 18 (“at least one **microelectronic device package** attached to said external substrate”); Ex. 1002, ¶114.) Therefore, the Fukunaga-Park combination discloses or suggests that the CPU (“component”) is a microelectronic device package (“packaged integrated circuit die”). (Ex. 1006, ¶[0028]; Ex. 1002, ¶114.)

15. Claim 25

“The computing device of claim 18, wherein the component is selected from a group consisting of a processor, a communications chip, and a digital signal processor.”

The Fukunaga-Park combination discloses or suggests this feature as the “component” discussed above in claim element 18[c] is a CPU (“processor”). (Ex. 1002, ¶115.)

B. Ground 2 – Fukunaga in View of Park and Chan Renders Claim 10 Obvious

1. Claim 10⁷

As discussed above in Section IX.A.5, the Fukunaga-Park combination discloses or suggests using a wet etch to recess interconnects 18. (*Supra* section IX.A.5.) To the extent PO argues that the Fukunaga-Park combination does not disclose or suggest claim 10, using a wet etch would have been obvious in further view of Chan. (Ex. 1002, ¶¶116-123.)

Chan, like Fukunaga and Park, is directed to copper interconnect structures embedded in dielectric material, where a recessed capping layer overlies the copper interconnect. For example, figure 5E of Chan shows copper interconnects 120 formed in trenches of the dielectric layer 82, where cobalt caps 124 cover the top surfaces of the interconnect. (Ex. 1007, ¶¶[0034], [0040]; Ex. 1002, ¶118.)

⁷ The claim language is not repeated.

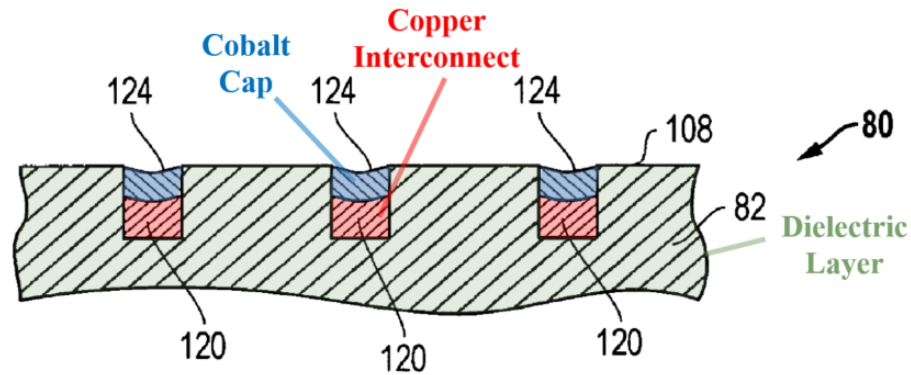


FIG. 5E

(Ex. 1007, FIG. 5E (annotated); Ex. 1002, ¶118.)

Like Fukunaga and Park, Chan discloses recessing copper that initially fills the trenches to form recessed interconnects 120 so that the caps are formed in the trench. (Ex. 1007, ¶¶[0038]-[0039].) Chan discloses that while the copper in the trenches can be recessed by chemical mechanical polishing (CMP), “[t]he recessing effect of chemical-mechanical polishing can vary across the surfaces 22 of copper interconnects 20 as shown in FIG. 1C,” which can result in a dish-like surface. (*Id.*, ¶[0004].) Moreover, Chan also discloses that recesses resulting from CMP are highly dependent on the geometry of the copper interconnects, where the depth of the recess can vary based on pattern density of the interconnect as well as the width of the copper interconnect. (*Id.*, ¶¶[0007]-[0008]; Ex. 1002, ¶119.)

Chan further discloses that using CMP to recess the copper interconnect can also remove portions of the dielectric, which is undesirable, and that shallow

recesses created by CMP can create problems, including lack of complete coverage for copper interconnects by the overlying cobalt capping layers. (Ex. 1007, ¶¶[0009]-[0010]; Ex. 1002, ¶120.) Rather than using CMP to form or deepen the recesses in the copper interconnects, Chan uses an acidic wet etch that does not substantially affect the dielectric layer. (Ex. 1007, ¶[0038]; Ex. 1002, ¶121.)

A POSITA implementing an interconnect structure like that of the Fukunaga-Park combination would have had good reason to look to Chan, particularly because all of these references are in the same field and disclose very similar interconnect structures. (Ex. 1002, ¶122.) Having looked to Chan, a POSITA would have found it obvious to use a wet etch to recess the copper interconnect in the trenches of the Fukunaga-Park combination, as such a wet etch avoids disadvantages resulting from using CMP for such recessing. (*Id.*) Moreover, a POSITA would have found it straightforward to use wet etching as disclosed by Chan, as doing so is nothing more than a straightforward application of a known method (wet etching to recess the copper interconnect as disclosed by Chan) to a similar device (the interconnect of the Fukunaga-Park combination) and would have produced predictable results (recessed interconnect ready for capping). (*Id.*, ¶123.) *See KSR* at 416-18. Moreover, such a skilled person would have had a reasonable expectation of success because Chan discloses using wet etching for a very similar interconnect structure.

Therefore, the Fukunaga-Park-Chan combination discloses or suggests claim 10.
(Ex. 1002, ¶123.)

C. Ground 3 – Fukunaga in View of Park and Song Renders Claims 20-23 Obvious

1. Claims 20-23

As discussed above, the Fukunaga-Park combination discloses or suggests that the hand-held device (e.g. cell phone) (“computing device”) includes components coupled to the board (substrate 220), including a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23). (*Supra* sections IX.A.10-13.) To the extent PO argues that the Fukunaga-Park combination does not disclose or suggest these features, they would have been obvious in further view of Song. (Ex. 1002, ¶¶124-130.)

Neither Fukunaga nor Park explicitly discloses a cell phone that includes a communications chip, camera, battery, or antenna, but Song discloses cell phones that include all of the features recited in claims 20-23, and, in view of Song, a POSITA would have found it obvious to implement the Fukunaga-Park cell phone such that it includes such well-known and widely-used features. (*Id.*, ¶126.)

Song discloses cell phones that include cameras (claim 21) and batteries (claim 22). (Ex. 1008, ¶[0002] (“For example, a wireless telephone can also include **a digital still camera, a digital video camera**, a digital recorder, and an audio file

player. ... However, power consumption of such portable devices can quickly deplete a **battery** and diminish a user's experience."); Ex. 1002, ¶127.)

Similarly, as shown in annotated figure 7 below, Song discloses a cell phone that includes a wireless controller 740 ("communications chip") coupled to an antenna 742. (Ex. 1008, ¶¶[0016], [0030]; Ex. 1002, ¶128.) Song further discloses that the wireless controller 740 is included with the other components in box 722 in a "system-in-package" or a "system-on-chip." Therefore, the wireless controller 740, as a stand-alone chip in the "system-in-package," or the "system-on-chip" that includes the wireless controller 740, is a "communications chip," as such a chip is coupled to the antenna to support communication using the antenna. (Ex. 1008, ¶[0030]; Ex. 1002, ¶128.)

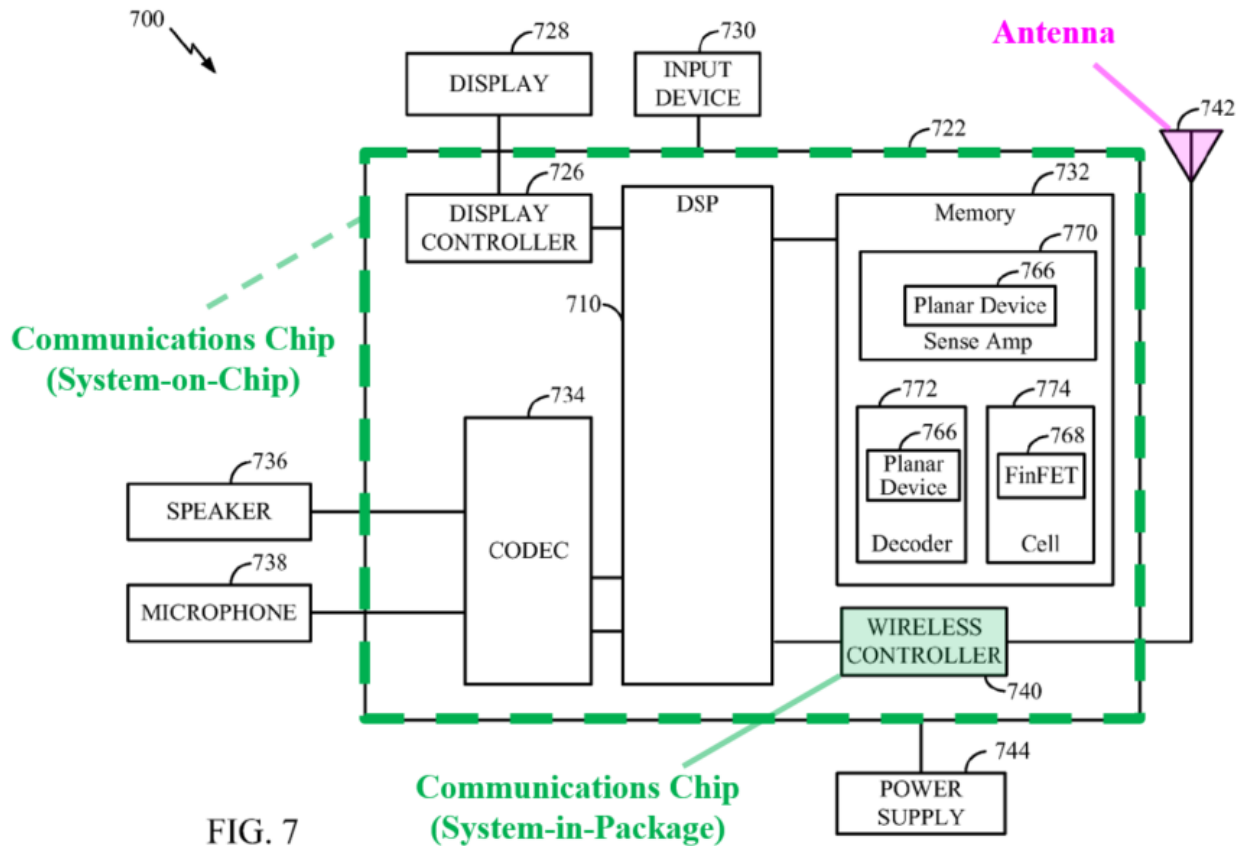


FIG. 7

(Ex. 1008, FIG. 7 (annotated); Ex. 1002, ¶128.)

Park does not disclose all of the details regarding the cell phones that incorporate the interconnect structure, and therefore a POSITA would have had good reason to look to Song, which discloses additional details regarding components included in cell phones. (Ex. 1002, ¶129.) In view of Song and their knowledge of state-of-the art cell phone features, such a POSITA would have found it obvious to include, and had a reasonable expectation of success in including, a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23)

coupled to the board in the cell phone of the Fukunaga-Park combination. (*Id.*) Such a POSITA would have been motivated to include such features in order to enable fundamental operational characteristics of the cell phone (communications using the communications chip and antenna powered by the battery) and provide added utility in the form of the ability to take pictures (camera). (*Id.*) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. (*Id.*) See *KSR* at 416-18. Therefore, the Fukunaga-Park-Song combination discloses or suggests the features of claims 19-23. (*Id.*, ¶130.)

D. Ground 4 – Kawahara Anticipates Claims 1-9 and 11-17

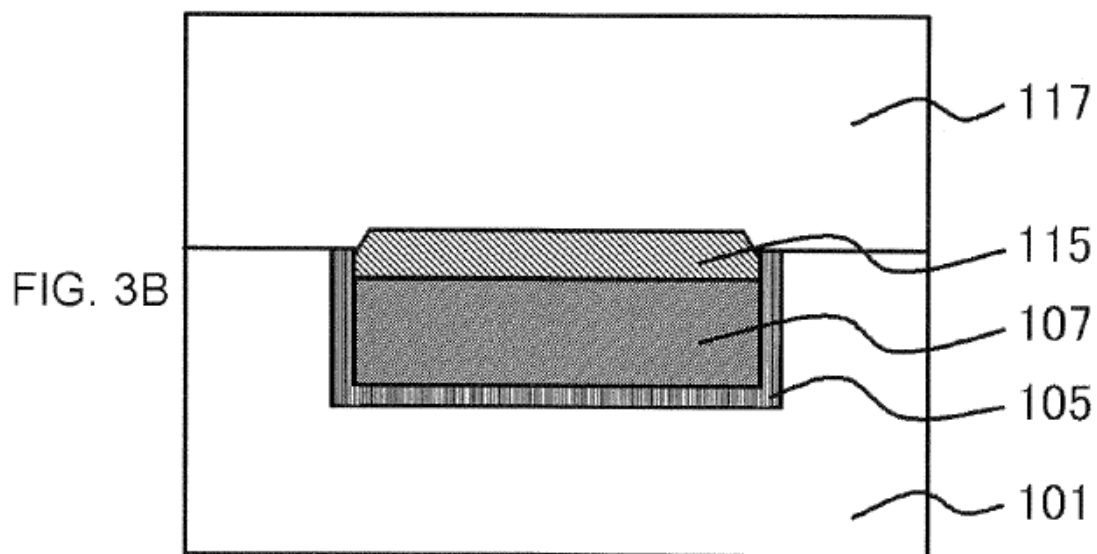
As shown in detail below, Kawahara discloses all of the features recited in claims 1-9 and 11-17 of the '183 patent in a manner consistent with Patent Owner's assertions in litigation. (Ex. 1002, ¶¶131-164.)

1. Claim 1

a) Element 1[a]

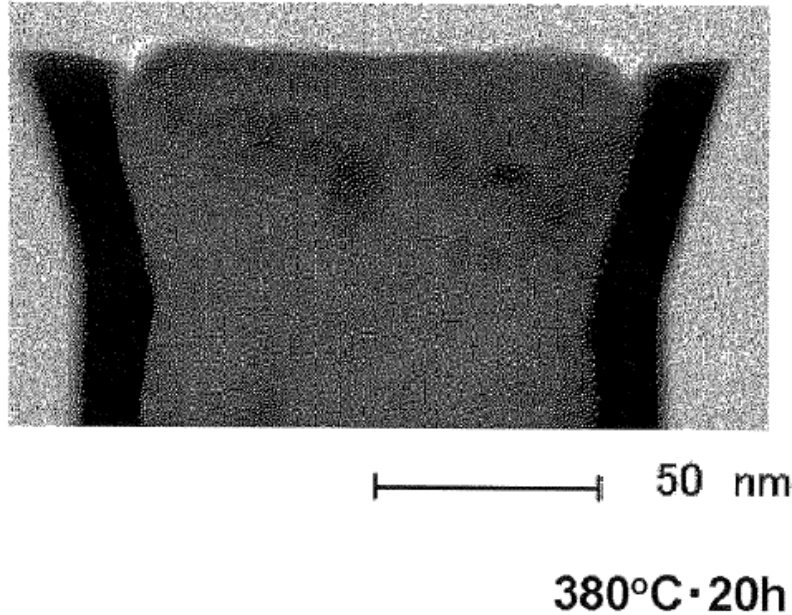
To the extent the preamble is limiting, Kawahara discloses “an integrated circuit structure.” (Ex. 1002, ¶¶132-133.) Kawahara discloses formation of an interconnect structure (“integrated circuit structure”) for semiconductor devices, which are formed on a silicon substrate. (Ex. 1009, 3:1-3, 6:49-52, 9:32-33; Ex.

1002, ¶132.) Figures 3B and 6B of Kawahara below show an interconnect structure included as a part of an integrated circuit. (Ex. 1009, 4:1-3, 6:45-48, 9:36-38; Ex. 1002, ¶133.)



(Ex. 1009, FIG. 3B.)

FIG. 6B

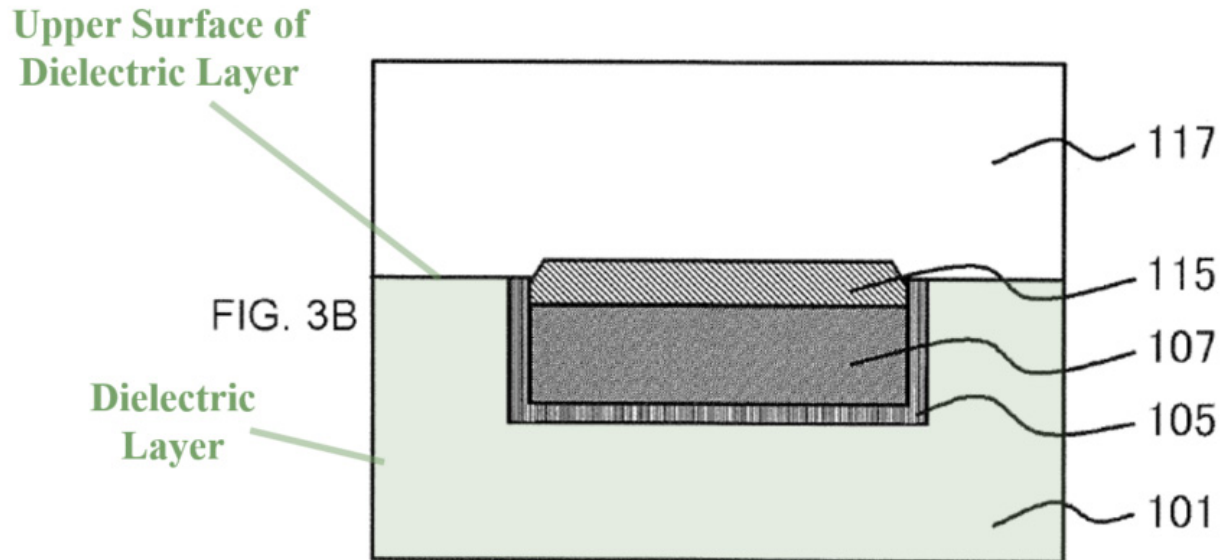


(*Id.*, FIG. 6B.)

b) Element 1[b]

Kawahara discloses claim element 1[b]. (Ex. 1002, ¶¶134-135.) As shown in annotated figure 3B below, Kawahara discloses the interconnect structure includes an insulating layer 101 (“dielectric layer”) having an upper surface. (Ex. 1009, 6:11-17, 6:49-52 (“First of all, as shown in FIG. 2A, the insulating interlayer 101 is formed on the silicon substrate (not shown).”); Ex. 1002, ¶134.)

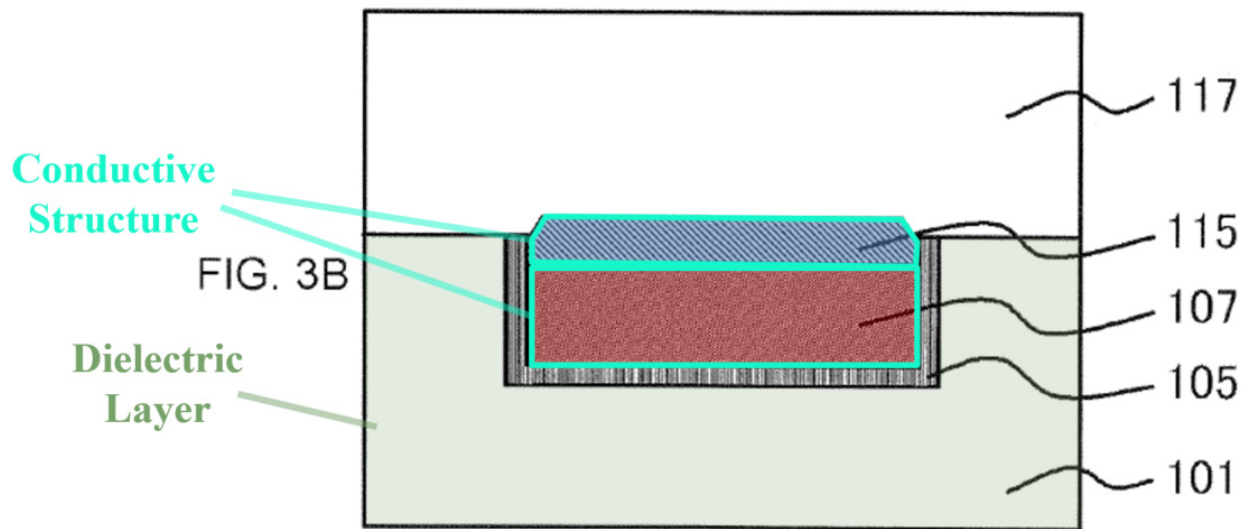
Kawahara further discloses “the insulating interlayer may be a low dielectric constant insulating film such as silicon oxycarbide (SiOC) film,” which includes silicon (Si), oxygen (O), and carbon (C). (Ex. 1009, 5:20-22; Ex. 1002, ¶135.)



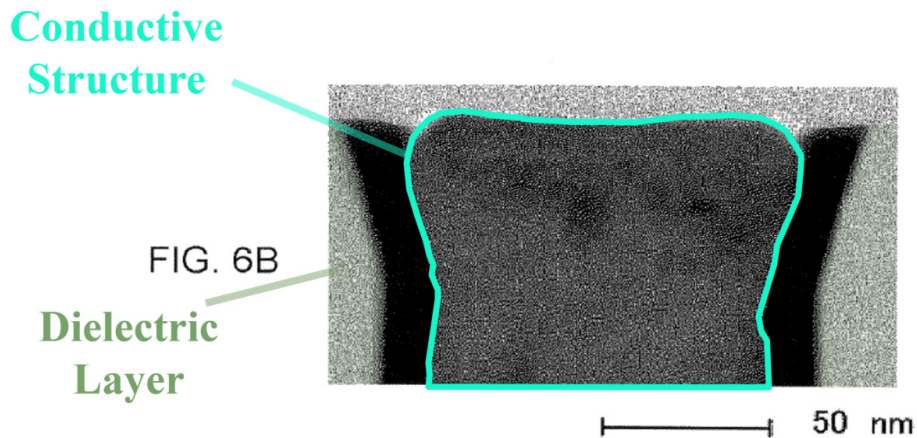
(Ex. 1009, FIG. 3B (annotated); Ex. 1002, ¶135.)

c) Element 1[c]

Kawahara discloses claim element 1[c]. (Ex. 1002, ¶¶136-137.) As shown in annotated figures 3B and 6B below, Kawahara discloses a conductive structure, which includes copper interconnect 107 and electrically conducting protective film 115, in the concave portion of the dielectric layer 101. (Ex. 1009, 4:43-51, 6:62-64; Ex. 1002, ¶¶136-137.)



(Ex. 1009, FIG. 3B (annotated); Ex. 1002, ¶136.)

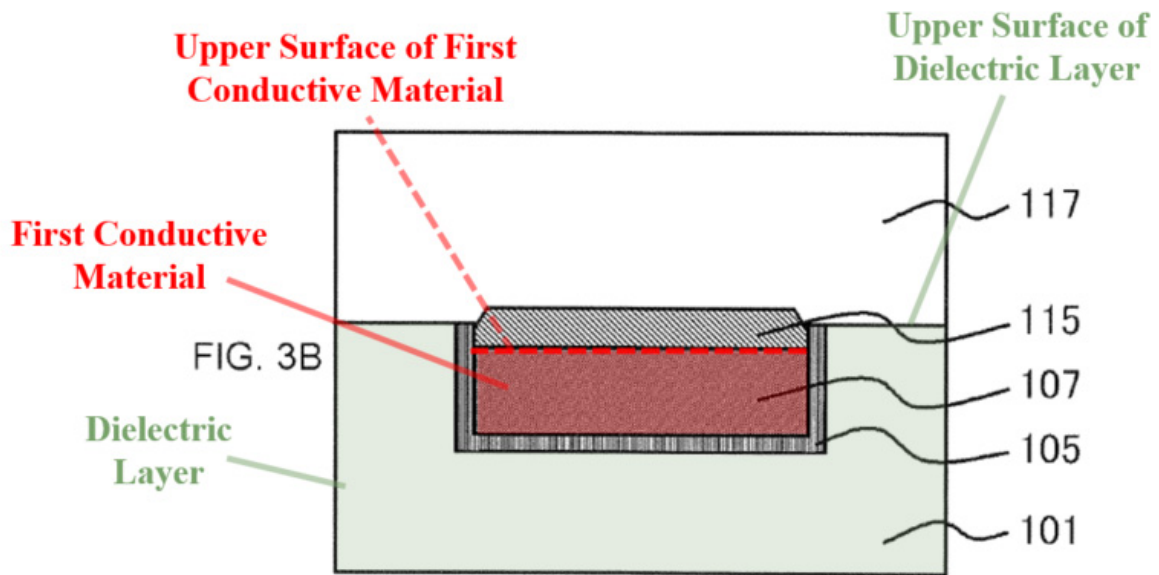


(Ex. 1009, FIG. 6B (annotated); Ex. 1002, ¶137.)

d) Element 1[d]

Kawahara discloses claim element 1[d]. (Ex. 1002, ¶¶138-139.) For example, as shown in annotated figure 3B below, lower layer copper interconnect 107 (“first conductive material”) has an upper surface, where a portion of the upper surface is

below a portion of the upper surface of the dielectric layer. (Ex. 1009, 4:43-46, 6:62-64; Ex. 1002, ¶138.)

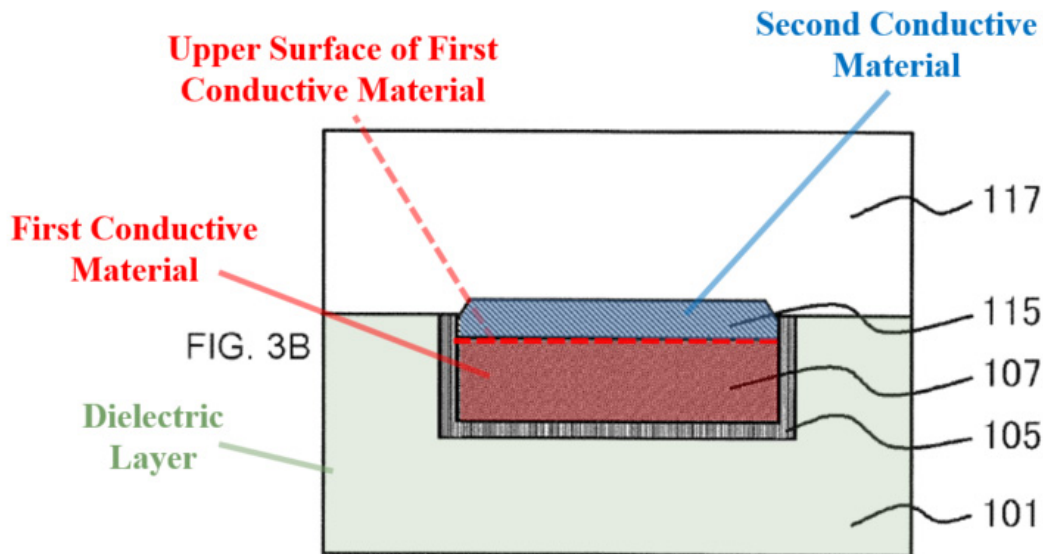


(Ex. 1009, FIG. 3B (annotated); Ex. 1002, ¶138.)

Kawahara discloses that the copper interconnect 107 is recessed in order to allow the cap metal film 111 to be formed on the surface of the interconnect 107 (thereby forming the electrically conducting protective film 115) while not extending “from the top of the concave portion 103 beyond the region for forming the barrier metal film 105 considerably exceeding the top of the insulating film 101, or from being considerably swelled to form a mushroom-shape.” (Ex. 1009, 8:40-52; *see also id.*, 6:64-7:3; Ex. 1002, ¶139.)

e) Element 1[e]

Kawahara discloses this claim element in a manner consistent with PO's assertions in litigation. (Ex. 1002, ¶¶140-147.) For example, as shown in annotated figure 3B below, Kawahara discloses forming the protective film 115 ("second conductive material") on the upper surface of the first conductive material. (Ex. 1009, 7:6-9 ("a COWP film is grown as the cap metal film 111 from the upper surface of the lower layer copper interconnect 107 by a selective plating process such as an electroless plating process and the like."); Ex. 1002, ¶140.)



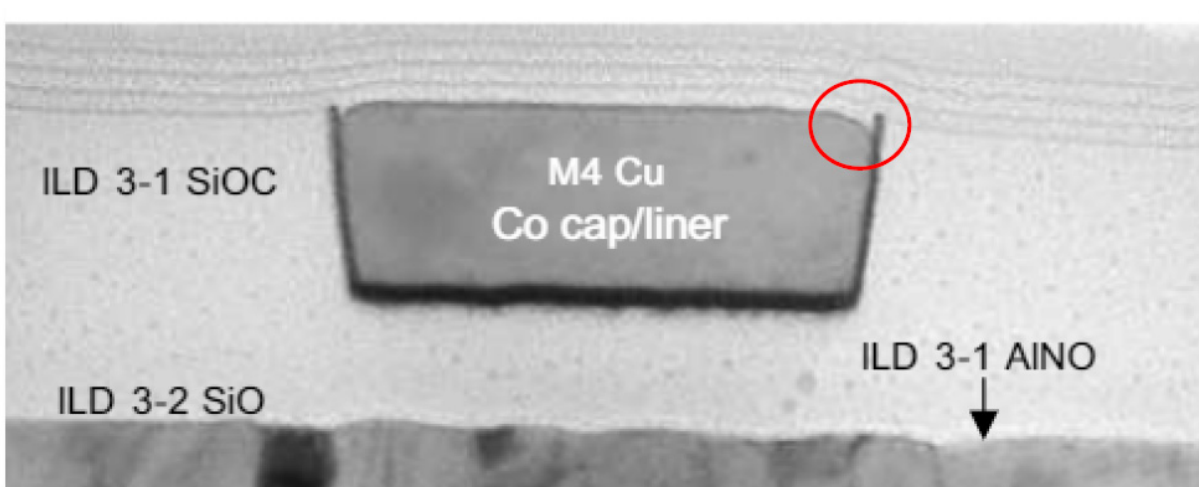
(Ex. 1009, FIG. 3B (annotated); Ex. 1002, ¶140.)

Kawahara further discloses that the protective film 115 ("second conductive material") includes cobalt. (Ex. 1009, 5:50-53; *see also id.*, 5:53-60, 7:4-9, 8:1-4; Ex. 1002, ¶141.)

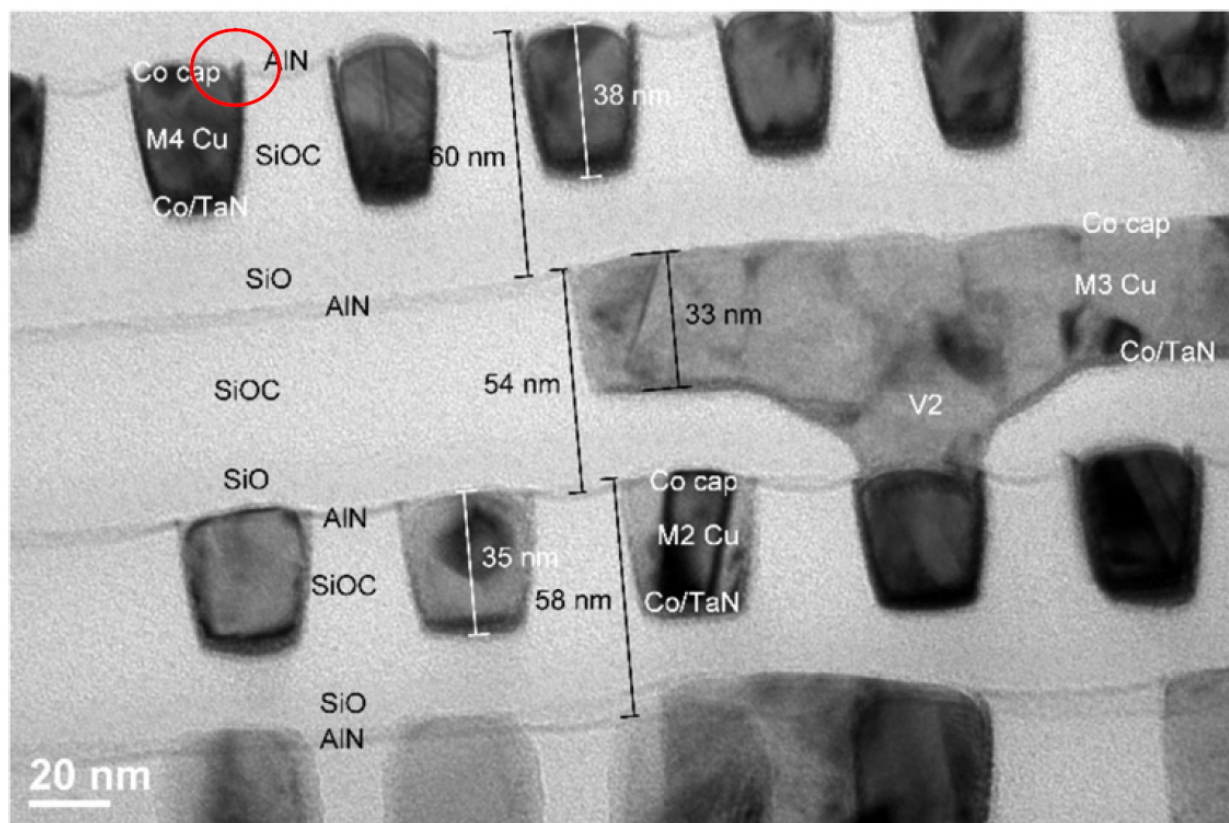
Kawahara discloses that the protective film 115 (“second conductive material”) covers the “entire upper surface” of the copper interconnect 107 (“first conductive material”), and therefore the first and second conductive materials, which are both contained by the concave portion of the dielectric layer 101, have the same width at the location where they meet. (Ex. 1009, 2:1-14; 7:15-21, 8:56-9:5; Ex. 1002, ¶142.)

In addition, Kawahara discloses “the second conductive material has an upper surface having a portion substantially co-planar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer” at least in a manner consistent with PO’s assertions in litigation. (Ex. 1002, ¶¶143-147.) In district court, PO contends that these features are met in the accused products based on the following images. (Ex. 1017, 115-118.)⁸

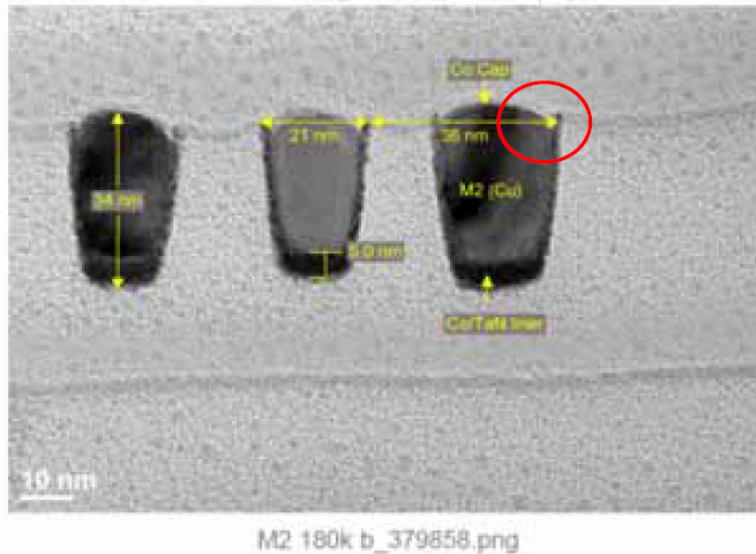
⁸ Page numbers correspond to those provided with Ex. 1017 in litigation.



(*Id.*, 113, (“a divot that falls a distance below the upper surface of the dielectric layer (circled in red)”)), 115 (“The divot forms a curved corner.”).)



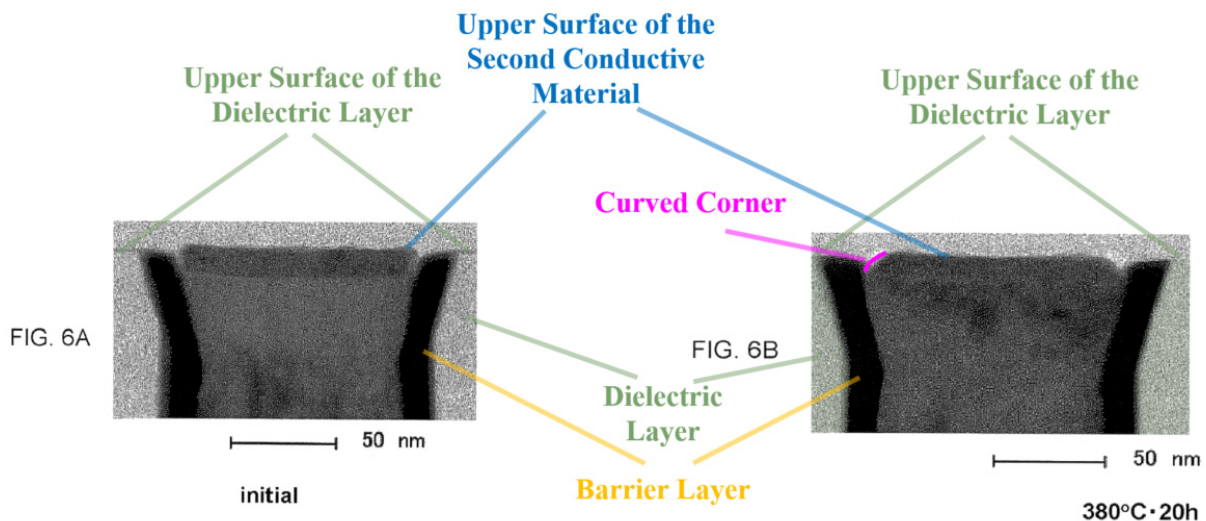
(*Id.*, 117.)



(*Id.*, 118.)

Without waiving any positions that may be presented in district court, under PO's broad interpretation, Kawahara discloses these features. (Ex. 1002, ¶¶143-147.) *See 10X Genomics, Inc. v. Bio-Rad Labs., Inc.*, IPR2020-00086, Paper 8 at 21-22 (PTAB Apr. 27, 2020) (permitting petitioner to base its challenge “on claim constructions implied by Patent Owner’s district court infringement contentions”). As shown in annotated figures 6A and 6B below, Kawahara discloses that “the second conductive material has an upper surface having a portion substantially coplanar with the portion of the upper surface of the dielectric layer, and wherein the upper surface of the second conductive material has a curved corner below the portion of the upper surface of the dielectric layer” in a manner consistent with PO’s

assertions in litigation. (Ex. 1002, ¶145.) Figures 6A and 6B include “a divot that falls a distance below the upper surface of the dielectric layer,” where the “divot forms a curved corner.” (*Id.*; Ex. 1017, 113, 115-118.)



(Ex. 1009, FIGs. 6A, 6B (annotated); Ex. 1002, ¶145.)

Kawahara discloses that the copper interconnect 107 is recessed in order to allow the cap metal film 111 to be formed on the surface of the interconnect 107 while not extending “from the top of the concave portion 103 beyond the region for forming the barrier metal film 105 considerably exceeding the top of the insulating film 101, or from being considerably swelled to form a mushroom-shape.” (Ex. 1009, 8:40-52; *see also id.*, 6:67-7:3 (“A height of the stepper portion 109 may be selected to be sufficiently larger to avoid a formation of the cap metal film 111

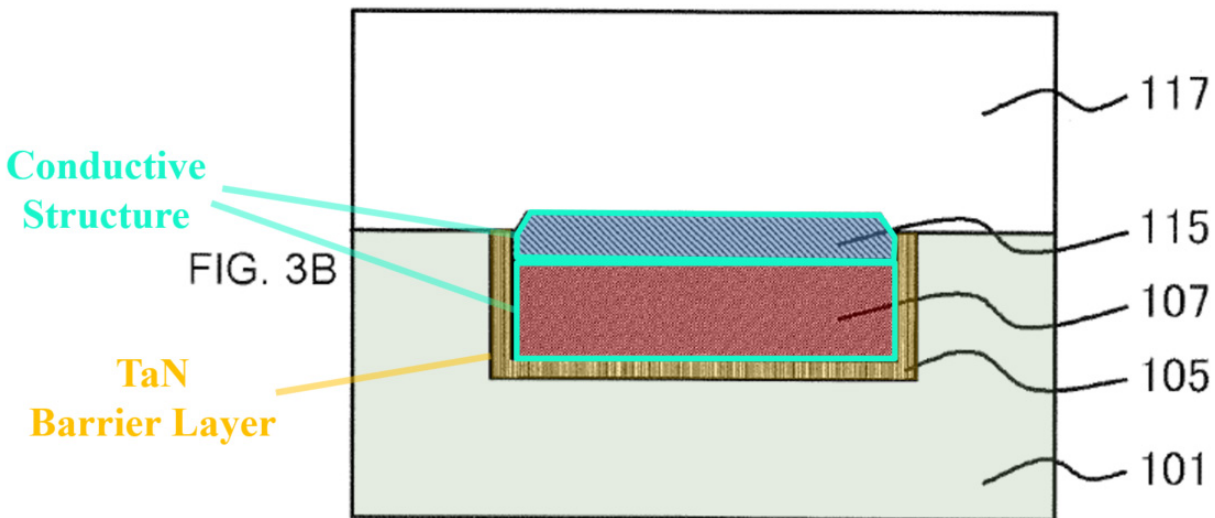
outside of the desired region”); Ex. 1002, ¶146.)⁹ Therefore, Kawahara discloses that by recessing the interconnect on which the cap metal film is formed, the cap metal film is formed so that an unwanted extension of the cap metal film can be avoided. (Ex. 1009, 1:46-56; Ex. 1002, ¶147.) For at least these reasons, Kawahara

⁹ While Kawahara discloses an example height of the stepper portion 109 (i.e., the gap left by recessing the interconnect 107) of 80 nm and an example thickness of the protective film 115 of about 120 nm, such thicknesses are only examples presented and should not be viewed as limiting. Such an understanding is confirmed by the claims of Kawahara, where claim 3 recites that the upper surface of the barrier metal film 105 is “substantially coplanar” with the uppermost surface of the insulating film 101, and claim 4, which depends from claim 3, recites that the uppermost surface of the insulating film is between the upper and lower surfaces of the electrically conducting film (“second conductive material”) 115. Therefore, while claim 4 corresponds to a scenario where the second conductive material protrudes above the insulating dielectric layer, other claims, including claims 1 and 3, demonstrate Kawahara’s disclosure is not limited to such a scenario.

discloses claim element 1[e] at least in a manner consistent with PO's assertions in litigation. (Ex. 1002, ¶147.)

f) Element 1[f]

Kawahara discloses this claim element. (Ex. 1002, ¶¶148-149.) Kawahara discloses forming a tantalum nitride (TaN) barrier metal film 105 (“barrier layer”) covering the inner wall of the concave portion 103, where the copper interconnect 107 (“first conductive material”) and protective film 115 (“second conductive material”) are formed such that the barrier layer 105 partially surrounds the conductive structure. (Ex. 1009, 4:42-43 (“a barrier metal film 105 covering an inner wall of the concave portion 103”), 4:54-55 (“barrier metal film 105 such as tantalum nitride (TaN) film”); *see also id.*, 4:38-59; Ex. 1002, ¶148.)



(Ex. 1009, FIG. 3B (annotated); Ex. 1002, ¶149.)

2. Claim 2

Kawahara discloses claim 2. (Ex. 1002, ¶150.) Kawahara discloses a barrier metal film 105 (“barrier layer”) formed of tantalum nitride (TaN), which includes tantalum and nitrogen. (Ex. 1009, 4:54-55; Ex. 1002, ¶150.)

3. Claims 3-8

Kawahara discloses claims 3-8. (Ex. 1002, ¶¶151-152.) Kawahara discloses forming the protective film 115 (“second conductive material”) using alloys that include cobalt and one or more of boron, phosphorus, and tungsten as recited in claims 3-8. (Ex. 1009, 5:50-53 (“The protective film 115 ... contain[s] for example, one or more element selected from Co and Ni and one or more element selected from tungsten (W) and phosphorus (P) and boron (B)”); Ex. 1002, ¶¶151-152.)

4. Claim 9

a) Element 9[a]

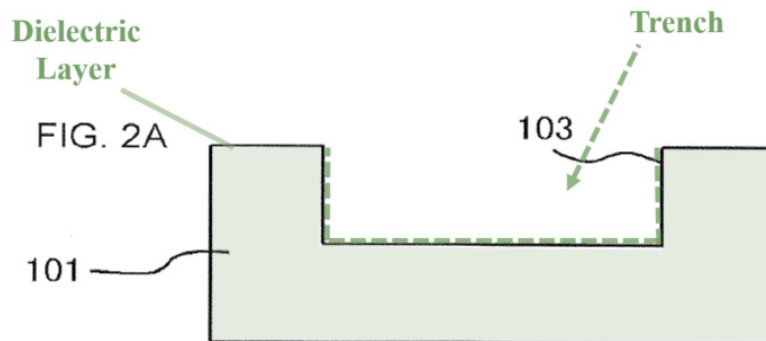
Kawahara discloses the preamble (claim element 9[a]) to the extent it is limiting. (Ex. 1002, ¶153.) For example, Kawahara discloses “a method for manufacturing the semiconductor device 100,” where, as discussed above for claim element 1[a], Kawahara discloses formation of an interconnect structure (“integrated circuit structure”) for semiconductor devices. (Ex. 1009, 6:11-14, 3:1-3; *supra* section IX.D.1(a); Ex. 1002, ¶153.)

b) Element 9[b]

Kawahara discloses this claim element. (Ex. 1002, ¶¶154-155.) Kawahara discloses forming an insulating interlayer 101, which is a low dielectric constant film (“dielectric layer”) of silicon oxycarbide (SiOC), which includes silicon (Si), oxygen (O), and carbon (C). (Ex. 1009, 5:16-22, 6:49-50, 6:15-16; Ex. 1002, ¶¶154-155.)

c) Element 9[c]

Kawahara discloses this claim element. (Ex. 1002, ¶156.) As shown in annotated figure 2A below, Kawahara discloses etching away portions of the insulating interlayer 101 (“dielectric layer”) to form a concave portion 103 (“trench”). (Ex. 1009, 6:52-54, 6:18-19; Ex. 1002, ¶156.)

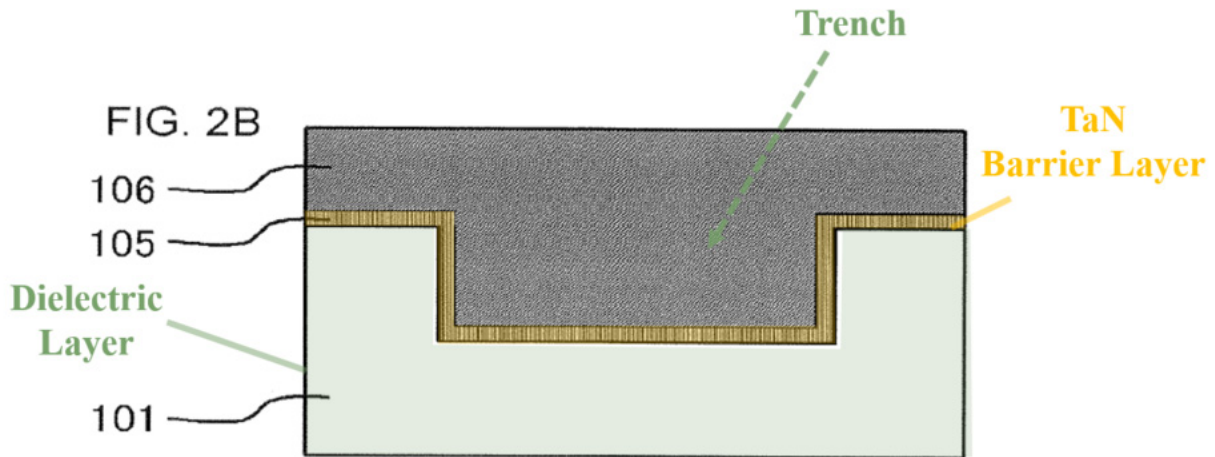


(Ex 1009, FIG. 2A (annotated); Ex. 1002, ¶156.)

d) Element 9[d]

Kawahara discloses this claim element. (Ex. 1002, ¶157.) As shown in annotated figure 2B below, Kawahara discloses forming TaN barrier metal film 105

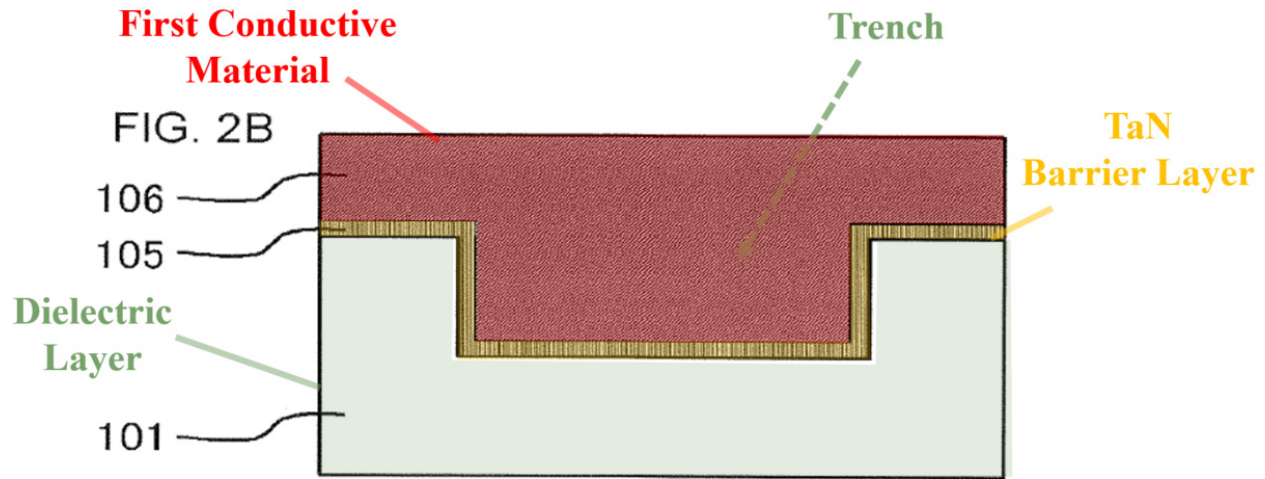
(“barrier layer”), which includes tantalum, in the trench. (Ex. 1009, 4:54-55, 6:55-56, 6:20-22; Ex. 1002, ¶157.)



(Ex 1009, FIG. 2B (annotated); Ex. 1002, ¶157.)

e) Element 9[e]

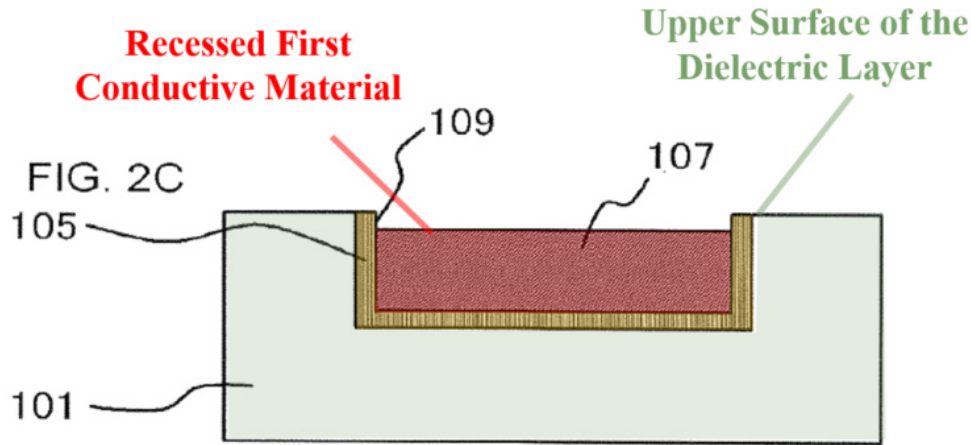
Kawahara discloses this claim element. (Ex. 1002, ¶158.) After forming the barrier layer, Kawahara discloses forming copper film 106 (“first conductive material comprising copper”) in the lined trench (“within the barrier layer”). (Ex. 1009, 6:56-57 (“[T]hen the Cu film 106 is formed so as to plug the concave portion 103....”), 6:23-26; Ex. 1002, ¶158.)



(Ex 1009, FIG. 2B (annotated); Ex. 1002, ¶158.)

f) Element 9[f]

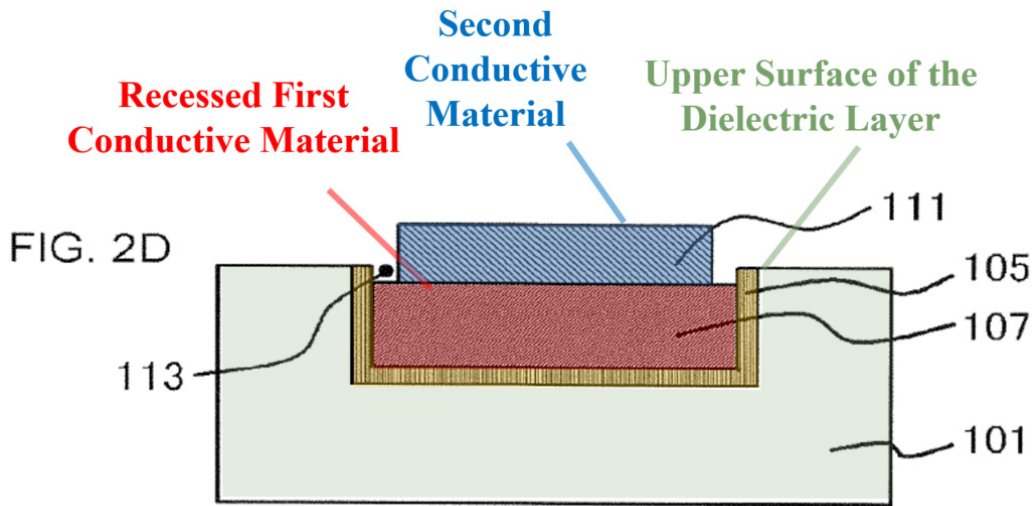
Kawahara discloses this claim element. (Ex. 1002, ¶159.) Kawahara discloses that “the upper surface of the lower layer of copper interconnect 107 is retracted [“recessed”] to be closer to the substrate than the upper surface of the insulating interlayer 101 to form a stepper portion 102 (FIG. 2C).” (Ex. 1009, 6:58-67; *see also id.*, 6:27-33; Ex. 1002, ¶159.)



(Ex 1009, FIG. 2C (annotated); Ex. 1002, ¶159.)

g) Element 9[g]

Kawahara discloses this feature in a manner consistent with PO's assertions in litigation for reasons similar to those presented above with respect to claim element 1[g]. (*Supra* section (IX.D.1(g); Ex. 1002, ¶¶160-162.) Kawahara discloses that, after recessing the interconnect 107 ("first conductive material"), metal film 111 ("second conductive material") is grown on the surface of the interconnect 107. (Ex. 1009, 7:4-9; *see also id.*, 6:34-38; Ex. 1002, ¶160.)



(Ex. 1009, FIG. 2D (annotated); Ex. 1002, ¶160.)

Kawahara further discloses that after forming the metal film 111, the substrate is heat treated to cause the migration of the metal film into the gap 113 so that the entire upper surface of the lower layer interconnect is covered. (Ex. 1009, 7:15-21; *see also id.*, 6:39-43; Ex. 1002, ¶161.) As discussed above for claim element 1[e], Kawahara discloses, in a manner consistent with PO's assertions in litigation, that the metal cap metal film 111 ("second conductive material") (1) is on the upper surface of the recessed first conductive material, (2) comprises cobalt, (3) has the same width where the second conductive material meets the first conductive material, and (4) has a curved corner below the portion of the upper surface of the dielectric layer. (*Supra* section IX.D.1(e); Ex. 1002, ¶162.)

5. Claim 11

Kawahara discloses claim 11 for the reasons discussed above with respect to claim 2. (*Supra* section IX.D.2; Ex. 1002, ¶163.)

6. Claims 12-17

Kawahara discloses claims 12-17 for the reasons discussed above with respect to claims 3-8. (*Supra* section IX.D.3; Ex. 1002, ¶164.)

E. Ground 5 – Kawahara in View of Chan Renders Claim 10 Obvious

1. Claim 10

Kawahara in view of Chan discloses or suggests claim 10. (Ex. 1002, ¶¶165-173.) As discussed above for claim elements 1[d] and 9[f], Kawahara discloses recessing the copper interconnect (“second conductive material”). (*Supra* sections IX.D.1(d), IX.D.4(f); Ex. 1002, ¶166.) Kawahara does not explicitly disclose using wet etching to recess the interconnect, but Chan discloses using wet etching for just such a purpose in a similar device, and a POSITA would have found it obvious to use wet etching to recess Kawahara’s interconnect for reasons similar to those presented above with respect to the Fukunaga-Park-Chan combination discussed above in Section IX.B. (*Supra* section IX.B; Ex. 1002, ¶167.) Like Kawahara, Chan discloses recessing copper that initially fills the trenches to form recessed interconnects 120 so that the caps are formed in the trench, and a POSITA

implementing an interconnect structure like that disclosed by Kawahara would have had good reason to look to Chan. (Ex. 1007, ¶¶[0038]-[0039]; Ex. 1002, ¶¶168-172.) Such a POSITA would have been motivated to use wet etching, and found it straightforward to use such wet etching, as opposed to chemical mechanical polishing (CMP) to recess Kawahara's interconnects in order to avoid applying a mechanical load to the substrate, which can damage the structure when low-k dielectric materials are used. (Ex. 1005, ¶[0057]; Ex. 1002, ¶¶172-173.)

F. Ground 6 – Kawahara and Fukunaga Render Obvious Claim 10

1. Claim 10

As discussed above in Section IX.E, Kawahara does not explicitly disclose using wet etching to recess the copper interconnect layer. (*Supra* section IX.E.) However, Fukunaga discloses using wet etching to remove extra copper and etching to recess a copper interconnect layer, and, in view of Fukunaga, a POSITA would have found it obvious to use wet etching to recess the copper interconnect of Kawahara. (Ex. 1002, ¶¶174-181.)

As discussed above for claim 1 in Section IX.A.1, Fukunaga, like Kawahara, is directed to forming interconnect for semiconductor devices, where copper interconnect overlies a barrier layer in a trench in a dielectric layer, and a capping layer is formed overlying the interconnect. (*Supra* section IX.A.1; Ex. 1002, ¶177.)

Therefore, a POSITA forming interconnect like that disclosed by Kawahara would have had good reason to look to Fukunaga. (Ex. 1002, ¶177.)

Fukunaga discloses that it is beneficial to use wet etching to remove extra copper material, like that shown in figure 2B of Kawahara, as wet etching does not require a mechanical load to be applied to the substrate, which can damage the structure when low-k dielectric materials are used. (Ex. 1005, ¶¶[0051], [0060] [0057]; Ex. 1002, ¶178.)

Having looked to Fukunaga, a POSITA would have found it obvious to remove the extra copper interconnect 106 in Kawahara using wet etching in order to avoid possible damage to the semiconductor device. (Ex. 1002, ¶179.) As discussed above for claim element 1[b], Kawahara discloses using a low-k SiOC dielectric material. (*Supra* section IX.D.1(b); Ex. 1009, 5:16-22; Ex. 1002, ¶179.) While Kawahara discloses removal of at least a portion of the copper interconnect 106 using CMP, a POSITA would have been motivated, in view of Fukunaga's teachings to use wet etching to recess the copper interconnect. (Ex. 1002, ¶179.) Indeed, Fukunaga teaches that CMP can damage the substrate, while wet etching does not raise such a concern. (Ex. 1005, ¶[0057]; Ex. 1002, ¶179.)

Moreover, a POSITA would have known that wet-etching using an acidic solution, as taught by Fukunaga, was a well-known technique for recessing

interconnect material like that of Kawahara. (Ex. 1002, ¶180; Ex. 1007, ¶[0038]; *see also id.*, ¶¶[0007]-[0008]; Ex. 1011, ¶[0066].)

Based on Fukunaga's teachings regarding wet etching, a POSITA would have been motivated to use wet etching to recess the interconnect as disclosed by Kawahara as it would have been an effective way of removing such material and would not have required the application of a load to the substrate, thereby avoid possible damage to the substrate. (Ex. 1002, ¶181.) Using wet etching would have been straightforward for a POSITA to implement, because Fukunaga discloses how to use wet etching, and wet etching was commonly used for such a purpose. (*Id.*) Using wet etching would have been the application of a known technique to a similar device and would have been produced the predictable result of a recessed copper interconnect ready for capping. (*Id.*, ¶181.) *KSR* at 416.

G. Ground 7 – Kawahara and Park Render Obvious Claims 18-25

1. Claims 18-25

Kawahara in view of Park discloses or suggests all of the features of claims 18-25. (Ex. 1002, ¶¶182-187.) Park, like Kawahara, is directed to copper interconnect structures embedded in low-k materials, where a recessed capping layer overlying the copper interconnect is used to prevent electromigration. (*Supra* section IX.A.1(b); Ex. 1002, ¶183.) Because Park discloses an interconnect structure

very similar to that of Kawahara, a POSITA implementing interconnect like that disclosed by Kawahara would have reason to look to Park. (Ex. 1002, ¶183.)

While Kawahara discloses that the interconnect structure can be used in semiconductor devices (Ex. 1009, 3:1-3, 6:49-52, 9:32-33), Kawahara does not explicitly disclose using the interconnect structure in a “computing device.” As discussed above in Sections IX.A.8-15, Park discloses a very similar interconnect structure used in a computing device and, in combination with Fukunaga, discloses or suggests the features of claims 18-25. (*Supra* sections IX.A.8-15.) For the same reasons presented above for the Fukunaga-Park combination, a POSITA would have found it obvious to use Kawahara’s interconnect structure discussed above for claim 1 in a semiconductor device that is a “computing device,” where the features recited in claims 18-25 are disclosed or suggested by the Kawahara-Park combination for the same reasons presented above for the Fukunaga-Park combination. (Ex. 1002, ¶¶184-185.) For example, using the Kawahara interconnect structure discussed above for claim 1 in computing devices as disclosed by Park, would have been a predictable combination of known components according to known methods to achieve a predictable result and would have increased the utility of such an interconnect structure through its implementation in such computing devices and provided the benefit of more reliable operation for the computing devices. (*Id.*,

¶186.) Moreover, a POSITA would have had a reasonable expectation of success in such a Kawahara-Park combination. (*Id.*) The inclusion of Kawahara's interconnect structure, instead of the Fukunaga-Park interconnect, in computing devices as disclosed or suggested by Park does not impact Park's disclosure or suggestion of the remaining features of claims 18-25. (*Id.*, ¶187.)

H. Ground 8 – Kawahara in View of Park and Song Renders Claims 20-23 Obvious

As discussed above in Section IX.G, the Kawahara-Park combination discloses or suggests all of the features of claims 20-23 for the same reasons discussed in Sections IX.A.10-13 for claims 20-23. (*Supra* sections IX.G, IX.A.10-13.) To the extent PO argues that the Kawahara-Park combination does not disclose or suggest these features, they would have been obvious in further view of Song for the same reasons presented above in Section IX.C for the Fukunaga-Park-Song combination. (Ex. 1002, ¶¶188-191.)

Park does not disclose all of the details regarding the cell phones that incorporate the interconnect structure, and therefore a POSITA would have had good reason to look to Song, which discloses additional details regarding components included in cell phones. (Ex. 1002, ¶190.) In view of Song and their knowledge of state-of-the art cell phone features, such a POSITA would have found it obvious to

include a communications chip (claim 20), a camera (claim 21), a battery (claim 22), and an antenna (claim 23) coupled to the board (substrate 220) in the cell phone of the Kawahara-Park combination. (*Id.*) Such a POSITA would have been motivated to include such features in order to enable fundamental operational characteristics of the cell phone (communications using the communications chip and antenna powered by the battery) and provide added utility in the form of the ability to take pictures (camera). (*Id.*) Such an implementation would have been a straightforward combination of well-known technologies using known methods and would have had predictable results. (*Id.*) See *KSR* at 416-18.

A POSITA would have had a reasonable likelihood of success in implementing such features as they were well-known and widely-implemented features of cell phones. (Ex.1002, ¶191.) The inclusion of Kawahara's interconnect structure, instead of the Fukunaga-Park interconnect, in computing devices as disclosed or suggested by Park and Song does not impact the disclosure or suggestion of the remaining features of claims 20-23. (*Id.*)

X. DISCRETIONARY DENIAL IS NOT APPROPRIATE

A. The Board Should Not Deny Institution Under *Fintiv*

The merits of Petitioner's arguments are compelling and the evidence in support is substantial. That "alone demonstrates that the PTAB should not

discretionarily deny institution under *Fintiv*.” (Ex. 1018 at 4-5.) But in any event, the six *Fintiv* factors do not justify denying institution.

The **first factor** is neutral because Samsung has not yet moved to stay the district court proceeding. *See, e.g., Hulu LLC v. SITO Mobile R&D IP, LLC et al.*, IPR2021-00298, Paper 11 at 10-11 (PTAB May 19, 2021).

The **second factor** weighs against denial. Jury selection is scheduled for May 20, 2024. (Ex. 1019, 1.) However, the median time from the filing of a civil case to trial in the Eastern District of Texas is 24.5 months (Ex. 1020, 37), placing the expected trial date in the parallel litigation around late September 2024. *See* Ex. 1018 at 8-9 (instructing Board to consider median time-to-trial statistics). Therefore, trial is expected to occur after the FWD in this IPR, which is expected around July 2024. And even if trial proceeds in May 2024, the above timing does not tip in favor of denying the petition in this case. *See also, e.g., Apple Inc. v. Aire Tech. Ltd.*, IPR2022-01135, Paper 11 at 5-6 (PTAB Jan. 4, 2023).

The **third factor** weighs strongly against denial. The district court case is in its infancy, and the Parties’ have made little investment to date. PO filed its complaint on September 12, 2022, served its initial infringement contentions on November 17, 2022, and just filed an amended complaint on January 24, 2023. Petitioner’s diligence in pursuing this petition less than five months after PO’s

complaint and shortly after receiving the infringement contentions weighs in favor of institution. *Facebook, Inc. v. USC IP P'ship, L.P.*, IPR2021-00033, Paper 13 at 13 (PTAB April 30, 2021) (finding it was reasonable for Petitioner to wait to file the Petition until shortly after receiving infringement contentions).

The **fourth factor** weighs against denial because this Petition challenges claims 3-17, which are not asserted against Petitioner in district court. This IPR petition is thus the only venue in which certain invalidity challenges will be adjudicated, which promotes system efficiency. *See Fintiv*, Paper 11 at 4. Accordingly, this factor weighs against denial. *See, e.g., Vudu, Inc. v. Ideahub, Inc.*, IPR2020-01688, Paper 16 at 14-15 (PTAB April 19, 2021).

Regarding the **fifth factor**, the Board should give no weight to the fact that Petitioner and PO are the same parties as in district court. *See Weatherford U.S., L.P., v. Enventure Global Tech., Inc.*, Paper 16 at 11-13 (April 14, 2021).

The **sixth factor** (other circumstances) weighs heavily against denial given the undeniable similarity between Boyanov '569 and the '183 patent. *See Align Technology, Inc. v. 3Shape A/S*, IPR2020-01087, Paper 15 at 42-43 (PTAB Jan 20, 2021); *see also* Section IX. There is also a significant public interest against “leaving bad patents enforceable,” and institution will further that interest. *Thryv, Inc v. Click-To-Call Techs., LP*, 140 S. Ct. 1367, 1374 (2020).

B. The Board Should Institute This Petition

Petitioner is filing an additional IPR petition challenging the claims of the '183 patent concurrently with the filing of this petition. The other petition relies on breaking the priority chain of the '183 patent, relies on a prior art reference not discussed in the present petition, and is being filed out of an abundance of caution because of the statutory estoppel provisions.

The unpatentability grounds presented in this petition differ substantially from that raised in the concurrently filed petition. Accordingly, the Board should institute review based on the substantially different grounds presented in this petition. Indeed, institution of both petitions is particularly justified given that the Board generally discourages follow-on petitions. *See General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper No. 19 at 9 (Sept. 6, 2017). Finally, Petitioner has narrowed the grounds presented in each of the petitions to achieve the goal of “just, speedy, and inexpensive resolution” consistent with 37 C.F.R. § 42.1(b).

C. The Board Should Not Deny Institution Under § 325(d)

None of the reference besides Park was considered during prosecution of the '183 patent. Moreover, even though the Examiner allowed pending claims over Park (Ex. 1004, 32-35), the Examiner did not rely on any of the *combinations* of the prior

art presented in this Petition. *See, e.g., Halliburton Energy Services, Inc. v. US Well Services, LLC*, IPR2021-01036, Paper 12 at 20 (PTAB Jan. 19, 2022) (granting institution when the Examiner cited a reference in a rejection during prosecution but the Petition set forth “obviousness grounds based on combinations of [the reference] with other prior art not considered by the Examiner”).

Park was never combined with Fukunaga or Kawahara during prosecution, as presented in this Petition. (*See generally* Ex. 1004.) *See Cont’l Auto. Sys.*, IPR2021-00322, Paper 7 at 19. Park was cited as a primary reference during prosecution of the ’183 patent, but is only cited in this Petition as a secondary reference to address certain features, where Applicant never disputed that Park disclosed such features during prosecution. (*See generally* Ex. 1004.) Indeed, the Examiner allowed the pending claims based on the lack of disclosure of the “curved corner” limitation in the prior art. (*See* Ex. 1004, 32-35.) Petitioner is not asking the Office to reconsider any arguments, but merely to make determinations consistent with the Examiner’s previous and uncontested finding that Park discloses certain features included in the challenged claims. Petitioner also presents additional evidence and analysis in the petition that were not before the Examiner, including the declaration of Dr. Shanfield (Ex. 1002).

Under these circumstances, Petitioner respectfully submits that denial of institution under § 325(d) would not be appropriate.

XI. CONCLUSION

For the foregoing reasons, Petitioner requests IPR and cancellation of claims 1-25 of the '183 patent.

Respectfully submitted,

Dated: February 3, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,727,183 contains, as measured by the word processing system used to prepare this paper, 13,577 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: February 3, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on February 3, 2023, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 10,727,183 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record:

KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

Respectfully submitted,

Dated: February 3, 2023

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner