Trials@uspto.gov
571-272-7822

Paper 62
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

LG ELECTRONICS, INC.,
Petitioner,

v.

ATI TECHNOLOGIES ULC,
Patent Owner.

Case IPR2015-00325
Patent 7,742,053 B2

Before JONI Y. CHANG, BRIAN J. McNAMARA, and RAMA G. ELLURU, *Administrative Patent Judges.*

CHANG, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

LG Electronics, Inc. ("LG") filed a Petition requesting an *inter partes* review of claims 1, 2, and 5–7 ("the challenged claims") of U.S. Patent No. 7,742,053 B2 (Ex. 1001, "the '053 patent"). Paper 2 ("Pet."). Patent Owner, ATI Technologies ULC ("ATI"), filed a Preliminary Response. Paper 12 ("Prelim. Resp."). Upon consideration of the Petition and Preliminary Response, we instituted this trial as to claims 1, 2, and 5–7 of the '053 patent on June 15, 2015. Paper 13 ("Dec.").

Subsequent to institution, ATI filed a Patent Owner Response (Papers 21, 22, "PO Resp."); LG filed a Reply to the Patent Owner Response (Papers 33, 34, "Reply"); and ATI filed a sur-reply to LG's Reply with respect to the antedating issue (Papers 39, 40).[1] An oral hearing was held on February 10, 2016.[2]

We have jurisdiction under 35 U.S.C. § 6(c). This Final Written Decision is issued pursuant to 35 U.S.C. § 318(a). For the reasons discussed herein, and in view of the record in this trial, we determine that LG has shown by a preponderance of the evidence that claims 1, 2, and 5–7 of the '053 patent are unpatentable.

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[1] The parties filed a confidential version and a redacted version of their papers. The Decisions denying the parties' Motions to Seal these documents and supporting evidence are entered concurrently with this Final Written Decision. Papers 63, 64. The citations to these papers are to the unredacted versions.

[2] A transcript of the oral hearing is entered in the record as Paper 61 ("Tr.").

A. Related Matter

The ’053 patent is asserted in *Advanced Micro Devices, Inc. v. LG Electronics, Inc.*, No. 3:14-cv-01012-SI (N.D. Cal.). Pet. 1.

B. The ’053 Patent

The ’053 patent discloses a computer system for multithreaded graphics processing. Ex. 1001, 2:36–41. The system includes a memory device for storing command threads and an arbiter for providing a command thread to a command processing engine, based on a priority scheme. *Id.* at 2:48–52, 3:29–35; *see* Paper 13, 2–3.

C. Illustrative Claim

Of the challenged claims, claims 1 and 5 are independent. Claim 2 depends from claim 1, and claims 6 and 7 depend directly from claim 5. Claim 5, reproduced below, is illustrative of the challenged claims.

> 5. A graphics processing system comprising:
>
> at least one *memory device* comprising a first portion operative to store a plurality of pixel command threads and a second portion operative to store a plurality of vertex command threads;
>
> an *arbiter*, coupled to the at least one memory device, operable to select a command thread from either of the plurality of pixel command threads and the plurality of vertex command threads; and
>
> a plurality of *command processing engines*, coupled to the arbiter, each operable to receive and process the command thread.

Ex. 1001, 8:4–15 (emphases added).

D. Prior Art Relied Upon

LG relies upon the following prior art references:

Lindholm	US 7,015,913 B1	Mar. 21, 2006	(Ex. 1004)
Stuttard	US 7,363,472 B2	Apr. 22, 2008	(Ex. 1005)
Moreton	US 7,233,335 B2	June 19, 2007	(Ex. 1006)
Whittaker	US 5,968,167	Oct. 19, 1999	(Ex. 1007)
Kimura	US 6,105,127	Aug. 15, 2000	(Ex. 1008)

Admitted Prior Art – Figure 1, and the Background of the Invention Section of the ’053 patent. Ex. 1001, 1:22–2:6, Fig. 1.

E. Instituted Grounds of Unpatentability

We instituted this trial based on the following grounds (Dec. 36–37):

Claims	Basis	References
5–7	§ 102(e)	Moreton
1 and 2	§ 103(a)	Moreton and Whittaker
1, 2, and 5–7	§ 103(a)	Lindholm in view of the Admitted Prior Art
1, 2, and 5–7	§ 103(a)	Stuttard in view of the Admitted Prior Art

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, claim terms in an unexpired patent are given their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b). Under the broadest reasonable interpretation standard, claim terms are given their ordinary and customary meaning as would be understood by one of ordinary skill in the

art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

"command thread"

Each of independent claims 1 and 5 recites "at least one memory device comprising a first portion operative to store a plurality of pixel *command threads* and a second portion operative to store a plurality of vertex *command threads*." Ex. 1001, 7:11–15, 8:5–8 (emphases added). Before institution, ATI urged us to construe "command thread" as "a sequence of commands." Prelim. Resp. 12–13. ATI also argued that a command thread does *not* encompass an *instruction*. *Id.* at 12.

In the Decision on Institution (Dec. 6–7), we noted that the word "command" is used in the Specification of the '053 patent consistent with its plain and ordinary meaning, as including an *instruction*. *See, e.g.*, Ex. 1001, 4:21–27; MICROSOFT COMPUTER DICTIONARY 111 (5th ed. 2002) (Ex. 3001) (defining "command" as an "instruction to a computer program that, when issued by the user, causes an action to be carried out"). Notably, the Specification discloses that "[u]pon the execution of the associated *command of the command thread*, the thread is thereupon returned to the station 302 or 304 at the same storage location with its status updated, once all possible sequential *instructions* have been executed." Ex. 1001, 4:21–27 (emphasis added). Dr. Nader Bagherzadeh testifies that, in the context of computer multithreading, a stream of instructions is called a thread. Ex. 1003 ¶¶ 23–24. This is consistent with the usage of the word "thread" in

the prior art of record. *See, e.g.*, Ex. 1005, 5:19–30. We further note that the plain meaning of "thread," in the context of computer programming, means a process that is part of a larger process or program. MICROSOFT COMPUTER DICTIONARY 518 (5th ed. 2002) (Ex. 3001). We, therefore, disagreed with ATI, in our Decision on Institution, that a command thread does not encompass an instruction, as it would be inconsistent with the term's plain and ordinary meaning. Rather—for purposes of the Decision on Institution—in light of the Specification, we construed the claim term "command thread" to encompass a stream of instructions or a process that is part of a larger process or program. Dec. 6–7.

After institution, ATI does not challenge our claim construction. PO Resp. 30. In fact, ATI's expert, Dr. Andrew Wolfe, testifies that one of ordinary skill in the art would have understood that the term "command thread" requires instructions. Ex. 2151 ¶¶ 57–58, 118. As such, we discern no reason to change our claim construction of "command thread" for this Final Written Decision.

"arbiter"

Each of independent claims 1 and 5 recites "an *arbiter*, coupled to the at least one memory device, operable to *select a command thread* from either of the plurality of pixel command threads and the plurality of vertex command threads." Ex. 1001, 7:16–19, 8:9–12.

In its Petition, LG proposes to construe the claim term "arbiter" as "any implementation of hardware and/or software that receives and provides

a thread." Pet. 9. As support, LG cites to the Specification, which explains that an "arbiter may be any implementation of hardware, software or combination thereof such that the arbiter receives the command thread and thereupon provides the command thread to a command processing engine." *Id.* (citing Ex. 1001, 2:48–52).

Before institution, ATI argued that LG's proposed construction "ignores arbitration," and proposed that the claim term "arbiter" should be construed as "a component for picking out a command thread among available pixel and vertex command threads." Prelim. Resp. 10–11. ATI's proposed construction, however, improperly would import other claim language—"*picking out* a command thread among available *pixel and vertex* command threads"—into the construction of the claim term "arbiter." Such a construction also would render other claim language superfluous—e.g., "select a command thread from either of the plurality of pixel command threads and the plurality of vertex command threads," recited in claim 5. Moreover, the Specification explains that "arbiter 204 retrieves a command thread via connection 214 and *provides* the retrieved command thread to the command processing engine." Ex. 1001, 3:8–10 (emphasis added). As such, we declined to adopt ATI's proposed construction. Rather—for purposes of the Decision on Institution—in light of the Specification, we construed the claim term "arbiter" as any computer hardware, software, or combination thereof that receives and provides a command thread. Dec. 7–8. After institution, neither party proffers a different construction for this term. *See* PO Resp.; Reply. Upon review of this record, we discern no

reason to change our claim construction of "arbiter" for this Final Written Decision.

"command processing engine"

Claim 5 recites "*a plurality of command processing engines*, coupled to the arbiter, *each* operable to receive and *process* the command thread." Ex. 1001, 8:13–15 (emphasis added). Claims 6 and 7 directly depend from claim 5, and further recite "wherein the plurality of command processing engines comprises at least *one arithmetic logic unit*" and "at least one *texture processing engine*," respectively. *Id.* at 8:16–21 (emphases added).

LG proposes to construe "command processing engine" as "any implementation of hardware and/or software that processes commands." Pet. 9. In its Patent Owner Response, ATI asserts that an ordinarily skilled artisan would have understood that the "command processing engine" limitation recited in claim 5 requires *each* command processing engine to be able to process *both* pixel and vertex command threads. PO Resp. 31; Ex. 2151 ¶ 125.

LG disagrees, arguing that the disputed limitation recited in claim 5 merely requires that the command processing engines are capable of processing *either* a pixel command thread *or* a vertex command thread because claim 5 recites "an arbiter . . . operable to select <u>a</u> command thread" and "a plurality of command processing engines . . . each operable to receive and process <u>the</u> command thread." Reply 14 (emphases added by LG).

Upon review of the claim language and Specification, we agree with LG. Nothing in the claim language requires a single command processing engine to be able to process both pixel and vertex command threads.

We note that ATI's proposed claim construction essentially requires *each* of the plurality of command processing engines to have the capability to process *all* of the command threads selected by the arbiter—excluding *type-specific* processing engines. The Specification of the '053 patent, however, does not support such a narrow construction. Notably, the Specification discloses that the "command processing engine may be *any suitable engine as recognized by one having ordinary skill in the art* for processing commands, such as a texture engine, an arithmetic logic unit, or any other suitable processing engine." Ex. 1001, 2:59–62 (emphasis added). Additionally, claims 5–7 are directed to the preferred embodiment illustrated in Figure 4 of the '053 patent, which is reproduced below.

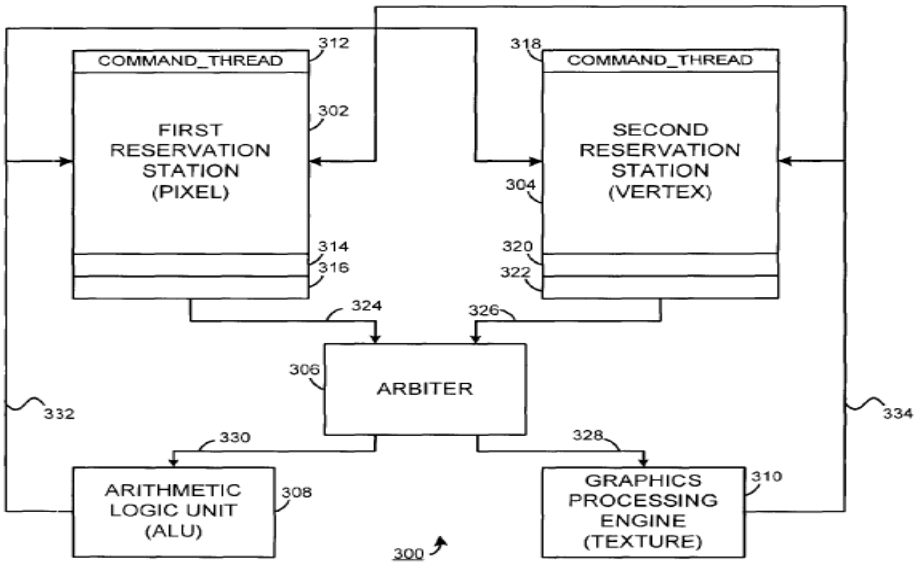

FIG. 4

As shown in Figure 4, processing system 300 includes first reservation station 302, which contains pixel command threads; second reservation station 304, which contains vertex command threads; arbiter 306; arithmetic logic unit 308; and texture engine 310. *Id.* at 3:62–4:33. The Specification explains that arbiter 306 retrieves pixel command thread 324 and vertex command thread 326 and then provides thread 328, which may be either pixel command thread 324 or vertex command thread 326, to texture engine 310. *Id.* at 4:28–33. Arbiter 306 further provides the other thread 330 to arithmetic logic unit ("ALU") 308. *Id.* Upon execution of the command, ALU 308 and text engine 310 return command threads 332 and 334 to the appropriate reservation station 302 or 304. *Id.* at 4:34–41. As the Specification explains, multiple *command operations* may be performed by ALU 308 or texture engine 310, but, in order to switch a thread from ALU 308 to texture engine 310, that thread must be returned back to the appropriate reservation station 302 or 304 and re-retrieved by arbiter 306 and thereupon provided to the other unit 308 or engine 310, respectively. *Id.* at 4:42–48.

Significantly, the Specification indicates that a thread is provided to a *specific type* of command processing engine (e.g., an ALU or texture engine) based on *the type of operations* (e.g., an ALU or texture operation). *Id.* at 3:62–4:48. ATI's own expert, Dr. Wolfe, testifies that "vertex command can also involve texture operations." Ex. 2151 ¶¶ 159, 165 (noting that "at least 10–20% of vertex command threads involving texture operations should be processed by the texture fetch processor"). Dr. Wolfe also explains that

pixel command threads can involve ALU operations. *Id.* ¶¶ 161–162 (noting "pixel command threads involving ALU operations, which contribute to 20–30% of the ALU operations"). This means that about 10–20% of vertex command threads involving texture operations cannot be processed in the ALU, and 20–30% of pixel command threads involving ALU operations cannot be processed in the texture engine. Put simply, ALU and texture engines are *type-specific* processing engines, and *each* unit or engine cannot process *all* of the threads selected by an arbiter.

Construing the "command processing engines" limitation recited in claim 5 to exclude *type-specific* processing engines, as proposed by ATI, would be inconsistent with the Specification. *Id.* at 2:59–62, 3:62–4:48, Fig. 4. Additionally, ATI's proposed claim construction would be inconsistent with claims 6 and 7, which recite "wherein the plurality of command processing engines comprises at least one arithmetic logic unit" and "at least one texture processing engine," respectively. *Id.* at 8:16–21.

More importantly, ATI's proposed claim construction would import improperly an extraneous negative limitation into the claims—excluding *type-specific* processing engines. *Hoganas AB v. Dresser Indus., Inc.*, 9 F.3d 948, 950 (Fed. Cir. 1993) ("It is improper for a court to add 'extraneous' limitations to a claim, that is, limitations added 'wholly apart from any need to interpret what the patentee meant by particular words or phrases in the claim.'"). Such a claim construction would not be reasonable as it would exclude the *very embodiment* that provides written description support for the claims at issue. *See Kaneka Corp. v. Xiamen Kingdomway*

Group Co., 790 F.3d 1298, 1304 (Fed. Cir. 2015) ("A claim construction that excludes a preferred embodiment is rarely, if ever, correct.").

For all of the reasons discussed above, we decline to adopt ATI's proposed claim construction that excludes *type-specific* processing engines and that requires *each* command processing engine to be able to process *all* of the command threads selected by an arbiter. Rather, consistent with the plain meaning of the claim language, we construe the "command processing engine" limitation recited in claim 5 as requiring each command processing engine to be coupled to an arbiter and operable to receive and process a command thread selected by the arbiter.

B. Antedating Lindholm, Moreton, and Stuttard

LG asserts that each of the following U.S. patents qualifies as prior art under 35 U.S.C. § 102(e)[3] against the challenged claims of the '053 patent, which has an effective filing date of September 29, 2003:

Lindholm filed June 27, 2003 (Ex. 1004, at [22]);

Moreton filed April 21, 2003 (Ex. 1006, at [22]); and

Stuttard filed October 9, 2001 (Ex. 1005, at [22]).

Pet. 10. LG relies upon the U.S. filing dates of these references as the prior art dates under § 102(e). *Id.* Indeed, neither Lindholm nor Moreton claims the benefit of an earlier-filed U.S. application. Ex. 1004, 1; Ex. 1006, 1.

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[3] Because the '053 patent was filed before the enactment of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), the pre-AIA version of 35 U.S.C. § 102(e) applies in this trial.

Stuttard claims under §§ 120 and 365(c), as a continuation, the benefit of International Application No. PCT/GB00/01332 ("the '332 PCT application"), which was filed on April 7, 2000, and published by the International Bureau in the English language as International Patent Publication No. WO 00/62182 ("the '182 international publication") on October 19, 2000. Ex. 1005, at [63], 1:5–9. The international filing date, April 7, 2000, however, is not a U.S. filing date for prior art purposes under § 102(e) because the '332 PCT application was filed prior to November 29, 2000, the effective date of § 102(e).[4] Therefore, the effective date of Stuttard as prior art is its U.S. filing date, October 9, 2001. *See Sun Studs, Inc. v. ATA Equip. Leasing, Inc.*, 872 F.2d 978, 983 (Fed. Cir. 1989) ("When patents are not in interference, the effective date of a reference United States Patent as prior art is its filing date in the United States, as stated in § 102(e), not the date of conception or actual reduction to practice of the invention claimed or the subject matter disclosed in the reference patent.").

As an initial matter, we note that the '182 international publication also is a prior art reference under § 102(b) because it was published on October 19, 2000, which is more than one year prior to the effective filing date of the '053 patent (September 29, 2003). Ex. 1005, at [63], 1:5–9;

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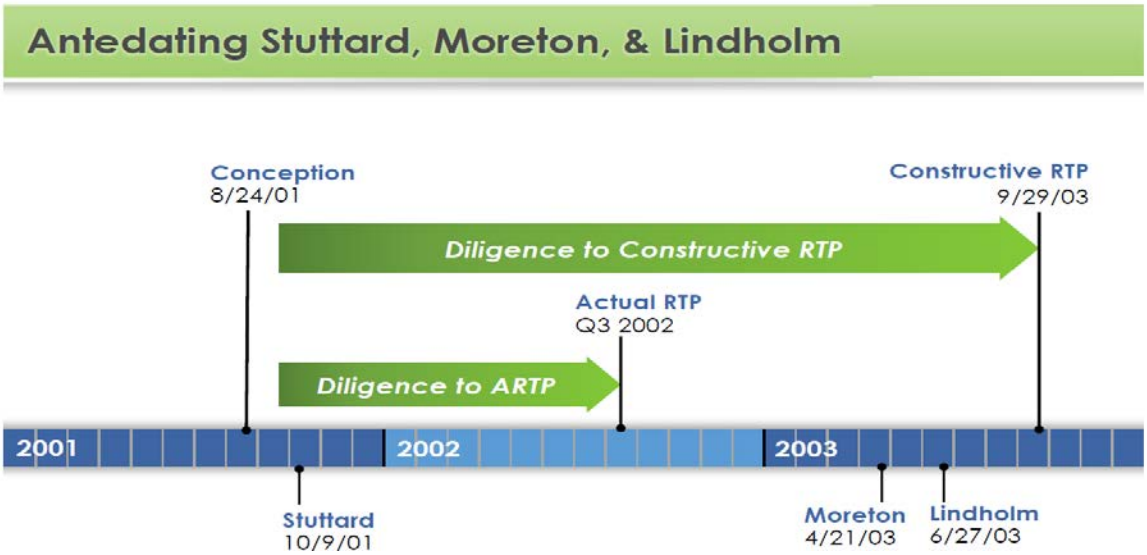
[4] *See* Sections 4505, 4508 of the American Inventors Protection Act of 1999, Pub. L. No. 106-113, 113 Stat. 1501A-552, 565–67 (1999), as amended by the Intellectual Property and High Technology Technical Amendment Act of 2002, Public Law 107-273, 116 Stat. 1158, 1902–03 (2002).

Ex. 3003; Ex. 1001, at [63]. Stuttard and the ’182 international publication have the same disclosure given Stuttard was issued as a patent from a continuation application of the ’332 PCT application that was published as the ’182 international publication. *See Transco Prods. Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 555 (Fed. Cir. 1994) (“‘Continuation and ‘divisional’ applications are alike in that they are both continuing applications based on the same disclosure as an earlier application.”). LG, however, did not assert the ’182 international publication in any of its grounds of unpatentability.

Here, ATI seeks to disqualify Lindholm, Moreton, and Stuttard as prior art under § 102(e) by establishing a date of invention prior to the U.S. filing dates of these references. PO Resp. 15–29. Section 102(e)(2) requires a prior art patent to have a U.S. filing date “before the invention by the applicant for patent.” *See Loral Fairchild Corp. v. Matsushita Elec. Indus. Co., Ltd.*, 266 F.3d 1358, 1362 (Fed. Cir. 2001). In particular, ATI alleges that the named inventors of the ’053 patent conceived the claimed subject matter of the ’053 patent no later than August 24, 2001, before the filing dates of Lindholm, Moreton, and Stuttard. *Id.* at 22–24, 27. ATI also contends that the named “inventors were reasonably and continuously diligent to reduce the claimed subject matter to practice.” *Id.* at 2, 24–26, 28–29. Thus, ATI argues diligence from the date of conception until the constructive reduction to practice of the claimed invention on the filing date of the application that issued as the ’053 patent. ATI also argues that the

claimed invention was actually reduced to practice before the filing dates of Lindholm and Moreton. *Id.* at 15–22.

ATI provides the following timeline:



Ex. 2155, 3. An inventor "may date his patentable invention back to the time of its conception, if he connects the conception with its reduction to practice by reasonable diligence on his part, so that they are substantially one continuous act." *Mahurkar v. C.R. Bard, Inc.*, 79 F.3d 1572, 1577 (Fed. Cir. 1996).

<u>Constructive Reduction to Practice</u>

Constructive reduction to practice occurs when a patent application on the claimed invention is filed. *Weil v. Fritz*, 572 F.2d 856, 865 n.16 (CCPA 1978). On its face, the '053 patent claims under § 120, as a continuation, the benefit of the filing date of U.S. Application 10/673,761, filed on September 29, 2003. Ex. 1001, at [63]. LG does not challenge that the effective filing date of the '053 patent is September 29, 2003. *See generally*

Reply. On this record, we, therefore, determine that ATI's date of constructive reduction practice is September 29, 2003.

Conception

"Conception must be proved by corroborating evidence which shows that the inventor disclosed to others his completed thought expressed in such clear terms as to enable those skilled in the art to make the invention." *Coleman v. Dines*, 754 F.2d 353, 359 (Fed. Cir. 1985).

Here, ATI alleges that the named inventors conceived the claimed subject matter no later than August 24, 2001, while designing a graphics processing unit known as the R400 Graphics Processing System ("the R400"). PO Resp. 1–3, 7–11, 23–24. ATI relies on Version 0.4 of the R400 Sequencer Specification (Ex. 2010) as evidence of conception. PO Resp. 11. As support, ATI also proffers a Declaration of Mr. Laurent Lefebvre (Ex. 2006), one of the named inventors of the '053 patent, and a Declaration of Dr. Wolfe (Ex. 2106 ¶ 240) to explain how the R400 Sequencer Specification discloses every element of each challenged claim.

LG does not dispute the sufficiency of the R400 Sequencer Specification for showing conception. *See generally* Reply. Based on the evidence before us, we are satisfied with the sufficiency of the documents to show conception, and they also serve as effective corroboration to Mr. Lefebvre's testimony as to establishing conception. Exs. 2006, 2106, 2010, 2028, 2040, 2041. On this record, we, therefore, determine that ATI has demonstrated by a preponderance of the evidence that the named inventors of the '053 patent conceived the claimed system no later than

August 24, 2001, prior to the U.S. filing dates of Stuttard, Moreton, and Lindholm.

Actual Reduction to Practice

In order to establish an actual reduction to practice, the inventor must establish that: (1) the inventor constructed an embodiment or performed a process that met all of the claim limitations; and (2) the invention would work for its intended purpose. *Cooper v. Goldfarb*, 154 F.3d 1321, 1327 (Fed. Cir. 1998). The inventor's testimony must be corroborated by independent evidence. *Id.* at 1330. A rule of reason applies to determine whether the inventor's testimony has been corroborated. *Price v. Symsek*, 988 F.2d 1187, 1194 (Fed. Cir. 1993). "The rule of reason, however, does not dispense with the requirement for some evidence of independent corroboration." *Coleman*, 754 F.2d at 360. The requirement of "independent" corroboration requires evidence other than the inventor's testimony. *In re NTP, Inc*. 654 F.3d 1279, 1291 (Fed. Cir. 2011).

Here, ATI asserts that the register-transfer level ("RTL") code (Exs. 2072–87) in hardware-description language for the R400 is a constructed embodiment of the claimed invention. PO Resp. 3, 16–22. As support, ATI proffers a Declaration of Dr. Wolfe (Ex. 2106) to demonstrate how the RTL code maps to each claim at issue, and a Declaration of Mr. Lefebvre (Ex. 2006) to explain why the first-triangle test shows that the RTL code worked for its intended purpose. PO Resp. 3.

LG counters that ATI fails to provide sufficient evidence to establish that the named inventors constructed a *physical* embodiment because

computer simulations that were never reduced to a physical embodiment cannot serve as an actual reduction to practice. Reply 2–3. LG also alleges that ATI has not shown that its code actually worked for its intended purpose because ATI's evidence shows that the code had a number of problems. *Id.* at 5–7. LG further contends that the evidence does not show the RTL code passed the first-triangle test on July 1, 2002, as the RTL code has a revision date of August 5, 2002, which is after the alleged test. *Id.* at 7; Ex. 2066, 6.

In its Sur-reply, ATI responds that a *physical* embodiment is not required to establish an actual reduction to practice. Sur-reply 2–4 (citing *Cooper*, 154 F.3d at 1328; *Yorkey v. Diab*, 601 F.3d 1279, 1290–91 (Fed. Cir. 2010)). ATI also asserts that the RTL code is an embodiment that discloses every claim element and maps to hardware. *Id.* at 3–4. According to ATI, its evidence shows that the first-triangle test was conducted successfully. *Id.* at 4. ATI cites to Mr. Lefebvre's testimony (Ex. 2006 ¶ 47), and the Program Review Slides (Ex. 2062, 4; Ex. 2066, 2, 6) for support.

Requirement of a physical embodiment

It is well settled that "[t]here cannot be a reduction to practice of the invention . . . without a *physical embodiment* which includes all limitations of the claim." *UMC Elecs. Co. v. United States*, 816 F.2d 647, 652 (Fed. Cir. 1987) (emphasis added). "It is equally well established that every limitation of the [claim] *must exist* in the embodiment and be shown to have performed as intended." *Newkirk v. Lulejian*, 825 F.2d 1581, 1582 (Fed. Cir. 1987) (emphasis added).

Here, based on the evidence in this trial, we are not persuaded that ATI has demonstrated that the claimed system was actually reduced to practice. In its Patent Owner Response and Sur-reply, ATI does not contend that it constructed a hardware device in accordance with the challenged claims. Nor has ATI established that an implementation based on the RTL code constitutes the subject matter of the challenged claims in this record. At best, ATI has shown that the RTL code constitutes software files in a hardware description language that describes the logical design and behavior of the system. ATI, however, has not demonstrated that the design *inferred* by the RTL code was synthesized into a set of interconnected hardware devices. It is well-established that an *equivalent* of a physical embodiment does not satisfy the first requirement of actual reduction to practice. *Eaton v. Evans*, 204 F.3d 1094, 1097–98 (Fed. Cir. 2000) (holding that a party cannot obviate the first requirement of constructing a physical embodiment through evidence of testing an equivalent).

At the outset, we note that the claims at issue are apparatus claims directed to a *graphics processing system*, and not a *circuit design*, as ATI alleges (Sur-reply 4). *See* Ex. 1001, 7:10–8:28. As Dr. Wolfe testifies, both circuit design and fabrication are necessary components of constructing a physical integrated circuit, commonly referred to as "a chip." Ex. 2106 ¶¶ 32–33. It is undisputed that ATI submits no evidence to show that a sample or prototype for the R400 was fabricated before the filing dates of the asserted references. PO Resp. 7–9; Sur-reply 3–4; Tr. 80:1–3. A *design*, by itself, is not a physical hardware element, let alone a graphics processing

system. Therefore, such a design is insufficient to show an actual reduction to practice of the claimed graphics processing system. *See UMC*, 816 F.2d at 652 ("It is not sufficient for a reduction to practice that [the inventor] built and tested only a part of the later-claimed model UMC-B accelerometer."); *Fitzgerald v. Arbib*, 268 F.2d 763, 765–66 (CCPA 1959) (noting that the reduction to practice of a three-dimensional design invention required the production of an article embodying that three-dimensional design and not a mere drawing); *In re McIntosh*, 230 F.2d 615, 619 (CCPA 1956) (holding that drawings and models could establish only conception, but not actual reduction to practice, because "there is nothing of record to suggest that appellant ever made or tested a full-sized airplane constructed in accordance with any of the appealed claims").

We are not persuaded by ATI's argument that a *physical* embodiment is not required to establish an actual reduction to practice of the recited system. PO Resp. 19–21; Sur-reply 2. ATI's reliance on *Cooper* to support its argument is misplaced. Sur-reply 2 (citing *Cooper*, 154 F.3d at 1328). In fact, *Cooper* specifically quotes *UMC*, which states that "[t]here cannot be a reduction to practice of the invention . . . *without a physical embodiment* which includes all limitations of the claim," and further explains that "the *physical* embodiment relied upon as an actual reduction to practice must include every limitation." *Cooper*, 154 F.3d at 1327 (quoting *UMC*, 816 F.2d at 652; citing *Correge v. Murphy*, 705 F.2d 1326, 1329 (Fed. Cir. 1983)) (emphases added). Moreover, it was undisputed that a physical embodiment was constructed in *Cooper*. The inventor in *Cooper* conducted

successfully a series of experiments with physical embodiments of the claimed artificial vascular graft. *Cooper*, 154 F.3d at 1324 ("The parties agree that a single successful graft in a dog would constitute an actual reduction to practice.").

ATI's reliance on *Yorkey* also is unavailing. PO Resp. 17; Sur-reply 2 (citing *Yorkey*, 601 F.3d at 1290–91). *Yorkey* involved *method claims* directed to a method of measuring saturation of a blood constituent, whereas the instant trial involves *apparatus claims* directed to a graphics processing system comprising an arbiter coupled to a memory device and a plurality of command processing engines. *Yorkey*, 601 F.3d at 1282; Ex. 1001, 7:10–8:28. To show an actual reduction to practice of a claimed apparatus, as here, the inventor must *construct a physical embodiment* that includes all the claimed apparatus elements. *UMC*, 816 F.2d at 652; *Fitzgerald*, 268 F.2d at 765–66; *Correge*, 705 F.2d at 1329 ("The *physical* embodiment relied upon as an actual reduction to practice of the invention . . . must include every essential limitation." (emphasis added)).

Furthermore, in *Yorkey*, it was uncontested that the method was performed successfully in measuring blood oxygen saturation, and the software program implementing the central equation of the eta methodology was tested using data collected from patients in hospitals and in-house clinical studies. *Yorkey*, 601 F.3d at 1287–90. Such circumstances are not present here. In fact, ATI does not contend that the computer system executing the RTL code encompasses the claimed graphics processing system, but rather the RTL code, by itself, which purportedly "defines the

actual hardware of the chip" and serves as "an accurate representation of a hardware chip design," is sufficient as an embodiment to show actual reduction to practice. PO Resp. 8–9, 16–21; Sur-reply 3–4; Ex. 2106 ¶¶ 31, 32. Simply mapping a software code to hardware features is insufficient to show that the hardware features actually existed. *See Newkirk*, 825 F.2d at 1582–83 (noting that proof of actual reduction to practice requires showing that the claimed apparatus features actually existed).

Calling the RTL software code an embodiment or implementation of the claimed system does not change the fact that the claimed hardware elements do not exist. At most, the RTL code represents a logical behavior design from which a hardware implementation can be *inferred*. However, "there can be no actual reduction to practice if the constructed embodiment . . . lacks an element recited in the [claim] or *uses an equivalent of that element*." *Eaton*, 204 F.3d at 1097 (emphasis added). Hence, we do not discern that either *Cooper* or *Yorkey* supports ATI's proposition that no *physical* embodiment is required, or that a "representation of a hardware chip design" constitutes an actual reduction to practice of a physical integrated circuit.

ATI also argues that a *physical* embodiment is not required simply because a *commercially acceptable* embodiment is not required for establishing actual reduction to practice. PO Resp. 19–21; Sur-reply 2–3. ATI, however, conflates the two distinct and separate requirements of actual reduction to practice: (1) constructing a physical embodiment, and (2) testing the embodiment. "An invention is actually reduced to practice

when [1] it is put into *physical form* and [2] shown to be operative in environment of its practical contemplated use." *See Technical Dev. Corp. v. United States*, 597 F.2d 733, 746–47 (Ct. Cl. 1979). For the testing requirement, "[l]aboratory tests, rather than tests under actual use or service conditions, may be sufficient to constitute actual reduction to practice if the conditions of the test adequately simulate the conditions of practical use." *Id.* at 747. However, permitting laboratory test simulation to satisfy the testing requirement does not eliminate the physical embodiment requirement. *See Eaton*, 204 F.3d at 1097; *Wetmore v. Quick*, 536 F.2d 937, 942 (CCPA 1976) (finding that, despite successful testing, there was no actual reduction to practice where the embodiment used an equivalent of an element).

ATI's reliance on *Scott v. Finney* also is misplaced, as the Court in *Scott* was addressing the *testing* requirement. 34 F.3d 1058, 1061 (Fed. Cir. 1994) (noting that actual reduction to practice "does not require that the invention, *when tested*, be in a commercially satisfactory stage of development" (emphasis added)). In *Scott*, there was no dispute that the physical embodiment actually existed. *Id.* at 1059. A videotape showed an operation where the surgeon inserted Dr. Scott's prototype device into an anesthetized patient. *Id.* at 1060–1063. Nothing in *Scott* suggests that a physical embodiment is not required, as alleged by ATI. *Id.* More importantly, in *Eaton*, the Federal Circuit expressly rejected the argument that satisfying the testing requirement eliminates, or acts as a surrogate for, the requirement of constructing a physical embodiment, because such an

argument "misapprehends this Court's precedent and conflates the two requirements." *Eaton*, 204 F.3d at 1098 (holding that a party cannot obviate the first requirement for a physical embodiment through evidence of testing an equivalent, regardless of the quality of such evidence). "Put simply, these are two distinct requirements and a party must satisfy each one to establish an actual reduction to practice." *Id.*

We also are not persuaded by ATI's argument that the inventive process for the claimed invention ended after chip design, "so it is logical that RTL is a valid reduction to practice." IPR2015-00330, Paper 36, Sur-reply 2. This argument squarely contradicts our reviewing Court's precedent that requires a physical embodiment, and that there is no actual reduction to practice if the embodiment is merely an equivalent. *Eaton*, 204 F.3d at 1097–98; *Wetmore*, 536 F.2d at 942; *Martin v. Snyder*, 214 F.2d 177, 180 (CCPA 1954) (holding that doctrine of equivalents does not apply when determining whether a constructed embodiment contained every element of the invention). Moreover, ATI's argument conflates actual reduction to practice with *conception*, which is established when the inventive process ends. *See Hybritech Inc. v. Monoclonal Antibodies Inc.*, 802 F.2d 1367, 1376 (Fed. Cir. 1986) (Conception is the "formation in the mind of the inventor of a definite and permanent idea of the complete and operative invention as it is thereafter to be applied in practice."); *Townsend v. Smith*, 36 F.2d 292, 295 (CCPA 1930) (defining conception as "the complete performance of the mental part of the inventive act"). As discussed above, actual reduction to practice is established only when the invention "is put

into *physical form* and shown to be operative in environment of its practical contemplated use." *Technical Dev.*, 597 F.2d at 746–47 (emphasis added).

In light of the foregoing, and consistent with our reviewing Court's precedent, we determine that a *physical* embodiment of the claimed graphics processing system is required here, and that a *circuit design*, by itself, is insufficient to establish actual reduction to practice.

ATI does not contend that the computer system executing the RTL code encompasses the claimed graphics processing system, but rather the RTL code, alone, is an embodiment of the claimed system. PO Resp. 7–9, 16–21; Sur-reply 3–4. ATI argues that the entire chip-design industry recognizes that once a chip has been defined in a hardware-description language, as here, "an embodiment of the chip has been constructed." PO Resp. 18–19. ATI alleges that the RTL code "defines the actual hardware of the chip," and, as a result, the RTL code is "an implementation" of the graphic processing unit ("GPU"). *Id.* at 8–9.

We are not persuaded by ATI's argument that the RTL code, alone, is sufficient to meet the first requirement of actual reduction to practice—constructing a *physical* embodiment. PO Resp. 7–9, 16–20; Sur-reply 3–4. At best, the RTL code is a chip design or a software program that represents the logical design behavior of the claimed graphics processing system. As ATI's own expert, Dr. Wolfe, explains, RTL code is "generally used to model, define, and instantiate a hardware design." Ex. 2106 ¶ 23. According to Dr. Wolfe, "[w]hile the design representation at this stage may resemble software, its primary purpose is to be an accurate representation of

a hardware chip design." *Id.* ¶ 32. Dr. Wolfe also testifies that the "R400 Emulator Code . . . emulates the behavior of the graphics-processing system recited in claims 1, 2, 5, 6, and 7 using software that executes on a computer." Ex. 2106 ¶ 37. Based on Dr. Wolfe's testimony, we observe that the RTL code is merely a representation of a chip *design* or a software program that *emulates* the behavior of a physical system that includes hardware elements, but it is not a *physical* embodiment of that system.

ATI further asserts that it is an integrated circuit design company, so that the actual reduction to practice was in the RTL code. PO Resp. 3. ATI argues that the fabrication phase begins only after the RTL code has been thoroughly tested, and the designer's final product is the RTL code, which is converted into a "GDSII or *tape-out* file and sent to a circuit-fabrication facility." *Id.* at 9 (emphasis in the original). According to ATI, the fabrication process "is very expensive, so a graphics-processing company, such as ATI, will typically tape-out a GPU only if the design is ready for commercialization—meaning that the GPU design has passed hundreds, if not thousands, of tests." *Id.*

ATI's evidence, however, shows that it was scheduled to obtain a sample or prototype of the R400 in May 2002. Ex. 2040, 8. ATI confirms that there was a plan, at the outset, to make a prototype of the chip. Tr. 81:10–16. ATI also acknowledges that "there was actually never a tape out, a sample, or a production for the R400," but ATI did not submit any evidence as to why ATI could not have obtained a prototype of the R400, other than commercially related reasons. Tr. 80:2–11, 82:5–10.

In any event, either allegation that ATI is a chip-design company or that the fabrication phase of making a chip is a very expensive process, even if they were true, does not discharge ATI from satisfying the requirement of constructing a *physical* embodiment. *Eaton*, 204 F.3d at 1098; *Fitzgerald*, 268 F.2d at 765–66. In addition, ATI's arguments are premised improperly on the notion that constructing a physical embodiment would require the inventors to fabricate, personally themselves, a chip with a commercially acceptable design. It is well-settled that a reduction to practice can be done by another on behalf of the inventor. *Solvay S.A., v. Honeywell Int'l Inc.*, 742 F.3d 998, 1000 (Fed. Cir. 2014); *In re De Baun*, 687 F.2d 459, 463 (CCPA 1982) ("[T]here is no requirement that the inventor be the one to reduce the invention to practice so long as the reduction to practice was done on his behalf."). "Commercially acceptable structure or operation is not necessary for a reduction to practice." *Goodrich v. Harmsen*, 442 F.2d 377, 383 (CCPA 1971). Furthermore, the inventors had the opportunity to establish constructive reduction to practice by filing a patent application upon conception, avoiding the cost and delay of constructing a physical embodiment of their invention. *See Weil*, 572 F.2d at 865 n.16; *In re Mulder*, 716 F.2d 1542, 1545 (Fed. Cir. 1983) (holding that appellants are entitled to rely on their filing date for a constructive reduction to practice); *see also Grabowsky v. Gallaher*, 39 App. D.C. 548, 551–52 (D.C. Cir. 1913) ("Appellant seeks to excuse this delay by the plea that he was a poor man and did not have the means to actually reduce the invention to practice, which, undoubtedly, would have involved considerable expense. Granting

this to be true, the record fails to show that he was unable to pay the cost of preparing and prosecuting an application, which it was his duty to do.”). Here, ATI chose to wait more than two years from conception to file a patent application, while others—Stuttard, Moreton, and Lindholm—filed their applications earlier. *Naber v. Cricchi*, 567 F.2d 382, 385 n.5 (CCPA 1977) (“Public policy favors the early disclosure of invention.”); *Gould v. Schawlow*, 363 F.2d 908, 921 (CCPA 1966).

Based on the evidence before us, we determine that ATI has not demonstrated by a preponderance of the evidence that the claimed invention was actually reduced to practice. For the reasons discussed below, even if we were to accept the RTL code as a physical embodiment of the claimed system, we find that ATI fails to provide sufficient evidence in this record to show that the RTL code was tested successfully and adequately to prove that the claimed system would have worked for its intended purpose.

Testing requirement

To show actual reduction to practice, the inventor also must demonstrate that the claimed invention would work for its intended purpose. *Cooper*, 154 F.3d at 1327. Here, ATI relies on Mr. Lefebvre’s testimony (Ex. 2006 ¶¶ 44–52) to show that the RTL code (Exs. 2072–87), submitted as evidence of actual reduction to practice, worked for its intended purpose, and several PowerPoint slides (*e.g.*, Ex. 2066, 2, 6) to corroborate Mr. Lefebvre’s testimony. PO Resp. 13–15, 21–22; Sur-reply 1, 4. LG counters that the high-level slides are insufficient corroborating evidence,

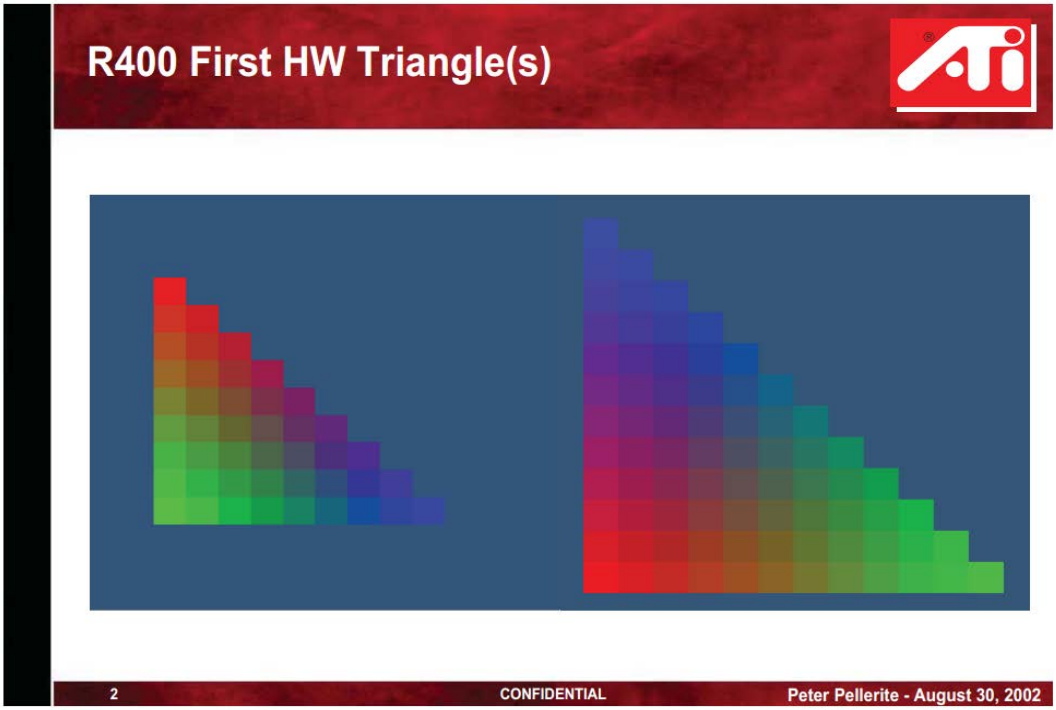
and that ATI does not proffer any witness to explain how the slides relate to the claimed elements. Reply 2. On this record, we agree with LG.

We recognize that "some inventions are so simple and their purpose and efficacy so obvious that their complete construction is sufficient to demonstrate workability." *Mahurkar*, 79 F.3d at 1572. "Complex inventions and problems in some cases require laboratory tests that accurately duplicate actual working conditions in practical use," however. *Scott*, 34 F.3d at 1062. "[T]he testing requirement depends on the particular facts of each case, with the court guided by a common sense approach in weighing the sufficiency of the testing." *Id.* at 1061. Commercial perfection or absolute replication of the circumstances of the claimed invention's ultimate use is not required. *Id.* at 1063. "Laboratory tests, rather than tests under actual use or service conditions, may be sufficient to constitute actual reduction to practice if the conditions of the test adequately simulate the conditions of practical use." *Technical Dev.*, 597 F.2d at 747; *Elmore v. Schmitt*, 278 F.2d 510, 513 (CCPA 1960).

Here, ATI does not assert that the claimed graphics processing system is so simple that it needs no testing to show actual reduction to practice. PO Resp. 13–15. Rather, ATI asserts that, "[t]o validate the R400 design and before a tape-out could occur, the design had to pass hundreds, if not thousands, of tests." *Id.*; Ex. 2006 ¶ 47. In the context of the '053 patent, we agree with ATI that testing is required to show that the claimed system would work for its intended purpose, but, on this record, we do not find that

there is sufficient evidence to show that the claimed invention would work for its intended purpose.

Mr. Lefebvre testifies that the R400 team developed the C++ emulation code and RTL code for the various blocks of the R400, and the code was tested extensively on individual blocks and the entire graphics core during the development process. Ex. 2006 ¶¶ 44–46. Yet, Mr. Lefebvre and ATI direct our attention to only one reported result of a "first triangle" test, which was allegedly conducted on July 1, 2002. *Id.* ¶¶ 44–49; PO Resp. 13–15, 21–22. That report is provided in the form of two high-level PowerPoint slides, reproduced below with a green marking added (Ex. 2066, 2, 6; Ex. 2155, 27; Papers 63, 64).



R400 Program Schedule

Task	Plan	Actual	Forecast
Significant Architecture Issue Identification Complete	10-15-01	10-10-01	
Emulator Test template Complete	01-18-02	01-18-02	
GC Emulator integration – 1 triangle	02-22-02	02-21-02	
Core Emulator pixel / shader tests run	03-15-02	03-19-02	
Block Testing Begins	04-16-02	05-01-02	
GC/Chip Integration Start	05-17-02	05-15-02	
Simulate 1 Triangle / Emulator ready for SW	06-15-02	07-01-02	
First Syntheses	07-12-02	08-03-03	
Verilog Feature Complete	09-16-02		09-30-02
IKOS Emulation start	10-11-02		10-11-02
Begin early block delivery	11-08-02		11-15-02
IKOS Emulation (w/ Software) begins	11-11-02		11-11-02
RTL Freeze / Final Netlist (Gate level ECO only)	11-15-02		12-15-02
A11 Base Layers Tapeout	01-10-03		02-14-03
A11 Metal Layers Tapeout	01-24-03		02-28-03
First Samples for Engineering			05-09-03
A12 Tapeout			06-14-03
A12 Samples for Engineering			07-12-03
R400 Customer Samples			07-19-03
Volume Ramp			08-19-03
Product Delivery			09-01-03

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Slide 2 shows two triangles with a heading "R400 First HW Triangle(s)" and Slide 6 is a high-level program schedule, which states, in part, "Simulate 1 Triangle / Emulate ready for SW" for the July 1, 2002 entry under the "Actual" column. *Id.* The slides are silent as to what was tested, how the triangles were generated, and what software program or computer system generated the triangles. Significantly, the slides do not indicate whether the key claimed elements were tested—e.g., what priority scheme, if any, was tested; how many command processing engines, if any, were tested; or whether each command process engine was tested to demonstrate that it can execute a pixel or vertex command thread.

The slides are said to be a part of Mr. Peter Pellerite's presentation. Sur-reply 4. Yet, ATI did not submit a declaration from Mr. Pellerite, or

anyone else who could explain meaningfully what these slides purportedly show. Nor does its expert, Dr. Wolfe, testify that he executed the RTL code and that the code actually worked. Ex. 1020, 305:11–22. In sum, the slides provide insufficient detail as to whether the RTL code actually passed the "first triangle" test. *See Newkirk*, 825 F.2d at 1583 ("Proof of actual reduction to practice requires more than theoretical capability.").

Mr. Lefebvre testifies that "I recall the first triangle test being successful approximately mid-way through the R400 project. Consistent with my memory, the PowerPoint slide shows that the first triangle was reported during a meeting on August 30, 2002." Ex. 2006 ¶ 49. Mr. Lefebvre also testifies that "[a]ccording to this presentation, the first triangle was completed on July 1, 2002." *Id*. However, Mr. Lefebvre's testimony is vague and conclusory, and is not corroborated with independent evidence. ATI's declarant, Mr. Watson, testifies that the files submitted as Exhibits 2072–2104 and 2108, which contain the RTL code and the emulator code, have a revision date of August 5, 2002. Ex. 2105 ¶ 132. According to ATI, the RTL code for R400 was not completed until October 31, 2002. PO Resp. 14–15; Ex. 2068, 1; Ex. 2069, 6; Ex. 2071, 7. It is unclear whether the particular RTL code with a revision date of August 5, 2002 (Exs. 2072–87), submitted as evidence of actual reduction to practice, is the same code that allegedly passed the "first triangle" test on July 1, 2002. ATI proffers insufficient explanation or credible evidence to show that they are the same code. As discussed above, the high-level PowerPoint slides (Ex. 2066, 2, 6) that both ATI and Mr. Lefebvre rely upon

do not identify which software program or computer system generated the triangles. ATI fails to provide sufficient independent evidence to corroborate Mr. Lefebvre's testimony that the RTL code passed the "first triangle" test on July 1, 2002, and, therefore, Mr. Lefebvre's testimony is entitled to little, if any, weight. *See NTP*, 654 F.3d at 1291; *Mahurkar*, 79 F.3d at 1577 (noting that the requirement for corroboration of inventor's testimony arose out of a concern that inventors testifying at trial would be tempted to remember facts favorable to their case by the lure of protecting their patent or defeating another's patent).

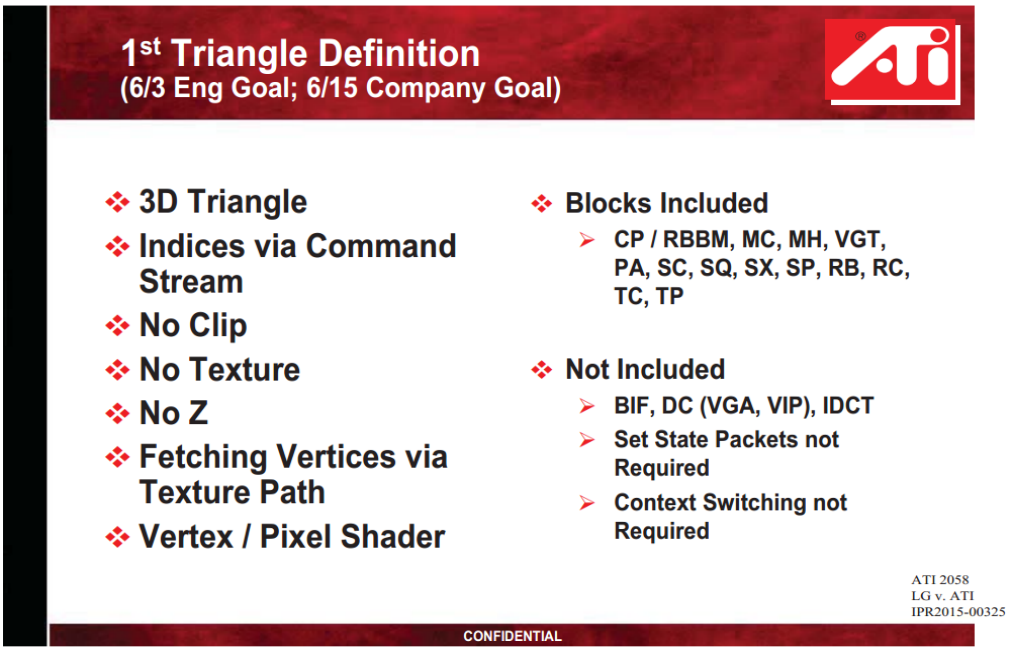
More importantly, neither ATI nor Mr. Lefebvre proffers any meaningful test results, test input or output files, simulation run logs, or input test parameters, which a person with ordinary skill in the art would have expected to see for testing. Ex. 2153, 112:2–14. At a minimum, ATI's evidence must show "the conditions of the test adequately simulate the conditions of practical use." *Technical Dev.*, 597 F.2d at 747. As discussed above, the picture of two triangles and high-level program schedule do not support that the RTL code was tested successfully to establish that the claimed graphics processing system would work for its intended purpose. *See McDonnell Douglas Corp. v. United States*, 670 F.2d 156, 161 (Ct. Cl. 1982) (Proof of actual reduction to practice must show "that the invention will perform its intended function beyond a probability of failure.").

In his declaration, Mr. Lefebvre also mentions other tests. Ex. 2006 ¶¶ 44–47 ("We ran many tests on the R400 during its development. . . . This code was tested extensively . . . . Tests could be run on both the emulation

code and the RTL code, and these tests could be run on individual blocks or the entire graphics core."). Again, Mr. Lefebvre's testimony is vague and is not corroborated sufficiently with independent evidence. There is no evidence in this record that those other tests were conducted successfully. As such, Mr. Lefebvre's testimony is entitled to little, if any, weight. *See NTP*, 654 F.3d at 1291; *Mahurkar*, 79 F.3d at 1577.

The PowerPoint presentation slides cited by ATI are too general, showing high-level schedules and general descriptions of the "first triangle" test. PO Resp. 13–15, 21–22; Ex. 2057, 6, 9; Ex. 2061, 2–5; Ex. 2062, 4; Ex. 2025, 5; Ex. 2071, 7.

For example, one of the PowerPoint presentation slides (Ex. 2058, 1; Papers 63, 64) is reproduced below:



This high-level slide does not show any test results, test input or output files, simulation run logs, or input test parameters. ATI's evidence

does not provide sufficient detail or explanation to demonstrate that the testing would simulate actually the characteristics and environment of an operative graphics processing system in its practical, contemplated setting. *See Technical Dev.*, 597 F.2d at 747–48; *Elmore*, 278 F.2d at 513; *McDonnell Douglas*, 670 F.2d at 162 ("Tests which fail to simulate the varying and multiple conditions of the invention's intended environment will not serve to prove the operability, stability and reliability of the invention for practical use."). ATI's evidence as a whole is insufficient to establish that the RTL code was tested successfully or adequately to show that the claimed system would work for its intended purpose. *See Gordon v. Hubbard*, 347 F.2d 1001, 1007 (CCPA 1965) (finding the evidence as a whole insufficient to establish actual reduction to practice when it "simply relates that tests were performed, and gives no definite indication or suggestion what results were attained or the results were satisfactory").

In his Declaration, Mr. Lefebvre also provides an example as to how the RTL code arbitrates between vertices and pixels. Ex. 2006 ¶¶ 50–51. However, the code alone does not necessarily show that it would accurately reproduce the operating conditions in which the claimed graphics processing system would be encountered in practical use. As discussed above, ATI acknowledges that, "[t]o validate the R400 design and before a tape-out could occur, the design had to pass hundreds, if not thousands, of tests." PO Resp. 13; Ex. 2006 ¶ 47. Without a sufficient showing of a successful test, the RTL code, by itself, does not demonstrate adequately that the claimed system would work for its intended purpose.

In addition, as LG points out, ATI's evidence indicates that there were significant problems in the code. Reply 5–7. For example, the entry on August 26, 2002, in an ATI document log, indicates that the code had a clamping problem that produced a degenerate triangle. Ex. 2048, 50. Mr. Lefebvre explains that a "degenerate triangle is a triangle that has all three vertices along the same axis, so basically transforms the area into a zero area triangle and makes the triangle disappear." Ex. 1035, 151:19–152:5. ATI's logs reveal this clamping problem was still an issue in February 2003. Ex. 2048, 31–32 ("Fixing clamping problem in the emulator."). As additional examples, the document logs for the sequencer's source code indicate the following problems: (1) the entry on July 15, 2002, stating "[f]ixed the event interface in the SQ [sequencer] . . . which was then crashing the numerical library" (Ex. 2048, 54); (2) the entry on August 5, 2002, stating "[f]ixed a parameter generation bug in SQ [sequencer] which was causing the emulator to crash" (*id.* at 52); (3) the entry on August 26, 2002, stating "[f]ixed 3 bugs in the HW accurate interpolators," which was causing two triangle tests to fail (*id.* at 50); (4) the entry on January 7, 2003, stating "[f]ound a major bug in the SQ [sequencer]" (*id.* at 36); (5) the entry on June 19, 2003, stating "this was causing a failure on a WQL test" and "[t]his was causing r400sx_wrapper _01.ccp to fail (this is a test that I wrote to duplicate the WQL test that was failing in order to run it on HW)" (*id.* at 21); and (6) the entry on November 11, 2003, stating "[t]hese shaders were all broken because the address register was not refreshed prior to use" (Ex. 2052, 46). In June 2003, one of ATI's engineers made a change to the

connection between the SX block and the SQ and explained that he was "not sure how this was working at all with the live SX" beforehand. Ex. 2049, 57. On October 8, 2003, an engineer "[a]dded needed include files" and remarked that it was "[s]trange how these compiled before this." *Id.* at 35. Mr. Vargas also testifies that the version of the code provided by ATI for his review may not have been able to pass a triangle test, noting that the comments in the RTL code indicate that there were known problems. Ex. 1013 ¶¶ 43–47 (citing Ex. 2072, 38:7, 42:11; Ex. 2078, 2:1–4; Ex. 2080, 20:17–18; Ex. 2081, 2:1–4). Although Dr. Wolfe testifies that the RTL code maps to each claimed element, Dr. Wolfe did not testify that he executed the RTL code and that the code actually worked. Ex. 1020, 305:11–22.

In its Sur-reply, ATI does not provide sufficient explanation or credible evidence as to why a code that forms a degenerate triangle would be considered to have passed the "first triangle" test. Rather, ATI responds that the comments identified by LG are related to the emulator code—the code that ATI does not rely on for its actual reduction to practice. Sur-reply 4. Dr. Wolfe, however, testifies that chip "designers would ordinarily use the emulator code such as this to design the integrated circuits as part of their design process." Ex. 2106 ¶¶ 38, 142. ATI confirms that the emulator code "can be tested in a simulated environment to determine whether the GPU design functions properly and is, therefore, an important first step in the GPU design process." PO Resp. 8. ATI further relies on the development and testing of the emulator code, as activities that were directed toward actual reduction to practice of the claimed system, to establish reasonable

diligence. *Id.* at 24–26. In light of the evidence before us, we are not persuaded that the RTL code, without testing, establishes that the claimed system would work for its intended purpose.

We have considered ATI's evidence in this record. We, however, are not persuaded that the evidence as a whole supports that the RTL code submitted by ATI, as evidence of actual reduction to practice (Exs. 2072–87), was tested successfully under conditions that adequately simulate the conditions of practical use. *McDonnell Douglas*, 670 F.2d at 163 (indicating that no reduction to practice until physical tests showed capability of actually working). For the foregoing reasons, even if we were to accept ATI's proposition that the RTL code is a physical embodiment of the claimed system, we determine that ATI fails to demonstrate by a preponderance of the evidence that the RTL code was tested successfully to show that the claimed system would work for its intended purpose.

Reasonable Diligence

"The reasonable diligence standard balances the interest in rewarding and encouraging invention with the public's interest in the earliest possible disclosure of innovation." *Griffith v. Kanamuru*, 816 F.2d 624, 626 (Fed. Cir. 1987). During the period in which reasonable diligence must be shown, there must be continuous exercise of reasonable diligence. *McIntosh*, 230 F.2d at 619; *see also Burns v. Curtis*, 172 F.2d 588, 591 (CCPA 1949) (referring to "reasonably continuous activity"). A party alleging diligence must account for the entire critical period. *Griffith*, 816 F.2d at 626. Even a short period of unexplained inactivity is sufficient to defeat a claim of

diligence. *Morway v. Bondi*, 203 F.2d 742, 749 (CCPA 1953); *Ireland v. Smith*, 97 F.2d 95, 99–100 (CCPA 1938).

To satisfy the reasonable diligence requirement, "the work relied on must ordinarily be directly related to reduction to practice of the invention." *Naber v. Cricchi*, 567 F.2d 382, 385–86 (CCPA 1977) (citing *Anderson v. Scinta*, 372 F.2d 523 (CCPA 1967); *Gunn v. Bosch*, 181 USPQ 758 (BPAI 1973); *Moore v. Harris v. Hale*, 92 USPQ 187 (BPAI 1951)) (holding that the work done directed at improving oxide and nitride layer deposition techniques generally applicable to all MNOS devices, not merely the drain-source protected device of the claimed invention, did not satisfy the requirement of reasonable diligence). The work done directed to the *generic* invention cannot be relied upon as evidence of diligence for the *specific* claimed invention. *In re Nelson*, 420 F.2d 1079, 1081 (CCPA 1970) ("[W]e must consider the evidence only as it relates to the specific invention claimed."). A party alleging diligence must provide corroboration with evidence that is specific both as to facts and dates. *Gould*, 363 F.2d at 920; *Kendall v. Searles*, 173 F.2d 986, 993 (CCPA 1949). The rule of reason does not dispense with the need for corroboration of diligence that is specific as to dates and facts. *Gould*, 363 F.2d at 920; *Kendall*, 173 F.2d at 993; *Coleman*, 754 F.2d at 360.

Here, ATI bears the burden of production in antedating the asserted references. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378–80 (Fed. Cir. 2015). ATI acknowledges that it must establish reasonable diligence from just before each reference's filing date until its

own constructive reduction to practice, September 29, 2003, because we determine that ATI did not meet its burden of establishing actual reduction to practice. PO Resp. 27. As discussed above, ATI's conception date is August 24, 2001, which predates Stuttard's filing date (October 9, 2001), Moreton's filing date (April 21, 2003), and Lindholm's filing date (June 27, 2003). *Id.* at 24–29. Accordingly, ATI must establish reasonable diligence for the following three critical periods:

Critical Period 1 – from just before Stuttard's filing date, October 9, 2001, to September 29, 2003;

Critical Period 2 – from just before Moreton's filing date, April 21, 2003, to September 29, 2003; and

Critical Period 3 – from just before Lindholm's filing date, June 27, 2003, to September 29, 2003.

To establish reasonable diligence during all three critical periods, ATI relies upon a Declaration of Mr. Lefebvre (Ex. 2006), and the metadata in document logs and folder histories (Exs. 2048–52, 2107) to show that over 100 project managers and designers worked every non-holiday business day to reduce the claimed system to practice. PO Resp. 11–13, 24–26, 28–29. As support, Mr. Lefebvre provides a calendar (Ex. 2006, Part V, 31–56) to show that at least one person on the R400 project team worked on the R400 design every non-holiday business day from August 24, 2001 until September 29, 2003. Ex. 2006 ¶ 42, Part V; Exs. 2048–52, 2107. The calendar references the following document logs and folder histories: R400 Sequencer Emulator Folder History (Ex. 2048, "Em."); R400 Sequencer

Parts Folder History (Ex. 2049, "Parts"); R400 Document Library Folder History (Ex. 2050, "Lib."); R400 Architecture Folder History (Ex. 2051, "Arch."); R400 GFX Testing Folder History (Ex. 2052, "Test"); and R400 Shader Pipe Parts Folder History (Ex. 2107, "SP Parts"). Ex. 2006, 31.

In its Reply, LG counters that ATI's calendar (Ex. 2006, Part V, 31–56) is directed to the entire R400 project, and not simply the claimed system of the '053 patent. Reply 8–9. LG notes, for example, the GFX Testing Folder History (Ex. 2052) includes all of the tests on the R400 project, and ATI failed to parse out which tests were related to the blocks that allegedly embody the claims and which tests related only to other blocks. *Id.* at 11. According to LG, "ATI's work for an entire graphics chip containing numerous subparts wholly unrelated to these features cannot establish diligence." Reply 9.

In response, ATI disagrees, asserting that the project team could not test the sequencer in isolation, which was the "heart of the chip" and "there was no way to apply the correct stimulus on just the sequencer." Sur-reply 5. ATI also submits that at least one document was checked in every business day during the critical periods, and the metadata associated with each check-in date describes the work that occurred. *Id.*

Upon consideration of the evidence in this entire record, we agree with LG. ATI's calendar, metadata, document logs, and folder histories (nearly 1,300 pages) are not self-explanatory and do not explain meaningfully as to which tasks are reasonably necessary for reducing the claimed elements to practice, and which tasks are directed toward

developing and testing other chip designs and optional features. Ex. 2006, Part V, 33–56; Exs. 2048–52, 2107. Moreover, Mr. Lefebvre's testimony, the only testimony that attempts to explain the work ATI relies upon in support of establishing reasonable diligence, is vague and not sufficiently corroborated by independent evidence. Ex. 2006 ¶¶ 41–43 ("This metadata also shows work on the design and development of the R400 generally."). "Mere work does not necessarily constitute diligence." *Gunn*, 181 USPQ at 761. To satisfy the reasonable diligence requirement, the work relied on must be directed toward, or reasonably necessary for, the reduction to practice of the claimed system. *See Naber*, 567 F.2d at 385.

We are not persuaded by ATI's contention that the work allegedly performed for the entire R400 project satisfies the reasonable diligence requirement. As discussed below, the work done for the entire R400 project includes developing and testing other chip designs and optional features to improve graphic processing systems generally, and not merely for the claimed elements. ATI's general allegation that the sequencer, shader, and texture blocks could not be worked and tested in isolation, or the sequencer was "the heart of the chip," does not explain sufficiently why the work performed on other chip designs and optional features was reasonably necessary for the reduction to practice of the claimed system. PO Resp. 11–12; Sur-reply 5. That allegation also squarely contradicts ATI's own evidence, showing that block level testing can be conducted—e.g., Mr. Lefebvre testifies that "[t]ests could be run on both the emulation code and the RTL code, and these tests could be run on individual blocks or the

entire graphics core." Ex. 2006 ¶¶ 44–47; *see also* Ex. 2056, 14 ("Tests from block level tests"); Ex. 2069, 8 ("Block Level Test Status"); Ex. 2049, 57 ("2003/07/01 by llefebvr . . . Now works on the SQSP testbench.").

Notably, ATI's evidence shows that the R400 project included developing and testing other chip designs: R200 (Ex. 2057, 7–10, 12–14), RV250 (*id.* at 11, 15), R300 (*id.* at 11, 13, 15), and RV450 (*id.* at 3, 16, 17). *See also* Ex. 2039, 5 ("Adding R500 modifications."); Ex. 2041, 6 ("The R450, aimed at a volume high end market."); Ex. 2048, 26 ("Neede[d] to validate load on the R500"); Ex. 2050, 359 ("Updated Appendix for delta between R300 and R400"), 391 ("R300 figures showing the wrapping policies"); Ex. 2059, 6 ("R300 Bring up"); Ex. 2061, 9 ("Entire SC Team consumed for 2 weeks for R300 Hangs (not yet resolved)"). Yet, ATI includes all of the activities for the entire R400 project, as evidence of reasonable diligence, without specifically explaining which activities are directed toward reducing the claimed elements to practice, and which activities are directed toward developing and testing other chip designs. Nor does ATI explain why activities that are directed toward the other chip designs are reasonably necessary for the reduction to practice of the claimed elements, which allegedly are embodied only in the R400 design (PO Resp. 11). In light of the foregoing, we determine that ATI fails to provide evidence that is specific both as to facts and dates for each of the three critical periods, during which diligence is required. *Gould*, 363 F.2d at 920; *Kendall*, 173 F.2d at 993.

Additionally, ATI relies on the first design of R400, as described in Version 0.4 of the R400 Sequencer Specification (Ex. 2010), to establish conception of the claimed invention as of August 24, 2001. PO Resp. 27; Tr. 48:20–49:12. According to ATI, this first design describes all of the claimed elements. PO Resp. 11; Tr. 49:2–4 (This first design "shows that the inventors conceived of the claimed invention, everything that is required for the claimed invention."). Notwithstanding that, Mr. Lefebvre redesigned the R400, after the conception date, to include an optional feature that is not recited in the claims at issue—a sequencer that is capable of processing an *unlimited number of clauses*. PO Resp. 12–13; Ex. 2006 ¶ 15. Mr. Lefebvre explains that "Microsoft wanted the sequencer to be able to run shaders with an unlimited number of clauses/instructions." Ex. 2006 ¶ 30. According to ATI, the reason for the redesign was Microsoft asked "for more general purpose – longer-living model." PO Resp. 12; Ex. 2060, 5. ATI's activities appear more in the nature of commercial development, which is not accepted as an excuse for delay. *See Griffin*, 816 F.2d at 627; *Fitzgerald*, 268 F.2d at 766 ("It is well settled that efforts to exploit an invention commercially do not constitute diligence in reducing it to practice."); *Naber*, 567 F.2d at 385–86 (rejecting the proposition that the reasonable diligence requirement was satisfied, notwithstanding delay due to general work on layer deposition techniques needed to produce a commercially-acceptable device).

ATI's evidence indicates that during the time period between August 24, 2001, and April 19, 2002, Mr. Lefebvre was working on the second chip design to include the optional feature. Ex. 2006 ¶¶ 14, 15;

Exs. 2010, 2028; Ex. 2039, 4 ("Changed the interfaces to reflect the changes in the SP," and "Changed the spec to reflect the new R400 architecture."). ATI also acknowledges that "the evidence goes to both designs and more than both designs." Tr. 51:18–19. Therefore, merely stating that the metadata shows "work on the design and development of the R400 generally" and that "over 100 ATI project managers and designers worked on the R400 project every non-holiday business day" does not satisfy ATI's burden of production. Ex. 2006 ¶¶ 41–42; PO Resp. 28–29. The work done that is directed to the second design for a commercially-acceptable device does not constitute reasonable diligence in reducing the claimed elements to practice. *See Naber*, 567 F.2d at 385–86; *Nelson*, 420 F.2d at 1081; *Fitzgerald*, 268 F.2d at 766. This time period overlaps with Critical Period 1 by at least six months—from just prior to Stuttard's filing date, October 9, 2001, to April 19, 2002. Without a meaningful explanation as to which activities listed in the metadata are directed to the second chip design and which activities are directed to reducing the claimed elements to practice, ATI fails to provide a sufficient account or adequate facts to support a showing of the continuity of activities required for reasonable diligence during the entire Critical Period 1. *See Rieser v. Williams*, 255 F.2d 419, 424 (CCPA 1958) (finding that there was no showing of diligence where no activity was shown during the first thirteen days of the critical period).

According to the R400 Architecture Proposal (dated November 13, 2000), the R400 was scheduled to "tape-out" by April 2, 2002, for fabricating of the chip, "samples" in May 2002, and "production" in

November 2002. Ex. 2040, 8. The R400 Top Level Specification (dated March 11, 2001) also states the "tape-out" for the R400 was scheduled to occur in July 2002. Ex. 2041, 6. Significantly, ATI's evidence indicates at least a delay of nearly eight months due to the redesigning for the optional feature—comparing Version 0.4 of the R400 Sequencer Specification (dated August 24, 2001) describing the first design, with Version 2.0 of the R400 Sequencer Specification (dated April 19, 2002) describing the second design. In fact, Mr. Lefebvre testifies during cross-examination that "the R400 project itself never got taped out." Ex. 1035, 70:20–21. Yet, ATI does not explain sufficiently why implementing the optional feature is reasonably necessary for reducing the claimed elements to practice. *See Griffith*, 816 F.2d at 626 ("The correct inquiry is . . . whether it is reasonable for [the inventor] to require the public to wait for the innovation, given the well settled policy in favor of early disclosure.").

Additionally, the R400 Architecture Proposal (Ex. 2040) and the R400 Top Level Specification (Ex. 2041) indicate that the R400 includes other optional features that are not recited in the challenged claims of the '053 patent—e.g., "nearly transparent dual chip," features for supporting "dual monitor," and a single programmable pipeline that is used for 2D video, 3D vertex, and 3D pixel operations. Exs. 2040, 2041. These documents also reveal that the R400 project includes work for improving other optional features of the prior design, the R300. *See* Ex. 2040, 7 ("We want to further improve the anti-aliasing used in the R300 by reducing the needed memory, and possibly increasing the number of samples per pixel.

The goal is more than fifty percent of the performance and less than three times the memory of anti-aliased rendering. We should also look into improved methods."), 8 ("I would still like to aim for 2x the internal processing capability of the R300"). As ATI's documents describe, the optional features increased costs and delays. *See, e.g.*, Ex. 2040, 6 ("To be able to address the very high end desktop/enthusiast market we will support a glueless two chip design instead of a 256 bit bus. . . . There will be costs added to the base chip to support this. Design time, pins, and area will be impacted by adding this support."), 13 ("Since we support dual monitor, this [total bandwidth requirement] is doubled."); Ex. 2041, 7.

It is well settled that "[d]elays in reduction to practice caused by an inventor's efforts to refine an invention to the most marketable and profitable form have not been accepted as sufficient excuses for inactivity." *Griffin*, 816 F.2d at 627; *Schweyer v. Thomas*, 68 F.2d 953 (CCPA 1934) (explaining that efforts toward commercial exploitation of an invention not yet reduced to practice do not constitute diligence); *see also Naber*, 567 F.2d at 385 (holding that, as "there need not be commercial utility to have a reduction to practice," the inventor cannot rely on the work related to layer deposition techniques, which was required to produce a "useful device," rather than a "mere laboratory device"). On this record, ATI does not explain adequately why developing and testing those optional features were reasonably necessary for reducing the claimed elements to practice. Nor does ATI explain why the team of engineers and designers could not have designed, built, and tested a chip embodying the claimed elements, without

those optional features. *See Naber*, 567 F.2d at 385 (noting that it is the inventor's burden to reconcile the waiting period with the reasonable diligence requirement).

Mr. Lefebvre testifies that he and his colleagues worked to implement the design for the R400 by updating the R400 Sequencer Specification, and by developing, testing, and debugging the emulation code and RTL code, including other components that supported and interacted with the sequencer. Ex. 2006 ¶¶ 34–43; Exs. 2007, 2009–2018, 2020–2039. Mr. Lefebvre also testifies that the "metadata shows work that was necessary for implementing the R400 design," and "we could not work on or test the sequencer block or the shader pipe block in isolation." Ex. 2006 ¶ 42. Once again, Mr. Lefebvre's testimony is too general and conclusory.

As discussed above, ATI's evidence shows that the R400 project involves other chip designs and optional features that are not recited in the claims at issue. Yet, Mr. Lefebvre does not explain meaningfully and specifically which activities listed in the metadata are directed to the reduction to practice of the claimed elements and which activities are directed to developing and testing other chip designs and optional features. Instead, Mr. Lefebvre relies upon a calendar and metadata (nearly 1,300 pages) for the entire R400 project (Ex. 2006, 31–56; Exs. 2048–52, 2107), without identifying specific facts and dates as to the particular work that was reasonably necessary for reducing the claimed features to practice. *See Gould*, 363 F.2d at 920; *Kendall*, 173 F.2d at 993. Such evidence fails to corroborate Mr. Lefebvre's testimony for establishing that the R400 team

performed reasonably continuous activities to reduce the claimed system to practice for each of the three critical periods during which diligence is required. As a result, Mr. Lefebvre's testimony (Ex. 2006 ¶¶ 34–43) is entitled to little, if any, weight. *See NTP*, 654 F.3d at 1291.

According to ATI, the RTL code for the R400 design was completed by October 31, 2002. PO Resp. 15; Ex. 2071, 7. ATI submitted thirty-one versions of the R400 Sequencer Specification (Exs. 2007, 2009–18, 2020–39), but the last version is dated on May 1, 2003. Ex. 2039, 5; Ex. 2006 ¶ 36. ATI also proffered nineteen versions of the R400 program review slide presentations (Exs. 2053–2071), but the last version is dated on November 12, 2002, which states that the first samples or prototype was scheduled for June 25, 2003 (Ex. 2071, 7). As discussed above, ATI confirms that there was a plan, at the outset, to make a prototype of the R400. Tr. 81:10–16. ATI also acknowledges that "there was actually never a tape out, a sample, or a production for the R400," but ATI did not submit any evidence as to why ATI could not have obtained a prototype of the R400, other than commercially related reasons. Tr. 80:2–11, 82:5–10. However, "efforts to exploit an invention commercially do not constitute diligence in reducing it to practice." *Fitzgerald*, 268 F.2d at 766; *Griffin*, 816 F.2d at 627; *Naber*, 567 F.2d at 385–86.

On this record, ATI does not provide sufficient explanation or credible evidence that is specific both as to facts and dates, regarding what particular work was done during the time period between June 25, 2003, and September 29, 2003, that is directed toward, or reasonably necessary for, the

reduction to practice of the claimed elements. *See Gould*, 363 F.2d at 920; *Kendall*, 173 F.2d at 993. This time period overlaps with all three critical periods by about three months—e.g., from just prior to June 27, 2003, Lindholm's filing date, to September 29, 2003. As such, ATI fails to provide a sufficient account or adequate facts to support a showing of the continuity of activities required for reasonable diligence during each of the three critical periods. *See Rieser*, 255 F.2d at 424; *Fitzgerald*, 68 F.2d at 766 (affirming a determination of lack of reasonable diligence where there was less than 1 month of inactivity during critical period).

In addition, ATI's reliance on *Keizer* is misplaced. *Keizer v. Bradley*, 270 F.2d 396, 398 (CCPA 1959). In *Keizer*, the Court noted that the Board excused the inventor from the usual requirement that the activity must be directed toward the claimed invention because the evidence supported that the work required to develop an operative receiver was necessary for the reduction to practice of the claimed automatic chroma control. *Id.* Such circumstances are not present here. As we discussed above, ATI has not shown that the other chip designs and optional features were required to develop and test the claimed elements.

We also are not persuaded by ATI's argument that the metadata associated with each check-in date describes the work that occurred. Sur-reply 5. Rather, we agree with LG that ATI's metadata, document logs, and folder histories do not show the actual work being done. Reply 12–13; Ex. 1035, 124:22–125:12, 126:3–5 ("the tool only collects the check-ins and not the work that goes in between the check-in"), 127:1–7 ("The perforce

logs we have would not tell you that [work was being done on each of those days in between].”).

As noted above, ATI’s calendar, metadata, document logs, and folder histories (nearly 1,300 pages) do not explain meaningfully the nature of the work that was reasonably necessary for reducing the claimed elements to practice. Ex. 2006, Part V, 33–56; Exs. 2048–52, 2107. ATI confirms that “a detailed description of the work that was done is not included in that log.” Tr. 75:17–20.

Notably, ATI’s metadata merely provide shorthand notations, vague statements, and generic descriptions of the tasks performed by the designers and engineers. Exs. 2048–52, 2107. For example, the R400 Shader Pipe Parts Folder History is reproduced below (Ex. 2107):

```
                    filelog-depot-r400-devel-parts_lib-src-sp.txt
Change 11107 on 2001/12/03 by pmitchel@pmitchel_r400_win_marlboro
        mv block dirs to gfx
Change 10478 on 2001/11/21 by askende@andi_r400
        further update of the I/O definition
Change 9918 on 2001/11/14 by askende@andi_r400
        first time check-in
Change 8480 on 2001/10/25 by askende@andi_r400
        inserted into source control by Andi S.
Change 6887 on 2001/09/25 by askende@andi_r400_devel
        more changes
Change 6810 on 2001/09/21 by askende@andi_r400_devel
        newly added files
Change 5440 on 2001/08/16 by askende@andi_r400_devel
        adding source code into source control
Change 5002 on 2001/08/02 by pmitchel@pmitchel_test_client
        directory creation
```

Vague and general entries, such as “more changes” and “newly added files,” are insufficient to indicate what work was done or how it was intended to

further the reduction of the apparatus recited in the challenged claims to practice. Consequently, such entries are insufficient to show reasonable diligence.

As another example, many of the entries in the R400 Document Library Folder History state generically: "deletion" (see, e.g., 2003/09/11 entry), "updates" (see, e.g., 2003/08/29, 2003/08/21, 2003/08/11 entries), "no change" (see, e.g., 2003/08/18 entry), and "[a]dded info" (see, e.g., 2003/08/15 entry). Ex. 2050. Given that the descriptions are general and vague, it is unclear to us what was updated or changed, and how the tasks are directed toward, or reasonably necessary for, the reduction to practice of the claimed invention.

ATI and Mr. Lefebvre also do not provide any meaningful explanation as to how the tasks listed in the metadata specifically relate to the particular work that was reasonably necessary for the reduction to practice of the claimed invention. ATI cannot reasonably expect us to search nearly 1,300 pages for evidence to support ATI's position, without some guidance from ATI as to what these document logs and folder histories show and how they show reasonable diligence in each critical period. *See DeSilva v. DiLeonardi*, 181 F.3d 865, 866-67 (Fed. Cir. 1999) ("A brief must make all arguments accessible to the judges, rather than ask them to play archeologist with the record.").

We do not find ATI's explanation that "since the code kept in the database is the master copy, checking in updated code would itself constitute changes to the master copy" meaningful. Sur-reply 5. Even if we reviewed

ATI's calendar and each of the six document files for each day over a time period of almost two years, ATI did not provide the updated code for each check-in date, and, as a result, it would be impossible for us, based on this record, to determine the changes made to the master copy or the actual work that occurred for each day. ATI fails to provide a reasonable way for us to determine whether unexplained lapses have not occurred. *See Mulder*, 716 F.2d at 1542–46 (affirming a determination of lack of reasonable diligence, where the evidence of record was lacking for a two-day critical period).

For the foregoing reasons, we determine that ATI fails to demonstrate by a preponderance of the evidence that there was a continuous exercise of reasonable diligence to reduce the claimed invention to practice, during each of the three critical periods. Therefore, Moreton, Lindholm, and Stuttard are prior art under § 102(e) against the claims of the '053 patent in this proceeding.

C. Principles of Law

To establish anticipation, each and every element in a claim, arranged as recited in the claim, must be found in a single prior art reference. *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008). It is well settled that "the reference need not satisfy an *ipsissimis verbis* test." *In re Gleave*, 560 F.3d 1331, 1334 (Fed. Cir. 2009); *In re Bond*, 910 F.2d 831, 832–33 (Fed. Cir. 1990). In an anticipation analysis, "it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw

therefrom." *In re Preda*, 401 F.2d 825, 826 (CCPA 1968); *In re Graves*, 69 F.3d 1147, 1152 (Fed. Cir. 1995) ("A reference anticipates a claim if it discloses the claimed invention such that a skilled artisan could take its teachings in combination with his own knowledge of the particular art and be in possession of the invention."). Prior art references must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (quoting *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) objective evidence of nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

D. The Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art at the time of the invention, we note that various factors may be considered, including "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology;

and educational level of active workers in the field." *In re GPAC, Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citing *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986)).

Although the parties' declarants provide two different definitions of a person with ordinary skill in the art, the parties do not challenge each other's definition; nor do they point out any material differences. Ex. 1003 ¶ 38; Ex. 2151 ¶ 29; PO Resp.; Reply. Further, it is well-settled that the level of ordinary skill in the art may be reflected by the prior art of record, as here. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc*., 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). One of ordinary skill is presumed to be aware of all pertinent prior art. *Standard Oil Co. v. American Cyanamid Co.*, 774 F.2d 448, 454 (Fed. Cir. 1985). Because there is no material dispute as to the level of ordinary skill in the art and because the level of skill is reflected by the prior art of record, we need not explicitly define the level of ordinary skill.

E. Dr. Bagherzadeh's Declaration

ATI argues that Dr. Bagherzadeh's Declaration (Ex. 1003) should be accorded little or no weight because the Declaration allegedly includes numerous conclusory statements without corroborating evidence. PO Resp. 59. ATI also contends that Dr. Bagherzadeh lacks meaningful experience in computer graphics, and did not consider any objective indicia of nonobviousness. *Id.* at 59–60. LG counters that Dr. Bagherzadeh's opinions

on the patentability of the challenged claims are supported adequately with detailed reasoning, citations to the art, and a view of the technology based on his experience. Reply 24–25.

We determine that ATI has not articulated a persuasive reason for giving Dr. Bagherzadeh's Declaration (Ex. 1003), as a whole, little or no weight. We have reviewed Dr. Bagherzadeh's testimony, curriculum vitae, and cross-examination testimony. Exs. 1003, 1009, 2146. Dr. Bagherzadeh testifies that he is a Professor in the Department of Electrical Engineering and Computer Science at the University of California at Irvine. Ex. 1003 ¶ 3. Dr. Bagherzadeh also was a member of the technical staff at AT&T Bell Laboratories, and the Chair of the Electrical/Computer Engineering and Electrical Engineering/Computer Science Department, as well as an IEEE Fellow. *Id.* ¶¶ 5–6. Dr. Bagherzadeh also published at least 94 articles and five book chapters, many of which relate to computer graphics. Ex. 1009.

There is no material dispute as to the level of ordinary skill in the art. ATI's expert, Dr. Wolfe, testifies that one of ordinary skill in the art would have had at least a bachelor's degree in electrical or computer engineering or computer science plus five years of experience in the computer graphics hardware industry, or a master's degree in electrical or computer engineering or computer science plus two years of experience in that industry, or an equivalent combination of education and experience. Ex. 2151 ¶ 29. Certainly, Dr. Bagherzadeh's qualification meets or exceeds that definition.

Given that, we determine that Dr. Bagherzadeh's qualification and experience are sufficient to qualify him as an expert in the pertinent field

under Federal Rule of Evidence ("FED. R. EVID.") 702. *See, e.g.*, Ex. 1003 ¶¶ 3–8; Ex. 1009. In addition, there is no requirement of a perfect match between the expert's experience and the relevant field. *SEB S.A. v. Montgomery Ward & Co.*, 594 F.3d 1360, 1373 (Fed. Cir. 2010).

We also are not persuaded by ATI's argument that Dr. Bagherzadeh "failed to consider any objective indicia of nonobviousness." PO Resp. 60. ATI's reliance on *Rambus Inc. v. Rea*, 731 F.3d 1248, 1257 (Fed. Cir. 2013) is misplaced, because it does not support ATI's proposition that an expert declarant must consider evidence of secondary considerations *before* the patentee presents such evidence (*id.*). At the time when LG submitted Dr. Bagherzadeh's Declaration in support of its Petition, ATI did not advance any contention as to secondary considerations of nonobviousness. ATI cannot reasonably require Dr. Bagherzadeh to consider such evidence before ATI presents it properly in the proceeding.

For the reasons stated above, we decline to accord Dr. Bagherzadeh's Declaration, as a whole, little or no weight, as urged by ATI. Rather, we exercise our discretion to determine the appropriate weight to be accorded to the evidence presented, including expert opinion, based on the disclosure of the underlying facts or data upon which that opinion is based.

F. Anticipation Ground based on Moreton

LG asserts that claims 5–7 are unpatentable under § 102(e) as anticipated by Moreton. Pet. 48–51. To support its assertion, LG explains how Moreton describes each claim limitation. *Id.* LG also relies upon

Dr. Bagherzadeh's Declaration for support. Ex. 1003. ATI responds that Moreton does not describe certain limitations, and cites to Dr. Wolfe's Declaration for support. PO Resp. 30–34; Ex. 2151. We begin below with a brief summary of Moreton, and then address the parties' contentions in turn.

Moreton

Moreton discloses a multithreaded graphics processing system. Ex. 1006, Abs. Figure 1 of Moreton, reproduced below.

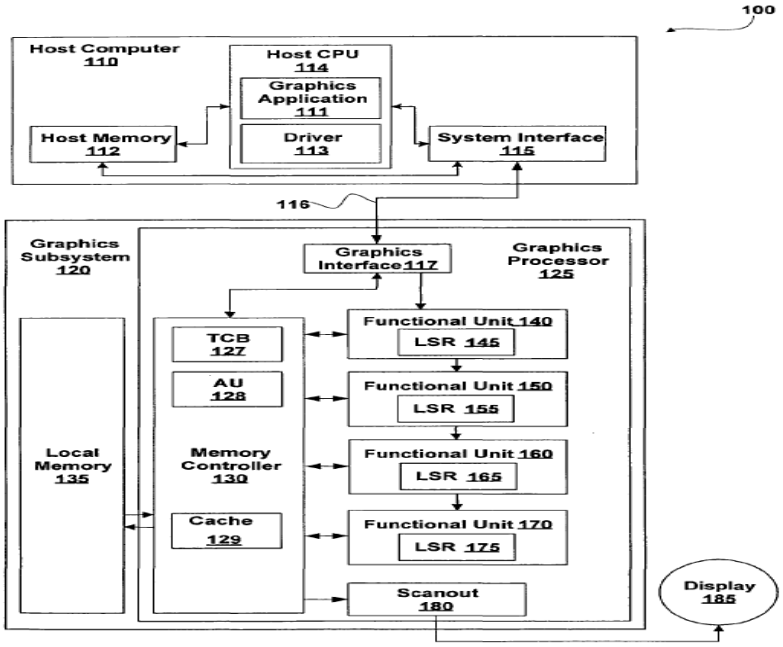


FIG. 1

As shown in Figure 1 of Moreton, graphics subsystem 120 includes graphic processor 125 and local memory 135. *Id.* at 3:56–66. Graphic processor 125 contains functional units 140–170, and memory controller 130, which includes thread control buffer 127, address unit 128, and cache unit 129. *Id.*

Memory device

Claim 5 recites "at least one memory device comprising a first portion operative to store a plurality of pixel command threads and a second portion operative to store a plurality of vertex command threads." Ex. 1001, 8:5–8. LG asserts that Moreton describes the claimed memory device. Pet. 42–44, 48–50. According to LG, Moreton's memory resource includes a first memory section for storing threads of a first thread type, and a second memory section for storing threads of a second thread type. *Id.* (citing Ex. 1006, Abs., 1:43–58, 6:21–37, 8:60–61, 15:48–67, 16:25–26). ATI does not dispute LG's contentions regarding the aforementioned "memory device" claim limitation. PO Resp. 29–34.

Having considered the Petition and Moreton, we agree with LG. Indeed, Moreton describes a graphics multithreaded processing system for processing pixel command threads and vertex command threads. Ex. 1006, Abs. More importantly, Moreton discloses a memory resource that contains at least two portions of a memory device, each storing a different thread type. *Id.* at 15:48–64.

Figure 5 of Moreton is reproduced below.

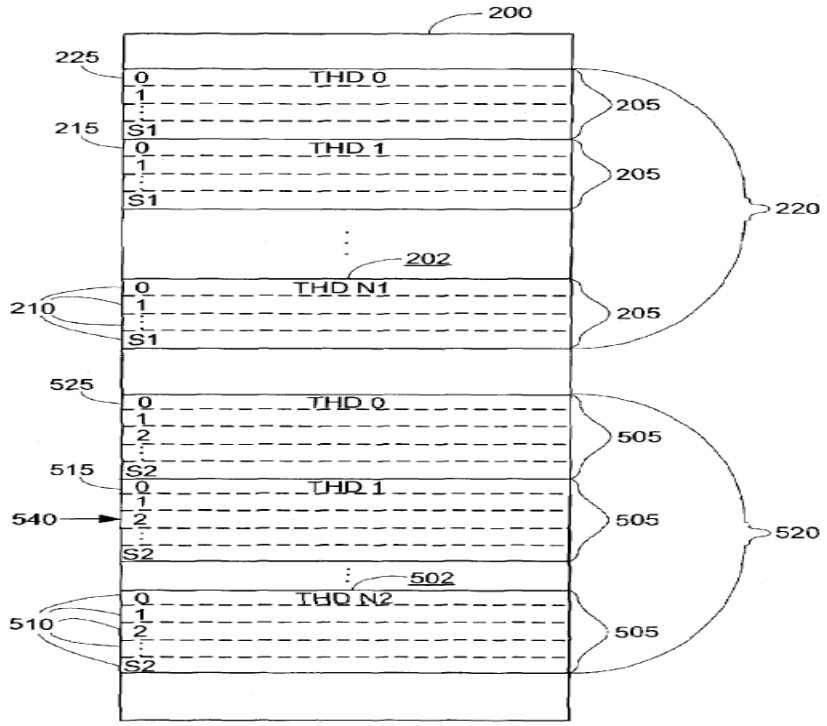


FIG. 5

As shown in Figure 5 of Moreton, memory resource 200 contains first memory section 220, and second memory section 520, each having at least two memory spaces 205, 505 for use by threads executing on graphics processor 125 (shown in Figure 1, reproduced previously). *Id.* First memory section 220 stores a first thread type, and second memory section 520 stores a second thread type. *Id.* The second thread type is different from the first thread type. *Id.*

Based on Moreton's disclosure, we find that Moreton describes a "memory device comprising a first portion operative to store a plurality of pixel command threads and a second portion operative to store a plurality of vertex command threads," as recited in claim 5.

Arbiter

Claim 5 recites "an *arbiter* . . . operable to select *a command thread* from either of the plurality of pixel command threads and the plurality of vertex command threads." Ex. 1001, 8:9–12 (emphases added). As discussed above, we construe the claim term "arbiter" as any computer hardware, software, or combination thereof that receives and provides a command thread. We also construe "a command thread" to include a stream of *instructions* or a process that is part of a larger process or program.

In this regard, LG asserts that Moreton's memory controller, which includes a thread control buffer, corresponds to the claimed arbiter. Pet. 48–49. LG notes that Moreton's thread control buffer selects and assigns a thread to the functional units for executing the thread. *Id.* at 44–46. ATI disagrees, arguing that Moreton's thread does not include instructions to process the pixel or vertex data at the time of thread assignment. PO Resp. 30. ATI also alleges that Moreton's arbitration is related to memory access and not to selection of a command thread. *Id.* at 31.

We are not persuaded by ATI's arguments and expert testimony (PO Resp. 30–31; Ex. 2151 ¶¶ 120–22), as they rest primarily on an incorrect assumption that Moreton's threads are not command threads, requiring a command thread to include *all* of the instructions for processing the pixel or vertex data at the time of thread assignment. Rather, upon review of Moreton in its entirety, we agree with LG that Moreton describes the claimed arbiter.

Similar to the ’053 patent, Moreton discloses a multithreaded graphics processing system for processing vertex and pixel threads. Ex. 1006, Abs. Moreton’s system reserves, assesses, and manages memory spaces for use by threads executing on a graphics processor. *Id.* at 1:7–10. According to Moreton, graphics data is processed on a graphics processor through the use of threads executing on the graphics processor. *Id.* at 1:14–16. Moreton also discloses a method for allocation of a memory resource for a plurality of threads of at least two thread types simultaneously executable in a graphics processor responsive to a graphics program module, including determining a first set of threads from the plurality of threads. *Id.* at 1:48–54.

Significantly, Moreton states that “a thread is a set of processes for processing a sample according to an instruction set associated with the sample.” *Id.* at 6:7–9. A sample refers to “primitive data, surface data, pixel data, vertex data, fragment data, or the like.” *Id.* at 5:24–25. Upon consideration of Moreton as a whole, we determine that Moreton’s threads are command threads that include instructions to process pixel or vertex sample data, contrary to ATI’s argument (PO Resp. 30).

ATI’s arguments and expert testimony also conflate Moreton’s threads with the “instruction sets” associated with the sample. *See* PO Resp. 30–31; Ex. 2151 ¶¶ 120–22; Ex. 1006, 1:48–58, 6:7–9, 4:34–47. Moreton discloses that “[a]n instruction set is a specific subset of program instructions of Graphics Application 111 (executing on Host CPU 114) used to process an associated sample.” *Id.* at 12:12–14; *see also id.* at 5:44–46. ATI’s arguments also fail to appreciate that there are various instructions in

a graphics processing system for processing pixel and vertex data. Nothing in the claims requires a command thread to contain *all* of the instructions necessary to process the pixel or vertex data at the time of assignment.

We agree with LG and find that Moreton's memory controller, which includes a thread control buffer, selects and assigns a thread to a plurality of functional units for executing the thread. Pet. 44–49; Ex. 1006, 4:4–20, 5:61–66, 7:39–42. Moreton discloses that, when a functional unit receives a sample, which includes pixel or vertex data, a sample type identifier associated with the sample, and a pointer to an instruction set associated with the sample, a thread is assigned to the sample by the thread control buffer. *Id.* at 5:61–66. The functional units are programmable units capable of executing threads in parallel, and performing vertex and pixel operations. *Id*. at 5:4–19, 5:65–66.

In light of the foregoing, we determine that LG has demonstrated sufficiently that Moreton describes an arbiter "operable to select a command thread from either of the plurality of pixel command threads and the plurality of vertex command threads," as recited by claim 5.

<u>A plurality of command processing engines</u>

Claim 5 recites "a plurality of command processing engines, coupled to the arbiter, each operable to receive and process the command thread." Ex. 1006, 8:13–15. In this regard, LG takes the position that Moreton's functional units that are connected to a memory controller correspond to the claimed "command processing engines." Pet. 49 (citing Ex. 1006, 5:20–23). ATI responds that Moreton does not disclose a single functional unit that is

capable of processing both *pixel and vertex* commands. PO Resp. 31–34. ATI alleges that Moreton's functional units are type-specific processing engines, and, therefore, each functional unit cannot process both types of data. *Id.* (citing Ex. 1006, 5:10–19, 5:33–40; Ex. 2151 ¶ 127).

ATI's arguments, however, rest on its proposed claim construction of the "command processing engine" limitation recited in claim 5, excluding *type-specific* processing engines and requiring *each* command processing engine to be able to process *all* of the command threads selected by the arbiter. PO Resp. 31–34. As discussed above, we decline to adopt ATI's proposed claim construction. Rather, we construe the "command processing engine" limitation as recited in claim 5, in a manner consistent with the plain meaning of the claim language, as requiring each command processing engine to be coupled to an arbiter and operable to receive and process a command thread selected by the arbiter.

As ATI acknowledges, Moreton discloses multiple functional units that process pixel and vertex data. PO Resp. 33. Indeed, Moreton describes a multithreaded graphics processing system that includes a plurality of functional units (command processing engines), each coupled to a memory controller that includes a thread control buffer (an arbiter) and operable to receive and process a thread selected by the thread control buffer. Ex. 1006, 5:10–48, 6:15–20. In light of the foregoing, we determine that LG has established sufficiently that Moreton describes "a plurality of command processing engines," as recited in claim 5.

Conclusion on Anticipation

ATI has not raised any additional arguments as to dependent claims 6 and 7 other than those addressed above. Upon review of LG's analysis and supporting evidence, we agree with LG's showing—and adopt it as our own—that Moreton describes the claimed features recited in claims 6 and 7. *See, e.g.*, Pet. 37–51; Ex. 1006, 5:10–48, 6:15–20; Ex. 1003 ¶¶ 176–78. For example, Moreton discloses a functional unit that is "a programmable vertex processor capable of performing pre-vertex computations (such as lighting and time-varying spatial offsets), subdivision surface algorithms (as known in the art), and N-patch algorithms (or 'normal patch', as known in the art)." Ex. 1006, 5:10–15. Moreton also discloses a functional unit that is "a programmable shader processor capable of performing per-pixel operations, such as texturing, lighting, bump mapping, or the like." *Id.* at 5:15–19. As Dr. Bagherzadeh testifies, Moreton's functional units include an arithmetic logic unit and a texture processing engine. Ex. 1003 ¶¶ 176–78.

For the foregoing reasons, we conclude that LG has shown by a preponderance of the evidence that claims 5–7 are anticipated by Moreton.

G. Obviousness Ground Based on Moreton and Whittaker

LG asserts that claims 1 and 2 are unpatentable under § 103(a) as obvious over Moreton and Whittaker. Pet. 37–48. In support of its assertion, LG provides detailed explanations as to how the combination of Moreton and Whittaker teaches or suggests each claim limitation and directs our attention to Dr. Bagherzadeh's Declaration (Ex. 1003). *Id.*

ATI counters that Moreton's thread assignment does not disclose selecting a command thread as required by claims 1 and 2. PO Resp. 34; Ex. 2151 ¶ 135. Essentially, ATI relies upon the same arguments presented in connection with independent claim 5. We have addressed those arguments in our anticipation analysis above, and conclude that those arguments are likewise unavailing here.

ATI also argues that Moreton does not disclose an arbiter that provides a command thread to the command processing engine, as required by claim 2. PO Resp. 36. ATI further contends that LG fails to provide a sufficient reason to combine Moreton and Whittaker. *Id.* at 34–36. As support, ATI cites to Dr. Wolfe's Declaration. Ex. 2151.

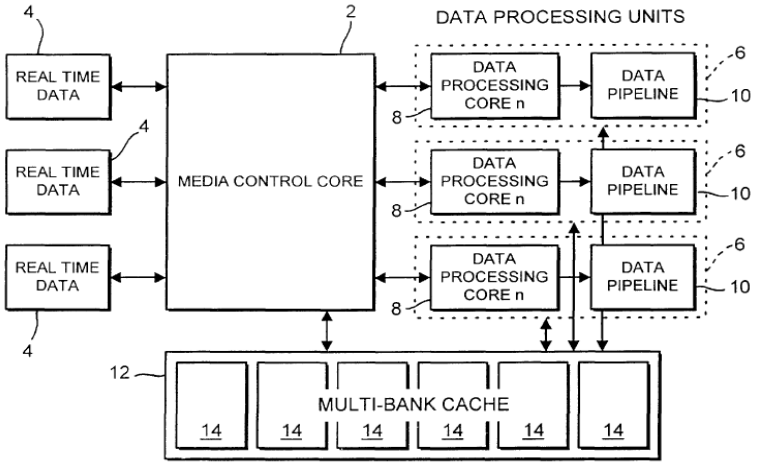
In our discussion below, we address the parties' contentions, after providing a brief summary of Whittaker.[5]

Whittaker

Whittaker discloses a multithreaded system that includes a media control core and data processing units for controlling the execution of instructions. Ex. 1007, 3:36–50. Figure 1 of Whittaker is reproduced below.

[5] A summary of Moreton has been provided previously in our anticipation analysis.

FIG. 1



As shown in Figure 1 of Whittaker, each data processing unit 6 includes data processing core 8 that decodes and sequences instructions for pipeline 10. *Id.* at 3:46–49. Media control core 2 is a multithreading processing unit that directs data from inputs to data processing core 8 or to storage and provides data to outputs. *Id.* at 3:56–58. Media control core 2 checks "which of the possible operations it could perform have all the resources available for those tasks to be executed and, of those, which has the highest priority." *Id.* at 3:60–65.

<u>Arbiter</u>

Claim 1 recites "an arbiter . . . operable to select a command thread . . . based on relative priorities of the plurality of pixel command threads and the plurality of vertex command threads." Ex. 1001, 7:16–20. Claim 2 recites "wherein the arbiter is further operable to provide the command thread to the command processing engine." *Id.* at 7:24–26.

LG asserts that Moreton's memory controller, which includes a thread control buffer, corresponds to the claimed arbiter, and that Moreton's functional units correspond to the claimed command processing engines. Pet. 38. As support, LG states that Moreton's thread control buffer "assigns threads to data samples and allows instructions and data to be provided to the plurality of functional units." *Id.* at 38–39 (citing Ex. 1006, 5:61–6:2, 12:19–36). LG also notes that Moreton's memory controller "arbitrates between hardware components of Graphics Subsystem 120 initiating access commands to memory resources containing memory spaces used by threads executing on Graphics Processor 125." *Id.* at 39 (citing Ex. 1006, 7:39–42).

Notwithstanding that Moreton does not disclose explicitly selecting a thread "based on relative priorities" of the threads, LG maintains that the combination of Moreton and Whittaker would have rendered the claimed subject matter, as a whole, obvious, as priority selection of threads was known in the art, as evidenced by Whittaker. Pet. 40–42. LG asserts that Whittaker discloses a graphics system in which a thread is selected for processing based on relative priorities of the threads. *Id.* (citing Ex. 1007, 3:60–67, 8:17–31). LG also submits that it would have been obvious to modify Moreton's system to include a priority selection function, in light of Whittaker, for achieving more efficient data movement and prioritizing processing of data that requires immediate output, as well as improving system performance. *Id.* at 41 (citing Ex. 1007, 3:5–8, 8:29–34).

ATI argues that Moreton does not describe an arbiter that *provides* a command thread to a command processing engine, as required by claim 2,

because Moreton's thread, instead of the memory controller, loads the instructions to the functional unit. PO Resp. 36. According to ATI, before the thread control buffer assigns a thread, a functional unit has received already the pointer to the instruction set. *Id.*

Once again, ATI's arguments and expert testimony rest primarily on an incorrect assumption that Moreton's thread is not a command thread, requiring a command thread to include *all* of the instructions for processing the pixel or vertex data at the time of thread assignment. PO Resp. 36; Ex. 2151 ¶¶ 144–45. They also conflate Moreton's threads with the "instruction sets" associated with the sample. As discussed above in our anticipation analysis, we find these arguments unavailing. Rather, upon review of Moreton as a whole, we find that Moreton's threads are command threads that include instructions to process pixel or vertex data. Ex. 1006, Abs., 1:7–10, 1:14–16, 1:48–54, 5:24–25, 6:7–9. Nothing in the claims requires a command thread to contain *all* of the instructions necessary to process the pixel or vertex data at the time of thread assignment.

Figure 1 of Moreton is reproduced below, with our annotation in green.

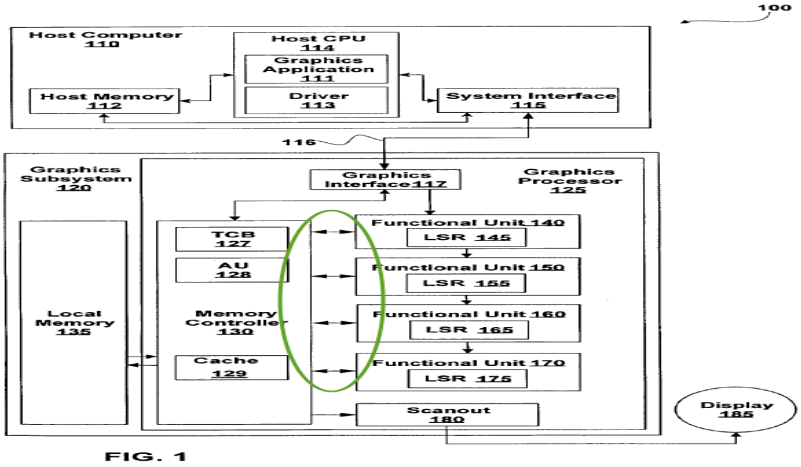


FIG. 1

As shown in Figure 1 of Moreton, memory controller 130, which includes thread control buffer 127 and address unit ("AU") 128, provides command threads, data associated with the command threads, and pointers or addresses to functional units 140–170. Ex. 1006, 5:31–64. More importantly, Moreton describes that, when functional units receive a sample, sample type identifier, and pointer to an instruction set associated with the sample, a thread is assigned to the sample by thread controller buffer 127. *Id.* Reading Moreton as a whole, we find that Moreton's memory controller *provides* the threads to the functional units. *Id.* We agree with LG that Moreton's memory controller (arbiter), as modified by Whittaker, is operable to select and provide a pixel or vertex command thread to a functional unit (command processing engine), as required by claim 2.

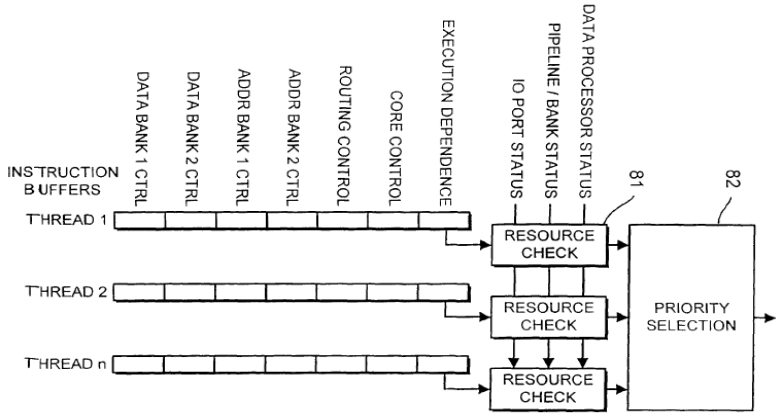
Rationale to combine

ATI asserts that a person of ordinary skill in the art would not have found it obvious to modify Moreton in view of Whittaker. PO Resp. 34–36. ATI advances several arguments. *Id.*

First, ATI alleges that Whittaker's prioritization scheme does not involve any pixel or vertex command threads. *Id*. at 35; Ex. 2151 ¶ 136. Attacking Whittaker individually, however, does not undermine LG's showing of obviousness that is based on the combination of Moreton and Whittaker. *See In re Keller*, 642 F.2d 413, 426 (CCPA 1981) (non-obviousness cannot be established by attacking references individually where the ground of unpatentability is based upon the teachings of a combination of references). The test for obviousness is whether the combination of references, taken as a whole, would have suggested the patentees' invention to a person having ordinary skill in the art. *In re Merck & Co., Inc.*, 800 F.2d 1091, 1097 (Fed. Cir. 1986).

As discussed above, LG relies on Moreton to disclose an arbiter that selects a command thread from a plurality of pixel and vertex command threads. Pet. 37–40. LG relies on Whittaker to disclose the priority selection scheme. *Id.* at 40–42. Indeed, Whittaker discloses a media control core that checks "which of the possible operations it could perform have all the resources available for those tasks to be executed and, of those, which *has the highest priority*." Ex. 1007, 3:60–65 (emphasis added).

Figure 6 of Whittaker is reproduced below.



As shown in Figure 6 of Whittaker, instruction buffers store a plurality of threads. *Id.* at 8:18–23. Each thread is sent to resource checker 81, ensuring that the resources required to execute the thread are in place. *Id.* at 3:66–67, 8:24–27. If the resources are available, the thread is sent to priority selection 82 that selects for execution the thread with the highest priority. *Id.* at 8:27–31. In view of these disclosures, we are persuaded that selecting a thread for processing based on relative priorities of the threads was known in the art at the time of the invention.

We also observe that LG's articulated rationale for combining Moreton and Whittaker is supported by Dr. Bagherzadeh's testimony. Pet. 41–42 (citing Ex. 1003 ¶¶ 163–166). Specifically, Dr. Bagherzadeh testifies that it would have been obvious to a person with ordinary skill in the art to implement the priority selection function in Moreton's system, in light of Whittaker, for achieving more efficient data movement, as well as prioritizing processing of data and improving the performance of the processing units through load balancing. Ex. 1003 ¶¶ 163–167. On this

record, we credit Dr. Bagherzadeh's testimony, as it is consistent with the prior art disclosures. *See* Ex. 1007, 3:5–8, 8:29–34. Therefore, we are persuaded by LG's arguments that one of ordinary skill in the art would have modified Moreton's graphics memory controller to select a command thread between a plurality of pixel command threads and a plurality of vertex command threads based on relative priorities of the threads, in light of Whittaker, to improve the efficiency and performance of the graphics processor. *See KSR*, 550 U.S. at 417 ("[I]f a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.").

Second, ATI argues that "Whittaker was non-analogous art to Moreton's technology since Whittaker is not relevant to a graphics processor." PO Resp. 35. ATI, however, does not explain why Whittaker's thread priority selection disclosure is not reasonably pertinent to the problem the named inventors of the '053 patent attempt to solve—namely, selecting a thread for processing based on relative priorities of the threads. *See In re Clay*, 966 F.2d 656, 658–59 (Fed. Cir. 1992) (noting that a reference is considered to be analogous if it is reasonably pertinent to the particular problem with which the inventor is concerned, regardless of the field of endeavor). Rather, ATI merely relies upon an attorney's argument in another proceeding. PO Resp. 35 (citing *Samsung Electronics Co., Ltd. v. NVidia Corp.*, IPR2015-01198, slip op. at 44, 48 (PTAB Sept. 4, 2015) (Paper 7)). We are not persuaded by ATI's argument here, as arguments of

counsel cannot take the place of evidence lacking in this record. *See Estee Lauder Inc. v. L'Oreal, S.A.*, 129 F.3d 588, 595 (Fed. Cir. 1997).

Finally, ATI contends that incorporating Whittaker's priority selection scheme into Morton would destroy Moreton's principle of operation. PO Resp. 35. ATI's argument and expert testimony assume that Moreton's principle of operation is matching thread type to the same sample type. *Id.* at 35–36; Ex. 2151 ¶¶ 137–40. That characterization is overly narrow. As LG notes, ATI's argument and expert testimony ignore Moreton's disclosure of a plurality of functional units that can process different types of command threads. Reply 16; Ex. 1006, 5:31–37. Whittaker determines priority by taking account of the available resources capable of processing the command thread. Ex. 1007, 3:60–65. For example, when using Whittaker's priority scheme, Moreton's memory controller would determine whether there is a functional unit available that is capable of processing a vertex command and, if such a functional unit is not available, the system would not give that vertex command the highest priority. *Id.* In light of Whittaker, it would have been obvious to a person of ordinary skill in the art to prioritize different types of command threads disclosed by Moreton. As LG's expert testifies, implementing Whittaker's priority scheme in Moreton's multi-thread graphics processing system would improve the efficiency of processing the different types of command threads, and the performance of the functional units through load balancing. Ex. 1003 ¶¶ 163–167. Based on the evidence before us, we are not persuaded that implementing a priority selection scheme in Morton's system would destroy

Moreton's principle of operation for processing different types of command threads using a plurality of functional units. *See In re Umberger*, 407 F.2d 425, 430–31 (CCPA 1969) (finding the principle set forth in *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959), inapplicable where the modified apparatus will operate "on the same principles as before").

Having considered the evidence in this record, we determine that LG has articulated reasoning with rational underpinnings why one with ordinary skill in the art would have modified Moreton in view of Whittaker, in a manner to arrive at the subject matter of claims 1 and 2.

Secondary considerations of nonobviousness

Factual inquiries for an obviousness determination include secondary considerations based on evaluation and crediting of objective evidence of nonobviousness. *Graham*, 383 U.S. at 17. Notwithstanding what the teachings of the prior art would have suggested to one with ordinary skill in the art at the time of the invention, the totality of the evidence submitted, including objective evidence of nonobviousness, may lead to a conclusion that the claimed invention would not have been obvious to one with ordinary skill in the art. *In re Piasecki*, 745 F.2d 1468, 1471–1472 (Fed. Cir. 1984). But, "secondary considerations of nonobviousness . . . simply cannot overcome a strong prima facie case of obviousness . . . where the inventions represented no more than 'predictable use of prior art elements according to their established functions,' the secondary considerations are inadequate to establish nonobviousness as a matter of law." *Wyers v. Master Lock Co.*, 616 F.3d 1231, 1246 (Fed. Cir. 2010) (quoting *KSR*, 550 U.S. at 417).

Here, ATI proffers evidence that purportedly establishes industry acceptance, arguing that ATI's *unified shader* has been adopted widely in the industry. PO Resp. 60. ATI also contends that companies implementing a unified shader are able to remain competitive in the marketplace. *Id.* (citing Ex. 2142, 14; Ex. 2148, 9, 21; Ex. 2149, 12; Ex. 2150, 5). As support Dr. Wolfe testifies that Microsoft's Direct X (DX10) has adopted the unified shader model. Ex. 2151 ¶¶ 222–223. Dr. Wolfe explains that a "unified shader" is a single shader that can perform both vertex and pixel calculations. *Id*. at ¶ 65.

LG counters that ATI's evidence rests on the premise that the industry has embraced the use of a "unified shader" in graphics processors. Reply 25. LG points out that none of the claims in the '053 patent use the term "unified shader," nor does this term appear in the Specification. *Id.* Upon review of ATI's evidence, the claims at issue, and the Specification of the '053 patent, we agree with LG.

To be of relevance, evidence of nonobviousness must be commensurate in scope with the claimed subject matter. *In re Tiffin*, 448 F.2d 791, 792 (CCPA 1971) (evidence of success for cups is not commensurate in scope with containers). In order to be accorded substantial weight, there must be a nexus between the merits of the claimed invention and the evidence of secondary considerations. *GPAC*, 57 F.3d at 1580. "Nexus" is a legally and factually sufficient connection between the objective evidence and the claimed invention, such that the objective evidence should be considered in determining nonobviousness. *Demaco*

Corp. v. F. Von Langsdorff Licensing Ltd., 851 F.2d 1387, 1392 (Fed. Cir. 1988). The burden of showing that there is a nexus lies with the patent owner. *Id.*

We are not persuaded by ATI's argument and evidence, as they fail to establish a nexus between the merits of the claimed invention and the alleged industry acceptance. As noted by LG, none of the claims at issue recites a "unified shader." Ex. 1001, 7:11–9:28. Neither ATI nor Dr. Wolfe points out which claim limitation requires a "unified shader." PO Resp. 60; Ex. 2151 ¶¶ 220–223. In fact, the Specification of the '053 patent discloses that the "command processing engine may be *any suitable engine as recognized by one having ordinary skill in the art* for processing commands, such as a texture engine, an arithmetic logic unit, or any other suitable processing engine." Ex. 1001, 2:59–62 (emphasis added).

Moreover, although Dr. Wolfe testifies that Microsoft's DirectX (DX10) has adopted the unified shader model, Dr. Wolfe does not explain sufficiently that Microsoft or other companies in the industry would have accepted the first design of the R400, which allegedly embodies the claimed system, without other unclaimed features. Ex. 2151 ¶¶ 222–223. In fact, Mr. Lefebvre, one of the named inventors, testifies that Microsoft *rejected* the first design of the R400. Ex. 2006 ¶¶ 15, 30 ("Again, the reason for the change was to meet the requirement of Microsoft's API, called DX10. In particular, Microsoft wanted the sequencer to be able to run shaders with an unlimited number of clauses/instructions."); PO Resp. 12; Ex. 2060, 5 ("Microsoft rejecting proposed model – Asking for more general purpose –

longer-living model"). The R400 was redesigned to include features that are not recited in the claims—e.g., a sequencer that could process *an unlimited number of clauses*—in order to meet Microsoft's acceptance. Ex. 2006 ¶¶ 15, 30.

More importantly, the feature—a "unified shader"—that is allegedly adopted by the industry stems from what was known in the prior art. *See, e.g.*, Ex. 1005; Ex. 3003. Contrary to ATI's argument and expert testimony, the named inventors of the '053 patent were not the first in the art to disclose a single graphics processing unit to perform both vertex and pixel operations. As ATI acknowledges, such a feature was known in the art. PO Resp. 53; Ex. 2151 ¶ 199 ("Stuttard's system processes vertex operations (i.e., geometry) and the so-called pixel operations (i.e., rasterization) . . . across all processing blocks of the whole system."). Indeed, both Stuttard and the '182 international publication, which was published on October 19, 2000, more than one year prior to the '053 patent's effective filing date, disclose a plurality of processor blocks, each capable of processing both vertex and pixel operations. Ex. 1005, 8:34–10:47, Fig. 3; Ex. 3003, 17:26–22:32, Fig. 3.

Where the offered secondary consideration actually results from something other than what is both claimed and novel in the claim, as here, there is no nexus to the merits of the claimed invention. *Cf. Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1369 (Fed. Cir. 2011) ("If commercial success is due to an element in the prior art, no nexus exists."); *see also Ormco Corp. v. Align Tech., Inc.*, 463 F.3d 1299, 1312, 1313 (Fed. Cir.

2006) ("[I]f the feature that creates the commercial success was known in the prior art, the success is not pertinent.") (reasoning that success that is due "'partially' to claimed features" and to unclaimed features and/or other features already in the art lacks the requisite nexus to show unobviousness) (citations omitted). In the absence of an established nexus with the claimed invention, secondary consideration factors are given little weight and generally have no bearing on the legal issue of obviousness. *See In re Vamco Machine & Tool, Inc.*, 752 F.2d 1564, 1577 (Fed. Cir. 1985). Accordingly, ATI's objective evidence is accorded little weight. Based on the evidence as a whole, we determine that ATI's evidence does not establish that the claimed system of the '053 patent gained industry acceptance.

We have weighed objective evidence proffered by ATI that allegedly demonstrates nonobviousness against the evidence of obviousness in the present record. For the foregoing reasons, we conclude that, on balance, the strong evidence of obviousness outweighs the weak evidence of nonobviousness. *See Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (holding that the objective considerations of nonobviousness presented, including substantial evidence of commercial success, praise, and long-felt need, were inadequate to overcome a strong showing of primary considerations that rendered the claims at issue invalid).

Conclusion on obviousness based on Moreton and Whittaker

For the foregoing reasons, we conclude that LG has demonstrated by a preponderance of the evidence that claims 1 and 2 are unpatentable over the combination of Moreton and Whittaker.

H. Obviousness Grounds Based on Lindholm and the Admitted Prior Art

LG asserts that claims 1, 2, and 5–7 are unpatentable under § 103(a) as obvious over Lindholm and the Admitted Prior Art. Pet. 22–24. As support, LG provides detailed explanations as to how the combination of Lindholm and the Admitted Prior Art meets each claim limitation. *Id.* LG also relies upon Dr. Bagherzadeh's Declaration. Ex. 1003.

ATI counters that LG fails to show Figure 1 and the discussion in the Background of the Invention Section of the '053 patent are admitted prior art. PO Resp. 38–39. ATI also argues that the combination of Lindholm and the Admitted Prior Art does not disclose certain limitations, and LG fails to provide a sufficient reason to combine the teachings of Lindholm and the Admitted Prior Art. PO Resp. 40–50. As support, ATI cites to Dr. Wolfe's Declaration. Ex. 2151.

In our discussion below, we address the parties' contentions after providing a brief summary of Lindholm and the Admitted Prior Art.

Lindholm

Lindholm describes a multithreaded graphics system that includes a programmable graphics processing pipeline. Ex. 1004, Abs., 4:4–12. Figure 2 of Lindholm is reproduced below.

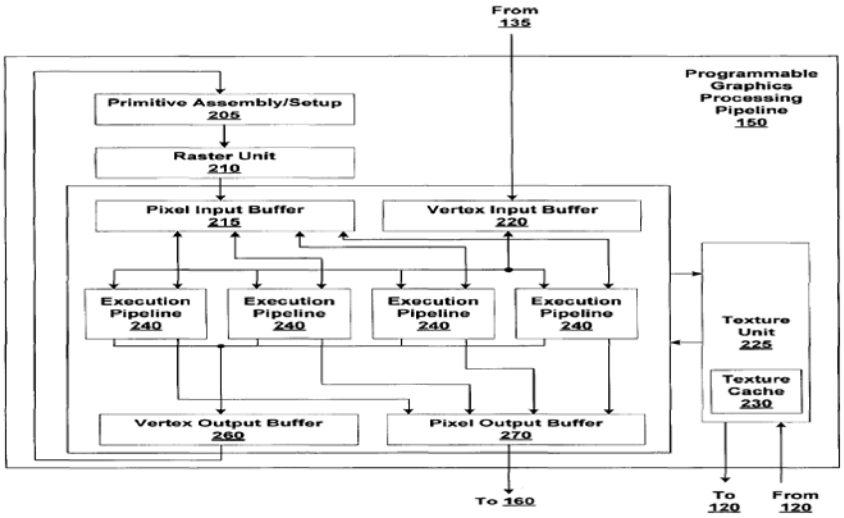


FIG. 2

As depicted in Figure 2, programmable graphics pipeline 150 includes pixel input buffer 215, vertex input buffer 220, execution pipelines 240, vertex output buffer 260, pixel output buffer 270, and texture unit 225.

Admitted Prior Art

Figure 1 of the ’053 patent is reproduced below.

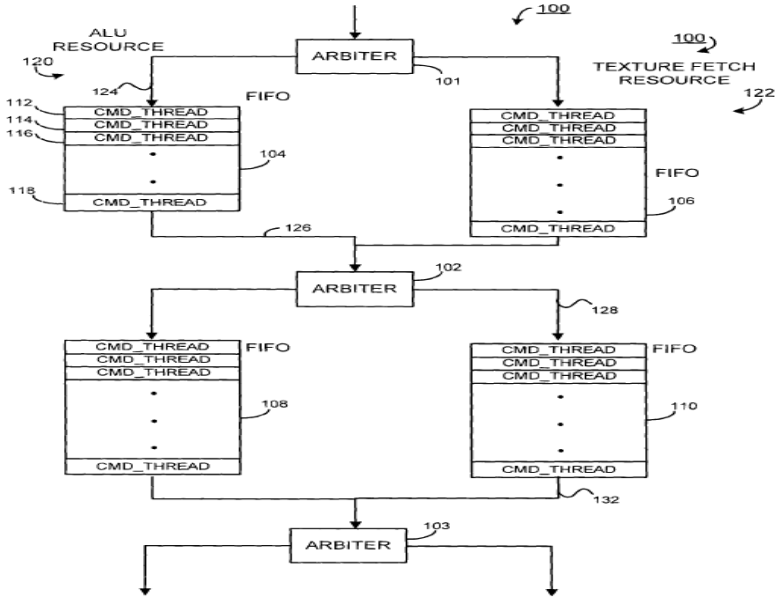


FIG. 1
(PRIOR ART)

As shown in Figure 1 of the ’053 patent, prior art sequencing system 100 includes arbiters 101–103 and buffers 104, 106, 108, 110. *Id.* at 1:32–64. In a typical embodiment, the buffers are first in and first out (“FIFO”) buffers, each stores multiple command threads. *Id.* System 100 is divided into resource divisions: ALU resource division 120 and texture fetch resource division 112. *Id.* Command thread 118 is withdrawn from reservation stations 104, 108 and provided to an ALU, and the command threads within texture fetch resource division 122 are withdrawn from reservation stations 106, 110 to be provided to texture fetch processors. *Id.* In short, the prior art sequencing system stores different types of command threads in different portions of the memory.

LG contends that Figure 1 and the Background of the Invention Section of the ’053 patent are Admitted Prior Art. Pet. 22–23, 36–37; Ex. 1001, 1:22–2:6. ATI counters that LG fails to show the relied upon text in the ’053 patent is actually admitted prior art. PO Resp. 4–5, 38–39. LG disagrees, arguing that ATI’s assertion is contrary to the controlling case law. Reply 18 (citing *Application of Nomiya*, 509 F.2d 566, 570–71 (CCPA 1975); *Riverwood Int’l Corp. v. R.A. Jones & Co.*, 324 F.3d 1346, 1354 (Fed. Cir. 2003)). LG further alleges that “nothing here suggests that the prior art described in the ’053 patent was the work of its inventors.” *Id.*

Upon review of the parties’ contentions and supporting evidence, we agree with LG. In *Nomiya*, when the appellants’ patent application included two figures, Figures 1 and 2, that were labeled as “prior art” and described as such in the specification, the Court held:

> We see no reason why appellants' representation in their application should not be accepted at face value as admission that Figs. 1 and 2 may be considered "prior art" for any purpose, including use as evidence of obviousness under § 103. . . . By filing an application containing Figs. 1 and 2, labeled prior art, *ipsissimis verbis*, and statements explanatory thereof appellants have conceded what is to be considered as prior art in determining obviousness of their improvement.

Nomiya, 509 F.2d at 570–71 (citations and footnote omitted).

Here, like in *Nomiya*, Figure 1 of the '053 patent is labeled as "PRIOR ART." The Background of the Invention Section of the '053 patent also describes Figure 1 as showing a prior art sequencing system. Ex. 1001, 1:32 ("FIG. 1 illustrates a prior art sequencing system 100."), 49 ("In the prior art embodiments of FIG. 1, the first buffer 104 receives an input command 124 and outputs a completed command thread 126 to the second arbiter 102."), 2:13–14 ("FIG. 1 illustrate[s] the schematic block diagram of a prior art command thread processing system."). ATI does not allege that the prior art embodiment was the named inventors' own work. PO Resp. 38–39. Nor does ATI contend that Figure 1 or the Specification of the '053 patent contains any error, or that the named inventors sought correction to the '053 patent. In fact, the same drawing with the "PRIOR ART" label and disclosure also were submitted in application No. 10/673,761, filed on September 29, 2003, now U.S. Patent No. 7,239,322 B2.

In view of the foregoing, we determine that LG has demonstrated by a preponderance of the evidence that Figure 1 and the related discussion in the

Background of the Invention Section of the ’053 patent are Admitted Prior Art against the claims at issue. Ex. 1001, 1:22–2:6, Fig. 1.

Memory device

Claims 1 and 5 recite “at least one memory device comprising a first portion operative to store a plurality of pixel command threads and a second portion operative to store a plurality of vertex command threads.” Ex. 1001, 7:1–15, 8:5–8. LG takes the position that Lindholm’s instruction cache unit and thread control buffer, as modified by the Admitted Prior Art, correspond to the claimed memory device. Pet. 13, 22. LG relies on Lindholm to disclose a graphics memory for storing pixel and vertex command threads, and relies on the Admitted Prior Art to disclose storing different types of command threads in different portions of the memory device. *Id.* at 22–24 (citing Ex. 1001, 1:42–64, Fig. 1). LG submits that it would have been obvious to modify Lindholm’s multithreaded graphics system to store different types of command threads in different portions of memory, in light of the Admitted Prior Art. *Id.* at 24.

ATI counters that the combination of Lindholm and the Admitted Prior Art does not disclose the claimed memory device because the Admitted Prior Art does not disclose explicitly storing pixel and vertex command threads, and an ordinarily skilled artisan would not have modified the Admitted Prior Art. PO Resp. 40–47. ATI also contends that such an artisan would not have combined Lindholm and the Admitted Prior Art. *Id.* at 44–47. ATI further alleges that combining Lindholm with the Admitted

Prior Art would not achieve faster access to command threads, flexible processing loads to reduce stalls, or performance improvement. *Id.*

Having reviewed the evidence in this record, we are not persuaded by ATI's arguments. Attacking the Admitted Prior Art individually does not undermine LG's showing of obviousness. *See Keller*, 642 F.2d at 426. The relevant inquiry here is whether the proposed prior art combination, taken as a whole, would have suggested the claimed subject matter to one of ordinary skill in the art. *See Merck*, 800 F.2d at 1097.

ATI's arguments with respect to modifying the Admitted Prior Art are misplaced. LG relies on the Admitted Prior Art to disclose a memory device that includes a first and second portion for storing different types of command threads. Pet. 22. Indeed, the Admitted Prior Art discloses that, at the time of the invention, a computer graphics system typically includes basic graphical processing elements, such as vertices and pixels. Ex. 1001, 1:24–28. The prior art system disclosed in the Admitted Prior Art has one set of buffers for storing ALU resource command threads and another set of buffers for storing texture fetch resource command threads. *Id.* at 1:42–64. Based on the evidence before us, we agree with LG that it was known in the art at the time of the invention to store different types of graphics command threads in different portions of a memory device.

We further are not persuaded by ATI's argument that LG has not articulated a sufficient reason to combine Lindholm with the Admitted Prior Art. Lindholm already stores pixel and vertex samples separately in different portions of a memory device. Ex. 1004, 4:35–39, 5:20–27, 7:27–

30 ("Thread Control Buffer 420 includes storage resources for each of at least two thread types, where the at least two thread types can include pixel, primitive, and vertex"), Fig. 2 (Pixel Input Buffer 215, Vertex Input Buffer 220, Vertex Output Buffer 260, Pixel Output Buffer 270). Dr. Bagherzadeh testifies that it would have been obvious to one with ordinary skill in the art to modify Lindholm's memory device to store different types of threads in different portions of memory, in light of the Admitted Prior Art, for "faster and convenient storage and retrieval functions, and thereby enhancing the logical layout of the thread processing system," taking "advantage of Lindholm's multithreaded architecture that allows the flexible processing of data loads to reduce calls." Ex. 1003 ¶¶ 105–07. Dr. Bagherzadeh's testimony is consistent with the prior art of record. Notably, the Admitted Prior Art indicates that, in a typical graphics processing system, vertices and pixels were processed through multiple steps providing for the application of textures and other processing instructions, and that to improve the efficiency of a graphics system, the control of the flow of the multiple command threads was preferred. Ex. 1001, 1:22–31. Based on the evidence before us, we credit the testimony of Dr. Bagherzadeh (Ex. 1003 ¶¶ 105–07) over that of Dr. Wolfe (Ex. 2151 ¶ 178). *See Yorkey*, 601 F.3d at 1284 (holding that the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so").

ATI and its expert testimony also are conclusory, as they do not explain specifically why storing pixel and vertex command threads in different portions of a memory device in a graphics processing system would

not improve the efficiency of thread processing. PO Resp. 55–57; Ex. 2151 ¶¶ 208–212. Nor do they provide sufficient or credible evidence that such an implementation would have been "uniquely challenging" or otherwise beyond the level of an ordinarily skilled artisan. *See Leapfrog*, 485 F.3d at 1162. As part of the obviousness analysis, "the knowledge of [a skilled] artisan is part of the store of public knowledge that must be consulted." *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013). Here, in fact, such a system was known in the art at the time of the invention, as evidenced by Moreton. Ex. 1006, Abs., 6:38–55, 15:53–64, Figs. 1, 5. There is no dispute that Moreton's graphics processing system stores pixel and vertex command threads in different portions of a memory device, as discussed above. *Id.*; PO Resp. 29–34.

For the foregoing reasons, we determine that LG has articulated reasoning with rational underpinnings why an ordinarily skilled artisan would have implemented, in light of the Admitted Prior Art, a memory device having a first portion operative to store a plurality of pixel command threads and a second portion operative to store a plurality of vertex command threads in Lindholm's graphics processing system, in a manner to achieve the subject matter of claims 1 and 5. We, therefore, conclude that LG has established sufficiently that the combination of Lindholm and the Admitted Prior Art would render the claimed "memory device" obvious.

<u>Arbiter and a plurality of command processing engines</u>

LG takes the position that: (1) Lindholm's instruction scheduler and dispatcher disclose the claimed "arbiter," as required by claims 1, 2, and 5;

and (2) Lindholm's computation resources within an execution unit disclose "a plurality of command processing engines, coupled to the arbiter, each operable to receive and process the command thread," as required by claim 5. Pet. 14–16 (citing Ex. 1004, 8:47–53, 9:5–8, 9:24–25, 9:41–47, 12:58–64).

ATI does not dispute that Lindholm's instruction scheduler and dispatcher teaches the claimed arbiter. *See* PO Resp. 40–50. Rather, ATI counters that each of Lindholm's computation resources is a type-specific processing engine, and cannot process both pixel and vertex command threads. *Id.* at 47–50. ATI also alleges that Lindholm does not describe a plurality of execution units coupled to a single arbiter. *Id.*

We are not persuaded by ATI's arguments. Once again, ATI's arguments and expert testimony are predicated on ATI's proposed claim construction to exclude *type-specific* processing engines and requiring *each* command processing engine to have the capability to process *all* of the command threads selected by the arbiter. *Id.* As discussed above, we decline to adopt that proposed claim construction, but instead, construe the "command processing engines" limitation recited in claim 5 as requiring each command processing engine to be coupled to an arbiter and operable to receive and process a command thread selected by the arbiter.

Based on our review of Lindholm, we agree with LG that Lindholm's computation resources within an execution unit disclose "a plurality of command processing engines, coupled to the arbiter, each operable to

receive and process the command thread," as required by claim 5. Figure 4 of Lindholm is reproduced below.

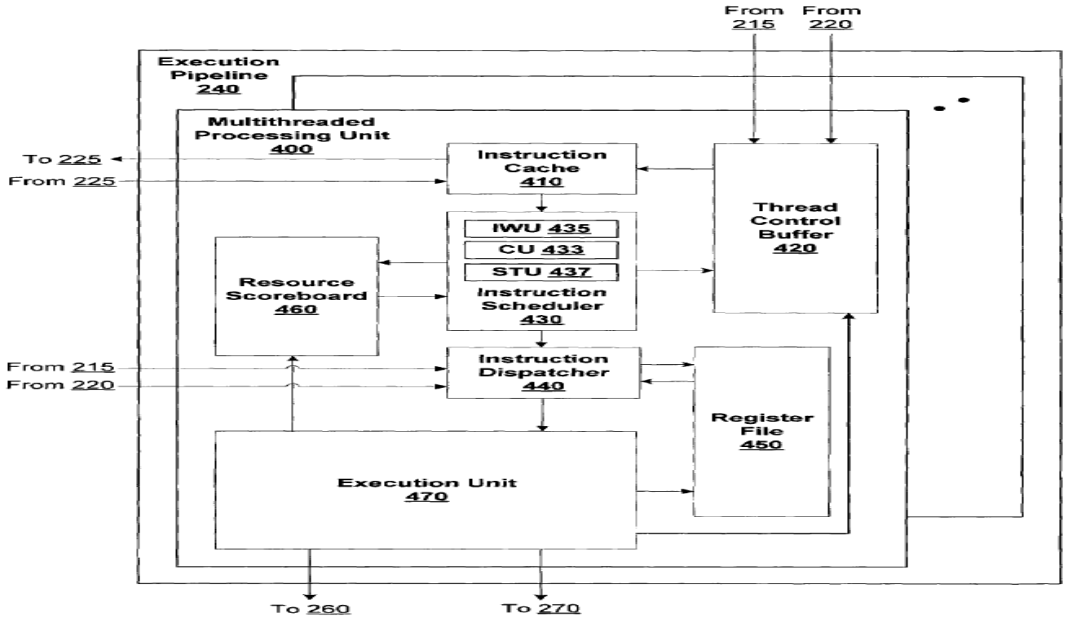


FIG. 4

As illustrated in Figure 4 of Lindholm, each execution pipeline 240 includes a plurality of multithreaded processing units 400 and thread control buffers 420 for receiving samples from pixel input buffer 215 or vertex input buffer 220. Ex. 1004, 7:19–42. Thread control buffer 420 includes storage resources for each thread type, e.g., pixel or vertex. *Id.* Instruction cache unit 410 is configured to read thread entries based on the priority assigned to each thread type, and it can be shared between multithreaded processing units 400. *Id.* at 8:4–20. Instruction scheduler 430 is configured to: (1) receive the program instructions, (2) determine availability of source data, and (3) schedule the program instructions for execution. *Id.* at 1:49–57. Instruction scheduler 430, working with instruction dispatcher 440, also schedules and dispatches pixel or vertex instructions for parallel execution.

Id. at 12:58–64. Instruction scheduler 430 evaluates the availability of *computation resources* in execution unit 470. *Id.* at 8:47–53. Each execution unit 470 is configured to process samples—e.g., vertices and pixels—"using *programmable computation units* to perform operations such as linear interpolation, derivative calculation, blending, and the like." *Id.* at 9:41–47 (emphasis added).

Contrary to ATI's argument and expert testimony that Lindholm does not describe multiple execution units coupled to a single arbiter (PO Resp. 49 (citing Ex. 2151 ¶¶ 186–88)), Lindholm explicitly discloses a plurality of computation resources or programmable computation units (command processing engines) within execution unit 470 that are coupled to a single instruction dispatcher working with an instruction scheduler (an arbiter). *Id.* Nothing in claim 5 requires the command processing engines to be coupled *directly* to the arbiter. Therefore, it is unnecessary to modify Lindholm, as alleged by ATI (PO Resp. 49–50; Ex. 2151 ¶¶ 189–91), for meeting the "command processing engines" limitation.

Given the evidence before us, we agree with LG that: (1) Lindholm's instruction scheduler and dispatcher teaches the claimed arbiter; and (2) Lindholm's computation resources or programmable computation units within an execution unit are command processing engines, coupled to an instruction scheduler and dispatcher (an arbiter), each operable to receive and process a pixel or vertex command thread selected by the arbiter, as required by claim 5. In view of the foregoing, we determine that LG has demonstrated sufficiently that Lindholm in combination with the Admitted

Prior Art would render the "arbiter" limitation, as recited in claims 1, 2, and 5, and the "command processing engines" limitation, as recited in claim 5, obvious.

Secondary considerations of nonobviousness

As discussed above in our obviousness analysis based on Moreton and Whittaker, we have considered ATI's evidence of secondary considerations pertaining to industry acceptance. PO Resp. 60 (citing Ex. 2142, 14; Ex. 2148, 9, 21; Ex. 2149, 12; Ex. 2150, 5). We find that ATI fails to establish the required nexus between the merits of the claimed invention and the alleged evidence of secondary considerations. Accordingly, ATI's objective evidence is accorded little weight. We conclude that, on balance, the strong evidence of obviousness outweighs the weak evidence of nonobviousness. *See Leapfrog*, 485 F.3d at 1162.

Conclusion on obviousness based on Lindholm and the Admitted Prior Art

ATI has not raised any additional arguments with regard to claims 6 and 7 other than those addressed above. Upon review of LG's analysis and supporting evidence, we agree with LG's showing—and adopt it as our own—that the combination of Lindholm and the Admitted Prior Art renders claims 6 and 7 obvious. *See, e.g.*, Pet. 11–24; Ex. 1001, 1:22–2:6, Fig. 1; Ex. 1004, 4:57–61, 5:36–40, 9:41–59, Fig. 4. For the foregoing reasons, we determine that LG has demonstrated by a preponderance of the evidence that claims 1, 2, and 5–7 are unpatentable over Lindholm and the Admitted Prior Art.

I. Obviousness Grounds Based on Stuttard and the Admitted Prior Art

LG asserts that claims 1, 2, and 5–7 are unpatentable under § 103(a) as obvious over Stuttard and the Admitted Prior Art. Pet. 24–37. In support of its assertion, LG provides detailed explanations as to how the combination of Stuttard and Admitted Prior Art meets each claim limitation. *Id*. LG also cites to Dr. Bagherzadeh's Declaration for support (Ex. 1003).

ATI counters that LG fails to show Figure 1 and the related discussion in the '053 patent are actually admitted prior art. PO Resp. 38–39. We addressed those arguments in our Lindholm obviousness analysis above and likewise determine that are unavailing here.

ATI also argues that the combination of Stuttard and the Admitted Prior Art does not disclose certain limitations, and LG fails to provide a sufficient reason to combine Stuttard and the Admitted Prior Art. PO Resp. 50–58. In support, ATI directs attention to Dr. Wolfe's Declaration. Ex. 2151. We begin our discussion with a brief summary of Stuttard, and we then address the parties' contentions in turn.[6]

<u>Stuttard</u>

Stuttard discloses a multithreaded graphics system that includes a memory device and processing core. Ex. 1005, 2:48–50, 4:38–5:40. Figure 3 of Stuttard is reproduced below with our annotation in green added.

[6] A summary of the Admitted Prior Art has been provided previously in our obviousness analysis based on Lindholm and the Admitted Prior Art.

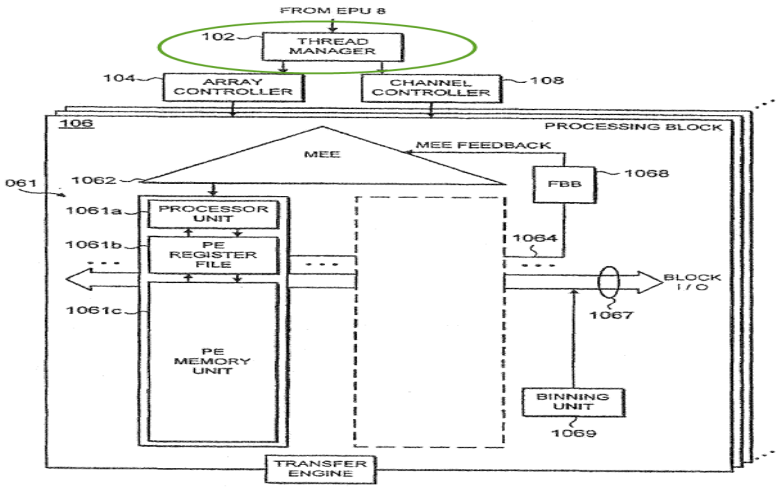
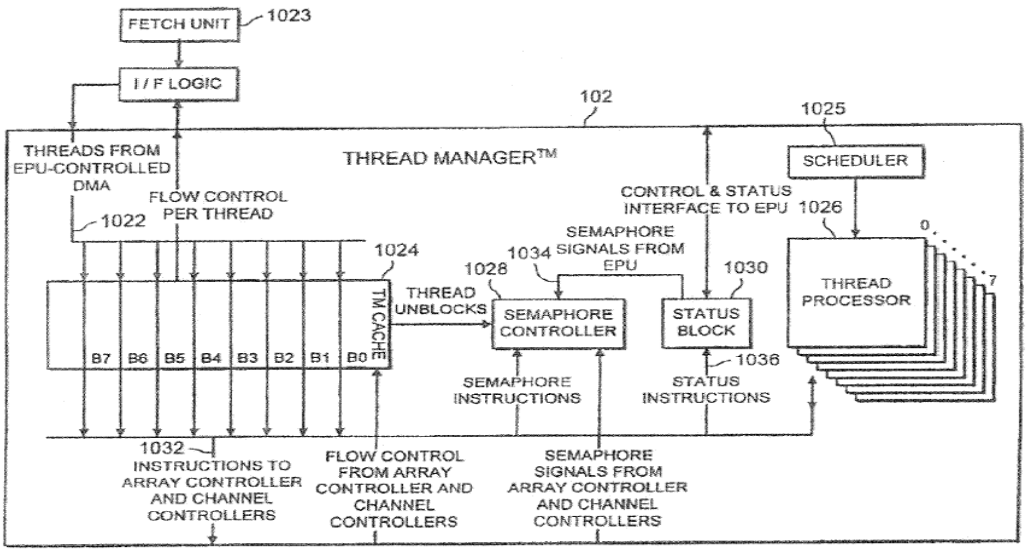


FIG. 3

As shown in Figure 3 of Stuttard, the processing core includes thread manager 102 that provides instructions to a plurality of processing blocks 106 through array controller 104 and channel controller 108. *Id.* at 4:43–64. Processing block 106 includes processor units 1061a for executing the instructions. *Id.* Thread manager 102 manages instruction streams or threads to increase efficiency and reduce response time. *Id.* at 5:19–44.

Figure 4 of Stuttard is reproduced below.



As shown in Figure 4 of Stuttard, thread manager 102 includes thread scheduler 1025 and thread processors 1026, as well as cache memory unit 1024 for storing instructions for each thread—having one buffer per thread. *Id.* at 5:45–52. The threads are assigned priorities relative to one another. *Id.* at 5:56. Thread scheduler 1025 determines which thread should be active at any one time. *Id.* at 6:19–21. Thread processors 1026 control the issuance of instructions from the thread manager to maintain processing of simultaneously active program threads. *Id.* at 5:65–6:4.

Memory device

With respect to the "memory device" limitation recited in claims 1 and 5, LG relies on Stuttard's cache unit for its disclosure of a memory device for storing pixel and vertex command threads. Pet. 27, 29–31 (citing Ex. 1005, 5:45–55, 9:50–65, 10:42–47). LG also relies upon the Admitted Prior Art for its disclosure of storing different types of command threads in different portions of the memory device. *Id.* at 36 (citing Ex. 1001, 1:42–46). LG submits that it would have been obvious to modify Stuttard's cache unit to store different types of command threads in different portions of memory, in light of the Admitted Prior Art, for "faster access to different types of command threads while also simplifying the storage of threads in memory of a multithreaded processor." *Id.* at 36–37.

ATI counters that it would not have been obvious to modify Stuttard in view of the Admitted Prior Art. PO Resp. 55–57 (citing Ex. 2151 ¶¶ 210–11). In particular, ATI argues that LG's proposed combination is based on an improper modification of the Admitted Prior Art. *Id.* at 56. ATI also

alleges that combining Stuttard with the Admitted Prior Art would not achieve faster access to command threads, reduction of memory, increases in operation speed, or performance improvement. *Id.*

ATI's arguments as to modifying the Admitted Prior Art are misplaced. As discussed above, the Admitted Prior Art discloses that, at the time of the invention, a computer graphics system typically includes basic graphical processing elements, such as vertices and pixels. Ex. 1001, 1:24–28. The prior art system disclosed in the Admitted Prior Art has one set of buffers for storing ALU resource command threads and another set of buffers for storing texture fetch resource command threads. *Id.* at 1:42–64. Based on the evidence before us, we agree with LG that it was known in the art at the time of the invention to store different types of graphics command threads in different portions of a memory device.

We are not persuaded by ATI's argument that LG has not articulated a sufficient reason to combine Stuttard with the Admitted Prior Art. As noted by LG, Stuttard discloses a graphics processing system for processing pixel and vertex operations, and the Admitted Prior Art discloses storing different types of command threads in different memory portions in a graphics processing system. Pet. 27, 29–31, 36–37; Ex. 1005, 5:45–55, 9:50–65, 10:42–47; Ex. 1001, 1:42–46, Fig. 1. Dr. Bagherzadeh testifies that it would have been obvious to one with ordinary skill in the art to modify Stuttard's cache unit to store different types of threads in different portions of memory, in light of the Admitted Prior Art, for "faster and convenient storage and retrieval functions, and thereby enhancing the logical layout of the thread

processing system," taking "advantage of Stuttard's multithreaded architecture that can more efficiently and speedily process graphics data." Ex. 1003 ¶¶ 142–44. That testimony is consistent with the prior art of record. Notably, the Admitted Prior Art indicates that, in a typical graphics processing system, vertices and pixels were processed through multiple steps providing for the application of textures and other processing instructions, and that, to improve the efficiency of a graphics system, the control of the flow of the multiple command threads was preferred. Ex. 1001, 1:22–31. Based on the evidence in this record, we credit the testimony of Dr. Bagherzadeh (Ex. 1003 ¶¶ 142–44) over that of Dr. Wolfe (Ex. 2151 ¶ 211). *See Yorkey*, 601 F.3d at 1284.

ATI and its expert testimony also are conclusory, as they do not explain specifically why storing pixel and vertex command threads in different portions of a memory device in a graphics processing system would not improve the efficiency of thread processing. PO Resp. 55–57; Ex. 2151 ¶¶ 208–212. Nor do they provide sufficient or credible evidence that such an implementation would have been "uniquely challenging" or otherwise beyond the level of an ordinarily skilled artisan. *See Leapfrog*, 485 F.3d at 1162. As part of the obviousness analysis, "the knowledge of [a skilled] artisan is part of the store of public knowledge that must be consulted." *Randall Mfg.*, 733 F.3d at 1362. Here, in fact, such a system was known in the art at the time of the invention, as evidenced by Moreton. Ex. 1006, Abs., 6:38–55, 15:53–64, Figs. 1, 5. There is no dispute that Moreton's graphics processing system stores pixel and vertex command threads in

different portions of a memory device, as discussed above. *Id.*; PO Resp. 29–34.

For the foregoing reasons, we determine that LG has articulated reasoning with rational underpinnings why an ordinarily skilled artisan would have implemented, in light of the Admitted Prior Art, a memory device having a first portion operative to store a plurality of pixel command threads and a second portion operative to store a plurality of vertex command threads in Stuttard's graphics processing system, in a manner to achieve at the subject matter of claims 1 and 5. We, therefore, conclude that LG has established sufficiently that the combination of Stuttard and the Admitted Prior Art would render the claimed "memory device" obvious.

Arbiter

Claim 1 recites an arbiter "operable to *select a command thread* from either of the plurality of pixel command threads and the plurality of vertex command threads *based on relative priorities* of the plurality of pixel command threads and the plurality of vertex command threads." Ex. 1001, 7:16–20 (emphases added). Claim 2 recites "wherein the arbiter is further operable to provide the command thread to the command processing engine." *Id.* at 7:24–26. Claim 5 recites an arbiter "operable to *select a command thread* from either of the plurality of pixel command threads and the plurality of vertex command threads." *Id.* at 8:9–12 (emphasis added).

LG asserts that Stuttard's thread scheduler and thread processors in the thread manager, collectively, disclose an "arbiter," as required by claims 1, 2, and 5, because the thread scheduler, working in conjunction with the

thread processors, schedules and activates the highest priority thread. Pet. 28 (citing Ex. 1005, 6:16–21, 11:13–12:25). LG also alleges that Stuttard's processing blocks correspond to the claimed "command processing engines." *Id.* at 25 (citing Ex. 1005, 9:61–62).

ATI does not dispute that Stuttard's processing blocks disclose a plurality of command processing engines, each operable to receive and process a pixel or vertex command thread, as required by claims 2 and 5. PO Resp. 50–58. Rather, ATI argues that Stuttard does not disclose an "arbiter that selects between pixel and vertex command threads because Stuttard's system performs graphics-processing operations in *discrete, sequential phases*, i.e., a phased system." *Id.* at 51–55 (emphasis added by ATI). ATI contends that Stuttard does not disclose selection between pixel and vertex threads because, during the vertex processing phase, the arbiter would select only from vertex threads, and, during the pixel processing phase, the arbiter would select only from pixel threads, but not select between pixel and vertex threads. *Id.* at 53–54.

ATI's arguments and expert testimony, however, narrowly focus on a *simplified* illustration of how each processing block works *when a thread manager is not utilized* and fail to consider Stuttard, as a whole, including the disclosure of a thread manager and scheduler. PO Resp. 51–55 (citing Ex. 1005, 9:51–10:47, 18:11–23; Ex. 2151 ¶¶ 192–206). "A reference must be considered for everything it *teaches* by way of technology and is not limited to the particular *invention* it is describing and attempting to protect." *EWP Corp. v. Reliance Universal Inc.*, 755 F.2d 898, 907 (Fed. Cir. 1985)

(emphases in original). In an obviousness analysis, we must consider the combination of references, as a whole, in light of the general knowledge of an ordinarily skilled artisan. *Merck*, 800 F.2d at 1097.

Based on Stuttard's disclosure as a whole, we are not persuaded by ATI's argument and expert testimony that Stuttard does not disclose selection between pixel and vertex command threads. As discussed above, Stuttard's cache unit stores a plurality of pixel and vertex command threads. Ex. 1005, 5:45–55, 9:50–65, 10:42–47. ATI acknowledges that Stuttard's system processes both pixel and vertex operations, and selects a pixel or vertex command thread for processing. PO Resp. 53–54. Indeed, Stuttard's thread manager, which includes a thread scheduler, selects a thread based on the relative priorities to one another from a plurality of command threads. Ex. 1005, 5:56–59 ("The threads are assigned priorities relative to one another."); 10:49–12:54 ("The thread scheduler, when running, recalculates which thread should be active whenever one of the following scheduling triggers occur: A thread with higher priority than the current active thread is READY . . . . [T]he scheduler activates the highest priority READY thread."). Nothing in Stuttard suggests that, when selecting a pixel thread, the thread manager would disregard all vertex threads, or when selecting a vertex thread, the thread manager would disregard all pixel threads, as alleged by ATI. PO Resp. 54. Further, as the Admitted Prior Art describes, an arbiter was known in the art to select a command thread between different types of command threads. Ex. 1001, 1:32–64, Fig. 1.

In view of the foregoing, we determine that LG has demonstrated sufficiently that Stuttard's thread manager, which includes a thread scheduler and thread processors, would have rendered the "arbiter" limitations, as recited in claims 1, 2, and 5, obvious.

Texture processing engine

With respect to claim 7, which requires a *texture* processing engine, LG asserts that one of ordinary skill in the art would have recognized that Stuttard's graphics data processing of lighting and shading would require a texture processing engine. Pet. 29 (citing Ex. 1005, 9:61–65). As support, Dr. Bagherzadeh testifies that because Stuttard discloses that the processing elements perform lighting and shading functions which are considered texture processing, the processing elements of Stuttard's processor units include a texture processing engine. Ex. 1003 ¶ 131.

ATI takes the position that Stuttard does not suggest a texture processing engine, as texture operation is an optional, but not a *necessary* step of lighting and shading. PO Resp. 57–58; Ex. 2151 ¶¶ 215–17. ATI also directs our attention to examples disclosed in several references that do not involve texture operations. Exs. 2004, 2005, 2138, 2139.

An obviousness analysis, however, "need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *KSR*, 550 U.S. at 418. Prior art must be read in context, taking account of the general knowledge possessed

by a person with ordinary skill in the art at the time of the claimed invention. *Translogic*, 504 F.3d at 1259–1262.

There is no dispute that the use of a texture processing engine in a graphics processing system was known in the art at the time of the invention. Ex. 1001, 1:32–48 ("FIG. 1 illustrates a prior art sequencing system . . . and the command threads within the texture fetch resource division 122 maybe withdrawn from the reservation stations 106 and 110 to be provided to a texture fetch processor."). Notably, in a typical graphics processing system at the time of the invention, basic graphical elements—vertices and pixels—were processed through multiple steps providing for the application of textures and other processing instructions; and arithmetic logic units, and texture processors were utilized for processing those elements and instructions. *Id.* at 1:22–48.

ATI acknowledges that Stuttard's system processes both vertex and pixel operations. PO Resp. 53; Ex. 1005, 9:50–10:47. Stuttard also discloses performing "three dimensional geometry, view, lighting and shading." Ex. 1005, 9:63–65. ATI's expert, Dr. Wolfe, testifies that "vertex commands can also involve texture operations." Ex. 2151 ¶¶ 159, 165 ("at least 10–20% of vertex command threads involving texture operations should be processed by the texture fetch processor"). Dr. Wolfe also agrees with Dr. Bagherzadeh that the majority of pixel command threads involve texture operations. *Id.* ¶¶ 161–162. Therefore, an ordinarily skilled artisan would have recognized that Stuttard's graphics processing system includes a texture processing engine to process pixel and vertex command threads.

Given the evidence in this record, we determine that LG has shown sufficiently that the combination of Stuttard and the Admitted Prior Art suggests a texture processing engine, as required by claim 7.

Secondary considerations of nonobviousness

As discussed above in our obviousness analysis based on Moreton and Whittaker, we have considered ATI's evidence of secondary considerations pertaining to industry acceptance. PO Resp. 60 (citing Ex. 2142, 14; Ex. 2148, 9, 21; Ex. 2149, 12; Ex. 2150, 5). We find that ATI fails to establish the required nexus between the merits of the claimed invention and the alleged evidence of secondary considerations. Accordingly, ATI's objective evidence is accorded little weight. We conclude that, on balance, the strong evidence of obviousness outweighs the weak evidence of nonobviousness. *See Leapfrog*, 485 F.3d at 1162.

Conclusion on obviousness based on Stuttard and the Admitted Prior Art

ATI has not raised any additional arguments with regard to dependent claim 6 other than those addressed above. Upon review of LG's analysis and supporting evidence, and for the reasons stated above, we agree with LG's showing—and adopt it as our own—that the combination of Stuttard and the Admitted Prior Art renders claim 6 obvious. *See, e.g.*, Pet. 24–37; Ex. 1001, 1:22–2:6, Fig. 1; Ex. 1005, 20:44–47, Fig. 11. For the foregoing reasons, we determine that LG has shown by a preponderance of the evidence that claims 1, 2, and 5–7 are unpatentable over Stuttard and the Admitted Prior Art.

J. Motion to Exclude Evidence

LG filed a Motion to Exclude Evidence, seeking to exclude portions of Mr. Watson's Declaration (Ex. 2105 ¶¶ 4, 5, 11–16, 22–135) and the documents these paragraphs purport to authenticate (Exs. 2007, 2009–18, 2020–42, 2053–104, 2108). Paper 46 ("Mot."), 1–3. ATI filed an Opposition (Paper 47), and LG filed a Reply (Paper 54) in support of its Motion to Exclude.

ATI relies on the documents (Exs. 2007, 2009–18, 2020–42, 2053–104, 2108) to antedate Moreton, Lindholm, and Stuttard. PO Resp. 1–29. We need not reach the merits of LG's Motion to Exclude Evidence because, even without excluding portions of Mr. Watson's Declaration and the documents, we have decided that issue in LG's favor. Accordingly, LG's Motion to Exclude Evidence is *dismissed as moot.*

III. CONCLUSION

For the foregoing reasons, we determine that LG has demonstrated by a preponderance of the evidence that claims 1, 2, and 5–7 of the '053 patent are unpatentable based on the following grounds:

Claims	Basis	References
5–7	§ 102(e)	Moreton
1 and 2	§ 103(a)	Moreton and Whittaker
1, 2, and 5–7	§ 103(a)	Lindholm in view of the Admitted Prior Art
1, 2, and 5–7	§ 103(a)	Stuttard in view of the Admitted Prior Art

IV. ORDER

For the foregoing reasons, it is

ORDERED that claims 1, 2, and 5–7 of the ’053 patent are held *unpatentable*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

PETITIONER:

Robert G. Pluta
Bryan Nese
Cliff Maier
Amanda Streff
Michael W. Maas
MAYER BROWN LLP
rpluta@mayerbrown.com
bnese@mayerbrown.com
cmaier@mayerbrown.com
astreff@mayerbrown.com

PATENT OWNER:

Jason D. Eisenberg
Michael Ray
Johnathan Tuminaro
Michael D. Specht
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
jasone-PTAB@skgf.com
mray-PTAB@skgf.com
jtuminar-PTAB@skgf.com
mspecht-PTAB@skgf.com