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Transcript of Massoud Pedram, Ph.D.

Date: January 4, 2023

Case: Certain Graphics Systems, Components Thereof (337-TA-1318)

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Fax: 888-503-3767

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

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January 4, 2023

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UNITED STATES INTERNATIONAL TRADE COMMISSION WASHINGTON, D.C. -----x In the Matter of : Investigation No. CERTAIN GRAPHICS SYSTEMS, : 337-TA-1318 COMPONENTS THEREOF, AND DIGITAL : TELEVISIONS CONTAINING THE SAME : -----x Videotaped Deposition of MASSOUD PEDRAM, PH.D. Irvine, California Wednesday, January 4, 2023 8:17 a.m. PST Job No.: 476194 Pages: 1 - 356 Reported By: Rhonda Norberg, RPR CSR No. 9265, CCRR No. 185	A P P E A R A N C E S ON BEHALF OF THE COMPLAINANT: ADAM S. RIZK, ESQUIRE NANA LIU, ESQUIRE MICHAEL MCNAMARA, ESQUIRE (REMOTE) MINTZ, LEVIN, COHN, FERRIS, GLOVSKY AND POPEO PC 1 Financial Center Boston, Massachusetts 02111 617.542.6000 TAWFIK GOMA, ESQUIRE GOMA LAW 712 South Ocean Shore Boulevard Suite 207 Flagler Beach, Florida 32136 386.259.0040		
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25
Videotaped Deposition of MASSOUD PEDRAM, PH.D., taken at Orrick, Herrington & Sutcliffe, LLP, 2050 Main Street, Suite 1100, Irvine, California. Pursuant to notice, before Rhonda Norberg, Certified Shorthand Reporter No. 9265, CCRR No. 185 in and for the State of California.	A P P E A R A N C E S C O N T I N U E D ON BEHALF OF RESPONDENT REALTEK: JEFFREY JOHNSON, ESQUIRE ORRICK, HERRINGTON & SUTCLIFFE LLP 609 Main Street 40th Floor Houston, Texas 77002 713.658.6450 ON BEHALF OF RESPONDENT TCL: JOHN P. SCHNURER, ESQUIRE PERKINS COIE LLP 11452 El Camino Real Suite 300 San Diego, California 92130 858.720.5705 ALSO PRESENT: JERRY BUTLER - Videographer		

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1 2 3 WITNESS: MASSOUD PEDRAM, PH.D. 4 EXAMINATION PAGE 5 BY MR RIZK 7 6 BY MR. RIZK (Continued) 172 7 8 EXHIBITS 9 EXHIBIT NO. DESCRIPTION PAGE 10 Exhibit 1 Expert Report 15 11 Exhibit 2 Expert Report Appendices 15 12 Exhibit 3 Handwritten Notes 35 13 14 15 16 17 18 19 20 21 22 23 24 25	5 7 1 and on behalf of the witness. 2 MR. SCHNURER: John Schnurur of Perkins 3 Coie representing the TCL respondents. 4 THE VIDEOGRAPHER: The court reporter today 5 is Rhonda Norberg, representing Planet Depos. 6 Would the reporter please swear in the 7 witness. 8 9 MASSOUD PEDRAM, PH.D., 10 being first duly sworn or affirmed to testify to the 11 truth, the whole truth, and nothing but the truth, 12 was examined and testified as follows: 13 14 EXAMINATION 15 BY MR RIZK: 16 Q Good morning, Dr. Pedram. 17 A Good morning. 18 Q Would you please state your -- your name 19 and address for the record. 20 A Massoud Pedram. I reside currently at 21 800 North Crescent Heights Boulevard in Los Angeles, 22 California 90046. 23 Q And you're currently a professor at the 24 University of South Carolina? 25 Sorry. South California.
6 1 PROCEEDINGS 2 3 THE VIDEOGRAPHER: Here begins Media 4 Number 1 in the videotaped deposition of 5 Dr. Massoud Pedram in the matter of Certain Graphics 6 Systems, Components Thereof, 337-TA-1318, in the 7 United States International Trade Commission, 8 Washington, D.C., Case Number 337-TA-1318. 9 Today's date is January 4th, 2023; and the 10 time on the video monitor is 8:18 a.m. Pacific 11 Standard Time. The videographer today is 12 Jerry Butler, representing Planet Depos. 13 This video deposition is taking place at 14 2050 Main Street, Irvine, California 92614. 15 Would counsel please voice-identify 16 themselves and state whom they represent. 17 MR. RIZK: This is Adam Rizk with the firm 18 of Mintz Levin on behalf of the complainants, 19 Advanced MicroDevices, Inc., and API Technologies 20 ULC. 21 I'm joined today by my colleague, Nana Liu, 22 also with the firm of Mintz Levin, as well as 23 Tawfik Goma of Goma Law, G-o-m-a, L-a-w. 24 MR. JOHNSON: I'm Jeffrey Johnson for 25 Orrick on behalf of Realtek, the Realtek entities,	8 1 A Yes. 2 Yes, there is another institute called 3 University of South Carolina; but I am a professor 4 at the University of Southern California, USC. 5 Q Yes. Appreciate the clarification. 6 And how long have you been at USC for? 7 A 30 some years, 31 years. 8 Q And what -- what is the -- what is the 9 subject area of your focus at USC? 10 A Generally very large integrated circuit and 11 system design, computer architecture, 12 computer-related design, neuromorphic computing, 13 parallel processing, and the like. 14 Q You -- you teach courses there? 15 A Yes, I do. 16 Q And what are the courses that you're 17 currently teaching? 18 A I've taught different courses over my long 19 career from switching theory to computer-aided 20 design, VLSI circuits and systems to advanced 21 courses in architecture and even more recently on 22 superconductor electronics. 23 Q Okay. What are you presently teaching? 24 What is your current workload for teaching? 25 A Usually I teach one course per semester.

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9 1 Because of the volume of the research I do, I get a 2 course relief. As a result, I get to teach only one 3 course per semester; and the current semester that's 4 about to start next Monday, I will be teaching an 5 undergraduate course on VLSI circuits. 6 Q And VLSI circuits, that -- that involves 7 the physical implementation of circuits; is that 8 correct? 9 A That's one aspect of the course; but, of 10 course, we teach the theory of the transistor 11 operation, how you build logical gates, how you 12 build data path components such as adders and 13 multipliers, barrel shifters, how you build static 14 random access memory, how you organize the SRAM 15 cells into arrays that act as a cache memory or 16 scratch pad memory. 17 I also do teach dynamic RAM and flash 18 devices. 19 Q Okay. Have -- have you ever -- have you 20 ever worked on the -- have you ever performed a 21 logical design of a graphics processing unit? 22 A I have designed many circuits and systems, 23 even. For example, in 2004/5 timeframe, as part of 24 a Defense Advanced Project Research Agency project 25 we built a complete embedded system for power	11 1 including graphics. 2 BY MR. RIZK: 3 Q Okay. You -- you understand what a 4 graphics processing unit is, correct? 5 A Yes, I do. 6 A graphics processing engine is an engine 7 that's specialized for graphics processing tasks; 8 but the basic idea in the graphics processing system 9 is to have a SIMD or SIMT operation, and many of the 10 systems that are built also support SIMD operation, 11 so that's why when you ask the question, it's not a 12 direct yes-or-no answer. 13 Q Well, it's a simple question, Doctor. 14 A I've given you -- 15 Q Wait. Wait. Hang on. 16 A -- all the background. 17 MR. RIZK: I will conduct the deposition -- 18 MR. JOHNSON: Don't interrupt. 19 MR. RIZK: Don't tell me what to do, 20 Jeffrey. 21 MR. JOHNSON: You can finish your answer. 22 If he interrupts you, you just continue to finish 23 your answer until you're done. 24 THE WITNESS: Yes. 25 MR. RIZK: Doctor, I'd ask that you focus
10 1 management and dynamic voltage frequency scaling 2 that included multiple cores and multiple IO 3 devices. 4 It was capable of running at the best 5 frequencies at the time and be able to do advanced 6 power thermal management, dynamic backlight scaling, 7 and so on. 8 I've also built -- 9 Q And I'm just asking about graphics 10 processing units. 11 Have you worked -- 12 A How do processing -- 13 Q On the design -- 14 MR. JOHNSON: Wait, wait, wait, wait. 15 Don't talk over each other. Let him finish, you let 16 him finish. The court reporter can't handle that. 17 THE WITNESS: Sure. Thank you. 18 So, again, the -- the kinds of systems I 19 have built include advanced processing units that 20 can also do graphics processing; so many core 21 systems, multicore systems, I've built them, I'm 22 verified them, I've used them, I've practiced their 23 capabilities. 24 But, again, those parallel processing 25 systems could target many different applications,	12 1 on answering my question. You're answering the 2 question that you want to answer, not the question 3 that I'm asking you. 4 THE WITNESS: Yes. 5 MR. RIZK: I think you know what a graphics 6 processing unit is. You just explained it to me 7 that it's a -- it's a circuit that's specialized for 8 graphics processing. 9 Q So it's a very simple question. Have you 10 designed a graphics processing unit, "yes" or "no"? 11 I'm not interested in -- in all these other circuits 12 that might be analogous to graphics processing 13 units. Specifically for graphics processing, have 14 you designed a graphics processing unit? 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: Again, as I've said before, 17 and I'll repeat my answer -- you might not like it, 18 sir, but that's my answer. 19 My answer is the kinds of systems I've 20 built can also do graphics processing because they 21 have SIMD capabilities, and I think that one could 22 reasonably state, therefore, that I have built these 23 kinds of systems, yes, sir. 24 BY MR. RIZK: 25 Q So you've built a graphics processing unit?

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13 1 A Again, the kinds of systems that can do 2 graphics processing, yes, sir, I have done that. 3 Q I'm not asking if you've built kinds of 4 systems that can do graphics processing, I'm asking 5 if you've built a graphics processing -- 6 A Can you give me an example of the kind of 7 GPU, graphics processing unit, that you have in mind 8 so -- for example, are you talking about a 9 particular system in mind? Then I can tell you no, 10 I have not built that kind of system. 11 Q A -- a system that is designed specifically 12 for graphics processing. 13 A Designed. 14 MR. JOHNSON: Objection; form. 15 THE WITNESS: Yeah. 16 A system that's designed specifically to do 17 graphics processing and nothing else, no, I have not 18 considered doing that, no. 19 BY MR. RIZK: 20 Q Okay. Have you designed a system that is 21 designed to do asynchronous shading? 22 A No, I have not designed a system that does 23 asynchronous shading as such. 24 Q Okay. And your -- all the work that you've 25 just mentioned, your focus was on the power	15 1 Q Have you ever designed the logical design 2 of an ALU? 3 A Of course, yes, sure. 4 MR. RIZK: I'm going to introduce what has 5 been marked for identification purposes as Exhibit 1 6 and Exhibit 2. 7 Exhibit 1 is the expert report of 8 Massoud Pedram regarding invalidity of U.S. Patent 9 Numbers 7,742,053 and 8,854,381, dated December 9, 10 2022. 11 (Exhibit 1 was marked for 12 identification by the Stenographer; 13 attached hereto.) 14 MR. RIZK: And Exhibit 2 are the 24 15 appendices that were attached to the expert report 16 of Dr. Pedram regarding invalidity of U.S. Patent 17 Number 7,742,503 and 8,854,381. 18 (Exhibit No. 2 was marked for 19 identification by the Stenographer; 20 attached hereto.) 21 22 MR. RIZK: Here you go, sir. 23 THE WITNESS: Yes. Thank you. 24 BY MR. RIZK: 25 Q Do you have Exhibits 1 and 2 in front of
14 1 management side of the equation when you say that 2 you've -- you've built these systems? 3 A No, not really. 4 I mean, I've -- over the years, I've had 5 many different projects early on in my career, and 6 that's how I made my name in this space initially, 7 was to focus on low-power electronics, low-power 8 design. 9 But since at least 2002 or '3, I've built 10 many other systems that -- that -- whose focus was 11 really on performance, on throughput. The latest 12 project, for example, I've been involved in for -- 13 again, for DARPA, Defense Advanced Research Project 14 Agency, is to build an accelerator chip that 15 contains many, many parallel cores to do homomorphic 16 computation, which means I can take cipher text and 17 directly act -- process ciphered information without 18 ever having to decipher it, and so I -- I increased 19 the privacy of the end users using this kind of 20 system. 21 And the system is quite complicated, 22 150-millimeter-square chip done in 12-nanometer 23 global family process containing at least 16 layers 24 of parallel processing units, each lane containing 25 multiple ALUs all working in parallel.	16 1 you? 2 A Yes, sir, I do. 3 Q And Exhibits 1 and 2 collectively are your 4 expert report that you have provided in this matter, 5 correct? 6 A That is correct, sir. 7 Q And who did you work on this report with? 8 A Counsel. 9 Q Okay. Which counsel? 10 A From Orrick, Jeff is -- is here. 11 Essentially mostly with Jeff. 12 Q Okay. Did you consult with anyone else 13 concerning your report? 14 A Outside the counsel, you mean, or -- 15 Q Let's start with within counsel. 16 A I think there was Johannes. I forget the 17 last name. I'm sorry. 18 Q It's okay. 19 A Who was also involved initially in some of 20 the discussions. 21 I've had discussions also with Chris and 22 Robert, again, from the counsel. 23 Q Okay. And outside of your counsel, have 24 you discussed your report with anybody? 25 A No, sir.

17 1 Q Okay. And who wrote your report? 2 A I did. 3 Q Okay. Did anybody else participate in the 4 authorship of your report? 5 A I mean, it's been an interactive process. 6 I mean, there are, of course, some parts of this 7 that have to do with the legal, I guess, principles 8 that I must abide by and understand that was 9 provided to me by the counsel; but the technical 10 parts all I've written myself. 11 Q And this report provides a statement and 12 bases for your -- for your opinion that Patent 13 Numbers 7,742,053 and 8,854,381 are invalid, 14 correct? 15 A That is correct, yes. 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: Not only this report. I 18 mean, my -- I have a lot of -- I mean, I've -- all 19 of my opinions are reflected here regarding the 20 invalidity of those two patents; but, again, I have 21 a lot of knowledge that's not necessarily conveyed 22 in -- in this report, background -- 23 MR. RIZK: Okay. Well, my focus today is 24 going to be on what you stated in your report. 25 THE WITNESS: That's fine.	19 1 the -- the paragraphs that I'll represent to you 2 have been stricken just so that way, we're -- we 3 have a clear record about what the subject of your 4 testimony is today. 5 A Can I have a pen, then, please? 6 Q Yes, of course. 7 A Thank you. 8 Please go ahead. 9 Q So let's start with Paragraphs 114 through 10 116 of Exhibit 1, which appear on Pages 46 through 11 48. If you can just cross those out using the pen 12 that was handed to you. 13 A So 114 -- 14 Q 114 all the way through 116. 15 A Including 116, yes. 16 Q Through and including 116, correct. 17 A Yes. 18 Q Okay. Also if you could strike 135 through 19 Paragraph 165. And that appears between Pages 54 20 through 67. 135 through 165, Pages 54 through 67. 21 If you could just cross out each one of those -- the 22 paragraphs that appear on those pages. 23 And if it's easier, if the whole page is 24 stricken, Doctor, you can just put a big "X" on the 25 page just to make it more simple.
18 1 MR. RIZK: I don't -- I'm not interested in 2 things that are outside the scope of your report. 3 Q So you -- you endeavored to use your best 4 efforts to provide your opinion and the bases 5 therefor in your report which is marked as 6 Exhibits 1 and 2, correct? 7 A Yes, sir. 8 Q Okay. So the subject matter of my 9 questioning today is going to focus on your report, 10 not on things that are outside of -- of your report. 11 Let's -- let's turn to Page 2 of Exhibit 1, 12 please. 13 A Yes. 14 Q And there you provide the summary of your 15 conclusions concerning invalidity, correct? 16 A Yes, sir. 17 Q And you understand that some of the 18 opinions that you've offered have been stricken, 19 correct? 20 A I heard yesterday that there was a ruling 21 from the judge, ALJ, in which some particular 22 paragraphs from this report have been stricken. 23 Q Yep. Okay. 24 A That -- that much, I know, yes. 25 Q Okay. So I'm going to ask you to mark	20 1 A No, that's fine. 2 So -- done, yes. 3 Q Okay. And then let's also strike 100 -- 4 Paragraph 169 through 172, which appears on Pages 69 5 through 71. 6 Actually, 69 through 72. 7 A Done. 8 Q And then Paragraph 250, which appears on 9 Page 103 to 104. 10 Can I see Exhibit 1, please, sir? Can you 11 hand me that exhibit? 12 A Sure. 13 Q Thank you. 14 A Here you are. 15 Q I'll just note that in Exhibit 1, 16 Paragraph 172 wraps into Page 72, which you didn't 17 mark, so I'll hand that back to you. It would make 18 sense to mark it just to keep clear. 19 A Sure. Thank you. 20 Q So to be clear, sir, the subject matter of 21 my questioning today is going to focus on the 22 paragraphs that you did not just mark with a -- with 23 an "X" to denote that it has been stricken, based 24 upon my representation of the paragraphs that were 25 stricken.

21 1 I'm not -- to the extent you have opinions 2 that extend into the paragraphs that have been 3 stricken, I'm not seeking your testimony on -- 4 A I understand that. 5 Q -- those paragraphs. 6 So on Page 2 of -- of Exhibit 1, which is 7 the summary of your conclusions, you identify two 8 grounds that we're going to discuss today for 9 obviousness of the '053 patent, grounds based on 10 obviousness based upon Studdard (phonetic) and 11 grounds of obviousness based upon Kimura (phonetic), 12 correct? 13 A I guess the implication here is that 14 because we took out some of the paragraphs, the 15 combination of Williams and Whitaker -- 16 Q Yes. 17 A -- is not considered anymore. 18 Q That's -- that's correct, we've stricken 19 Williams and Whitaker. 20 A So subject to that, yes, your statement is 21 accurate. 22 Q All right. And it's your opinion that -- 23 that both -- both Studdard and Kimura by themselves 24 render the '053 patent obvious, correct? 25 A Claims -- Claims 1 to 9 of that patent,	23 1 focusing on '381. Then I go on into the file 2 history and conclude with the asserted claims of the 3 '381 in Paragraph 78. 4 Q So -- okay. 5 And in Paragraph 70 of your report, you 6 provide a definition of the term "thread" as a 7 single stream of instructions that implements a 8 shader program. 9 Do you see that in the first sentence of 10 Paragraph 70? 11 A Yes. 12 Q And that's your understanding of what a 13 thread is? 14 A I guess the emphasis here is on the 15 singular stream of instructions. A shader program 16 may involve multiple threads. It's not necessarily 17 a single thread; but a thread is a singular stream 18 of instructions that implements some -- some part of 19 a shader program. 20 Q Okay. A -- a shader program can be a 21 thread, but it's not necessarily a thread, correct? 22 MR. JOHNSON: Objection; form. 23 THE WITNESS: A shader program can comprise 24 of a single thread or multiple threads. 25 ///
22 1 yes, sir. 2 Q Okay. All right. And if we could -- I 3 could direct your attention to Paragraph 60 through 4 68 of your report, that provides an overview of the 5 '053 patent, correct? Starting on Page 15. 6 A I mean, it's not only the '053, but -- 7 there is a technology background as well. 8 But essentially, yes, it's technology 9 background plus a summary of '056 [sic]. 10 Q You -- and that continues through 11 Paragraph 68 of your report, correct? 12 A Up to Paragraph 67, I describe the 13 technology background, the '053 as well as the 14 prosecution history, the file history. 15 On Paragraph 68, as you see, I'm just 16 simply providing a description of the claims on the 17 litigation, Claims 1 to 9. 18 Q And directing your attention to 19 Paragraph 69 of your report -- 20 A Yes. 21 Q -- which is on Page 22, there -- that's 22 where you start providing your overview of the '381 23 patent; is that correct? 24 A Again, there's some technology background; 25 but starting on Paragraph 71, it's specifically	24 1 BY MR. RIZK: 2 Q Okay. Can a thread comprise of a single 3 shader program? 4 A That's not how the logical hierarchy works. 5 I mean, a thread -- a single thread could correspond 6 to a shader program also, a very simple shader 7 program, yes. 8 Q Okay. And a very simple shader program can 9 correspond to a thread? 10 A A single thread. 11 Yes, that's possible. 12 Q Okay. 13 A Usually it's not the case. Usually that's 14 not the case, a shader program would be multiple 15 threads. But yeah, it's possible. 16 Q Okay. And what is a shader program? 17 A It's a piece of software code that 18 implements some graphics shading task, whether it's 19 fragment shading or vertex shading or geometry 20 shading, and then so on. 21 Q How does it do that? 22 A It contains a sequence of instructions 23 and -- in the form of a single thread or multiple 24 threads, and these instructions actually describe 25 what needs to be done with respect to that

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25 1 particular job. 2 For example, if it's a vertex shading 3 program, it will -- it's a program that we run on 4 individual verticis of a graphics object or set of 5 objects, and we'll do certain operations on them. 6 Maybe it's averaging of the -- some -- some -- some 7 attributes, maybe it's doing some kind of coordinate 8 transformation, maybe it's doing some kind of 9 lighting, and so on and so forth. 10 Q Okay. And there are different types of 11 shader programs. You can have a pixel shader 12 program, vertex shader program, so on and so forth, 13 correct? 14 A Correct, sir, yes. 15 Q Okay. And a -- a vertex shader program 16 would be a sequence of instructions that's 17 applicable to vertex processing, correct? 18 A Yes. 19 Q Okay. And a pixel shader program would be 20 a sequence of instructions applicable to pixel 21 processing, correct? 22 A Yes, you could say that. 23 Q Okay. Turning to Page 44 of your report, 24 please -- 25 And 44, Page 44, Paragraph -- actually,	27 1 There you go. 2 A Yes, that's correct. Very good. 3 I guess in your question, by the "element," 4 you mean the at least one memory device comprising a 5 first portion operative to restore a plurality of 6 pixel command threads and a second portion operative 7 to store a plurality of vertex command threads. 8 Assuming that's the case, yes, I do. 9 Q Okay. And you provide the -- the basis of 10 your opinion that Studdard satisfies the element 11 that you just recited in Paragraphs 109 through 113 12 of your report, correct? 13 A Yes, sir. 14 Q Okay. And in turning to Paragraph 112 -- 15 Do you have that paragraph in front of you? 16 That's on Page 45 of your report. 17 A Yes, sir, I do. 18 Q Okay. And -- and you cite to the fact that 19 you believe that the cache 1024 receives and stores 20 instructions as the basis for your belief that the 21 cache receives and stores command threads, correct? 22 A What I say here -- I can read it to you; 23 but if you want more details, I would like to go to 24 the citation that I have included here for Studdard. 25 What I said here -- said here is that as
26 1 sorry. Let me -- let me go back for a second. 2 So you, in your report, summarized the 3 Court's construction of "command thread," correct? 4 A Yes, I did. 5 Q Okay. And you understand that the Court 6 has construed "command thread" to be a sequence of 7 commands applicable to the corresponding element? 8 A So the claim constructions by ALJ start on 9 Page 29 of my report. 10 Q And on Page 30, you can see that "command 11 threads" was construed as a sequence of commands 12 applicable to the corresponding element, right? 13 A Correct, sir, yes. 14 Q And then going back to Page 44 of your 15 report, Paragraphs 109 through 110, that -- those 16 paragraphs provide part of your opinion with respect 17 to why you believe the memory device of Studdard 18 satisfies the element, correct? Element 1-A of the 19 '053 patent? 20 A May I have the Studdard reference, please, 21 first before I answer the question? 22 Q Okay. It's -- it is in your report, 23 Exhibit 2, Tab 9. 24 Is that 9 in front of you? 25 You're in Tab 8 right now. Tab 9 is here.	28 1 discussed earlier, the processing blocks 106 that 2 receive instructions from the thread manager 102 3 containing cache unit 1024 process both pixel and 4 vertex data. 5 Q Okay. But the -- the claim construction 6 requires that the command thread be a sequence of 7 commands, not a sequence of instructions, correct? 8 A But the Court has construed the command 9 thread to be a sequence of commands applicable to 10 the corresponding element without ALJ construing 11 what a command itself is. 12 I think the construction is about "command 13 thread," not "command," and so when we see -- so 14 instructions could be examples of commands in this 15 case. 16 Q Okay. So you would understand that a -- a 17 sequence of instructions applicable to the 18 corresponding element would satisfy the 19 Administrative Law Judge's construction of a command 20 thread as a consequence of commands applicable to 21 the corresponding element, correct? 22 MR. JOHNSON: Objection; form. 23 THE WITNESS: Again, to me, the issue here 24 is the -- the notion of a thread, which is a 25 sequence of instructions; and a command thread in

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29 1 the -- in this context is -- is a sequence of 2 commands. 3 Now, commands could be high-level or 4 low-level, but that's besides the point. With 5 respect to this particular, I guess, element of the 6 claim, I have stated that the sequence of 7 instructions that is received from the thread 8 manager meets the -- is the -- the requirement of 9 the claim. 10 BY MR. RIZK: 11 Q Okay. An instruction is a type of command, 12 in your mind as a POSITA, correct? 13 A Yes, instruction would be a type of 14 command, correct, yes, sir. 15 Q Okay. Let me direct your attention to 16 Paragraph -- sorry, Page 26, Paragraph 73 of your 17 report. 18 A Yes, sir. 19 Q And at Paragraph 73, you -- that's part of 20 your technical overview of the '381 patent, correct? 21 A Yes, sir. 22 Q Okay. And there you talk about, in 23 Paragraph 73, the claimed engines, correct? 24 A Yes, among other things, I also discuss the 25 engines, plurality of virtual engines that are	31 1 Q Okay. Does each engine of the plurality 2 engines -- of engines have to be configured to load 3 state data associated with at least one task of the 4 plurality of tasks? 5 A No, sir, that's not my reading and that's 6 not what a POSITA would understand -- 7 Q Okay. 8 A -- from this description. 9 Q Okay. So how would a POSITA determine 10 whether a given component can be included within the 11 structure identified as a plurality of engines? 12 What -- what -- what is the attribute that 13 would make a -- a component an engine that would 14 qualify it to be included within the plurality of 15 engines? 16 A That's an excellent question. Thank you. 17 So as long as the plurality of engines as a 18 whole is able to receive from a scheduling module 19 associated with a second processing unit a set of 20 tasks -- tasks, and as long as this plurality of 21 engine is also capable of loading the state data 22 associated with each of these tasks, the -- the -- 23 the claim element has been satisfied. 24 There is no requirement here that each and 25 every one of the engines is capable of doing both
30 1 described in '381, which include a first background 2 engine 202-A; a second background engine 202-B; a 3 realtime low-latency engine 202-C; a primary 3D 4 engine, 202-D; and a low latency 3D engine, 202-E. 5 Q Okay. And in your mind, Doctor, as a -- 6 speaking as a POSITA, what is the function of the 7 claimed engine of the '381 patent? 8 MR. JOHNSON: Objection; form. 9 THE WITNESS: I'd like to refer to asserted 10 Claim 15 in responding to this question, which 11 clearly states that this plurality of engines is 12 configured to receive from a scheduling module 13 associated with a second processing unit a plurality 14 of tasks to load state data associated with issue of 15 the plurality of tasks. 16 So essentially what this is saying is that 17 this plurality of engines has two tasks to perform. 18 One is to receive a plurality of tasks from a 19 scheduling module, and to load state data associated 20 with these -- with each of these plurality of tasks. 21 Q Does each engine within the plurality of 22 engines have to be configured to receive a task of 23 the plurality of tasks? 24 A Not necessarily, no, sir. That's not my 25 reading.	32 1 tasks at the same time. In fact, I would like to 2 point out that the patent -- the -- the people who 3 drafted the patent, the patent owner, knew how to 4 word -- use the word "each" in the proper context; 5 so when they wanted to say each of the plurality of 6 tasks, they said it, but they never said a plurality 7 of engines each configured to receive this and each 8 able to load state data. 9 There is no such statement here; so 10 therefore, a POSITA would just look at this 11 and as -- including myself, and say the plurality of 12 engines as a whole should do it. 13 So going back to the basic question you 14 asked, which is, therefore, what qualifies an engine 15 to be part of the plurality of engines, it -- it 16 is -- the -- the -- the requirement is that it 17 should do either of these two tasks. 18 Either it's configured to receive a 19 plurality of tasks or it can do loading of the state 20 data on the -- but the plurality as a whole should 21 be able to perform both tasks. 22 Q So any one individual alleged engine within 23 the plurality of engines need not perform any of the 24 functions that are recited in the claims? 25 A No, sir. I didn't say that.

33 1 Q Okay. 2 A Absolutely not, no. 3 Q Well, so -- so let's focus -- I -- I -- I'm 4 not interested at this point about the plurality. 5 I'm only asking you about what is the meaning that 6 you ascribed to a singular engine. 7 As a person of ordinary skill in the art, 8 what meaning to you give to the term -- the 9 standalone term "engine" outside of the context of a 10 plurality of engines but within the context of 11 the -- the patent's teaching of what an engine is? 12 A So a plurality of -- so engines can perform 13 both tasks. We seem both to agree on that. 14 Now, an engine that can do either of these 15 two tasks or facilitate the -- the implementation or 16 execution of these tasks could be part of the 17 plurality of engines, so I could have an 18 intermediate block, functional block, or component 19 being -- being included in the plurality of engines 20 if it is facilitating other components in the 21 plurality of engines to perform these functions. 22 That's also possible, sir. 23 Q Okay. But I'm not asking you about the 24 plurality at this point. I'm just asking you about 25 the standalone term "engine."	35 1 MR. RIZK: I'll mark for identification 2 purposes Exhibit 3, which is a handwritten attempt 3 at me transcribing what I believe you believe an 4 engine is. 5 (Exhibit No. 3 was marked for 6 identification by the 7 videoconference technician; 8 attached hereto.) 9 BY MR. RIZK: 10 Q Do you have Exhibit 3 in front of you, sir? 11 A Yes, I do. I see -- 12 MR. JOHNSON: Wait, wait. Let me see it 13 before you go any further. 14 THE WITNESS: Sure, I'll let you; but it's 15 not what I've said because already some terms are 16 different -- 17 MR. RIZK: That's okay. I'll give you the 18 opportunity to correct it. 19 MR. JOHNSON: Objection; form. 20 MR. RIZK: And I -- I didn't -- this wasn't 21 intended to be a transcription -- a literal 22 transcript of what you said, Doctor, so my 23 apologies. I used best efforts to capture what I 24 believe you're saying. 25 Q So can you please correct Exhibit 3, using
34 1 A But I -- I answered it. I -- 2 Q What is -- what is -- can you provide a 3 definition of the term "engine" as a standalone term 4 as it is used in the '381 patent? 5 A First of all, based on my reading of the 6 specs, this is a virtual engine, so a -- a virtual 7 engine, in this case, is -- is -- is capable of 8 receiving a plurality of tasks or loading state data 9 associated with the plurality of tasks, or 10 facilitating other engines in the plurality to 11 perform either of these functions. 12 Q Okay. So if -- so you have an engine must, 13 Number 1, load and -- this is in the alternative -- 14 state data; Number 2, or receive at least one task; 15 or 3, facilitate 1 or 2 by another engine, correct? 16 MR. JOHNSON: Objection; form, 17 mischaracterizes testimony. 18 THE WITNESS: So an engine must, 1, load 19 the state data; or it should be configured to 20 receive from a scheduling module associated with the 21 second processing unit a plurality of tasks -- 22 tasks; or it should facilitate, enable, other 23 engines in the plurality to perform either of these 24 tasks. 25 That's what I've said.	36 1 the pen that is next to you, to correct what you 2 believe an engine to be? 3 A Sure, I can do that; but, again, there is a 4 transcript. I'm not sure what the point of this -- 5 this is. I mean, there is a transcript -- 6 Q I'm just -- yeah, that's okay. If you 7 don't mind correcting it because we're going to be 8 using that definition throughout the day, and I just 9 want to make sure we're clear on -- we're using -- 10 I'm using the right words, so if you can please just 11 make a correction -- 12 A Again, I will say it and you can make the 13 correction. I'm not going to write on this. It's 14 not my -- my -- my -- my writing. I'll -- I'll 15 state, and I'll be glad if you -- 16 Q Well, if you can tell me what needs to be 17 corrected -- 18 A Sure. 19 Q -- I'm happy to make the correction. 20 A Yes, I'll do that. 21 So the -- to load -- the part that says the 22 load state data should be load state data associated 23 with each of the plurality of tasks. 24 Q Okay. Could I see Exhibit 1? 25 A Exhibit --

37 1 Q I'm sorry. Exhibit 3. 2 A 3, yes. 3 So basically follow the language of the 4 claim, load state data associated with each of the 5 plurality of tasks. 6 Q Okay. I'm handing Exhibit 3 back to you. 7 And for the record, I've -- I've amended 8 Exhibit 3 using a red pen to include the correction 9 that you identified. 10 A Sure. 11 Q Do you see -- does that correct it 12 properly? 13 A That element, yes. 14 Q Okay. 15 A Second is -- it's not a second processor, 16 it's a second processing unit. 17 Q Okay. 18 A And then you say -- that's fine, yes -- 19 Q Okay. 20 A -- for now. But there is other 21 corrections. 22 Go ahead. 23 Q Could I see Exhibit 3? 24 A Yeah. 25 Q Do you see that I've handed Exhibit 3 back	39 1 Q Okay. And Exhibit 3 back to you, does that 2 look accurate to you? 3 A So with the caveat that you asked me to not 4 specify the claim requirements with respect to the 5 plurality of engines, but just focus on any one of 6 those engines, this is my view, yes. 7 Q Okay. Of what -- what a singular engine 8 is, correct? 9 A Is configured to do, yes. 10 Q You can keep Exhibit 3 with you. 11 A Sure. 12 Q Okay. And in reaching your opinion about 13 what a singular engine must be configured to do, did 14 you consult the specification of the '381 patent? 15 A Of course, yes. 16 Q Okay. And is there anywhere in the '381 17 patent that states that a singular engine must 18 perform one of those three functions that you 19 identified in the alternative? 20 A Not explicitly, no, sir; but -- but, again, 21 a person of skill in the art, including myself, who 22 has at least the qualifications of a skilled person 23 in the art at the time of the invention, my -- my 24 understanding, my reading, is that if you look at an 25 individual engine within the plurality of engines,
38 1 to you and I've corrected what I believe to be the 2 issue that you had with Number 2 in Exhibit 3? 3 Does that correct Number 2? 4 A Yes, sir. 5 Q Okay. 6 A And I would add to 3 facilitate or enable 7 another engine in the plurality of engines to 8 perform 1 or 2. 9 Q I'll take Exhibit 3 back. 10 Okay. I've handed Exhibit 3 back to you 11 and I've and notated Number 3 with what I believe to 12 be your correction. 13 Does that correct it? 14 A Yes. 15 The preamble, you say "must." I would use 16 the term here from the claim that says it's 17 configured -- 18 Q Okay. 19 A -- so -- and subject to that, I'm done, 20 yes. 21 Q Okay. Configured or configured to? 22 A No. 23 Configured to -- 24 Q Okay. 25 A -- correct, yes.	40 1 it should perform at least one of these three 2 functions, this, this, or this. 3 Q I'm just trying to understand where you got 4 that understanding from. There -- there is no 5 disclosed embodiment in the '381 patent where an 6 engine performs only one of those functions; agree 7 or disagree? 8 A Sure, but that's not the process as far as 9 I understand it. Correct me. You're a lawyer, so 10 you can tell me better; but the -- the -- the claim 11 is what it is, so the -- the -- the claim, as read 12 by me, understood by me or a person skilled in the 13 art, in view of the specs, certainly allows a -- an 14 engine to not perform all of the functions that are 15 required by the plurality of engines. 16 It -- it should just, in -- in combination 17 with other engines, perform that functionality. 18 That's the logical reading, interpretation of the 19 meaning of the claim element in view of the specs. 20 Q But that wasn't my question, sir. My 21 question isn't asking you to justify how you got to 22 your construction. 23 My question is, did you find in your review 24 of the '381 patent a single disclosed embodiment of 25 an engine in the spec that performed only one of the

41 1 three functions that you -- that are identified on 2 Exhibit 3? 3 MR. JOHNSON: Objection; form. 4 THE WITNESS: So in the -- the 5 embodiment -- I'd like to look at the '381 so 6 that -- 7 MR. RIZK: Sure. And that's Tab 2 of 8 Exhibit 2. 9 THE WITNESS: There is an embodiment in 10 Figure 2 that describes -- that corresponds to the 11 excerpt that I read to you before responding to your 12 question that shows these background engines, 13 realtime low-latency engines, and so on. 14 These engines are included in the command 15 processor code that runs on the command processor; 16 and these engines, in the context of this particular 17 embodiment, they work in the way that's described in 18 the patent, which is that they -- they -- they 19 perform -- their plurality, again, performs the -- 20 the -- the required functions here, which is to 21 receive a plurality of tasks and to load state data. 22 Your question is any one of them can do 23 both of these tasks in the context of Figure 2. 24 From the specs, that's what I recall, yes; but 25 that's just an embodiment.	43 1 it because the explicit disclosure is what is about 2 the plurality of engines. I'm responding to your 3 question, sir. 4 BY MR. RIZK: 5 Q Well, there is -- there is explicit 6 disclosure of embodiments of engines that perform 7 both functions of 1 and 2 of Exhibit 3, correct? 8 A Yes, in Figure 2, there are these virtual 9 engines, 202-A through E, that perform these 10 functions. 11 Q Okay. In fact, if we look at Tab 2 of 12 Exhibit 2, and I'll direct you to Column 4, Line 48, 13 I'll read the -- the first two sentences starting on 14 Line 46 of Column 4 into the record. 15 It says (reading): 16 In accordance with an 17 embodiment, a processing unit 18 includes a plurality of virtual 19 engines embodied on a single shader 20 core. 21 Each virtual engine is 22 configured to receive data parallel 23 processing tasks, e.g., graphics 24 processing tasks and general 25 compute tasks, and independently
42 1 MR. RIZK: No, I didn't ask you if anyone 2 of them can do both. 3 Q My -- my question to you was -- and I'll -- 4 I'll represent to you, and you can tell me if you 5 believe that I'm wrong, there is no disclosure in 6 the '381 patent of a -- an explicitly described 7 embodiment where an engine performs only one of the 8 three functions that are identified in -- in 9 Exhibit 3; right or wrong? 10 MR. JOHNSON: Objection; form. 11 THE WITNESS: There is no explicit 12 disclosure in '381 of a -- a -- the requirements on 13 a particular engine from around the plurality of 14 engines; but because there was no need for, I guess, 15 '381 authors to describe it in -- in that way, 16 they -- their focus was on the plurality of engines, 17 and their thinking was, and as long as the plurality 18 of engines can do this, the -- the -- the required 19 functions have been performed. 20 You asked me to go out of my way to explain 21 to you what would be the requirements not on a 22 plurality of engines, but on a single engine, and I 23 did that, and then you come back and say but there 24 is no explicit disclosure about that. 25 Yes, there is no explicit disclosure about	44 1 execute these tasks on the single 2 shader core. 3 Do you see that? 4 A Yes, sir, I do. 5 Q Okay. So -- so that's a disclosure of an 6 explicitly described embodiment where each engine 7 has to perform function Number 2 of Exhibit 3, 8 correct? 9 A Yes, but it's interesting that in the -- 10 that's why it's -- it's a haphazard exercise to try 11 to change the claim as you like because of something 12 that was said in the spec. What is claimed is what 13 matters in view of the specs. 14 We just have to understand what has been 15 claimed in view of the specs and nothing more. If 16 the authors decided to claim it this way, they get 17 all the privileges of that claim, but also 18 everything else that comes with it. 19 In this exact quote that you read to me, 20 they say each virtual engine is configured to 21 receive data parallel processing tasks, so data 22 parallel is not in the claim, so they're broadening 23 it that way. 24 And then they says and independently 25 execute these tasks on the single shader core, which

45 1 is not there, even. It's not in the claim. The 2 claim doesn't have that; and the claim has another 3 thing that says load state data associated with the 4 plurality of tasks, and this particular excerpt 5 doesn't have it. 6 So you can't just be selective, or we 7 cannot be selective, and say because that's -- it's 8 a statement here that we know doesn't even read on 9 the claim itself, and extends it in some ways, and 10 limits it in other ways, narrows it down and so on, 11 still that means the meaning of the claim is that. 12 No, that's not my reading. That would not 13 be a POSITA's reading either. 14 Q So do you believe that the excerpt I read 15 into the record, Column 4, Lines 46 through 51, is 16 within the scope of Claim 15? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: So within the scope means 19 that -- I'm trying to understand the meaning you 20 intend. 21 Maybe you can elaborate on that, what you 22 mean, within the scope means that it reads on the 23 claim? 24 MR. RIZK: That the claim reads on it. 25 That the claim is broad enough to encompass the	47 1 going to assume "and" here means "and/or," and then 2 I'm responding to you. 3 Q Do you generally understand "and" to mean 4 "and/or"; or as a person of ordinary skill in the 5 art, do you understand "and" to be in the 6 conjunctive? 7 A If it's "and" -- if it -- so if I -- I'll 8 answer it this way. If the "and" here is a 9 conjunction that is each virtual engine is 10 configured to receive data parallel processing tasks 11 and, conjunctively, independently execute these 12 tasks on the single shader core, it's certainly not 13 in the scope of this particular element of the 14 claim. 15 We are talking about this particular 16 element. We are looking at one element of the 17 claim. Then there is a discussion of the shader 18 core and all that, so I'm not answering the -- with 19 respect to the full claim; but respect to that 20 particular claim element that we're discussing, that 21 claim element then would not read on this sentence 22 as written with the conjunctive "and." 23 Q Would it read on Claim 15, the whole claim? 24 MR. JOHNSON: Objection; form. 25 THE WITNESS: Yes, I would say so, yes.
46 1 embodiment that's disclosed and described in 2 Column 4, Line 46 through 51. 3 MR. JOHNSON: Objection; form. 4 THE WITNESS: I mean, there is an "and 5 independently execute these tasks on a single shader 6 core." If I take the "and" to mean "and/or" -- 7 right? -- then yes, it is within the scope; but -- 8 "and," to me, is a logical "and," is a conjunction. 9 I understand sometimes in legal circles, "and" is 10 read as "and/or," so what do you want to take it, 11 and then I -- 12 MR. RIZK: I want to take it to be "and." 13 If it's what is stated -- 14 Q My question is if it is exactly what is 15 stated, Column 4, Line 46 through 51, is that within 16 the scope of 15 -- Claim 15 of the '381 patent? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: Again, with the 19 interpretation that it -- this "and" is "and/or," 20 then yes, it is within the scope. 21 MR. RIZK: I'm not asking you to interpret 22 it that way, sir. I've explicitly asked you not to 23 change anything. 24 THE WITNESS: But, sir, I'm responding to 25 you only in that way. I'm responding by saying I'm	48 1 BY MR. RIZK: 2 Q Now, in your report you have certain 3 materials that you -- you -- in preparing your 4 report, you considered certain materials, correct? 5 A Yes, sir, I did. 6 MR. JOHNSON: If you're switching gears, 7 we've been going a little over an hour. I'd like to 8 take a break. 9 MR. RIZK: Okay. Just give me a couple 10 minutes, and when I wrap up the line of questioning, 11 we'll take a break. 12 You identify your materials considered on 13 Page 6 of your report. 14 Q That's where you start identifying your -- 15 your materials considered? 16 A Page 6. 17 Q Yeah. 18 So Page -- Page 6, Paragraph 25, Doctor. 19 That's where you introduce -- you identify the 20 exhibit that has your materials considered? 21 A Yes, yes. 22 Q Okay. And then Tab 4 of Exhibit 2, which 23 is the exhibits that were attached to your report, 24 has your list of materials considered in preparing 25 your report, correct?

49 1 A Yes, sir, it does. 2 Q Okay. And these are the materials that you 3 considered in rendering your opinion, correct? 4 A Yes, this is the material that I have 5 explicitly considered; but as I've said before, 6 there is a lot more that goes on in terms of my 7 background and knowledge of the subject matter. 8 Q Okay. Did you -- you didn't identify the 9 expert report of Dr. Fister (phonetic) on your 10 materials considered list, correct? 11 A No, I did not. 12 Q Have you seen the expert report of 13 Dr. Fister? 14 A I've learned about it from the counsel -- 15 Q Okay. 16 A -- but I have not personally reviewed it, 17 no. 18 Q Okay. You understand that Dr. Fister is 19 respondent's noninfringement expert, one of 20 respondent's noninfringement experts, correct? 21 A Yes, sir. 22 Q Okay. And I'll represent to you that in 23 the expert report of Dr. Fister, Paragraph 180, 24 citing to the '381 patent, he states that, and I'll 25 quote, the specification describes the engines as	51 1 statement? 2 A It's not in the claim. Command buffer has 3 not been mentioned in the claim. 4 Again, you -- the -- the law is that -- if 5 I understand it correctly. I am, of course, a 6 technical guy, so -- so I may not be able to fully 7 accurately describe to you the -- the -- the 8 principles of law; but you get all the privileges 9 and benefits of claiming something; but if you 10 decided for any reason to broaden your claim scope 11 to not include command buffers, you cannot 12 implicitly read into it a command buffer that's 13 never been mentioned in any of the claims. 14 That's not how it works. 15 Q Okay. So it's -- 16 A Read between the -- I'm sorry. 17 Read between the black all the white space, 18 and that's what it means. 19 Q Okay. So you wouldn't look outside of the 20 claims to determine what an engine is? 21 A Of course I look at the specs. 22 MR. JOHNSON: Objection; form. 23 THE WITNESS: Sorry. 24 Of course I look at the spec. Of course I 25 look at the file history, I look at the claim
50 1 having a function to service command buffers. 2 Do you agree with that statement? 3 MR. JOHNSON: Objection; form. 4 THE WITNESS: I'm sorry, I don't know what 5 the context was in which he was speaking, what he 6 was asked, what he was saying, so I cannot confirm 7 or deny or anything related to that. 8 You can ask me a specific question about 9 command buffers and I'll answer it -- 10 MR. RIZK: Yeah. 11 THE WITNESS: -- but I cannot -- I don't 12 want to second -- 13 MR. RIZK: I'm not asking you to. I'm 14 actually just asking you to do exactly as you said, 15 Doctor. 16 THE WITNESS: Yeah. 17 BY MR. RIZK: 18 Q So my question to you is, do you agree with 19 me that an inherent function of an engine as 20 disclosed and described by the '381 patent is to 21 service a command buffer? 22 A No, sir, I do not. 23 MR. JOHNSON: Objection; form. 24 BY MR. RIZK: 25 Q And what is the basis of your last	52 1 constructions, I try to digest everything, and 2 that's what I have done, and it is not my 3 understanding in any way that the -- the claim, as 4 stated, requires a command buffer to be associated 5 with an engine, to provide data to the engine, to 6 receive data from the engine. 7 Nothing like that is there or described. 8 MR. RIZK: Okay. Well, in Exhibit 3, we've 9 identified three functions in the disjunctive; if 10 one of them exists within a component, you would 11 consider it to be an engine. 12 Q Would you consider a component to also be 13 an engine if it services a command buffer? 14 MR. JOHNSON: Objection; form. 15 THE WITNESS: I can't answer the question. 16 This is a hypothetical. I don't know what that 17 component is, where the command buffer lies, what 18 kind of connections it has to the other engines. I 19 cannot answer that question. 20 You give me the full set of information I 21 need, the block diagram, connections, functional 22 description, give me time to analyze it, I'll 23 deliberate on it, I'll give you an answer. I can't 24 answer that. 25 ///

53 1 BY MR. RIZK: 2 Q Well, you'd agree with me that the '381 3 patent identifies as a function of -- one of the 4 functions of the identified engines is to service a 5 command buffer? 6 A Where? Can you show me, please? 7 Q Have you -- did you not see that? 8 A Can you show me, please? 9 Q I'm asking you, in your review, did you 10 consider the '381 patent specification's disclosure 11 that an engine services a command buffer? 12 A Again, I read a lot of material, and I read 13 many of these things months ago. Right? So if you 14 have a specific question regarding parts of '381, 15 please point me to that. 16 It's not a -- a test of my memory or your 17 memory or anything. Right? Let's be precise, 18 right? Let's -- let's not have this kind of 19 haphazard sort of discussions. Tell me what portion 20 of the '381 you have in mind, I'll respond to you 21 precisely, sir. 22 Q You don't recall -- 23 A No, I do -- 24 Q -- considering that disclosure in -- in 25 your assessment of what an engine means, correct?	55 1 In a conventional system, an OS 2 scheduler would provide tasks 404 3 to a single command buffer in a 4 serial fashion and a conventional 5 GPU would serially process the 6 tasks. 7 Unlike such a conventional 8 system, OS scheduler 310 provides 9 each task 404 to one of a plurality 10 of command buffers 420-A through N 11 based on the priority type 12 specified by the applications 402. 13 For Example, OS scheduler 310 14 provides a first type of tasks, 15 e.g., high priority tasks, to a 16 first command buffer, a second type 17 of taskS, e.g. graphics processing 18 tasks, to a second command buffer 19 420-B, and so on. 20 GPU 110 includes a plurality of 21 virtual engines 432-A through N 22 each configured to service one of 23 command buffers 420-A through N. 24 Do you see that? 25 A Yes, sir, I do.
54 1 A No, I do recall. I do recall. 2 Q Okay. 3 A I just don't want to respond in this way to 4 questions to even not set the precedent. Show me 5 what part of my report you're referring to, show me 6 what part of -- or excerpt in '381 you have in mind 7 that supports your position, and I'll give you my 8 interpretation of that to the best of my ability. 9 Q Yeah, I'm just trying -- we'll get there, 10 sir. Okay? But before we do that, I want to 11 explore your -- what you actually considered in 12 providing your opinions. 13 So you did consider the '381 patent's 14 disclosure that a function of an engine is to 15 service a command buffer? 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: Again, I read the specs 18 carefully. I do recall discussions of the command 19 buffer; but I need to see the particular context you 20 have in mind before I respond to you, sir. 21 MR. RIZK: Okay. So let's look at 22 Column 10, and we can start with Lines 22 all the 23 way through 32. And I'll -- I'll just read it into 24 the record. 25 (Reading):	56 1 Q Okay. So why didn't you include this 2 function of servicing a command buffer as a function 3 that would indicate that a component is an engine? 4 MR. JOHNSON: Objection; form. 5 THE WITNESS: Figure 4 is one embodiment of 6 this invention. The top of Column 10 starts by 7 saying "For example, Figure 4 is an example of 8 workflow illustrating various layers of software and 9 hardware between one or more applications running on 10 a computing system, e.g., computing system 100, and 11 GPU 110 included in the computing system," and then 12 goes on to say the embodiment of Figure 4, there are 13 two types of processing units, CPU and GPU, so on 14 and so forth. 15 So, in fact, in the same sentence, it says 16 "For example, an example of workflow," and then 17 later on, it says it's just an embodiment. Right? 18 So the -- the claim stands by itself in view of the 19 specs I interpreted; but I do not limit it, narrow 20 it down, to any particular specs -- sorry -- any 21 particular -- I misspoke -- any particular 22 embodiment or example workflow described in the 23 specs. 24 I'm sure if I had done that and the other 25 side would have found it beneficial, they would have

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57 1 objected saying "You cannot do this. You cannot 2 narrow the scope of a claim based on one example of 3 workflow." 4 That's not what I -- I'm supposed to do, 5 that's not what a POSITA would do, and -- and I 6 think that's certainly incorrect for anyone to read 7 into that claim an additional requirement for either 8 the plurality of virtual engines as a whole or any 9 single one of them to service one of command buffers 10 or any command buffer. 11 MR. RIZK: Okay. But that's -- that's a 12 little bit different from my question, sir, because 13 you've drafted -- let's say the definition that 14 we're working with in Exhibit 3 of an engine is -- 15 has its requirements in the disjunctive. 16 Q Do you agree? 17 A Yes. 18 MR. JOHNSON: Objection; form. 19 BY MR. RIZK: 20 Q Okay. So why is it the case that if a 21 component services -- services a command buffer, 22 that you would consider it an engine in the -- in 23 the disjunctive, so it doesn't perform Items 1 24 through 3 in Exhibit 3, but it serves as a command 25 buffer?	59 1 Q Why isn't it the case that the fact that a 2 component services a command buffer, that it could 3 be considered to be an engine? 4 A Because command buffer -- 5 MR. JOHNSON: Objection; form. 6 THE WITNESS: Command buffer is not in the 7 language of any of the asserted claims. 8 BY MR. RIZK: 9 Q Okay. So you wouldn't look outside of the 10 language of the asserted claims to determine the 11 characteristic of a component that could make it an 12 engine, correct? 13 MR. JOHNSON: Objection; form. 14 THE WITNESS: I would not add to an 15 asserted claim a new limitation that will narrow the 16 scope of the claim for any reason. 17 MR. RIZK: Okay. 18 THE WITNESS: I would certainly consult the 19 specs to determine the meaning of the claim to 20 understand what the functionality of the plurality 21 of engines is, or even in response to a question 22 like "Tell me about the singular engine," provide my 23 understanding of what the functionality or 24 requirements of a singular engine are. 25 ///
58 1 Why wouldn't that be considered an engine? 2 MR. JOHNSON: Objection; form. 3 THE WITNESS: So I -- based -- I'm 4 responding to your question. I -- I came up with 5 this set of requirements for a single engine out of 6 the plurality of engines, but -- but this is 7 grounded in the language of the claim. I didn't 8 just make it up. Right? 9 I said loading the state data, receiving a 10 plurality of tasks, or helping with one of these 11 two, right? Facilitating, enabling. I -- I didn't 12 add to it; and at the same time, it should also 13 provide services of a certain type to the shader 14 core or receive its data from some other unspecified 15 in the language of the claim resource. 16 The basis for my definition of the engine 17 was the claim language itself. Command buffer is 18 not in the claim language. You cannot add it in 19 because you find it beneficial at this point to your 20 case that it should be. It's not there. 21 MR. RIZK: Yeah, I'm not -- I'm not -- a 22 little bit different, though, Doctor. You see, I'm 23 not asking you to add it as an additional 24 requirement in addition to 1, 2, or 3. I'm -- my 25 question is very simple.	60 1 BY MR. RIZK: 2 Q But to the extent that the -- the spec 3 describes functionality of a singular engine that is 4 not expressed by the claim, you would not include it 5 in the definition of the term "engine," correct? 6 MR. JOHNSON: Objection; form. 7 THE WITNESS: Of course I consider it. 8 I've thought about it, but I do not find it 9 plausible for anyone to add a new limitation to the 10 asserted claim based on one example of workflow in 11 the specs. 12 BY MR. RIZK: 13 Q Okay. But you'd agree that the spec is 14 distinguishing between conventional GPUs and 15 nonconventional GPUs in that disclosure that we read 16 into the record, correct? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: Yes, the -- the -- the -- the 19 specs in the excerpts that you read to me talks 20 about the conventional GPUs versus GPU 110, which is 21 the embodiment of Figure 4 of this '381, so I would 22 say they are trying to differentiate, but there 23 could be many other differentiations. 24 The point is what did they claim or what 25 they thought would be the inventive aspects of their

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61 1 invention that they wanted to include in the claim 2 language. 3 There could be many other things here that 4 differentiates GPU 110 from conventional -- 5 conventional systems. Many of them may not be 6 material or substantial or have much novelty. 7 It's just something that the authors felt 8 like they should state, but it was -- it did not go 9 through the assessment and critical analysis of the 10 USPTO. Maybe if they had included this, the claim 11 would not have been approved. 12 MR. RIZK: Okay. 13 THE WITNESS: It would have been rejected. 14 How would one know? So we cannot do this. This is 15 not allowed. 16 BY MR. RIZK: 17 Q Is servicing a command buffer a source of 18 facilitating a reception of tasks? 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: Ask -- it's not quite right, 21 the question, so is -- what's -- can you repeat the 22 question, please? 23 BY MR. RIZK: 24 Q Is the function of servicing a command 25 buffer a form of facilitating a reception of tasks?	63 1 BY MR. RIZK: 2 Q And -- and what is "them" in your answer? 3 A What is "them." 4 Command buffers. 5 Q So you would not consider command buffers 6 as a component that facilitates the performance of 7 the two functions, 1 and 2, on Exhibit 3? 8 MR. JOHNSON: Objection; form. 9 THE WITNESS: Again, in the embodiment of 10 Figure 4, they provide the function. That function 11 is provided to the operating system. Operating 12 system uses them as part of its own space to sort of 13 send commands and -- and what have you. 14 MR. RIZK: Yeah. 15 THE WITNESS: But -- but -- 16 BY MR. RIZK: 17 Q You're referring to the command buffers by 18 "them" again, right? 19 A Yes, yes, command buffers. 20 Q Okay. So my question is a little bit 21 different, though. 22 So if a component services a command 23 buffer -- I'm not asking you if a component is a 24 command buffer. 25 If a component services a command buffer,
62 1 MR. JOHNSON: Objection; form. 2 THE WITNESS: But we are not talking about 3 functions here. I mean, we are talking about 4 virtual engines, which are pieces of code that run 5 on the command processor that would provide tasks -- 6 a plurality of tasks that -- sorry -- that receive a 7 plurality of tasks and load state data, so whether 8 there is a command buffer on the operating system 9 side as an intervening component between the OS and 10 these virtual engines or not is irrelevant to the 11 function of the engine itself; and when I said 12 "facilitating," I was talk about facilitating the 13 performance of those two functions, receiving tasks 14 or loading the state data, and those things are not 15 part of the engines. 16 It is -- if anything, the command buffers 17 would be on the side of the operating system, and 18 operating system may or may not want to use them, 19 and -- and so I would not consider them to be part 20 of the engines, as I read the specs and understand 21 it; and I would not consider them, as such, to 22 facilitate the performance of these two functions by 23 the engines. 24 It helps the OS side, perhaps. 25 ///	64 1 does it satisfy Number 3 or any of the other numbers 2 on Exhibit 3? 3 A And what does "it" refer to? 4 Q The component. 5 If the component services a command buffer, 6 does that component satisfy any of the disjunctive 7 characteristics of an engine that are identified on 8 Exhibit 3? 9 A It can. 10 Q Okay. So -- 11 A It may. 12 Q So a component that only acts to service a 13 command buffer and nothing else, in your view as a 14 POSITA, can be an engine? 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: What does it mean to service 17 a command buffer? 18 BY MR. RIZK: 19 Q What do you understand that to mean? 20 A I'm not sure. Your question. 21 Q How does the '381 patent -- I'm using it in 22 the context of the -- of the disclosure in the '381 23 patent to service a command buffer; so however it's 24 used in the excerpt that I read into the record of 25 servicing a command buffer.

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65 1 If -- if a component services a command 2 buffer in the manner that is described in Column 10, 3 Line 33 to 34, and nothing else, would you consider 4 it to be an engine? 5 MR. JOHNSON: Objection; form. 6 THE WITNESS: So if -- if a component is 7 configured to service some command buffer in the 8 same context that the virtual engines of embodiment 9 of Figure 4 of '381 service their command buffers, 10 then yes; but if it's in a different context, no. 11 That's why I say maybe. If the -- the -- 12 the command buffer that you identify in some 13 product, or the engine that you -- or the component 14 that you identify in that product meet all the 15 contextual requirements of the same corresponding 16 component and command buffer, in that embodiment, 17 the answer is yes. Otherwise, no. 18 MR. RIZK: Okay. So that was a long 19 answer. I'm going to try to -- 20 THE WITNESS: Sure. 21 MR. RIZK: -- streamline it. 22 MR. JOHNSON: Adam, I have to have a break. 23 MR. RIZK: Okay. 24 MR. JOHNSON: We've been going over an hour 25 and a half. I asked 25 minutes ago for a break. I	67 1 give rise to a component being considered an engine 2 that it services a command buffer in the manner in 3 which is described in the embodiment of Figure 4? 4 A No, I do not. 5 Q Okay. And why is that? 6 A Because it's not in the claim language. As 7 simple as that. It has to be in the claim so 8 that -- or a basis in it in the claim for it so that 9 I can sort of even try to speculate that this would 10 be one of the required functions. 11 It's not there. The -- the term "command 12 buffer" is never to be found in the claims, asserted 13 claims, at least as far as I can see. 14 Q Okay. So if a component services a command 15 buffer in the manner in which is described of the 16 embodiment of Figure 4 of the '381 patent, and 17 nothing else, you would not consider it to be an 18 engine, correct? 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: Again, that's not what I 21 said. 22 I -- I -- I already agreed to you -- with 23 you that if there is a component that services a 24 command buffer in the manner that's described -- 25 that's described in the embodiment of Figure 4,
66 1 need to go to the -- 2 MR. RIZK: Let's take a break. 3 THE VIDEOGRAPHER: Please stand by. 4 We're going off the record. The time on 5 the video monitor is 9:52 a.m. 6 (A recess was taken from 9:53 a.m. 7 to 10:08 a.m.) 8 THE VIDEOGRAPHER: We are back on the 9 record. The time on the monitor is 10:08 a.m. 10 MR. RIZK: Welcome back, Doctor. 11 Just a quick housekeeping matter. I'm 12 joined also by a colleague of the firm of Mintz 13 Levin who is participating remotely in this 14 deposition, Michael McNamara, also representing the 15 complainants in this investigation. 16 So, Doctor, before the break, we were 17 talking about the possibility that a component that 18 services a command buffer in the manner in which is 19 described of Figure 4, that it could be considered 20 an engine as well. 21 Q Do you recall that? 22 A Yes, I do. 23 Q Okay. So would you agree with me that we 24 can amend the definition of "engine" in Exhibit 4 25 [sic] to include as a fourth possibility that could	68 1 exact same manner, same context, and so on, it -- it 2 can be considered to be an engine; but based on the 3 plain-language definition of the plurality of 4 engines and the functions they have to perform, if I 5 were to assign functionality to any individual 6 engine, I would certainly not add the servicing of a 7 command buffer as an option there because there is 8 no basis for it in the claim language itself. 9 MR. RIZK: Okay. I'm not asking you to add 10 it as an additional requirement. Perhaps that's 11 where there's a disconnect. The way you've defined 12 engine in your testimony today, you have -- 13 THE WITNESS: Disjunction. 14 MR. RIZK: You've done it disjunctively. 15 THE WITNESS: Yes. 16 BY MR. RIZK: 17 Q So my question to you is, if a component 18 services a command buffer in the manner in which is 19 described in the embodiment of Figure 4, and nothing 20 else, can it be considered an engine within the 21 scope of the claims? 22 MR. JOHNSON: Objection; form. 23 THE WITNESS: I've answered the question 24 previously saying yes. 25 ///

69 1 BY MR. RIZK: 2 Q Okay. So why can't we add that as a 3 disjunctive characteristic that would lead one to 4 determine that a component is an engine? 5 MR. JOHNSON: Objection; form. 6 THE WITNESS: That definition I provided 7 with respect to the claim language and trying to 8 decipher what the -- or determine what the specific 9 functionality of a singular engine out of the 10 plurality of engine -- engines is in response to 11 your question, so to me, if I were to add anything 12 that goes beyond the scope of the claim, I'm not 13 being truthful to the claim, so that's why I 14 hesitate to add a new requirement to the definition 15 of the functionality associated with the singular 16 engine in the context of that claim language itself. 17 MR. RIZK: Okay. Okay. I'll make it 18 simple, Doctor. Can I see Exhibit 3, please? 19 I'm going to add -- I'm going to amend 20 Exhibit 3, using a red pen, to add a Number 4 in the 21 disjunctive. 22 For the record, I have amended Exhibit 3 23 with a red pen to include as another disjunctive 24 characteristic of an engine, or Number 4, "Service a 25 command buffer in the manner and context described	71 1 MR. JOHNSON: Objection; form. 2 THE WITNESS: What I've said before is that 3 a component that services a command buffer in the 4 manner and context as the one that's been described 5 in Figure 4 embodiment of the '381 patent, this 6 component can serve as an engine; but what I do not 7 want to do is to add an additional disjunctive 8 clause for the functions associated with the engine, 9 singular engine, which is not supported in the claim 10 language itself. 11 That, I cannot say. 12 BY MR. RIZK: 13 Q So I -- I'm trying to understand if a 14 component meets -- meets Number 4 on Exhibit 3, but 15 doesn't meet Numbers 1 through 3, you don't consider 16 it to be an engine as claimed, correct? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: It is -- a component that 19 services a command buffer in the manner and context 20 described in Figure 4 would be in the scope of the 21 claim. 22 MR. RIZK: Okay. I'm -- I'm not going to 23 refer to the '381 spec anymore. At this point, I'm 24 just asking you about Exhibit 3. 25 Q A component that meets Number 4 in
70 1 in the embodiment of Figure 4 of the '381 patent." 2 I'm going to hand the exhibit back to the witness. 3 Q Do you have the -- Exhibit 3 in front of 4 you? 5 A Yes, sir. 6 Q Okay. Do you agree that if a component 7 meets any one of the four enumerated bullets that 8 are on Exhibit 3, that it could be considered an 9 engine? 10 MR. JOHNSON: Objection; form. 11 THE WITNESS: I've answered the question 12 before. The answer is no. 13 BY MR. RIZK: 14 Q Okay. And which one do you disagree with? 15 A I didn't -- I would not include 4 as a 16 disjunction -- disjunctive clause to the previous 17 three requirements because it's not supported in the 18 claim itself. 19 Q Okay. So just to be clear, if a component 20 services a command buffer in the manner and context 21 as that which is described in Figure 4 of the '381 22 patent, and does not meet any of the other 23 requirements of 1 to 3 as stated on Exhibit 3, you 24 would not consider it to be an engine as that term 25 is claimed, correct?	72 1 Exhibit 3 but doesn't meet 1 through 3 of Exhibit 3, 2 engine or not? 3 MR. JOHNSON: Objection; form. 4 THE WITNESS: It can be. I've never said 5 it cannot be. 6 BY MR. RIZK: 7 Q Okay. So where is the term "facilitate" in 8 the claim, Claim 15 of the '381 patent? 9 A It's not there. 10 Q Where did you get that term from? 11 A My understanding is a POSITA reading the 12 claim in view of the specs and in response to your 13 question. 14 It's not even in my report. I just 15 responded to your question because you asked it. 16 Q Okay. And I would submit to you that it's 17 not in the patent either, "facilitate." 18 Do you dispute that? 19 A I have not checked; but probably not, yes. 20 I have not checked. 21 Q And, in fact, there is no disclosure in the 22 claim of that if a component facilitates the receipt 23 of a task, that it would be considered an engine, 24 correct? 25 A The claim describes requirements for the

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73 1 plurality of engines. It never described the 2 functional requirements of a singular engine. 3 You asked me a question, I provided you 4 with my best answer. 5 Q Okay. 6 A And now you're saying "Why did you give me 7 an answer in the first place?" 8 Because you asked me. 9 Q Okay. 10 A That's -- 11 Q Well, that's the process today, that I ask 12 you questions and you give me answers. 13 A That's what I'm doing, sir. 14 Q So you would agree with me that Item 15 Number 3 in Exhibit 3 is not found in the claim 16 itself in terms of a singular definition of what 17 could constitutes an engine? 18 A It's not explicitly -- 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: It's not explicitly there; 21 but, again, a person reading the claims, in view of 22 the specs and the claim constructions and the file 23 history, as I've done, having deliberated about 24 this, if asked the question "Can you tell me what 25 the functions associated with a singular engine	75 1 to facilitate these other two capabilities, 2 functionalities, for the virtual engines could be 3 part of the plurality of the engines itself. 4 BY MR. RIZK: 5 Q When you say that there's no explicit 6 discussion of the functionality of any one engine, 7 you're referring to within the claims or within the 8 specification? 9 A Within the claims, sir. 10 Q Okay. So my question is about the 11 specification. 12 There is nowhere in the '381 patent 13 specification that says that if a component 14 facilitates or enables another engine in the 15 plurality of engines to load state data associated 16 with each of the plurality of tasks or to receive 17 from a scheduling module associated with a second 18 processing unit a plurality of tasks, that that 19 component could be considered an engine, correct? 20 A So it's not explicitly discussed, but it's 21 not excluded either. 22 Q Okay. 23 A It's a possibility. 24 Q So let me direct your attention to 25 Column 70 -- 7 of the '381 patent, Tab 2 of
74 1 are?" would understand it the way I described. 2 BY MR. RIZK: 3 Q Okay. But the claim, you agree, does not 4 define what the function of a singular engine are, 5 correct? 6 A Not explicitly, yes, sir. No, sir, 7 explicitly, it does not. 8 Q Okay. And the spec nowhere says that if a 9 component facilitates or enables another engine in 10 the plurality of engines to load state data 11 associated with each of the plurality of tasks or to 12 receive from a scheduling module associated with a 13 second processing unit a plurality of tasks, that 14 that component could be considered an engine, 15 correct? 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: There is no explicit 18 discussion of the functionality of any one engine. 19 It's always a discussion about functionality of the 20 plurality of the engines as being claimed in the 21 asserted claims of the '381; and in view of the 22 asserted claims and my understanding of the specs 23 and the file history and the claim construction, I 24 believe it would be understood by a POSITA, 25 including myself, that a component whose function is	76 1 Exhibit 2. 2 Do you have that in front of you? 3 A Column 77? 4 Q Yes, Column 7, you can go to Line 50 -- you 5 can start on Line 25, really. 6 Sorry. I take that back. You can start on 7 Line 34. 8 Do you have that in front of you, Column 7, 9 Line 34? 10 A Yes, sir. 11 Q Okay. And -- and there it talks about -- 12 I'll read the first sentence into the record. It 13 says (reading): 14 Graphics preprocessing logic 15 includes vertex analyzer 208 and 16 stand converter 212. Tasks from 17 primary 3D engine 202 and 18 low-latency 3D engine 202-B are 19 sent to the graphics preprocessing 20 logic. 21 Do you see that sentence? 22 A Yes, sir, I do. 23 Q Okay. Would you agree with me that the 24 preprocessing logic can be considered to be part of 25 the plurality of engines?

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77 1 MR. JOHNSON: Objection; form. 2 THE WITNESS: In the -- in the context of 3 the embodiment of Figure 2, the inventors are very 4 clear what the engines are. It's not for me to add 5 a new engine. I mean, they have described them to 6 be 202-A through 202-E. 7 That's their definition of what the engines 8 are, these virtual engines are, and I have no reason 9 to add anything to it. 10 BY MR. RIZK: 11 Q I'm asking you to -- to tell me, leaving 12 aside that it's -- these -- these devices are not 13 called engines, which I agree with you, that they're 14 not called engines, would you, as a person of 15 ordinary skill in the art, given your definition and 16 understanding of what an engine is -- would you 17 consider preprocessing logic to be an engine? 18 MR. JOHNSON: Objection; form. 19 THE WITNESS: Why would I want to do that? 20 I mean already these other virtual engines have 21 performed the associated functionality. I mean, a 22 person skilled in the art would not assume that 23 possible would be wasteful of their silic- -- 24 valuable silicon resources to add duplicative 25 functionality.	79 1 analyzer receives it, scan converter receives the 2 tasks. Of course, arbitration logic receives it. 3 Of course, the shader cores must receive it; and so 4 all of them are engines. 5 No. I mean no, that's not the -- the way 6 these things work, right? 7 Q Okay. 8 A So every component has its unique -- 9 specific functionality. Once that functionality is 10 performed, other components that come after will 11 also receive the task to process it, but it doesn't 12 mean they're engines. 13 Q So if we look at the embodiment that is 14 disclosed in Figure 2 of the '381 patent, there are 15 one, two, three, four, five different engines that 16 are explicitly identified as engines as part of the 17 plurality of engines, correct? 18 A Yes, sir. 19 Q Okay. And the functionality of receiving a 20 plurality of tasks and loading the state data is 21 implemented by only two of those engines? 22 A First of all, you're -- you're sort of 23 dropping an important part of the claim language. 24 Right? So they have to receive the plurality of 25 tasks from a scheduling module associated with a
78 1 The functionality that's required by this 2 command, this -- this GPU, including the command 3 processor and the shader core and all that -- that 4 functionality associated with the engines has 5 already been met by 202-A through E, so it would be 6 duplicative, redundant, in some ways foolish to add 7 that functionality into some other component when 8 it's already being performed. 9 BY MR. RIZK: 10 Q So you would agree with me that a component 11 that receives a plurality of tasks is not 12 necessarily an engine, correct? 13 MR. JOHNSON: Objection; form. 14 THE WITNESS: With respect to the claim, 15 the plurality of engines have to perform certain 16 functionality, and once that functionality is 17 performed by those engines, if some other block 18 somewhere else receive a set of tasks -- because, of 19 course, the task that comes in to the plurality of 20 engines has to be passed down to get to the shader 21 core to be executed and acted on, so, obviously, 22 intrinsically, in fact, it's necessary for the tasks 23 that were coming in to continue to go through the 24 rest of graphics pipeline, and you can go and, 25 therefore, with this definition, say, well, vertex	80 1 second processing unit. So don't forget about that. 2 It's not just receiving tasks, it has to 3 receive the tasks from the scheduling module; so any 4 other component that you claim that might or might 5 not serve as a virtual engine -- virtual engine -- 6 first of all, it has to be virtual, also -- has to 7 meet these additional requirements, right? Which is 8 in my claim. 9 In -- in Exhibit 3, we did say that 10 scheduling -- they have to receive these tasks from 11 a scheduling module associated with a second 12 processing unit. 13 Q Yeah. 14 And each of the engines that are shown in 15 the command processor 230 perform both of those 16 functions, 1 and 2, in Exhibit 3, correct? 17 A In -- in Figure 2 embodiment of 18 Exhibit 3 -- 19 Q I'm sorry. You're -- you're on exhibit -- 20 you're on Exhibit 2 right now, and you're on 21 Figure 2 of Tab 2 of Exhibit 2, just for clarity of 22 the record. 23 A That's correct, yes, sir. 24 Q Go ahead. 25 A Thank you. Thank you.

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81 1 So -- 2 Q So do you want me to repeat my question for 3 you, Doctor? 4 A No, no. 5 Q My question is each one -- with reference 6 to Figure 2, which appears in Tab 2 of Exhibit 2, 7 each one of the engines that are depicted, 202-A 8 through 202-E, implement Functions 1 and 2 as those 9 functions are stated on Exhibit 3, which is the 10 piece of paper that you have sitting next to you? 11 A That is correct, yes, sir. 12 Q Okay. So we don't need 202-C through 202-E 13 because 202-A and 202-B by themselves carry out both 14 of the functions that are required of the plurality 15 of engines, correct? 16 A I -- I wouldn't say that because, again, 17 the claim is not just one element of the claim. I 18 mean, you have to look at the -- the full claim, 19 right? 20 So the full claim has a preamble, the first 21 element, the second element, the third element; so 22 these engines that have been identified should sort 23 of fit in the scope of the claim and -- and all the 24 other requirements that precede and -- or -- or 25 succeed it, so in -- in that way, for example, let's	83 1 engines, say background engine A and B, maybe even 2 realtime low-latency engine, those three engines by 3 themselves, do they meet the requirement of this 4 independent claim. 5 Is that your question, sir? 6 Q No, that's not my question. 7 A Please ask the question. 8 Q And I'd appreciate it if you can -- I'm 9 going to try to keep my questions shorter, and I'd 10 appreciate it if you can try to keep your answers 11 shorter and -- and stay on track with what my 12 question is. 13 A Sure. 14 So -- 15 Q So let me -- let me reask -- 16 A Let me say also this. I'd -- I'd like to 17 respond. 18 So if -- if your question is a -- compound 19 questions with many things at work, right? -- so to 20 make sure there is no misunderstanding between you 21 and me, what you ask me is what I understand, and I 22 properly respond, I have to go through the details 23 and tell you what my understanding of the question 24 is before I respond. 25 Q Yeah, I'd like you to --
82 1 look at the claim language itself -- right? -- for 2 the '381. 3 I have to look for it unless you can direct 4 me to it. 5 So let's look at Claim -- Independent 6 Claim 15 of '381 is a computer processing system 7 that has a memory, a first processing unit, a bus 8 coupled to the memory in the first processing unit; 9 and then this first processing unit comprises a 10 plurality of engines but also a shader core. 11 We have been discussing the plurality of 12 engines at length now, but the shader core itself is 13 configured to receive the plurality of tasks from at 14 least one of these engines and to execute a first 15 task from the first plurality of tasks while 16 executing a second task from the plurality of the 17 tasks based on the respective state data associated 18 with each of the first and second tasks. 19 So whatever you describe as a plurality of 20 engines has to fit in that full scope. Your -- your 21 question is can I arbitrarily go and drop the 3D 22 engine and the low-latency engine that go through 23 the FIFOs and the vertex analyzer and the scan 24 converter and the arbitration logic and get to the 25 shader core, do they satisfy; then the remaining	84 1 A You don't want to get -- you don't want to 2 get answers to questions that you never asked, 3 right? Like the one -- 4 Q Yeah, I didn't -- I -- the answer that you 5 provided had nothing to do with my question, but 6 we'll move on. I'll withdraw the question. 7 A All right. 8 Q All right? I'll make it simple for you. 9 In your earlier testimony, you said that 10 the preprocessing logic cannot be considered an 11 engine even though it receives a plurality of tasks, 12 correct? Yes or no? 13 MR. JOHNSON: Objection; form. 14 THE WITNESS: The preprocessing logic 15 refers to vertex analyzer 208 and scan converter 212 16 in Embodiment 2 -- 4 of Figure 2? 17 Is that -- 18 MR. RIZK: It's the preprocessing logic 19 that we discussed in your -- in the earlier 20 testimony about a few minutes ago. 21 THE WITNESS: Just making sure that's what 22 you mean still. 23 All right. So it's not being described 24 that way in the patent, no? 25 ///

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85 1 BY MR. RIZK: 2 Q You wouldn't -- you wouldn't -- even though 3 it's -- you agree with me preprocessing logic 4 receives a plurality of tasks, yes? 5 A Yes. 6 Q Okay. But you disagree that a person of 7 ordinary skill in the art would consider 8 preprocessing logic to be an engine, correct? 9 MR. JOHNSON: Objection; form. 10 THE WITNESS: The preprocessing logic has 11 to receive a plurality of tasks from a scheduling 12 module associated with the second processing unit. 13 MR. RIZK: Okay. 14 THE WITNESS: So the background engines 15 202-A and other engines up to 22 -- 202-E receive 16 the tasks from the scheduling module; vertex 17 analyzer receives these tasks from the engines. 18 So vertex analyzer, scan converter, they do 19 receive tasks, but they don't receive it from the 20 scheduling module, they receive it from the engines. 21 BY MR. RIZK: 22 Q And why can't they just be considered 23 another engine? 24 A Because they receive it from the engines. 25 Q But it receives a task; so you're saying	87 1 analyzer, scan converter, arbitration logic, and 2 eventually the shader core, and then goes to be 3 written out. 4 I would not, in the context of this 5 embodiment or my understanding of the claim 6 language, consider the vertex analyzer or scan 7 converter to be the engine, according to this 8 embodiment. 9 Q What -- what is the attribute of an engine 10 that is -- that is missing from vertex analyzer that 11 disqualifies it from -- from being an engine? 12 MR. JOHNSON: Objection; form. 13 THE WITNESS: At least two. 14 One, it's not virtual; two, it's not 15 receiving it from the scheduling module. The 16 function has already been performed. 17 You're trying to associate a duplicative 18 function to a component in the system, and no person 19 of -- skilled in the art, no one that understands 20 the cost associated with building chips or -- or -- 21 or providing functionality and services to systems 22 that make use of this chip would understand that 23 this duplicative functionality would be implemented 24 in practice. 25 It's just nonsensical to do it. If I
86 1 that if a component receives a task, that's not 2 enough to make it an engine? 3 A It has to -- 4 MR. JOHNSON: Objection; form. 5 THE WITNESS: It -- it -- it -- it has to 6 receive it from a second -- I'm sorry -- from a 7 scheduling module associated with a second 8 processing unit; otherwise, with that definition, 9 almost anything, any hardware, software component 10 that -- that exists in this system, including shader 11 core itself, and arbitration logic, would be 12 considered an engine because they receive tasks, 13 right? 14 MR. RIZK: Okay. 15 THE WITNESS: According to your definition. 16 So -- 17 BY MR. RIZK: 18 Q Don't you agree that -- that these 19 components, the preprocessing logic receives tasks 20 indirectly from a scheduling module? 21 A The tasks that are received by the virtual 22 engines -- virtual engines are also -- the important 23 part is "virtual," so -- are -- and state data being 24 added to them, loaded, provided, that full 25 combination now gets passed down to the vertex	88 1 already have the function, why would I want to 2 repeat that same function again? I wouldn't do it. 3 It's done. The engines already have done what they 4 needed to do. 5 I have the -- the data, the task received; 6 I've loaded the state data that I need to it, I've 7 created this package. I'm sending it to the vertex 8 analyzer, which is a hardware component, whereas 9 these engines are virtual, software, as far as my 10 understanding would be, although I -- I know the 11 claim construction from the Court, so -- so, yeah, 12 it doesn't work like that. 13 BY MR. RIZK: 14 Q Okay. And when you were applying your -- 15 when you provided the definition that you provided 16 to me today which is reflected in Exhibit 3 of a 17 singular engine, did you apply the -- a virtual 18 requirement? 19 A No, I -- 20 MR. JOHNSON: Objection; form. 21 THE WITNESS: So for the purpose of the -- 22 understanding the meaning of the claim and defining 23 the scope of the claim, of course I abide by the 24 construction of the ALJ. 25 MR. RIZK: Okay. I'm not asking you --

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89 1 THE WITNESS: Yeah -- 2 MR. RIZK: I'm not asking you -- 3 THE WITNESS: -- so I'm applying that 4 construction; so therefore, in my definition I 5 provided to you, configured to do this, this, this, 6 and that, or -- or that, I -- I did not apply 7 anything else other than the ALJ's construction. 8 MR. RIZK: Okay. So throughout today, I -- 9 I understand that you had disagree with the 10 Administrative Law Judge that the engines don't need 11 to be virtual engines, and you also disagree with 12 the Administrative Law Judge that the engines can be 13 implemented in hardware. 14 Am I -- am I right? 15 A My view is -- 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: Yeah, my view is that if you 18 look at the -- and I've talked about this in my 19 report, so we can go to the corresponding 20 paragraphs. 21 So my -- my view is that the -- the virtual 22 engines, as has been disclosed in the specification, 23 is a software-only implementation; but the judge, 24 ALJ, has construed it otherwise. 25 I go with that construction. I don't	91 1 Q Do I understand correctly? 2 A Not only that. This -- this duplicative 3 functionality argument is an important one, in my 4 view, because whenever you apply a principle and 5 then at the end it becomes ridiculous, you should 6 give up on that principle, right? 7 So if I take the view that any component, 8 whether it's hardware or software, that receives a 9 task can be included either directly or indirectly, 10 as you have said, as long as I'm coupling to it 11 somehow indirectly, it's receiving the task -- 12 right? -- according to what you have posed to me, 13 then everything that you see in Figure 2 embodiment, 14 every component here you see -- right? -- perhaps 15 with the exception of the memory system, would be an 16 engine. 17 Again, that's a ridiculous position to take 18 for anyone. No POSITA would assume that's the 19 meaning of an engine. You could say it; but, again, 20 it's not a matter of what you say, it's a matter of 21 what a POSITA would understand at the time of the 22 invention; and no one would assume it because there 23 is a separate element related to the shader core. 24 According to your definition, shader core 25 would be also an engine. Why not?
90 1 question it, I accept it; and then on the basis of 2 that construction, then I have some arguments that 3 says now this is indefinite because there is not -- 4 there is not disclosure for -- to a person skilled 5 in the art to be able to practice the full scope of 6 the claim. 7 MR. RIZK: Okay. 8 THE WITNESS: But that's a different 9 discussion perhaps we'll get to later. 10 MR. RIZK: We'll talk about the 11 indefiniteness later; but for the purposes of my 12 question -- questioning today, unless I'm asking you 13 about your indefiniteness opinion with respect to 14 virtual, I'm -- I'm asking you to apply the Court's 15 construction. 16 THE WITNESS: Correct, sir. 17 MR. RIZK: So -- so I'm not interested in 18 your opinions, at this point, about why you believe 19 that the engines need to be software, need to be 20 virtual. 21 So the only reason that you've provided 22 that is within the -- the way the Court has 23 constructed engines, that preprocessing logic isn't 24 an engine, is that it doesn't receive the tasks from 25 a scheduling logic.	92 1 Q Okay. So -- so I suppose, though, that 2 you're assuming that the engines that are in the 3 plurality of engines load all of the state data 4 associated with the tasks? Or do they -- they only 5 required to load some of the state data associated 6 with the task? 7 A I don't recall. 8 Again, please point me to part of the '381 9 if otherwise is true. I do not recall that there 10 was -- there was any statement in '381 that all of 11 the state data has to be received within -- by the 12 engines. 13 Q Okay. So if the -- if the preprocessing 14 logic loads some state data that wasn't already 15 loaded by the plurality of engines, you would 16 consider the preprocessing logic in that 17 circumstance to be an engine? 18 MR. JOHNSON: Objection; form. 19 THE WITNESS: I mean, I'm going back to the 20 claim language. So it says this plurality of 21 engines are configured to receive tasks, but also to 22 load the state data associated with each of the 23 plurality of tasks. 24 It is not saying that it should be the full 25 state data or -- I mean, a person skilled in the art

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93 1 could read it one way or the other. I think it's 2 hard for me, based on this, and even in view of the 3 specs, to say that the plurality of engines have to 4 receive what you call the full state data, which I 5 don't know what it is, even. 6 It is -- by the way, what is a full state 7 data? When you say complete, full state data, what 8 does that mean. 9 MR. RIZK: State data, I think the spec 10 provides examples of state data as like a texture 11 handle. That's an example, and there are other 12 examples that are provided in the spec. 13 So let's suppose the plurality of engines 14 load the texture handles but don't load some other 15 constant that the spec identifies as state data; and 16 then the preprocessing logic loads another piece of 17 state data. 18 Q Would you consider the preprocessing logic 19 to be an engine? 20 A But, I mean, in that sense, then the shader 21 core probably also will load some state data, 22 because the -- the shader core needs to know where 23 to read the data from and where to write it to, if 24 there are some intermediate results, so it has to 25 have some information about where to at least write	95 1 can tell you the meaning of my -- my definition of a 2 singular engine would apply to background -- to -- 3 to engines 202-A to 202-E, but not to the other 4 components that -- that -- that are here because 5 otherwise, it just becomes ridiculous. 6 Q Well, what -- how do we define "engine," 7 then, to -- because the definition that's on 8 Exhibit 3 doesn't exclude, I think you stated the 9 shader core is going to load some state data. 10 A Potentially. 11 Again, I don't know, and I -- I don't 12 recall. 13 Q Okay. 14 A Otherwise -- 15 Q Well, that was your testimony, sir. You -- 16 you said -- 17 A First of all, I can correct my testimony, 18 right? But -- but that's not what I'm doing. I'm 19 just clarifying it, right? 20 So I'm just saying that I don't recall 21 that -- if any state data is being loaded by the 22 vertex analyzer, and -- I don't recall it, actually. 23 Shader core, I don't recall being described 24 explicitly; but it is possible that there is some 25 state information that's being used by these things.
94 1 any intermediate results. 2 So, again, it's one of those hypotheticals 3 that you are presenting to me today which, if I 4 apply it, almost anything then could satisfy the 5 requirement of an engine. 6 Q Well, I agree with you. I happen to agree 7 with you about that, Doctor; and that's what I'm 8 trying to get to. I'm trying to understand what is 9 the meaning that we give to the term "engine"; and I 10 think that both you and I are in agreement that if 11 you apply the -- the definition that's on Exhibit 3 12 of meeting any one of those requirements, that 13 wouldn't work because then everything would be an 14 engine, correct? 15 A I guess the answer here is that you asked 16 me a question about what the functionality of a 17 singular engine is, whereas the claim language 18 itself only describes the functionality of a 19 plurality of engines. 20 I provided you with my best response 21 regarding what a singular engine has to do, but you 22 have to be careful when you apply it so that it does 23 not turn into something that applies to -- to 24 everything. 25 So in -- in the context of Embodiment 2, I	96 1 I just don't -- 2 Q Yeah. So -- 3 A -- don't know. 4 Q -- my question to you is how do we then -- 5 assuming the -- the likely possibility that there's 6 some state data loaded by the shader core that's not 7 loaded by the engines associated with the task, how 8 do we distinguish between an engine and a shader 9 core? 10 What is the distinguishing feature of a 11 shader core that makes it not an engine at this 12 point? 13 A Shader core does processing. It does -- 14 it's the workhorse of the GPU. It does processing. 15 The -- the virtual engines do not do any -- 16 do not do processing in terms of pixel shading or 17 vertex shading or graphics processing-type 18 operations; so the main differentiation there would 19 be that, right? That the shader core receives the 20 tasks. 21 Of course it has to receive the tasks. 22 Maybe it does receive some local state data. I'm 23 not sure. But certainly it does a lot more. Its 24 main functionality in the scope of the invention is 25 to do the actual processing of the graphics tasks.

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97 1 Q So the component that does actual 2 processing of the tasks, you would not consider to 3 be an engine? 4 MR. JOHNSON: Objection; form. 5 THE WITNESS: Let's put it this way. I 6 like where you're going, so I'm going to try to 7 agree with what you're saying, but let me modify it. 8 So a component such as shader core that 9 does the processing of graphics shading tasks, 10 whether vertex or pixel or fragment or what have 11 you, or does, for example, scan conversion, which 12 is -- right? -- part of the graphics processing task 13 itself, is part of the fixed pipeline that people 14 usually use, or -- or -- or even the vertex and 15 analyzer that does some kind of graphics processing 16 to prepare the verticis that are going to be 17 provided to the actual shader core, and so on -- so 18 they are doing graphics processing tasks either -- 19 so well-defined tasks on the received computational 20 tasks, on the received instruction streams -- I'm 21 sorry -- on the -- that's -- on the received data -- 22 right? -- I would not consider them to be part of 23 the engines -- the -- the -- the -- the virtual 24 engines as claimed here. 25 So the virtual engines might do some	99 1 graphics processing on the task, correct? 2 MR. JOHNSON: Objection; form. 3 THE WITNESS: One, it does not receive the 4 tasks from the scheduling module associated with the 5 second processing unit. You say but indirectly, 6 they get there. That's nothing I've -- it's not 7 what I've stated in my definition of engine; but 8 that's what you said; and yes, it indirectly 9 receives the task, but that's -- to -- to me, that's 10 not good enough. 11 And then you -- you come back and say 12 but -- so therefore, this -- this must be considered 13 an engine; and I would say if a POSITA is looking at 14 Figure 2 embodiment, would not say vertex analyzer 15 is the engine because vertex analyzer performs a 16 very specific graphics processing function. 17 It's part of the graphics processing 18 pipeline as described in this patent. I mean, so if 19 you look at the way we get to the preprocessing 20 logic -- let -- let me actually point it out, where 21 it is that talks about graphics. 22 MR. RIZK: I'll take your word for it, 23 Doctor. We've got to -- we need to -- I think that 24 you've -- you've answered the question that I have 25 pending.
98 1 transformations, some local processing themselves, 2 some preparation; but they are not doing vertex 3 shading, they are not doing pixel shading, they are 4 not -- as such, right? 5 So they are not doing ALU computations in 6 terms of calculating new coordinates, 7 transformations in space, and so on, so -- 8 BY MR. RIZK: 9 Q Okay. So in the context of the -- just to 10 be clear, I think you had said earlier that the 11 vertex analyzer, which is part of the preprocessing 12 logic we've been talking about, that's -- you 13 understand that to be a hardware component, right? 14 A Yes, vertex analyzer is a hardware 15 component. 16 Q So I think it's your testimony that a 17 person of ordinary skill in the art would not 18 understand a hardware engine to be a component that 19 performs processing -- graphics processing on the 20 task. 21 A I never used the term "hardware engine." 22 Do you want to modify your question? 23 Q Yeah. 24 So -- so you wouldn't consider the vertex 25 analyzer to be an engine because it performs	100 1 So I have -- I do have a follow-up question 2 for you. 3 Q Do you agree or disagree that a hardware 4 engine in the context of a GPU must perform graphics 5 processing on the task? 6 MR. JOHNSON: Objection; form. 7 THE WITNESS: No, I did not say that. 8 BY MR. RIZK: 9 Q So do you disagree with that statement? 10 MR. JOHNSON: Objection; form. 11 MR. RIZK: I'm not saying that you said it, 12 sir. I'm -- I -- this is a new question. 13 Q Agree or disagree, a hardware engine in the 14 context of a GPU, to qualify as a hardware engine, 15 it must perform graphics processing on the task? 16 A I'm sorry. Hardware -- 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: Hardware engine is not in the 19 claim, it's not in the specification. It's a term 20 you just made -- made up. 21 What is a hardware engine? Can you -- 22 MR. RIZK: You tell me. You're -- you're 23 the person of ordinary skill -- 24 THE WITNESS: Sorry, I can't know what -- 25 what you have in your mind.

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101 1 BY MR. RIZK: 2 Q So you wouldn't understand would a person 3 of ordinary skill in the art understand, in the 4 context of graphics processing units, that an engine 5 implemented in hardware must necessarily perform 6 graphics processing? 7 A As far as Claim 15 is concerned, right? 8 Because -- 9 Q As -- as far as a person of ordinary skill 10 in the art and what they would understand a 11 hardware-based engine to be generally. 12 MR. JOHNSON: Objection to form. 13 THE WITNESS: As far as '381 is concerned? 14 MR. RIZK: As far as '381 is concerned, 15 sure. 16 MR. JOHNSON: Objection to form. 17 THE WITNESS: So as far as '381 patent is 18 concerned, there is a disclosure of these engines, 19 virtual engines; and the question you're asking me 20 is that these virtual engines being part of the -- 21 running on the command processor, or at least shown 22 here to be part of the command processor block 23 diagram -- these engines, there is no required 24 functionality for them to perform graphics 25 processing.	103 1 many different things to many different people, 2 depending on what the system is that you're talking 3 about. 4 It's like saying processing element, what 5 is a processing element? It depends how you define 6 it. What is an engine? It depends how you define 7 it. It could be -- engine could be a simple ALU, 8 could be the whole GPU, could be a portion of the 9 GPU, could be one of the lanes that's been 10 parallelized. 11 I mean, so many different things, so there 12 is no clear answer here, and not because I'm trying 13 to avoid your question, just honestly, truthfully, 14 there is absolutely no such common understanding of 15 what an engine is at any time, even today. Forget 16 for 2009. 17 Q Let's stay in 2009. 18 A Yeah, in 2009. 19 Q So in 2009, just this summarize, you would 20 agree with me that a person of ordinary skill in the 21 art would not understand the -- the phrase "engine" 22 in the context of GPU hardware to necessarily be 23 limited to a component that performs graphics 24 processing? 25 A An engine could be part of the graphics
102 1 I mean, the requirements are what's there, 2 right? I mean, the plurality of engines configured 3 to receive a plurality of tasks and to load state 4 data associated with the plurality of tasks. 5 MR. RIZK: Okay. 6 THE WITNESS: These are the requirements. 7 MR. RIZK: I'm going to change the question 8 on you. Now let's -- we were talking about -- you 9 gave me the answer in the context of the '381 10 patent. 11 THE WITNESS: Yes. 12 BY MR. RIZK: 13 Q In the context of the field of graphics 14 processing at the time of the invention of the '381 15 patent, generally, and that -- I will provide a date 16 of September 3rd, 2009, or prior -- in that 17 timeframe, would a person of ordinary skill in the 18 art understand the term "engine" in the context of 19 GPU hardware to connote a component that performs 20 graphics processing on tasks? 21 A There is no standard meaning or definition 22 associated with an engine in the context of GPUs or 23 CPUs or anything. 24 I mean, "engine" is one of those -- almost 25 like nunc (phonetic) words, right? It can mean	104 1 processing unit, some part, could be the whole 2 graphics processing unit if the person is meaning it 3 that way. 4 No -- normally people looking at engines, 5 unless it's otherwise defined -- which is the case 6 in the '381 patent, it's otherwise defined. Unless 7 it's otherwise specifically defined, we'd assume 8 it's doing some kind of computation within the 9 overall system; but what kind of computation it does 10 depends on the system, depends on the context. 11 Q It could just be doing something as simple 12 as handling or facilitating data flow without 13 performing any computation? 14 MR. JOHNSON: Objection; form. 15 THE WITNESS: Probably not. 16 Again, if you think about an engine -- it's 17 like your -- your car's engine, right? So it's -- 18 it's doing some work for you. It's not just there 19 for you to change, I don't know, the -- the 20 air-conditioning level so that you feel more 21 comfortable as a driver sitting in the car. 22 It's actually -- the engine of the car is 23 doing something. Now, what -- what I'm saying to 24 you is that a person skilled in the art, when you 25 tell them an engine in the context of GPU, he or she

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105 1 would probably know it's doing some kind of 2 computational work; but exactly what that 3 computational work is, what's the granularity, 4 what's the amount, what's the scope, what kind of 5 inputs it receives, what kind of outputs it 6 provides, it's an all unknown, undefined to him at 7 that point. 8 Give him a system, he can tell you, but -- 9 or her; but otherwise, it's very hard to sort of 10 limit and define precisely what an engine is. 11 But -- but -- but if -- if your statement 12 was that outside '381, somebody hearing the term 13 engine, would it assume it to be some -- something 14 that facilitates data transfer, probably not. 15 Probably not. 16 Would it assume that it's something that 17 does some amount of processing? Probably yes. Is 18 it universally applicable? Probably not, no; but 19 I'm sure you find sort of instances where dominance 20 of the instances in -- is that an engine typically 21 would require some kind of computational work to be 22 done. 23 BY MR. RIZK: 24 Q Okay. But then going back to the context 25 of the '381, you would understand that the engine	107 1 Q Okay. And then if we go back to 2 Paragraph 109, which is -- that starts on Page 43, 3 that's where you start talking about the at least 4 one memory device element, 1-A, in your report 5 for -- in -- in view of Studdard, right? 6 A Yes. 7 Q Okay. And I think we had previously 8 established that you identify the cache unit 1024 as 9 the at least one memory device, correct? 10 A I'm sorry. I'd like to see the '053 11 patent. I have it in front of me, and I think 12 that's Exhibit 1. 13 Q Yeah, the '053 patent is Exhibit 1, yes. 14 A And give me a minute, please. I'd like to 15 look at the claims, also have them in front of me. 16 Q The claims? 17 A The asserted claims of the '053. 18 Q Okay. And I can orient you. It's in 19 Exhibit 2. 20 Let me just -- 21 A Yeah, please. 22 Q Okay. Do you see you have the claims in 23 front of you now? 24 A All right. Very good. 25 MR. JOHNSON: It feels like we're switching
106 1 that is disclosed there does not perform 2 computational work? 3 A Yes, in the context of the Figure 2 4 embodiment, in the context of the asserted claims, 5 that is my understanding. That's why I say it's 6 otherwise defined. 7 Q Let's turn back to your report; and we can 8 go to Page 33, starting on Paragraph 84 of your 9 report. That's Exhibit 1. 10 Do you see that? 11 And from Pages 33 all the way through 12 pages -- Page 41, I'm talking specifically about 13 Paragraphs 84 through 104. 14 That's where you -- you provide a -- a 15 brief overview of various references that you 16 considered in your analysis of the '053 patent, 17 correct? 18 A Yes, sir, that's right. 19 Q Okay. And then I think we said earlier 20 that your opinion on invalidity based upon 21 obviousness of -- in view of Studdard is 22 Paragraphs 105 through 113 on Pages 42 through 46, 23 and then it continues with Paragraphs 117 all the 24 way through 134 on Page 54 of your report, correct? 25 A Correct, yes, sir.	108 1 away from engines and into something else. We've 2 been going a little over an hour. Can we take a 3 break? 4 MR. RIZK: Sure. 5 THE VIDEOGRAPHER: Please stand by. 6 We are going off the record. The time on 7 the video monitor is 11:11 a.m. 8 (A recess was taken from 11:11 a.m. 9 to 11:24 a.m.) 10 THE VIDEOGRAPHER: We are back on the 11 record. The time on the video monitor is 11:24 a.m. 12 MR. RIZK: Welcome back, sir. 13 Q Did you confer with anybody about your 14 testimony during the break? 15 A No, sir, I did not. 16 Q And I -- I -- I think that you have been -- 17 I didn't ask you some setup questions in the very 18 beginning of your deposition. 19 You've been -- this isn't your first 20 deposition, correct? 21 A No, it's not. 22 Q Okay. You -- you know the general rules, 23 it -- so it appears, correct? 24 A Yes, yes, I do. 25 Q Okay. All right. You understand that

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109 1 you're -- you're under oath today, correct? 2 A Sure, yes, sir. 3 Q Okay. So, Doctor, just before we start 4 talking about the '053, it just occurred to me -- 5 you still have Exhibit 3 next to you, right? That's 6 the piece of paper -- the sheet of paper with the -- 7 A Yes. 8 Q -- definition of "engine" -- 9 A Yes. 10 Q -- singular engine that we've been working 11 with? 12 A Yes, sir. 13 Q And I think you disagree with Item 14 Number 4, that that could be a, you know, standalone 15 definition of "engine," right? 16 A In the -- in the -- in the context of the 17 claim, yes. 18 Q Okay. So let's -- can you cross out -- 19 just cross out Number 4 since you don't agree? 20 A I don't want to touch this paper. You can 21 cross it for me. 22 Q Okay. Is -- is there a reason why you're 23 hesitant to -- I just -- 24 A I just don't like this kind of thing, I 25 mean, that I -- I write on a piece of paper, and so	111 1 a car. 2 No. It has to be an engine in the first 3 place; and then it loads the state data, it receives 4 from the scheduling module associated with the 5 second processing unit a plurality of tasks or 6 facilitate another engine in the parallel -- in the 7 plurality of engines to perform 1 or 2. 8 That's really the intention, the meaning 9 that I have intended to convey to you. 10 Q Okay. So what makes a component an engine 11 in the first place? 12 A Again, that's -- it's not well-defined, or 13 at least explicitly defined in the claim, certainly, 14 but also in the specs, the embodiments, and so on, 15 so -- but my view is that a POSITA looking at the 16 claim and the specification would understand an 17 engine to have some amount of computational 18 capability to do some processing. 19 It's not going to finish the graphics 20 processing tasks that are going through it; but it 21 might do some kind of processing, maybe transform -- 22 transforms data, certainly loads the state data and 23 associates it with the tasks going through; but it 24 can do some amount of processing on the tasks or 25 data associated with the tasks that goes through it
110 1 on. It's your writing, you started it, that's your 2 initiative, you felt it was necessary. 3 Q Okay. I will cross out Number 4 -- 4 A Go ahead. 5 Q -- and I think that we'll refer back to 6 this with that cross-out that I put on Exhibit 3 on 7 Item Number 4. 8 You -- 9 A Yeah, I mean, one thing I want to say now 10 that you brought this up again is that when I 11 defined the functions of a singular engine in the 12 first place in the context of the claim, one thing 13 that should be clear, that an engine should be a 14 engine anyway, right? 15 So these are like this engine is doing 16 these things, right? It doesn't mean that if you do 17 these things only, then you qualify as an engine. 18 That -- that's not what I have in mind. 19 If that's your reading, that's -- that's -- 20 I want to correct that. That's not correct. So, 21 for example, if you look at -- I say my car has four 22 wheels and is blue, and that's part of my 23 requirement for some -- some -- some -- some -- some 24 claim I have, you -- you cannot say the -- my -- my 25 suitcase, which is also blue and has four wheels, is	112 1 before it passes it onto the graphics pipeline below 2 it. 3 My intention was not to exclude that 4 possibility. 5 Q Okay. So what is the minimum amount of 6 processing that an engine must perform on a task to 7 qualify as an engine? 8 MR. JOHNSON: Objection; form. 9 THE WITNESS: I can't respond to this 10 question because it's hard to specify a threshold 11 below which you are not an engine, above which is an 12 engine. Not because I'm trying to avoid it, but 13 it's just -- I don't think that's the right metric 14 that one should use, that, well, if I do this much 15 work, I'm an engine, if I don't, then I'm not. 16 I mean, I -- I think it's enough to say it 17 has -- it can do some amount of processing on the 18 tasks or the data associated with tasks going 19 through this set of engines, load state data and -- 20 and so on; but exactly what that is, I can't say. 21 MR. RIZK: Well, I -- I'm trying to 22 understand your -- your earlier testimony that you 23 don't want me to think that merely if a component 24 meets any one of the three clauses on Exhibit 3, 25 that it would necessarily constitute an engine, and

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113 1 that it, as a threshold matter, would have to be 2 considered an engine, and then on top of that, meet 3 one of -- at least one of the three clauses. 4 I think that's generally what you -- what 5 you've testified. 6 Q Am I -- am I misstating your testimony? 7 So beyond the -- the three clauses that are 8 in Exhibit 3, what type of processing must a 9 component perform in order to be considered an 10 engine? 11 A I cannot answer the question in terms of 12 what type of processing it must perform. It could 13 be many different systems, many different 14 arrangements of different components within the 15 systems; and therefore, depending on what the system 16 requirements are and what the partitioning of the 17 functionality was across different components, and 18 so on, you -- you -- an engine may do different 19 processing not only in terms of the type of 20 processing but also in terms of the amount of 21 processing. 22 But I can think of examples of the kind of 23 processing that, potentially, an engine could do, 24 potentially, would be, maybe, state -- sorry -- 25 the -- the tasks come in and then the -- the tasks	115 1 way, maybe it does it some other way. But the point 2 here, the key point, the important point, is 3 because -- if -- if there is a component that does 4 1, 2, and 3, or 3, that component may have nothing 5 to do with being an engine because it's not an 6 engine. It's just something else, right? 7 So it has to be an engine; and then that 8 engine has to satisfy these things, right? It must 9 be configured to do loading of the state data, 10 receiving the tasks, or facilitating. 11 Q Well, it has to do some processing plus one 12 of 1, 2, or 3 in Exhibit 3? 13 A Well, it has to be an engine, and an engine 14 typically will do -- can do -- again, maybe an 15 engine -- it's like when we talk about functions, 16 right? So a function could be a -- an identity 17 function. 18 Nobody says an identity function is not a 19 function. It's still a function, right? So take 20 the input and pass it on, for example. Usually 21 that's not what we mean by "function," so -- usually 22 function does something useful. 23 And that's what I'm saying. Engines should 24 do some kind of processing. Whether they do it all 25 the time -- if it's a useful engine, it does some
114 1 could get, maybe, translated from a -- one form to 2 another form, maybe -- even potentially -- you know, 3 I don't know. 4 It's not in the specs, and you're trying -- 5 you're asking me to hypothesize and speculate what 6 these kind of processing -- 7 Q Well, you've added this new requirement -- 8 A -- would be. 9 I'm sorry. Let me finish. 10 So maybe one example would be you take a 11 complex command within the instruction -- the 12 command stream and replace it with two or three 13 simpler commands. Maybe you take a -- maybe the 14 data that comes in is in one form and you slightly 15 modify the form or you apply some kind of filtering 16 to eliminate some of the data, corson (phonetic) the 17 data. 18 I mean, I don't know. I mean, it's -- many 19 different possibilities are there for an engine to 20 do some kind of processing as it encounters -- 21 receives these tasks and passes them forward; and my 22 examples are not meant to be comprehensive, they are 23 not even meant to be, necessarily, what an engine is 24 supposed to do or can do. 25 It's just maybe. Maybe it does it this	116 1 processing. 2 Q Okay. And that processing would have to be 3 in addition to 1, 2, and 3 of Exhibit 3? 4 MR. JOHNSON: Objection; form. 5 THE WITNESS: The way I've written this -- 6 I didn't write it, you write it; but I said it. 7 The way I said was that in the context of 8 Claim 15 of the '381, and then in response to your 9 question about what would be the function of these 10 engines, these are the functions of the engines. 11 I just don't want you to -- you or anyone 12 else to have an understanding that any component 13 that meets these -- one of these three is an engine 14 because it may not be an engine in the first place. 15 BY MR. RIZK: 16 Q So what else would it need to -- what else 17 would it need to have? Today is -- today is the day 18 for you to provide to me and to provide to the Court 19 what your definition is of the term "engine." 20 Do you understand that? 21 A Yes. 22 Q Okay. So we've been going over this same 23 concept for a while now. It doesn't seem to be that 24 you have a clear definition in your mind of what a 25 singular engine is in the context of the '381

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1 patent. 2 I recognize that this is a complex subject, 3 what an engine is in the context of the '381 patent; 4 but it sounds like you don't agree that an engine 5 would -- would be a component that satisfies any one 6 of the three clauses on Exhibit 3, and it requires 7 something else. 8 And my question to you is, what is your 9 definition of "engine" in addition to satisfying one 10 of the three clauses in Exhibit 3? What -- what 11 else would -- would -- would need to be included in 12 a component for it to be considered an engine by 13 you? 14 A So first of all, there is no requirement to 15 describe the functionality or characteristics of an 16 individual engine when the claim itself talks about 17 plurality of engines. 18 But you asked me the question about the 19 engine; and I responded to that question by saying 20 that in the context of this claim, the engine should 21 satisfy one of these three requirements, as far as I 22 can see; and then you're asking me now what is an 23 engine, and I'm telling you I've said it before. 24 You're asking me to say it again. I'll oblige. 25 An engine is a piece of -- let's go with	117 119 1 it, you -- you don't think that's sufficient -- 2 Q Let's -- let's stick -- let's stick to the 3 question, Doctor. So please stick to answering my 4 questions. I understand that -- we don't need to 5 have this back-and-forth where -- where you're going 6 on -- 7 A That's what I'm doing. 8 Q -- for -- for minutes about me not liking 9 your answers. 10 I'm just asking questions, and I'd ask that 11 you provide an answer directed toward answering my 12 question. 13 A That's what I've done. 14 Q Okay. So with respect to the processing 15 capability, going back to the '381 patent, Figure 2, 16 this additional requirement that you've now added 17 for "engine," you would agree that the preprocessing 18 logic has processing capability? 19 A Yes, it does. 20 Q Okay. So -- and the preprocessing logic 21 performs graphics processing. 22 Can graphics processing capability -- would 23 that satisfy the processing capability requirement 24 of an engine or no? 25 THE STENOGRAPHER: Can you repeat the end
118 1 the Court construction, with a piece of hardware or 2 software or a combination thereof that can perform 3 these functionality, or one of them; but at the same 4 time, it must be an engine and it -- a POSITA would 5 understand an engine to have certain other 6 capabilities, including some processing capability, 7 and therefore, potentially, do some processing of 8 the data that's going through it. 9 You're asking me what is that processing 10 capability. I gave you some examples and I said 11 these are not examples that are comprehensive or -- 12 or -- or necessarily what the engines in the context 13 of '381 -- or -- or -- or some other context that 14 I'm not aware of are doing; but it could be some 15 kind of processing capability. 16 You are asking me for a particular 17 threshold; and I told you it's hard for me or for 18 anyone, as far as I can see, to give you that 19 threshold. This has now all become hypothetical, 20 right? 21 "So hypothetically, if there is this engine 22 that is doing this, tell me what the threshold is 23 for it to qualify." 24 I'm doing my best, I'm giving you my 25 answers. You don't like the answers, I understand	120 1 of your question, please? "Would that satisfy 2 the --" 3 BY MR. RIZK: 4 Q Does -- does graphics processing capability 5 of the preprocessing logic satisfy the processing 6 capability requirement of your definition of engine? 7 MR. JOHNSON: Objection; form. 8 THE WITNESS: So as long as the -- the -- I 9 don't see any reason that an engine would do 10 duplicative work that's already been done by the 11 graphics pipeline itself. 12 All I'm provisioning or allowing is that 13 this -- these engines do some kind of processing, 14 and I can't tell you for sure what the threshold is 15 or even what the type of processing is. 16 I just think it's possible, as part of the 17 being an engine, to do some amount of processing and 18 some type of processing; and in the context of the 19 claim, the embodiment of Figure 2 of the '381, I do 20 not consider the preprocessing logic to be an 21 engine. 22 There are engines already in the system. 23 The engines take the tasks, they add loads -- 24 they -- they add state data to it, they pass it on 25 to this other component, and then it does some other

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121 1 processing. 2 To me the concept of engines in that 3 embodiment is very well-defined. It's there, the -- 4 the inventors say it. I have no reason to want to 5 modify their -- their -- their -- their 6 characterization. 7 Your point here is that the way I've 8 described it here in response to your request that I 9 try to define exactly what the -- not only 10 functional requirements, but now you're asking what 11 the characteristics of this -- attributes of this -- 12 these engines are. 13 I -- that's what I have said, and I cannot 14 add more to it at this point. That's my testimony 15 today. 16 MR. RIZK: And part of the problem is that 17 you, in preparing your opinion, did not endeavor to 18 define the term "engine" as a singular term. 19 THE WITNESS: It was not necessary, sir. 20 BY MR. RIZK: 21 Q So in your -- rendering your opinion, you 22 did not endeavor to give a meaning to the term 23 "engine" as that term is used as a singular term 24 within the '381 patent? 25 A Again, I -- I have an understanding.	123 1 not asking you if it's excluded. 2 I'm asking you did you -- are you relying 3 on any disclosure in the specification for your 4 opinion that an engine has processing capability? 5 A It's running on a command processor; so if 6 it's running on a command processor or, if I go with 7 the ALJ's construction, it's part of a command 8 processor -- right? -- it's doing some kind of 9 processing. 10 Otherwise, why -- why would it run there or 11 why would be -- why would it be part of a command 12 processor? I think the -- the -- the -- the proof 13 is in the pudding, right? I mean, so look at 14 Figure 2 embodiment. 15 It is included as part of the command 16 processor -- processor. What does a command 17 processor do if it's not processing also? 18 Q Okay. Well, you can have a component; you 19 could have, for example, a -- I'll give you -- I'll 20 give you a quick example. 21 A Please do. 22 Q You could have a power management circuit 23 that is part of a microprocessor that isn't 24 providing processing capability. 25 A Absolutely wrong, sir. I've -- I've
122 1 That's why I'm giving you this, right? So -- so I'm 2 giving you my understanding of that; but I did not 3 articulate it, I did not write it in my report. It 4 was unnecessary to do it. 5 And I believe what I've said about engine 6 is -- is correct; that in the context of the claim, 7 an engine is an engine, has some kind of processing 8 capability, and it does these -- one of these other 9 functions. 10 Q Where does it say in the claim that an 11 engine has processing capability? 12 A An engine has an engine. 13 Q No, no. I'm not asking you your 14 definition. You're giving me your person of 15 ordinary skill definition of engine. 16 I'm asking you does the claim say engine 17 has processing capability? Is that a limitation in 18 the claim, that is stated in the claim, has 19 processing capability? 20 A No, sir, it's not explicitly stated -- 21 Q Okay. 22 A -- in the claim, but it's understood. 23 Q Is it stated anywhere in the specification? 24 A It's not excluded either. 25 Q Is it -- that's not my question, sir. I'm	124 1 written power management tools and designed 2 hardware. This is absolutely -- absolutely false. 3 Any kind of power management scheme has 4 some processing capability also. It needs to look 5 at the sensor data that comes in, it needs to 6 make -- make predictions about what the temperature 7 would be or what the power consumption is going to 8 be; it needs to get loading from -- workload 9 information; it needs to make projections about what 10 the workload would look like; it will have to do 11 comparisons. 12 I mean definitely a power management unit 13 is a complicated circuit that has usually embedded 14 processors or state machines and ALUs and this and 15 that to perform its functionality. You are -- you 16 are incorrect, sir. 17 Q You're providing an example of a more 18 sophisticated power management system. I'm thinking 19 of a power management component in a microprocessor 20 that provides a fixed power supply voltage. 21 Is there such a thing? 22 A That's not called power management, it's 23 called a power source. 24 Q Okay. 25 A A power source.

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125 1 Q A microprocessor can have a power source, 2 right? 3 A But it's not -- but it's not going to be 4 called a power management. 5 MR. RIZK: Okay. Let's call it power 6 source. 7 (Mr. Rizk and the witness speak 8 simultaneously.) 9 THE STENOGRAPHER: One at a time please. 10 BY MR. RIZK: 11 Q True or false, a microprocessor can contain 12 a power source? 13 A Yes, it can contain a power source. 14 Q Okay. And does the power source, 15 standalone fixed power source, provide processing 16 capability? 17 A No, it does not. 18 Q Okay. 19 A It's a power source. 20 Q So a component of a processor does not 21 necessarily provide processing capability, correct? 22 A If you mean the power and ground 23 connections to a processor, you're right. 24 If you mean any other component that I can 25 think of in a normal processor, fetch decode,	127 1 included in a processor that don't provide 2 processing capability? 3 A Depends what you mean also by "processing 4 capability." If processing means take input data 5 and transform it in some way to create new data, no, 6 they do not produce new data. Their whole function 7 for those kinds of memory is to store data and allow 8 you to retrieve it. 9 Q Okay. And -- and the way that you've been 10 using processing capability as imparting meaning to 11 the term engine, do those -- does the processing 12 capability as you've used that term or phrase today 13 require taking data and transforming it in some way 14 to create new data? 15 A Not only data, but also instructions, 16 potentially. 17 Again, I don't know. I really don't -- 18 don't want to limit the scope of what that 19 processing is. I'm just saying some kind of 20 processing is happening. Maybe it's some -- some 21 kind of data processing, maybe some kind of 22 microcode generation, or what have you. 23 I -- it could be something, right? Some -- 24 some kind of processing that -- that -- that affects 25 the tasks, the threads going through.
126 1 execution, write-back, even memory, all of those 2 have well-defined functions that they perform, 3 right? So you -- you -- you are going with the 4 extreme case of, yeah, there's a power source. 5 Of course, VDD is at, say, 1.5 volts, and 6 ground is at 0 volts, and there's no processing. 7 Yeah, okay, fine. But, of course -- but if you do 8 power gating, it's not true. 9 But, anyway -- so I think that's not a good 10 example, sir. 11 Q Okay. And does a memory provide processing 12 capability if a processor contains memory that 13 provides processing capabilities? 14 A Some memories do, absolutely. 15 There is the whole area of in-memory 16 computing or near-memory computing in which you 17 actually do computations inside the memory. 18 I'm not saying all memories are like this; 19 but you cannot say memory doesn't do computation. 20 Q Okay. So there's -- are there -- 21 A There's a whole -- there's a whole field 22 of -- 23 Q Are there -- 24 A -- engineering that does that. 25 Q Are there some forms of memory that can be	128 1 Q Okay. And take that -- I want you to keep 2 in mind the definition that you've just applied for 3 "processing capability" that you're imparting to the 4 meaning of engine. 5 Do you have that in your mind, whatever it 6 is you're -- however it is you're using that phrase? 7 A Yes, sir. 8 Q Okay. Is there some form of memory that 9 could be included in a processor that doesn't have 10 that type of processing capability? 11 A Yes. 12 Q Okay. And so the fact that that memory is 13 contained within a processor unit does not 14 necessarily mean that it has the processing 15 capability that you have in mind for engine, 16 correct? 17 A Except that it's not going to be called an 18 engine, it's going to be called memory. Nobody 19 calls a memory an engine. If you call something an 20 engine, it is an engine. It does something. 21 That's what a POSITA would understand. You 22 can't call apple an orange and assume that you're 23 going to have the -- the -- the taste of an orange 24 when you're eating an apple, right? So it's -- 25 different terms have been used.

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129 1 Again, you are talking about the knowledge 2 of a POSITA, their understanding. If the -- the 3 inventors meant these components to be something as 4 passive as the kind of memory that you have in mind, 5 they would have not called it "engine." They called 6 it "engine," right? 7 Q Okay. And what do the -- what -- where is 8 the disclosure in the spec that says that the 9 engines transform the -- the tasks? 10 A I mean, again, I said it -- you are asking 11 me a repeat question. Fine. 12 Q Please just answer the question, sir. 13 A I'll be glad to oblige. Yes, I'm doing 14 that. 15 These engines are part of a command 16 processor. Command processor is known to do 17 processing; so therefore, these engines involve some 18 amount of processing. 19 Q Can you point me to any other disclosure or 20 is that all you have? 21 A That's enough. 22 Q Okay. So that's your testimony? 23 A Yes, sir. 24 Q Okay. Let me direct your attention to 25 Figure 4 of the '381 patent.	131 1 boundary around the GPU and arbitrarily extend it to 2 command buffer -- and why not extend it to the OS 3 scheduler? Because, probably, you don't find it 4 useful -- and then you under that, redrawing of-- 5 of the embodiment that's described here, answer this 6 hypothetical question whether a command buffer 7 included inside the virtual engine -- I'm sorry -- 8 the GPU would be considered to be a -- a -- a -- an 9 engine when we have other engines which are included 10 clearly here as part of the command processing unit. 11 If you were to tell me that this command 12 buffer is part of the internal register file of that 13 command processor, then maybe; but if the command 14 buffer is something totally -- maybe meaning in the 15 sense that, yeah, it's, maybe, included, therefore, 16 it's part of the virtual engine, so I would say the 17 virtual engine 432 with the command buffer 18 integrated into the command processor acting as 19 supporting for the virtual engine is, therefore, 20 part of that virtual engine together combined, 21 maybe; but otherwise if it's a separate thing inside 22 the GPU but also outside the command processor, no, 23 sir. 24 Q You would not consider it -- if it's 25 outside of the command processor, you would not
130 1 A Yes, sir. 2 Q Okay. Now, do you see that the tasks 3 404-A, 404-B, 404-C, 404-D are received by the 4 command buffers 420-A -- I think there's a typo, it 5 should be 420-B, but it's 402-B, and 420-N? 6 A Yes, sir, I see. 7 Q Okay. And would you consider the command 8 buffers to be engines? 9 A I've answered the question before. 10 No, I do not. 11 Q Why not? 12 A Can we look at the claim language again? 13 These command engines are part of the first 14 processing unit, and the first -- so therefore, 15 those command buffers have to be part of the first 16 processing unit. 17 Q Okay. So if the -- if the command buffer 18 was included within the bounds of the GPU, but was 19 otherwise structured as described in -- as described 20 and disclosed by the '381 patent, would you agree 21 that a person of ordinary skill in the art would -- 22 could consider each of the command buffers to be an 23 engine? 24 A It's a hypothetical. So you're asking me 25 now to go and change the specification, change the	132 1 consider the command buffers to be part -- to -- to 2 be -- to be engines, correct? 3 A If the command buffer was included in GPU 4 as a separate hardware, I guess you mean, or 5 software? 6 Do you know what that is? 7 Q Hardware. 8 A Hardware. 9 So there is a separate hardware unit that's 10 outside the command processor and that feeds into 11 that virtual engine which is implemented on the 12 command processor; and you would say that command 13 buffer, is it by itself yet another command -- 14 virtual engine? 15 Is that the question? 16 Q If it's an engine. I'm not asking about 17 virtual engines. 18 A In that case, I -- I might say that 19 there's -- the combination -- again, in response to 20 that hypothetical -- and I really have to deliberate 21 on this more; so I'll give you an answer, but it's 22 just -- this is a hypothetical, so I'm only 23 responding to it on the fly because you're asking me 24 to do -- to do it, and -- the command buffer, then I 25 would probably -- if -- if it was me, I would

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133 1 draw -- draw a box around the virtual engine and 2 that command buffer and say -- the current virtual 3 engine, right? 4 MR. RIZK: I'm not asking you -- 5 (Mr. Rizk and the witness speak 6 simultaneously.) 7 MR. RIZK: I'm not asking you to combine 8 them. 9 THE WITNESS: No, I'm not. 10 BY MR. RIZK: 11 Q I'm asking you if the command buffers can 12 constitute separate engines is, each command buffer 13 can constitute a singular engine under the 14 definition that you've been applying of engine, if 15 it's included within the GPU but not included in the 16 command processor. 17 That's what I'm asking you. 18 A I -- I don't -- I can't answer that 19 hypothetical. You could take different views. 20 Depends on how you define it. 21 It -- that command buffer by itself doesn't 22 have any kind of processing capability, so I 23 normally -- I -- I tend to say no because it's just 24 a buffer, does nothing else other than that, so by 25 itself, it cannot be, in my view, as I stand here	135 1 command buffer to be, by itself, a virtual engine. 2 Also, it doesn't perform any kind of 3 processing whatsoever. It's just a pipe. Data goes 4 through the pipe; so I would not, in that way, 5 consider it to be an independent command -- engine, 6 but in combination with some other components, such 7 as virtual engine 432, when it's combined with 8 integrated command buffer 420-A, then yeah, that 9 combination would constitute a -- a single engine. 10 Q Yeah, I'm not asking about the combination. 11 I'm only focused -- 12 A Well, you asked. 13 Q No, I never asked you about the 14 combination. 15 I'm only asking you about whether an 16 individual command buffer could be considered an 17 individual engine if it is included within the 18 command processor. That is the only question I've 19 ever asked you. 20 A Yeah. 21 Q But let's -- so let's it's with my 22 question. 23 A Yes; and my answer to that is that a 24 command buffer that's integrated in the RT level 25 description of the command processor as a resource
134 1 today -- be an independent virtual engine, but it 2 can be part of a virtual engine if it's included the 3 way you describe it inside the GPU, but -- but even 4 preferably as part of the command processor. 5 Yeah, in the context of this patent and the 6 embodiments of this patent, the virtual engine must 7 be implemented on the command processor. 8 Q Okay. 9 A Analysis what I see. 10 Q Okay. Well, let's say that the command 11 buffer is included, structured exactly as described, 12 but it's included within the RTL module called 13 command processor. 14 Do you understand the -- 15 A Yes. 16 Q -- the assumption -- 17 A The hypothetical. 18 Q -- I'm asking you to make? 19 A The hypothetical, I understand, yes, sir. 20 Q Okay. In that circumstance, would you 21 consider the command buffers to be individual 22 engines by themselves, each one by itself an 23 individual engine? 24 A Because I already have another virtual 25 engine disclosed here, I would not consider that	136 1 inside the command processor that receives tasks 2 from the OS scheduler and that sends it to the 3 virtual engine -- that command buffer, by itself, I 4 would not consider it to be a -- a virtual engine. 5 In combination with the other components, 6 yes. 7 Q And that's because the command buffer by 8 itself doesn't provide the processing capability 9 that you have in mind? 10 A Also it doesn't do state data loading. I 11 mean, it's not -- here the issue is more substantial 12 than whether it does processing or not. It's just 13 where does the command buffer do loading of the 14 state? 15 Q Why does -- why does a singular engine need 16 to do loading of a state? 17 A So we are talking about this embodiment, 18 right? In this embodiment -- 19 Q No. I'm talking about the claim. I'm 20 talking about the claim. 21 A Sir, you cannot change on me. 22 Q I'm not. I'm not -- 23 A You're going back and forth. I -- you 24 cannot go back and forth. I don't know even what we 25 are -- what the scope of this discussion is.

137 1 Q Let's reset. 2 A Yes, reset. 3 Q Okay. Let's reset. 4 What we're talking about is the meaning of 5 the term "engine" as that term is used in the claim. 6 Okay? And we're talking about what is the scope of 7 the meaning of the term "engine," what are the metes 8 and bounds of that term "engine" as that term is 9 used in the claim with reference to a hypothetical 10 that I'm giving you. 11 I'm trying it figure out whether or not 12 this hypothetical would fit within the meaning of 13 the term "engine" as it -- as it is used in the 14 claim; and the hypothetical is that the command 15 buffer 420-A, 420-B, and 420-N, that those are part 16 of the command processor but are otherwise 17 structured as -- and -- and -- and -- and provided 18 as disclosed. 19 So the question to you is, would any one of 20 those command buffers by itself qualify as a 21 singular engine within the -- the meaning of the 22 term "engine" as it's used in the claim to a POSITA? 23 MR. JOHNSON: Objection; form. 24 THE WITNESS: Again, looking at this 25 embodiment which is in front of me, going with your	139 1 BY MR. RIZK: 2 Q My question to you is -- either one. 3 Whichever one you want. You can -- you can give me 4 both. 5 My question isn't about the engines that 6 are identified in Figure 4, the -- the virtual 7 engines identified in Figure 4. 8 My question is whether you apply in your 9 definition of "engine" as -- as a singular unit, 10 "engine" -- whether you would consider a command 11 buffer to constitute an engine if it is disposed 12 within the command processor of the GPU. 13 A Again, I don't have the full information. 14 I need to see the block diagram, the RT-level 15 description of that command processor 230 to know 16 how this command buffer is connected -- connected 17 through GPIO or some other kind of -- PCIE, 18 something, right? I don't know -- to -- to the OS 19 scheduler, which we know is running on the CPU as -- 20 right? 21 So the interactions between the CPU and 22 that command buffer inside the command processor is 23 unknown. The connection between the command buffer 24 and the virtual engine that could be hardware or 25 software or a combination thereof is not known; and
138 1 hypothetical, which extends the boundary of the GPU 2 to include the command buffers, on -- on top of 3 that, moves the external command buffers into the 4 command processor in -- in ways that I don't know 5 what it means, so what are those -- and I put them 6 there how do they -- who writes to them? 7 The data comes from OS scheduler, but what 8 other hardware mechanism is there? I mean, you have 9 to describe the full hardware mechanism for me. How 10 does the OS scheduler now write into a command 11 buffer inside a command processor, and -- and then 12 that command processor has what kind of connectivity 13 to the virtual engine which could be hardware or 14 software or a combination thereof? 15 There is a lot of details missing here. 16 You're -- 17 MR. RIZK: Using wires and passthroughs, 18 sir. 19 THE WITNESS: No, sorry, I -- I don't know. 20 Virtual engines could be hardware or software. 21 MR. RIZK: Okay. 22 THE WITNESS: If it's software -- 23 MR. RIZK: We'll make it hardware. We'll 24 make it hardware or software. I don't really care. 25 THE WITNESS: No. Which one?	140 1 you're asking me "In spite of all there's unknowns, 2 please make a prediction. Tell me what you think." 3 No, I don't want to tell you what I think. 4 I don't know. I don't have the details. Give me 5 time, give me all the information I need, I'll give 6 you an answer. 7 If you are really interested in my answer, 8 please ask your expert or yourself -- I know you 9 have an engineering background also, so come up with 10 a drawing and say "This is what I mean." 11 I mean, you were quite comfortable writing 12 this, right? So please feel comfortable, draw a 13 block diagram of what you mean exactly inside of 14 the -- the -- with all the components that I need. 15 I need to know what the interfaces are, what the 16 connections are to the -- to the cache memory, 17 and -- and where -- where the virtual engine is, 18 what kind of entity is the virtual engine. 19 Give me that information, I'll 20 hypothesize -- I'll try to answer that hypothetical. 21 MR. RIZK: That information wasn't present 22 for the prior art that you analyzed. The prior art 23 that you analyzed in this investigation didn't have 24 full disclosure of every single interconnection 25 between multiple components.

141 1 THE WITNESS: It had enough. It had 2 enough. 3 The point here is that your hypothetical 4 doesn't provide me with enough information. The 5 prior art references gave me enough for me to form 6 my opinion. That's the difference. 7 BY MR. RIZK: 8 Q So what else would you need? 9 If I draw a block diagram for you -- 10 A Yeah. 11 Q -- would you be able to answer my question? 12 A I-- I need to know the command processor, 13 you have to identify exactly what the virtual 14 engines are, what kind of RT-level description is 15 there for these, this is -- is it a state machine? 16 Is it another buffer? 17 Is it something that has access to memory? 18 Which kind of memory? How does it load state data? 19 I mean, you have to show me where the state data 20 comes, does it affect the command buffer the way 21 you -- you want to integrate it. 22 You draw this -- 23 Q It's exactly -- you're -- you've been in 24 this business pretty long, I can tell. 25 A Yeah.	143 1 A No, I do not. 2 Q Okay. You would agree with me that there 3 is a circumstance -- is there any circumstance in 4 which a command buffer is included within the 5 command processor of Figure 4 that you would 6 consider that command buffer to be an engine? 7 A I have to see the details to answer this. 8 Q I'm just asking you if there's -- is there 9 any hypothetical circumstance? 10 MR. JOHNSON: Objection; form. 11 THE WITNESS: I'm sorry, I cannot consider 12 all hypothetical circumstances. There is infinitely 13 many of them, potentially, right? So I'm sitting 14 here, you're asking me on the fly come up with the 15 full range of hypotheticals and is there any one 16 hypothetical in which -- like Dr. Strange, looking 17 at 10 million parallel universes and one of those 18 universes, are we going to be able -- 19 MR. RIZK: Sir, if the answer is no, you 20 can say "I can't --" 21 THE WITNESS: I said no, yeah. 22 MR. RIZK: -- "I can't answer your 23 question." 24 THE WITNESS: Yeah, I -- I -- I -- I told 25 you. You're pressing it, so that's why we end up
142 1 Q And what I'm asking you is to just assume 2 that the command buffer is within the -- the RTL 3 block for the GPU, but it's -- and -- and the 4 command processor, but it's otherwise connected to 5 the virtual engine as described. 6 It's -- it's a pretty simple hypothetical, 7 sir. 8 A No, I do not agree this is simple. Maybe 9 it looks simple to you, but it's not simple -- it's 10 not actually a simple problem, sir. 11 It's a complicated problem, requires more 12 analysis. I need to have a lot more data. Give me 13 all that, give me enough time, I'll come up with the 14 answer. I'll be glad to write a supplemental report 15 in which -- in -- in -- in response to your theory 16 now -- 17 Q I'll make it -- I'll make it simple for 18 you, sir. I'm going to withdraw my question. All 19 right. 20 A Thank you. 21 Q You would agree with me that there is a 22 circumstance in which a command buffer, as described 23 by the -- the '381 patent, could have zero 24 processing capability but still constitute an engine 25 as you've defined that term?	144 1 there. 2 MR. RIZK: I'm just asking for yes-or-no 3 answers, sir. 4 THE WITNESS: Repeatedly, of course; but 5 that's fine. You're -- it's your privilege to ask 6 those questions. Please go ahead. 7 MR. RIZK: Let's continue. So let's go to 8 the -- let's go to your report. 9 THE WITNESS: Parallel universes. 10 MR. RIZK: Page 43. 11 Actually, you can turn to Paragraph 109 of 12 your report; and you can pull up, if you want -- you 13 have the claims. Excuse me. I'm just going to 14 handle your exhibit here to help you with the 15 claims. 16 THE WITNESS: Thank you. 17 MR. RIZK: Here's the claim for the '053 in 18 front of you; and you have Paragraph 109 of your 19 report, which is Exhibit 1. It's on your right-hand 20 side, underneath Exhibit 3. 21 Q Okay. Do you have 109 in front of you? 22 A Yes, sir. 23 Q You identify the cache unit 1024 as the 24 alleged memory device of Studdard, correct? 25 A Yes.

145 1 Q And, in fact, the only memory device you 2 identify in your report is the cache unit 1024, 3 correct? 4 A Yes. 5 Q Now, directing your attention to Studdard, 6 there's a figure that you have reproduced from 7 Studdard, Figure 4. 8 You'd agree that that cache memory device 9 1024 is a component of Studdard's thread manager, 10 correct? 11 A Yes, sir. 12 Q Okay. And looking at Paragraph 112 of your 13 report, you acknowledge that Studdard does not 14 explicitly disclose that the cache unit 1024 stores 15 pixel command threads and vertex command threads, 16 correct? 17 A Yes, sir, that's what I said there, 18 correct, yes. 19 Q In fact, Studdard never explicitly 20 throughout its disclosure identifies the phrase 21 "pixel command thread," correct? 22 A I'd like to look at Studdard. 23 Q We're -- we're not going to have time to -- 24 to look at Studdard. 25 In your report, you don't identify any	147 1 I didn't say that Studdard does not even mention 2 vertex command threads or pixel command threads or 3 what have you, right? 4 All I have said -- by the way there's a 5 typo in here, right? Both is written as "vertex," 6 "vertex." One is "pixel," one is "vertex." 7 Did -- I -- I had some corrections. Jeff, 8 did we -- typos, did we pass it to the -- or do you 9 want to -- so there are some typos here, typos. 10 BY MR. RIZK: 11 Q So you see a typo in what paragraph? 12 A So Paragraph 112, and unfortunately, 113 13 also, you can see that I say "While Studdard does 14 not explicitly disclose that this cache unit 1024 15 stores a plurality of vertex command threads and a 16 plurality of vertex command threads." 17 That's, obviously, a typo. What I meant is 18 that one of the two, either the first or the second, 19 is a pixel command thread. 20 Q Okay. Can you please correct -- 21 A Sure. 22 Q -- Paragraph 112 using this red pen? 23 A Sure. 24 Q And for the record, you're going to make 25 that correction in Exhibit 1?
146 1 explicit disclosure in Studdard of the phrase 2 pixel command thread? 3 A If that's what you say, yes. 4 Q Well, I'm asking you if, in your report -- 5 A I have to look at it. 6 Q Okay. 7 A I mean, again, this is -- I reviewed these 8 things months ago, right? And I have some 9 citations, 20 to 23, 21 to 7, and you're asking me 10 don't look at it, just -- just agree to me; and so 11 fine, I'll agree to you because that's what you say. 12 I trust you're being truthful in telling me 13 what -- what is there, but I don't know. I haven't 14 looked at it. 15 Q Let me try it this way. 16 When you stated that -- that Studdard does 17 not explicitly disclose pixel command threads and 18 vertex command threads, what did you mean by that? 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: What I mean is what I've 21 written. 22 This -- this cache unit 1024 stores a 23 plurality of vertex command threads and a plurality 24 of vertex command threads. This is not something 25 that's been explicitly disclosed in -- in Studdard.	148 1 A Yes. 2 And also in Paragraph 113. Unfortunately, 3 it's my problem, my mistake, a typo. 4 Q That's okay. 5 A Cut and paste. 6 Q Okay. So what does Studdard explicitly 7 disclose about the storage of threads in -- in the 8 cache unit 1024? 9 A I want to look at those citations. 10 Q Okay. You have Studdard. It's Tab 9 of 11 Exhibit 2 in the binder that's in front of you. 12 A So, for example, on Page 11, starting 13 Line 12, the statement of Studdard is that 14 instructions for a thread are fetched from local 15 memory or the EPU-8 by the fetch unit 1023 and 16 supplied to the cache unit 1024; and we know these 17 threads can be either pixel or vertex threads, and 18 so looking at this, obviously, the -- this cache 19 memory is storing these instructions which 20 correspond to pixel and/or vertex threads. 21 Q Okay. But there's no disclosure here that 22 those pixel and/or vertex threads are stored in the 23 cache at the same time -- 24 A Why not. 25 Q -- that's explicit.

149 1 A Why not? 2 Q Show me the explicit disclosure where it 3 says that both pixel threads and vertex threads are 4 stored in the cache 1024 at the same time? 5 A It's there. I mean -- 6 Q Give me a citation. Please show me -- I 7 don't see it, so tell me where is the explicit 8 disclosure where it says vertex threads and pixel 9 threads are stored in 1024 at the same time. 10 A All threads are stored there. We know that 11 the threads are both pixel or vertex processing 12 threads; therefore, both of them should be stored 13 there on the cache memory. 14 Q I'm not asking you to tell me what you 15 think, sir, I'm asking you -- 16 A It's not what I think. It's what it is. 17 MR. JOHNSON: Don't -- 18 BY MR. RIZK: 19 Q I'm asking you -- I am asking you to point 20 me to an explicit disclosure in Studdard that says 21 that pixel threads and vertex threads are stored 22 simultaneously within the cache unit 1024. 23 MR. JOHNSON: Dr. Pedram, please don't 24 interrupt him when he's asking you a question. Let 25 him finish.	151 1 Skilled people in the art would know, 2 therefore, that these threads are vertex threads or 3 pixel threads. We know also from the previous 4 sentences I read to you that all of these threads 5 are stored in the cache memory 1024; so to me, this 6 is really as explicit as you need it to be; but if 7 you are saying "I don't see in -- a sentence that 8 has a plurality of vertex command threads and a 9 plurality of the pixel command threads being 10 simultaneously stored in the cache unit," no, it's 11 not explicitly there, and that's what I've said in 12 my report. 13 BY MR. RIZK: 14 Q And the -- the -- the disclosure that 15 you're relying on for potential disclosure of vertex 16 and pixel threads being stored simultaneously is the 17 disclosure that says threads 2 to 7 assigned to 18 executing 3D activities such as calculating 19 verticis, primitives, or rastering? 20 A This is one example. I'm not saying this 21 is exhaustive. Just one example. 22 Q For the disclosure that you just stated in 23 your testimony? 24 A Yes, yes. 25 Q Okay. And those threads 2 to 7 is -- where
150 1 THE WITNESS: I'm sorry. I apologize. 2 To me, this is explicit, so I'll read it to 3 you. You probably will -- see if -- what you think. 4 All right. So for example on the same 5 page, starting Line 21. 6 MR. RIZK: What page are we on, sir? I'm 7 sorry. 8 THE WITNESS: Page 11, Line 21. 9 For example, thread 0 -- so -- so the 10 context here is that the -- the -- the -- these 11 threads are being sort of assigned to -- to be 12 processed, and then -- so I'll read the full 13 sentence. 14 (Reading): 15 At any particular moment in 16 time, each thread may be assigned 17 to any one of a number of tasks. 18 For example, thread 0 may be 19 assigned for general system 20 control, thread 1 is assigned to 21 execute two-dimensional activities, 22 and threads 2 to 7 assigned to 23 executing 3D activities such as 24 calculating verticis, primitives, 25 or rastering.	152 1 is -- there's -- there's no explicit disclosure -- 2 at least in this section, you would agree with me 3 that there is no explicit disclosure that some of 4 the threads in 2 to 7 can perform would be vertex 5 threads and some of the threads would be pixel 6 threads? 7 A Again, the terminology "vertex" -- "vertex" 8 is used, "pixel" is not used, but anyone who is 9 familiar with rasterization or primitive processing 10 would know that this involves pixel processing, so 11 it's clear to a POSITA, I would say, and clear to 12 me. 13 Q Yeah, but I'm talking about -- let's stay 14 on that page, sir. Please stay on Page 11. Okay? 15 We're still -- I haven't moved off of this page yet. 16 So we're talking about threads 2 to 7 as 17 described in the disclosure that you relied upon for 18 your proposition that pixel and vertex threads are 19 stored at the same time in the cache unit 1024. 20 A Yes, sir. 21 Q Okay? 22 There is no disclosure here that one of the 23 threads in 2 to 7 could be a pixel thread and 24 another of the threads in 2 to 7 could be a vertex 25 thread, is there?

153 1 It doesn't say that in this disclosure. 2 We'll go to other disclosures later, but I'd like 3 you to stay with me. I see you looking at other 4 pages in the exhibit. I'd like you to stay with me 5 on Page 11 because that's the page I'm talking 6 about. 7 A Sir, you -- you can ask me the question, 8 I'll answer the question, but you cannot tell me 9 what I'm looking at. Maybe I want to look ahead or 10 look before it, I mean, so what's the point? 11 Q I -- I would like to focus on this 12 disclosure -- 13 A Sure. 14 Q -- that is the subject of my question. 15 A Please go ahead. 16 Give me time to look at some other things? 17 Do you want to give me time? 18 Q I -- I am directing my question to the 19 specific disclosure on Page 11. 20 A Sure, fine. 21 Q We can -- we can talk -- I'll let you -- I 22 will give you the opportunity and your counsel will 23 have the opportunity to -- to talk about other 24 things. Right now I'm talking about this one 25 paragraph on Page 11, and I'd like you to stay with	155 1 referring you now to Figure 3. 2 A Okay. 3 Okay. 4 Q Okay. Do you see the Figure 3 has a 5 processing block 106; and within that processing 6 block, there's an array of PEs, or processing 7 elements, 1061. 8 Do you see that? 9 A Yes. 10 Q Okay. And Figure 9 -- let's go back to 11 Page 20. 12 You'll agree with me -- I'm reading from 13 Line 23 -- Figure 9 illustrates simplified steps and 14 a graphics data processing method using a system -- 15 system of Figures 1 through 8, correct? 16 A Yes. 17 Q Okay. So it's referring that it includes 18 Figure 3 and Figure 4 of the Studdard reference, 19 correct? 20 A Okay. 21 Q Okay. And you -- do you agree with me that 22 the PEs are the devices within the processing block 23 that are generating the threads 1022? 24 A Generating or processing? You mean 25 generating?
154 1 me there, sir. 2 A Again, I'm going to stay with you; but you 3 cannot force me, sir, to not look at some other 4 page. I will answer your question. 5 MR. JOHNSON: Wait for a question. Just 6 stop and wait for a question. 7 BY MR. RIZK: 8 Q My question for you is, on Page -- the 9 third paragraph of Page 11, is there any disclosure 10 that some of the threads of 2 to 7 can be assigned 11 to pixel while other threads of the 2 to 7 can be 12 assigned to vertex? 13 A There is no such disclosure, no. 14 Q Okay. Directing your attention now to a 15 different page, I'm going to direct your attention 16 to Page 20, Lines 20, through 22, Lines -- Line 32. 17 Do you have that section in front of you? 18 A Yes. 19 Q Okay. Now, in that section, it is 20 referring to the work performed by the various PEs 21 that are within a processing block, correct? 22 A What is a processing block? 23 Q So if you look at Figure 3 -- 24 A Yeah, that -- that relates to Figure 9. 25 Q Okay. I understand, but I'm -- I'm	156 1 Q They're -- they're providing the threads 2 1022 as shown in Figure 4. 3 Let me withdraw the question. 4 The -- the threads that are coming out B-0 5 through B-7, do you see those -- 6 A Yes. 7 Q -- on Figure 4? 8 Do you see the threads B-0 to B-7? 9 A Yes. 10 Q Okay. Those B-0 to B-7 threads that are 11 shown on Figure 4 correspond to the threads 0 12 through 8 that were referred to on Page 11, Line 16 13 through 25, correct? 14 A Sure. 15 Q Okay. And those threads are processed 16 by -- as described in -- in the context of Figure 9, 17 those threads are processed by eight PEs that are 18 part of a processing block, correct? 19 A You're referring now to thread processors 20 1026 or you're talking about the PEs inside the 21 computational core, especially 1061 processor units, 22 and so on? 23 Q I'm talking about the array of PEs 1061. 24 A Okay. 25 Q So each one of those threads corresponds to

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157 1 a PE within the array of PEs, correct? 2 A That's fine. 3 Q Is that right? 4 A Yes. 5 Q And then in the -- the disclosure that 6 appears on Page 20 through Page 22, where it's 7 talking about the operation, simplified steps and a 8 graphics data processing method using the system of 9 Figure 1 through 8 -- 10 A Yes. 11 Q -- it talks about how those PEs consume the 12 threads 0 through 7 that were referred to earlier, 13 correct? 14 A I don't know if the term "consumed" is 15 being used, but I -- I know that they're being 16 processed there, so -- give me time, please, to look 17 at this -- this excerpt regarding Figure 9. 18 Q Let me make it simple for you, sir. 19 A You don't have to make it simple for me, 20 just give me time. 21 Q I'll simplify the question because, 22 respectfully, while I appreciate that you're 23 interested in reading through the reference and that 24 it's been a while since you wrote your report, we -- 25 we have a limited amount of time today.	159 1 data; so if all eight of them are always necessarily 2 organized in such a way that they have to perform 3 the exact same instruction, then at any given point 4 in time, you could not have different types of 5 threads running through them as described in 11. 6 Q So if -- if, in fact, the array is a SIMD 7 array -- let's presume that. I understand your 8 concern about how is it possible that thread 0 and 9 thread 1 are doing something else. 10 A Yeah. 11 Q But let's presume that Page 9, Lines 5 12 through 9, is an accurate characterization of the 13 operation of the processor. 14 You would agree with me that any -- at any 15 given moment in time, that processing -- that array 16 of processor elements 1061 is either doing pixel or 17 vertex but not both? 18 A So under the SIMD assumption that you 19 mentioned for the array 1061, they would be doing 20 the exact same set of instructions under SIMD. Not 21 under SIMT, but SIMD is fine. 22 And then that's correct with respect to one 23 of the processing blocks; but, of course, you have 24 multiple of these. 25 Q Sir, we're talking about just about the
158 1 The PEs make up a SIMD unit, correct? 2 The -- the eight SIMDs make up a SIMD unit, correct? 3 A Can you point me to a particular part of 4 Studdard that does say that? Because if that was 5 the case, how is it that you're -- according to the 6 Page 11 reference -- 7 Q So Page 9, Line 5, it says the array of 8 processor elements provides a single instruction 9 multiple data processing structure, correct? 10 (The witness reads sotto voce.) 11 THE WITNESS: Yes, I see that; but, again, 12 I want to point out before you move on that in the 13 excerpt that you read on Page 11, for example, 14 thread 0 may be assigned for general system control, 15 thread 1 is assigned to execute 2D activities, and 16 threads 2 to 7 assigned to executing 3D activities. 17 Obviously, these eight different threads 18 could not be executing the same instruction at the 19 same time. One of them is general purpose. System 20 control, one of them is 2D, one -- six of them are 21 3D, so -- 22 BY MR. RIZK: 23 Q And -- and is that inconsistent with the 24 processing elements being organized in a SIMD? 25 A SIMD means single instruction multiple	160 1 array of processing elements, which is what's in 2 your report. That's all I'm focused on today, what 3 is -- what is stated in your report. 4 In your report, you talk about the array of 5 processing elements, you don't talk about different 6 blocks, so I'm focusing on the array of processing 7 elements for now. 8 If your -- your counsel wants to talk about 9 blocks, we can deal with that -- that later; but for 10 now, my questions are directed toward the -- the 11 array of processing elements. 12 So for the array of processing elements, if 13 you assume that Studdard is accurate that it is a 14 SIMD, you would agree with me that the cache 15 unit 1024 at any given moment of time would not 16 necessarily store both pixel and vertex threads? 17 A I disagree. 18 Q Why is that? 19 A Because there could be other processing 20 arrays that are doing pixel processing, they are 21 doing it independently of the first array, but they 22 still have to store their data in the cache memory. 23 Q But there's no explicit disclosure in 24 Studdard of those other blocks performing pixel 25 processing while one block is doing vertex

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161 1 processing. 2 A It's -- it's understood. It's quite common 3 for all kinds of GPUs, including this system, or all 4 kind of multiple processing element systems that 5 they are doing different things at the same time. 6 That's why you provide all the 7 computational capability that's needed to speed up 8 graphics processing tasks, for example. There's no 9 requirement -- in fact, it's going to be, probably, 10 discouraged -- not probably. It's 100 percent 11 discouraged from limiting yourself to only do vertex 12 processing and no pixel processing whatsoever 13 because we know pixel processing is usually a much 14 more intensive task than vertex processing, at least 15 in the number of pixels that you have compared to 16 the number of vertices, so if you have all these 17 resources and only use them to do vertex processing 18 at the time without starting any kind of pixel 19 processing in the pipeline fashion, then you are not 20 making use of the resources that you are provided. 21 You have paid for the resources, you have 22 built them, you have put them in, you're not making 23 use of them. That's nonsensical. 24 Q I'm not asking you -- I'm not asking you -- 25 I'm asking you if Studdard explicitly discloses it.	163 1 processing; and if you have some of your processing 2 arrays, under SIMD assumption, doing vertex, some 3 doing pixel, of course, the cache that supports this 4 kind of processing would have to store pixel and 5 vertex threads simultaneously. 6 Q Okay. But Studdard doesn't actually say 7 that. This is -- this is what you're saying. This 8 is what you believe as a POSITA, but it's not in 9 Studdard, correct? 10 MR. JOHNSON: Objection; form. 11 THE WITNESS: Again, to me, it is clear 12 from the specification in Studdard that this is 13 there. You are always, seems to be -- seem to be 14 looking -- 15 MR. RIZK: I'd like you to show me -- 16 THE WITNESS: I'm sorry. I have to finish 17 my sentence. 18 So you're looking for the exact statement 19 that Studdard would make that would be the sentence 20 of the asserted claim of '381. That's not how it 21 works. Studdard precedes '381. It doesn't know 22 about '381. 23 It doesn't use that terminology or that 24 notion; but the description here is very clear that 25 threads could be assigned to different types of
162 1 Does Studdard explicitly disclose that one 2 processing block will be performing pixel while the 3 other processing block will be performing vertex? 4 A Yes, to me, that's explicit. 5 Q Where -- where is it explicitly disclosed? 6 A So -- so, for example, when -- when they 7 talk about -- I understand, and I -- I -- I pointed 8 that out myself, that there is a little bit of 9 contention here with respect to SIMD assumption 10 versus the disclosure on Page 11; but on Page 11, it 11 clearly states that you could have different threads. 12 My only -- if I were to reconcile these 13 things, I would assume what they meant, potentially, 14 was that maybe different processing arrays have 15 different arrangements so that one processing array 16 is doing sort of general system control, the other 17 processing array is doing 2D, some other processing 18 arrays are doing 3D, that's really what they meant 19 on Page 11, or that Studdard meant on Page 11, but I 20 don't know. I'm not sure. It's not explicit in 21 that way. 22 But, again, under the -- even under the 23 SIMD assumption, there is no requirement or 24 implication or reality, in fact, that you'd be doing 25 by all of your processing arrays only vertex	164 1 tasks; that you have these parallel processing 2 arrays that could be activated at the same time, 3 they could be running different threads. The cache 4 that supports them, therefore, would be storing both 5 pixel and vertex. 6 You're saying there is no exact sentence to 7 that. Yes, there is no exact sentence that says it. 8 MR. RIZK: Okay. And for what it's 9 worth I -- I didn't ask you about the '381 patent. 10 THE WITNESS: I'm sorry. '053. My 11 mistake. 12 MR. JOHNSON: So our lunch is here. 13 MR. RIZK: Okay. Let me -- let me wrap it 14 up, probably need about five more minutes. 15 Q So, Doctor, staying with Studdard, can you 16 point me to any other disclosure in Studdard that 17 explicitly or implicitly states that multiple 18 threads -- that -- that you have pixel and vertex 19 threads that are being processed at the same time? 20 A In my report, I'll read it and go to the 21 citations. 22 The processing blocks 106 -- so I'm not 23 talking about the array. The processing blocks 106 24 that receive instructions from the thread manager 25 102 containing cache unit 1024 process both pixel

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165 1 and vertex data, and the reference I use here is 2 Page 20, Column 23 -- not "column" -- Line 23, to 3 21, Line 7. 4 Q Okay. Let's stay -- let's stick with that. 5 So for that -- 6 A That's vertex. 7 Q -- for -- for -- for -- yes. 8 A That's vertex. 9 Q So in that -- in that section that you just 10 identified, 20-23 to 21-7 -- 11 A Yes. 12 Q -- only vertex is being processed -- 13 A Correct, sir. 14 Q -- in that section. 15 A Sure. Sure. 16 THE STENOGRAPHER: I'm sorry. 17 MR. RIZK: Go ahead. I'm sorry. 18 THE STENOGRAPHER: Please start over with 19 your question; and one at a time, please. 20 BY MR. RIZK: 21 Q In that section that you've identified, 22 namely, 20-23 to 21-7, the -- the processing system 23 of Studdard is only processing vertex, correct? 24 A Correct, sir, yes. 25 Q Okay. So --	167 1 high-definition image containing thousands -- 2 millions of pixels -- do the verticis first and only 3 then start doing pixels. 4 What they will do is to use the notion of 5 pipelining. You know of pipelining, right? 6 So the idea of pipelining is that I have 7 this linear pipeline, so some of my processing 8 elements -- for example -- I'm giving a very simple 9 example for a layperson to understand. 10 Imagine I have four quadrants in my image. 11 I'll take the top left quadrant and start doing 12 vertex processing on it; and I exhaust my resources, 13 and I -- I -- I -- I do the vertex processing there. 14 Then I want to move -- move to the top right 15 quadrant of the image. 16 As I move there to do vertex processing, I 17 will have extra resources to use. I will use my 18 extra resources now to do the pixel processing on 19 the top left for which I've already concluded my 20 vertex processing. 21 This is the idea of pipelining, functional 22 pipelining. I do vertex processing on the top right 23 as I'm doing pixel processing on the top left for 24 which the vertex processing has already been 25 completed; so at any instance in time when I just
166 1 A And then -- 2 Q So -- so -- so and then after that, at that 3 point in time, then you're going to -- what's next? 4 22-4, 32? 5 A Yes. 6 Q And in 22-4, 32, is that where you contend 7 that -- that the pixels are being processed? 8 A Yes, sir. 9 Q Okay. In this disclosure that appears 10 between 20-23 to 21-7, that -- that disclosure that 11 you're relying on in 22-4 to 32 only happens after 12 the vertex processing has been completed; isn't that 13 correct? 14 A Yes. 15 There is a linear graphics pipeline 16 described here with a particular ordering between 17 vertex and pixel processing, but we are talking 18 about a system that is trying to render a 19 three-dimensional image on a two-dimensional screen 20 running -- operating on different parts of an image 21 to try to do vertex and pixel processing for 22 different verticis and different primitives and 23 different pixels. 24 No system would limit itself to only do 25 vertex processing of the full image which could be a	168 1 look at the data -- right? -- that's flowing in the 2 graphics pipeline and present there, I will see both 3 pixel and vertex data. I'll see my processing 4 engines doing both pixel processing and vertex 5 processing; but, of course, they are working on 6 different data. 7 The data is not the same. The data is 8 different, but it's just happening at the same time 9 so that cache memory must store the vertex data for 10 the top right verticis and the pixel data for the 11 top left quadrant pixels. 12 Q Well, that presumes, of course, that -- 13 you're presuming, I think, in the hypothetical that 14 you've now created that the -- the number of 15 processing blocks that are in the system are 16 sufficient to service the needs of vertex processing 17 for the first quadrant because if they're not 18 sufficient to service the needs of the first 19 quadrant, then it would be impossible to move on. 20 You'd have pixel starvation, in fact, if 21 you tried to move on to pixel processing before you 22 completed it; so you're building into your 23 hypothetical, I think, that you're assuming that 24 there's a sufficient number of processing blocks to 25 service both the needs of pixels and verticis; is

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169 1 that correct? 2 MR. JOHNSON: Objection; form. 3 THE WITNESS: So, of course, if there is 4 only one processing element, you can only do vertex 5 or pixel at any given time. That's just one 6 process. 7 MR. RIZK: Well -- 8 THE WITNESS: I let you finish your 9 question. 10 MR. RIZK: Go ahead. Go ahead. 11 THE WITNESS: If you have two of them, you 12 can potentially do one vertex, one pixel. Your 13 point here is that but there's so many verticis and 14 so I have to probably use -- I can. I can. 15 You're not even suggesting that you -- I 16 will necessarily have to do it that way; but saying 17 because there are so many verticis, you have just 18 two processing elements, maybe do the two. Okay. 19 Fine. I'll give you that. 20 If I have 20, yeah, maybe. If I have 200, 21 oh, maybe. If I have 2,000, if I have 20,000, if I 22 have 200,000 processing elements, then, of course, 23 you have a lot of processing power now. 24 And the -- the point here -- and it's 25 well-known by a POSITA and well-known at the time of	171 1 possible but more than likely that at times, I will 2 run out of the need to do vertex processing, a lot 3 of my PEs will remain idle, and I -- I ask them to 4 do pixel processing. 5 So on those points in time -- not every 6 time, but those portions of time in which I'm -- I 7 don't need that many processors for my verticis 8 because they're so -- so much fewer, then I use them 9 to do pixel processing. 10 Anyone that says no, no you're going to 11 wait until -- you put the synchronization barrier, 12 you wait for the -- all the verticis to be 13 completed, only do pixels, that's foolish. Nobody 14 would do it. 15 MR. RIZK: Okay. So let's -- let's take 16 that. 17 So you would agree that -- 18 THE STENOGRAPHER: I need a break. 19 MR. RIZK: Okay. Why don't we -- why don't 20 we call it, then. 21 THE VIDEOGRAPHER: Please stand by. 22 We're going off the record. The time is 23 12:52 p.m. 24 (A recess for lunch was taken from 25 12:53 p.m. to 1:50 p.m.)
170 1 the invention that these graphics processing units 2 have to have a lot of computational power to do this 3 kind of SIMD operation and now you have a vert- -- 4 set of verticis and a set of pixels. 5 Verticis are much fewer than pixels. I'm 6 not talking about fewer by 2X or 3X or 5X. We are 7 talking about 1000X, right? So the number of 8 verticis in an image is usually orders of magnitude 9 smaller than the number of pixels. 10 If I'm a designer trying to build a system 11 that will deliver performance, therefore, it will 12 have a market value, I'll build a system that can 13 accelerate graphics processing; so if I try to 14 target the pixels side, I just need so many 15 processors. 16 If I target the vertex processing side, I 17 will have much, much fewer processors, so I'll look 18 at my silicon real estate, the cost that I can 19 afford, and so on, and I put as many processing 20 elements that I can for different types of 21 applications. 22 Some images might be small images, 32 by 32 23 pixel; some could be high-definition, 4000 by 2000 24 pixels, and so on. Right? And so I will be having 25 a lot of processing element, and it's quite not only	172 1 P R O C E E D I N G S 2 3 THE VIDEOGRAPHER: We are back on the 4 record. The time is 1350 p.m. 5 CONTINUED EXAMINATION 6 BY MR. RIZK: 7 Q So, Doctor, back to Studdard for the '053 8 patent, to be clear -- this is a yes or no -- it is 9 possible for Studdard's processing blocks 106 to 10 process only vertex or pixel at any given moment in 11 time, correct? 12 A It is possible, but also it's possible to 13 be processing both vertex and pixels at the same 14 time. 15 Q And if the -- the disclosure in Studdard 16 about the configuration of -- of its PEs 1061 is a 17 SIMD, then those PEs -- the PE array would only 18 process either pixel or vertex at any given moment 19 in time, correct? 20 A Any one of those arrays, if it's organized 21 as SIMD, then would be processing only one type of 22 thread, but blocks contain multiple threads -- 23 multiple arrays. 24 Q And at least in your report, the section 25 that you identified in your report -- I think the --

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173 1 the disclosure that you identified for the inclusion 2 of pixel and vertex was shown on Paragraph 112 of 3 your report, and you cited to Page 20, Line 23, to 4 Page 21, Line 7, and Page 22, Line 4 through Line 32 5 of Studdard. 6 Do you see that? That's what you cited to 7 in Studdard for the proposition that the cache 8 stores both pixel and vertex? 9 A Sure, that's the citations I have there 10 with the explanation I provided today also. 11 Q Okay. There's no explicit disclosure in -- 12 in what you relied upon that Studdard's processing 13 blocks 106 -- let me withdraw that. 14 There's no disclosure in the support that 15 you relied upon of infrastructure that dynamically 16 allocates Studdard's processing blocks 106 to pixel 17 or vertex processing depending on workload 18 requirements and -- and the number of processing 19 blocks, correct? 20 MR. JOHNSON: Objection; form. 21 THE WITNESS: So it's a compound question. 22 First of all, this process of sharing a GPU 23 resource among different types of threads does not 24 necessarily be called a dynamic allocation of the 25 resources. It could have been done also statically	175 1 allocation of the different processing blocks. It 2 could be done statically at compile time also; and 3 then the fact that you have this complex set of 4 resources, the vast amount of them, and a person of 5 ordinary skill in the art knowing that you don't 6 want to leave resources under- -- underutilized or 7 unused when you can simply make use of them using 8 functional pipelining techniques, standard, 9 well-known to the person skill in the art, all of 10 that tells me that, in fact, a POSITA having read 11 Studdard would understand that you could be doing 12 both pixel and vertex processing at the same time in 13 the GPU of Studdard. 14 Q And if, in fact, the disclosure of Studdard 15 is that the processing blocks 106 at any given 16 moment in time either process pixel or vertex but 17 not both, then you would agree with me that it's not 18 necessarily true that the cache unit stores both 19 pixel and vertex threads at the same time, correct? 20 A So this is a hypothetical which is 21 incorrect. 22 The first part of it, I do not agree with; 23 but if I go with your hypothetical that supposedly 24 the disclosure of Studdard is that not only the 25 processing array 1061 but the full processing block
174 1 at compile time. Both options are possible. 2 But if I set aside this "dynamically" part 3 of it and focus on the rest of the question, then I 4 would say I personally find support for this in 5 paragraphs that we have discussed before; for 6 example, on Page 11, Line 21 to 25 -- sorry -- yes, 7 Line 21 to 25, where they clearly teach us that 8 different threads could be doing different kinds of 9 processing at the same time. 10 MR. RIZK: What you've identified is 11 referring to threads within a single processing 12 block 106. 13 THE WITNESS: I realize that. That's 14 correct, yes, that's -- 15 MR. RIZK: Okay. Yeah. 16 Q There's no disclosure in what you've 17 identified and relied upon for your support of 18 infrastructure in Studdard that dynamically 19 allocates different processing blocks to processing 20 pixels and vertexes so that way pixels and vertexes 21 can be processed at the same time by different 22 processing blocks, correct? 23 A Again, as I answered before, there is no 24 requirement for dynamic allocation; therefore, there 25 is no need for infrastructure that does dynamic	176 1 106 at any given moment in time either processes 2 this -- pixels or verticis, not both, then for that 3 particular task, high-level task running, the -- the 4 data in the cache would correspond to either the 5 vertex or the pixel streams that are being 6 processed. 7 Q But not necessarily both at the same time, 8 correct? 9 A Again, assuming it's a single task 10 running -- also it's possible that you're running 11 multiple tasks with multiple threads. I'm not sure 12 how the system is going to be used in Studdard. 13 So the system is very complicated, very 14 capable, could not only do multiple threads or 15 streams of instructions associated with a single 16 task, but potentially multiple tasks themselves, as 17 was revealed in -- on Page 11, where some tasks are 18 general system control, some are 2D, some are 3D. 19 So then at that point, although, maybe, the 20 3D activity is only limited to, say, vertex 21 processing, but the 2D could be doing something that 22 is similar to fragments, shading or pixel shading. 23 I mean, who knows what's running, right? 24 Or maybe two different 3D tasks are 25 running, one of them is in the pixel processing

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177 1 stage, one of them is in the vertex progress stage 2 and therefore, there is associated data with them 3 stored. 4 I would certainly not conclude from 5 anything I read in Studdard that even under the 6 assumption that you -- you mentioned, there is going 7 to be a limit in terms of what is stored in the 8 cache itself. 9 Q Doctor, that was a very long answer to a 10 very simple question. Okay? My -- I'm asking 11 you -- I think that you would agree with me -- this 12 is a yes-or-no question. 13 You would agree with me that if the 14 processing blocks 106 of Studdard at any given 15 moment in time either processed pixel or vertex but 16 not both, then it's not necessarily true that the 17 cache unit stores both pixel and vertex threads at 18 the same time, correct? 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: So when you say "processing 21 blocks 106," all of them? 22 MR. RIZK: Yeah. 23 THE WITNESS: All of the processing blocks 24 in the Studdard's GPU are doing, say, only vertex 25 processing, and there was no task that was swapped	179 1 and you can explain to him all day long; but for my 2 time, if I'm asking you a yes-or-no question, I'd 3 ask that you try to give me a "yes" or "no" and keep 4 your answers succinct, if possible. I don't need 5 the alternative explanation. 6 THE WITNESS: But the question is not a 7 yes-or-no question, it requires explanation. 8 MR. RIZK: Okay. Well, you're -- you're -- 9 the -- the level of explanation that you're 10 providing is talking about things that are 11 completely different, so we -- I -- I'm not -- I 12 can't force you to change your answers. 13 You're going to -- you're -- you're in 14 control. You're going to be providing today's 15 testimony. But I am saying that if this continues, 16 then -- and you continue to provide these 17 long-winded answers that are not on point, we're 18 going to have to hold today's deposition open and 19 continue on a different day because I won't be able 20 to get through. 21 THE WITNESS: And I have no problem with 22 that. 23 MR. RIZK: Okay. 24 THE WITNESS: That's fine if that's what 25 you decide to do.
178 1 out for this new task to run, then the answer would 2 be yes; but consider that there was another task 3 that was -- 4 MR. RIZK: Doctor, you've answered my 5 question. 6 THE WITNESS: I'm sorry. I -- but -- but 7 I -- really, because you're asking questions, I 8 understand -- 9 MR. RIZK: Doctor -- Doctor, I apologize, 10 but -- but, you know, I asked you "This is a 11 yes-or-no question," and your -- your answers are -- 12 are quite lengthy, not on point, and we're not going 13 to have time to finish your deposition today if it 14 continues this way. 15 I've -- I've -- I've given you some 16 latitude to try to provide explanation; but 17 respectfully, I -- I -- I have a need to get through 18 my questioning today and if every answer is a 19 five-minute answer that isn't on point, then 20 we're -- we're going to have to hold today's 21 deposition open. 22 So I don't want to do that, so I just ask 23 that you -- I understand you want to explain to -- 24 explain to me. Your counsel will have an 25 opportunity to redirect you if -- if needed, and --	180 1 MR. RIZK: Okay. 2 THE WITNESS: And -- 3 MR. RIZK: Let's -- let's continue. Let's 4 continue with the questioning and just see how it 5 goes. I would just ask that when I ask you for a 6 yes-or-no answer, try your best to give me a 7 yes-or-no answer. 8 If you have a short qualifier, I'm not -- 9 I'm not trying to prevent you from doing that. Your 10 counsel will have an opportunity to redirect you. 11 But we're not going to be able to get through today 12 if it continues this way. 13 Q All right. So moving on, I'm going to 14 refer you, again, Page 43, Paragraphs 109 through 15 113 where you're talking about the memory storing a 16 thread, and -- and in Paragraph 112 in particular is 17 where you cite to the receipt of instructions as 18 evidence of the storage of -- of threads within the 19 cache unit 1024, right? 20 A Yes. 21 Q Okay. And you cite to, as your support for 22 that, that it -- it receives instructions, 23 Page 20-23 through 21-7, 22-4 through 32 of 24 Studdard, correct? 25 A Yes, I do.

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181 1 Q And in this section of Studdard that you 2 cite to, there is no disclosure that the cache 3 unit 1024 receives and stores all of the 4 instructions pertaining to any given thread 5 simultaneously, correct? 6 MR. JOHNSON: Objection; form. 7 THE WITNESS: I'm sorry. The question is 8 not well posed. I cannot answer it. 9 I don't even think it's possible to receive 10 instructions pertaining to any given thread 11 simultaneously. Of course, they come sequentially 12 one after the other, cannot be received 13 simultaneously. 14 BY MR. RIZK: 15 Q There's no evidence in Studdard that at any 16 given moment in time, the memory device that you 17 point to, cache unit 1024, stores all of the 18 instructions pertaining to a thread simultaneously; 19 that all of the instructions corresponding to a 20 thread are stored in the cache unit at the same 21 time? 22 MR. JOHNSON: Objection; form. 23 THE WITNESS: I apologize in advance 24 because I know you want a yes-or-no answer -- 25 MR. RIZK: You don't --	183 1 That's typically what happens in these kind 2 of systems. It's called pre-fetch and execute, and 3 you try to overlap, therefore, the actual fetch and 4 execute operation. 5 BY MR. RIZK: 6 Q So at any given moment in time -- 7 A Yes, sir. 8 Q -- the cache unit 1024 might never store 9 all of the instructions in a thread? 10 A May or may not. 11 It's not clear from the description exactly 12 what the policy and the implementation is with 13 respect to when I start executing the instruction. 14 I just know in this, they have a ready status and -- 15 and yielding status, and this and that, so there is 16 some checks that they do in terms of when I can do 17 some instruction or a stream of instructions, but my 18 reading of this is not that all instructions have to 19 already be received and stored before I can start my 20 processing. 21 I mean, I could do -- be doing it 22 concurrently out of -- with proper phase difference, 23 right? Phase lag. 24 Q So the -- the arbiter -- there's an arbiter 25 element in this, in the '053 patent, correct?
182 1 (Mr. Rizk and the witness speak 2 simultaneously.) 3 THE WITNESS: -- but there is really no 4 yes-or-no answer here. I just need to provide a 5 little bit of more technical context and background 6 so that we appreciate what the complexity is when I 7 try to respond to a question like this. 8 Standard processing is that you pre-fetch 9 instructions while you're executing the already 10 received instructions; so, again, you -- we do not 11 normally put a synchronization barrier saying wait 12 for all of the instructions of a thread to arrive; 13 when all of them are there, only then start 14 processing. 15 No one does that. So instructions come, 16 they are pre-fetched. When I'm ready to execute and 17 when the instructions have no data dependencies that 18 allow me to execute them, then I start executing 19 them. 20 So therefore, maybe only 20 percent, 21 30 percent of the instructions that comprise a 22 thread have been received, have been stored, and I 23 start doing the processing; and while I'm doing it, 24 somebody else is providing the remaining 25 instructions for the thread.	184 1 A Yes, correct. 2 Q So that arbiter element can be satisfied 3 and it can select commands from the thread that is 4 stored in the memory even though the -- the full 5 thread is not stored in the memory at a given moment 6 in time? 7 MR. JOHNSON: Objection; form. 8 MR. RIZK: Are you looking for the patent? 9 THE WITNESS: No; for the claims. I know 10 it's in the patent, but my eyes are going to be 11 stressed if I try to read it there. I'd rather 12 read -- 13 MR. RIZK: Okay. 14 THE WITNESS: -- the larger font size in my 15 own report. 16 So Page 21 -- so now you are talking about 17 the arbiter, if I understand correctly. 18 MR. RIZK: Yeah. 19 Let me try to -- let me withdraw the 20 question, I'll try to make it simple. 21 Q For the memory device element to be 22 satisfied, at least one memory device comprising a 23 first portion, that element to be satisfied, does 24 the memory device need to store all of the 25 instructions that are in the command thread

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185 1 simultaneously, meaning that -- that all of the 2 instructions exist in the memory at the same time? 3 A I don't see at the same time requirement 4 here. I mean, they have to be stored there. 5 Q Eventually. 6 A Yes, over time, they have to be stored so 7 that I can process -- read them and process them; 8 but whether all of the instructions are there before 9 I start executing, I don't see that requirement in 10 this claim element. 11 Q Okay. So as a person of ordinary skill in 12 the art, the way that you've applied this element of 13 at least one memory device is that you don't -- you 14 don't believe that the memory -- the at least one 15 memory device needs -- that the instructions 16 pertaining to the thread need to be stored 17 contemporaneously in the memory device, correct? 18 A When I expressed my opinion, I did not even 19 consider this question; so therefore, my opinions 20 are independent of the answer to the question that 21 you're asking me now; and so I allow for both 22 possibilities that they have been received already 23 or that they are being received but some subset is 24 already there and I can process it, and I don't see 25 any issue with either of these possibilities as I	187 1 going to be the critical path. That is, when I'm 2 ready to process, the instruction is there. It 3 wasn't there at the beginning; but when I've done 4 the first and the second and the third, the fourth 5 is going to be there, the fifth is going to be 6 there, and the sixth is there; and when I'm done 7 with the sixth, the seventh and the eighth and the 8 ninth are there. 9 Usually that's how it's done. In typical 10 systems, that's how it's done so that performance is 11 maximized. And I'm not saying if Studdard is 12 necessary -- 13 Q I'm not asking if you have to wait. Okay? 14 That's not my question, if you -- I'm not saying is 15 it still a memory device if you -- if the arbiter 16 has to wait for all. I'm not asking you about that. 17 What I'm asking you about is for a memory 18 device to qualify as the claim memory device, does 19 it need to be sized to store all of the instructions 20 within any given thread that it receives? 21 A I -- I would think the memory device would 22 have to be large enough to contain, store, many 23 threads; otherwise, again, you're going to create an 24 artificial bottleneck in the system in which all 25 these processing elements are able and ready to
186 1 sit here and deliberate on the question; but when I 2 did my opinions, I didn't even consider this. 3 Q So to you, it doesn't matter if the memory 4 device that's in the -- whether -- in the piece of 5 prior art, whether it is sized in such a way that it 6 could never fit an entire thread? 7 A No, that's not what I said. 8 Q Okay. 9 A So what -- because usually the thread size 10 is much smaller than the size of the cache, so I 11 think that is not a possibility that I would 12 entertain. 13 What I said is, for performance reasons, in 14 some systems -- and I'm not sure if Studdard is 15 doing this or not; but in some systems, you don't 16 wait for the full stream of instructions to -- to -- 17 to arrive before you start processing the very first 18 instruction and the second instruction. 19 Of course, you keep going until there is 20 data dependency and that you have to wait or that 21 there is a -- maybe you want to go to the hard disk 22 to bring some values, you swap out or, in this case, 23 you are waiting for instructions to arrive. 24 However, as far as I know, the system would 25 be designed in such a way that the pre-fetch is not	188 1 perform but there is nothing for them to do, and a 2 designer would not want to do that, right? So -- 3 Q I'm talking about a single thread. All of 4 the instructions within a single thread. Let's 5 leave the many threads aside. 6 A Yeah. Okay. 7 Single thread, I would say the single 8 thread would fit. 9 Q Okay. So -- so for a device to qualify as 10 the claim memory device, it needs to be sized to 11 store all of the instructions contemporaneously 12 within a single thread? 13 A Again, that's not the requirement of the 14 claim. 15 If you are saying in general -- 16 Q No, I'm talking about the requirement of 17 the claim, so let's -- 18 A You are not or you are? 19 Q -- let's go with that. 20 I am talking about the requirement of the 21 claim. 22 So does the claim require all of the 23 instructions of a single thread -- the memory to be 24 sized appropriately such that all of the 25 instructions of a single thread to be stored within

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189 1 that memory at the same time? 2 A I -- I haven't considered this question. I 3 need to go back to '381 and really read the 4 specification again looking for the answer for this 5 question. 6 I need time to do it, you know, because I 7 cannot assign meaning or limitations -- this is a 8 limitation, right? -- to one element of Claim 1 9 without really looking at the specs, and even the 10 file history to make sure this was not disowned or 11 excluded. 12 Q With respect -- respectfully, sir, I mean, 13 you've had months to work on your opinion here; and 14 this is -- I'm asking you a question about what is 15 the meaning that you ascribe as a person of ordinary 16 skill in the art having read through the patents, 17 looked at the file history, and -- and did 18 everything else that you did, to determine a 19 thread -- whether it necessarily means, when it says 20 one memory device operative to store a plurality of 21 pixel command threads and -- and a plurality of 22 vertex command threads, does that mean that all of 23 the instructions within each of those threads have 24 to be stored contemporaneously within the memory 25 device or not?	191 1 within every single thread is contemporaneously 2 stored in the -- in the cache unit, so it does 3 matter, sir. 4 A And -- and that's not my reading of the 5 claim element. I understand this is your reading of 6 the claim element. I give you that, but that's not 7 my reading. 8 Q Okay. 9 A My reading of the claim element is not that 10 this -- this element is saying all the instructions 11 associated with a particular pixel command thread 12 have to be contemporaneously being stored in the 13 memory. That's not the limitation I read into 14 this -- 15 Q That's all I'm trying to understand. 16 So your interpretation is that if -- if the 17 at least one memory device stores a portion of a 18 command thread, it -- it stores a command thread, 19 correct? 20 If it stores some of the instructions of a 21 command thread, then it stores a command thread? 22 A That's not even what I'm saying. 23 MR. JOHNSON: Objection; form. 24 THE WITNESS: I'm looking at evolution of 25 this over time, so we are looking at from only one
190 1 It's a simple question. 2 A Again, I understand you -- you think it's a 3 simple question; but "contemporaneously" is what you 4 add in that makes it a complex question, in part, 5 because now I have to think about whether the 6 specification itself provides any pointers as to 7 whether the -- I -- I -- my memories are storing 10 8 threads, for each of those 10 threads, only 9 50 percent of the instructions have been received, 10 or no, it must necessarily, for example, store 5 11 threads, all of the instructions have been fully 12 received, and I don't know. 13 I -- I -- I -- I hon- -- truly don't know. 14 This was not important to my opinion as far as 15 invalidity was concerned. Maybe it's important in 16 some other context that I'm thought aware of; but as 17 far as I'm concerned, to the -- going back to the 18 issue of invalidity in view of Studdard, this is not 19 a point that matters. 20 Q Well, it -- it does matter because if the 21 memory device -- if -- if thread means that the 22 memory device has to store all of the instructions 23 of each thread that is -- that the claim requires to 24 be stored in the memory device, then Studdard 25 doesn't disclose that every single instruction	192 1 instance, one point in time, right? 2 MR. RIZK: Okay. 3 THE WITNESS: So when I look at it over 4 time, of course the memory has to receive and store, 5 some form, all of the pixel command instructions 6 associated with the pixel command thread. 7 The question is does it have to be that at 8 any given point in time, if I look at the content of 9 the memory, all the instructions associated with 10 that thread are there at the same time, and that's 11 the one that I don't read in the claim and that's 12 the one that I didn't see anything in '381 that 13 points to it. I can go back and check. 14 MR. RIZK: You mean '053, just to clarify 15 your testimony. 16 THE WITNESS: '053, yes, sir. 17 BY MR. RIZK: 18 Q All right. So where in your report -- so 19 going back to where we were before -- we're still on 20 the memory device of Studdard -- you don't 21 demonstrate that prior to the selection -- let me -- 22 let me back it up. 23 You would agree with me that for a sequence 24 of commands to qualify as a thread in the context of 25 the '053 patent, its first instruction must be in

193 1 execution, correct? 2 MR. JOHNSON: Objection; form. 3 MR. RIZK: I'll try it -- let me withdraw 4 it and state it another way. 5 Q A sequence of commands applicable to vertex 6 processing is not a thread until it begins 7 executing, correct? 8 A No, sir, I -- I cannot agree with you this. 9 I don't know where -- what -- what even that means. 10 A -- a -- a thread is what it is, a sequence of 11 commands or instructions; and -- and this -- this 12 has -- I don't see any bearing on whether its first 13 instruction is being executed or some of its 14 instructions is being executed for it to be a 15 thread. 16 I mean, I understand there is a task that 17 comes in, comes as -- as -- potentially as multiple 18 threads, and these multiple threads are received and 19 stored in the memory either contemporaneously or 20 otherwise, which I don't want to opine on; but that 21 is -- has nothing to do with whether the -- those -- 22 those threads are being executed for each to 23 constitute a thread. 24 Maybe you're referring to like software 25 thread versus hardware thread and stuff like that,	195 1 Q So turning to the arbiter element of 2 Studdard where you -- you allege that Studdard 3 discloses an arbiter -- that shows up -- you provide 4 your opinions in Paragraphs 117 through 118 of your 5 report on the arbiter element, correct? 6 A Yes, sir. 7 Q And in your report, you point to the thread 8 scheduler 1025 and -- and thread processors 1026 as 9 the alleged arbiter, correct? 10 A Yes. 11 Q Okay. You don't identify other structures 12 as the alleged arbiter in your report. I think 13 Paragraph 117 is where you set forth your opinion 14 about what the alleged arbiter is. 15 A No, I do not. 16 Q Okay. And the -- in your report, you don't 17 cite to any evidence that the alleged arbiter thread 18 scheduler 1025 and thread processors 1026, are 19 configured to select between at least two pixel 20 command threads and at least two vertex command 21 threads, for a total of four threads, do you? 22 A No, I do not. 23 Q And that's not a requirement that you 24 applied as a person of ordinary skill in the art in 25 determining whether or not the claim limitation 1-B
194 1 but I'm not sure what you mean. You have to make it 2 more precise to me what you mean. 3 Q Okay. We'll, I'm -- I'm referring to any 4 context of a thread, the context in which the ALJ 5 construed the term "thread." 6 So is it your -- for the lens that you 7 applied as a POSITA interpreting the term "thread" 8 and applying the ALJ's construction, it is your 9 belief that a thread can exist prior to its -- 10 the -- the execution of any commands within the 11 thread? 12 A Again, this is not something that I -- I 13 have considered as being necessary or -- or -- or 14 important when I formed my opinion. I still believe 15 that this is a hypothetical question related, 16 perhaps, to some other context that I'm not aware 17 of. 18 But -- but regardless, when I read your 19 question, I -- I would not make a requirement for a 20 thread to be formed to exist to the fact that it's 21 being executed or not. It may be an execution 22 state, may still not be an execution state. 23 It is, of course, being received to be 24 executed, but may not -- the execution on that 25 thread may have not begun.	196 1 was met, correct? 2 A I didn't even consider it. I did not apply 3 that requirement to choose one thread from among 4 four different threads, two of them pixel type, two 5 of them vertex type. 6 I did not consider it and I did not opine 7 on it. 8 Q Okay. And I'll direct your attention to -- 9 sitting here now, you -- you don't have an opinion 10 on that, correct? 11 A I understand this is some of the -- I guess 12 the language that ALJ has used, although they didn't 13 construe the term, but this is some things that was 14 said, but I did not read it as a claim construction 15 order, that this is how you should really define the 16 function of an arbiter. 17 Q Okay. All right. Moving on to Claim 5 of 18 the '053 patent, and you provide your analysis on -- 19 Actually, before we move there, you provide 20 your analysis for Dependent Claims 2 through 4 in 21 Paragraphs 119 through 123 of your report, correct? 22 A Yes, sir. 23 Q That's where you provide your analysis for 24 Studdard? 25 And then Paragraph 124 is where you begin

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197 1 your analysis for Independent Claim 5 of the '053 2 patent invalidity based upon Studdard, correct? 3 A Yes, sir, that's correct. 4 Q Okay. And for the command processing 5 engines, you identify for each command processing 6 engine the processing block 106 of Studdard 7 corresponding to each command processing engine, 8 correct? 9 A You're talking about Dependent Claim 2 now? 10 Q No; I'm talking about Claim 5 -- 11 A Oh. 12 Q -- which has 5-C, a plurality of command 13 processing engines, and they're coupled to the 14 arbiter. 15 If it's helpful, I'd refer you to 16 Paragraphs 119 through 120 of your report, which is 17 Dependent Claim 2. 18 A Yeah, that's what I was doing, yes. 19 Yes, that's correct, so in the context of 20 Claim 2, but also in Claim 5, Independent Claim 5, 21 corresponding element, I've identified this command 22 processing engine to comprise of the plurality of 23 processing blocks 106. 24 Q Okay. So I just want to -- I want to be 25 clear. You're -- you're alleging that -- your --	199 1 store -- 2 THE STENOGRAPHER: I'm sorry. 3 MR. RIZK: Sorry. Let me withdraw that. 4 Q The command thread that is referred to in 5 Element 5-C is the command thread that is selected 6 by the arbiter of Element 5-B, correct? 7 A Yes. 8 Q Okay. And the selected command thread -- 9 well, let me try it a little bit differently. 10 Each of the plurality of command processing 11 engines has no control over whether the claimed 12 arbiter selects a pixel command thread or a vertex 13 command thread, correct? 14 A That is correct, yes. 15 Q Okay. So each of the command processing 16 engines must be operable to receive and process 17 whatever command thread is provided to it by the 18 arbiter, correct? 19 A Certainly this is one possibility, that the 20 issue of the plurality of the command processing 21 engines will process the command thread that's 22 passed through it. 23 Q Each command processing engine must be 24 operable to receive and process the command thread 25 passed to it by the arbiter, correct?
198 1 your opinion is that each processing block 106 2 corresponds to one of the plurality of the command 3 processing engines as required by the claim. 4 That's -- that is, your map. You're 5 mapping a command processing block to -- I'm 6 sorry -- a processing block 106 to a command 7 processing engine in the claim. 8 A Yes. 9 Q You're not mapping something else to the 10 command processing engine; each -- each command 11 processing engine, in your opinion, corresponds to 12 a -- a single processing block 106? 13 A Yes. 14 Q And for each of those single processing 15 blocks 106 -- we can stay on -- actually, why don't 16 we go to Claim 5, since we were there before. 5-C 17 in particular. 18 Do you see that Claim 5-C requires each of 19 the plurality of command processing engines be 20 operable to receive and process the command thread? 21 A Yes, sir, I do. 22 Q Okay. And the command thread that is being 23 referred to is the command thread that is recited in 24 claim -- the same claim, a plurality of pixel 25 command threads and a second portion operative to	200 1 A Yes, that's correct, yes. 2 Q The -- a pixel command thread or a vertex 3 command thread, correct? 4 MR. JOHNSON: Objection; form. 5 THE WITNESS: I mean, yes, I -- I -- I can 6 agree to this, although, again, as I said, this is 7 one possibility, so there -- there are other 8 possibilities also, but this is certainly one 9 possibility. 10 MR. RIZK: The claim says that each -- 11 that's what -- I'm just reading what the claim says. 12 Q Do you agree? 13 A Yeah, I -- 14 MR. JOHNSON: Objection; form. 15 MR. RIZK: I'm not -- I'm not reading -- 16 I'm not trying to read a possibility from the claim, 17 I'm reading literally what the claim says; and the 18 claim says that each of the command processing 19 engines has to be operable to receive and process 20 whichever of the vertex command threads or pixel 21 command threads were selected by the arbiter. 22 MR. JOHNSON: Objection; form. 23 BY MR. RIZK: 24 Q Correct? 25 A I mean, so -- so the -- the -- a little bit

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201 1 of the nuance here is that -- I want to bring it up, 2 and that's the reason I hesitate. 3 So when you read the Claim 5-B, I 4 understand there's an arbiter and that the arbiter 5 is operable to select a command thread from either 6 the plurality of the pixel command threads or the 7 plurality of the vertex command threads; and it is 8 also possible that the plurality of the command 9 threads that's being presented to the arbiter is 10 homogeneous comprising of pixel command threads 11 only, or it is homogeneous comprising of a plurality 12 of vertex command threads only; so therefore, when I 13 look at Claim 5-B in combination with Claim 5-C, 14 there is this possibility that, in fact, a system 15 would read on this Independent Claim 5 where the 16 system has been set up in such a way that the 17 arbiter at any point in time is only presented with 18 pixel command threads from which it's going to 19 select one and pass it on to be processed by these 20 command processing engines, and then a completely 21 different point in time, it's presented with a 22 plurality of vertex command threads and picks one 23 and sends it to the command processing engine. 24 Under that possibility, then the command 25 processing engines themselves may not -- may have	203 1 Q So if, as the ALJ noted, the claim itself 2 requires a selection of a single command thread from 3 among at least four such threads, two or more pixel 4 threads and two or more vertex threads, do you 5 understand that assumption I'm asking you to make -- 6 A Yes, sir. 7 Q -- which is the ALJ's guidance? 8 Do you understand it? 9 A Yes, I do. 10 Q With that guidance, when you apply it, then 11 you would agree with me that each engine of the 12 plurality of command processing engines of 13 Element 5-C must be operable to receive and process 14 whichever command thread is provided to it by the 15 arbiter, be it a pixel command thread or a vertex 16 command thread? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: It seems right. 19 BY MR. RIZK: 20 Q Okay. Now, in your analysis and your 21 invalidity analysis of Studdard, you don't state in 22 your opinion that's expressed in your expert report 23 whether the alleged command processing engine 24 processes both pixel command threads and vertex 25 command threads, do you?
202 1 specialized to do pixel processing or to do vertex 2 processing because the ones which are specialized to 3 do vertex processing will do the vertex threads, and 4 similarly for the pixel threads. 5 I do give you the possibility that you 6 describe, but there is another possibility. To me, 7 the scope of this claim is broader than what you 8 described. 9 Q Agree or disagree, the -- the claim itself 10 requires a selection of a single command thread from 11 among at least four such threads, two or more pixel 12 threads and two or more vertex threads. 13 MR. JOHNSON: Objection; form. 14 THE WITNESS: To me, two -- two command 15 threads is enough to -- to assign meaning and 16 understand the scope of this claim. 17 I understand ALJ, in its order, discussed 18 this four-thread combination, but it did -- did not 19 construe -- construe it to make it a requirement. 20 It's just this comment box showing the -- the -- the 21 Honorable Judge's thinking at the time, but I -- it 22 was not construed as a required thing that I have to 23 apply, so I did not adopt that construction because 24 it was not construed that way. 25 MR. RIZK: Okay. Well, let's apply it.	204 1 A I did not take it as a requirement that the 2 command processing engine must process or be capable 3 of or operate to process both pixel command threads 4 and vertex command threads; although I must say that 5 if you look at some of the dependent claims -- for 6 example, Claim 6 that comes -- emanates from 7 Claim -- Independent Claim 5 -- when you have, for 8 example, your command processing engine comprising 9 an arithmetic logic unit, by definition, an 10 arithmetic logic unit is -- provides a complete set 11 of functionality, meaning that an arithmetic logic 12 unit, by definition and construction, as used in 13 practice by a person skilled in the art, can do 14 anything, any kind of processing, right? 15 Because all processing is negation, and 16 gate, or gate. That's it, there is nothing else. 17 All processing in the world is that, all 18 decomposable at the fundamental level to that. This 19 is called complete basis for functions, right? 20 Executing functions. 21 So it's a complete machine itself once it 22 has an arithmetic logic unit as known by a person 23 skilled in the art; but -- but -- but that's not 24 going to be efficient, right? So in terms of 25 performance efficiency, it's not going to be there

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205 1 to use ALU only to do both pixel and vertex and 2 everything else how it can be done. 3 So it's not a surprise to me if we come 4 back and say "Well, consider the command processing 5 engines, all of them being able to do at the very 6 fundamental level all kinds of processing, including 7 pixel and vertex -- vertex processing." 8 That's not going to be efficient. 9 Q Okay. So just to be clear, though, you 10 don't provide an opinion in your report -- I'm 11 looking at Paragraph -- you cross-reference Claim 2, 12 for example, of the Dependent Claim 2; and -- and 13 that's where you say you should -- in Paragraphs 119 14 through 121, you don't provide an opinion in those 15 paragraphs that each processing block processes both 16 pixel and vertex threads. 17 A I have a statement here on 121 that says 18 these processor elements 1061 process -- process 19 both pixel and vertex command threads, so it's 20 there. I -- I basically allow for that possibility. 21 I'm not excluding -- again, I hope you are 22 not taking my testimony today as excluding that 23 possibility. I don't. I'm just saying there are 24 other possibilities; and the scope of the claim is 25 broader than that, as I read it; but my opinions	207 1 a single command thread from among at least four 2 such threads, two or more pixel threads and two or 3 more vertex threads, so the selection must be based, 4 at least in part, on considerations other than 5 merely the command thread type, then in that 6 circumstance, you would agree that Element 5-C would 7 require each of the engines to process both pixel 8 and vertex threads? 9 MR. JOHNSON: Objection; form. 10 THE WITNESS: Yes, I do. 11 MR. RIZK: Okay. Let's move to Page 68 of 12 your report; and that's the beginning of the section 13 on Kimura for the '053 patent. 14 All right. And for Kimura, there are 15 certain stricken sections that I think we've noted 16 before. 17 THE WITNESS: Yes. 18 BY MR. RIZK: 19 Q And the opinion that you provide for 20 invalidity based on Kimura shows up between Pages 68 21 to 77, subtracting out the stricken sections, 22 correct? 23 A That is correct, yes. 24 MR. JOHNSON: Can we take a break if you're 25 going to start --
206 1 remain the same whether the scope is limited to this 2 that each and every one of the blocks can do both 3 pixel and vertex command processing or that they are 4 specialized such that some functions are performed 5 with high performance on one type versions on other 6 type. That's all. 7 Q And -- and, Doctor, to be clear, the 8 citation in your report that you referred to when 9 you said you were -- that you -- in your report, it 10 says that the -- the processing blocks 106 perform 11 both; but what you refer to in the sentence is these 12 processor elements 1061 process both pixel and 13 vertex commands threads, correct? 14 A Yes, that's correct; but one follows from 15 the other because the processing block comprises of 16 these -- multiple of these processing elements, 17 1061, so if the lower levels of the hierarchy, the 18 processing elements, can do it, therefore, the 19 higher levels, which are the processing blocks, 20 should also be able to do it. There's no 21 inconsistency there. 22 Q Just to be -- so we have the record clear, 23 you would agree with me that if we apply a 24 requirement to the claim, which is -- I'll read it. 25 If the claim itself requires a selection of	208 1 MR. RIZK: Sure. 2 THE VIDEOGRAPHER: Stand by. 3 We are off the record. The time is now 4 1451 p.m. 5 (A recess was taken from 2:52 p.m. 6 to 3:00 p.m.) 7 THE VIDEOGRAPHER: And we are back on the 8 record. The time on the video monitor is 1500 9 hours. 10 BY MR. RIZK: 11 Q Doctor, Kimura is not directed toward a 12 graphics processing unit, correct? 13 MR. JOHNSON: Objection; form. 14 THE WITNESS: I disagree. In my report I 15 say it is my opinion that Kimura is directed to a 16 graphics processing system. 17 But can we first find it? I'm sorry. 18 Which tab is it? 19 MR. RIZK: Okay. So you start on 20 Paragraph 166 of your report, and Kimura is Tab -- 21 THE WITNESS: I found it. Thank you. 22 MR. JOHNSON: What tab is it? 23 MR. RIZK: 11 of Exhibit 2. 24 Q Kimura doesn't mention graphics processing 25 unit anywhere, correct?

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209 1 MR. JOHNSON: Objection; form. 2 THE WITNESS: Again, in my report, I 3 provide citation to Column 1, Lines 9 -- sorry -- 4 Lines 54 to 67. Specifically, if I read just a 5 subset of these lines here. 6 MR. RIZK: Well, let me read the whole 7 section you just cited. 8 THE WITNESS: Please go ahead. 9 MR. RIZK: All right? 10 It says (reading): 11 Being provided with three pairs 12 of the instruction fetching that's 13 501 and the decode units 502, the 14 multithreaded processor shown in 15 Figure 1 can fetch and decode three 16 instruction streams in parallel. 17 As for the relationship between 18 the three instruction streams and 19 the programs in the instruction 20 cache 500 or in the main memory 21 path shown in the figure, one 22 program may correspond to one 23 instruction stream, that is, the 24 three instruction streams are 25 generated by three programs, or one	211 1 in your report that supports that Kimura discloses a 2 graphics processing unit? Because it's not here 3 where you just pointed me to now. 4 It doesn't say it there, so where in your 5 report do you provide evidence that Kimura discloses 6 a graphics processing unit? 7 A So I cited this particular section in my 8 report, and I provided no other citations. 9 Q Okay. So you're not relying -- in your 10 report, you don't rely on anything else. 11 Would it surprise you, sir, that Kimura, in 12 fact, nowhere in its disclosure mentions graphics at 13 all? It doesn't use the term "graphics"? 14 Does that surprise you? 15 A No, it does not surprise me. 16 Q Does it surprise you that Kimura doesn't 17 use the term "pixel" anywhere in its disclosure? 18 A No, it does not surprise me. 19 Q You -- you understand that Kimura doesn't 20 disclose the term "pixel"? 21 A Correct, yes. 22 Q And it never discloses "vertex," correct? 23 A That's correct, sir. 24 Q Never discloses "vertex thread," correct? 25 A Correct.
210 1 program can -- may correspond to 2 multiple instruction streams, that 3 is, the three instruction streams 4 were generated by one program. 5 The latter includes the case 6 where one image processing program 7 is performed as multiple 8 instruction streams with respect to 9 different image data. 10 Did I read that correctly? 11 A Yes, sir, you did. 12 Q Okay. It doesn't mention graphics. The 13 term "graphics" is not in that excerpt that you 14 identified in your report, correct? 15 A Yes, that's correct. 16 Q It -- it does mention "image processing," 17 correct? 18 A Yes, it does. 19 Q Okay. And you could have a device that is 20 an image processor but not a graphics processor, 21 correct? 22 A It's a not a simple yes-or-no answer. 23 Q Where does Kimura say that there's -- you 24 pointed me to this section. 25 Is there another section that you identify	212 1 Q Never discloses "pixel thread," correct? 2 A Correct, sir, yes. 3 Q And, in fact, the system that is disclosed 4 in Kimura is an image processor, correct? 5 A It's not a simple yes-or-no answer. 6 Q You don't know. 7 Do you know one way or the other if the 8 system disclosed in Kimura was designed to be an 9 image processor? 10 A Again, it's not a simple yes-or-no answer. 11 I'd have to elaborate on this if you want me to. 12 Q If you can elaborate briefly -- 13 A Sure. 14 Q -- then that is fine. 15 A So the combination of Kimura's system being 16 able to do image proc- -- processing and at the same 17 time being able to do multiple instruction stream 18 generation by one program, that, to me, as a person 19 skilled in the art, would mean that the kind of 20 image processing that it's doing corresponds to the 21 functions that a graphics processor performs. 22 Q Well, it's possible that a system could do 23 image processing of multiple instruction streams 24 generated by a single program without performing 3D 25 graphics processing, correct?

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213 1 A Yes, it's possible. 2 Q Okay. With -- you're familiar with the 3 field of image compression, right? 4 A Yes. 5 Q Video compression and image compression? 6 A I've written papers on it, yes. 7 Q Okay. And image processors, one of their 8 functions is to perform processing on multiple 9 instruction screens generated by a single pro- -- 10 program, but they don't work with graphics 11 processing, correct? 12 A You called video compression and image 13 compression as examples of image processing. That's 14 typically not how the term is used. 15 Q Okay. What would you understand to be an 16 image processor? 17 A One example is graphics processor. 18 Q So you understand image processor and 19 graphics processor units to be the same thing? 20 A Not exactly, no. 21 Q Okay. What's the difference between a -- 22 an image processor and a graphics processor? 23 A So, for example, you might have something 24 in the frame buffer and you want to actually use a 25 controller to display it on the screen. You are	215 1 discussed and described in Kimura. 2 Q So if a graphics processing unit is 3 understood in the art as taking a 3D scene and 4 displaying it on a two-dimensional screen, there's 5 not what Kimura discloses, correct? 6 MR. JOHNSON: Objection; form. 7 THE WITNESS: A -- a graphics processing 8 unit could do many things, including 2D, but also 9 3D. It can do even different types of 10 general-purpose computing, in some cases, like 11 GP GPUs, general purpose graphics processing units. 12 So it has a lot of different functionality 13 it can perform; so to limit a graphics progress unit 14 to only do 3D rendering is -- is just one example, 15 it could be just one example, but not the full 16 scope. 17 MR. RIZK: Yeah. So let's -- let's try it 18 this way. 19 Q If we define the term GPU to at least 20 require the taking of a 3D scene and displaying -- 21 displaying it on a two-dimensional screen to have 22 that minimum requirement -- it can do other things, 23 but as that minimum requirement, Kimura doesn't 24 disclose that type of a GPU? 25 A It does not explicitly teach it. No, it
214 1 not -- it's -- it's doing some kind of image 2 processing, but it's not doing graphics processing 3 as such, potentially, yes; but that doesn't mean -- 4 yes. 5 Q Graphics processing generally involves the 6 conversion of a 3D model defined by verticis into a 7 2D representation of pixels on the screen, correct? 8 A Not necessarily. 9 I mean, graphics -- yeah, not necessarily. 10 Q How about 3D graphics processing? 11 A Correct, I would agree to that. 12 Q Okay. So you would agree with me that an 13 image processor is different than a 3D graphics 14 processor? 15 A That's not what I've said. 16 Q Kimura doesn't disclose the conversion of a 17 3D model defined by verticis into a 2D 18 representation of pixels on the screen, does it? 19 A No, sir, it does not. 20 Q Okay. So it does not disclose graphics 21 processing in that context, correct? 22 A If -- if -- if you limit the graphics 23 processing to be 3D processing involving taking a 3D 24 scene and displaying it on a two-dimensional screen, 25 I -- I -- I don't see that being explicitly	216 1 does not. 2 Q And you wouldn't understand as a person -- 3 if -- if that is the definition that we're going to 4 ascribe to GPU, which is, at a minimum, takes a 3D 5 scene and displays it on a two-dimensional screen, 6 you wouldn't understand the phrase "image processor" 7 to necessarily provide that minimum functionality, 8 correct? 9 A Not necessarily. 10 Q Okay. And turning to your -- the portion 11 of your opinion on Kimura related to the -- the 12 memory device, the structure that you identify 13 corresponding to the memory device of Element 1-A is 14 the cache memory 100, correct? 15 If it's helpful, you can look at 16 Paragraph 167 of your report. 17 A Yes, that's correct. 18 Q You don't identify other structures, right? 19 A Yes. 20 Q And then turning to Element 1-B of your 21 report, which shows up on -- starts on 22 Paragraph 173, the alleged arbiter that you point to 23 is the combination of the instruction issue control 24 unit 150 and a priority control unit 60, correct? 25 A That is correct, yes.

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217 1 Q Okay. And in your view, those two -- those 2 two structures in Kimura combined make up the 3 claimed arbiter, correct? 4 As a person of ordinary skill in the art, 5 that's how you see it? 6 A Yes, sir. 7 Q Okay. And you would agree with me that 8 those arbiter -- those structures that you 9 identified, the instruction issue control unit 150 10 and priority control unit 60, have no information as 11 to whether the arbitrated threads are pixel command 12 threads or vertex command threads? 13 A That is correct, yes, sir. 14 Q They do not consider whether the arbitrated 15 threads are pixel command threads or vertex command 16 threads in making the selection, correct? 17 A The arbiter does not, yes. 18 Q Okay. And in your view as a person of 19 ordinary skill in the art, a -- in other words, to 20 satisfy the claimed arbiter element, Element 1-B, 21 the arbiter need not arbitrate based upon whether 22 the thread is a pixel command thread or a vertex 23 command thread, correct? 24 MR. JOHNSON: Objection; form. 25 THE WITNESS: So when -- need not arbitrate	219 1 If I'm referring to the Jao reference that 2 is in the file history, I'll specifically note that 3 patent number. 4 A I appreciate it. 5 Q But if I'm otherwise using the -- the term 6 "Jao" without specifically mentioning the patent 7 number, then I am -- I am referring to the -- the 8 Jao reference that you relied upon for your 9 invalidity opinion, which is, for the record 10 8,319,774. 11 So if I'm referring to the Jao reference 12 that you've relied upon, I will just say Jao; 13 otherwise, I'll call out the patent number and it 14 will be different than -- 15 A Very good. I appreciate it. Thank you. 16 Q Okay. So your -- your invalidity opinion 17 based upon Jao is stated in Paragraphs 216 through 18 253 of your report, and that appears 80 -- Page 86 19 through Page 105, except for the stricken 20 paragraphs, obviously, correct? 21 A Yes, sir. 22 Q Okay. And for Jao, you identify for the 23 first processing unit element the computational core 24 204 as the structure corresponding to the first 25 processing unit of the '381 patent; is that right?
218 1 based on whether the thread is a pixel command 2 thread or a vertex command thread, correct. 3 MR. RIZK: Okay. So let's move on to the 4 dependent claims. 5 Q You provide your analysis and opinion 6 concerning the validity of the dependent claims in 7 Paragraphs 180 through 192 with respect to Kimura, 8 correct? 9 A Yes, sir. 10 Q And let's go to Page 78 of your report, 11 please. 12 A Yes, I'm there. 13 Q Page 78 of your report is where you begin 14 to provide an overview of the prior art references 15 that are part of your opinion in connection with 16 invalidity of the '381 patent, and that continues 17 through Paragraph 215, which is on Page 86, correct? 18 A Yes, sir. 19 Q And your -- the -- the substance of your 20 opinion concerning invalidity of the '381 patent 21 based upon the Jao (phonetic) reference. And to be 22 clear, throughout the day today, when I refer to Jao 23 -- there are Jao references -- 24 A Yes. 25 Q -- at issue here.	220 1 I'll withdraw that question and restate it. 2 It says should be a pretty short question. 3 The structure you identified in Jao as 4 corresponding to the first processor unit is 5 computational core 204, and that's in Paragraph 220 6 of your report? 7 A That's correct, yes. 8 Q And then the structure that you identify as 9 the -- as the second processing unit is the command 10 stream processor 406; is that correct? 11 A Yes, sir. 12 Q Okay. And the structure that you identify 13 as the scheduling module of Jao is the EU pool 14 control and vertex stream cache 206, correct? 15 A Yes, sir. 16 Q Okay. And you would agree with me that the 17 structure that you -- you identify as the alleged 18 engines are the vertex shader 304, geometry shader 19 306, and pixel shader 310? 20 A Yes, sir. 21 Q Correct? 22 Okay. And those alleged engines, 304, 306, 23 and 310, and the EU pool control vertex stream cache 24 206, they all reside within the same graphics 25 processing unit, correct?

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221 1 A Yes, they are all receiving graphics 2 processing unit 114, I guess you're talking about, 3 or you're talking -- which is our main -- there are 4 numbers associated with these. 5 They're a part of 202, right? A system 6 called 202, but -- 7 Q Yeah, they're -- they're all part of the 8 same graphics processor 202, correct? 9 A Yes. 10 Q So you would agree, then, that EU pool 11 control 206 and the alleged engines VS-304, geometry 12 shader 306, and pixel shader 310 are associated with 13 the same processing unit graphics processor, which 14 is 202, correct? 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: In -- in the context of the 17 claim, I do not equate the processing unit with a 18 processor, as the term you have used, so -- so the 19 answer is not exactly. 20 BY MR. RIZK: 21 Q Okay. What is the basis of your testimony 22 that you do not equate a graphics processor with a 23 processing unit? 24 MR. JOHNSON: Objection; form. 25 THE WITNESS: So the -- the "processing	223 1 Q Okay. And the computational core 204 and 2 the EU pool control 206 are associated with the same 3 processing unit 114, correct? 4 A Yes. 5 Q Okay. And that didn't factor into your 6 opinion that the EU pool control 206 and 7 computational core 204 are associated with different 8 processing units? 9 A It did factor in. 10 Q Okay. In your opinion, you -- you opine 11 that computational core 204 and EU pool control 206 12 are associated with different processing units, 13 correct? 14 A Yes, I -- 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: So -- so I identify these two 17 elements, the computational core 204 and EU pool 18 control 206, as you summarized before where the EU 19 pool control 206 is my scheduling module, which is 20 associated with the second processing unit that is 21 the command stream processor 406, and then I 22 identified the computational core 204 to be the 23 first processing unit. 24 I noticed and I realized that these two 25 processors that I've identified as first and second
222 1 unit" has been used in this claim language. 2 "Processor" is not used, so I only am looking at, in 3 a prior art reference, to see if there are elements 4 of -- that's been disclosed there that correspond to 5 first and second processing units, and that's what 6 I've done. 7 Q Okay. 8 A I did not look for processors. 9 Q All right. Let me try it this way, then. 10 Do you see on Figure 2, there's a GPU 114? 11 Figure 2 of Jao. And if it's helpful, that's Tab 16 12 of your Exhibit 2, and it's identified as Exhibit 16 13 to your report. 14 A Yes, sir. 15 Q Do you have Figure 2 -- 16 A Yes, I do. 17 Q -- of Jao in front of you? 18 A Yes. 19 Q Do you see GPU 114? 20 A Yes. 21 Q Okay. That stands for graphics processing 22 unit, correct? 23 A Yes. 24 Q That's a processing unit, correct? 25 A Yes, sir.	224 1 processing units are within 202, which is the 2 graphics processor of Jao reference, but Jao system 3 is a multiprocessor system, has multiple other units 4 inside of it, processing units inside of it, and so 5 my construction is valid, or my -- my 6 interpretation, to me, is valid. 7 BY MR. RIZK: 8 Q Well, there's only one graphics processor 9 202 in GPU 114. Figure 2 only shows 1, do you 10 agree? 11 A Yes, I -- yes, I do. 12 Q Okay. And there's only one GPU in the 13 system depicted in Figure 1 of Jao? 14 A We have no disagreement there, yes. 15 Q Okay. So it's your opinion that the EU 16 pool control 206 and computational core 204 can be 17 both associated with the same processor and 18 associated with different processing units at the 19 same time? 20 That's your -- that's your testimony today? 21 A So -- 22 MR. JOHNSON: Objection; form. 23 THE WITNESS: Not exactly. 24 MR. RIZK: Well, you testified earlier 25 today that computational core 204 and EU pool

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225 1 control 206 are associated with the same processing 2 unit 114. 3 Q We're in agreement about that, right? 4 A We do not disagree there. 5 Q Okay. And at the same time, you testified 6 that EU pool control is associated with a different 7 processing unit than the computational core 204. 8 A Yes, that's also correct. 9 Q So you -- you interpret the -- the phrase 10 associated with a first processing unit or 11 associated with a -- and associated with a -- a 12 second processing unit to not necessarily exclude 13 the possibility that the scheduling module and the 14 engines might also be associated with the same 15 processing unit? 16 A So, again, maybe there is a 17 misunderstanding either on your part or mine, I'm 18 not sure; but when -- when you first asked me 19 associated with, I assumed the meaning you intended 20 is that these components 204 and 406, which are the 21 first and second processing units of Jao, are 22 contained within a more complex system, which is 23 called a graphics processor 202, which itself is 24 contained inside GPU 114. 25 So when I said "association" in that sense,	227 1 components. 2 I'm just looking at the claim, looking at 3 the language of the claim, and looking at the prior 4 art, seeing what elements in the prior art 5 correspond to which limitation, and -- and -- and 6 which component of the asserted claims. 7 So that's the methodology I'm using here, 8 and -- and -- and so here, whether you call 202 a 9 graphics processor or a graphics processing unit X, 10 and then call GPU a graphics processing unit Y or 11 just GPU, it -- it doesn't matter to me. 12 In my interpretation of this, looking at 13 the claim, asserted claim, and elements of that, and 14 see which of the components in Jao actually 15 corresponds to these various elements, and -- and, 16 to me, the fact that you have a command stream 17 processor and a computational core 204 inside a 18 graphics processor 202 or inside the GPU 114, it 19 just means that this is a multiprocessor system and 20 I just need to identify within that system what 21 processors respond to which elements of the claim. 22 Q Well, that's not what you said before, sir, 23 respectfully. 24 Your testimony was that -- and I'll quote 25 you. You "said I do not equate a processing unit
226 1 that's what I meant. 2 Q Okay. And just -- 3 A But -- but -- but so there is -- I'm sorry. 4 Let me finish. I'll try to be brief. 5 But, in fact, in -- in addition to this 6 containment relationship, which I acknowledge, there 7 is an association -- functional association between 8 the EU pool control unit, which is the arbiter, and 9 a second processing unit, which is command stream 10 processor 406, and an association and an 11 identification of a first processing unit, which is 12 204. 13 All of these are contained inside the 14 graphics processor 202. 15 Q Okay. Graphics processing unit 114, 16 that's the -- I think that that's the processing 17 unit where we would agree together that both EU pool 18 control and computational core 204 are associated 19 with the same graphics processing unit 114. 20 I thought your earlier testimony was you 21 don't agree that graphics processor 202 is a 22 processing unit. 23 A It's -- it's not a matter of terminology 24 here. I'm not trying to sort of create sort of 25 differences based on the names I assigned to	228 1 with a processor." 2 A In the context of the claim. I'm sorry. 3 Q That was your testimony, that you did not 4 equate a processor with a processing unit. 5 Is that not your testimony? 6 A Yes, it was. 7 Q Okay. 8 A But it was in the context of the -- 9 Q Okay. 10 A -- the claim language. 11 I'm saying the claim language requires the 12 first processing unit, it doesn't require a 13 processor, so let's not confuse the two. 14 Q Okay. And so let's -- let's take that. 15 I -- I happen to agree with you that we -- we 16 shouldn't confuse the two. 17 And you would agree with me that the 18 command stream processor 406 does not say command 19 stream processing unit, correct? 20 A Yeah, the name is not that. 21 Q Okay. So we shouldn't equate it, then, 22 with a processing unit? 23 A That's wrong. You are misreading my -- my 24 statement. That's not what I meant. 25 If you want me -- you understood it this

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229 1 way, I am correcting it now. So that's not what I 2 meant. 3 The -- the -- the name I use to call a cat 4 doesn't matter. The cat is a cat by itself. 5 Whether I call it in French one word or in German 6 another word, it doesn't matter. 7 So here we are talking about claim with 8 specific components, elements, first processing 9 unit, second processing unit. I find a component in 10 Jao that actually corresponds to this, performs the 11 same functions and has the same kinds of 12 relationship to other components and elements of the 13 claim, I identify it. 14 Whether that component is called processor 15 or processing unit or cat or -- it doesn't matter. 16 Q Well, when I asked you about this graphics 17 processor 202, and I asked you whether or not that's 18 a processing unit, you said "I do not equate the 19 processing unit with a processor, so the answer is 20 not exactly." 21 So at least in the context of this graphics 22 processor 202, you did not equate that with a 23 processing unit as that term is used in the claim? 24 A So, sir, what I'm saying -- 25 MR. JOHNSON: Objection; form.	231 1 other; and so when I try to see if this claim is 2 rendered obvious or anticipated by some other prior 3 art reference, the methodology I use, I read to 4 understand what the claim is in the specs, then I 5 look at the prior art, I understand it, I look at 6 the claim constructions that the judge has issued, I 7 understand and apply it and then try to create an 8 association between what I find in the prior art 9 reference and what I find in different claim 10 elements. 11 And the association I found is what I've 12 described in my report. In that association, I was 13 able to identify the command stream processor 406 14 that might have been called Object X -- right? -- 15 or cat, or command stream processor, or command 16 stream processing unit, or whatever else you like. 17 I identify that component in Jao to read on 18 the second processing unit of the asserted claim. 19 Similarly, I identified the EU pool control and 20 vertex stream cache 206 in Jao reference to perform 21 the same function, have the same association, and so 22 on and so forth, as the arbiter that we need, and so 23 on and so forth. 24 So that's the process I've used. If you 25 disagree with it, please let me know --
230 1 MR. RIZK: Let me -- I'm going to -- I'm 2 going to -- I'll ask you the question now. All 3 right? So here is the question for you. 4 Q What is -- what makes the -- the -- the -- 5 why is it that the graphics processor 202 is not a 6 processing unit by the command stream processor 406 7 is a processing unit? 8 MR. JOHNSON: Objection; form. 9 BY MR. RIZK: 10 Q What's the -- let me withdraw that. 11 What is the difference between the graphics 12 processor 202 and the command stream processor 406 13 that qualifies the command stream processor as a 14 processing unit but does not qualify the graphics 15 processor 202 as a processing unit? 16 A So, sir, the issue -- can I answer? 17 Q Go ahead. 18 A And it's not a yes-or-no answer. 19 Q I didn't ask you for a yes-or-no answer in 20 this case. 21 A So I'm looking at Claim 15. It has 22 multiple elements; and within these multiple 23 elements, there are many different components 24 that -- that have been referenced with a particular 25 functional description and association with each	232 1 Q Okay. I don't disagree with your process, 2 but what I do disagree with is that you're still not 3 answering my question. You answered whatever you 4 wanted to answer, which wasn't my question. 5 My question is what is the difference 6 between the command stream processor 406 and the 7 graphics processor 202 that makes the command stream 8 processor 406 qualify as the claim processing unit 9 but the graphics processor 202 does not qualify as a 10 claim processor? 11 MR. JOHNSON: Objection; form, 12 mischaracterizes testimony. 13 THE WITNESS: And -- and the answer is the 14 graphics processing -- processor 202 does not have 15 all the required elements, functional and 16 association-wise, as what a second processing unit 17 in this claim should be. 18 BY MR. RIZK: 19 Q Okay. And what is -- what is the 20 requirements of a second processing unit as the 21 claim requires that -- that qualifies the command 22 processor 406 to be a processing unit but not the 23 graphics processor 202? 24 A So the -- the requirement as described in 25 15-D is that there should exist a scheduling module

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233 1 that's associated with this second processing unit, 2 and that this scheduling module is providing a 3 plurality of tasks -- a plurality of tasks to a 4 plurality of engines where those engines are 5 included in or in a first processing unit, and -- 6 and this continues because now -- 7 Q So the only thing that you read into the 8 record that relates to whether or not something is 9 a -- is a processing unit is that it has to be 10 associated with a scheduling module, and the -- the 11 graphics processor 202 has within it the thing that 12 you call the scheduling module, so why isn't it 13 associated with a scheduling module and why doesn't 14 it qualify as the processing unit? 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: Again, so -- so -- I'm not 17 trying -- 18 MR. RIZK: You said it's not -- 19 THE WITNESS: I'm not sure -- yeah, I'm not 20 sure how to respond to this question. 21 I mean, if you have a -- a alternative 22 mapping between the elements of the claim and what 23 you find in Jao, you're welcome to present it; but 24 if you're asking about my mapping, this is what I've 25 done.	235 1 BY MR. RIZK: 2 Q Okay. So you would agree, then, that the 3 graphics processor 202 can qualify as a graphics 4 processing -- sorry -- as a processing unit? 5 A In some other context, yes; but not in the 6 context of this claim. 7 Q Why not? 8 A I'm looking at the context of the claim. 9 Again, sir, I've gone a mapping to you, so I've 10 explained carefully to you, to the best of my 11 ability, how it is that I think Jao actually 12 discloses all elements of the claim. 13 I've given you the mapping, and you're 14 saying why didn't you do it this other way? Explain 15 to me why you didn't -- well, that's not my job. I 16 mean, that's not the -- the -- my task at this 17 point. 18 I can try to tell you, and I did tell you. 19 I mean, I'm happy to again repeat this to you again. 20 To me, there are certain requirements -- 21 for example, for the first processing unit, it must 22 comprise a plurality of engines that are configured 23 to receive from a scheduling module associated with 24 the second processing unit a plurality of tasks -- 25 Q Okay.
234 1 MR. RIZK: Well, you -- 2 THE WITNESS: You're asking me what your 3 mapping is, and I'm telling you the mapping, and 4 you're saying but this mapping, you didn't do it 5 this other way. Why didn't you do it this other 6 way -- 7 MR. RIZK: That's not what I said, sir. 8 THE WITNESS: -- and I explained why -- 9 that's why -- 10 MR. RIZK: That's not what I said. 11 You -- you said that you would not equate 12 graphics processor 202 with a processing unit, but 13 you would equate -- sorry -- you wouldn't equate 14 graphics processor 202 with a processing unit, which 15 is what's in the claim, but you would equate 16 graphics processing unit 114 with a processing unit. 17 MR. JOHNSON: Objection; form, 18 mischaracterizes testimony. 19 MR. RIZK: That's what you -- that was your 20 testimony, sir. 21 MR. JOHNSON: Objection; form. 22 THE WITNESS: No, that's not my testimony. 23 If -- even if you think that was my 24 testimony, I'm correcting it now. 25 ///	236 1 A -- and also be able to load the state data 2 associated with the issue of the plurality of tasks. 3 I looked at Jao, I identified some 4 components to you, and you're saying why didn't do 5 you this other one? I didn't. 6 Q Well, you said "I don't equate graphics 7 processor 202 with a claim processor." 8 THE WITNESS: Sir -- 9 MR. JOHNSON: Objection; form. 10 MR. RIZK: So let's -- I'll put it to 11 you -- I'll -- I'll give you one opportunity to -- 12 to respond and, perhaps, correct your testimony. 13 Q You would agree with me that based upon -- 14 that the graphics processor 202 is a processing unit 15 that is associated both with EU pool control and 16 vertex screen cache 206 and computational core 204, 17 correct? 18 A So the graphics processor 202, which is 19 described fully or more carefully in more detail in 20 Figure 4 of the Jao reference, contains many 21 components; and those components include the ones 22 that you have mentioned here, which is the EU pool 23 control and vertex cache 206, computational core 24 202, command stream processor 406. 25 So they are all contained inside of it, but

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237 1 the -- the -- the -- the -- and you're saying that 2 means associated -- associated with. There is no 3 construction of associated with. 4 As I understand it, the association with 5 that has been used here is some kind of relationship 6 between the -- the component that's identified -- 7 that's been identified, or the two components that 8 are associated with, and it's not a simple 9 containment relationship. 10 But that's your -- your construction if 11 that's you would like to do. 12 Q No, I'm not -- I'm not the person who is 13 being deposed today. You're -- you're the one who 14 is answering the questions -- 15 A Yes. 16 Q -- and you're the one who has provided an 17 opinion in this investigation, sir. 18 A Yes. 19 Q I'm asking you to provide me with your lens 20 that you used when you were analyzing the prior art. 21 That's what I'm asking you for. 22 So would a person of ordinary skill in the 23 art consider -- and this is a yes-or-no question -- 24 EU pool control 206 and computational core 204 could 25 both be associated with the same processing unit,	239 1 scheduler. 2 Q Do you recall that? 3 A Yes. 4 Q Okay. And that OS scheduler, the -- the 5 processing unit that it is identified as associated 6 with is the host CPU of the '381 patent, correct? 7 A Yes. 8 Q And the -- the scheduling module actually 9 executes on the host CPU, correct? 10 A Yes. 11 Q So why isn't that the relationship that's 12 described by the '381? Because it seems to me that 13 if you look at the '381, the -- the -- the OS 14 scheduler, which is the scheduling module that's 15 claimed, doesn't exchange information with the CPU, 16 it's executing on the CPU and providing tasks to the 17 GPU, correct? 18 A You're correct, and your question is a good 19 one. I can answer it if you want, if you allow me. 20 Q I've received the answer that -- that I 21 need for now. I'll move on to other questions that 22 are related; and I'll give you an opportunity to add 23 to it, or your counsel can ask you follow-up 24 questions if I don't -- don't get to it. 25 In fact, there is no other disclosure of an
238 1 graphics processor 202? 2 A I mean, in view of the specification, I 3 would say no because when I look at the 4 specification, these components are typically 5 separate from each other, and so the containment 6 relationship was not really -- in my understanding 7 of the claim in view of the specs, was not the 8 meaning that was assumed or taken by the inventors, 9 it was more of a functional association between 10 these separate components that -- that has been 11 captured in this claim. 12 Q So what is the meaning that you ascribe to 13 "associated with" based upon your understanding of 14 the '381 patent and your -- your review? 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: So this -- so some kind of 17 information exchange between the two units that are 18 associated with each other -- I need some data, I 19 get it from you, so I -- I'm associated to you or to 20 that unit because of the kind of data exchange that 21 takes place between us. That's the meaning I would 22 take. 23 MR. RIZK: Now, in the context of the '381 24 patent, the scheduling module that's in Claim 15 25 corresponds to what the spec refers to as the OS	240 1 association in the '381 between the scheduling 2 module of the OS scheduler and its processing unit, 3 other than where it's a piece of software that 4 executes on the -- on the processing unit, correct? 5 A In that one embodiment, yes, sir. 6 Q Well, that's the only embodiment, sir. 7 A Correct. 8 Q Okay. But that's not the association that 9 you've identified in Jao. You've identified a very 10 different association. 11 You have it identified that the EU pool 12 control is a piece of software that's executing on 13 the command stream processor, correct? 14 A So there's no -- it's not a yes-or-no 15 answer. Do you want me -- you want my full answer? 16 Q Well, have -- have -- does the EU pool 17 control execute software on the command stream 18 processor? 19 A No, it does not. 20 Q Okay. Is the EU pool control software? 21 A Oh, is it software? 22 No, it's not software. 23 Q Is it an OS scheduler? 24 A No, it's not an OS scheduler. 25 Q Okay. The command stream processor, the

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241 1 information that comes out of it actually ends up 2 and has a function of controlling what goes into the 3 engines, correct? What goes into the alleged 4 engines? 5 A I'd like to check the portion of my report 6 related to second processing unit. 7 So I have quoted text from Jao that 8 describes what this command stream processor 406 9 does. I'll read it to you. 10 (Reading): 11 The command stream processor 12 406 provides triangled vertex 13 indices to the EU pool control 14 unit 206. In the embodiment of 15 Figure 4, the indices are 256 bits. 16 The EU pool control unit 206 17 assembles vertex shader inputs from 18 the stream cache and sends data to 19 the computational core 204, input 20 E. The EU pool control unit 206 21 also assembles geometry shader 22 inputs and provides these inputs to 23 the computational core 204, input 24 F. 25 In general, EU pool control	243 1 Q Okay. 2 A -- and sends data to the computational 3 core. 4 Your question was about some other unit. 5 Q The indices that are provided by the 6 command stream processor are used in that assembly 7 process to provide the vertex shader inputs, 8 correct? 9 Try it this way. What's the relationship 10 between the indices that are provided to the -- from 11 the command stream processor 406 to the EU pool 12 control and the vertex shader inputs input E? 13 A That -- that -- that is a correct 14 statement, the EU pool control unit would make use 15 of this information from the command stream 16 processor to put together the vertex information. 17 Q Okay. So if we apply a broad definition of 18 "associated with," the command stream processor 406 19 is also associated with computational core 204 20 because it provides indirect input? 21 MR. JOHNSON: Objection; form. 22 THE WITNESS: You can establish many types 23 of associations if you like, but all I have to do is 24 to show one particular mapping that renders all 25 claims or elements of the claim obvious or
242 1 unit 206 controls the respective 2 inflow and outflow to the 3 computational core 204. 4 So the function that this command stream 5 processor 406 provides is that of producing, 6 providing, triangled vertex indices to the EU pool 7 control unit 206 through some lines, and that's the 8 meaning of the association that I -- I have adopted 9 for the relationship between the second processing 10 unit and the EU pool control unit. 11 Q And the vertex shader inputs that are 12 provided to input E are based on the indices 13 provided by the command stream processor 406, 14 correct? 15 A I don't recall at this point. Can you 16 point me to the specs that describes this? 17 Q Well, you just said that it's the -- the EU 18 pool control is getting the indices for the -- the 19 primitives and the -- the triangles from the command 20 stream processor and then it's providing vertex 21 shader inputs in the form of primitives to input E. 22 A Yeah, I mean, it's -- what -- what I read 23 to you is the EU pool control unit 206 assembles 24 vertex shader inputs from the stream cache, from the 25 stream cache --	244 1 anticipated disclosed, I should say, and that's what 2 I have done. 3 You know, I've not looked at all other 4 possibilities that I could have read Jao to try to 5 see if -- if it discloses the -- the asserted claim. 6 Just one. That's the one I've done. 7 Maybe there are other ones. I -- I don't 8 oppose to them, I just -- this is the one I've done. 9 MR. RIZK: I understand. 10 Q But if we apply a broad definition of the 11 term "associated" and "associated with," you would 12 agree with me that command stream processor 406 is 13 associated with computational core 204, correct? 14 A That's not what I have done. 15 Q I understand that's not what you've done. 16 I'm asking you to answer the question, though. 17 A And you're saying a broad definition of the 18 term, and the broad means -- 19 Q Apply -- 20 A -- indirectly coupled also? 21 Q -- the plain and ordinary meaning of 22 "associated." 23 MR. JOHNSON: Objection; form. 24 THE WITNESS: To me, the association here 25 was a direct exchange between the two, not that I

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245 1 sent something to some other block and it goes to 2 some other place and gets processed and modified 3 and -- and eventually makes its way to some other 4 distance block, and then I say, oh, these two are 5 associated. 6 That's not the meaning I adopted. 7 BY MR. RIZK: 8 Q Okay. But the meaning that you adopted, to 9 be clear, isn't in the -- it's not expressed in the 10 '381 patent? 11 MR. JOHNSON: Objection; form. 12 THE WITNESS: It is in the -- it is in the 13 claim, the -- the term "associated," and I wanted to 14 say -- I mean, the way you are discussing it as if 15 "associated" is only used one time in that claim. 16 I mean, there is another place, at least 17 one other place, to load state data associated with 18 each of the plurality of tasks, so the term 19 "association" has been used even multiple times 20 within different elements of the claim, so that's 21 why my job as a POSITA is to try to make sense of 22 what this association means in the context of the 23 claim, the -- the -- the specs, the -- the -- the 24 file history, the court's claim construction, and 25 that's what I've done.	247 1 A No. 2 I've previously answered those question 3 saying I don't think that's the -- the right sense 4 of "association" in this context of this claim and 5 the specs. 6 Q Okay. You don't agree that if the -- the 7 engines are part of a processing unit, that makes 8 them associated with that processing unit? 9 A That -- correct, sir, that's -- that's what 10 I'm saying now, yes. 11 Q I'm not sure if I understand what you are 12 saying. 13 So is it -- do you agree that if the 14 engines are part of a processing unit, that makes 15 them associated with that processing unit? 16 A In the context of this claim? 17 Q Yes. 18 A Not general English language. 19 So in the context of the claim, I see 20 "association with" used two ways, and for each one 21 of them, it has a particular meaning in the context 22 in view of the specs. 23 And I do agree with you "association" -- 24 one example would be a code running on some CPU, an 25 association would be a data exchange between two
246 1 It's not just one time, even, that the term 2 has been used. 3 MR. RIZK: Yeah. So let's come up with the 4 definitions for "associated with" as that term is 5 used in the claim. 6 I think you would agree with me that -- and 7 I'm not saying that these are limiting 8 definitions -- that the scheduling module, the claim 9 scheduling module, can be considered to be 10 associated with a processing unit if it executes on 11 that processing unit. 12 Q Do you -- do you agree with me about that? 13 A Oh, yes, sir. 14 Q That's one type of association? 15 A Correct, yes. 16 Q Another type of an association which is 17 expressly disclosed in the '381 patent, you would 18 agree, is if it is a hardware component and it is 19 embodied on, it is built on, another processing 20 unit. 21 So you have the engines that are associated 22 with a -- a processing unit because they are 23 embodied on that process. 24 Would you agree that "embodied on" is 25 another form of that association?	248 1 blocks that are talking to each other, and the 2 containment relationship, I do not consider it with 3 respect to first appearance of "associated with" as 4 meeting that requirement. 5 I don't see why even that would make sense 6 in the context of this claim itself as described, 7 there -- there is another "associated with," "load 8 state data associated with," and that's even a 9 different meaning. 10 That means the plurality of tasks have a 11 certain state data that they need to run on to -- to 12 be able to run, and the association comes really 13 from the fact that the state data is necessary for 14 the task to be -- to -- to execute, and so that's a 15 different type of association in that context. 16 Q Okay. And if I direct your attention to 17 Paragraph 76 of your report, which is on Page 27, 18 that's where you talked about the file history of 19 the '381 patent; and specifically with reference to 20 Jackson '712 in view of Jao '053, and there is an 21 office action response that -- that you discuss in 22 this paragraph. 23 And in the office action response in 24 Paragraph 76, you -- you note that the applicant 25 highlighted the thread scheduler and hardware units

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249 1 in Jao were associated with the same processing unit 2 shader core, and those did not teach or suggest the 3 shader core associated with the first processing 4 unit and configured to receive the plurality of 5 tasks from at least one of the plurality of engines. 6 So you would agree that at least in that 7 context, the applicant appeared to be distinguishing 8 the prior art on the basis that the alleged 9 scheduling module -- that the -- the hardware unit 10 and the alleged scheduling module were both part of 11 the same processing unit, correct? 12 A I'm sorry. Maybe you can repeat the 13 question again because the transcript is missing 14 some of your words. 15 Q Yeah. 16 The applicant distinguished the alleged 17 prior art on the basis that the alleged scheduling 18 module and the alleged engines were -- 19 A In the prior art. 20 Q -- they were embodied on the same 21 processing units, correct? 22 A Yes, in the prior art, right? 23 MR. JOHNSON: Objection; form. 24 THE WITNESS: In Jao's reference. 25 MR. RIZK: Yes.	251 1 reference by saying the association is different; 2 but whether the meaning of the association was 3 containment or not, I can't -- I don't know. 4 BY MR. RIZK: 5 Q You didn't consider that as part of your 6 analysis of what it means for the scheduling module 7 to be associated with a processing unit? 8 A So to me, association -- to me -- 9 Q It's a simple -- sir, I'm asking you 10 whether or not you considered this specific issue in 11 the file history that we just went through where you 12 said "I have no idea" -- did you consider this 13 specific portion of the file history in your 14 assessment of what it means to a person of ordinary 15 skill in the art as to whether or not the scheduling 16 module and the engines are associated with the same 17 processing unit? 18 A No, I did consider it. I -- I did consider 19 it in the sense that I -- I understood that the 20 scheduler and the hardware units in -- in Jao were 21 associated with the same processing unit; and the 22 applicant argued that their scheduler and hardware 23 units, I guess the shader core and -- and processors 24 and so on, are associated with different processing 25 units, the first and a second processing unit.
250 1 THE WITNESS: Yes, that's what they did, 2 right. 3 They said -- they said that their new -- 4 their invention, alleged invention, is separate from 5 Jao prior art's reference because their scheduling 6 module is associated with the second processing 7 unit, which is separate from the first processing 8 unit. 9 BY MR. RIZK: 10 Q Okay. So at least the applicant, during 11 the prosecution of the patent, used the term 12 "associated with" to refer to a containment issue 13 that, because the -- the alleged engines and the 14 alleged scheduling module were contained within the 15 same processing unit, therefore, they did not meet 16 the "associated with" limitation, correct? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: I'm not sure if that was the 19 only basis or that was the main basis. I just don't 20 remember. I have to look at the Jao reference 21 again, the original reference as well as the file 22 history to see exactly in that context what they 23 were saying. 24 I do read and I do see what's there, and -- 25 and clearly they have differentiated from that Jao	252 1 That was completed considered. I agree 2 with it. The only question is this question of 3 containment as an example of association. That's 4 what you have been asking; and it is possible that 5 they made that distinction based on the containment 6 relationship also, but I -- I just don't recall at 7 this one. 8 If you give me the Jao original reference, 9 maybe it's someplace, I'll look at it and -- 10 Q But you didn't consider that -- you -- you 11 didn't consider why they were deemed to be 12 associated with the same processing unit in your 13 analysis that you applied to the definition of 14 "associated with"? 15 A It -- it -- 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: It wasn't important for -- 18 for me at this -- at that point. All I needed to 19 know was that the scheduler and the hardware units, 20 what they called hardware units, which is their 21 core, have to be associated with different 22 processing units. 23 That's the -- that's exactly what the 24 meaning of the association was. Containment or not 25 didn't draw my particular focus or attention. It

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253 1 could be that, and that's okay too, so -- it doesn't 2 change any of my opinions. 3 BY MR. RIZK: 4 Q Okay. And "associated with" -- you would 5 agree there's nothing in the plain meaning of the 6 term "associated with" which means directly 7 associated with, correct? Directly connected? 8 Nothing in the plain -- I'll withdraw that. 9 Nothing in the plain meaning of "associated 10 with" requires direct connection? 11 A Yes, but this is one of those concepts that 12 if you sort of extend it to the limit, it becomes 13 ridiculous in the sense that of course I have my own 14 first -- my family, and then my -- but then my 15 family could be your family if you go enough 16 distance and saying, well, your family has its own 17 family, and that family has its own family, and 18 finally, we're going to meet, so everybody is a 19 family, right? 20 So that's the -- the kind of thing. So we 21 have to be careful when you apply these kinds of 22 things; so when I looked at this in view of the 23 specs and the claim language, I was looking for a 24 direct connection, which I found, data exchange 25 between the two, and that was sufficient.	255 1 I'm not asking you whether or not that's 2 required by the claim or not required by the claim. 3 I'm just asking you, applying the plain, broad 4 meaning of "associated with," is the command stream 5 processor 406 in its operation as described by Jao 6 associated with computational core 204. That's. 7 A yes-or-no answer. 8 A So yes in the same sense that the CPU of 9 the '381 is associated with the GPU of '381, because 10 they also have connections. 11 MR. RIZK: Okay. Would now be a good time 12 for a break? 13 THE VIDEOGRAPHER: Stand by. 14 We're going off the record at 1613. 15 (A recess was taken from 4:13 p.m. 16 to 4:27 p.m.) 17 THE VIDEOGRAPHER: We are back on the 18 record, and the time on the monitor is 1628. 19 MR. RIZK: Let's go to Paragraphs 277 20 through 299 of your report. 21 Q That's the section of your report where you 22 provide the -- your invalidity opinion for the '381 23 patent based upon the Studdard reference and the 24 basis therefor, correct? 25 A Correct, yes, sir.
254 1 Whether -- whether there are other ways of 2 creating this association, yes, there are. 3 Q Okay. And if we just apply the plain 4 meaning of "associated with" and -- and we don't 5 limit it any way, we just apply the plain meaning, 6 as broad as that plain meaning is, you would agree 7 that the command stream processor 406 is associated 8 with the computational core 204, correct? 9 A But the association is required between the 10 scheduling module and the second processing unit. 11 It's not required between the second processing unit 12 and the first processing unit, which is your 13 question. 14 You're asking -- you are asking me is what 15 I've identified as the second processing unit -- 16 Q No, that's not my question, is whether it's 17 required. 18 A But that's what you asked, sir. 19 Q I didn't -- I didn't ask you if it's 20 required. 21 I asked you if you apply the -- the 22 broadest plain meaning of associated with -- 23 okay? -- is the command stream processor 406 24 associated with the 406, not associated with the 25 computational core 204.	256 1 Q In Paragraph 283 of your report, you 2 identify the components that you consider to be the 3 alleged engines in -- in Studdard, correct? 4 And those components that you identify as 5 the alleged engines for Studdard are the binning 6 unit 1069, the channel controller 108, the array 7 controller 104, and components of the thread 8 manager, 102, including the cache memory unit 1024, 9 the thread processors 1026, and the status block 10 1030, correct? 11 A Yes, sir. 12 Q Okay. Let's start with the thread manager. 13 It's your opinion that the thread manager 14 receives tasks from the alleged scheduling module, 15 correct? 16 A So what I've said in my report is that the 17 thread manager 102 receives control signals from an 18 embedded processor unit EPU-8 to fetch instructions 19 and subsequently provide them to the array 20 controller 104 and the channel controller 108. 21 Q Okay. Is it or is it not your opinion that 22 the thread manager receives a plurality of tasks 23 from a scheduling module? 24 A So what I've said here is that the 25 combination of all these units that I've identified

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257 1 as the plurality of engines, they work together to 2 receive from a scheduling module a plurality of 3 tasks. That's what I've said. 4 Q Okay. This seems like a very simple 5 question. 6 Does the thread manager receive a plurality 7 of tasks from a scheduling module? And if so, what 8 are those alleged plurality of tasks? 9 Because I don't see it in your report. In 10 fact, I don't see it for any of the specific modules 11 where you've identify tasks received by anything. 12 So you tell me. 13 We'll start -- starting with the thread 14 manager, does the thread manager receive a plurality 15 of tasks? If so, what are they? 16 A So the disclosure that is in the reference, 17 the Studdard reference, is what I just read to you 18 before, so the thread manager receives control 19 signals from an embedded processor EPU-8 to fetch 20 instructions and subsequently provide them to the 21 array controller. 22 So these instructions are instructions of 23 the threads; so the thread manager, having received 24 the control signals from the embedded processor, is 25 fetching the instructions and subsequently providing	259 1 A I don't recall any disclosures; so as far 2 as my memory allows me, I would have to agree with 3 you that it has been silent on whether you receive a 4 single task completely or you receive multiple 5 tasks. I don't recall. 6 Q Studdard is silent as to whether the 7 processing blocks 106 have to complete execution of 8 a single task before moving on to a second task? 9 A Again, as far as I remember, there is no 10 disclosure in Studdard that a task has to be 11 completed before a new task comes in or -- or -- or 12 before a new task is being executed, you start 13 executing a new task. 14 Q There's no disclosure in Studdard also that 15 multiple tasks execute at the same time in the 16 processing blocks 106? 17 A So I have some references here in -- on 18 Paragraph 287 that we need to check together, if you 19 like, in which I do show that the processing blocks 20 106 receive the plurality of tasks from the thread 21 manager 102 via the array controller 104; and there 22 are also citations about the processing blocks being 23 available to process respective group of data items, 24 which are these, I guess, instructions coming in. 25 So I do have support for it, but we have to
258 1 them to other units. 2 So to me, that means that the thread 3 manager is actually receiving, fetching, these 4 threads, these instructions. 5 Q Okay. And your -- your opinion is that 6 those threads or instructions are, in fact, tasks, 7 correct? 8 A No, that's not my opinion. 9 Q Well, does the thread manager -- this is 10 what's in the claim, sir. This -- this should be an 11 easy question for you to answer. 12 A So -- 13 Q Does the thread manager receive a plurality 14 of tasks? 15 A And the answer is yes. Yes. 16 Q What are those tasks that the thread 17 manager receives? 18 A The tasks comprise of threads, the threads 19 comprise of instructions, the -- the thread manager 20 is receiving these instructions, therefore, it is 21 receiving tasks, three -- 22 Q Studdard is silent as to whether or not the 23 tasks -- the alleged tasks received by the thread 24 manager come in one at a time or multiple tasks at 25 the same time, correct?	260 1 walk through it if you like. 2 Q No, you don't, because Paragraph 288 is 3 where you discuss that, allegedly, the -- the 4 alleged shader core in Studdard, which I believe you 5 allege to be the plurality of processing blocks 6 106 -- that -- let me withdraw that question. 7 You don't have support because where you 8 allege that the shader core, which you allege to be 9 the processing blocks 106 together, execute multiple 10 tasks at the same time, you don't provide any 11 identification of support in Studdard. 12 Do you see that, Paragraph 288 where you -- 13 you cite to no support? 14 A No, it -- yes, I do see it -- 15 Q Okay. 16 A -- and that particular paragraph doesn't 17 have any citations in it; but it's a "therefore," 18 right? So the support for that Paragraph 288 is 19 really provided in Paragraph 287. That's why I 20 start by saying "Studdard, therefore, discloses," 21 because I've previously proven it. 22 Q Okay. Well, let's -- let's -- what is 23 the -- what is the citation here that we should be 24 looking at that provides support for multiple tasks 25 executing at the same time within the processing

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1 blocks 106 of Studdard? 2 A So first of all, I even have a direct quote 3 to abstract that says the processing elements are 4 operably divided into a plurality of processing 5 blocks, the processing blocks being operable to 6 process respective groups of data items. 7 That means respective groups of tasks with 8 their data items, and then I have reference to 9 9-11-20. We can look at it. 10 Q So you interpret -- just before we move on, 11 are you interpreting the data items, respective 12 groups of data items, to be the tasks now? 13 Is that what you're -- where you're going 14 with that? 15 A No. I'm saying -- 16 No, sir. What I said to you was that if 17 you read the abstract, in the abstract, it says that 18 this data processing apparatus comprises SIMD array 19 of processing elements; these processing elements 20 are divided into blocks, and these blocks are 21 operable to process respective groups of data items, 22 which means in a SIMD sort of setup, you are 23 executing multiple instructions at the same time, 24 operating on multiple data items, so that's -- 25 that's one -- one thing that's said in the abstract,	261 1 I do agree you need more support for it. 2 Q So let's -- let's look, then, at 9-11 3 through 20, because I didn't see that support when I 4 looked at your -- your report and the citations that 5 you identify. 6 So 9-11 through 20 -- 7 A I'm sorry. What tab is -- is this? 8 Studdard -- 9 Q It's Tab Number 9. Tab Number 9 of 10 Exhibit 2. 11 So 9-11 through 20 doesn't mention tasks at 12 all? 13 A Yes, it doesn't mention tasks. 14 Q Okay. 15 A But it talks about instructions. 16 Q Okay. But that doesn't mean that multiple 17 tasks are executed in the processing blocks at the 18 same time, correct? 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: It could also mean that, 21 but -- 22 BY MR. RIZK: 23 Q It's silent. 24 A Yeah. 25 Q It doesn't -- you can't tell.
262 1 but there is further proof, 9-11-20, and -- 2 Q Well, we'll walk through them -- 3 A Okay. 4 Q -- but you'd agree with me that executing 5 multiple threads at the same time is not the same as 6 executing multiple tasks at the same time. 7 You may be executing multiple tasks at the 8 same time but you're not necessary executing 9 multiple tasks at the same time, correct? 10 A I do agree with that, yes. 11 Q Okay. So it depends on whether or not the 12 system is designed to handle and allow for multiple 13 tasks to be executed at the same time? 14 A You are correct there. 15 Q Okay. 16 A Yes, sir. 17 Q So to determine whether or not multiple 18 tasks are -- are executed at the same time, it 19 wouldn't be enough for us to just point to a 20 plurality of threads being executed at the same time 21 and conclude from that that multiple -- that the 22 capability is there to execute multiple tasks at the 23 same time, correct? 24 A Perhaps. 25 I mean, you need more support for it. I --	264 1 A By itself, correct. I mean -- 2 Q Let's go to the next citation. You have 3 17-28 through 18-8. And I'm reading from the 4 citations that you identified in your Paragraph 287. 5 So 17-28 through 18-8 just talks about how 6 there are multiple processing blocks that include 7 arrays of processing elements, and they process 8 data. 9 They -- they don't -- it doesn't talk about 10 executing multiple tasks at the same time across the 11 multiple processing blocks, correct? 12 A So this -- this excerpt is talking about 13 just one of the processing blocks 106 that's 14 operating in the SIMD fashion, as we discussed 15 previously also as part of this deposition; and so 16 if -- if you apply SIMD in that particular 17 processing block, then it's not showing that, 18 necessarily, multiple tasks are being run. 19 Maybe you are doing -- because as you may 20 recall, in '381, the parallel processing system can 21 do spatial as well as temporal partitioning to 22 achieve parallel execution; and so in view of that 23 disclosure there in '391, one could also read this 24 that although this is SIMD, maybe you are doing 25 temporal partitioning and therefore, multiple tasks

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265 1 are running on that same block. 2 Q But that's disclosed in the '381 patent, 3 not in Studdard, sir. 4 A Yeah, but -- 5 Q Okay. 6 A Correct, yes. That's correct. 7 Also -- 8 Q We need to -- I'm looking at -- sir, I'm 9 not looking at the '381 patent and I'm not looking 10 for you to fill in the gaps of Studdard with the 11 '381 patent. Okay? 12 A I'm not -- yeah. 13 Q That -- that is not what I'm asking you to 14 do. 15 In fact, in a SIMD processor, sir, the -- 16 the multiple threads that are running on a single 17 SIMD would never pertain to more than one task, 18 correct? In fact, they're running the same 19 instruction. 20 A On any one of those processing blocks, 21 under SIMD assumption, you're correct. 22 Q Well, that's what this disclosure that you 23 pointed me to is concerned with, a single processing 24 block. It says "one of the processing blocks." You 25 pointed that out to me, and I agree.	267 1 also are the same threads that run in the -- on the 2 core computational blocks, so according to that 3 disclosure, those eight threads running would -- 4 would -- would correspond to different tasks. 5 Q But they would never run at the same time, 6 even if they did. So let's -- let's take it in 7 turn. 8 So Number 1, if this is actually a SIMD, 9 you would agree that this is going to be one task? 10 A Per block. 11 Q Let's turn to -- let's pretend that -- that 12 the patent doesn't say that this is a SIMD. Let's 13 pretend that Studdard doesn't say that about the 14 processing block and turn to Page 23, which provides 15 the detailed description of the thread manager. 16 A Yes, sir. 17 Q And it says here -- I'll read it into the 18 record, Line 18 through Line 21. "At any given 19 time, only one thread is executing." 20 So out of those eight threads that you 21 identified on Page 11, at any given time, only one 22 thread is executing. 23 Do you see that? 24 A Yes, I see that. 25 Q Okay. So --
266 1 This is -- this disclosure that you cited 2 to in your report relates to one of the processing 3 blocks, not to multiple processing blocks, correct? 4 A Yes; but in Studdard, as we read before, 5 and I'll point out in -- on Page 11, Lines 16 to 6 25 -- which I have not referenced here, but that one 7 clearly has a discussion in which the eight parallel 8 threads, they are doing different tasks. 9 Thread 0 is doing a general system control, 10 thread 1 is doing a 2D, threads 2 to 7 are doing 3D 11 activities; so I -- I should have probably included 12 that reference also here, which I omitted, correct, 13 but it's there. 14 It's in the reference in the -- in the -- 15 in the prior arts reference. 16 Q Okay. Well, let's go with this. 17 So when you go with -- with this discussion 18 of the thread manager, this isn't actually talking 19 about what is being executed on the cores, this 20 actually talking about what could be assigned to any 21 one of a number of tasks, correct? 22 A That is correct; but then if you look at 23 the rest of the embodiment in Figure 3 or 8, 24 whichever it was, as you pointed out also earlier 25 today, the -- the eight threads that get assigned	268 1 A But -- But then can you read the rest of 2 it, please, for the record? 3 Q "And the scheduling of the time 4 multiplexing between threads is determined by the 5 dynamic conditions of the program execution." 6 So you would agree with me, sir, that, 7 turning to Page 11, at any particular moment in 8 time, those eight threads that you identified, only 9 one of them could be executing on the core, on the 10 processing block, correct? 11 A From this description? 12 At any one point in time, one thread is 13 executing per block, I give you that; but then there 14 is the time -- 15 Q I -- that's -- that's all I asked you. 16 A But -- 17 Q Your counsel can -- can -- if you have more 18 to add to that -- 19 A Sure. 20 Q -- your counsel can redirect you later; but 21 for now, that's all I'm asking you, Doctor. 22 A Very good. 23 Q So, in fact -- in fact, sir, there -- there 24 really is no disclosure -- express disclosure in 25 Studdard of multiple tasks executing at the same

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1 time on the processing blocks 106, correct? 2 A Clarification question for me. "At the 3 same time" means what? 4 Q Concurrently. 5 A At the same exact instance in time? 6 Q Yes. 7 A There is time multiplexing; but otherwise, 8 you're right. 9 Q Okay. And time multiplexing, to be clear, 10 if there are multiple tasks, they wouldn't be 11 executing at exactly the same time, correct? 12 A This would correspond to temporal 13 partitioning where you're doing parallel processing 14 in the '381 patent that's been disclosed in this -- 15 Q And there is no express disclosure in -- 16 and I'm talking about explicit disclosure -- in 17 Studdard that multiple tasks are actually 18 time-partitioned? 19 It doesn't explicitly say that multiple 20 tasks will be time-partitioned, correct? 21 A Studdard talks about threads, correct, not 22 tasks -- 23 Q Okay. 24 A -- in this context. 25 Q Okay.	269 1 blocks 106 as your shader core, so the question 2 is -- I'll refer you to Figure 3. 3 The thread manager exists outside of the 4 alleged shader core, correct? 5 A Yes, it does. 6 Q Okay. And state data can exist within the 7 thread manager, correct? 8 A Can exist? 9 Q Yeah. 10 Let me try it this way. The fact that -- 11 agree or disagree, since the thread manager is 12 outside of your alleged shader core, state data 13 cannot exist inside of the thread manager, it's not 14 state data until it's inside of the shader core? 15 A Can you repeat your question? Because one 16 says inside the thread manager, and then you say 17 inside the shader core, so which one? 18 Q Yeah. 19 So my question is, for state data to exist, 20 does it need to be stored inside of the alleged 21 shader core? 22 A Not necessarily. 23 Q Okay. So a person of ordinary skill in the 24 art, which is the lens that you applied -- a person 25 of ordinary skill in the art would not understand --
270 1 A But threads correspond to a -- a -- a group 2 of threads become one task. 3 Q Does the thread manager load state data? 4 A So what I have said in -- on Paragraph 284 5 of my report is that Studdard teaches that the 6 status block 1030 within the thread manager 102 7 receives status information 1036 from each of the 8 threads, and then keeps going, explaining -- 9 Q I see what your report says, but that -- 10 my -- my question to you isn't what does your report 11 say, sir. 12 My question to you is, does the thread 13 manager that you identified in Studdard receive 14 state data? 15 A Yes. 16 Q Okay. Let's go to Figure 3. 17 Does -- does the -- let me ask you a 18 follow-up question. 19 Does the thread manager load state data? 20 A Yes, it does. 21 Q Okay. You'd agree with me that the thread 22 manager exists outside of your alleged shader core 23 in Studdard, correct? 24 For the record, I think it alleges that 25 the -- you're alleging the plurality of processing	271 1 withdraw it. 2 A person of ordinary skill in the art would 3 understand that state data can exist outside of the 4 shader core, correct? 5 A Can exist? 6 Q Can exist. 7 A Sure, yes. 8 Q Okay. 9 A Can. 10 Q And a person of ordinary skill in the art 11 would understand that state data can exist prior to 12 execution of the tasks associated with that state 13 data, correct? 14 A Yes. 15 Q Let's go to Figure 3 of Studdard. 16 The thread manager provides the alleged 17 tasks to the array controller and the channel 18 controller, correct? 19 A Yes, sir. 20 Q Okay. So how could the array controller 21 and the channel controller be engines? 22 A So this is the same discussion about the 23 engines we had earlier today at the beginning of 24 the -- 25 Q It is, because it strikes me that the
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273 1 thread manager has both received a plurality of 2 tasks and it's loaded a plurality of tasks, so to 3 your point, nothing is left to be done. 4 Sorry. Let me -- let me withdraw that. 5 The thread manager has both received a 6 plurality of tasks and -- and it has loaded the 7 state data associated with those plurality of tasks, 8 so nothing left to be done, array controller, 9 channel controller cannot be engines. 10 A I mean, if you -- I'll read to you the 11 discussion about the array controller, and so on. 12 Q I'm not asking you to -- I'm not asking you 13 to read anything to me. I'm asking you to answer my 14 question. 15 Given that the thread manager is upstream 16 with respect to the array controller and the channel 17 controller, and it will have already received a 18 plurality of tasks and loaded the state data 19 associated with that plurality of tasks, per your 20 earlier testimony, you wouldn't consider array 21 controller, channel controller, to be engines, 22 otherwise, everything is an engine? 23 A So the PE instruction sequence of 1044 24 and/or the load-stored controller 1045 within the 25 array controller 104 load the state data associated	275 1 thread manager loads state data; is that true? 2 A Yes. I mean -- 3 Q Agree or disagree, thread manager loads 4 state data? 5 A It receives the status information from 6 1036 unit for each of the threads; but loading the 7 state data so that they could be then provided to 8 the shader core, and so on, is really done by this 9 array controller. 10 Q Okay. Well, then why isn't the thread 11 manager just redundant of the functionalities in the 12 array controller and the channel controller? We 13 don't -- we don't need it. 14 A No, it receives the tasks. 15 Q Okay. So to receive, it has to directly 16 receive? Because the array controller and the 17 channel controller receive the tasks too. 18 A They receive it from the thread manager. 19 Q Okay. So -- so what? So that's not from 20 the scheduling module? 21 A So, again, when I receive a task at the 22 higher -- closer to the front of the graphics 23 system, I need to pass it downstream to the next 24 block and the next block and the next block; and so 25 when you say the intermediate blocks therefore
274 1 with each task, the data associated with each task 2 that is present in the PE register file 1061-B and 3 the -- the PE memory unit 1061-C, so that's a 4 function that they perform to actually load the 5 state data associated with each task. 6 Q Well, that's redundant to the function 7 that's performed by the thread manager. That -- 8 that receives the plurality of tasks and loads state 9 data. 10 If you apply the definition that you're now 11 applying to your testimony earlier, everything is an 12 engine. 13 A No, I -- I -- maybe I misspoke before 14 because I'm going by memory and there's a lot of 15 information here. 16 So you asked me a question about does the 17 thread manager also do the loading of the state 18 data; and I said fine, because, yeah, it looked like 19 that to me; but now that I read my own excerpt more 20 carefully, I -- I must make the correction that the 21 array controller is actually the one that's doing 22 the loading of the state data associated with each 23 task. 24 I misspoke before. I apologize. 25 Q So you withdraw your testimony that the	276 1 receive also tasks, the fact remains that the thread 2 manager is the -- the person -- the -- the unit that 3 received the task under -- because of the 4 instructions, the control information it received 5 from -- I think it was EP-8 unit, so that's the one 6 that receives the instructions. 7 You cannot -- so the -- the problem with 8 what you are proposing is that you -- you're either 9 cutting the legs or cutting the head of the person 10 and saying now walk or think. 11 Q This is your -- I'm applying your 12 definition, sir. 13 A But that's -- 14 Q Let's -- let me ask you a different 15 question. 16 A Yes, please. 17 Q Okay. You opine that the array controller 18 and the channel controller loads state data, 19 correct? Paragraphs 284 to 285 of your report. 20 A Alternatively, one or the other 21 alternatively, yes. 22 Q Well, I'm not asking you about your 23 alternative, sir. I'm asking you -- 24 A But that's -- 25 Q Hang on.

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277 1 I'm asking you factually, based on your 2 review of the reference, both of those devices load 3 state data? 4 A Again, if -- I have to go by my report, 5 right? So my report, Paragraph 284, I -- I describe 6 how the loading of the state data is done by the 7 array controller 104, and then I start Paragraph 285 8 saying "Alternatively." 9 Q I understand -- I'm not asking you to read 10 from your report. 11 I'm asking you -- it's very simple, 12 yes-or-no answer, does, in your opinion as a person 13 of ordinary skill in the art, the array controller 14 load state data, yes or no? 15 A Yes. 16 Q Does the channel controller, in your 17 opinion as a person of ordinary skill in the art, 18 load state data, yes or no? 19 A Yes. 20 Q If we go back -- 21 A Perhaps not the same state data, but yes. 22 Q If we go back to Figure 3, the array 23 controller 104 and the channel controller provide 24 instructions to the processing blocks, correct? 25 A Yes.	279 1 facilitation for the array controller in this case. 2 Q So any -- how do we identify -- how do we 3 distinguish between a downstream component that 4 receives tasks and loads state data from -- from an 5 engine? 6 Because it seems like if we apply the 7 definition that you're providing, to me, a 8 preprocessing block can be an engine. No -- no 9 reason why it can't be an engine. 10 The preprocessing block in the '381 patent, 11 no different than what you're identifying the 12 binning unit here. 13 A I don't see that correspondence. I mean, 14 I -- I -- I know you see it. I don't see it. 15 Q What is the difference -- what makes the 16 binning unit an engine but the -- the preprocessing 17 blocks as described in the '381 patent not an 18 engine? 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: In '381, the engines are 21 clearly described, annotated, named. They perform 22 the functions that's been claimed. That work is 23 done. There is no facilitation or additional 24 enablement or anything is needed -- 25 ///
278 1 Q Okay. And the binning unit is part of the 2 processing blocks, correct? 3 THE STENOGRAPHER: I'm sorry. The what 4 unit? 5 BY MR. RIZK: 6 Q The binning unit 1069 is part of the 7 processing blocks? 8 A Correct, yes. 9 Q And you identify the binning unit as 10 another engine, correct? 11 A Yes. 12 Q Okay. And how is the binning unit an 13 engine if the tasks have been received by the array 14 controller and the channel controller, and the state 15 data is loaded by those elements? 16 A Again, it goes back to our discussion 17 earlier today that I identified a plurality of 18 engines that collectively performed the required 19 functions of the claim element; and some of these 20 engines only facilitate, help enable other 21 components to function as they should to meet the 22 required claim elements. 23 So the binning unit is one of those 24 facilitators block -- facilitator blocks that's 25 there to provide additional support, enablement,	280 1 BY MR. RIZK: 2 Q Sir, I'm -- I'm asking you what is -- in 3 your definition of the term "engine," what is the 4 meaning that you are ascribing to that term that 5 make the binning engine -- the binning unit an 6 engine but precludes the preprocessing blocks of the 7 '381 patent from being an engine if you apply your 8 definition? 9 MR. JOHNSON: Objection; form. 10 THE WITNESS: In this case, in Studdard's 11 case, the four blocks I've identified work together 12 to perform the claimed functions. In the '381, 13 their 202-A through E engines already do those 14 functions. 15 We didn't enter the graphics processing 16 pipeline, and the graphics processing pipeline has a 17 preprocessor, followed by the actual final 18 processing, and so that's part of the overall 19 graphics pipeline there. 20 It's not part of the engines that receive 21 tasks or to load state data and pass it on 22 downstream for the preprocessing stage and then the 23 final stage of computation of the graphics tasks, 24 whereas here, binning unit is really providing 25 additional support in terms of points of look-ups

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281 1 and so on for the array controller that provides 2 some additional state information in the alternative 3 to the processing blocks 106. 4 The functions are quite different, what is 5 being received, what is being processed, what's 6 being provided is quite different, so that's how I 7 draw the distinction. 8 MR. RIZK: The binning unit actually sorts 9 verticis, sir. That's what it does. That's part of 10 the graphics pipeline. 11 Q In fact, it's part of the shader core, 12 isn't it? 13 A Yeah, it is -- 14 MR. JOHNSON: Objection; form. 15 THE WITNESS: So -- so the -- the -- the -- 16 the binning unit is -- is providing information to 17 the array controller as described in 18 Paragraph 285 -- I'm sorry. I -- I keep saying 19 "array controller." I stand corrected -- to the 20 channel controller 108, to the channel controller 21 108, in order for it to provide certain information 22 that I consider to be state data information as is 23 named also in that excerpt to the processing unit. 24 MR. RIZK: Okay. 25 THE WITNESS: I understand it's inside of	283 1 engine does, it can be considered an engine with the 2 lens that you're applying, correct? 3 A No, it does not. That's not what I meant, 4 that's not what I said. 5 Q Okay. So what differentiates the binning 6 unit from the preprocessing block that makes the 7 binning unit an engine but the preprocessing block 8 not? 9 MR. JOHNSON: Objection; form. 10 THE WITNESS: The preprocessing units in 11 '381, they receive threads with associated state 12 data. They are acting on those threads to transform 13 them, to so-called preprocess them so that they can 14 be passed to the main processing elements of the 15 graphics pipeline to do the various shading tasks. 16 The binning unit here in 1069 is only 17 assisting the channel controller 108 to provide 18 certain state data to -- so that they can be added 19 to the tasks so that the tasks have complete 20 information to run on the processing elements in 21 their graphics pipeline of the Studdard, in the 22 graphics pipeline of the Studdard. 23 So that's -- they are doing different 24 functions altogether. 25 ///
282 1 the block 106; but it supports what the channel 2 controller does, which is outside the processing 3 block. 4 BY MR. RIZK: 5 Q So if it supports what an alleged engine 6 does, then it can be considered an engine? Is that 7 the standard we're going to apply? 8 A Again, I'm -- 9 MR. JOHNSON: Objection; form. 10 THE WITNESS: I've -- we have gone through 11 this many times, and I'm not sure if I can add 12 anything, so -- to -- to that discussion. 13 My -- my point still is we discussed what 14 the requirements are on a single engine, what -- we 15 just talked about the plurality of engines and their 16 functions, and you want to keep going back to the 17 same topic. 18 MR. RIZK: I want a yes-or-no -- 19 THE WITNESS: I'm not sure I can add 20 anything to this. 21 MR. RIZK: I want a yes-or-no answer to my 22 question. That's what I want. So I'll repeat my 23 question, and I would appreciate an answer without 24 the argument -- the argument. 25 Q If a component supports what an alleged	284 1 BY MR. RIZK: 2 Q Well, the -- the preprocessing blocks also 3 receives tasks and transforms them to -- to 4 preprocess them; and the binning unit also receives 5 tasks and transforms them. It takes verticis and 6 sorts them, does it not? 7 A Absolutely not. It does not receive tasks. 8 Q Okay. 9 A It does not receive -- binning unit here 10 does not receive tasks, no. 11 Q Does it -- what -- what does it receive? 12 A Let me read it again. 13 Q We're -- we're not going to have time for 14 you to read the reference, sir; so do you -- do you 15 know -- when you rendered your opinion, did you know 16 what the binning unit received? 17 A Of course I -- I did then, I -- I do now. 18 It's in my report. 19 But you -- you don't want me to read 20 through it, you want me to try to say it from 21 memory, and that's not -- 22 Q Well, you're reading from your report, and 23 your report doesn't get into what the primary 24 function of the binning unit is, which is to receive 25 and sort verticis, which is a graphics processing

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285 1 task and transformation. 2 A I -- I don't see any connections here in 3 Figure 3 that shows information coming above the 4 verticis into the binning unit. Binning unit 5 basically is about pointers and -- and sorting of 6 the pointers that -- that associate -- that are 7 associated with -- with some -- some -- some of the 8 data, but -- so there is a binning context, there is 9 bin lists, a region to be rasterized, operation 10 mold, and so on; and it's taking all that 11 information and providing some additional state 12 information to the channel controller. 13 Q So bottom line, your testimony is that an 14 engine can be within the alleged shader core, 15 correct? 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: In the context of Studdard, 18 that's one of the blocks I've identified is inside 19 of processing block 106, that is correct. 20 MR. RIZK: Okay. 21 THE WITNESS: But I'm not -- 22 BY MR. RIZK: 23 Q So a person of ordinary skill reading the 24 '381 patent would understand that the engine can be 25 inside of the shader core, correct?	287 1 believe that a POSITA would understand that the 2 claimed engines can be included within the claimed 3 shader core. 4 THE WITNESS: That's not my testimony. 5 BY MR. RIZK: 6 Q So that's not? 7 So -- so then you don't -- it is not your 8 testimony, then, that the binning unit is an engine 9 of the plurality of engines? 10 A In the context of Studdard, I've identified 11 it there; but I'm not saying by any means that 12 somebody looking at '381 would draw a conclusion one 13 way or the other about the overlap between the 14 engines and the shader core. 15 Q Are you -- 16 A Probably they wouldn't. 17 Q Are you withdrawing your opinion that the 18 binning unit of Studdard qualifies as an engine of 19 the plurality of engines per the '381 patent? 20 MR. JOHNSON: Objection; form. 21 THE WITNESS: First of all, I've said this 22 is an alternative, so the channel controller and the 23 binning unit is the alternative. I have the thread 24 manager and the array controller, and my opinion has 25 been that I -- I -- we -- I -- I could include the
286 1 MR. JOHNSON: Objection; form. 2 THE WITNESS: That's not what I'm saying, 3 actually, because if a person not -- if -- if -- if 4 you only look at the '381, you don't see that 5 relationship. 6 MR. RIZK: Well, that's what you've 7 identified -- 8 THE WITNESS: When I tried to do the 9 mapping in this case, I did the mapping by 10 identifying this binning unit which has a very 11 specific function that it performs that provides the 12 state data to the channel controller; and for me to 13 say the channel controller does its job, I included 14 binning units also there, but I'm not implying 15 somebody who's not seen Studdard and just looking at 16 the '381 would draw the conclusion that you said. 17 MR. RIZK: Well, but that's -- you have 18 stated an opinion. You've offered an opinion in 19 this investigation, and your opinion was that the -- 20 the processing block is the alleged -- the 21 processing blocks were the alleged shader core and 22 the -- the binning unit is one of the alleged 23 plurality of engines. 24 That was your opinion, sir; so I'm going 25 to -- I interpret that opinion to mean that you	288 1 binning unit that supports, because of the specific 2 function it does, the function of the channel 3 controller, I wanted to be complete, and therefore, 4 I included there, as part of the engines that 5 receive tasks and -- and -- and load state data and 6 then pass them on to the shader core for processing. 7 MR. RIZK: Sir, it's either an engine 8 within the meaning of the '381 patent claim or not. 9 You've -- you've -- in your report, you identify the 10 binning unit which is part of your alleged shader 11 core as an engine, so you have to pick. 12 Q Is -- is it the case that a person of 13 ordinary skill in the art looking at the '381 14 patent -- is it the case that they would understand 15 that the claimed shader core can exist -- sorry -- 16 the claimed -- one of the claimed engines can exist 17 within the claimed shader core? 18 MR. JOHNSON: Objection; form. 19 THE WITNESS: Reading the '381 patent, the 20 claims and specs, a person of skill in the art would 21 not consider one of the engines to be part of the 22 shader core. I -- I tend to agree with that. 23 MR. RIZK: Okay. So I'll take that answer. 24 Q A person of ordinary skill in the art would 25 understand that the binning unit of Studdard does

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289 1 not constitute an engine? 2 A Yeah, probably, yes. 3 Q Let's turn to the Wilt (phonetic) 4 reference. 5 Your opinion on Wilt starts on 6 Paragraph 254 of your report and extends to 276. 7 That's where you state your opinion on invalidity 8 based on Wilt, correct? 9 A Yes. 10 Q Okay. And Paragraph 261, you identify the 11 work distribution 210, the front end 212, and the 12 core interface 303 as your alleged engines, correct? 13 A Yes. 14 Q And it's your opinion that these units 15 received tasks from software programs on the CPU, 16 correct? 17 A Yes. 18 Q And you don't opine that the front end unit 19 loads the state data, correct? 20 A I mean, it's been a while, so I don't 21 remember the details of exactly what the 22 functionality of each of these components was. I 23 think we should go to the -- 24 Q It's not in your report, sir. 25 A It is not?	291 1 that -- that might help you out. 2 THE WITNESS: Thank you. 3 BY MR. RIZK: 4 Q Does that help? 5 A Yes. 6 What I say here -- 7 Q Okay. 8 A -- is the core interface loads the state 9 parameters associated with each command thread into 10 the core. 11 Q Okay. 12 A Yes. 13 Q And that's the basis of your opinion 14 that -- that you provide in your report that the 15 plurality of engines loads state data, correct? 16 A Yes. 17 Q You don't opine that the front end loads 18 state data, right? 19 A Yes, that's correct. 20 Q And, in fact, the front end unit receives 21 commands from a host interface 206, correct? 22 A Let's even switch to Wilt. I'm still on 23 Studdard. So what tab? 24 Q Tab 17 of Exhibit 2. 25 A Okay.
290 1 Q You don't opine in your report that the 2 front end unit loads state data, correct? 3 A So what I have said in my report is that 4 the combination of all these three does the required 5 functions, which is to receive the tasks and to load 6 the state data. 7 Which one does what, I'd have to go and 8 check the citations and all that, and -- and so I'll 9 be glad to walk with you or -- or -- or if you have 10 looked at it and you find a problem, let me know; 11 but I believe I've provided support that this 12 combination that I've identified does both 13 functions. 14 Q You haven't identified what component 15 specifically in your report loads state data, have 16 you? 17 MR. JOHNSON: Objection; form. 18 THE WITNESS: I have given a number of 19 references here -- 20 MR. RIZK: I'll -- I'll make it easy for 21 you, sir. 22 Paragraph 263 is where I believe, in your 23 report, you identify the components that you believe 24 load the state data; so why don't you -- just to 25 orient you, if you look at the last sentence,	292 1 MR. JOHNSON: We've been going about an 2 hour, so -- 3 MR. RIZK: Can we go for another like five? 4 MR. JOHNSON: Yeah. 5 THE WITNESS: I'm sorry. I'd like to take 6 a break. It's just switching too quickly between 7 references and it's sort of turning into a memory 8 game in terms of what I remember about the different 9 components of these -- 10 BY MR. RIZK: 11 Q Let me -- can I finish this one question, 12 sir? It shouldn't take longer than five minutes. 13 A No. Seriously, if I can request 14 respectfully -- 15 Q You need a break? 16 A -- let's take a break. 17 MR. RIZK: Okay. All right. Let's take a 18 break. 19 THE WITNESS: Thank you. 20 THE VIDEOGRAPHER: Please stand by. 21 We're going off the record. The time is 22 1728 on the monitor. 23 (A recess was taken from 5:28 p.m. 24 to 5:41 p.m.) 25 THE VIDEOGRAPHER: We are back on the

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293 1 record and the time on the screen is 1741 p.m. 2 MR. RIZK: All right. I think I had as my 3 pending question to you, sir, that the front end 4 unit of Wilt receives commands from a host interface 5 206; and to help orient you, I directed your 6 attention to Column 3, Line 56 of -- of Wilt, Tab 17 7 in your Exhibit 2. 8 While we're pulling it up, I'll read it 9 into the record. 10 (Reading): 11 Host interface 206 generates 12 packets for other signals for 13 transmission on communication path 14 113, and also receives all incoming 15 packets or other signals from 16 communication path 113 and directs 17 them to appropriate components of 18 PPU-202. 19 I'll give you a different cite. 20 Starting on Line 60 (reading): 21 For example commands related to 22 processing tasks may be directed to 23 a front end unit 212, while 24 commands related to memory 25 operations, e.g. reading or writing	295 1 correct? 2 A No. 3 Q Okay. So why is the host interface not an 4 engine, then? If all it's doing is serving as a 5 passthrough of the alleged tasks, what makes it an 6 engine? 7 Sorry. Let me try -- let me 8 rephrase -- rephrase that. 9 Why is the front end an engine? 10 A Again, what I've tried to do -- you don't 11 want a yes-or-no answer, you want -- 12 Q I asked you the -- the -- the "why," yes. 13 A So -- so there are two functions to be 14 performed to meet this requirement for the plurality 15 of engines. One is to receive tasks and one is to 16 load the state data associated with them. 17 And so when I do this, I don't want to -- 18 so the -- I -- I -- I identify the set of blocks 19 that I need to have so that the combination allows 20 data to pass through from input to output, and then 21 at the same time performs those functions, so as a 22 result, there could be something that is there in 23 the middle that helps with that connectivity from 24 input to output where the different blocks are doing 25 the -- one or the other of the required functions so
294 1 to PP memory 204, may be directed 2 to a memory interface 214. 3 Host interface 206, front end 4 unit 212, and memory interface 214 5 may be of generally conventional 6 design, and a detailed description 7 is fomented as not being critical 8 to the present invention. 9 So I'll repeat my question. 10 Q The front end unit receives commands from 11 an interface 206, correct? 12 A Yes. 13 Q And the work distribution unit -- and those 14 commands are -- are, by the way, your alleged tasks, 15 or they make up your alleged tasks, correct? 16 A Correct, yes. 17 Q Any one command may not be a singular task, 18 it may take multiple commands to make up a task, 19 correct? 20 A That is correct, yes. 21 Q Okay. And the work distribution receives 22 commands from the front end unit, correct? 23 A I believe so, yes. 24 Q And there's no disclosure in the reference 25 that the front end unit processes the commands,	296 1 that the data flow is established, and so -- but 2 definitely the point is not that -- that one of 3 those blocks by itself can do all of these things or 4 can do even some of these things. 5 It's just I identified them in a way that 6 the data flow is established -- 7 Q Okay. 8 A -- present. 9 Q Well, the host interface, you'd agree with 10 me, can be also considered an engine to a POSITA, 11 correct? 12 That's a -- it receives a plurality of 13 tasks? 14 A Maybe, but -- but that's not what I 15 identified. 16 I just wanted to have enough of the 17 components that I'd like to map so that I show that 18 this plurality of engines are there; and the front 19 end unit 212 and the work distribution unit 210, I 20 identified because they talk to each other, and then 21 according to Phase 301 -- 303 -- 22 Q But you'd agree with me, though, that 23 the -- the front end doesn't receive the alleged 24 tasks directly from the scheduling module, it 25 actually receives it from the host interface,

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297 1 correct? 2 A But the host interface is getting it from 3 the software driver or from the -- that's running on 4 the host CPU, so the -- the -- the originator of 5 these set of tasks was the software program running 6 on the host CPU similar to '381 where the scheduling 7 module was the operating system, and then that 8 scheduling module associated with their CPU, second 9 processing unit, is very similar to what Wilt is 10 doing, so I'm not sure what the objection here. 11 Is in the same way that 381 can do it, Wilt 12 also discloses it. 13 Q In your earlier testimony, you indicated 14 that to receive the plurality of tasks from the 15 scheduling module, it -- receiving it indirectly 16 from another component, that would render that 17 limitation meaningless. 18 That was your testimony, sir. 19 A But that -- that was -- when we are talking 20 about the plurality of engines and what's included 21 in the engines and the association of a scheduling 22 module to a second processing unit, I was not 23 talking about the host CPU having an OS running on 24 it and how does the OS provide that information to a 25 graphics processing unit or card that has all these	299 1 is on Wilt's GPU. 2 A I guess in retrospect, yes, you could -- I 3 could have done it. Again, I didn't do it. I 4 didn't feel it's necessary; but I don't see, as I 5 stand here and look at the drawing -- I tend to 6 agree with you why -- why not. 7 I mean, I could have also said host 8 interface 206 would be one of the engines. I didn't 9 say it; I didn't feel the need to say it; but I'm 10 not excluding it, necessarily. 11 Q Paragraph 227 of your report, which is on 12 Page 92, you'd agree with me that tasks would be 13 decomposed into shader programs, correct? 14 A What I can say is the tasks get decomposed 15 into threads, and the threads comprise of 16 instructions. 17 Whether you consider a shader program 18 itself to be a thread, probably yes in the context 19 that we are discussing. Yeah, sure. 20 Q I'm reading your -- 21 A Yeah. 22 Q -- literally reading from your report, and 23 you say this task will be decomposed into a 24 plurality of fixed-function graphics operations, 25 e.g., vertex and cover pixel generation, and shader
298 1 engines and shader core and so on and so forth on 2 it. 3 The fact is that there's going to be no 4 direct connection from the host CPU to a GPU. I 5 mean, there are buses, there are interface 6 controllers, there's lots of things in between, 7 so -- 8 Q So you could consider both the host 9 interface and the front end to be engines, correct? 10 Each individually an engine -- correct? -- with the 11 definition that you apply? 12 A I've not done that, so I -- I've not done 13 that. Again, maybe there is a -- a second way of 14 doing it, which I've not done. 15 Q I'm asking you to apply your definition, 16 sir. Apply the definition that a POSITA would -- 17 you -- you -- you have testified that you are a 18 POSITA -- 19 A Yes. 20 Q -- and that you've reviewed the patent. 21 Apply your lens of a POSITA and the 22 definition and tell me why wouldn't you consider the 23 host interface to be an engine? 24 And I'll point out to you host interface is 25 not the host CPU. That's a device that is -- that	300 1 programs, e.g., vertex processing, lighting, line 2 segment processing, pixel processing, color, and 3 texture mapping. 4 So I'll -- I'll repeat my question to you 5 again. You would agree that tasks, a person of 6 ordinary skill in the art would understand that they 7 get decomposed into shader programs, correct? 8 A So it depends what the -- the definition of 9 the task is, but yes. That's a "yes," but it 10 depends really on the definition because there 11 are -- when you say tasks, it could be high-level 12 tasks, lower-level tasks -- 13 Q Well, let's ask -- talk about that. 14 So the task that's defined in the '381 15 patent is the high-level task, right? Is the 16 higher-level task? 17 A Yes. 18 Q Okay. We're not -- the '381 patent, when 19 it's talking about tasks, it's not talking about 20 lower-level tasks, correct? 21 A Yes, I tend to agree with, yes. 22 Q It's not talking about tasks, for example, 23 that are later generated by a shader program, 24 correct? 25 A I -- I tend -- yes.

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301 1 Q Okay. It -- it -- meaning -- I want to 2 make sure that I get a clear answer from you. 3 When the '381 patent refers to "tasks," 4 it's not referring to the types of lower-level tasks 5 that might be generated by a shader program, 6 correct? 7 A Yes. 8 Q Okay. Let's -- still on Wilt, you opine in 9 your report -- sorry. Let me withdraw that. 10 Wilt doesn't expressly disclose that 11 multiple tasks in the context of the '381 patent 12 definition of tasks are received by the alleged 13 plurality of engines at the same time. At best, 14 Wilt discloses that more than one command is 15 received by the engines, correct? 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: I mean, Wilt speaks of 18 commands related to processing tasks that are 19 received and -- and -- and -- and sort of processed, 20 and so on, so I -- I agree with you that he talks 21 about these commands being received, but he does say 22 that they are associated with tasks, processing 23 tasks. 24 He has explicit language that says it, 25 right?	303 1 minute. I need to remind myself of something. 2 Q Sure. 3 Okay. I don't know if it's helpful or not, 4 but in Wilt, Tab 17, Figure 2 shows what I believe 5 you're referring to as the cores, the individual 6 cores of the PPU, and I -- I think in your report, 7 on Paragraph 264, you're saying that the core inside 8 each PPU -- each -- each core is a claimed shader 9 core. 10 A Okay. Yes, the -- the core 208 inside each 11 PPU is the claimed shader core. 12 Q Okay. That's what you're -- so the 13 structure -- just to get the record clear here, the 14 structure that you're -- in Wilt that you're 15 alleging is the claim shader core is a single core 16 within a PPU, correct? 17 A I think I have an alternative in which -- 18 I'm looking for that alternative, but I couldn't 19 find it as I'm looking at it now, but I believe I 20 have an alternative in which I describe the PPU also 21 to be the whole PPU, which includes -- not the -- 22 Q I don't see it here in Paragraph 264. 23 A No, in Paragraph 264, you're right. 24 Q It's not there, right? 25 A Yes.
302 1 MR. RIZK: No, he doesn't. So let's talk 2 about the shader -- 3 THE WITNESS: I can read it to you. 4 MR. RIZK: Let's talk about the shader core 5 15-E and your allegations with respect to -- to 6 Wilt. 7 Q Wilt doesn't explicitly disclose that 8 the -- your alleged shader core in Wilt executes 9 multiple tasks at the same time; and for the record, 10 I -- I believe that you're alleging that each core 11 in the PPU is the claimed shader core; that a single 12 core within the PPU is the claimed shader core. 13 So let me withdraw the question and ask it 14 again. 15 You -- in your -- in your opinion, you 16 identify the core as the claimed shader core, Wilt's 17 core, correct? 18 THE WITNESS: Page -- 19 MR. JOHNSON: Objection -- 20 MR. RIZK: 264, Paragraph 264 of your 21 report. 22 MR. JOHNSON: Objection; form. 23 MR. RIZK: Page 110. 24 Q Do you see Paragraph 264, sir? 25 A Yes. I'm sorry. Yes. Just give me a	304 1 Q And if you find it somewhere else in your 2 report, feel free to let me know; but I haven't -- I 3 haven't seen any alternatives. 4 In Paragraph 264, that's where you provide 5 and state your opinion about how Claim 15-E is met, 6 correct? 7 A Correct, yes. 8 Q Okay. And there, the structure that you 9 identify corresponding to the claimed shader core is 10 for a single core within PPU, correct? 11 A Yes, that's what it says, yes. 12 Q Okay. Okay. And you would agree with me 13 that you cite to -- to a number of disclosures in 14 Wilt suggesting that the shader core is configured 15 to execute concurrent tasks based on respective 16 state parameters; but I didn't see that disclosure 17 in Wilt, at least as to the higher-order tasks that 18 are covered by the '381 patent, so is it your 19 understanding when you -- when you -- when you say 20 that it executes concurrent tasks, you're referring 21 to the lower-level types of tasks, not the type that 22 are referred to in the '381 patent, correct? 23 MR. JOHNSON: Objection; form. 24 THE WITNESS: So to -- it's not a yes-or-no 25 answer.

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305 1 BY MR. RIZK: 2 Q Well, there's no explicit disclosure in 3 Wilt of the higher-order tasks that are described by 4 the '381 patent being -- multiple of those being 5 executed simultaneously on a single core, correct? 6 A So that's not my reading of the -- Wilt. 7 When I read Wilt and -- and the citations that I 8 have here, my conclusion has been that it allows for 9 multiple tasks, even higher-level tasks, to be 10 running concurrently, not directly, because those 11 tasks get decomposed into shaders and threads and 12 instructions and so on; but when you do those 13 lower-level commands or instructions in parallel, 14 you are actually doing different tasks in parallel. 15 Q Yeah, but are you referring to higher-order 16 tasks as described in the -- 17 A Even higher-order tasks, yes. 18 Q Okay. Okay. So I just want to understand 19 where is that explicit disclosure that says -- 20 because it's not necessarily the case that a system 21 that is capable of executing multiple lower- -- 22 lower-level commands in parallel is necessarily 23 capable of executing multiple higher-order tasks in 24 parallel, agree? 25 A No, it is. To me, it's clear that if a	307 1 Q Well, but it -- it could also be executing 2 multiple instructions corresponding to a single 3 task. You don't know that from looking at Wilt. 4 MR. JOHNSON: Objection; form. 5 THE WITNESS: It may also be that, but -- 6 MR. RIZK: In fact, let me -- let me direct 7 your attention to Column 3, Line 60 through 67 of 8 Wilt; and there it says that the front end is a -- 9 of conventional design. 10 Q You can't -- you don't know one way or the 11 other if that conventional design of the front end 12 actually had the serialized command buffer structure 13 that was described as a conventional design in the 14 '381 patent, do you? 15 MR. JOHNSON: Objection; form. 16 THE WITNESS: First of all, your reading of 17 that particular excerpt is -- is, I think, 18 incorrect. He's not saying that -- Wilt is not 19 saying that these are all designed as a conventional 20 design; he's just saying the host interface, front 21 end unit, and memory interface have a conventional 22 hardware design, right? 23 BY MR. RIZK: 24 Q Okay. And that conventional hardware 25 design might include a serialized command buffer,
306 1 system can process multiple threads at the same 2 time, it does not necessarily care about whether 3 those threads belong to the same higher-level task 4 or multiple different higher-level tasks. 5 I understand that maybe some portions of 6 this structure would be SIMT, and -- and which is -- 7 which allows still by -- for different structures to 8 run statement; but the -- the full system can still 9 run concurrent high-level tasks. 10 Q Well, that presumes, of course, that 11 there's sufficient infrastructure in the GPU that 12 would allow more than one task to be provided to the 13 alleged shader core for processing simultaneously; 14 and as we saw in the '381 patent, there were 15 conventional systems that utilized a serialized 16 command buffer structure that only submitted one 17 task at a time for processing. 18 And Wilt doesn't actually disclose what its 19 command buffer structure is; do you agree? It 20 doesn't say "command buffer" anywhere in Wilt? 21 A But Wilt has this parallel processing 22 subsystem that includes multiple PPUs, and these 23 multiple PPUs could be executing multiple sets of 24 instructions responding to multiple higher-level 25 tasks.	308 1 correct? As described in the '381 patent? 2 A That's not my understanding. 3 Q Where does Wilt say that it utilizes the -- 4 the invention of the '381 patent -- 5 A It doesn't. 6 Q It doesn't. 7 A No, it doesn't. 8 Q So -- so you don't know -- 9 A But that's not the only way. 10 Q You don't know if the -- the front end that 11 is disclosed in Wilt -- Wilt is silent as to the 12 structure of its front end, correct? 13 A Yes, because it -- it will enable multiple 14 parallel threads to run, and a person skilled in the 15 art looking at Wilt would understand that because of 16 all the resources and all the capability that Wilt's 17 system provides, multiple tasks could run in 18 parallel; and you're saying the only way -- I mean, 19 I guess the implication of your question is the only 20 way to enable execution of multiple threads that 21 belong to multiple high-level tasks is to use the 22 '381 patent. 23 No. They have their own scheme to do it, 24 they have their own design. 25 Q But it doesn't disclose any specific design

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1 to enable, so if you -- you don't know what the 2 command buffer structure is. You don't know if it 3 uses what was described as the conventional 4 serialized approach in the '381 patent or if it uses 5 something else. It's silent on what the front end 6 structure is, isn't it? 7 MR. JOHNSON: Objection -- 8 MR. RIZK: It says that the front end 9 structure is conventional design and isn't described 10 in this reference. 11 Q Isn't that what it says? 12 MR. JOHNSON: Objection; form. 13 THE WITNESS: It says the internal design 14 of those components. I mean, my reading of this -- 15 when I look at that sentence, my reading is that, 16 well, I don't have really to tell you how to do a 17 memory interface. It's well-known. 18 MR. RIZK: Okay. 19 THE WITNESS: You just use the memory 20 interface design, right? It's not saying now 21 internally, when I -- when I look at this how the 22 front end unit is organized and -- and it -- it just 23 says you can use sort of conventional hardware 24 design techniques to do it. 25 MR. RIZK: Okay.	309 1 you provided an answer to my question. 2 So my -- my question -- my next follow-up 3 question to you is, if, in fact, the front end that 4 is identified in Wilt uses as its design the 5 serialized command buffer structure that is 6 described in the background section of the '381 7 patent, which -- of conventional design, then you 8 would agree with me that it is possible that the 9 alleged shader core, the core within the PPU of 10 Wilt, only processes one task at a time? 11 A So this is a hypothetical. You're saying 12 let's assume that the Wilt system actually adopts 13 and uses the command buffer structure that was 14 revealed -- disclosed in '381 patent as a serial 15 command buffer structure, and then subject to that 16 happening, it's possible that the alleged shader 17 core within the PPU of Wilt only processes one task 18 at a time. 19 Yes, it's possible; but otherwise is also 20 possible. 21 Q Okay. And you don't know, to be clear -- 22 you don't know what the command buffer structure of 23 Wilt is, correct? 24 A No, I don't know the command buffer 25 structure of Wilt; but I know from the -- the
310 1 THE WITNESS: It's not anything about the 2 architecture and the flow of the threads or tasks -- 3 MR. RIZK: It doesn't say conventional 4 design techniques, sir. It says conventional 5 design, generally conventional design. Those are 6 two different things. It's not talking about design 7 techniques, so let's just -- let's keep it -- let's 8 keep it accurate. 9 Q But you would agree that a conventional 10 design of a GPU that was known at the time of Wilt 11 was the -- the serialized command buffer structure 12 that is described in the background section as a 13 conventional design in the '381 patent? 14 A Yes, a conventional design of a GPU would 15 have been that; but there are other conventional 16 designs of a GPU that might not use a serialized 17 command -- command buffer even at the time of the 18 invention. 19 The -- the -- the point here is that -- 20 Q I'm not -- 21 A -- the '381 did not claim in any of its 22 claim language this non-serialized command buffer, 23 asynchronous dispatch, this and that -- none of it 24 is actually in the claims -- 25 Q Okay. I think I have -- I got -- you --	312 1 various disclosures in Wilt with so many PPUs 2 existing, so many cores, that multiple -- many, many 3 threads would be running, and there is no reason to 4 assume that these threads will all have to 5 correspond to a single high-level task. 6 In fact, unlikely. The -- the -- it's much 7 more likely that multiple high-level tasks are 8 running, each generating its own set of threads, but 9 then running -- running on different resources. 10 Q You haven't identified any definitive 11 evidence of that beyond a lot of threads are 12 running; and with all due respect, sir, you're a 13 person of ordinary skill in the art, you understand 14 that multithreading and multitasking are two 15 different constructs and concepts, and it isn't 16 necessary that just because you have a processor 17 that is running a lot of threads, that it is 18 necessarily running a lot of tasks. 19 That's separate functionality that would be 20 built in, and Wilt just doesn't disclose that. 21 It -- you -- you can't show me the infrastructure 22 that is necessary because Wilt is silent on how its 23 front end is constituted. 24 MR. JOHNSON: Objection; form. 25 THE WITNESS: Again, there's not my

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313 1 understanding as a POSITA of -- of Wilt's reference. 2 To me, Wilt's review of the system that he 3 describes, all of the capabilities that it offers, 4 all of the ability to run many, many threads, it -- 5 it -- it can run multiple tasks, high-level tasks at 6 the same time. 7 BY MR. RIZK: 8 Q Okay. So your opinion is if a reference 9 merely can run a lot of threads, then that means 10 that it necessarily has the capability and 11 functionality of running multiple tasks on a single 12 shader core at the same time? 13 A That's not -- 14 Q That's your testimony? 15 A No, that's not -- 16 MR. JOHNSON: Objection; form. 17 THE WITNESS: That's not my testimony. 18 I'm saying if I look at the Wilt's system 19 with the description that I see for Wilt's system in 20 terms of all the PPU contacts that are different 21 from each other, why would you have different PPU 22 contacts if you're trying to run the exact same 23 tasks? 24 So you have different PPU contacts that are 25 being provided; these contacts are being --	315 1 parallel processing unit to satisfy 2 the first processing unit of 3 Claim 15. 4 Is that -- that's your opinion, right? 5 A Yes, that's what I've said, yeah. 6 Q Okay. Let's go to -- to Jao. 7 On Jao, I think we already have where you 8 stated your opinion on Jao, but just to reorient 9 here, I think you started your opinion on Jao on 10 Page 86, Paragraph 216. 11 A Yes. 12 And what tab is Jao? 13 Q Jao would be Tab 16. 14 I think you already testified today -- do 15 you have it in front of you? 16 A Yes. 17 Q Okay. You already testified today that 18 the -- Jao's vertex shader 304, geometry shader 306, 19 pixel shader 310, those are your alleged engines, 20 right? 21 A Yes. 22 Q Okay. And those are shader programs, 23 right? 24 A Yes. 25 Q So you're alleging now that an engine can
314 1 MR. RIZK: We're -- sir, we're only talking 2 about a single PPU. That's -- that was your 3 opinion. I'm not asking you about different PPU 4 contacts with different PPUs. I'm asking about a 5 single PPU, cores inside of a single PPU. 6 That was what was in your report -- 7 THE WITNESS: Right. 8 MR. RIZK: -- and that's what I'm asking 9 you about. 10 THE WITNESS: But a PPU context for a 11 high-level task -- for a high-level task itself -- 12 so the PPU context could correspond to multiple 13 high-level tasks, so I have the -- 14 MR. RIZK: It could but it could not. 15 Q It could correspond to a single task, 16 correct? 17 A It -- it could also, yes. 18 Q All right. Your opinion -- Paragraph 259 19 of your report, your opinion is based on a single 20 PPU is the first processing unit, correct? 21 You identified Paragraph 259. I'll just 22 read it into the record. 23 (Reading:) 24 A person of ordinary skill in 25 the art would understand Wilt's	316 1 be a shader program? That's your testimony? 2 MR. JOHNSON: Objection; form. 3 BY MR. RIZK: 4 Q If it's helpful -- are you trying to figure 5 out whether or not they're shader programs? 6 A Yeah. 7 I'm looking at my -- 8 Q I'll just direct your attention, because 9 we -- we don't have -- we're running out of time 10 here, sir, and we need to move it along. 11 So Column 6, Line 59, of Jao, various types 12 of shader programs can be executed or mapped for the 13 computational core 204, including the vertex shader 14 304, geometry shader 306, and pixel shader 310. 15 You agree with me that those three things, 16 the vertex shader 304, geometry shader 306, pixel 17 shader 30 -- 310 are shader programs, correct? 18 A So the -- the distinction here is that 19 there are instances of a shader program or there 20 are -- where the shader programs of appropriate 21 time -- type arrive and get sort of transmitted to 22 down -- to downstream pipeline, so the vertex shader 23 304, of course, is instead of generating these 24 vertex shaders and sending them through -- but it's 25 not just one vertex shader sitting there, it's an

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317 1 engine that routes the vertex shading tasks down to 2 the downstream pipeline. 3 Q Okay. Number one, it doesn't say instance 4 of a shader program here, does it? 5 A No, but that's my -- 6 Q Does it -- does it use those words again? 7 A No; but, again, a POSITA looking at this 8 would understand that it doesn't make sense for the 9 VS-304, for example, which is the vertex shader, to 10 be just one instance of a program, right? 11 I mean, it has to be some -- some -- some 12 block, some engine that generates various vertex 13 shading program or receives them somehow and passes 14 them forward to the rest of the system. Otherwise, 15 the system is useless if I can only do one specific 16 instance of a vertex shader. 17 Intrinsically, almost, it's evident that 18 these -- these -- these units would be receiving 19 different instance of a vertex shading tasks, and 20 then sort of pass them through to the rest of the 21 pipeline. 22 Q Agree or disagree, vertex shader 202, pixel 23 shader 204 -- I'm sorry. I messed up the numbers -- 24 vertex shader 304, geometry shader 306, and pixel 25 shader 310 are shader programs?	319 1 computing requirements imposed by 2 shader tasks associated with 3 various shader programs, including 4 a vertex shader, geometry shader, 5 and/or pixel shader, processing 6 data for the graphics pipeline? 7 Do you see that? 8 A Yes. 9 Q Okay. So I think we've established now 10 that vertex shader 304, geometry shader 306, pixel 11 shader 310, those are shader programs, correct? 12 A Yeah, they are shader programs. 13 Q Okay. 14 A I have -- 15 MR. RIZK: That's all I'm asking, sir. 16 (Mr. Rizk and the witness speak 17 simultaneously.) 18 MR. RIZK: That's all I'm asking. 19 Q So it's your opinion that an engine can be 20 a shader program, correct? 21 A Again, the nuance here is that it's not 22 just one shader program, it's just that you -- the 23 shader programs of a given type arrives through that 24 path and get distributed to the rests of the system. 25 Q An instance of a shader program can be an
318 1 A This is where the vertex shader programs 2 arrive and get rerouted for sure, yes; and -- and 3 similarly for the GS and the PS in the block diagram 4 of 204 that I see, right? 5 So -- because this is -- Figure 4 6 embodiment that I have in front of me is the general 7 description of the processing engine of Jao; and, 8 obviously, it cannot be that there is just one 9 vertex shader program that's -- that's there, right? 10 So multiple vertex shader programs comes 11 throughout that channel -- right? -- and then gets 12 routed to the rest of the system. 13 Q Doctor, I'm going to withdraw my last 14 question. This is a yes-or-no question. 15 Is vertex shader 304 a shader program, yes 16 or no? 17 A Yes, it's a shader program. 18 Q Okay. And I'm going to read to you from 19 Column 5 of the -- of the '774 Jao patent, which is 20 the Jao patent that you relied upon for your 21 invalidity opinion, Line 47. 22 It states (reading): 23 The computational core 204 24 comprises a pool of multiple 25 execution units to meet the	320 1 engine, in your opinion as a POSITA, correct? 2 A I didn't say that. 3 Did I say that? 4 Q Okay. Well, you're pointing to the 5 individual pixel shader program, geometry shader 6 program, vertex shader program as the alleged 7 engines, are you not? 8 You say -- I'll read it to you in 9 Paragraph 223 of your report (reading): 10 A person of ordinary skill in 11 the art would have understood the 12 vertex shader 304, geometry shader 13 306, the pixel shader 310 in the 14 graphics pipeline 208 of GPU 114 to 15 be engines. 16 That's what you said in your report. 17 A Yes. 18 Q Okay. So you would understand -- your -- 19 your testimony today is that a POSITA would 20 understand that a -- a shader program can be an 21 engine? 22 That's your testimony? 23 A Shader programs -- 24 Q No. I want single -- single -- you 25 identified each one of those as an engine, so we're

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321 1 not -- we can talk about programs later, or your 2 counsel can clean it up on redirect. We're talking 3 about each one, you alleged as an engine, and each 4 one is a program. 5 So is it your opinion, yes or no, shader 6 program can be an engine? 7 A The vertex shader programs would -- would 8 constitute one engine, the geometry shader programs 9 another engine, the pixel shader program is another 10 engine. 11 That's what I see. 12 Q Okay. And at -- at least in Jao, what it 13 discloses is that those shader programs that you 14 identify as your engines, they generate some form of 15 lower-level task, correct? 16 If it's helpful, Jao, Column 9, 35 to 38. 17 A Yes, that's what it says, the various 18 shader tasks are generated by the vertex shader 304, 19 and so on and so forth. 20 Q But you're not relying on those lower-level 21 tasks as the tasks that satisfy the claim language 22 for simultaneous execution of tasks by the shader 23 core, are you? 24 A The -- the -- the way the task has been 25 construed by the Court is that it's a unit of	323 1 Q You'd agree that the patent, the '381 2 patent, when it's talking about its tasks, it states 3 that a task can comprise multiple pixel shader and 4 vertex shader programs, correct? 5 A Yes -- 6 Q A single task can comprise more than one 7 pixel and vertex shader program, correct? 8 A That's possible, yes. 9 Q Well, that's what the patent says. 10 A Yeah, high-level task, yes. 11 Q Okay. And that's the task that's -- that 12 we're talking about in the '381 patent. 13 A Yes. 14 Q Okay. So merely having tasks that are 15 generated by shader programs, by a vertex and pixel 16 shader program, doesn't mean that you have multiple 17 of the higher-level tasks that are described by the 18 '381 patent. 19 The -- the -- if you have a single vertex 20 shader program, single pixel shading program, 21 they're both generating lower-level tasks, the sum 22 of those lower-level tasks does not necessarily 23 equal multiple higher-level tasks, agree? 24 A Not necessarily; but also it's quite 25 possible and, in fact, more than likely --
322 1 workload or a portion of an application running in 2 the system, and the portion of the workload could be 3 interpreted at different levels of granularity, so 4 that's one point. 5 The second point I'd like to make is that 6 when I have a high-level task, this high-level task 7 generates, maybe, some lower-level tasks; and if I 8 process all of the lower-level tasks, I've actually 9 processed the high-level task. 10 I don't see a discrepancy here; so when I 11 say I've finished all of my lower-level tasks, I've, 12 obviously, finished also the high-level task. So 13 let me say it one more time more clearly. 14 I have a high-level task, it generates 15 multiple lower-level tasks. I receive all of the 16 lower-level -- the lower-level tasks in some order 17 or fashion. I process them after having provided 18 them with the state data that -- that they need for 19 processing. 20 So once I'm done with that -- that, I've 21 actually received a high-level task, I've provided 22 the state data to it, I've processed it, I'm done. 23 I don't see a discrepancy here. 24 Q Okay. I'll try to point it out to you. 25 A Yes, please.	324 1 Q I'm not asking you about -- I'm not asking 2 about what's possible, Doctor. 3 A -- that it is -- 4 Let me just finish this. I'm sorry. 5 So it's possible and quite likely that, in 6 fact, they correspond to multiple higher-level 7 tasks. 8 Q There's no disclosure in Jao that says that 9 the tasks that are generated by the vertex pixel 10 shader programs correspond to the higher-level tasks 11 that are required and claimed in the '381 patent -- 12 no explicit disclosure, correct? 13 A I think you are reading into -- the Court 14 has done a claim construction. We have to go by the 15 claim construction. You cannot now change the claim 16 construction of the order by ALJ. 17 According to that claim construction, the 18 task is a work -- you need to workflow; so, in fact, 19 I could say, according to that construction, even a 20 shader task is a task. Even a lower-level task is a 21 task. 22 There is no distinction, according to 23 that -- so I understand from a sort of -- this -- if 24 I'm trying to explain the differences between Jao 25 reference versus the '381, you could draw a

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325 1 distinction between their high-level task and these 2 other lower-level tasks, but that's not Court's 3 construction. 4 You have to apply Court's construction. In 5 view of the Court's construction, ALJ's 6 construction, I do stand by my testimony and my 7 opinion here that, in fact, multiple tasks are 8 running in -- in Jao's system. 9 Q So your view is that under the Court's 10 construction, the lower-level tasks that are 11 generated by the shader program, even if they don't 12 correspond to multiple higher-level tasks, would 13 qualify as multiple tasks as the Court has construed 14 that term? 15 A Yes. 16 Q Okay. And correspondingly, if we apply the 17 Court's construction, threads would also qualify as 18 tasks under the Court's construction? 19 A No, no. 20 Q Why not? 21 A I think that the ALJ was very clear that 22 tasks are not threads, and so threads are a -- a -- 23 a different construct than a -- a task as construed 24 by the Court. 25 Q It's -- it's a unit of processing work.	327 1 that makes one a task and the other not? 2 Let's presume for a moment, sir, that the 3 court determined -- the court goes with your earlier 4 testimony today, which is that how the '381 patent 5 describes task is of the higher order of task 6 variety. 7 Are you with me? 8 A Yes. 9 Q Do you understand what I'm asking you to 10 assume? That's a reasonable assumption, right? 11 Because that's how you'd understand "task" as 12 described by -- 13 A No, I -- I don't understand task to be only 14 high-level task. It could be also low-level task. 15 Q No, no. I'm asking you in terms of '381 16 patent. 17 A Yeah, I think in '381, my reading would be 18 it's a higher-level task, but -- 19 Q Okay. So let's presume that the court goes 20 with the reading of the '381 because that's -- that 21 is something that's reasonable for the court to do. 22 If the court goes with the reading of the 23 '381, the generation of the multiple tasks by those 24 shader programs that you identified in -- in Jao 25 doesn't necessarily correspond to generation and
326 1 A But -- but that's how it's been construed, 2 so the -- the construction here is that the task is 3 a unit of processing load, and that might be 4 decomposed into threads that have associated state 5 data that they -- they need -- 6 Q I'm sorry, sir, but -- but, actually, the 7 court didn't construe threads in this case. 8 A Yeah, I know. It just said tasks, right, 9 so -- 10 Q So -- so why can't a thread be a task? 11 A But I've said in my report that thread is 12 not a task. 13 (Mr. Rizk and the witness speak 14 simultaneously.) 15 MR. JOHNSON: Don't talk over each other, 16 please. 17 MR. RIZK: I know that's what you said, but 18 now you just testified that a task doesn't need to 19 be of a higher-order-type task, and instead, it 20 could be something that's just generated by a -- a 21 shader program, and -- and not -- and still meet the 22 court's definition of task. 23 Q So I just want to understand what is the 24 difference between the -- the lower-level tasks that 25 are generated by these shader cores and a thread	328 1 simultaneous execution of multiple higher-order 2 tasks as described in '381? 3 A Under that hypothetical, the conditions you 4 described, yes. 5 Q Well, let's -- let's make sure I 6 understand -- get that correctly. 7 Under the hypothetical I described, you 8 would agree with me -- I'll make this a yes-or-no 9 question. 10 A Please. 11 Q You would agree with me that under the 12 hypothetical that I described, which is the Court 13 agrees that the task that is described and claimed 14 by the '381 patent is of the higher-order variety, 15 which is, I believe, your understanding of task -- 16 in that circumstance, the tasks that are generated 17 by the shader programs you identified in Jao do not 18 necessarily correspond to multiple of the '381 19 tasks, correct? 20 A I tend to agree. 21 Q Okay. And -- and, therefore, again, if 22 that's the construction that the Court applies and 23 the lens that the Court applies for the term 24 "tasks," the -- there isn't evidence in Jao 25 separately that the -- the alleged shader core would

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329 1 execute multiple of those higher-order tasks, 2 correct? 3 A So -- so -- so, again, a POSITA reading Jao 4 would understand that there are so many tasks 5 running, low-level tasks running, and he would not 6 presume that they all belong to the same high-level 7 task, so that presumption that because it's not 8 clearly being stated in Jao that these lower-level 9 tasks correspond to multiple high-level tasks, 10 therefore, that possibility is not there, is not 11 warranted. 12 But I do agree in that case Jao does not 13 explicitly describe high-level tasks of-- of-- of 14 '381 type and describes its own tasks, which are 15 all, according to ALJ's construction, still tasks. 16 Q Okay. So if you apply the -- the lens of a 17 POSITA -- I'm not asking you to apply a strict 18 application of the ALJ's construction, but how 19 the -- you know, how you would understand tasks as 20 described by the '381 in view of the Court's 21 construction, just to be clear, Jao is silent one 22 way or the other whether the alleged shader cores -- 23 the alleged shader core can execute multiple 24 higher-order tasks in parallel? 25 A As I stand here today and as I recall, no,	331 1 your hypothetical, that's a different situation; but 2 according to current ALJ's construction, the tasks 3 that Jao describes are going to correspond to -- are 4 going to be running parallel -- in parallel and they 5 correspond -- they're different. 6 MR. RIZK: Well, to be fair to the ALJ's 7 construction, the ALJ's construction actually 8 defines a task as a unit of processing work -- 9 THE WITNESS: Yes. 10 MR. RIZK: Okay? 11 -- and that unit of processing work comes 12 from a scheduling module; so when you're thinking 13 about what that unit of processing work is, it is a 14 that higher-order unit of processing work. 15 Q So if you interpret the ALJ's 16 construction -- let me -- let me put it to you this 17 way. If you interpret the ALJ's construction of 18 unit of processing work to refer to the unit of 19 processing work of the scheduling module -- okay? 20 Are you with me? 21 A Uh-huh. 22 Q Do you understand what I'm asking you to 23 do? 24 Then that would be consistent with your 25 reading of the '381 patents and its disclosure of --
330 1 I don't think it does; but, again, maybe I'm missing 2 something. 3 At this point, as I stand here -- 4 Q I don't understand what you mean. And 5 I'm -- I'm sorry, sir. I'm just trying to get 6 clear -- 7 A Yeah, the question is also -- 8 Q I'm asking you -- I think the answer is 9 yes, that the -- that Jao is silent, it doesn't talk 10 about how many higher-order tasks are executed in 11 the alleged shader core, it only refers to the 12 lower-level tasks. So I'll -- I'll restate my 13 question. 14 A person of ordinary skill in the art 15 applying the ALJ's construction and the description 16 of what a task is in the '381 patent would not be 17 able to tell definitively from looking at Jao 18 whether the alleged shader core executes one task at 19 a time or multiple tasks simultaneously? 20 MR. JOHNSON: Objection; form. 21 THE WITNESS: I -- I disagree with this 22 because you -- you -- you block the ALJ's 23 construction. I -- I -- I -- I do stated it before 24 also that according to ALJ's construction, current 25 construction -- if it revises it to come up with	332 1 of its tasks, correct? 2 A I disagree, and I have reason for this 3 disagreement. 4 Q Okay. 5 A There are many different APIs, application 6 programmer interfaces, between the CPU and the GPU. 7 Some of these APIs are known to be high-level APIs, 8 such as, for example, CUDA programming or OpenGL, 9 some are known to be low-level APIs that actually 10 work much closer to the level of the shader tasks 11 that exist, and so depending on what the API is that 12 conducts the business between the CPU and the GPU, 13 you could be receiving directly through the channels 14 you're describing to me either a high-level task or 15 low-level task. 16 Q Okay. And if -- if the ALJ determines that 17 his construction means that it's the unit of 18 processing work that is supplied by the scheduling 19 module, whatever the alleged scheduling module is -- 20 in this case, I think in Wilt -- I'm sorry -- in 21 Jao, you identified the EU pool control as your 22 alleged scheduling module. 23 In that circumstance, the -- you can't tell 24 from looking at Jao whether or not multiple tasks 25 are executed simultaneously on the alleged shader

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333 1 core? 2 A Can you reformulate the -- 3 Q Yeah. 4 If the ALJ determines that the unit of 5 processing work has to be the unit of processing 6 work of the scheduling module, then you can't tell 7 from looking at Jao whether the shader core that is 8 alleged will necessarily execute multiple tasks at 9 the same time or will execute only a single task at 10 a time? 11 A I-- I disagree with this statement also. 12 Q And why is that? 13 A Because, as I said before, depending on the 14 API, the -- the kind of objects, items, that need to 15 be scheduled by the scheduling module could be 16 low-level or high-level tasks; and so -- depends on 17 that API more than anything else. 18 Now, if the -- the -- the Judge decides 19 that, no, my construction of the unit of workload 20 should be modified to say it's a high-level -- 21 higher level of unit of workload like this and that, 22 then I can agree to some of the questions you're 23 asking me to agree to, but otherwise no. 24 Q What makes it easy, though, is that these 25 tasks that you're referring to in Jao are actually	335 1 You don't know if the tasks that are 2 generated by those shader programs and executed at 3 the same time on a shader core correspond to a 4 single task at a time executed on -- on the shader 5 core or multiple tasks executed at the same time on 6 a shader core. 7 So do you -- do you agree or disagree with 8 that? 9 A So, again, Jao is silent on what kind of 10 API exists in his system in terms of the type of 11 tasks that comes through the -- the scheduling 12 module; so if you want me to agree that, yeah, it's 13 silent on the -- on the question, fine. 14 Q Okay. And, in fact -- so for any given 15 number of tasks that are generated by Jao's shader 16 programs, you can't tell me definitively that while 17 you -- you know that they may be executed at the 18 same time as lower-level tasks on the same shader 19 core, Jao is silent as to whether or not they -- 20 they could be grouped into multiple higher-order 21 tasks in the unit of processing work of the 22 scheduling module, correct? 23 A I-- I don't -- 24 MR. JOHNSON: Objection; form. 25 THE WITNESS: I -- I did not find
334 1 generated by the -- the vertex pixel and geometry 2 shader programs, right? 3 A Programs, right. 4 Q Right? 5 So -- so you know for a fact that those 6 aren't the units of processing work of the 7 scheduling module, those are generated on the fly by 8 the shader programs, so you can't tell from looking 9 at Jao that multiple tasks of the same unit of 10 processing work of the scheduling module are 11 executed simultaneously on its shader core, correct? 12 A I'm sorry. Ask the question again. I 13 can't make sense of the transcript, so please ask 14 the question again. 15 Q Sure. 16 I think you understood the fact that I gave 17 you to help you out with your answer, which is that 18 the shader programs actually just generate their own 19 tasks. 20 So there is no disclosure or correlation 21 between the tasks that are generated -- the 22 lower-level tasks that are generated by the shader 23 programs -- right? -- and the unit of processing 24 work that is supplied by your alleged scheduling 25 module, which, in this case, is the EU pool control.	336 1 citations, as far as I can recall now, that -- 2 anything in Jao that would distinguish between 3 high-level tasks and low-level tasks; so therefore, 4 the question you are asking me cannot -- is not 5 there -- the answer is not there because it doesn't 6 make that distinction. 7 The tasks come, and -- and then it gets 8 processed, so -- 9 MR. RIZK: Well, in fact, in Column 4, 10 Line 55 to 59, where it talks about the 11 implementation of Jao's graphics processor -- I'll 12 read it into the record. 13 It says (reading): 14 In some implementations, the 15 graphics processing system 100 may 16 be configured as a computer system. 17 The graphics processor system 100 18 may comprise a display device 102 19 driven by a display interface unit 20 GIU-104, and a local memory 106, 21 e.g., which may comprise a display 22 buffer, frame buffer, texture 23 buffer, command buffer, et cetera. 24 Q It doesn't say multiple command buffers, 25 does it?

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337 1 A No, it doesn't say multiple command 2 buffers. 3 Q Okay. So this could very well be -- this 4 command buffer structure that Jao actually discloses 5 could be the serialized command buffer structure 6 disclosed in the background section of the '381 7 patent and characterized as a conventional design? 8 A Or it may not. 9 Q Okay. But it could very well be that Jao 10 is designed in such a way that its command buffer 11 structure only emits one task at a time to the GPU, 12 one higher-order task at a time to the GPU? 13 A Or IT may not. 14 Q Okay. So you don't know, correct? 15 A I would not -- by looking at this one 16 reference, this one sentence here, I would not draw 17 the -- the conclusion you're trying to draw, drive, 18 no. 19 Q Well, you can't draw a conclusion one way 20 or the other? 21 MR. JOHNSON: Objection; form. 22 THE WITNESS: The conclusion I -- I -- I -- 23 I draw about the Jao system being able to process 24 multiple units of work is consistent -- 25 simultaneously is consistent with ALJ's construction	339 1 BY MR. RIZK: 2 Q By the way -- I'm sorry. Before we jump 3 there, so you're -- just to be clear, on the vertex 4 shader, pixel shader programs, those don't 5 actually -- they receive information from the EU 6 pool control; they don't actually receive the 7 higher-order tasks that you referred to earlier from 8 the EU pool control, necessarily. 9 Jao doesn't say that, agree or disagree? 10 A I don't remember. You'll have to show me 11 either -- 12 (Mr. Rizk and the witness speak 13 simultaneously.) 14 THE STENOGRAPHER: One at a time, please. 15 MR. RIZK: Sorry. 16 Let's go to Paragraph 224 of -- of your 17 report. 18 You say -- you identify the -- the alleged 19 engines as the -- the programs, the vertex shader 20 304, geometry shader 306, and pixel shader 310 21 program, and then you say these shaders receive and 22 process graphics data to produce pixel data. 23 Q Is that what you say? 24 A I'm sorry. I don't know which line you're 25 reading, so --
338 1 and is supported by the -- the disclosures in Jao. 2 You are taking the position that maybe we 3 should revise the construction of ALJ and -- 4 MR. RIZK: That's not the position -- 5 THE WITNESS: I'm sorry. Let me finish. 6 MR. RIZK: You've answered my question, 7 sir. 8 THE WITNESS: But I'm in the middle of my 9 question. I have to finish. 10 So you're -- you're -- you're making the 11 statement -- 12 MR. RIZK: What I'm saying doesn't matter, 13 sir. 14 THE WITNESS: Okay. But what I understood 15 you said -- that's -- that's important, right? So 16 what I understood you said was that are we going to 17 modify ALJ's construction so that it's not a 18 high-level task; and under that, then the -- the Jao 19 reference doesn't show multiple high-level tasks are 20 running in parallel, yes. 21 MR. RIZK: Okay. So let's turn to your 22 opinion on Paragraph 231 concerning loading of state 23 data. 24 THE WITNESS: Okay. 25 ///	340 1 (Mr. Rizk and the witness speak 2 simultaneously.) 3 THE WITNESS: You're going too fast for me 4 to follow. 5 (Mr. Rizk and the witness speak 6 simultaneously.) 7 BY MR. JOHNSON: 8 Q -- 223 of your report, you state a person 9 of ordinary skill in the art would have understood 10 that vertex shader 304, geometry shader 306, pixel 11 shader 310, and graphics pipeline 208 of GPU 114 to 12 be engines as cited in Claim 15. These shaders -- 13 A I'm sorry. What paragraph is it again? 14 Q I've stated it several times, but it's 223. 15 A 223. Because I see -- okay. 16 223. Okay. I see it now. All right. 17 Q So what these shaders receive is actually 18 graphics data, correct? 19 A E.g., graphics primitives, yes. 20 Q Okay. And that's your alleged task that -- 21 that the shader is receiving? 22 A What -- what is the alleged task? 23 Q The primitives. 24 A That's the -- that's the data, right? 25 Q Okay. So what's the alleged task?

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341 1 A The task is the task of shading. 2 Q Where -- how does it -- the -- all the EU 3 pool control vertex stream cache is providing are 4 vertex shader inputs, geometry shader inputs, and 5 vertex cache spill. 6 That's -- that's not tasks, that's data, 7 sir, correct? 8 A So this goes back to the answer I've 9 provided before that -- when I tried to distinguish 10 between a particular instance of a vertex shader or 11 a geometry shader versus the group of vertex shaders 12 and geometry shader programs coming through, I 13 explained to you that my understanding of Figure 4 14 embodiment of Jao is that in the block diagram, when 15 they show 204 as part of the 204 is this GS-304 or 16 GS-306 or PS-310. 17 That's really the -- the -- the channels 18 through which the -- the -- the -- the different 19 shader -- corresponding shader programs arrive and 20 get rerouted through the rest of the system for 21 processing. 22 Q But that's not what the reference says. 23 The reference calls these shader programs. That's 24 what the reference says. 25 So I appreciate your, you know, bringing me	343 1 but, again, I have to be given time to even think 2 about the questions and -- 3 Q Nowhere in your report do you identify how 4 the driver sends tasks to the vertex shader, 5 geometry shader, pixel shader through the EU pool 6 control. 7 Do you see it somewhere in your report, yes 8 or no? 9 A So identify this scheduling module to be 10 the driver software, the driver software is the 11 driver that provides the various tasks. That's the 12 only way. The driver software will provide the 13 tasks to the GPU, and those tasks are received 14 through the different channels and then get 15 distributed. 16 Q Okay. But there's no -- you have pointed 17 to no disclosure in Jao that shows that that driver 18 program talks to the alleged vertex shader, geometry 19 shader, pixel shader through the EU pool control, 20 did you? 21 A That is correct, there is no -- no clear 22 description of that; but, again, a person skilled in 23 the art would understand that's how it works. 24 Q All I -- it was a yes-or-no question. 25 So let's go to Paragraph 231 of your
342 1 back to that; but respectfully, that's just not in 2 the reference, and you weren't able to show it to 3 me. But I'll -- I'll ask you a different question, 4 sir. 5 There is no evidence that the driver that 6 is disclosed in Jao actually sends its tasks to the 7 vertex shader 304, geometry shader 306, pixel shader 8 310, through the EU pool control and vertex stream 9 cache, correct? 10 And it's a yes-or-no question. 11 A So Jao discloses -- I'm reading 12 Paragraph 224 of my report -- that each execution 13 unit 420 of the EU pool 414 may store a plurality of 14 tasks or thread -- threads in some embodiments, up 15 to 32 at the same time. I give the citation for it. 16 He also teaches that there exists thread 17 slots within each of the execution units of the EU 18 pool. 19 Q I'm sorry, sir, but this has nothing to do 20 with drivers. I'm -- I've asked you a very specific 21 question. You're -- you're reading from your report 22 at this point as opposed to answering my question. 23 A I'm trying to remember the details because 24 these are complicated references with lots of 25 information; and I know we are trying to speed up,	344 1 report. 2 In Paragraph 231, you refer to thread slots 3 in combination with the shaders as -- as an engine, 4 correct? 5 A Yes. 6 Q Okay. You don't opine that the thread 7 slots load state data, correct? In your report? 8 A No, I haven't shown or -- or said anything 9 like -- like that in my report that I can see. 10 Q Thank you. 11 And you opine that the shaders -- the 12 shader programs load state data from the constant 13 data pool, correct? 14 A Again, you have to point me either to a 15 portion of my report -- 16 Q I pointed you to Paragraph 231, sir. 17 It says, in your -- in Paragraph 231, which 18 is what I pointed you to -- it says the following 19 (reading): 20 When rendering an object or 21 group of objects for a given 22 rendering context, a shader 23 utilizes a constant data pool. 24 That's what I believe you're -- you're 25 pointing to for loading state data, so your -- your

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345 1 opinion here is that it's the shaders that load 2 state data from constant data pool, correct? 3 A Yes, and -- and -- and that's -- yes. 4 Q Okay. And your support for that is you 5 cite to the background section of Jao, Column 1, 6 Line 50, through Line 58; is that right? 7 A Yes. 8 Q Okay. And that section, if we turn to it, 9 doesn't actually describe the functionality of the 10 shaders in Jao, correct? 11 I'll read it into the record. 12 (Reading:) 13 Each object or group of objects 14 may have specific visual properties 15 related to the appearance of 16 surfaces, e.g. materials reflecting 17 shapes, textures, et cetera, and/or 18 operations related to the same, 19 e.g., required transformations, 20 which may be collectively referred 21 to as a rendering context for this 22 group or group of objects. 23 When rendering an object or 24 group of objects for a given 25 rendering context, a shader	347 1 Jao? 2 A What -- what -- what I'm saying is that 3 this background section that -- that Jao has 4 describes some known practices that have been also 5 adopted here because Jao did not try to 6 differentiate and say, no, I do it differently. So 7 they do it this way, I do it this other way. 8 Normally that's how -- 9 Q You provided no motivation to combine in 10 your report of this sentence in the background 11 section of Jao with the embodiment that is disclosed 12 in Jao in which the GPU contains shader programs, 13 vertex shader, pixel shader, geometry shader? 14 It's a yes-or-no question. I want to know 15 did you specifically state a motivation to define 16 Jao's background section with Jao's disclosed 17 embodiments? 18 A I didn't -- 19 MR. JOHNSON: Objection; form. 20 THE WITNESS: I did not find the need to, 21 no. 22 MR. RIZK: You did not. Okay. 23 THE STENOGRAPHER: I can't go any further. 24 I'm -- I'm -- I'm dead. 25 MR. RIZK: Okay. I have like two questions
346 1 utilizes a constant data pool, 2 e.g., context-specific constants 3 stored in a constant buffer. 4 Do you see that? 5 A What was it? 6 I believe -- yeah, yes, sure. Okay. Yes, 7 I see it, yeah. 8 Q Okay. That's -- this -- this particular 9 excerpt that you've -- you've cited to, it appears 10 in the background of Jao, correct? 11 A Yes, it does. 12 Q Okay. This is referring to shader 13 operation generally, not specifically to the shader 14 programs that are identified in Jao, correct? 15 A I think they do apply to the shader 16 programs that are identified in Jao. Jao basically 17 is giving you background information, saying 18 remember all of this is important. My system also 19 satisfies this background. 20 It's not trying to actually distinguish 21 itself, saying, oh, this is prior art and my -- my 22 thing is different, so it does apply to -- 23 Q So you believe that this is actually -- 24 this background section in Jao is actually a 25 description of the embodiments that are disclosed in	348 1 left, literally. It's -- I'll tell you what. Why 2 don't we take a -- a five-minute break, and we 3 should be able to wrap up in a few minutes. 4 THE VIDEOGRAPHER: Stand by. 5 We're going off the record. The time is 6 1905. 7 (A recess was taken from 7:05 p.m. 8 to 7:09 p.m.) 9 THE VIDEOGRAPHER: We are back on the 10 record. The time is 1909 p.m. 11 MR. RIZK: Let's turn to Page 2 of your 12 report, which is Exhibit 1. 13 THE WITNESS: Yes. 14 BY MR. RIZK: 15 Q You've provided an obviousness opinion with 16 respect to Studdard and Kimura for the '053 patent, 17 correct? 18 A For the three -- 19 Q For the '053 patent, you allege the '053 20 patent to be -- 21 A Yes. 22 Q -- obvious in view of Studdard or obvious 23 in view of Kimura, correct? 24 A Correct, yes. 25 Q You don't allege anticipation by Studdard

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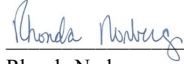
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1 or Kimura, correct? 2 A No, I did not. 3 Q Okay. And you provide, in your opinion, at 4 least the portions that haven't been stricken -- you 5 provide no evidence of what would -- what informs 6 your opinion of what a person of ordinary skill in 7 the art would know, correct? 8 MR. JOHNSON: Objection; form. 9 THE WITNESS: What does that mean? 10 BY MR. RIZK: 11 Q You don't cite to any evidence supporting 12 your positions on what a person of ordinary skill in 13 the art would know, correct? 14 A I've based it on it. 15 I'm not sure what that means. I really 16 don't know what you mean. I -- I have to disagree. 17 No. 18 Q In the -- in the non-stricken portions of 19 your report, you cite to no specific evidence of 20 what a person of ordinary skill in the art would 21 know to support your obviousness opinion for 22 Studdard or Kimura, correct? 23 A If by a specific evidence you mean 24 additional citations to other patents or documents, 25 no, I don't; but, of course, I've based my --	349 1 of a person of ordinary skill in the art, correct? 2 A Correct. 3 Q And the same thing for your obviousness 4 opinion of the '381 patent in view of Studdard, you 5 don't cite to a single reference other than Studdard 6 to support your obviousness opinion or the knowledge 7 of a person of ordinary skill in the art? 8 A Yes, sir, correct. 9 Q You have a 112 section where you allege 10 invalidity based upon lack of written description 11 and enablement of a hardware engine; is that 12 correct? 13 A Yes. 14 Q Okay. That's for the '381 patent. 15 Your opinion is that the '381 patent only 16 discloses a software-based virtual engine; is that 17 right? 18 MR. JOHNSON: Objection; form. 19 THE WITNESS: That's -- that's not what I'm 20 saying. I -- I think we have to read through that 21 section carefully; but basically what -- what I'm 22 saying is that based on the ALJ's construction of 23 the engines, plurality of engines, which is 24 hardware, software, or a combination thereof, when I 25 looked for any kind of evidence related to a
350 1 Q That's all I'm asking, sir. 2 A Yes. 3 Q You don't cite to a single reference other 4 than Studdard in support -- in support of your 5 obviousness opinion with respect to the '053 patent, 6 correct? 7 A That's -- 8 MR. JOHNSON: Objection; form. 9 BY MR. RIZK: 10 Q You don't cite to a single reference other 11 than Kimura in support of your obviousness opinion 12 of the '053 patent in view of Kimura, correct? 13 A External reference, I agree, I have no 14 other external references. 15 Q Okay. Same thing for your obviousness 16 opinion of the '381 patent in view of Jao. 17 The -- the only reference that you cite to 18 is Jao, you don't cite to any other references to 19 support your obviousness opinion or the knowledge of 20 a person of ordinary skill in the art, correct? 21 A Correct, yes. 22 Q Okay. Same thing for your obviousness 23 opinion of the '381 patent in view of Wilt, you -- 24 you don't cite to a single reference other than Wilt 25 to support your obviousness opinion or the knowledge	352 1 hardware realization of these engines, or even a 2 combined hardware/software realization, I found 3 nothing; and so if that ALJ's construction is held, 4 which is -- which it is, then there's ground for 5 invalidity based on indefiniteness. 6 BY MR. RIZK: 7 Q The only engine that's disclosed in the 8 '381 patent that is enabled and has a sufficient 9 written description is the virtual engine, correct? 10 A Yes, the virtual engines, yes. 11 Q Okay. And show me where in the '381 patent 12 it says that those virtual engines are implemented 13 in software. 14 MR. JOHNSON: Objection; form. 15 BY MR. RIZK: 16 Q Can you show me where it says that in the 17 '381 patent, that those virtual engines are 18 implemented in software? 19 A But, I mean, that's a new discussion. 20 (Mr. Johnson and the witness speak 21 simultaneously.) 22 THE STENOGRAPHER: I'm sorry. Please ask 23 your question again. 24 BY MR. RIZK: 25 Q Show me where in the '381 patent it says

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353 1 the virtual engines are implemented in software. 2 MR. JOHNSON: Objection; form. 3 THE WITNESS: So what -- the ALJ has 4 already determined, ruled on -- on this, there's 5 hardware, software, or a combination thereof; and -- 6 and so my opinion that it's one way or the other 7 doesn't matter, right? 8 I've applied that to the -- my opinion. I 9 mean, when I formed my opinion, I applied ALJ's 10 discussion, so it's a moot discussion from my point 11 of view. If you want me to go and explain it, I 12 can; and I have it in my report. I have to go 13 through it. 14 I mean, I know we're trying to wrap this up 15 in two minutes. 16 (Mr. Rizk and the witness speak 17 simultaneously.) 18 MR. RIZK: Let's stick to answering my 19 question, then. Okay? 20 Q My question is, are you aware of any 21 disclosure -- it's a yes-or-no question. 22 Are you aware of any disclosure in the '381 23 patent, because I couldn't find any, that says a 24 virtual engine is implemented in software? 25 MR. JOHNSON: Objection; form.	355 1 I, the undersigned, a Certified Shorthand 2 Reporter of the State of California, do hereby certify: 3 That the foregoing proceedings were taken 4 before me at the time and place herein set forth; that 5 any witnesses in the foregoing proceedings, prior to 6 testifying, were duly sworn; that a record of the 7 proceedings was made by me using machine shorthand, 8 which was thereafter transcribed under my direction; 9 that the foregoing transcript is a true record of the 10 testimony given. 11 Further, that if the foregoing pertains to 12 the original transcript of a deposition in a federal 13 case, before completion of the proceedings, review of 14 the transcript [] was [] was not requested. 15 16 I further certify I am neither financially 17 interested in the action nor a relative or employee of 18 any attorney or party to this action. 19 IN WITNESS WHEREOF, I have this date 20 subscribed my name. 21 22 Dated: January 9, 2023 23 24  Rhonda Norberg 25 CSR No. 9265, CCRR No. 185
354 1 THE WITNESS: There is no such explicit 2 statement that I found; but, again, the -- the -- 3 the term "virtual engine," in view of the 4 prosecution history, in view of the specification, 5 and all of that convinces me that this is software 6 only. 7 But, again, ALJ last construed it 8 otherwise -- otherwise. 9 BY MR. RIZK: 10 Q So if the ALJ determines that a virtual 11 engine can be hardware -- okay? You've, I think, so 12 far determined that the claim invention can be 13 hardware. 14 If the ALJ determines that a virtual engine 15 can be hardware or can be software -- 16 A That's fine. I'll abide by it. 17 MR. RIZK: Okay. All right. That's all I 18 have. 19 THE VIDEOGRAPHER: Please stand by. 20 This marks the end of the deposition of 21 Dr. Massoud Pedram. We are going off the record at 22 1917 p.m. 23 (Off the record at 7:17 p.m. PST.) 24 25	356 1 DECLARATION UNDER PENALTY OF PERJURY 2 Case Name: IN RE THE MATTER OF CERTAIN GRAPHICS SYSTEMS 3 Date of Deposition: January 4, 2023 4 5 6 I, MASSOUD PEDRAM, PH.D., hereby certify 7 under penalty of perjury under the laws of the State of 8 _____ that the foregoing is true and 9 correct. 10 Executed this _____ day of 11 _____, 20____, at _____. 12 13 14 15 _____ 16 MASSOUD PEDRAM, PH.D. 17 18 19 20 21 22 23 24 25