

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-00567
Patent 10,049,080 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and
KRISTI L. R. SAWERT, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc. (collectively, “Samsung”), and Qualcomm, Inc. (“Qualcomm”) filed a Petition requesting *inter partes* review of claims 1–24 (the “challenged claims”) of U.S. Patent No. 10,049,080 B2 (Ex. 1001, the “’080 patent”). Paper 4 (“Pet.”). With our authorization, Samsung and Daedalus Prime LLC (“Patent Owner”) filed a Joint Motion to Terminate as to Samsung. Paper 10. We granted the Joint Motion to Terminate and Samsung was terminated from the proceeding. Paper 11.¹ The proceeding is now maintained between Patent Owner and Qualcomm (“Petitioner”). *See id.* Following the termination of Samsung, Patent Owner filed a Preliminary Response. Paper 12 (“Prelim. Resp.”).

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We therefore institute *inter partes* review as to all of the challenged claims of the ’080 patent and all of the asserted grounds of unpatentability.

B. Related Proceedings

The parties identify the following district court and ITC proceedings involving the ’080 patent: (1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor*

¹ The caption for this case has been revised to reflect the termination of Samsung as a party.

Corporation, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (USITC); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). Pet. 1–2; Paper 6, 1.

C. Real Parties-in-Interest

Petitioner identifies the following real parties-in-interest: Qualcomm Incorporated and Qualcomm Technologies, Inc. Pet. 1.

Without conceding that any such party is a real party-in-interest, Petitioner further identifies Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, and Visteon Corporation as parties that Patent Owner has accused of infringing the '080 Patent in *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.) and *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC), based on their incorporation of Qualcomm products. *Id.*

At this stage, neither party challenges those identifications.

D. The '080 Patent

The '080 patent is titled “Asymmetric Performance Multicore Architecture with Same Instruction Set Architecture.” Ex. 1001, (54). The

'080 patent relates to multi-core processors in computing systems and methods of managing power in multi-core processors. *Id.* at 1:16–1:20; 2:1–2:42; 3:50–4:19.

According to the '080 patent, typically, power management schemes scale up processing performance as the system's workload increases and scale down processing performance as the system's workload decreases. *Id.* at 2:22–26. Scaling process performance with workload is usually accomplished by enabling or disabling entire cores and raising or lowering core supply voltages and operating frequencies in response to workload. *Id.* at 2:30–33. For example, all cores are enabled under a maximum performance/power consumption state, and only one core is enabled under a minimum performance/power consumption state. *Id.* at 2:33–41; *see also id.* Fig. 2.

The '080 patent explains that some prior art multi-core processor power management schemes have been implemented on processors whose constituent cores are identical, while others have been implemented on processors in which the cores are radically different from each other (i.e., asymmetric). Ex. 1001, 3:34–39. For example, a processor with cores that are different from each other may have a low power core that lacks sizeable chunks of logic circuitry responsible for executing the program code instructions compared to the other cores in the processor and supports a reduced instruction set. *Id.* at 3:39–46. However, processors with cores that are different from each other can suffer from drawbacks because it is difficult for system software to adjust switch operation between processor cores having different instruction sets. *Id.* at 3:46–49.

The '080 patent purports to address this issue by disclosing multi-core processors in which at least one of the cores is designed to be lower performance and therefore consumes less power than other cores in the processor. *Id.* at 3:50–4:9. According to the '080 patent, the lower power cores have the same logic design as the higher power cores and support the same instruction set, but consume less power by having narrower drive transistor widths than the higher power cores or other power consumption-related design features. *Id.* at 3:50–62.

The '080 patent explains that the lower power core allows the multi-processor “to entertain a power management strategy that is the same/similar to already existing power management strategies, yet, still achieve an even lower power consumption in the lower/lowest performance/power states.” *Id.* at 4:20–46; *see also id.* Fig. 5. The process begins with a multi-core processor in which multiple high power cores and at least one low power core are operating. *Id.* Fig. 6 (610), 4:54–59. When the demand on the processor drops below a threshold, a high power core is disabled. *Id.* at 4:54–59. This process is repeated with the enabled high power cores each time demand reaches a lower threshold. *Id.* at 4:54–5:6. When all of the high power cores are disabled and the demand on the processor continues to drop, the low power cores are disabled one by one in the same manner until only one low power core is enabled and the lower power state is reached. *Id.* at 5:25–35.

E. Illustrative Claims

The Petition challenges claims 1–24, of which claims 1, 9, and 17 are independent. Claim 1 is illustrative of the claimed subject matter and reproduced below:²

1. A multi-core processor comprising:

[[a]i] a first plurality of cores and a second plurality of cores that support a same instruction set,

[[a]ii] wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores; and

[[b]i] power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,

[[b]ii] wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Ex. 1001, 7:56–8:3.

Independent claim 9 is directed to a method of operating a multi-core processor. *Id.* at 8:38–53. Independent claim 17 is directed to “[a] non-transitory machine readable medium containing program code” that causes the method of claim 9 to be performed. *Id.* at 9:24–41.

F. References and Other Evidence

The Petition relies on the following references:

² Paragraph labeling in brackets is based on those provided by Petitioner.

Name	Reference	Publication Date	Exhibit(s)
Sutardja '748 ³	US 2008/0288748 A1	Nov. 20, 2008	Ex. 1007
Sutardja '785	US 2007/0083785 A1	Apr. 12, 2007	Ex. 1008
Carmack	US 2009/0309243 A1	Dec. 17, 2009	Ex. 1006
Rychlik	US 2011/0145615 A1	Jun. 16, 2011	Ex. 1009
Mathieson ⁴	US 2011/0213950 A1	Sep. 1, 2011	Ex. 1005

In addition, Petitioner submits the Declaration of Trevor Mudge (Ex. 1002, “Mudge Decl.”).

G. Asserted Grounds of Unpatentability

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. § ⁵	References
1–4, 7–12, 15–20, 23, 24	103	Sutardja ⁶

³ Sutardja '748 incorporates by reference the disclosure of Sutardja '785 (Ex. 1008) in its entirety. *See* Ex. 1007, 1:8–12; Pet. 9 (chart).

⁴ Petitioner represents that Mathieson incorporates by reference the disclosure of Carmack in its entirety. Pet. 5 n.3; *see also id.* at 15–16.

⁵ Because the earliest application from which the '080 patent claims priority was filed before March 16, 2013, the pre-AIA (“America Invents Act”) version of § 103 applies. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011).

⁶ Petitioner states that it relies on Sutardja '748 and Sutardja '785, combined, “as a single reference obviousness ground.” Pet. 4 n.2. Petitioner

Claims Challenged	35 U.S.C. § ⁵	References
5, 6, 13, 14, 21, 22	103	Sutardja, Rychlik
7, 15, 23	103	Sutardja, Carmack
1–4, 7–12, 15–20, 23, 24	103	Mathieson, Sutardja
5, 6, 13, 14, 21, 22	103	Mathieson, Sutardja, Rychlik

See Pet. 4–5.

H. Overview of the Prior Art

1. Sutardja ’748 (Ex. 1007)

Sutardja ’748 is titled “Dynamic Core Switching.” Ex. 1007, (54). Sutardja ’748 relates to dynamically switching cores of multi-core processing systems of mobile computing devices. *Id.* ¶ 2. Sutardja ’748 explains that processor systems in such computing devices may be asymmetric, with the processors or cores having different instruction set architectures, or symmetric with the processors or cores having identical instruction set architectures. *Id.* ¶¶ 7–8, Figs. 1A, 1B.

Sutardja discloses obtaining increased power savings by using a multi-core processing system with a low-speed, low-power (LP) core and a high-speed, high-power (HP) core. *Id.* ¶ 212. The instruction set

refers to the combined references as “combined Sutardja” or just “Sutardja.” *See id.*; Mudge Decl. ¶¶ 71–72.

architecture (ISA) of the LP core may differ from the ISA of the HP core, or alternatively, both may use the same ISAs. *Id.* ¶ 213.

Sutardja '748 discloses using “core morphing” to optimize power consumption and improve performance. *Id.* ¶ 216. In core morphing, cores are dynamically enabled (i.e., activated) or disabled (i.e., deactivated) based on the system load. *Id.* ¶ 218. When one core is active, other cores may be disabled (i.e., deactivated) to save power. *Id.* For example, the other cores may be put in a standby mode wherein the clock frequency and/or the supply voltage of the other cores may be decreased to values that are lower than when the cores are active. *Id.* Alternatively, the other cores may be completely shut down by disconnecting the power supply to the cores. *Id.*

Sutardja '748 discloses that “[c]ore morphing may be used in multi-core systems comprising one LP core and one HP core. When applications demand still higher performance than that provided by one HP core, multiple HP cores may be used.” *Id.* ¶ 219. In the HP mode, the HP core is in the active state and processes threads. *Id.* ¶ 223. The LP core may also operate during the HP mode. In other words, the LP core may be in the active state during all or part of the HP mode. *Id.* Sutardja '748 discloses that core morphing is useful for optimizing battery life and performance of mobile devices. *Id.* ¶¶ 217, 222.

2. Sutardja '785 (Ex. 1008)

Sutardja '785 is titled “System with High Power and Low Power Processors and Thread Transfer.” Ex. 1008, (54). Sutardja '785 and Sutardja '748 are related, in that the application for Sutardja '785 (the '996 application) is the grandparent (through a continuation and continuation in

part) of the application for Sutardja '748. *Id.* (21).⁷ As previously noted, the entirety of the Sutardja '785 disclosure is incorporated by reference in Sutardja '748. *See supra*, Section I.F.

Sutardja '785 relates to low power data storage systems. Ex. 1008 ¶ 3. Sutardja '785 discloses a computing device with a system on chip (“SOC”) that includes first and second processors. *Id.* ¶ 9. The first processor implemented by the SOC has active and inactive states and processes first and second sets of threads during the active state. *Id.* The second processor implemented by the SOC also has active and inactive states. *Id.* Sutardja '785 explains that the second processor consumes less power in its active state than the first processor when it is in its active state. *Id.*

A control module implemented by the SOC communicates with the first and second processors and selectively transfers the second set of threads from the first processor to the second processor and selects the inactive state of the first processor. *Id.*

3. Rychlik (Ex. 1009)

Rychlik is titled “System and Method for Controlling Central Processing Unit Power Based on Inferred Workload Parallelism.” Ex. 1009, (54). Rychlik discloses portable computing devices with multiple cores and methods of controlling power in such devices. *Id.* ¶¶ 3–4, 26–30. Rychlik

⁷ Sutardja '748 is a publication of U.S. Patent Application No. 12/215,760, which is a continuation of U.S. Patent Application No. 12/145,660, which is a continuation-in-part of U.S. Patent Application No. 11/523,996 (“the '996 application”). Ex. 1007, (21), (63).

explains that a computing device includes an operating system with a scheduler that schedules tasks, threads, or a combination of the two for execution within the cores, a parallelism monitor that tracks the workload on the cores, and a controller that controls the power to the cores (i.e., powers them on or off). *Id.* ¶¶ 35–38. When the workload on the cores meets or exceeds a threshold value, the controller may wake up another core, and when the workload on the cores falls below a threshold value, the controller may power off or put a core into standby mode. *Id.* ¶¶ 39–40, 88, 95–96. According to Rychlik, this process may reduce power consumption. *Id.* ¶¶ 4, 95, 97.

4. Carmack (Ex. 1006)

Carmack is titled “Multi-core Integrated Circuits Having Asymmetric Performance Between Cores.” Ex. 1006, (54). Carmack discloses a multi-core integrated circuit with asymmetric cores that are each capable of implementing substantially all the functionality of the integrated circuit. *Id.* Abstract, ¶ 3. Carmack specifies that the cores may have the same hardware design, but different component device designs such that the first core may be implemented using a high threshold voltage transistor with a lower leakage current, and the second core may be implemented using a low threshold voltage transistor with a lower switching delay and lower supply voltage. *Id.* ¶ 15.

Carmack also describes methods of controlling cores based on performance parameters such as workload, operating frequency, power consumption, quality of service, or operating temperature. *Id.* Carmack explains that a core control circuit determines which one or more of the

cores to use based on the performance parameters and then utilizes a first core and idles a second core if a performance parameter is within a first range, and utilizes a second core and idles a first core if a performance parameter is within a second range. *Id.* Abstract, ¶¶ 4–5, 23. A particular core may be idled by turning off its power rail, internally gating its power rail, back biasing its substrate, or gating its clock. *Id.* ¶ 16.

5. Mathieson (Ex. 1005)

Mathieson is titled “System and Method for Power Optimization.” Ex. 1005, (54). Mathieson is a continuation-in-part of U.S. Patent Application No. 12/137,053 (“the ’053 application”) and incorporates its disclosures. *Id.* (63), ¶ 1. Carmack issued from the ’053 application. Ex. 1006, (21).

Mathieson discloses a system and method for power optimization. Ex. 1005 ¶ 3. Mathieson discloses a method for optimizing power in a multi-core processing complex that includes a first set of cores comprising one or more fast cores, a second set of cores comprising one or more slow cores, and a controller that determines which mode of operation is more power efficient and causes processing operations to be executed by the first set of cores or the second set of cores to achieve the lowest total power consumption. Ex. 1005, Abstract, ¶¶ 20, 28, 38.

Mathieson explains that a controller within the CPU switches between a first mode of operation and a second mode of operation based on workload characteristics, performance characteristics of the cores, power characteristics of the cores, and operating conditions of the processing complex. *Id.* Abstract, ¶¶ 8–10, 25, 30, Fig. 2. Mathieson discloses that

“[i]n the first mode of operation, the first set of cores is enabled and operable and the second set of cores is disabled” and “[i]n the second mode of operation, the second set of cores is enabled and operable and the first set of cores is disabled.” *Id.* ¶ 30 (reference numbers omitted).

The method begins when a processor’s controller directs one or more operations to be executed by a first set of cores. *Id.* ¶ 55, Fig. 4A. Next, the controller evaluates a processing parameter associated with processing the operations, such as a processing frequency or instruction throughput, and determines whether the parameter is above a threshold value. *Id.* ¶¶ 55–56. If the parameter exceeds the threshold, the processor continues processing operations using the first set of cores. *Id.* If the parameter is not above the threshold value, the controller directs one or more operations to be executed by a second set of cores. *Id.*

II. REQUEST FOR DENIAL OF INSTITUTION UNDER 35 U.S.C. § 325(d)

A. Background

Patent Owner argues that the Petition should be denied under 35 U.S.C. § 325(d).⁸ Prelim. Resp. 10–22. Patent Owner contends that “[e]ach of Petitioner’s cited references is materially similar to the art involved during examination.” *Id.* at 11.

⁸ “[T]he Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. § 325(d).

In evaluating arguments under § 325(d), we use a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). We must also consider the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part), which “provide useful insight into how to apply the framework” under § 325(d). *Advanced Bionics*, Paper 6 at 9. Those non-exclusive factors include:

- (a) the similarities and material differences between the asserted art and the prior art involved during examination;
- (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
- (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
- (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
- (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
- (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson, Paper 8 at 17–18. “If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office.”

Advanced Bionics, Paper 6 at 10.

For the reasons given below, we are not persuaded to exercise our discretion to deny the Petition based on § 325(d).

B. Analysis

Part I of the *Advanced Bionics* framework asks whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office. *Advanced Bionics*, Paper 6 at 8. Patent Owner contends that Sutardja ’748 was considered during prosecution of the ’080 patent. Prelim. Resp. 11. Patent Owner points to the fact that “Sutardja ’748 is identified on the face of the ’080 Patent as one of the ‘References Cited.’” *Id.* at 11–12 (citation omitted). Patent Owner also contends that Sutardja ’785 was considered because it is incorporated by reference into Sutardja ’748 and because its parent, Sutardja ’324⁹, was considered. *Id.* at 12–13. In addition, Patent Owner contends that Mathieson “is cumulative of at least the Grochowski reference [Ex. 2002] that was considered during prosecution.” *Id.* at 11. We address Mathieson and the Sutardja references individually below.

⁹ US Patent App. Pub No. 2008/0263324 A1 (Ex. 2001).

1. Mathieson

Petitioner asserts that Mathieson was not “presented to or considered by the Examiner during prosecution.” Pet. 8–9. Petitioner contends further that Mathieson is not cumulative of Grochowski, a reference that was considered by the examiner. *Id.* at 9–11. Petitioner explains that Grochowski’s disclosure of enabling high-power (A) cores and disabling low-power (B) cores in response to decreasing parallelism differs from the power saving techniques disclosed in Mathieson. *Id.* at 10–11. Petitioner asserts that, in contrast to Grochowski, Mathieson is not “based on ‘parallelism’ as Grochowski is.” *Id.* at 10. Petitioner explains that “Mathieson instead includes express teachings to consider ‘workloads’ against ‘threshold’ values to determine the claimed ‘demand.’” *Id.* at 10–11.

We agree with Petitioner that Mathieson was not before the examiner during prosecution of the ’080 patent. We also agree that there are material differences between the disclosures of Mathieson and Grochowski that prevent Mathieson from being cumulative. The prosecution history of the ’080 patent confirms this view. Responding to the examiner’s rejection of the pending claims over Grochowski, the applicant’s argument emphasized Grochowski’s failure to meet the recitation in claim 1 (application claim 20) of disabling the first plurality of cores in response to a drop in demand below a threshold:

[T]he Applicant notes that the cited portions of Grochowski do not appear to teach or suggest the Applicant’s claims. For example, the cited portions of Grochowski do not appear to teach or suggest:

...

power management hardware to, from a state where the first plurality of cores and the second plurality of cores

are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores, wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.

Ex. 1004, 56 (emphasis added by applicant).¹⁰ The examiner allowed the pending claims in the next Office action. *Id.* at 21.

Patent Owner's response to Petitioner's evidence is unavailing. Instead of attempting to demonstrate alleged similarities between the references cited and those before us, Patent Owner criticizes Petitioner's distinctions as inadequate. Prelim. Resp. 15 ("Petitioner does not explain how Mathieson allegedly works differently than Grochowski, or how Mathieson allegedly presents different considerations than Grochowski did."). We disagree and find that on this record, Petitioner's argument and evidence show there are material differences between the references such that Mathieson is not cumulative of Grochowski. Patent Owner does not persuade us that the applicant's argument before the examiner during prosecution of the '080 patent was not based on the distinction between the amount of parallelism in Grochowski and the drop in demand below a threshold in Mathieson. *See* Prelim. Resp. 14–16. That feature of the claims was emphasized in applicant's argument quoted *supra*.

Nor are we convinced by Patent Owner's assertion that "Mathieson is materially similar to Sutardja '748, which was involved in examination."

¹⁰ Unless otherwise indicated, citations to exhibits use the page numbers provided by the parties and not the original page numbers.

Prelim. Resp. 14. Patent Owner contends that “Petitioner asserts . . . that Mathieson discloses or suggests the same limitations that it asserts Sutardja ’748 discloses . . . , for similar reasons. These alleged similarities [between] Sutardja ’748 and Mathieson confirm that Mathieson is materially [sic] examination.” *Id.* at 14. In this same vein, Patent Owner cites Petitioner’s argument that “like Mathieson and the ’080 Patent, Sutardja [’748] teaches operating the multi-core processor in a high-power mode (with the high-power cores and, optionally, the low-power cores enabled) and a low-power mode (with only the low power cores enabled), based on system loading.” *Id.* We find these arguments of Patent Owner for similarity of the references based on claim limitations unavailing. Some overlap in arguments of this nature will likely always occur because the same claims are being analyzed. “Viewing the prior art through the lens of the claims would usually produce similarities in arguments.” *See CallMiner, Inc. v. NICE Ltd.*, IPR2020-00221, Paper 11 at 32 (PTAB June 17, 2020).

We have reviewed Patent Owner’s additional arguments but find them unavailing. Prelim. Resp. 14–16. In sum, we determine that on this record, Part I of the *Advanced Bionics* framework is not satisfied as to Mathieson, and therefore we do not advance to *Advanced Bionics* Part II.

2. Sutardja et al.

Petitioner asserts that “none of Sutardja ’785, Mathieson, Carmack, or Rychlik were presented to or considered by the Examiner during prosecution.” Pet. 8 (citations omitted).

We see nothing in the prosecution record indicating that Sutardja ’785 was before the examiner, or that the examiner actually considered Sutardja

'785. Nor are we willing to presume that Sutardja '785 was considered, as Patent Owner suggests, simply because it was incorporated by reference in Sutardja '748. *See* Prelim. Resp. 12–13. Patent Owner presents no authority supporting this argument. Patent Owner's cited case law does not support creating this presumption because that case law involves prior art listed on the face of the patent and is, therefore, distinguishable.¹¹

While we see merit in Petitioner's argument that the combined Sutardja references, alone and in combination with the Carmack or Rychlik references, were not before the examiner, we do not need to decide those questions for the reasons stated in connection with Mathieson, and in light of our assessment of the merits of Petitioner's challenges based on Mathieson and Sutardja, *infra*. *See SAS Inst. Inc. v Iancu*, 138 S.Ct. 1348, 1356 (2018) (rejecting PTO's practice of partial institution); 37 C.F.R § 42.108 (a) ("When instituting *inter partes* review, the Board will authorize the review to proceed on all of the challenged claims and on all grounds of unpatentability asserted for each claim.").

III. ANALYSIS OF THE CHALLENGED CLAIMS

A. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art of the '080 patent would have possessed "a bachelor's degree in electrical engineering, computer science, computer engineering, material science, physics, applied

¹¹ *See Stone Basket Innovations, LLC v. Cook Med. LLC*, 892 F.3d 1175, 1179 (Fed. Cir. 2018) ("when prior art is listed on the face of a patent, the examiner is presumed to have considered it"), cited at Prelim. Resp. 12.

physics, or a related field” and would have had “at least two years of experience in the research, design, development, or testing of electronic circuits or components or software for controlling electronic circuits or components, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 13 (citing Mudge Decl. ¶ 25).

At this stage, Patent Owner does not dispute Petitioner’s description of a person of ordinary skill in the art or provide its own description.

We regard Petitioner’s description as consistent with the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (prior art itself may reflect an appropriate level of skill). Thus, for the purpose of our decision, we adopt Petitioner’s proposal.

B. Claim Construction

We construe claim terms only as relevant to the parties’ contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Neither party proposes claim constructions for our consideration. Petitioner reports that it “does not believe that any term requires explicit construction.” Pet. 14 (citing Mudge Decl. ¶¶ 77–78). Patent Owner does not dispute Petitioner’s position or discuss claim construction. Therefore, we determine there are no claim terms that need to be construed at this stage.

C. Obviousness

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that

the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

D. Obviousness of Claims 1–4, 7–12, 15–20, 23, and 24 Based on Sutardja

Petitioner asserts that Sutardja teaches or suggests each limitation of claims 1–4, 7–12, 15–20, 23, and 24 and provides an element-by-element analysis. Pet. 19–42; Mudge Decl. ¶¶ 79–152. Patent Owner disputes these assertions. Prelim. Resp. 26–41. Patent Owner’s arguments will be discussed *infra*.

1. Independent Claim 1

a. Preamble: *A multi-core processor comprising*

Petitioner contends Sutardja ’748 teaches a multi-core processor. Pet. 19 (citing Ex. 1007 ¶ 221; Fig. 3B); Mudge Decl. ¶¶ 79–80. Dr. Mudge testifies that “Sutardja [’748] teaches a multi-core processor in the form of ‘a multi-core processing system having a LP core and a HP core.’” Mudge Decl. ¶ 80 (citing Ex. 1007 ¶ 221).

At this stage, Patent Owner does not dispute this contention. We determine that on this record, Petitioner demonstrates sufficiently that the preamble of claim 1 is taught or suggested by Sutardja.¹²

- b. Element 1[a][i]: *a first plurality of cores and a second plurality of cores that support a same instruction set,*

Petitioner contends that Sutardja meets this element. Pet. 20.

Petitioner contends that Sutardja '748 discloses a high-speed, high-power (HP) core and a low-speed, low-power (LP) core, both of which support the same instruction set. *Id.* (citing Ex. 1007 ¶ 225). Further, Petitioner contends that “Sutardja ['748] also teaches a plurality of HP cores and a plurality of LP cores.” *Id.* (citing Mudge Decl. ¶¶ 83–94; Ex. 1007 ¶¶ 219, 248).

Patent Owner contends that “Petitioner has failed to demonstrate that the Sutardja references, even in combination, disclose or suggest ‘a first plurality of cores and a second plurality of cores that support a same instruction set’ as claimed.” Prelim. Resp. 29. Patent Owner continues, “as Petitioner implicitly acknowledges, Sutardja '748 describes a system with just a *single* ‘low-speed, low-power (LP) core.’” *Id.* (citing Pet. 20).

We find that Petitioner has made a sufficient showing at this stage that this claim element is met by Sutardja '748. Dr. Mudge testifies that “[a person of ordinary skill] would have been motivated to include multiple LP cores” in Sutardja’s multi-core processor. Mudge Decl. ¶ 84. He reasons that “it was well-known to include multiple low-power cores together with

¹² We do not express an opinion on whether the preamble is limiting.

multiple high-power cores in a multi-core processor.” *Id.* Dr. Mudge backs up his opinion with citations to technical literature. *Id.* He testifies further that “Sutardja [’748] also provides explicit motivation for including multiple LP cores.” *Id.* ¶ 85. He continues, “[a]s Sutardja [’748] explains, various types of applications may be executed on Sutardja’s multi-core processor.” *Id.* (citing Ex. 1007 ¶ 226). This includes first applications “that require relatively low processing speed during operation” and second and third applications, “each with their own processing requirements.” *Id.* ¶¶ 85–86 (citing Ex. 1007 ¶¶ 226–227). He testifies that a person of ordinary skill “seeking to implement Sutardja’s teachings in a system in which a large number of applications that require relatively low processing speed during operation are expected to operate would therefore have been motivated to include multiple LP cores capable of handling the execution of such applications without needing to transfer the execution of any of the applications to the HP cores.” *Id.* ¶ 91 (internal quotation marks omitted).

Patent Owner contends that “there would be no need or motivation to add additional LP cores [in Sutardja ’748]: the system is designed to replace single-core processors with more power-efficient setups, but adding multiple LP cores would thwart that purpose.” Prelim. Resp. 30 (citing Ex. 1007 ¶ 215). At this stage, we do not find this argument persuasive. “[A]n obviousness showing ‘does not require that a particular combination must be the preferred, or the most desirable, combination described in the prior art in order to provide motivation for the current invention.’” *Intel Corp. v. Qualcomm Inc.*, No. 2020 2092, 2022 WL 880681, at *4 (Fed. Cir. Mar. 24, 2022). Petitioner needs to “show only that ‘there is something in the prior art as a whole to suggest the *desirability* . . . of making the combination,’ not

whether there is something in the prior art as a whole to suggest that the combination is the *most desirable* combination available.” *Id.*; *see also Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (“[It is] not necessary to show that a combination is ‘the *best* option, only that it be a *suitable* option.’”).

Alternatively, Petitioner relies on the teachings of Sutardja ’785 for this claim element. Pet. 22–23. Patent Owner challenges this argument, contending that Sutardja ’785 does not disclose multiple cores, only multiple processors. Prelim. Resp. 31–32. Because we do not rely on Sutardja ’785 to meet this aspect of the claim for purposes of institution, we do not address that issue at this time.

- c. Element 1[a][ii]: *wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores*

Petitioner relies on Sutardja ’748 to meet this claim element. Pet. 23–24. Petitioner explains that “[t]he second cores (Sutardja’s LP cores) consume less power, for a same applied operating frequency and supply voltage, than the first cores (Sutardja’s HP cores).” *Id.* at 24; Mudge Decl. ¶ 96.

Patent Owner challenges Petitioner’s analysis of this claim element. Prelim. Resp. 32–34. Patent Owner asserts that “[a]lthough Sutardja ’748 discloses that its HP and LP cores have different properties and capabilities . . . it does not disclose or suggest that the LP core consumes less power than the HP core for a same applied operating frequency and supply voltage as required.” *Id.* at 32 (internal quotation marks and emphasis omitted). Patent Owner continues, “Sutardja ’748 explains just the

opposite—the LP core consumes less power because it operates at a lower frequency (Hz).” *Id.* (emphasis omitted). At this stage, we do not agree with this assertion. Dr. Mudge testifies that “the power consumption of a core with narrow transistors will be less than a core with wider transistors.” Mudge Decl. ¶ 96. He concludes that “[a person of ordinary skill] would recognize that Sutardja [’748]’s LP core will consume less power than its HP cores for the same reason.” *Id.* (citing Ex. 1007 ¶ 230). His testimony is supported by Sutardja ’748, which discloses that “[t]he transistors 106 of the HP core 24 tend to consume more power during operation in the active state than the transistors 110 of the LP core 28 Gates of the transistors 106 may be larger than gates of the transistors 110.” Ex. 1007 ¶ 230 (quoted in Mudge Decl. ¶ 96).

At this stage we find Dr. Mudge’s testimony to be credible in light of Sutardja ’748. Patent Owner’s argument, on the other hand, is unsupported at this stage by expert testimony. We, therefore, find that, on this record, Petitioner demonstrates sufficiently that Sutardja ’748 meets this limitation.

- d. Element 1[b][i]: *power management hardware to, from a state where the first plurality of cores and the second plurality of cores are enabled, disable all of the first plurality of cores for a drop in demand below a threshold without disabling any of the second plurality of cores,*

Petitioner relies on Sutardja ’748 to meet this element. Pet. 24–30; Mudge Decl. ¶¶ 97–111. Patent Owner responds that “Sutardja ’748 does not disclose or suggest the claimed ‘power management hardware.’” Prelim. Resp. 34. On this record, we disagree with Patent Owner. Petitioner identifies the “hypervisor” in Sutardja ’748 as meeting this element. Pet. 29–30. Petitioner explains that “[a person of ordinary skill] would have

understood that the hardware on which the disclosed hypervisor is installed corresponds to the claimed power management hardware.” *Id.* at 30 (citing Mudge Decl. ¶ 111).

Patent Owner contends also that Sutardja ’748 does not disclose, “from a state where the first plurality of cores and the second plurality of cores are enabled, disabling all of the first plurality of cores for a drop in demand below a threshold,” as claimed. Prelim. Resp. 35 (emphasis omitted). We disagree. We find also that Petitioner demonstrates sufficiently that the first and second plurality of cores are enabled and the first plurality of cores is disabled (but not the second plurality) when there is a drop in demand. Pet. 24–29. Petitioner contends that Sutardja ’748 discloses this claim element. Pet. 24–30. Referring to Figure 4 of Sutardja ’748, Petitioner explains that “[a person of ordinary skill] would have . . . understood that the transition from the HP mode (with both the HP and LP cores enabled) to the LP mode (with only the LP cores enabled) would occur without disabling any of the LP cores (the claimed second plurality of cores).” Pet. 28–29. Dr. Mudge provides supporting testimony. Mudge Decl. ¶¶ 98–99. At this stage, we find this explanation supported by expert testimony to be sufficient. On this record, we find that Petitioner has sufficiently shown that Sutardja ’748 meets this element.

- e. Element 1[b][ii]: *wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand.*

Petitioner asserts that Sutardja ’748 meets this element. Pet. 31–32; Mudge Decl. ¶¶ 113–117. Referring to Figure 5 of Sutardja ’748, Petitioner identifies Kernel Module 220 and PMS Module 242 as the claimed operating

system software. *Id.* at 31. Petitioner contends that “Sutardja ’[748] further discloses that the operating system (kernel module and PMS module) controls the power management hardware (core switching module) based on the demand.” *Id.* at 32 (citing Ex. 1007 ¶ 253).

Patent Owner responds that “[c]ontrary to Petitioner’s assertion, neither the power management system nor its core profile module are part of the operating system of Sutardja ’748.” Prelim. Resp. 39. Patent Owner continues, “merely being ‘executed by’ the operating system does not make an application or module part of the operating system.” *Id.* (emphasis omitted)

We do not agree with this argument. Patent Owner mischaracterizes Petitioner’s argument. Petitioner contends that the PMS module and the kernel module together form part of an operating system that functions to control the functioning of the multi-core processor. Pet. 32 (citing Mudge Decl. ¶ 116). Dr. Mudge testifies that “Sutardja [’748] discloses an operating system that *includes* kernel module and PMS module 242.” Mudge Decl. ¶ 116 (emphasis added).

At this stage, we find this explanation supported by expert testimony to be sufficient. On this record, we find that Petitioner has sufficiently shown that Sutardja ’748 meets this element.

f. Summary

We find, on this record, that Petitioner demonstrates a reasonable likelihood of prevailing on this challenge,

2. Independent Claims 9 and 17

Petitioner's analysis of these claims incorporates its analysis of claim 1. Pet. 40–41. Patent Owner does not address these claims separately, referring back to its arguments for claim 1. Prelim. Resp. 40–41. For the reasons given for claim 1, we find on this record that Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

3. Dependent Claims 2–4, 7, 8, 10–12, 15, 16, 18–20, 23, and 24

Petitioner provides an analysis for each of these dependent claims in relation to Sutardja. Pet. 33–39 (claims 2–4, 7, 8), 41–42 (claims 10–12, 15, 16, 18–20, 23, 24). Patent Owner does not address these claims separately.

For the reasons given above, and in the Petition, we find on this record that Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

E. Obviousness of Claims 5, 6, 13, 14, 21, and 22 Based on Sutardja '748 and Rychlik

Petitioner provides an analysis for each of these dependent claims in relation to Sutardja '748 and Rychlik. Pet. 43–48. Petitioner asserts that Sutardja '748 and Rychlik teach each limitation of claims 5, 6, 13, 14, 21, and 22. *Id.*, Mudge Decl. ¶¶ 153–169.

Petitioner provides a motivation for combining the teachings of Sutardja '748 and Rychlik. *See* Pet. 45 (“A [person of ordinary skill] would have been motivated to apply Rychlik’s teachings to Sutardja’s LP cores, to disable an additional core of Sutardja’s LP cores (the claimed second plurality of cores), for each continued drop in workload (the claimed demand) below a next lower threshold, until only one LP core remained

enabled.”). Dr. Mudge testifies that “[a person of ordinary skill] seeking to implement Sutardja’s teachings in a system with multiple of Sudardja’s LP cores, would understand that . . . disabling one or more of those LP cores when demand is low, would save power.” Mudge Decl. ¶ 161.

At this stage, Patent Owner does not address these challenges separately. For the reasons given above and in the Petition, we find on this record that Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

F. Obviousness of Claims 7, 15, and 23 Based on Sutardja ’748 and Carmack

Petitioner provides an analysis for each of these dependent claims in relation to Sutardja ’748 and Carmack. Pet. 48–49. Petitioner asserts that Sutardja ’748 and Carmack teach each limitation of claims 7, 15, and 23. *Id.*; Mudge Decl. ¶¶ 170–73. Petitioner provides a motivation for combining the teachings of Sutardja ’748 and Carmack. *See* Pet. 49 (“A [person of ordinary skill] would have been motivated to set the high value to the maximum frequency of Sutardja’s HP cores, as taught by Carmack, to maintain desired performance levels during periods of high demand.”) (citing Mudge Decl. ¶ 173).

At this stage, Patent Owner does not address Petitioner’s arguments separately. For the reasons given above and in the Petition, we find on this record that Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

G. Obviousness of Claims 1–4, 7–12, 15–20, 23, and 24 Based on Mathieson and Sutardja '748

Petitioner asserts that Mathieson and Sutardja '748 teach each limitation of claims 1–4, 7–12, 15–20, 23, and 24 and provides an element-by-element analysis for each. Pet. 51–80; Mudge Decl. ¶¶ 174–255. Petitioner contends that a person of ordinary skill would have been motivated to combine Mathieson with Sutardja '748 with a reasonable expectation of success. Pet. 50. Among other reasons, “each relates to the same well-known subject matter of power management in multi-core processors, both teaching techniques for reducing power consumption in response to decreased demand/workload.” *Id.* (citing Mudge Decl. ¶ 175).

1. Motivation to Combine Mathieson and Sutardja '748

Patent Owner contends that Petitioner’s argument for a motivation to combine these references is not sufficient and “relies on hindsight.” Prelim. Resp. 41–43. For example, Patent Owner contends that “as to power management of processor cores, Mathieson and Sutardja '748 actually teach divergent methods.” *Id.* at 42. Patent Owner continues, “Sutardja '748 is explicitly carried out via software, whereas a dedicated hardware structure is used in Mathieson.” *Id.* We disagree. As discussed *supra*, in Section III.D.1.d., Sutardja '748 discloses “power management hardware” consisting of a hypervisor installed on underlying hardware. *See also* Pet. 30. Dr. Mudge testifies that in addition to the reasons discussed *supra*, “both references contemplate that the differences in power consumption

between the cores may be achieved through differences in the constituent transistors.” Mudge Decl. ¶ 175. Patent Owner disputes this, but does not provide any evidence to support this argument. Prelim. Resp. 41.

We find that, on this record, Petitioner has demonstrated sufficiently a motivation to combine Mathieson and Sutardja ’748. In the analysis that follows we do not rely on ’Sutardja ’785, and therefore we do not address the motivation to combine Mathieson with that reference at this time.

2. Independent Claim 1

Petitioner contends that Mathieson and Sutardja, together, meet the limitations of claim 1 and provides an element-by-element analysis. Pet. 51–64. Petitioner provides supporting testimony from Dr. Mudge. Mudge Decl. ¶¶ 178–211. For example, Petitioner identifies Mathieson and Sutardja ’748 as disclosing the claimed “first plurality of cores and a second plurality of cores that support a same instruction set” in element 1[a][i]. Pet. 52–53. Petitioner identifies Mathieson as teaching claim element 1[a][ii] (“wherein the second plurality of cores consume less power, for a same applied operating frequency and supply voltage, than the first plurality of cores”). *Id.* at 55–56. And Petitioner relies on Mathieson to meet the “power management hardware” limitation of element 1[b][i]. *Id.* at 56–60.

Patent Owner contends that the Petition fails to show that a person of ordinary skill in the art would have been motivated to combine Mathieson and Sutardja ’748, and that Mathieson and Sutardja ’748 fail to teach claim limitations 1[a][i], 1[b][i], and 1[b][ii]. Prelim. Resp. 41–53.

a. Element 1[a][i]

We have addressed the motivation to combine issue *supra*, in Section III.G.1. Patent Owner contends that “Petitioner does not assert that Mathieson discloses the first and second pluralities of cores supporting the same instruction set.” Prelim. Resp. 43. This argument is unavailing. As Patent Owner recognizes, Sutardja ’748 discloses that both the HP and IP cores “may use the same ISAs [Instruction Set Architecture].” *Id.* at 46 (citing Ex. 1007 ¶ 213); *see also* Pet. 54 (“Sutardja [’748] . . . provides express teachings to use the ‘same instruction set’ for different cores.”).

b. Element 1[b][i]

Patent Owner contends that “Petitioner has failed to demonstrate that Mathieson, alone or in combination with the Sutardja References, discloses or suggests ‘a state where the first plurality of cores and the second plurality of cores are enabled’ to perform operations as claimed.” Prelim. Resp. 47. We disagree. Patent Owner acknowledges that the CPU in Mathieson operates in both the first mode and second mode during a transition period. Prelim. Resp. 47. Dr. Mudge provides expert testimony on this issue which is uncontradicted by any evidence from Patent Owner. Mudge Decl. ¶¶ 194–2000. Dr. Mudge testifies that “Mathieson teaches a state where the first plurality of cores (Mathieson’s first set of cores 210) and the second plurality of cores (Mathieson’s second set of cores 220) are both enabled.” Mudge Decl. ¶ 195 (citing Ex. 1005 Fig. 4A). Still referring to Figure 4A, he testifies that “Mathieson teaches disabling all of the first plurality of cores (Mathieson’s first set of cores 210) for a drop in demand (Mathieson’s workload) below a threshold without disabling any of the second plurality of

cores (Mathieson’s second set of cores 220).” *Id.* ¶ 198. He testifies that “[a person of ordinary skill] would have understood that the second set of cores 220 would remain enabled throughout the switch from the first mode of operation (in which both the first set of cores 210 and the second set of cores 220 are enabled) to the second mode of operation (in which only the second set of cores 220 are enabled).” *Id.* ¶ 200. As noted, Patent Owner provides no testimony or other evidence in rebuttal.

c. Element 1[b][ii]

Patent Owner contends that “Petitioner has failed to demonstrate that Mathieson, alone or in combination with the Sutardja References, discloses or suggests ‘wherein an operating system to execute on the multi-core processor is to monitor a demand for the multi-core processor and control the power management hardware based on the demand’ as claimed.”

Prelim. Resp. 52–53. Patent Owner contends that controller 240 in Mathieson is not part of an operating system executing on CPU 102, but is “hardware within the CPU.” *Id.* at 52. We do not agree with this argument. As Patent Owner recognizes, Mathieson discloses that the controller can be “implemented in software and is executed by the CPU 102.” *Id.* at 53 (quoting Ex. 1005 ¶ 43). We find that, at this stage, this sufficiently meets the claim element calling for an operating system executing on hardware.

d. Summary and Conclusion

For the reasons given in the Petition and those summarized *supra*, on this record we determine that Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge.

3. Independent Claims 9 and 17

Petitioner's analysis of these claims refers back to its analysis of claim 1. Pet. 77–78. Patent Owner does not address these claims separately. For the reasons given for claim 1, we find on this record that Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

4. Dependent Claims 2–4, 7, 8, 10–12, 15, 16, 18–20, 23 and 24

Petitioner provides an analysis for each of these dependent claims in relation to Mathieson and Sutardja. Pet. 64–77 (claims 2–4, 7, 8), 78–80 (claims 10–12, 15, 16, 18–20, 23, 24). Patent Owner does not address these claims separately.

For the reasons given in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

2. Obviousness of Claims 5, 6, 13, 14, 21, and 22 Based on Mathieson, Sutardja '748, and Rychlik

Petitioner asserts that Mathieson, Sutardja '748, and Rychlik teach each limitation of claims 5, 6, 13, 14, 21, and 22. Pet. 80–82; Mudge Decl. ¶¶ 256–263. Petitioner provides a motivation for combining the teachings of Mathieson, Sutardja '748 and Rychlik. *Id.* at 80–81; Mudge Decl. ¶¶ 257–260.

At this stage, Patent Owner does not address these challenges separately. For the reasons given in the Petition, we find that on this record Petitioner demonstrates a reasonable likelihood of prevailing on these challenges.

IV. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

V. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '080 patent is hereby instituted for all of the challenged claims on all of the asserted grounds; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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Patent 10,049,080 B2

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