

**UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

ELEMENT CAPITAL COMMERCIAL
COMPANY PTE. LTD,

Plaintiff,

v.

BOE TECHNOLOGY GROUP CO.,
LTD; BEIJING BOE DISPLAY
TECHNOLOGY CO., LTD; AND
MOTOROLA (WUHAN) MOBILITY
TECHNOLOGIES COMMUNICATION
CO., LTD..

Defendant.

Civil Action No.

JURY TRIAL DEMANDED

COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Element Capital Commercial Company PTE. LTD (“Element Capital” or “Plaintiff”) files this Complaint against Defendants BOE Technology Group Co., Ltd, Beijing BOE Display Technology Co., Ltd, and Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. (collectively “Defendants”), based on its own knowledge as to itself and its own actions, and based on information and belief as to all other matters, alleging as follows:

INTRODUCTION

This matter involves Element Capital’s active-matrix display product patents (U.S. Patent No. 7,259,736 B2, U.S. Patent No. 8,164,267 B2, and U.S. Patent No. 8,525,760) infringed by Defendants’ display products (“Defendants’ products” or

“Accused Products”). Active-matrix display products are now included in nearly every mobile phone and device. Technology underlying the manufacture and use of active-matrix display products is, in short, extremely valuable.

I.

THE PARTIES

1. Plaintiff Element Capital Commercial Company PTE. LTD (“Element Capital”) is a Singaporean company located at 60 Paya Lebar Road #11-04, Paya Lebar Square, Singapore 409051.

2. On information and belief, Defendant BOE Technology Group Co., Ltd is a Chinese company located at 181 No.12 Xihuanzhong Rd, BDA, Beijing, 100176, China.

3. On information and belief, Defendant Beijing BOE Display Technology Co., Ltd is a Chinese company located at 118 Jinghai 1 Road Economic Tech Development Zone Beijing, 100176, China. BOE is a subsidiary of BOE Technology Group Co. Ltd., produces certain Accused Products abroad, including in China, that are then sold for importation into the United States, imported into the United States, and/or sold within the United States after importation.

4. On information and belief, Defendant Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. is a Chinese company located at No.19, Gaoxin 4th Road, Wuhan East Lake High-tech Zone, Wuhan, Wuhan Hubei 430000, China.

II.

NATURE OF THE ACTION

5. This is an action for patent infringement.

6. Element Capital is informed and believes and alleges that Defendants have been and are currently infringing and/or contributing to and/or actively inducing others to infringe claims of U.S. Patent No. 7,259,736 B2, U.S. Patent No. 8,164,267 B2, and U.S. Patent No. 8,525,760 B2 (“the ‘736 Patent,” “the ‘267 Patent,” and “the ‘760 Patent” or collectively “the Asserted Patents”).

III.

JURISDICTION AND VENUE

7. This action arises under the patent laws of the United States, Title 35 of the United States Code, 35 U.S.C. § 1 *et seq.*

8. This Court has subject matter jurisdiction over this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. On information and belief, BOE Technology Group Co., Ltd is subject to this Court’s specific and general personal jurisdiction pursuant to due process, the federal long arm statute, and/or the Texas Long Arm Statute, due at least to its substantial business in this State and judicial district, including at least part of its infringing activities alleged herein, and regularly doing or soliciting business, engaging in other persistent conduct, and/or deriving substantial revenue from goods sold and services provided to Texas residents.

10. For example, BOE Technology Group Co., Ltd's "subsidiaries are located in 19 countries and regions, including USA, Germany, UK, France, Switzerland, Japan, Korea, Singapore, India, Russia, Brazil, UAE, etc. The service system covers major regions in Europe, USA, Asia, and Africa worldwide." *See* BOE Technology Group Co., Ltd website (<https://www.boe.com/en/about/index>). BOE Technology Group Co., Ltd asserts that its ultra-high definition, flexible and micro-display solutions have been widely used in famous brands at home and abroad, and global market research agency Omdia data shows that in 2020, BOE Technology Group Co., Ltd in smart phones, tablet PCs, notebook computers, monitors, TV and other five major applications of display shipments are ranked first in the world. *Id.*

11. This Court has personal jurisdiction over BOE Technology Group Co., Ltd, directly or through intermediaries, including its subsidiaries and intermediaries within the United States, because it has established minimum contact within the United States and Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice. BOE Technology Group Co. Ltd. has placed and continues to place infringing display products into the stream of commerce via an established distribution channel with the knowledge and/or intent that those products were sold and continue to be sold in the United States and Texas, including in this District.

12. This Court has personal jurisdiction over Beijing BOE Display Technology Co., Ltd in this action because it has established minimum contact within the United States and Texas such that the exercise of jurisdiction would not offend traditional

notions of fair play and substantial justice. BOE Display Technology Co., Ltd has purposefully directed activities at the United States and Texas, in particular, directing display products for sale to customers and distributors within Texas, including within this District.

13. This Court has personal jurisdiction over Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. in this action because it has established minimum contact within the United States and Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice. Motorola (Wuhan) Mobility Technologies Communication Co., Ltd. has placed and continues to place infringing display products, including Motorola RAZR, into the stream of commerce via an established distribution channel with the knowledge and/or intent that those products were sold and continue to be sold in the United States and Texas, including in this District.

14. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b), 1391(c), 1391(d) and/or 1400(b) because a substantial part of the events giving rise to Element Capital's claims occurred in the Eastern District of Texas and because Defendants are subject to personal jurisdiction in the Eastern District of Texas.

IV.

FACTUAL BACKGROUND

15. The Asserted Patents relate to electronic devices including an active-matrix substrate which reduces directional viewing variation between the column and row directions.

16. On August 21, 2007, U.S. Patent No. 7,259,736, titled “Electro-Optical Device, Active-Matrix Substrate, and Electronic Apparatus,” was duly and legally issued by the United States Patent and Trademark Office to Hayato Nakanishi. A true copy of the ‘736 Patent is attached as **Exhibit 1**.

17. Element Capital is the owner of the ‘736 Patent with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the ‘736 Patent against infringers, and to collect damages for infringement during all relevant times.

18. On April 24, 2012, U.S. Patent No. 8,164,267, titled “Electro-Optical Device, Active-Matrix Substrate, and Electronic Apparatus,” was duly and legally issued by the United States Patent and Trademark Office to Yojiro Matsueda et al. A true copy of the ‘267 Patent is attached as **Exhibit 2**.

19. Element Capital is the owner of the ‘267 Patent with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the ‘267 Patent against infringers, and to collect damages for infringement during all relevant times.

20. On September 3, 2013, U.S. Patent No. 8,525,760, titled “Active-Matrix Substrate, Electro-Optical Device, and Electronic Device,” was duly and legally issued by the United States Patent and Trademark Office to Yojiro Matsueda. A true copy of the ‘760 Patent is attached as **Exhibit 3**.

21. Element Capital is the owner of the '760 Patent with all substantive rights in and to that patent, including the sole and exclusive right to prosecute this action and enforce the '760 Patent against infringers, and to collect damages for infringement during all relevant times.

22. The '736 Patent, the '267 Patent, and the '760 Patent are directed to electro-optical devices that include an active-matrix substrate to be implemented in a display. The active-matrix substrate includes multiple pixels arranged in a matrix form including electro-optical devices driven by receiving electric power from an electric power supply circuit. Based on the configuration of the active-matrix substrate, the electro-optical device has a reduced directional viewing variation between column and row directions.

23. Element Capital manufactures or licenses other companies to manufacture the electronic apparatus claimed in the Asserted Patents. This electronic apparatus is sold to various electronic manufacturers who obtain the right to use the patented inventions in their electronic apparatuses by purchasing from Element Capital or from an authorized manufacturer. Companies who do not obtain a license from Element Capital do not have permission to manufacture or sell the patented electronic apparatus.

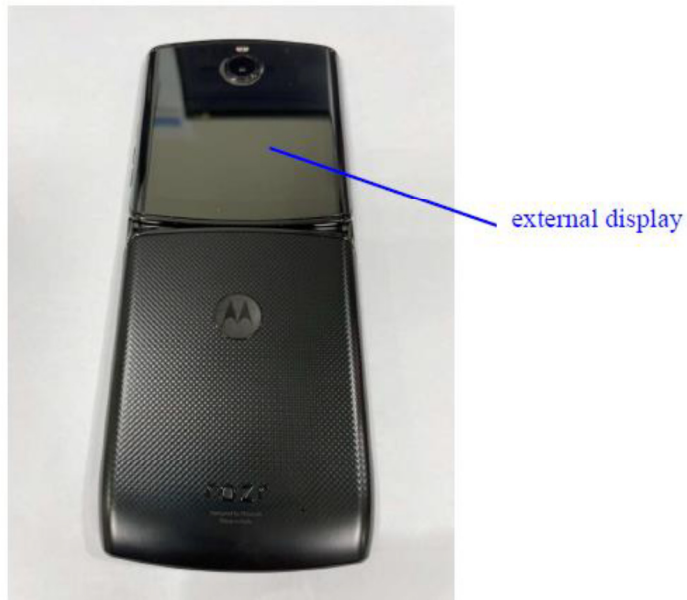
24. Element Capital is informed and believes and alleges that Defendants have made, used, provided, supplied, distributed, sold, and/or offered for sale in the United States and in this district, electronic apparatuses that infringe the Asserted Patents, without authorization from Element Capital and continues to do so now.

25. Defendants have manufactured and sold Defendants' electronic apparatuses that infringe the Asserted Patents and which include at least Motorola RAZR mobile phones.

26. As shown in more detail below, Defendants electronic apparatuses include each and every limitation of at least claims 3-5, 7, 9, and 13-17 of the '736 Patent, claim 1 of the 267 Patent, and claim 1 of the '760 Patent, and therefore literally infringe these claims. Element Capital reserves the right to assert infringement under the doctrine of equivalents in light of information learned during discovery or in view of this Court's claim construction order.

27. An image of Defendants electronic apparatus found in the Motorola RAZR is shown below. Motorola RAZR features a 2.7 inch external OLED panel made by BOE, which is an electro-optical device.

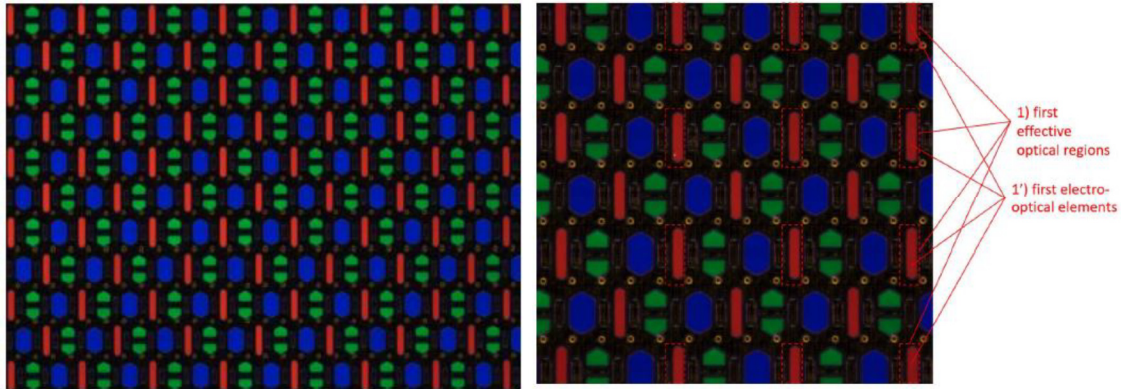




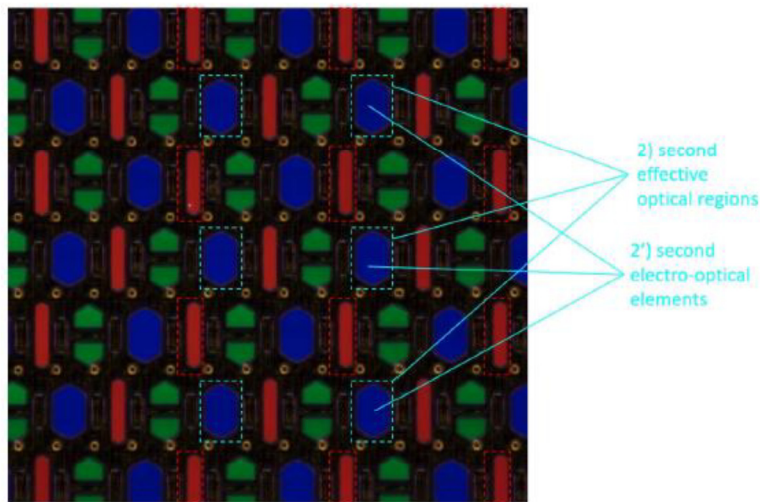
28. As shown below, the external OLED panel of Motorola RAZR has a substrate.



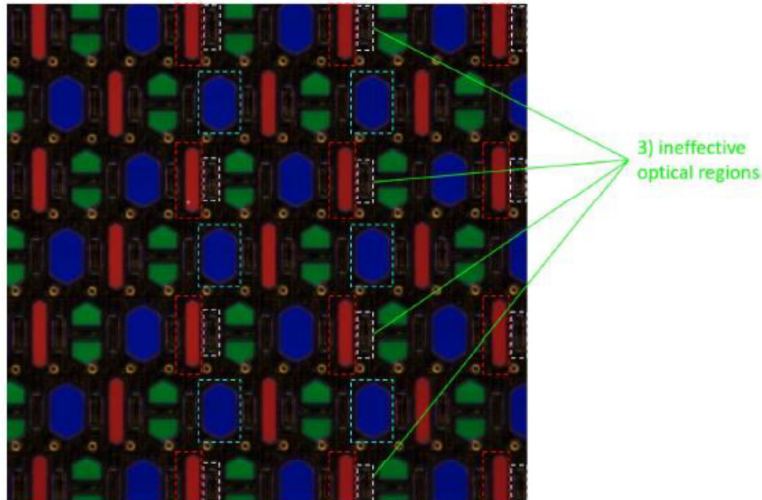
29. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 300 times and 500 times magnifications, the external OLED panel has a plurality of 1) first effective optical regions provided above the substrate, and 1') first electro-optical elements are provided in 1) the first effective optical region.



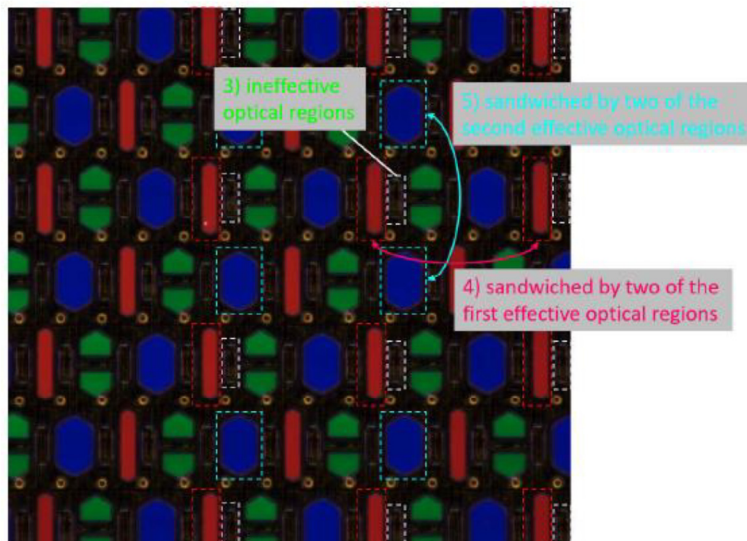
30. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification, the external OLED panel has a plurality of 2) second effective optical regions provided above the substrate, and 2') second electro-optical elements are provided in the 2) second effective optical regions.



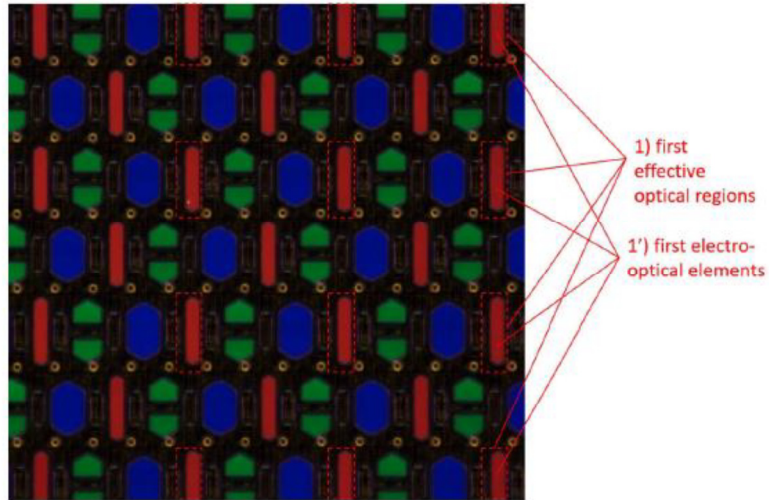
31. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification, the external OLED panel has a plurality of 3) ineffective optical regions provided above the substrate, and no electro-optical elements are provided in the ineffective optical regions.



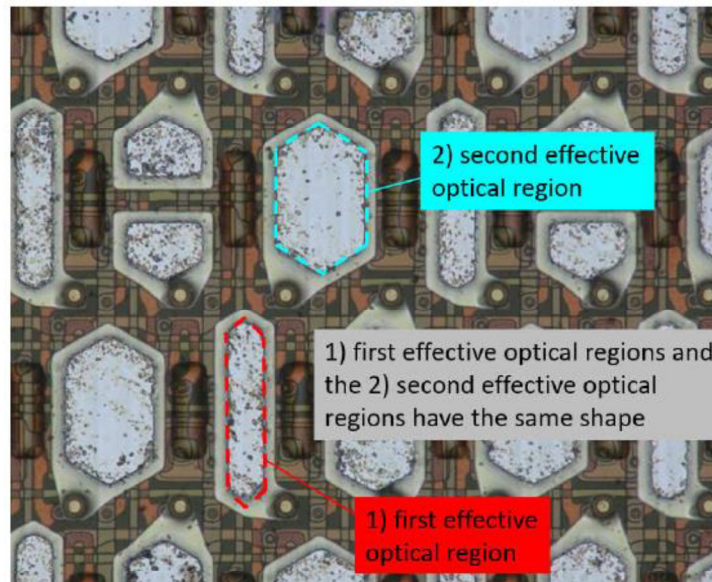
32. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification, the external OLED panel of Motorola RAZR, each of the whole 3) ineffective optical regions is arranged so as to be 4) sandwiched by two of the first effective optical regions and so as to be 5) sandwiched by two of the second effective optical regions.



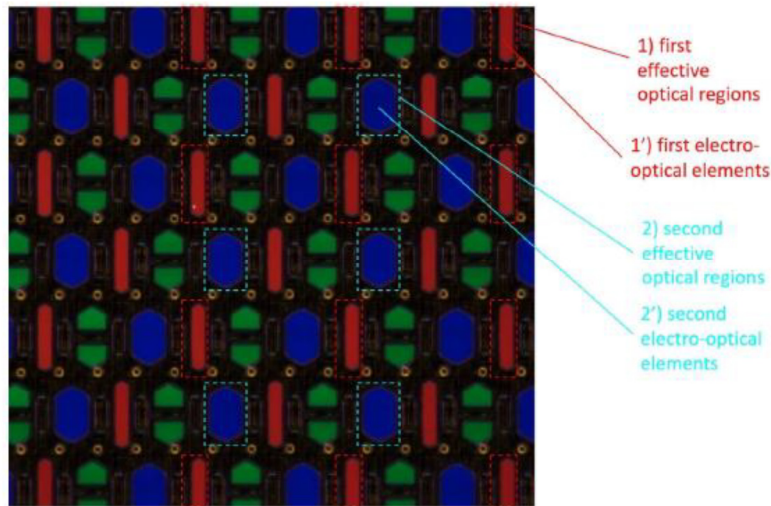
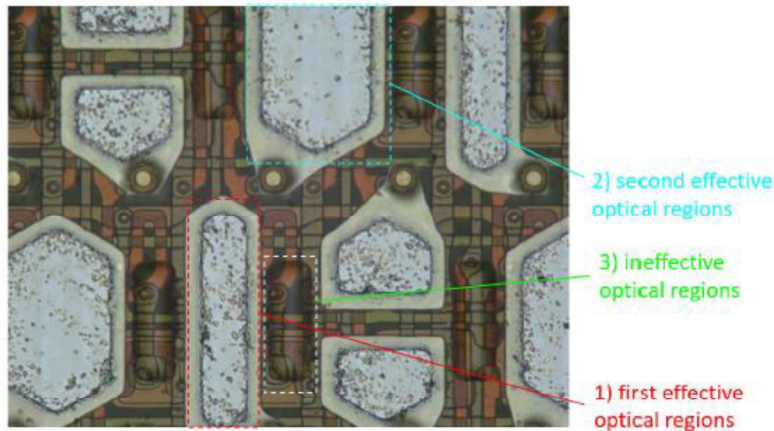
33. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification, the external OLED panel of Motorola RAZR, the 1) first effective optical regions are not adjacent to each other.

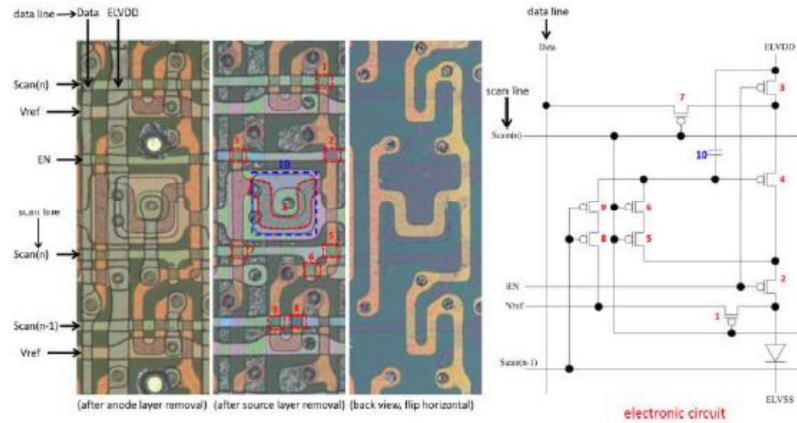


34. As shown below, in the pixels of the external display of the Motorola RAZR displayed the external OLED panel of Motorola RAZR, the 1) first effective optical regions and the 2) second effective optical regions have the same shape.

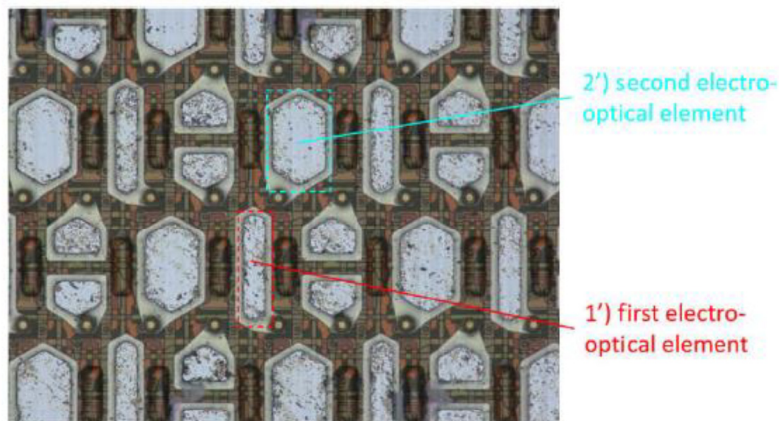


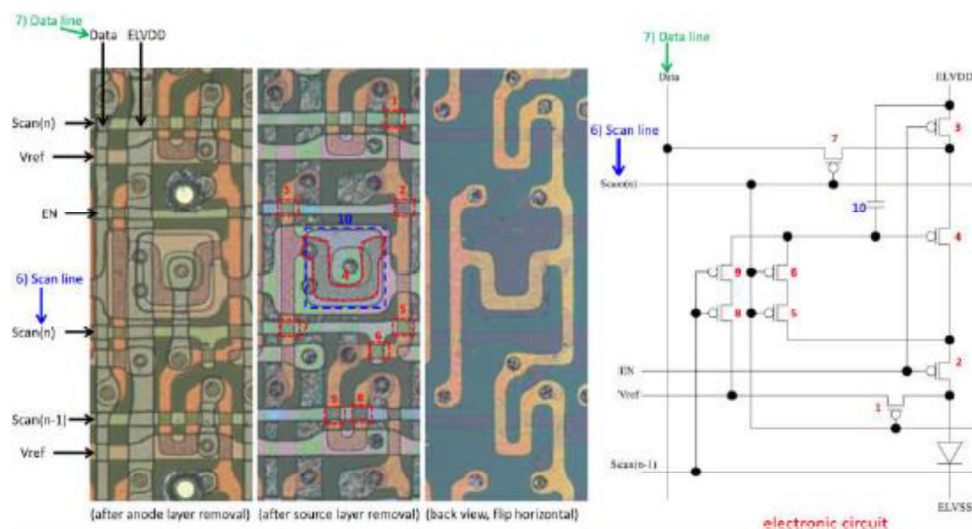
35. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification and the external OLED panel of Motorola RAZR being illuminated, the 1) first and 2) second effective optical regions do have respective electronic circuits to drive the electro-optical elements 1') and 2') provided in the 1) first and 2) second effective optical regions.



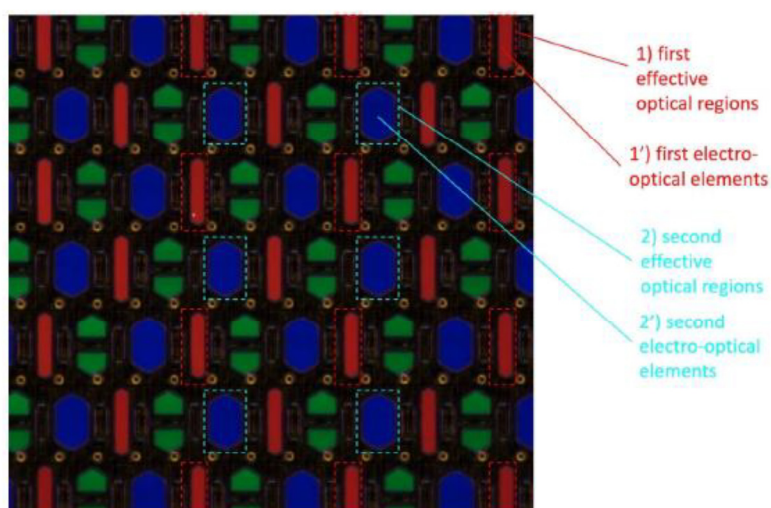


36. As shown below, in a pixel circuit of the external display of the Motorola RAZR, the external OLED panel of Motorola RAZR, there are pixels provided so as to correspond to respective intersections of a plurality of 6) scan lines and a plurality of 7) data lines, the electronic circuits drive the electro-optical elements 1') and 2') in accordance with scan signals from the 6) scan lines and data signals from the 7) data lines.

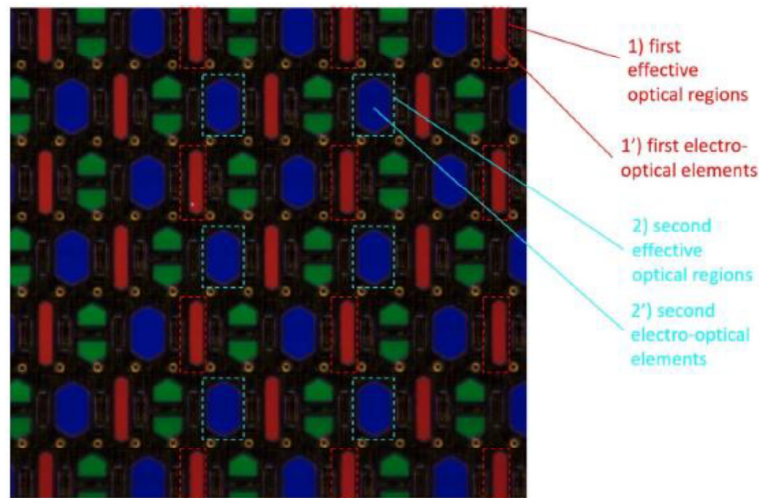
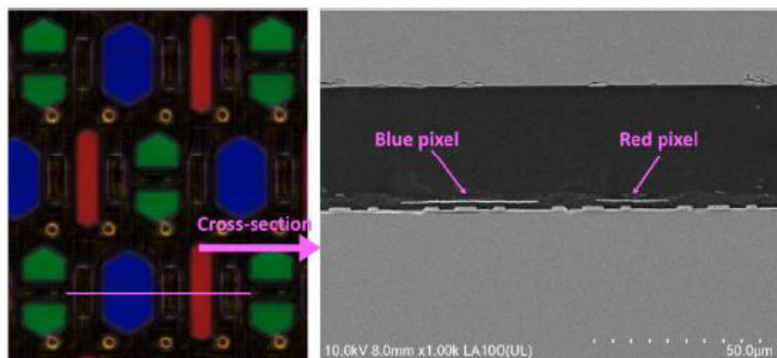


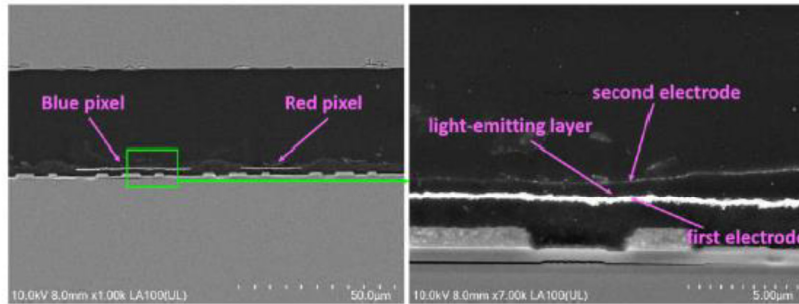


37. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification and the external OLED panel of Motorola RAZR being illuminated, the 1') first electro-optical element (red) and 2') the second electro-optical element (blue) include two electro-optical elements selected from an electro-optical element that emits green, an electro-optical element that emits blue, and an electro-optical element that emits red.

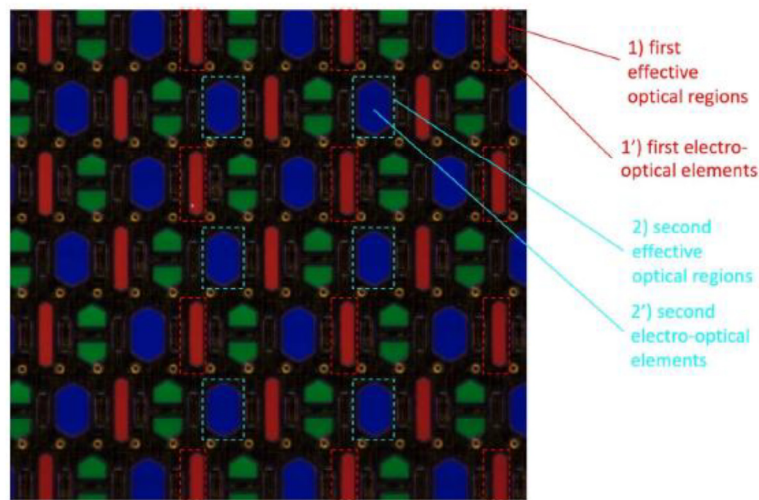


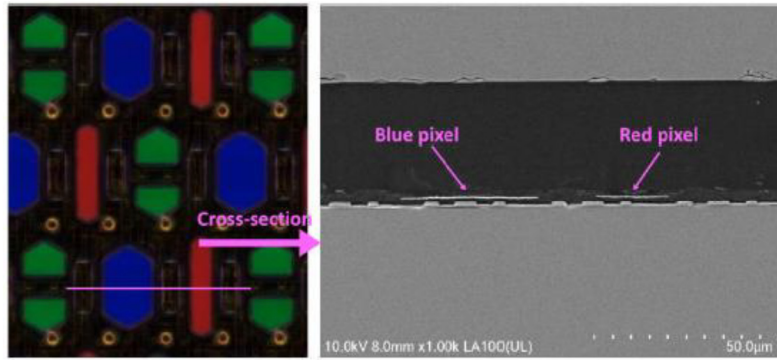
38. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification and the external OLED panel of Motorola RAZR being illuminated, each of the 1') first electro-optical elements and the 2') second electro-optical elements is an electroluminescent element. The external OLED panel has a first electrode, a second electrode, and a light emission layer that is disposed between the first electrode and the second electrode.



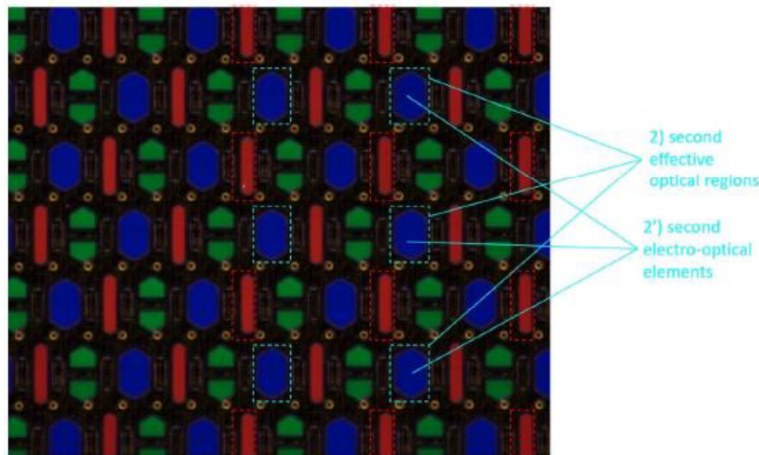


39. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification and the external OLED panel of Motorola RAZR being illuminated, the 1') first electro-optical element has a light-emitting layer that includes organic material so as to emit red light, and the 2') second electro-optical element has a light-emitting layer that includes organic material so as to emit blue light.

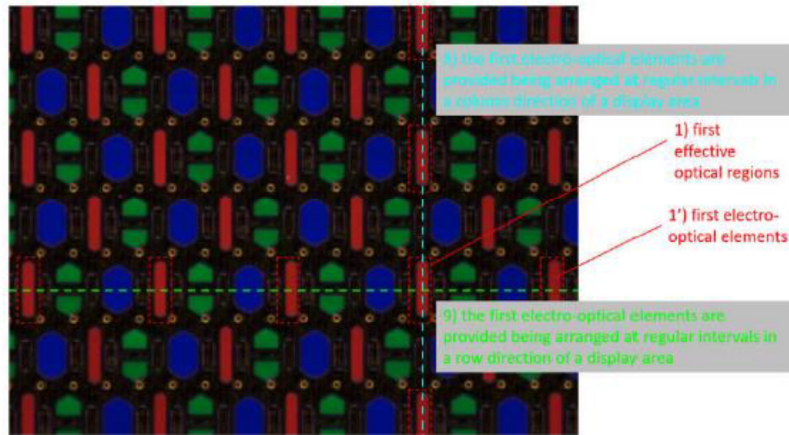




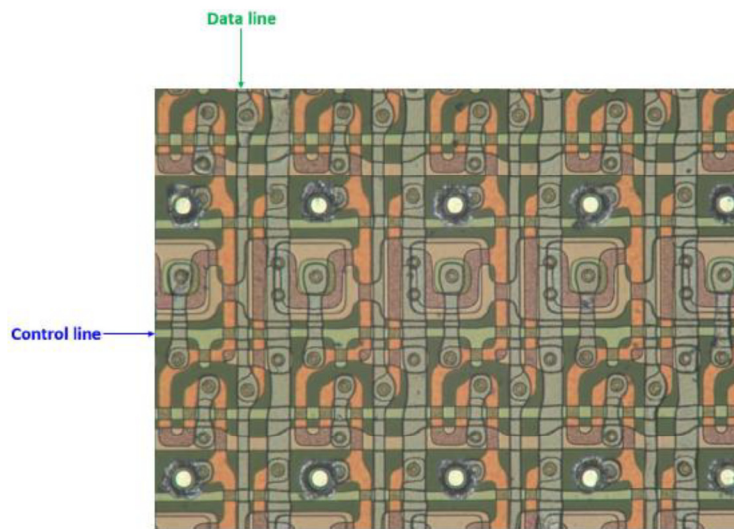
40. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification, in the external OLED panel of Motorola RAZR, 2) the second effective optical regions are not arranged so as to be adjacent to each other.



41. As shown below, in the pixels of the external display of the Motorola RAZR displayed at 500 times magnification, in the external OLED panel of Motorola RAZR, each of the 1) first effective optical regions in which the 1') first electro-optical elements are provided being arranged at regular intervals in a 8) column and 9) row directions of a display area.

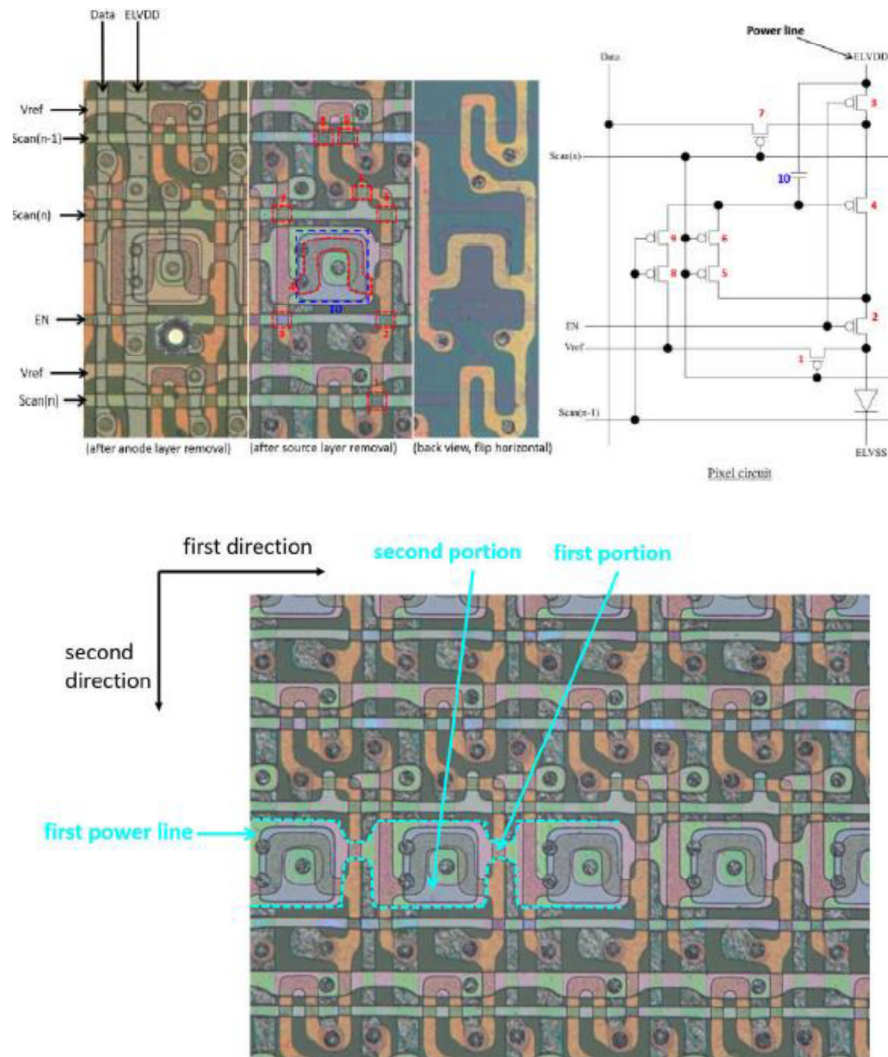


42. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer removed and displayed at 1500x magnification, the external OLED panel of Motorola RAZR has a data line and a control line.

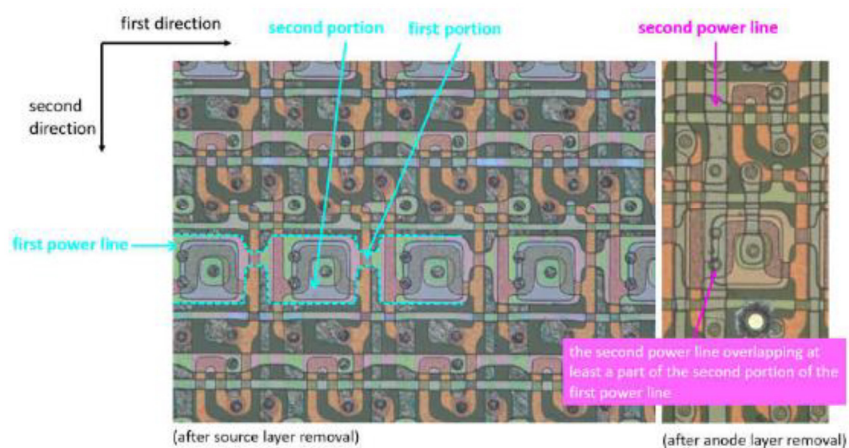


43. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer and source layer are removed and displayed at 1500x magnification, the external OLED panel has a first power line that has a first portion

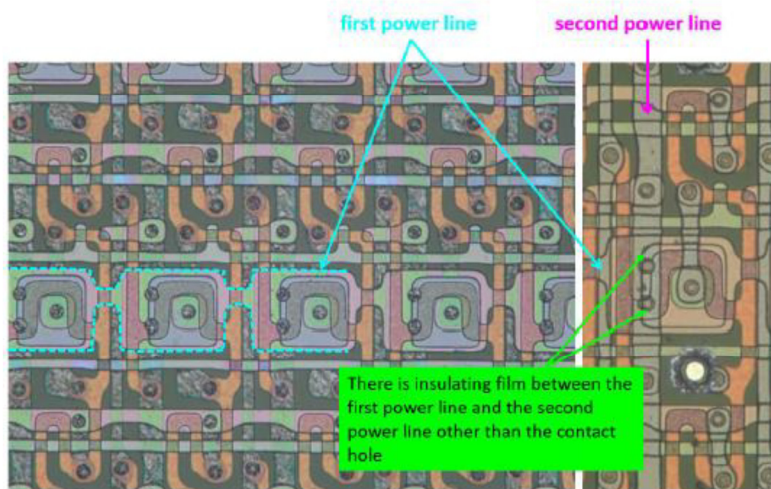
extending in a first direction and a second portion extending in a second direction that intersects the first direction.

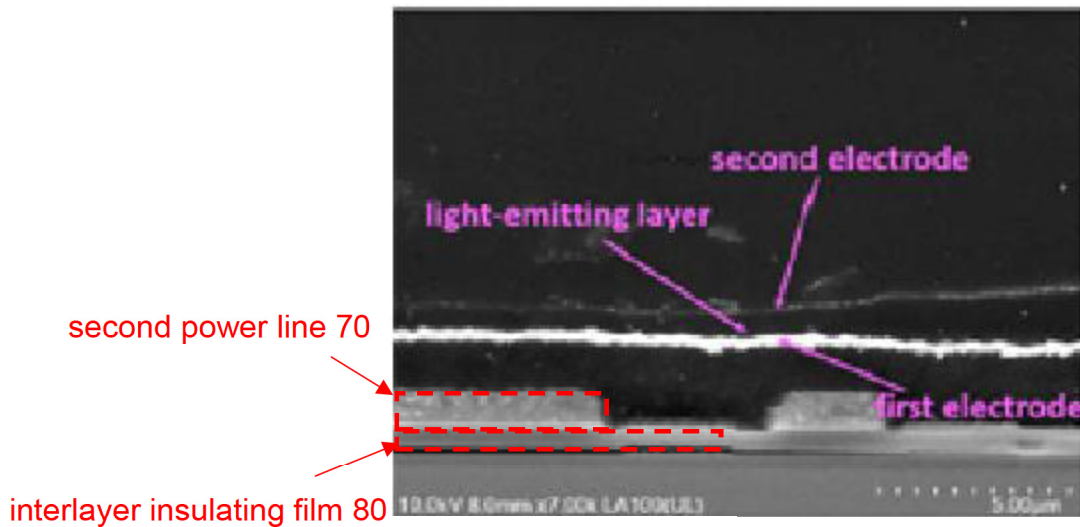


44. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer is removed and displayed at 1500x magnification, the external OLED panel has a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line.

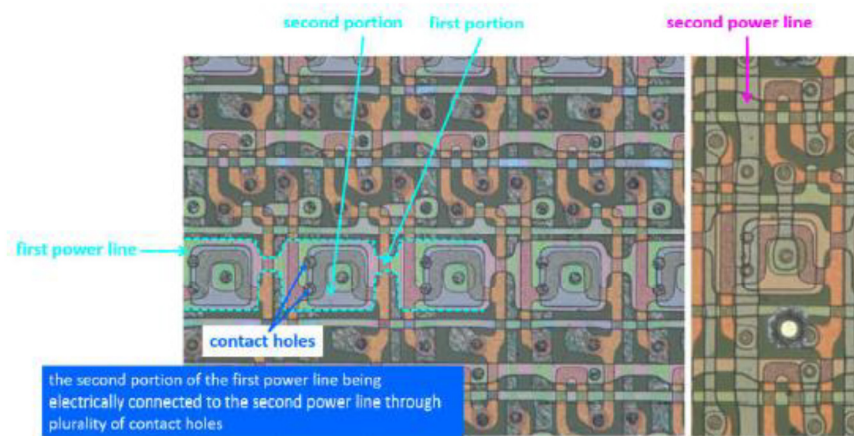


45. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer and source layer are removed and displayed at 1500x magnification, the external OLED panel has an inter-layer insulating film that is disposed between the first power line and the second power line.



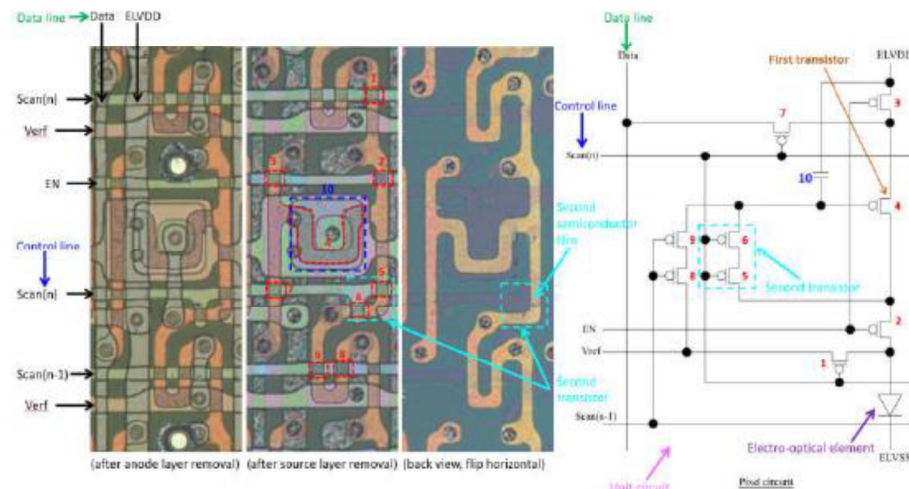


46. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer and source layer are removed and displayed at 1500x magnification, in the external OLED panel, the second portion of the first power line is electrically connected to the second power line through plurality of contact holes.

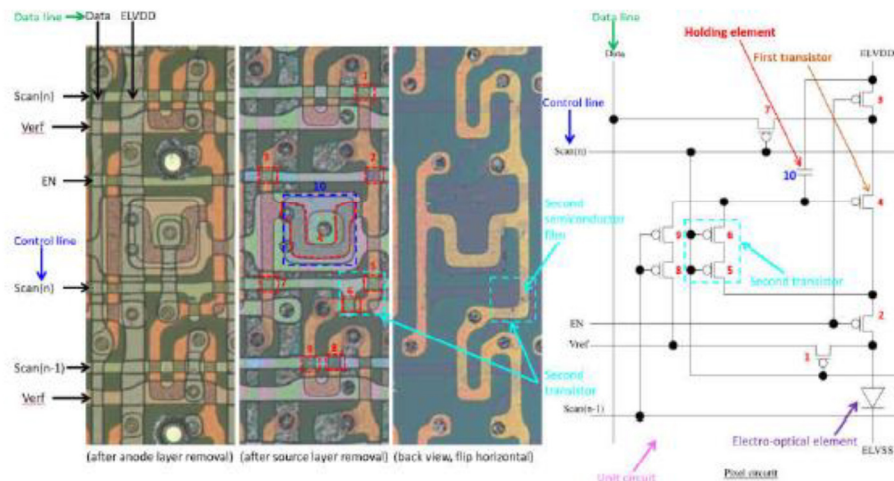


47. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer are removed and in a pixel circuit of the external display of the Motorola RAZR after source layer are removed and displayed at 1500x magnification, the unit circuit of the external OLED panel has a second transistor that includes a second

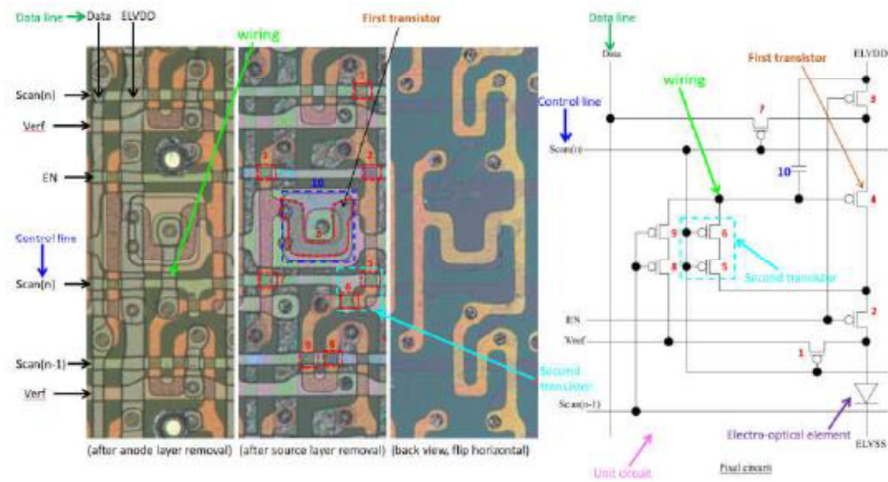
semiconductor film, and the second transistor is connected between the one of the source or the drain and a gate of the first transistor.



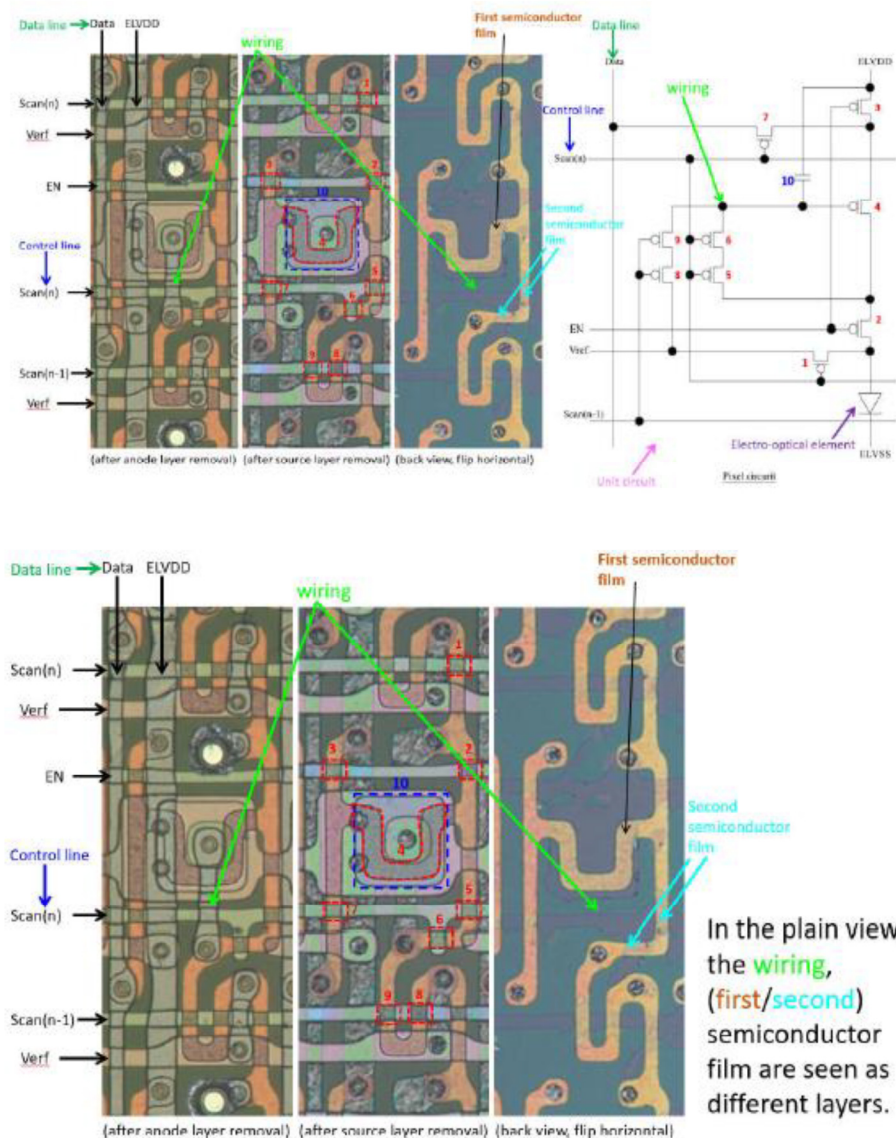
48. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer are removed and in a pixel circuit of the external display of the Motorola RAZR after source layer are removed and displayed at 1500x magnification, the unit circuit of the external OLED panel has a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal.



49. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer is removed and displayed at 1500x magnification, the unit circuit of the external OLED panel has a wiring connected between the second transistor and the gate of the first transistor, and the first transistor supplying a current based on the gate voltage to the electro-optical element.

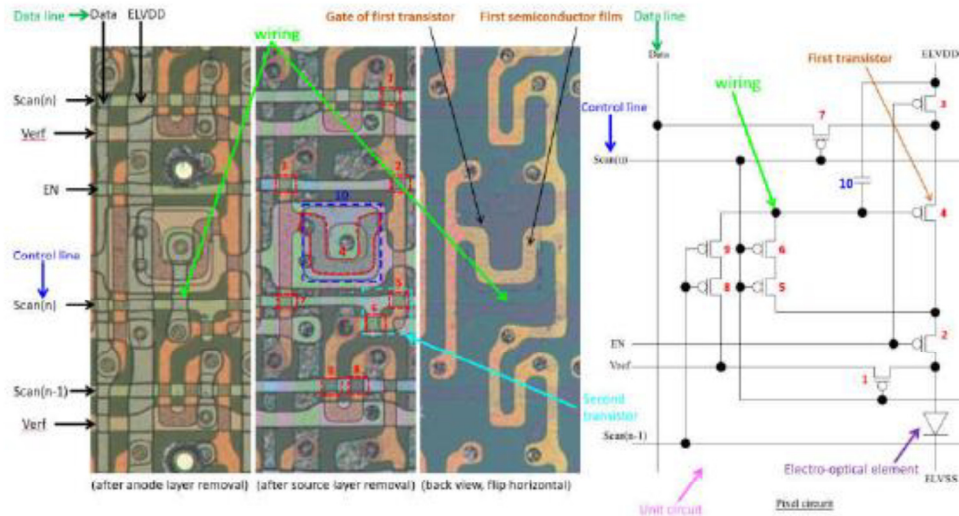


50. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer are removed and in a back view of a pixel circuit of the external display of the Motorola RAZR both displayed at 1500x magnification, in the unit circuit of the external OLED panel, the wiring is formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed.



51. As shown below, in a pixel circuit of the external display of the Motorola RAZR after anode layer are removed, in a pixel circuit of the external display of the Motorola RAZR after source layer are removed, and in a back view of a pixel circuit of the external display of the Motorola RAZR all displayed at 1500x magnification, in the unit circuit of the external OLED panel, the wiring having a portion formed in the layer

different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.



52. Defendant BOE Technology Group Co., Ltd and its subsidiaries were previously licensed to practice '736 Patent, the '267 Patent, and the '760 Patent. BOE was fully aware of the patents in suit when entering into the license agreement in 2014. However, BOE chose not to take a license to these patents in 2019 when the previous license expired. BOE has been practicing these patents since 2014 on a knowingly basis. Defendants continued to actively and knowingly contribute to, encourage, aid, and abet others to import, sell, offer to sell, and use the infringing active-matrix display products in the United States and Texas. Accordingly, Defendants have engaged in direct and/or indirect infringement with full knowledge of their infringement and the infringement of their customers, as well as willful infringement.

V.

CLAIMS FOR RELIEF

COUNT 1: INFRINGEMENT OF THE ‘736 PATENT

53. The allegations of Paragraphs 1-52 are repeated and realleged as if fully set forth in this Count I of the Complaint.

54. Defendants continued, after notice of infringement and without authority, to make, use, sell, offer to sell, and/or import into the United States Defendants’ products as shown above.

55. Defendants thus have infringed and continues to infringe at least one of claims 3-5, 7, 9, and 13-17 of the ‘736 Patent literally and/or under the doctrine of equivalents.

56. Defendants have also actively induced and will continue to actively induce the infringement of at least one of claims 3-5, 7, 9, and 13-17 of the ‘736 Patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively and knowingly aiding and abetting infringement of others through activities such as creating and/or distributing data sheets, requirements documents, assembly instructions and/or similar materials with instructions on creating, manufacturing, designing, assembling and/or implementing infringing products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States products that fall within the scope of the ‘736 Patent without license or authority from Plaintiff. On information and belief, Defendants know that the induced acts constitute infringement of the ‘736 Patent.

57. Defendants individually, collectively, or through others or intermediaries, have contributorily infringed, and/or is contributorily infringing, at least one claim of the ‘736 Patent by making, using, offering for sale, selling, and/or importing, material parts of the inventions claimed in the ‘736 Patent, which are not a staple article or commodity of commerce suitable for substantial non-infringing use, and knowing the accused parts to be especially made or especially adapted for use in an infringement of the ‘736 Patent.

58. Defendants had knowledge of the ‘736 Patent and of its infringement before the filing of this action.

59. Defendants have knowledge of the ‘736 Patent at least as of the date when it was notified of the filing of this action. Defendants’ direct and indirect infringement of the ‘736 Patent have thus been committed with knowledge of the ‘736 Patent, making Defendants liable for direct, indirect, and willful infringement.

60. Defendants’ infringement of the ‘736 Patent will continue to damage Element Capital, causing irreparable harm for which there is no adequate remedy at law, unless it is enjoined by this Court.

61. Element Capital has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants is liable to Element Capital in an amount that adequately compensates it for such infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

62. Element Capital and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law.

COUNT 2: INFRINGEMENT OF THE '267 PATENT

63. The allegations of Paragraphs 1-62 are repeated and realleged as if fully set forth in this Count II of the Complaint.

64. Defendants continued, after notice of infringement and without authority, to make, use, sell, offer to sell, and/or import into the United States Defendants' products as shown above.

65. Defendants thus have infringed and continues to infringe at least claim 1 of the '267 Patent literally and/or under the doctrine of equivalents.

66. Defendants have also actively induced and will continue to actively induce the infringement of at least claim 1 of the '267 Patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively and knowingly aiding and abetting infringement of others through activities such as creating and/or distributing data sheets, requirements documents, assembly instructions and/or similar materials with instructions on creating, manufacturing, designing, assembling and/or implementing infringing products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States products that fall within the scope of the '267 Patent without license or authority from Plaintiff. On information and belief, Defendants know that the induced acts constitute infringement of the '267 Patent.

67. Defendants individually, collectively, or through others or intermediaries, have contributorily infringed, and/or is contributorily infringing, at least one claim of the ‘267 Patent by making, using, offering for sale, selling, and/or importing, material parts of the inventions claimed in the ‘267 Patent, which are not a staple article or commodity of commerce suitable for substantial non-infringing use, and knowing the accused parts to be especially made or especially adapted for use in an infringement of the ‘267 Patent.

68. Defendants had knowledge of the ‘267 Patent and of its infringement before the filing of this action.

69. Defendants have knowledge of the ‘267 Patent at least as of the date when they were notified of the filing of this action. Defendants’ direct and indirect infringement of the ‘267 Patent have thus been committed with knowledge of the ‘267 Patent, making Defendants liable for direct, indirect, and willful infringement.

70. Defendants’ infringement of the ‘267 Patent will continue to damage Element Capital, causing irreparable harm for which there is no adequate remedy at law, unless it is enjoined by this Court.

71. Element Capital has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants is liable to Element Capital in an amount that adequately compensates it for such infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

72. Element Capital and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law.

COUNT 3: INFRINGEMENT OF THE ‘760 PATENT

73. The allegations of Paragraphs 1-72 are repeated and realleged as if fully set forth in this Count III of the Complaint.

74. Defendants continued, after notice of infringement and without authority, to make, use, sell, offer to sell, and/or import into the United States Defendants’ products as shown above.

75. Defendants thus have infringed and continues to infringe at least claim 1 of the ‘760 Patent literally and/or under the doctrine of equivalents.

76. Defendants have also actively induced and will continue to actively induce the infringement of at least claim 1 of the ‘760 Patent, in violation of 35 U.S.C. § 271(b), by, among other things, actively and knowingly aiding and abetting infringement of others through activities such as creating and/or distributing data sheets, requirements documents, assembly instructions and/or similar materials with instructions on creating, manufacturing, designing, assembling and/or implementing infringing products, with the specific intent to induce others to directly make, use, offer for sale, sell, and/or import into the United States products that fall within the scope of the ‘760 Patent without license or authority from Plaintiff. On information and belief, Defendants know that the induced acts constitute infringement of the ‘760 Patent.

77. Defendants individually, collectively, or through others or intermediaries, have contributorily infringed, and/or are contributorily infringing, at least one claim of the ‘760 Patent by making, using, offering for sale, selling, and/or importing, material parts of the inventions claimed in the ‘760 Patent, which are not a staple article or commodity of commerce suitable for substantial non-infringing use, and knowing the accused parts to be especially made or especially adapted for use in an infringement of the ‘760 Patent.

78. Defendants had knowledge of the ‘760 Patent and of its infringement before the filing of this action.

79. Defendants have knowledge of the ‘760 Patent at least as of the date when they were notified of the filing of this action. Defendants’ direct and indirect infringement of the ‘760 Patent have thus been committed with knowledge of the ‘760 Patent, making Defendants liable for direct, indirect, and willful infringement.

80. Defendants’ infringement of the ‘760 Patent will continue to damage Element Capital, causing irreparable harm for which there is no adequate remedy at law, unless it is enjoined by this Court.

81. Element Capital has been damaged as a result of the infringing conduct by Defendants alleged above. Thus, Defendants is liable to Element Capital in an amount that adequately compensates it for such infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

82. Element Capital and/or its predecessors-in-interest have satisfied all statutory obligations required to collect pre-filing damages for the full period allowed by law.

VI.

PRAYER FOR RELIEF

83. **WHEREFORE**, Plaintiff Element Capital asks this Court to enter judgment in its favor against Defendants and grant the following relief:

84. An adjudication that Defendants have infringed and continue to infringe the ‘736 Patent;

85. An accounting of all damages sustained by Element Capital as a result of Defendants’ acts of infringement of the ‘736 Patent, the ‘267 Patent, and the ‘760 Patent;

86. An award to Element Capital of actual damages adequate to compensate Element Capital for Defendants’ acts of patent infringement, together with prejudgment and post-judgment interest;

87. An award to Element Capital of enhanced damages, up to and including trebling of Element Capital’s damages pursuant to 35 U.S.C. § 284 for Defendants’ willful infringement of the ‘736 Patent, the ‘267 Patent, and the ‘760 Patent;

88. An award of Element Capital’s costs of suit and reasonable attorneys’ fees pursuant to 35 U.S.C. § 285 due to the exceptional nature of the case, or otherwise permitted by law;

89. A grant of a permanent injunction pursuant to 35 U.S.C. § 283, enjoining Defendants, and each of its agents, servants, employees, principals, officers, attorneys, successors, assignees, and all those in active concert or participation with Defendants, including related individuals and entities, customers, representatives, OEMs, dealers, and distributors from further acts of (1) direct infringement, (2) contributory infringement, and (3) active inducement to infringe with respect to the claims of the '736 Patent, the '267 Patent, and the '760 Patent; and

90. Any further relief that this Court deems just and proper.

VII.

JURY DEMAND

Plaintiff Element Capital requests a jury trial on all issues triable to a jury in this matter.

DATE: April 18, 2022

/s/ J. Thad Heartfield
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ATTORNEYS FOR PLAINTIFF

CIVIL COVER SHEET

The JS 44 civil cover sheet and the information contained herein neither replace nor supplement the filing and service of pleadings or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. (SEE INSTRUCTIONS ON NEXT PAGE OF THIS FORM.)

I. (a) PLAINTIFFS

Element Capital Commercial Company PTE. LTD

(b) County of Residence of First Listed Plaintiff Singapore
(EXCEPT IN U.S. PLAINTIFF CASES)

(c) Attorneys (Firm Name, Address, and Telephone Number)

J. Thad Heartfield, The Heartfield Law Firm, 2195
Dowlen Rd., Beaumont, Texas 77706, (409) 866-3318

DEFENDANTS

BOE Technology Group Co., Ltd; Beijing BOE Display

County of Residence of First Listed Defendant
(IN U.S. PLAINTIFF CASES ONLY)NOTE: IN LAND CONDEMNATION CASES, USE THE LOCATION OF
THE TRACT OF LAND INVOLVED.

Attorneys (If Known)

II. BASIS OF JURISDICTION (Place an "X" in One Box Only)

- ☐ 1 U.S. Government Plaintiff
- ☒ 3 Federal Question
(U.S. Government Not a Party)
- ☐ 2 U.S. Government Defendant
- ☐ 4 Diversity
(Indicate Citizenship of Parties in Item III)

III. CITIZENSHIP OF PRINCIPAL PARTIES (Place an "X" in One Box for Plaintiff and One Box for Defendant)

- | | PTF | DEF | | PTF | DEF |
|---|----------------------------|----------------------------|---|----------------------------|----------------------------|
| Citizen of This State | ☐ 1 | ☐ 1 | Incorporated or Principal Place of Business In This State | ☐ 4 | ☐ 4 |
| Citizen of Another State | ☐ 2 | ☐ 2 | Incorporated and Principal Place of Business In Another State | ☐ 5 | ☐ 5 |
| Citizen or Subject of a Foreign Country | ☐ 3 | ☐ 3 | Foreign Nation | ☐ 6 | ☐ 6 |

IV. NATURE OF SUIT (Place an "X" in One Box Only)

Click here for: [Nature of Suit Code Descriptions.](#)

CONTRACT	TORTS	FORFEITURE/PENALTY	BANKRUPTCY	OTHER STATUTES
☐ 110 Insurance	PERSONAL INJURY	☐ 625 Drug Related Seizure of Property 21 USC 881	☐ 422 Appeal 28 USC 158	☐ 375 False Claims Act
☐ 120 Marine	☐ 310 Airplane	☐ 690 Other	☐ 423 Withdrawal 28 USC 157	☐ 376 Qui Tam (31 USC 3729(a))
☐ 130 Miller Act	☐ 315 Airplane Product Liability		INTELLECTUAL PROPERTY RIGHTS	☐ 400 State Reapportionment
☐ 140 Negotiable Instrument	☐ 320 Assault, Libel & Slander		☐ 820 Copyrights	☐ 410 Antitrust
☐ 150 Recovery of Overpayment & Enforcement of Judgment	☐ 330 Federal Employers' Liability		☒ 830 Patent	☐ 430 Banks and Banking
☐ 151 Medicare Act	☐ 340 Marine		☐ 835 Patent - Abbreviated New Drug Application	☐ 450 Commerce
☐ 152 Recovery of Defaulted Student Loans (Excludes Veterans)	☐ 345 Marine Product Liability		☐ 840 Trademark	☐ 460 Deportation
☐ 153 Recovery of Overpayment of Veteran's Benefits	☐ 350 Motor Vehicle	LABOR	☐ 880 Defend Trade Secrets Act of 2016	☐ 470 Racketeer Influenced and Corrupt Organizations
☐ 160 Stockholders' Suits	☐ 355 Motor Vehicle Product Liability	☐ 710 Fair Labor Standards Act	SOCIAL SECURITY	☐ 480 Consumer Credit (15 USC 1681 or 1692)
☐ 190 Other Contract	☐ 360 Other Personal Injury	☐ 720 Labor/Management Relations	☐ 861 HIA (1395ff)	☐ 485 Telephone Consumer Protection Act
☐ 195 Contract Product Liability	☐ 362 Personal Injury - Medical Malpractice	☐ 740 Railway Labor Act	☐ 862 Black Lung (923)	☐ 490 Cable/Sat TV
☐ 196 Franchise		☐ 751 Family and Medical Leave Act	☐ 863 DIWC/DIWW (405(g))	☐ 850 Securities/Commodities/Exchange
REAL PROPERTY	CIVIL RIGHTS	☐ 790 Other Labor Litigation	☐ 864 SSID Title XVI	☐ 890 Other Statutory Actions
☐ 210 Land Condemnation	☐ 440 Other Civil Rights	☐ 791 Employee Retirement Income Security Act	☐ 865 RSI (405(g))	☐ 891 Agricultural Acts
☐ 220 Foreclosure	☐ 441 Voting	IMMIGRATION	FEDERAL TAX SUITS	☐ 893 Environmental Matters
☐ 230 Rent Lease & Ejectment	☐ 442 Employment	☐ 462 Naturalization Application	☐ 870 Taxes (U.S. Plaintiff or Defendant)	☐ 895 Freedom of Information Act
☐ 240 Torts to Land	☐ 443 Housing/Accommodations	☐ 465 Other Immigration Actions	☐ 871 IRS—Third Party 26 USC 7609	☐ 896 Arbitration
☐ 245 Tort Product Liability	☐ 445 Amer. w/Disabilities - Employment			☐ 899 Administrative Procedure Act/Review or Appeal of Agency Decision
☐ 290 All Other Real Property	☐ 446 Amer. w/Disabilities - Other			☐ 950 Constitutionality of State Statutes
	☐ 448 Education			
	PRISONER PETITIONS			
	Habeas Corpus:			
	☐ 463 Alien Detainee			
	☐ 510 Motions to Vacate Sentence			
	☐ 530 General			
	☐ 535 Death Penalty			
	Other:			
	☐ 540 Mandamus & Other			
	☐ 550 Civil Rights			
	☐ 555 Prison Condition			
	☐ 560 Civil Detainee - Conditions of Confinement			

V. ORIGIN (Place an "X" in One Box Only)

- ☒ 1 Original Proceeding
- ☐ 2 Removed from State Court
- ☐ 3 Remanded from Appellate Court
- ☐ 4 Reinstated or Reopened
- ☐ 5 Transferred from Another District (specify)
- ☐ 6 Multidistrict Litigation - Transfer
- ☐ 8 Multidistrict Litigation - Direct File

VI. CAUSE OF ACTION

Cite the U.S. Civil Statute under which you are filing (Do not cite jurisdictional statutes unless diversity):
35 U.S.C. § 1 et seq., 28 U.S.C. §§ 1331 and 1338(a)Brief description of cause:
Patent infringement

VII. REQUESTED IN COMPLAINT:

☐ CHECK IF THIS IS A CLASS ACTION UNDER RULE 23, F.R.Cv.P.

DEMAND \$

CHECK YES only if demanded in complaint:

JURY DEMAND: ☒ Yes ☐ No

VIII. RELATED CASE(S) IF ANY

(See instructions):

JUDGE

DOCKET NUMBER

DATE

SIGNATURE OF ATTORNEY OF RECORD

04/18/2022

/s/ J. Thad Heartfield

FOR OFFICE USE ONLY

RECEIPT #

AMOUNT

APPLYING IFP

JUDGE

MAG. JUDGE

INSTRUCTIONS FOR ATTORNEYS COMPLETING CIVIL COVER SHEET FORM JS 44

Authority For Civil Cover Sheet

The JS 44 civil cover sheet and the information contained herein neither replaces nor supplements the filings and service of pleading or other papers as required by law, except as provided by local rules of court. This form, approved by the Judicial Conference of the United States in September 1974, is required for the use of the Clerk of Court for the purpose of initiating the civil docket sheet. Consequently, a civil cover sheet is submitted to the Clerk of Court for each civil complaint filed. The attorney filing a case should complete the form as follows:

- I.(a) Plaintiffs-Defendants.** Enter names (last, first, middle initial) of plaintiff and defendant. If the plaintiff or defendant is a government agency, use only the full name or standard abbreviations. If the plaintiff or defendant is an official within a government agency, identify first the agency and then the official, giving both name and title.
 - (b) County of Residence.** For each civil case filed, except U.S. plaintiff cases, enter the name of the county where the first listed plaintiff resides at the time of filing. In U.S. plaintiff cases, enter the name of the county in which the first listed defendant resides at the time of filing. (NOTE: In land condemnation cases, the county of residence of the "defendant" is the location of the tract of land involved.)
 - (c) Attorneys.** Enter the firm name, address, telephone number, and attorney of record. If there are several attorneys, list them on an attachment, noting in this section "(see attachment)".
- II. Jurisdiction.** The basis of jurisdiction is set forth under Rule 8(a), F.R.Cv.P., which requires that jurisdictions be shown in pleadings. Place an "X" in one of the boxes. If there is more than one basis of jurisdiction, precedence is given in the order shown below.
- United States plaintiff. (1) Jurisdiction based on 28 U.S.C. 1345 and 1348. Suits by agencies and officers of the United States are included here. United States defendant. (2) When the plaintiff is suing the United States, its officers or agencies, place an "X" in this box.
- Federal question. (3) This refers to suits under 28 U.S.C. 1331, where jurisdiction arises under the Constitution of the United States, an amendment to the Constitution, an act of Congress or a treaty of the United States. In cases where the U.S. is a party, the U.S. plaintiff or defendant code takes precedence, and box 1 or 2 should be marked.
- Diversity of citizenship. (4) This refers to suits under 28 U.S.C. 1332, where parties are citizens of different states. When Box 4 is checked, the citizenship of the different parties must be checked. (See Section III below; **NOTE: federal question actions take precedence over diversity cases.**)
- III. Residence (citizenship) of Principal Parties.** This section of the JS 44 is to be completed if diversity of citizenship was indicated above. Mark this section for each principal party.
- IV. Nature of Suit.** Place an "X" in the appropriate box. If there are multiple nature of suit codes associated with the case, pick the nature of suit code that is most applicable. Click here for: [Nature of Suit Code Descriptions](#).
- V. Origin.** Place an "X" in one of the seven boxes.
- Original Proceedings. (1) Cases which originate in the United States district courts.
- Removed from State Court. (2) Proceedings initiated in state courts may be removed to the district courts under Title 28 U.S.C., Section 1441.
- Remanded from Appellate Court. (3) Check this box for cases remanded to the district court for further action. Use the date of remand as the filing date.
- Reinstated or Reopened. (4) Check this box for cases reinstated or reopened in the district court. Use the reopening date as the filing date.
- Transferred from Another District. (5) For cases transferred under Title 28 U.S.C. Section 1404(a). Do not use this for within district transfers or multidistrict litigation transfers.
- Multidistrict Litigation – Transfer. (6) Check this box when a multidistrict case is transferred into the district under authority of Title 28 U.S.C. Section 1407.
- Multidistrict Litigation – Direct File. (8) Check this box when a multidistrict case is filed in the same district as the Master MDL docket.
- PLEASE NOTE THAT THERE IS NOT AN ORIGIN CODE 7.** Origin Code 7 was used for historical records and is no longer relevant due to changes in statute.
- VI. Cause of Action.** Report the civil statute directly related to the cause of action and give a brief description of the cause. **Do not cite jurisdictional statutes unless diversity.** Example: U.S. Civil Statute: 47 USC 553 Brief Description: Unauthorized reception of cable service.
- VII. Requested in Complaint.** Class Action. Place an "X" in this box if you are filing a class action under Rule 23, F.R.Cv.P.
- Demand. In this space enter the actual dollar amount being demanded or indicate other demand, such as a preliminary injunction.
- Jury Demand. Check the appropriate box to indicate whether or not a jury is being demanded.
- VIII. Related Cases.** This section of the JS 44 is used to reference related pending cases, if any. If there are related pending cases, insert the docket numbers and the corresponding judge names for such cases.

Date and Attorney Signature. Date and sign the civil cover sheet.

Exhibit 1



US007259736B2

(12) **United States Patent**
Nakanishi

(10) **Patent No.:** **US 7,259,736 B2**
(45) **Date of Patent:** **Aug. 21, 2007**

(54) **ELECTRO-OPTICAL DEVICE,
ACTIVE-MATRIX SUBSTRATE, AND
ELECTRONIC APPARATUS**

(75) Inventor: **Hayato Nakanishi**, Toyama (JP)

(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 440 days.

(21) Appl. No.: **10/712,381**

(22) Filed: **Nov. 14, 2003**

(65) **Prior Publication Data**

US 2004/0130512 A1 Jul. 8, 2004

(30) **Foreign Application Priority Data**

Nov. 29, 2002 (JP) 2002-348622

(51) **Int. Cl.**
G09G 5/00 (2006.01)

(52) **U.S. Cl.** **345/82**; 345/76; 345/103;
345/84; 349/73; 315/169.3

(58) **Field of Classification Search** 345/76-83,
345/204-205, 87-103; 257/552; 340/815.45;
313/498; 315/169.3, 169.4
See application file for complete search history.

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* cited by examiner

Primary Examiner—Lun-Yi Lao

(74) *Attorney, Agent, or Firm*—Oliff & Berridge, PLC

(57) **ABSTRACT**

To provide an electro-optical device and an electronic apparatus which reduce directional viewing variation that occurs between the column and row directions and to provide an active matrix substrate suitable for the electro-optical device. In each pixel circuit arranged at a display panel portion in a matrix, the upper left side of the formation region is allotted to a green pixel-forming region having an organic EL element that emits green, the upper right side is allotted to a blue pixel-forming region having an organic EL element that emits blue, the lower left side is allotted to a dummy forming region having no light-emitting organic EL element, and the lower right side is allotted to a red pixel-forming region having an organic EL element that emits red. Two adjacent same-color organic EL elements are formed at regular intervals with one forming region interposed therebetween.

37 Claims, 8 Drawing Sheets

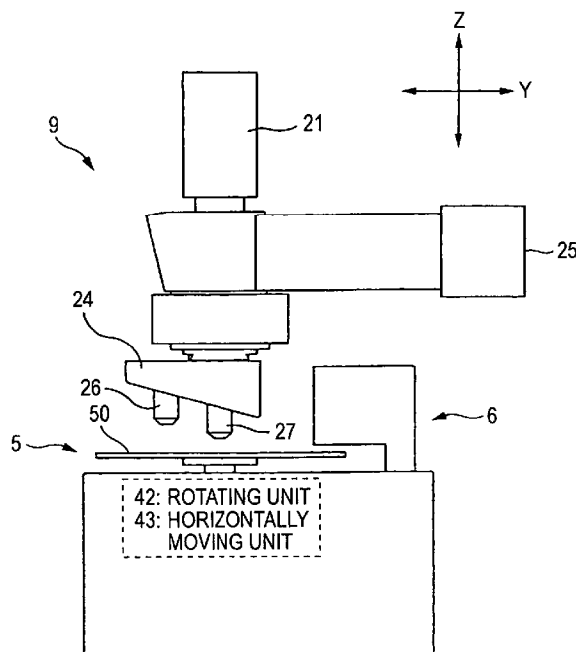
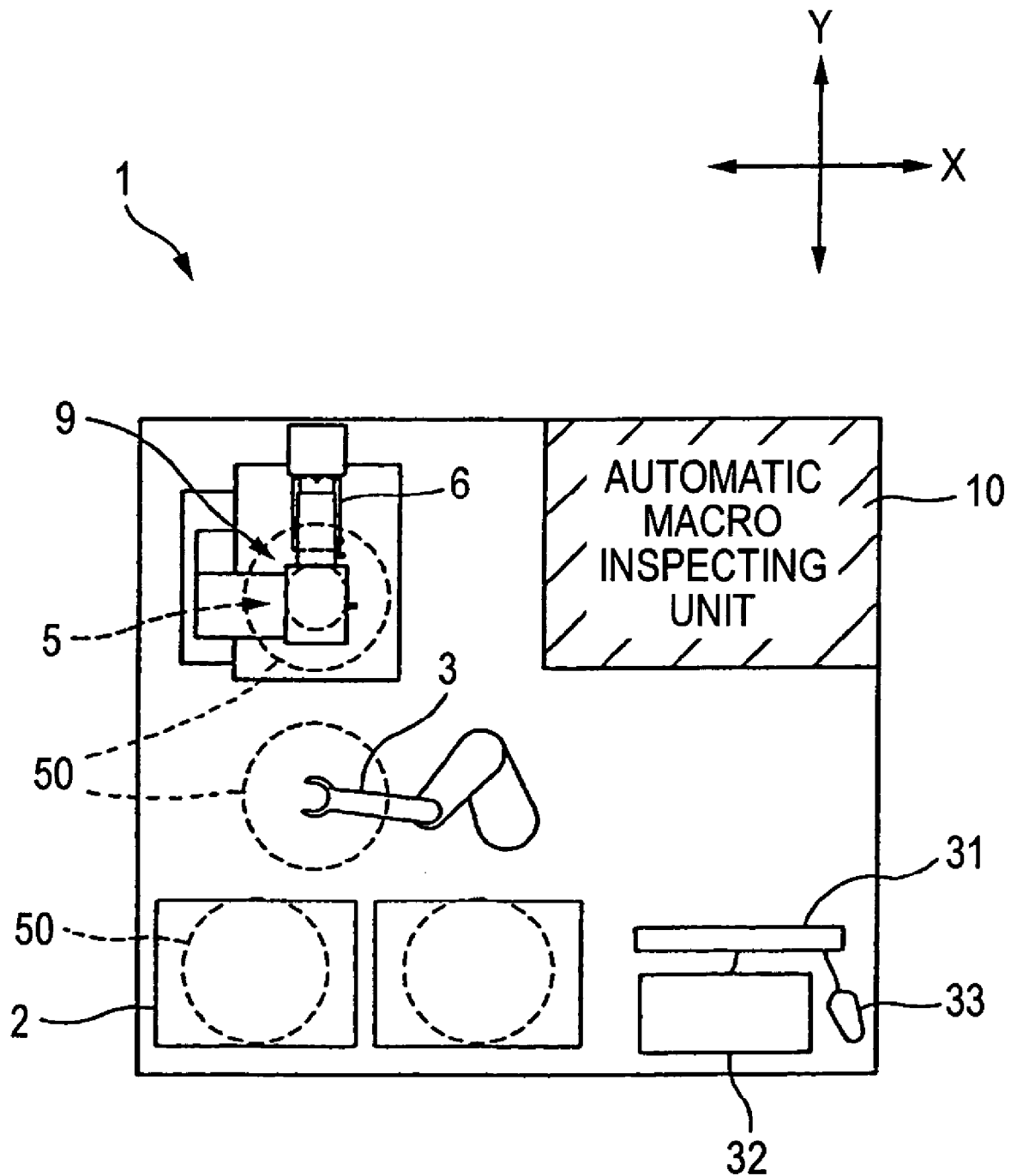


FIG. 1



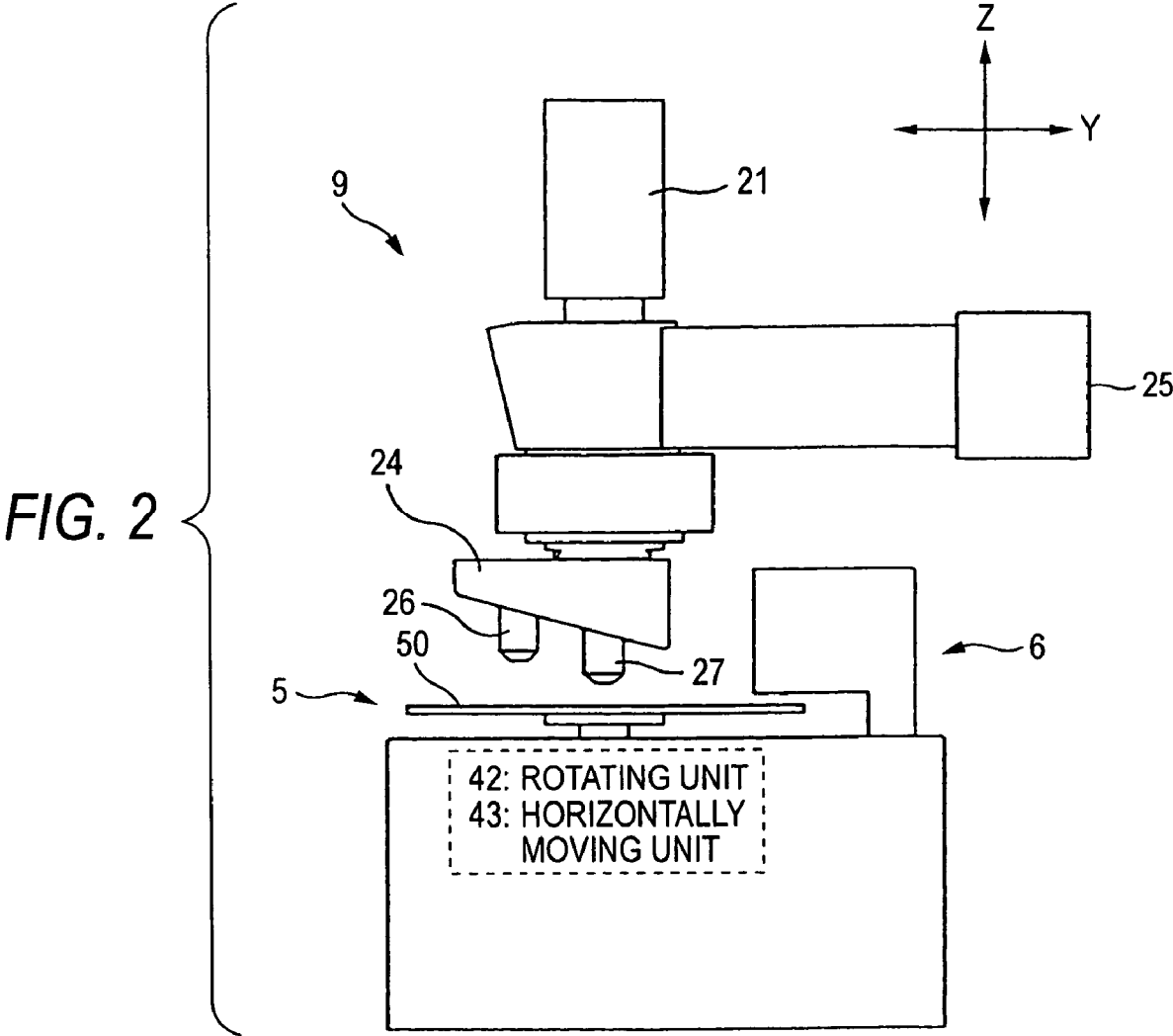


FIG. 3A

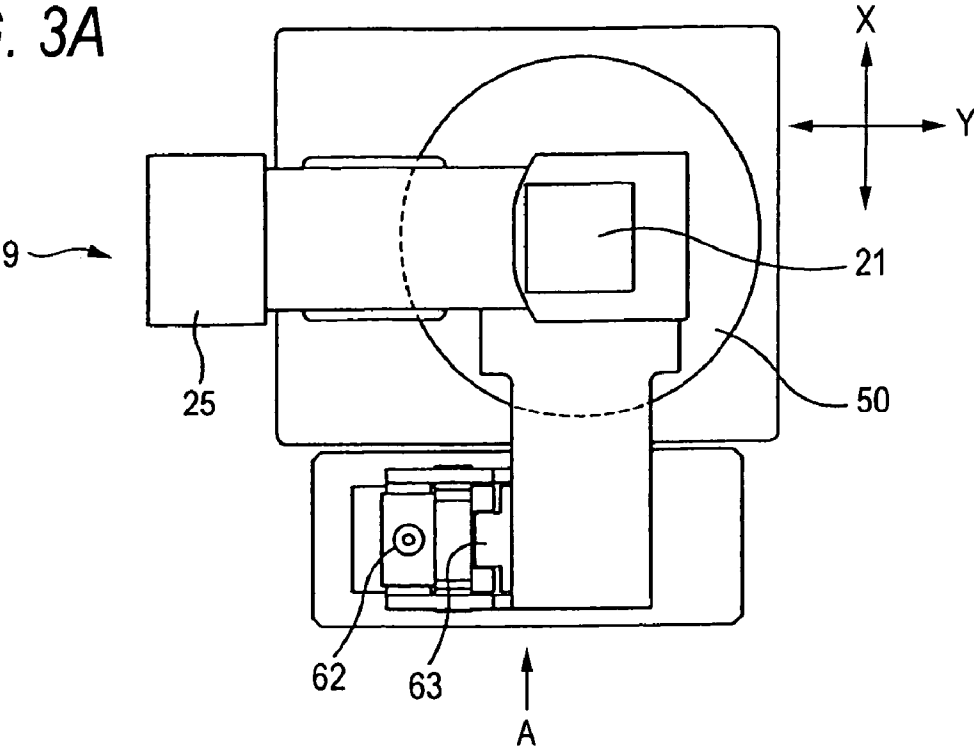


FIG. 3B

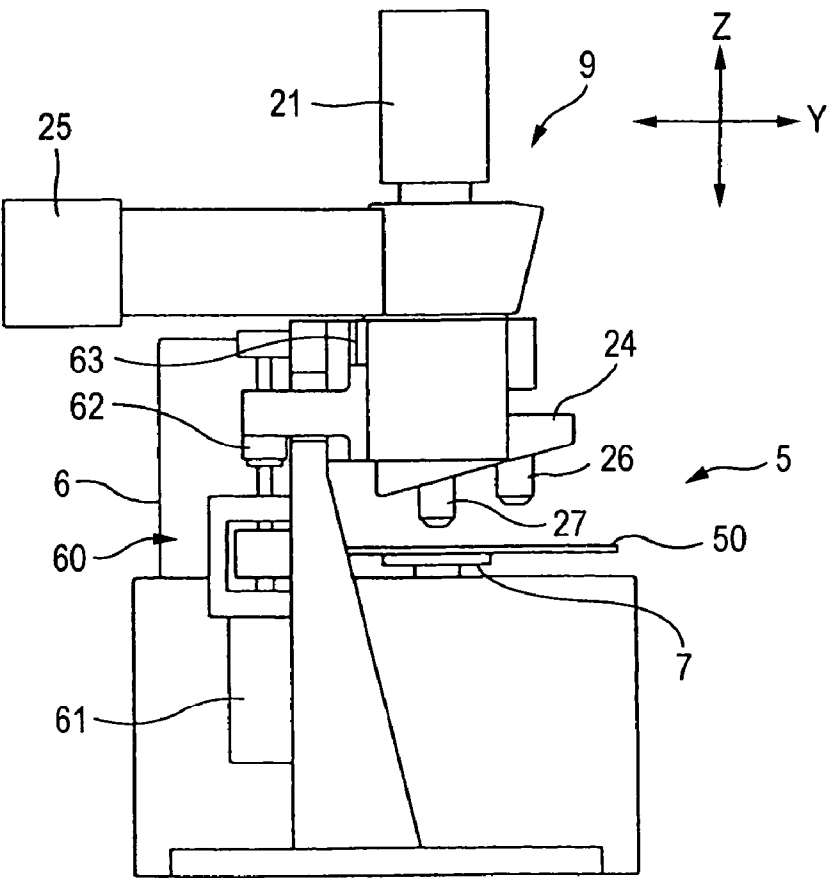


FIG. 4A

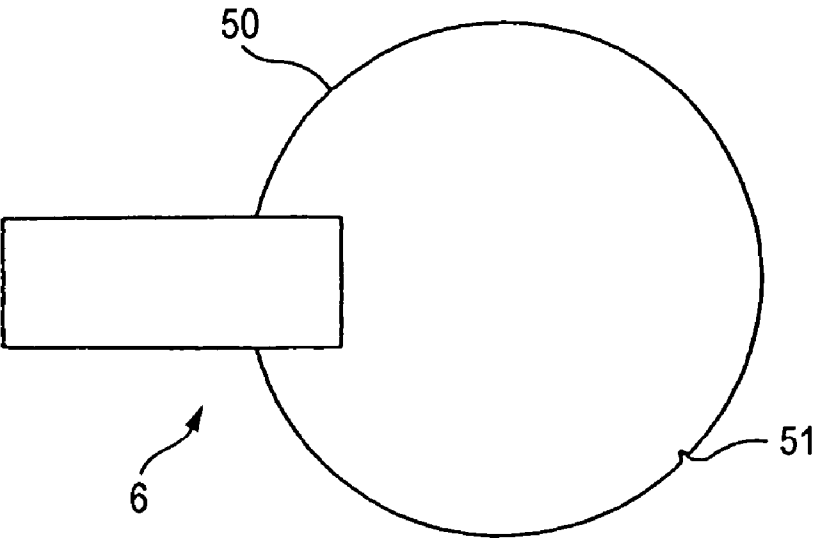


FIG. 4B

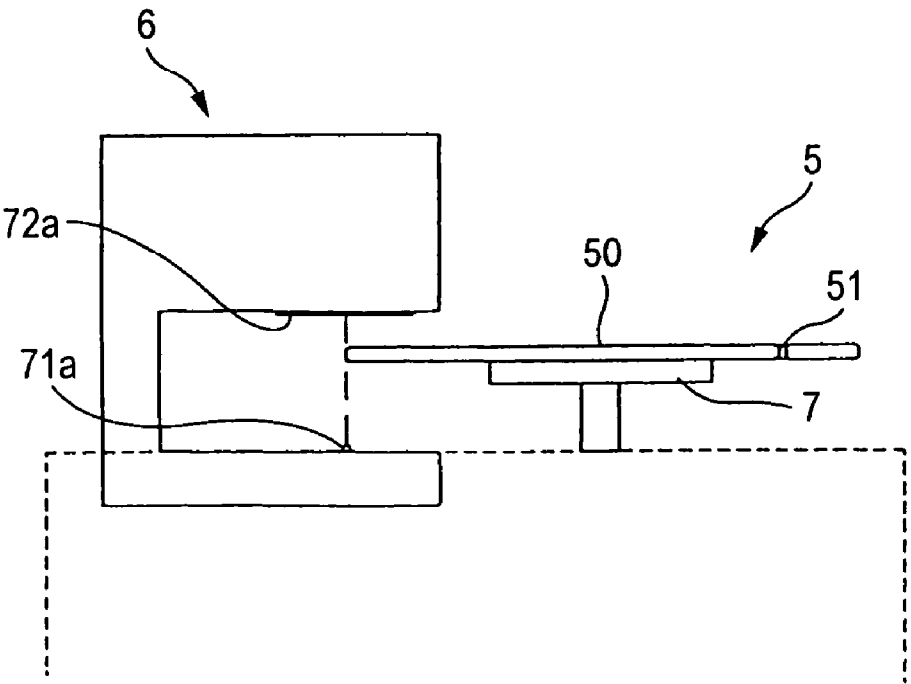


FIG. 5

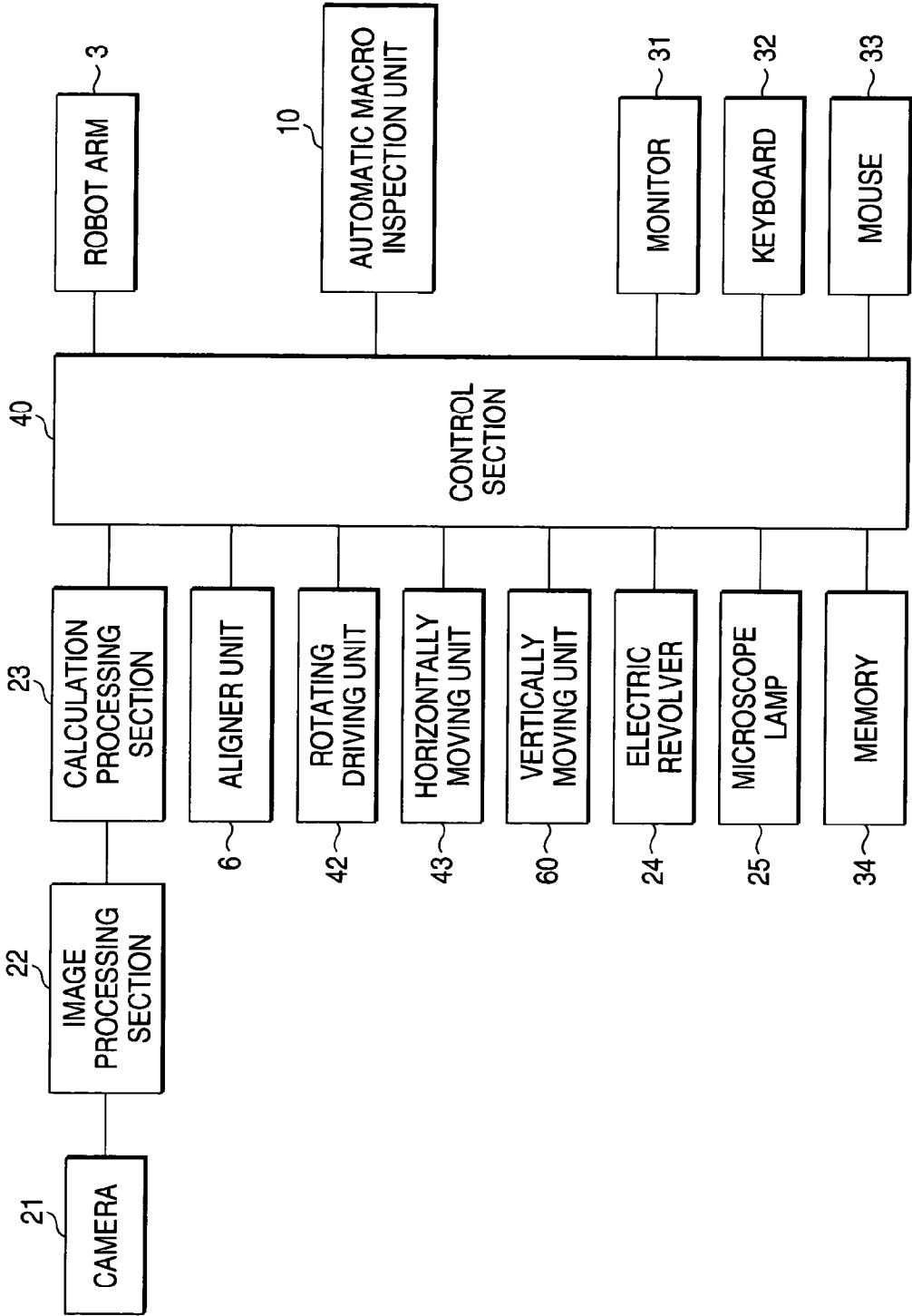


FIG. 6

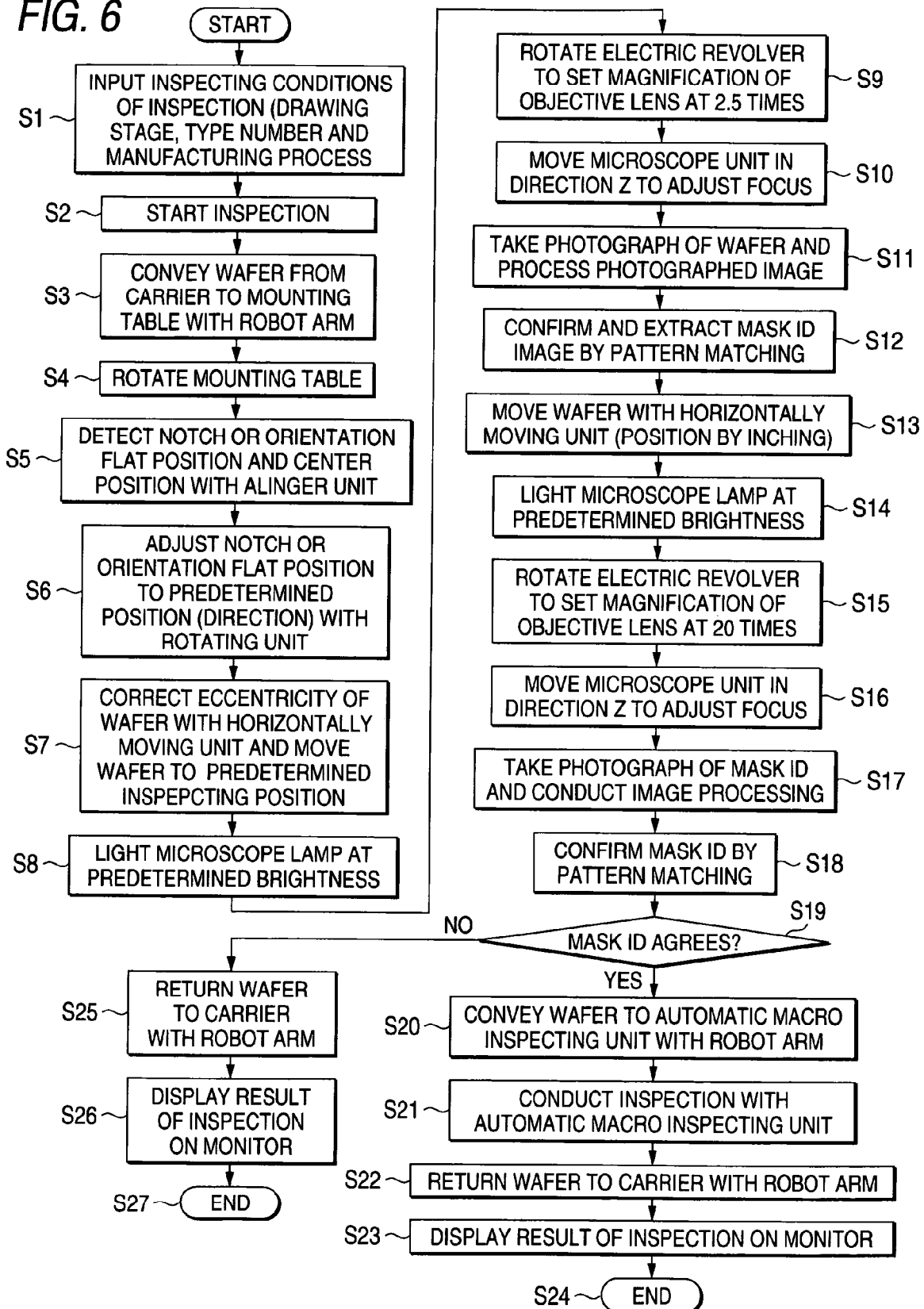


FIG. 7

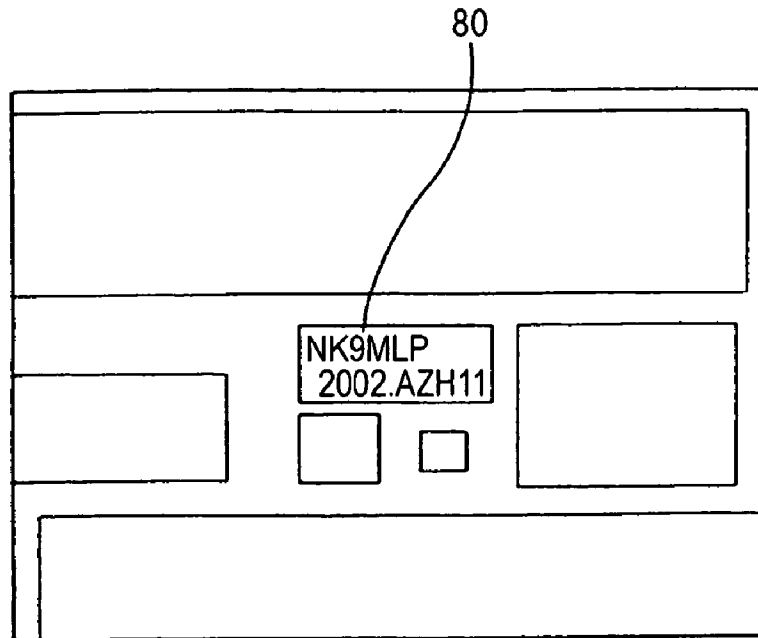
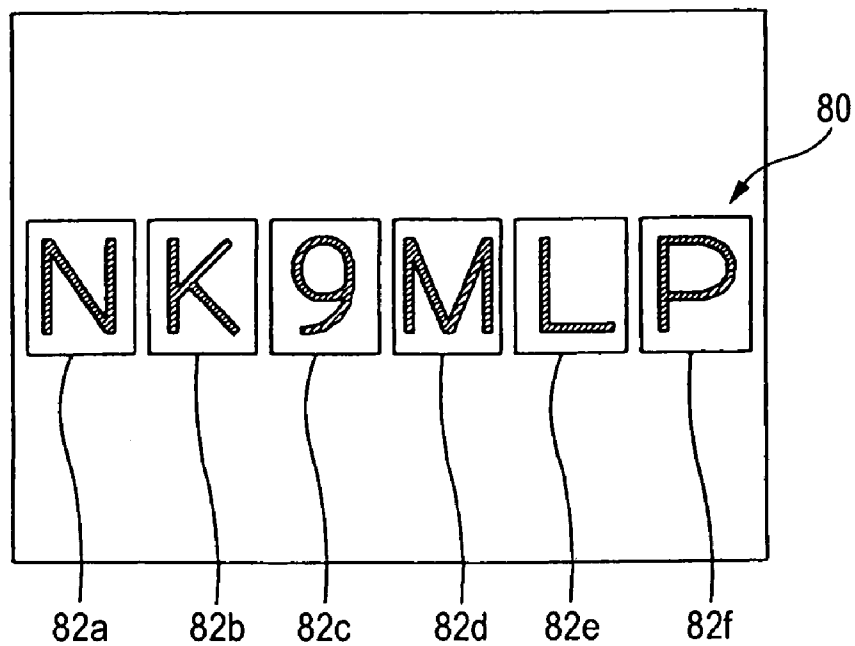


FIG. 8



U.S. Patent

Aug. 21, 2007

Sheet 8 of 8

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FIG. 9A

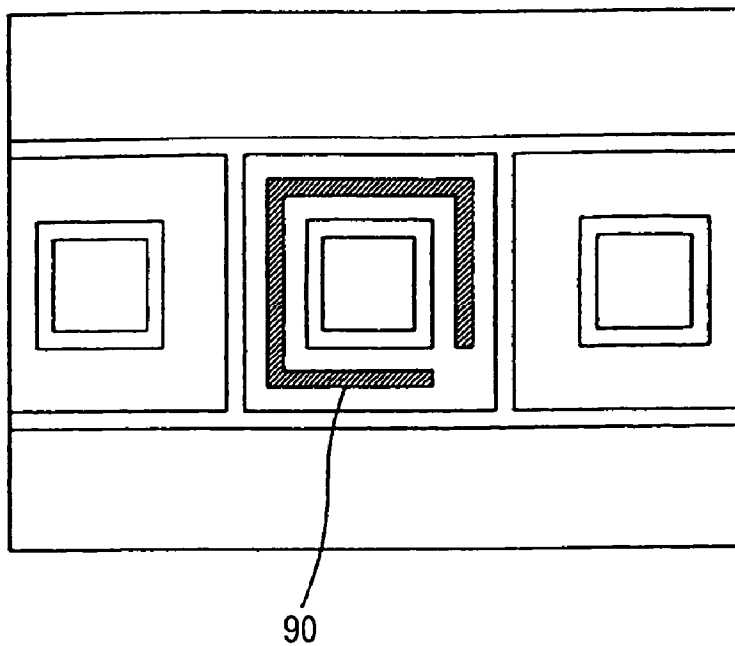
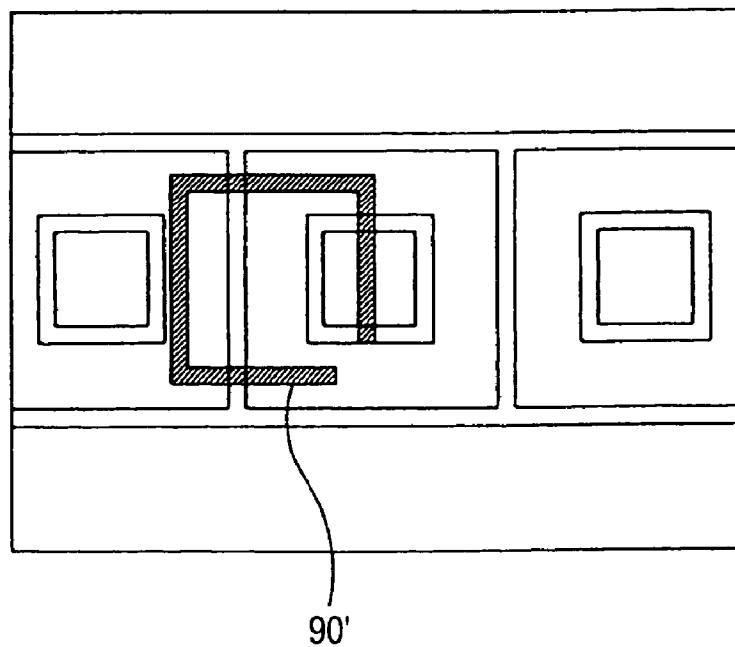


FIG. 9B



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ELECTRO-OPTICAL DEVICE, ACTIVE-MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to an electro-optical device, an active matrix substrate, and an electronic apparatus.

2. Description of Related Art

One type of driving system for a related art display having liquid-crystal elements, organic EL (electroluminescent) elements, electrophoresis elements, electron emitting elements, or the like is an active matrix drive system. An active-matrix drive system display includes a display panel that has a plurality of pixels in a matrix. The pixels have respective pixel circuits, each of which is constituted by electro-optical elements and driving transistors for supplying drive power to the electro-optical elements. The pixel circuits are arranged so as to correspond to respective intersections of data lines and scan lines (see Pamphlet of International Publication No. WO98/36407).

When the pixel circuits have different shapes and/or different pitches in the column direction (data-line direction) and the row direction (scan-line direction) of the display panel portion, directional viewing variation occurs between the column direction and the row direction of the display panel. As a result, an image displayed on the display panel portion may be distorted in the column direction (data-line direction) or the row direction (scan-line direction). In particular, for a full-color display, color irregularities occur in addition to the distortion of the image in the column and row directions. Thus, the display quality of the display is reduced.

SUMMARY OF THE INVENTION

The present invention provides an electro-optical device and an electro-optical apparatus which reduce directional viewing variation between the column and row directions. The present invention provides an active matrix substrate suitable for the electro-optical device.

An electro-optical device according to an aspect of the present invention includes a plurality of effective optical regions that are provided above a substrate and that have electro-optical elements and a wiring region that is provided on the substrate and that has wires to supply power or electric signals to the electro-optical elements. At least three of the effective optical regions are in contact with ineffective-optical regions directly or via part of the wiring region, the electro-optical elements not being provided in the ineffective-optical regions.

According to an aspect of the present invention, the effective optical regions having the electro-optical elements are arranged so as to sandwich the ineffective optical regions that have no electro-optical elements. Thus, it is possible to uniformly arrange the electro-optical elements in the column and row directions of a display. As a result, directional viewing variation that occurs between the column direction and the row direction of the display panel portion can be reduced, thereby making it possible to reduce distortion of an image.

In this electro-optical device, the plurality of effective optical regions may include a plurality of first effective optical regions in which first electro-optical elements are provided and a plurality of second effective optical regions in which second electro-optical elements are provided, and

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the ineffective optical region may be arranged so as to be sandwiched by two of the first effective optical regions and so as to be sandwiched by two of the second effective optical regions.

With this arrangement, allotting the electro-optical elements to electro-light emitting elements that emit green and blue allows the electro-optical device to display a full-color image. In such a case, it is possible to reduce color irregularities in the column and row directions of the display panel portion of the electro-optical device. As a result, for a full-color display, the generation of color irregularities can be suppressed in the column and row directions in addition to the suppression of image distortion. Thus, the display quality of the display can be enhanced.

An electro-optical device according to an aspect of the present invention includes a plurality of first effective optical regions that are provided above a substrate and that have first electro-optical elements, a plurality of second effective optical regions that are provided above the substrate and that have second electro-optical elements, and a plurality of ineffective optical regions that are provided above the substrate and that have no electro-optical elements. Each of the ineffective optical regions is arranged so as to be sandwiched by two of the first effective optical regions and so as to be sandwiched by two of the second effective optical regions.

According to an aspect of the present invention, the first electro-optical elements or the second electro-optical elements can be arranged so as to sandwich the ineffective optical regions having no electro-optical elements.

In this electro-optical device, the first effective optical regions or the second effective optical regions may not be arranged so as to be adjacent to each other.

With this arrangement, the first electro-optical elements and the second electrical elements can be arranged in regular directions and at regular intervals in the column and row directions of the display. As a result, directional viewing variation that occurs between the column direction and the row direction of the display panel portion can be reduced, thereby making it possible to reduce distortion of an image.

In this electro-optical device, the first effective optical regions and the second effective optical regions may have the same shape.

With this arrangement, the first and second electro-optical elements can be formed on the same condition, thereby making it possible to reduce coating spots during the formation of the first and second electro-optical elements.

In this electro-optical device, the ineffective optical regions may have anti-reflection members.

With this arrangement, since the anti-reflection member is provided in the ineffective optical region included in one pixel, black can be reliably displayed at one pixel and a contrast ratio can be increased.

In this electro-optical device, the first and second effective optical regions may have respective electronic circuits to drive the electro-optical elements provided in the first and second effective optical regions.

With this arrangement, the first and second electro-optical elements provided in the first and second effective optical regions are driven by the electronic circuits provided in the same effective optical regions.

In this electro-optical device, at least one of the first and second effective optical regions may have an electronic circuit to drive the electrical optical element provided in another first or second effective optical region.

With this arrangement, the electronic circuit to drive the first or second electro-optical element provided in the first or

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second effective optical region can be provided in the first or second effective optical region. As a result, the aperture ratio of pixels can be increased.

In this electro-optical device, the ineffective optical region may have an electronic circuit to drive the electro-optical elements provided in at least one of the first effective optical regions and at least one of the second effective optical regions.

With this arrangement, the individual electronic circuits to drive the first and second electro-optical elements provided in the first and second effective regions can be formed in the ineffective optical regions. As a result, the aperture ratio of pixels can be increased.

In this electro-optical device, at least one of the effective optical regions may be in contact with an ineffective optical region in which no electronic circuit is provided below an electrode provided in the effective optical region or the electrode is not provided above the electronic circuit.

With this arrangement, the ineffective optical regions and the effective optical regions can be planarized, thereby making it possible to eliminate pixel irregularities. Also, the aperture ratio in the effective optical regions can be increased, thereby making it possible to provide a display having yet lower power consumption.

This electro-optical device may further include pixels that are provided so as to correspond to respective intersections of a plurality of scan lines and a plurality of data lines. The electronic circuits may drive the electro-optical elements in accordance with scan signals from the scan lines and data signals from the data lines.

With this arrangement, it is possible to increase the display quality of the electro-optical device that drives the electro-optical elements in accordance with the scan signals from the scan lines and the data signals from the data lines.

In this electro-optical device, the electronic circuits may include first transistors to supply data signals during electrical conduction; capacitance elements to store, as an amount of charge, the data signals supplied from the first transistors; and second transistors to supply an amount of current corresponding to the electrical-conduction state to the electro-optical elements. The electrical-conduction state is controlled in accordance with the amount of charge stored by the capacitance elements.

With this arrangement, when the first transistors to supply the data signals are put into the electrical conduction states, the data signals to be supplied via the first transistors are supplied to the corresponding capacitance elements. The electrical conduction states of the second transistors are controlled based on an amount of charge in accordance with data signals stored by the capacitance elements. The second transistors supply an amount of current corresponding to the electrical conduction states to the electro-optical elements.

In this electro-optical device, the first electro-optical element and the second electro-optical element may be constituted by two electro-optical elements selected from an electro-optical element that emits green, an electro-optical element that emits blue, and an electro-optical element that emits red.

With this arrangement, it is possible to display a color image that is reduced in color irregularities in the column and row directions of the display panel portion.

In this electro-optical device, each of the first electro-optical elements and the second electro-optical elements may be an EL element.

With this arrangement, each EL element emits light so as to correspond to the conduction state of the corresponding second transistor.

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In this display panel, the EL element may have a light-emitting layer that is made of organic material.

In this case, the light-emitting layer of the EL element is constituted by an organic EL element that is made of organic material.

An electro-optical device according to an aspect of the present invention includes a plurality of first light-emitting regions that are provided above a substrate and that have first light-emitting films, a plurality of second light-emitting regions that are provided above the substrate and that have second light-emitting films, and a plurality of non-luminous regions that are provided above the substrate and that have no light-emitting films. Each of the non-luminous regions is arranged so as to be sandwiched by two of the first light-emitting regions and so as to be sandwiched by two of the second light-emitting regions.

According to an aspect of the present invention, the first light-emitting films or the second light-emitting films can be arranged so as to sandwich the non-luminous regions having no light-emitting films.

In this electro-optical device, the first light-emitting films or the second light-emitting films are not arranged so as to be adjacent to each other.

With this arrangement, the first and second light-emitting films can be arranged in regular directions and at regular intervals in the column and row directions of the display. As a result, directional viewing variation that occurs between the column direction and the row direction of the display panel portion can be reduced, thereby making it possible to reduce distortion of an image.

In this electro-optical device, the first light-emitting regions and the second light-emitting regions may have the same shape.

With this arrangement, the first and second light-emitting films can be formed on the same condition, thereby making it possible to reduce coating spots during the formation of the first and second light-emitting films.

In this electro-optical device, the non-luminous regions may have anti-reflection members.

With this arrangement, since the anti-reflection member is provided in the non-luminous region included in one pixel, black can be reliably displayed at one pixel and a contrast ratio can be increased.

In the electro-optical device, the first and second light-emitting regions may have respective electronic circuits to control light emission of the corresponding first and second light-emitting films.

With this arrangement, the first and second electro-optical elements provided in the first and second effective optical regions are driven by the electronic circuits provided in the same effective optical regions.

In this electro-optical device, at least one of the first and second light-emitting regions may have an electronic circuit to control light emission of the first or second light-emitting film provided in another first or second light-emitting region.

With this arrangement, the electronic circuit to drive the first or second light-emitting film provided in the first or second light-emitting region can be formed in the first or second light-emitting region. As a result, the aperture ratio of pixels can be increased.

In this electro-optical device, the non-luminous region may have an electronic circuit to control light emission of the first or second light-emitting film provided in at least one of the first or second light-emitting regions.

With this arrangement, the individual electronic circuits to drive the first and second light-emitting films provided in the

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first and second light-emitting regions can be formed in the non-luminous regions. As a result, the aperture ratio of pixels can be increased.

This electro-optical device may further include pixels that are provided so as to correspond to respective intersections of a plurality of scan lines and a plurality of data lines. The electronic circuits for the corresponding pixels may control light emission of the first or second light-emitting films in accordance with scan signals from the scan lines and data signals from the data lines.

With this arrangement, it is possible to increase the display quality of the electro-optical device that drive the first or second light-emitting films in accordance with the scan signals from the scan lines and the data signals from the data lines.

In this electro-optical device, the first light-emitting film and the second light-emitting film may be constituted by two light-emitting films selected from a light-emitting film that emits green, a light-emitting film that emits blue, and a light-emitting film that emits red.

With this arrangement, it is possible to display a color image that is reduced in color irregularities in the column and row directions of the display panel portion.

In this electro-optical device, each of the first and second light-emitting films may be made of organic material.

In this case, the EL element is constituted by an organic EL element the light-emitting layer of which is made of organic material.

An active matrix substrate according to an aspect of the present invention includes a plurality of element forming regions that are provided above a substrate and that have electrodes for connection with electronic elements, and a wiring region that is provided above the substrate and that has wires to supply various electrical signals to the electronic elements via the electrodes. At least three of the element forming regions are in contact with non-element-forming regions directly or via part of the wiring region, the electronic elements being not provided in the non-element-forming region.

According to an aspect of the present invention, the element forming regions are formed so as to sandwich the corresponding non-element-forming regions. Thus, it is possible to uniformly arrange the element forming regions in the column and row directions of the active matrix substrate.

An active matrix substrate according to an aspect of the present invention includes a plurality of first element forming regions that are provided above a substrate and that have first electro-optical elements, a plurality of second element forming regions that are provided above the substrate and that have second electro-optical elements, and a plurality of non-element-forming regions that are provided above the substrate and that have no electro-optical elements. Each of the non-element-forming regions may be arranged so as to be sandwiched by two of the first element forming regions and so as to be sandwiched by two of the second element forming regions.

According to an aspect of the present invention, the first element forming regions or the second element forming regions can be arranged so as to sandwich the corresponding non-element-forming regions.

In the active matrix substrate of an aspect of the present invention, the non-element-forming regions may have anti-reflection members.

In this case, since the anti-reflection members are formed in the non-element-forming regions, black can be displayed in the non-element-forming regions.

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In the active matrix substrate of an aspect of the present invention, each of the first and second element forming regions may have an electronic circuit to drive the first or second electro-optical element that is provided therein.

With this arrangement, the first and second electro-optical elements provided in the first and second effective optical regions are driven by the electronic circuits provided in the same effective optical regions.

In the active matrix substrate of an aspect of the present invention, at least one of the first element forming regions and the second element forming regions may have an electronic circuit to drive the electro-optical element that is provided in another first or second element forming region.

With this arrangement, the electronic circuit to drive the first or second light-emitting film provided in the first or second light-emitting region can be formed in the first or second light-emitting region. As a result, the aperture ratio of pixels can be increased.

In the active matrix substrate of this exemplary embodiment, the non-element-forming region may have an electronic circuit to drive the electro-optical element that is provided in at least one of the first or second element forming regions.

With this arrangement, the individual electronic circuits to drive the first and second light-emitting films provided in the first and second light-emitting regions can be formed in the non-luminous regions. As a result, the aperture ratio of pixels can be increased.

An electronic apparatus according to an aspect of the present invention includes the electro-optical device as described above.

The electro-optical device can provide an electro-optical device that is reduced in directional viewing variation between the column and row directions.

The electronic apparatus of an aspect of the present invention incorporates the active matrix substrate as described above.

This electronic apparatus, therefore, includes the active matrix substrate suitable for the electro-optical device that is reduced in directional viewing variation between the column and row directions.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a circuit block schematic illustrating the circuit configuration of a display of a first exemplary embodiment;

FIG. 2 is a circuit block schematic illustrating the internal circuit configuration of a display panel portion and a data-line drive circuit;

FIG. 3 is a circuit schematic of a pixel circuit in the first exemplary embodiment;

FIG. 4 is a partial sectional view of a display panel portion in the first exemplary embodiment;

FIG. 5 is a circuit schematic of a pixel circuit in a second exemplary embodiment;

FIG. 6 is a partial sectional view of a display panel portion in the second exemplary embodiment;

FIG. 7 is a perspective view illustrating the configuration of a mobile personal computer according to a third exemplary embodiment; and

FIG. 8 is a perspective view illustrating the configuration of a portable telephone according to the third exemplary embodiment.

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DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

First Exemplary Embodiment

A first exemplary embodiment of the present invention will now be described below with reference to FIGS. 1 to 4. FIG. 1 is a circuit block schematic illustrating the circuit configuration of a display. FIG. 2 is a circuit block schematic illustrating the internal circuit configuration of a display panel portion and a data-line drive circuit. FIG. 3 is a circuit schematic of a pixel circuit.

A display 10 includes a control circuit 11, a display panel portion 12, a scan-line drive circuit 13, and a data-line drive circuit 14. The control circuit 11, the scan-line drive circuit 13, and the data-line drive circuit 14 may be constituted by electronic components that are independent from each other. For example, the control circuit 11, the scan-line drive circuit 13, and the data-line drive circuit 14 may each be constituted by a one-chip semiconductor integrated circuit unit. Alternatively, some or all of the control circuit 11, the scan-line drive circuit 13, and the data-line drive circuit 14 may be constituted by programmable IC chips, and the functions of the circuits may be realized through software, i.e., a program written in the IC chips.

The display panel portion 12 has a display area P, where a plurality of pixel circuits 20 are arranged and formed on an active matrix substrate S. As shown in FIG. 2, in the display panel portion 12, data lines are arranged so as to extend in the column direction thereof. The data lines are constituted by data lines XG_m for green, data lines XB_m for blue, and data lines XR_m for red (m is a natural number). The green, blue, and red data lines XG_m, XB_m, and XR_m are arranged in the order of a first green data line XG₁, a first blue data line XB₁, a first red data line XR₁, a second green data line XG₂, . . . and so on from the left end of the display panel portion 12. A plurality of scan lines Y_n (n is a natural number) are also arranged so as to extend in the row direction of the display panel portion 12.

Further, the pixel circuits 20 are arranged and formed in a matrix at positions corresponding to the respective intersections of the scan lines Y_n and the green, blue, and red data lines XG_m, XB_m, and XR_m.

Each pixel circuit 20 is constituted by three types of pixel circuits, namely, a pixel circuit 20G for green, a pixel circuit 20B for blue, and a pixel circuit 20R for red. The green pixel circuit 20G has an organic EL (electroluminescent) element 21G for green. The organic EL element 21G emits green light from a light-emitting layer made of organic material. The blue pixel electrode 20B has an organic EL element 21B for blue. The organic EL element 21B emits blue light from a light-emitting layer made of organic material. The red pixel electrode 20R has an organic EL element 21R for red. The organic EL element 21R emits red light from a light-emitting layer made of organic material. A set of the green, blue, and red pixel circuits 20G, 20B, and 20R provides one pixel.

As shown in FIG. 3, in a region where each pixel circuit 20 is formed, a pixel forming region ZG for green, a pixel forming region ZB for blue, a pixel forming region ZR for red, and a dummy forming region ZS are provided in a square lattice. The green pixel forming region ZG has the green pixel circuit 20G and the organic EL element 21G therein emits green light. The blue pixel forming region ZB has the blue pixel circuit 20B and the organic EL element 21B therein emits blue light. The red pixel forming region ZR has the red pixel circuit 20R and the organic EL element

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21R therein emits red light. In the dummy forming region ZS, none of the pixel circuits 20G, 20B, and 20R is formed, but an anti-reflection member made of black polyimide or the like is formed in this exemplary embodiment. Thus, black is displayed in the dummy forming region ZS. Thus, the formation of the dummy forming regions ZS can ensure that black is displayed on the display panel portion 12. As a result, the contrast ratio of the display 10 can be enhanced.

In this exemplary embodiment, all of the green pixel forming regions ZG, the blue pixel forming regions ZB, the red pixel forming regions ZR, and the dummy forming regions ZS have the same shape. Thus, in the green pixel forming region ZG, the blue pixel forming region ZB, the red pixel forming region ZR, and the dummy forming region ZS, all of the corresponding organic EL elements 21G, 21B, and 21R can be formed on the same condition. As a result, coating spots generated during the formation of the organic EL elements 21G, 21B, and 21R can be reduced.

With regard to the arrangement of the forming regions ZG, ZB, ZR, and ZS (pixel circuits 20G, 20B, and 20R) allotted in a square lattice in this exemplary embodiment, as shown in FIGS. 2 and 3, each upper left side is allotted to the green pixel forming regions ZG, and each upper right side is allotted to the blue pixel forming region ZB. Also, each lower left side is allotted to the dummy forming region ZS and each lower right side is allotted to the red pixel forming region ZR.

That is, except for the pixel circuits 20 that are located at the top, bottom, left, and right edges, the dummy forming regions ZS of the pixel circuits 20 are arranged so as to be sandwiched by the green pixel forming regions ZG in the vertical direction (column direction). The dummy forming regions ZS are also arranged so as to be sandwiched by the red pixel forming regions ZR in the horizontal direction (row direction). The green pixel forming region ZG, the blue pixel forming region ZB, the red pixel forming region ZR, and the dummy forming region ZS, which are formed in a square lattice, constitute one pixel region. As a result, the green, blue, and red organic EL elements 21G, 21B, and 21R can be arranged in regular directions and at regular intervals in the column and row directions of the display panel portion 12. Thus, this arrangement can reduce directional viewing variation that occurs between the column direction and the row direction of the display panel portion 12, which makes it possible to suppress the distortion of an image displayed on the display panel portion 12.

As shown in FIG. 3, the green pixel circuit 20G formed in the green pixel forming region ZG in each pixel circuit 20 has a driving transistor QdG, a switching transistor Qs, and a storing capacitor Co that serves as a capacitance element. The driving transistor QdG is constituted by a p-channel FET (field effect transistor). The switching transistor Qs is constituted by an n-channel FET.

The drain of the driving transistor QdG is connected to the anode of the organic EL element 21G that emits green light, and the source of the driving transistor QdG is connected to a power-supply line LG for green. An operating voltage VG for green is applied to the power-supply line LG. The storing capacitor Co is connected between the gate and the source of the driving transistor QdG.

The gate of the switching transistor Qs in the green pixel circuit 20G is connected to the corresponding scan line Y_n. The drain of the switching transistor Qs is connected to the green data line XG_m, which is a part of data lines X_m, and the source of the switching transistor Qs is connected to the gate of the driving transistor QdG.

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Similarly, the blue pixel circuit **20B** formed in each blue pixel-forming region **ZB** has the driving transistor **QdB**, the switching transistor **Qs**, and the storing capacitor **Co**. The driving transistor **QdB** is constituted by a p-channel FET. The switching transistor **Qs** is constituted by an n-channel FET.

The drain of the driving transistor **QdB** is connected to the anode of the organic EL element **21B** that emits blue light, and the source of the driving transistor **QdB** is connected to a power-supply line **LB** for blue. An operating voltage **VB** for blue is applied to the power-supply line **LB**. The storing capacitor **Co** is connected between the gate and the source of the driving transistor **QdB**.

The gate of the switching transistor **Qs** in the blue pixel circuit **20B** is connected to the corresponding scan line **Yn**. The drain of switching transistor **Qs** is connected to the blue data line **XBm**, which is a part of the data lines **Xm**, and the source of the switching transistor **Qs** is connected to the gate of the driving transistor **QdB**.

The red pixel circuit **20R** formed in each red pixel-forming region **ZR** also has the driving transistor **QdR**, the switching transistor **Qs**, and the storing capacitor **Co**. The driving transistor **QdR** is constituted by a p-channel FET. The switching transistor **Qs** is constituted by an n-channel FET.

The drain of the driving transistor **QdR** is connected to the anode of the organic EL element **21R** that emits red light, and the source of the driving transistor **QdR** is connected to a power-supply line **LR** for red. An operating voltage **VR** for red is applied to the power-supply line **LR**. The storing capacitor **Co** is connected between the gate and the source of the driving transistor **QdR**. The other end of the storing capacitor **Co** is connected to the power-supply line **LR** for red.

The gate of the switching transistor **Qs** in the red pixel circuit **20R** is connected to the corresponding scan line **Yn**. The drain of the switching transistor **Qs** is also connected to the red data line **XRm**, which is a part of the data lines **Xm**, and the source of the switching transistor **Qs** is connected to the gate of the driving transistor **QdR**.

The active matrix substrate **S** will now be described in detail with reference to FIG. 4. FIG. 4 is a partial sectional view of the display panel portion **12** including the dummy forming regions **ZS** and the green pixel forming regions **ZG** that are arranged adjacent thereto. The partial sectional view shown in FIG. 4 corresponds to the section along the plane A-A shown in FIG. 3 in which the driving transistors **QdG**, which are included in the pixel circuits **20G** in the green pixel forming regions **ZG**, are formed. Since the blue and red pixel forming regions **ZB** and **ZR** also have structures similar to that of the green pixel forming regions **ZG**, the descriptions thereof will be omitted.

As shown in FIG. 4, the display panel portion **12** includes a substrate **Sd**, an element forming layer **DZ** that is provided above the substrate **Sd**, and green light-emitting films **LFG** and non-luminous films **NLF** which are provided on the element forming layer **DZ**. The green light-emitting films **LFG** constitute the green organic EL elements **21G**. The element forming layer **DZ** is a layer where the green pixel circuits **20G** are formed so as to correspond to the green light-emitting films **LFG**. Further, the element forming layer **DZ** is a layer where the other blue and red pixel circuits **20B** and **20R** are formed so as to correspond to blue and red light emitting films, which are not shown, as well as the green pixel circuits **20G**.

The element forming layer **DZ** has the driving transistors **QdG**, **QdB**, and **QdR**, which are included in the correspond-

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ing pixel circuits **20G**, **20B**, and **20R**. The element forming layer **DZ** has wires to electrically connect the green light-emitting films **LFG**, the blue and red light emitting films, and the driving transistors **QdG**, **QdB**, and **QdR**. The region in which the wires are formed will be referred to as a "wiring region" in this exemplary embodiment.

The substrate **Sd** is made of silicon in this exemplary embodiment. An insulating layer **31** is formed on the substrate **Sd**. The insulating layer **31** has a first insulating film **31a** and a second insulating film **31b** which are made of silicon dioxide. The pixel circuits **20R**, **20G**, and **20B** are not formed on the first insulating film **31a** below the region where the non-luminous films **NLF** are formed (i.e., the dummy forming regions **ZS**).

On the other hand, various elements that constitute the green pixel circuits **20G** are formed below the regions (i.e., the green pixel forming regions **ZG**) where the green light-emitting films **LFG** are formed. Examples of the various elements include silicon portions **T** that constitute the gates, source, and drains of the driving transistors **QdR**.

The second insulating film **31b** is formed on the silicon portions **T** and the first insulating film **31a**. On the second insulating film **31b**, gate electrodes **33G** of the driving transistors **QdR** are formed at positions opposing the silicon portions **T**. Also, on the second insulating film **31b**, drain electrodes **33D** and source electrodes **33S** are formed at positions opposing the drains and the sources of the silicon portions **T**.

A first interlayer insulating film **32a** is formed on the second insulating film **31b**. A second interlayer insulating film **32b** is formed on the first interlayer insulating film **32a**. The second interlayer insulating film **32b** includes wires **35a**, which electrically connect the corresponding drain electrode **33D** and pixel electrodes **34**, and wires **35b**, which electrically connect the source electrodes **33S**, the power supply lines **LR**, and the storing capacitors **Co**.

On the second interlayer insulating film **32b**, the pixel electrodes **34** and first banks **36a** are formed, and the first banks **36a** are made of inorganic material, and to electrically insulate the individual pixel electrodes **34** from each other. A part of each pixel electrode **34** has an opening. The non-luminous films **NLF**, which are made of black polyimide, and the green light-emitting films **LFG** are formed on the corresponding pixel electrodes **34** so as to cover the positions of the openings of the pixel electrodes **34**. The pixel electrodes **34** for the non-luminous films **NLF** are not connected to the driving transistors. The second interlayer insulating film **32b** is evenly formed in the regions where the green light-emitting films **LFG** are formed and the regions where the non-luminous films **NLF** are formed. The second interlayer insulating film **32b** is evenly formed also in the regions where the blue and red light-emitting films, not shown, other than the green light-emitting films **LFG**, are formed as in the regions where the non-luminous films **NLF** are formed. Thus, the display area **P** in which the pixel circuits **20** are arranged and formed can be planarized. As a result, color irregularities of pixels can be eliminated.

Second banks **36b**, which are made of organic material, are formed on the first banks **36a**. The second banks **36b** serve to provide isolation between the green light-emitting films **LFG** and the non-luminous films **NLF**. A first cathode layer **38a** is formed on the green light-emitting films **LFG**, the non-luminous films **NLF**, and the second banks **36b**. A second cathode layer **38b** is formed on the first cathode layer **38a**. The first and second cathode layers **38a** and **38b** constitute a cathode layer **38**. The cathode layer **38** serves as

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an opposing electrode for the pixel electrodes **34** to supply electrical current to the green light-emitting films LFG.

Thus, as described above, the regions where the green light-emitting films LFG and the blue and red light-emitting films are provided and the regions where the non-luminous films NLF are provided are evenly formed, thereby making it possible to suppress color irregularities of the pixels.

As shown in FIG. 2, the data-line drive circuit **14** includes single-line drive circuits **23G** for green, single-line drive circuits **23B** for blue, and single-line drive circuits **23R** for red for the individual data lines X_m .

Each green single-line drive circuit **23G** supplies a green data signal VDG to the corresponding green pixel circuit **20G** via the green data line X_{Gm} , which is a part of the data lines X_m , in accordance with a data control signal from the control circuit **11**. When the internal state (the amount of charge in the storing capacitor C_o) of the green pixel circuit **20G** is set in accordance with the green data signal VDG, the value of current flowing through the organic EL element **21G** is controlled correspondingly.

Each blue single-line drive circuit **23B** supplies a blue data signal VDB to the corresponding blue pixel circuit **20B** via the blue data line X_{Bm} , which is a part of the data lines X_m , in accordance with a data control signal from the control circuit **11**. When the internal state (the amount of charge in the storing capacitor C_o) of the blue pixel circuit **20B** is set in accordance with the blue data signal VDB, the value of current flowing through the organic EL element **21B** is controlled correspondingly.

Each red single-line drive circuit **23R** supplies a red data signal VDR to the corresponding red pixel circuit **20R** via the red data line X_{Rm} , which is a part of the data lines X_m , in accordance with a data control signal from the control circuit **11**. When the internal state (the amount of charge in the storing capacitor C_o) of the red pixel circuit **20R** is set in accordance with the red data signal VDR, the value of current flowing through the organic EL element **21R** is controlled correspondingly.

The scan-line drive circuit **13** appropriately selects one of the scan lines Y_1 to Y_n to select a group of pixel circuits **20** in one row. The scan-line drive circuit **13** is adapted to appropriately select one of the scan lines Y_1 to Y_n in accordance with a scan control signal from the control circuit **11** and to output a scan signal corresponding to the one line.

In turn, the switching transistors Q_s of the pixel circuits **20** (the pixel circuits **20G**, **20B**, and **20R**) that are provided on the scan line selected by the scan signal are turned on. At this point, the green, blue, and red data signals VDG, VDB, and VDR are supplied to the corresponding storing capacitors C_o via the data lines X_{Gm} , X_{Bm} , and X_{Rm} .

The control circuit **11** converts display data (image data) sent from an external device into matrix data representing tones of light emitted by each organic EL element **21**. The matrix data contains a scan control signal to specify a scan line to output the scan signal to select a group of pixel electrodes in one row and also contains a data control signal to determine the green, blue, and red data signal VDG, VDB, and VDR to set the brightness of the organic EL elements **21G**, **21B**, and **21R** of the selected group of pixel electrodes. The scan control signal is supplied to the scan-line drive circuit **13**. The data control signal is supplied to the data-line drive circuit **14**.

According to the display **10** of this exemplary embodiment, the individual scan lines Y_n are sequentially selected and the green, blue, and red data signals VDG, VDB, and VDR are supplied via the corresponding data lines X_{Gm} ,

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X_{Bm} , and X_{Rm} to the corresponding storing capacitors C_o of the pixel circuits **20** (the pixel circuits, **20G**, **20B**, and **20R**) on the selected scan lines Y_n . Correspondingly, the organic EL elements **21G**, **21B**, and **21R** of the pixel circuits **20G**, **20B**, and **20R** emit light, thereby displaying an image.

An electro-optical device recited in the claims corresponds to, for example, the display **10** in this exemplary embodiment. Also, electronic elements, a first electro-optical element, and a second electro-optical element recited in the claims correspond to, for example, two organic EL elements selected from the organic EL elements **21G**, **21B**, and **21R** in this exemplary embodiment. Further, a first effective optical region or a first light emitting region and a second effective optical region or a second light emitting region recited in the claims correspond to, for example, two pixel forming regions selected from the green, blue, and red pixel forming regions Z_G , Z_B , and Z_R in this exemplary embodiment. An ineffective optical region recited in the claims corresponds to the dummy forming region Z_S , for example, in this exemplary embodiment.

A first light-emitting film and a second light-emitting film recited in the claims correspond to, for example, two light-emitting films selected from the green light-emitting film LFG, blue light-emitting film, and red light-emitting film in this exemplary embodiment. Electronic circuits, first transistors, second transistors, and capacitance elements recited in the claims correspond to, for example, the pixel circuits **20**, the switching transistors Q_s , the green, blue, and red driving transistors Q_{dG} , Q_{dB} , Q_{dR} , and the storing capacitors C_o , respectively, in this exemplary embodiment. A substrate, first element forming regions, second element forming regions, and non-element-forming regions recited in the claims correspond to, for example, the active matrix substrate S , the green, blue, and red pixel-forming regions Z_G , Z_B , and Z_R , and the dummy forming regions Z_S , respectively, in this exemplary embodiment. Electrodes recited in the claims correspond to, for example, the pixel electrodes **34** in this exemplary embodiment.

The display **10** of this exemplary embodiment can provide the following advantages.

(1) In this exemplary embodiment, in each pixel region of the display panel portion **12**, the green pixel forming region Z_G having the green pixel circuit **20G** including the green organic EL element **21G**, is allotted to the upper left side, and the blue pixel forming region Z_B having the blue pixel circuit **20B** including the blue organic EL element **21B**, is allotted to the upper right side. Also, the dummy forming region Z_S that does not have any of the color pixel circuits but has the anti-reflection member, is allotted to the lower left side, and the red pixel forming region Z_R having the red pixel circuit **20R** including the red organic EL element **21R**, is allotted to the lower right side. Further, in the adjacent pixel circuits **20**, except for the pixel circuits **20** that are located at the top, bottom, left, and right edges, the green pixel forming regions Z_G , the blue pixel forming regions Z_B , the red pixel forming regions Z_R , and the dummy forming regions Z_S are arranged in a positional relationship in which another forming region is provided between two adjacent same-color forming regions. Thus, since two adjacent same-color organic EL elements **21G**, **21B**, and **21R** are arranged at regular intervals in the column and row directions with one forming region interposed therebetween, it is possible to reduce directional viewing variation that occurs between the column direction and the row direction of the display panel portion **12**.

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(2) In this exemplary embodiment, each dummy forming region ZS has an anti-reflection member. This can ensure that black is displayed on the display panel portion 12.

Thus, this exemplary embodiment can provide a display having a high contrast ratio compared to the known configuration.

(3) In this exemplary embodiment, all of the green pixel forming regions ZG, the blue pixel forming regions ZB, the red pixel forming regions ZR, and the dummy forming regions ZS have the same shape. Thus, it is possible to reduce coating spots that result from the formation of the organic EL elements 21G, 21B, and 21R in the corresponding green pixel forming region ZG, the blue pixel forming regions ZB, and the red pixel forming regions ZR.

(4) In this exemplary embodiment, in the active matrix substrate S, the regions where the green light-emitting film LFG and the blue and red light-emitting films are provided and the regions where the non-luminous films NLF are provided are evenly formed. As a result, color irregularities of the pixel electrodes can be reduced.

Second Exemplary Embodiment

A second exemplary embodiment of the present invention will now be described below with reference to FIG. 5. The second exemplary embodiment is analogous to the first exemplary embodiment except that the formation positions of the pixel circuits 20G, 20B, and 20R in the first exemplary embodiment are different. Thus, in the second exemplary embodiment, the same members as those in the first exemplary embodiment are denoted with the same reference characters and detailed descriptions thereof will be omitted.

FIG. 5 is a circuit schematic of pixel circuits 30 that are formed at positions corresponding to the intersections of the scan lines Yn and the green, blue, and red data lines XGm, XBm, and XRM. Each pixel circuit 30 includes four forming regions, i.e., a green pixel forming region ZG, a blue pixel forming region ZB, a red pixel forming region ZR, and a dummy forming region ZS.

In the green pixel forming region ZG, a green organic EL element 21G is arranged and formed. In the dummy forming region ZS, a green pixel circuit 20G, which includes a switching transistor Qs, a storing capacitor Co, and a green driving transistor QdG, except for the green organic EL element 21G, is formed. In the blue pixel forming region ZB, a blue organic EL element 21B is formed. In the red pixel forming region ZR, a red pixel circuit 20B, which includes a switching transistor Qs, a storing capacitor Co, and a red driving transistor QdR, except for the red organic EL element 21B, is formed.

Thus, the aperture ratios in the green pixel forming region ZG and the blue pixel forming region ZB can be increased.

In the red pixel forming region ZR, a red organic EL element 21R is formed. The blue circuit 20B, except for the blue organic EL element 21B, is formed in the red pixel forming region ZR.

In the dummy forming region ZS, the green pixel circuit 20G, except for the green organic EL element 21G is formed. Further, in the dummy forming region ZS, a red pixel circuit 20R, which includes a switching transistor Qs, a storing capacitor Co, and a red driving transistor QdR, except for the red organic EL element 21R, is formed.

In the dummy forming region ZS, an anti-reflection member made of black polyimide or the like is provided. Thus, the dummy forming region ZS displays black in the same manner as the first exemplary embodiment.

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That is, except for the pixel circuits 30 that are located at the top, bottom, left, and right edges of the display panel portion 12, the green pixel forming regions ZG, the blue pixel forming regions ZB, the red pixel forming regions ZR, and the dummy forming regions ZS of the pixel circuits 30 are formed in a matrix in a positional relationship in which another forming region is provided between two same-color forming regions. Thus, two same-color organic EL elements 21G, 21B, and 21R are formed at positions apart from each other with one forming region interposed therebetween at regular intervals in the vertical and horizontal directions.

The structure of the active matrix substrate S in the second exemplary embodiment will now be described with reference to FIG. 6. FIG. 6 is a partial sectional view of the display panel portion 12 including the dummy forming region ZS and the green pixel forming region ZG that is arranged adjacent thereto. The partial sectional view shown in FIG. 6 corresponds to the section along the plane B-B shown in FIG. 5 in which two driving transistors QdG and QdR, which are included in the green and red pixel circuits 20G and 20R, are formed.

As shown in FIG. 6, the display panel portion 12 includes a substrate Sd, a green light-emitting film LFG and a non-luminous film NLF which are formed above the substrate, and an element forming layer DZ formed between the substrate Sd and the green light-emitting film LFG and the non-luminous film NLF. The element forming layer DZ has the pixel circuit 20R, 20G, and 20B. As in the first exemplary embodiment, the element forming layer DZ has the driving transistors QdG, QdB, and QdR, which are included in the corresponding pixel circuits 20G, 20B, and 20R. The element forming layer DZ has wires to electrically connect the green light-emitting film LFG, the blue and red light emitting films, and the driving transistors QdG, QdB, and QdR. The region in which the wires are formed will be referred to as a "wiring region" in this exemplary embodiment as well.

An insulating layer 31 is formed on the substrate Sd. The insulating layer 31 includes a first insulating film 31a and a second insulating film 31b which are made of silicon dioxide. On the first insulating film 31a, silicon portions T are formed below the position where the non-luminous film NLF is formed. The silicon portions T constitute the corresponding gates, sources, drains of the driving transistors QdG and QdR included in the green pixel circuit 20G and the red pixel circuit 20R. The second insulating film 31b is formed on the silicon portions T and the first insulating film 31a. On the second insulating film 31b, the gate electrodes 33G of the driving transistors QdG and QdR are formed at positions opposing the silicon portions T. Also, drain electrodes 33D and source electrodes 33S are formed at positions corresponding to the drains and the sources of the respective silicon portions T.

A first interlayer insulating film 32a is formed on the second insulating film 31b. A second interlayer insulating film 32b is formed on the first interlayer insulating film 32a. The second interlayer insulating film 32b includes wires 35a, which electrically connect the drain electrodes 33D and pixel electrodes 34, and wires 35b, which electrically connect the source electrodes 33S, the power supply lines LR, and the storing capacitors Co.

On the second interlayer insulating film 32b, first banks 36a, which are made of inorganic material, are formed between the pixel electrodes 34 to provide electrical insulations between the pixel electrodes 34. A part of each pixel electrode 34 has an opening. The light-emitting films LFG and the non-luminous films NLF are formed on the corre-

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sponding pixel electrodes **34** so as to cover the positions of the openings of the pixel electrodes **34**. Second banks **36b**, which are made of organic material, are formed on the first banks **36a**. The second banks **36b** serve to provide isolations between the green light-emitting films LFG and the non-luminous films NLF. A cathode layer **38a** is formed on the green light-emitting films LFG, the non-luminous films NLF, and the second banks **36b**. A second cathode layer **38b** is formed on the first cathode layer **38a**. The first and second cathode layers **38a** and **38b** constitute a cathode layer **38**. This cathode layer **38** serves as an opposing electrode for the pixel electrodes **34** to supply electrical current to the green light-emitting films LFG.

Thus, the regions where the green light-emitting films LFG are provided and the regions where the non-luminous films NLF are provided can be planarized. As a result, color irregularities of the pixels can be reduced.

Thus, in addition to the advantages of the first exemplary embodiment, the second exemplary embodiment can increase the aperture ratios in the red pixel forming region ZR and the blue pixel forming region ZB compared to the known configuration. As a result, a display having reduced power consumption can be provided.

Further, the formation of the pixel elements, which control the green and red organic EL elements **21G** and **21R**, in the dummy forming region ZS can reduce the area of the pixel circuit **30**. Thus, a high-definition display can be provided.

Third Exemplary Embodiment

An electronic apparatus incorporating the display **10**, which serves as an electro-optical device and which is described in the first or second exemplary embodiments, will now be described with reference to FIGS. **7** and **8**. The display **10** is applicable to various electronic apparatuses, such as mobile personal computers, portable telephones, and digital cameras.

FIG. **7** is a perspective view of the configuration of a mobile personal computer. Referring to FIG. **7**, a personal computer **50** includes a main unit **52**, which has a keyboard **51**, and a display unit **53**, which incorporates the display **10**. In this case, the display unit **53** incorporating the display **10** provides the same advantages as the exemplary embodiments described above. As a result, it is possible to provide a mobile personal computer **50** having the display **10** that is reduced in color irregularities, high in contrast, superior in display quality, and low in power consumption compared to a known personal computer.

FIG. **8** is a perspective view of the configuration of a portable telephone. Referring to FIG. **8**, a portable telephone **60** includes a plurality of operation buttons **61**, an earpiece **62**, a mouthpiece **63**, and a display unit **64** that incorporates the display **10**. In this case as well, the display unit **64** incorporating the display **10** provides the same advantages as the exemplary embodiments described above. As a result, it is possible to provide a portable telephone **60** having the display **10** that is reduced in color irregularities, high in contrast, and superior in display quality compared to a known portable telephone.

The present invention is not limited to the above-described exemplary embodiments.

For example, in the illustrated exemplary embodiments, the green pixel forming region ZG and the blue pixel forming region ZB are allotted to the upper left side and the upper right side of the display panel portion **12**, respectively. Further, the dummy forming region ZS and the red pixel

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forming region ZR are allotted to the lower left side and the lower right side, respectively. Instead, for example, the red pixel forming region ZR and the green pixel forming region ZG may be allotted to the upper left side and the upper right side of the display panel portion **12**, respectively. Further, the dummy forming region ZS and the blue pixel forming region ZB may be allotted to the lower left side and the lower right side, respectively.

That is, the formation positions of the green pixel-forming regions ZG, the blue pixel-forming regions ZB, the dummy forming regions ZS, and the red pixel-forming regions ZR which constitute the pixel circuits **20** are not limited. Thus, any arrangement may be used as long as two adjacent same-color organic elements **21G**, **21B**, and **21R** are arranged at regular intervals in the vertical and horizontal directions with one forming region interposed therebetween.

In the second exemplary embodiment, the driving transistors QdG and QdR to control the green and red organic EL elements, the storing capacitors Co, and the switching transistors Qs are formed in the dummy forming regions ZS. Also, the driving transistors QdB to control the blue organic EL elements **21B**, the storing capacitors Co, and the switching transistors Qs are formed in the red pixel-forming regions ZR.

Instead, the driving transistors, QdG, QdB and QdR to control the green, blue, and red organic EL elements **21G**, **21B**, and **21R**, the storing capacitors Co, and the switching transistors Qs may be formed in the dummy forming regions ZS. With this arrangement, it is possible to further increase the aperture ratios in the green pixel-forming regions ZG, the blue pixel-forming regions ZB, the dummy forming regions ZS, and the red pixel-forming regions ZR. As a result, a display having reduced power consumption can be provided.

In the above exemplary embodiments, although the driving transistors QdG, QdB, and QdR are each constituted by a p-channel FET and the switching transistors Qs are each constituted by a p-channel FET, the present invention is not limited thereto. For example, the driving transistors QdG, QdB, and QdR and the switching transistors Qs may be each constituted by a p-channel FET.

In the above exemplary embodiments, although the pixel circuits **20** and **30** are embodied as electronic circuits to provide preferable advantages, they may be embodied as electronic circuits to drive electro-optical elements, for example, light-emitting elements, such as LED or FED, other than the organic EL elements **21G**, **21B**, and **21R**.

In the above exemplary embodiments, the electro-optical elements of the pixel circuits **20** are embodied as the organic EL elements **21G**, **21B**, and **21R**, they may be embodied as inorganic EL elements. That is, the electro-optical elements may be applied to an inorganic EL display having inorganic EL elements.

What is claimed is:

1. An electro-optical device comprising:

a substrate;

a plurality of effective optical regions and a plurality of ineffective-optical regions provided in a square lattice above the substrate, the square lattice having a column direction and a row direction;

electro-optical elements provided in the effective optical regions and not provided in the ineffective-optical regions;

a wiring region provided on the substrate, wires to supply power or electric signals to the electro-optical elements being provided in the wiring region; and

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a plurality of first effective optical regions in which first electro-optical elements are provided; and
 a plurality of second effective optical regions in which second electro-optical elements are provided,
 wherein the ineffective optical regions are arranged on the lattice so as to be sandwiched between the first effective optical regions in the column direction and sandwiched between the second effective optical regions in the row direction.

2. An electronic apparatus, comprising:
 the electro-optical device according to claim 1.

3. An electro-optical device comprising:
 a substrate;
 a plurality of first effective optical regions provided above the substrate, first electro-optical elements being provided in the first effective optical regions;
 a plurality of second effective optical regions provided above the substrate, second electro-optical elements being provided in the second effective optical regions; and
 a plurality of ineffective optical regions provided above the substrate, no electro-optical elements being provided in the ineffective optical regions,
 each of the whole ineffective optical regions being arranged so as to be sandwiched by two of the first effective optical regions and so as to be sandwiched by two of the second effective optical regions.

4. The electro-optical device according to claim 3, wherein the first effective optical regions are not adjacent to each other.

5. The electro-optical device according to claim 3, the first effective optical regions and the second effective optical regions having the same shape.

6. The electro-optical device according to claim 3, the ineffective optical regions having anti-reflection members.

7. The electro-optical device according to claim 3, the first and second effective optical regions having respective electronic circuits to drive the electro-optical elements provided in the first and second effective optical regions.

8. The electro-optical device according to claim 7, at least one of the effective optical regions being in contact with an ineffective optical region in which no electronic circuit is provided below an electrode provided in the effective optical region or the electrode is not provided above the electronic circuit.

9. An electro-optical device according to claim 7, further comprising:
 pixels provided so as to correspond to respective intersections of a plurality of scan lines and a plurality of data lines, the electronic circuits driving the electro-optical elements in accordance with scan signals from the scan lines and data signals from the data lines.

10. The electro-optical device according to claim 9, the electronic circuits comprising:
 first transistors to supply data signals during electrical conduction;
 capacitance elements to store, as an amount of charge, the data signals supplied from the first transistors; and
 second transistors to supply an amount of current corresponding to the electrical-conduction state to the electro-optical elements, the electrical-conduction state being controlled in accordance with the amount of charge stored by the capacitance elements.

11. The electro-optical device according to claim 3, at least one of the first optical regions and at least one of the second optical regions having respective electronic circuits

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to drive the electro-optical elements provided in another first effective optical region and another effective optical region.

12. The electro-optical device according to claim 3, the ineffective optical regions having electronic circuits to drive the electro-optical elements provided in at least one of the first effective optical regions and at least one of the second effective optical regions.

13. The electro-optical device according to claim 3, the first electro-optical element and the second electro-optical element including two electro-optical elements selected from an electro-optical element that emits green, an electro-optical element that emits blue, and an electro-optical element that emits red.

14. The electro-optical device according to claim 3, each of the first electro-optical elements and the second electro-optical elements being an electroluminescent element.

15. The electro-optical device according to claim 14, the electroluminescent element having a light-emitting layer that includes organic material.

16. The electro-optical device according to claim 3, wherein the second effective optical regions are not arranged so as to be adjacent to each other.

17. The electro-optical device according to claim 3, each of the first effective optical regions in which the first electro-optical elements are provided being arranged at regular intervals in a column and row directions of a display area.

18. An electro-optical device, comprising:
 a substrate;
 a plurality of first light-emitting regions provided above the substrate, first light-emitting films being provided in the first light-emitting regions;
 a plurality of second light-emitting regions provided above the substrate, second light-emitting films being provided in the second light emitting regions; and
 a plurality of non-luminous regions provided above the substrate, no light-emitting films being provided in the non-luminous regions,
 each of the whole non-luminous regions is arranged so as to be sandwiched by two of the first light-emitting regions and so as to be sandwiched by two of the second light-emitting regions.

19. The electro-optical device according to claim 18, wherein the first light-emitting films are not adjacent to each other.

20. The electro-optical device according to claim 18, the first light-emitting regions and the second light-emitting regions having the same shape.

21. The electro-optical device according to claim 18, the non-luminous regions having anti-reflection members.

22. The electro-optical device according to claim 18, the first and second light-emitting regions having respective electronic circuits to control light emission of the corresponding first and second light-emitting films.

23. The electro-optical device according to claim 18, at least one of the first and second light-emitting regions having an electronic circuit to control light emission of the first or second light-emitting film provided in another first or second light-emitting region.

24. The electro-optical device according to claim 18, the non-luminous region has an electronic circuit to control light emission of the first or second light-emitting film provided in at least one of the first and second light-emitting regions.

25. The electro-optical device according to claim 18, further comprising:
 pixels provided so as to correspond to respective intersections of a plurality of scan lines and a plurality of

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data lines, the electronic circuits for the corresponding pixels controlling light emission of the first or second light-emitting films in accordance with scan signals from the scan lines and data signals from the data lines.

26. The electro-optical device according to claim 18, the first light-emitting film and the second light-emitting film include two light-emitting films selected from a light-emitting film that emits green, a light-emitting film that emits blue, and a light-emitting film that emits red.

27. The electro-optical device according to claim 18, each of the first and second light-emitting films includes organic material.

28. The electro-optical device according to claim 18, wherein the second light-emitting films are arranged so as to not be adjacent to each other.

29. The electro-optical device according to claim 18, each of the first light-emitting regions in which the first light-emitting films are provided being arranged at regular intervals in a column and row directions of a display area.

30. An active matrix substrate comprising:
a substrate;

a plurality of element forming regions and non-element forming regions provided in a square lattice above the substrate, the element forming regions having electrodes to connect with electronic elements, the electronic elements not being provided in the non-element forming regions, and the lattice having a column direction and a row direction; and

a wiring region provided above the substrate, wires to supply various electrical signals to the electronic elements via the electrodes being provided in the wiring region,

wherein the ineffective optical regions are arranged on the lattice so each ineffective region is sandwiched between a pair of first effective optical regions in the column direction and sandwiched between a pair of second effective optical regions in the row direction.

31. The active matrix substrate according to claim 30, the non-element forming regions having anti-reflection members.

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32. An electronic apparatus, comprising:

the active matrix substrate according to claim 26.

33. An active matrix substrate comprising:
a substrate;

a plurality of first element forming regions provided above the substrate, first electro-optical elements being provided in the first element forming regions;

a plurality of second element forming regions provided above the substrate, second electro-optical elements being provided in the second element forming regions; and

a plurality of non-element-forming regions provided above the substrate, no electro-optical elements being provided in the non-element-forming regions,

each of the whole non-element-forming regions being arranged so as to be sandwiched by two of the first element forming regions and so as to be sandwiched by two of the second element forming regions.

34. The active matrix substrate according to claim 33, each of the first and second element forming regions has an electronic circuit to drive the first or second electro-optical element that is provided therein.

35. The active matrix substrate according to claim 33, at least one of the first and second element forming regions has an electronic circuit to drive the electro-optical element that is provided in another first or second element forming region.

36. The active matrix substrate according to claim 33, the non-element-forming region having an electronic circuit to drive the electro-optical element that is provided in at least one of the first and second element forming regions.

37. The active matrix substrate according to claim 33, each of the first element forming regions in which the first electro-optical elements are provided being arranged at regular intervals in a column and row directions of a display area.

* * * * *

Exhibit 2



US008164267B2

(12) **United States Patent**
Matsueda et al.

(10) **Patent No.:** **US 8,164,267 B2**
(45) **Date of Patent:** **Apr. 24, 2012**

(54) **ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS**

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(73) Assignee: **Seiko Epson Corporation**, Tokyo (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 376 days.

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(21) Appl. No.: **12/219,592**

(22) Filed: **Jul. 24, 2008**

(65) **Prior Publication Data**

US 2008/0290807 A1 Nov. 27, 2008

Related U.S. Application Data

(63) Continuation of application No. 10/676,067, filed on Oct. 2, 2003, now abandoned.

(30) **Foreign Application Priority Data**

Oct. 7, 2002 (JP) 2002-293696

(51) **Int. Cl.**

H01J 1/62 (2006.01)

(52) **U.S. Cl.** **315/169.3; 257/72; 257/99; 313/506**

(58) **Field of Classification Search** 315/160, 315/161, 167, 169.2, 169.3; 313/483, 505, 313/506, 306; 257/40, 72, 98, 99
See application file for complete search history.

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Primary Examiner — Thuy Vinh Tran

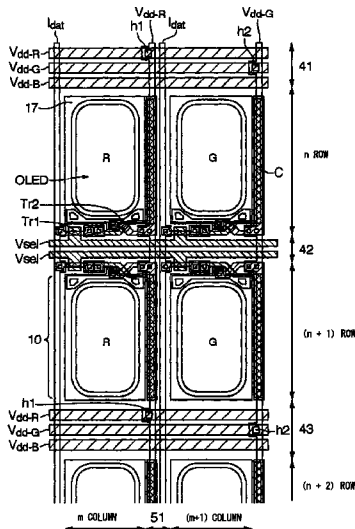
(74) *Attorney, Agent, or Firm* — Oliff & Berridge, PLC

(57)

ABSTRACT

To provide a wiring layout of electric power lines, which improves the aperture ratio of the pixel while forming pixels with the same pixel pitch. An electric-optical apparatus according to the present invention comprises multiple pixels (10) arranged in matrix including electro-optical devices driven by receiving electric power from an electric power supply circuit, wherein the aforementioned multiple pixels (10) make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and any of line forming regions (31, 32, 33, 34) is disposed between adjacent pixel groups of the aforementioned pixel groups, wherein the aforementioned line forming regions (31, 32, 33, 34) are formed with generally the same width.

7 Claims, 7 Drawing Sheets



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Fig. 1

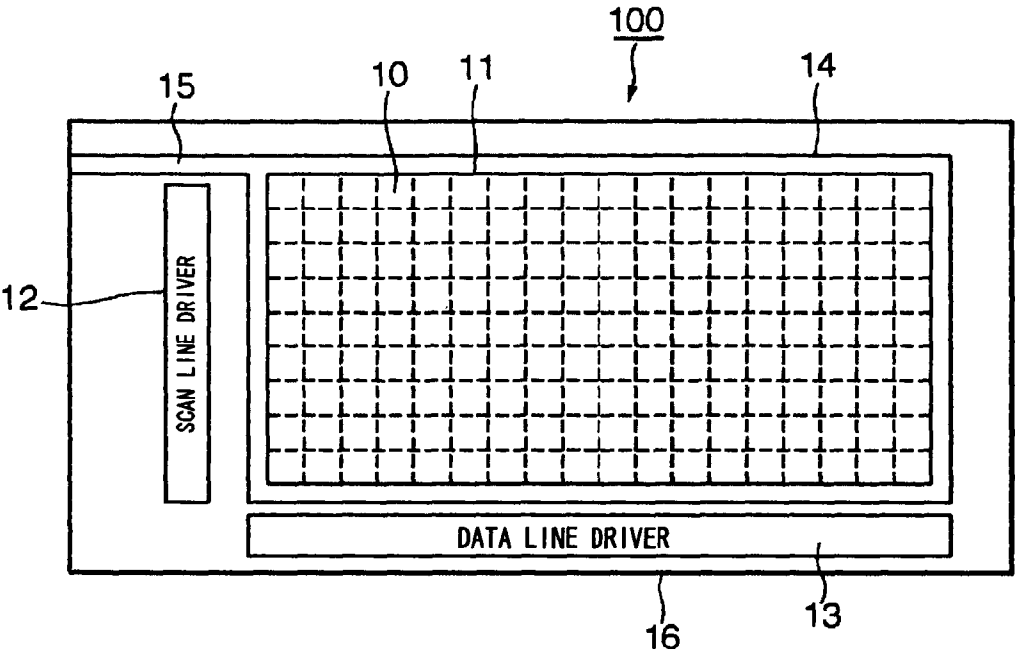
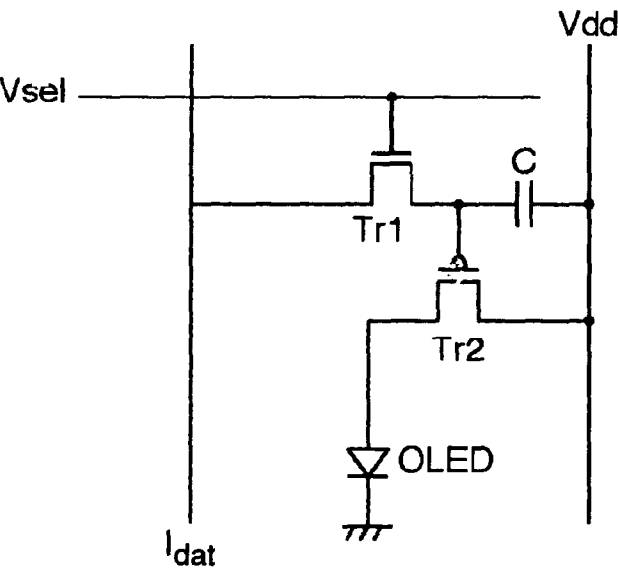
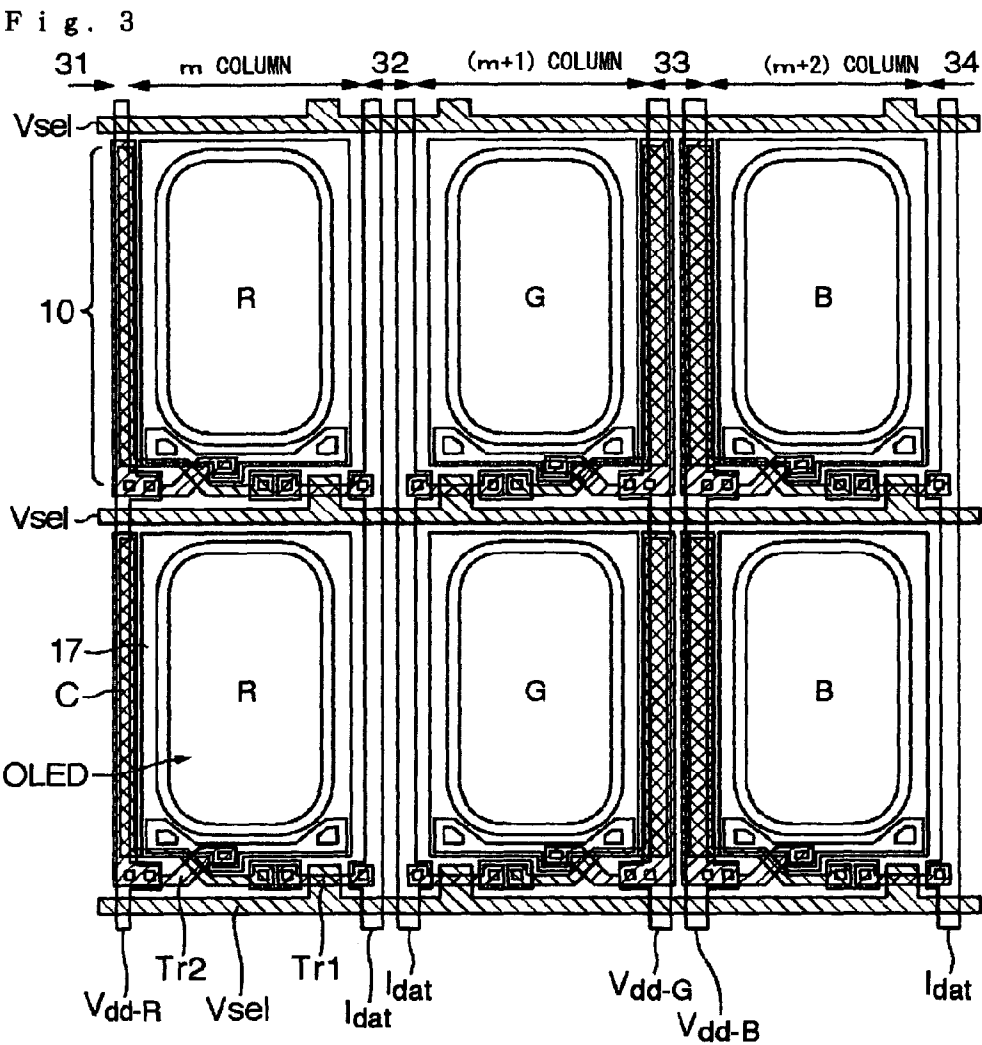


Fig. 2





F i g . 4

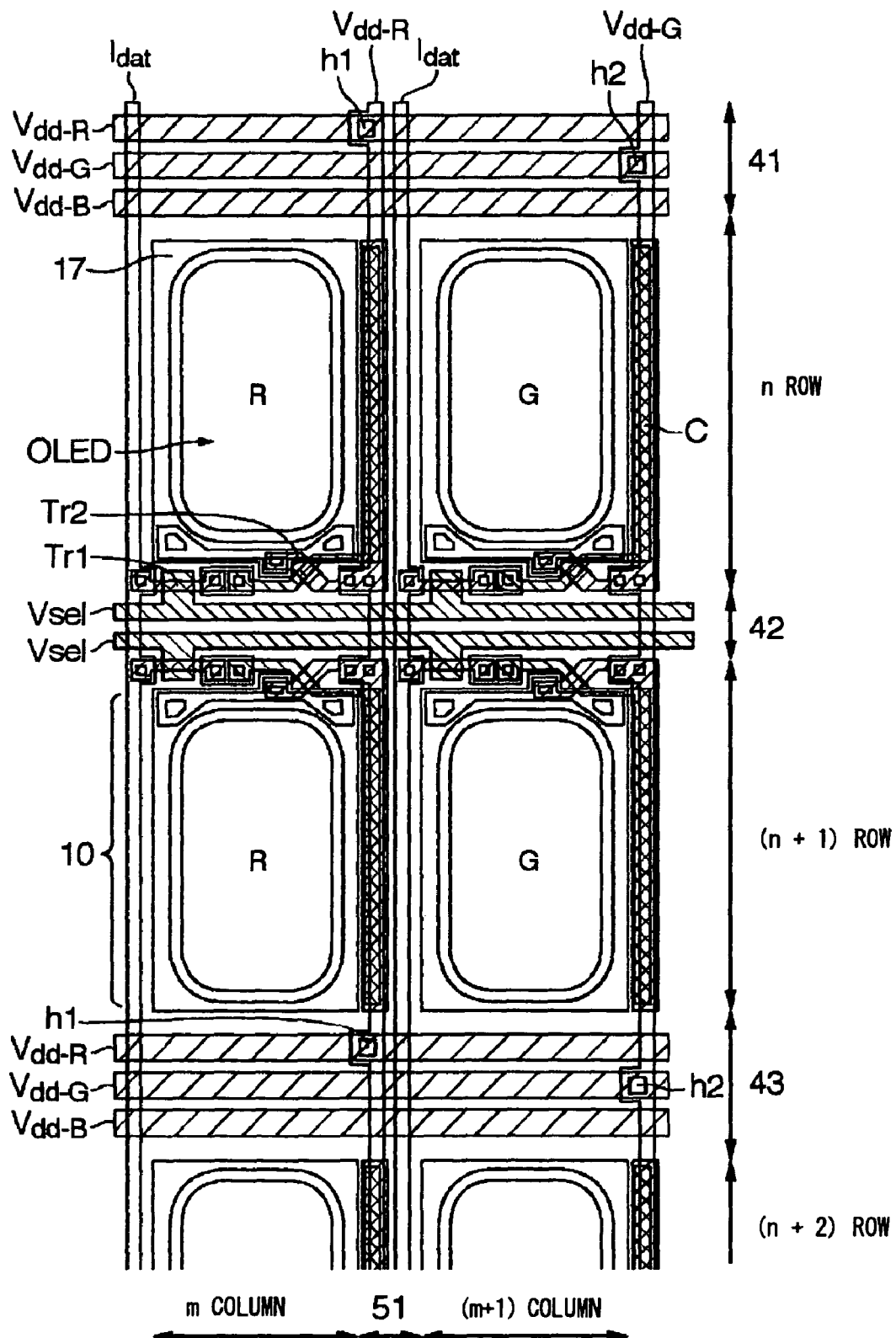
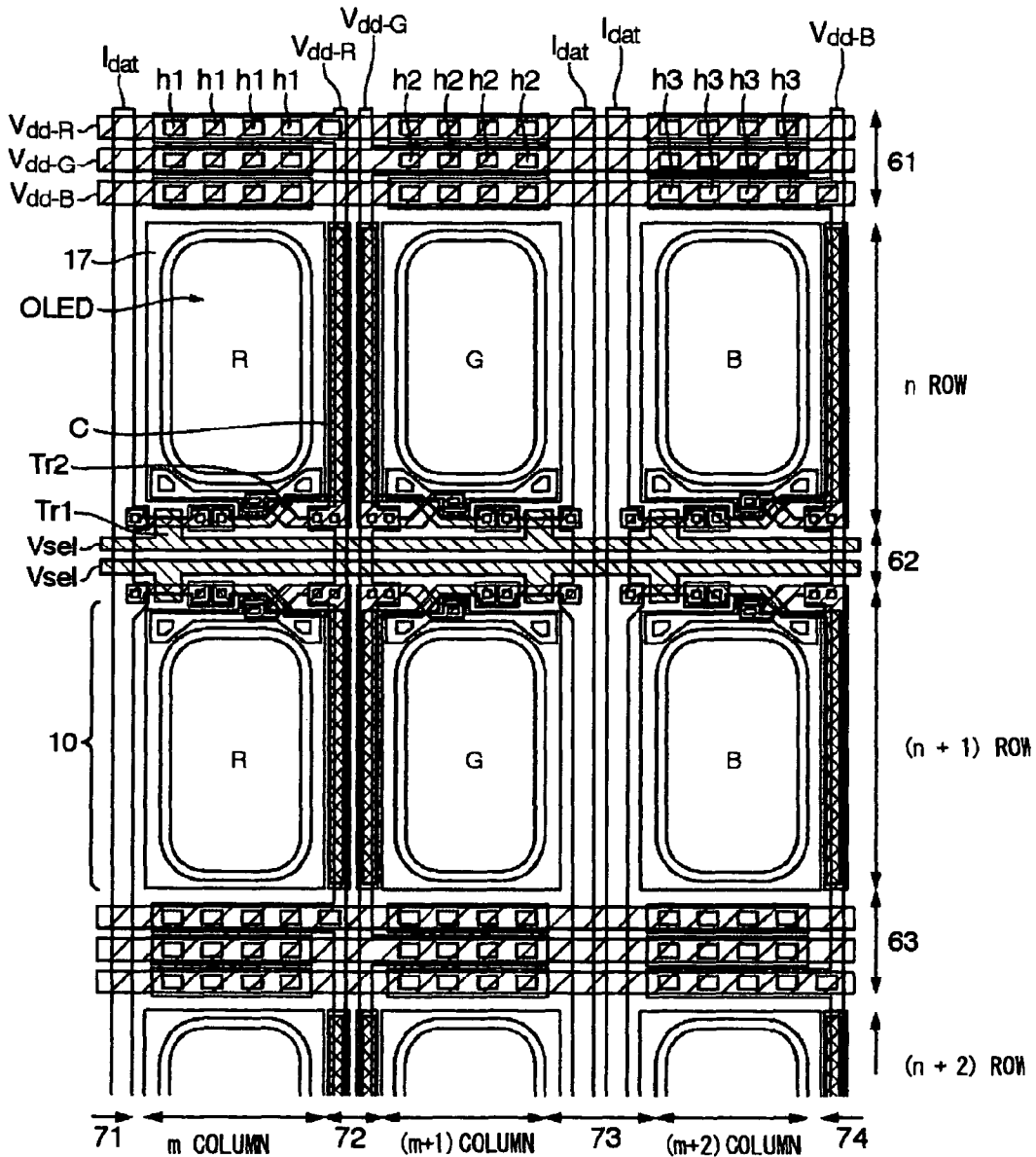


Fig. 5



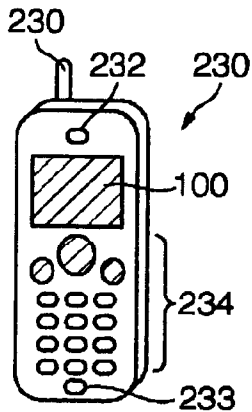


Fig. 6 A

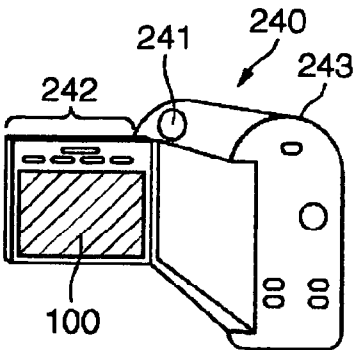


Fig. 6 B

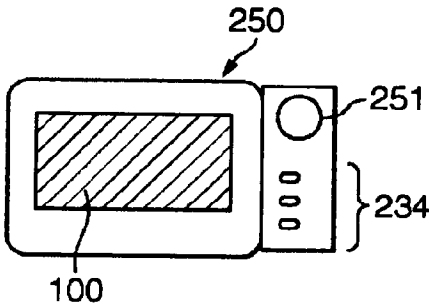


Fig. 6 C

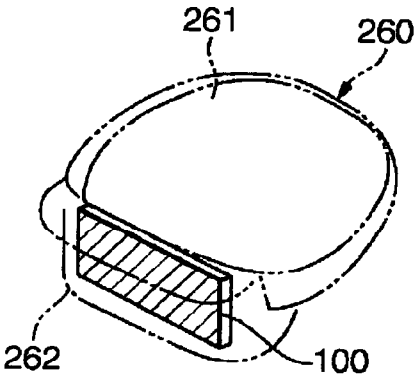


Fig. 6 D

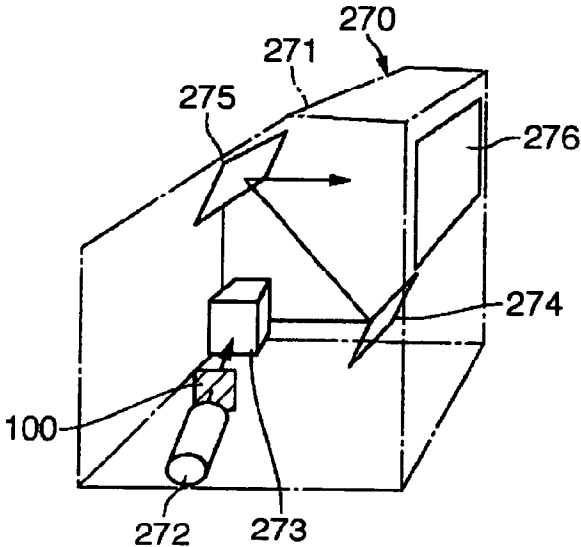


Fig. 6 E

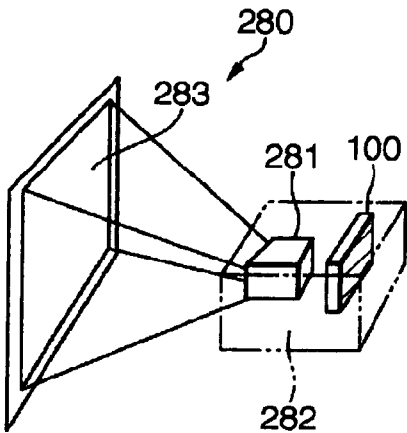
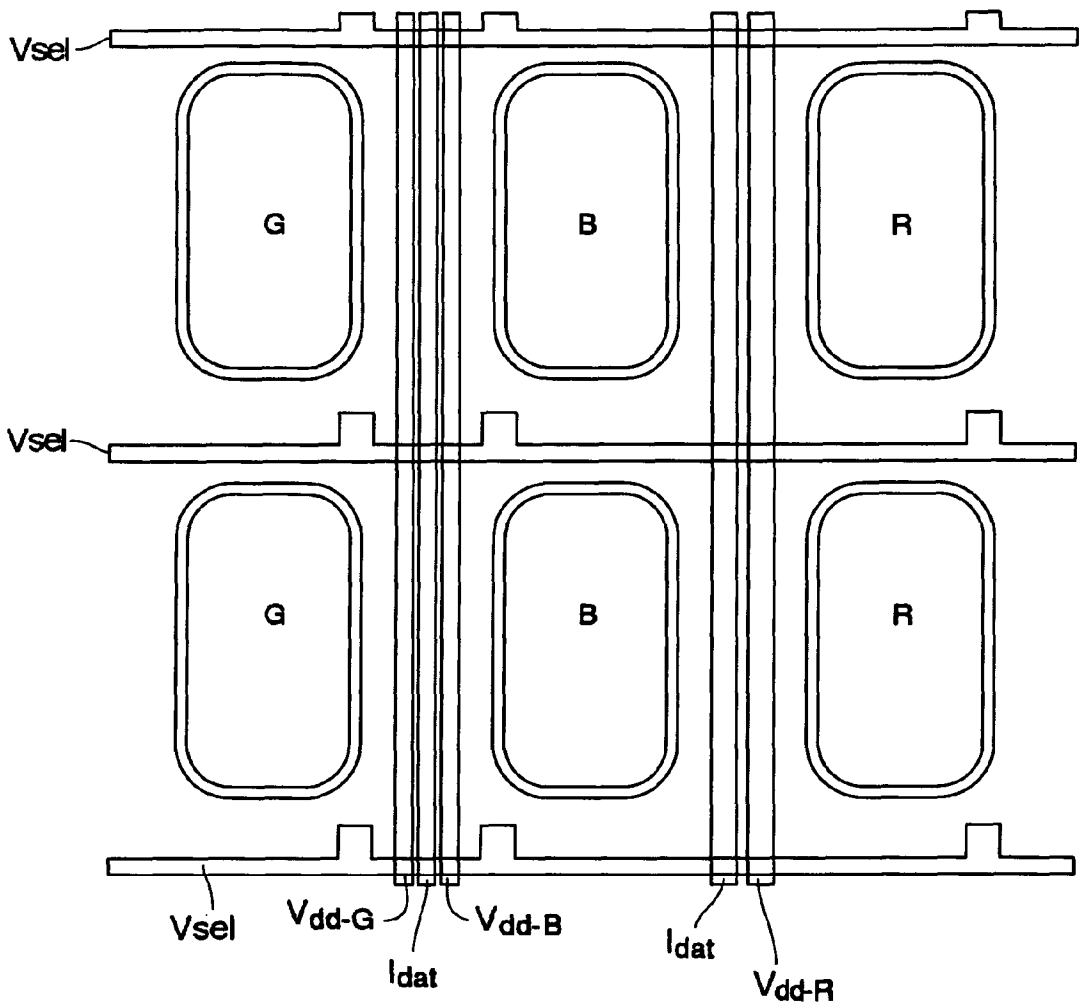


Fig. 6 F

Fig. 7



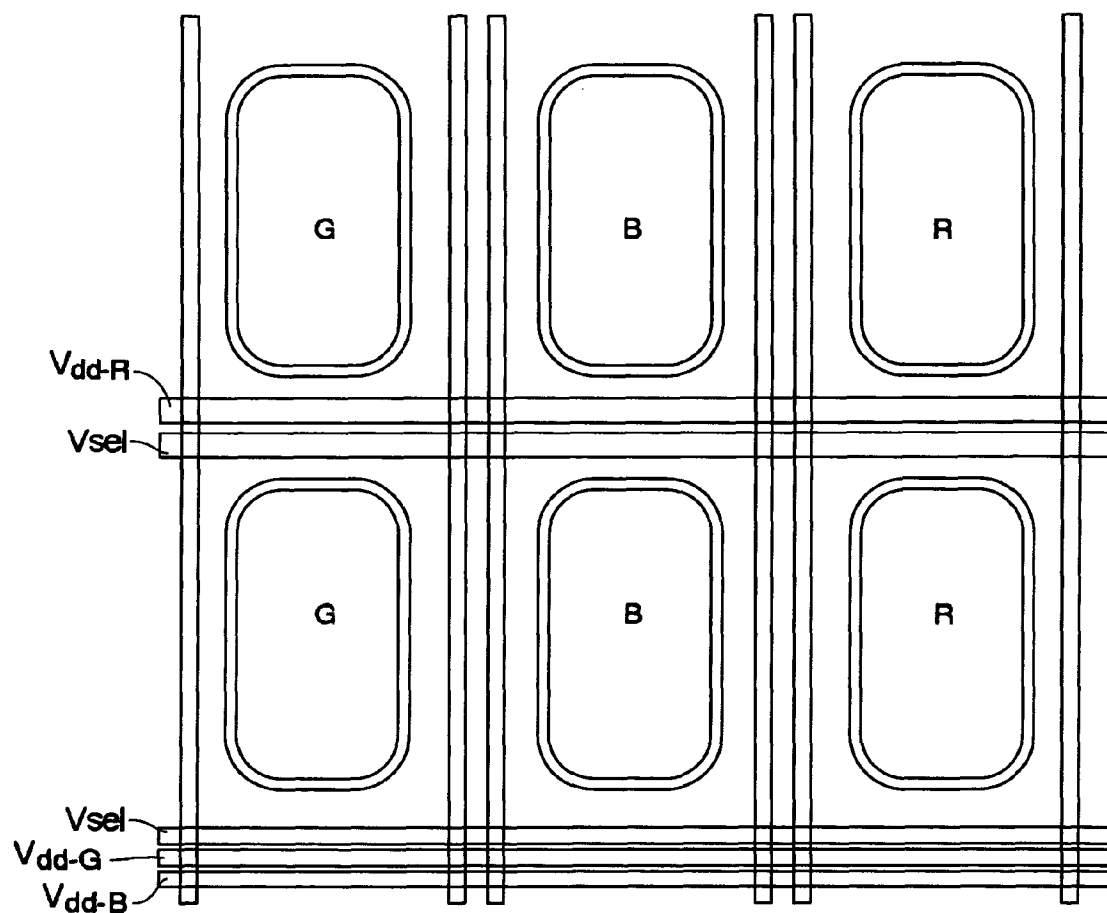
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Fig. 8



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ELECTRO-OPTICAL DEVICE, MATRIX SUBSTRATE, AND ELECTRONIC APPARATUS

This is a Continuation of application Ser. No. 10/676,067 filed Oct. 2, 2003 which was abandoned. The disclosure of the prior application is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to a wiring layout suitable for an electro-optical device including electro-optical devices.

2. Description of Related Art

Organic EL devices are current-driven self-light-emitting devices, and accordingly, there are an advantage of no need to provide a backlight, as well as other advantages such as low power consumption, a wide range of vision, and a high contrast ratio, so there is high expectation for development of flat panel displays employing EL devices. The organic EL device is an electro-optical device including a light-emission layer introduced between an anode and a cathode, wherein, upon supplying forward bias current between both the electrodes, self-light-emission is effected due to the recombination energy at the time of recombination of a hole injected from the anode and an electron injected from the cathode. Accordingly, a supply of electric power from an external circuit is required in order to cause the organic EL device to emit light.

With conventional color-display active-matrix-driven display panels, an M number each of electric power lines and data lines are disposed in the column direction on a pixel matrix with an N number of columns and an M number of rows formed on a pixel region, as well as an N number of selection lines being disposed in the row direction on the aforementioned matrix. With a given pixel of such a wiring layout, a data line is disposed between the given pixel and the left-adjacent pixel, and an electric power line is disposed between the given pixel and the right-adjacent pixel. That is to say, with the lines disposed between adjacent pixels in the column direction, a layout is formed so that one data line and one electric line make up one pair. With the above-described configuration, disposed at an intersection of a scan line and a data line are: a switching transistor, a holding capacitance, a driving transistor, and an organic EL device for emitting light in one color of the RGB three primary colors, and these devices make up a pixel.

SUMMARY OF THE INVENTION

With the conventional arrangements, a light-emission layer is formed of a material corresponding to each color of the RGB three primary colors, and accordingly, the organic EL device is operated with greatly different power consumption corresponding to each color, so the optimal width of the electric power line is greatly different for each color. Accordingly, with the above-described wiring layout, while there is the need to determine the pixel pitch according to the maximal width for disposing the electric power lines, there is the need to form a pixel matrix with the same pixel pitch due to the restriction from the manufacturing process for a display, and accordingly, there is the need to determine the pixel layout at the sacrifice of the aperture ratio. On the other hand, in the event of reducing the aperture ratio, there is the need to increase the amount of electric current supplied to the organic EL device for obtaining predetermined luminance, and accordingly, there is the need to form the electric power line

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with a greater width, leading to further reduction of the aperture ratio from the above-described reason.

As described above, with the conventional wiring layout, the width of the electric line and the aperture ratio of the pixel are in the relation of trade off each other, and it is difficult to maintain a large aperture ratio while maintaining the electric power line with a suitable width for each color under the condition that the pixel matrix is formed with the same pixel pitch.

Accordingly, it is an object of the present invention to provide a wiring method for electric power lines, wherein the aperture ratio of the pixel can be increased while maintaining a pixel matrix with the same pixel pitch.

In order to solve the above-described problems, an electro-optical device according to the present invention comprises multiple pixels, disposed in the form of a matrix, including electro-optical devices driven by receiving electric power from an electric power supply circuit, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein the line forming regions are formed with generally the same width. With such a configuration, the pixel pitch can be made the same.

Here, "electro-optical device" means a general electronic device for changing the optical state of light by using electric effects, and include, besides self-light-emitting devices such as electro-luminescence devices, electronic devices for displaying grayscale by adjusting the state of the polarized light, similarly to liquid crystal devices. With the present invention, the electro-luminescence devices are preferably employed. With the present invention, the electro-luminescence devices are employed, whereby current-driven self-light-emission devices can be obtained.

Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein at least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein both at least one electric power line of the multiple electric power lines and at least one scan line of the multiple scan lines are

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formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

Another electro-optical device according to the present invention comprises multiple scan lines, multiple data lines, multiple pixels, disposed at portions corresponding to the intersections of the scan lines and the data lines, including electro-optical devices, and multiple electric power lines for supplying driving voltage to the electro-optical devices, wherein the multiple pixels make up multiple pixel groups formed of a series of pixels arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel groups of the multiple pixel groups, and wherein both at least one electric power line of the multiple electric power lines and at least one data line of the multiple data lines are formed in at least one line forming region of the multiple line forming regions. With such a configuration, a pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio while forming electric power lines with the optimal width.

The aforementioned line forming regions are preferably formed with generally the same width. With the present invention, the line forming regions are formed with generally the same width, whereby the pixel matrix can be formed with the same pixel pitch.

The aforementioned electro-optical device preferably includes electro-optical devices which are operated with different driving voltages, wherein the electric power lines for supplying voltage to the electro-optical devices are formed with different widths corresponding to the driving voltage. Even with such a configuration wherein the electric power lines are formed with different widths, the wiring layout is designed as described above, whereby the pixel matrix can be formed with the same pixel pitch while improving the aperture ratio.

The aforementioned electro-optical device preferably is a light-emission device, wherein the electric power lines are formed with each different width corresponding to the emission light color of the light-emission device. With the present invention, the optimal width of the electric power line is determined corresponding to the properties of the electro-optical device, thereby facilitating design of devices.

The color of the light which is to be emitted is preferably red, green, or blue. This enables full-color display.

The electro-optical device preferably is an electro-luminescence device. With the electro-luminescence device, the grayscale due to light emission can be controlled by current control.

An electronic apparatus according to the present invention comprises an electro-optical device according to the present invention. The electronic apparatus is not particularly restricted so long as it includes a display device, and can be applied to, for example, cellular phones, video cameras, personal computers, head mount displays, projectors, facsimiles, digital cameras, portable TVs, DSP devices, PDAs, palmtops, and the like.

A matrix substrate according to the present invention comprises multiple pixel electrodes disposed in the form of a matrix, wherein the multiple pixel electrodes make up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups, and wherein the line

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forming regions are formed with generally the same width. With such a configuration, the pixel pitch can be made the same.

Another matrix substrate according to the present invention comprises multiple scan lines, multiple data lines, multiple pixel electrodes disposed at portions corresponding to the intersections of the scan lines and the data lines, and multiple electric power lines for supplying voltage to the multiple pixel electrodes, wherein the multiple pixel electrodes make up multiple pixel electrode groups formed of a series of pixel electrodes arrayed in at least one direction of the row direction and the column direction, and wherein multiple line forming regions are formed between adjacent pixel electrode groups of the multiple pixel electrode groups, and wherein at least two lines selected from at least one electric power line of the multiple electric power lines, at least one scan line of the multiple scan lines, and at least one data line of the multiple data lines, are formed in at least one line forming region of the multiple line forming regions. With such a configuration, the pixel matrix can be formed with the same pixel pitch, and also with a high aperture ratio, while forming the electric power lines with the optimal width.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of an organic EL display panel according to the present invention.

FIG. 2 is a principal circuit configuration diagram of a pixel.

FIG. 3 is an explanatory diagram for describing a wiring layout according to a first embodiment.

FIG. 4 is an explanatory diagram for describing a wiring layout according to a second embodiment.

FIG. 5 is an explanatory diagram for describing a wiring layout according to a third embodiment.

FIG. 6(a) through FIG. 6(f) are explanatory diagrams for describing application examples employing the organic EL display according to the present invention;

FIG. 7 is an explanatory diagram for describing a wiring layout according to a fourth embodiment.

FIG. 8 is an explanatory diagram for describing a wiring layout according to a fifth embodiment.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present embodiment will now be described with reference to the drawings.

FIG. 1 is an overall configuration diagram which illustrates an active-matrix organic-EL display panel 100 according to the present embodiment. As shown in the drawing, the display panel 100 comprises a display region 11 including multiple pixels 10 disposed in the form of a matrix with an N number of columns and an M number of rows, a scan line driver 12 for outputting scan signals to scan lines arrayed in the row direction which are connected to a group of pixels 10, a data line driver 13 for supplying data signals and electric power to data lines and electric power lines arrayed in the column direction which are connected to a group of pixels 10, wherein these components are disposed on a substrate 16. An organic EL device is formed on each pixel 10 for emitting light in a color of the RGB three primary colors. A cathode 14 is formed in the form of a film as a common electrode on the entire face of the display region 11, and is connected to an external circuit through cathode output electrode 15.

Note that while the organic EL display panel 100 shown in the drawing is a so-called "top-emission configuration dis-

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play panel" which emits light from the side of the substrate 16, the present invention is not restricted to this arrangement, but rather, the present invention can also be applied to a bottom-emission configuration display panel which emits light from a transparent cathode.

FIG. 2 is a principal circuit configuration diagram of the pixel 10. The pixel 10 comprises a switching transistor Tr1, a driving transistor Tr2, holding capacitance C, a light-emission portion OLED, and is driven with the dual transistor method. The switching transistor Tr1 comprises an n-channel FET, wherein the gate terminal thereof is connected to the scan line V_{sel} , and the drain terminal thereof is connected to the data line I_{dat} . The driving transistor Tr2 comprises a p-channel FET, wherein the gate terminal is connected to the source terminal of the switching transistor Tr1. Furthermore, the source terminal of the transistor Tr2 is connected to the electric power line V_{dd} , and the drain terminal thereof is connected to the light-emission portion OLED. Furthermore, holding capacitance is formed between the gate and the source of the transistor Tr2. With the above-described configuration, upon outputting a selection signal to the scan line V_{sel} , and opening the transistor Tr1, the data signals supplied through the data line I_{dat} are written to the holding capacitance C as a voltage value. Subsequently, the holding voltage written to the holding capacitance C is held during one frame period, and the conductance of the driving transistor Tr2 is determined according to the holding voltage in an analog manner, whereby forward bias current corresponding to light-emission level is supplied to the light-emission portion OLED.

FIG. 3 is a diagram for describing a wiring layout in the pixel region. In the drawing, in order to simplify description, a wiring layout for six pixels disposed with the two rows and the three columns is shown. In the drawing, reference characters R, G, and B denote the pixels 10 for emitting light in red, green, and blue, respectively, and the RGB pixels are disposed in the column direction. Furthermore, reference character V_{dd-R} denotes an electric line for a red pixel, V_{dd-G} denotes an electric line for a green pixel, V_{dd-B} denotes an electric line for a blue pixel, and 17 denotes a pixel electrode (anode) of an organic EL device. Detailed description regarding other components described above will be omitted. Furthermore, reference numeral 31 denotes a line forming region in the form of a line which is formed between a pixel group of the (m-1) column and a pixel group of the m column, and is extending in the column direction over generally the same length as the pixel array length in the column direction. In the same way, reference numeral 32 denotes a line forming region formed between pixel groups of the m column and the (m+1) column, 33 denotes a line forming region formed between pixel groups of the (m+1) column and (m+2) column, and 34 denotes a line forming region formed between pixel groups of the (m+2) column and the (m+3) column. For convenience of description, a pixel group of the (m-1) column and a pixel group of the (m+3) column are not shown in the drawing. With the present embodiment, in order to determine the line forming regions 31 through 34 with the width as same as possible, two or more lines, disposed on the aforementioned line forming regions, are determined with the same total width. While the electric power line V_{dd} is formed with a width corresponding to a material of the emission layer of the organic EL device, now, for convenience of description, let us make an assumption that the width of the electric power lines increases in the order of green, red, and blue. That is to say, let us assume that the relation: width of V_{dd-G} > width of V_{dd-R} > width of V_{dd-B} , holds.

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With the above-described assumption, in order to form the line forming regions 31 through 34 with the width as same as possible, a combination is determined such that the total width of the electric power line V_{dd} and the data line I_{dat} is approximately the same. For example, making an assumption that: the total width of V_{dd-G} which has the maximal width and V_{dd-B} of the minimal width; the total width of V_{dd-R} of an intermediate width and the data line I_{dat} of an intermediate width; and the total width of the two data lines I_{dat} are determined to be generally the same value, the combinations of these electric power lines V_{dd} and the data line I_{dat} are formed in the line forming regions 31 through 34. With the arrangement shown in the drawing, a combination of V_{dd-G} with the maximal width and V_{dd-B} with the minimal width is formed on the line forming region 33, a combination of V_{dd-R} with the intermediate width and the data line I_{dat} with the intermediate width is formed in the line forming regions 31 and 34, and a combination of the two data lines I_{dat} is formed on the line forming region 32. Note that with the line forming region 31, only the electric power line V_{dd-R} is shown in the drawing, and with the line forming region 34, only the data line I_{dat} is shown in the drawing. On the other hand, a scan line V_{sel} is disposed on each line forming region in the form of a line, between pixel groups arrayed in the row direction, with generally the same length as the pixel array length of the pixel group. The wiring layout shown in the drawing corresponds to one unit of a periodically repeating wiring pattern, and any portion of the wiring layout of the RGB pixels 10 randomly selected has the same pattern as shown in the drawing. Accordingly, in the event that an imaginary layout-diagram sheet, determining the layout of the line forming regions formed along the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other.

With the present embodiment, the same kind of electric power line, extending in the column direction of the pixel matrix, is formed with generally the same array pitch in the row direction, and accordingly, the pixels can be formed with the same pixel pitch, thereby facilitating design of a layout for a device, wherein power consumption is different for each color, such as an organic EL display. In particular, in the event of forming light-emission layers using the ink-jet method, the pixels are preferably formed with the same pixel pitch, and accordingly, an arrangement according to the present embodiment has the great advantage of facilitating the manufacturing process. Furthermore, with the present embodiment, the electric power line can be formed with a width suitable for each color, thereby reducing power consumption while maintaining the high aperture ratio and the optimal color balance.

Note that the above-described arrangement is only an example of the present invention, and the present invention is not restricted to the above-described arrangement. For example, three combinations of two electric power lines selected from the three RGB lines V_{dd} can be made, and accordingly, with the present embodiment, three wiring layout patterns can be made. Furthermore, while description has been made regarding a configuration wherein a scan line V_{sel} is disposed on each line forming region in the row direction, and any two lines selected from the three electric power lines V_{dd} and the three data line I_{dat} are disposed on the line forming regions 31, 32, and 33 in the column direction, the present invention is not restricted to this arrangement. Description will be made below regarding various modifications.

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Second Embodiment

FIG. 4 is an explanatory diagram for describing a wiring layout according to a second embodiment of the present invention.

The present embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} make up a combination, and are disposed in the row direction on a line forming region 41 between the pixel group of the (n-1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines V_{sel} make up a combination, and are disposed in the row direction in a line forming region 42 between the pixel groups of the n row and the (n+1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration wherein the combination of the electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} , and the combination of the two scan lines V_{sel} are disposed periodically and repeatedly. Accordingly, a line forming region 43 between the pixel groups of the (n+1) row and the (n+2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 41.

On the other hand, one electric power line V_{dd} and one data line I_{dat} make up a combination, and are disposed in the column direction and are disposed on a line forming region between pixel groups arranged in the column direction. With an arrangement shown in the drawing, the electric power line V_{dd-R} and the data line I_{dat} make up a combination, and are disposed on a line forming region 51 between the R-pixel group of the m column and the G-pixel group of the (m+1) column, which are arrayed in the column direction. In the same way, the electric power line V_{dd-G} and the data line I_{dat} make up a combination, and are disposed on a line forming region between the G-pixel group of the (m+1) column and the B-pixel group (not shown) of the (m+2) column, which are arrayed in the column direction, wherein only the electric power line V_{dd-G} is shown in the drawing for convenience of description. Furthermore, the electric power lines V_{dd-R} and V_{dd-G} are disposed in the row and column directions are formed in different layers, and are electrically connected with each other through contact holes h1 formed in an inter-layer insulating film. The electric power lines V_{dd-G} are electrically connected with each other through contact holes h2 in the same way.

With the present embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same array pitch, and accordingly, the present embodiment has the same advantages as with the first embodiment, and furthermore, the electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, cross-talk can be reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present embodiment is particularly advantageous.

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Third Embodiment

FIG. 5 is an explanatory diagram for describing a wiring layout according to a third embodiment of the present invention.

The present embodiment has a configuration wherein, in the event that an imaginary layout diagram sheet, determining the layout of the line forming regions formed along the row direction and the column direction of the pixels, is folded with any line forming region of the multiple line forming regions as the center line, the line forming regions having the same configuration of the lines are overlaid on each other. The three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} make up a combination, and are disposed in the row direction on a line forming region 61 between the pixel group (not shown) of the (n-1) row and the pixel group of the n row, which are arrayed in the row direction, and the two scan lines V_{sel} make up a combination, and are disposed in the row direction in a line forming region 62 between the pixel groups of the n row and the (n+1) row, which are arrayed in the row direction. The basic pattern of the wiring layout in the row direction has a configuration wherein the combination of the three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} , and the combination of the two scan lines V_{sel} are disposed periodically and repeatedly. Accordingly, a line forming region 63 between the pixel groups of the (n+1) row and the (n+2) row, which are arrayed in the row direction, has the same wiring layout as with the line forming region 61.

On the other hand, three combinations of two lines selected from the three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} , and the three data lines I_{dat} are formed between the pixel groups arrayed in the column direction. With an arrangement shown in the drawing, the electric power line (not shown) and the data line I_{dat} make up a combination, and are disposed in a line forming region 71 between the B-pixel group (not shown) of the (m-1) column and the R-pixel group of the m column, which are arrayed in the column direction, and the two electric power lines V_{dd-G} and V_{dd-R} make up a combination, and are disposed on a line forming region 72 between the R-pixel group of the m column and the G-pixel group of the (m+1) column, which are arrayed in the column direction. Furthermore, the two data lines I_{dat} make up a combination, and are disposed on a line forming region 73 between the G-pixel group of the (m+1) column and the B-pixel group of the (m+2) column, which are arrayed in the column direction, and the electric power line V_{dd-G} and the data line I_{dat} make up a combination, and are formed on a line forming region 74 between the B-pixel group of the (m+2) column and the R-pixel group (not shown) of the (m+3) column, which are arrayed in the column direction.

The electric power lines disposed in the column and row directions are formed in different layers, and are electrically connected with each other through the contact holes h1 formed on an inter-layer insulating film. In the same way, the electric power lines V_{dd-G} in the column and row directions, and the electric power lines V_{dd-B} in the column and row directions, are formed in different layers, and the electric power lines in the column and row directions are electrically connected with each other through the contact holes h2 and h3. With the present embodiment, a plurality of each of the contact holes h1, h2, and h3 are formed, whereby the present embodiment has the advantage of preventing wiring breakage, and furthermore has the advantage of reducing the wiring resistance.

With the present embodiment, the same kind of electric power line extending in the row direction of the pixel matrix is formed in the column direction with generally the same

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array pitch, the same kind of electric power line extending in the column direction of the pixel matrix is formed in the row direction with generally the same array pitch, and accordingly, the present embodiment has the same advantages as with the first embodiment, and furthermore, the electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} are disposed on a pixel region in the row direction and the column direction in the form of a matrix, and accordingly, the wiring resistance of the electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} can be reduced, thereby enabling sufficient current supply to the organic EL devices. Accordingly, occurrence of non-uniformity of luminance due to insufficient current supply to a particular electric power line can be suppressed, and furthermore, the occurrence of cross-talk can be reduced. In particular, a large-screen display requires sufficient and uniform current over the screen thereof, and accordingly, the present embodiment is particularly advantageous.

Fourth Embodiment

FIG. 6(a) through FIG. 6(f) are diagrams which illustrate examples of electronic apparatuses to which the electric-optical device according to the present invention can be applied. FIG. 6(a) shows an example of application to a cellular phone, wherein the cellular phone 230 comprises an antenna unit 231, an audio output unit 232, an audio input unit 233, an operating unit 234, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 according to the present invention can be employed as a display unit of the cellular phone 230. FIG. 6(b) shows an application example to a video camera, wherein the video camera 240 comprises a TV-camera unit 241, an operating unit 242, an audio input unit 243, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a viewfinder or a display unit. FIG. 6(c) shows an application example to a portable personal computer, wherein the computer 250 comprises a camera unit 251, an operation unit 252, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as a display device.

FIG. 6(d) shows an application example to a head mount display, wherein the head mount display 260 comprises a belt 261, an optical system storage unit 262, and the organic EL display panel 100 according to the present invention. As described above, the organic EL display panel 100 can be employed as an image display unit. FIG. 6(e) shows an application example to a rear projector, wherein the projector 270 comprises a casing 271, a light source 272, a synthesizing optical system 273, mirrors 274 and 275, a screen 276, and the organic EL display panel 100 according to the present invention. FIG. 6(f) shows an application example to a front projector, wherein the projector 280 comprises a casing 282, an optical system 281, and the organic EL display panel 100 according to the present invention, wherein an image can be displayed on a screen 283. As described above, the organic EL display panel 100 can be employed as an image display unit.

FIG. 7 is an explanatory diagram for describing a wiring layout according to another embodiment. Specifically, combinations of lines selected from the three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} , and the data lines I_{dat} are formed between the pixel groups arrayed in the column direction. In addition, scan lines V_{sel} are formed between pixel groups arrayed in the row direction.

FIG. 8 is an explanatory diagram for describing a wiring layout according to another embodiment. Specifically, com-

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binations of lines selected from the three electric power lines V_{dd-G} , V_{dd-R} , and V_{dd-B} , and the scan lines V_{sel} are formed between pixel groups arrayed in the row direction.

What is claimed is:

1. An electro-optical device comprising:

a scan line;
a data line that intersects the scan line;
a first electrode;
a second electrode;
a light emission layer that is disposed between the first electrode and the second electrode;
a first power line that has a first portion extending in a first direction and a second portion extending in a second direction that intersects the first direction;
a second power line that extends in the second direction, the second power line overlapping at least a part of the second portion of the first power line; and
an inter-layer insulating film that is disposed between the first power line and the second power line, the second portion of the first power line being electrically connected to the second power line through plurality of contact holes.

2. The electro-optical device according to claim 1, the second portion of the first power line extending from the first portion along the second direction to only one side,

the second portion being positioned on one side of the first portion of the first power line with respect to the first portion of the first power line, and

the second portion not being positioned on the other side with respect to the first portion of the first power line.

3. The electro-optical device according to claim 1, the second power line being electrically connected to the first electrode.

4. The electro-optical device according to claim 1, the plurality of contact holes extending along the first direction.

5. An electro-optical device comprising:

a plurality of scan lines;
a plurality of data lines that intersect the plurality of scan lines;

a plurality of pixels that is disposed corresponding to a plurality of intersections of the plurality of scan lines and the data lines, each of the plurality of pixels including a first pixel and a second pixel, each of the first pixel and the second pixel having a light emission layer between a first electrode and a second electrode, the first pixel and the second pixel being aligned along a first direction along which the plurality of scan lines extend;

a first power line that extends along the first direction;

a second power line that extends along a second direction that intersects the first direction; and

a third power line that extends along the second direction, the first power line being electrically connected to the second power line at a first connecting portion, the first connecting portion being located in the first pixel, the first power line being electrically connected to the third power line at a second connecting portion, and the second connecting portion being located in the second pixel.

6. The electro-optical device according to claim 5, the first power line being electrically connected to the first pixel and the second pixel.

7. The electro-optical device according to claim 5, the second power line being electrically connected to the first electrode.

* * * * *

Exhibit 3



US008525760B2

(12) **United States Patent**
Matsueda

(10) **Patent No.:** **US 8,525,760 B2**
(45) **Date of Patent:** ***Sep. 3, 2013**

(54) **ACTIVE MATRIX SUBSTRATE,
ELECTRO-OPTICAL DEVICE, AND
ELECTRONIC DEVICE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

This patent is subject to a terminal disclaimer.

(21) Appl. No.: **12/917,885**

(22) Filed: **Nov. 2, 2010**

(65) **Prior Publication Data**

US 2011/0042692 A1 Feb. 24, 2011

Related U.S. Application Data

(60) Continuation of application No. 11/483,109, filed on Jul. 10, 2006, now Pat. No. 7,982,692, which is a division of application No. 10/299,861, filed on Nov. 20, 2002, now Pat. No. 7,483,001.

(30) **Foreign Application Priority Data**

Nov. 21, 2001 (JP) 2001-356007
Dec. 5, 2001 (JP) 2001-371403
Dec. 5, 2001 (JP) 2001-371410

(51) **Int. Cl.**
G09G 3/30 (2006.01)

(52) **U.S. Cl.**
USPC 345/76; 315/169.3

(58) **Field of Classification Search**
USPC 345/76-83; 315/169.1-169.4; 349/42, 349/43, 46

See application file for complete search history.

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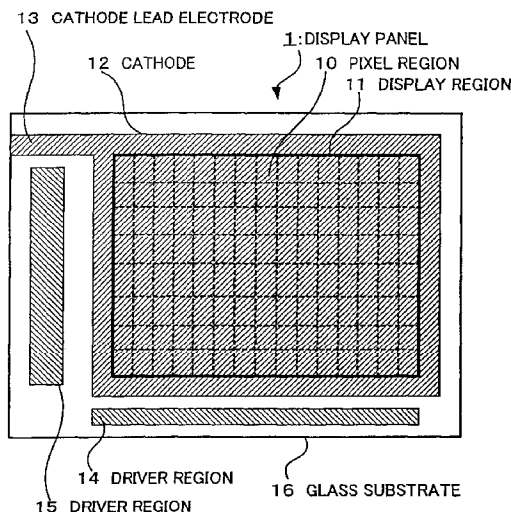
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(57) **ABSTRACT**

An active matrix substrate is provided which does not cause reductions in the brightness of electroluminescence elements, and which comprises appropriate peripheral circuitry occupying a small area. The active matrix substrate comprises peripheral circuits to supply current to EL elements provided for each pixel, and corresponding to EL elements, and further comprises a holding element (C) which holds a control voltage, a first active element (T1) connected to the holding element (C) and which supplies current to a light-emitting portion (OLED) based on a control voltage, and a second active element (T2) connected to the holding element (C) and which controls the charging and discharging of the holding element. In particular, the second active element (T2) is configured as a multiple-control-terminal type active element. As a result, there are no fluctuations in the programmed current.

11 Claims, 15 Drawing Sheets



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Fig. 1

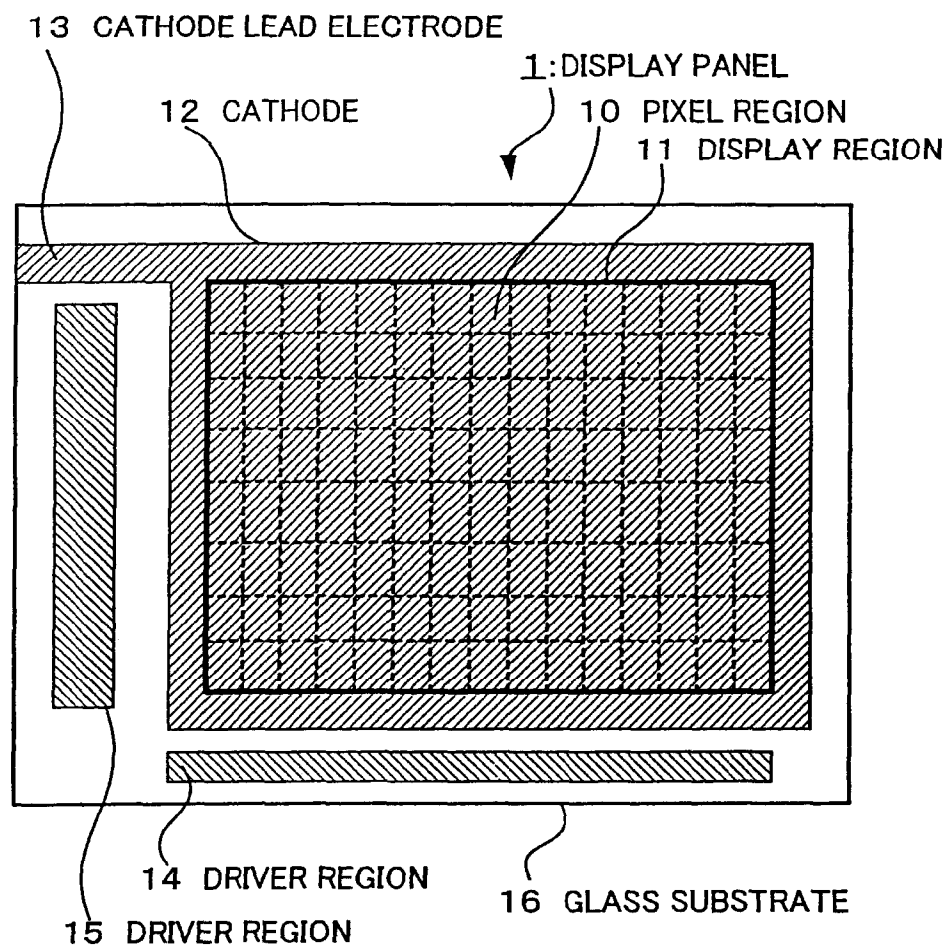


Fig.2

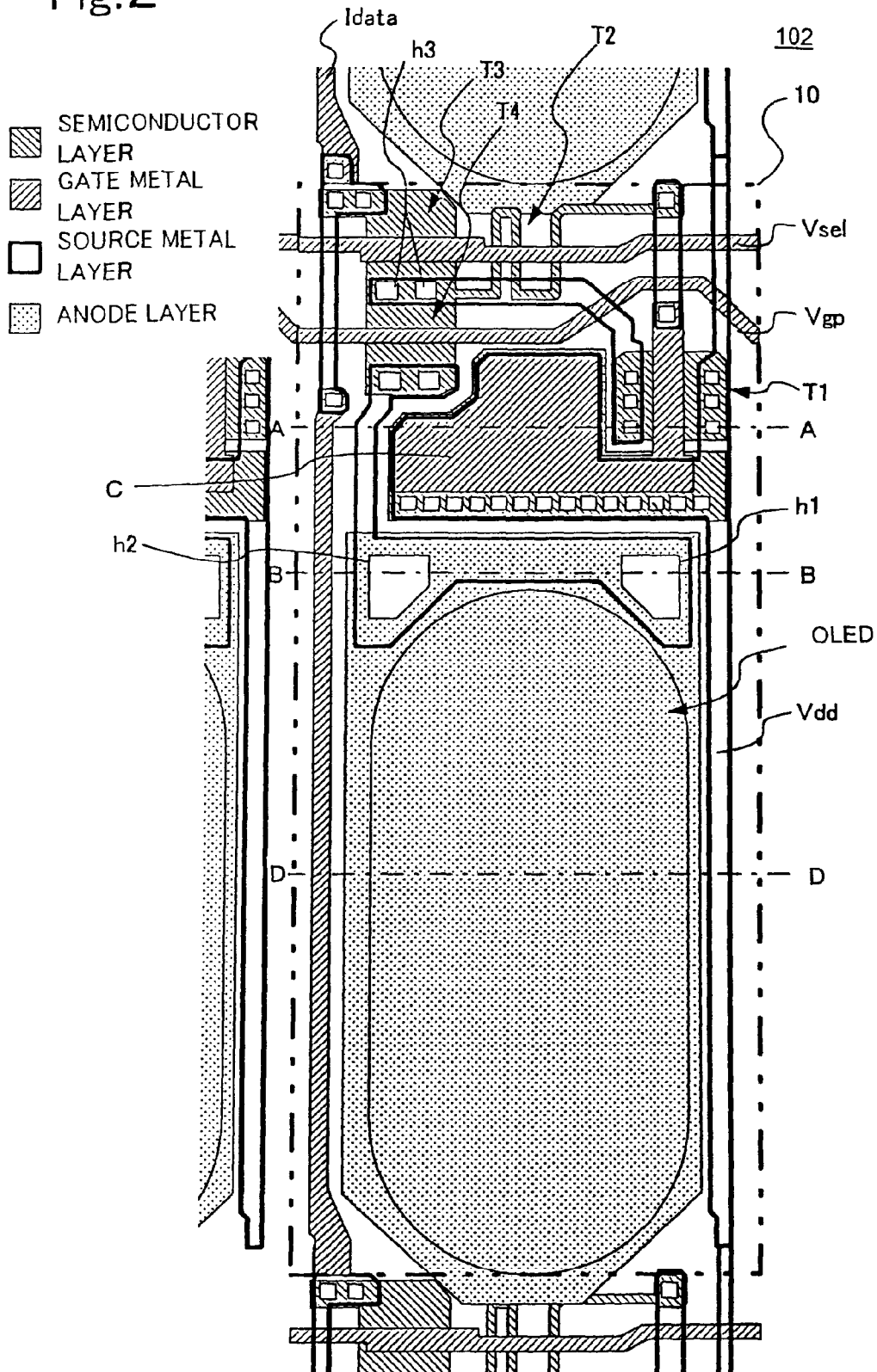


Fig.3A

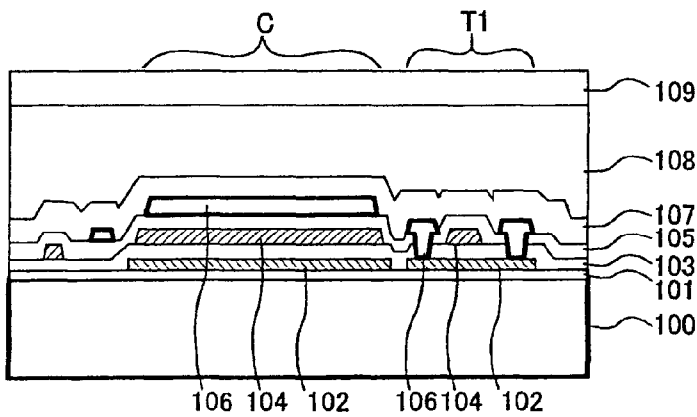


Fig.3B

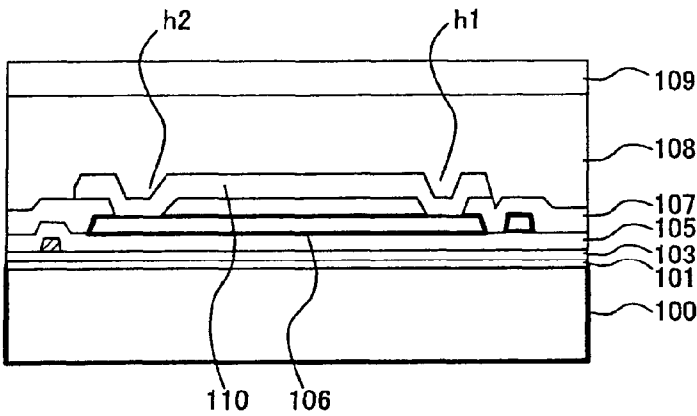
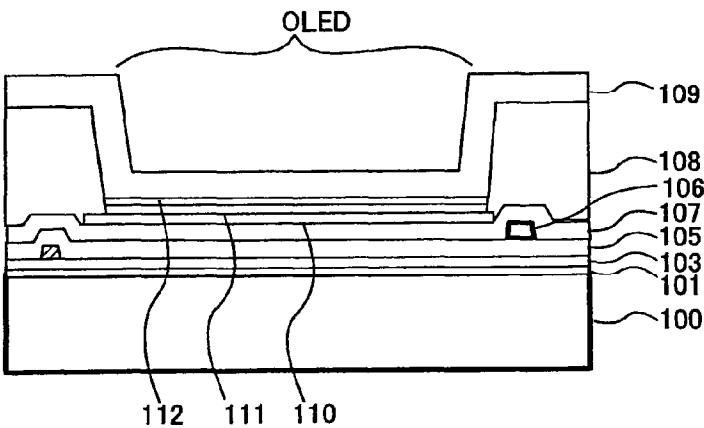


Fig.3C



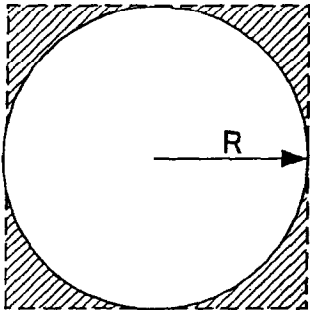


Fig.4A

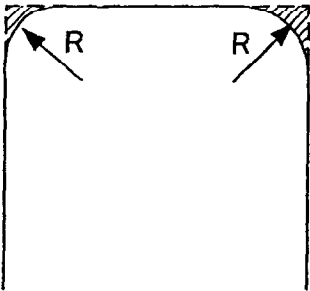


Fig.4B

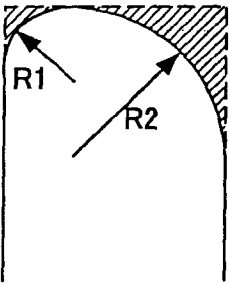


Fig.4C

Fig.5

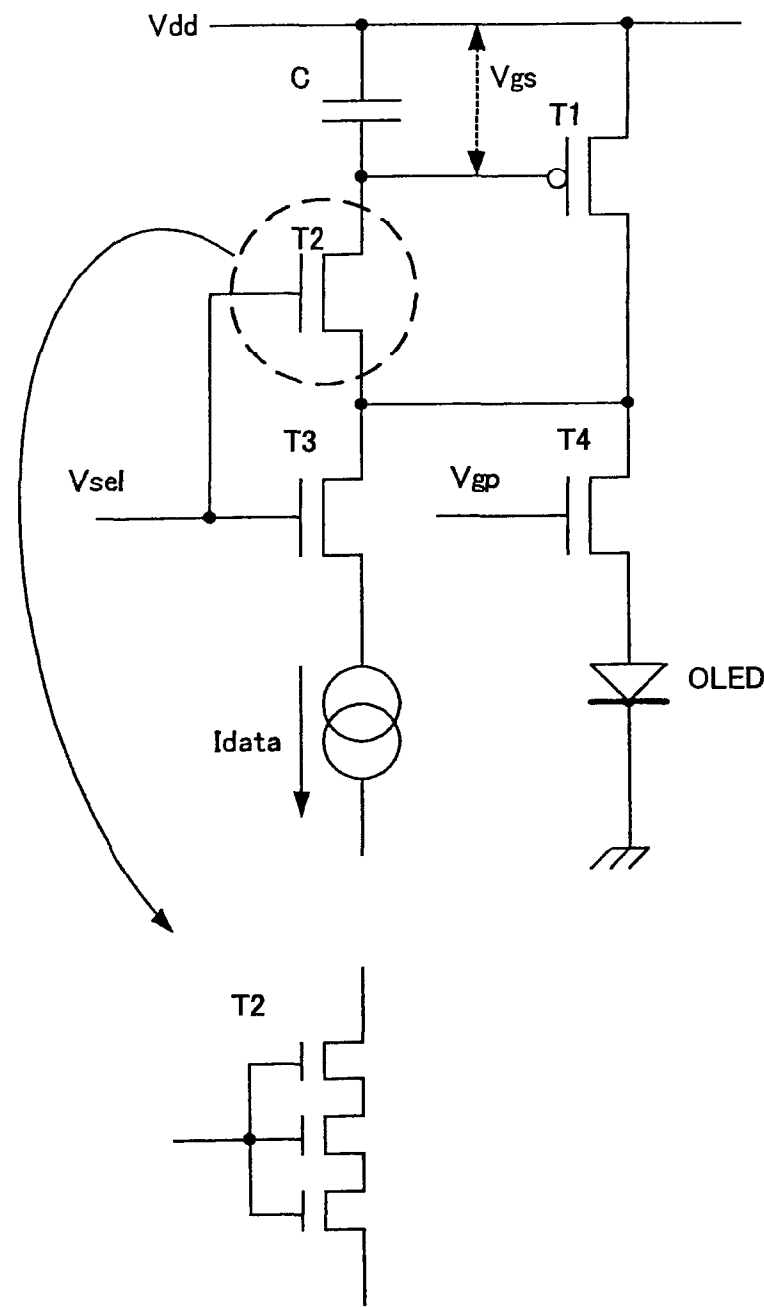


Fig.6

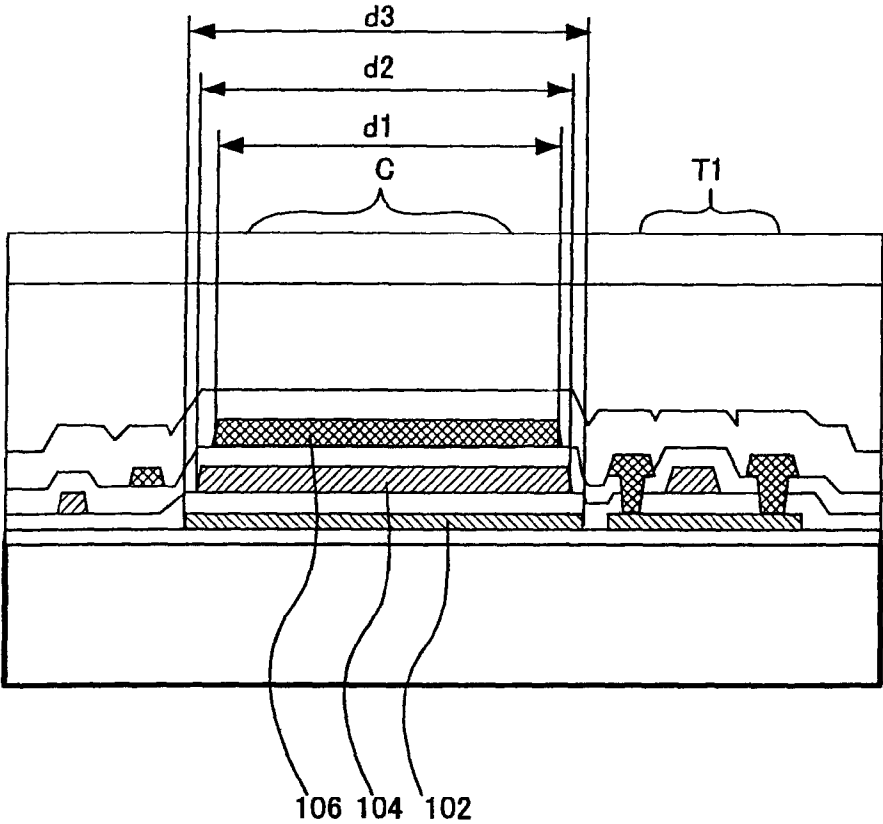


Fig.7

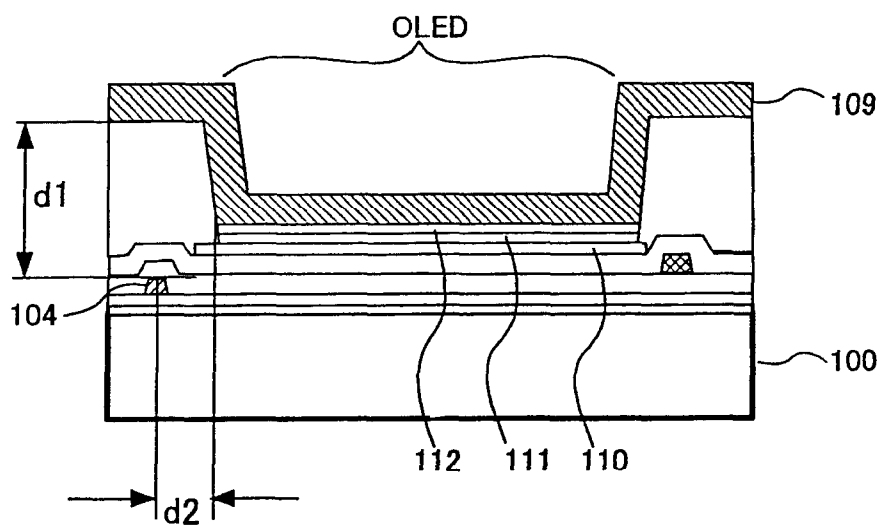


Fig.8

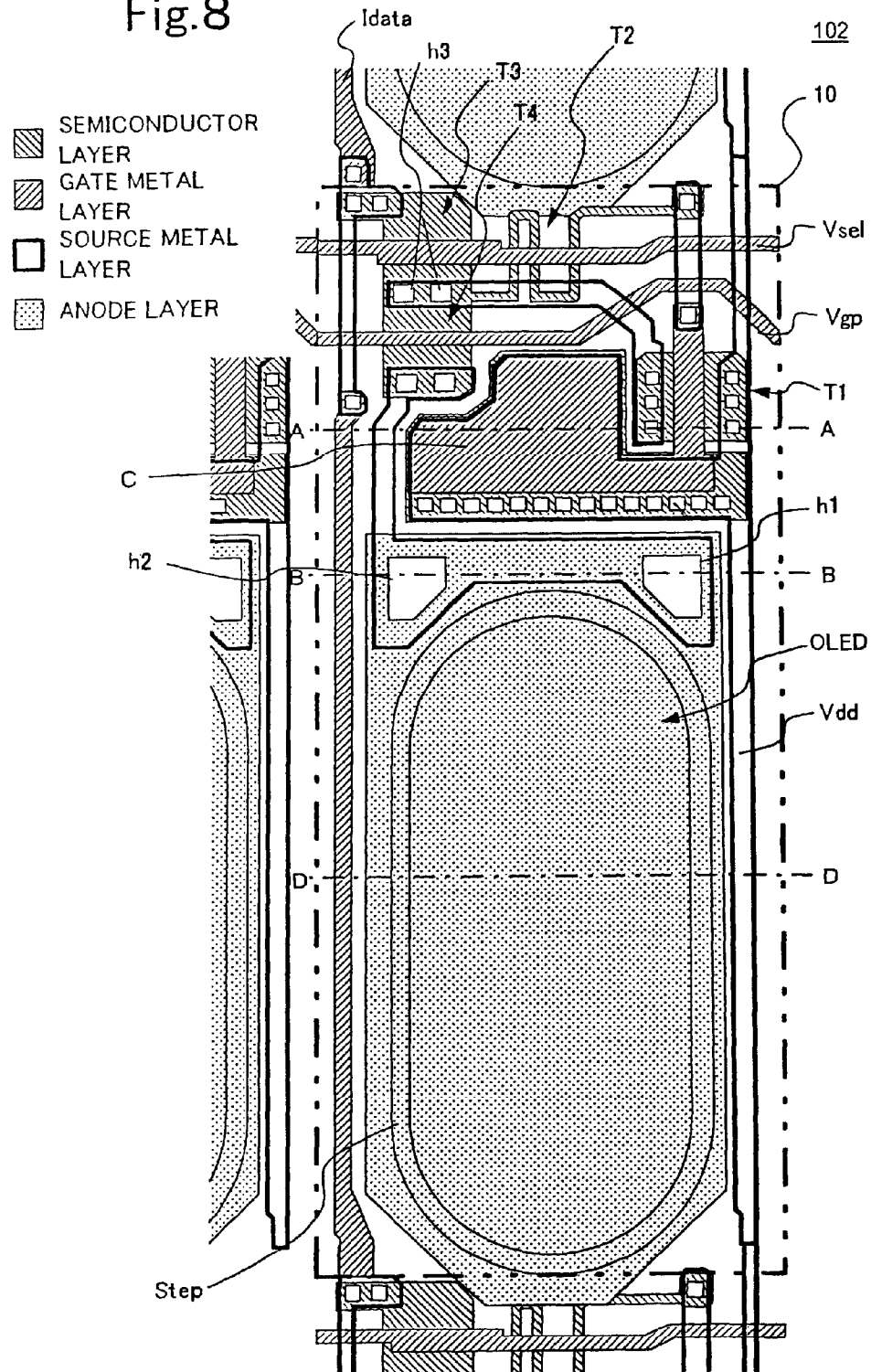


Fig.9A

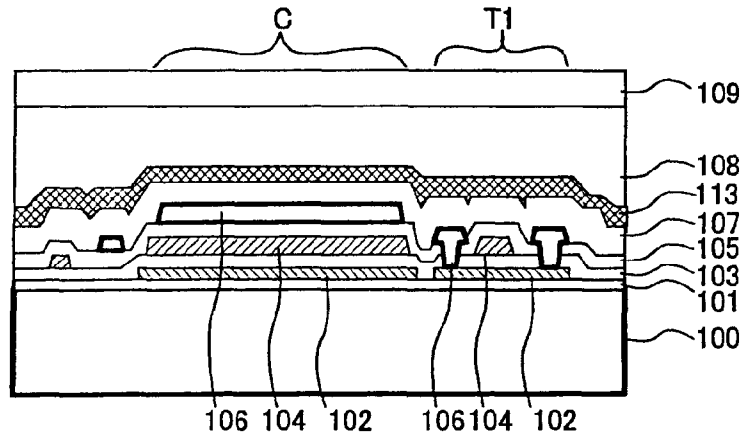


Fig.9B

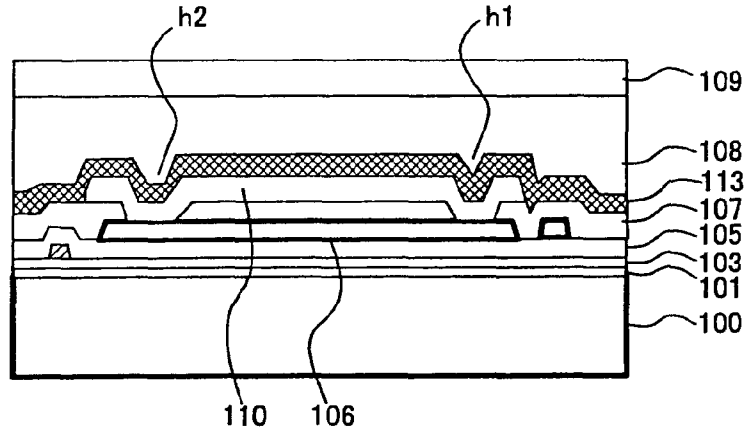


Fig.9C

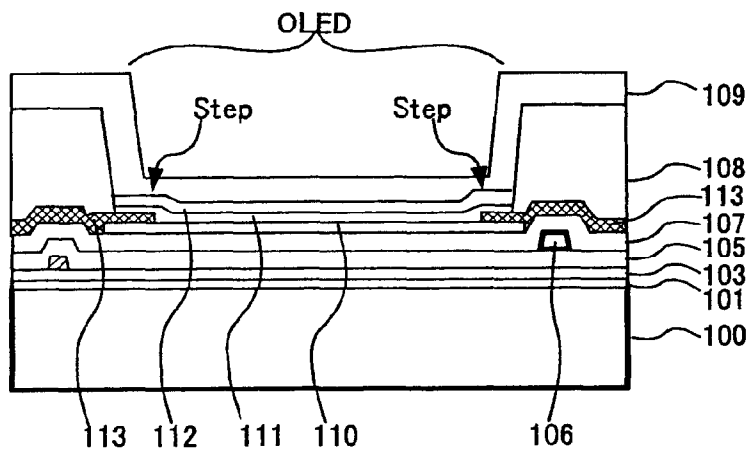


Fig. 10

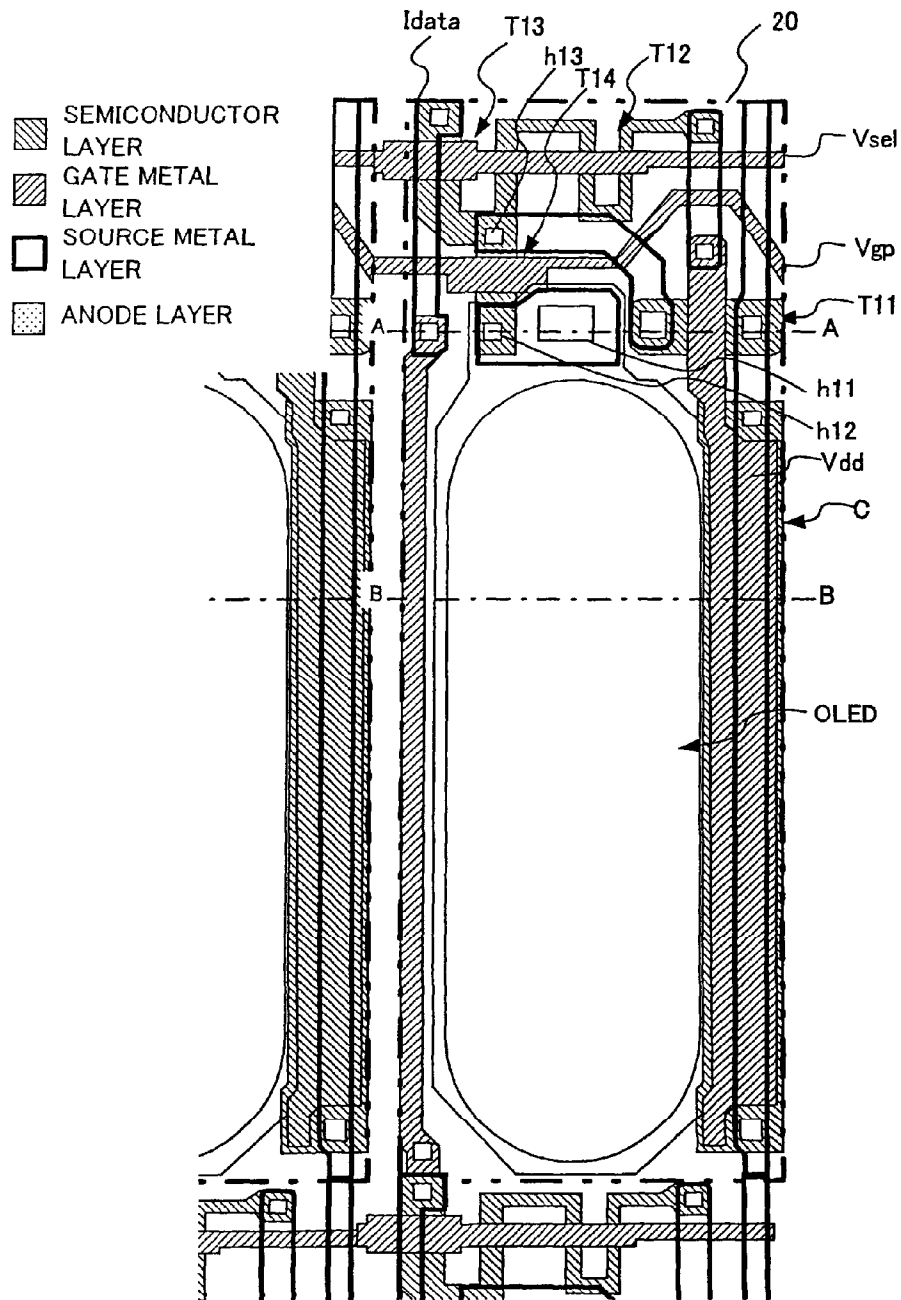


Fig. 1 1 A

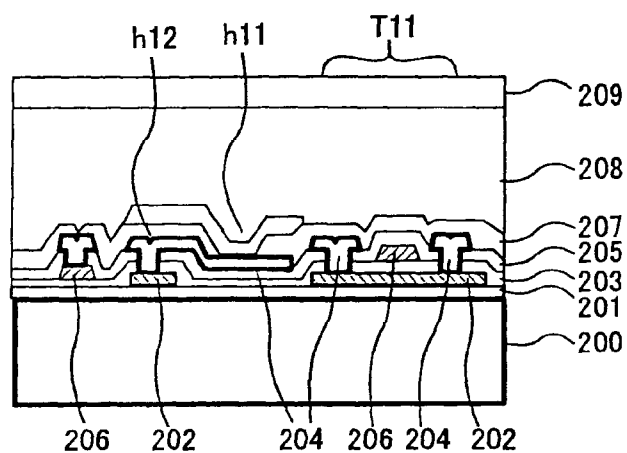


Fig.1 1B

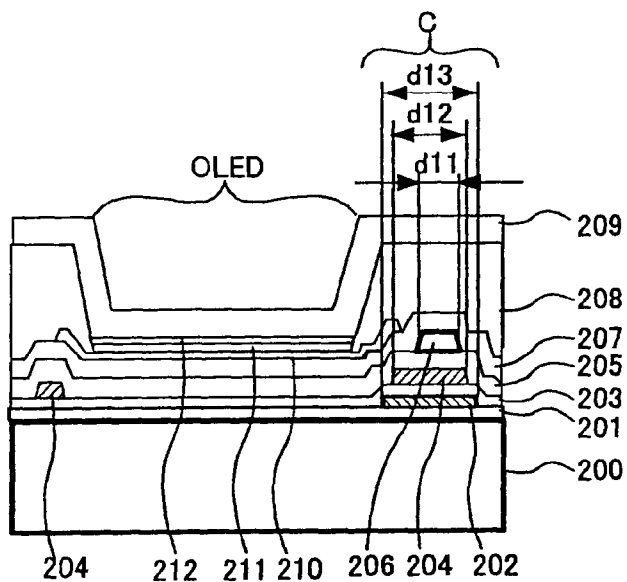


Fig. 12

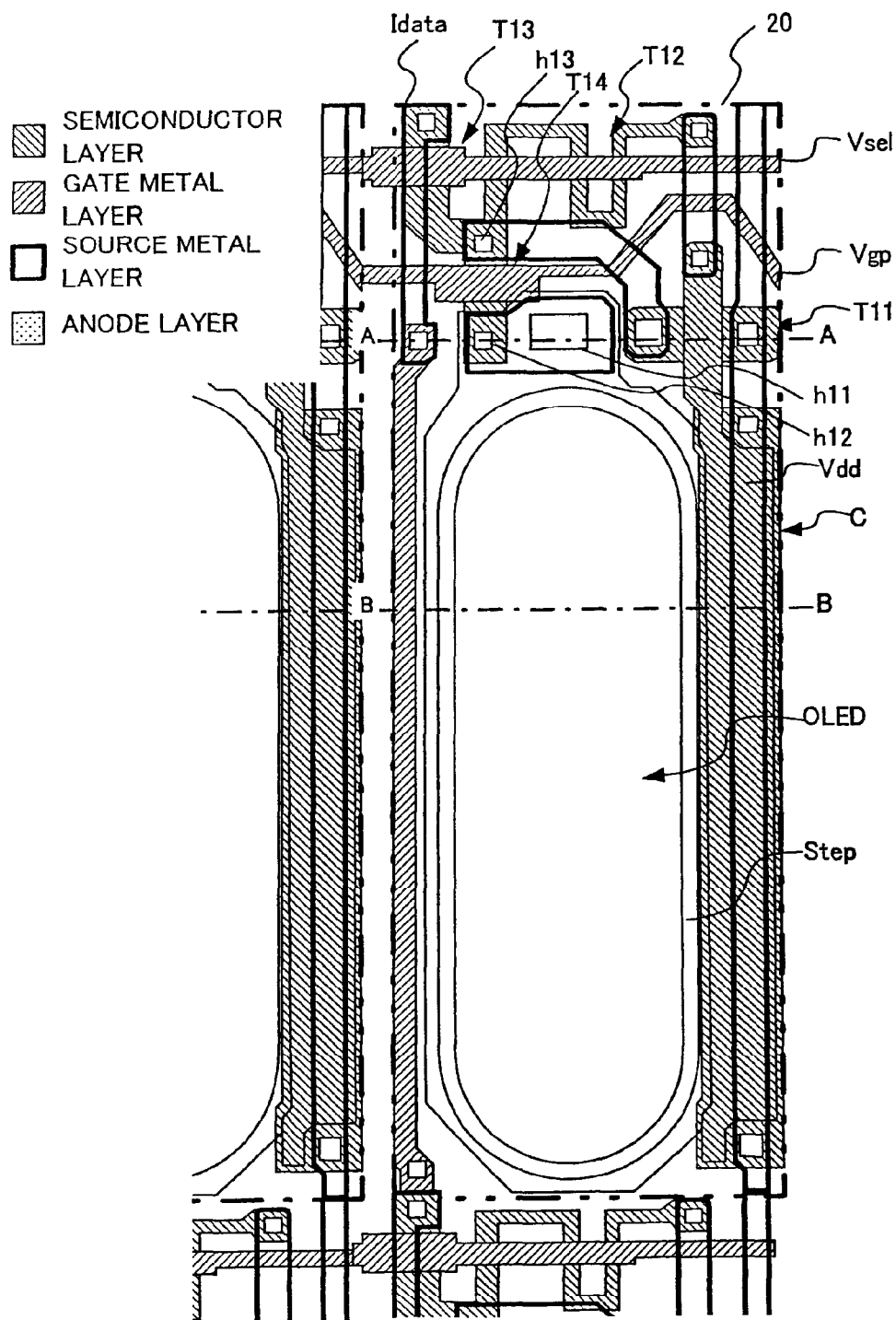


Fig. 13A

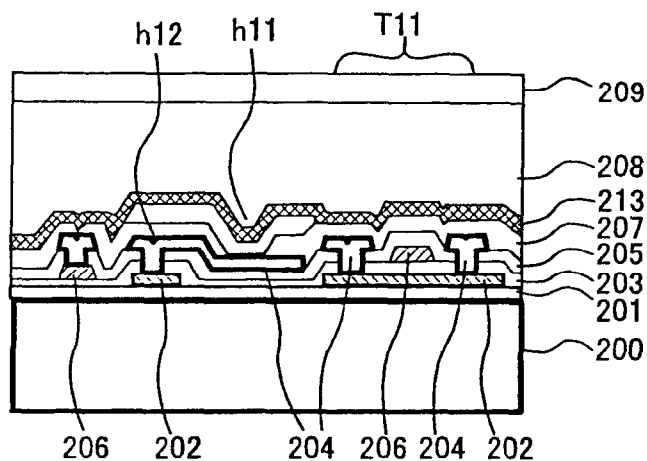


Fig. 13B

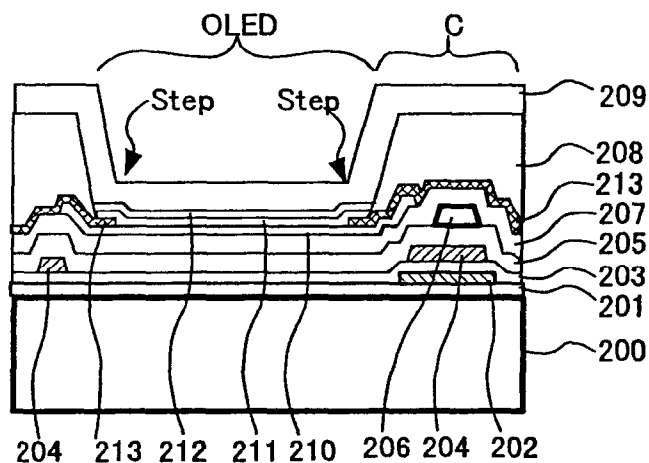
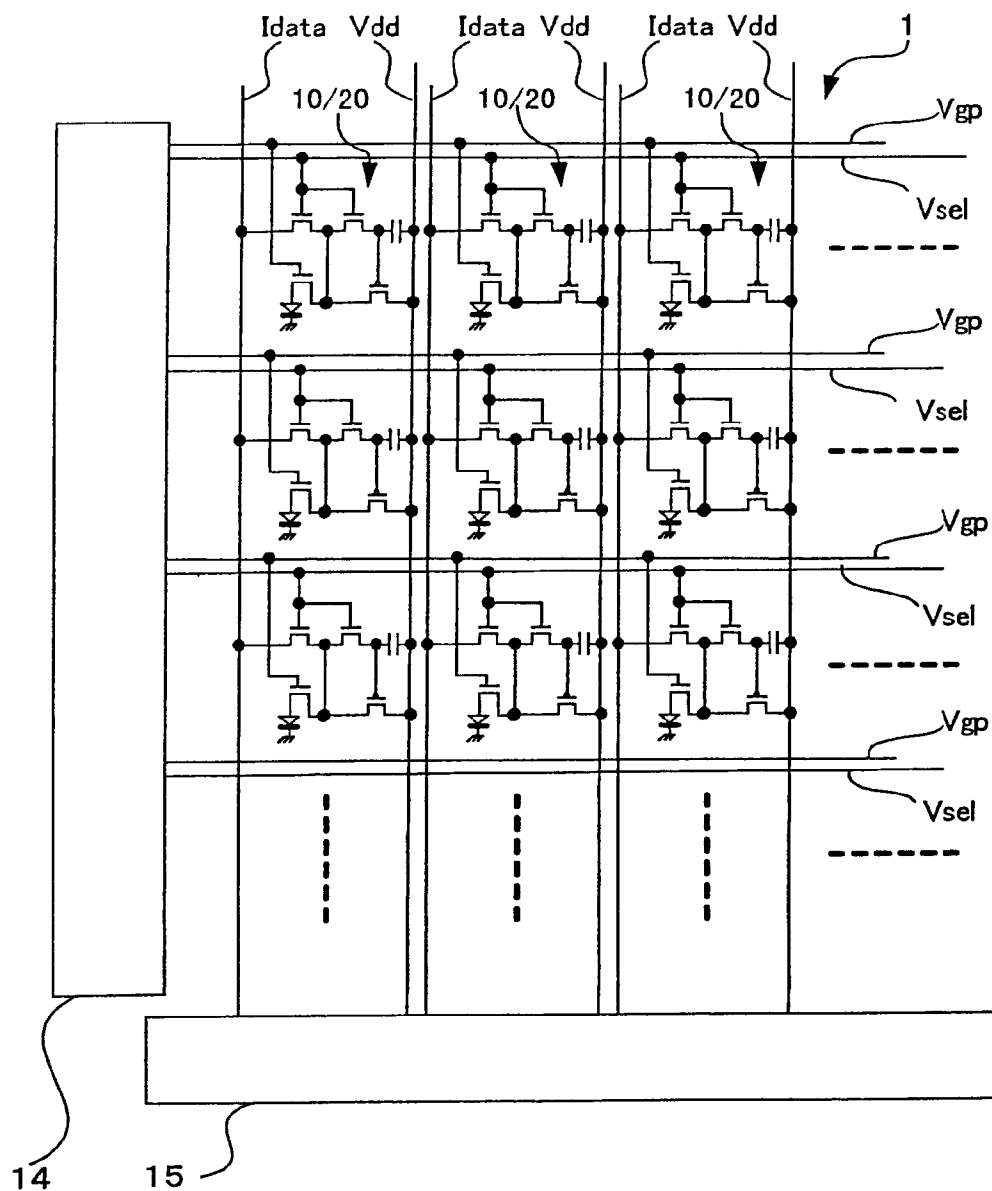


Fig. 14



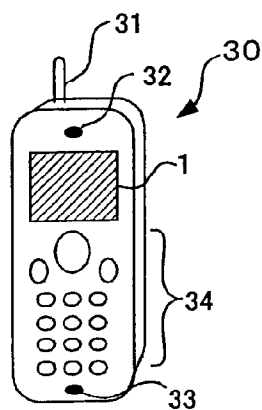


Fig. 15A

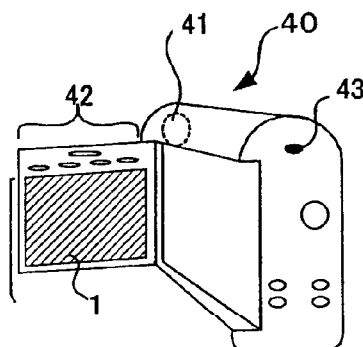


Fig. 15B

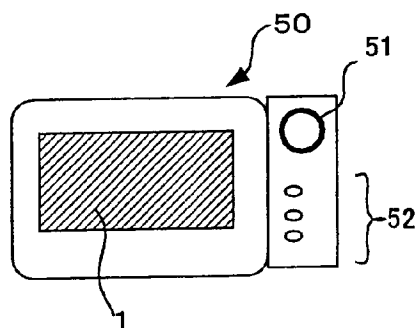


Fig. 15C

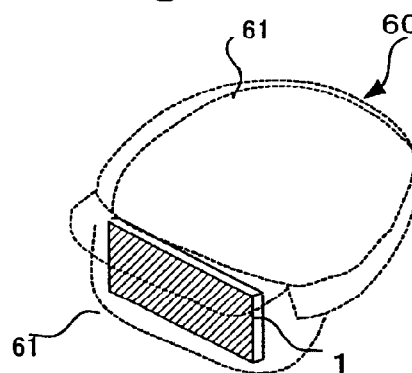


Fig. 15D

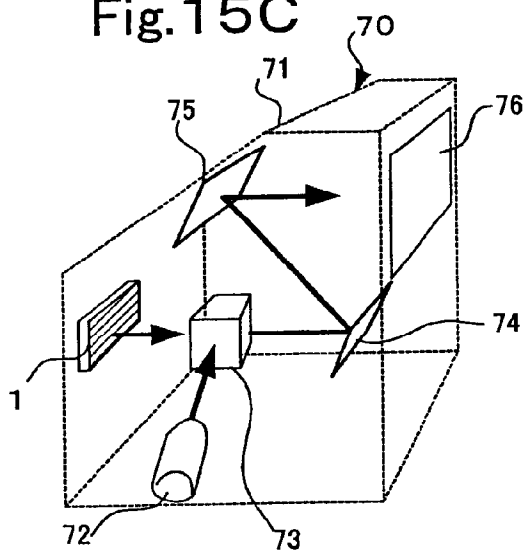


Fig. 15E

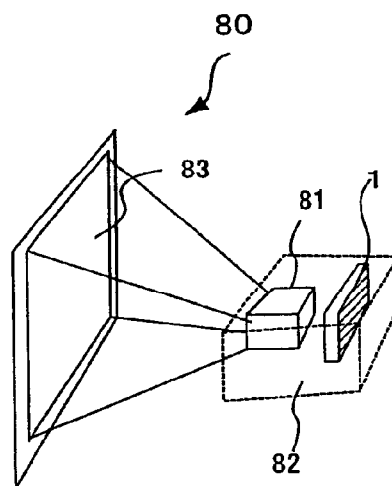


Fig. 15F

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ACTIVE MATRIX SUBSTRATE, ELECTRO-OPTICAL DEVICE, AND ELECTRONIC DEVICE

This is a Continuation of application Ser. No. 11/483,109 filed Jul. 10, 2006, which is a Divisional of application Ser. No. 10/299,861 filed Nov. 20, 2002. The entire disclosure of the prior application is hereby incorporated by reference herein in its entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to an active matrix substrate suitable for electro-optical devices, an electro-optical device, and electronic device.

2. Description of the Related Art

The active matrix driving method is one method of driving electro-optical devices comprising liquid crystal elements, organic electroluminescence (EL) elements, electrophoretic elements, electronic emission elements, and similar. In an electro-optical device driven by the active matrix driving method, a plurality of pixels are arranged in a matrix on the display panel. Each of the plurality of pixels comprises a pixel circuit, in turn comprising an electro-optical element and a driving transistor which supplies driving power to the electro-optical element. Each of the plurality of pixel circuits is arranged to correspond to the intersection of a data line and a scan line (see, for example, patent reference 1: Internationally disclosed pamphlet no. WO98/36407).

In order to precisely control brightness in an electro-optical device, the amount of power supplied to electro-optical elements must be precisely controlled. In particular, because organic EL elements are current-driving type electro-optical elements, the brightness is directly affected by the current. Hence there is a need to precisely supply the desired current to organic EL elements; and in addition to optimizing the driving circuit and driving method, the pixel layout must also be optimized. Problems encountered in actual pixel layouts include, for example, contact between pixel electrodes and peripheral circuitry, stability of holding capacitances, and transistor turn-off currents.

The present invention was devised in light of the above circumstances, and has as an object the provision of an active matrix substrate, electro-optical device, and electronic device comprising an optimal pixel layout for the stable driving of electro-optical elements.

SUMMARY OF THE INVENTION

In order to resolve the above problems, a first active matrix substrate of this invention is an active matrix substrate comprising peripheral circuitry to supply a current to electro-optical elements provided in each pixel according to the electro-optical element; each peripheral circuit comprises a holding element to hold a control voltage, a first active element, connected to the holding element, to supply a current to the electro-optical element based on the control voltage, and a second active element, connected to the holding element, to control the charging and discharging of the holding element; and the above second active element has a structure which prevents leakage currents during shutoff.

Here "electro-optical element" refers to general elements which emit light, or change a status of light in response to external light, due to electrical action, and comprises both elements which themselves emit light, and elements which control the transmission of external light. For example, elec-

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tro-optical elements include liquid crystal elements, electrophoretic elements, EL elements, and electron emission elements which emit light by causing electrons generated through application of an electric field to strike an emission plate.

"Peripheral circuits" refers to the aggregation of circuit elements which drive each pixel in an active-matrix type electro-optical device, and comprises, for example, TFTs (thin film transistors) or similar.

"Active matrix substrate" refers to general substrates on which is mounted peripheral circuitry, regardless of whether electro-optical elements are formed or not.

There is no particular restriction on "active elements", which may include, for example, TFTs and other transistors and diodes, or similar.

Here "holding element" refers to, for example, capacitors, memory, and other elements which hold electrical signals.

Normally, when an active element is in the non-conducting state, whereas ideally there should be no current flowing, a current, albeit slight, may flow; an active element having a "structure to prevent leakage currents during shutoff" refers to an active element configured with the object of preventing the occurrence of such a current (leakage current).

An example of such an element is a multi-gate type active element. A multi-gate type active element is an active element which functions as a single element, but strictly speaking comprises a plurality of active elements connected in series, configured to function similarly to a device with control terminals connected together.

In configuring a multi-gate type active element, the semiconductor layer may be in a curved shape, as in an embodiment described below, or the gate shape may be curved.

The second active element may be a transistor with a structure selected from the group consisting of an LDD structure, GDD structure, or DDD structure. Here "LDD" is an abbreviation of "Lightly Doped Drain"; "GDD" is an abbreviation of "Graded Diffused Drain"; and "DDD" is an abbreviation of "Double Diffused Drain". In a transistor having these structures, in order to limit the adverse effects of hot electrons and similar during fine MOSFET fabrication, the maximum electric field near the drain is weakened. For example, in such transistors the drain region of the transistor is lightly doped with impurities to relax the electric field in regions where impurity diffusion is performed and between silicon substrates; for example, n-type regions may be formed using self-alignment.

In such transistors, because the source-drain resistance while the transistor is turned off is extremely high and leakage currents are reduced, electric charge accumulated in the holding element is not released, and the electric potential applied to a control terminal can be maintained at a constant level.

A second active matrix substrate of this invention is an active matrix substrate comprising a plurality of unit circuits, arranged to correspond to the intersections of a plurality of data lines and a plurality of scan lines. Each of the above plurality of unit circuits comprises a first transistor, which comprises a first control terminal, first terminal, and second terminal; a holding element, connected to the above first control terminal, comprising a first electrode and a second electrode; and a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, wherein the above third terminal and the above fourth terminal are respectively connected to the above first terminal and to the above first electrode; and the above second transistor has a multi-gate structure.

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In the above active matrix substrate, in place of a multi-gate structure, the above second transistor may be a transistor with a structure selected from an LDD structure, GDD structure, or DDD structure.

By adopting a multi-gate structure and an LDD structure, GDD structure, or DDD structure, the leakage current when the second transistor is in the turned-off state can be reduced, so that the electric charge accumulated in the holding element can be maintained for a long period of time.

In the above active matrix substrate, it is preferable that the above first transistor and the above second transistor have different conduction types. In this case, it is preferable that the semiconductor film constituting the above first transistor and the semiconductor film constituting the above second transistor be separated.

For example, it is preferable that the above first transistor be p-type, and that the above second transistor be n-type.

The above active matrix substrate may further comprise a third transistor, comprising a fifth terminal, a sixth terminal, and a third control terminal, with the above third control terminal connected to one scan line among the above plurality of scan lines, and the above fifth terminal connected to one data line among the above plurality of data lines.

The above sixth terminal may be connected to the above third terminal and to the above first terminal.

In the above active matrix substrate, the above active matrix substrate may have a stacked-layer structure comprising a plurality of layers; the above plurality of layers may comprise a semiconductor layer, in which is formed a semiconductor film constituting the above first and second transistors, and a gate metal layer, in which are formed the above second control terminals; and in the above gate metal layer there may be formed at least one portion of at least one scan line among the above plurality of scan lines.

By this means, the above second control terminal and at least one portion of the scan line can be formed in the same process, so that manufacturing processes can be shortened.

In the above active matrix substrate, the above active matrix substrate may have a stacked-layer structure comprising a plurality of layers; the above plurality of layers may comprise a semiconductor layer, in which is formed a semiconductor film constituting the above first and second transistors, and a gate metal layer, in which are formed the above second control terminals; and in the above gate metal layer there may be formed at least one portion of at least one data line among the above plurality of data lines.

By this means, the above second control terminal and at least one portion of the data line can be formed in the same process, so that manufacturing processes can be shortened.

In the above active matrix substrate, the above active matrix substrate may have a stacked-layer structure comprising a plurality of layers; the above plurality of layers may comprise a semiconductor layer, in which is formed a semiconductor film constituting the above first and second transistors, a gate metal layer, in which are formed the above second control terminals, and a source metal layer, in which is formed a source electrode or drain electrode connected to the source or to the drain of the above second transistor; and at least one portion of at least one data line among the above plurality of data lines may be formed in the layer closer to the above semiconductor layer among the above source metal layer and the above gate metal layer.

By this means, when an electro-optical device is formed in which electro-optical elements are arranged above the active matrix substrate, at least one portion of a data line can be separated from the electrodes of electro-optical elements, so

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that operation delays due to stray capacitances occurring between electrodes and data lines can be reduced.

A third active matrix substrate of this invention comprises unit circuits, comprising transistors, as well as data lines and scan lines, and has a stacked-layer structure comprising a plurality of layers; the above plurality of layers comprises a semiconductor layer, in which is formed a semiconductor film constituting transistors, and a gate metal layer, in which are formed the gate terminals of the above transistors; and at least one portion of either the above scan lines, or the above data lines, or both, is formed in the above gate metal layer.

By this means, transistor gate terminals and at least one portion of the scan lines or data lines can be manufactured by the same process, so that manufacturing processes can be shortened.

A fourth active matrix substrate of this invention comprises unit circuits, comprising transistors, as well as data lines and scan lines, and has a stacked-layer structure comprising a plurality of layers; the above plurality of layers comprises a semiconductor layer, in which is formed a semiconductor film constituting transistors, a gate metal layer, in which are formed the gate terminals of the above transistors, and a source metal layer in which are formed the source electrodes or drain electrodes which are connected to the sources or drains of the above transistors; and at least one portion of either the above scan lines, or the above data lines, or both, is formed in the layer, among the above gate metal layer and the above source metal layer, which is closer to the above semiconductor layer.

In the above active matrix substrate, when an electro-optical device is formed in which electro-optical elements are arranged above the active matrix substrate, at least one portion of data lines or scan lines can be separated from the electrodes of electro-optical elements, so that delays in signal supply due to stray capacitances occurring between electrodes and data lines or scan lines can be suppressed.

In the above active matrix substrate, it is preferable that a unit circuit comprise a first transistor, comprising a first control terminal, a first terminal, and a second terminal; a holding element, connected to the above first control terminal, and comprising a first electrode and a second electrode; and a second transistor, comprising a third terminal, a fourth terminal, and a second control terminal, wherein the above third terminal and the above fourth terminal are respectively connected to the above first terminal and to the above first electrode; and that the unit circuit have at least a structure selected from an LDD structure, GDD structure, DDD structure, or multi-gate structure.

The LDD structure, GDD structure, DDD structure, and multi-gate structure are appropriate structures for suppressing current leaks, and so by employing such a configuration, the electric charge accumulated in the holding element can be maintained for long periods of time.

A first electro-optical device of this invention comprises the above active matrix substrate, and electro-optical elements.

A second electro-optical device of this invention comprises peripheral circuits to supply current to electro-optical elements provided for each pixel, corresponding to the above electro-optical elements; each of the above peripheral circuits comprises a light emission-controlling active element to supply current to the above electro-optical element during the light emission period, a holding element to hold a control voltage, a first active element the gate terminal of which is connected to the above holding element and which supplies a current based on the above control voltage applied to the gate terminal to the above electro-optical element, via the above

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light emission-controlling active element, a current-controlling active element which passes a constant current (or a data current) via the above first active element during the selection period, and a second active element connected between the above current-controlling active element and the above holding element, which charges the above holding element during the above selection period and which stores the above control voltage; and the above second active element comprises a structure to prevent leakage currents during shutoff.

As the above structure to prevent leakage currents, similarly to the case of the above active matrix substrates, for example, an LDD structure, GDD structure, DDD structure, or multi-gate structure can be adopted.

In the above electro-optical device, as the above first active element and the above second active element, it is preferable that, for example, a transistor be used. In this case, it is preferable that the transistors have different conduction types. For example, it is preferable that the above first active element be p-type, and that the above second active element be n-type.

Corresponding to this, a configuration may be adopted comprising a first driver circuit which supplies negative-logic data signals to the first active element, and a second driver circuit which supplies positive-logic scan signals to the second active element.

In the above electro-optical device, a configuration may be adopted comprising data lines which supply data signals to first active elements, and scan lines, intersecting the data lines, which supply scan signals to second active elements.

In the above electro-optical device, it is preferable that either the data lines or the scan lines be wired by means of the metal layer, among the source metal layer and the gate metal layer which comprise the first active elements and second active elements, which is separated from the common electrodes of the electro-optical elements. This is because if the metal layer which is more distant from the common electrodes is used, the stray capacitance arising between the signal lines and the common electrodes can be reduced.

Specifically, the scan lines may for example be wired using the gate metal layer which forms the gate terminals of the second active elements.

In the above electro-optical device, it is preferable that, among the plurality of active elements, the plurality of active elements having the same polarity be formed continuously and in planar fashion in the same semiconductor layer. This is because, if the semiconductor layer is thus made continuous, the area used for wiring can be reduced, and the aperture ratio can be increased.

At this time, connection points between a plurality of active elements having the same polarity comprise common contact holes, and wiring is performed from contact holes to active elements having a polarity differing from these active elements. This is because when the polarity is different, normal wiring must be performed. By this means, contact holes can be made common, and the area of occupation of connection portions in the entire area of the driving circuit can be reduced.

In one embodiment described below, a plurality of active elements having the same polarity comprises second active elements, light emission-controlling active elements, and current-controlling active elements; however, the present invention is of course not limited thereto.

As the gate terminals of the above second active elements and the above current-controlling active elements, common scan lines may be used; in this case, with respect to common

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gate terminal connections, by using scan lines without modification the wiring area can be reduced and the aperture ratio can be raised.

However, if the above second active elements and the above current-controlling active elements are not driven with the same timing, then of course different signal lines can be used as the respective gate terminals.

A third electro-optical device of this invention comprises electro-optical elements, and peripheral circuitry driving the above electro-optical elements; the above electro-optical elements are formed such that the boundaries of the electro-optical elements have at least a prescribed curvature, and at least a portion of the peripheral circuits is formed in the region surrounded by the boundaries having at least the prescribed curvature and by polygonal boundaries circumscribing the electro-optical elements.

A shape having a "prescribed curvature" is particularly effective when electro-optical elements are formed using liquid materials; in this case, it is desirable that the prescribed curvature be set according to the viscosity and surface tension of the liquid material, and according to the material of the layer below the electro-optical elements. However, even in cases where the electro-optical elements are formed by evaporation deposition or other means without using liquid materials, there is the advantageous result that short-circuits are prevented.

It is preferable that a plurality of boundary portions having this prescribed curvature be formed. It is also preferable that the plurality of boundary portions thus formed be arranged essentially symmetrically with respect to a center line passing through the geometric center of the electro-optical element.

For example, a portion of the peripheral circuit formed in this region is a contact hole comprised by wiring of the peripheral circuit. It is preferable that this contact hole be of polygonal shape compatible with the shape of the region. A contact hole comprised by the wiring of the peripheral circuit is, for example, a contact hole which supplies current to at least one of the electrodes of the electro-optical element. It is preferable that there be a plurality of contact holes, arranged essentially symmetrically with respect to a center line passing through the geometric center point of the above electro-optical element.

When using a liquid material to form electro-optical elements, by providing an affinity-controlling layer which adjusts the affinity for the liquid material near the boundaries of electro-optical elements, the film thickness of the functional layer constituting the electro-optical elements can be controlled, and flatness can be improved. Also, by making the affinity for the liquid material of, at least, the walls of the bank layer different from that of the above affinity-controlling layer, the effectiveness may be further increased. For example, by making the affinity for the liquid material of the walls of the bank layer lower than that of the affinity-controlling layer, the film formed by the liquid material no longer adheres to the walls of the bank layer, and the flatness of the film formed by the liquid material is further improved.

This affinity-controlling layer may be formed so as to have a staircase-shape on the inside of the electro-optical elements with respect to the walls formed by the bank layer.

Here a "bank" is a partition member to partition pixel regions. A bank is also effective for securing a distance from cathodes or common electrodes and data lines, scan lines, or other wiring which supplies signals. By securing a sufficient distance, the parasitic capacitance is reduced, and delays when supplying signals can be suppressed.

In general, data signals are greatly affected by stray capacitances of scan signals, which can cause operation delays, and

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so a sufficient distance must be secured between data signals and common electrodes or cathodes.

It is preferable that, in boundary portions having a prescribed curvature, at least one of the electrodes constituting the electro-optical element be patterned according to the shape of the boundary portion. This is because, by patterning electrodes in a manner compatible with the curvature, at least a portion of the peripheral circuit can be arranged more easily. For example, at least a portion of the peripheral circuit is a contact region to enable connection between the peripheral circuit and the above electrode.

A fourth electro-optical device of this invention comprises a light-emitting portion, and a peripheral circuit which controls the current supplied to the above light-emitting portion via a pixel electrode; the area of the above light-emitting portion is smaller than the area of the above pixel electrode, and the shape of the above light-emitting portion is different from the shape of the above pixel electrode.

A fifth electro-optical device of this invention comprises a light-emitting portion, and a peripheral circuit which controls the current supplied to the above light-emitting portion via a pixel electrode; the area of the above light-emitting portion is smaller than the area of the above pixel electrode; the shape of the above light-emitting portion is a shape having a curvature, and the shape of the above pixel electrode is polygonal.

A sixth electro-optical device of this invention comprises a light-emitting portion, and a peripheral circuit which controls the current supplied to the above light-emitting portion via a pixel electrode; the area of the above light-emitting portion is smaller than the area of the above pixel electrode; the above light-emitting portion has a polygonal shape having n vertices (where n is an integer equal to 4 or greater); the above pixel electrode has a polygonal shape having m vertices (where m is an integer equal to 3 or greater); and the relation $n > m$ obtains.

In the above electro-optical device, the light-emitting portion has a shape having a curvature, or has a polygonal shape with four or more vertices, so that short-circuits in the edge portions of light-emitting portion can be prevented. And when forming light-emitting portions using a liquid material, the liquid material can be made to extend thoroughly to the edge portions of light-emitting portions, so that a uniform film can be formed.

In the above electro-optical device, it is preferable that the entire region of the above light-emitting portion be formed on the above pixel electrode, and that a contact region for connection to the above peripheral circuit and to the above pixel electrode be provided in the portion of the above pixel electrode where the above light-emitting portion is not formed.

A seventh electro-optical device of this invention comprises an electro-optical element, a holding capacitance which regulates the current supplied to the above electro-optical element, and an active element which supplies a current according to the voltage recorded in the holding capacitance; a first electrode constituting the holding capacitance is formed by patterning a portion of a metal layer which forms a power supply line supplying current to the electro-optical element.

An eighth electro-optical device of this invention is configured to enable the supply of current to an electro-optical element by an active element according to the voltage recorded in a holding capacitance, and comprises a first metal layer connected to a power supply, and a second metal layer patterned to comprise a portion of a control terminal of an active element; a first electrode constituting the holding capacitance is formed by patterning a portion of the first metal layer.

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Here "layer" comprises, in addition to a metal layer, a layer which affects formation of the holding capacitance, such as for example a semiconductor layer.

A second electrode constituting the holding capacitance is formed by patterning a portion of the metal layer which forms the control terminal of the active element.

In the above electro-optical device, the above first electrode may be a portion of the power supply line, and a portion of the metal layer forming the control terminal of the active element in a portion of the power supply line may be overlapped in patterning to form the above second electrode. By means of this configuration, there is no need in particular to provide wiring to connect the holding capacitance and the active element, so that the aperture ratio can be increased.

It is preferable that a semiconductor layer be comprised, overlapping electrodes constituting the holding capacitance and formed in the shape of the electrodes. This semiconductor layer may for example have impurities introduced. The semiconductor layer may be doped with impurities to metallize or to lower the resistance.

It is preferable that the holding capacitance be formed in a region other than the region in which the electro-optical element and active element are formed, so that the aperture ratio is raised. For example, each of the layers comprising the electrodes of the holding capacitance may be formed on a polygon, such as for example a pentagon, corresponding to the shape of the region other than the region in which are formed the electro-optical element and active element.

In the above electro-optical device, it is preferable that, of the layers comprising the holding capacitance electrodes, the region occupied by the layer positioned on the lower side be formed to be greater than the region occupied by the layer positioned on the upper side.

In the above electro-optical device, the region occupied by the layer positioned on the lower side is formed by patterning into a shape such that, even if the greatest possible position shift that can occur during formation of the layer positioned on the upper side occurs, the region of the layer positioned on the upper side is contained within the region of the layer positioned on the lower side.

In the above electro-optical device, it is preferable that a bank layer be further comprised in order to isolate neighboring electro-optical elements, and that the holding capacitance be formed under the bank layer.

In addition, an affinity-controlling layer may be further comprised, within the bank layer or below the bank layer, in order to control the affinity of the liquid material during formation of electro-optical elements.

The overlap region in which is formed the holding capacitance may be provided in a region in which at least one among the first metal layer and the second metal layer is formed in a power supply wiring pattern.

It is further preferable that the wiring pattern formed by the second metal layer be positioned at a prescribed distance or greater from at least one among the two electrodes connected to the electro-optical element. By means of this configuration, unwanted capacitance can be reduced.

A fifth active matrix of this invention is an active matrix substrate comprising pixel electrodes and paths positioned corresponding to the intersections of data lines and scan lines; the above pixel electrodes are connected to a power supply line via at least one transistor; a holding element connected to the gate of the above one or more transistors is provided; and a first electrode constituting the above holding element is connected to the above power supply line.

A sixth active matrix substrate of this invention is an active matrix substrate comprising pixel electrodes and paths posi-

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tioned corresponding to the intersections of data lines and scan lines; the above pixel electrodes are connected to a power supply line via at least one transistor; a holding element connected to the gate of the above one or more transistors is provided; and a first electrode constituting the above holding element is a portion of the above power supply line.

In the above active matrix substrate, a second electrode constituting the above holding element is the gate of the above one or more transistors.

A seventh active matrix substrate of this invention is an active matrix substrate comprising unit circuits each comprising a transistor, corresponding to the intersections of scan lines and data lines; a semiconductor film constituting the above transistors is formed in a semiconductor layer; at the intersections of the above scan lines and the above data lines, either the above scan line or the above data line is formed in a first conducting layer; and the portions of the above scan line and the above data line other than at the above intersection are formed in a second conducting layer. In this active matrix substrate, it is preferable that the above second conducting layer be positioned between the above first conducting layer and the above semiconductor layer.

By combining the above active matrix substrate with electro-optical elements, an electro-optical device can be configured.

A ninth electro-optical device of this invention is an electro-optical device comprising electro-optical elements corresponding to the intersections of scan lines and data lines; either the above scan lines or the above data lines are formed in a first conducting layer at the intersections of the above scan lines and the above data lines, together with a pair of electrodes which supply power to the above electro-optical element; the portions of the above scan lines and the above data lines other than in the above intersections are formed in a second conducting layer; and the above second conducting layer is positioned at a greater distance than the above first conducting layer from one of the above pair of electrodes.

Here, the above electro-optical elements may be electroluminescence (EL) elements. "Electroluminescence elements" refer in general to elements, whether employing an organic or an inorganic (such as Zn:S) light-emitting material, which utilize electroluminescence phenomena in which the application of an electric field causes holes injected from an anode and electrons injected from a cathode to recombine, so that the recombination energy causes the light-emitting material to emit light. As the layer structure enclosed between the electroluminescence element, in addition to a light-emitting layer comprising light-emitting material, a hole transport layer or an electron transport layer, or both, may also be comprised. Specifically, as layer structures, in addition to a cathode/light-emitting layer/anode structure, a cathode/light-emitting layer/hole transport layer/anode, cathode/electron transport layer/light-emitting layer/anode, cathode/electron transport layer/light-emitting layer/hole transport layer/anode, or similar may be adopted.

The above active matrix substrates may also be employed in electronic device. Here there is no particular restriction on "electronic device", which includes a device comprising a display device comprising an active matrix substrate, such as for example portable telephones, video cameras, personal computers, head-mounted displays, rear- or front-projectors, and also fax machines with display functions, the viewfinder of digital cameras, portable TV sets, DSP devices, PDAs, electronic organizers, and similar.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an overall drawing of a display panel of this embodiment;

FIG. 2 is a plane view of a pixel region in embodiment 1;

FIG. 3 shows plane views of a pixel region in embodiment 1; FIG. 3A is a cross-section along A-A in FIG. 2, FIG. 3B is a cross-section along B-B in FIG. 2, and FIG. 3C is a cross-section along C-C in FIG. 2;

FIG. 4 shows examples of modification of the boundary shape of the light-emitting portion; FIG. 4A shows the case of a circular light-emitting portion, FIG. 4B shows the case of a light-emitting portion having a curved portion symmetrical about a center line, and FIG. 4C shows the case of a light-emitting region having a curved portion asymmetrical about a center line;

FIG. 5 is a circuit diagram of a pixel region in embodiment 1;

FIG. 6 is a drawing explaining the alignment of a metal layer in embodiment 1;

FIG. 7 is a drawing explaining processing to separate gate metal in embodiment 1;

FIG. 8 is a plane view of a pixel region in embodiment 2;

FIG. 9 shows cross-sectional views of a pixel region in embodiment 2; FIG. 9A is a cross-section along A-A in FIG. 8, FIG. 9B is a cross-section along B-B in FIG. 8, and FIG. 9C is a cross-section along C-C in FIG. 8;

FIG. 10 is a plane view of a pixel region in embodiment 3;

FIG. 11 shows cross-sectional views of a pixel region in embodiment 3; FIG. 10A is a cross-section along A-A in FIG. 10, and FIG. 10B is a cross-section along B-B in FIG. 10;

FIG. 12 is a plane view of a pixel region in embodiment 4;

FIG. 13 shows cross-sectional views of a pixel region in embodiment 4; FIG. 13A is a cross-section along A-A in FIG. 12, and FIG. 13B is a cross-section along B-B in FIG. 12;

FIG. 14 is a connection diagram for a display panel in embodiment 5; and,

FIG. 15 shows examples of electronic device in embodiment 5, showing examples of application of a display panel of this invention to a portable telephone in FIG. 15A, to a camcorder in FIG. 15B, to a portable personal computer in FIG. 15C, to a head-mounted display in FIG. 15D, to a rear projector in FIG. 15E, and to a front projector in FIG. 15F.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Next, preferred embodiments of the invention are explained, referring to the drawings as examples. The following embodiments are no more than examples of embodiments of this invention, and do not limit the scope of application.

Embodiment 1

This embodiment of the invention relates to a display panel which is an electro-optical device employing EL elements as electro-optical elements. FIG. 1 is an overall drawing of a display panel comprising an active matrix panel, comprising EL elements.

As shown in FIG. 1, the display panel 1 is configured by positioning a display region 11 and driver regions 14 and 15 on a glass substrate 16. A cathode 12 is formed over the entirety of the display region 11, and is connected to the cathode lead electrode 13. Pixel regions 10 are arranged in a matrix in the display region 11. In the case of a color display, the pixel regions 10 are configured to enable emission of primary colors (for example, the three primary colors red,

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blue, green) taken as necessary for color display; a combination of pixel regions emitting light of each primary color becomes one pixel element. For example, the driver region **15** positioned in the column direction of the display region **11** outputs a write control line Vsel and a light emission control line Vgp; and the driver region **14** positioned in the row direction of the display region **11** outputs, in addition to the power supply line Vdd, data current signals to the data line Idata. By controlling the light-emission state in each pixel region **10** by means of driver circuits, not shown, formed in the driver regions **14** and **15**, an arbitrary image can be displayed in the display region **11**.

FIG. 2 shows a plane view which explains the wiring pattern in one pixel region and the periphery. In FIG. 2, the patterns can be seen in the semiconductor layer **102**, which is particularly important and is shown in FIG. 3, in the gate metal layer **104**, source metal layer **106**, and anode layer **110**.

As shown in FIG. 2, the light-emitting portion OLED and peripheral circuitry to drive this portion are all positioned in the region enclosed by the power supply line Vdd and the data line Idata. The power supply line Vdd is positioned at a distance from the data line Idata, with the light-emitting portion OLED intervening. The peripheral circuit comprises a transistor T1 as a first active element, a transistor T2 as a second active element, a transistor T3 as a current-controlling active element, a transistor T4 as a light emission-controlling active element, and a holding capacitor C as a holding element. No restrictions in particular are placed on the conduction types of the transistors T1 to T4, but in this embodiment, the conduction type of transistor T1 is p type, and that of all the other transistors is n type.

The source of the transistor T1 is connected to the power supply line Vdd, and the drain is connected to the drain side of transistor T4. The source of transistor T4 is connected to the anode of the light-emitting portion OLED. The holding capacitor C is formed between the power supply line Vdd and the gate of transistor T1. The source of transistor T2 is connected to the holding capacitor C and to the gate of transistor T1, and the drain is connected to the drain of transistor T3 and between transistors T1 and T4. The source of transistor T3 is connected to the data line Idata, and the gate is connected, in common with the gate of transistor T2, to the write-control line Vsel.

FIG. 3 shows cross-sections to explain the layer structure in each of the cross-sectional planes shown in FIG. 2. FIG. 3A, FIG. 3B, and FIG. 3C show the layer structure in the A-A cross-sectional plane, B-B cross-sectional plane, and C-C cross-sectional plane, respectively.

As shown in FIG. 3A, the pixel region **10** is configured by stacking, on the glass substrate **100** (the glass substrate **16** in FIG. 1), an underlayer protection film **101**, semiconductor layer **102**, gate insulating film **103**, gate metal layer **104**, first interlaminar insulating film **105**, source metal layer **106**, second interlaminar insulating film **107**, bank layer **108**, and cathode layer **109** (the cathode **12** in FIG. 1). Further, as shown in FIG. 3B and FIG. 3C, the electric field light-emitting portion OLED is configured by stacking an anode layer **110**, hole transport layer **111**, and light-emitting layer **112**.

As the glass substrate **100**, because the EL elements of this embodiment emit light on the substrate side and it is necessary that light be transmitted, soda lime glass, low-expansion glass, quartz glass, and other non-alkaline glasses are employed. However, when an optically transmissive material is used as the cathode layer **109** and EL elements are configured such that light is emitted from the cathode side, it is also possible to use metal or other conductive materials, as well as

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silicon carbide (SiC), alumina (Al₂O₃), aluminum nitride (AlN), and other non-transparent insulating materials.

As the underlayer protective film **101**, silicon oxide film (SiO_x: 0<x≤2), silicon nitride film (Si₃N_x: 0<x≤4), and other insulating materials can be used. The underlayer protective film is formed in order to prevent sodium (Na) and other mobile ions contained in the glass substrate from penetrating into the semiconductor layer and exerting adverse effects on impurity control in the semiconductor layer.

After first washing the substrate **100** with deionized water and alcohol or another organic solvent, the underlayer protection layer **101** is formed on the substrate by atmospheric-pressure chemical vapor deposition (APCVD), low-pressure chemical vapor deposition (LPCVD), plasma-enhanced chemical vapor deposition (PECVD), or another CVD method, or by sputtering.

As the semiconductor layer **102**, in addition to a group IV single-element semiconductor layer of silicon (Si), germanium (Ge) or similar, a complex with a group IV element, such as silicon germanium (Si_xGe_{1-x}: 0<x<1), silicon carbide (Si_xC_{1-x}: 0<x<1), or germanium carbide (Ge_xC_{1-x}: 0<x<1), as well as a compound of group III and group V elements such as gallium arsenide (GaAs) and indium antimonide (InSb), a compound of group II and group VI elements such as cadmium selenide (CdSe), or other different complex compounds such as silicon germanium gallium arsenide (Si_xGe_yGa_zAs_z: x+y+z=1), can be employed.

The semiconductor layer **102** is formed by first depositing silicon or similar by, for example, the APCVD, LPCVD, PECVD or other CVD method, or by sputtering, evaporation deposition, or other PVD method, and then irradiating with laser light to induce a polycrystalline structure. As the laser light, the fundamental and higher harmonics of an excimer laser, argon ion laser, or YAG laser are used as appropriate. For example, when a polycrystalline structure is induced in silicon, polysilicon is obtained. This polycrystalline semiconductor layer **102** is patterned so as to be compatible with the element shapes of the holding capacitance C and each of the TFTs (thin film transistors) T1 to T4. For example, by performing reactive ion etching using a mixture of CF₄ and oxygen gases, a semiconductor layer in an amorphous state can be patterned into an island morphology compatible with element shapes. After patterning, for example, a gate metal layer is formed, and then the gate metal layer is used as a mask to introduce impurities into the semiconductor layer. Specifically, phosphorus (P), arsenic (As), antimony (Sb), or other donor elements are added for each element to obtain n-type semiconductor layer, and boron (B), aluminum (Al), gallium (Ga), indium (In), and other acceptor elements are added to obtain p-type semiconductor layer. In this embodiment, impurities are introduced such that the semiconductor layer constituting the holding capacitor C are n-type semiconductor layer. When TFTs with an LDD structure are employed and the threshold voltage of the TFTs is to be adjusted, channel doping to introduce impurities in low concentrations is performed.

As the gate insulating film **103**, for example, a silicon dioxide film is formed using tetraethyl orthosilicate (TEOS) as the raw material. The gate insulating film **103** is formed by, for example, plasma CVD in a microwave-discharge plasma, ECR plasma, or other oxygen or nitrogen atmosphere.

As the gate metal layer **104**, a conductive material such as, for example, tantalum (Ta), tungsten (W), chromium (Cr), or aluminum (Al) is used. The gate metal layer **104** is formed by first depositing a film by sputtering or other means, and then patterning into the shape of a gate electrode.

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As the first interlaminar insulating film **105**, silicon oxide, silicon nitride, or some other insulating film can be used. The first interlaminar insulating film is formed by sputtering or similar, and, for example, contact holes are then formed in order to form TFT source and drain electrodes.

As the source metal layer **106**, in addition to aluminum (Al), for example, tantalum, molybdenum, titanium, tungsten, or some other conductive material can be used. The source metal layer is formed by using sputtering or another method to uniformly layer a conductive material, and then patterning according to the electrode shape.

As the second interlaminar insulating film **107**, silicon oxide, silicon nitride, or some other insulating film can be used. The second interlaminar insulating film is formed by sputtering or other means, and then, for example, contact holes **h1** and **h2** for the anode layer **110** are formed.

As the anode layer **110**, for example, indium tin oxide (ITO) alloy or some other optically transmissive conducting material can be used. When there is no need for optical transmission properties, tin oxide (NESA), gold, silver, platinum, copper, or another material can be used as the anode layer. After using sputtering or some other method to form the anode layer, patterning is performed according to the shape of the light-emitting portion OLED. No restrictions in particular are placed on the shape of the anode layer (or the pixel electrodes), but it is desirable that the area be larger than that of the light-emitting portion OLED. Through such a configuration, a contact region for electrical connection of a peripheral circuit or pixel circuit with the pixel electrodes can be provided in a region other than the light-emitting portion of the pixel electrodes. Through such a configuration, the flatness of, at least, the light-emitting portion can be improved.

As the bank layer **108**, silicon oxide, silicon nitride, polyimide, or some other insulating material can be employed. The bank layer is formed by deposition using sputtering or a similar method, after which an aperture portion is provided in a position corresponding to the light-emitting portion OLED.

As the hole transport layer **111**, for example, N,N'-diphenyl-N,N'-bis-(3-methylphenyl)-(1,1'-biphenyl)-4,4'-diamine (TPDA) is used. The hole transport layer is deposited in the aperture portion provided in the bank layer **109**, using a metal mask or similar.

As the light-emitting layer **112**, for example, tris-(8-quinolinol) aluminum (Alq₃) or another arbitrary light-emitting material is used. The light-emitting layer can be formed by evaporation deposition using a metal mask or silicon mask; however, an ink jet method may be employed to arrange a solvent comprising the light-emitting material in the aperture portion, after which the solvent component is caused to evaporate.

As the cathode layer **109**, a material the energy level of which enables use as the cathode of an EL element, such as aluminum or an alloy of aluminum with another element (such as lithium), or calcium or similar, is used. The cathode layer is formed using a metal mask or similar, and is patterned by photolithography or using a shadow mask method.

In this embodiment, pixel electrodes are anodes and the common electrode is a cathode; however, a configuration may be employed in which the pixel electrodes are cathodes and the common electrode is an anode. Typically, cathode materials are often metals, but when the pixel electrodes are cathodes, the light emitted by the light-emitting portion OLED is then emitted on the side opposite the substrate **100**. Of course, even when the pixel electrodes are anodes and the common electrode is a cathode, by using a transparent material as the

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cathode material, or by making the film thickness sufficiently thin that light is transmitted, light can be emitted on the side opposite the substrate **100**.

Below, several features regarding wiring patterns in this embodiment are explained in sequence.

Planar Shape of the Light-Emitting Portion

One method of manufacture of EL elements involves using an ink jet method to discharge a liquid material comprising a light-emitting material, carrier transport material or carrier blocking material into an aperture portion, followed by drying, to form the light-emission layer. In this manufacturing method, it is important that the discharged liquid material extend uniformly to all areas of the aperture portion. If the liquid material does not extend uniformly, the thickness of the light-emitting layer after film deposition is uneven, the intensity of light emitted within the light-emitting region is uneven, and the image quality of the display panel is diminished. If for example it is supposed that the planar shape of the aperture portion is square, then under the influence of the surface tension and viscosity of the liquid material, the height of the surface of the liquid material discharged into the corners of the aperture portion will differ from other areas. Hence there is the possibility that for a light-emitting portion with such a shape, the thickness of the light-emitting layer after film formation will be uneven.

On the other hand, there is a need to increase the brightness of the display panel, and so there are requests to increase insofar as possible the size of the region in which light is emitted, that is, the light-emitting portion, and to reduce insofar as possible the region occupied by peripheral circuitry, that is, to raise the aperture ratio. The pattern layout cannot be designed considering only the ease of manufacture.

In order to satisfy all these requests, in this embodiment the boundaries of the light-emitting portion are formed so as to have at least a prescribed curvature, and at least a portion of the peripheral circuit is formed in the region surrounded by these boundaries having the prescribed curvature and the boundaries of a polygon circumscribing the boundaries of this light-emitting portion.

Based on FIG. 4, a specific concept is explained. FIGS. 4A, 4B and 4C show, partially or entirely, the planar shape of a light-emitting portion to which the concept of this invention is applied. FIG. 4A is the case in which the boundary of the light-emitting portion is circular, that is, the entire boundary has a fixed curvature R. A portion of the peripheral circuit is provided within the region, indicated by shading, enclosed by this circle and by a polygon circumscribing the circle, that is, the square shown by a broken line. The light-emitting portion of this circle is regarded as having an ideal shape for rendering uniform the film thickness of the light-emitting portion, insofar as the shape is symmetrical about any center line passing through the center. However, as shown in FIG. 4A, effective utilization of the shaded portion is necessary in order to improve the aperture ratio of the light-emitting portion.

FIG. 4B is an example in which this invention is applied to the corners of a rectangular shape; in this example, the boundaries of the light-emitting portion are provided with a fixed curvature R. In this example, the circumscribing polygon is a rectangle, shown by a broken line; the shaded regions surrounded by the boundaries of the light-emitting portion and the boundaries of the rectangle are the regions in which a portion of, or the entirety of, the peripheral circuit is provided. The present embodiment pertains to this example; as the curvature R is increased, an oblong planar shape for the light-emitting portion results, such as in this embodiment. In this example also, the shape is symmetrical laterally and vertically about a center line passing through the center of the

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light-emitting portion, and moreover the curvature of the corner portions is equal to or greater than a fixed value, so that a light-emitting portion with uniform film thickness can be formed.

FIG. 4C is an example in which the curvature of the corner portions is set to be unequal with respect to a center line. The curvature R1 of the corner portion on the left side facing the drawing is smaller than the curvature R2 of the corner portion on the right side.

In this example, the circumscribing polygon is a rectangle, shown by a broken line, and the shaded regions surrounded by the boundaries of the light-emitting portion and the boundaries of the rectangle are regions in which a portion of or the entirety of the peripheral circuit is provided. Even when the curvature is unequal in this way, by setting the minimum curvature to be greater than or equal to a constant value, a light-emitting portion with uniform film thickness can be formed. Because the minimum curvature is affected by the viscosity and surface tension of the discharged solution, and by the water repellence or liquid repellence (affinity to water or to liquids) of the discharge surface, the minimum curvature should be determined by experiment for each set of conditions.

In this embodiment, a light-emitting portion with a rectangular planar shape, such as shown in FIG. 2, is adopted. And, a portion of the peripheral circuit, namely, the contact holes h1 and h2 (see FIG. 3B), is formed within the region surrounded by the boundaries of the light-emitting layer and the boundaries of the rectangle (not shown) circumscribing the boundaries of the light-emitting portion. In this embodiment, the regions indicated by shading in FIG. 4B which normally are wasted space are used for these contact holes, and this satisfy demands for effective use of space.

In addition to contact holes, any other elements of the peripheral circuit, such as for example transistors and capacitors, may be formed in the regions surrounded by the boundaries of the light-emitting portion and the boundaries of a polygon circumscribing the light-emitting portion. Moreover, it is not necessary to include the entirety of an independently functioning element in these regions; a portion of an element or contact, that is, a portion of the peripheral circuit, may be included in the region. In other words, it is essential that placement be performed so as to make effective use of space.

In cases where a liquid material is not used to form the light-emitting portion, even when, for example, evaporation deposition or similar is used to form the light-emitting portion, by employing a shape in which the edge portions of the light-emitting portion have a curvature, there is the enduring advantage that the danger of short-circuits between the pixel electrode at the edge portions of the light-emitting portion OLED and the common electrode is reduced.

Strictly speaking, a curvature can be represented as a collection of fine straight lines, and so the shape of the light-emitting portion can be interpreted as a polygon having more numerous vertices than the shape of the pixel electrode.

Contact Holes for the Light-Emitting Portion

In an EL element, provision of a contact hole in a region surrounded by the boundaries of the light-emitting portion and the boundaries of a polygon circumscribing the light-emitting portion, as shown in FIG. 2, is significant. In other words, by providing a comparatively large contact hole in this region, the region can be used effectively, and sufficient current can be supplied to the light-emitting portion.

It is further preferable that a plurality of contact holes be provided. That is, in the EL element, a certain amount of current in the light-emitting layer must be passed uniformly

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to the entirety of the light-emitting portion. If a contact hole used for connection to an anode directly supplying current is provided in an eccentric position, the supply of current may be uneven. An uneven supply of current appears as irregularities in the intensity of light emission.

If, as in this embodiment, a plurality of contact holes are provided in positions which are symmetrical with respect to a center line passing through the center of the light-emitting portion, then this problem can be resolved. That is, as shown in FIG. 2, in this embodiment a plurality of comparatively large contact holes are provided in regions provided symmetrically with respect to a prescribed center line passing through the center of the light-emitting portion. By providing these contact holes in symmetrical regions, the demand for uniform film deposition in the light-emitting portion, as well as the demand that current supplied to the light-emitting portion be uniform, can both be satisfied.

Alignment of Metal Layers

Depending on the EL element driving method, the stability of the current supplied to the light-emitting portion may be affected by fluctuations in the holding capacitance. In this embodiment also, it is undesirable for the capacitance value of the holding capacitor C to fluctuate either from one pixel to another, or from one display panel to another. However, when stacking metal layers in a process to manufacture a display panel, there may occur shifts from planned positions. Because the numerical area of overlapping metal layers determines the holding capacitance, shifts in position give rise to fluctuations or scattering in capacitance values, and there are cases in which capacitance values of holding capacitances may cause fluctuations either among pixel regions, or among display panels.

Hence in this embodiment, in the vicinity of overlapping regions forming the holding capacitor C, among the plurality of layers related to formation of the holding capacitor C, that is, among the source metal layer 106, gate metal layer 104, and semiconductor layer 102, the occupied region or width of a layer positioned on the lower side (relative to the source metal layer, the gate metal layer and semiconductor layer) is formed to be larger than the occupied region or width of the layer positioned on the upper side (relative to the semiconductor layer, the gate metal layer and source metal layer; relative to the gate metal layer, the source metal layer).

This feature can be seen in the plane view of FIG. 2, but is explained in greater detail referring to the A-A cross-section shown in FIG. 6. As shown in FIG. 6, if the width of the source metal layer 106 is d1, the width of the gate metal layer 104 is d2, and the width of the semiconductor layer 102 is d3, then the relation $d3 > d2 > d1$ obtains. The lower the layer, the larger is the pattern shape.

The extent to which [the pattern shape] should be increased will vary depending on the precision of the manufacturing processes and the pattern density. As one approach, patterns should be formed for each layer such that, when forming layers positioned on the upper side, even when the maximum possible shift in position occurs, the region in the layer positioned on the upper side will be contained within the region in the layer positioned on the lower side. In this embodiment also, the differences $d3 - d2$ and $d2 - d1$ are designed to be equal to or greater than predicted position shifts in manufacturing processes.

Formation of Separations Between Gate Metal Layers

EL elements comprise a common electrode; the common electrode is formed over the entirety of the display region. In this embodiment also, a cathode 13 (cathode layer 109) is formed over the entirety of the display region 11 as shown in FIG. 1 as the common electrode for the light-emitting portion

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OLED. However, if the common electrode is formed over the entirety, there is the problem that a capacitance occurs with the gate metal layer connected to the gates of transistors. If such stray capacitance appears, lags occur in transistor operation, and operation with the timing of the design cannot be guaranteed.

Hence in this embodiment, the wiring pattern formed by the gate metal layer is positioned with a separation of at least a prescribed distance from at least one among the electrodes of the light-emitting layer. A problem due to low impedance arises due to the distance between the cathode layer 109 which is the common electrode and the gate metal layer 104. Also, the cathode layer 109 is a small distance from the lower side in the light-emitting portion OLED, so that the distance from the gate metal layer in the vicinity of the light-emitting portion poses a problem. Hence in this embodiment, as shown in FIG. 7 (equivalent to the C-C cross-section in FIG. 2), patterns are formed such that, near the light-emitting portion, the distance d1 in the depth direction between the cathode layer 109 and the gate metal layer 104 and the distance d2 in the plane are both equal to or greater than a prescribed distance.

Here the prescribed distance will change variously depending on the area of the gate metal layer and the dielectric constants of intervening layers, and so cannot be specified generally; however, it is preferable that patterning should be at as great a distance as possible, within the range allowed by the area of pixel regions and other.

Wiring to supply data signals, scan signals, and other electrical signals must be laid out in consideration of operation delays caused by stray capacitances. In this embodiment, the data lines Idata and scan lines Vsel use the gate metal layer 104 which is at a greater distance from the cathode 109 which is a common electrode, and at the intersections between data lines Idata and scan lines Vsel, data lines Idata are formed in the source metal layer 106, but the portions of data lines Idata outside intersections and the scan lines Vsel are formed in the gate metal layer 104.

When it is necessary to further reduce the stray capacitances to which data lines Idata contribute, the entirety of the data lines Idata may be formed in the conducting layer which is at the greatest distance from the common electrode. To give an explanation corresponding to this embodiment, at the intersections between data lines Idata and scan lines Vsel, scan lines Vsel are formed in the source metal layer 106, and the entirety of data lines Idata as well as the portion of scan lines Vsel outside intersections may be formed in the gate metal layer 104.

In order to remove signals lines such as scan lines and data lines farther from the common electrode and from pixel electrodes, a conducting layer may be formed in the same layer as the semiconductor layer 102; and, if a so-called bottom-gate configuration for transistors is employed, then the conducting layer may be provided below the semiconductor layer, and this conducting layer can be used for wiring of signal lines.

Operation of Peripheral Circuits

Next, the operation of the peripheral circuit of an EL element of this embodiment is explained. FIG. 5 shows a circuit diagram for one pixel circuit constituting the pixel region 10.

1) The circuit of this embodiment has a circuit configuration which operates through the supply of current data as data signals. Pixel display begins with the selection of the write control line Vsel as a data writing operation, putting the transistors T2 and T3 into the turned-on state.

2) When the transistors T2 and T3 are put into the conducting state, the transistor T1 reaches a steady state after a pre-

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scribed time, and electric charge accumulates in the holding capacitor C according to the data current Cdata.

3) As light emission action, the write control line Vsel is put into the unselected state, the transistors T2 and T3 are turned off, and after stopping supply of the data current Cdata, the light emission control line Vgp is selected. As a result, the transistor T4 is turned on, and a current corresponding to the potential difference Vgs between the voltage stored in the holding capacitor C and the power supply voltage Vdd is supplied to the light-emitting portion OLED via the transistors T1 and T4, so that light is emitted from the light-emitting layer.

Improvement of Current Maintenance Performance in Peripheral Circuits

Below, features of this embodiment in the peripheral circuitry are explained.

In the prior art, no consideration in particular has been paid to active elements controlling the charging and discharging of holding capacitances. In miniaturized FETs, when the gate voltage is below the threshold, the drain current also depends on the drain voltage. That is, the injection current in the source-drain channel increases as an exponential function of the gate voltage, and leakage currents occur. For example, when a leakage current occurs in transistor T2 shown in FIG. 5, the cross-terminal voltage Vgs of the holding capacitor C deviates from the value corresponding to the supplied data signal, and the drain current of the transistor T1 which takes this voltage as a control voltage for input to its gate fluctuates. This fluctuation appears as a change in brightness in the light-emitting portion OLED, so that light emission at a stable brightness can no longer be guaranteed.

Hence in this embodiment, as shown in FIG. 1 and FIG. 5, transistor T2 which is an active element directly connected to the holding capacitor C is an active element with multiple control terminals, that is, a multi-gate type transistor. Using such a transistor, as indicated by the arrow in FIG. 5, is for practical purposes equivalent to directly connecting a plurality of transistors, and the leakage current is greatly suppressed. A current corresponding to the supplied data signal is reliably supplied to the light-emitting portion OLED.

As the transistor T2, instead of, or in addition to, a multi-gate type structure, an LDD, GDD, or DDD structure can also be employed. By employing such a structure, the leakage current can be reduced, and adverse effects due to hot electrons when a FET is miniaturized are suppressed, so that element reliability is enhanced.

In this embodiment, in consideration of the polarity of control signals, transistor T1 and transistor T2 have opposite polarities, that is, transistor T1 is a p-type FET, and transistors T2 to T4 are n-type FETs. However, whether to use a p-type or an n-type [transistor] can be decided arbitrarily according to the polarity and other details of signals which are to be used, and no restrictions apply.

Moreover, the placement of elements is not limited to that of FIG. 5. For example, the electrical potential relationships of the holding capacitor, transistor T1, and light-emitting portion OLED can be reversed. In this case, it is desirable that the common electrode of the light-emitting portion be an anode, and that the polarities of each of the transistors (whether n-type or p-type) be reversed.

Reduction of Peripheral Circuit Space

As explained above, in order to increase the brightness or aperture ratio in a display device, it is demanded that the region occupied by peripheral circuitry be decreased as much as possible. To this end, in this embodiment a wiring pattern is formed such that at least one active element among the plurality of transistors and other active elements is connected

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to another active element by the same contact hole. Specifically, as shown in FIG. 2, transistors T2, T3, and T4 are interconnected by the same contact hole h3. In this way, the layout is optimized such that there are more numerous common connection points or contacts in a circuit, and by arranging elements such that portions which are common contact points are connected by the same connection points, the number of contact holes can be reduced and the area occupied by the peripheral circuitry is reduced due to these contact holes.

Embodiment 2

FIG. 8 shows a plane view explaining one pixel region and the wiring pattern in the vicinity thereof for an EL element of embodiment 2 of this invention. FIG. 9 shows cross-sectional views which explain the layer structure in cross-sections of FIG. 8. FIG. 9A shows the layer structure in a cross-section along the A-A plane, FIG. 9B is a cross-section along B-B, and FIG. 9C is a cross-section along C-C. In these drawings, similarly to embodiment 1, the patterns of the principal semiconductor layer 102, gate metal layer 104, source metal layer 106, and anode layer 110 are shown.

The configuration of the EL element in embodiment 2 is, except for the existence of an affinity-controlling film 113 which forms a step shape, similar to the EL element of embodiment 1. Hence components similar to those of embodiment 1 are assigned the same symbols in the drawings, and explanations are omitted.

Below, features of this embodiment are described.

Affinity-Controlling Layer

As shown in FIG. 9C, the light-emitting portion OLED in embodiment 2 comprises an affinity-controlling layer 113, between the second interlaminar insulating film 107 and the bank layer 108. This affinity-controlling layer 113 need not be formed over the entire pixel region, but when forming a light-emitting portion OLED using a liquid material, should preferably be provided at least near the boundaries of the light-emitting portion. The affinity-controlling layer 113 must have an affinity for the liquid material used in forming the light-emitting portion. In this embodiment, the bank layer 108 forms a wall near the boundary of the light-emitting portion; a material is selected which exhibits no affinity for the liquid material used when forming the light-emitting layer 110, and [the bank layer] is stacked on top of the affinity-controlling layer 113. Consequently the affinity-controlling layer 113 forms a step shape Step on the inside of the light-emitting portion in the wall formed by the bank layer, as shown in FIG. 8 and FIG. 9C.

The material of the affinity-controlling layer 113 is determined according to the kind of properties of the liquid material which is used to fill the light-emitting region by the ink jet method. For example, if the liquid material comprises a liquid such as water which is highly polar, it is desirable that the affinity-controlling layer have polar bases, at least in the portion making contact with the liquid material or on the surface. Conversely, if the liquid material comprises a non-polar liquid, it is desirable that the affinity-controlling layer have nonpolar bases, at least in the portion making contact with the liquid material or on the surface. Also, the extent of the affinity of the affinity-controlling layer is determined by the surface tension of the liquid material which fills the light-emitting region.

For example, even if a material which chemically has a weak affinity for water is used as an affinity-controlling layer, if the liquid material comprises large quantities of a solvent with a surface tension lower than that of water, the surface tension of the liquid material will be lower than that of water,

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and so the affinity-controlling layer will exhibit affinity for the liquid. Hence the type of material to use in the affinity-controlling layer is changed variously according to the liquid material to be used.

It is preferable that the affinity-controlling layer 113 comprise an inorganic compound or organic compound which in turn comprises one among Al, Ta or another metal, silicon oxide, silicon nitride, amorphous silicon, polysilicon, polyimide, an organic compound with fluoride bonds, or a photoresist. If insulating properties are necessary, the affinity-controlling layer comprises a nonmetallic compound. The affinity of these materials is determined by differences in the contact angle with respect to the liquid material. That is, the degree of affinity or absence of affinity is determined in relative and not absolute terms. The degree of affinity can also be adjusted through surface treatment methods.

It is preferable that the bank layer 108 comprise a material with weaker affinity than the affinity-controlling layer 113. This is because, by making the affinity of the bank layer weaker than that of the affinity-controlling layer, the absence of affinity of the bank layer can repel the liquid material to prevent flowing of the liquid material into neighboring pixel regions and avoid short-circuits. Also, the absence of affinity of the bank layer prevents liquid material from being drawn excessively toward the bank layer side so that a concave-shape film is formed.

Thus in this embodiment, an affinity-controlling layer with an affinity for the liquid material is provided near the boundaries of the light-emitting portion, so that a light-emitting layer of uniform film thickness can be formed.

In this way, according to this embodiment, an affinity-controlling layer with affinity for the liquid material is provided near the boundaries of the light-emitting portion, so that the uniformity of the thickness of the hole injection layer, light-emitting layer, and other layers constituting the light-emitting portion is improved.

In this embodiment, the affinity-controlling layer 113 is formed in a step shape; but when the thickness of the layer cross-section can be made sufficiently great, walls without a step shape, that is, a single wall without a step with the bank layer, may be formed.

Other advantageous results of embodiment 2 are similar to those of embodiment 1, and an explanation is omitted.

Embodiment 3

FIG. 10 shows a plane view which explains one pixel region and the peripheral wiring pattern for an EL element in embodiment 3. FIG. 11 shows cross-sectional views explaining the layer structure in cross-sections indicated in FIG. 10. FIG. 11A and FIG. 11B show the layer structures in the cross-sections along A-A and B-B respectively in FIG. 10. In these drawings, similarly to embodiment 1, patterns in the principal semiconductor layer 202, gate metal layer 204, source metal layer 206, and anode layer 210 can be seen.

In the pattern shape of the EL element in embodiment 3, the width of the pixel region 20 is smaller than the width of the pixel region 10 in embodiment 1. However, the circuit configuration is similar to that of embodiment 1 (see FIG. 5), and the materials forming each layer are also similar to embodiment 1, and so components which are the same as in embodiment 1 are assigned the same symbols in the drawings, and explanations are omitted. The glass substrate 100, underlayer protection film 101, semiconductor layer 102, gate insulating film 103, gate metal layer 104, first interlaminar insulating film 105, source metal layer 106, second interlaminar insulating film 107, bank layer 108, cathode layer 109, anode

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layer 110, hole transport layer 111, and light-emitting layer 112 in embodiment 1 correspond, respectively, to the glass substrate 200, underlayer protection film 201, semiconductor layer 202, gate insulating film 203, gate metal layer 204, first interlaminar insulating film 205, source metal layer 206, second interlaminar insulating film 207, bank layer 208, cathode layer 209, anode layer 210, hole transport layer 211, and light-emitting layer 212 in embodiment 3. Also, the transistors T1 to T4 in embodiment 1 correspond respectively to the transistors T11 to T14 in embodiment 3, and the contact holes h1 to h3 in embodiment 1 correspond respectively to the contact holes h11 to h13 in embodiment 3.

Below, features of the wiring pattern in this embodiment are explained.

Holding Capacitor Under the Power Supply Line

In embodiment 1, the holding capacitor C was positioned between the power supply line Vdd and the data line Idata, outside the light-emitting portion (in the upper portion of the light-emitting portion in FIG. 2). However, when the area of the pixel region is comparatively small as in this embodiment, that is, when the pixel density is high, it is not possible to secure sufficient element space for occupation by the holding capacitor.

Hence in this embodiment, the holding capacitor C is formed in the region in which at least one among a first metal layer (for example, the source metal layer 206) or a second layer forms a power supply wiring pattern. Specifically, as shown in FIG. 10, the holding capacitor C is formed by stacking a gate metal layer 204 in parallel below the power supply line Vdd (source metal layer 206) positioned on the side of the light-emitting portion OLED.

The holding capacitor C is formed by causing an overlapping region to occur among the plurality of layers (for example, the source metal layer 206, gate metal layer 204, and semiconductor layer 202) relating to formation of the holding capacitor C, similarly to the holding capacitor explained in embodiment 1; near the overlapping region in which the holding capacitor C is formed, the region occupied by the layer positioned on the lower side among the plurality of layers is formed to be larger than the region occupied by layers positioned on the upper side. Specifically, as shown in FIG. 11B, if the width of the source metal layer 206 is d11, the width of the gate metal layer 204 is d12, and the width of the semiconductor layer 202 is d13, then the relation $d13 > d12 > d11$ obtains. The lower the layer, the larger the pattern shape is made.

The extent to which the size is increased will depend on the precision of the manufacturing processes and the pattern density. As one approach, patterns should be formed for each layer such that, when forming layers positioned on the upper side, even when the maximum possible shift in position occurs, the region in the layer positioned on the upper side will be contained within the region in the layer positioned on the lower side. In this embodiment also, the differences $d13 - d12$ and $d12 - d11$ are designed to be equal to or greater than predicted position shifts in manufacturing processes.

Holding Capacitor Below the Bank Layer

It is preferable that the above-described holding capacitor be formed below the bank layer 208, in order to isolate the above-described neighboring light-emitting portion. That is, because the bank layer is necessary for pixel separation, by superposing the wiring region for the power supply line and the overlapping region for the holding capacitor, the area occupied by the peripheral circuit can be greatly reduced, and a sufficient aperture ratio can be secured.

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Reduction of Peripheral Circuit Space

Similarly to embodiment 1, in embodiment 2 a wiring pattern is fabricated such that at least one active element among a plurality of transistors and other active elements is connected to another active element by the same contact hole. Specifically, as shown in FIG. 10, the transistors T12, T13 and T14 are interconnected by the same contact hole h13. In this way, by designing the circuit such that there are numerous common contact points in the circuit, and arranging elements such that portions which are common contact points are connected by the same connection points, the number of contact holes can be reduced, and the occupied area of the peripheral circuit used for contact holes can be decreased.

Other features, such as for example the planar shape of the light-emitting portion, separation from the electrodes of the gate metal layer, peripheral circuit operation, and improvement of the current maintenance performance of the peripheral circuit, are similar to those of embodiment 1, and an explanation is omitted.

Embodiment 4

FIG. 12 shows a plane view which explains one pixel region and the peripheral wiring pattern for an EL element in embodiment 3 of this invention. FIG. 13 shows cross-sectional views which explain the layer structure at cross-sections indicated in FIG. 12. FIG. 13A and FIG. 13B show the layer structure at cross-sections A-A and B-B respectively in FIG. 12. As in embodiment 3, in these drawings the patterns of the principal semiconductor layer 202, gate metal layer 204, source metal layer 206, and anode layer 210 can be seen.

Except for the existence of an affinity-controlling film 213 forming a step shape, the configuration of the EL element of embodiment 4 is the same as the EL element of embodiment 3. Hence the same symbols in drawings are assigned to components which are the same as in embodiment 3, and an explanation is omitted.

Features of this embodiment are explained below.

Affinity-Controlling Layer

As shown in FIG. 13B, the light-emitting portion OLED in embodiment 4 comprises an affinity-controlling layer 213 between the second interlaminar insulating film 207 and the bank layer 208. This affinity-controlling layer 213 need not be formed over the entire pixel region, but must be provided, at least, near the boundaries of the light-emitting portion. The affinity-controlling layer 213 must have affinity with the liquid material used in forming the light-emitting portion. In this embodiment, the bank layer 208 forms walls near the boundaries of the light-emitting portion; a material which exhibits a lack of affinity with the liquid material used when forming the light-emitting layer 212 or hole injection layer 211 is selected, and is stacked on top of the affinity-controlling layer 213. Consequently the affinity-controlling layer 213 forms a step shape on the inside of the light-emitting portion with respect to the wall formed by the bank layer, as shown in FIG. 12 and FIG. 13B.

The material of the affinity-controlling layer 113 is determined according to the properties of the liquid material with which the light-emitting region is filled using the ink jet method. For example, if the liquid material comprises a liquid such as water which is highly polar, it is desirable that the affinity-controlling layer have polar bases, at least in the portion making contact with the liquid material or on the surface. Conversely, if the liquid material comprises a non-polar liquid, it is desirable that the affinity-controlling layer have nonpolar bases, at least in the portion making contact with the liquid material or on the surface. Also, the extent of

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the affinity of the affinity-controlling layer is determined by the surface tension of the liquid material which fills the light-emitting region.

For example, even if a material which chemically has a weak affinity for water is used as an affinity-controlling layer, if the liquid material comprises large quantities of a solvent with a surface tension lower than that of water, the surface tension of the liquid material will be lower than that of water, and so the affinity-controlling layer will exhibit affinity for the liquid. Hence the type of material to use in the affinity-controlling layer is changed variously according to the liquid material to be used.

It is preferable that the affinity-controlling layer 213 comprise an inorganic compound or organic compound which in turn comprises one among Al, Ta or another metal, silicon oxide, silicon nitride, amorphous silicon, polysilicon, polyimide, an organic compound with fluoride bonds, or a photoresist. If insulating properties are necessary, the affinity-controlling layer comprises a nonmetallic compound. The affinity of these materials is determined by differences in the contact angle with respect to the liquid material. That is, the degree of affinity or absence of affinity is determined in relative and not absolute terms. The degree of affinity can also be adjusted through surface treatment methods.

It is preferable that the bank layer 108 comprise a material with weaker affinity than the affinity-controlling layer 113. This is because, by making the affinity of the bank layer weaker than that of the affinity-controlling layer, the absence of affinity of the bank layer can repel the liquid material to prevent flowing of the liquid material into neighboring pixel regions and avoid short-circuits. Also, the absence of affinity of the bank layer prevents liquid material from being drawn excessively toward the bank layer side so that a concave-shape film is formed.

Thus in this embodiment, an affinity-controlling layer with an affinity for the liquid material is provided near the boundaries of the light-emitting portion, so that the uniformity of the thickness of the hole injection layer, light-emitting layer, and other layers constituting the light-emitting portion can be improved.

According to this embodiment, a bank layer forming a wall near the boundaries of the light-emitting portion exhibits a lack of affinity with the liquid material, so that short-circuits with the neighboring pixel regions can be prevented.

In this embodiment, the affinity-controlling layer 213 is formed in a step shape; but when the thickness of the layer cross-section can be made sufficiently great, walls without a step shape, that is, a single wall without a step with the bank layer, may be formed.

Other advantageous results of embodiment 4 are similar to those of embodiment 1, and an explanation is omitted.

Embodiment 5

This embodiment relates to a display panel which is an electro-optical device having EL elements which are electro-optical elements explained in the above embodiments, and electronic device comprising such a display panel.

FIG. 14 shows a connection diagram for a display panel 1 of this embodiment. As indicated in FIG. 1, in display panel 1, pixel regions are arranged in the display region 11. As pixel regions, the pixel regions 10 of embodiment 1 or embodiment 2, or the pixel regions 20 of embodiments 3 or 4 may be employed. Control signals are supplied to each pixel region from the driver region 14, via the light-emission control lines Vgp and write-control lines Vsel. Data signals and a power

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supply voltage are supplied to each pixel region from the driver region 15, via data lines Idata and power supply lines Vdd.

The display panel 1 of this embodiment can be employed in various electronic device. FIG. 15 shows examples of electronic device which can employ the display panel 1.

FIG. 15A is an example of application to a portable telephone set; the portable telephone 30 comprises an antenna portion 31, voice output portion 32, voice input portion 33, operation portion 34, and a display panel 1 of this invention. Thus a display panel of this invention can be utilized as the display portion.

FIG. 15B is an example of application to a camcorder; the camcorder 40 comprises an imaging portion 41, operation portion 42, audio input portion 43, and a display panel 1 of this invention. Thus a display panel of this invention can be utilized as a viewfinder or display portion.

FIG. 15C is an example of application to a portable personal computer; the computer 50 comprises a camera portion 51, operation portion 52, and a display panel 1 of this invention. Thus a display panel of this invention can be utilized as a display portion.

FIG. 15D is an example of application to a head-mounted display; the head-mounted display 60 comprises a band 61, optical system housing portion 62, and a display panel 1 of this invention. Thus a display panel of this invention can be utilized as an image display source.

FIG. 15E is an example of application to a rear projector; the projector 70 comprises a housing 71, light source 72, synthetic optical system 73, mirror 74, mirror 75, screen 76, and a display panel 1 of this invention. Thus a display panel of this invention can be utilized as an image display source.

FIG. 15F is an example of application to a front projector; the projector 80 comprises a housing 82, optical system 81, and a display panel 1 of this invention, and is capable of displaying images on a screen 83. Thus a display panel of this invention can be utilized as an image display source.

Electro-optical devices of this invention are not limited to the above examples, but extend to all electronic device to which active-matrix type display devices can be applied. For example, in addition to the above, utilization in fax machines with display functions, in the viewfinders of digital cameras, in portable TV sets, in DSP devices, in PDAs, in electronic organizers, in electro-optical bulletin boards, in displays for advertising and announcements, and in other areas is possible.

- FIG. 1
- 13 CATHODE LEAD ELECTRODE
- 12 CATHODE
- 1 DISPLAY PANEL
- 10 PIXEL REGION
- 11 DISPLAY REGION
- 14 DRIVER REGION
- 15 DRIVER REGION
- 16 GLASS SUBSTRATE

- FIG. 2
- SEMICONDUCTOR LAYER
- GATE METAL LAYER
- SOURCE METAL LAYER
- ANODE LAYER

- FIG. 8
- SEMICONDUCTOR LAYER
- GATE METAL LAYER
- SOURCE METAL LAYER
- ANODE LAYER

- FIG. 10
- SEMICONDUCTOR LAYER

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GATE METAL LAYER
SOURCE METAL LAYER
ANODE LAYER

FIG. 12
SEMICONDUCTOR LAYER

GATE METAL LAYER
SOURCE METAL LAYER
ANODE LAYER

What is claimed is:

1. An electro-optical device comprising:

a data line;

a control line; and

a unit circuit arranged corresponding to an intersection of the data line and the control line, the unit circuit including:

a first transistor that includes a first semiconductor film; an electro-optical element electrically connected to one of a source or a drain of the first transistor;

a second transistor that includes a second semiconductor film, the second transistor connected between the one of the source or the drain and a gate of the first transistor;

a holding element that is connected to the gate of the first transistor and holds a gate voltage of the first transistor according to a data signal; and

a wiring connected between the second transistor and the gate of the first transistor,

the first transistor supplying a current based on the gate voltage to the electro-optical element,

the wiring being formed in a layer which is different from a layer in which the first semiconductor film and the second semiconductor film are formed,

the wiring having a portion formed in the layer different from a gate layer in which the gate of the first transistor is formed, the portion crossing the control line.

2. The electro-optical device according to claim 1, wherein the first transistor has a conduction type different from a conduction type the second transistor has.

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3. An electric device comprising an electro-optical device according to claim 2.

4. The electro-optical device according to claim 1, wherein the control line supplies a control signal to a gate of the second transistor.

5. The electro-optical device according to claim 4, wherein the unit circuit further includes a third transistor coupled between the holding element and the data line, and

wherein the second transistor and the third transistor are controlled according to the control signal.

6. An electric device comprising an electro-optical device according to claim 5.

7. An electric device comprising an electro-optical device according to claim 4.

8. An electric device comprising an electro-optical device according to claim 1.

9. The electro-optical device according to claim 1, further comprising a power line, the power line being formed in a layer in which the data line and the wiring are formed.

10. The electro-optical device according to claim 9, wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

11. The electro-optical device according to claim 9, wherein the first transistor has a first terminal, a second terminal, and a channel region disposed between the first terminal and the second terminal, the first terminal being disposed between the power line and the second terminal, and

the first transistor controlling an electrical connection between the first terminal and the second terminal.

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