Liquid Crystal Displays

ADDRESSING SCHEMES AND ELECTRO-OPTICAL EFFECTS

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Element Exhibit 2011 / Page 1 of 10

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Foreword

Preface

About the Auth

1 Introduct

2 Liquid Cr
2.1 Proper
2.1.1
2.1.2
2.2 The O
2.2.1
2.2.2

3 Electro-o
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3.2.1
3.2.2
3.2.3
3.2.4
3.2.5
3.2.6
3.2.7
3.2.8

Addressing Schemes for Liquid Crystal Displays

The addressing circuit has the task of imposing a given grey shade at a prescribed time onto an individual pixel without causing discernible crosstalk to other pixels. The addressing of the LCDs may be performed electronically, optically or by plasma columns, where each physical effect realizes a switch allowing it to feed in the grey shade information (Kaneko, 1987; Lueder, 1998a, Scheffer and Nehring, 1998; Luo, 1990; Kaneko, 1998).

The grey shades are defined by the linear portion of the curve in Figure 2.13 representing the transmitted luminance versus the voltage V_{LC} across the LC cell. Assuming that the linear portion in Figure 2.13 belongs to a swing of 2 V, then 256 grey shades translate into a change of 7.8 mV per grey shade. This demonstrates how accurately the voltage across the LC cell has to be maintained in order to display an unadulterated picture. The range below the reduced threshold voltage V_{th}/V_0 in Figure 2.13 is required to keep parasitic crosstalk voltages from changing the luminance, and hence the grey shades. As a consequence, the chosen addressing schemes have to limit the sum of all crosstalk voltages to values below V_{th}.

The electronic addressing is subdivided into three sub-groups. The direct addressing in Figure 10.1 connects each portion of the display called a segment, which is supposed to exhibit various grey shades, to an external electrode carrying the voltage applied with respect to the ground electrode common for the entire display area. To avoid an unrealizably large number of connecting links, however, this approach, is limited to a small number of fixed segments, such as the seven segments of a digit in Figure 10.1.

A more versatile addressing is matrix addressing, which uses only the external contact pads in Figure 2.9 at the ends of rows and columns to reach the individual pixels. The Passive Matrix addressed LCD (PMLCD) in Figure 10.2 uses the row address voltages V_r at the row electrodes and the column address voltages V_c at the individual column electrodes which carry the video information to determine the individual grey shade of each pixel.

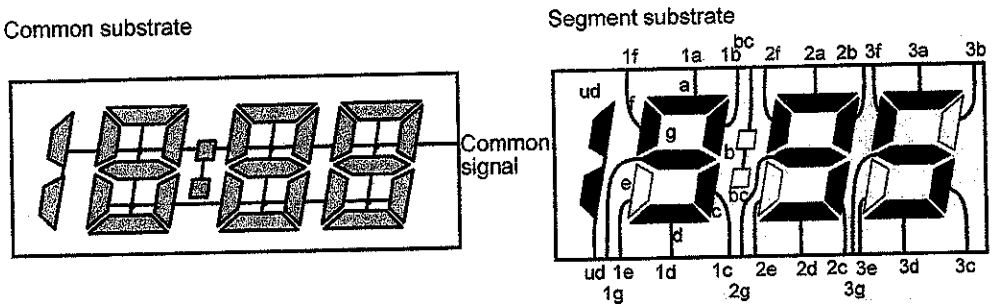

Figure 10.1 The direct addressing of the seven segments of a digit

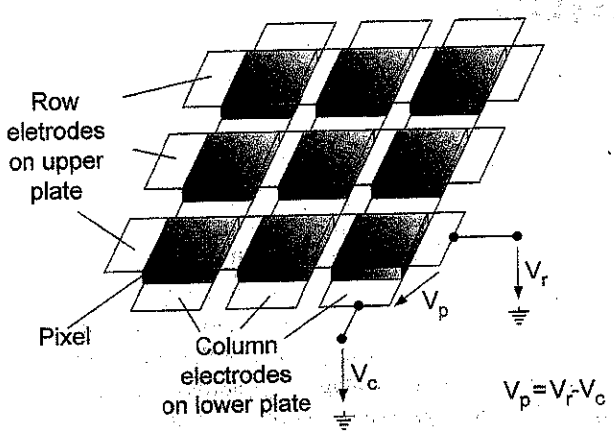

Figure 10.2 The Passive Matrix LCD (PMLCD) with row and column electrodes

As we shall see, an even more powerful control of the grey shades is realized by Active Matrix addressed LCDs (AMLCDs) in Figure 10.3, where each pixel possesses an electronic switch allowing the video information to reach the pixel.

Optical addressing involves the transfer of optical image information of a camera or on a display screen directly into an LCD. As this LCD is not pixellized at all, a high resolution picture may be obtained.

The Plasma Addressed LC (PALC) display uses an ignited and a turned-off plasma column as a switch for the addressing of large area LCDs with a diagonal, at present, up to 42".

There is a variety of electronic switches. Most important are Thin Film Transistors (TFTs) with a-Si, poly-Si or CdSe as the semiconductor. TFTs are Field-Effect-Transistors (FETs). Their manufacture and application for LCDs is well established, especially for a-Si-TFTs. TFTs with CdSe as the semiconductor now play a minor role (Brody *et al.*, 1973; Lee *et al.*, 1991; Lueder, 1994b).

Somewhat more frequent is the use of Metal-Insulator-Metal (MIM) devices as a switch. Semiconductor diodes as switches were investigated for a long time, but have now virtually disappeared in the display field. Nonlinear voltage dependent resistors, called *varistors*,

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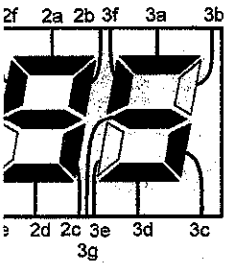
IPR2023-00605
Element Exhibit 2011 / Page 4 of 10



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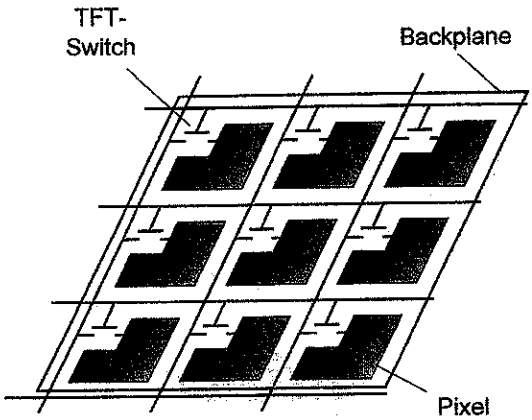

Figure 10.3 The Active Matrix addressed LCD (AMLCD) with a TFT as pixel switch

could not withstand the onslaught of the economically fabricated a-Si-TFTs, and are hence not discussed here.

Waveforms and addressing circuitry are very similar for all nematic LCDs, the PDLCDs and the guest-host displays, whereas for bistable devices such as ferroelectric LCDs and chiral nematic LDCs, different waveforms and addressing circuits are mandatory. As bistable displays do not require a control of continuous grey shades, the expensive AM addressing is not needed. Therefore, the addressing of bistable displays is done with PM schemes.

14.7 Layouts of Pixels with TFT Switches

The performance of a display depends strongly upon the layout of the pixels. Key features are a large enough aperture ratio A, defined in percent for a transmissive display as

$$A = \frac{\text{transmissive area of a pixel}}{\text{total area of a pixel}} 100\%, \tag{14.86}$$

which produces high brightness and a large enough storage capacitor C_s for holding the information during the frame time, for reducing the effect of parasitic capacitive coupling in Equation (14.18) to the pixel voltage, and for shielding the pixel against detrimental couplings from pulses travelling on the columns and rows. For a reflective display, the word 'transmissive' in Equation (14.85) should be replaced by 'reflective'. The increased C_s and the shielding, as a rule, diminish the aperture ratio, as the materials used are not transparent. It is up to the designer to find an ingenious solution benefiting all criteria.

The basic pixel layout in Figure 14.22(a) (Lueder, 1998a) possesses a column made of Al or Cr-Al-Cr, which is insulated from the rows made of Cr or Mo-Ta. The rows are widened in the region of the storage capacitor C_s, which has a dielectric of SiO_2 or Si_3N_4 and an upper electrode of Al or ITO. This placement of C_s leaves more space for the ITO electrode, thus enhancing the aperture ratio to, as a rule, 65 percent. The a-Si TFT requires only about

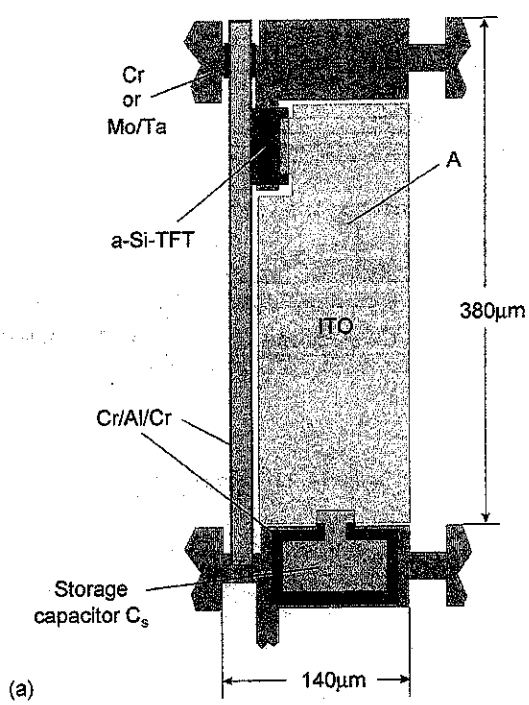

Figure 14.22 (a) Basic pixel layout of an AMLCD; (b) pixel layout with storage capacitor along the edges of the ITO-electrode; (c) cross-section along the line A–A′ in Figure 14.22(b)

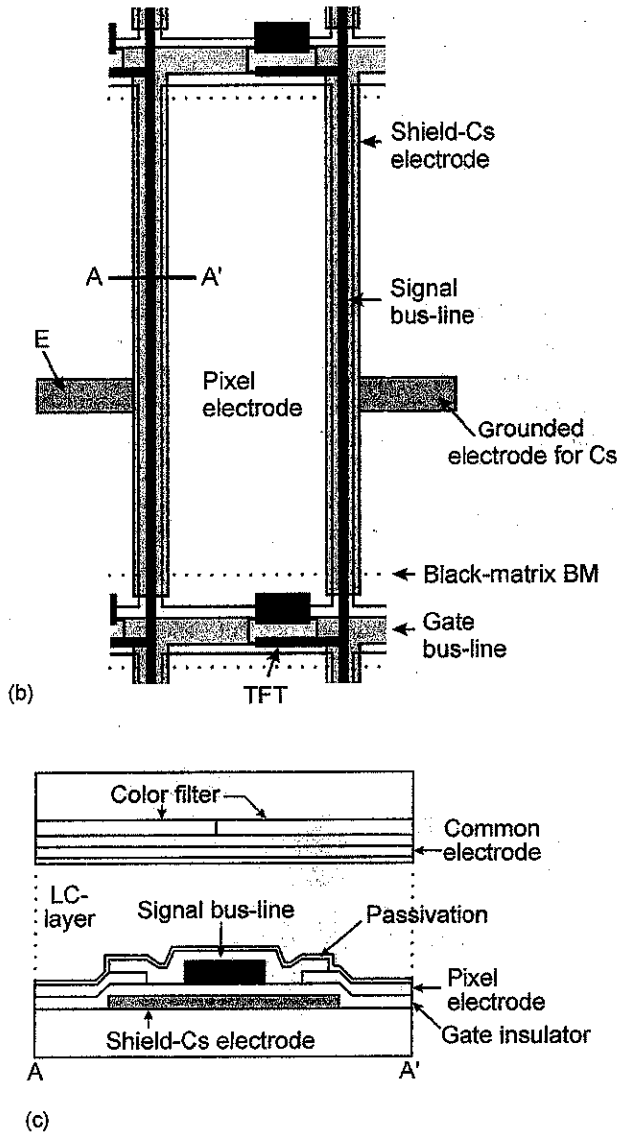

Figure 14.22 (continued)

2 percent of the area. As a rule, the black matrix is deposited on the opposite glass plate together with the colour filter.

The layout in Figure 14.22(b) with the cross-section in Figure 14.22(c) (Kitazawa *et al.*, 1994; Suzuki, 1994; Kim, 1996) places the capacitor C_s along the edges of the ITO electrode. Most importantly, it is shielded against crosstalk by a shield electrode. This electrode in Figure 14.22(c), from Mo-Ta, also serves as an additional black matrix layer. Furthermore, C_s is no longer connected to the gate-line, but has its own transparent ITO electrode E in Figure 14.22(b), not shown in the cut $A-A'$ in Figure 14.22(c). Hence C_s and,

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as a consequence, V_{LC} is no longer affected by the pulses on the former bottom electrode of C_s. There is, however, still the downward shift of V_{LC} stemming from the gate pulse coupled in through the gate-source capacitance C_{GS}. The black matrix BM on the active matrix plate has the beneficial effect of blocking the oblique light beam O from the backlight, shown in the cross-section of the pixel depicted in Figure 14.23. Without the BM on the active matrix plate, backlight would be transmitted in the direction shown by the dashed arrow. Further advantages of the additional BM are the shielding of the imperfectly controlled LC stripe along the edge of the ITO electrode, and the introduction of the overlap of the two BMs in the range w, allowing for small misalignments of the two glass plates (Kim, 1996).

Figure 14.24 shows schematically some layers of a pixel in which the storage capacitor C_s is completely placed underneath the ITO pixel electrode (Maier, 1997). For a transmissive pixel, all layers have to be transparent, which is satisfied by the ITO bottom and pixel electrodes and the Si_3N_4 dielectric, which is also used as gate dielectric. The electric field from the neighbouring column ends mostly on the extended bottom electrode, resulting in a shielding of the capacitor C_s. The completed pixel layout with the light shield omitted is shown in Figure 14.25. C_s possesses the large value of 200 fF on an area of 1300 μm^2, with a thickness of 400 nm, which helps to diminish all effects of the parasitic couplings.

The pixel layout for a reflective cell drawn in Figure 14.26(a) (Egelhaaf *et al.*, 2000) shows that the entire pixel apart from the interpixel gap is covered by an Al mirror, yielding

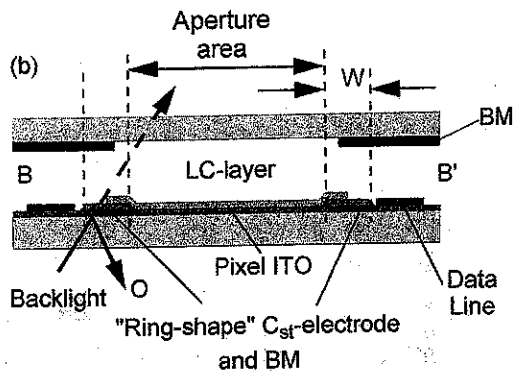

Figure 14.23 Cross-section of a pixel with an additional black matrix on the active matrix plate

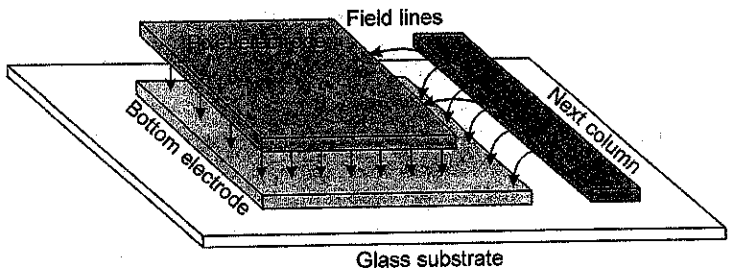

Figure 14.24 Pixel with the storage capacitor underneath the pixel electrode

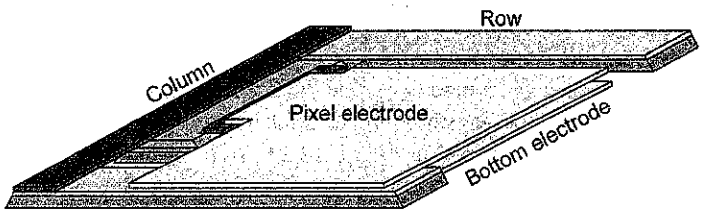

Figure 14.25 A pixel with C_s underneath the ITO electrode

a 92.6 percent aperture ratio. The TFT, the storage capacitor, the rows and columns are all underneath the mirror, as depicted in the cross-section in Figure 14.26(b). The column is shielded by a grounded electrode, preventing capacitive coupling of the video pulses onto the pixel voltage.

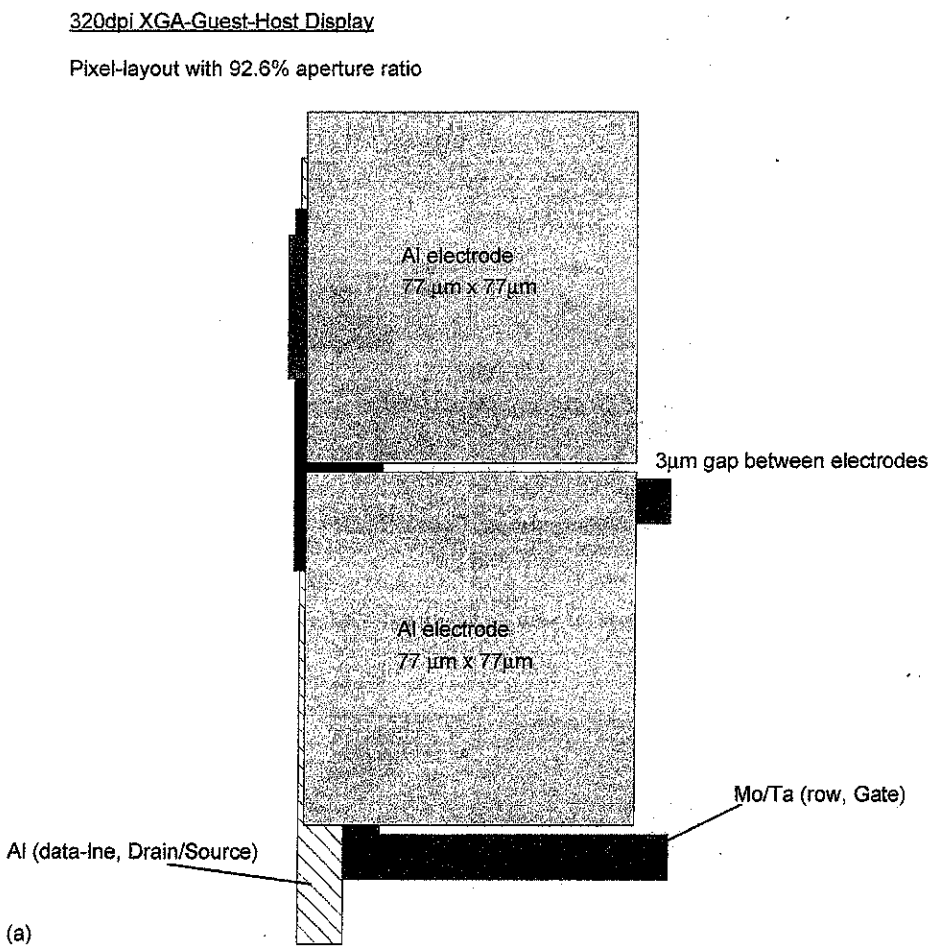

Figure 14.26 (a) The top view of a pixel in a reflective display with a mirror, which also covers the rows and columns; (b) cross-section of the pixel in Figure 14.26(a)

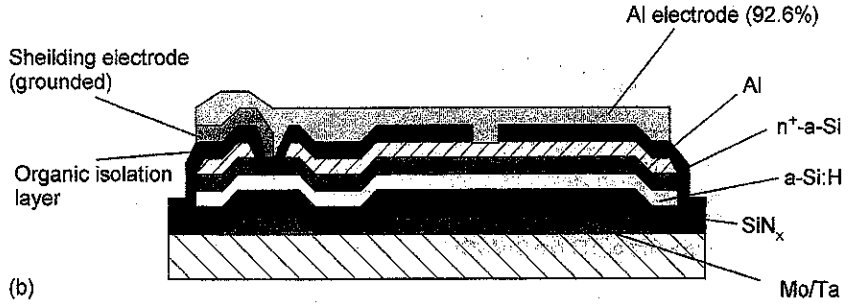

Figure 14.26 (continued)

14.8 Fabrication Processes of a-Si TFTs

A criterion for the usefulness of a TFT fabrication process is a low mask count, presently in the range of 4 to 6. The rationale behind this is that a small number of mask alignments and a small number of processing steps associated with a small mask count is synonymous with an economic process. This is, however, only true if the low mask count does not narrow the process window, and still allows for a high fabrication yield. Furthermore, a small number of masks is only acceptable if it does not degrade the performance of the display.

Figure 14.27 depicts the sequence of fabrication steps involved in a four mask fabrication of bottom gate a-Si TFTs (Glueck *et al.*, 1994; Lueder, 1994c). After a glass substrate (e.g. 0.7 mm thick) has been chemically cleaned in an ultrasonic bath, a 200 nm Cr- or Mo/Ta layer is sputtered and chemically wet etched to form the rows, the gate electrodes and the bottom electrode of the storage capacitor. The patterning shown in Figure 14.27(a) requires the first mask. The next three layers in Figure 14.27a are deposited by [Plasma Enhanced Chemical Vapour Deposition (PECVD)]. They are Si_3N_4 as gate dielectric and as the dielectric for C_s, intrinsic a-Si : H (i-a-Si : H) as semiconductor and n^+-a-Si as a layer providing an ohmic contact for drain and source. In the semiconductor, dangling bonds are neutralized by H, which enhances the electron mobility to values from 0.5 cm^2/Vs to 1 cm^2/Vs. This mobility of the amorphous Si layer is still far below the mobility of monocrystalline Si-FETs reaching more than 500 cm^2/Vs. Finally, a Cr/Al/Cr- or Mo/Ta layer is sputtered and chemically wet etched in Figure 14.27(b) to form the pattern for the drain and source electrode and the top electrode of C_s. For this, the second mask is required. The pattern of the Cr/Al/Cr serves as a mask for plasma etching of n^+-a-Si in Figure 14.27(b). As plasma etching also attacks a-Si, an end point control is required by watching the edging time or by monitoring the plasma emission at 204.4 nm stemming from CF and SiF radicals. This back channel etch is the most subtle step, as it has to remove all n^+-a-Si residues while leaving an a-Si-layer with a homogeneous thickness of around only 50 nm. This small thickness off current below 1 pA. A second plasma etch is required to reduce the using a third mask in Figure 14.27(c) removes i-a-Si : H, forming the i-a-Si islands for the TFTs. The sputtering and patterning of the ITO pixel electrode by a lift-off process, or preferably by plasma etching in Figure 14.27(d), requires the fourth mask. Finally, a PECVD passivation layer of SiN_x requires a fifth mask for opening the bond pads, whereas the deposition of a metallic light shield on top of the array uses a sixth mask. The two last masks do not have to be aligned as precisely as the others, and as a rule are not counted as yield-determining masks.

IPR2023-00605
Element Exhibit 2011 / Page 10 of 10