Introduction to Flat Panel Displays

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About the author

Preface

Acknowledgemen

1 Introduction
1.1 Flat panel
1.2 Emissive a
1.3 Display sp
1.3.1 Phys
1.3.2 Brig
1.3.3 Com
1.3.4 Spat
1.3.5 Effic
1.3.6 Flex
1.4 Applicatio
1.4.1 Liqu
1.4.2 Ligh
1.4.3 Plas
1.4.4 Orga
1.4.5 Fiel
References

2 Color science
2.1 Introductio
2.2 The eye
2.3 Colorimetr
2.3.1 Trich
2.3.2 CIE
2.3.3 CIE
2.3.4 Colo
2.3.5 Ligh

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Field emission displays

8.1 Introduction

A field emission display (FED) has a simple structure and a high luminance efficiency. This type of display does not need a backlight, color filter, polarizer or the other optical films that are required in a liquid crystal display (LCD). Therefore, the structure of a FED is simpler than that of a LCD. Additionally, FEDs have a shorter response time, a wider viewing angle and a larger temperature range than LCDs.[1] They can display static pictures and motion pictures, in cold ambient and hot ambient, for personal use and public use.[2] The structure of a FED is similar to that of a cathode ray tube (CRT). Both FEDs and CRTs use phosphors to produce brightness and depend on a vacuum to maintain the lifetime of electron emission. The operating mechanism of FEDs involves field emission electrons to excite a phosphor and generate luminance. Field emission uses a high electric field rather than a thermionic approach to extract electrons in a vacuum.[3]

8.2 Physics of field emission

Electrons may be emitted from a solid surface into a vacuum by many mechanisms, including thermionic emission, photoemission and field emission.[4,5] Thermionically emitted electrons are thermally excited over the potential energy barrier while photoemitted electrons are excited over the potential energy barrier by incoming photons. In field emission, electrons tunnel though the surface potential energy barrier, which has been thinned and shaped by a strong electric field. A sharp emitter structure usually offers a strong electric field even when the applied voltage is low. Since the ions generated by the residual gas can damage the emitter, less residual gas and a lower operating voltage are needed. To achieve a low operating voltage, an emitter material with a low work function and a sharp structure is required. A vacuum is also required to eliminate residual gas and thus reduce emitter damage which, in turn, increases emitter lifetime.

8.2.1 Work function and field enhancement

For a metal surface without an applied electric field, the surface potential energy E for a typical Fermi level E_F and work function Ψ is as presented in Figure 8.1,[6] where Z is the distance from the metal surface and the surface barrier is the sum of E_F and Ψ. This diagram is for electrons at a metal surface in the absence of an electric field.

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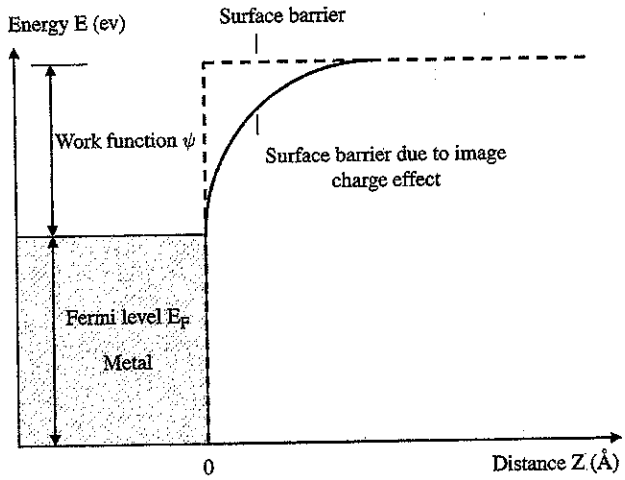

Figure 8.1 Surface potential energy diagram in the absence of applied electric field.

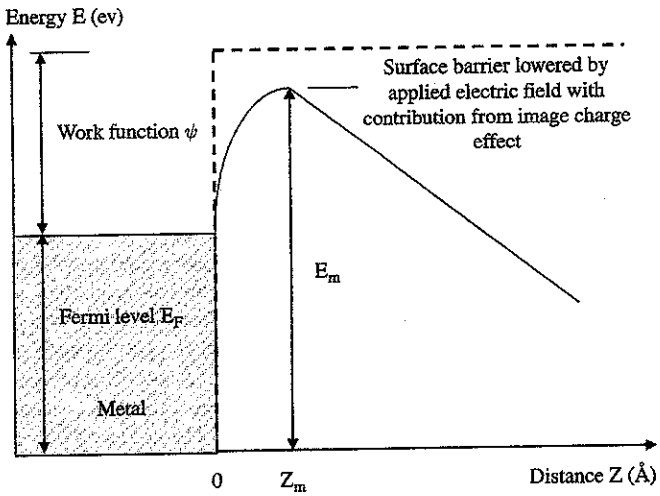

Figure 8.2 Surface potential energy diagram with applied electric field.

The straight line of the surface barrier is smoothed by the image charge effect. However, the maximum height of the barrier is as high as the sum of the Fermi level E_F and the work function Ψ. An applied electric field bends the surface barrier line, as shown in Figure 8.2, where E_m is the maximum surface barrier.

Z_m is the distance from the metal surface to the position the maximum of the surface barrier. This shaping of the potential energy is the result of the image potential energy and a strong electric field. As the applied electric field increases, the surface barrier is bent more and becomes thinner. When the applied electric field is as high as 10^7 V cm^{-1}, the surface barrier is sufficiently thin to enable electrons to tunnel through the barrier.

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Since the image potential energy E_i is equal to $-e^2/4\pi\varepsilon 4Z$, where ε is the permittivity in a vacuum, the surface potential energy $E(z)$ that is seen by an electron on the vacuum side of the metal–vacuum interface is asymptotically given by

$$E(z) = E_F + \Psi - \frac{e^2}{4\pi\varepsilon 4Z}, \tag{8.1}$$

where $E(z)$, E_F and Ψ are in eV. When an electric field F is applied to the surface, the surface potential energy that is seen by an electron becomes

$$E(z) = E_F + \Psi - \frac{e^2}{4\pi\varepsilon 4Z} - eFz \tag{8.2}$$

and the maximum surface barrier E_m is given by

$$E_m = E_F + \Psi - \sqrt{\frac{e^3 F}{4\pi\varepsilon}} \tag{8.3}$$

or

$$E_m = E_F + \Psi - 3.79 \times 10^{-5}\sqrt{F}\ \text{eV}, \tag{8.4}$$

where F is in V m^{-1}. The surface barrier is maximum at Z_m where

$$Z_m = \sqrt{\frac{e}{4\pi\varepsilon 4F}} \tag{8.5}$$

or

$$Z_m = 1.9 \times 10^{-5}\sqrt{F}\,\text{m}. \tag{8.6}$$

Several equations have been used to describe field emission. One equation, derived by Fowler and Nordheim in 1928,[7] ignores the lowering of the barrier by the image effect.[8,9] This form of the Fowler–Nordheim equation is

$$J(F) = \frac{6.2 \times 10^{-6}\sqrt{E_F}}{(\Psi + E_F)\sqrt{\Psi}} F^2 \exp\left(\frac{-6.8 \times 10^7 \sqrt{\Psi^3}}{F}\right). \tag{8.7}$$

where current density J is in A cm^{-2}, electric field F is in V cm^{-1} and Fermi level E_F and work function Ψ are in eV. Another equation considers the lowering of the barrier by the image effect.[10,11] This modified Fowler–Nordheim equation is typically presented in the form

$$J(F) = \frac{1.54 \times 10^{-6}}{\Psi t^2(y)} F^2 \exp\left(\frac{-6.8 \times 10^7 \sqrt{\Psi^3}\, v(y)}{F}\right). \tag{8.8}$$

where emission current density J is in A cm^{-2}, electric field F is in V cm^{-1}, work function Ψ is in eV and the Schottky lowering of the work function barrier is given by

$$y = 3.79 \times 10^{-4}\sqrt{F}/\Psi. \tag{8.9}$$

The functions $v(y)$ and $t(y)$ have been computed, and are presented in Figure 8.3.[12] The approximation $t^2(y) = 1.1$ and $v(y) = 0.95 - y^2$ can be applied to Equation (8.8).

Equations (8.7) and (8.8) clearly reveal that the electric field dominates the current density. Restated, a strong electric field is required to yield a high current density.

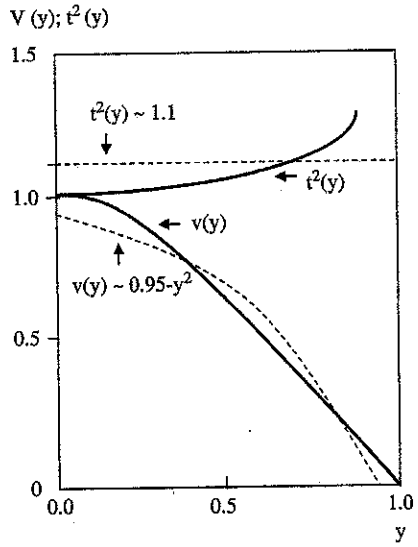

Figure 8.3 Comparison of approximate forms with exact solutions of the Fowler–Nordheim field emission functions $v(y)$ and $t^2(y)$.

In addition to field emission, thermionic emission can become important as the temperature rises. In thermionic emission, the metal is heated to excite electrons and to move them over a potential energy barrier. The equation of thermionic emission is

$$J = 120T^2 e^{-\Psi/kT}, \tag{8.10}$$

where emission density J is in A cm^{-2}, absolute temperature T is in K, work function Ψ is in eV and the Boltzmann constant k is 8.625×10^{-5} eV K^{-1}.[13] For thermionic emission, temperature dominates the current density; in field emission, the electric field dominates the current density. Figure 8.4 shows the range of thermionic current emission and field emission for an emitter with a work function of 4.5 eV,[14, 15] indicating that, in a strong enough field, most of the emission is field emission. However, at sufficiently high temperature and low electric field, the emission is mainly thermionic emission.

8.2.2 Vacuum mechanism

A vacuum is required to reduce the amount of residual gas. Meanwhile, the probability of undesired ionization is reduced as the distance from the cathode to the anode decreases to less than the electron mean free path (λ_c). The equation for the electron mean free path is

$$\lambda_c = \frac{T}{273pP_c(v)}\text{cm}, \tag{8.11}$$

where $P_c(v)$ is the average number of collisions made by an electron as it travels through 1 cm in a gas at a pressure of 1 torr at 0 °C, v is the potential applied to generate the electron velocity, T is the absolute temperature in kelvin and p is the pressure in torr.[16] Since $P_c(v)$ is typically about 70, p must be less than 3.14 torr for $T = 300$°K and $d = 50$ μm. However, the lifetime of the device increases with

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8.3 FED structure

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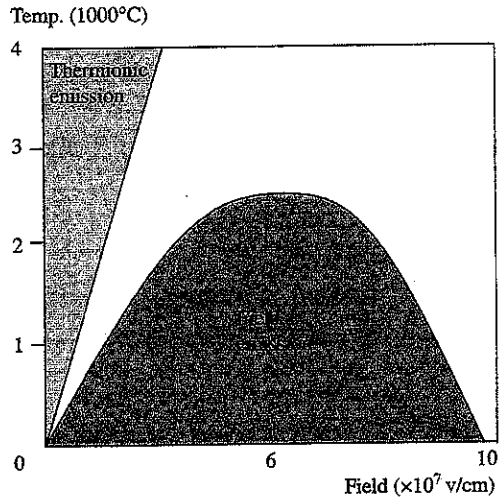

Figure 8.4 Ranges of thermionic emission and field emission for an emitter with a work function of 4.5 eV.

a higher vacuum since ion bombardment decreases. The typical vacuum in a field emission device is in the region of 10^{-7} torr.

8.3 FED structure and display mechanism

A FED panel comprises a field emission array (FEA) plate and a phosphor plate. The FEA plate is a structure that generates field emission.[17] Additionally, gated field emission is typically required to modulate the emission of electrons.[18] Adding a third electrode (gate) between the anode and the cathode causes gated field emission. The emitter is on top of the cathode. The gate is typically much closer to the emitter than to the anode to control (or modulate) the electron emission. This emission current is extracted from the emitter and is a function of the voltage between the gate and the cathode. The voltage between the anode and the gate governs the magnitude of the emission current flowing to the anode and to the gate. A structure in which the gate is placed above the cathode is called a vertical structure. Figure 8.5 shows the vertical structure of a gated conic emitter in a FED.[19] In this figure, r is the radius of the emitter, which is typically hundreds of angstroms; d is the diameter of the gate opening, which is typically a few or a few tens of micrometers; h is the height of the emitter, which is typically a few or a few tens of micrometers; x is the tip elevation above the top edge of the gate, which is typically less than 1 μm; S_{ag} is the distance between the anode and the gate, which is typically from a few tens of micrometers to a few millimeters; V_{ge} is the voltage between the gate and the emitter; and V_{ag} is the voltage between the anode and the gate. Notably, the electric field $F = f(r, d, h, s, V_{ge})$ and the emission current density is $J = f(F)$.

In Figure 8.5, electrons are emitted from the emitter and vertically excite RGB phosphors. The phosphors used in the field emission device are of the electron-excited type. However, the gate and the cathode can also be arranged in a horizontal configuration, as presented in Figure 8.6. The gate is placed at the same elevation as the cathode. Since the emitted electron must fly over the gate to reach the anode, the gate receives more current than the anode. Modeling experiments show that the anode of the vertical structure collects more current than the anode of the horizontal structure under the same operating conditions. This is a shortcoming for a horizontal gated emitter, although this type of gated emitter has a simple structure and process steps.

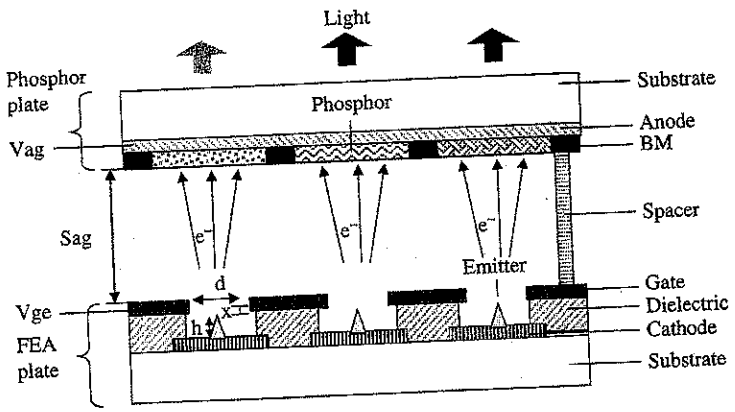

Figure 8.5 Vertical structure of gated conic emitter in a FED.

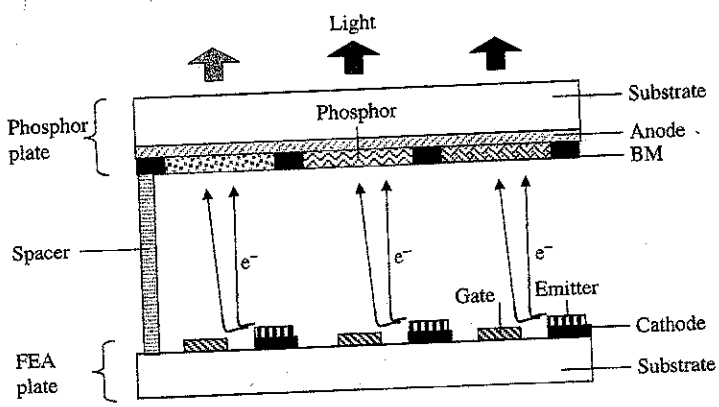

Figure 8.6 Horizontal gated emitter in a FED.

8.4 Emitter

The emitter has an important role in FEDs. Field emitter structures can be conic, wedge-shaped or tubular.[20] The emitting region of a conic emitter is its tip, while those of the other structures are edges. The many emitters include the Spindt emitter, the carbon nanotube (CNT) emitter and the surface conduction emitter (SCE).[21] The Spindt emitter is a sharp cone while the CNT emitter has nanometric diameter carbon tubes. The SCE uses a material called PdO with a nanometric gap structure to generate surface electrons. Table 8.1 compares these emitters. These forms of field emission need a high vacuum of

Table 8.1 Comparison of Spindt emitter, CNT emitter and SCE.

Item	Spindt	CNT	SCE
Feature	Sharp conic structure	Nano-diameter of carbon tube	Nano-gap of slit
Operating voltage (V)	Few tens	Few tens to hundreds	Few tens
Major process	Conic emitter formation	CNT formation	Nano-gap formation
Key issue	Large area of evaporation	CNT activation or CNT growth rate	High gate drawn current

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Work function (e
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typically 10^{-7} torr. The operating voltages are typically from a few tens to a few hundreds of volts. Since a higher operating voltage of driver integrated circuits (ICs) is more expensive, higher operating voltage indicates higher driver costs. Therefore, the driver costs for Spindt emitters and SCEs are low due to their relatively low operating voltages. The major processes of formation of the Spindt emitter, the CNT emitter and the SCE are conic formation, CNT formation and nano-gap formation, respectively. The key difficulties in the formation of the Spindt emitter, the CNT emitter and the SCE are the large area of evaporation, the challenge of CNT activation and the high gate drawn current, respectively. The high gate drawn current of the SCE is due to its horizontal gated structure. This horizontal gated structure is helpful to make a nano-gap slit between the cathode and the gate. In spite of the convenience to make a nano-gap slit for the horizontal gated structure, the emitted electron of SCE for this structure must fly over the gate and results in high gate drawn current. The effective current applied to the anode is therefore reduced and results in lower current efficiency of the SCE. Compared with the SCE, the Spindt and CNT emitters using vertical gated structures have lower gate drawn currents and higher anode current. In other words, Spindt and CNT emitters have lower power consumption for the same operating voltage. Moreover, the emitter elevation also affects the gate drawn current for the vertical gated structure. When the emitter elevation is low, the gate drawn current will be high. For the Spindt emitter, one can control the emitter elevation and the gate drawn current effectively. However, the Spindt emitter suffers from the uniformity difficulty for large-area evaporation. As regards the CNT emitter, the control of emitter elevation is a challenge and the emitter elevation is typically low. Therefore, the CNT emitter usually has higher gate drawn current than the Spindt emitter. In addition, the CNT emitter also suffers from the effective activation difficulty or the low growth rate of the tube.

Notably, a smaller value of r of an emitter corresponds to not only a higher emission current density J, but also a smaller emitting area. If the emitter is too sharp, then the emission current I may be decreased because the product of J and A is smaller. The emission currents vary from different tips.[22] Restated, one emitter may require a lower emitting voltage while another emitter may require a higher emitting voltage. The variation of the emitting voltage among the emitters results in the problem of uniformity and raises the challenge of modulating the gray levels of the display.

8.4.1 Spindt emitter

Many materials, including semiconductors, can be used in Spindt field emitters.[23,24] Ideally, the field emitter should be a material with a high melting point to withstand a large current, a low work function to provide large emission and low vapor pressure to maintain the necessary vacuum in a sealed device.[25] An emitter should also be sharp to generate a sufficiently strong electric field for electron emission at low voltage.[26–28] Low-voltage operation reduces the probability of dielectric breakdown. Table 8.2 presents the common emitters silicon,[28–33] tungsten,[34,35] molybdenum,[36–38] LaB_6[39,40] and tantalum[41,42] used in field emission devices, along with some of their properties.

Among these emitters, tungsten has the highest melting point and the lowest vapor pressure while silicon has the lowest emitter radius. Since silicon can be formed using standard semiconductor fabrication

Table 8.2 Most common Spindt field emitters.

Item	Si	W	Mo	LaB_6	Ta
Melting point (°C)	1410	3410	2617	>1500	2996
Work function (eV)	4.50	4.50	4.50	2.66	4.25
Vapor pressure (torr)	10^{-6} at 1200 °C	10^{-11} at 1800 °C	7×10^{-7} at 1800 °C	—	5×10^{-10} at 1800 °C
Reported emitter radius (Å)	<10	<200	400	—	<200

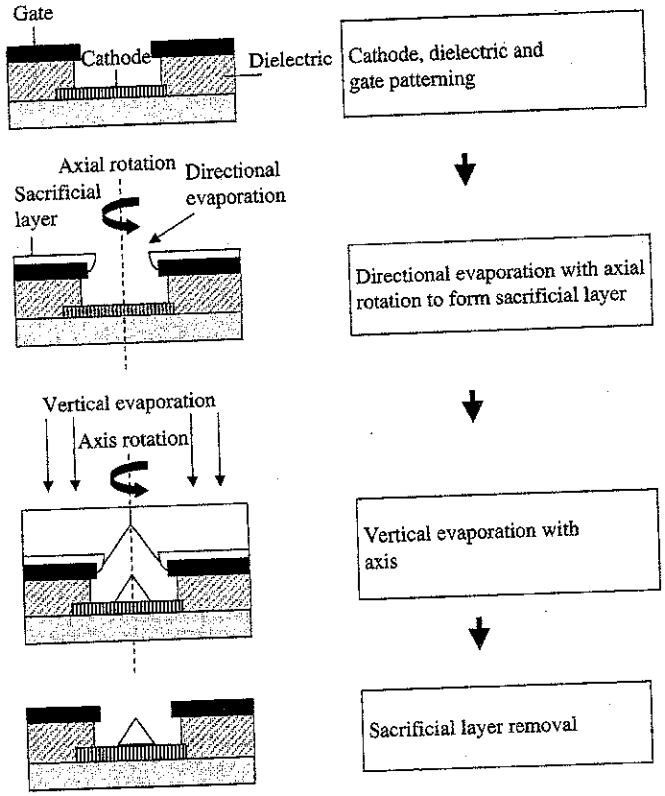

Figure 8.7 Typical process flow for a conic emitter.

technologies into sharp tips, it has been studied and used widely as a field emitter despite its lower melting point and higher vapor pressure than other materials such as tungsten, molybdenum and tantalum.[43]

Field emitters must be sharp since the electric field varies with sharpness and electron emission depends strongly on the electric field.[44] Sharp emitters also enable electron emission devices to operate at low voltage.[45] Figure 8.7 shows a typical process flow to form a conic emitter.[46] At the beginning of the process, the cathode, the dielectric and the gate are patterned. Then, directional evaporation with axial rotation is performed to form a sacrificial layer. After the sacrificial layer is formed, vertical evaporation with axial rotation is performed to form a conic emitter. The final step in this process is to remove the sacrificial layer to form a gated field emitter.

8.4.2 *CNT emitter*

Spindt-type (sharp-cone-type) emitters have been widely studied in the last few decades. However, the evaporation used in the Spindt emitter process for forming displays with large areas is difficult. Restated, this is the main difficulty that maintains the uniformity of the sharp-conic emitter when a larger display is desired. Accordingly, the use of a CNT as an emitter is an alternative approach of forming FEDs.[47–49] CNT is a carbon material with a nanosized structure. Since it is tubular with a diameter of a few tens or hundreds of nanometers, it is naturally sharp and can act as a field emitter.

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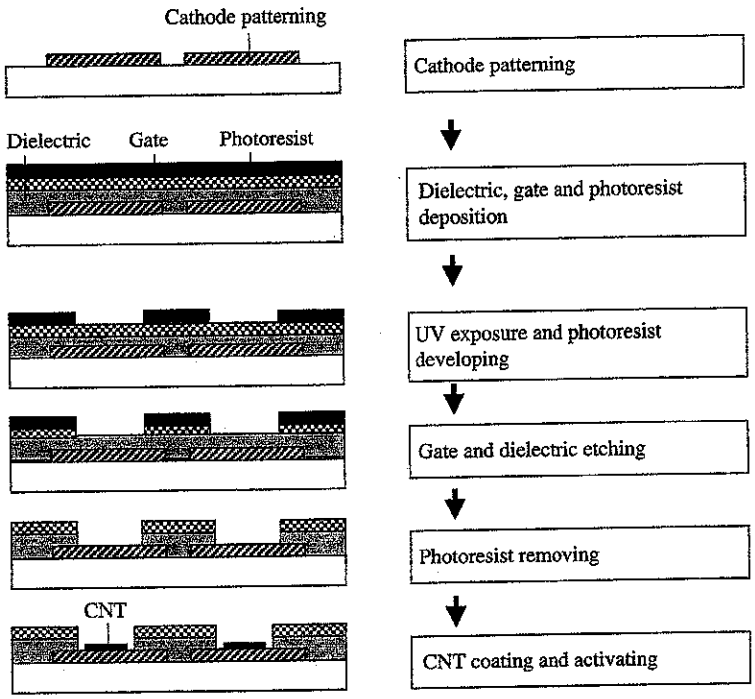

Figure 8.8 Typical indirect approach for forming CNT emitters.

Indirect and direct approaches can be adopted to form CNT emitters. In an indirect approach, the CNT is grown by arcing and then broken up into a powder. A solvent is added to this powder of CNT to form a paste.[50] A CNT emitter is then formed by screen printing the CNT paste onto a substrate and then activating it.[51] Figure 8.8 shows the typical process, in which the maximum process temperature is close to about 450 °C.[52] At the beginning of this process, the cathode, the dielectric and the gate are patterned. The following process is to coat the CNT paste onto the substrate and then activate the CNT, while the CNT paste is prepared in a separated process.

Since the CNT is formed by high-temperature arcing, it has high purity. However, the uniformity of the CNT emitter cannot be effectively controlled since pulverizing and screen printing randomly redistribute the CNT.[53] Accordingly, the direct approach to the formation of a CNT emitter is adopted to solve the uniformity problem. Two methods, chemical vapor deposition (CVD) and electrophoretic deposition (EPD), are used to form the CNT emitter.[54–56] Figure 8.9 shows the typical process of CVD for forming CNT emitters.

The cathode, dielectric and gate are patterned at the beginning of this process. The following process is the deposition of a catalyst. A typical catalyst is Fe/Ni/Co and the process temperature is about 600 °C. The process temperature can be reduced by using the plasma CVD process. The reaction for forming the CNT is

$$C_2H_2 \rightarrow 2C + H_2. \tag{8.12}$$

Although the CVD process yields a more uniform CNT, the growth rate is a little slow. Accordingly, EPD can be adopted as an alternative approach for growing CNT. Figure 8.10 shows a deposition mechanism

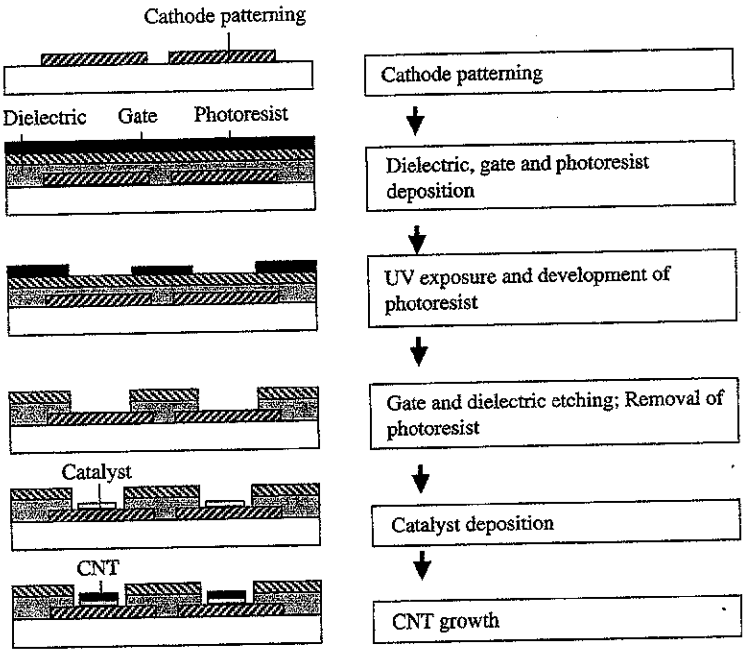

Figure 8.9 Typical CVD process for forming CNT emitters.

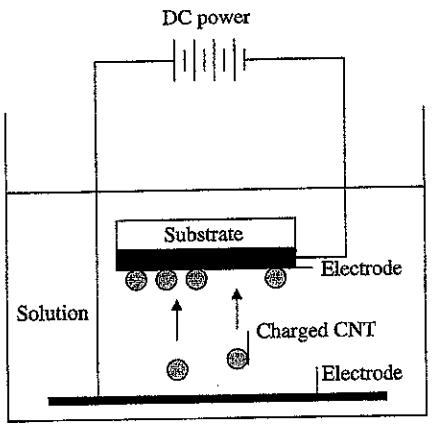

Figure 8.10 Typical deposition mechanism in the EPD process.

of the EPD process. In this deposition mechanism, the substrate is placed in an electrophoresis solution. The CNTs in the solution are charged and then move to the electrode. Following the motion, the CNTs are deposited onto the electrode.

CNTs can be grown directly onto the substrate using either CVD or EPD. Although the uniformity obtained using the CVD or EPD approach exceeds that obtained using the arcing method, the purity obtained is lower.

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8.4.3 Surface conduction emitter

In a SCE device, a palladium oxide (PdO) film is used as an emitter and a nano-gap is used to extract the electrons from the surface of he PdO film.[57] These electrons are called surface conduction electrons. The structure of the SCE display differs a little from the display structure using the Spindt-type emitter and the CNT emitter. Figure 8.11 shows a typical structure of a SCE display, which is commonly called a surface electron display (SED). In this figure, the electron is horizontally extracted from the emitter to the gate. An anode voltage is applied to collect the emitted electron.

The gap between the gate and the cathode is about 10 nm. The cathode and the gate are made of platinum. The emitter is PdO. The platinum film is patterned by photolithography while the PdO film of the emitter is deposited by ink-jet printing. Figure 8.12 shows a typical process flow for a SCE. At

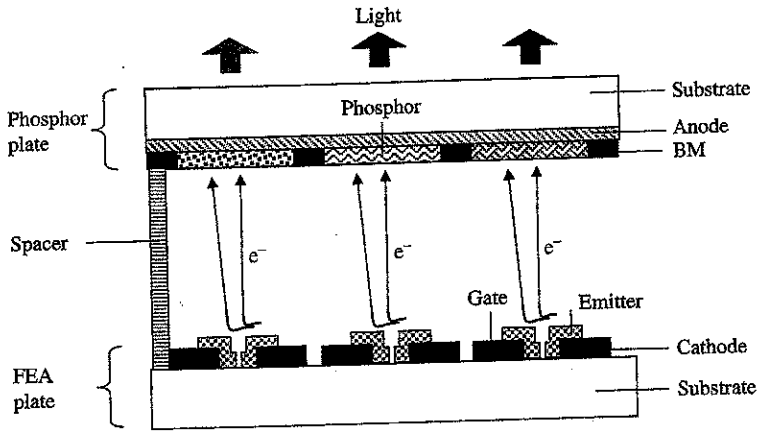

Figure 8.11 Typical structure of a SCE display (surface electron display).

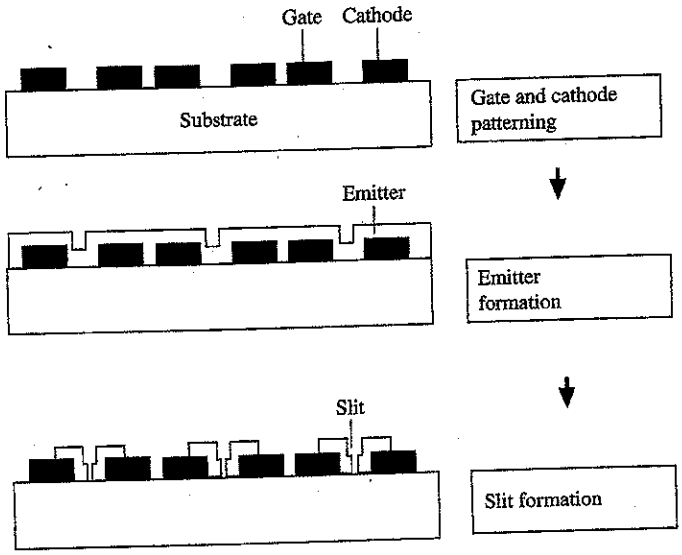

Figure 8.12 Typical process flow for a SCE.

the beginning of this process, the gate and cathode are patterned. The following step is to coat a layer of emitter material. After the coating of the emitter material is completed, a slit is formed with nanometric dimensions. This slit formation is critical since a slit with a nanostructure is required.

8.5 Panel process

The panel process involves a FEA plate and a phosphor plate and comprises assembly and aging processes. Figure 8.13 shows a typical process flow. One of the main processes for the FEA plate is the emitter formation process while the major process for the phosphor plate is the phosphor formation process. Assembly and aging processes are associated with panel alignment, vacuum-tight sealing and characteristic stabilization.

As stated in a previous section, the three main emitters are the Spindt emitter, the CNT emitter and the SED emitter. Figure 8.14 shows the display process of the Spindt emitter. The major process for the FEA plate was described in the previous section. For the phosphor plate, black matrix (BM) formation is commonly used to increase the contrast ratio of the display. Following BM formation, phosphor formation is performed. Notably, red (R), green (G) and blue (B) phosphors are deposited and patterned in phosphor formation. After the FEA plate and the phosphor plate have been formed, assembly and aging are conducted so that the process of the FED panel is completed.

Figure 8.15 shows the display process of a CNT-type emitter. The preceding section described the main process for a FEA plate. The CNT paste is prepared in a separate process, as presented in Figure 8.15. At the beginning of the CNT paste preparation, CNTs are formed and then purified. Following CNT purification, a solvent and a binder are typically added to form the CNT paste. As to the phosphor plate, BM formation is commonly employed to increase the contrast ratio of the display. After BM formation has been completed, R, G and B phosphors are deposited and patterned. After the FEA plate and phosphor plate are formed, the assembly and aging processes are conducted to complete the FED panel.[58]

Figure 8.16 shows the display process for a SCE. The previous section described the main process for the FEA plate. Additionally, PdO paste is prepared in separate processes, as presented in Figure 8.16. The preparation of the PdO paste begins with formation of PdO powder. Then, a solvent and binder are typically added to form the PdO paste. As to the phosphor plate process, BM formation is commonly adopted to increase the contrast ratio of the display. After BM formation, R, G and B phosphors are deposited and patterned during phosphor formation. Following the formation of the FEA plate and the phosphor plate, the assembly and aging process complete the FED panel.[59]

Screen printing,[60] photolithography and sandblasting are the three major approaches for forming layers in the FED process. Among these major approaches, screen printing is the most commonly used approach for the FED process. This approach can be adopted for the cathode, gate electrode, dielectric, BM and phosphors layers. Figure 8.17 shows the side view of a typical screen-printing process.

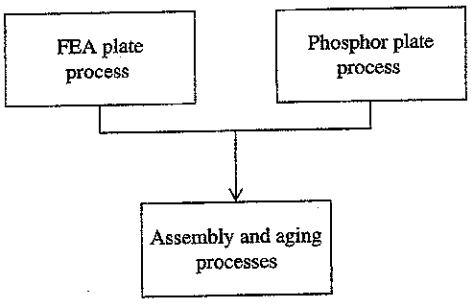

Figure 8.13 Typical process flow for a FED.

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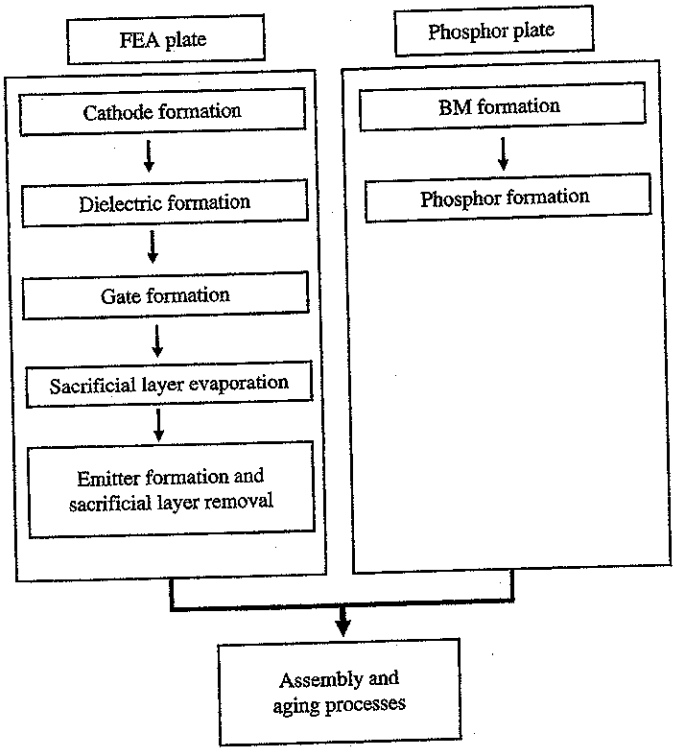

Figure 8.14 Typical process flow of FED with Spindt emitter.

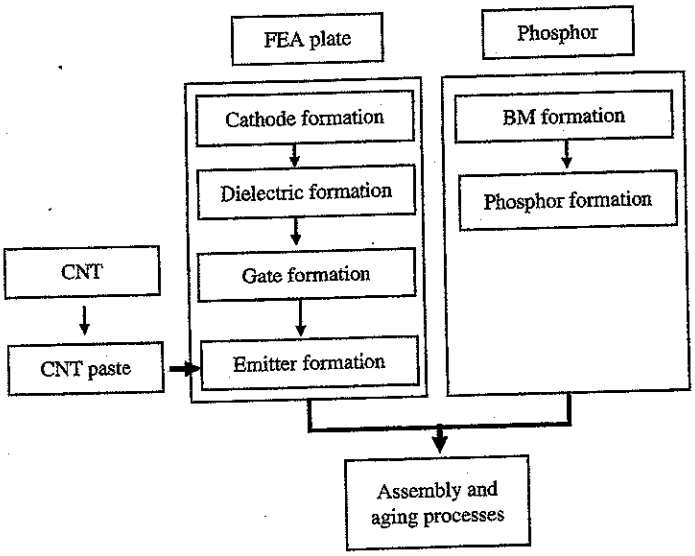

Figure 8.15 Typical process flow for FED with CNT emitter.

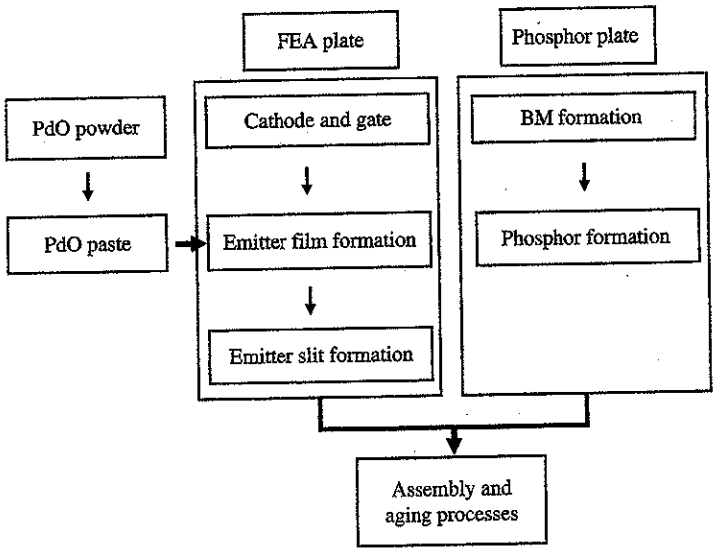

Figure 8.16 Typical process flow for FED with SCE.

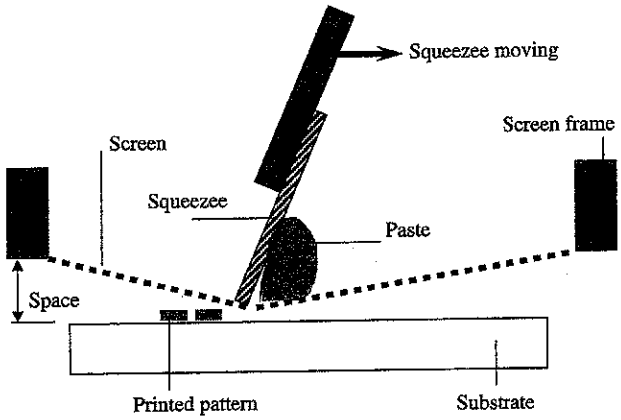

Figure 8.17 Side view of screen printing.

The screen mask, the paste and the printing machine are three major elements of screen printing.[61] A good paste should easily pass through a screen mask when a shear force is applied to the paste. However, the pattern of the paste should become solid and stand still when no shear force is applied, such that it does not diffuse and high resolution is maintained. After the paste is deposited, it must be dried and fired. Drying removes the solvent: the process temperature is typically under 150 °C. Firing removes the binder and melts the particle at a typical process temperature of more than 400 °C. Figure 8.18 shows the typical process temperature profile with process time.

The critical aspect of the drying process is the uniformity of drying from the outer surface to the inner core as well as from the edge to the center of the paste layer. In the firing process, the binder must be fully removed and the accumulated stress must be reduced as much as possible.

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8.6 Field emission

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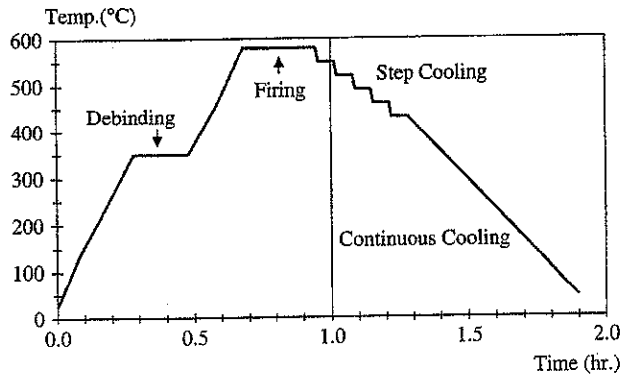

Figure 8.18 Typical process temperature profile.

Photolithography is another important approach used in the FED process which is also commonly used in display and semiconductor processes. This process uses a photoresist to form a pattern and subsequent etching of the desired material. Stripping the photoresist leaves the desired pattern.

8.6 Field emission array plate techniques

An optimal field emission device must have the following features: (1) a sharp emitter; (2) an emitter with a low work function to enhance electron emission;[61] (3) an emitter with a high melting point to withstand the high temperature caused by resistive heating;[62] (4) a small gate opening for a gated emitter structure to increase the electric field;[63] and (5) a thick dielectric film between the electrodes to maintain the necessary operating voltage without breakdown or significant leakage. Field emission devices include many devices that use an electron source, such as a scanning tunneling microscope.[64]

The substrate in a FED not only provides a base for the film or paste deposition but also isolates the vacuum. Therefore, substrates with a smooth surface and a robust mechanical strength are required. The additional issue associated with FED substrates is thermal expansion due to the high temperature of the FED process. Sodalime glass is typically used in a FED substrate with a thickness of typically 2.8 mm. Since thermal expansion may produce an error in the image position,[65] sodalime glass with a high strain point is used to eliminate the thermal expansion of the substrate and control the error in the image position. As the FED panel is a high-vacuum device, the substrate receives an air pressure of about 1 atm from outside of the panel. Accordingly, deployment of spacers at particular positions of the FEA plate or phosphor plate is demanded. Deformation can occur when the spacer deployment is insufficient. Meanwhile, the glass should also be sufficiently strong to sustain the pressure difference. Additionally, the substrate in the FEA plate typically must have an exhausting hole. During the evacuation, normal air is pumped through this exhausting hole.

The floating process is commonly adopted for the formation of sodalime glass, as shown in Figure 8.19. At the beginning of this process, raw material is placed in the melting furnace. Molten glass is formed and then floats on the surface of the molten metal. This molten glass therefore has a smooth surface. Glass is formed upon annealing. The floating process is a traditional process for forming soadlime glass and is cost-effective.

An electrode in a FEA plate typically comprises a cathode and a gate electrode. The cathode provides an electrical base for the emitter and the cathode is typically silver paste with a thickness of 10 μm. The process for forming the cathode typically is screen printing, as shown in Figure 8.20. The silver paste

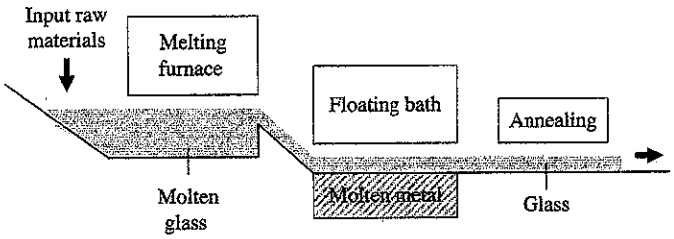

Figure 8.19 Typical floating process for forming glass.

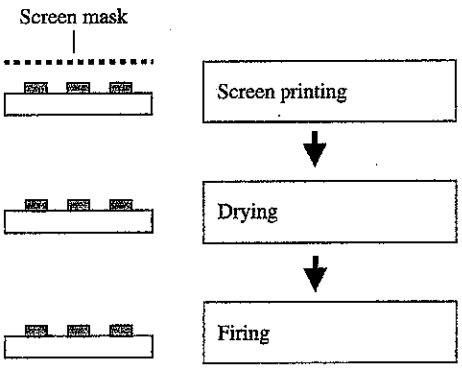

Figure 8.20 Typical cathode formation using screen printing.

is screen-printed through a patterned screen mask. The pattern is formed on the substrate and then dried and fired. A firm and solid pattern of electrode is therefore formed.

The alternative approach for forming a cathode is to deposit photosensitive silver paste on the substrate and then to form a pattern by photolithography. The line width resolution achieved using the photolithographic approach is 20 μm, which is better than the 50 μm of the screen-printing approach. Screen printing is a commonly used approach for forming a cathode since the material cost is lower and the process steps are simpler.[66]

The dielectric is the layer between the gate electrode and the cathode. The layer must be a good insulator to reduce leakage current. The dielectric layer is typically formed by screen printing with a thickness of 20 μm or using a CVD process with a thickness of 2 μm. The thickness of this film is dominated by the need to minimize leakage current.

The gate electrode is used to control or to modulate the emission from the cathode, which is typically silver paste with a thickness of 10 μm. The cathode is typically formed by screen printing. The alternative approach for forming the gate electrode is to deposit a photosensitive silver paste on the dielectric layer and then to form a pattern photolithographically.

8.7 Phosphor plate techniques

The phosphor plate comprises substrate, anode and phosphor layers. Its major function is to generate brightness. The substrate in the phosphor plate is similar to the substrate used in the FEA plate. The anode in the phosphor plate is an electrical base for phosphor. The anode voltage can reach hundreds or tens of thousands of volts.

The phosphors used in FEDs are electron-excited.[67] The luminescence mechanism is cathodoluminescence.[68] The distance between the gate and the anode is kept short to keep electron emission as a

Table 8.3 Comm

Item	
Blue-green	ZnO:Z
Blue	ZnS:Z
	ZnS:A
Green	ZnS:C
	$Zn_{0.65}$
Red	(ZnCe
	Y_2O_2S

Table 8.4 Phosp

Item	
Blue	ZnS:Ag
Green	ZnS:Cu,
Red	Y_2O_2S:E

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8.8 Assembly and

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Element Exhibit 2012 / Page 18 of 24

Table 8.3 Common phosphors used in low-voltage applications.

Item		Decay time (μs)	Relative efficiency (%)	Luminance efficiency (lm W^{-1})	Excitation energy (V)
Blue-green	ZnO:Zn	8	10	5.0–10.0	200–400
Blue	ZnS:Zn	—	~1	0.5–0.8	200–400
	ZnS:Ag,Al	—		0.3–0.6	200–400
Green	ZnS:Cu,Al	250	3	1.0–1.5	200–400
	$Zn_{0.65}Cd_{0.35}S$:Ag,Cl	—	—	4.5	200–400
Red	(ZnCd)S:Ag	150–300	4	0.5–1.0	200–400
	Y_2O_2S:Eu	—	—	0.5–1.0	200–400

Table 8.4 Phosphors commonly used in high-voltage applications.

Item		Decay time (μs)	Relative efficiency (%)	Luminance efficiency (lm W^{-1})	Excitation energy (kV)
Blue	ZnS:Ag	30–50	21	—	10–30
Green	ZnS:Cu,Al	30–50	17–23	40–65	10–30
Red	Y_2O_2S:Eu	200	13	—	10–30

proximity focusing and not to spread wide. The applied voltage must be low since the distance is short. Table 8.3 presents the phosphors commonly used in low-voltage applications.[69,70] Most of the materials have low luminance efficiency in the range of the applied voltage. ZnO phosphor is a favorable exception with relatively high luminance efficiency.[71] However, the green saturation of ZnO is not high, with the green color being mixed with light blue color. Accordingly, ZnO is commonly adopted in monochrome FEDs but it is not commonly used in color FEDs. Additionally, the luminance efficiency varies with the applied voltage. Restated, the luminance efficiency typically increases with increasing applied voltage.

Although a short distance between gate and anode can ensure a sufficiently narrow distribution of emission spot sizes, only low-voltage phosphors, which typically have low luminance efficiency, can be used.[72] To increase luminance efficiency, high-voltage phosphor is used, as shown in Table 8.4.[73] These phosphors have relative high efficiency around the applied voltage. However, the distance between the gate and the anode must be sufficiently large that the device will not break down.

Notably, the distribution of phosphor particle sizes is also important.[74] Figure 8.21 shows the normal distribution of the sizes of phosphor particles. Since a uniform distribution of phosphor particle sizes typically provides a higher pixel resolution, large and small phosphor particles should be removed before or during the phosphor process.

Outgas from the surface layers of the FED device may contaminate and degrade the phosphor. As the phosphor is degraded, the brightness is reduced. The phosphor layer is typically formed by screen printing with a thickness of 30 μm for each color. Figure 8.22 shows the typical screen-printing process of the phosphor layer. In this process, phosphor paste is deposited followed by drying and firing. Drying removes the solvent material and firing removes the binder material.

8.8 Assembly and aging techniques

The assembly process binds an FEA plate and a phosphor plate into a display panel with vacuum-tight sealing and evacuation.[75] After assembly, aging is required to expose defects and stabilize the quality of the display. Figure 8.23 presents a typical assembly and aging process. At the beginning of this process, a spacer and sealing layer are formed. Then, panel alignment, sealing, evacuation and aging are performed.

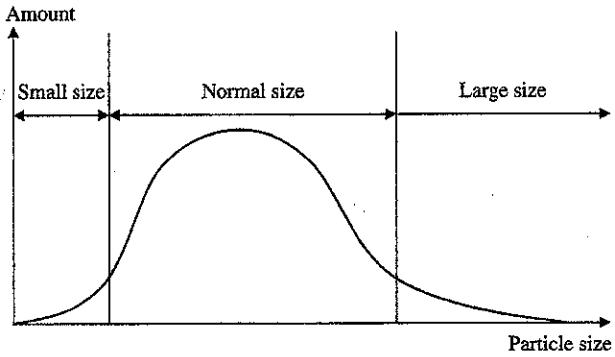

Figure 8.21 Normal distribution of sizes of phosphor particles.

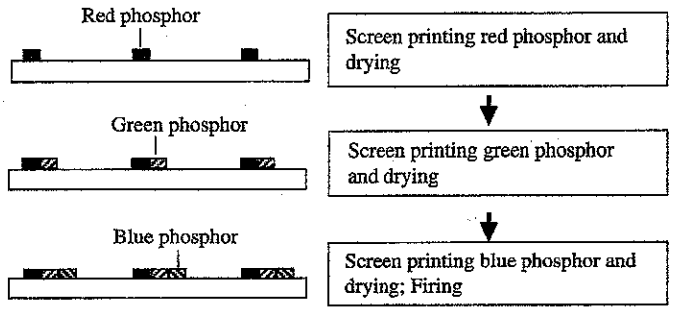

Figure 8.22 Typical screen-printing process for forming a phosphor layer.

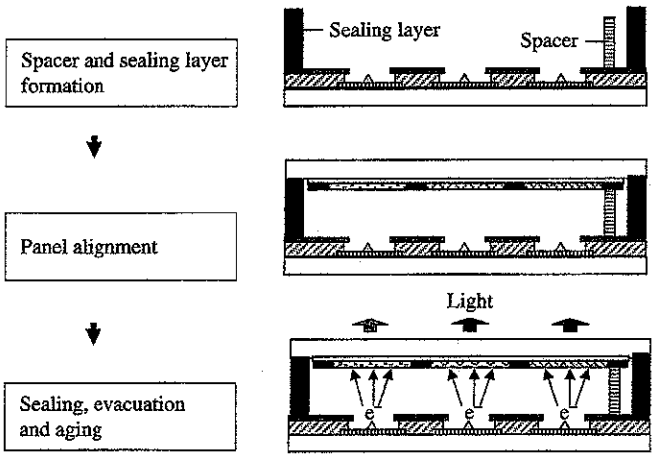

Figure 8.23 Typical assembly and aging process.

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Element Exhibit 2012 / Page 20 of 24

8.8.1 Spacer

The spacer maintains a uniform space between the FEA plate and the phosphor plate.[76] Therefore, the height of the spacer determines the distance between the gate and anode. In a high-vacuum device, such as a FED, the spacer supports the substrates and prevents them from deforming or cracking. Accordingly, the spacer not only should be a high-vacuum material but also must be tough with high compressive strength. Its width is preferably less than tens of micrometers, since the area of the spacer cannot display. For an insufficiently thin width of spacer, the resolution of the display is limited. The spacer is typically from 100 to 1000 μm in height.[77] The spacer height is determined by the applied voltage. In general, a high voltage is required to yield high luminance efficiency. At a low voltage of a few hundred volts, a short spacer, about 100 μm long, is sufficient to withstand the applied voltage. For a high anode voltage of more than a few thousand volts, long spacers, of over 1000 μm, are required to prevent breakdown. Notably, electron emission spreads widely when the spacer is long. Hence, the emission spot in the phosphor plate becomes large.[78] In all cases, the spacer must have a high aspect ratio structure.

The material of the spacer is typically dielectric. Accordingly, the spacer is easily charged when electrons travel towards the anode. The charging mechanism in the spacer can undesirably discharge during display. This phenomenon causes undesirable arcing inside the display cell. Slight arcing disturbs the display quality. Seriously arcing damages the device. To prevent these phenomena, a spacer material must be a slightly conductive dielectric rather than a normal dielectric.

Screen printing, placement and dispensing approaches can be adopted to form a spacer. Since the screen-printing approach must be repeated many times, the spacer width is not easily controlled and the process is time-consuming. Therefore, the placement approach, shown in Figure 8.24, is an alternative and effective approach for forming the spacer. In this process, sealing pastes are deposited at the desired locations of the FEA plate. After this step has been completed, spacers are placed on top of these sealing pastes and then the sealing paste is cured. The dispensing approach provides a higher aspect ratio, which is the ratio of the rib height to the width.[79]

8.8.2 Sealing layer formation and panel alignment

Typical sealing layer materials are glass frits and glass powder, which is a vacuum material and provides a vacuum-tight sealing.[80, 81] The material must have a low melting point, and thus be compatible with glass substrate. The use of epoxy material, commonly used in LCDs, as a sealing layer is not appropriate

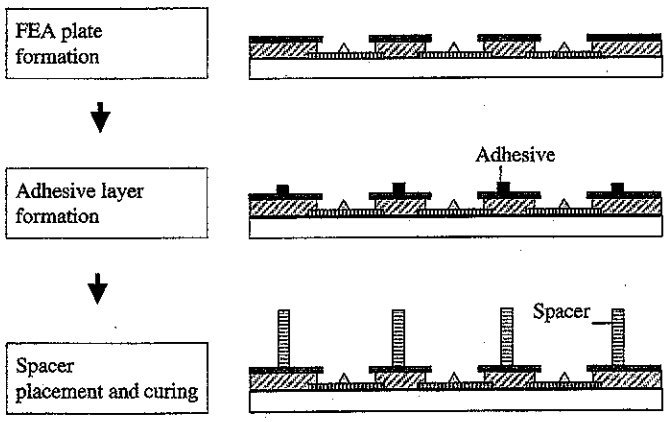

Figure 8.24 Placement approach for spacer formation.

in the FED process since outgas is usually given out of the epoxy material after the sealing process. This outgas can contaminate the display cell and degrade the performance of the display. The first step of the sealing process is to dispense a sealing layer onto the surrounding area of a FEA plate or phosphor plate.

The next step is to align the FEA plate and the phosphor plate. The accuracy of this alignment is critical and can affect the display quality. The main challenge of this process is the alignment shift during the high-temperature sealing process. The alignment of the FEA plate and phosphor plate is typically maintained by clippers.

When the FEA plate and the phosphor plate are aligned and clipped, an additional sealing paste must also be deposited in the area that surrounds the small opening of the FEA plate. Then, an exhausting tube is placed on the deposited area of the small opening of the FEA plate. An alternative approach, called tubeless sealing, does not use an exhausting tube. The advantages of this tubeless sealing approach are the faster evacuation and thinner panel.[82] The evacuation is faster because the panel vacuum is obtained from a ready vacuum of the whole chamber and this chamber vacuum can pump down before the panel process. The panel can be thinner when a tip-off tail of the exhaust tube is absent. However, the gas given off by the sealing paste using tubeless sealing can be sealed inside of the panel and can then contaminate the panel. Tubeless sealing demands extra work to clean the contamination inside of the panel.[83]

8.8.3 Sealing

The sealing process melts the material of the sealing layer to bind the FEA plate to the phosphor plate permanently.[84] The gas given off during the sealing process contaminates the emitter. Because of the thermal characteristics of the glass frits and glass powder, the sealing is typically performed at high temperature. The typical sealing process temperature is 450 °C. Clipper selection is important since the clipper may lose binding strength during sealing. For an improper selection of clipper, the panel alignment may be shifted during sealing. Moreover, the glass substrate may crack during sealing at high temperature.

8.8.4 Evacuation and sealing off

The evacuation begins in the viscous flow region, in which the mean free path is short and the vacuum pumping speed is rather high. When a high-vacuum environment is achieved, the evacuation is in the molecular flow regime, in which the mean free path is large and the vacuum pumping speed is rather slow. Since the display cell depends on a high-vacuum environment, a vacuum process to evacuate all of the gas from each display cell is critical. In addition to the physical vacuum pump, chemical getting is adopted in FED processing to assist the vacuum pump and adsorb these impurities.

The getter is the main material in a chemical pump.[85] This getter is a material that can absorb gas to yield a vacuum.[86] Radiofrequency heating is commonly adopted to activate and heat the getter but not the glass substrate. Improper heating of the getter can crack the substrate. The additional function of the getter is to absorb the impurities which sometimes are poison gases. Since the poison gases may be emitted into the display cell in the sealed panel, this poison gas must be removed from the sealed panel. The getter can act as a poison gas absorber and maintain a clean gas environment in the display cell. Getters are of two types: evaporation getters (EGs) and nonevaporation getters (NEGs). The EG type has a larger effective area for reaction with gas but the evaporated material may evaporate onto the undesired area and contaminate the device.

The tipping-off of the exhausting tube must be performed carefully so that gas given off during the tip-off process can evacuate out and not be left inside of the panel. Therefore, a preliminary tip-off process is typically needed to evacuate the gas given off so that only very little given-off gas is left inside the panel. In order to perform the tip-off process, electric heating or gas heating on the exhausting

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8.8.5 Aging

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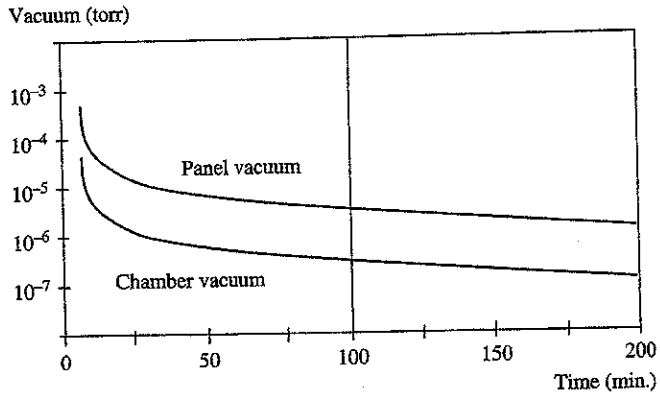

Figure 8.25 Pump chamber vacuum and panel vacuum for a 3-inch panel with 200 μm high spacers.

tube is commonly used. Electric heating uses electricity to heat a ceramic and the heated ceramic is used to tip off the exhausting tube, while gas heating uses gas directly to tip off the exhausting tube. Most importantly, electrical heating needs more apparatus than gas heating, although electrical heating is relatively controllable.

Notably, the pressure of the vacuum in the pump chamber differs by one to two orders of magnitude from that in the panel. Figure 8.25 shows plots of the chamber vacuum and the panel vacuum for a 3-inch panel with 200 μm high spacers.

8.8.5 Aging

The purpose of aging is to expose defects. Contamination of the emitter surface and defects in the dielectric and in the electrode are revealed during the aging process. Aging can also stabilize the emission since it can polish or smooth the emitter surface and remove surface contamination from the emitter.

8.9 System techniques

FED circuits perform power supply, signal processing and scan/data driving functions. Figure 8.26 shows a typical block diagram. In this diagram, the FED panel is driven by a driver circuit while the signal processing circuit provides a video signal to the panel.

Since a few tens of volts must be applied to operate a FED panel, a high-voltage driver IC is required. Additionally, amplitude and pulse width modulation are commonly adopted in FEDs because field emission devices have linear current–voltage (I–V) and high response characteristics.[87] Among scan addressing, direct addressing, matrix addressing and other addressing approaches, matrix addressing can address more data in a short address time. Additionally, each pixel is electrically connected to each row and each column in matrix addressing. For VGA (640 × 480) data format, the number of scan lines is 480 and the number of data lines is 640. Figure 8.27 shows typical matrix addressing.

As shown in Figure 8.27, data 1 to 640 are sent to the panel when row 1 is scanned. After row 1 is scanned, row 2 is scanned. Data 1 to 640 are sent to panel when row 2 is scanned. Such scanning proceeds sequentially from row 1 to row 480 to display.

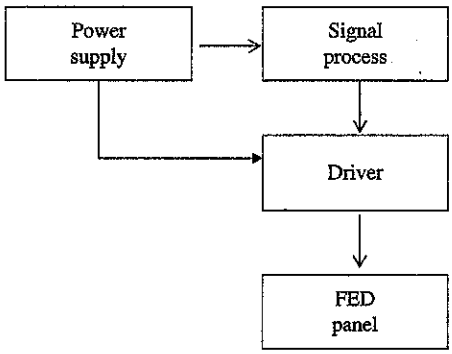

Figure 8.26 Typical FED system.

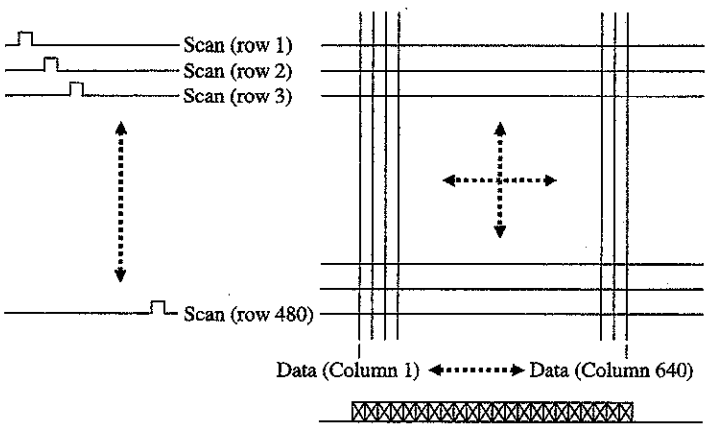

Figure 8.27 Typical matrix addressing.

Homework problems

8.1 Draw a trajectory of electrons that are emitted from emitter to anode for distances of 100 μm and 5000 Å. Does the spot size of the electrons at a distance of 100 μm differ from that at 5000 μm?

8.2 Classify the emission when the electric field is 5×10^7 V cm^{-1} and the temperature is 500 K. Does field emission dominate?

8.3 Describe the process constraints of the Spindt emitter, CNT emitter and SCE.

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IPR2023-00605
Element Exhibit 2012 / Page 24 of 24