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For

**A METHOD, APPARATUS, AND SYSTEM FOR ENERGY EFFICIENCY AND ENERGY
CONSERVATION INCLUDING POWER AND PERFORMANCE BALANCING BETWEEN
MULTIPLE PROCESSING ELEMENTS AND/OR A COMMUNICATION BUS**

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**A METHOD, APPARATUS, AND SYSTEM FOR ENERGY EFFICIENCY AND ENERGY
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FIELD

[0001] This disclosure pertains to energy efficiency and energy conservation in integrated circuits, as well as code to execute thereon, and in particular but not exclusively, to balancing power and performance between processing elements and/or a communication bus.

BACKGROUND

[0002] Advances in semi-conductor processing and logic design have permitted an increase in the amount of logic that may be present on integrated circuit devices. As a result, computer system configurations have evolved from a single or multiple integrated circuits in a system to multiple hardware threads, multiple cores, multiple devices, and/or complete systems on individual integrated circuits. Additionally, as the density of integrated circuits has grown, the power requirements for computing systems (from embedded systems to servers) have also escalated. Furthermore, software inefficiencies, and its requirements of hardware, have also caused an increase in computing device energy consumption. In fact, some studies indicate that computers consume a substantial amount of the entire electricity supply for the United States of America.

[0003] As a result, there is a vital need for energy efficiency and conservation associated with integrated circuits. And as servers, desktop computers, notebooks, ultrabooks, tablets, mobile phones, processors, embedded systems, etc. become even

more prevalent (from inclusion in the typical computer, automobiles, and televisions to biotechnology), the effect of computing device sales stretches well outside the realm of energy consumption into a substantial, direct effect on economic systems.

[0004] Furthermore, as integrated circuit density has grown, the ability to consolidate multiple devices in a single integrated circuit and/or package has similarly increased. As an illustrative example, system on chip (SOC) devices have recently gained popularity. However, often SOC's (and like components) integrate multiple devices into a single device/circuit, but they also inherit each individual device's power, performance, and thermal constraints. Therefore, a device with a host processor and a graphics processor usually implements power savings policies individually and separately. And even if a power policy is defined for the entire package, it often only contemplates assumed power requirements for each of the individual devices without balancing power and performance amongst asymmetric cores to achieve maximum overall performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention is illustrated by way of example and not intended to be limited by the figures of the accompanying drawings.

[0006] Figure 1 illustrates an embodiment of a logical representation of a system including an integrated circuit having a multi-processing element processor and integrated graphics processor.

[0007] Figure 2 illustrates an embodiment of a logical representation of a computer system configuration.

[0008] Figure 3 illustrates another embodiment of a logical representation of a computer system configuration.

[0009] Figure 4 illustrates another embodiment of a logical representation of a computer system configuration.

[0010] Figure 5 illustrates an embodiment of a logical representation of an integrated circuit to balancing power among processing elements to achieve maximum overall performance.

[0011] Figure 6 illustrates another embodiment of a logical representation of an integrated circuit to balancing power among processing elements to achieve maximum overall performance.

[0012] Figure 7 illustrates an embodiment of a flow diagram for balancing power between a processor and graphics processor to achieve maximum performance within a power limit.

[0013] Figure 8 illustrates another embodiment of a flow diagram for balancing power between a processor and graphics processor to achieve maximum performance within a power limit.

[0014] Figure 9 illustrates an embodiment of a logical representation of a block diagram for units/modules to balancing power among processing elements and/or a communication bus to achieve maximum overall performance.

[0015] Figure 10 illustrates an embodiment of a flow diagram for balancing power between a processor, a graphics processor, and/or a communication bus to achieve maximum performance within a power limit.

DETAILED DESCRIPTION

[0016] In the following description, numerous specific details are set forth, such as examples of specific types of specific processor and system configurations, specific hardware structures, specific architectural and micro architectural details, specific register configurations, specific structures for determining workloads, specific modules to determine and set performance/power limits, specific types of performance limits, specific types of processing devices, specific types of program code, specific performance bottleneck assumptions, specific devices including asymmetric processors, etc. in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that these specific details need not be employed to practice the present invention. In other instances, well known components or methods, such as specific and alternative processor architectures, specific logic circuits/code for described algorithms, specific firmware code, specific interconnect operation, specific workload determination, specific frequency setting techniques, specific power limit determination and implementation algorithms, and other specific operational details of processors haven't been described in detail in order to avoid unnecessarily obscuring the present invention.

[0017] Although the following embodiments are described with reference to energy conservation and energy efficiency in specific integrated circuits, such as in computing platforms or microprocessors, other embodiments are applicable to other types of integrated circuits and logic devices. Similar techniques and teachings of embodiments described herein may be applied to other types of circuits or semiconductor

devices that may also benefit from better energy efficiency and energy conservation. For example, the disclosed embodiments are not limited to desktop computer systems. And may be also used in other devices, such as handheld devices, systems on a chip (SOC), and embedded applications. Some examples of handheld devices include cellular phones, Internet protocol devices, digital cameras, personal digital assistants (PDAs), and handheld PCs. Embedded applications typically include a microcontroller, a digital signal processor (DSP), a system on a chip, network computers (NetPC), set-top boxes, network hubs, wide area network (WAN) switches, or any other system that can perform the functions and operations taught below. Moreover, the apparatus', methods, and systems described herein are not limited to physical computing devices, but may also relate to software optimizations for energy conservation and efficiency. As will become readily apparent in the description below, the embodiments of methods, apparatus', and systems described herein (whether in reference to hardware, firmware, software, or a combination thereof) are vital to a 'green technology' future balanced with performance considerations .

[0018] The method and apparatus described herein are for balancing power between multiple asymmetric devices to achieve maximum overall performance. Specifically, power balancing and allocation is primarily discussed below in reference to an integrated circuit and/or package including a central/host processor (or cores thereof) and a graphics processor (or cores thereof). Yet, the apparatuses and methods described herein are not so limited, as they may be implemented in conjunction with any integrated circuit device including any type of asymmetric or symmetric processing cores. For

example, power balancing and allocation, as described herein, may be utilized between two host processing cores, between processing cores and memory, and/or between integrated I/O devices. And as discussed above, it may be utilized in servers, desktops, ultrabooks, tablets, small form-factor devices, handheld devices, SOCs, or embedded applications.

[0019] Referring to **Figure 1**, an embodiment of an integrated circuit (or package) including multiple devices/cores is illustrated. Integrated Circuit (IC) **100** includes any processor or processing device, such as a microprocessor, an embedded processor, a digital signal processor (DSP), a network processor, a handheld processor, an application processor, a co-processor, or other device to execute code. Processor **100**, in one embodiment, includes at least two central, host, or processing cores—core **101** and **102**, which may be asymmetric cores or symmetric cores (the illustrated embodiment), as well as an Input/Output (I/O) device **180**, such as a graphics processor (or cores thereof). However, IC **100** may include any number of processing elements that may be symmetric or asymmetric.

[0020] In one embodiment, a processing element refers to hardware or logic to support a software thread. Or in another embodiment a processing element refers to a core or processing logic of a device, such as a graphics processor/core, network controller, embedded processor, microcontroller, etc. Other Examples of hardware central processing elements include: a thread unit, a thread slot, a thread, a process unit, a context, a context unit, a logical processor, a hardware thread, a core, and/or any other element, which is capable of holding a state for a processor, such as an execution state or

architectural state. In other words, a processing element, in one embodiment, refers to any hardware capable of being independently associated with code, such as a software thread, operating system, application, or other code. A physical processor typically refers to an integrated circuit, which potentially includes any number of other processing elements, such as cores or hardware threads.

[0021] A processing (or central processing unit) core often refers to logic located on an integrated circuit capable of maintaining an independent architectural state, wherein each independently maintained architectural state is associated with at least some dedicated execution resources. In contrast to cores, a hardware thread typically refers to any logic located on an integrated circuit capable of maintaining an independent architectural state, wherein the independently maintained architectural states share access to execution resources. As can be seen, when certain resources are shared and others are dedicated to an architectural state, the line between the nomenclature of a hardware thread and core overlaps. Yet often, a core and a hardware thread are viewed by an operating system as individual logical processors, where the operating system is able to individually schedule operations on each logical processor.

[0022] Physical package **100**, as illustrated in **Figure 1**, includes two processing cores, core **101** and **102**. Here, core **101** and **102** are considered symmetric cores, i.e. cores with the same configurations, functional units, and/or logic. In another embodiment, core **101** includes an out-of-order processor core, while core **102** includes an in-order processor core. However, cores **101** and **102** may be individually selected from any type of core, such as a native core, a software managed core, a core adapted to

execute a native Instruction Set Architecture (ISA), a core adapted to execute a translated Instruction Set Architecture (ISA), a co-designed core, or other known core. Yet to further the discussion, the functional units illustrated in core **101** are described in further detail below, as the units in core **102** operate in a similar manner.

[0023] As depicted, core **101** includes two hardware threads **101a** and **101b**, which may also be referred to as hardware thread slots **101a** and **101b**. Therefore, software entities, such as an operating system, in one embodiment potentially view processor **100** as four separate processors, i.e. four logical processors or processing elements capable of executing four software threads concurrently. As eluded to above, a first thread is associated with architecture state registers **101a**, a second thread is associated with architecture state registers **101b**, a third thread may be associated with architecture state registers **102a**, and a fourth thread may be associated with architecture state registers **102b**. Here, each of the architecture state registers (**101a**, **101b**, **102a**, and **102b**) may be referred to as processing elements, thread slots, or thread units, as described above. As illustrated, architecture state registers **101a** are replicated in architecture state registers **101b**, so individual architecture states/contexts are capable of being stored for logical processor **101a** and logical processor **101b**. In core **101**, other smaller resources, such as instruction pointers and renaming logic in rename allocator logic **130** may also be replicated for threads **101a** and **101b**. Some resources, such as reorder buffers in reorder/retirement unit **135**, ILTB **120**, load/store buffers, and queues may be shared through partitioning. Other resources, such as general purpose internal

registers, page-table base register(s), low-level data-cache and data-TLB **115**, execution unit(s) **140**, and portions of out-of-order unit **135** are potentially fully shared.

[0024] Processor **100** often includes other resources, which may be fully shared, shared through partitioning, or dedicated by/to processing elements. In **Figure 1**, an embodiment of a purely exemplary processor with illustrative logical units/resources of a processor is illustrated. Note that a processor may include, or omit, any of these functional units, as well as include any other known functional units, logic, or firmware not depicted. As illustrated, core **101** includes a simplified, representative out-of-order (OOO) processor core. But an in-order processor may be utilized in different embodiments. The OOO core includes a branch target buffer **120** to predict branches to be executed/taken and an instruction-translation buffer (I-TLB) **120** to store address translation entries for instructions.

[0025] Core **101** further includes decode module **125** coupled to fetch unit **120** to decode fetched elements. Fetch logic, in one embodiment, includes individual sequencers associated with thread slots **101a**, **101b**, respectively. Usually core **101** is associated with a first Instruction Set Architecture (ISA), which defines/specifies instructions executable on processor **100**. Often machine code instructions that are part of the first ISA include a portion of the instruction (referred to as an opcode), which references/specifies an instruction or operation to be performed. Decode logic **125** includes circuitry that recognizes these instructions from their opcodes and passes the decoded instructions on in the pipeline for processing as defined by the first ISA. For example, as discussed in more detail below decoders **125**, in one embodiment, include

logic designed or adapted to recognize specific instructions, such as transactional instruction. As a result of the recognition by decoders **125**, the architecture or core **101** takes specific, predefined actions to perform tasks associated with the appropriate instruction. It is important to note that any of the tasks, blocks, operations, and methods described herein may be performed in response to a single or multiple instructions; some of which may be new or old instructions.

[0026] In one example, allocator and renamer block **130** includes an allocator to reserve resources, such as register files to store instruction processing results. However, threads **101a** and **101b** are potentially capable of out-of-order execution, where allocator and renamer block **130** also reserves other resources, such as reorder buffers to track instruction results. Unit **130** may also include a register renamer to rename program/instruction reference registers to other registers internal to processor **100**. Reorder/retirement unit **135** includes components, such as the reorder buffers mentioned above, load buffers, and store buffers, to support out-of-order execution and later in-order retirement of instructions executed out-of-order.

[0027] Scheduler and execution unit(s) block **140**, in one embodiment, includes a scheduler unit to schedule instructions/operation on execution units. For example, a floating point instruction is scheduled on a port of an execution unit that has an available floating point execution unit. Register files associated with the execution units are also included to store information instruction processing results. Exemplary execution units include a floating point execution unit, an integer execution unit, a jump execution unit, a load execution unit, a store execution unit, and other known execution units.

[0028] Lower level data cache and data translation buffer (D-TLB) **150** are coupled to execution unit(s) **140**. The data cache is to store recently used/operated on elements, such as data operands, which are potentially held in memory coherency states. The D-TLB is to store recent virtual/linear to physical address translations. As a specific example, a processor may include a page table structure to break physical memory into a plurality of virtual pages.

[0029] Here, cores **101** and **102** share access to higher-level or further-out cache **110**, which is to cache recently fetched elements. Note that higher-level or further-out refers to cache levels increasing or getting further way from the execution unit(s). In one embodiment, higher-level cache **110** is a last-level data cache—last cache in the memory hierarchy on processor **100**—such as a second or third level data cache. However, higher level cache **110** is not so limited, as it may be associated with or include an instruction cache. A trace cache—a type of instruction cache—instead may be coupled after decoder **125** to store recently decoded traces.

[0030] In the depicted configuration, processor **100** also includes bus interface module **105**. Historically, controller **170**, which is described in more detail below, has been included in a computing system external to processor **100**. In this scenario, bus interface **105** is to communicate with devices external to processor **100**, such as system memory **175**, a chipset (often including a memory controller hub to connect to memory **175** and an I/O controller hub to connect peripheral devices), a memory controller hub, a northbridge, or other integrated circuit. And in this scenario, bus **105** may include any known interconnect, such as mutli-drop bus, a point-to-point interconnect, a serial

interconnect, a parallel bus, a coherent (e.g. cache coherent) bus, a layered protocol architecture, a differential bus, and a GTL bus.

[0031] Memory **175** may be dedicated to processor **100** or shared with other devices in a system. Common examples of types of memory **175** include dynamic random access memory (DRAM), static RAM (SRAM), non-volatile memory (NV memory), and other known storage devices. Similar to the discussion above, I/O device(s) **180** have been traditionally included in a computing system external to a central processing unit. Here, device **180** may include a graphic accelerator, processor or card coupled to a memory controller hub, data storage coupled to an I/O controller hub, a wireless transceiver, a flash device, an audio controller, a network controller, or other known device.

[0032] Note however, that in the depicted embodiment, the controller **170** and I/O device **180** are illustrated as part of processor **100**. Recently, as more logic and devices are being integrated on a single die, such as System on a Chip (SOC), each of these devices may be incorporated on processor **100** to form a single package or single integrated circuit with multiple devices. For example in one embodiment, memory controller hub **170** and a graphics processor/device **180** are included on the same package and/or die with a central processor unit to form IC **100**, which may be referred to herein as processor **100** that includes an integrated memory controller **170** and graphics device **180**. Here, a portion of the core (an on-core portion) includes one or more controller(s) **170** for interfacing with other devices such as memory **175** and/or a graphics device **180**. The configuration including an interconnect and controllers for interfacing with such

devices is often referred to as an on-core (or un-core configuration). As an example, bus interface **105** includes a ring interconnect with a memory controller for interfacing with memory **175** and a graphics controller for interfacing with graphics processor **180**. And graphics processor **180** may even have direct access to cache **110**. Yet, in the SOC environment, even more devices, such as the network interface, co-processors, memory **175**, graphics processor **180**, and any other known computer devices/interface may be integrated on a single die or integrated circuit to provide small form factor with high functionality and low power consumption. And as discussed in more detail below, when power policies are developed for the entire IC **100**, the techniques for power balancing between prominent, integrated devices, such as cores **101-102** and graphics device **180** become even more important.

[0033] In one embodiment, processor **100** is capable of executing a compiler, optimization, and/or translator code **177** to compile, translate, and/or optimize application code **176** to support the apparatus and methods described herein or to interface therewith. A compiler often includes a program or set of programs to translate source text/code into target text/code. Usually, compilation of program/application code with a compiler is done in multiple phases and passes to transform hi-level programming language code into low-level machine or assembly language code. Yet, single pass compilers may still be utilized for simple compilation. A compiler may utilize any known compilation techniques and perform any known compiler operations, such as lexical analysis, preprocessing, parsing, semantic analysis, code generation, code transformation, and code optimization.

[0034] Larger compilers often include multiple phases, but most often these phases are included within two general phases: (1) a front-end, i.e. generally where syntactic processing, semantic processing, and some transformation/optimization may take place, and (2) a back-end, i.e. generally where analysis, transformations, optimizations, and code generation takes place. Some compilers refer to a middle, which illustrates the blurring of delineation between a front-end and back end of a compiler. As a result, reference to insertion, association, generation, or other operation of a compiler may take place in any of the aforementioned phases or passes, as well as any other known phases or passes of a compiler. As an illustrative example, a compiler potentially inserts operations, calls, functions, etc. in one or more phases of compilation, such as insertion of calls/operations in a front-end phase of compilation and then transformation of the calls/operations into lower-level code during a transformation phase. Note that during dynamic compilation, compiler code or dynamic optimization code may insert such operations/calls, as well as optimize the code for execution during runtime. As a specific illustrative example, binary code (already compiled code) may be dynamically optimized during runtime. Here, the program code may include the dynamic optimization code, the binary code, or a combination thereof.

[0035] Similar to a compiler, a translator, such as a binary translator, translates code either statically or dynamically to optimize and/or translate code. Therefore, reference to execution of code, application code, program code, or other software environment may refer to: (1) execution of a compiler program(s), optimization code optimizer, or translator either dynamically or statically, to compile program code, to

maintain software structures, to perform other operations, to optimize code, or to translate code; (2) execution of main program code including operations/calls, such as application code that has been optimized/compiled; (3) execution of other program code, such as libraries, associated with the main program code to maintain software structures, to perform other software related operations, or to optimize code; or (4) a combination thereof.

[0036] In one embodiment, power control module **160**, which may include hardware, firmware, software, or a combination thereof, is able to balance and allocate power/frequency between devices of IC **100** to achieve maximum performance; even when IC **100** is under a power limit. Additionally, such allocation, in one scenario, is based on actual workload of devices, instead of assumptions of workload or power consumption. For example, a power limit (either a maximum power limit or a reduced limit during power saving modes) is provided for IC **100**. Previously, a maximum current (and as a corollary frequency) was reduced for all processing elements of IC **100** to meet the power limit. Instead, in this scenario, a device that is determined to be a bottleneck for performance, such as throughput performance as viewed from the perspective of an application, is allocated more current/frequency, while the other competing device is capped/limited to ensure the power limit is still met. In other words, a dynamic balance is continuously struck between devices to ensure the device that needs more resources for better overall performance is allocated such extra resources, while other devices are 'balanced' (reduced in performance) to meet a given power limit.

[0037] As a specific illustrative example, assume that I/O device **180** is a graphics processor. Here, processing cores **101, 102** and graphics device **180** form a producer and consumer relationship. Cores **101,102** receive and process instructions; some of which are offloaded to graphics processor **180** for processing (e.g. CPU cores **101, 102** send a pixel to GPU **180** to be textured, GPU **180** calculates a texture of the pixel to obtain a texel). Therefore, if the CPU cores **101, 102** are overworking (i.e. producing too much work for the GPU **180** to handle at its current performance level), then overall performance from a maximum potential is degraded (the extra performance that the CPU cores **101-102** are utilizing to overproduce could have been allocated to GPU **180**). Note that this overproducing scenario potentially occurs even when CPU cores **101, 102** are operating at the same or lower frequency than GPU **180**. And inversely, if CPU cores **101, 102** are under-producing (i.e. not generating enough work to keep GPU **180** busy), then once again the maximum potential performance is likely not being achieved. Moreover, the producer-consumer relations may also be view from the other perspective, where CPU cores **101,102** are to consume graphics output from producer **180** before CPU cores **101,102** can make further forward progress.

[0038] Therefore, in one embodiment, processing workload of cores **101-102** and graphics workload of graphics device **180** are determined. For example, an amount of activity (e.g. number of cycles active) over a quantum or period of time is determined for both cores **101-102** and graphics core **180**. And based on those workloads, performance of cores **101-102** and graphics core **180** are balanced to achieve maximum overall performance. As an illustrative example, if one of the devices (CPU cores **101-102** or

GPU cores **180**) are working at or near the maximum, while the other device is not fully occupied, then the near maximum device is allocated more performance (e.g. more frequency).

[0039] Note that when a power limit exists and IC **100** is not up against the power limit, the immediately aforementioned increase in performance may not include a counterbalancing reduction in the other device. For example, assume GPU cores **180** are fully occupied (all cycles during a period of time are active) and CPU cores **101-102** are only active 70% of the cycles during the period of time. In this scenario, CPU cores **101-102** are not working at their full capacity, but are still overproducing for GPU **180**. When IC **100** is not at a set power limit, then GPU **180** frequency, in one embodiment, is increased to meet the overproduction of CPU **101-102**. However, once GPU **180** starts consuming at a higher rate, CPU cores **101-102** are able to produce at even a higher rate. And if a power or thermal limit for IC **100** is reached, then if GPU **180** is to increase frequency (e.g. from the same assumptions above), then CPU **101-102**, in one embodiment, are limited/capped to ensure the power or thermal limit is not exceeded. However, the power and performance within that limit are intelligently allocated to ensure maximum, 'balanced' performance.

[0040] Referring to **Figures 2-4**, embodiments of a computer system configuration adapted to include processors to balance performance and power between processing element/cores on integrated circuits is illustrated. In reference to **Figure 2**, an illustrative example of a two processor system **200** with an integrated memory controller and Input/Output (I/O) controller in each processor **205, 210** is illustrated. Note that

processors **205, 210** each may include integrated graphics processors/cores, as discussed above. Although not discussed in detail to avoid obscuring the discussion, platform **200** illustrates multiple interconnects to transfer information between components. For example, point-to-point (P2P) interconnect **215**, in one embodiment, includes a serial P2P, bi-directional, cache-coherent bus with a layered protocol architecture that enables high-speed data transfer. Moreover, a commonly known interface (Peripheral Component Interconnect Express, PCIe) or variant thereof is utilized for interface **240** between I/O devices **245, 250**. However, any known interconnect or interface may be utilized to communicate to or within domains of a computing system.

[0041] Turning to **Figure 3** a quad processor platform **300** is illustrated. As in **Figure 2**, processors **301-304** are coupled to each other through a high-speed P2P interconnect **305**. And processors **301-304** include integrated controllers **301c-304c**. **Figure 4** depicts another quad core processor platform **400** with a different configuration. Here, instead of utilizing an on-processor I/O controller to communicate with I/O devices over an I/O interface, such as a PCI-E interface, the P2P interconnect is utilized to couple the processors and I/O controller hubs **420**. Hubs **420** then in turn communicate with I/O devices over a PCIe-like interface.

[0042] Referring next to **Figure 5**, an embodiment of a logical representation of modules to balance power between multiple processing elements to achieve maximum performance is depicted. Although only two cores are illustrated in **Figure 5**, any type of processing element and number thereof may be utilized. For example, in the most commonly discussed scenario herein (a CPU and GPU), both the CPU and GPU

potentially includes multiple cores. And as a result, workload determination (which is described in more detail below) may be in reference to individual cores or groupings of cores, such as a workload in regard to all CPU cores in comparison to all GPU cores.

[0043] However, to further the discussion in regards to **Figure 5**, core **505** is referred to below as a CPU core (or collection of CPU cores), while core **510** is referred to as a GPU core (or collection of GPU cores). It is also worth noting that although the discussion herein primarily focuses on power balancing between asymmetric cores; such balancing, in one embodiment, is also utilized between cores of the same type. For example, assume cores **505** and **510** are both CPU cores and are executing related threads (e.g. producer and consumer related threads, such as a main thread of a single application executing on core **505** and a run-ahead helper thread for the single application execution on core **510**, where the run-ahead helper thread produces information to be consumed by the main thread). Consequently, power/frequency balancing may be performed to achieve maximum performance between the threads (e.g. if core **510** executing the helper thread is running too far ahead, such as acquiring too many future locks or prefetching too much information, then core **510**'s frequency is decreased, while core **505**'s frequency is increased to consume at a higher rate and catch up with the prefetching of core **510**).

[0044] Continuing the discussion of **Figure 5**, workload module **515** is to determine a workload of core **505**, core **510**, or both. Determining a workload includes any known method for determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of

a processing element. As one example, a workload for core **505** includes an amount time core **505** is active during a period of time. Activity may be determined as when core **505** is in an active performance state versus a sleep or low power state or a number of cycles executing or performing operations.

[0045] As a corollary to the multitude of potential workload measurements, the components to measure such workload may also vary. To further discussion of the potential components for workload measurement, it's assumed below that workload is measured as a number of active cycles over a period of time (i.e. a total number of cycles for measurement). As a first example, a hardware register, counter, and/or accumulator associated with each of cores **505**, **510** track active cycles. And upon expiration of a period of measurement, the number of active cycles is determined for the period. As another example, a microcontroller executes code that causes hardware to track active cycles over a period. Moreover, microcode, privileged-level code, application code, or other code may be executed to similarly cause hardware to track active cycles over the period of measurement.

[0046] In one embodiment, power module **520** is to dynamically balance performance between cores **505**, **510** based on workload determination from workload module **515**. Balancing 'performance' between cores includes modifying any metric or factor that affects core performance and/or power. For example, if separate power delivery is provided for CPU core **505** from GPU core **510**, then the power delivery or limits thereof may be altered to balance performance there between. However, often when CPU core **505** and GPU core **510** are included on the same package, power delivery

is not separate. Therefore, as another example frequency between the individual cores is balanced. In this scenario, power module **520** is to dynamically tune frequency allocation between core **505** and core **510** based on a power limit for an integrated circuit or package including cores **505,510** and one or more workloads as determined by workload module **515**. Note that frequency may not be directly altered in some embodiments, but rather an underlying metric, such as current, is altered to affect the change in frequency.

[0047] As one example, power module **520** is to increase frequency for core **505** and/or decrease frequency for core **510** in response to the dynamically determined workload for core **505** being greater the workload for core **510**. Here, if one core is demonstrating a greater need of performance due to a higher workload, then its frequency is increased. And when an integrated circuit including cores **505** and **510** are up against a power limit, then the core demonstrating less need for performance requirements is decreased in frequency to counterbalance/compensate for the increase in frequency to the other core. In another example, power module **520** is to increase frequency for core **505** and/or decrease frequency for core **510** in response to determining core **505** is a performance bottleneck. In other words, core **505** is limiting overall performance, because core **510** is relying on output from core **505** to continue further execution. But core **505** is operating too slowly. Then, core **505**'s frequency is increased to ensure overall performance is accelerated. Yet again, if a power limit is encountered, then core **510**'s frequency may be similarly decreased to ensure the power limit is enforced. Note that in some embodiment, hysteresis may be utilized to avoid a 'see-saw' effect, where power/performance balance bounces between settings. For example, CPU frequency is

raised quickly (e.g. upon first detection of requiring more performance/frequency), while reduction of frequency from lack of demand is determined over multiple consecutive (or non-consecutive but closely related) periods of measurement.

[0048] In one embodiment, a basic assumption of potential bottlenecks allows the process to be simplified. For example, assume core 505 is a collection of CPU cores and core 510 is a collection of GPU cores. Here, as an exemplary base assumption, it's assumed that when GPU cores 510 are operating at a maximum (i.e. fully occupied), then GPU cores 510 are the performance bottleneck (i.e. GPU is working as fast as it can under the current limits, but it's not completing the work fast enough). As a result of the assumption, if GPU cores 510 are operating over a workload/activity threshold, it's considered to be a bottleneck. So, the frequency of the GPU is increased. And if a power limit is reached, the CPU frequency is capped (or decreased) to ensure the power limit is upheld. However, if workload module 520 determines the GPU 505's frequency is below a threshold (i.e. not working/consume at maximum capacity), then any CPU 505's frequency cap or limit is increased to cause more production, such that GPU cores 510 workload increases accordingly.

[0049] Any hardware, firmware, microcode, software, or combination thereof may perform the balancing, tuning, and/or allocating described above. As one example, the balancing policies are implemented in a Power Control Unit (PCU), which often includes a microcontroller configured to execute collocated power code. Here, the power code, when executed by the microcontroller, loads workload information from workload module 515, determines an appropriate balancing action (e.g. increasing frequency of

cores **510**), and initiates the balancing action (e.g. indicates the frequency increase, enabling hardware/logic to actually increase the frequency). As another example, code and hardware are both utilized for balancing. In one scenario, a graphics driver for GPU cores **510** loads the graphics workload information from workload module **520** (e.g. hardware activity tracking logic). And either the device driver, a privileged level power service routine (e.g. OS service routine), or other code/hardware determines if a balancing action is to be taken at least based on the graphics workload information. Additionally, CPU core **505** workload information may also be taken into account to determine the appropriate balancing action.

[0050] In one embodiment, the balancing decision maker also takes into account a software hint to determine how performance/power is to be balanced among processing elements. For example, GPU cores **510** workload information is determined, as discussed above. And an executing application provides a software hint of whether a future workload (i.e. a portion of the application) is to include a larger or smaller graphics workload in comparison to a previous portion of the application that resulted in the measured workload. Here, if the GPU is close to a threshold (or close to fully occupied) and the applicant hints that a next period is associated with a greater graphics workload, then the power module **520** may determine that GPU frequency is to be increased and CPU frequency is to be capped; even if the previous activity has not reached an activity threshold. As a result, the hint aids in predicting future activity; instead of relying purely on previous, measured workload information. Note that a hint may be provided through an Instruction Set Architecture defining such a hint, an Application Program Interface

(API), or other known structure/method for communicating information from software to hardware.

[0051] Turning to **Figure 6**, another embodiment of a logical representation of modules to balance power among processing devices to achieve maximum overall performance is illustrated. In one embodiment, Graphics Processing Unit (GPU) cores **605** and Central Processing Unit (CPU) cores **610** are on the same die, integrated circuit, package, or other grouping, which may be subject to an overall power or performance limit. For example, a thermal design power (TDP) power limit is often provided for an integrated circuit or package. In other words, a power limit is provided for a maximum thermal dissipation capacity of the integrated circuit. However, in another embodiment, GPU cores **605** and CPU cores **610** are separate integrated circuits to be inserted in a single platform, which may similarly be subject to an overall platform power and/or thermal limit.

[0052] Workload monitor **606** is illustrated as associated with GPU cores **605**, and workload monitor **611** is illustrated as associated with CPU cores **610**. As stated above, workload monitor **606** and **611** may be implemented in hardware associated with GPU cores **605** and CPU cores **610**, workload code to be executed by a micro-controller, and/or code (e.g. micro-code, driver code, other code) executed on GPU Cores **605** and/or CPU cores **610**.

[0053] Device driver **620**, which may be executing on CPU cores **610**, is to read/load workload information from workload monitor **606**. For example, a number of cycles GPU cores **605** are active is held in a register, counter, and/or accumulator in GPU

605. Device driver **620** loads the count every period and determines GPU **605** activity. Here, in one embodiment, device driver **620** makes the balancing decision based on the graphics activity from workload monitor **606**. In one scenario, if the workload activity is greater than a threshold, then driver **620** indicates that GPU cores **605** are occupied (i.e. a fully active and may be a bottleneck). In this embodiment, power management/balancing module **630** (hardware, firmware, code, or a combination thereof) receives the occupied indication and performs the appropriate balancing action (e.g. capping CPU cores **610** frequency and/or increasing GPU core frequency **605**). As specific illustrative examples, power module **630** includes a PCU, power code, microcode, application code, privileged level code, an Operating System (OS) power management service, etc.

[0054] In another embodiment, power management module **630** (e.g. such as a privileged power management service) loads CPU activity information from monitor(s) **611**. And with GPU cores **605** activity information either directly from workload monitor **606** or device driver **620**, power management module **630** makes the balancing decision. And module **630** also either directly implements the balancing decision or indicates that the balancing is to be performed by some other module, unit, or entity.

[0055] As one example, power management module **630**, which in some embodiments encompasses device driver **620**, sets a performance limit for one or more of the CPU cores **610** and/or GPU cores **605**. Here, assume that an overall power or thermal limit for GPU cores **605** and CPU cores **610** has been reached. And during workload measurement, it's determined that GPU cores **605** activity exceeds an occupied threshold. As an illustrative example of a threshold, a number of cycles to consider a GPU occupied

may range from over 50% of cycles in a period active to 100% of cycles in a period active. For example, assume the activity threshold is 95% activity, then if workload monitor 606 detects 96%-100% active cycles, then it's determined the activity threshold is exceeded.

[0056] As a result, a performance limit (e.g. a maximum operating frequency for CPU cores 610, a maximum turbo frequency for CPU cores 610, a maximum current for CPU cores 610, and a maximum energy consumption for CPU cores 610) is set. This action alone may be enough to balance the production of CPU cores 610 to match the consumption rate of GPU 605. However, in another embodiment, a performance metric for GPU cores 605, which may be the same performance metric limited for CPU cores 610 or a different performance metric, is increased. Here, the increase for GPU 605 is intelligently selected to balance with CPU cores 610's increase, such that the power or thermal limit that has already been encountered is not exceeded. Inversely, if the GPU workload is below a threshold and a cap/limit has been placed on CPU cores 610 from a previous period, then that cap is either increased or removed. Essentially, if GPU cores 605 is being under-utilized, it's assumed that CPU 610 is not producing at a fast enough rate to fully utilize GPU 605. Therefore, CPU 610 is increased or allowed to run-to-completion to generate more work for GPU cores 605. Also much like the discussion above, if a power limit is reached, then GPU 605's performance metric, such as frequency, may be reduced, since it doesn't need full performance to complete its workload that was below an activity threshold.

[0057] As can be seen from above, the power consumption that has reached a limit is intelligently redistributed among processing elements to achieve an optimal balance that provides the best overall performance. In contrast, if power wasn't balanced as discussed herein, then the power limit is enforced but one of the processing elements may act as a performance bottleneck that limits overall performance. In contrast, such intelligent redistribution enables bottlenecks to be alleviated, even under power constraints, which enables maximum performance under the most efficient energy consumption constraints.

[0058] Moving to **Figure 7**, an embodiment of modules and/or a representation of a flow diagram for balancing power between a processor and graphics processor to achieve maximum performance within a power limit is depicted. Note that the flows (or modules) are illustrated in a substantially serial fashion. However, both the serial nature of these flows, as well as the depicted order, is not required. Also, flows are illustrated in a substantially linear. However, the flows may be performed in parallel over the same time period. In addition, any of the illustrated flows or logical blocks may be performed within hardware, software, firmware, or a combination thereof. As stated above and below, each flow, in one embodiment, represents a module, portion of a module, or overlap of modules. Moreover, any program code in the form of one or more instructions or operations, when executed, may cause a machine to perform the flows illustrated and described below. For example, in one embodiment, program code includes a device driver, such as a graphics driver; a privileged service routine, a portion of power code for a Power Control Unit, a portion of micro-code for a processor, or a combination thereof.

[0059] In flow **705**, a graphics processor and or central processor workload over a period of time is received (or loaded) from one or more workload monitors. As one example, an activity count is read/loaded from a hardware register in the devices. Yet, any known method of tracking workload or activity over a period of time may be utilized.

[0060] Then in flow **710**, it's determined if a limit, such as a thermal design power (TDP) limit, is reached. Although any power or energy limit may be encountered, often a power limit based on electrical and thermal limits for a package including the GPU and CPU (i.e. TDP limit for the package) is utilized. If the power limit has not been reached and either the CPU or GPU workload indicates an increase in performance is needed (flow **715**), then the power or performance metric, such as frequency, is increased up to a maximum allowable to accommodate the workload in flow **720**. Here, if there is no concern of hitting a power limit, then a potential bottleneck is eliminated through purely providing more performance. In contrast, if no performance increase is needed, as indicated by the workloads from flow **705**, then the flow resets to measure workload and read once again in flow **705** after a subsequent period. Note that in flow **715** it may instead be determined that performance of a device, such as a GPU, may be lowered and the GPU would still be able to accommodate the measured workload. As a result, GPU performance is reduced, which in turn decreases power consumption, while maintaining workload performance.

[0061] However, if a limit has been encountered, then the power and/or performance is balanced to alleviate as much of a bottleneck as possible. Therefore, in flow **725** it's determined if the loaded GPU workload is greater than a workload/activity

threshold. If the GPU workload is above the threshold, then in flow **730** a performance limit is imposed on the CPU. In other words, the GPU is being overworked and the CPU's production is capped. As can be seen, one way to alleviate the GPU's workload is to cap CPU production. However, to further alleviate the bottleneck, GPU performance, such as frequency is increased. Because of the increase in GPU frequency, the GPU power consumption is increased. And without the decrease or capping of CPU frequency, which results in lower CPU power consumption, the encountered TDP limit would be exceeded. However, the balancing of capping CPU performance and the similar increase in GPU frequency ensures the TDP limits are not exceeded. But instead, the available power is intelligently redistributed among the GPU and CPU to obtain the best performance based on actual, measured GPU workload.

[0062] Yet, if the GPU workload is not greater than a threshold, then in flow **735** it is determined if a previous CPU limit has been imposed. If no limit has been imposed, then the CPU continues to operate according to existing policies in flow **745**. However, if the GPU is below an activity threshold and the CPU has a current performance limit, then the limit is increased and/or removed in flow **740**. As discussed above, in this scenario the GPU is not working hard, so the production of the CPU is increased. Consequently, if no CPU cap is in place, the low graphics activity may be due to an application that is not graphics intensive. In contrast, if a CPU performance limit has been imposed, then it is increased to potentially also increase the CPU's production for the GPU.

[0063] Referring to **Figure 8**, another embodiment of modules and/or a representation of a flow diagram for balancing power between a processor and graphics

processor to achieve maximum performance within a power limit is depicted. Similar to **Figure 7** and flow **705**, a processing workload activity for a central processor and a graphics workload activity for a graphics processor is determined. And in flow **810**, as in flow **710**, it's determined if a platform, package, integrated circuit, or other form holding the central processor and graphics processor has reached a power limit, a thermal limit, or combination thereof (e.g. a TDP limit).

[0064] In flow **825**, it's determined if the graphics processor is a performance bottleneck based at least on the graphics workload activity determined in flow **805**. As one example, such a determination is based on whether the graphics workload activity is greater than a graphics activity threshold. Here, if the activity is greater than a threshold it's assumed that the GPU is a bottleneck. However, if the activity is less than the threshold, then it's assumed for flow **825** that the CPU is the bottle neck. However, such comparisons of activity to a threshold are not required. For example, workloads may be directly compared. And if one is higher than the other, it is determined to be the bottleneck.

[0065] Therefore, in flow **830**, a processor performance limit for the central processor is set below a previous processor performance limit in response to determining the graphics processor is the performance bottleneck in flow **825**. Or in flow **840**, a graphics performance limit for the graphics processor is set below a previous graphics processor performance limit in response to determining the central processor is the performance bottleneck in flow **835**. And similar to the discussion above, the competing device may be increased to further alleviate any bottleneck.

[0066] Although the discussion has primarily focused on competing devices being central processors and graphics processors, any devices that have a producer-consumer relationship, contend for power or performance resources, or are regulated under an overall power or thermal limit may similarly have power/performance balanced between them. Therefore, available power is intelligently allocated between devices to provide the best possible performance from an overall perspective, instead of each individual component being charged with its own power and performance regulation without being cognizant of their application level contribution or monopolization of resources.

[0067] Turning next to **Figure 9**, an embodiment of a logical representation of units, modules, and/or software entities to dynamically balance power between multiple units/devices, such as CPU cores, GPU cores, and communication interfaces, is illustrated. The apparatus and methodology of balancing power/performance above has been in regard to a producer consumer relationship (e.g. one device producing for another, such as a CPU and GPU). One specific example of such a relationship also includes a core, such as a CPU and/or GPU, and a communication bus/memory. Here, a core often produces for a communication bus (i.e. a core generates requests that are transmitted by a communication bus). Therefore, just as a CPU, GPU, or other core may be a bottleneck to performance (even under a power limit), so might a communication bus. Therefore, in one embodiment, power (e.g. current, voltage, frequency, or other metric affecting power consumption) is balanced between one or more cores and a communication bus.

[0068] This communication bus scenario is discussed in more detail below, but may be applied in a more broad sense. In fact, in a phone or tablet space, the power balancing methodologies described herein may be utilized between other units. For example, a radio or network interface may be dynamically balanced under a limit with cores or other interconnects. As a specific illustrative example, power of a radio may be reduced to save power if the network is not a bottleneck and the power may be allocated to a core or other interconnect. And inversely, if the radio transceiver is a bottleneck, then a core or other interconnect frequency may be reduced to free up power to be allocated to the radio for obtaining more bandwidth. As can be seen from this example, such dynamic power allocation at a limit may be utilized between any functional units of a device, from a traditional processor to a SOC, phone, embedded, or other device/system.

[0069] Communication bus **950** includes any known bus or interconnect. In one scenario, bus interface **950** is to communicate with devices external to processor **100**, such as system memory, a chipset (often including a memory controller hub to connect to memory and an I/O controller hub to connect peripheral devices), a memory controller hub, a northbridge, or other integrated circuit. And in this scenario, bus **950** may include any known type of interconnect, such as multi-drop bus, a point-to-point interconnect, a serial interconnect, a parallel bus, a coherent (e.g. cache coherent) bus, a layered protocol architecture, a differential bus, and a GTL bus. In another embodiment, communication bus **950** is to communicate with devices integrated on the same package or die as cores **905, 910**, such as a memory controller hub, a graphics processor/device, and/or a cache

memory. In this case, a portion of the processor (an on-core portion) includes one or more controller(s) for interfacing with other devices such as a memory and/or a graphics device. The configuration including an interconnect and controllers for interfacing with such devices is often referred to as an on-core (or un-core configuration).

[0070] As the illustrative example depicts, bus **950** includes a ring interconnect topology to connect GPU cores **910**, CPU cores **905**, and a cache memory **960** (e.g. a last level cache, a level-two cache, a level three cache, or other known cache memory). However, such a ring interconnect may include any other known devices, as well as excluding or replacing illustrated devices (e.g. a memory controller instead of a cache memory **960**). Here, graphics cores **910** may even have direct access to cache **960** through ring interconnect **950**. Yet, in the SOC environment, even more devices, such as the network interface, co-processors, memory, I/O devices, and any other known computer devices/interface may be integrated on a single die or integrated circuit to provide small form factor with high functionality and low power consumption. And as discussed in more detail below, when power policies are developed for the entire IC, the techniques for power balancing between prominent, integrated devices become even more important.

[0071] In one embodiment, power management service **920** is to dynamically balance power, which may be in the form of voltage, current, frequency, clock, or other known processor power changing knob, between cores (e.g. **910** and/or **905**) as well as communication bus **950**. With specific reference to **Figure 9**, GPU cores **910** are associated with a workload monitor **911** to determine GPU workload, while CPU cores

905 are associated with CPU workload monitor **935** to determine CPU workload.

Additionally, communication bus **950** is associated with a workload monitor **951**. As mentioned above, determining a workload includes any known method for determining activity of hardware, a workload of software, a number of instructions executed or to execute, or any other metric for determining use of a processing element. As one example, a workload for cores **905** includes an amount time cores **905** are active during a period of time. Activity may be determined as when cores **905** is in an active performance state versus a sleep or low power state or a number of cycles executing or performing operations. Alternatively, activity may be measured in a number of active cycles (i.e. the number of cycles in a period that CPU cores **905** are fetching, decoding, issuing, executing, and/or retiring instructions). In a similar manner, workload monitor **951** determines activity of communication bus (i.e. number of cycles or number of work slots occupied by activity on bus **950**). For example, if the bus is able to handle a request or work slot per cycle, then activity in this case may be measured by how many work slots are occupied by activity of a period or time frame of total work slots. As a specific example, a counter counts a number of slots or entries that are issued over cycles (i.e. if the queue is empty during any of the cycles or no entry/request is issued during a cycle).

[0072] As a corollary to the multitude of potential workload measurements, the components to measure such workload may also vary. To further discussion of the potential components for workload measurement, it's assumed below that workload is measured as a number of active cycles over a period of time (i.e. a total number of cycles for measurement). As a first example, a hardware register, counter, and/or accumulator

associated tracks active cycles or occupied work slots. And upon expiration of a period of measurement, the number of active cycles is determined for the period. As another example, a microcontroller executes code that causes hardware to track active cycles over a period. Moreover, microcode, privileged-level code, application code, or other code may be executed to similarly cause hardware to track active cycles over the period of measurement.

[0073] Once the workloads are determined, then power is balanced among the selected devices (e.g. cores **910**, cores **905**, and bus **960**) based on those measured workloads. As aforementioned, such a determination of how to balance power may be made by hardware (i.e. logic in the device, such as a power control unit), firmware (i.e. microcode or collocated code to be executed by cores or a control unit with a microcontroller), and/or software (e.g. power management service **920** that is part of operating system **915**, user-level code, device driver code **925**, or other code). The discussion below will primarily focus on power management service routine **920**; however, it's important to note that the discussion similarly applies to application in hardware, firmware, or other software code.

[0074] Here, if communication bus **950** is too busy (i.e. the workload is too high, such as over a threshold), then any executing application slows down based on the communication bottleneck between cores **905**, cores **910**, and cache memory **960**. Therefore, in one embodiment, in response to encountering such a situation, the communication bus frequency/power is increased (i.e. a clock generator **940** for communication bus **950** is accelerated/stepped-up). However, as encountered above, if

integrated circuit **900** is operating at a maximum (e.g. power or thermal limit), then the increase in communication bus frequency **960** is counterbalanced in the CPU and/or GPU.

[0075] In this case, any number of balancing effects may be utilized. For example, both CPU cores **905** and GPU cores **910** may be capped (i.e. decreased limit in power/frequency) to decrease the load on communication bus **950**. However, a more intelligent balancing methodology may be utilized instead. In this scenario, caps may be dynamically and separately altered for each component or unit. As an illustrative example, assume that communication bus **960** is operating at 100% workload (i.e. all work slots in a given time period were occupied as measured by workload monitor **951**), GPU cores **910** are operating at a 97% workload activity, and CPU cores **905** are operating at a 80% workload activity. As can be seen from this example, the biggest bottleneck in the system is the communication bus **950**, as it's fully occupied. But GPU cores **910** also have a high workload activity in comparison to CPU cores **910**. As a result, if IC **900** is up against a power, thermal, or other limit, CPU cores **905** may be capped or limited the most (i.e. frequency and/or power is capped), while power to GPU cores **910** are slightly capped, maintained, or actually increased. And communication bus **950** is allocated even more power. Therefore, a power increase for communication bus **950** (and potentially for GPU cores **910**) is dynamically balanced with a cap of CPU cores **905** (and potentially GPU cores **910**) to alleviate the bottlenecks in the system to increase performance, while not exceeding the current limit for IC **900**.

[0076] As can be seen, any methodology for dynamically allocating power between units/cores may be utilized to stay under a limit and maximize performance. In fact, in some implementations increasing a bus in frequency results in less extra power consumption than the same reduction in frequency for cores **905**. For example, assume a one-step increase in frequency for communication bus **950** results in a 1 watt power increase. But if IC **900** is at a power limit, then CPU cores **905** may be capped. Yet, a one-step decrease in frequency in CPU cores **905** may result in a 2 watt drop in power. As a result, if CPU cores **905** are simply increase one frequency stepping, while bus **950** is decreased by one frequency stepping, then additional power is left under the limit for extra performance. Consequently, in one embodiment, other actions (e.g. a simultaneous increase in frequency for GPU cores **910** or a 2x stepping for bus **950**) may be performed to ensure a limit is not exceeded, but that performance/power is not left on the table.

[0077] Furthermore, in another embodiment, power planes (or clocking domains) of different cores/units may be tied together. As a result, a dynamic power balancing methodology, in some implementations, should take that into account. For example, in some embodiments, clock generators **940** and **904** are shared between CPU cores **904** and communication bus **950**. As a result, a stepping in frequency for communication bus **950** includes a similar stepping for CPU cores **905**. Therefore, a step in the consumer frequency may actually cause one of the producers (CPU cores **905**) to increase production. As a result, the balancing algorithm takes such a tying into account, so GPU cores **909** may be reduced to balance the effect from bus **950** and CPU cores **905** being increased.

[0078] In another embodiment, a lower limit may be provided for one or more of the devices, cores, and/or units. For example, assume a game is executing on IC 900. Here, GPU cores 910 are have a 100% workload, even when processor 904 and communication bus 950 are operating at a very low workload. In fact, CPU cores 905 and communication bus 950 may be reduced dramatically to bare operation to give GPU cores 910 all the possible power/frequency for maximum performance. But if communication bus 950 is reduced too low (i.e. the frequency is very low), then a request made to cache 960 takes a long time to complete due to the low frequency. And GPU cores 910 may start to stall and wait on information to return. Essentially, the GPU is the primary produces, and the most power is allocated there. But when the GPU is to consume from communication bus 950, the bus frequency can't be too low that it slows overall performance. Therefore, in one embodiment, a lower limit is provided for communication bus 950. For example, a frequency level (e.g. between 400Mhz to multiple GHz) is imposed. So in this scenario, communication bus 950 is capped and reduced to provide as much power to the bottleneck (GPU cores 910) as possible until it reaches the low frequency limit. At that point, the balancing algorithm (e.g. power management service 920) doesn't reduce communication bus frequency 950 any further to avoid adversely affecting overall performance. As a result, the advantage of obtaining maximum performance at a high limit for IC 900 is maintained by utilizing a low limit for units or cores in conjunction with the power balancing.

[0079] Referring next to **Figure 10**, an embodiment of a flow diagram for a method of balancing power between cores and a communication bus is illustrated. Note

that the discussion below is often in reference to a power management routine (such as the routine **920** of **Figure 9**) making such decisions; however, similar flows and operating may be performed in hardware, software, firmware, or a combination thereof. Additionally, the flow assumes a primary graphics bottleneck that is evaluated first in flow **1035** before a communication bus workload or CPU workload. Yet, in other embodiment, any workload may be determined first. Moreover, power balancing is not limited to CPU cores, GPU cores, or communication interfaces, but rather it may be extended to other interfaces, units, or logic.

[0080] In flows **1005**, **1010**, and **1015** workloads of elements of interest are determined. For example, workload monitor **911** determines a GPU workload and provides it to device driver **925** that provides it to power management service **920** in OS **915**, workload monitor **935** provides a CPU workload to service **920**, and workload monitor **951** provides interconnect workload to service **920**. Note that such providing may done by reading from the workload monitors in flow **1020** (e.g. device driver **925** loads the GPU workload from monitor **911**, while service **920** loads from CPU monitor **935** and bus monitor **951**).

[0081] In flow **1025**, the power service routine **920** (or other hardware, firmware, software, or combination in other embodiments) determines if IC **900** is operating within limits. For example, IC **900** may have a TDP limit. And a PCU determines if IC **900** has reached a thermal, power, or other limit. If IC **900** is not operating at or above a limit, then existing methodologies, such as race to finish methodologies (i.e. increase power to

one or more elements to improve performance) are utilized. However, if IC **900** is at a limit, then the power/frequency is balanced at that limit between the elements.

[0082] As an illustrative example of a potential algorithm, the power service routine **920** determines if the GPU is fully occupied. For example, service **920** compares the workload from monitor **911** to a threshold. And if the workload exceeds the threshold, then service **920** determines GPU cores **910** are fully occupied. Note that in one embodiment, such threshold may be 99% or 100%. In this scenario, GPU cores **910** are considered fully occupied if they are 100% active. However, any threshold level may be utilized. If not above the threshold (i.e. not fully occupied, then routine **920** determines if there is a cap of frequency for CPU cores **905** (i.e. a cap previously imposed by service **920**) in flow **1055**. If not, then previous methodologies are utilized in flow **1030**. However, if there is a CPU cap, then the Cap is increased by one step in flow **1060**, since the GPU is not fully occupied (i.e. the consumer in this scenario is not full, so we are able to increase the producer).

[0083] Yet, if the GPU is fully occupied in flow **1035**, then in flow **1040** service **920** determines if there is sufficient room on the communication bus to accommodate the current workload **1040**. Similar to above, this flow may include a threshold comparison. As an example, if communication bus is above a workload threshold, then it is considered fully occupied (i.e. there is not sufficient room). Here, there is not enough available work slots, then the communication bus frequency cap is increased by a step in flow **1045** to accommodate more work by potentially increasing GPU frequency due to it being fully occupied, as determined in flow **1035**. Or if it's below the threshold, then it has room

(i.e. available work slots) for more work, so the communication bus and/or CPU frequency may be capped in flow **1050** to balance the potential increase of GPU frequency from determining it's fully occupied in flow **1035**. Note that discussion of increasing a GPU frequency is included. However, in some embodiments, a GPU is already at a maximum frequency. So capping of bus frequency and CPU frequency is to free up (save) power, when the GPU is the bottleneck. In other words, the CPU and communication bus don't have to operate so fast when they are waiting on the GPU anyways. Here, that allocated power may be saved to increase energy efficiency or to be utilized during later timeframes when power is increased above a limit. Or in other embodiments, the GPU may not be at a maximum frequency and that freed power from the communication bus and/or CPU may be allocated to the GPU to increase performance.

[0084] Although **Figure 10** only illustrates a simplified embodiment of a power balancing algorithm, it may be utilized to understand how any number variations may be used to perform similar balancing, as mentioned above. Moreover, the flow of **Figure 10** was discussed in reference to the logical block diagram of **Figure 9**. Therefore, many of the flows were discussed as being performed by an Operating System service routine **920**. But these flows, as well as others not depicted, may be performed in hardware, firmware, software, or a combination thereof. For example, a power control unit including a microcontroller and power code may be utilized to perform one or more of the flows. Or specific hardware may be included, such as a small asymmetric core or device tasked with profiling and power balancing type duties. In addition, device microcode may

include similar routines. Or light weight profiling software (at a privileged or user level) may be utilized to track these workload and make such balancing decisions.

[0085] A module as used herein refers to any combination of hardware, software, and/or firmware. As an example, a module includes hardware, such as a micro-controller, associated with a non-transitory medium to store code adapted to be executed by the micro-controller. Therefore, reference to a module, in one embodiment, refers to the hardware, which is specifically configured to recognize and/or execute the code to be held on a non-transitory medium. Furthermore, in another embodiment, use of a module refers to the non-transitory medium including the code, which is specifically adapted to be executed by the microcontroller to perform predetermined operations. And as can be inferred, in yet another embodiment, the term module (in this example) may refer to the combination of the microcontroller and the non-transitory medium. Often module boundaries that are illustrated as separate commonly vary and potentially overlap. For example, a first and a second module may share hardware, software, firmware, or a combination thereof, while potentially retaining some independent hardware, software, or firmware. In one embodiment, use of the term logic includes hardware, such as transistors, registers, or other hardware, such as programmable logic devices.

[0086] A value, as used herein, includes any known representation of a number, a state, a logical state, or a binary logical state. Often, the use of logic levels, logic values, or logical values is also referred to as 1's and 0's, which simply represents binary logic states. For example, a 1 refers to a high logic level and 0 refers to a low logic level. In one embodiment, a storage cell, such as a transistor or flash cell, may be capable of

holding a single logical value or multiple logical values. However, other representations of values in computer systems have been used. For example the decimal number ten may also be represented as a binary value of 1010 and a hexadecimal letter A. Therefore, a value includes any representation of information capable of being held in a computer system.

[0087] Moreover, states may be represented by values or portions of values. As an example, a first value, such as a logical one, may represent a default or initial state, while a second value, such as a logical zero, may represent a non-default state. In addition, the terms reset and set, in one embodiment, refer to a default and an updated value or state, respectively. For example, a default value potentially includes a high logical value, i.e. reset, while an updated value potentially includes a low logical value, i.e. set. Note that any combination of values may be utilized to represent any number of states.

[0088] The embodiments of methods, hardware, software, firmware or code set forth above may be implemented via instructions or code stored on a machine-accessible, machine readable, computer accessible, or computer readable medium which are executable by a processing element. A non-transitory machine-accessible/readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine, such as a computer or electronic system. For example, a non-transitory machine-accessible medium includes random-access memory (RAM), such as static RAM (SRAM) or dynamic RAM (DRAM); ROM; magnetic or optical storage medium; flash memory devices; electrical storage devices; optical storage

devices; acoustical storage devices; other form of storage devices for holding information received from transitory (propagated) signals (e.g., carrier waves, infrared signals, digital signals); etc, which are to be distinguished from the non-transitory mediums that may receive information there from.

[0089] Reference throughout this specification to “one embodiment” or “an embodiment” means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment of the present invention. Thus, the appearances of the phrases “in one embodiment” or “in an embodiment” in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0090] In the foregoing specification, a detailed description has been given with reference to specific exemplary embodiments. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative sense rather than a restrictive sense. Furthermore, the foregoing use of embodiment and other exemplarily language does not necessarily refer to the same embodiment or the same example, but may refer to different and distinct embodiments, as well as potentially the same embodiment.

CLAIMS

What is claimed is:

- 1 1. An apparatus for efficient energy consumption comprising: an integrated circuit
2 including,
3 a first core;
4 a communication bus coupled to the first core;
5 a core workload monitor configured to determine a core workload for the first
6 core;
7 a bus workload monitor configured to determine a bus workload for the
8 communication bus; and
9 balancing control adapted to dynamically tune power allocation between the first
10 core and the communication bus based on a power limit for the integrated
11 circuit and at least the bus workload.

- 1 2. The apparatus of claim 1, further comprising a second core and a second core
2 workload monitor configured to determine a second core workload for the second
3 core, wherein the first core includes a host processing core, the second core
4 includes a graphics processing core, and the communication bus includes a ring
5 interconnect, and wherein the balancing control is further adapted to dynamically
6 tune power allocation between the first core, the second core, and the
7 communication bus based on a power limit for the integrated circuit and at least
8 the bus workload, the core workload, and the second core workload.

- 1 3. The apparatus of claim 1, wherein a core workload monitor configured to
2 determine the core workload for the first core includes first hardware to track a
3 first number of cycles the first core is active during a period of time.
- 1 4. The apparatus of claim 1, wherein the balancing control adapted to dynamically
2 tune power allocation between the first core and the communication bus based on
3 a power limit for the integrated circuit and at least the bus workload comprises the
4 balancing control, in response to the integrated circuit operating at the power
5 limit, being adapted to:
6 increase frequency for communication bus and cap frequency for the first core in
7 response to the bus workload being greater than a bus workload threshold
8 and
9 decrease frequency for the communication bus and increase the cap frequency for
10 the first core in response to the bus workload being less than the bus
11 workload threshold.

1 5. The apparatus of claim 1, the balancing control is further adapted to implement a
2 low frequency limit for the communication bus.

1 6. A non-transitory medium including code, when executed, to cause a machine to
2 perform the energy efficiency operations of:
3 receiving a bus workload for a communication bus and a first processing element
4 workload for a first processing element
5 based on an integrated circuit including the communication bus and the first
6 processing element reaching a limit;
7 determining if the first processing element workload indicates the first
8 processing element is a performance bottleneck;
9 determining if a communication bus is able to accommodate the bus
10 workload;
11 capping a bus frequency of at least the communication bus in response to
12 determining the first processing element workload indicates the
13 first processing element is a performance bottle neck and
14 determining the communication bus is able to accommodate the
15 bus workload; and
16 increasing a previous cap on bus frequency of at least the communication
17 bus in response to determining the first processing element
18 workload indicates the first processing element is a performance

19 bottle neck and determining the communication bus is not able to
20 accommodate the bus workload.

- 1 7. The non-transitory medium of claim 6, wherein the first processing element
2 includes one or more graphics cores, the communication bus includes a ring
3 interconnect, and wherein the code includes privileged level power service code.
- 1 8. The non-transitory medium of claim 7, wherein the code, when executed, further
2 causes the machine to perform the operations of:
3 increasing a previous cap on frequency for one or more processor core in response
4 to determining the one or more graphics cores is not a performance
5 bottleneck;
6 capping frequency for the one or more processor cores in response to determining
7 the first processing element workload indicates the first processing
8 element is a performance bottle neck and determining the communication
9 bus is able to accommodate the bus workload.
- 1 9. The non-transitory medium of claim 6, wherein the limit includes a thermal
2 design power limit.

1 10. A method for efficient energy consumption comprising:
2 determining a processing workload activity for a central processor on a package;
3 determining a graphics workload activity for a graphics processor on the package;
4 determining a bus workload activity for a communication bus on the package;
5 determining if the package has reached a thermal or power limit; and
6 in response to determining the package has reached the thermal or power limit,
7 dynamically balancing power between the central processor, the graphics
8 processor, and the communication bus based on at least the graphics
9 workload activity and the bus workload activity.

1 11. The method of claim 10, wherein dynamically balancing power between the
2 central processor, the graphics processor, and the communication bus based on at
3 least the graphics workload activity and the bus workload activity comprises:
4 determining if the graphics workload activity is greater than a graphics activity
5 threshold;
6 determining if there is sufficient room on the communication bus based on the bus
7 workload activity in response to determining the graphics workload
8 activity is greater than a threshold; and
9 increasing a maximum allowed frequency for the communication bus in response
10 to determining there is not sufficient room on the communication bus; and

11 decreasing a maximum allowed frequency for the communication bus in response
12 to determining there is sufficient room on the communication bus.

1 12. The method of claim 10, wherein the method is performed in response to
2 execution of privileged level power service code.

1 13. The method of claim 11, wherein the method is performed in response to
2 execution of privileged level power service code.

ABSTRACT

[0091] An apparatus, method and system is described herein for efficiently balancing performance and power between processing elements based on measured workloads. If a workload of a processing element indicates that it is a bottleneck, then its performance may be increased. However, if a platform or integrated circuit including the processing element is already operating at a power or thermal limit, the increase in performance is counterbalanced by a reduction or cap in another processing elements performance to maintain compliance with the power or thermal limit. As a result, bottlenecks are identified and alleviated by balancing power allocation, even when multiple processing elements are operating at a power or thermal limit.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Travis	T.	Schuessler		
Residence Information (Select One)		☒ US Residency ☐ Non US Residency ☐ Active US Military Service			
City	Hillsboro	State/Province	OR	Country of Residence i	US
Citizenship under 37 CFR 1.41(b) i		US			
Mailing Address of Applicant:					
Address 1	1242 SE 63rd Ln				
Address 2					
City	Hillsboro	State/Province	OR		
Postal Code	97123	Country i	US		
Applicant 2					Remove
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Russell	J.	Fenger		
Residence Information (Select One)		☒ US Residency ☐ Non US Residency ☐ Active US Military Service			
City	Beaverton	State/Province	OR	Country of Residence i	US
Citizenship under 37 CFR 1.41(b) i		US			
Mailing Address of Applicant:					
Address 1	8697 SW 168th Avenue				
Address 2					
City	Beaverton	State/Province	OR		
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All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					Add

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For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X	
		Application Number		
Title of Invention	A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus			
Customer Number	59796			
Email Address	david.p.mcabee@intel.com	Add Email	Remove Email	
Email Address	docketing@cpaglobal.com	Add Email	Remove Email	

Application Information:

Title of the Invention	A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		
Attorney Docket Number	P38525X	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	1

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Customer Number	59796		

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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13/327670	2011-12-15
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
			Remove
Application Number	Country ⁱ	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☒ No
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Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.				
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If the Assignee is an Organization check here. ☐				
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Mailing Address Information:				
Address 1				
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Email Address				
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Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/David P. McAbee/Reg. No. 58104			Date (YYYY-MM-DD)	2012-02-16
First Name	David P.	Last Name	McAbee	Registration Number	58104

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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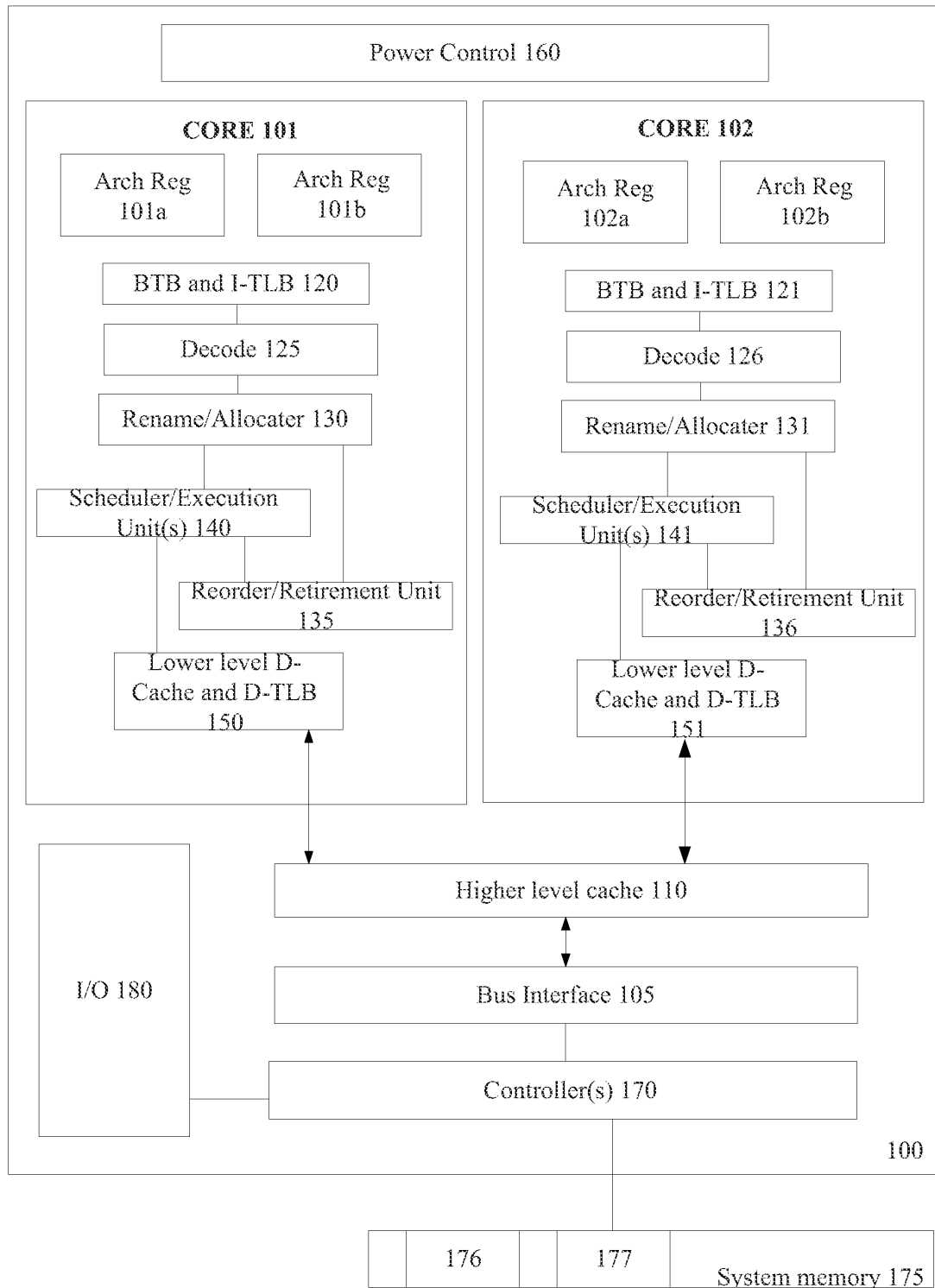


FIG. 1

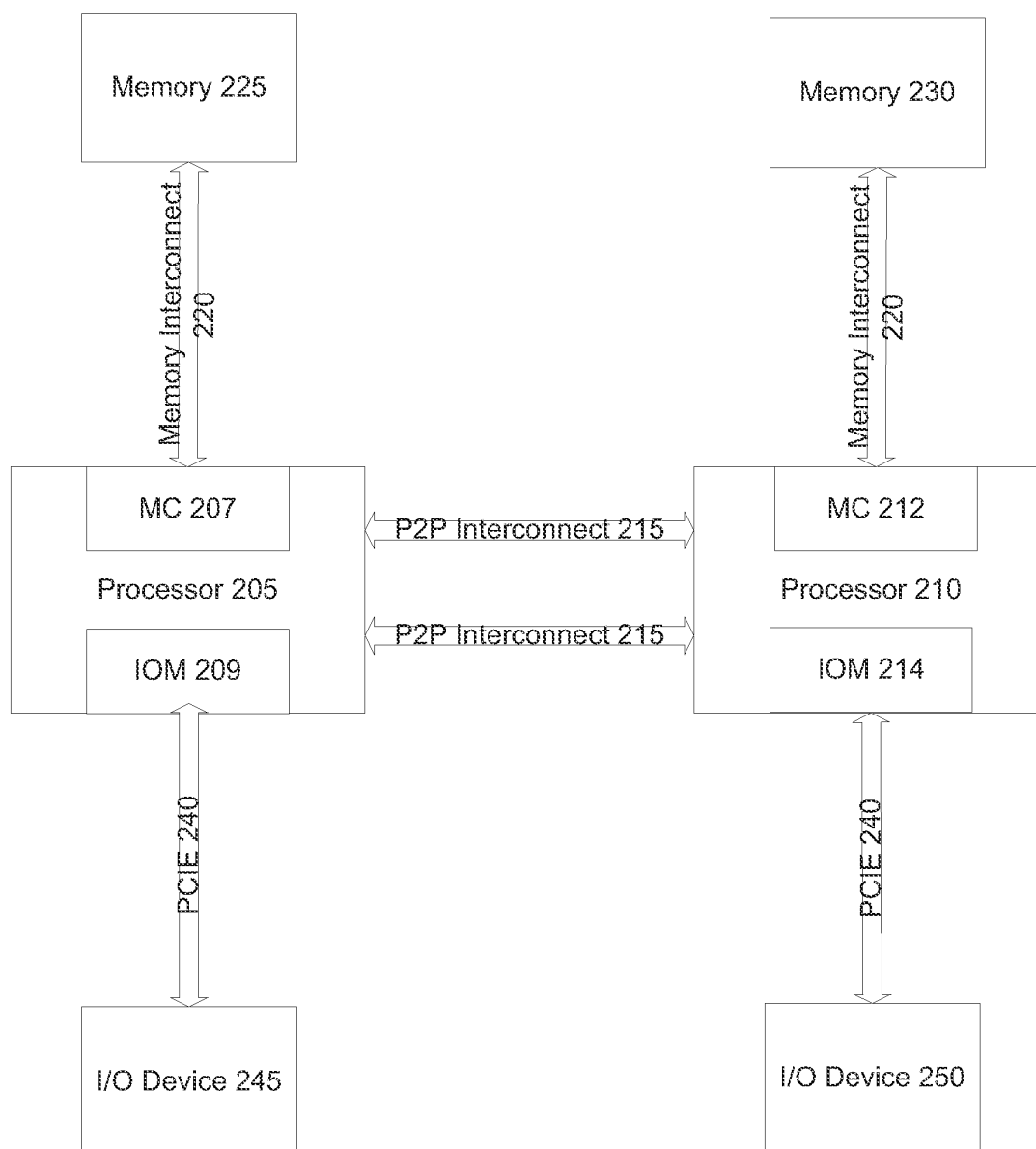


FIG. 2

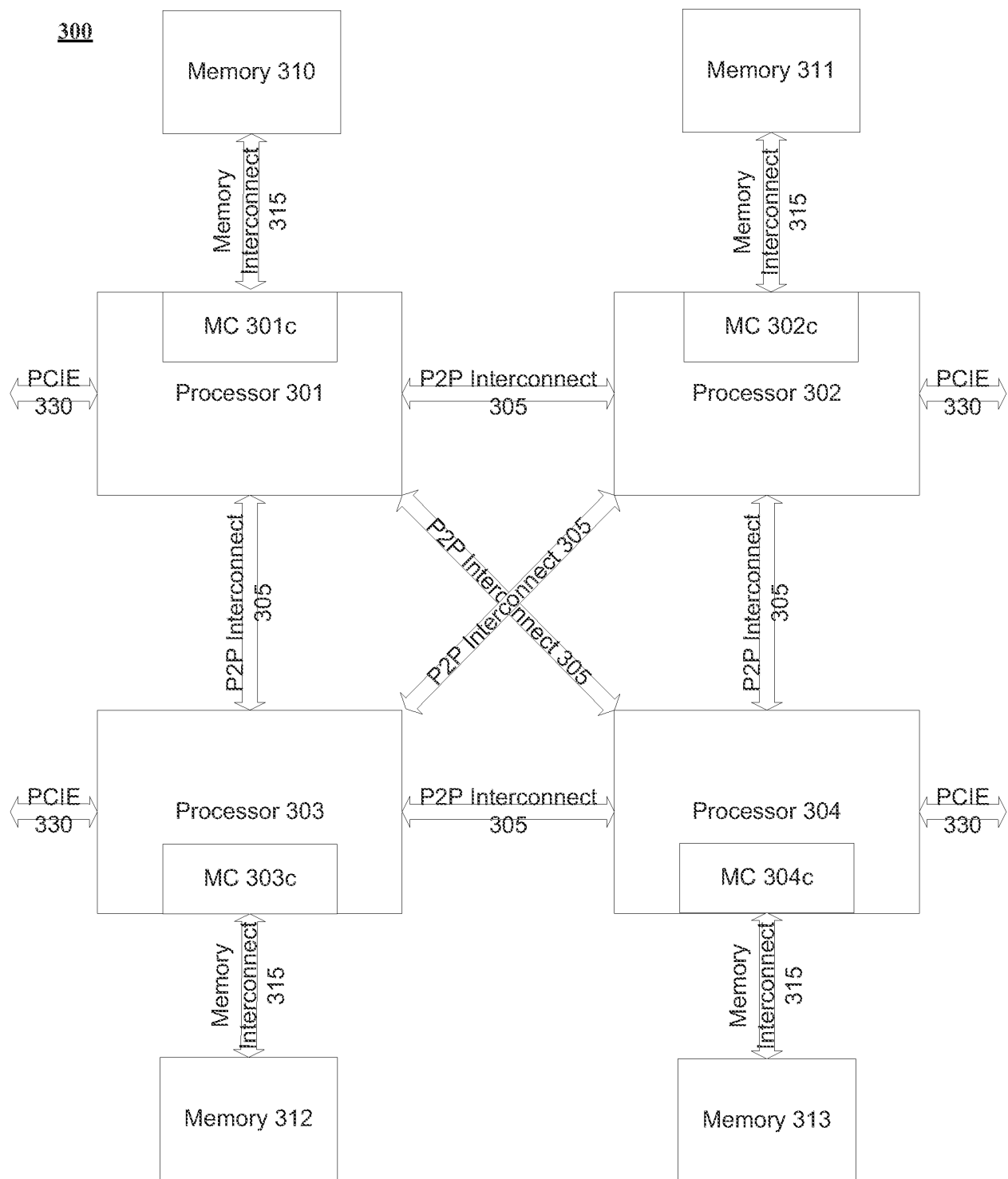


FIG. 3

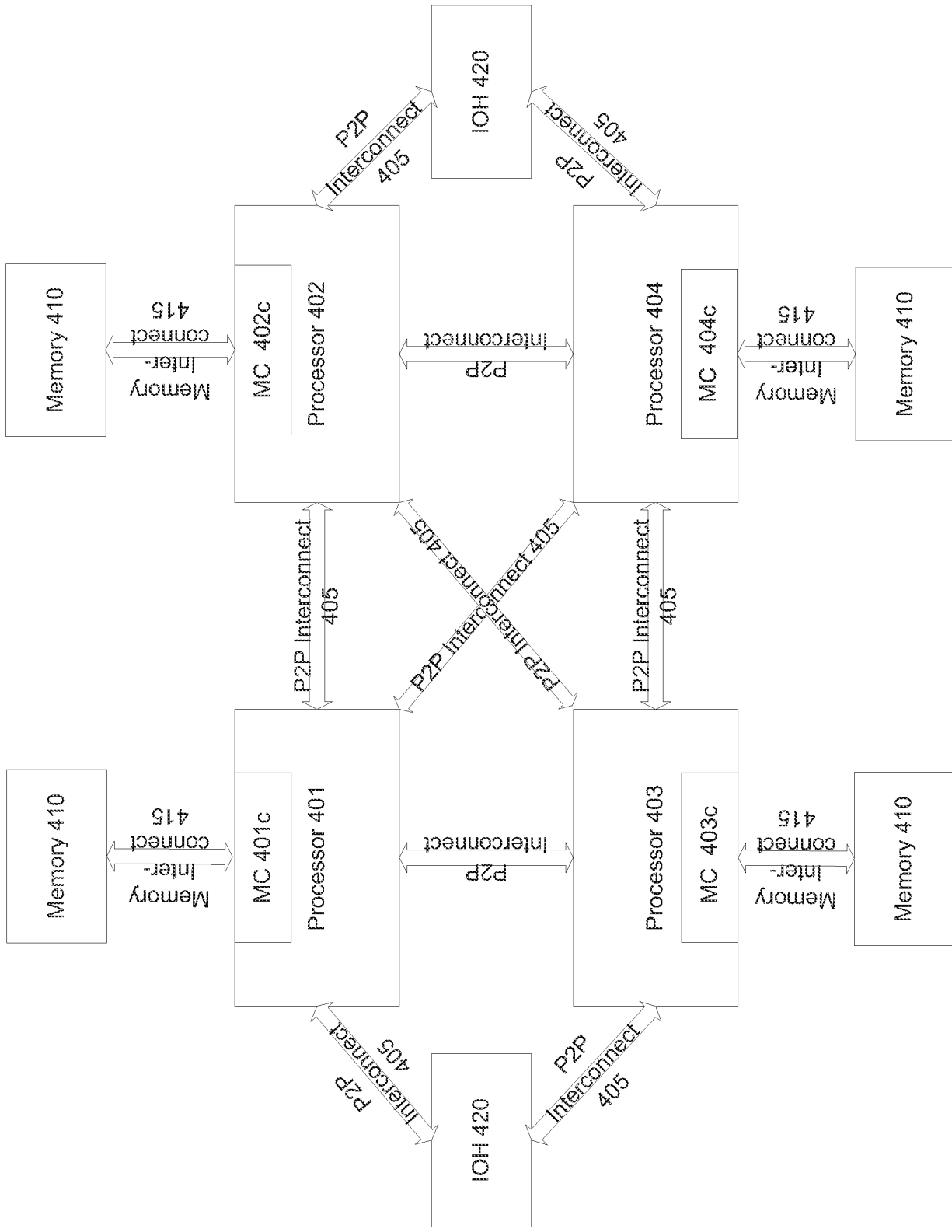


FIG. 4

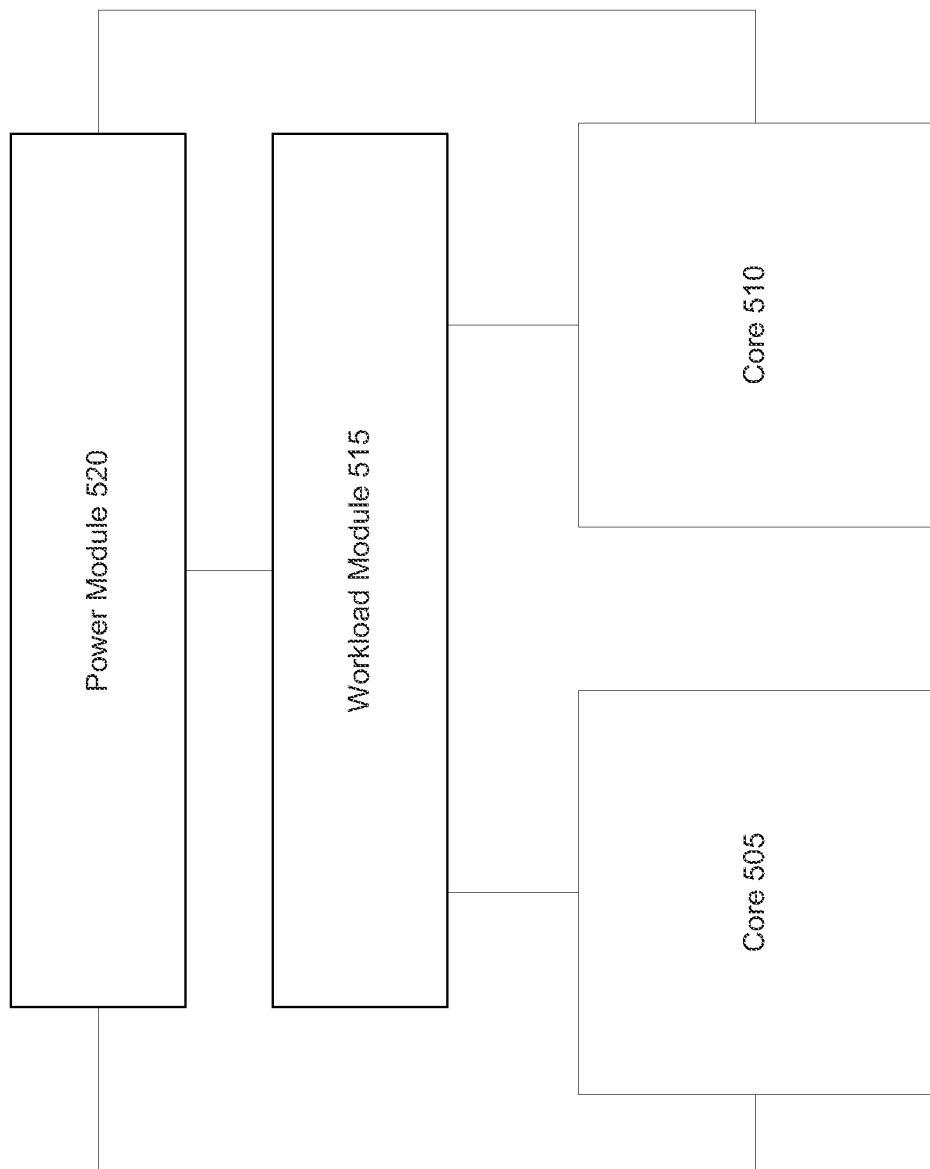


FIG. 5

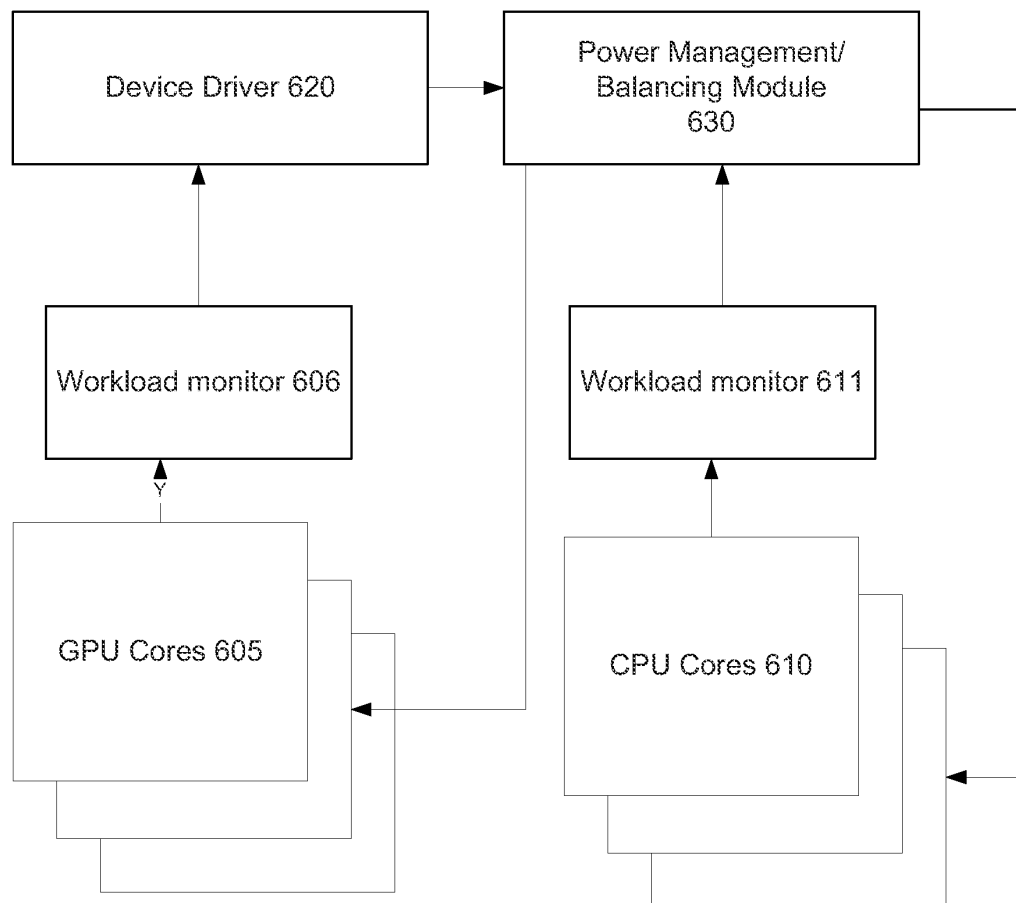


FIG. 6

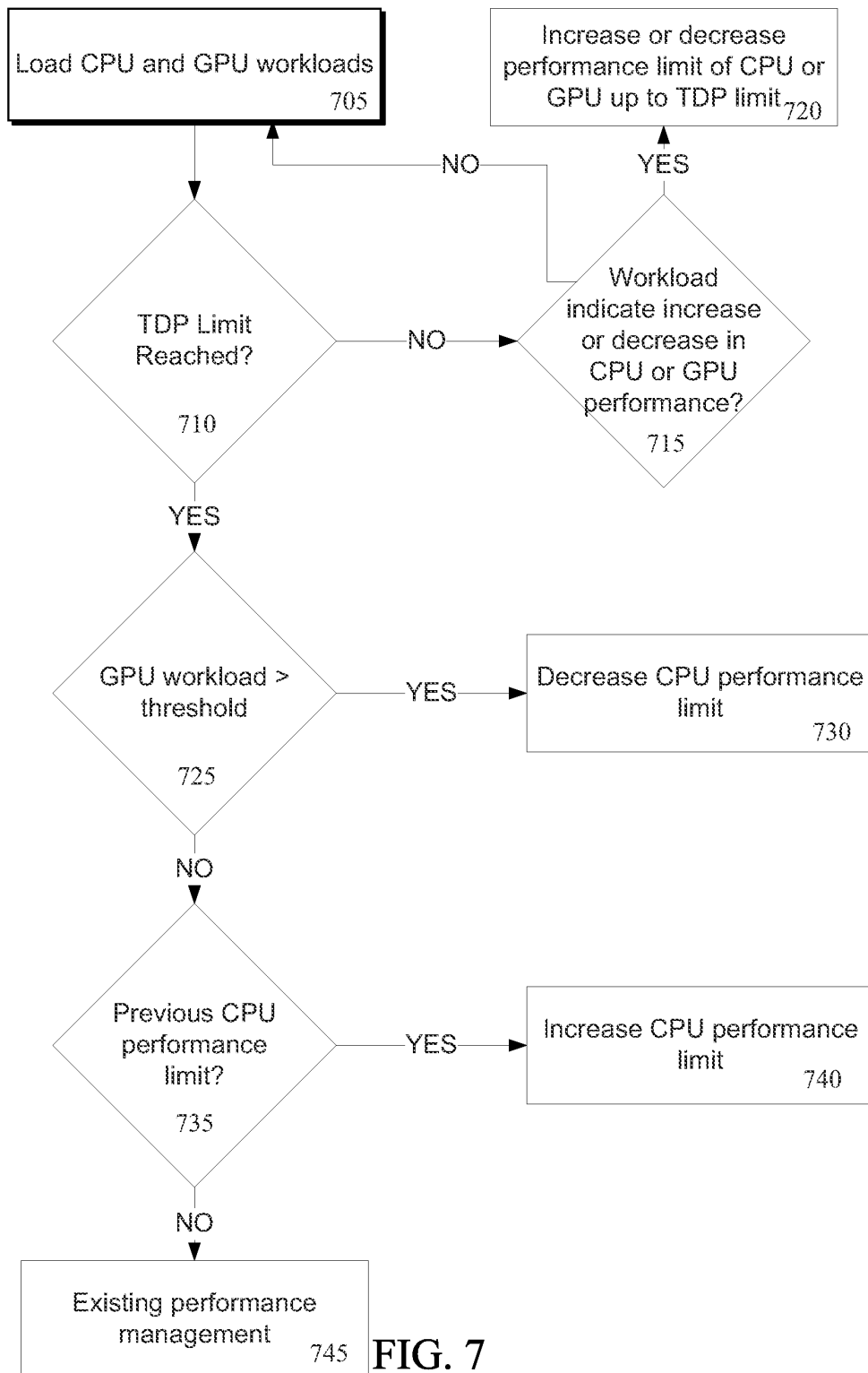


FIG. 7

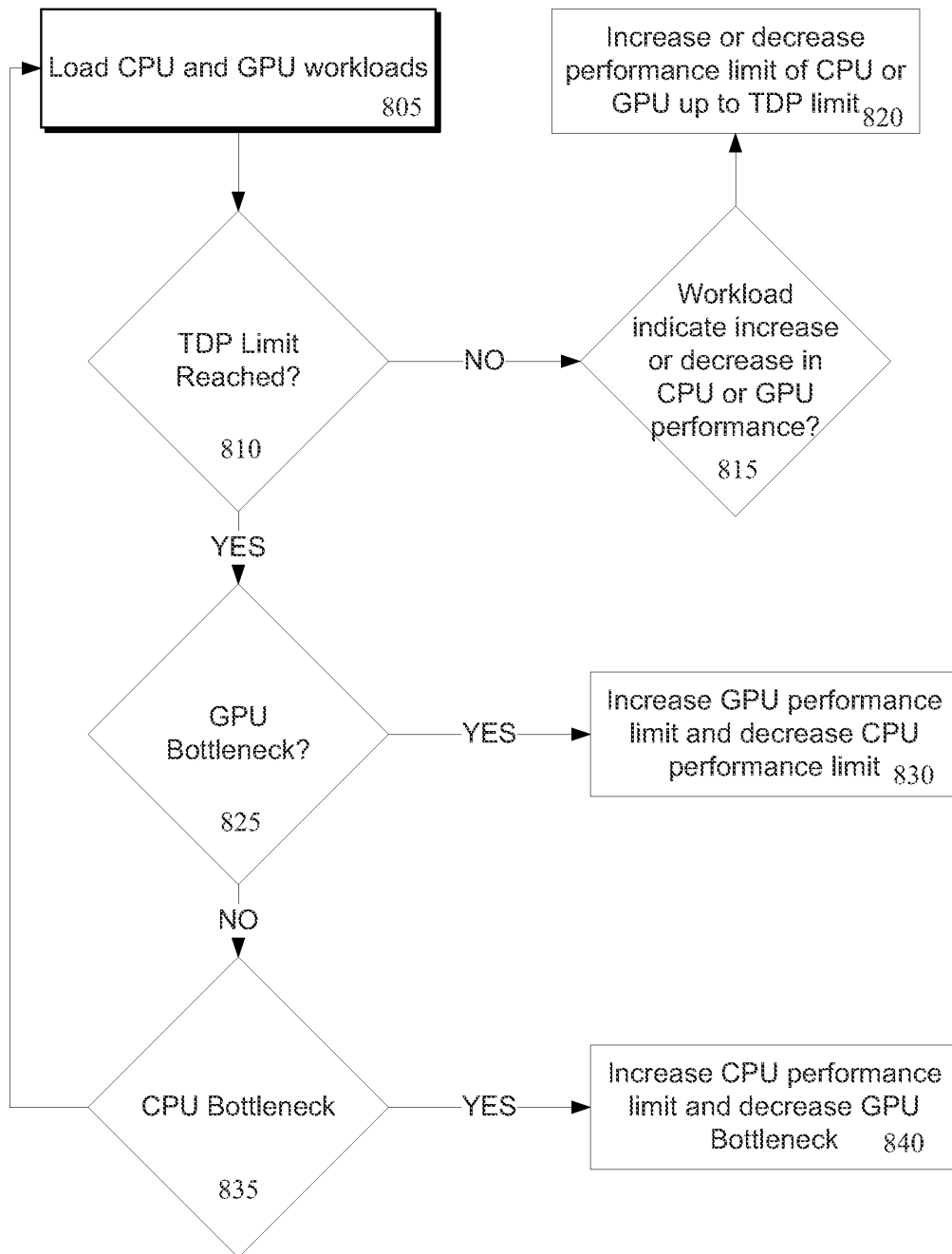


FIG. 8

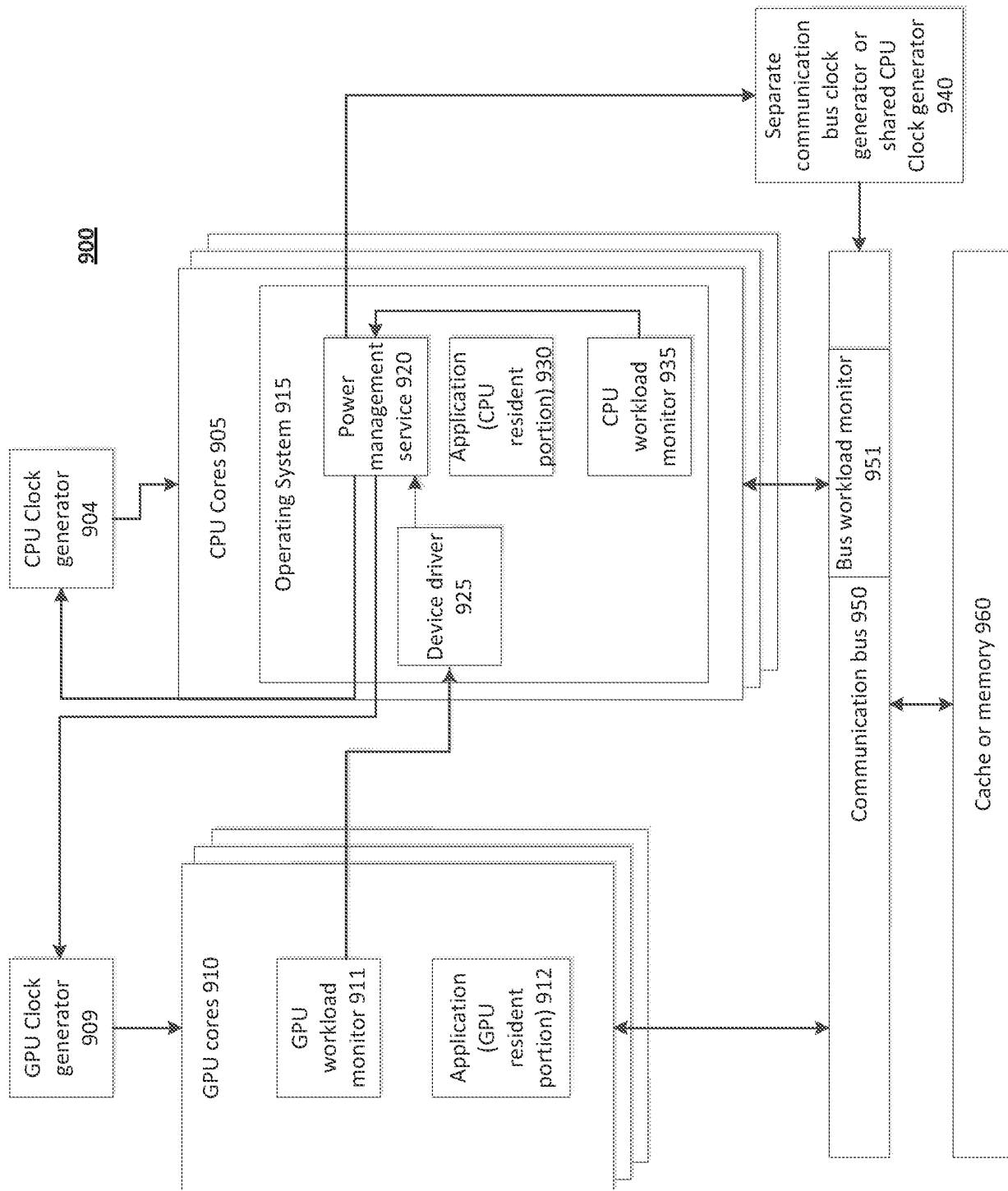


FIG. 9

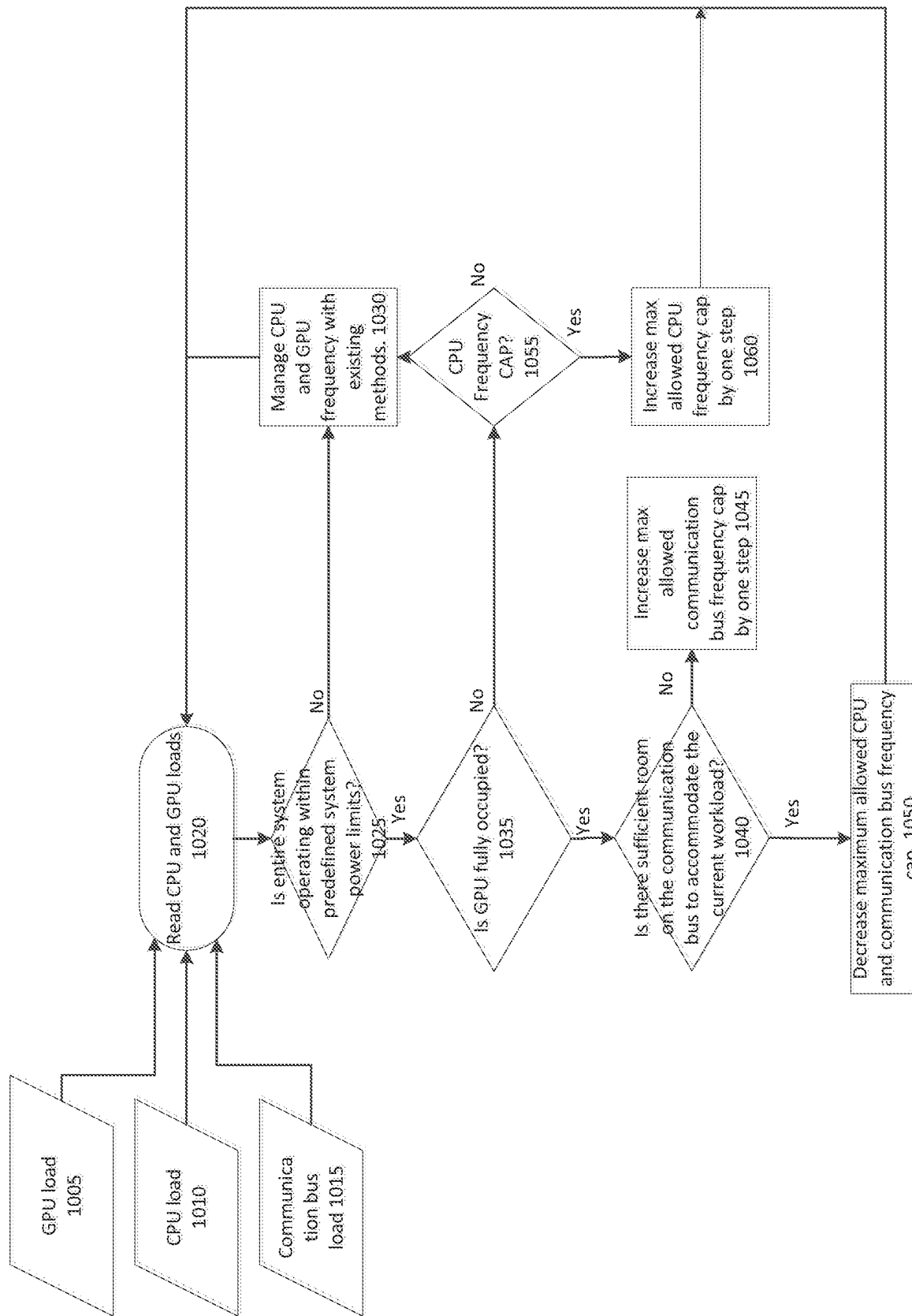


FIG. 10

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		
First Named Inventor/Applicant Name:		Travis T. Schluessler		
Filer:		David P. McAbee/Rachel Guidarelli		
Attorney Docket Number:				
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1250

Electronic Acknowledgement Receipt	
EFS ID:	12097862
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	59796
Filer:	David P. McAbee/Rachel Guidarelli
Filer Authorized By:	David P. McAbee
Attorney Docket Number:	
Receipt Date:	16-FEB-2012
Filing Date:	
Time Stamp:	18:24:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1250
RAM confirmation Number	5705
Deposit Account	500221
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1		P38525X_Application.pdf	244599	yes	53
			a706d4d5ba1a43c87ffb5b5d12a1b41294a663d		
	Multipart Description/PDF files in .zip description				
	Document Description	Start	End		
	Specification	1	44		
	Claims	45	51		
	Abstract	52	53		
Warnings:					
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2	Application Data Sheet	P38525X_ADS.pdf	1905971	no	5
			1a06b09cae9c135e8f7a6437a0d724b5c27b8944		
Warnings:					
Information:					
3	Drawings-only black and white line drawings	P38525X_figs.pdf	155759	no	10
			eb3c621f937cea49166639b9cb6dbba3c5645012		
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Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32962	no	2
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Warnings:					
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/398,641	02/16/2012	2816	1250	P38525X	13	3

CONFIRMATION NO. 1050

59796
INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

FILING RECEIPT



OC000000052867695

Date Mailed: 03/05/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Travis T. Schluessler, Hillsboro, OR;
Russell J. Fenger, Beaverton, OR;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/327,670 12/15/2011

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/398,641**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus

Preliminary Class

327

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where

the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/398,641				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250			
TOTAL CLAIMS (37 CFR 1.16(i))	13	minus 20 = *			OR	x 60 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *			OR	x 250 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/398,641	02/16/2012	Travis T. Schluessler	P38525X

CONFIRMATION NO. 1050

FORMALITIES LETTER



59796
INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

Date Mailed: 03/05/2012

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.

A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.

Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of **\$130** for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is **\$130** for a non-small entity

- **\$130** Surcharge.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.

<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/ldvan/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

S/N 13/398,641

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Travis T. Schluessler et al. Examiner: Unknown
Serial No.: 13/398,641 Group Art Unit: 2816
Filed: February 16, 2012 Docket: P38525X
Confirmation No.: 1050
Title: METHOD, APPARATUS, AND SYSTEM FOR ENERGY EFFICIENCY AND
ENERGY CONSERVATION INCLUDING POWER AND PERFORMANCE
BALANCING BETWEEN MULTIPLE PROCESSING ELEMENTS AND/OR A
COMMUNICATION BUS

COMMUNICATION RE: NOTICE TO FILE MISSING PARTS

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In response to the "Notice to File Missing Parts", enclosed is a copy of the Combined Declaration and Power of Attorney in compliance with 37 CFR 1.63, for the above-identified application. Applicant includes authorization to charge Deposit Account 50-0221 in the amount of \$130.00 as Fee for Surcharge.

Applicant assumes the application is now in proper order and in condition for examination. Please direct any inquiries to the undersigned attorney at 503-712-4988.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-0221.

Respectfully submitted,

Customer Number: 59796

Date: May 4, 2012

By: /David P. McAbee/
Attorney: David P. McAbee
Reg. No. 58,104

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe I am the original and first inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**METHOD, APPARATUS, AND SYSTEM FOR ENERGY EFFICIENCY AND ENERGY
CONSERVATION INCLUDING POWER AND PERFORMANCE BALANCING BETWEEN
MULTIPLE PROCESSING ELEMENTS AND/OR A COMMUNICATION BUS**

the specification of which (check one):

☒ is attached hereto.
☐ was filed on February 16, 2012 as
United States Application Number 13/398,641
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby authorize and request my attorney, associated with Customer Number 59796, to insert on the designated lines above, the filing date, application number, PCT International Application Number and amendment date, as applicable, of the patent application should this Declaration be filed after filing the specification.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Continuation-in-part of U.S. Patent Application No. 13/327,670, filed on December 15, 2011.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)	Priority Claimed?	Certified Copy Attached?
.....		

Docket No.: P38525X
PATENT

(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No
.....			Yes	No	Yes	No
.....			Yes	No	Yes	No

I hereby appoint practitioners associated with the Customer Number: **59796**
as my/our attorney(s) or agents(s), with full power of substitution and revocation, to prosecute this application and to
transact all business in the United States Patent and Trademark Office connected therewith.

Please direct all correspondence to the address associated with the Customer Number: **59796**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made
on information and belief are believed to be true; and further that these statements were made with the
knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both,
under Section 1001 of Title 18 of the United States Code and that such willful false statements may
jeopardize the validity of the application or any patent issued thereon.

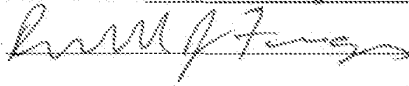
Full Name of First Inventor Travis T. Schluessler

Inventor's Signature _____ Date _____

Residence Hillsboro, OR Citizenship US
(City, State) (Country)

Post Office Address 1242 SE 63rd Ln
Hillsboro, OR, US 97123

Full Name of Second/Joint Inventor Russell J. Fenger

Inventor's Signature  Date 5/2/2012

Residence Beaverton, OR Citizenship US
(City, State) (Country)

Post Office Address 8607 SW 168th Avenue
Beaverton, OR, US 97007

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
 - (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.
- (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and
- (1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
 - (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

- (c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:
- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.
- (e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address, and citizenship are as stated below, next to my name.

I believe I am the original and first inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**METHOD, APPARATUS, AND SYSTEM FOR ENERGY EFFICIENCY AND ENERGY
CONSERVATION INCLUDING POWER AND PERFORMANCE BALANCING BETWEEN
MULTIPLE PROCESSING ELEMENTS AND/OR A COMMUNICATION BUS**

the specification of which (check one):

is attached hereto.
X was filed on February 16, 2012 as
United States Application Number 13/398,641
or PCT International Application Number _____
and was amended on _____
(if applicable)

I hereby authorize and request my attorney, associated with Customer Number 59796, to insert on the designated lines above, the filing date, application number, PCT International Application Number and amendment date, as applicable, of the patent application should this Declaration be filed after filing the specification.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Continuation-in-part of U.S. Patent Application No. 13/327,670, filed on December 15, 2011.

I acknowledge the duty to disclose all information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or (f), or 365(b) of any foreign application(s) for patent, inventor's or plant breeder's rights certificate(s), or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent, inventor's or plant breeder's rights certificate(s), or any PCT international application having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)	Priority Claimed?	Certified Copy Attached?
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Docket No.: P38525X
PATENT

(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No
(Number)	(Country)	(Foreign Filing Date - MM/DD/YYYY)	Yes	No	Yes	No

I hereby appoint practitioners associated with the Customer Number: 59796
as my/our attorney(s) or agents(s), with full power of substitution and revocation, to prosecute this application and to
transact all business in the United States Patent and Trademark Office connected therewith.

Please direct all correspondence to the address associated with the Customer Number: 59796

I hereby declare that all statements made herein of my own knowledge are true and that all statements made
on information and belief are believed to be true; and further that these statements were made with the
knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both,
under Section 1001 of Title 18 of the United States Code and that such willful false statements may
jeopardize the validity of the application or any patent issued thereon.

Full Name of First Inventor Travis T. Schluessler
Inventor's Signature Travis T. Schluessler Date 4/10/12
Residence Hillsboro, OR Berthoud, CO Citizenship US
(City, State) 333 (Country)
Post Office Address 7242 SE 63rd Ln 3719 Coyote Trail JTS
Hillsboro, OR, US 97123 Berthoud, CO 80513

Full Name of Second/Joint Inventor Russell J. Fenger
Inventor's Signature _____ Date _____
Residence Beaverton, OR _____ Citizenship US
(City, State) _____ (Country)
Post Office Address 8697 SW 168th Avenue
Beaverton, OR, US 97007

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

- (1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
 - (2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.
- (b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and
- (1) It establishes, by itself or in combination with other information, a *prima facie* case of unpatentability of a claim; or
 - (2) It refutes, or is inconsistent with, a position the applicant takes in:
 - (i) Opposing an argument of unpatentability relied on by the Office, or
 - (ii) Asserting an argument of patentability.

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- (c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:
- (1) Each inventor named in the application;
 - (2) Each attorney or agent who prepares or prosecutes the application; and
 - (3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.
- (d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.
- (e) In any continuation-in-part application, the duty under this section includes the duty to disclose to the Office all information known to the person to be material to patentability, as defined in paragraph (b) of this section, which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

Electronic Patent Application Fee Transmittal				
Application Number:	13398641			
Filing Date:	16-Feb-2012			
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus			
First Named Inventor/Applicant Name:	Travis T. Schluessler			
Filer:	David P. McAbee/Rachel Guidarelli			
Attorney Docket Number:	P38525X			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				130

Electronic Acknowledgement Receipt	
EFS ID:	12705974
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	59796
Filer:	David P. McAbee/Rachel Guidarelli
Filer Authorized By:	David P. McAbee
Attorney Docket Number:	P38525X
Receipt Date:	04-MAY-2012
Filing Date:	16-FEB-2012
Time Stamp:	14:17:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$130
RAM confirmation Number	550
Deposit Account	500221
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1	Miscellaneous Incoming Letter	P38525X_MP_Communication.pdf	69045 4bc071f184f02fcd2033ae4e9a3414049b8e7e32	no	1
Warnings:					
Information:					
2	Oath or Declaration filed	P38525X_Fenger_Dec.pdf	587150 7bab8947a0ed483d3d34d1849139b8925703702c	no	3
Warnings:					
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Information:					
3	Oath or Declaration filed	P38525X_Schuessler_Dec.PDF	1708118 7622d8acef89a9b0c2ca7a79a056617128de7f0c	no	3
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	30428 8592b37bed2e57a732ab46ae7e15718ecd30680d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			2394741		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/398,641	02/16/2012	2816	1380	P38525X	13	3

CONFIRMATION NO. 1050

UPDATED FILING RECEIPT



OC000000054219785

59796
INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

Date Mailed: 05/16/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Travis T. Schluessler, Berthoud, CO;
Russell J. Fenger, Beaverton, OR;

Power of Attorney: The patent practitioners associated with Customer Number 59796

Domestic Priority data as claimed by applicant

This application is a CON of 13/327,670 12/15/2011

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 02/29/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/398,641**

Projected Publication Date: 06/20/2013

Non-Publication Request: No

Early Publication Request: No

Title

Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus

Preliminary Class

327

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 13/398,641				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	620			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250			
TOTAL CLAIMS (37 CFR 1.16(j))	13	minus 20 = *			OR	x 60 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *			OR	x 250 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1250			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641
	Filing Date		2012-02-16
	First Named Inventor	Schluessler, Travis T.	
	Art Unit	2115	
	Examiner Name	Lee, Thomas C.	
	Attorney Docket Number	P38525X	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7558966		2009-07-07	Durham et al.	
	2	7818596		2010-10-19	Fenger et al.	
	3	7917789		2011-03-29	Fenger et al.	
	4	7692457		2010-04-06	To et al.	
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U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20100131781	A1	2010-05-27	Memon et al.	
	2	20090007120	A1	2009-01-01	Fenger et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641	
	Filing Date		2012-02-16	
	First Named Inventor	Schluessler, Travis T.		
	Art Unit	2115		
	Examiner Name	Lee, Thomas C.		
	Attorney Docket Number	P38525X		

	3	20060143486	A1	2006-06-29	Lamdan et al.	
	4	20110289380	A1	2011-11-24	Wilkerson et al.	
	5	20130007475	A1	2013-01-03	Ganesan et al.	
	6	20120159264	A1	2012-06-21	Azam et al.	

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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(Not for submission under 37 CFR 1.99)

Application Number	13398641
Filing Date	2012-02-16
First Named Inventor	Schluessler, Travis T.
Art Unit	2115
Examiner Name	Lee, Thomas C.
Attorney Docket Number	P38525X

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13398641
	Filing Date	2012-02-16
	First Named Inventor	Schuessler, Travis T.
	Art Unit	2115
	Examiner Name	Lee, Thomas C.
	Attorney Docket Number	P38525X

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David P. McAbee/Reg. No. 58104	Date (YYYY-MM-DD)	2013-05-19
Name/Print	David P. McAbee	Registration Number	58,104

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	15812627
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	59796
Filer:	David P. McAbee/Alycia Morell
Filer Authorized By:	David P. McAbee
Attorney Docket Number:	P38525X
Receipt Date:	19-MAY-2013
Filing Date:	16-FEB-2012
Time Stamp:	21:15:14
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P38525X_IDS.pdf	612522 cba4605da4a9b53714aac513159072feeb37a4e	no	5

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641	
	Filing Date		2012-02-16	
	First Named Inventor	Schuessler, Travis T.		
	Art Unit	2816		
	Examiner Name	Unknown		
	Attorney Docket Number	P38525X		

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
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NON-PATENT LITERATURE DOCUMENTS							Remove	
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641
	Filing Date		2012-02-16
	First Named Inventor	Schluessler, Travis T.	
	Art Unit	2816	
	Examiner Name	Unknown	
	Attorney Docket Number	P38525X	

	1	SCHLUESSLER et al., "Limiting CPU Power Consumption for Efficient Computation of 3D Workloads", IEEE International Conference on Energy Aware Computing, IEEE, December 3-5, 2012, Guzelyurt, Cyprus.	☐
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13398641
	Filing Date	2012-02-16
	First Named Inventor	Schuessler, Travis T.
	Art Unit	2816
	Examiner Name	Unknown
	Attorney Docket Number	P38525X

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David P. McAbee/Reg. No. 58104	Date (YYYY-MM-DD)	2013-06-10
Name/Print	David P. McAbee	Registration Number	58,104

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	15996200
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	59796
Filer:	David P. McAbee/Jenny Kathman
Filer Authorized By:	David P. McAbee
Attorney Docket Number:	P38525X
Receipt Date:	10-JUN-2013
Filing Date:	16-FEB-2012
Time Stamp:	16:37:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL1.pdf	4997353 153bdc55507a89150aaf0e7b59a902fa15c28cc3	no	6

Warnings:

Information:

2	Information Disclosure Statement (IDS) Form (SB08)	P38525X_IDS_6_10_13.pdf	612254 e1deaaae16f08aeb4663bebf3a090d717ba c7ea0	no	4
Warnings:					
Information:					
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Total Files Size (in bytes):			5609607		
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/398,641	02/16/2012	Travis T. Schluessler	P38525X

CONFIRMATION NO. 1050

59796
INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

PUBLICATION NOTICE



Title: Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus

Publication No.US-2013-0159741-A1

Publication Date:06/20/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publicly available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	P38525X	1050
59796 7590 10/04/2013 INTEL CORPORATION c/o CPA Global P.O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER CHAN, DANNY	
			ART UNIT 2115	PAPER NUMBER
			NOTIFICATION DATE 10/04/2013	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

heather.l.adamson@intel.com
inteldocs@cpaglobal.com

Office Action Summary	Application No. 13/398,641	Applicant(s) SCHLUESSLER ET AL.	
	Examiner DANNY CHAN	Art Unit 2115	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on February 16, 2012.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-13 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-13 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☒ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on February 16, 2012 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some * c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>6/10/2013 and 5/19/2013</u> . | 4) ☐ Other: ____. |

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. This Office Action is sent in response to Applicant's Communication received February 16, 2012 for application number 13/398641. The Office hereby acknowledges receipt of the following and placed of record in file: Specification, Drawings, Abstract, Oath/Declaration, and claims.
3. Claims 1 – 13 are presented for examination.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: **Element 115 cited in [0022] in applicant's specification is not shown in the drawings**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Title

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The examiner believes that the title of the invention is imprecise. A descriptive title indicative of the invention will help in proper indexing, classifying, searching, etc. See MPEP 606.01. However, the title of the invention should be limited to 500 characters.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 6-9 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

As per **claim 6**, the claim recites a “non-transitory medium.” Applicant’s specification defines non-transitory medium to include optical storage medium and transitory matter, such as carrier waves, infrared signals, and digital signals. **A propagated signal cannot properly be classified in any of the statutory categories of machine, article of manufacture, process, or composition of matter.** Therefore, the claimed invention is directed to non-statutory subject matter.

Double Patenting

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least

one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit <http://www.uspto.gov/forms/>. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to <http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp>.

8. Claims 1-13 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1-20 of copending Application No. 13/327,670 in view of **Evoy** USPAT 5,758,133.

Instant Application 13/398641	Co-Pending Application 13/327670
1. An apparatus for efficient energy consumption comprising: an integrated circuit including, a first core; a communication bus coupled to the first core; a core workload monitor configured to determine a core workload for the first core; a bus workload monitor configured to determine a bus workload for the communication bus; and balancing control adapted to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and at least the bus workload.	1. An apparatus for efficient energy consumption comprising: an integrated circuit including, a first core and a second core, the first and second cores being asymmetric cores; a workload monitor adapted to dynamically determine a first workload for the first core and a second workload for the second core; and a balancing module adapted to dynamically tune frequency allocation between the first core and the second core based on a power limit for the integrated circuit and at least the second workload.
6. A non-transitory medium including code, when executed, to cause a machine to perform the energy efficiency operations of: receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit including the communication bus and the first processing element reaching a limit; determining if the first processing element workload indicates the first processing element is a performance bottleneck; determining if a communication bus is able to accommodate the bus workload; capping a bus frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is a performance bottle neck and determining the communication bus is able to accommodate the bus workload; and increasing a previous cap on bus	11. A non-transitory medium including code, when executed, to cause a machine to perform the energy efficiency operations of: receiving a graphics workload activity over a period of time of a graphics processor on an package including a host processor; determining if the package has reached a thermal design power (TDP) limit; in response to determining the package has reached the TDP limit, indicating a performance-related limit for the host processor is to be decreased responsive to the graphics workload activity over the period of time being greater than an activity threshold; indicating a previous performance-related limit for the host processor it to be increased in response to the graphics workload activity over the period of time being less than the activity threshold.

frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is a performance bottle neck and determining the communication bus is not able to accommodate the bus workload.	
10. A method for efficient energy consumption comprising: determining a processing workload activity for a central processor on a package; determining a graphics workload activity for a graphics processor on the package; determining a bus workload activity for a communication bus on the package; determining if the package has reached a thermal or power limit; and in response to determining the package has reached the thermal or power limit, dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity.	16. A method for efficient energy consumption comprising: determining a processing workload activity for a central processor on a package; determining a graphics workload activity for a graphics processor on the package; determining if the package has reached a thermal or power limit; and in response to determining the package has reached the thermal or power limit, determining if the central processor or the graphics processor is a performance bottleneck based at least on the graphics workload activity, setting a processor performance limit for the central processor below a previous processor performance limit in response to determining the graphics processor is the performance bottleneck, and setting a graphics performance limit for the graphics processor below a previous graphics processor performance limit in response to determining the central processor is the performance bottleneck.

9. Claim 1 of the co-pending application discloses all of the limitations of the instant application except for the limitations regarding a bus and monitoring the bus workload.

Evoy teaches monitoring the workload of a bus coupled to a core [col. 2 lines 21-38 and col. 1 line 42: processor bus]. Evoy's power saving and noise reduction method alters the frequency of a bus based on the utilization of the bus to run at an optimal power consumption and performance.

It would have been obvious to one of ordinary skill in the art to combine claim 1 of the 13/327670 application with Evoy to achieve claim 1 of the instant application because they both direct to a reduction of frequency of components for optimized performance. Evoy's teaching of altering the frequency of a bus would allow a bus connected to a core to reduce power consumption during low bus workloads. The reduction of power consumption would allow for more resources to allocate to the cores or vice versa, as described in claim 1 of the instant.

This is a provisional nonstatutory double patenting rejection.

Claim Rejections - 35 USC § 103

10. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

12. **Claims 1, 3-6, and 9-13** are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Naffziger et al. (hereinafter as **Naffziger**) PGPUB 2008/0104428, and further in view of **Evoy** USPAT 5,758,133.

13. As per **claims 1 and 10**, Naffziger teaches an apparatus for efficient energy consumption comprising: an integrated circuit [FIG. 1 module 100] including,

a first core [FIG. 1 processor 1, 106];

a core workload monitor configured to determine a core workload for the first core [0013]; and

balancing control adapted to dynamically tune power allocation on the first core based on a power limit for the integrated circuit and at least the workload [0013-0014].

Naffziger does not teach a communication bus coupled to the first core; a bus workload monitor configured to determine a bus workload for the communication bus. Specifically, Naffziger determines the workload of a first core and a second core and allocates more frequency or power to the higher workload core while decreasing frequency to the lower workload core to maintain an overall power consumption. However, Naffziger does not explicitly teach a bus connected to a core or a method for monitoring a bus workload.

Evoy teaches a method for monitoring the workload of a bus coupled to a core [col. 2 lines 21-38 and col. 1 line 42: processor bus]. Evoy's power saving and noise reduction method alters the frequency of a bus based on the utilization of the bus to run at an optimal power consumption and performance.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Naffziger and Evoy because they direct to changing the frequency of components for optimized performance. Evoy's teaching of altering the frequency of a bus would allow a bus connected to a core taught by Naffziger, to reduce power consumption during low bus workloads. The reduction of power consumption in the bus would allow Naffziger to allocate more frequency or power to the cores for optimal performance.

Naffziger teaches:

[0013] The methods and devices described herein overcome the above described problems associated with fixed power allocations. **In summary, the processors 106, 108 indicate their processing requirements to the power manager 110, which monitors the power consumption of the entire module 100. The power manager 110 may then enable the processors 106, 108 to change their operating frequencies depending on the available power.** As an example, the total power available to the module 100 may be one hundred watts. The power manager 110 may, by default, allocate fifty watts to each processor. At one point, the first processor 106 may be relatively idle and may only use thirty watts during this idle period. Accordingly, the first processor 106 is operating at its optimal performance using only thirty watts. The second processor 108 may be executing a lot of code and may be operating at the frequency limit for its fifty watt allocation. **Accordingly, the second processor 108 is not operating optimally, but it could operate optimally if it could increase its operating frequency. In order to increase the operating frequency of the second processor 108, the power manager 110 may allocate power that would otherwise be used by the first processor 106 to the second processor 108. The second processor 108 may then increase its frequency to correspond to the increased available power.**

[0014] **The operating frequency of the first processor 106 is then limited because some of its power has been allocated to the second processor 108. Should the first processor 106 need to increase its operating frequency, it will have to do so by way of the power manager 110.** For example, the first processor 106 may send a signal or the like to the power manager 110 indicating that it needs to increase its operating frequency and,

Art Unit: 2115

thus, needs to use more power. **The power manager 110 may then instruct the second processor 108 to reduce its power consumption or operating frequency so that power may be allocated to the first processor 106. The power allocation will shift between the processors 106, 108 until both processors are operating at the same fraction of optimal performance.** This fraction of optimal performance is sometimes referred to as optimability. It is noted that optimal performance is achieved when a processor is able to operate with the need to increase its operating frequency.

Evoy teaches:

[Col. 2 lines 21-38] In accordance with one embodiment of the present invention, **a method for altering a frequency of a bus based on utilization of the bus** is disclosed. **The method comprises the steps of: monitoring the bus for a predetermined number of clock cycles; lowering the frequency that the bus runs at if the bus is underutilized; and increasing the frequency that the bus runs at if the bus is at or near saturation.** The step of monitoring the bus may further comprise the steps of: clearing a clock cycle counter; clearing an idle bus counter; monitoring the bus during a clock cycle to determine if the bus is idle; increasing the clock cycle counter by one; increasing the idle bus counter by one if the bus was idle during the bus cycle; comparing the clock cycle counter to a preset clock cycle number; monitoring the bus during a next clock cycle for idleness if the clock cycle counter is not equal to the preset clock cycle number; comparing the idle bus counter to a preset idle bus number to determine if the bus was underutilized, nearing saturation or at saturation.

14. As per **claim 3, Evoy** teaches the apparatus of claim 1, wherein a core workload monitor configured to determine the core workload for the first core includes first hardware to track a first number of cycles the first core is active during a period of time [col. 3 lines 10-23].

15. As per **claim 4, Evoy** teaches the apparatus of claim 1, wherein the balancing control adapted to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and at least the bus

workload comprises the balancing control, in response to the integrated circuit operating at the power limit, being adapted to:

increase frequency for communication bus and cap frequency for the first core in response to the bus workload being greater than a bus workload threshold [col. 2 lines 26-27 and col. 3 lines 29-32] and

decrease frequency for the communication bus and increase the cap frequency for the first core in response to the bus workload being less than the bus workload threshold [col. 2 lines 25-26 and col. 3 lines 25-28].

16. As per **claim 5**, **Naffziger** teaches the apparatus of claim 1, the balancing control is further adapted to implement a low frequency limit for the communication bus [0018].

17. As per **claim 6**, **Naffziger** teaches increasing a previous cap on bus frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is a performance bottle neck and determining the communication bus is not able to accommodate the bus workload [0018]. The remainder of claim 6 is rejected on similar grounds as to claim 1.

18. As per **claim 9**, **Naffziger** teaches the non-transitory medium of claim 6, wherein the limit includes a thermal design power limit [0008: limited amount of power].

19. As per **claim 11**, **Naffziger and Evoy** teach the method of claim 10, wherein dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity comprises:

determining if the graphics workload activity is greater than a graphics activity threshold [Naffziger 0013];

determining if there is sufficient room on the communication bus based on the bus workload activity in response to determining the graphics workload activity is greater than a threshold [Naffziger 0013 and Evoy col. 2 lines 25-26 and col. 3 lines 25-28]; and

increasing a maximum allowed frequency for the communication bus in response to determining there is not sufficient room on the communication bus [Evoy col. 2 lines 26-27 and col. 3 lines 29-32]; and

decreasing a maximum allowed frequency for the communication bus in response to determining there is sufficient room on the communication bus [Evoy col. 2 lines 25-26 and col. 3 lines 25-28].

20. As per **claims 12 and 13**, **Evoy** teaches the method of claims 10 and 11, wherein the method is performed in response to execution of privileged level power service code [col. 3 lines 11-32¹].

21. **Claims 2 and 7-8** are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Naffziger et al. (hereinafter as **Naffziger**) PG PUB 2008/0104428 in view of **Evoy** US PAT 5,758,133, and further in view of Borkar et al. (hereinafter as **Borkar**) PHPUB 2007/0074011.

22. As per **claim 2 and 7**, Naffziger and Evoy teach the apparatus of claim 1, further comprising a second core [FIG. 1 processor 2, 108] and a workload monitor configured

¹ Privileged level power service code refers to tracking active cycles during period of measurements. Evoy tracks active cycles during a period of monitoring.

to determine a second core workload for the second core [Naffziger 0013], wherein the first core includes a host processing core [Naffziger 0006], the second core includes a graphics processing core [Naffziger 0006²], and wherein the balancing control is further adapted to dynamically tune power allocation between the first core, the second core, and the communication bus based on a power limit for the integrated circuit and at least the bus workload, the core workload, and the second core workload [Naffziger 0013-0014 and Evoy Col. 2 lines 21-38].

Naffziger and Evoy do not teach a second core workload monitor or the communication bus includes a ring interconnect. Naffziger monitors the workload of processors through a single power manager, but it would have been obvious to one of ordinary skill in the art to have dedicated workload monitors for each core. Evoy teaches a communication bus but does not specify that the communication bus is a ringed interconnect.

Borkar teaches another power optimization system utilizing an interconnect to link a plurality of cores for fast communication and redistribution of tasks to cores [0018]. Borkar teaches a ringed interconnect which is also linked to system memory [FIG. 7 interconnect 710] [0039].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Naffziger, Evoy, and Borkar because they direct to achieving optimized performance while maintaining a power consumption level. Borkar's teaching of an interconnect linking a plurality of cores for redistribution of tasks would allow the

² Processors have cores. Naffziger also states that the die could be any device or circuits, but they are referred to as processors. Therefore, asymmetric processors or cores of any type using Naffziger's power management techniques are anticipated by Naffziger.

combination of Naffziger and Evoy to reallocate the workload of cores and perform frequency adjustments less often, which would save on power for computations and transitioning.

Borkar teaches:

[0018] Once a dynamic profile has been created for each core, cores in a many-core processor may be grouped into different bins according to their characteristics. For example, cores with high maximum operating frequency may be labeled as fast cores; cores with low power consumption may be labeled as low power consumption cores; cores with good trending information may be labeled as reliable cores; etc. Based on dynamic profiles and the grouping information, the operating system ("OS") or an intermediate software layer may allocate a task to those cores that are most suitable for the task. For example, if the task requires intensive computation, the task may be assigned to fast cores. **Once certain cores are selected for the task, the interconnect fabric in the many-core processor may be reconfigured to ensure a high level of connectivity among the selected cores so that an at least acceptable bandwidth and latency across the selected cores may be achieved.** Additionally, the OS may re-allocate cores to a task in response to changes in the environment and the interconnect fabric may be re-configured accordingly.

[0039] FIG. 7 shows yet another example computing system 700 where a many-core processor may be used. In system 700, **system interconnect 710** that connects multiple processors (e.g., 720A, 720B, 720C, and 720D) is a links-based point-to-point connection. **Each processor may connect to the system interconnect** through a links hub (e.g., 730A, 730B, 730C, and 730D). **In some embodiments, a links hub may be colocated with a memory controller, which coordinates traffic to/from a system memory. One or more processor may have many cores. The many core processor(s) may have a dynamic profiling apparatus to build a dynamic profile for each core.** Dynamic profiles may be built through periodic testing initiated by the dynamic profiling apparatus itself or through tests initiated by the OS. Each dynamic profile may include information on a core's maximum operating frequency, power consumption, power leakage, functional correctness, and other parameters. The dynamic profile may also include the trending information of these parameters.

23. As per **claim 8**, **Naffziger** teaches causing the machine to perform the operations of:

increasing a previous cap on frequency for one or more processor core in response to determining the one or more graphics cores is not a performance bottleneck [0014];

capping frequency for the one or more processor cores in response to determining the first processing element workload indicates the first processing element is a performance bottle neck and determining the communication bus is able to accommodate the bus workload [0018].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR §1.111(c).

24. Ananthakrishnan et al. (2013/0061064) dynamically allocates frequency to different domains of a processor to meet a power budget.

25. Burchard et al. (PGPUB 2011/0113274) teaches changing the operating frequency of a system on chip device to meet a workload.

26. Burchard et al. (USPAT 8,185,215) teaches determining the workload of an electronic device.

27. Lint et al. (PGPUB 2006/0069936) adjusts the performances of processors based on received power management requests.
28. Gupta (PGPUB 2004/0121797) teaches an embodiment where the frequency of one processor is increased and the frequency of another processor is reduced.
29. Donovan (USPAT 8,281,170) determines the frequency of a bus based on the number of outstanding requests.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANNY CHAN whose telephone number is (571)270-5134. The examiner can normally be reached on Monday-Friday, 8AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 5712723667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Art Unit: 2115

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/DANNY CHAN/
Examiner, Art Unit 2115

/Thomas Lee/
Supervisory Patent Examiner, Art Unit 2115

Notice of References Cited	Application/Control No. 13/398,641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.	
	Examiner DANNY CHAN	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0104428	05-2008	Naffziger et al.	713/300
*	B	US-5,758,133	05-1998	Evoy, David R.	713/501
*	C	US-2007/0074011	03-2007	Borkar et al.	712/227
*	D	US-2011/0113274	05-2011	Burchard et al.	713/322
*	E	US-2013/0061064	03-2013	Ananthakrishnan et al.	713/300
*	F	US-2011/0113274	05-2011	Burchard et al.	713/322
*	G	US-8,185,215	05-2012	Burchard et al.	700/22
*	H	US-2006/0069936	03-2006	Lint et al.	713/320
*	I	US-2004/0121797	06-2004	Gupta, Vivek G.	455/550.1
*	J	US-8,281,170	10-2012	Donovan, Timothy J.	713/322
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

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	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	09/27/2013								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
	11	✓								
	12	✓								
	13	✓								

Search Notes 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300	9/27/2013	DC
713	320	9/27/2013	DC

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Search - PALM	9/26/2013	DC
Text Search - EAST; PGPUB; USPAT	9/26/2013	DC
IDS - EAST: PGPUB; USPAT	9/27/2013	DC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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BIB DATA SHEET

CONFIRMATION NO. 1050

SERIAL NUMBER 13/398,641	FILING or 371(c) DATE 02/16/2012 RULE	CLASS 713	GROUP ART UNIT 2115	ATTORNEY DOCKET NO. P38525X		
APPLICANTS Travis T. Schluessler, Berthoud, CO; Russell J. Fenger, Beaverton, OR; ** CONTINUING DATA ***** This application is a CON of 13/327,670 12/15/2011 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/29/2012						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /DANNY CHAN/ Acknowledged Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CO	SHEETS DRAWINGS 10	TOTAL CLAIMS 13	INDEPENDENT CLAIMS 3
ADDRESS INTEL CORPORATION c/o CPA Global P.O. BOX 52050 MINNEAPOLIS, MN 55402 UNITED STATES						
TITLE Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus						
FILING FEE RECEIVED 1380	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit			

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S2	33542	allocat\$3 near5 frequenc\$3	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:21
S3	247	S2 and "713"/\$.cls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:21
S4	734	(equilibrium or maintain\$3 or constant or balanc\$3) near4 (power) same frequenc\$3 and "713"/\$.cls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:21
S5	32	S3 and S4	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:21
S6	22	S5 and bus	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:22
S7	18	S6 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:23
S8	4	bus near5 workload near5 monitor	US-PGPUB; USPAT	OR	OFF	2013/09/26 17:26
S9	11	bus with monitor with workload	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:08
S10	13532	bus near5 frequency	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:09
S11	8	bus near5 frequency with workload	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:09
S12	260	variable near5 bus near3 frequency	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:10
S13	20	S12 and "713"/\$.cls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:10
S14	5995235	(increas\$3 or decreas\$3) bus near3 frequency	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:12
S15	1039	(increas\$3 or decreas\$3) with bus near3 frequency	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:12
S16	156	S15 and "713"/\$.cls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:12
S17	3	S15 same workload and "713"/\$.cls.	US-PGPUB;	OR	OFF	2013/09/26 18:13

			USPAT			
S18	1106	bus near5 frequency with increase\$3	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:19
S19	138	S18 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:19
S20	950	(increas\$3 or decreas\$3) near5 bus near3 frequency	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:19
S21	151	S20 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:19
S22	35	S20 same (request\$1 or pend\$3 or queue\$3 or latenc\$3 or consump\$5 or utiliz\$5 or max\$3) and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2013/09/26 18:29
S23	1	"13398641"	US-PGPUB; USPAT	OR	OFF	2013/09/27 10:30
S24	1	("20070074011").PN.	US-PGPUB; USPAT	OR	OFF	2013/09/27 12:20
S25	0	(2004/0121797).CCLS.	US-PGPUB; USPAT	OR	OFF	2013/09/27 13:26
S26	1	("20040121797").PN.	US-PGPUB; USPAT	OR	OFF	2013/09/27 13:26
S27	1	(13/327670).APP.	US-PGPUB; USPAT	OR	OFF	2013/09/27 14:25
S28	1	13/327670	US-PGPUB; USPAT	OR	OFF	2013/09/27 16:50
S29	2	"13327670"	US-PGPUB; USPAT	OR	OFF	2013/09/27 16:51
S30	19	("20060143486" "20100131781" "5758133" "7917789" "20110113274" "20130061064" "20110289380" "7818596" "20070074011" "8185215" "20120159264" "7558966" "20090007120" "20130007475" "7692457" "20040121797" "20060069936" "20080104428" "8281170").PN.	US-PGPUB; USPAT	OR	OFF	2013/09/27 18:23
S31	5367	713/320.ccls.	US-PGPUB; USPAT	OR	OFF	2013/09/27 18:32
S32	8265	713/300.ccls.	US-PGPUB; USPAT	OR	OFF	2013/09/27 18:32

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Receipt date: 05/19/2013

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13398641 - GAU: 2115

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641
	Filing Date		2012-02-16
	First Named Inventor	Schuessler, Travis T.	
	Art Unit	2115	
	Examiner Name	Lee, Thomas C.	
	Attorney Docket Number	P38525X	

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	1	7558966		2009-07-07	Durham et al.	
	2	7818596		2010-10-19	Fenger et al.	
	3	7917789		2011-03-29	Fenger et al.	
	4	7692457		2010-04-06	To et al.	
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	1	20100131781	A1	2010-05-27	Memon et al.	
	2	20090007120	A1	2009-01-01	Fenger et al.	

Receipt date: 05/19/2013 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641	13398641 - GAU: 2115
	Filing Date		2012-02-16	
	First Named Inventor	Schuessler, Travis T.		
	Art Unit	2115		
	Examiner Name	Lee, Thomas C.		
	Attorney Docket Number	P38525X		

	3	20060143486	A1	2006-06-29	Lamdan et al.	
	4	20110289380	A1	2011-11-24	Wilkerson et al.	
	5	20130007475	A1	2013-01-03	Ganesan et al.	
	6	20120159264	A1	2012-06-21	Azam et al.	

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Examiner Signature	/Danny Chan/	Date Considered	09/27/2013
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641 13398641 - GAU: 2115
	Filing Date		2012-02-16
	First Named Inventor	Schluessler, Travis T.	
	Art Unit	2115	
	Examiner Name	Lee, Thomas C.	
	Attorney Docket Number	P38525X	

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Receipt date: 05/19/2013 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641 13398641 - GAU: 2115
	Filing Date		2012-02-16
	First Named Inventor	Schuessler, Travis T.	
	Art Unit	2115	
	Examiner Name	Lee, Thomas C.	
	Attorney Docket Number	P38525X	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David P. McAbee/Reg. No. 58104	Date (YYYY-MM-DD)	2013-05-19
Name/Print	David P. McAbee	Registration Number	58,104

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Receipt date: 06/10/2013

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13398641 - GAU: 2115

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13398641
	Filing Date	2012-02-16
	First Named Inventor	Schluessler, Travis T.
	Art Unit	2816
	Examiner Name	Unknown
	Attorney Docket Number	P38525X

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641	13398641 - GAU: 2115
	Filing Date		2012-02-16	
	First Named Inventor	Schluessler, Travis T.		
	Art Unit	2816		
	Examiner Name	Unknown		
	Attorney Docket Number	P38525X		

1	SCHLUESSLER et al., "Limiting CPU Power Consumption for Efficient Computation of 3D Workloads", IEEE International Conference on Energy Aware Computing, IEEE, December 3-5, 2012, Guzelyurt, Cyprus.	☐
If you wish to add additional non-patent literature document citation information please click the Add button Add		
EXAMINER SIGNATURE		
Examiner Signature	/Danny Chan/	Date Considered 09/27/2013
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.		

Receipt date: 06/10/2013 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641 13398641 - GAU: 2115
	Filing Date		2012-02-16
	First Named Inventor	Schuessler, Travis T.	
	Art Unit	2816	
	Examiner Name	Unknown	
	Attorney Docket Number	P38525X	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

- ☐ See attached certification statement.
- ☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/David P. McAbee/Reg. No. 58104	Date (YYYY-MM-DD)	2013-06-10
Name/Print	David P. McAbee	Registration Number	58,104

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Schluessler, et al.	§	Group Art Unit:	2115
		§		
Serial No.:	13/398,641	§	Conf. No.:	1050
		§		
Filed:	February 16, 2012	§	Examiner:	Chan, Danny
		§		
		§	Atty. Dkt. No.:	ITL.3139P1US
		§		(P38525X)
		§		
For:	Method, Apparatus, And System For	§		
	Energy Efficiency And Energy	§		
	Conservation Including Power And	§		
	Performance Workload-Based Balancing	§		
	Between Multiple Processing Elements	§		
	And/Or A Communication Bus (As	§		
	Amended)	§		

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REPLY TO OFFICE ACTION MAILED OCTOBER 4, 2013

Sir:

In response to the Office Action mailed October 4, 2013, please amend the above-referenced patent application as follows:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendments to the Specification:

Please amend the title as shown below:

A Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Workload-Based Balancing Between Multiple Processing Elements and/or a Communication Bus

Please amend paragraph 23 beginning on page 8 with the following amended paragraph:

[0023] As depicted, core 101 includes two hardware threads 101a and 101b, which may also be referred to as hardware thread slots 101a and 101b. Therefore, software entities, such as an operating system, in one embodiment potentially view processor 100 as four separate processors, i.e. four logical processors or processing elements capable of executing four software threads concurrently. As ~~eluded~~ alluded to above, a first thread is associated with architecture state registers 101a, a second thread is associated with architecture state registers 101b, a third thread may be associated with architecture state registers 102a, and a fourth thread may be associated with architecture state registers 102b. Here, each of the architecture state registers (101a, 101b, 102a, and 102b) may be referred to as processing elements, thread slots, or thread units, as described above. As illustrated, architecture state registers 101a are replicated in architecture state registers 101b, so individual architecture states/contexts are capable of being stored for logical processor 101a and logical processor 101b. In core 101, other smaller resources, such as instruction pointers and renaming logic in rename allocator logic 130 may also be replicated for threads 101a and 101b. Some resources, such as re-order buffers in reorder/retirement unit 135, ILTB 120, load/store buffers, and queues may be shared through partitioning. Other resources, such as general purpose internal registers, page-table base register(s), low-level data-cache and data-TLB [[115]], execution unit(s) 140, and portions of out-of-order unit 135 are potentially fully shared.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for efficient energy consumption comprising: an integrated circuit including, a first core;

a communication bus coupled to the first core;

a core workload monitor configured to determine a core workload for the first core;

a bus workload monitor configured to determine a bus workload for the communication bus; and

balancing control adapted to receive the bus workload and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and at least a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit.

2. (Currently Amended) The apparatus of claim 1, further comprising a second core and a second core workload monitor configured to determine a second core workload for the second core, wherein the first core includes a host processing core, the second core includes a graphics processing core, and the communication bus includes a ring interconnect, and wherein the balancing control is further adapted to dynamically tune power allocation between the first core, the second core, and the communication bus based on [[a]] the power limit for the integrated circuit and at least the bus workload, the core workload, and the second core workload.

3. (Canceled)

4. (Currently Amended) The apparatus of claim 1, wherein the balancing control ~~adapted to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and at least the bus workload comprises the~~

~~balancing control~~, in response to the integrated circuit operating at the power limit, being adapted to:

increase frequency for the communication bus and cap frequency for the first core in response to the bus workload being greater than ~~[[a]]~~ the bus workload threshold;

and

decrease frequency for the communication bus and increase the ~~cap~~ frequency for the first core in response to the bus workload being less than the bus workload threshold.

5. (Canceled)

6. (Currently Amended) A non-transitory storage medium including code, when executed, to cause a machine to perform the energy efficiency operations of:

receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit including the communication bus and the first processing element reaching a limit;

determining if the first processing element workload indicates the first processing element is a performance bottleneck;

determining if a communication bus is able to accommodate the bus workload;

capping a bus frequency of at least the communication bus and a frequency of a second processing element in response to determining the first processing element workload indicates the first processing element is a performance ~~bottle-neck~~ bottleneck and determining the communication bus is able to accommodate the bus workload; and

increasing a previous cap on bus frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is a performance ~~bottle-neck~~ bottleneck and determining the communication bus is not able to accommodate the bus workload.

7. (Currently Amended) The non-transitory storage medium of claim 6, wherein the first processing element includes one or more graphics cores, the second processing element includes one or more processor cores, the communication bus includes a ring interconnect, and wherein the code includes privileged level power service code.

8. (Currently Amended) The non-transitory storage medium of claim 7, wherein the code, when executed, further causes the machine to perform the operations of:

increasing a previous cap on frequency for one or more processor core in response to determining the one or more graphics cores is not a performance bottleneck;

capping frequency for the one or more processor cores in response to determining the first processing element workload indicates the first processing element is a performance bottleneck and determining the communication bus is able to accommodate the bus workload.

9. (Currently Amended) The non-transitory storage medium of claim 6, wherein the limit includes a thermal design power limit.

10. (Currently Amended) A method for efficient energy consumption comprising:
determining a processing workload activity for a central processor on a package;
determining a graphics workload activity for a graphics processor on the package;
determining a bus workload activity for a communication bus on the package;
determining if the package has reached a thermal or power limit; and
in response to determining the package has reached the thermal or power limit,
dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity, including adjusting a maximum allowed frequency for the communication bus by a plurality of steps and adjusting a maximum allowed frequency for the central processor by a step.

11. (Currently Amended) The method of claim 10, wherein dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity comprises:

determining if the graphics workload activity is greater than a graphics activity threshold;
determining if there is sufficient room on the communication bus based on the bus workload activity in response to determining the graphics workload activity is greater than a threshold; [[and]]

increasing [[a]] the maximum allowed frequency for the communication bus in response to determining there is not sufficient room on the communication bus; and

decreasing a maximum allowed frequency for the communication bus in response to determining there is sufficient room on the communication bus.

12. (Original) The method of claim 10, wherein the method is performed in response to execution of privileged level power service code.

13. (Original) The method of claim 11, wherein the method is performed in response to execution of privileged level power service code.

14. (New) The apparatus of claim 1, wherein the balancing control is to receive a hint regarding a future workload and to dynamically tune the power allocation further based on the hint.

15. (New) The apparatus of claim 2, wherein the balancing control is to increase a frequency of the second core and to reduce a frequency of the first core when the second core is to execute a producer thread and the first core is to execute a consumer thread to consume information produced by the producer thread.

16. (New) The apparatus of claim 4, wherein the balancing control is to increase the communication bus frequency by a different amount than the first core frequency decrease.

17. (New) The apparatus of claim 4, wherein the balancing control is to further increase frequency for a second core, the second core and the communication bus having power planes tied together.

18. (New) The non-transitory storage medium of claim 6, wherein the code, when executed further causes the machine to perform the operations of receiving a hint regarding a future workload and dynamically tuning power allocation between the first processing element and the second processing element based on the hint.

19. (New) The non-transitory storage medium of claim 7, wherein the code, when executed, further causes the machine to perform the operations of increasing the frequency of the second processing element and reducing the frequency of the first processing element when the second processing element is to execute a producer thread and the first processing element is to execute a consumer thread to consume information produced by the producer thread.

20. (New) The non-transitory storage medium of claim 19, wherein the code, when executed, further causes the machine to perform the operations of increasing the communication bus frequency by a different amount than an amount by which the frequency of the first processing element is decreased.

REMARKS/ARGUMENTS

The specification has been amended such that the drawings are co-extensive with the specification and thus it is respectfully submitted that the objection to the drawings is overcome.

Provided herewith is a new title and thus it is respectfully submitted that the objection to the title is overcome.

Provided herewith is a Terminal Disclaimer and thus it is respectfully submitted that the non-statutory double patenting rejection is overcome.

Claims 6-9 have been amended to clarify that the medium is a non-transitory storage medium and as such, the §101 rejection is overcome.

Pending claims 1, 3-6 and 9-13 stand rejected under 35 U.S.C. §103(a) over U.S. Publication No. 2008/0104428 (Naffziger) and further in view of U.S. Patent No. 5,758,133 (Evoy). Applicants respectfully traverse the rejection. As to claim 1, the art, alone and in combination, fails to anywhere teach or suggest the recited balancing control that is adapted to receive a bus workload and to dynamically tune power allocation based on a power limit and a comparison between the bus workload and a bus workload threshold.

Here, the Office Action concedes that the primary reference Naffziger fails to anywhere address this bus workload matter whatsoever. Instead, reliance is on the secondary reference Evoy. However, Evoy fails to teach or suggest the arrangement in claim 1. Rather, all that is taught in Evoy is that a bus speed can be reduced based on an idleness of the bus. Yet this idleness is not a bus workload determined by a bus workload monitor. Nor is there any teaching or suggestion of comparison between a bus workload and a bus workload threshold.

Furthermore, even when combined the references fail to teach or suggest that this power allocation also be based on a power limit that corresponds to a thermal dissipation capacity for an integrated circuit. Here, all that the Office Action refers to is paragraphs 13 and 14 of Naffziger, which simply teaches that a processor has an available power level. But nothing in the reference anywhere teaches or suggests that this corresponds to a thermal dissipation capacity. Accordingly, for all these reasons claim 1 and the claims depending therefrom are patentable over the cited art.

Regarding independent claim 6 the art fails to teach or suggest the arrangement of the claim. This is the case, at least because even assuming that Naffziger and Evoy are combined, there is absolutely nothing to recommend capping both a bus frequency and a frequency of a

second processing element in response to determining that a first processing element workload indicates that that processing element is a performance bottleneck. Here, neither of the references anywhere teach or suggest such capping in response to determination of a performance bottleneck.

Rather in Naffziger all that is taught is that a processor is provided a higher operating frequency if it is currently operating at less than a requested frequency for the processor. But this does not meet the subject matter regarding performance bottleneck determination. And even when combined, this subject matter regarding capping of both bus frequency and other processing element frequency is nowhere taught or suggested, in that Evoy simply is concerned with bus speed based on bus utilization only, and nowhere addresses anything with regard to processing elements, and certainly not any determination of performance bottleneck as set forth in the claim. Accordingly, claim 6 and its dependent claims are patentable over the cited art.

Regarding independent claim 11, the cited art fails to teach or suggest, at least, that a maximum allowed frequency for a communication bus is adjusted by multiple steps and a maximum allowed frequency for a central processor is adjusted by a step. Here, none of the references anywhere teach or suggest any type of step control, and certainly not where one adjustment is by multiple steps and another adjustment is by a step. Accordingly, claim 10 and its dependent claims are patentable over the cited art.

New claims 14-20 are patentable for at least the same reasons as the independent claims.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Date: January 3, 2014

Respectfully submitted,
/Mark J. Rozman/
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REJECTION OVER A PENDING "REFERENCE" APPLICATION**Docket Number (Optional)
ITL.3139P1US (P38525X)

In re Application of: Schluessler, et al.

Application No.: 13/398,641

Filed: February 16, 2012

For: METHOD, APPARATUS, AND SYSTEM FOR ENERGY EFFICIENCY AND ENERGY CONSERVATION INCLUDING POWER AND PERFORMANCE BALANCING BETWEEN MULTIPLE PROCESSING ELEMENTS AND/OR A COMMUNICATION BUS

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1/3/14
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Application Number	13/398,641
Filing Date	February 16, 2012
First Named Inventor	Travis T. Schluessler
Title	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
Art Unit	2115
Examiner Name	Chan, Danny
Attorney Docket Number	ITL.3139P1US (P38525X)

SIGNATURE of Applicant or Patent Practitioner			
Signature		Date (Optional)	11/3/14
Name	Mark J. Rozman	Registration Number	42,117
Title (if Applicant is a juristic entity)	Attorney		
Applicant Name (if Applicant is a juristic entity)		Intel Corporation	
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.			
☐ *Total of _____ forms are submitted.			

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B(07-12)

Approved for use through 11/30/2014. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

- ☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

47795

OR

- ☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

- ☒ The address associated with the above-mentioned Customer Number.

OR

- ☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant:

- ☐ Inventor or Joint Inventor
☐ Legal Representative of a Deceased or Legally Incapacitated Inventor
☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign
☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature

Name

Heather L. Adamson

Date

Telephone

503-712-5273

Title and Company

Administrator of Patents, Intel Corporation

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

- ☒ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: Schluessler, et al.

Application No./Patent No.: 13/398,641

Filed/Issue Date: February 16, 2012

Titled: Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus

Intel Corporation, a corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 030371, Frame 0478, or for which a copy thereof is attached.
- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.☐ Additional documents in the chain of title are listed on a supplemental sheet(s).☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Mark J. Rozman

Printed or Typed Name

Date

42,117

Title or Registration Number

Electronic Patent Application Fee Transmittal				
Application Number:		13398641		
Filing Date:		16-Feb-2012		
Title of Invention:		Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		
First Named Inventor/Applicant Name:		Travis T. Schluessler		
Filer:		Mark J. Rozman/Pamela Polnick		
Attorney Docket Number:		P38525X		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Statutory or Terminal Disclaimer	1814	1	160	160
Total in USD (\$)				160

Electronic Acknowledgement Receipt	
EFS ID:	17815930
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	59796
Filer:	Mark J. Rozman/Pamela Polnick
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	P38525X
Receipt Date:	03-JAN-2014
Filing Date:	16-FEB-2012
Time Stamp:	16:32:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$160
RAM confirmation Number	2767
Deposit Account	201504
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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1		ITL_3139P1US_ROA_10-4-2013.pdf	36464 37ef0389d483dbc3ea1665156bbe6b5537923d0	yes	9
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Specification		2	2	
	Claims		3	7	
	Applicant Arguments/Remarks Made in an Amendment		8	9	
Warnings:					
Information:					
2	Terminal Disclaimer Filed	ITL_3139P1US_Terminal_Disclaimer.pdf	139203 b72b5cf12d3aa0d91ad16f75c097557558f047754	no	1
Warnings:					
Information:					
3	Power of Attorney	ITL_3139P1US_POA.pdf	401831 47d8c35505918fe53c3d8bee9d9f6ecc4fa995e4	no	2
Warnings:					
Information:					
4	Assignee showing of ownership per 37 CFR 3.73.	ITL_3139P1US_373.pdf	184872 d54fe8dd2e918065acd24513759bb0f746836ff9	no	2
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30608 1cf3a7e63ad6542b46d8e6ca98be8fb1ac7c46a2	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			792978		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 13/398,641	Filing Date 02/16/2012	☐ To be Mailed
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO						
APPLICATION AS FILED – PART I						
(Column 1)		(Column 2)				
FOR	NUMBER FILED	NUMBER EXTRA			RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*			X \$ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*			X \$ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL	
APPLICATION AS AMENDED – PART II						
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT	01/03/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
	TOTAL ADD'L FEE					0
(Column 1)		(Column 2)		(Column 3)		
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	*	Minus	**	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
	TOTAL ADD'L FEE					
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/398,641	02/16/2012	Travis T. Schluessler	ITL.3139P1US (P38525X)

CONFIRMATION NO. 1050

POA ACCEPTANCE LETTER

47795
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631



Date Mailed: 01/10/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/03/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/gbien-aime/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/398,641	02/16/2012	Travis T. Schluessler	P38525X

59796
INTEL CORPORATION
c/o CPA Global
P.O. BOX 52050
MINNEAPOLIS, MN 55402

CONFIRMATION NO. 1050
POWER OF ATTORNEY NOTICE



Date Mailed: 01/10/2014

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/03/2014.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/gbien-aime/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Application Number 	Application/Control No. 13/398,641	Applicant(s)/Patent under Reexamination SCHLUESSLER ET AL.	
Document Code - DISQ		Internal Document – DO NOT MAIL	

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 1/03/14	This patent is subject to a Terminal Disclaimer	

Approved/Disapproved by:

jean proctor

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641	
	Filing Date		2012-02-16	
	First Named Inventor	Travis T. Schluessler, et al.		
	Art Unit	2115		
	Examiner Name	Danny Chan		
	Attorney Docket Number	ITL.3139P1US (P38525X)		

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S. PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20120324248		2012-12-20	Schluessler, et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add
NON-PATENT LITERATURE DOCUMENTS							Remove	
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641
	Filing Date		2012-02-16
	First Named Inventor	Travis T. Schluessler, et al.	
	Art Unit	2115	
	Examiner Name	Danny Chan	
	Attorney Docket Number	ITL.3139P1US (P38525X)	

	1		☐
If you wish to add additional non-patent literature document citation information please click the Add button Add			
EXAMINER SIGNATURE			
Examiner Signature		Date Considered	
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			
¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.			

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13398641
	Filing Date	2012-02-16
	First Named Inventor	Travis T. Schluessler, et al.
	Art Unit	2115
	Examiner Name	Danny Chan
	Attorney Docket Number	ITL.3139P1US (P38525X)

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2014-03-07
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13398641		
Filing Date:		16-Feb-2012		
Title of Invention:		Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		
First Named Inventor/Applicant Name:		Travis T. Schluessler		
Filer:		Mark J. Rozman/Stephanie Petreas		
Attorney Docket Number:		ITL.3139P1US (P38525X)		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	18400932
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.3139P1 US (P38525X)
Receipt Date:	07-MAR-2014
Filing Date:	16-FEB-2012
Time Stamp:	12:20:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$180
RAM confirmation Number	10338
Deposit Account	201504
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	ITL3139P1USIDSciting3139.pdf	611967 dde69048105280cb9b4d2f35411569fa40576c33	no	4
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30813 3210a5287811ca3ffbc28b71b38df02474db2b6a	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			642780		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	ITL.3139P1US (P38525X)	1050
47795 7590 04/22/2014 TROP, PRUNER & HU, P.C. 1616 S. VOSS RD., SUITE 750 HOUSTON, TX 77057-2631			EXAMINER CHAN, DANNY	
			ART UNIT 2115	PAPER NUMBER
			MAIL DATE 04/22/2014	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 13/398,641	Applicant(s) SCHLUESSLER ET AL.	
	Examiner DANNY CHAN	Art Unit 2115	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on January 3, 2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-20 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|--|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date <u>3/7/2014</u> | 4) ☐ Other: ____ |

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.
2. Claims 1-2, 4, and 6-20 are pending.
3. Claims 1-2, 4, 6-11, 14-20 have been amended.
4. Claims 14-20 are new.
5. This action is Final.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (**pre-AIPA** 35 U.S.C. 102(e)).

7. **Claims 1, 4, 10-14, 16-17, and 20** are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Barr et al. (hereinafter as **Barr**) PG PUB 2005/0060594.

8. As per **claim 1**, Barr teaches an apparatus for efficient energy consumption comprising: an integrated circuit [0028] including,

a first core [FIG. 1A devices 146 and paragraph 0037];

a communication bus coupled to the first core [FIG. 1A PCI bus 110];

a core workload monitor configured to determine a core workload for the first core [FIG. 1A frequency manager 158];

a bus workload monitor configured to determine a bus workload for the communication bus [FIG. 1A frequency manager 158¹]; and

balancing control adapted to receive the bus workload and to dynamically tune power allocation on the first core based on a power limit for the integrated circuit and a comparison between the workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit [0056 and 0059²].

9. As per **claim 4**, Barr teaches the apparatus of claim 1, wherein the balancing control, in response to the integrated circuit operating at the power limit, being adapted to:

¹ Frequency manager 158 monitors the workload of devices connected and the bandwidth requirements of the buses [see paragraph 0056 and 0059]. Therefore, the frequency manager monitors device (which can be cores) workloads and bus workloads.

² The frequency manager allocates a system power or thermal budget according to demands. A device or bus that is accessed more often would receive higher clock frequencies than another device or bus that is accessed less often, while still maintaining a budget. The bus has a threshold in the form of bandwidth requirements. Exceeding the bandwidth means it is accessed often.

increase frequency for the communication bus and cap frequency for the first core in response to the bus workload being greater than the bus workload threshold; [0059³] and

decrease frequency for the communication bus and increase the frequency for the first core in response to the bus workload being less than the bus workload threshold [0059⁴].

10. As per **claim 10**, Barr teaches a method for efficient energy consumption comprising:

determining a processing workload activity for a central processor on a package [FIG. 1A devices 146 and 0056, 0059];

determining a graphics workload activity for a graphics processor on the package [FIG. 1A devices 148 and 0056, 0059];

determining a bus workload activity for a communication bus on the package [0056 and 0059];

determining if the package has reached a thermal or power limit [0059]; and

in response to determining the package has reached the thermal or power limit, dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus

³ The frequency manager increases the clock frequency of the bus when it is accessed more often and limits the frequency of another device or core.

⁴ When communication bus is accessed less often, frequency is reallocated. The communication bus frequency decreases and the frequency of the device or core increases.

workload activity [0059⁵], including adjusting a maximum allowed frequency for the communication bus by a plurality of steps and adjusting a maximum allowed frequency for the central processor by a step [0052 and 0059⁶].

11. As per **claim 11**, Barr teaches the method of claim 10, wherein dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity comprises:

determining if the graphics workload activity is greater than a graphics activity threshold [0059];

determining if there is sufficient room on the communication bus based on the bus workload activity in response to determining the graphics workload activity is greater than a threshold [0059]; and

increasing a maximum allowed frequency for the communication bus in response to determining there is not sufficient room on the communication bus [0059]; and

decreasing a maximum allowed frequency for the communication bus in response to determining there is sufficient room on the communication bus [0059⁷].

⁵ The frequency manager determines the workload of several devices that can be processors or graphic processors, and their respective buses. The frequency manager allocates power to the devices and buses while still maintaining a thermal or power budget.

⁶ The frequency manager can select a minimal clock frequency for a device in a single step [0059]. The frequency manager can then iteratively select higher clock frequencies for another device or bus until the budget is met.

⁷ The frequency manager determines the workload associated with each device and bus. If the workload of a device or bus is greater than a threshold, it means it is accessed more often. Similarly, if a device or bus is accessed less often, it means that the workload is below a threshold. The frequency manager

12. As per **claims 12 and 13**, Barr teaches the method of claims 10 and 11, wherein the method is performed in response to execution of privileged level power service code [0042 and 0050].

13. As per **claim 14**, Barr teaches the apparatus of claim 1, wherein the balancing control is to receive a hint regarding a future workload and to dynamically tune the power allocation further based on the hint [0063].

14. As per **claim 16**, Barr teaches the apparatus of claim 4, wherein the balancing control is to increase the communication bus frequency by a different amount than the first core frequency decrease [0052 and 0059⁶].

15. As per **claim 17**, Barr teaches the apparatus of claim 4, wherein the balancing control is to further increase frequency for a second core, the second core and the communication bus having power planes tied together [0059⁸].

16. **Claim 20** is rejected on the same grounds as claim 16.

17. **Claims 6-7 and 19** are rejected under pre-AIA 35 U.S.C. 102(e) as being anticipated by **Nakao** PG PUB 2011/0310413.

18. As per **claim 6**, Nakao teaches a non-transitory storage medium including code, when executed, to cause a machine to perform the energy efficiency operations of:

receiving a bus workload for a communication bus and a first processing
element workload for a first processing element based on an integrated circuit

allocates more frequency to buses that are accessed more often and decreases the allowed frequency to buses that are accessed less often.

⁸ Barr increases or decreases the frequency of the bus based on how often the attached device is used. Therefore, the power plane of the attached device (which is a processing unit) and the bus are tied together.

including the communication bus and the first processing element reaching a limit [FIG. 7 S101 and S109, 0084 and 0116];

determining if the first processing element workload indicates the first processing element is a performance bottleneck [0116 and 0120];

determining if a communication bus is able to accommodate the bus workload [0118 and 0121];

capping a bus frequency of at least the communication bus [FIG. 3 bus 217] and a frequency of a second processing element [FIG. 3 image processing unit 207] in response to determining the first processing element workload indicates the first processing element is a performance bottleneck and determining the communication bus is able to accommodate the bus workload [0121⁹]; and

increasing a previous cap on bus frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is a performance bottleneck and determining the communication bus is not able to accommodate the bus workload [0119].

19. As per **claim 7**, Nakao teaches the non-transitory storage medium of claim 6, wherein the first processing element includes one or more graphics core [FIG. 3 image processing unit 207], the second processing element includes one or more processor

⁹ The bus is connected to another processing unit as shown in FIG. 3. When it is determined that the bottleneck is only at the CPU and that the bus can support the workload, only the CPU's frequency is increased. The frequency of the bus and the other components attached to the bus are not increased, and are capped to the power that is allocated to them.

cores [FIG. 3 CPU 201], the communication bus includes a ring interconnect [FIG. 3 bus 217], and wherein the code includes privileged level power service code [0262].

20. As per **claim 19**, Nakao teaches the non-transitory storage medium of claim 7, wherein the code, when executed, further causes the machine to perform the operations of increasing the frequency of the second processing element and reducing the frequency of the first processing element when the second processing element is to execute a producer thread and the first processing element is to execute a consumer thread to consume information produced by the producer thread [FIG. 3 and 0050¹⁰].

Claim Rejections - 35 USC § 103

21. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

22. **Claim 2** is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Barr et al. (hereinafter as **Barr**) PG PUB 2005/0060594, and further in view of Borkar et al. (hereinafter as **Borkar**) PHPUB 2007/0074011.

23. As per **claim 2**, Barr teaches the apparatus of claim 1, further comprising a second core [device 148 and paragraph 0037] and a second core workload monitor configured to determine a second core workload for the second core [FIG. 1A frequency manager 158], wherein the first core includes a host processing core [0037], the second core includes a graphics processing core [0048¹¹], and wherein the balancing control is further adapted to dynamically tune power allocation between the first core, the second

¹⁰ The image processing unit is connected to the CPU through the bus. The image processing unit is responsible for the processing of images, directed by the CPU. Therefore, the image processing unit consumes the thread while the CPU produces the thread.

¹¹ Paragraph 0049 indicates that the device can be a graphics processor or controller.

core, and the communication bus based on a power limit for the integrated circuit and at least the bus workload, the core workload, and the second core workload [0059].

Barr do not teach the communication bus includes a ring interconnect. Barr dynamically allocates frequency and power between a device and another device and its bus, while maintaining a power or thermal budget [0059]. However, Barr does not teach that the bus is a ring interconnect.

Borkar teaches another power optimization system utilizing an interconnect to link a plurality of cores for fast communication and redistribution of tasks to cores [0018]. Borkar teaches a ringed interconnect which is also linked to system memory [FIG. 7 interconnect 710] [0039].

It would have been obvious to one of ordinary skill in the art to combine the teachings of Barr and Borkar because they direct to achieving optimized performance while maintaining a power consumption level. Borkar's teaching of an interconnect linking a plurality of cores for redistribution of tasks would allow Barr to reallocate the workload of devices and perform frequency adjustments less often, which would save on power for computations and preparation of frequency transitioning.

24. **Claims 8-9 and 18** are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over **Nakao** PG PUB 2011/0310413, and further in view of Barr et al. (hereinafter as **Barr**) PG PUB 2005/0060594.

25. As per **claim 8**, Nakao teach the non-transitory storage medium of claim 7, wherein the code, when executed, further causes the machine to perform the operations of:

capping frequency for the one or more processor cores in response to determining the first processing element workload indicates the first processing element is a performance bottle neck and determining the communication bus is able to accommodate the bus workload [0121].

Nakao determines if the processing element is a performance bottle neck and also determines if the communication bus is able to support the workload. If the processing element is a bottleneck and the bus is not too slow, only the frequency of the processing element is increased [0121]. The frequency of the bus and other components connected to the bus are not increased, and thus, they are capped.

Nakao does not teach increasing a previous cap on frequency for one or more processor core in response to determining the one or more graphics cores is not a performance bottleneck. Nakao does not increase the cap of a processing unit if a graphic processing unit is not a bottleneck.

Barr teaches increasing the cap of a processing unit if a graphic processing unit is not a bottleneck. Barr teaches devices connected to the PCI bus that can be processing units or graphic controllers [0049]. Barr further teaches reallocation of frequency based on how often a device is accessed [0059]. If a graphic controller is not a bottleneck, it is not accessed as often and its frequency is decreased. A processing unit is accessed more often and therefore, its frequency cap is increased.

It would be obvious to one of ordinary skill in the art to combine the teachings of Nakao and Barr because they both direct to increasing the frequency of a bottlenecked unit. Barr's teachings would allow Nakao to allocate even more frequency resources to

the bottlenecked unit by reducing the frequency resources of a less commonly used component.

26. As per **claim 9**, Nakao teach the non-transitory storage medium of claim 6.

Nakao does not teach wherein the limit includes a thermal design power limit.

Nakao's frequency allocation method does not explicitly mention a thermal limit.

Barr teaches another frequency allocation method having a thermal or power limit [0059]. Barr teaches a thermal budget that has to be maintained.

It would be obvious to one of ordinary skill in the art to combine the teachings of Nakao and Barr because they both direct to increasing the frequency of a bottlenecked unit. Barr's teachings would allow Nakao to redistribute frequency resources when a maximum frequency allocation is reached.

27. As per **claim 18**, Nakao teaches the non-transitory storage medium of claim 6.

Nakao does not teach wherein the code, when executed further causes the machine to perform the operations of receiving a hint regarding a future workload and dynamically tuning power allocation between the first processing element and the second processing element based on the hint.

Barr teaches receiving an indication of a future workload and dynamically tuning power allocation between the processing elements. Specifically, Barr determines an expected demand and reallocates a system's power or thermal budget [0063].

It would be obvious to combine the teachings of Nakao and Barr because they both direct to increasing the frequency of a bottlenecked unit. Barr's teachings would allow Nakao to adjust the frequency allocation based on expected workload.

28. **Claim 15** is rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Barr et al. (hereinafter as **Barr**) PG PUB 2005/0060594 in view of Borkar et al. (hereinafter as **Borkar**) PHPUB 2007/0074011, and further in view of **Nakao** PG PUB 2011/0310413.

29. As per **claim 15**, Barr and Borkar teach the apparatus of claim 2. Barr and Borkar teach increasing the frequency of one processing unit in a device while reducing the frequency of another less commonly used processing unit in another device to maintain a thermal or power budget [Barr 0049 and 0059].

Barr and Borkar do not teach the second core is to execute a producer thread and the first core is to execute a consumer thread to consume information produced by the producer thread. Specifically, Barr and Borkar do not teach that a processing device attached to the bus produces a thread for another processing device attached to the bus to consume.

Nakao teaches the a processing unit producing a thread for another processing unit to consume. The image processing unit is connected to the CPU through the bus [FIG. 3]. The image processing unit is responsible for the processing of images, directed by the CPU [0050]. Therefore, the image processing unit consumes the thread while the CPU produces the thread.

It would have been obvious to combine the teachings of Barr, Borkar, and Nakao because they direct to optimizing performance through frequency control. Nakao teaches that the devices used by Barr can generate threads for other connected devices to execute.

Response to Arguments

30. Claims 1 has been amended to incorporate the limitation of “**a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit.**”

31. Claim 6 has been amended to incorporate the limitation of “capping a bus frequency of at least the communication bus **and a frequency of a second processing element.**” The prior art used in the previous Office action only limited or capped one component, but did not cap both the bus and a second processing element.

32. Claim 10 has been amended to incorporate the limitation of “**including adjusting a maximum allowed frequency for the communication bus by a plurality of steps, and adjusting a maximum allowed frequency for the central processor by a step.**”

33. Applicant's arguments, see pages 8 and 9, filed January 3, 2014, with respect to the rejection(s) of claim(s) 1, 6, and 10 under U.S.C. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of newly found prior art.

Conclusion

34. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANNY CHAN whose telephone number is (571)270-5134. The examiner can normally be reached on Monday-Friday, 8AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 5712723667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

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USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DANNY CHAN/
Examiner, Art Unit 2115

/THOMAS LEE/

Supervisory Patent Examiner, Art Unit 2115

Notice of References Cited	Application/Control No. 13/398,641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.	
	Examiner DANNY CHAN	Art Unit 2115	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0060594	03-2005	Barr et al.	713/600
*	B	US-2011/0310413	12-2011	NAKAO, Takehisa	358/1.9
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant		☐ CPA		☐ T.D.		☐ R.1.47			
CLAIM		DATE							
Final	Original	09/27/2013	04/17/2014						
	1	✓	✓						
	2	✓	✓						
	3	✓	✓						
	4	✓	✓						
	5	✓	✓						
	6	✓	✓						
	7	✓	✓						
	8	✓	✓						
	9	✓	✓						
	10	✓	✓						
	11	✓	✓						
	12	✓	✓						
	13	✓	✓						
	14		✓						
	15		✓						
	16		✓						
	17		✓						
	18		✓						
	19		✓						
	20		✓						

Receipt date: 03/07/2014

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13398641 - GAU: 2115

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13398641
	Filing Date	2012-02-16
	First Named Inventor	Travis T. Schluessler, et al.
	Art Unit	2115
	Examiner Name	Danny Chan
	Attorney Docket Number	ITL.3139P1US (P38525X)

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	1	20120324248		2012-12-20	Schluessler, et al.			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641	13398641 - GAU: 2115
	Filing Date		2012-02-16	
	First Named Inventor	Travis T. Schluessler, et al.		
	Art Unit	2115		
	Examiner Name	Danny Chan		
	Attorney Docket Number	ITL.3139P1US (P38525X)		

	1		☐
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EXAMINER SIGNATURE

Examiner Signature	/Danny Chan/	Date Considered	04/17/2014
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Receipt date: 03/07/2014 INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13398641 13398641 - GAU: 2115
	Filing Date		2012-02-16
	First Named Inventor	Travis T. Schluessler, et al.	
	Art Unit	2115	
	Examiner Name	Danny Chan	
	Attorney Docket Number	ITL.3139P1US (P38525X)	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Mark J. Rozman/	Date (YYYY-MM-DD)	2014-03-07
Name/Print	Mark J. Rozman	Registration Number	42,117

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /D.C./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	7656	power adj plane\$1	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:26
L2	576	1 same bus	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:26
L3	89446	2 abd "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:26
L4	80	2 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:26
L5	137	1 near5 bus	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:29
L6	130	5 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:30
L7	1	"13398641"	US-PGPUB; USPAT	OR	OFF	2014/04/17 13:34
L13	1	"20120324248"	US-PGPUB; USPAT	OR	OFF	2014/04/17 14:18
L14	8867	713/300.ccls.	US-PGPUB; USPAT	OR	OFF	2014/04/17 14:26
L15	5805	713/320.ccls.	US-PGPUB; USPAT	OR	OFF	2014/04/17 14:26
S1	0	bus\$2 near2 work1load\$1	US-PGPUB; USPAT	OR	OFF	2014/03/11 19:45
S2	161	bus\$2 near2 work\$1load\$1	US-PGPUB; USPAT	OR	OFF	2014/03/11 19:45
S3	142	S2 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/11 19:45
S4	76	(bus or buses) near2 work\$1load\$1	US-PGPUB; USPAT	OR	OFF	2014/03/11 19:46
S5	69	S4 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/11 19:46
S6	16	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses) near5	US-PGPUB;	OR	OFF	2014/03/11 20:01

		work\$1load\$1	USPAT			
S7	1191	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses) near5 power	US-PGPUB; USPAT	OR	OFF	2014/03/11 20:06
S8	755	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses) near2 power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/11 20:06
S9	2	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses) near5 power\$3 with work\$1load\$1	US-PGPUB; USPAT	OR	OFF	2014/03/11 20:07
S10	5	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses) near5 power\$3 with activit\$3	US-PGPUB; USPAT	OR	OFF	2014/03/11 20:07
S11	201	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses) with (activit\$3 or work\$1load\$1)	US-PGPUB; USPAT	OR	OFF	2014/03/11 20:09
S12	10	S11 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/11 20:09
S13	5706	713/320.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 09:21
S14	1	"13398641"	US-PGPUB; USPAT	OR	OFF	2014/03/12 09:21
S15	1	S14 and bus\$2 near5 frequency	US-PGPUB; USPAT	OR	OFF	2014/03/12 09:21
S16	1	S14 and bus\$2 same process\$3 near3 element\$1	US-PGPUB; USPAT	OR	OFF	2014/03/12 09:35
S17	32582	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:13
S18	4400	S17 with (power or frequenc\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:14
S19	1609	S18 and 7\$2/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:14
S20	161	bus\$2 near2 work\$1load\$1	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:18
S21	142	S20 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:18
S22	142	S21 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:18
S23	1386	S19 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:24
S24	1673	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) near5 (power or frequenc\$3) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:25
S25	546	S24 and 7\$2/\$.ccls.	US-PGPUB;	OR	OFF	2014/03/12 10:26

			USPAT			
S26	503	S25 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:26
S27	1148	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5) near5 (power or frequenc\$3) near8 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:29
S28	385	S27 and 7\$2/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:29
S29	364	S28 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 10:29
S30	16	trade\$1off near5 (bus or buses) with (power or frequenc\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/12 14:51
S31	1	("2005/0044440").URPN.	USPAT	OR	OFF	2014/03/12 15:00
S32	3	("2005/0044442").URPN.	USPAT	OR	OFF	2014/03/12 15:00
S33	5	("2005/0060594").URPN.	USPAT	OR	OFF	2014/03/12 15:00
S34	1	(10/646079).APP.	USPAT; USOCR	OR	OFF	2014/03/12 15:02
S35	32	("20040139363" "5560022" "5630110" "5630148" "5664165" "5745375" "5754867" "5790877" "5815734" "5918061" "5930496" "5964879" "6070207" "6073244" "6134621" "6185692" "6211715" "6295568" "6484222" "6510473" "6513124" "6564279" "6714890" "6763478" "6772263" "6782438" "6948020" "6954813" "6963990").PN. OR ("7206960").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:02
S36	1	(10/646099).APP.	USPAT; USOCR	OR	OFF	2014/03/12 15:03
S37	29	("20040139363" "5560022" "5630110" "5630148" "5664165" "5745375" "5754867" "5790877" "5815734" "5918061" "5930496" "6070207" "6073244" "6134621" "6185692" "6211715" "6295568" "6484222" "6510473" "6513124" "6564279" "6714890" "6763478" "6772263" "6782438" "6948020" "6954813" "6963990").PN. OR ("7146519").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:03
S38	1	("2005/0044440").URPN.	USPAT	OR	OFF	2014/03/12 15:03
S39	7	("20050044440" "20080016308" "20080082779" "20090006781" "20090150710" "6941437" "7484065").PN. OR ("8166316").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:03
S40	1	(10/646078).APP.	USPAT; USOCR	OR	OFF	2014/03/12 15:03
S41	28	("20040139363" "5560022" "5630110" "5630148" "5664165" "5745375" "5754867" "5790877" "5815734"	US-PGPUB; USPAT;	OR	OFF	2014/03/12 15:03

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S42	41	S41 S37 S35 S31 S32 S33	US- PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:04
S43	2	"20080104428"	US- PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:16
S44	3	("2008/0104428").URPN.	USPAT	OR	OFF	2014/03/12 15:16
S45	16	("20040098650" "20040121797" "20050289365" "20060069936" "20070074011" "20070088966" "20070124608" "20070226482" "5142684" "6711691" "6922783" "6990598" "7162279" "7398414").PN. OR ("7844838").URPN.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:16
S46	19	S44 S45	US- PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:16
S47	14	S46 and (bus or buses)	US- PGPUB; USPAT; USOCR	OR	OFF	2014/03/12 15:18
S48	38118	bus near4 (clock\$1 or frequenc\$3)	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:51
S49	4055	S48 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:51
S50	1555	S48 and "713"/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:51
S51	640	S48 and "713"/300.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:51
S52	17084	bus near2 (clock\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:52
S53	944	S52 and "713"/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:52
S54	2702	S52.ab,clm.	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:53
S55	230	S54 and "713"/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/12 16:53
S56	228	S55 and @ad<"20111215"	US- PGPUB;	OR	OFF	2014/03/12 16:53

			USPAT			
S57	3109	S52 with generat\$3	US-PGPUB; USPAT	OR	OFF	2014/03/12 16:55
S58	290	S57 and "713"/3\$.cls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 16:55
S59	270	S58 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 16:56
S60	2709	(balanc\$3 or budget\$3 or allocat\$5 or shift\$5 or transfer\$5) and S57	US-PGPUB; USPAT	OR	OFF	2014/03/12 16:59
S61	232	S60 and "713"/3\$.cls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 16:59
S62	212	S61 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:00
S63	803	S52 with (dedicat\$3 or own or separat\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:06
S64	46	S63 and "713"/3\$.cls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:07
S65	40515	frequenc\$3 with differ\$5 with power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:47
S66	2199	"same" near3 frequenc\$3 with differ\$5 with power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:47
S67	670	"same" near3 frequenc\$3 with differ\$5 near3 power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:48
S68	563	"same" near3 frequenc\$3 with different near3 power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:48
S69	16	S67 same (bus or buses or core\$1 or processor\$1 or CPU\$1 or GPU\$1)	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:49
S70	228	"same" adj2 frequenc\$3 with different adj2 power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:52
S71	8	S70 and "713"/3\$.cls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:53
S72	893	naffziger	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:54
S73	202	naffziger-sam\$.in.	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:55
S74	37	S73 and "713"/3\$.cls.	US-PGPUB; USPAT	OR	OFF	2014/03/12 17:55
S75	1178	clock\$5 near5 relat\$5 near5 power\$1	US-PGPUB;	OR	OFF	2014/03/13 09:23

			USPAT			
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S77	223	S75 and "713"/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:23
S78	17090	bus near2 (clock\$1)	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:25
S79	2203	"same" near3 frequenc\$3 with differ\$5 with power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:25
S80	0	S78 and S79	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:25
S81	202	naffziger-sam\$.in.	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:26
S82	4	S81 and S78	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:26
S83	40558	frequenc\$3 with differ\$5 with power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:27
S84	407	S78 and S83	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:28
S85	15882	frequenc\$3 near6 differ\$5 near4 power\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:28
S86	224	S78 and S85	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:28
S87	71	S86 and "713"/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 09:29
S88	75	relation\$5 near5 (CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/13 10:33
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S90	0	(revers\$3 ord invers\$3 or opposit\$3) near5 (relat\$3 or relation\$5) with (CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/13 10:50
S91	0	(revers\$3 ord invers\$3 or opposit\$3) near5 (relat\$3 or relation\$5 or ratio\$3) with (CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/13 10:50
S92	34	(revers\$3 ord invers\$3 or opposit\$3) near5 (relat\$3 or relation\$5 or ratio\$3) with (CPU or core\$1 or processor\$1) with	US-PGPUB; USPAT	OR	OFF	2014/03/13 10:51

		(frequenc\$3 or clock\$1) with (bus or buses)				
S93	432	(ratio\$3 or relat\$3 or relation\$5) near5 (CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/13 10:52
S94	69	S93 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 10:53
S95	499	(trad\$5 or transfer\$5 or exchang\$5) near5 (power or frequenc\$3) with (bus or buses) with (core\$1 or CPU\$1 or processor\$1)	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:18
S96	85	S95 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:19
S97	350	between near5 (CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:29
S98	35	S97 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:29
S99	52	(CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) near5 (bus or buses) near5 (factor\$1 or scal\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:36
S100	22935	between near5 (frequenc\$3 or clock\$1) near3 generat\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:54
S101	8617715	(ratio\$3 or relat\$3 or relation\$5 or factor\$3) between near5 (frequenc\$3 or clock\$1) near3 generat\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:55
S102	2866	(ratio\$3 or relat\$3 or relation\$5 or factor\$3) with between near5 (frequenc\$3 or clock\$1) near3 generat\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:56
S103	13	S102 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:56
S104	3678	between near5 (frequenc\$3 or clock\$1) near3 generat\$3 same power	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:58
S105	51	S104 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 11:58
S106	685	bus near2 (clock\$1) and clock\$3 near3 generators	US-PGPUB; USPAT	OR	OFF	2014/03/13 12:06
S107	74	S106 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 12:06
S108	363	bus near2 (clock\$1) and clock\$3 near3 generators and (balanc\$3 or budget\$3 or allocat\$5 or distribut\$5) same (power or frequenc\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/13 12:15
S109	58	S108 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 12:15
S110	4	bus near2 (clock\$1) and borrow\$3 near5	US-	OR	OFF	2014/03/13

		(frequenc\$3 or power\$1)	PGPUB; USPAT			12:28
S111	849	borrow\$3 near5 (frequenc\$3 or power\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:29
S112	10	(bus or buses) same borrow\$3 near5 (frequenc\$3 or power\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:30
S113	63	(bus or buses) same (borrow\$3 or lend\$3 or loan\$3) near5 (frequenc\$3 or power\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:31
S114	3698	(bus or buses) same (tak\$3) near5 (frequenc\$3 or power\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:38
S115	1127	(bus or buses) with (tak\$3) near3 (frequenc\$3 or power\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:38
S116	48	S115 and 713/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:39
S117	71	bus near5 (clock\$3 frequenc\$3 or power\$1) near5 every near5 (CPU or processor or core\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:42
S118	12	bus near5 (clock\$3 frequenc\$3 or power\$1) near5 every near5 (increas\$3 or decreas\$3)	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:45
S119	88	bus near2 (clock\$1) and clock\$3 near3 generators same power	US- PGPUB; USPAT	OR	OFF	2014/03/13 12:46
S120	22	bus near2 (clock\$1) near5 generators	US- PGPUB; USPAT	OR	OFF	2014/03/13 13:10
S121	659	bus near2 (clock\$1) near3 generator	US- PGPUB; USPAT	OR	OFF	2014/03/13 13:34
S122	102	S121 and 713/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 13:34
S123	176	compensat\$5 same bus near clock\$1	US- PGPUB; USPAT	OR	OFF	2014/03/13 14:24
S124	4	S123 and 713/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 14:24
S125	6	step\$5 near5 (increas\$3 or decreas\$3) same bus near clock\$1	US- PGPUB; USPAT	OR	OFF	2014/03/13 14:25
S126	775	power with bus near clock\$1	US- PGPUB; USPAT	OR	OFF	2014/03/13 14:27
S127	158	S126 and 713/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 14:27
S128	1560	power near5 bus near clock\$1	US- PGPUB; USPAT	OR	OFF	2014/03/13 14:27
S129	3214	(balanc\$3 or budget\$3 or allocat\$5 or	US-	OR	OFF	2014/03/13

		shift\$5 or transfer\$3 or distribut\$5) with (bus or buses) near2 clock\$1	PGPUB; USPAT			14:28
S130	266	S129 with power	US-PGPUB; USPAT	OR	OFF	2014/03/13 14:29
S131	21	S130 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 14:29
S132	2351	bottle\$1neck\$3 with bus	US-PGPUB; USPAT	OR	OFF	2014/03/13 14:44
S133	19	S132 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 14:44
S134	72022	(bottle\$1neck\$3 or jam\$3 or congest\$5 or hold\$1up or clog\$3 or block\$5) with bus	US-PGPUB; USPAT	OR	OFF	2014/03/13 14:59
S135	1417	S134 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 15:00
S136	4228	(bottle\$1neck\$3 or jam\$3 or congest\$5 or hold\$1up or clog\$3) with bus	US-PGPUB; USPAT	OR	OFF	2014/03/13 15:07
S137	42	S136 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 15:07
S138	256	(cap\$3 or limit\$3) with S136	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:18
S139	1	S138 and 713/3\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:19
S140	147	S138 and 7\$2/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:20
S141	6	S138 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:23
S142	419	S136 same (unnecessary or un\$1needed or wait\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:29
S143	99	S136 same (unnecessary or un\$1needed)	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:29
S144	5	S136 same (wast\$5) with wait\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:35
S145	18666	(cap\$3 or limit\$3) near3 bus	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:37
S146	242	S145 near3 frequenc\$3	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:38
S147	35	S146 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/13 16:38
S148	55	(cap\$3 or limit\$3) with over\$1load\$3	US-	OR	OFF	2014/03/13

		near5 bus	PGPUB; USPAT			16:57
S149	3	(cap\$3 or limit\$3) with flood\$3 near5 bus	US- PGPUB; USPAT	OR	OFF	2014/03/13 17:13
S150	265	(cap\$3 or limit\$3 or restrict\$3) near3 bus near3 frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/03/13 17:13
S151	41	S150 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 17:14
S152	1	("2003/0189945").URPN.	USPAT	OR	OFF	2014/03/13 17:53
S153	1	"20050060594"	USPAT	OR	OFF	2014/03/13 18:09
S161	1214	G06F9/50.cpc.	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:49
S162	686	G06F9/5094.cpc.	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:49
S163	14	(US-20100211707-\$ or US-20080117931-\$ or US-20070050653-\$ or US-20120079147-\$ or US-20060190649-\$ or US-20050060594-\$ or US-20050044442-\$ or US-20050044440-\$ or US-20030189945-\$).did. or (US-7949817-\$ or US-7606960-\$ or US-8543860-\$ or US-7865749-\$ or US-7206960-\$).did.	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:52
S164	1698	G06F1/08.cpc.	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:52
S165	9889	G06F1/3203.cpc.	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:52
S166	2669	G06F1/206.cpc.	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:52
S167	13	S161 and S162	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:55
S168	1	S161 and S164	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:55
S169	4	S161 and S166	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:55
S170	23	S161 and S165	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:55
S171	1	S162 and S164	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:58
S172	90	S162 and S166	US- PGPUB; USPAT	OR	OFF	2014/03/13 18:58
S173	275	S162 and S165	US-	OR	OFF	2014/03/13

			PGPUB; USPAT			18:58
S174	4	bus near3 work\$1load\$1 with threshold\$1	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:20
S175	1	bus near3 work\$1load\$1 with (max\$5 or limit\$3)	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:21
S176	24052	bus near3 (max\$5 or limit\$3 or threshold\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:22
S177	351	(bus or buses) with (activit\$3 or traffic\$3 or work\$1load\$1) near3 (max\$5 or limit\$3 or threshold\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:23
S178	317	S177 and @ad<"20111215"	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:25
S179	261	(bus or buses) near5 (activit\$3 or traffic\$3 or work\$1load\$1) near3 (max\$5 or limit\$3 or threshold\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:25
S180	197	(bus or buses) near3 (activit\$3 or traffic\$3 or work\$1load\$1) near3 (max\$5 or limit\$3 or threshold\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:25
S181	190	S180 and @ad<"20111215"	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:26
S182	218	(bus or buses) near3 (activit\$3 or traffic\$3 or work\$1load\$1) with frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:30
S183	45	S182 and 713/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:30
S184	7	(bus or buses) near3 (activit\$3 or traffic\$3 or work\$1load\$1) near3 (max\$5 or limit\$3 or threshold\$1) with frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:33
S185	1	(bus or buses) near3 (activit\$3 or traffic\$3 or work\$1load\$1) near5 (above or exceed\$3 or greater) with frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:34
S186	212	bus near3 work\$1load\$1	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:35
S187	7	S186 and 713/3\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/03/13 19:35
S189	3669	bus\$2 near2 (threshold\$1 or limit\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/26 11:40
S190	91	increas\$3 near3 bus\$2 near2 (threshold\$1 or limit\$1)	US- PGPUB; USPAT	OR	OFF	2014/03/26 11:41
S191	0	(decreas\$3 reduc\$3 or lower\$3) near3 bus\$2 near2 (threshold\$1 or limit\$1) with wait\$3	US- PGPUB; USPAT	OR	OFF	2014/03/26 12:18
S192	0	(decreas\$3 reduc\$3 or lower\$3) near3 bus\$2 near2 (threshold\$1 or limit\$1) with bottle\$5	US- PGPUB; USPAT	OR	OFF	2014/03/26 12:18

S193	10	bus\$2 near2 (threshold\$1 or limit\$1) with bottle\$5	US-PGPUB; USPAT	OR	OFF	2014/03/26 12:18
S194	359	(decreas\$3 reduc\$3 or lower\$3) near3 bus\$2 with wait\$3	US-PGPUB; USPAT	OR	OFF	2014/03/26 12:21
S195	291	(decreas\$3 reduc\$3 or lower\$3) near3 (bus or buses) with wait\$3	US-PGPUB; USPAT	OR	OFF	2014/03/26 12:22
S196	284	S195 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/03/26 12:22
S197	72	(decreas\$3 reduc\$3 or lower\$3) near3 (bus or buses) with wait\$3 with (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 14:45
S198	59	(decreas\$3 reduc\$3 or lower\$3) near3 (bus or buses) with wait\$3 near5 (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 14:54
S199	1817	(bus or buses) near5 wait\$3 near5 (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:08
S200	45	(decreas\$3 reduc\$3 or lower\$3) near3 (bus or buses) near5 wait\$3 near5 (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:08
S201	0	(cap\$3) near3 (bus or buses) near5 wait\$3 near5 (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:14
S202	22	(cap\$3) near3 (bus or buses) with (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:14
S203	519	bottle\$1neck\$3 near3 (bus or buses) with (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:16
S204	2800	(bottle\$1neck\$3 or hold\$3 or jam\$3 or obstacl\$3) near5 (core\$1 or GPU\$1 or CPU\$1 or process\$3) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:18
S205	24	S204 with frequenc\$3	US-PGPUB; USPAT	OR	OFF	2014/03/26 15:18
S206	182	(bus or buses) near2 cap\$3	US-PGPUB; USPAT	OR	OFF	2014/03/27 16:59
S207	94	bus near3 exchange near5 (frequenc\$3 or power)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:22
S208	42	bus near3 exchange near5 (allocat\$5 or distribut\$5)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:25
S209	1654	bus near2 waiting	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:31
S210	318	S209 with (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:31
S211	27	S210 and "713"/\$.ccls.	US-PGPUB;	OR	OFF	2014/03/27 18:31

			USPAT			
S212	66463	wait\$3 near2 (core\$1 or GPU\$1 or CPU\$1 or process\$3)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:33
S213	460	S212 with frequenc\$3	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:33
S214	127	S213 and "713"/\$.ccls.	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:33
S215	97	S214 and (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:34
S216	30	S213 same (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:35
S217	2260	(halt\$3 or stall\$3) near2 (core\$1 or GPU\$1 or CPU\$1 or process\$3) same (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:40
S218	50	(halt\$3 or stall\$3) near2 (core\$1 or GPU\$1 or CPU\$1 or process\$3) with frequenc\$3 same (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:41
S219	3	bus with until near3 (core\$1 or GPU\$1 or CPU\$1 or process\$3) near3 finish\$3 with frequenc\$3	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:47
S220	16	bus with until near3 (core\$1 or GPU\$1 or CPU\$1 or process\$3) with frequenc\$3	US-PGPUB; USPAT	OR	OFF	2014/03/27 18:47
S221	62	(zero\$1sum or zero\$3 near3 sum\$3) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 14:18
S222	10	frequenc\$4 with bid\$3 with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 15:46
S223	95	return\$3 near5 frequenc\$3 with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 15:48
S224	89	S223 and @ad<"20111215"	US-PGPUB; USPAT	OR	OFF	2014/04/02 15:50
S225	5795	parallel with bus with access\$3	US-PGPUB; USPAT	OR	OFF	2014/04/02 15:57
S226	102009	bus near5 over\$5	US-PGPUB; USPAT	OR	OFF	2014/04/02 16:01
S227	81	band\$3 near5 limit\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 16:04
S228	6248	(zero) near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 16:18
S229	1610	band\$5 near5 limit\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 16:33
S230	208	giv\$3 near5 frequenc\$5 near5 (bus or buses)	US-PGPUB;	OR	OFF	2014/04/02 16:37

			USPAT			
S231	735	band\$5 near5 utilizat\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 16:59
S232	46	work\$5 near3 plan\$3 with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:02
S233	22	work\$5 near3 (plans or plan or planning) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:02
S234	1658	pend\$3 near3 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:05
S235	713	idl\$3 near5 (core\$1 or processor\$1 or cpu\$1) with (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:07
S236	11	priorit\$3 near5 AGP near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:10
S237	48	priorit\$5 near5 frequenc\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:11
S238	0	willing\$3 near3 spar\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:37
S239	1042	spar\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/02 17:37
S240	0	demand near5 inactiv\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/03 10:32
S241	124	supply\$3 near5 demand\$3 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/03 10:33
S242	11	S241 same frequenc\$3	US-PGPUB; USPAT	OR	OFF	2014/04/03 11:31
S243	48	frequenc\$3 near5 (stall\$3 or wait\$3) near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/03 11:40
S244	4	("6519711" "6948086").PN. OR ("7640449").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2014/04/03 11:57
S245	771	power\$3 near3 sav\$4 near5 (bus or buses)	US-PGPUB; USPAT	OR	OFF	2014/04/03 16:19
S246	255	S245 and 713/3\$2.ccls.	US-PGPUB; USPAT	OR	OFF	2014/04/03 16:19
S247	154	bus near5 reach\$3 near2 threshold\$1	US-PGPUB; USPAT	OR	OFF	2014/04/04 10:14
S248	350	bus near5 broker\$3	US-PGPUB; USPAT	OR	OFF	2014/04/04 10:16
S249	949	balanc\$3 near3 bus	US-	OR	OFF	2014/04/04

			PGPUB; USPAT			10:19
S250	4387	bus near3 consum\$5	US- PGPUB; USPAT	OR	OFF	2014/04/04 10:30
S251	149	S250 with frequen\$5	US- PGPUB; USPAT	OR	OFF	2014/04/04 10:31
S252	1387	bus with lower\$3 near4 frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 10:47
S253	311	S252 and "713"/\$.cls.	US- PGPUB; USPAT	OR	OFF	2014/04/04 10:48
S254	166	bus with lower\$3 near4 power near4 frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 10:48
S255	71	S254 and "713"/\$.cls.	US- PGPUB; USPAT	OR	OFF	2014/04/04 10:48
S256	166	bus with lower\$3 near4 power near4 frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 11:37
S257	6261	power near2 budget\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 11:53
S258	48	S257 near5 bus	US- PGPUB; USPAT	OR	OFF	2014/04/04 11:53
S260	47	S258 and @ad<"20110101"	US- PGPUB; USPAT	OR	OFF	2014/04/04 11:54
S261	6	S258 same frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 11:56
S262	6261	power near2 budget\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 19:12
S263	48	S262 near5 bus	US- PGPUB; USPAT	OR	OFF	2014/04/04 19:12
S264	28	S263 and frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/04 19:12
S265	6261	power near2 budget\$3	US- PGPUB; USPAT	OR	OFF	2014/04/07 06:24
S266	48	S265 near5 bus	US- PGPUB; USPAT	OR	OFF	2014/04/07 06:24
S267	12	"5,758,133"	US- PGPUB; USPAT	OR	OFF	2014/04/10 14:26
S268	12	"5758133"	US- PGPUB; USPAT	OR	OFF	2014/04/10 14:26
S269	43	2007/0074011	US-	OR	OFF	2014/04/10

			PGPUB; USPAT			14:31
S270	0	"20070074011".app.	US- PGPUB; USPAT	OR	OFF	2014/04/10 14:31
S271	1	"20070074011".pn.	US- PGPUB; USPAT	OR	OFF	2014/04/10 14:31
S272	71	bus near5 too near5 slow	US- PGPUB; USPAT	OR	OFF	2014/04/15 15:42
S273	6	S272 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/04/15 16:47
S274	7	S272 same frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 16:47
S275	16	bus near5 bottle\$1neck\$1 with frequenc\$5	US- PGPUB; USPAT	OR	OFF	2014/04/15 16:54
S276	191	slow with bus with frequenc\$5	US- PGPUB; USPAT	OR	OFF	2014/04/15 18:46
S277	47	S276 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/04/15 18:46
S278	762	bus near5 limit\$3 with frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 18:49
S279	97	bus near5 slow with frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 18:49
S280	34	S279 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/04/15 18:50
S281	20	("3571806" "4670837" "5021679" "5218704" "5263172" "5416434" "5418969" "5430881" "5491814").PN. OR ("5758133").URPN.	US- PGPUB; USPAT; USOCR	OR	OFF	2014/04/15 18:52
S282	89	bus near5 (free\$3 or sav\$3) near5 frequenc\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 18:53
S283	137	bus near5 frequenc\$3 with wait\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 19:28
S284	23	S283 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/04/15 19:28
S285	1	bus near5 bottle\$1neck\$1 with frequenc\$5 with wait\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 19:33
S286	106	bus near5 slow with wait\$3	US- PGPUB; USPAT	OR	OFF	2014/04/15 19:34
S287	9	S286 and "713"/\$.ccls.	US- PGPUB; USPAT	OR	OFF	2014/04/15 19:34

EAST Search History

S288	28	bus near5 frequenc\$5 with waiting	US-PGPUB; USPAT	OR	OFF	2014/04/15 19:38
S289	71	bus near5 too near5 slow	US-PGPUB; USPAT	OR	OFF	2014/04/16 10:53

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S154	12553	bus near5 clock\$1	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:17
S155	506	S154 and 713/3\$.ccls.	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:17
S156	1	(borrow\$3 or lend\$3 or loan\$3) near5 frequenc\$3 with bus	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:18
S157	14	(borrow\$3 or lend\$3 or loan\$3) near5 power with frequenc\$3	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:19
S158	24	relation\$5 near5 (CPU or core\$1 or processor\$1) near3 (frequenc\$3 or clock\$1) near5 (bus or buses)	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:21
S159	18	(revers\$3 ord invers\$3 or opposit\$3) near5 (relat\$3 or relation\$5 or ratio\$3) with (CPU or core\$1 or processor\$1) with (frequenc\$3 or clock\$1) with (bus or buses)	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:24
S160	18	(revers\$3 or invers\$3 or opposit\$3) near5 (relat\$3 or relation\$5 or ratio\$3) with (CPU or core\$1 or processor\$1) with (frequenc\$3 or clock\$1) with (bus or buses)	US-PGPUB; UPAD	OR	OFF	2014/03/13 18:24
S188	1	"Term Removed"	US-PGPUB	OR	OFF	2014/03/13 18:52

4/ 17/ 2014 2:27:13 PM

C:\ Users\ dchan\ Documents\ EAST\ Workspaces\ 13398641\ 13398641 amendment.wsp

Search Notes 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 1/08, 1/3203, 1/206	3/13/2014	DC
G06F 9/50, 9/5094	3/13/2014	DC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300	9/27/2013	DC
713	320	9/27/2013	DC
713	300	4/17/2014	DC
713	320	4/17/2014	DC

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Search - PALM	9/26/2013	DC
Text Search - EAST; PGPUB; USPAT	9/26/2013	DC
IDS - EAST: PGPUB; USPAT	9/27/2013	DC
Updated Text Search - EAST (PGPUB; USPAT)	4/17/2014	DC
IDS - EAST (PGPUB; USPAT)	4/17/2014	DC

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

JUN 16 2014

Applicants:	Schluessler, et al.	§	Group Art Unit:	2115
		§		
Serial No.:	13/398,641	§	Conf. No.:	1050
		§		
Filed:	February 16, 2012	§	Examiner:	Chan, Danny
		§		
		§	Atty. Dkt. No.:	ITL3139P1US
		§		(P38525X)
		§		
For:	Method, Apparatus, And System For	§		
	Energy Efficiency And Energy	§		
	Conservation Including Power And	§		
	Performance Workload-Based Balancing	§		
	Between Multiple Processing Elements	§		
	And/Or A Communication Bus (As	§		
	Amended)	§		

Via Facsimile: 571-270-6134

AGENDA FOR TELEPHONE INTERVIEW OF JUNE 16, 2014

- I. Barr Does Not Disclose Integrated Circuit-Internal Thermal Control;
 - a. Barr is simply directed to system level control
 - b. Barr fails to disclose integrated circuit power limit, or maximum thermal dissipation capacity
 - c. Barr fails to disclose dynamic tuning of power allocation between core and communication bus

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JUN 16 2014

TROP, PRUNER & HU, P.C.

INTELLECTUAL PROPERTY LAW ATTORNEYS

7320 N. MoPac Expy., Suite 307
Austin, Texas 78731
Bus: (512) 418-9944
Fax: (512) 418-0544**Fax****To:** Examiner Danny Chan**From:** Mark J. Rozman
Reg. No. 42,117**Company:** USPTO**Date:** June 15, 2014**Fax:** (571) 270-6134**Pages:** 2 including cover sheet**Re:** 13/398,641**Our Re:** IT>3139P1US(P38525X)☐ Urgent ☒ For Review ☐ Please Comment ☐ Please Reply ☒ Confirm

Receipt

◆ **Notice:** This information is intended to be for the use of the individual or entity named on this transmittal sheet. If you are not the intended recipient, be aware that any disclosure, copying, distribution, or use of the contents of this faxed information is prohibited. If you have received this facsimile in error, please notify the sender by telephone immediately so that arrangements can be made for the retrieval of the original document at no cost to you.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	ITL.3139P1US (P38525X)	1050
47795 7590 06/23/2014 TROP, PRUNER & HU, P.C. 1616 S. VOSS RD., SUITE 750 HOUSTON, TX 77057-2631			EXAMINER CHAN, DANNY	
			ART UNIT 2115	PAPER NUMBER
			MAIL DATE 06/23/2014	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

<i>Applicant-Initiated Interview Summary</i>	Application No.	Applicant(s)	
	13/398,641	SCHLUESSLER ET AL.	
	Examiner	Art Unit	
	DANNY CHAN	2115	

All participants (applicant, applicant's representative, PTO personnel):

(1) DANNY CHAN. (3) Mark J. Rozman (Reg. no. 42117).

(2) Thomas Lee. (4) ____.

Date of Interview: 17 June 2014.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: ____.

Issues Discussed ☐ 101 ☐ 112 ☒ 102 ☐ 103 ☐ Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: Barr et al. (PGPUB 2005/0060594).

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Applicant's representative discussed claim 1 and the reference used in the 102 rejection. An agreement could not be made, but examiners indicated that the other independent claims are closer to a condition for allowance than claim 1.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/DANNY CHAN/ Examiner, Art Unit 2115	
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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Request for Continued Examination (RCE) Transmittal

Address to:
Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	13/398,641
Filing Date	2012-02-16
First Named Inventor	Travis T. Schluessler
Art Unit	2115
Examiner Name	Danny Chan
Attorney Docket Number	ITL3139P1US (P38525X)

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. **Submission required under 37 CFR 1.114** Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

- a. ☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.
- i. ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ii. ☐ Other _____
- b. ☒ Enclosed
- i. ☒ Amendment/Reply
- iii. ☐ Information Disclosure Statement (IDS)
- ii. ☐ Affidavit(s)/ Declaration(s)
- iv. ☐ Other _____

2. Miscellaneous

- a. ☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)
- b. ☐ Other _____

3. Fees

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to

- a. ☒ Deposit Account No. 20-1504
- i. ☒ RCE fee required under 37 CFR 1.17(e)
- ii. ☐ Extension of time fee (37 CFR 1.136 and 1.17)
- iii. ☒ Other any additional fees
- b. ☐ Check in the amount of \$ _____ enclosed
- c. ☒ Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	/Mark J. Rozman/	Date	2014-07-18
Name (Print/Type)	Mark J. Rozman	Registration No.	42117

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature	Filed Via EFS	Date	
Name (Print/Type)			

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Instruction Sheet for RCEs

(not to be submitted to the USPTO)

NOTES:

An RCE is not a new application, and filing an RCE will not result in an application being accorded a new filing date.

Filing Qualifications:

The application must be a utility or plant application filed on or after June 8, 1995. The application cannot be a provisional application, a utility or plant application filed before June 8, 1995, a design application, or a patent under reexamination. See 37 CFR 1.114(e).

Filing Requirements:

Prosecution in the application must be closed. Prosecution is closed if the application is under appeal, or the last Office action is a final action, a notice of allowance, or an action that otherwise closes prosecution in the application (e.g., an Office action under *Ex parte Quayle*). See 37 CFR 1.114(b).

A submission and a fee are required at the time the RCE is filed. If reply to an Office action under 35 U.S.C. 132 is outstanding (e.g., the application is under final rejection), the submission must meet the reply requirements of 37 CFR 1.111. If there is no outstanding Office action, the submission can be an information disclosure statement, an amendment, new arguments, or new evidence. See 37 CFR 1.114(c). The submission may be a previously filed amendment (e.g., an amendment after final rejection).

WARNINGS:

Request for Suspension of Action:

All RCE filing requirements must be met before suspension of action is granted. A request for a suspension of action under 37 CFR 1.103(c) does not satisfy the submission requirement and does not permit the filing of the required submission to be suspended.

Improper RCE will NOT toll Any Time Period:

Before Appeal - If the RCE is improper (e.g., prosecution in the application is not closed or the submission or fee has not been filed) and the application is not under appeal, the time period set forth in the last Office action will continue to run and the application will be abandoned after the statutory time period has expired if a reply to the Office action is not timely filed. No additional time will be given to correct the improper RCE.

Under Appeal - If the RCE is improper (e.g., the submission or the fee has not been filed) and the application is under appeal, the improper RCE is effective to withdraw the appeal. Withdrawal of the appeal results in the allowance or abandonment of the application depending on the status of the claims. If there are no allowed claims, the application is abandoned. If there is at least one allowed claim, the application will be passed to issue on the allowed claim(s). See MPEP 1215.01.

See MPEP 706.07(h) for further information on the RCE practice.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13398641		
Filing Date:		16-Feb-2012		
Title of Invention:		Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus		
First Named Inventor/Applicant Name:		Travis T. Schluessler		
Filer:		Mark J. Rozman/Stephanie Petreas		
Attorney Docket Number:		ITL.3139P1US (P38525X)		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt	
EFS ID:	19624780
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Method, Apparatus, and System for Energy Efficiency and Energy Conservation Including Power and Performance Balancing Between Multiple Processing Elements and/or a Communication Bus
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	47795
Filer:	Mark J. Rozman/Stephanie Petreas
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.3139P1 US (P38525X)
Receipt Date:	18-JUL-2014
Filing Date:	16-FEB-2012
Time Stamp:	17:54:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1200
RAM confirmation Number	4052
Deposit Account	201504
Authorized User	ROZMAN, MARK J.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment Submitted/Entered with Filing of CPA/RCE	ITL3139P1USRCE.pdf	134410	no	10
			39f599f713c2a557beff4a2e038c94ed793fb209		
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	ITL3139P1USReqtoCorrectPriorityClaim.pdf	86309	no	2
			d512b0fbc90e2f5b9fdb25781bad0e920feb019		
Warnings:					
Information:					
3	Application Data Sheet	ITL3139P1USRevisedADSToFile.pdf	694917	no	6
			ca2af2d8a6976105e0d298cff81a829d9f38b024		
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
4	Request for Continued Examination (RCE)	ITL3139P1USRCETransToFile.pdf	193224	no	3
			047c45280d7c12927d33dc9b3fd787946f7ace2b		
Warnings:					
This is not a USPTO supplied RCE SB30 form.					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30827	no	2
			90969e8554df5d8c9b66cac9a7728269bf317b4		
Warnings:					
Information:					
Total Files Size (in bytes):			1139687		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Schluessler, et al.	§	Group Art Unit:	2115
		§		
Serial No.:	13/398,641	§	Conf. No.:	1050
		§		
Filed:	February 16, 2012	§	Examiner:	Chan, Danny
		§		
		§	Atty. Dkt. No.:	ITL.3139P1US
		§		(P38525X)
		§		
For:	Method, Apparatus, And System For	§		
	Energy Efficiency And Energy	§		
	Conservation Including Power And	§		
	Performance Workload-Based Balancing	§		
	Between Multiple Processing Elements	§		
	And/Or A Communication Bus (As	§		
	Amended)	§		

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT SUBMITTED WITH RCE

Sir:

This paper is submitted in conjunction with the enclosed Request for Continuing Examination (RCE) in the above-identified Patent Application. Further examination and reconsideration are respectfully requested in view of the Amendments and Remarks set forth below.

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims begin on page 3 of this paper.

Remarks/Arguments begin on page 8 of this paper.

Amendments to the Specification:

Please add the following paragraph before paragraph 1 on page 1:

This application is a continuation-in-part of United States Patent Application Serial No. 13/327,670, filed December 15, 2011, the content of which is hereby incorporated by reference.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) ~~An apparatus for efficient energy consumption~~ A processor comprising:

an integrated circuit including[[,]]:

a first core;

a cache memory;

a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;

a core workload monitor configured to determine a core workload for the first core;

a bus workload monitor configured to determine a bus workload for the communication bus; and

balancing control adapted to receive the bus workload from the bus workload monitor and to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit, wherein a power consumption of one of the first core and the communication bus is to be reduced, the power consumption reduction to be limited to maintain operation of the one of the first core and the communication bus above a low limit.

2. (Currently Amended) The ~~apparatus~~ processor of claim 1, further comprising a second core and a second core workload monitor configured to determine a second core workload for the second core, wherein the first core includes a host processing core, the second core includes a graphics processing core, and the communication bus includes a ring interconnect, and wherein the balancing control is further adapted to dynamically tune power allocation between the first core, the second core, and the communication bus based on the power limit and at least the bus workload, the core workload, and the second core workload.

3. (Canceled)

4. (Currently Amended) The ~~apparatus~~ processor of claim 1, wherein the balancing control, in response to the integrated circuit operating at the power limit, being adapted to:

increase frequency for the communication bus and cap frequency for the first core in response to the bus workload being greater than the bus workload threshold;

and

decrease frequency for the communication bus and increase the frequency for the first core in response to the bus workload being less than the bus workload threshold.

5. (Canceled)

6. (Currently Amended) A non-transitory storage medium including code, when executed, to cause a machine to perform the energy efficiency operations of:

receiving a bus workload for a communication bus and a first processing element workload for a first processing element based on an integrated circuit reaching a limit, the integrated circuit including the communication bus and the first processing element, wherein the communication bus is to connect the first processing element with at least one other device of the integrated circuit reaching a limit;

determining if the first processing element workload indicates the first processing element is a performance bottleneck;

determining if ~~[[a]]~~ the communication bus is able to accommodate the bus workload;

capping a bus frequency of at least the communication bus and a frequency of a second processing element in response to determining the first processing element workload indicates the first processing element is ~~[[a]]~~ the performance bottleneck and determining the communication bus is able to accommodate the bus workload; and

increasing a previous cap on the bus frequency of at least the communication bus in response to determining the first processing element workload indicates the first processing element is ~~[[a]]~~ the performance bottleneck and determining the communication bus is not able to accommodate the bus workload.

7. (Previously Presented) The non-transitory storage medium of claim 6, wherein the first processing element includes one or more graphics cores, the second processing element includes one or more processor cores, the communication bus includes a ring interconnect, and wherein the code includes privileged level power service code.

8. (Currently Amended) The non-transitory storage medium of claim 7, wherein the code, when executed, further causes the machine to perform the operations of:

increasing a previous cap on a frequency for the one or more processor ~~[[core]]~~ cores in response to determining the one or more graphics cores is not a performance bottleneck;

capping the frequency for the one or more processor cores in response to determining the first processing element workload indicates the first processing element is ~~[[a]]~~ the performance ~~bottle-neck~~ bottleneck and determining the communication bus is able to accommodate the bus workload.

9. (Previously Presented) The non-transitory storage medium of claim 6, wherein the limit includes a thermal design power limit.

10. (Currently Amended) A method ~~for efficient energy consumption~~ comprising:
determining a processing workload activity for a central processor on a package;
determining a graphics workload activity for a graphics processor on the package;
determining a bus workload activity for a communication bus on the package;
determining if the package has reached a thermal or power limit; ~~[[and]]~~
communicating the processing workload activity, the graphics workload activity and the bus workload activity to a power controller of the package; and

in response to determining the package has reached the thermal or power limit, dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity, including adjusting a maximum allowed frequency for the communication bus by a plurality of steps and adjusting a maximum allowed frequency for the central processor by a step.

11. (Currently Amended) The method of claim 10, wherein dynamically balancing power between the central processor, the graphics processor, and the communication bus based on at least the graphics workload activity and the bus workload activity comprises:

determining if the graphics workload activity is greater than a graphics activity threshold;
determining if there is sufficient room on the communication bus based on the bus workload activity in response to determining the graphics workload activity is greater than a threshold;

increasing the maximum allowed frequency for the communication bus in response to determining there is not sufficient room on the communication bus; and

decreasing ~~[[a]]~~ the maximum allowed frequency for the communication bus in response to determining there is sufficient room on the communication bus.

12. (Original) The method of claim 10, wherein the method is performed in response to execution of privileged level power service code.

13. (Original) The method of claim 11, wherein the method is performed in response to execution of privileged level power service code.

14. (Currently Amended) The ~~apparatus~~ processor of claim 1, wherein the balancing control is to receive a hint regarding a future workload and to dynamically tune the power allocation further based on the hint.

15. (Currently Amended) The ~~apparatus~~ processor of claim 2, wherein the balancing control is to increase a frequency of the second core and to reduce a frequency of the first core when the second core is to execute a producer thread and the first core is to execute a consumer thread to consume information produced by the producer thread.

16. (Currently Amended) The ~~apparatus~~ processor of claim 4, wherein the balancing control is to increase the communication bus frequency by a different amount than the first core frequency decrease.

17. (Currently Amended) The ~~apparatus~~ processor of claim 4, wherein the balancing control is to further increase frequency for a second core, the second core and the communication bus having power planes tied together.

18. (Previously Presented) The non-transitory storage medium of claim 6, wherein the code, when executed further causes the machine to perform the operations of receiving a hint regarding a future workload and dynamically tuning power allocation between the first processing element and the second processing element based on the hint.

19. (Previously Presented) The non-transitory storage medium of claim 7, wherein the code, when executed, further causes the machine to perform the operations of increasing the frequency of the second processing element and reducing the frequency of the first processing element when the second processing element is to execute a producer thread and the first processing element is to execute a consumer thread to consume information produced by the producer thread.

20. (Previously Presented) The non-transitory storage medium of claim 19, wherein the code, when executed, further causes the machine to perform the operations of increasing the communication bus frequency by a different amount than an amount by which the frequency of the first processing element is decreased.

REMARKS/ARGUMENTS

By way of the above amendment, priority is set forth to confirm that the pending application is in fact a continuation-in-part of U.S. Serial No. 13/327,670.

Claims 1, 4, 10-14, 16-17 and 20 stand rejected under 35 U.S.C. §102(b) over U.S. Publication No. 2005/0060594 (Barr). Applicants respectfully traverse the rejection. Regarding claim 1, Barr fails to anywhere disclose or even suggest the arrangement in the claim in which a processor comprises an integrated circuit that includes, *inter alia*, a first core, a cache memory and a communication bus to connect the core and the cache memory. Instead, Barr is simply directed to an overall computer system that has a PCI bus 110 that couples peripheral devices to an IO adapter.

Next, the Office Action contends that Barr meets the recited bus workload manager by the disclosure of a frequency manager 158. However, all that this frequency manager does is to query system devices for information and control clock signals generated on a PCI bus and memory bus. Barr, paragraph 41. Nonetheless, this has nothing to do with the subject matter in the claim of a processor internal bus workload monitor configured to determine a bus workload for the above-recited communication bus.

The rejection is further overcome, in that nothing in Barr anywhere discloses or suggests that a balancing control be configured such that a power consumption reduction to one of a core and a bus is to be limited to maintain operation of the limited component above a low limit. Nowhere in Barr is there disclosure or even suggestion of this low limit maintenance. Support for this amendment can be found in the original Specification, e.g., at paragraph 78. For all these reasons, claim 1 and the claims depending therefrom are patentable over the cited art.

Independent claim 10 is patentable for at least similar reasons in light of Barr's failure to disclose or even suggest the arrangement of a package including a central processor, a graphics processor and a communication bus, along with a power controller. Still further, the rejection is overcome, in that Barr fails to anywhere disclose or even suggest that a maximum allowed frequency for the communication bus be adjusted by multiple steps and a maximum allowed frequency for the central processor be adjusted by a step. Here, the mere selection of a high clock frequency to some devices and no clock frequency to other devices fails to meet the recited method for adjusting maximum allowed frequency with multiple steps for a communication bus and adjusting maximum allowed frequency by a step for a central processor.

Claims 6-7 and 19 stand rejected under 35 U.S.C. §102(e) over U.S. Publication No. 2011/0310413 (Nakao). Applicants respectfully traverse the rejection. Regarding claim 6, Nakao fails to teach or suggest the arrangement of the claim 6 subject matter, where an integrated circuit includes a communication bus and a processing element. Rather, the Nakao system is instead an image processing apparatus, namely a copy machine. Furthermore, nowhere in Nakao is there any teaching or suggestion of the recited bus workload receipt and processing element workload receipt. Instead, all that Nakao teaches is that control of a bus operating frequency or CPU operating frequency is based on conversion times of intermediate data into raster data. Nonetheless, this is not either of a bus workload or processing element workload that indicates that either the processing element is a performance bottleneck or whether the communication bus is able to accommodate a workload. Nor is there any disclosure or even suggestion in the reference that in one instance the communication bus frequency and a second processing element frequency be capped and a previous cap on bus frequency be increased in another condition. Instead, as discussed above the CPU operating frequency control is simply based on conversion time processing. Accordingly, claim 6 and the claims depending therefrom are patentable over the cited art.

STATEMENT OF SUBSTANCE OF THE INTERVIEW

The undersigned gratefully thanks the Examiner for the time and courtesy extended during the telephonic interview which occurred on June 16, 2014.

While agreement was not reached, it is believed that the above amendment is sufficient to place the application in condition for allowance. Furthermore, the undersigned agrees with the comments provide in the Applicant-Initiated Interview Summary form mailed by the Examiner on June 23, 2014.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Date: July 18, 2014

Respectfully submitted,
/Mark J. Rozman/
Mark J. Rozman
Registration No. 42,117
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Customer No.: 47795

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Schluessler, et al.	§	Group Art Unit:	2115
		§		
Serial No.:	13/398,641	§	Conf. No.:	1050
		§		
Filed:	February 16, 2012	§	Examiner:	Chan, Danny
		§		
		§	Atty. Dkt. No.:	ITL.3139P1US
		§		(P38525X)
For:	Method, Apparatus, And System For	§		
	Energy Efficiency And Energy	§		
	Conservation Including Power And	§		
	Performance Workload-Based Balancing	§		
	Between Multiple Processing Elements	§		
	And/Or A Communication Bus (As	§		
	Amended)	§		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST TO CORRECT PRIORITY CLAIM

Sir:

Applicants hereby request to correct the priority claim as listed on the Application Data Sheet filed with the application. The correction is as follows:

This case is a CONTINUATION-IN-PART, not a continuation.

A revised Application Data Sheet is enclosed herewith noting this correction. Please correct the priority claim as such.

Issuance of a corrected Official Filing Receipt is also respectfully requested.

It is believed that pursuant to M.P.E.P. §211.03 that no fee or petition is needed for correcting the timely submitted benefit claim. However, the Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 20-1504.

Respectfully submitted,

Date: July 18, 2014

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1						Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	Travis	T.	Schluessler				
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Hillsboro	State/Province	OR	Country of Residence	US		
Mailing Address of Inventor:							
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Address 2							
City	Hillsboro	State/Province	OR				
Postal Code	97123	Country	US				
Inventor 2						Remove	
Legal Name							
Prefix	Given Name	Middle Name	Family Name	Suffix			
	Russell	J.	Fenger				
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service							
City	Beaverton	State/Province	OR	Country of Residence	US		
Mailing Address of Inventor:							
Address 1	8697 SW 168th Avenue						
Address 2							
City	Beaverton	State/Province	OR				
Postal Code	97007	Country	US				
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add							

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		

☐ An Address is being provided for the correspondence information of this application.

Customer Number	~~59796~~ <u>47795</u>	
Email Address		Add Email Remove Email

Application Information:

Title of the Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		
Attorney Docket Number	~~P38525X~~ <u>IN 3139P/US (P 38525X)</u>	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	10	Suggested Figure for Publication (if any)	

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	~~59796~~ <u>47795</u>		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of <u>Continuation in part</u>	13327670	2011-12-15
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove			
Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. ☐ NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.
--

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices
--

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

- | | | |
|---|--|--------------------------------------|
| ☐ Assignee | ☐ Legal Representative under 35 U.S.C. 117 | ☐ Joint Inventor |
| ☐ Person to whom the inventor is obligated to assign. | ☐ Person who shows sufficient proprietary interest | |

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☐

Prefix	Given Name	Middle Name	Family Name	Suffix

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		

Mailing Address Information For Applicant:			
Address 1			
Address 2			
City		State/Province	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.				
Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee Data may be generated within this form by selecting the Add button.				

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	P38525X
		Application Number	
Title of Invention	A Method, Apparatus, And System For Energy Efficiency And Energy Conservation Including Power And Performance Balancing Between Multiple Processing Elements And/Or A Communication Bus		

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature	/Mark J. Rozman/			Date (YYYY-MM-DD)	2014-07-18
First Name	Mark	Last Name	Rozman	Registration Number	42117
Additional Signature may be generated within this form by selecting the Add button.					

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number		Filing Date		☐ To be Mailed	
Substitute for Form PTO-875				13/398,641		02/16/2012			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR	NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL					
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	07/18/2014	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 18	Minus	** 20	= 0	X \$80 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE						0			
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE									
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

47795 7590 07/30/2014
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

EXAMINER

CHAN, DANNY

ART UNIT

PAPER NUMBER

2115

DATE MAILED: 07/30/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	ITL3139P1US (P38525X)	1050

TITLE OF INVENTION: Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	10/30/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

47795 7590 07/30/2014
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	ITL3139P1US (P38525X)	1050

TITLE OF INVENTION: Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	10/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHAN, DANNY	2115	713-320000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	ITL3139P1US (P38525X)	1050
47795	7590	07/30/2014	EXAMINER	
TROP, PRUNER & HU, P.C.			CHAN, DANNY	
1616 S. VOSS RD., SUITE 750			ART UNIT	
HOUSTON, TX 77057-2631			PAPER NUMBER	

2115

DATE MAILED: 07/30/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/398,641	Applicant(s) SCHLUESSLER ET AL.	
	Examiner DANNY CHAN	Art Unit 2115	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the communication filed on July 18, 2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1,2,4 and 6-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☐ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/DANNY CHAN/ Examiner, Art Unit 2115	/THOMAS LEE/ Supervisory Patent Examiner, Art Unit 2115
---	--

DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Pursuant to MPEP 606.01, the title has been changed to read:

-- Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached --

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DANNY CHAN whose telephone number is (571)270-5134. The examiner can normally be reached on Monday-Friday, 8AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 5712723667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Art Unit: 2115

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/DANNY CHAN/
Examiner, Art Unit 2115

/THOMAS LEE/
Supervisory Patent Examiner, Art Unit 2115

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	"13398641"	US-PGPUB; USPAT	OR	OFF	2014/07/26 21:42
L2	744	bus near5 shar\$3 near3 power	US-PGPUB; USPAT	OR	OFF	2014/07/26 21:46
L3	46	bus adj3 too adj slow	US-PGPUB; USPAT	OR	OFF	2014/07/26 21:49
L4	9157	713/300.ccls.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:04
L5	6056	713/320.ccls.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:04
L6	1774	G06F1/08.cpc.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:05
L7	10177	G06F1/3203.cpc.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:05
L8	637	G06F1/3206.cpc.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:05
L9	1200	G06F9/50.cpc.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:05
L10	793	G06F9/5094.cpc.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:05
L11	35	Schluessler-Travis.in.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:09
L12	37	Schluessler-Travis-\$.in.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:09
L13	35	Fenger-Russell-J.in.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:09
L14	35	Fenger-Russell-\$.in.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:10
L15	105	11 12 13 14	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:10
L16	2	15 and workload adj monitor.clm.	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:10
L29	876	(balanc\$3 or budget\$3) near5 between near5 core\$1	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:27
L30	30	power near3 (balanc\$3 or budget\$3) near5 between near5 core\$1	US-PGPUB; USPAT	OR	OFF	2014/07/26 22:32

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L17	4704	G06F1/3203.cpc.	USPAT; UPAD	OR	OFF	2014/07/26 22:24
L18	158	G06F1/3206.cpc.	USPAT; UPAD	OR	OFF	2014/07/26 22:24

EAST Search History

L19	457	G06F9/50.cpc.	USPAT; UPAD	OR	OFF	2014/07/26 22:24
L20	270	G06F9/5094.cpc.	USPAT; UPAD	OR	OFF	2014/07/26 22:24
L21	5363	713/300.ccls.	USPAT; UPAD	OR	OFF	2014/07/26 22:24
L22	4202	713/320.ccls.	USPAT; UPAD	OR	OFF	2014/07/26 22:24
L23	13	Schluessler-Travis.in.	USPAT; UPAD	OR	OFF	2014/07/26 22:26
L24	12	Schluessler-Travis-\$.in.	USPAT; UPAD	OR	OFF	2014/07/26 22:26
L25	14	Fenger-Russell-J.in.	USPAT; UPAD	OR	OFF	2014/07/26 22:26
L26	14	Fenger-Russell-\$.in.	USPAT; UPAD	OR	OFF	2014/07/26 22:26
L27	30	bus adj3 too adj slow	USPAT; UPAD	OR	OFF	2014/07/26 22:26
L28	454	(balanc\$3 or budget\$3) near5 between near5 core\$1	USPAT; UPAD	OR	OFF	2014/07/26 22:27
L31	9	power near3 (balanc\$3 or budget\$3) near5 between near5 core\$1	USPAT; UPAD	OR	OFF	2014/07/26 22:35

7/26/2014 10:36:32 PM

C:\Users\dchan\Documents\EAST\Workspaces\13398641\13398641 rce.wsp



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BIB DATA SHEET

CONFIRMATION NO. 1050

SERIAL NUMBER 13/398,641	FILING or 371(c) DATE 02/16/2012 RULE	CLASS 713	GROUP ART UNIT 2115	ATTORNEY DOCKET NO. ITL.3139P1US (P38525X)		
APPLICANTS INVENTORS Travis T. Schluessler, Berthoud, CO; Russell J. Fenger, Beaverton, OR; ** CONTINUING DATA ***** This application is a CON of 13/327,670 12/15/2011 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 02/29/2012						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/DANNY CHAN/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CO	SHEETS DRAWINGS 10	TOTAL CLAIMS 13	INDEPENDENT CLAIMS 3
ADDRESS TROP, PRUNER & HU, P.C. 1616 S. VOSS RD., SUITE 750 HOUSTON, TX 77057-2631 UNITED STATES						
TITLE Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached						
FILING FEE RECEIVED 1380	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees		
				☐ 1.16 Fees (Filing)		
				☐ 1.17 Fees (Processing Ext. of time)		
				☐ 1.18 Fees (Issue)		
				☐ Other _____		
				☐ Credit		

Search Notes 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 1/08, 1/3203, 1/206	3/13/2014	DC
G06F 9/50, 9/5094	3/13/2014	DC
G06F 1/08, 1/3203, 1/206	7/26/2014	DC
G06F 9/50, 9/5094	7/26/2014	DC

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
713	300	9/27/2013	DC
713	320	9/27/2013	DC
713	300	4/17/2014	DC
713	320	4/17/2014	DC
713	320	7/26/2014	DC
713	300	7/26/2014	DC

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor Search - PALM	9/26/2013	DC
Text Search - EAST; PGPUB; USPAT	9/26/2013	DC
IDS - EAST: PGPUB; USPAT	9/27/2013	DC
Updated Text Search - EAST (PGPUB; USPAT)	4/17/2014	DC
IDS - EAST (PGPUB; USPAT)	4/17/2014	DC
Updated Text Search - EAST (PGPUB; USPAT)	7/26/2014	DC
Interference Search	7/26/2014	DC

INTERFERENCE SEARCH

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US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
713	320	7/26/2014	DC
713	300	7/26/2014	DC
G06F	1/3203, 1/3206	7/26/2014	DC
G06F	9/50, 9/5094	7/26/2014	DC

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<i>Index of Claims</i> 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant					☐ CPA					☐ T.D.					☐ R.1.47				
CLAIM		DATE																	
Final	Original	09/27/2013	04/17/2014	07/26/2014															
1	1	✓	✓	=															
2	2	✓	✓	=															
-	3	✓	-	-															
3	4	✓	✓	=															
-	5	✓	-	-															
4	6	✓	✓	=															
5	7	✓	✓	=															
6	8	✓	✓	=															
7	9	✓	✓	=															
8	10	✓	✓	=															
9	11	✓	✓	=															
10	12	✓	✓	=															
11	13	✓	✓	=															
12	14		✓	=															
13	15		✓	=															
14	16		✓	=															
15	17		✓	=															
16	18		✓	=															
17	19		✓	=															
18	20		✓	=															

Issue Classification 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.	
	Examiner DANNY CHAN	Art Unit 2115	

CPC					
Symbol				Type	Version
G06F		1	3203	F	2013-01-01
G06F		9	50	A	2013-01-01
G06F		9	5094	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

/DANNY CHAN/ Examiner.Art Unit 2115 (Assistant Examiner)	07/26/2014 (Date)	Total Claims Allowed: 18	
/THOMAS LEE/ Supervisory Patent Examiner.Art Unit 2115 (Primary Examiner)	07/28/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7

Issue Classification 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
713		320				G	0	6	F	1 / 32 (2006.01.01)									
CROSS REFERENCE(S)																			
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
713	300																		

/DANNY CHAN/ Examiner.Art Unit 2115 (Assistant Examiner)	07/26/2014 (Date)	Total Claims Allowed: 18	
/THOMAS LEE/ Supervisory Patent Examiner.Art Unit 2115 (Primary Examiner)	07/28/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7

Issue Classification 	Application/Control No. 13398641	Applicant(s)/Patent Under Reexamination SCHLUESSLER ET AL.
	Examiner DANNY CHAN	Art Unit 2115

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	15	17												
2	2	16	18												
-	3	17	19												
3	4	18	20												
-	5														
4	6														
5	7														
6	8														
7	9														
8	10														
9	11														
10	12														
11	13														
12	14														
13	15														
14	16														

/DANNY CHAN/ Examiner.Art Unit 2115 (Assistant Examiner)	07/26/2014 (Date)	Total Claims Allowed: 18	
/THOMAS LEE/ Supervisory Patent Examiner.Art Unit 2115 (Primary Examiner)	07/28/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 7



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
13/398,641	02/16/2012	2115	1380	ITL.3139P1US (P38525X)	13	3

CONFIRMATION NO. 1050

CORRECTED FILING RECEIPT



OC000000070771064

47795
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Date Mailed: 09/16/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Travis T. Schluessler, Berthoud, CO;
Russell J. Fenger, Beaverton, OR;

Applicant(s)

Travis T. Schluessler, Berthoud, CO;
Russell J. Fenger, Beaverton, OR;

Power of Attorney: The patent practitioners associated with Customer Number 47795

Domestic Priority data as claimed by applicant

This application is a CIP of 13/327,670 12/15/2011

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 02/29/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/398,641**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached

Preliminary Class

713

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

47795 7590 07/30/2014
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	02/16/2012	Travis T. Schluessler	ITL3139P1US (P38525X)	1050

TITLE OF INVENTION: Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	10/30/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHAN, DANNY	2115	713-320000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☒ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Trop. Pruner & Hu, P.C.
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.111. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Intel Corporation

Santa Clara, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☒ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 20-1504 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Mark J. Rozman/

Date 10-24-2014

Typed or printed name Mark J. Rozman

Registration No. 42,117

"FEE ADDRESS" INDICATION FORM

Address to:
Mail Stop M Correspondence
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fax to:
571-273-6500

- OR -

INSTRUCTIONS: The issue fee must have been paid for application(s) listed on this form. In addition, only an address represented by a Customer Number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. **When to check the first box below:** If you have a Customer Number to represent the fee address. **When to check the second box below:** If you have no Customer Number representing the desired fee address, in which case a completed Request for Customer Number (PTO/SB/125) must be attached to this form. For more information on Customer Numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

For the following listed application(s), please recognize as the "Fee Address" under the provisions of 37 CFR 1.363 the address associated with:



Customer Number:

00197

OR



The attached Request for Customer Number (PTO/SB/125) form.

PATENT NUMBER (if known)	APPLICATION NUMBER
	13/398,641

Completed by (check one):



Applicant/Inventor

/Mark J. Rozman/

Signature



Attorney or Agent of record 42,117
(Reg. No.)

Mark J. Rozman

Typed or printed name



Assignee of record of the entire interest. See 37 CFR 3.71.
Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

512-418-9944

Requester's telephone number



Assignee recorded at Reel _____ Frame _____

10-24-2014

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.



* Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.363. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 5 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND COMPLETED FORMS TO THIS ADDRESS.

SEND TO: Mail Stop M Correspondence, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		13398641		
Filing Date:		16-Feb-2012		
Title of Invention:		Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached		
First Named Inventor/Applicant Name:		Travis T. Schluessler		
Filer:		Mark J. Rozman/David Hopper		
Attorney Docket Number:		ITL.3139P1US (P38525X)		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	20510067
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	47795
Filer:	Mark J. Rozman/David Hopper
Filer Authorized By:	Mark J. Rozman
Attorney Docket Number:	ITL.3139P1US (P38525X)
Receipt Date:	24-OCT-2014
Filing Date:	16-FEB-2012
Time Stamp:	14:09:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	420
Deposit Account	201504
Authorized User	ROZMAN, MARK J.
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees) Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	ITL_3139P1US_FEE_TRANS.pdf	191267 b5aa8273c7fd50b708aff881da215a6c7e37b00d	no	1
Warnings:					
Information:					
2	Miscellaneous Incoming Letter	ITL_3139P1US_Fee_Address.pdf	204779 13f6ec3f199e3a263a533a03c6dfee6a1a1012f	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30632 fc5ce730dbbecacaab8c538bee06e93017302eff	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			426678		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/398,641	11/25/2014	8898494	ITL.3139P1US (P38525X)	1050

47795 7590 11/05/2014
TROP, PRUNER & HU, P.C.
1616 S. VOSS RD., SUITE 750
HOUSTON, TX 77057-2631

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 108 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Travis T. Schluessler, Berthoud, CO;
Russell J. Fenger, Beaverton, OR;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	13/398,641
Filing Date	February 16, 2012
First Named Inventor	Travis T. Schluessle
Title	Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached
Art Unit	2115
Examiner Name	Danny Chan
Attorney Docket Number	D0480-PA-13289-US-02

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ian D. MacKinnon/	Date (Optional)	January 27, 2022
Name	Ian D. MacKinnon	Registration Number	34,660
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date
13/398,641	February 16, 2012

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above:

00164

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Intel Corporation

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

January 25, 2022

Name

Lisa Hopkinson

Title

Administrator of Patents

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☒ Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	44849923
Application Number:	13398641
International Application Number:	
Confirmation Number:	1050
Title of Invention:	Power budgeting between a processing core, a graphics core, and a bus on an integrated circuit when a limit is reached
First Named Inventor/Applicant Name:	Travis T. Schluessler
Customer Number:	47795
Filer:	Ian David MacKinnon
Filer Authorized By:	
Attorney Docket Number:	ITL.3139P1US (P38525X)
Receipt Date:	27-JAN-2022
Filing Date:	16-FEB-2012
Time Stamp:	15:58:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	2022-01-27_POA_D0480-PA-13289-US-02.pdf	1248924	no	2
			4b05ab27e1ebbb24516866e458df37bdab7f27e75		

Warnings:

Information:	
Total Files Size (in bytes):	1248924
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/398,641	02/16/2012	Travis T. Schluessler	D0480-PA-13289-US-02

CONFIRMATION NO. 1050

POA ACCEPTANCE LETTER

164
KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002



Date Mailed: 02/04/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/27/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/agizaw/



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/398,641	02/16/2012	Travis T. Schluessler	ITL.3139P1US (P38525X)

CONFIRMATION NO. 1050

POWER OF ATTORNEY NOTICE

47795
TROP, PRUNER & HU, P.C.
PO Box 41790
HOUSTON, TX 77241



OC000000131547037

Date Mailed: 02/04/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 01/27/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/agizaw/

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court District of Delaware on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO.	DATE FILED 8/23/2022	U.S. DISTRICT COURT District of Delaware
PLAINTIFF Daedalus Prime LLC		DEPENDANT Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., MediaTek Inc., MediaTek USA Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, and Visteon Corporation
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 See Attached		
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	US 8,775,833 B2	7/8/2014	Daedalus Prime LLC
2	US 8,898,494 B2	11/25/2014	Daedalus Prime LLC
3	US 9,575,895 B2	2/21/2017	Daedalus Prime LLC
4	US 10,049,080 B2	8/14/2018	Daedalus Prime LLC
5	US 10,394,300 B2	8/27/2019	Daedalus Prime LLC
6	US 10,705,588 B2	7/7/2020	Daedalus Prime LLC

AO 120 (Rev. 08/10)

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☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO.	DATE FILED 8/23/2022	U.S. DISTRICT COURT District of Delaware
PLAINTIFF Daedalus Prime LLC		DEPENDANT Arrow Electronics, Inc.; Avent, Inc.; Digi-Key Electronics; Future Electronics Inc.; Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc.; Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC; Mouser Electronics, Inc.; Newark, NXP Semiconductors N.V., NXP USA, Inc.; Rochester Electronics, LLC; and Visteon Corporation
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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6	US 10,705,588 B2	7/7/2020	Daedalus Prime LLC

AO 120 (Rev. 08/10)

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DOCKET NO.	DATE FILED 8/23/2022	U.S. DISTRICT COURT District of Delaware
PLAINTIFF Daedalus Prime LLC		DEPENDANT Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, Qualcomm Inc., Qualcomm Technologies, Inc., and Visteon Corporation
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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5	US 10,394,300 B2	8/27/2019	Daedalus Prime LLC
6	US 10,705,588 B2	7/7/2020	Daedalus Prime LLC

AO 120 (Rev. 08/10)

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In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been
 filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.);

DOCKET NO. 2:22cv352	DATE FILED 9/12/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF Daedalus Prime LLC		DEPENDANT Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Taiwan Semiconductor Manufacturing Company Limited
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,775,833	7/8/2014	Daedalus Prime LLC
2 8,898,494	11/25/2014	Daedalus Prime LLC
3 10,049,080	8/14/2018	Daedalus Prime LLC
4 10,705,588	7/7/2020	Daedalus Prime LLC
5 9,831,306	11/28/2017	Daedalus Prime LLC

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

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 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

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 filed in the U.S. District Court Eastern District of Texas on the following

☐ Trademarks or ☐ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 2:22cv352	DATE FILED 9/12/2022	U.S. DISTRICT COURT Eastern District of Texas
PLAINTIFF Daedalus Prime LLC		DEPENDANT Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., and Taiwan Semiconductor Manufacturing Company Limited
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 10,319,812	6/11/2019	Daedalus Prime LLC
2 10,700,178	6/30/2020	Daedalus Prime LLC
3 11,251,281	2/15/2022	Daedalus Prime LLC
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
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