

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

QUALCOMM INCORPORATED,
Petitioner,

v.

DAEDALUS PRIME LLC,
Patent Owner.

IPR2023-00617
Patent 8,898,494 B2

Before WILLIAM V. SAINDON, THOMAS L. GIANNETTI, and
KRISTI L. R. SAWERT, *Administrative Patent Judges*.

GIANNETTI, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Samsung Electronics Co., Ltd., Samsung Electronics America, Inc. (collectively, “Samsung”), and Qualcomm, Inc. filed a Petition requesting *inter partes* review of claims 1, 3, 12, 14, and 15 (the “challenged claims”) of U.S. Patent No. 8,898,494 B2 (Ex. 1001, the “’494 patent”). Paper 4 (“Pet.”). With our authorization, Samsung and Daedalus Prime LLC (“Patent Owner”) filed a Joint Motion to Terminate as to Samsung. Paper 10. We granted the Joint Motion to Terminate and Samsung was terminated from the proceeding. Paper 11.¹ The proceeding is now maintained between Patent Owner and Qualcomm, Inc. (“Petitioner”). *See id.* Following the termination of Samsung, Patent Owner filed a Preliminary Response. Paper 12 (“Prelim. Resp.”).

For the reasons stated below, we determine that Petitioner has established a reasonable likelihood that it would prevail with respect to at least one claim. We therefore institute *inter partes* review as to all of the challenged claims of the ’494 patent and all of the asserted grounds of unpatentability.

B. Related Proceedings

The parties identify the following district court and ITC proceedings involving the ’494 patent: (1) *Daedalus Prime LLC v. Arrow Electronics, Inc.*, 1:22-cv-01107 (D. Del.); (2) *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.); (3) *Daedalus Prime LLC v. Mazda*

¹ The caption of this proceeding has been changed to reflect this termination.

Motor Corporation, 1:22-cv-01108 (D. Del.); (4) *Daedalus Prime LLC v. Samsung Electronics Co., Ltd.*, 2:22-cv-00352 (E.D. Tex.); (5) *Certain Integrated Circuits, Mobile Devices Containing the Same, and Components Thereof*, Inv. No. 337-TA-1335 (USITC); and (6) *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). Pet. 2–3; Paper 6, 1.

C. Real Parties-in-Interest

Petitioner identifies the following real parties-in-interest: Qualcomm Incorporated and Qualcomm Technologies, Inc. Pet. 2.

Without conceding that any such party is a Real Party-in-Interest, Petitioner further identifies Mazda Motor Corporation, Mazda North American Operations, Mazda Motor of America, Inc., Mercedes-Benz Group AG, Mercedes-Benz AG, Mercedes-Benz USA, LLC, and Visteon Corporation as parties that Patent Owner has accused of infringing the '494 Patent based on incorporation of Qualcomm products in *Daedalus Prime LLC v. Mazda Motor Corporation*, 1:22-cv-01109 (D. Del.) and *Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles*, Inv. No. 337-TA-1332 (USITC). *Id.*

At this stage, neither party challenges those identifications.

D. The '494 Patent

The '494 patent is titled “Power Budgeting Between a Processing Core, a Graphics Core, and a Bus on an Integrated Circuit When a Limit is Reached.” Ex. 1001, (54). The '494 patent relates to an apparatus, method,

and system for efficiently balancing performance and power between processing elements or a communication bus by identifying and alleviating bottlenecks based on measured workloads. *Id.* at Abstract, 1:12–16.

Bottlenecks can occur at the level of processing elements such as a CPU or GPU, or at a communication bus, and can cause applications to slow down. *Id.* at 15:8–21, 17:4–7. The '494 patent describes alleviating bottlenecks by allocating more current or frequency to the bottleneck component and capping or limiting competing devices. This strikes a dynamic balance between devices so that a device that needs more resources for better overall performance is allocated extra resources, while other devices are reduced in performance to meet a given power limit. *Id.* at 7:51–61, 17:4–41.

E. Illustrative Claims

The Petition challenges claims 1, 3, 12, 14, and 15, of which claim 1 is independent. Claim 1 is illustrative of the claimed subject matter and reproduced below:²

1. A processor comprising:
 - 1[a] an integrated circuit including:
 - 1[b] a first core;
 - 1[c] a cache memory;
 - 1[d] a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;
 - 1[e] a core workload monitor configured to determine a core workload for the first core;

² Paragraph labeling has been added based on those provided by Petitioner.

1[f] a bus workload monitor configured to determine a bus workload for the communication bus; and

1[g], 1[g.i] balancing control adapted to receive the bus workload from the bus workload monitor and

1[g.ii] to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit and

1[g.iii] a comparison between the bus workload and a bus workload threshold, the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit,

1[g.iv] wherein a power consumption of one of the first core and the communication bus is to be reduced, the power consumption reduction to be limited to maintain operation of the one of the first core and the communication bus above a low limit.

Ex. 1001, 21:17–39.

F. References and Other Evidence

The Petition relies on the following references:

Name	Reference	Publication/Issue Date	Exhibit(s)
White	US 7,263,457 B2	Aug. 28, 2007	Ex. 1008
Fukatsu	US 2008/0005607 A1	Jan. 3, 2008	Ex. 1006
Bose	US 7,421,601 B2	Sept. 2, 2008	Ex. 1005
Simeral	US 2009/0150689 A1	June 11, 2009	Ex. 1009
Naffziger	US 8,510,582 B2	Aug. 13, 2013	Ex. 1007

In addition, Petitioner submits the Declaration of Trevor Mudge. (Ex. 1002, “Mudge Decl.”).

G. Asserted Grounds of Unpatentability

Petitioner asserts the challenged claims are unpatentable on the following grounds:

Claims Challenged	35 U.S.C. §³	References
1, 12	103	Bose
3, 12, 14, 15	103	Bose, Fukatsu
1, 3, 12, 14, 15	103	Bose, Naffziger
1, 3, 14, 15	103	White, Simeral

See Pet. 5.

H. Overview of the Prior Art

1. Bose (Ex. 1005)

Bose is a U.S. Patent titled “Method and System for Controlling Power in a Chip Through a Power-Performance Monitor and Control Unit.” Ex. 1005, (54). Bose discloses a system and method for controlling power and performance in a microprocessor system that includes a monitoring and control system. *Id.* at Abstract, 1:17–22. The monitoring and control system maintains the maximum power of the chip or system within a programmable limit, maintains the peak temperature of the monitored

³ Because the earliest application from which the ’494 patent claims priority was filed before March 16, 2013, the pre-AIA (“America Invents Act”) version of § 103 applies. Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284, 285–88 (2011).

regions of the chip or system below a specified limit, and targets a net throughput for maximization. *Id.* at 2:16–24, 4:19–29. An example of a monitoring and control system is shown in Figure 1 from Bose (reproduced

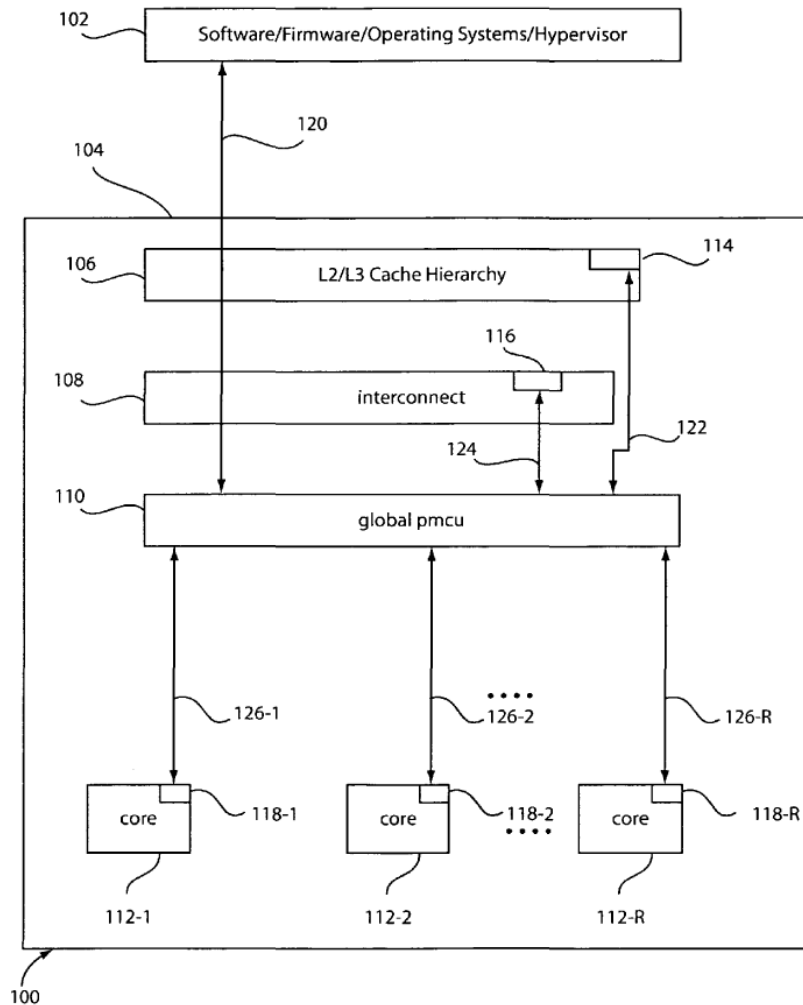


FIG. 1

below).

Figure 1 “is a block diagram showing a hierarchical power-performance monitor and control unit (PMCU) integrated into a chip/system.” Ex. 1005, 3:59–61. Figure 1 includes a monitoring and control system (100) with local components (114, 116, 118-1, 118-2, 118-R) and global components (110) which monitor and control a multi-core chip. *Id.* at 6:60–67. The

monitoring and control system is organized so that each core 112-1, 112-2, 112-R or other element in the system is monitored using the local components and reports usage information (such as power usage and temperature usage) to a global monitoring and control unit that assesses the information, determines a power mode, and chooses appropriate power optimizations for each core element. *Id.* at 6:56–7:17.

Bose specifies that “the performance of the chip or system may be targeted for maximization by one or more of the following: (a) use and deployment of one or more additional cores (that would otherwise be powered off or excluded from the design” and “(b) at a given response point and given a choice of power mode allocations per core, an allocation is made such as to maximize the chip (or system)—level throughput performance.” *Id.* at 12:18–41. The power modes are transmitted to each core such that their power levels are decreased or increased. *Id.*

2. Fukatsu (Ex. 1006)

Fukatsu is a published U.S. Patent Application titled “Method of Controlling Information Processing Device, Information Processing Device, Program, and Program Converting Method.” Ex. 1006, (54). Fukatsu discloses “a method of controlling an information processing device which includes a processor having a cache memory, and a clock supplying unit that supplies a clock signal to the processor.” *Id.* at Abstract. Generally, the clock increases the CPU clock frequency and decreases the bus and memory clock frequencies when the cache hit rate is high, and decreases the CPU clock frequency and increases the bus and memory clock frequencies when the cache hit rate is low. *Id.* ¶ 6. Fukatsu’s “method includes: predicting a

hit rate of the cache memory; and controlling the clock supplying unit so as to change a frequency of the clock signal in accordance with the predicted hit rate.” *Id.* at Abstract, ¶ 8.

Fukatsu discusses two ways of determining the predicted hit rate: (1) by “detecting an occurrence of a first process in the processor; identifying a type of a second process which starts as a result of the detected occurrence of the first process; and predicting the hit rate in accordance with the identified type;” and (2) obtaining the current cache hit rate on a regular basis by a timer using a cache hit rate monitoring circuit, storing the hit rate, and performing statistical analyses on the recorded values to predict the hit rate. *Id.* ¶¶ 12, 100–105.

3. Naffziger (Ex. 1007)

Naffziger is a U.S. Patent titled “Managing Current and Power in a Computing System.” Ex. 1007, (54). Naffziger discloses a system and method for efficient power transfer on a die comprising two or more computation units (e.g., processors), at least two different voltage regulators, and a power manager. *Id.* at Abstract, 3:42–44. Naffziger explains that the activity levels of the computation units can be measured and reported to the power manager, which uses the activity data to transfer power to or away from computation units to support the activity levels. *Id.* at 1:22–38, 1:66–2:29. Naffziger states that “[a]ny of a variety of techniques may be utilized to determine power consumption of a given computation unit,” for example, by using thermal sensors or current sensors. *Id.* at 4:14–51.

Naffziger further explains that “[w]hen a given computation unit does not have a high or moderate workload, its activity level may decrease below

a given threshold. Accordingly, its measured power usage value decreases.” *Id.* at 5:28–31. Naffziger explains that “[t]he resulting reduced power usage value is conveyed to the power management unit.” *Id.* at 5:31–32. Further, “[i]n response to the reduced power usage value, the power management unit . . . may redistribute the power credits of the die.” *Id.* at 5:32–34. “For example, the power management unit . . . may lend power credits of a determined inactive computation unit to a computation unit that is determined to be highly active.” *Id.* at 5:34–37.

4. White (Ex. 1008)

White is a U.S. Patent titled “System and Method for Operating Components of an Integrated Circuit at Independent Frequencies and/or Voltages.” Ex. 1008, (54). White discloses a processor or other integrated circuit with multiple logic cores that are configured to operate at independent frequencies and voltages and may be connected to other sub-systems, components, or peripherals external to the integrated circuit, such as memory or communications busses. *Id.* at 2:15–22, 2:45–67, 6:23–40. Figure 1 (reproduced below) depicts “a block diagram illustrating an integrated circuit including multiple logic cores configured to operate at independent voltages and/or frequencies.” *Id.* at 5:18–31.

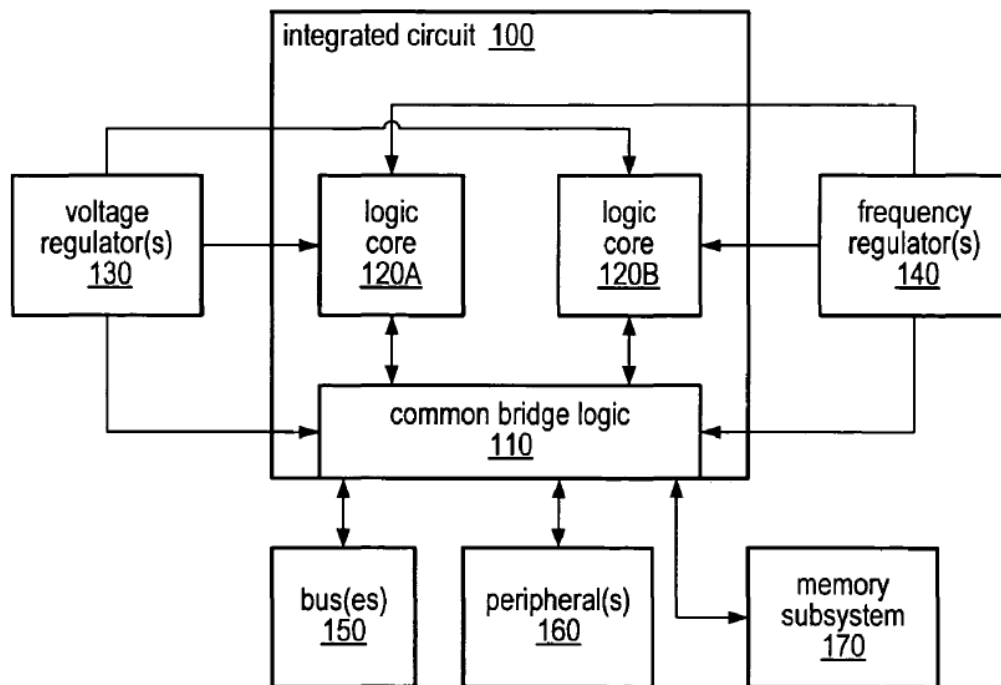


FIG. 1

Ex. 1008, Fig. 1. Figure 1 includes an integrated circuit (100) with two logic cores (120A, 120B), voltage regulators (130), frequency regulators (140), and common bridge logic (110) “configured to communicate with the logic cores as well as with other elements or peripherals either internal or external to integrated circuit 100, such as bus 150, peripheral 160 and/or memory subsystem 170.” *Id.* at 6:41–7:7.

White explains that a system including an integrated circuit may also include power management logic which may be configured to control the operating characteristics, such as the operating voltage and/or operating frequency of the logic cores. *Id.* Fig. 2, 8:59–65. The processor’s cores can be individually adjusted or adjusted as a group to operate at lower frequencies and/or voltages to save power or generate less heat to avoid an

unwanted shutdown. *Id.* at 1:53–2:11, 2:22–44, 3:20–52. For example, if the system is running on battery power, power management logic can be configured to adjust the operating frequency and/or voltage of the logic cores to save power. *Id.* at 8:59–9:24.

In another example, temperature sensors measure the temperature of the integrated circuit, a region of the integrated circuit, or individual cores of the integrated circuit. *Id.* at 11:61–12:37. If the sensors detect that the temperature is too high, the operating frequency or the voltage of the components in the device may be decreased. *Id.* at 12:59–14:20.

White also explains that the processor’s cores can be adjusted to alleviate bottlenecks. *Id.* at 9:25–53. In such a case, the cores can be supplied with lower voltages and/or frequencies so the bottlenecked element can be supplied with a higher voltage and/or frequency. *Id.*

5. Simeral (Ex. 1009)

Simeral is a U.S. Patent Application Publication titled “Data Path Controller with Integrated Power Management to Manage Power Consumption of a Computing Device and Its Components.” Ex. 1009, (54). Simeral discloses a data path controller, a computer device, an apparatus, and a method for integrating power management functions into a data path controller to manage power consumed by processors and peripheral devices. *Id.* at Abstract.

The data path controller can manage power in different modes, which can be implemented separately or concurrently. *Id.* ¶ 20. Simeral describes a mode in which the data path controller modifies operational characteristics of components to conserve power while providing sufficient resources to

support a workload, and a mode in which the data path controller modifies operational characteristics of components as corrective action to bring one or more noncompliant activity levels back into compliance. *Id.* 20–21, 24.

The modes may be operated according to different performance profiles which indicate priorities for various components of the system based on the use of the system. *Id.* ¶¶ 27–28. For example, if “the user desires a higher performing computing device over one that minimizes power consumption (e.g., higher operating speeds are preferred over extending battery life),” the performance profile may describe a range of frequencies and a range of voltages for operating the processor at high speeds, without necessarily conserving power. *Id.*

II. ANALYSIS OF THE CHALLENGED CLAIMS

A. Level of Ordinary Skill in the Art

Petitioner contends a person of ordinary skill in the art of the ’494 patent would have possessed “a bachelor’s degree in electrical engineering, computer engineering, computer science, or a related field” and would have had “at least two years of experience in the research, design, development, and/or testing of semiconductors, processors, power management, and related firmware and software, or the equivalent, with additional education substituting for experience and vice versa.” Pet. 8 (citing Mudge Decl. ¶¶ 22–26, 38–58) (emphasis omitted).

At this stage, Patent Owner does not dispute Petitioner’s description of a person of ordinary skill in the art or provide its own description.

We regard Petitioner’s description as consistent with the prior art before us. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001)

(prior art itself may reflect an appropriate level of skill). Thus, for the purpose of our decision, we adopt Petitioner’s proposal.

B. Claim Construction

We construe claim terms only as relevant to the parties’ contentions and only to the extent necessary to resolve the issues in dispute. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Neither party proposes claim constructions for our consideration. Petitioner reports that it “does not believe that any term requires explicit construction.” Pet. 9 (citing Mudge Decl. ¶ 87). Patent Owner does not dispute Petitioner’s position or discuss claim construction. Therefore, we determine there are no claim terms that need to be construed at this stage.

C. Obviousness

A claim is unpatentable as obvious under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called “secondary considerations,” including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383

U.S. 1, 17–18 (1966). At this stage, neither party has presented any evidence on the fourth *Graham* factor.

D. Obviousness of Claims 1 and 12 Based on Bose

Petitioner asserts that Bose teaches each limitation of claims 1 and 12 and provides an element-by-element analysis. Pet. 20–38; Mudge Decl. ¶¶ 88–127. Patent Owner contests elements 1[d], 1[g.ii], and 1[g.iii]. Prelim. Resp. 10–14

1. Claim 1 preamble, elements 1[a]–1[c], 1[e], 1[f], 1[g], 1[g.i], and 1[g.iv]

Petitioner contends that the preamble of claim 1 (“A processor comprising”) is met by Bose’s disclosure of a microprocessor system. Pet. 20 (citing Ex. 1005, Fig. 1).

Petitioner contends that element 1[a] (“an integrated circuit”) is met by Bose’s disclosure of a processor system including chip 104. *Id.* at 21–22 (citing Ex. 1005, Fig. 1).

Petitioner asserts that element 1[b] (“a first core”) is met by Bose’s disclosure that chip 104 “comprises at least one core.” *Id.* at 22 (citing Ex. 1005, Fig. 1).

Petitioner contends that element 1[c] (“a cache memory”) is met by Bose’s disclosure that “chip 104 comprises L2/L3 cache 106 . . . , which provides temporary storage, as part of the management hierarchy of the integrated circuit 104.” *Id.* at 22–23.

Petitioner contends that element 1[e] (“a core workload monitor . . .”) is met by Bose’s disclosure that “each core has an associated local PMCU^[4] monitor-and-control unit, which is a core workload monitor.” *Id.* at 25–27.

Petitioner contends that element 1[f] (“a bus workload monitor . . .”) is met by Bose’s disclosure “that the interconnect has an associated local PMCU monitor-and-control unit.” *Id.* at 27–29. Petitioner explains that “Bose’s bus workload monitor, PMCU 116, determines the bus workload for the communications bus.” *Id.* at 28.

Similarly, Petitioner contends that elements 1[g] and 1[g.i] (both reciting “balancing control”) are met by Bose’s PCMU. *Pet.* 29–31.

Element 1[g.iv] calls for limiting the power consumption reduction “to maintain operation of the one of the first core and the communication bus above a low limit.” Petitioner contends that Bose’s disclosure of “reducing power consumption of either the core or communication bus to above a low limit” meets this limitation. *Id.* at 36–37.

At this stage, Patent Owner does not dispute these contentions. We determine that Petitioner demonstrates sufficiently at this stage that these claim elements are met by Bose.

2. Claim elements 1[d], 1[g.ii], and 1[g.iii]

Petitioner contends Bose meets claim limitations 1[d], 1[g.ii], and 1[g.iii]. *Pet.* 23–25 (element 1[d]), 31–36 (elements 1[g.ii], and 1[g.iii]). Patent Owner disputes these assertions by Petitioner and contends that the

⁴ Power-performance Monitor and Control Unit. *Ex.* 1005, 4:5–7.

Petition fails to show that Bose teaches these claim elements. Prelim. Resp. 10–17.

a. Element 1[d]: “a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory”

Petitioner contends that Bose meets this element by disclosing “a communication bus coupled to the first core and connecting that core to a cache memory.” Pet. 24. Referring to Figure 1 of Bose, Petitioner explains that “Bose discloses that chip 104 comprises several components, including an interconnect [108].” *Id.*

Patent Owner responds that “Bose does not disclose that the cores are connected to the logic cache via the specific ‘interconnect 108’ that Petitioner aligns with the claimed ‘communication bus.’” Prelim. Resp. 10. Patent Owner continues, “[t]o the contrary, FIG. 1 illustrates the interconnect 108 is specifically avoided by the connection 122 between the cores 118 and the cache (via the global PMCU 110).” *Id.* (emphasis omitted).

We disagree with Patent Owner’s argument on this record. Dr. Mudge explains that “[a person of ordinary skill] would have understood that, while Figure 1 does not depict lines connecting interconnect 108 to core 112-1 and to L2/L3 cache hierarchy, Figure 1’s arrowed lines represent the hierarchical organization of reports and commands between components, not their physical connections.” Mudge Decl. ¶ 99. Dr. Mudge’s testimony is supported by Bose’s description of Figure 1 as showing “a hierarchical power-performance monitor.” Ex. 1005, 3:59–61. Elsewhere, Bose refers to this figure as showing a “management hierarchy” (*id.* at 6:18) and explains that “[t]o clearly define the responsibility of each layer of the hierarchy, the

layers are designed and configured such that the layers report upward and command downward in the hierarchy” (*id.* at 6:49–52). This disclosure in Bose supports Dr. Mudge’s conclusion that “[b]ased on Bose’s depicted and described hierarchical organization of reports and commands between components, and, based on Bose’s use of the well-known term of art ‘interconnect,’ it would have been obvious to a [person of ordinary skill] that Bose’s interconnect 108 couples and connects to each core and to L2/L3 cache hierarchy.” Mudge Decl. ¶ 99.

We find that on this record Petitioner has demonstrated sufficiently at this stage that this element is met by Bose.

b. Element 1[g.ii]: “to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit . . . the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit”

Petitioner contends that Bose meets this element by disclosing that “global PMCU 110 is given an overall chip 104 power budget, and is responsible for assigning the budget to each core element 112-1, 112-2, 112-R, 106, and 108, according to thermal packaging, power supply and other considerations.” Pet. 31 (internal quotation marks omitted).

Patent Owner responds that Petitioner “fails to demonstrate that Bose discloses tuning power allocation ‘between’ the components as claimed.” Prelim. Resp. 11–13. We disagree. Dr. Mudge testifies that “[a person of ordinary skill] would have understood such power optimizations as global PMCU dynamically tuning power allocation between the core 112-1 and interconnect 108.” Mudge Decl. ¶ 114. He explains that “[a person of ordinary skill] would have understood that Bose’s overall chip power budget

is a power limit for the integrated circuit. It was well-known in the art that a power budget for the system is a power limit for the system.” *Id.*

We find that Petitioner, supported by this testimony from Dr. Mudge, has demonstrated sufficiently at this stage that this element is met by Bose.

c. Element 1[g.iii]: “and a comparison between the bus workload and a bus workload threshold”

Petitioner contends that Bose meets this element by disclosing that “[g]lobal PMCU 110 calculates for each core a ‘power budget’ and ‘power mode.’” Pet. 32 (citing Ex. 1005, 8:35–40). Petitioner explains that “[e]ach ‘power mode’ has an associated ‘power budget.’” *Id.* Petitioner also asserts that “Bose further teaches a predicted power and performance for each defined power mode included in its ‘Power/Performance Trade-off Table 206.’” *Id.* at 33.

Patent Owner responds that “Petitioner failed to demonstrate that Bose discloses or suggests ‘a bus workload threshold,’ as claimed.” Prelim. Resp. 13–17. Patent Owner contends that “Petitioner does not explain how or why it asserts that Bose’s ‘power budget’ serves as the claimed ‘workload threshold.’” *Id.* at 13. And Patent Owner contends that “Petitioner does not explain how or why it asserts that Bose’s ‘predicted values included in the Trade-off Table 206’ serve as the claimed ‘workload threshold.’” *Id.* at 14. Finally, Patent Owner contends “Petitioner has also failed to demonstrate that Bose discloses or suggests ‘a comparison between the bus workload and a bus workload threshold,’ as claimed.” *Id.*

We disagree with these arguments by Patent Owner as they are not supported by the evidence of record. At this stage, we find Dr. Mudge’s explanation of how this element is met by Bose sufficient. Dr. Mudge

testifies that “each component’s power mode may be representative of the workload at which the core is currently executing.” Mudge Decl. ¶ 118. He testifies that “if the workload threshold (i.e., the associated ‘power budget’ for that power mode) is too high or too low, in comparison with the workload threshold, then the global PMCU may switch that core into a different power mode more appropriate for its current workload.” *Id.* He testifies that “this switch over may be based on the defined power modes in trade-off table 206, which would also have been considered a workload threshold.” *Id.*

He testifies that “Bose’s teaching of reading real time statistics discloses the claimed workload.” *Id.* ¶ 119. He explains that “[a person of ordinary skill] would have understood that Bose suggests comparing those real time statistics to the power budget assigned to each component, as determined in Power/Performance Trade-off Table 206.” *Id.* ¶ 120. He explains that “[a person of ordinary skill] would have understood that if the workload of a component exceeded a threshold for a given power budget or power mode that Bose’s global PMCU would allocate additional power to that component.” *Id.*

He concludes that, “[a]lthough Bose discloses that the global PMCU calculates the power budget and power mode for each core but does not explicitly state the same is true for the interconnect, a [person of ordinary skill in the art] would have understood that the same calculation is applicable to the interconnect.” *Id.* ¶ 123.

We find that Petitioner, supported by this testimony from Dr. Mudge, has demonstrated sufficiently at this stage that this element is met by Bose.

3. Claim 12

Claim 12 depends from claim 1. The claim recites “The processor of claim 1, wherein the balancing control is to receive a hint regarding a future workload and to dynamically tune the power allocation further based on the hint.” Ex. 1001, 23:18–20. Petitioner asserts that Bose meets this additional limitation. Pet. 37–38. Dr. Mudge provides supporting testimony. Mudge Decl. ¶¶ 126–127.

Patent Owner does not separately address this claim. We find that Petitioner, supported by this testimony from Dr. Mudge, has demonstrated sufficiently at this stage that this element is met by Bose.

4. Summary

For the reasons given, Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge to claims 1 and 12.

E. Obviousness of Claims 3, 12, 14, and 15 Based on Bose and Fukatsu

Petitioner asserts that Bose and Fukatsu teach each limitation of claims 3, 12, 14, and 15 and provides an element-by-element analysis. Pet. 38–49; Mudge Decl. ¶¶ 128–153. Petitioner also provides a motivation to combine the references with a reasonable expectation of success. Pet. 38–42; Mudge Decl. ¶¶ 128–136. For example, Petitioner explains that “[b]oth teach methods for controlling power and performance in a processor to improve processing efficiency and reduce power consumption and making trade-offs between power performance and processing efficiency.” Pet. 38. Also, “both Bose and Fukatsu teach similar components and structures, with shared resources connected to processor cores through a bus or interconnect.” *Id.*

Patent Owner responds that this challenge fails for the same reasons set forth in response to the challenge to claim 1 based on Bose, *supra*. We find those arguments unavailing for the reasons given in Sections II.D.1 and II.D.2, *supra*.

For the reasons given, Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge to claims 3, 12, 14, and 15.

F. Obviousness of Claims 1, 3, 12, 14, and 15 Based on Bose and Naffziger

Petitioner asserts that Bose and Naffziger teach each limitation of claims 1, 3, 12, 14, and 15 and provides an element-by-element analysis supported by testimony from Dr. Mudge. Pet. 49–61; Mudge Decl. ¶¶ 154–182. Patent Owner disputes this assertion and contends that the Petition fails to show that a person of ordinary skill in the art would have been motivated to combine Bose and Naffziger, and further contends that Bose and Naffziger fail to teach claim limitations 1[d], 1[g.ii], and 1[g.iii]. Prelim. Resp. 17–22.

1. Motivation to Combine Bose and Naffziger

Petitioner provides a motivation to combine these references with a reasonable expectation of success. Pet. 49–53; Mudge Decl. ¶¶ 154–158. For example, Petitioner explains that “[b]oth relate to similar methods for controlling or managing power consumption and performance in a processor, and both specifically describe transferring or adjusting power allocation between cores or dies for efficiently managing or controlling the processor’s power consumption.” Pet. 50. Petitioner asserts also that “Bose and Naffziger have similar components and structures.” *Id.*

Patent Owner responds that, for several reasons, a person of ordinary skill would not have been motivated to combine Bose and Naffziger. Prelim. Resp. 17–20. For example, Patent Owner argues that Petitioner has not explained how the two references relate to “similar methods.” *Id.* at 17. Patent Owner argues that “[a]llocating power between cores or dies for efficient management or control of a processor’s power consumption is too remote a connection to demonstrate that these references ‘relate to similar method’ as Petitioner asserts.” *Id.* at 18. Patent Owner argues that “[m]erely alleging that references are compatible and would have led to a ‘more efficient and better functioning processor’ does not provide a motivation to combine them.” *Id.* at 19. And Patent Owner argues that “Petitioner’s additional support for a motivation to combine these references is grounded in impermissible hindsight.” *Id.*

We find that at this stage, Petitioner has demonstrated a sufficient rationale for combining Bose and Naffziger. Pet. 49–53. Both are directed to the same problem of controlling or managing power consumption in a processor. Mudge Decl. ¶ 154. Both provide similar solutions to the problem, “[s]pecifically, both describe transferring or adjusting power allocation between cores or dies for efficiently managing or controlling the processor’s power consumption.” *Id.* The Federal Circuit instructs us that this is sufficient evidence of a motivation to combine. *See In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1380 (Fed. Cir. 2007) (“One skilled in the art would naturally look to prior art addressing the same problem as the invention at hand, and in this case would find an appropriate solution.”); *In re Kurzweil*, 4 F. App’x 823, 826 (Fed. Cir. 2001) (“The motivation to combine references can be inferred from the fact that they address the same

problem.”); *Pro-Mold & Tool Co. v. Great Lakes Plastics, Inc.*, 75 F.3d 1568, 1573 (Fed. Cir. 1996) (“[The motivation to combine references] may also come from the nature of the problem to be solved, leading inventors to look to the references relating to possible solutions to that problem.”).

2. Claim elements 1[d], 1[g.ii], and 1[g.iii]

Patent Owner contends that Petitioner fails to show that these claim elements are taught by Bose and Naffziger. Prelim. Resp. 20–22.

Patent Owner argues that because Petitioner relies on Bose to meet element 1[d], this challenge fails for the reasons given in connection with the previous challenge based on Bose alone. *See* Section II.D.2, *supra*. For the reasons previously discussed, we do not find those arguments by Patent Owner persuasive, and for the reasons given by Petitioner, we find that at this stage, Petitioner has sufficiently demonstrated that Bose teaches this limitation.

In this challenge, Petitioner relies on Naffziger to meet element 1[g.ii]. Pet. 54. Dr. Mudge testifies that “Naffziger teaches allocating power credits between computational units and that the number of power credits available to be allocated depends on the TDP [Thermal Design Point] for the integrated circuit, which a [person of ordinary skill] would have understood corresponds to a maximum amount of power a cooling system in a computer is able to dissipate.” Mudge Decl. ¶ 161 (citing Ex. 1022 ¶ 21).

Patent Owner responds that Petitioner “fails to demonstrate that a [person of ordinary skill] would have incorporated the identified teachings with Bose.” Prelim. Resp. 21. This argument is unavailing because it does not take into account the reference as a whole. The Federal Circuit has

rejected a similar argument, reversing the Board’s finding of no motivation to combine in *General Electric Co. v. Raytheon Technologies Corp.*, 983 F.3d 1334, 1351–52 (Fed. Cir. 2020) (“[T]he Board’s approach would require a motivation to combine each element of the claim—even those present together in a reference. This analysis unduly dissects prior art references into collections of individual elements, requiring a party showing obviousness to re-do the work already done in the prior art reference.”).

We find that for the reasons given, at this stage Petitioner demonstrates a sufficient motivation to combine Bose and Naffziger, and further, that Naffziger meets element 1[g.ii].

For claim element 1[g.iii], Petitioner again relies on Naffziger. Pet. 54–55. Dr. Mudge testifies that Naffziger discloses a power management unit that compares reported activity levels to “corresponding thresholds.” Mudge Decl. ¶ 162. He testifies that “[a person of ordinary skill in the art] would have readily applied this threshold comparison to Bose’s similar power management scheme because Bose’s tables for calculating power budgets and power modes includes performance statistics from all local PMCUs, which includes the workload of the interconnect.” *Id.* (citing Ex. 1005, Fig. 2, 6:56–60, 7:41–61, 8:45–51).

Patent Owner’s response mirrors its response to element 1[g.ii], discussed *supra*. We find that for the reasons given for that element and those in the Petition, at this stage Petitioner demonstrates that Naffziger meets element 1[g.iii].

3. Summary

At this stage, Patent Owner does not separately address claims 3, 12, 14, or 15. For the reasons given above, and in the Petition, Petitioner has at this stage demonstrated a reasonable likelihood of prevailing on this challenge to claims 1, 3, 12, 14, and 15.

G. Obviousness of Claims 1, 3, 14, and 15 Based on White and Simeral

Petitioner asserts that White and Simeral teach each limitation of claims 1, 3, 14, and 15 and provides an element-by-element analysis. Pet. 62–89; Mudge Decl. ¶¶ 183–231. Patent Owner disputes this assertion and contends that the Petition fails to show that a person of ordinary skill in the art would have been motivated to combine White and Simeral, and further contends that White and Simeral fail to teach claim limitations 1[d], 1[e], 1[f], 1[g.ii], and 1[g.iii]. Prelim. Resp. 22–33.

1. Motivation to combine White and Simeral

Petitioner provides a motivation to combine these references with a reasonable expectation of success. Pet. 62–65; Mudge Decl. ¶¶ 183–187. For example, Petitioner explains that “both relate to similar methods of managing power in circuits by adjusting power consumption of circuit components.” Pet. 62. Further, “White teaches managing power by adjusting the power consumption and operating frequencies of logic cores and common bridge logic to avoid overheating the integrated circuit, while Simeral similarly discloses adjusting the operational characteristics of the bus in comparison to a threshold activity level.” *Id.* (citation omitted). Dr. Mudge testifies that “[a person of ordinary skill] would have been motivated to combine White’s teachings with Simeral’s teachings for managing power

by monitoring activity associated with the bus in comparison to a threshold and accordingly adjusting circuit components activity levels because Simeral's teachings would improve White's ability to respond quickly to power-related events, such as spikes in bus activity, thus increasing the number and duration of power saving opportunities." Mudge Decl. ¶ 183.

Patent Owner's response echoes its previous arguments alleging lack of motivation to combine other references. Prelim. Resp. 23–25. For example, Patent Owner asserts that "[i]nclusion of such generic processor components does not provide a motivation to combine; otherwise, every reference describing any processor would be combined, and the entire motivation to combine analysis would be mooted." *Id.* at 24. Further, Patent Owner asserts that "merely because references could be compatible or relate to the same subject matter does not provide a motivation to combine them." *Id.* Also, Patent Owner asserts that "Petitioner does not identify any reason or justification why a [person of ordinary skill] would have been motivated to modify White by combining it with Simeral, just that doing so could be beneficial." *Id.* at 24–25.

Patent Owner's arguments are unavailing on this record. The Federal Circuit has instructed us that "[t]he motivation-to-combine analysis is a flexible one. '[A]ny need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed.'" *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1379 (Fed. Cir. 2023) (quoting *KSR*, 550 U.S. at 420). Reversing the Board's finding of no motivation to combine, the Federal Circuit specifically addressed an argument similar to Patent Owner's assertion that the Petitioner "does not identify any reason or justification":

Additionally, “universal” motivations known in a particular field to improve technology provide “a motivation to combine prior art references *even absent any hint of suggestion* in the references themselves.” *Intel [Corp. v. Qualcomm Inc.]*, 21 F.4th at 797–99 (cleaned up) (emphasis in original) (determining that the Board’s rejection of “increasing energy efficiency,” a “generic concern” in electronics, as a motivation to combine lacked substantial evidence (cleaned up)).

Intel Corp., 61 F.4th at 1380. Patent Owner’s arguments for lack of motivation to combine attempt appear to be inconsistent with the cases we cite above. For the reasons given, at this stage we find that Petitioner has demonstrated a sufficient rationale for combining White and Simeral.

2. Claim elements 1[d], 1[e], 1[f], 1[g.ii], and 1[g.iii]

Patent Owner contends that the Petition fails to show that a person of ordinary skill in the art would have been motivated to combine White and Simeral, and contends further that White and Simeral do not teach claim limitations 1[d], 1[e], 1[f], 1[g.ii], and 1[g.iii]. Prelim. Resp. 22–33. We addressed the motivation to combine the references in Section II.G.1, *supra*. Here we address the disputed claim elements.

a. Element 1[d]: “a communication bus coupled to the first core, the communication bus to connect the first core and the cache memory;”

Patent Owner contends that for element 1[d], “White nowhere discloses that the cores are connected to the logic cache with the specific ‘common bridge logic 110’ that Petitioner aligns with the claimed ‘communication bus.’” Prelim. Resp. 26. This argument is contrary to the expert testimony offered by Dr. Mudge. He testifies that “[g]iven the common bridge logic’s function of connecting the logic cores to the various elements of integrated circuit 100, it would have been obvious to a [person

of ordinary skill] to connect the cores to the logic cache 1128.” Mudge Decl. ¶ 199. Referring to the technical literature for support, he testifies that “[i]t was well-known in the art of circuit design to use an interconnect to connect cores to various system components, including to shared memory.” *Id.* (citing Ex. 1024 ¶ 44; Ex. 1025, Fig. 4; Ex. 1026, 1:19–33). At this stage, we find this testimony credible, and for the reasons summarized above and those given in the Petition, we find that at this stage, Petitioner demonstrates sufficiently that White meets element 1[d].

b. Element 1[e]: “a core workload monitor configured to determine a core workload for the first core;”

For element 1[e], Patent Owner contends “Petitioner does not assert that White discloses any component that monitors the *workload* of the core, instead alleging that the ‘power management logic 200 [is] configured to monitor and adjust the operating frequency and/or voltage.’” Prelim. Resp. 27 (alteration in original). Patent Owner continues, “as the ’494 Patent’s descriptions make clear, that workload is not the same as ‘performance metric[s]’ such as frequency and/or voltage.” *Id.* (alteration in original).

We disagree with this argument. The ’494 patent, in the passage quoted by Patent Owner, states: “Determining a workload includes *any known method* for determining activity of hardware.” Prelim. Resp. 27 (quoting Ex. 1001, 9:47–57) (emphasis added). At this stage, we find that the specification does not support Patent Owner’s argument that determining workload requires a particular measurement. For the reasons given, we find that at this stage, Petitioner demonstrates sufficiently that White discloses this element. *See* Pet. 72–73.

c. Element 1[f]: “a bus workload monitor configured to determine a bus workload for the communication bus;”

For this element, Patent Owner asserts “Petitioner does not assert that White discloses any component that monitors the *workload* of the bus, instead alleging that the ‘power management logic 200 [is] configured to monitor and adjust the operating frequency and/or voltage.’” Prelim. Resp. 28 (alteration in original). Patent Owner continues, “as discussed above with respect to Claim 1[e], the ’494 Patent’s description makes clear that a workload is not the same as ‘performance metric[s]’ such as frequency and/or voltage.” *Id.* at 28–29 (alteration in original).

We find that at this stage, Petitioner demonstrates sufficiently that White discloses this element for the reasons given for element 1[e]. *See* Pet. 73–74. In addition, Petitioner demonstrates that Simeral “also teaches a bus workload monitor that determines workload for the communication bus.” *Id.* at 74–76. Patent Owner’s argument that Petitioner “does not explain why a [person of ordinary skill] would have been motivated to combine [White and Simeral] in the manner claimed” has been previously addressed. Prelim. Resp. 29.

d. Element 1[g.ii]: “to dynamically tune power allocation between the first core and the communication bus based on a power limit for the integrated circuit...the power limit corresponding to a maximum thermal dissipation capacity for the integrated circuit,”

For this element, Patent Owner argues “Petitioner asserts that White discloses that power management logic can control the voltage and/or frequency of the cores or the bridge logic, but fails to demonstrate that White discloses tuning power allocation ‘between’ them as claimed.” Prelim. Resp. 30.

We disagree with this argument. Dr. Mudge testifies that “White’s power management logic controls and adjusts the operating characteristics of the cores and common bridge logic.” Mudge Decl. ¶ 208. He testifies that “White teaches that these adjustments are based, at least in part, on the temperature of the integrated circuit.” *Id.* ¶ 209. He explains that “[a person of ordinary skill] would have understood White’s reference to the circuit’s maximum operating temperature as corresponding to the claimed power limit.” *Id.* Further, “White discloses the same adjustments may apply to the common bridge logic.” *Id.* ¶ 210.

For the reasons given, we find that at this stage, Petitioner demonstrates sufficiently that White discloses this element. *See* Pet. 77–78.

e. Element 1[g.iii]: “and a comparison between the bus workload and a bus workload threshold”

For this element, Patent Owner argues that “Petitioner asserts ‘White teaches dynamically tuning power allocation between the cores and common bridge to avoid bottlenecking at the bridge,’ but fails to demonstrate that White disclosed a system that could monitor and account for ‘bottlenecking.’” Prelim. Resp. 32.

We disagree. We note first that the claims do not refer to “bottlenecking,” nor does Patent Owner propose a construction for this term. In any event, Dr. Mudge testifies that White and Simeral disclose this limitation, as well as element 1[g.i]. Mudge Decl. ¶¶ 211–216. Dr. Mudge testifies that “White teaches dynamically tuning power allocation between the cores and common bridge to avoid bottlenecking at the bridge.” Mudge Decl. ¶ 211 (citing Ex. 1008, 7:46–56). He continues, “[a person of ordinary skill] would have understood ‘bottlenecking’ as referring to a comparison of

the bridge's monitored frequency and/or voltage with its operating capacity, because when the bridge's monitored frequency exceeds its operating capacity, it causes a bottleneck to overall performance.” *Id.* (citing Ex. 1008, 9:39–53).

Dr. Mudge asserts further that “like White’s power management logic, Simeral’s data path controller 100 and its power management controller 106 disclose the claimed balancing control.” *Id.* ¶ 212 (citing Ex. 1009, Fig. 1A). He explains that “Simeral further discloses data path controller 100 as dynamically tuning power allocation because it ‘manage[s] power consumption for any component’ and ‘react[s] to power-related events in real-time or (nearly so).” *Id.* ¶ 213 (quoting Ex. 1009 ¶¶ 20, 23) (alterations in original). Also, he explains that “Simeral further discloses such dynamic power allocation based on a comparison between the bus workload and a bus workload threshold, by increasing/decreasing operational characteristics such as the ‘bandwidth of a bus.’” *Id.* ¶ 214 (citing Ex. 1009 ¶ 21).

Patent Owner responds that “Petitioner also relies on Simeral as allegedly disclosing this limitation, but fails to demonstrate that a [person of ordinary skill] would have incorporated the identified teachings with White’s.” Prelim. Resp. 32. We discuss *supra* the reasons why this argument is unavailing. *See supra*, Section II.F.2 (citing *General Electric Co.*, 983 F.3d at 1351–52).

For the reasons given in the Petition and the supporting testimony of Dr. Mudge, we determine that on this record, Petitioner demonstrates sufficiently that White and Simeral meet this element.

3. Summary

For the reasons given, Petitioner has demonstrated a reasonable likelihood of prevailing on this challenge to claims 1, 3, 14, and 15.

III. CONCLUSION

For the foregoing reasons, we have determined that there is a reasonable likelihood that the Petitioner would prevail with respect to at least one of the claims challenged in the Petition. We therefore institute trial as to all challenged claims on all grounds stated in the Petition.

IV. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of the '494 patent is hereby instituted for all of the challenged claims on all of the asserted grounds; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this Decision.

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Patent 8,898,494 B2

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