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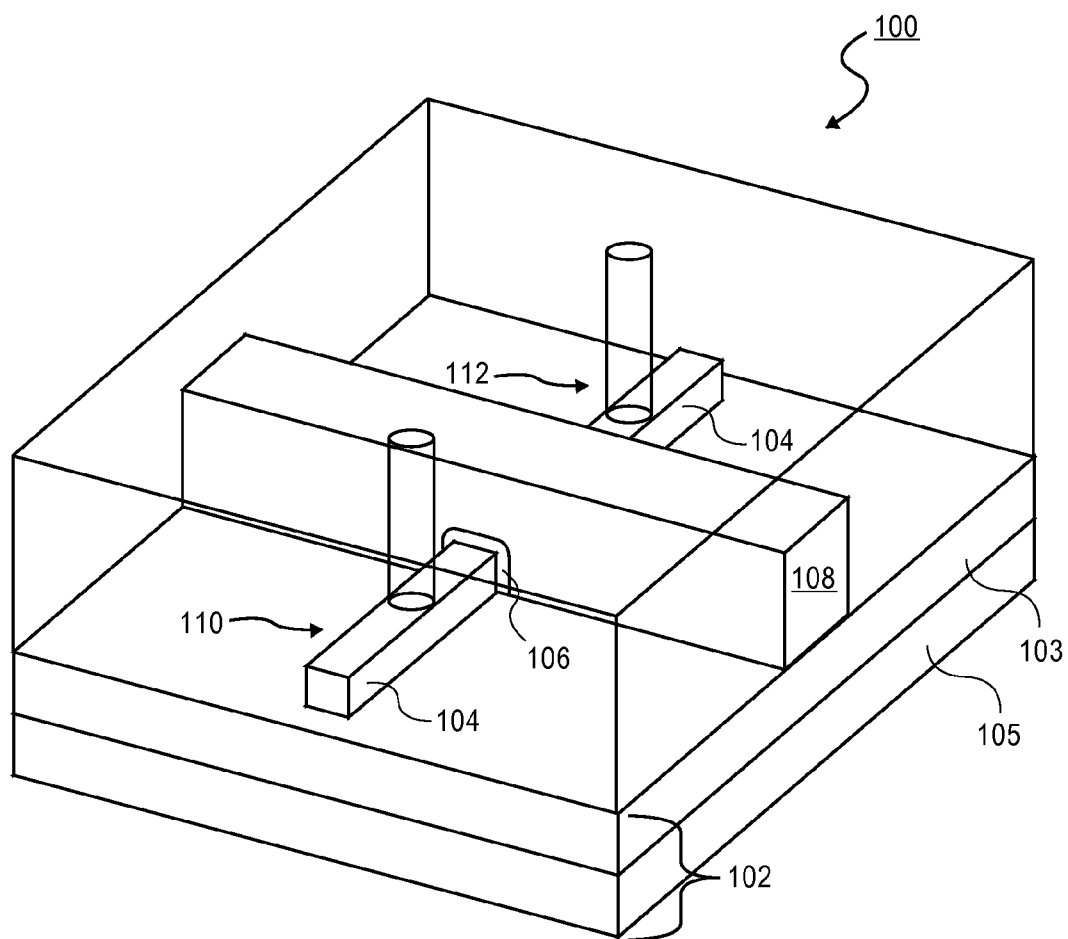
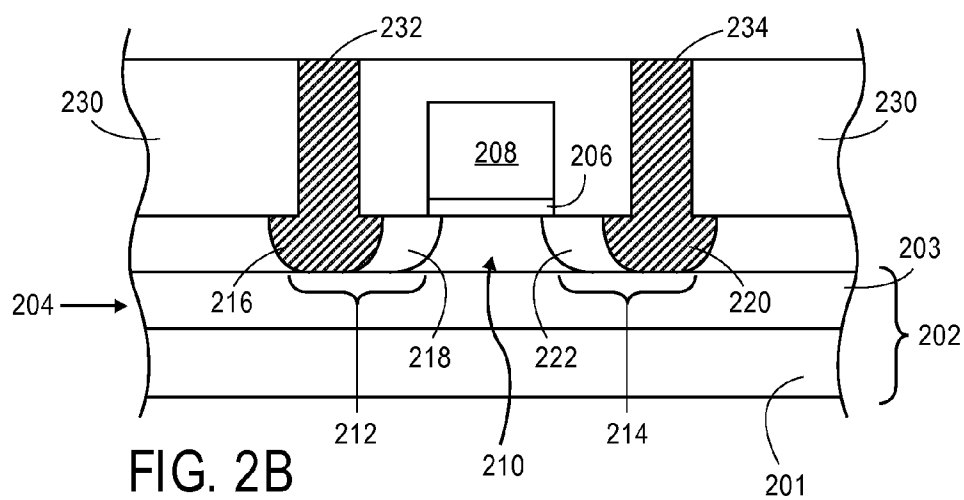
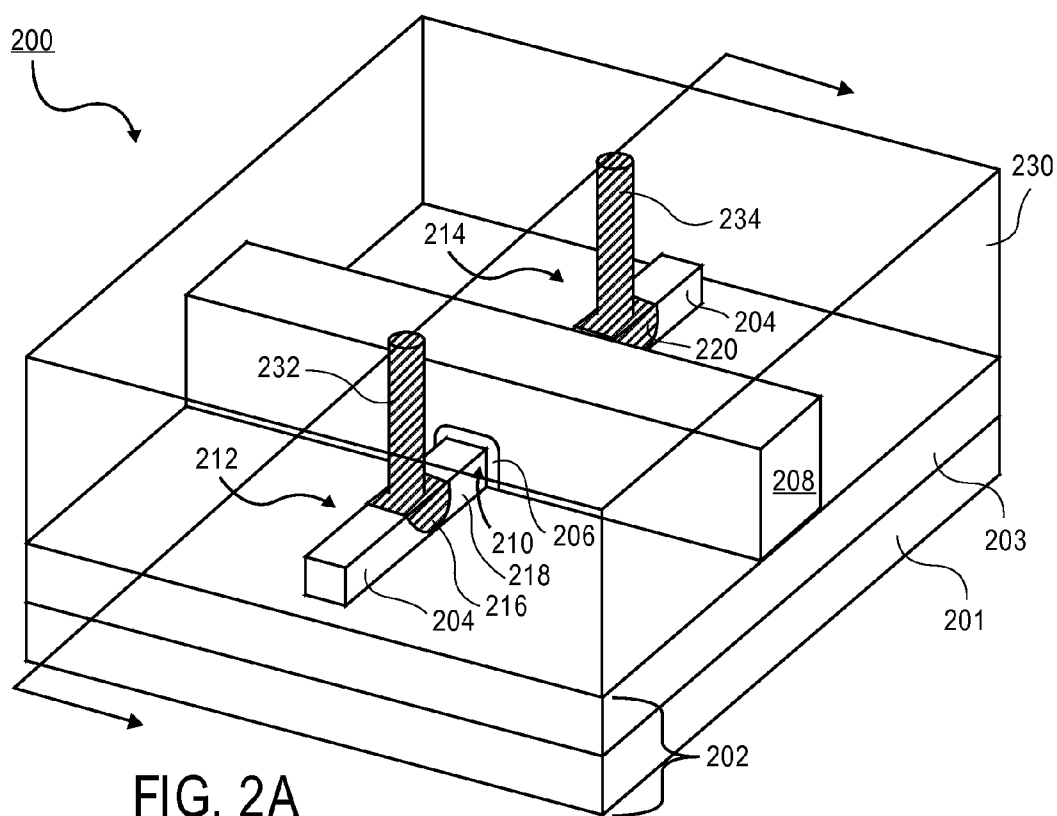
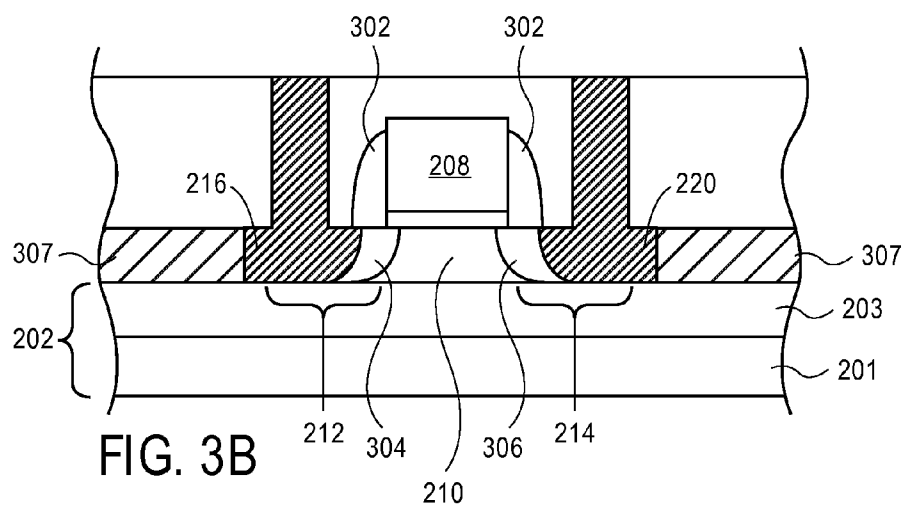
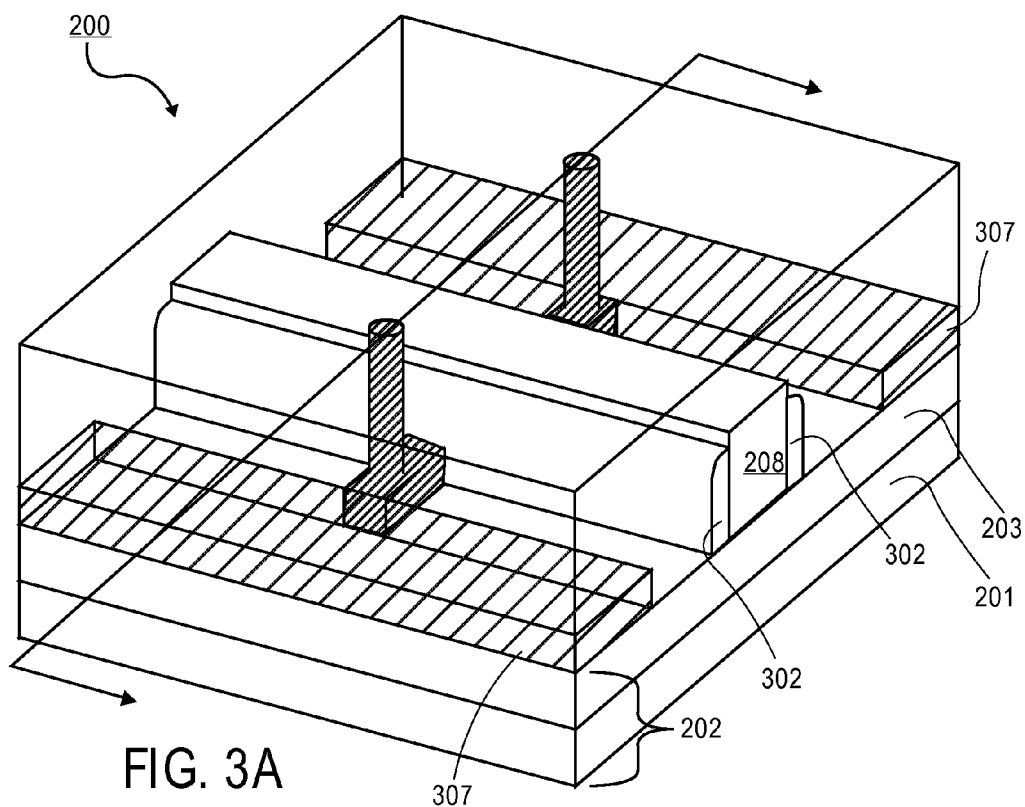
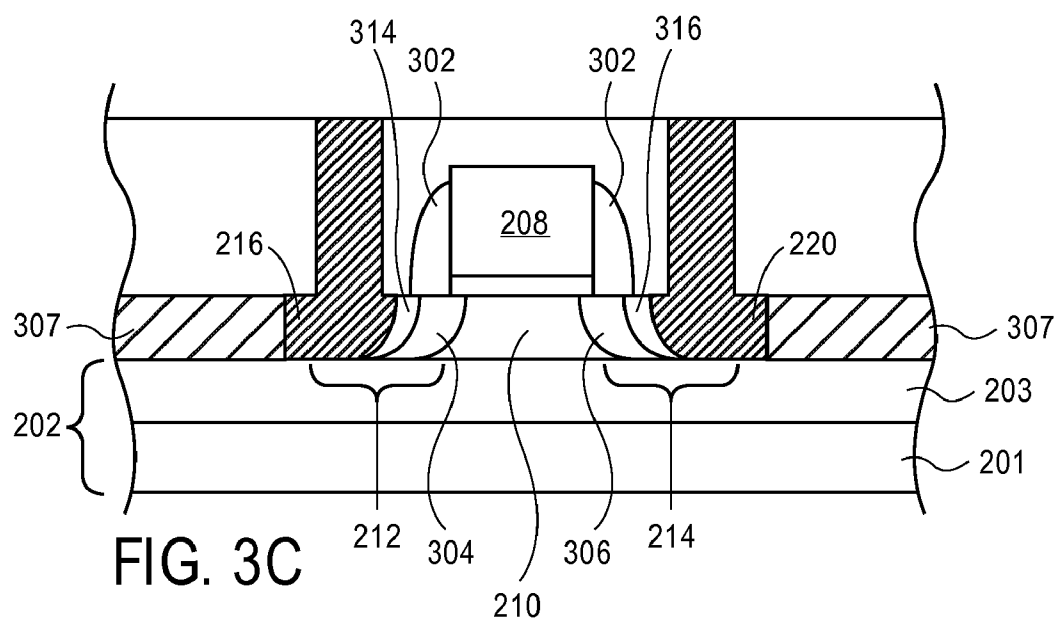


FIG. 1
(PRIOR ART)







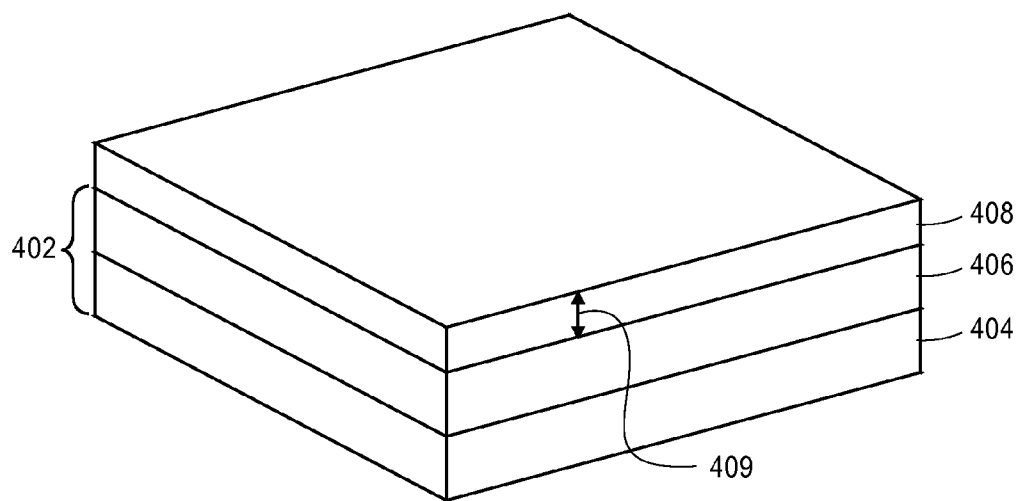


FIG. 4A

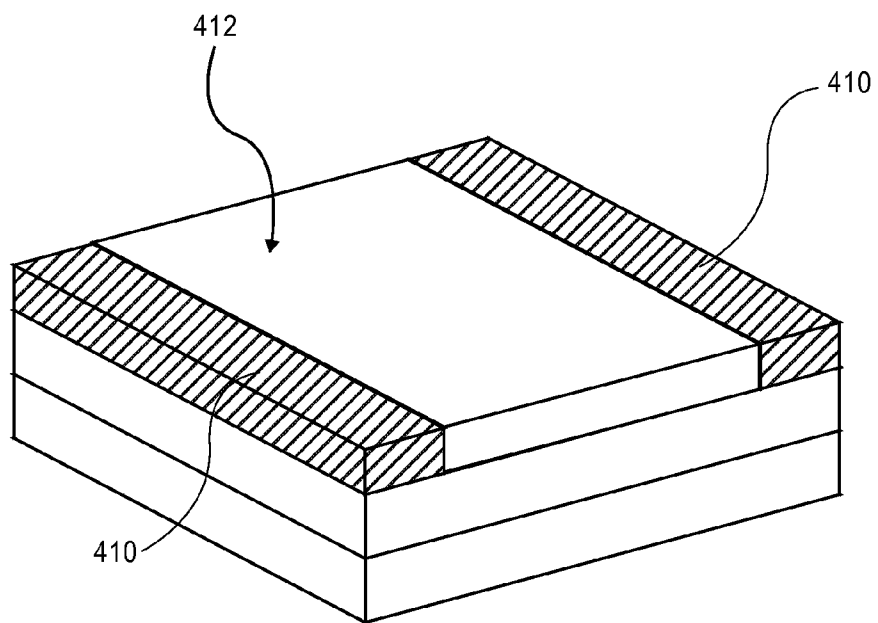


FIG. 4B

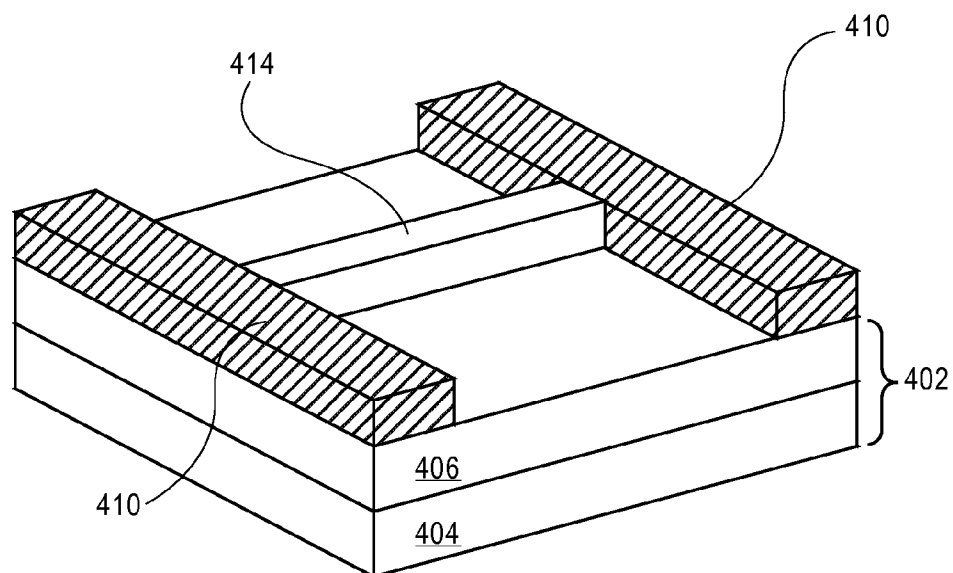


FIG. 4C

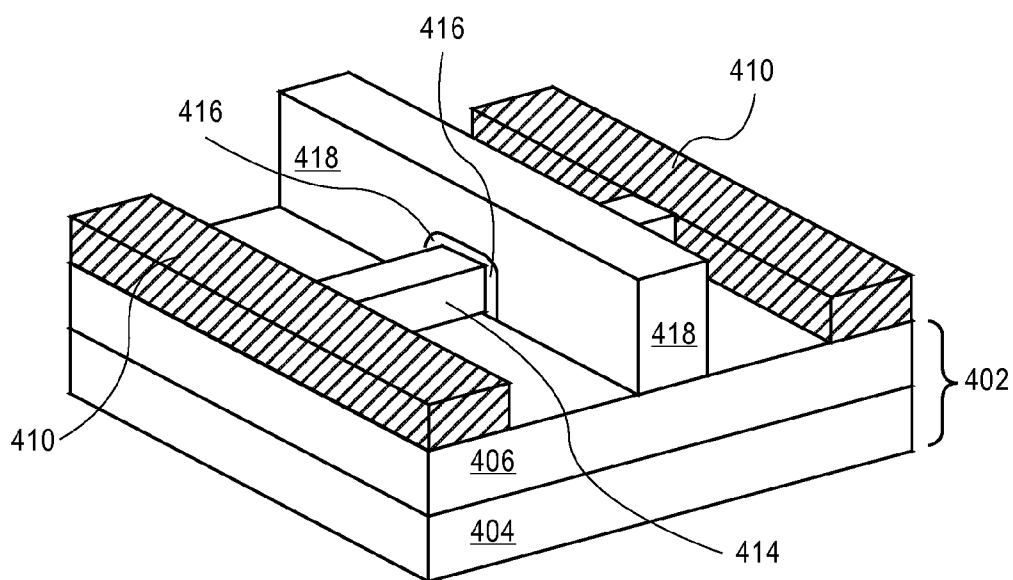


FIG. 4D

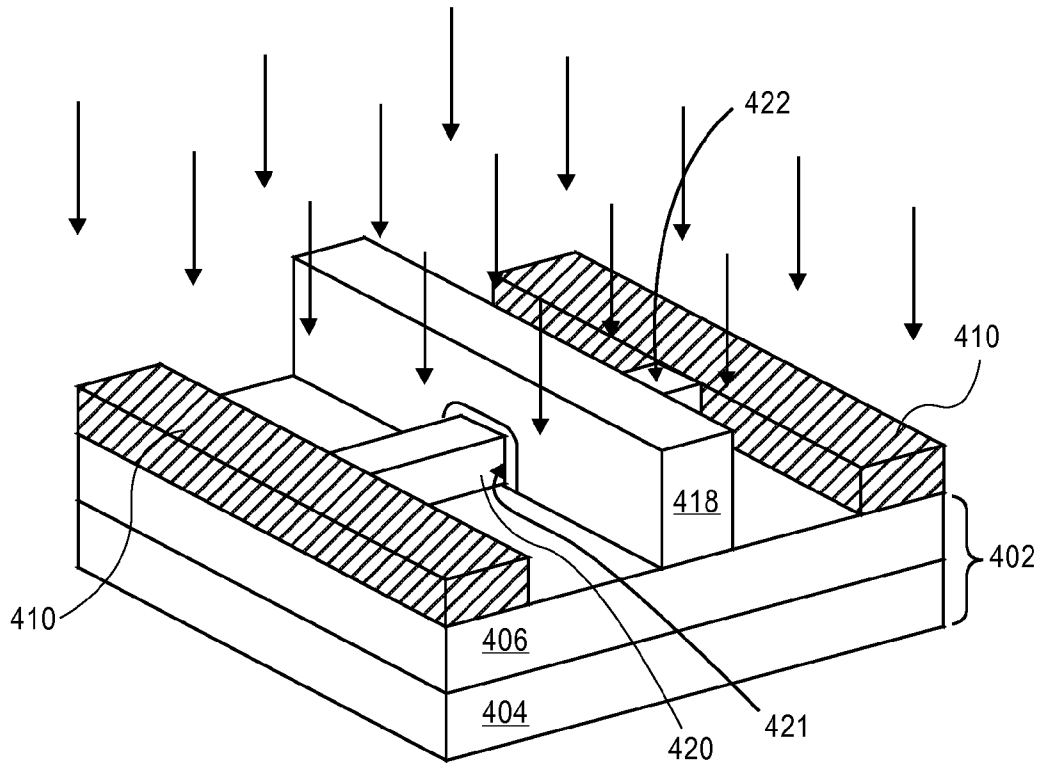


FIG. 4E

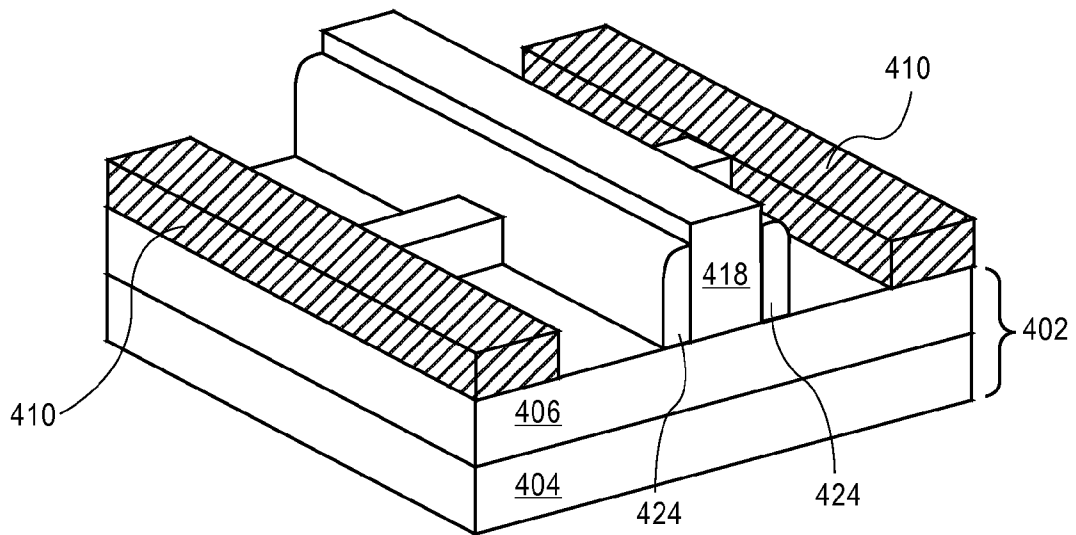


FIG. 4F

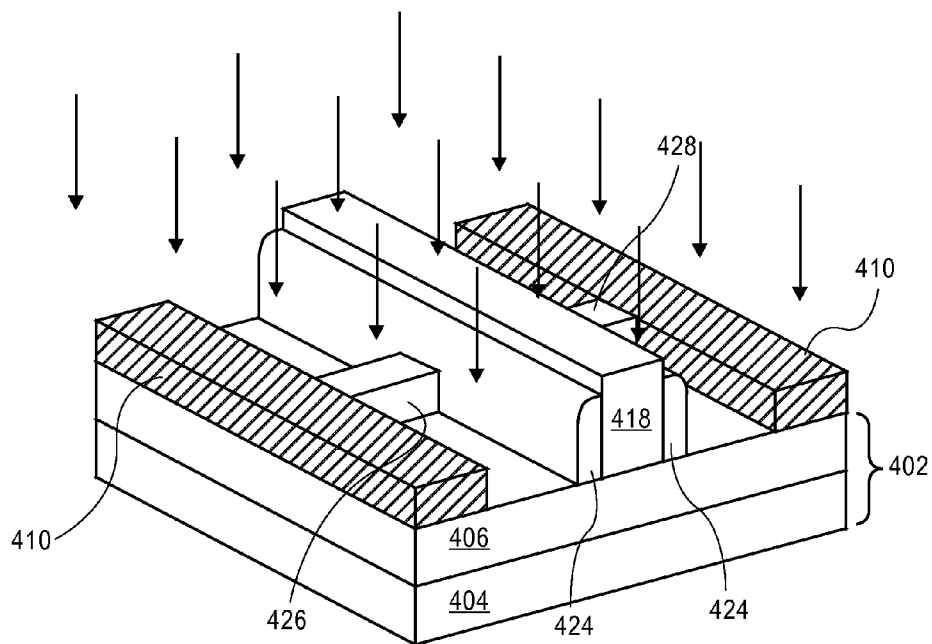


FIG. 4G

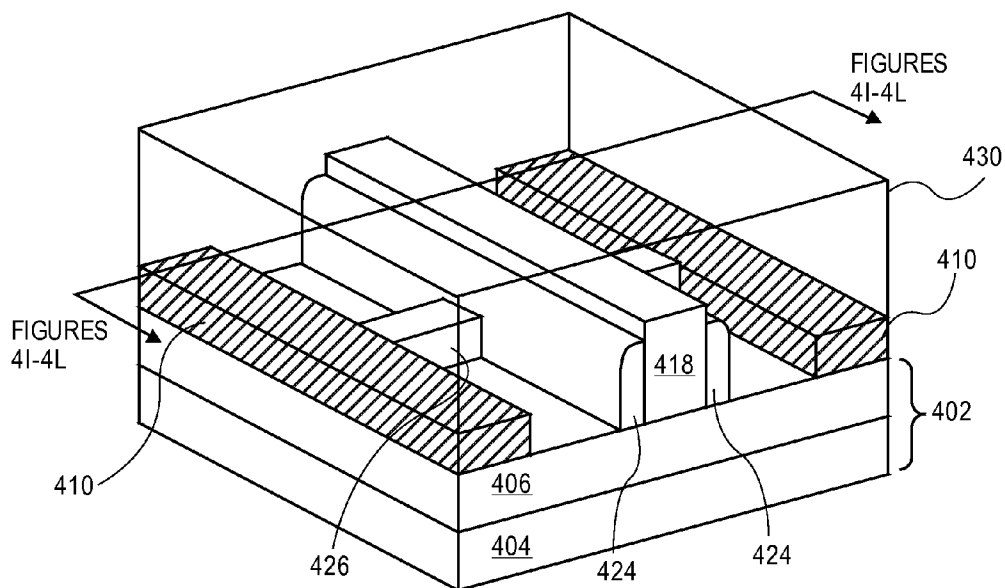


FIG. 4H

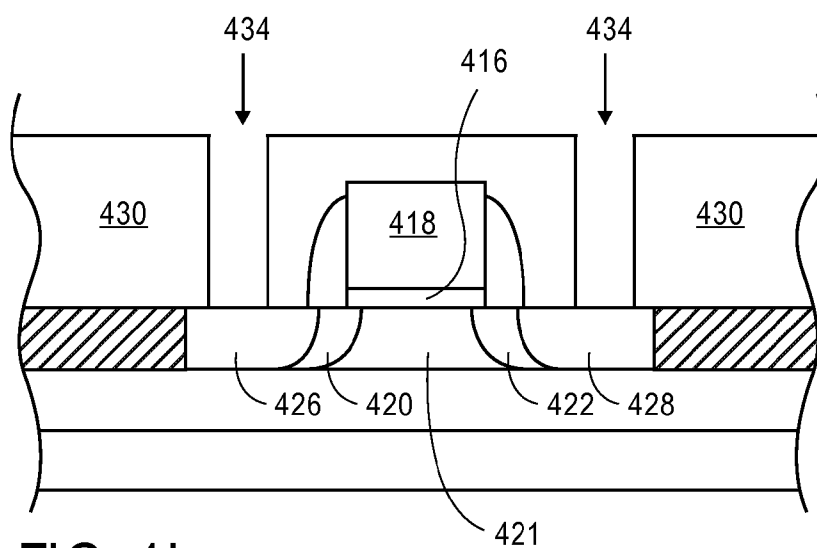


FIG. 4I

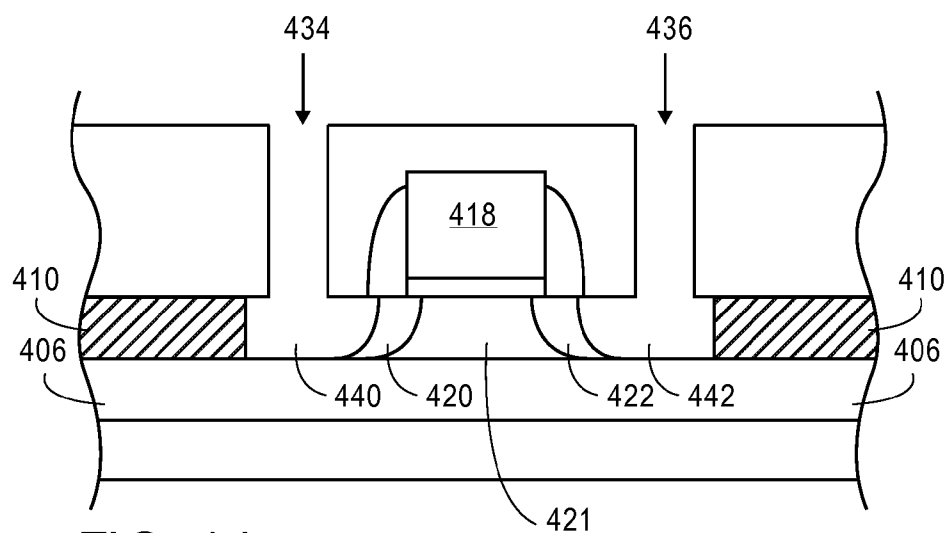


FIG. 4J

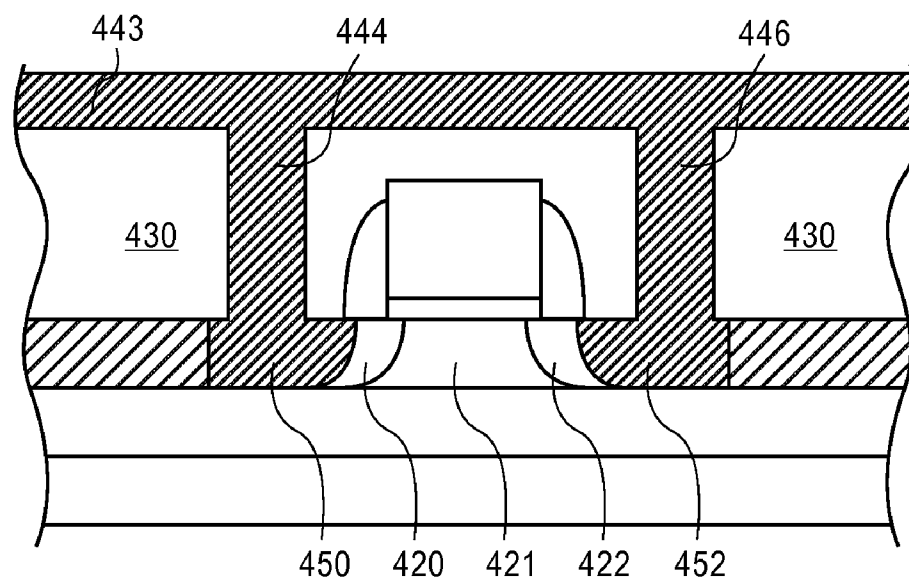


FIG. 4K

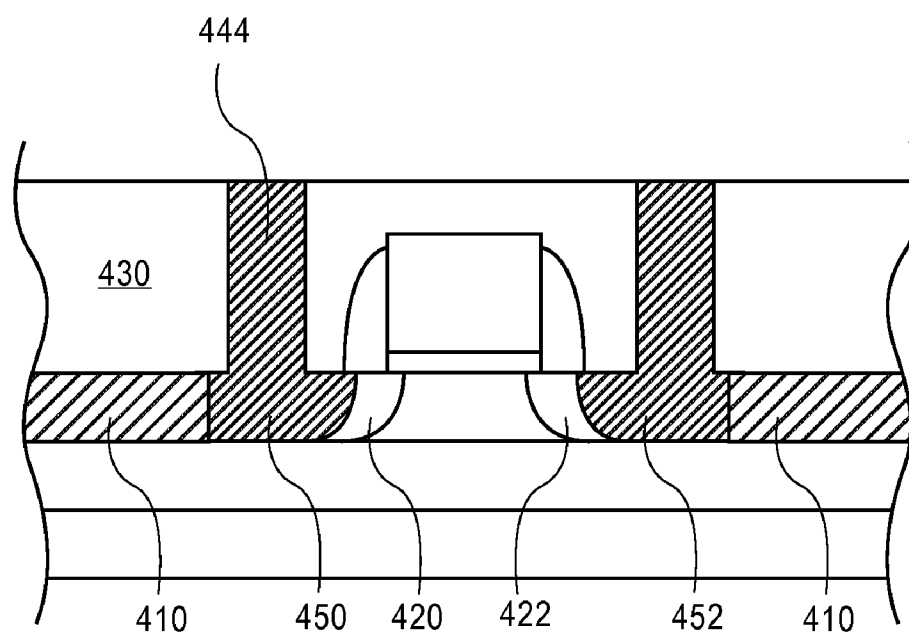


FIG. 4L

FIELD EFFECT TRANSISTOR WITH METAL SOURCE/DRAIN REGIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a divisional of U.S. patent application Ser. No. 11/080,765, filed Mar. 14, 2005, now U.S. Patent Application Publication No. US 2006-0202266, published Sep. 14, 2006, the entire contents of which are hereby incorporated by reference herein.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to the field of semiconductor devices and more particularly to a semiconductor device having a source/drain region comprising a semiconductor portion and a metal portion.

[0004] 2. Discussion of Related Art

[0005] In order to increase the performance of modern integrated circuits, such as microprocessors, silicon on insulator (SOI) transistors have been proposed. Silicon on insulator (SOI) transistors have an advantage in that they can be operated in a fully depleted manner. Fully depleted transistors have an advantage of an ideal subthreshold gradient for optimized on-current/off-current ratios. An example of an proposed SOI transistor which can be operated in a fully depleted manner is a tri-gate transistor **100**, such as illustrated in FIG. 1. Tri-gate transistor **100** includes a silicon body **104** formed on insulating substrate **102** having a buried oxide layer **103** formed on a monocrystalline silicon substrate **105**. A gate dielectric layer **106** is formed on the top and sidewalls of silicon body **104** as shown in FIG. 1. A gate electrode **108** is formed on the gate dielectric layer and surrounds the body **104** on three sides essentially providing a transistor **100** having three gate electrodes (G1, G2, G3) one on each side of silicon body **104** and one on the top surface of the silicon body **104**. A source region **110** and a drain region **112** are formed in the silicon body **104** on opposite sides of the gate electrode **108** as shown in FIG. 1. An advantage of the tri-gate transistor **100** is that it exhibits good short channel effects (SCE). One reason tri-gate transistor **100** has good short channel effects is that the nonplanarity of the device places the gate electrode **108** in such a way as to surround the active channel region. Unfortunately, as tri-gate devices become increasingly smaller, the external contact resistance (R_{ext}) is increasingly becoming more significant portion of the overall device resistance. This is particularly problematic in three dimensional transistors (formed both by etching of Si wafer, or by chemical synthesis of nanowires), where the source region **110** and drain region **112** are formed in the narrow silicon body **104**. Unfortunately, standard techniques for reducing contact resistance, such as by forming "raised" source/drain regions where additional epitaxial silicon is formed on the silicon body **104** is difficult to implement in nonplanar transistors. For example, it is difficult to grow "raised" epitaxial source/drain regions on the sides of the silicon body **104**. For these reasons the devices suffer from high R_{ext} and degraded performance.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is an illustration of a cross-sectional view of a nonplanar transistor.

[0007] FIG. 2A is an illustration of an overhead/side view of a nonplanar transistor having a metal source and drain region in accordance with the present invention.

[0008] FIG. 2B is a cross-sectional view of a transistor illustrated in FIG. 2A taken through the semiconductor body.

[0009] FIG. 3A is an illustration of an overhead/side view of a nonplanar transistor having a metal source/drain region in accordance with an embodiment of the present invention.

[0010] FIG. 3B is a cross-sectional view a transistor illustrated in FIG. 3A taken through the semiconductor body.

[0011] FIG. 3C is a cross-section view of a transistor having a source and drain extension each comprising a metal portion, a doped semiconductor contact portion and an extension portion.

[0012] FIGS. 4A-4L illustrate a method of forming a nonplanar transistor having metal portions of a source and drain regions in accordance with embodiment of the present invention.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0013] The present invention is a field effect transistor with metal source/drain regions and its method of fabrication. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. In other instances, well known semiconductor processes and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the present invention.

[0014] In embodiments of the present invention, include a metal oxide semiconductor field effect transistor having a pair of source/drain regions which each comprise a semiconductor portion and a metal portion. In an embodiment of the present invention, a replacement source/drain technique is used to etch away a portion of the doped source/drain regions so that they can be replaced with a high conductivity metal, such as platinum and palladium. In this way, a lower R_{ext} may be achieved since the metallic interconnect extends much closer towards the channel region. In an embodiment of the present invention, the metal portion of the source/drain region is made extremely close to the channel region such that the metal is formed adjacent to and in contact with the tip or source/drain extension portion of the source and drain regions. By forming the source region and drain region with a metal portion and a semiconductor portion allows for the scalable switching of the PNP or NPN junctions while bringing the high conductivity metal source/drain electrodes as close to the channel region as possible. In this way, the metal source and drain regions can extend all the way to the tips of the transistor enhancing the external conductivity while circumventing known disadvantages of metal source/drains in direct contact with the channel material (e.g., ambipolar conduction). Although the source/drain structure of the present invention is ideally suited for use in very small width and narrow transistors, such as nonplanar devices, the present invention can be utilized in any transistor where its small size or dimensions causes the transistor to have a high R_{ext}.

[0015] An example of a transistor **200** having source/drain regions with metal portions in accordance with an embodiment of the present invention is illustrated in FIGS. 2A and 2B. FIG. 2A is an illustration of an overhead/side view of transistor **200** while FIG. 2B is an illustration of a cross-sectional view of transistor **200** taken through the semiconductor body. Transistor **200** includes a semiconductor body

204, such as an epitaxial silicon body, formed on an insulating substrate **202**. The semiconductor body has top surface opposite a bottom surface formed on an insulating substrate and a pair of laterally opposite sidewalls. In an embodiment of the present invention, the semiconductor body has a height which is approximately equal to its width. A gate dielectric layer **206** is formed on the top surface and sidewalls of the semiconductor body **204** as shown in FIG. 2A. A gate electrode **208** is formed on and around the gate dielectric layer **206** formed on the top surface and sidewalls of the semiconductor body **204**. The gate electrode **208** surrounds the channel region **210** of the semiconductor body **204** illustrated in FIG. 2A.

[0016] A source region **212** and a drain region **214** are formed in the semiconductor body **204** on opposite sides of the gate electrode **208** as shown in FIGS. 2A and 2B. The source region **212** includes a metal portion **216** and a doped semiconductor portion **218** and drain region **214** includes a metal portion **220** and a doped semiconductor portion **222**. The portion of the semiconductor body **204** located between the source region **212** and drain region **214** defines a channel region **210** of transistor **200**. The doped semiconductor portions **218** and **222** contact the channel region **210** of the semiconductor device. In an embodiment of the present invention, the metal portions **216** and **220** of the source and drain regions **212** and **214**, respectively, extend as close as possible to the channel region **210** without actually contacting the channel region. In an embodiment of the present invention, the metal portion **216** and **220** are offset from the channel region **210** by doped semiconductor portions **218** and **222** by approximately 5 nanometers. In an embodiment of the present invention, the doped semiconductor regions have a doping concentration of between $1\text{e}20$ and $1\text{e}21/\text{cm}^3$. In an embodiment of the present invention, the doped semiconductor portions **218** and **222** are doped to the opposite conductivity type than the dopant conductivity of the channel region **210** of the semiconductor body **204**. In an embodiment of the present invention, metal regions **216** and **220** and the doped semiconductor regions **218** and **222** of the source and drain regions **212** and **214** extend completely through the semiconductor body **204** and contact the insulating substrate **202**. In an embodiment of the present invention, the metal portions **216** and **220** are formed from a high conductivity metal. In an embodiment of the present invention, the metal portion **216** for the source region **212** and the metal portion **220** of the drain region **214** are formed from a material which forms favorable "Schottky barrier" properties with doped semiconductor portions **218** and **222** of the source and drain regions. In an embodiment of the present invention, when semiconductor portions **218** and **222** are silicon the metal portion may be platinum. In an embodiment of the present invention, when semiconductor **218** and **222** are carbon nanotubes the metal portions may be palladium. In an embodiment of the present invention, when forming a PFET (a p type field effect transistor) where the doped portions of source and drain regions are doped to a p type conductivity and the majority carriers are holes, the metal portions **216** and **220** of the source region **212** and drain region **214** can be a metal, such as but not limited to palladium and platinum. In an embodiment of the present invention, when forming NFET (an n type field effect transistor) where the doped source and drain regions are doped to an n type conductivity and the majority carriers are electrons, the metal portions of the source and drain region can be fabricated from a metal, such as but not limited to aluminum

and titanium. It is to be appreciated that the source region **212** and drain region **214** can be collectively referred to as a pair of source/drain regions.

[0017] As shown in FIGS. 2A and 2B, an interlayer dielectric layer **230**, such as but not limited to a silicon dioxide layer or a low-K dielectric, such as a fluorine doped silicon dioxide, a carbon doped oxide layer or a zeolite dielectric layer is formed over and around transistor **200**. The interlayer dielectric layer **230** isolates transistor **200** from the upper levels of metallization used to interconnect the various transistors **200** formed on substrate **202** into functional integrated circuits, such as microprocessors, digital signal processors and memory devices. Metal plugs **232** and **234** are formed through the interlayer dielectric layer **230** and contact the metal portions **216** and **220** of the source and drain regions so electrical contact can be made thereto.

[0018] In an embodiment of the present invention, as illustrated in FIGS. 3A and 3B, transistor **200** can further include a pair of sidewall spacers **302** which are formed along and adjacent to the laterally opposite sidewalls of gate electrode **208**. Sidewall spacers **302** can be formed from any suitable insulating layer, such as but not limited to silicon dioxide, silicon nitride or composite stack thereof. In an embodiment of the present invention, spacers **302** have a width of between 5-20 nanometers. In an embodiment of the present invention, transistor **200** includes a source extension or tip **304** and a drain extension or tip region **306**. The source extension region **304** and drain extension region **306** are formed in the semiconductor body and are doped to n type conductivity for an NFET and doped to a p type conductivity for a PFET. The source and drain extensions are located beneath the sidewall spacers and extend slightly beneath the sidewalls of the gate electrode **208**. In an embodiment of the present invention, the source extension and drain extension have a doping concentration level of between $5\text{e}19$ - $5\text{e}20/\text{cm}^3$. In an embodiment of the present invention, the metal portion **216** of the source region **212** and the metal portion **220** of the drain region **214** extend slightly beneath the sidewall spacers and are in contact with the source and drain extension regions **304** and **306**, respectively, as shown in FIG. 3B.

[0019] In an embodiment of the present invention, isolation regions **307** are formed on insulating substrate **202** in order to isolate transistor **200** from adjacent transistors formed on substrate **202**. Isolation regions **307** can be formed from an insulating oxide film, such as silicon dioxide. In an embodiment of the present invention, the metal portion **216** of the source region **212** and the metal portion **220** of the drain region **214** are formed in contact with isolation region **306** as well as in contact with the source and drain extension regions **304** and **306**, respectively.

[0020] In an embodiment of the present invention, the source region **212** further includes a source contact region **314** and a drain contact region **316** formed in semiconductor body **204**. The source and drain contact regions **314** and **316** are heavily doped regions. Heavily doped contact region **314** and **316** are doped to the same conductivity type as the source and drain extensions **304** and **306**, but are typically doped to a higher concentration level. In an embodiment of the present invention, the source and drain contact region have a doping concentration between $1\text{e}20$ - $1\text{e}21/\text{cm}^3$. The heavily doped source and drain contact region **314** and **316** are formed between the source/drain extension regions **304** and **306**, and the metal portions **216** and **220** as illustrated in FIG. 3C. As such, in an embodiment of the present invention, the metal

portion **216** of the source region **212** is formed in direct contact with the heavily doped source contact region **314** and the metal portion **220** of the drain region **214** is in direct contact with the heavily doped drain contact region **316** as illustrated in FIG. 3C.

[0021] Gate electrode **208** can be formed of any suitable gate electrode material. In an embodiment of the present invention, gate electrode **208** comprises a polycrystalline silicon doped to a concentration density between 1×10^{19} to 1×10^{20} atom/cm³. In an embodiment of the present invention, the gate electrode can be a metal gate electrode, such as but not limited to tungsten, tantalum, titanium and their nitrides. In an embodiment of the present invention, the gate electrode is formed from a material having a midgap work function between 4.6 to 4.8 eV. It is to be appreciated, that gate electrode **208** need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a polycrystalline silicon/metal electrode or a metal/polycrystalline silicon electrode.

[0022] Semiconductor body **204** can be formed of any well known semiconductor material, such as but not limited to silicon (Si), germanium (Ge), silicon germanium (Si_xGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb, and carbon nanotubes. Semiconductor body **204** can be formed of any well known material which can be reversely altered from an insulating state to a conductive state by applying external electrical controls. Semiconductor body **204** is ideally a single crystalline film when the best electrical performance of transistor **200** is desired. For example, semiconductor body **204** is a single crystalline film when transistor **200** is used in high performance applications, such as a high density circuit, such as microprocessors. Semiconductor body **204**, however, can be a polycrystalline film when transistor **200** is used in applications requiring less stringent performance, such as in liquid crystal displays.

[0023] In an embodiment of the present invention, substrate **202** is an insulating substrate which includes a lower monocrystalline silicon substrate **201** upon which is formed in insulating layer **203**, such as silicon dioxide film. Transistor **200**, however, can be formed on any well known insulating substrate, such as a substrate formed from silicon dioxide, nitrides, oxides and sapphires. In an embodiment of the present invention, substrate **202** can be a semiconductor substrate, such as but not limited to a monocrystalline silicon substrate and a gallium arsenide substrate.

[0024] In an embodiment of the present invention, the channel region **210** is intrinsic or undoped monocrystalline silicon. In an embodiment of the present invention, the channel region **210** is doped monocrystalline silicon. When channel region **210** is doped, it is typically doped to a conductivity level between 1×10^{16} to 1×10^{19} atom/cm³. When channel region **210** is doped, it is typically doped to the opposite conductivity type of the doped semiconductor portion of the source region **212** and the doped semiconductor portion drain region **214**.

[0025] Gate dielectric layer **206** is formed on and around the sides of semiconductor body **204** as shown in FIG. 2A. Gate dielectric layer **206** can be any well known gate dielectric layer. In an embodiment of the present invention, the gate dielectric layer is a silicon dioxide (SiO₂), silicon oxynitride (SiO_xN_y), or a silicon nitride (Si₃N₄) dielectric layer. In an embodiment of the present invention, the gate dielectric layer **206** is a silicon oxynitride film formed to a thickness between 5-20 Å. In an embodiment of the present invention, gate

dielectric **206** is a high k gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum pentaoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide and various silicates or other high k dielectrics, such as lead zirconate titanate (BZT) and barium strontium titanate (BST). (For the purpose of the present invention, a high k dielectric layer is any dielectric film having a dielectric constant k greater than silicon dioxide (k=4.0) and ideally greater than 10).

[0026] A method of fabricating a field effect transistor with source and drain regions having metal portions in accordance with embodiments of the present invention is illustrated in FIGS. 4A-4L. The fabrication of the field effect transistor begins with a substrate **402**. A silicon or semiconductor film **408** is formed on substrate **402** as shown in FIG. 4A. In an embodiment of the present invention, the substrate **402** is an insulating substrate such as shown in FIG. 4A. In an embodiment of the present invention, insulating substrate **402** includes a lower monocrystalline silicon substrate **404** and a top insulating layer **406**, such as a silicon dioxide film or silicon nitride film. Insulating layer **406** isolates semiconductor film **408** from substrate **404** and in an embodiment is formed to a thickness between 200-2000 Å. Insulating layer **406** is sometimes referred to as "a buried oxide" layer. When a silicon or semiconductor film **408** is formed on an insulating substrate **402**, a silicon or semiconductor-on-insulator (SOI) substrate is created. In other embodiments of the present invention, substrate **402** can be a semiconductor substrate, such as but not limited to a silicon monocrystalline substrate and a gallium arsenide substrate. Although semiconductor film **408** is ideally a silicon film, in other embodiments it can be other types of semiconductor films, such as but not limited to germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb as well as carbon nanotubes.

[0027] In an embodiment of the present invention, semiconductor film **408** is an intrinsic (i.e., undoped) silicon film. In other embodiments, semiconductor film **408** is doped to a p type or n type conductivity with a concentration level between 1×10^{16} to 1×10^{19} atoms/cm³. Semiconductor film **408** can be insitu doped (i.e., doped while it is deposited) or doped after it is formed on substrate **402** by, for example, ion implantation. Doping after formation enables both PFET and NFET devices to be fabricated easily on the same insulating substrate. The doping level of the semiconductor film **408** determines the doping level of the channel region of the device. In an embodiment of the present invention, semiconductor film **408** is formed to a thickness which is approximately equal to the height desired for the subsequently formed semiconductor body or bodies of the fabricated transistor. In embodiments of the present invention, semiconductor film **408** has a thickness or height **409** of less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, semiconductor film **408** is formed to a thickness approximately equal to the gate "length" desired of the fabricated transistor. In an embodiment of the present invention, semiconductor film **408** is formed thicker than the desired gate length of the device. In an embodiment of the present invention, a semiconductor film **408** is formed to a thickness which will enable the fabricated transistor to be operated in a fully depleted manner for a desired gate length (L_g).

[0028] Semiconductor film **408** can be formed on insulating substrate **402** in any well known method. In one method of forming a silicon-on-insulator substrate, known as the

“SIMOX” technique, oxygen atoms are implanted at a high dose into a single crystalline silicon substrate and then annealed to form the buried oxide **406** within the substrate. The portion of the single crystalline silicon substrate above the buried oxide becomes a silicon film. In another method an epitaxial silicon film transfer technique which is generally referred to as bonded SOI may be utilized to form a SOI substrate.

[0029] In an embodiment of the present invention, as shown in FIG. 4B, isolation regions **410** can be formed in the semiconductor film **408** to isolate the various transistors formed in semiconductor film **408** from one another. Isolation regions **410** can be formed by etching away portions of the semiconductor film **408** adjacent to the transistor fabrication area **412** in semiconductor film **408**. Well known photolithography and etching techniques can be used to remove the semiconductor film at locations where isolation regions **410** are desired. An insulating film, such as but not limited to silicon dioxide, can then be blanket deposited into the areas where the semiconductor film **408** has been etched out as well as on over the semiconductor film **408** in the device fabrication area **412**. The deposited insulating film can then be polished back by, for example, chemical mechanical polishing (CMP) to remove the insulating film from the device fabrication area **412** and thereby form isolation regions **410** which are planar with the top surface of the semiconductor film **408** in the device fabrication area **412**. Other well known and suitable techniques may be utilized to form isolation regions **410**.

[0030] Next, a semiconductor body **414** is formed from semiconductor film **408** as shown in FIG. 4C. Semiconductor body **414** can be formed by forming a photoresist mask over the locations of semiconductor film **408** where a semiconductor body **414** is desired. A photoresist mask can be formed with well known photolithography techniques including masking, exposing and developing a blanket deposited photoresist film. Semiconductor film **408** would then be etched in alignment with the photoresist mask to form semiconductor body **414**. Any well known semiconductor etching techniques, such as anisotropic plasma etching or reactive ion etching, can be used to etch semiconductor film **408** in alignment with the photoresist mask to form semiconductor body **414**. In an embodiment of the present invention, the semiconductor body is etched so that it has a width (i.e. distance between laterally opposite sidewalls) which is approximately equal to its height.

[0031] Next, as shown in FIG. 4D, a gate dielectric layer **416** is formed on and around semiconductor body **414**. The gate dielectric layer **416** is formed on a top surface of the semiconductor body as well as on the laterally opposite sidewalls of the semiconductor body **414**. The gate dielectric layer **416** can be a deposited dielectric or a grown dielectric. In an embodiment of the present invention, the gate dielectric layer **416** is a silicon dioxide dielectric film grown with a dry/wet oxidation process. In an embodiment of the present invention, the silicon oxide film is grown to a thickness between 5-15 Å. In an embodiment of the present invention, the gate dielectric layer is deposited dielectric, such as but not limited to a high dielectric constant film, such as a metal oxide dielectric, such as tantalum pentoxide, titanium oxide, hafnium oxide, zirconium oxide, aluminum oxide and various silicates or other high k dielectrics, such as lead zirconate titanate (BZT) and barium strontium titanate (BST). A high dielectric constant film can be formed by any well known

technique, such as but not limited to chemical vapor deposition (CVD) and atomic layer deposition (ALD).

[0032] Next, as also shown in FIG. 4D, a gate electrode **418** is formed. Gate electrode **418** is formed on gate dielectric layer **416** formed on the top surface of semiconductor body **414** and is formed on or adjacent to the gate dielectric layer **416** formed on or adjacent to the sidewall of the semiconductor body **414** as shown in FIG. 4D. The gate electrode **418** has a top surface opposite a bottom surface formed on insulating substrate **402** and has a pair of laterally opposite sidewalls which run perpendicular to the sidewalls of semiconductor body **414**. Gate electrode **418** can be formed by blanket depositing a suitable gate electrode material to a thickness between 200-3000 Å. The gate electrode material is then patterned with well known photolithography and etching techniques to form a gate electrode **418** from the gate electrode material. In an embodiment of the present invention, the gate electrode material comprises a polycrystalline silicon. In an embodiment of the present invention, the gate electrode material comprises a polycrystalline silicon germanium alloy. In yet another embodiment of the present invention, the gate electrode material can comprise a metal film, such as tungsten, tantalum and their nitrides. Alternatively, to a subtractive approach for forming the gate electrode **418**, other techniques may be utilized.

[0033] Next, a pair of source/drain regions are formed in the semiconductor body **414** on opposite sides of gate electrode **418**. As stated above, the source and drain regions each comprise a doped semiconductor portion and a metal portion. First, the semiconductor portions of the source/drain regions can be formed. In an embodiment of the present invention, the doped semiconductor portions include tip or source/drain extension regions. Source and drain extension regions **420** and **422** can be formed by placing dopants into the semiconductor body **414** on both sides of gate electrode **418** as shown in FIG. 4E. For a p type transistor, the semiconductor body is doped to a p type conductivity and to a concentration of between 1×10^{20} - 1×10^{21} atoms/cm³. For an n type transistor, the semiconductor body is doped with n type conductivity ions to a concentration between 1×10^{20} - 1×10^{21} atoms/cm³. In an embodiment of the present invention, the silicon body is doped by ion implantation. In an embodiment of the present invention, the ion implantation occurs in a vertical direction (i.e., a direction perpendicular to substrate **402**) as shown in FIG. 4E. When gate electrode **418** is a polysilicon gate electrode, it can be doped during the ion implantation process. Gate electrode **418** acts as a mask to prevent the ion implantation step from doping the channel region **421** of the transistor. The channel region **421** is the portion of the semiconductor body **414** located beneath or surrounded by gate electrode **418**. In other embodiments or other methods, such as solid source diffusion may be used to dope the semiconductor body **414** to the source and drain extension regions **420** and **422**.

[0034] Next, in an embodiment of the present invention, dielectric sidewall spacers **424** can be formed on the sidewalls of gate electrode **418**. Sidewall spacers can be used to offset heavy source/drain contact implants. Spacers can be formed by blanket depositing a conformal dielectric film, such as but not limited to silicon nitride, silicon oxide, silicon oxynitride or combinations thereof over the substrate of FIG. 4E. The spacer dielectric film is deposited in a conformal manner so that it forms to substantially equal thickness on vertical surfaces, such as sidewalls of the gate electrode **418** as well as on horizontal surfaces, such as on the top surface of silicon body

414 and gate electrode **418**. In an embodiment of the present invention, the dielectric film is a silicon nitride film formed by a hot wall lower pressure chemical vapor deposition (LPCVD) process. The deposited thickness of the dielectric film determines the width or thickness of the formed spacers. In an embodiment of the present invention, the spacer dielectric film is formed to a thickness between 20-200 Å. The spacer dielectric film can then be anisotropically etched by, for example, plasma etching or reactive ion etching to form sidewall spacers **424**. The anisotropic etch removes the dielectric film from horizontal surfaces and leaves the dielectric sidewall spacers adjacent to vertical surfaces, such as the sidewalls of gate electrode **418**. The result is the formation of sidewall spacers **424** which run along the laterally opposite sidewalls of gate electrode **418** as shown in FIG. 4F.

[0035] Next, if desired, heavy source/drain contact implants can be made to form heavily doped semiconductor film **414**. Heavily doped source/drain contact regions can be formed by ion implantation with a vertical ion implantation process. The ion implantation process dopes the semiconductor body **414** located adjacent to the sidewall spacers to a concentration between 1×10^{20} - 1×10^{21} atoms/cm³ to form source contact region **426** and drain contact region **428**. Sidewall spacers **424** offset the source/drain contact implantation step and define the tip regions as the regions of the doped semiconductor body **414** beneath sidewall spacers **424**. The contact regions are the regions of the semiconductor body which are adjacent to the outside edges of the sidewall spacers **424**.

[0036] Next, an interlayer dielectric (ILD) **430** is blanket deposited over the substrate as shown in FIG. 4H. The interlayer dielectric may be referred to as ILD0 because it is used to isolate the transistor from a subsequently formed first level of metallization. The interlayer dielectric (ILD) **430** is formed above isolation regions **410** and over and above gate electrode **418** as well as above and around the exposed portion of semiconductor body **414**. The interlayer dielectric **430** fills the gap made between semiconductor body **414**, isolation region **410** and the gate electrode/sidewall spacers **424/418**. Interlayer dielectric **430** is formed to a thickness sufficient to isolate gate electrode **418** and semiconductor body **414** from a first level of metallization subsequently formed on the top surface of the interlayer dielectric **430**. In an embodiment of the present invention, the interlayer dielectric **430** is formed to a thickness between 100 and 500 nm. Interlayer dielectric **430** can be formed from any suitable dielectric material, such as silicon dioxide, which can be used as an interlayer dielectric. Additionally, interlayer dielectric **430** need not be a single dielectric film and can be a composite dielectric formed from two or more dielectric layers. Additionally, prior to the formation of interlayer dielectric **430**, a stress providing layer, such as silicon nitride, can be formed over and around the transistor in order to place the channel region **421** of the device under stress to improve the carrier mobility therein. In an embodiment of the present invention, the interlayer dielectric **430** can be a low k dielectric (i.e., have a dielectric constant less than the dielectric constant of silicon dioxide which is approximately 4.0) in order to prevent capacitance coupling between adjacent contacts. In an embodiment of the present invention, an interlayer dielectric is formed from a low k material, such as but not limited to fluorine doped SiO₂, a carbon doped oxide (CDO), polyimides, and zeolites.

[0037] In an embodiment of the present invention, ILD **430** is formed of a material which can be selectively etched with

respect to semiconductor body **414** so that an opening can be etched into the semiconductor body without laterally etching into ILD **430** adjacent to the sidewalls of the semiconductor body **414**. In an embodiment of the present invention, interlayer dielectric **430** is formed from the same material, such as silicon dioxide, which is used to form isolation regions **410**. In an embodiment of the present invention, after depositing interlayer dielectric **430**, the dielectric layer can be planarized by, for example, chemical mechanical planarization in order to form the interlayer dielectric **430** with a planar top surface. Any suitable technique can be used to deposit the interlayer dielectric **430**, such as but not limited to chemical vapor deposition (CVD) and high density plasma (HDP) CVD.

[0038] Next, as illustrated in 4I-4L, contact openings are etched through interlayer dielectric **430** and into semiconductor body **414** and then filled with a metal to form the metal portions of the source and drain regions. It is to be appreciated that FIGS. 4I-4L illustrate a cross-sectional view taken through the semiconductor body **414** as set forth in FIG. 4H.

[0039] First, as illustrated in FIG. 4I, a pair of contact opening **434** and **436** is formed through interlayer dielectric and down to the source contact region **426** and the drain contact **428** of semiconductor body **414**. Well known photolithography techniques can be used to form a photoresist mask to define the locations where openings **434** and **436** are to be formed and then well known etching techniques can be used to etch the openings **434** and **436**. Any well known and suitable etching technique including dry etching and wet etching may be used to form openings **434** and **436**. In an embodiment of the present invention, when ILD **430** is a silicon dioxide film and semiconductor body **414** is silicon, an etchant comprising HF may be used. In an embodiment of the present invention, the etchant used to form contact openings **434** and **436** is selective semiconductor **414** so that it can etch through the interlayer dielectric **430** and essentially stop etching on the semiconductor body **414**. In an embodiment of the present invention, an etchant which has an etch selectivity ratio between silicon dioxide and silicon of at least 10:1 is used.

[0040] Next, as illustrated in FIG. 4J, openings **440** and **442** are etched into semiconductor body **414**. In an embodiment of the present invention, the semiconductor body etchant etches laterally towards the channel of the device. In an embodiment of the present invention, the etching of the openings **440** and **442** is continued until the tip or extension portions **420** and **422** of the source and drain regions are reached as illustrated in FIG. 4J. In an alternative embodiment of the present invention, the etching may not quite reach the tip portions **420** and **422** of the source and drain regions and may leave a portion of the heavily doped source/drain contact regions **426** and **428** as discussed earlier. Additionally, in an embodiment of the present invention, the openings **440** and **442** are etched vertically downward until they reach buried oxide layer **406** as illustrated in FIG. 4J. Additionally, in an embodiment of the present invention, the openings are etched laterally or horizontally outward until isolation regions **410** are reached as illustrated in FIG. 4J. In an embodiment of the present invention, the openings **440** and **442** are etched with an etchant which has a high selectivity to interlayer dielectric **430**, isolation regions **410** and buried oxide layer **406**. That is an etchant is used which etches semiconductor body **414** but not interlayer dielectric **430**, isolation regions **410** or buried oxide layer **406**. In this way, the openings **440** and **442** are securely contained between buried oxide layer **406**, the isolation

region **410** and the interlayer dielectric **430** as illustrated in FIG. **4J**. Any suitable wet or dry etching techniques may be utilized to form openings **440** and **442**. The etching process should be substantially isotropic in order to provide for lateral undercutting of openings **434** and **436** as illustrated in FIG. **4J**. In an embodiment of the present invention, when interlayer dielectric **430** and insulating layer **410** are oxide films and the semiconductor body is a silicon, then the silicon body can be etched to form openings **440** and **442** with an etchant comprising KOH.

[0041] Next, as illustrated in FIG. **4J**, openings **440** and **442** formed in semiconductor body **414** and contact openings **434** and **436** are filled with a metal film **443** to form source and drain contacts **444** and **446** and the metal portions **450** and **452** of the source and drain regions. The source and drain metal portions **450** and **452** make direct contact with highly doped semiconductor portion of the source and drain regions. In an embodiment of the present invention, the doped semiconductor portion is the tip or source/drain extension regions **420** and **422**. In an alternative embodiment of the present invention, the metal portions **450** and **452** make direct contact with the heavily doped source and drain contact regions **426** and **428**. Additionally, in an embodiment of the present invention, metal portions **450** and **452** are formed directly onto the buried oxide layer **406** and in an embodiment of the present invention, in contact the outside portions of isolation regions **410** as illustrated in FIG. **4K**. In an embodiment of the present invention, the metal **443** is formed by a conformal deposition process so that the contact openings **440** and **442** formed in the semiconductor body **414** can be completely filled with the metal film. A blanket deposition of a conformal metal film by, for example, chemical vapor deposition (CVD) or atomic layer deposition (ALD) will also deposit the film onto the top surface of the interlayer dielectric layer **430** as illustrated in FIG. **4K**. In an embodiment of the present invention, the metal film **443** is a low resistance, high conductivity metal film. In an embodiment of the present invention, the metal film **443** is a film which can form a Schottky contact with the doped semiconductor portion of the semiconductor body. In an embodiment of the present invention, when forming an NFET type device, the metal film can be a metal selected from the group consisting of aluminum and titanium. In an embodiment of the present invention, when forming PFET type device, the metal film can be a metal selected from the group consisting of palladium and platinum. In an embodiment of the present invention, when semiconductor body is formed from silicon the metal film can be platinum. In an embodiment of the present invention, when the semiconductor body is formed from carbon nanotubes, the metal film can comprise palladium and aluminum.

[0042] Next, as shown in FIG. **4L**, the metal film **443** formed on the top surface of the interlayer dielectric **430** is removed by well known techniques. Metal film **443** on the top surface of the interlayer dielectric area **430** can be removed by, for example, chemical mechanical planarization or by a plasma etch back process. This completes the fabrication of a field effect transistor having source and drain regions with metal portions to improve external resistance (Rext) of the device.

[0043] It is to be appreciated that although the present invention has been described with respect to a nonplanar transistor, such as a tri-gate transistor, the present invention is not to be limited to these types of transistors. For example, the present invention is equally applicable to the formation of

source and drain regions of a planar transistor where the gate electrode and gate dielectric layer are formed on a single surface of semiconductor film as is well known in the art. Additionally, the present invention is equally applicable to FINFET devices or dual gate devices where the gate electrode/gate dielectric is formed on two sides of the semiconductor body and not on the top surface of the semiconductor body as is well known in the art.

We claim:

1. A method of forming a transistor comprising:
 - forming a gate electrode having a pair of laterally opposite sidewalls on a gate dielectric layer formed on a semiconductor layer;
 - forming a pair of source/drain extensions in said semiconductor layer on opposite sides of said gate electrode;
 - forming a pair of sidewall spacers adjacent to said sidewalls of said gate electrode and on said source/drain extensions;
 - forming a pair of source/drain contact regions in said semiconductor layer on opposite sides of said sidewall spacers;
 - forming an interlayer dielectric adjacent to said sidewall spacers and over said source/drain contact regions;
 - etching a pair of contact openings through said interlayer dielectric to expose a portion of said source/drain contact regions;
 - etching away a portion of said source/drain contact regions to form a pair of etched-out source/drain contact regions; and
 - depositing a metal film into said contact openings and into said etched-out source/drain contact regions.
2. The method of claim 1 wherein said metal film in said etched-out source/drain contact regions directly contact said source/drain extensions.
3. The method of claim 1 wherein said metal film is formed beneath said sidewall spacers.
4. The method of claim 1 wherein said source/drain extensions are formed by ion implanting dopants in alignment with said sidewalls of said gate electrode.
5. The method of claim 1 wherein said source/drain contact regions are formed by ion implanting dopants into said semiconductor film in alignment with the outside edges of said sidewall spacers.
6. A method of forming a nonplanar transistor comprising:
 - forming a semiconductor body having a top surface opposite a bottom surface formed on an insulating layer of an insulating substrate, said semiconductor body having a pair of laterally opposite sidewalls;
 - forming a gate dielectric layer on the top surface and sidewalls of said semiconductor body;
 - forming a gate electrode having a pair of laterally opposite sidewalls on said gate dielectric layer and on the top surface of said semiconductor body and adjacent to said gate dielectric layer on said sidewalls of said semiconductor body;
 - forming a pair of source/drain extensions in said semiconductor body on opposite sides of said gate electrode;
 - forming a pair sidewall spacers adjacent to said gate electrode and on and adjacent to said source/drain extensions formed in said semiconductor body;
 - forming a pair of source/drain contact regions in said semiconductor body on opposite sides of said sidewall spacers;

forming an interlayer dielectric layer over and adjacent to said semiconductor body and adjacent to said sidewall spacers;
etching a pair of contact openings through said interlayer dielectric layer to said source/drain contact regions in said semiconductor body;
etching away a portion of said source/drain contact regions in said semiconductor body; and
depositing a metal film in said contact openings and in said etched away portion of said semiconductor body.

7. The method of claim 6 wherein said etching of said portion of said source/drain contact region in said semiconductor body etches until said insulating layer of said insulating substrate is reached.

8. The method of claim 7 wherein said metal film in said etched away portion of said semiconductor body contact said source/drain extension regions.

9. The method of claim 6 wherein said opening in said semiconductor body is larger than the contact opening formed through said interlayer dielectric.

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