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OPINION

# All About Interconnects

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*Why interconnects are becoming the performance bottleneck in advanced-node chips.*

DECEMBER 18TH, 2017 - BY: **LARRY ZHAO** ([HTTPS://SEMIENGINEERING.COM/AUTHOR/LARRY-ZHAO/](https://semiengineering.com/author/larry-zhao/))



It's well known that advanced chips contain billions of transistors – this is an incredible, mind-blowing fact to be sure – but did you know that large-scale integrated chips (about the size of a fingernail) can contain ~30 miles of interconnect “wires” in stacked levels? These wires function like highways or pipelines to transport electrons, connect transistors and other components to each other, and make them functional. And just as the speed you can drive your sports car depends (at least in part) on how clogged the freeway is, chip performance depends on the ability to move signals and power through these ultra-tiny wires. In fact, as the shrinking of feature dimensions (scaling) has continued, interconnects are now becoming the speed bottleneck in today's most advanced chips. So, let's spend a little time learning about them.

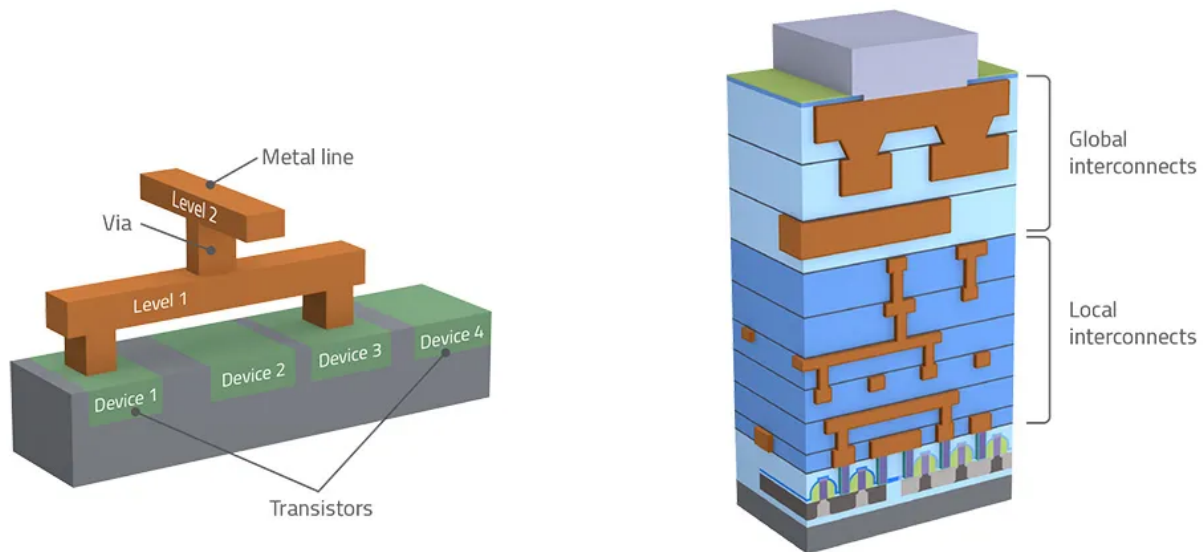
## Interconnect Layers

During the first portion of chip-making (or front-end-of-line), the individual components (transistors, capacitors, etc.) are fabricated on the wafer. In the back-end-of-line, these components are connected to each other to distribute signals, as well as power and ground. There simply isn't room on the chip surface to create all those connections in a single layer, so chip manufacturers build vertical levels of interconnects. While simpler integrated circuits (ICs) may have just a few metal layers, complex ICs can have ten or more layers of wiring.

Interconnects close to the transistors need to be small, as they attach/join to the components that are themselves very small and often closely packed together. These lower-level lines – called local interconnects – are usually thin and short in length. Global interconnects are higher up in the structure; they travel between different blocks of the circuit and are thus typically thick, long, and widely separated. Connections between interconnect levels, called vias, allow signals and power to be transmitted from one layer to the next.

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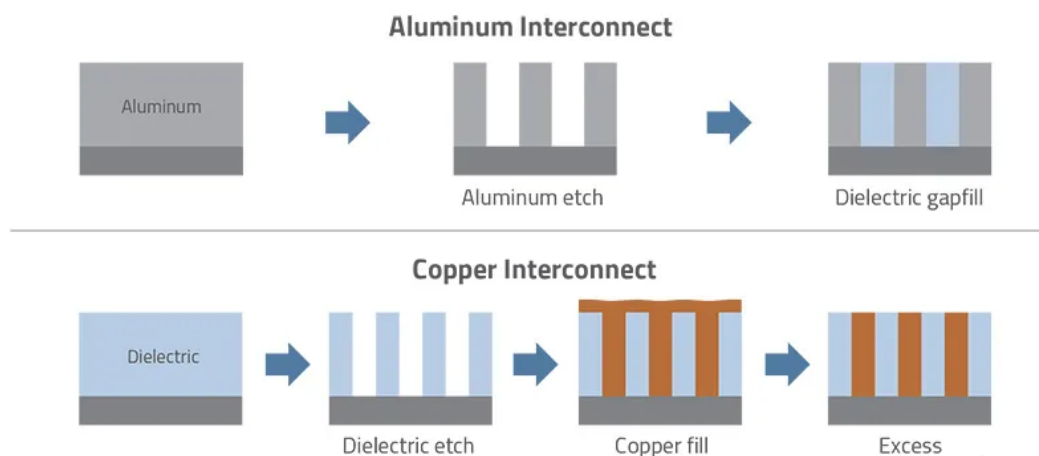


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### Interconnect Materials

For decades, aluminum interconnects were the industry standard. To create these interconnects, a layer of aluminum was deposited. Then, the metal was patterned and etched, and insulating material was deposited to separate the conducting lines. In the late 1990s, chipmakers switched to copper, which conducts electricity better than aluminum – somewhat similar to how a copper-bottomed frying pan heats up faster than an all-aluminum pan.

Higher conductivity lines improved overall IC performance. In addition, copper lines could be made smaller, keeping pace with transistor size scaling. Copper wiring is also more durable and reliable. However, creating copper interconnects is much more complex, and a whole new manufacturing scheme had to be developed for this [technology inflection](https://blog.lamresearch.com/tech-brief-the-role-of-technology-inflections/) (<https://blog.lamresearch.com/tech-brief-the-role-of-technology-inflections/>). The copper interconnect process starts with deposition of an insulating (dielectric) material, for example silicon dioxide, followed by the creation of trenches. The trenches are then filled with copper (using chemical/electroplating technologies), and the excess is removed to form a flat surface for subsequent processing.



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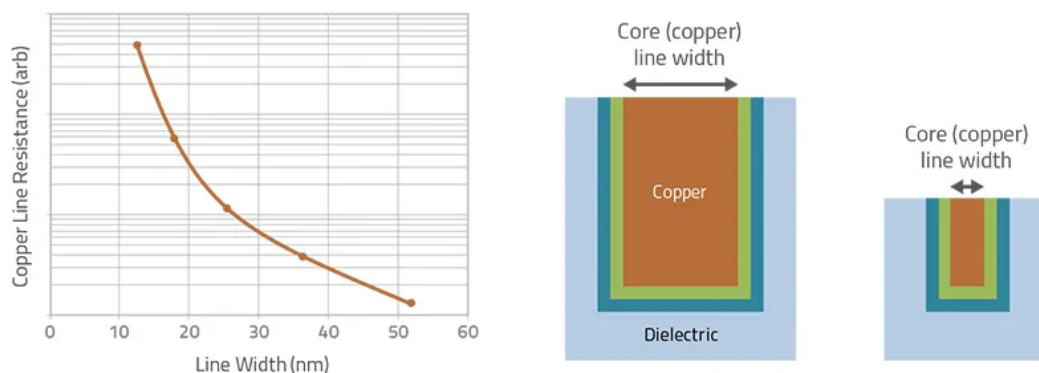
## The RC Challenge

Over the years, transistors have decreased dramatically in size. As transistors have gotten smaller and smaller, interconnects also have had to scale in size. Today, we're at the point where conventional copper interconnects are facing a significant roadblock to further scaling, and that roadblock is known as the RC challenge. Let's pause to define these two variables.

The electrical resistance (R) of a material describes how difficult it is to move electrical current through a particular cross-section of that material, which is a function of the orientation and proximity of the material's atoms. Capacitance (C) refers to a material's ability to store electrical charge. The product of resistance and capacitance (RC) needs to be low to create fast chips since device speed is inversely proportional to RC (lower RC = faster devices).

Looking at the "R" side of this challenge, higher-resistance lines carry less current, which slows device speed. This is because higher resistance reduces electron flow, so it takes longer to build up the minimum charge (number of electrons) or "threshold voltage" at a transistor's "gate" to turn it on. While transistor speed continues to improve with scaling (reducing the distance electrons must travel), the challenge for interconnect scaling is to not become a bottleneck and lose that performance improvement by slowing the flow of electrons between transistors.

### Higher Resistance with Smaller Line Width



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On the "C" side, capacitance is a function of the insulating dielectric material around the metal lines and the distance between them. Higher capacitance slows electrons and can create unwanted "cross talk," where the signal (voltage change) in one metal line influences the signal in a neighboring line and causes the device to malfunction. In addition to maintaining a suitable distance between lines, the development of "low-k" dielectric materials (capacitance is a function of a material's "k value") has significantly lowered capacitance. Today's dielectric materials average around  $k = 2.5$ , compared with  $k = 4.2$  for pure silicon dioxide. Various methods exist to achieve lower values; however, the resulting ultra-low-k films become increasingly fragile as the k value decreases, posing additional challenges for use in manufacturing.

## Scaling Solutions and Future Directions

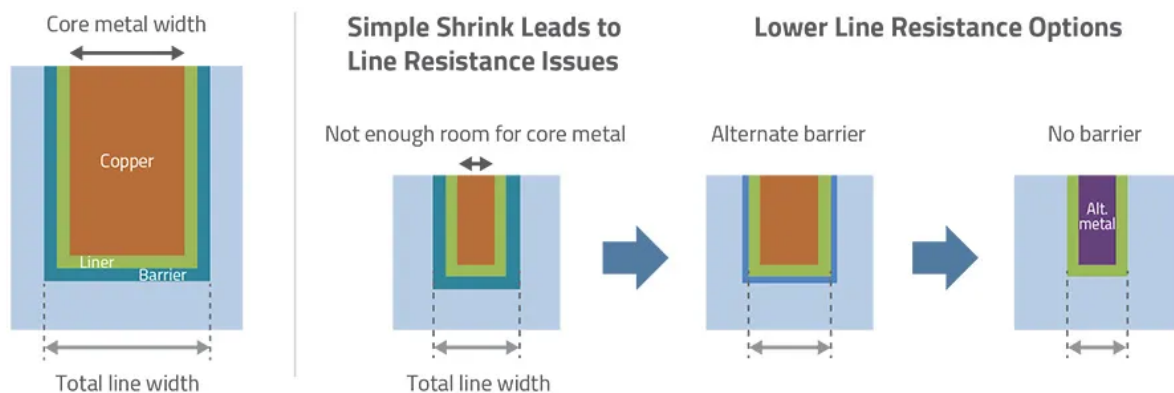
To address these issues for further scaling, the industry continues to identify ways to manage RC, particularly focusing on the metals involved. Copper has been successfully used for multiple device generations, so the industry is investing significant effort in developing new approaches to extend its use. Creating copper lines involves a series of layers – typically a tantalum nitride barrier (prevents metal diffusion into the dielectric), a tantalum liner (improves barrier adhesion), a copper seed layer (improves the metal fill/plating), and finally, the bulk (core

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conducting) copper metal. A key area of development focus is identifying strategies for improving the barrier/liner/seed layers to lower overall resistance and enable smaller lines by creating “space” for the bulk copper fill.

One strategy is to make the high-resistance barrier and liner thinner. However, opportunity for further thinning of these layers is limited. Both need to be continuous (no gaps or voids in the film) in order to achieve good reliability performance. This requires a minimum thickness of about 1.5 nm to 2 nm for each layer, which leads to a combined thickness of 3-4 nm on both sides of the trench structures.

A potential alternative being studied is a new type of “self-forming” barrier that reacts with and forms on the dielectric surface adjacent to the copper line, which allows more room for copper. Also, new liners made of cobalt and ruthenium are being developed to replace tantalum. They adhere better to the copper seed, enabling it to be more conformal (eliminating voids) and thinner. Already, new technologies are in place to achieve void-free copper fill of small trenches. Around the 5 nm technology node, however, copper as the primary conducting metal will ultimately have to be replaced with a conducting material that does not require a barrier for these ultra-thin lines.



([https://i0.wp.com/semiengineering.com/wp-content/uploads/2017/12/Lam\\_Tech\\_Brief\\_Interconnects\\_Fig4.jpg?ssl=1](https://i0.wp.com/semiengineering.com/wp-content/uploads/2017/12/Lam_Tech_Brief_Interconnects_Fig4.jpg?ssl=1))

While much attention is placed on the metals, there’s also some investigation into improvements on the dielectric side. Here, the holy grail is to reduce the dielectric constant as much as possible, the ultimate being  $k = 1$ , which is air. Indeed, novel developments using “air gaps” have been used, but both fabrication and production cost challenges are significant. Thus, many of the ideas being explored for interconnect scaling involve the development of new metals, designs, and processes – and those new technologies that are in the “pipeline” are sure to make ever smaller, faster connections a reality.

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Larry Zhao is technical director at Lam Research. Zhao holds a Ph.D. in electrical and electronics engineering from KU Leuven; a Ph.D. in Materials Science from Columbia University; an M.S. degree in engineering from Dartmouth College; and a B.S. in materials science from Shanghai Jiao Tong University. He has previously worked at GlobalFoundries, Imec, Intel, AMD, Philips Research and Shanghai Research Institute of Materials.

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JRP Says:

July 18, 2020 at 11:51 pm (<https://semiengineering.com/all-about-interconnects/#comment-381565>)

Hi,

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Why the interconnects spacing (Say M1 of net1 to M1 of net2) depends on voltage

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