

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: Glenn A. Glass, et al.
U.S. Patent No.: 11,251,281 Attorney Docket No.: 39843-0154IP1
Issue Date: February 15, 2022
Appl. Serial No.: 16/881,541
Filing Date: May 22, 2020
Title: CONTACT RESISTANCE REDUCTION EMPLOYING GERMA-
NIUM OVERLAYER PRE-CONTACT METALIZATION

Mail Stop Patent Board

Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

PETITION FOR *INTER PARTES* REVIEW OF
UNITED STATES PATENT NO. 11,251,281
PURSUANT TO 35 U.S.C. §§ 311–319, 37 C.F.R. § 42

TABLE OF CONTENTS

I.	REQUIREMENTS FOR IPR	1
A.	Grounds for Standing.....	1
B.	Challenge and Relief Requested.....	1
II.	OVERVIEW OF THE '281 PATENT	2
A.	Subject Matter Overview	2
B.	Summary of the Prosecution History.....	5
C.	Level of Ordinary Skill in the Art.....	5
D.	Priority Date of the Challenged Claims.....	6
III.	CLAIM CONSTRUCTION	7
IV.	THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	8
A.	[GROUND 1A] – Obviousness based on Tung in view of Yu and Simonelli (Claims 1, 5-8).....	8
1.	Overview of Tung	8
2.	Overview of Yu	9
3.	Overview of Simonelli	10
4.	Obviousness Analysis	11
B.	[GROUND 1B] – Obviousness based on Yu in view of Tung and Simonelli (Claims 1, 5-8).....	75
C.	[GROUND 2A] Obviousness based on Conway, Tung, Yu, and Simonelli (Claims 12-20).....	84
1.	Overview of Conway	84
2.	Obviousness Analysis	85
D.	[GROUND 2B] – Obviousness based on Conway, Yu, Tung, and Simonelli (Claims 12-20).....	91
V.	DISCRETIONARY CONSIDERATIONS	91
A.	§ 325(d) – <i>Advanced Bionics</i>	91
B.	§314(a) - <i>Fintiv</i>	92
VI.	MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1).....	93
A.	Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1).....	93
B.	Related Matters Under 37 C.F.R. § 42.8(b)(2).....	93
C.	Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3).....	93
D.	Service Information	94
VII.	FEES	94
VIII.	CONCLUSION.....	94

EXHIBITS

- SAMSUNG-1001 U.S. Patent No. 11,251,281 to Glass (“the ’281 Patent”)
- SAMSUNG-1002 File History of the ’281 Patent
- SAMSUNG-1003 Expert Declaration of Dr. Fred Schubert
- SAMSUNG-1004 [RESERVED]
- SAMSUNG-1005 Certified English Translation of Japanese Patent Application
Publication No. 2010-171337 (“Tezuka”)
- SAMSUNG-1006 U.S. Patent App. Pub. No. 2010/0276761 (“Tung”)
- SAMSUNG-1007 U.S. Patent App. Pub. No. 2011/0073952 (“Kwok”)
- SAMSUNG-1008 U.S. Patent App. Pub. No. 2010/0148217 (“Simonelli”)
- SAMSUNG-1009 U.S. Patent App. Pub. No. 2012/0139015 (“Yu”)
- SAMSUNG-1010 U.S. Patent App. Pub. No. 2009/0325607 (“Conway”)
- SAMSUNG-1011 U.S. Patent App. Pub. No. 2011/0042748 (“Anderson”)
- SAMSUNG-1012 Japanese Patent Application Publication No. 2010-171337
(Original Japanese version of Tezuka)
- SAMSUNG-1013 Excerpts of the File History of EP Patent App. No. 19188924.5
- SAMSUNG-1014 Complainant Daedalus Prime LLC’s Infringement Claim Chart
for U.S. Patent No. 10,700,178 (Exhibit 47 to Complaint), *In
the Matter of Certain Semiconductor Devices, Mobile Devices
Containing the Same, and Components Thereof* (ITC Investiga-
tion No. 337-TA-1336)
- SAMSUNG-1015 Complainant Daedalus Prime LLC’s Infringement Claim Chart
for U.S. Patent No. 11,251,281 (Exhibit 48 to Complaint), *In
the Matter of Certain Semiconductor Devices, Mobile Devices*

Containing the Same, and Components Thereof (ITC Investigation No. 337-TA-1336)

- SAMSUNG-1016 Findlay Shearer, *Power Management in Mobile Devices - A View of Energy Conservation - Part IV*, EE Times, May 5, 2008, available at <https://www.eetimes.com/power-management-in-mobile-devices-a-view-of-energy-conservation-part-iv/>
- SAMSUNG-1017 U.S. Patent App. Pub. No. 2011/0147842 (“Cappellani”)
- SAMSUNG-1018 U.S. Patent No. 7,288,443 (“Zhu”)
- SAMSUNG-1019 U.S. Patent No. 2007/0235802 (“Chong”)
- SAMSUNG-1020 U.S. Patent App. Pub. No. 2005/0184316 (“Kim I”)
- SAMSUNG-1021 U.S. Patent App. Pub. No. 2007/0082451 (“Samoilov”)
- SAMSUNG-1022 A. Nishida et al., *Elimination of Misfit Dislocations in Si_{1-x}Ge_x/Si Heterostructures by Limited-area Molecular-beam Epitaxial Growth*, J. Appl. Phys 71 at 5913-5917 (1992) (“Nishida”)
- SAMSUNG-1023 E.A. Fitzgerald, *The Effect of Substrate Growth Area on Misfit and Threading Dislocation Densities in Mismatched Heterostructures*, J. Vac. Sci. Tech. B7 at 782-788 (1989) (“Fitzgerald”)
- SAMSUNG-1024 Arne Larsen, *Epitaxial Growth of Ge and SiGe on Si Substrates*, Materials Science in Semiconductor Processing 9 at 454-459 (2006) (“Larsen”)
- SAMSUNG-1025 Schubert, *Room Temperature Properties of Si, Ge, GaAs, and GaN* (“Schubert Materials Datasheet”)
- SAMSUNG-1026 Elsevier, *Encyclopedia of Materials: Science and Technology* at pp. 8479-8486 (2001) (“Elsevier”)

- SAMSUNG-1027 Kim et al., *Increased Critical Thickness for High Ge-Content Strained SiGe-on-Si Using Selective Epitaxial Growth*, American Institute of Physics, Applied Physics Letter 97, 262106 (2010) (“Kim II”)
- SAMSUNG-1028 Semiconductor Doping Technology, *available at* <https://www.iue.tuwien.ac.at/phd/wittmann/node7.html>
- SAMSUNG-1029 Natalie Stavitski, *Silicide-to-Silicon Specific Contact Resistance Characterization: Test Structures and Models* (2009) (“Stavitski”)
- SAMSUNG-1030 EP Application No. 1 575 082 A2 (“Demeurisse”)
- SAMSUNG-1031 U.S. Patent No. 5,296,386 (“Aronowitz”)
- SAMSUNG-1032 U.S. Patent App. Pub. No. 2006/0286755 (“Brask”)
- SAMSUNG-1033 U.S. Patent App. Pub. No. 2011/0024804 (“Chang”)
- SAMSUNG-1034 Peter Hadley, Semiconductor Doping, Institute of Solid State Physics, *available at* <https://lampx.tugraz.at/~hadley/psd/problems/doping/s.pdf>
- SAMSUNG-1035 Mirabella et al., *Mechanisms of Boron Diffusion in Silicon and Germanium*, Journal of Applied Physics 113, 031101 (2013) (“Mirabella”)
- SAMSUNG-1036 U.S. Patent App. Pub. No. 2006/0071275 (“Brask”)
- SAMSUNG-1037 Brown et al., *Lattice stability and point defect energetics of $TiSi_2$ and $TiGe_2$ allotropes from first-principles calculations*, Journal of Applied Physics 129, 085104 (2021) (“Brown”)
- SAMSUNG-1038 U.S. Application Serial No. 13/990,224 (“the ’224 Application”)
- SAMSUNG-1039 U.S. Patent App. Pub. No. 2009/0325350 (“Radosavljevic”)

- SAMSUNG-1040 Peter Caputa, Efficient High-Speed On-Chip Global Interconnects, Linkopings Universitet Institute of Technology, Dissertation No. 992 (2006)
- SAMSUNG-1041 Larry Zhao, *All About Interconnects*, Semiconductor Engineering, *available at* <https://semiengineering.com/all-about-interconnects> (retrieved Jan. 17, 2023)
- SAMSUNG-1042 U.S. Patent App. Pub. No. 5,439,848 (“Hsu”)
- SAMSUNG-1043 U.S. Patent App. Pub. No. 2010/0123198 (“Kim III”)
- SAMSUNG-1044 U.S. Patent No. 7,692,254 (“Anderson”)
- SAMSUNG-1045 U.S. Application Serial No. 12/975,278 (“the ’278 Application”)
- SAMSUNG-1046-1100 [RESERVED]
- SAMSUNG-1101 Daedalus Prime LLC’s Complaint *In the Matter of Certain Semiconductor Devices, Mobile Devices Containing the Same, and Components Thereof* (ITC Investigation No. 337-TA-1336)
- SAMSUNG-1102 Complaint, *Daedalus Prime LLC v. Samsung Electronics Co. Ltd. et al.*, Civil Action No. 2:22-cv-352 (E.D. Tex.) (September 12, 2022)
- SAMSUNG-1103 Order Granting Stay, *Daedalus Prime LLC v. Samsung Electronics Co. Ltd. et al.*, Civil Action No. 2:22-cv-352 (E.D. Tex.) (November 1, 2022)
- SAMSUNG-1104 Director Katherine K. Vidal’s Memorandum re Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings With Parallel District Court Litigation (June 21, 2022)

CLAIM LISTING

Element	Claim Language
[1pre]	An integrated circuit structure, comprising:
[1a]	a fin comprising silicon;
[1b]	a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;
[1c]	a first dielectric spacer along the first side of the gate electrode;
[1d]	a first source or drain region in the fin proximate the first side of the gate electrode,
[1e]	a portion of the first source or drain region beneath the first dielectric spacer,
[1f]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[1g]	a second dielectric spacer along the second side of the gate electrode;
[1h]	a second source or drain region in the fin proximate the second side of the gate electrode,
[1i]	a portion of the second source or drain region beneath the second dielectric spacer,
[1j]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[1k]	a dielectric layer over the first source or drain region and over the second source or drain region,

Element	Claim Language
[1l]	the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;
[1m]	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[1n]	a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;
[1o]	a first contact plug in the first opening and on the first germanide layer; and
[1p]	a second contact plug in the second opening and on the second germanide layer.
[5]	The integrated circuit structure of claim 1, further comprising: an isolation region, wherein the fin protrudes through the isolation region, and wherein a portion of the gate electrode, a portion of the first dielectric spacer, and a portion of the second dielectric spacer are over the isolation region.
[6]	The integrated circuit structure of claim 1, further comprising: a gate dielectric layer, wherein the gate electrode is on the gate dielectric layer, wherein the gate dielectric layer comprises a high-k dielectric material, and wherein the gate electrode comprises a metal layer.
[7]	The integrated circuit structure of claim 1, wherein the first source or drain region comprises two or more facets, and the second source or drain region comprises two or more facets.
[8pre]	An integrated circuit structure, comprising:
[8a]	a body comprising silicon;
[8b]	a gate electrode over the body, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;

Element	Claim Language
[8c]	a first dielectric spacer along the first side of the gate electrode;
[8d]	a first source or drain region in the body proximate the first side of the gate electrode,
[8e]	a portion of the first source or drain region beneath the first dielectric spacer
[8f]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[8g]	a second dielectric spacer along the second side of the gate electrode;
[8h]	a second source or drain region in the body proximate the second side of the gate electrode,
[8i]	a portion of the second source or drain region beneath the second dielectric spacer,
[8j]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[8k]	a dielectric layer over the first source or drain region and over the second source or drain region,
[8l]	the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;
[8m]	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[8n]	a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer

Element	Claim Language
	comprising silicon, germanium and titanium;
[8o]	a first contact plug in the first opening and on the first germanide layer; and
[8p]	a second contact plug in the second opening and on the second germanide layer.
[12pre]	A computing device, comprising:
[12a]	a board; and
[12b]	a component coupled to the board, the component including an integrated circuit structure, comprising:
[12c]	a fin comprising silicon;
[12d]	a gate electrode over the fin, the gate electrode having a first side, and the gate electrode having a second side opposite the first side;
[12e]	a first dielectric spacer along the first side of the gate electrode;
[12f]	a first source or drain region in the fin proximate the first side of the gate electrode,
[12g]	a portion of the first source or drain region beneath the first dielectric spacer,
[12h]	wherein the first source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[12i]	a second dielectric spacer along the second side of the gate electrode;
[12j]	a second source or drain region in the fin proximate the second side of the gate electrode,
[12k]	a portion of the second source or drain region beneath the second dielectric spacer,

Element	Claim Language
[12l]	wherein the second source or drain region comprises silicon and germanium having a germanium concentration graded to a concentration in excess of 50%;
[12m]	a dielectric layer over the first source or drain region and over the second source or drain region,
[12n]	the dielectric layer having a first opening exposing only a portion of the first source or drain region, and the dielectric layer having a second opening exposing only a portion of the second source or drain region;
[12o]	a first germanide layer in the first opening and over the portion of the first source or drain region, the first germanide layer comprising silicon, germanium and titanium;
[12p]	a second germanide layer in the second opening and over the portion of the second source or drain region, the second germanide layer comprising silicon, germanium and titanium;
[12q]	a first contact plug in the first opening and on the first germanide layer; and
[12r]	a second contact plug in the second opening and on the second germanide layer.
[13]	The computing device of claim 12, further comprising: a memory coupled to the board.
[14]	The computing device of claim 12, further comprising: a communication chip coupled to the board.
[15]	The computing device of claim 12, further comprising: a camera coupled to the board.
[16]	The computing device of claim 12, further comprising: a battery coupled to the board.
[17]	The computing device of claim 12, further comprising: an antenna coupled to the board.

Element	Claim Language
[18]	The computing device of claim 12, wherein the component is a packaged integrated circuit die.
[19]	The computing device of claim 12, wherein the component is selected from the group consisting of a processor, a communications chip, and a digital signal processor.
[20]	The computing device of claim 12, wherein the computing device is selected from the group consisting of a mobile phone, a laptop, a desk top computer, a server, and a set-top box.

Samsung Electronics Co., Ltd. (“Petitioner” or “Samsung”) petitions for *In-ter Partes* Review (“IPR”) of claims 1, 5-8, and 12-20 (“the Challenged Claims”) of U.S. Patent No. 11,251,281 (“the ’281 Patent”).

I. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the ’281 Patent is available for IPR. This petition is being filed within one year of service of a complaint against Samsung. Samsung is not barred or estopped from requesting review of the Challenged Claims on the below-identified grounds.

B. Challenge and Relief Requested

Petitioner requests IPR of the Challenged Claims on the grounds set forth in the table shown below. Additional explanation and support for each ground is set forth in the expert declaration of Dr. Fred Schubert (SAMSUNG-1003), referenced throughout this Petition. Dr. Schubert’s analysis is corroborated by citation to exhibits of record including SAMSUNG-1016 through -1045.

Ground	Claims	Basis Under 35 U.S.C. §103
1A	1, 5-8	Tung-Yu-Simonelli
1B	1, 5-8	Yu-Tung-Simonelli
2A	12-20	Conway-Tung-Yu-Simonelli
2B	12-20	Conway-Yu-Tung-Simonelli

The Challenged Claims are entitled to a priority date no earlier than September 30, 2011 (“Critical Date”), for the reasons described further below in Section II.D. SAMSUNG-1003, ¶¶51-53. Petitioner has applied prior art in this Petition that predates the Critical Date, and each of the references cited in Grounds 1A-2B qualifies as prior art to the ’281 Patent as shown below¹:

Reference	Filed	Published	Pre-AIA Prior Art Qualification
Tung	01/06/2010	11/04/2010	§§102(a), (e)
Yu	12/07/2010	06/07/2012	§102(e)
Simonelli	12/11/2008	06/17/2010	§§102(a)-(b), (e)
Conway	05/28/2009	12/31/2009	§102(a)-(b), (e)

II. OVERVIEW OF THE ’281 PATENT

A. Subject Matter Overview

The ’281 Patent generally describes techniques for forming germanide-based

¹ Each of the references cited in this Petition also predates the earliest claimed priority date of the ’281 Patent (i.e., December 21, 2010). The Challenged Claims would have been obvious even if December 21, 2010 was applied as the Critical Date. SAMSUNG-1003, ¶23.

contacts to the source and drain regions of a field-effect transistor (“FET”). SAMSUNG-1001, Abstract; SAMSUNG-1003, ¶40; *see also id.*, ¶¶41-46. The inventors purportedly sought to “reduce the band misalignment value and contact resistance” of such contacts by forming the germanide from an “**intermediate boron doped germanium layer**” (also referred to as a germanium “**cap layer**”) “between the source/drain and contact metals,” where the “cap layer” is composed of more than ninety atomic-percentage germanium. SAMSUNG-1001, 2:58-64, 7:16-20, 10:43-49, 12:32-41, 14:3-10.

To illustrate, Figure 5F depicts an example in which boron-doped germanium cap layers 317/319 have been formed over source/drain regions 318/320. *Id.*, 12:58-67. A suitable contact metal 325/327, such as titanium, is deposited over cap layers 317/319. The contact metals 325/327 are then annealed with their respective cap layers 317/319 to form germanide layers that electrically couple the source and drain regions 318/320 to external circuitry via metal contact plugs 329/331. *Id.*, 11:60-12:41, 13:7-13:12.

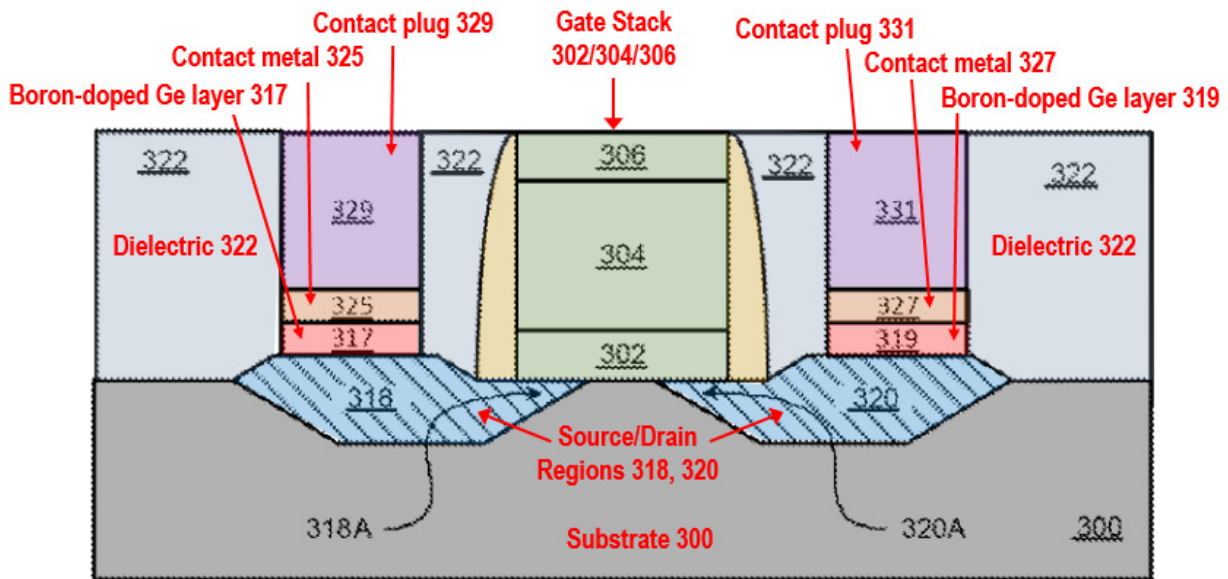
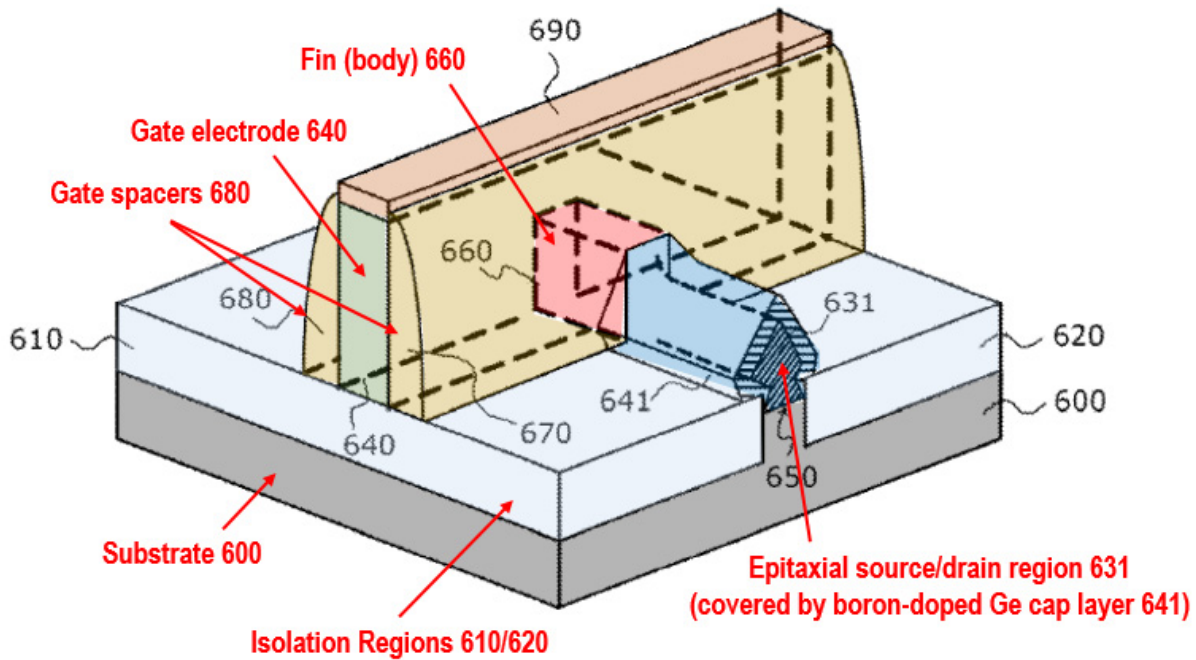


FIG. 5F

SAMSUNG-1001, FIG. 5F (annotated); *see also id.*, FIG. 3I.

The '281 Patent further explains how the boron-doped germanium caps can be used to improve contact resistance in a range of FETs, “including both planar and non-planar transistor structures (e.g., FinFETs).” *Id.*, 2:32-33. The Challenged Claims are specifically directed to non-planar devices (e.g., FinFETs or other devices that were known to have multiple gates that would wrap a “fin” or channel body on multiple sides), an embodiment of which is depicted in Figure 6:



SAMSUNG-1001, FIG. 6; *see also id.*, 13:15-14:14.

As shown in Figure 6, “[a] cap layer 641 is deposited over the epitaxial regions 631” of the source and drain regions. *Id.*, 13:47-51. This results in a “bi-layer structure” between an epitaxially grown SiGe region 631 (which provides the source and drains of the device) and a cap layer 641. *Id.*, 13:67-14:3.

B. Summary of the Prosecution History

The application that led to the '281 Patent was allowed without the Examiner having made any substantive rejections against the claims. SAMSUNG-1002, 193-99, 10-18; *see also id.*, 196-97; SAMSUNG-1003, ¶¶47-48.

C. Level of Ordinary Skill in the Art

A person of ordinary skill as of the Critical Date (“POSITA”) would have

had a Master's degree in electrical engineering, physics, or a related field, and two years of work experience in integrated circuit design or manufacturing. Additional education could substitute for professional experience, or significant experience in the field could substitute for formal education. SAMSUNG-1003, ¶¶23-25.

D. Priority Date of the Challenged Claims

Independent claims 1, 8, and 12 of the '281 Patent each recite features directed to (i) first and second "opening[s]" in a dielectric layer that expose respective portions of first and second source or drain regions of an integrated circuit structure, (ii) first and second "germanide layer[s]" in the openings, and (iii) first and second "contact plug[s]" in the openings and on the germanide layers. SAMSUNG-1001, 18:62-19:12, 20:14-31, 21:17-22:4. These features correspond to structures depicted and described, for example, with respect to FIGS. 4 and 5C-5F of the '281 Patent. *Id.*, 12:42-67, FIGS. 5C-5F; *supra*, Section II.A.

Although the '281 Patent's earliest priority claim is to an application filed December 21, 2010 (i.e., U.S. Serial 12/975,278, SAMSUNG-1045), the claim features noted above are not described in the '278 Application. For example, the '278 Application discloses source and drain cap layers 317/319 formed over source and drain regions 318/320, but these cap layers 317/319 and their corresponding germanide layers are formed before interlayer dielectric layer 222 is deposited and,

thus, are not formed in any “opening[s]” in the dielectric layer, as claimed. SAMSUNG-1045, [0039]-[0047], FIGS. 3G-3J.

Disclosure of techniques for forming germanide layers in openings of a dielectric layer and providing contact plugs in the openings was only later introduced in a continuation-in-part application filed September 30, 2011 (i.e., U.S. Serial 13/990,224, SAMSUNG-1038). *See* SAMSUNG-1038, [0041]-[0042], FIGS. 4, 5A-5F; SAMSUNG-1003, ¶53. The disclosure of the '278 Application would not have reasonably conveyed possession of these claim features by December 21, 2010, and the '278 Application lacks written description support for these features in the Challenged Claims. SAMSUNG-1003, ¶¶51-53. Accordingly, the Challenged Claims are entitled to a priority date no earlier than September 30, 2011.

III. CLAIM CONSTRUCTION

All claim terms should be construed according to the *Phillips* standard.

Phillips v. AWH Corp., 415 F.3d 1303 (Fed. Cir. 2005); 37 C.F.R. §42.100.

“[C]laim terms need only be construed to the extent necessary to resolve the controversy.” *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011); SAMSUNG-1003, ¶¶49-50.

Petitioner reserves the right to respond to any constructions offered by Patent Owner or adopted by the Board. Petitioner is not conceding that the Challenged Claims satisfy all statutory requirements including those under 35 U.S.C. §

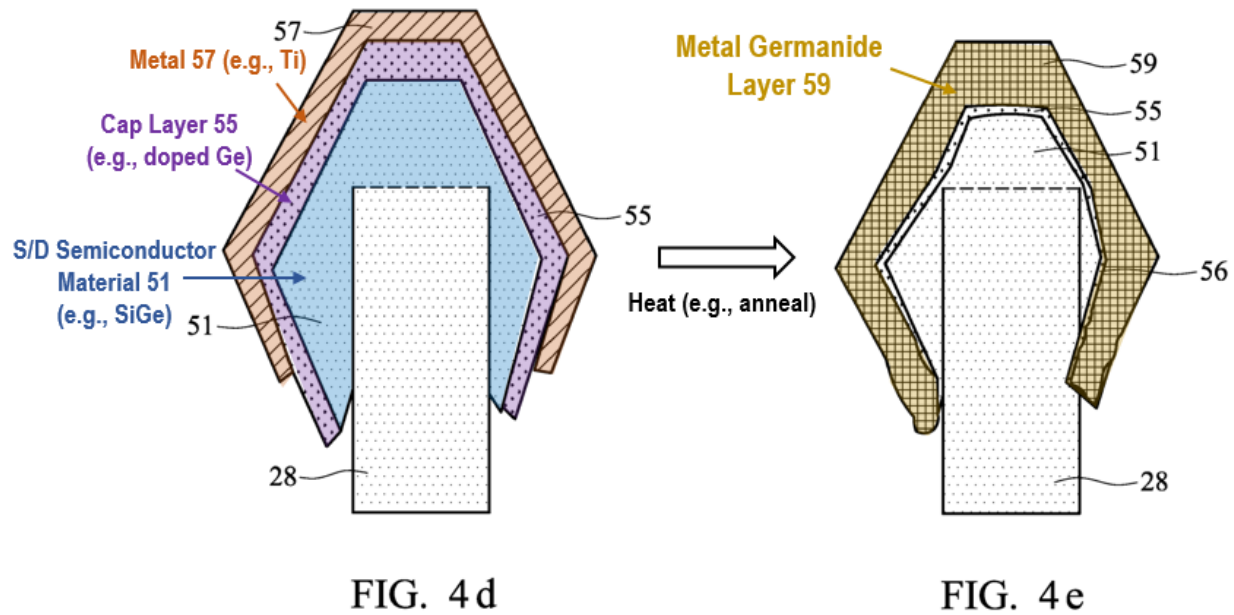
112.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. [GROUND 1A] – Obviousness based on Tung in view of Yu and Simonelli (Claims 1, 5-8)

1. Overview of Tung

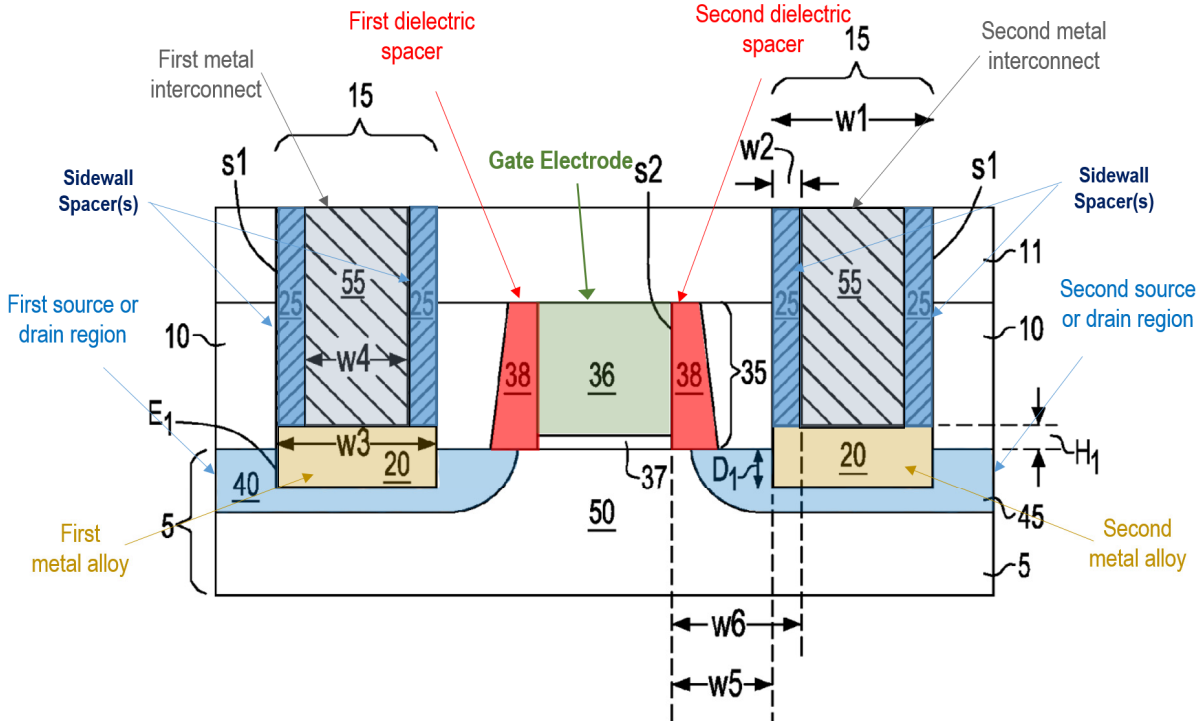
Tung describes techniques for forming non-planar FETs (e.g., FinFETs) with improved contacts to the source and drain regions. SAMSUNG-1006, [0005]-[0006], [0019]-[0021]. Tung's process involves forming a doped semiconductor cap layer 55 over an outer surface of a semiconductor material 51 of the source or drain region, depositing a metal 57 such as titanium over the cap layer 55, and annealing the metal 57 over the cap layer 55 to form a metal silicide or germanide layer 59. *Id.*, [0043]-[0045]. The cap layer 55 can be a doped germanium layer, and the resulting germanide layer 59 provides a contact structure to the source or drain region with a low contact resistance and reduced Schottky barrier height. *Id.*, [0058], [0078]; SAMSUNG-1003, ¶54.



Tung, FIGS. 4d-4e (annotated)

2. Overview of Yu

Yu describes techniques for forming contacts 20 to the source and drain regions 40/45 of a field-effect transistor ("FET") within openings 15 of an inter-level dielectric layer ("IDL") 10. SAMSUNG-1009, [0071]-[0075], FIGS. 3-4, FIG. 6; SAMSUNG-1003, ¶55. Yu's IDL 10 is part of a set of interconnect structures that facilitate implementation of Yu's FET in an integrated circuit ("IC"), e.g., an IC that may have additional layers of components or wiring formed above the transistor to connect components in the IC and to deliver electrical power and signals to the components. SAMSUNG-1003, ¶55; SAMSUNG-1009, [0030]-[0038], FIGS. 1-6.



Yu, FIG. 6 (annotated)

3. Overview of Simonelli

Simonelli describes “planar and three-dimensional complementary metal oxide semiconductor (CMOS) devices comprising a compound layer with graded germanium content.” SAMSUNG-1008, [0001], Abstract; SAMSUNG-1003, ¶56.

For example, Simonelli describes techniques for epitaxially growing source/drain regions in a multi-gate device (e.g., a FinFET) “using a graded high-germanium content silicon-germanium film stack 1400” like that illustrated in FIG. 14. SAMSUNG-1008, [0051]-[0058], FIGS. 12, 14-15.



FIG. 14

Simonelli, FIG. 14 (annotated)

4. Obviousness Analysis

As described in further detail below, it would have been obvious (1) to augment Tung's FinFET with interconnect structures based on Yu and (2) to grade the germanium content in the source and drain regions of Tung's FinFET based on the teachings of Simonelli. SAMSUNG-1003, ¶60; *see also id.* ¶¶59-89.

Integration of Interconnect Structures based on Yu with Tung's FinFET

As discussed above, Tung describes methods for forming respective metal germanide layers 59² over the source and drain regions of a FinFET. *Supra*, Section IV.A.1. Tung also refers to a "contact ... disposed" on each germanide layer

² Tung's generically labeled "silicide" layer 59 would have been understood to be a "germanide" layer at least when it is formed by annealing a metal such as titanium over a **germanium** cap layer 55 composed of "doped Ge" or "doped SiGe" formed

59, although this “contact” is neither shown in the figures nor discussed in detail in Tung. *See* SAMSUNG-1006, [0023], [0036], [0064]. Tung only mentions, for example, that “[c]ontacts (not shown) are subsequently formed on ... layer 59 and subsequent processing including metallization proceeds as in conventional processing.” *Id.*, [0064].

Notwithstanding Tung’s lack of detail in this regard, it would have been obvious to a POSITA to implement the contacts formed over Tung’s germanide layer 59 as an electrical interconnect (e.g., a metal contact plug) to other circuit components (e.g., other transistors, or power or signal lines) in an IC. SAMSUNG-1003, ¶¶61-62. In this context, a POSITA would have found it obvious to augment Tung’s FinFET with a more complete set of interconnect structures like those described in Yu. SAMSUNG-1003, ¶63. For example, as shown below, it would have been obvious and straightforward based on Yu to form an IDL 10 over Tung’s FET including over each of the source and drain regions 39. *Id.* Further,

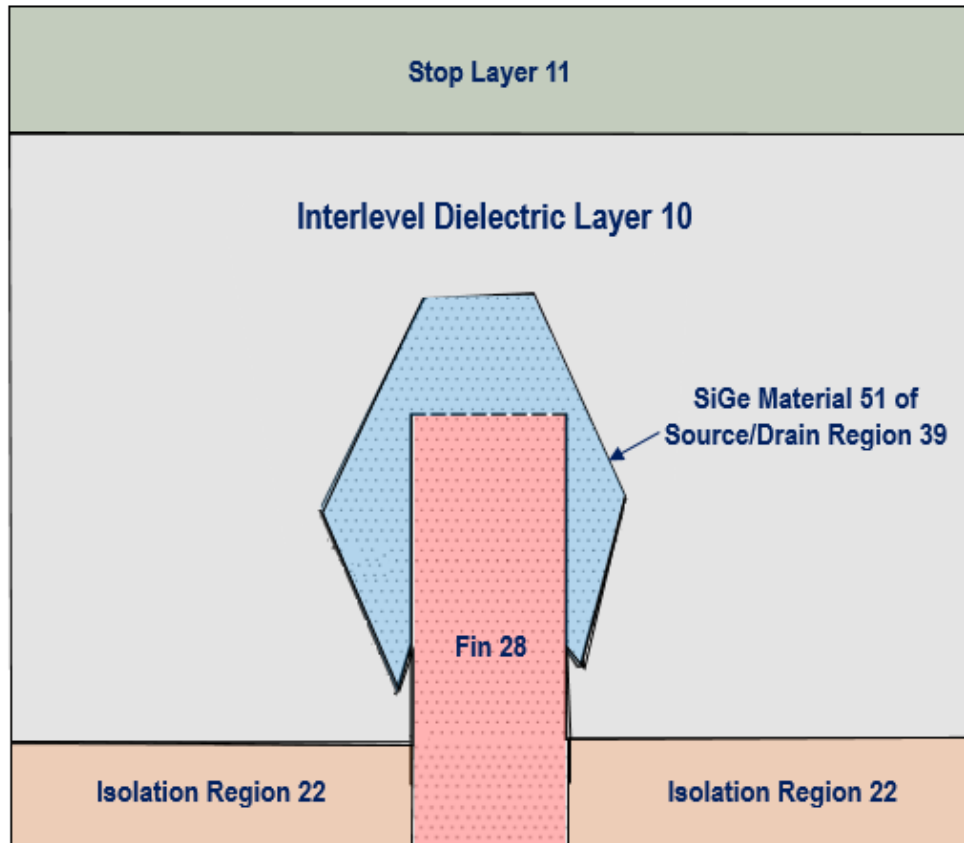
predominantly of germanium (e.g., in excess of 90% Ge). SAMSUNG-1006, [0058], [0078]; SAMSUNG-1001, 9:34-42, 10:43-50, 12:21-27, 16:14-17; SAMSUNG-1003, ¶61, FN 1. By contrast, for example, a layer formed by annealing metal with pure silicon would be understood to be a silicide rather than a germanide. SAMSUNG-1003, ¶61, FN 1.

consistent with Yu's teachings, it would have been obvious (i) to form openings 15 in IDL 10 exposing portions of the source and drain regions 39, (ii) to form the germanide layers 59 in the openings 15 and over exposed portions of the source and drain regions 39 in a manner analogous to the formation of Yu's metallized contact layer 20 (such that germanide layers 59 are formed over exposed portions of the SiGe material 51 of Tung's source and drain regions 39 in the combination), (iii) to form dielectric sidewall spacers 25 on sidewalls of openings 15, and (iv) to form contact plugs akin to Yu's interconnects 55 in the openings 15 of the IDL 10 and on the respective germanide layers 59. SAMSUNG-1009, [0030]-[0038], FIGS. 1, 6; SAMSUNG-1003, ¶63.

To illustrate, the following sequence of figures shows the application of interconnect structures based on Yu to the source/drain region 39 of a FinFET as taught in Tung (e.g., starting with the source/drain region 39 depicted in Tung's FIG. 4b).³ SAMSUNG-1003, ¶64.

³ Illustrations of the Tung-Yu-Simonelli combination are provided only by way of example, and should not be understood as limiting the manner in which it would have been obvious to combine the teachings of the respective references. SAMSUNG-1003, ¶64, FN 2. A POSITA also would have understood that the illustrations are not necessarily to scale. *Id.* For instance, a POSITA would have found it

- (1) Form IDL 10 and stop layer 11 over source/drain region 39. SAM-SUNG-1009, [0030]-[0031], [0050]-[0051]; SAMSUNG-1003, ¶65.

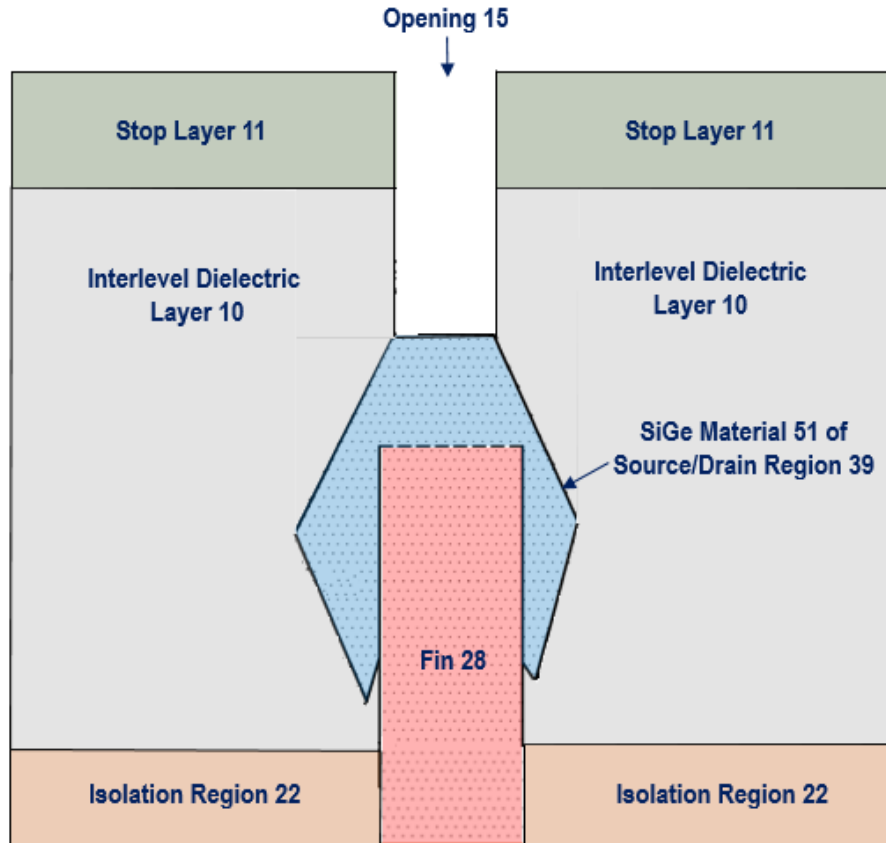


Tung-Yu-Simonelli (Example Formation Illustration 1)

obvious for the top surface of the source/drain region 39 to be even wider (or narrower) than its depiction in Tung's FIGS. 4b-4e. *Id.* Likewise, it would have been obvious to form a similar set of interconnect structures over an epitaxially regrown source/drain region 39 like that taught in Simonelli (e.g., rather than over an over-grown SiGe material 51 over a fin structure 28). *See* SAMSUNG-1008, FIG. 12; *infra*, [1f]/[1j]; SAMSUNG-1003, ¶64, FN 2.

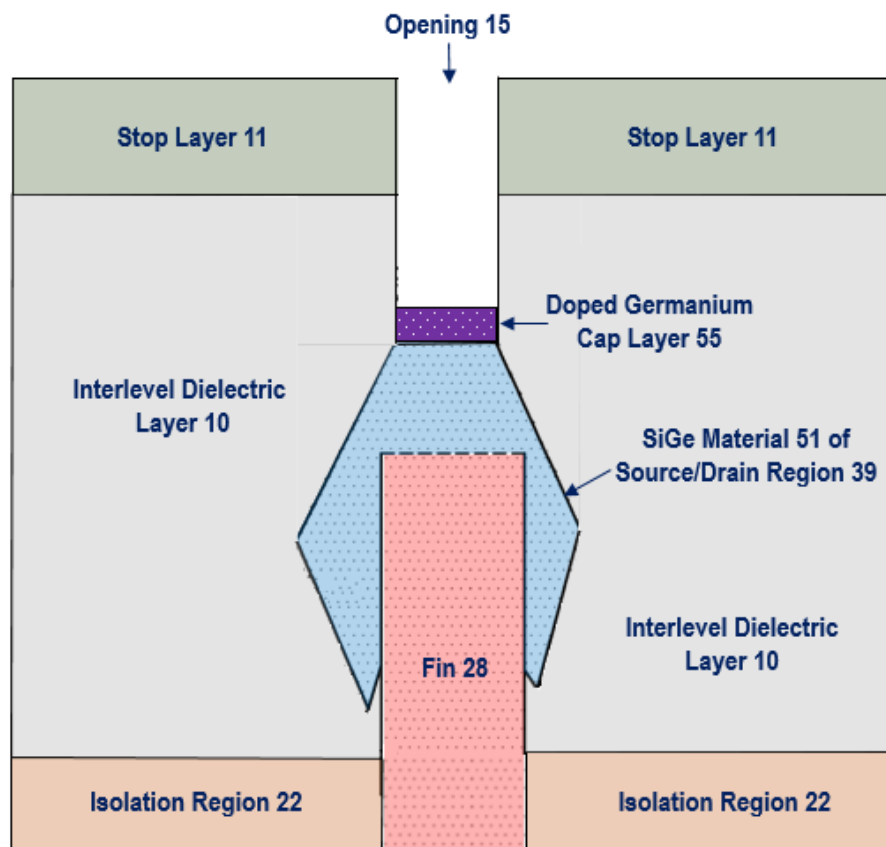
- (2) Form opening 15 in IDL 10 and stop layer 11 to expose a portion of the SiGe material 51 of source/drain region 39.⁴ SAMSUNG-1009, [0063]-[0065], FIG. 2A SAMSUNG-1003, ¶¶66-67.

⁴ A POSITA would have understood and it would have been obvious to select a width for the opening 15 over the SiGe material 51 of source/drain region 39 so as to optimize one or more characteristics of the FinFET in the resulting combination. SAMSUNG-1003, ¶67. For example, the width of the opening 15 (and hence the width and surface area available for forming the germanide layer 59 and contact plug (interconnect) over the source/drain region 39) would predictably impact the contact resistance to the source/drain region 39, the amount of epitaxial growth required to form germanium cap layer 55, and the distance between the contact plug and other structures such as the gate electrode or source/drain regions of other FETs. SAMSUNG-1003, ¶67. It would have been obvious, e.g., through routine experimentation, to select a width for the opening 15 that optimizes desired fabrication and performance characteristics of the FET. The opening 15 may thus be wider or narrower than that of the examples depicted by the illustrations of the Tung-Yu-Simonelli combination. *Id.*



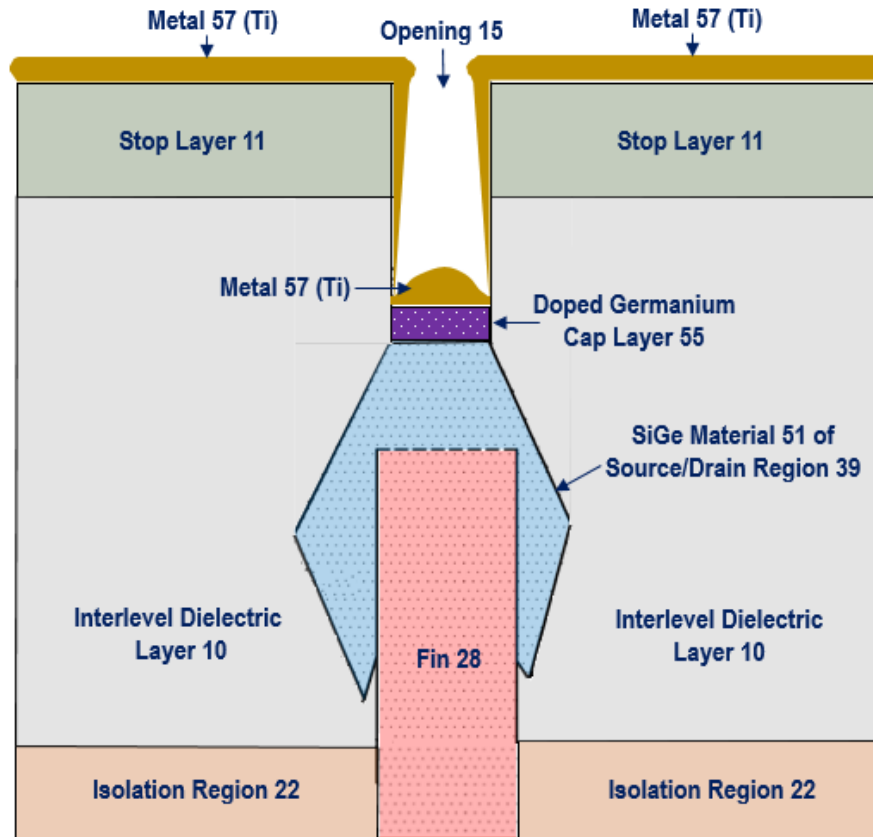
Tung-Yu-Simonelli (Example Formation Illustration 2)

- (3) Form a germanide layer 59 consistent with Tung's teachings and analogously to Yu's metal semiconductor alloy contact layer 20. SAMSUNG-1009, [0071]-[0075], FIGS. 3-4 SAMSUNG-1003, ¶68.
- a) Form a doped germanium cap layer 55 in the opening 15 and over the exposed portion of SiGe material 51 of source/drain region 39. SAMSUNG-1006, [0041], [0078], FIGS. 4c, 14; SAMSUNG-1009, [0071]-[0075], FIGS. 3-4.



Tung-Yu-Simonelli (Example Formation Illustration 3(a))

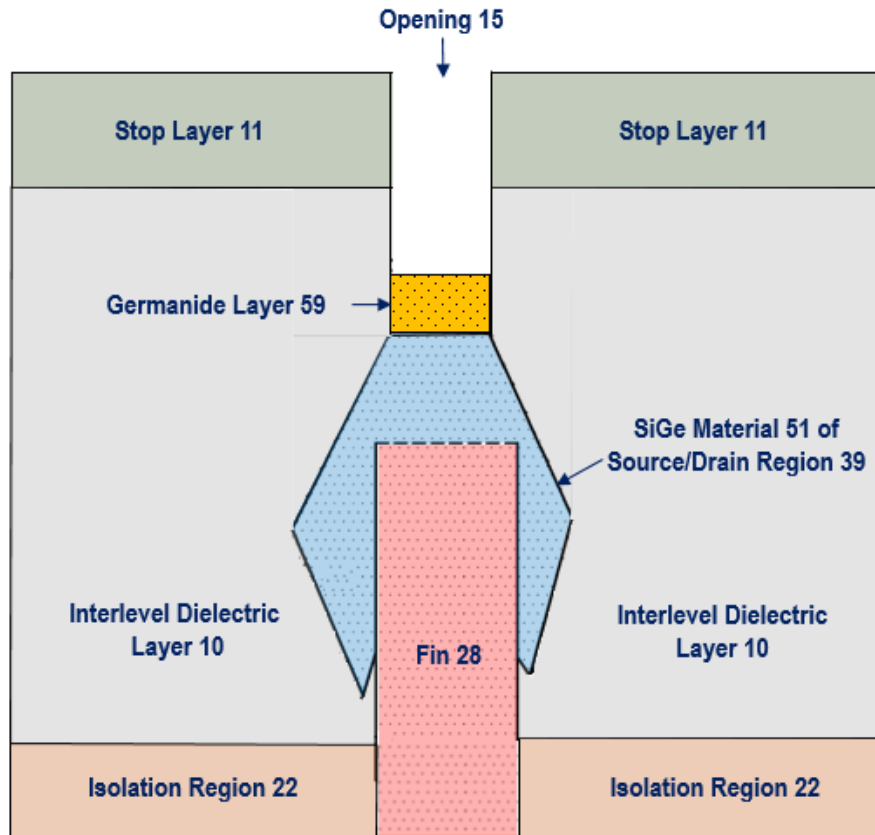
- b) Deposit a metal layer 57 (e.g., titanium) as taught in Tung and analogously to Yu's metal containing layer 22. SAMSUNG-1009, [0072]-[0074], FIG. 3; SAMSUNG-1006, [0042], [0079]-[0080], FIGS. 15.



Tung-Yu-Simonelli (Example Formation Illustration 3(b))

- c) Anneal metal layer 57 (e.g., titanium) with germanium cap layer 55 to form a germanide layer 59, and remove unreacted metal 57.⁵ SAMSUNG-1009, [0075], FIG. 4; SAMSUNG-1006, [0043]-[0045], [0081], FIGS. 4e, 16.

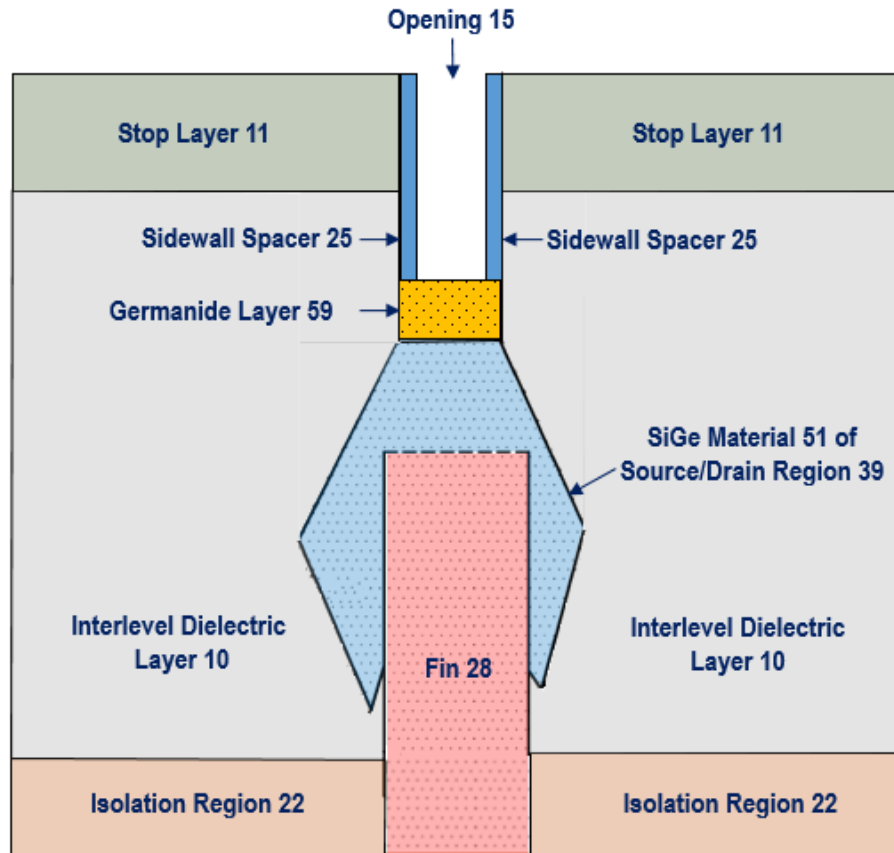
⁵ The location or depth of the interface between germanide layer 59 and an under-layer such as the SiGe material 51 of source/drain region 39 may vary based on



Tung-Yu-Simonelli (Example Formation Illustration 3(c))

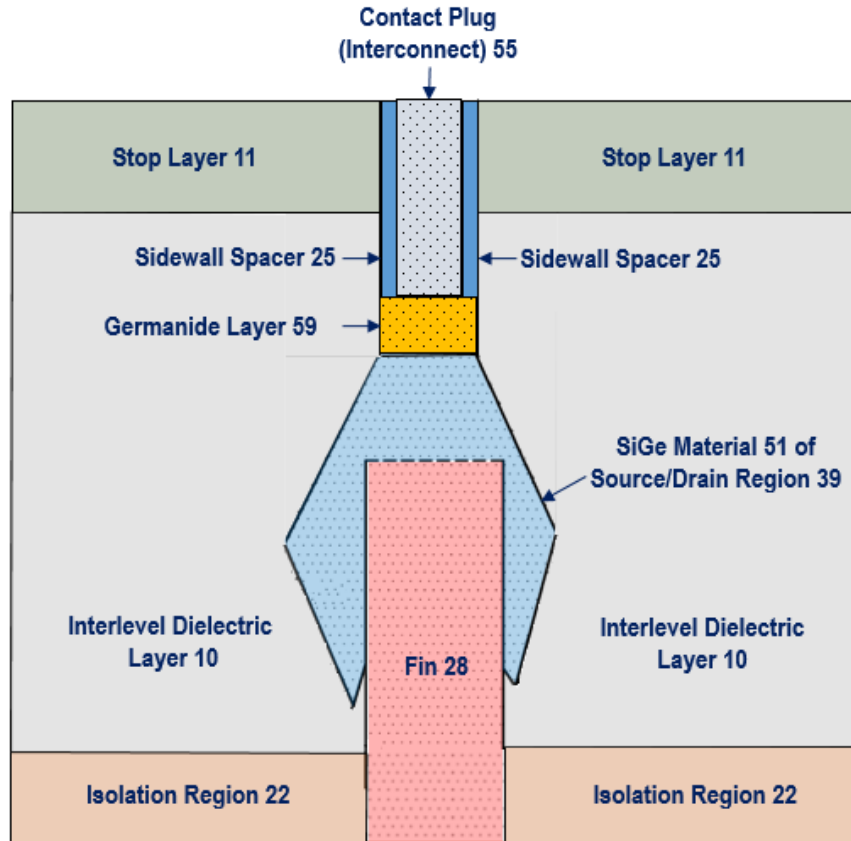
- (4) Form sidewall spacers 25 within opening 15. SAMSUNG-1009, [0076]-[0079], FIGS. 5-6; SAMSUNG-1003, ¶69.

how much material, including material from the germanium cap layer 55, is consumed through the annealing process. SAMSUNG-1006, [0043]-[0045], [0081]; *infra*, [1m]-[1n]; SAMSUNG-1003, ¶68, FN 5.



Tung-Yu-Simonelli (Example Formation Illustration 4)

- (5) Form contact plug (interconnect) 55 within opening 15 and on germanide layer 59. SAMSUNG-1009, [0080], FIG. 1; SAMSUNG-1003, ¶70.



Tung-Yu-Simonelli (Example Formation Illustration 5)

A POSITA would have sought to implement Yu-like interconnect structures with Tung's FinFET to make use of the FinFET in an ordinary IC having one or more layers of interconnect wiring. SAMSUNG-1003, ¶71. Tung itself indicates that FETs are commonly implemented in ICs, e.g., with its explanation that “[s]emiconductor devices compris[ing] **integrated circuits** [] are formed on semiconductor wafers.” SAMSUNG-1006, [0003] (emphasis added). Interconnect structures based on Yu would have been useful in the combination to facilitate connections between the FinFET and other components in an IC through one or more

layers of interconnect wiring, e.g., by coupling the source and drain regions 39 to metal contact plugs (interconnects) 55 by way of germanide layers 59. SAMSUNG-1003, ¶71.

Moreover, a POSITA would have appreciated and it would have been obvious based on Yu to implement an IDL 10 in the FinFET of the resulting Tung-Yu-Simonelli combination to isolate conductive components of the transistor from each other and from components at other layers in the IC. SAMSUNG-1003, ¶72. A POSITA would have been prompted to form openings 15 in the IDL 10 as taught in Yu to provide access to respective portions of the source/drain regions 39 for the formation of contacts to the source/drain regions 39. *Id.* A POSITA would have sought to form germanide layers 59 over the exposed portions of the source/drain regions 39 and in openings 15 as taught by Tung and consistent with Yu to provide an improved contact structure that would expectedly reduce the Schottky barrier height and lower resistance to the source/drain regions 39. *Id.* More, it would have been obvious to fill openings 15 with metal contact plugs 55 as taught in Yu to electrically couple the source/drain regions 39 via germanide layer 59 to interconnect wiring in one or more layers above the FinFET in the IC. SAMSUNG-1003, ¶72.

A POSITA also would have been motivated to apply Yu's interconnect

structures in combination with Tung's FinFET to obtain the benefits of Yu's dielectric sidewall spacers 25. SAMSUNG-1003, ¶73. Yu explains that dielectric sidewall spacers 25 are beneficial to isolate the contact plugs (interconnects) 55 from the gate electrode, thereby "reduc[ing] incidence of shorting" between contact 55 and the gate electrode. SAMSUNG-1009, [0042]. With increased isolation, the contact openings (and ultimately the contact plugs 55) can be formed more closely to the gate electrode, which can in turn lead to reduced contact resistance to the source/drain regions 39 and improved capabilities for the transistor to be produced at smaller scales as explained in Yu. *Id.*, [0018]-[0019], [0042]; SAMSUNG-1003, ¶73.

Implementing interconnect structures based on Yu with Tung's FinFET also would have amounted to a merely obvious application of Yu's techniques to improve a similar device based on Tung in substantially the same way. SAMSUNG-1003, ¶74. Here, "when a patent 'simply arranges old elements with each performing the same function it had been known to perform' and yields no more than one would expect from such an arrangement, the combination is obvious." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 417 (2007). Tung expressly focuses on solutions for reducing contact resistance in a non-planar transistor (e.g., a FinFET), and specifically indicates that additional interconnect structures including a "contact"

should be formed over the germanide layers 59 to complete fabrication of the device. SAMSUNG-1006, [0005], [0032]-[0034], [0036], [0064]. Yu then describes straightforward techniques for forming interconnect structures consistent with Tung's suggestions for the same. SAMSUNG-1003, ¶74. A POSITA would have had a reasonable expectation of success implementing the combination in light of Yu's extensive disclosure and structural similarities between the transistors described in each of Tung and Yu. *Id.* For example, Yu specifically teaches that its techniques are suitable for a wide range of semiconductor devices **including Fin-FETs**, and Yu's interconnect structures would be formed in the combination with a FinFET in a substantially similar manner to their formation as disclosed in Yu. *Id.*; SAMSUNG-1009, [0020], [0081].

Further, a POSITA would have found it obvious to form germanide layers 59 in the transistor of the Tung-Yu-Simonelli combination by first forming a doped germanium cap layer akin to Tung's layer 55 *within* openings 15 over portions of the source and drain regions 39 (e.g., over portions of the epitaxially grown silicon-germanium akin to Tung's SiGe material 51) exposed by the openings 15, and then depositing and annealing a metal compound such as titanium over the cap layer. SAMSUNG-1009, [0030]-[0038], FIGS. 1, 6; SAMSUNG-1003, ¶75. This approach is consistent with Yu's teaching to form metallized semiconductor contact layer 20 within openings 15 of IDL 10, and it would have been obvious for a

POSITA seeking to implement interconnect structures based on Yu to follow Yu's teaching in this regard. SAMSUNG-1003, ¶75. In fact, Yu specifically touts advantages of its interconnect structures with respect to contacts that are confined within openings 15 rather than contacts formed before the IDL 10, which would have led a POSITA to maintain a similar configuration in the Tung-Yu-Simonelli combination. SAMSUNG-1009, [0018]-[0019], [0042]; SAMSUNG-1003, ¶75.

To be sure, it would not be necessary to form Tung's doped germanium cap layer 55 over substantially an entire outer surface of the SiGe material 51 of the source/drain regions 39 as shown in Tung's figures to realize the benefits of a germanide layer 59 formed by annealing a metal with such a cap layer 55 that had been originally formed over such a large area. SAMSUNG-1003, ¶76. A POSITA would have understood and it would have been obvious that these benefits would still be substantially realized in the areas that the germanide layers 59 are actually formed, including within openings 15 as taught in Yu. *Id.* For example, using doped germanium cap layers 55 within openings 15 to form germanide layers 59 within openings 15 would still improve source/drain contact resistance by reducing the Schottky barrier height at the contact interface. SAMSUNG-1003, ¶76. Likewise, epitaxial growth of the germanium cap layer 55 would still have been obvious to perform in an opening 15 according to well-known processes, e.g., to achieve uniform doping and to "prevent[] nucleation of residual defects" as taught

in Tung. SAMSUNG-1006, [0005], [0020]-[0021]; SAMSUNG-1003, ¶76. Tung never indicates that the germanide layer 59 must be formed before an IDL in order to make effective use of the germanide layer 59. To the contrary, Tung emphasizes that its techniques “can be embodied in a wide variety of ... contexts” and are not limited to the specific examples disclosed in the specification. SAMSUNG-1006, [0019]-[0020], [0009], [0082]-[0084]. This is consistent with the ’281 Patent itself, which also identifies nothing innovative about forming the germanide layers within openings in the dielectric layer. The ’281 specification describes different embodiments in which the germanide layers are formed either before or after the inter-layer dielectric over, and the specification specifically frames these alternatives as obvious design choices for which “any suitable combination of mask-ing/patterning and selective deposition techniques” would be suitable. *Cf.*, SAMSUNG-1001, 12:64-67; *compare* FIGS. 3A-3I with FIGS. 5A-5F.

Further, a POSITA would have appreciated, as suggested by Tung, that formation of germanide over the entirety of the source/drain region would reduce the spacing between the germanide and (i) the gate electrode and (ii) neighboring transistors. SAMSUNG-1006, [0058], [0075]. A POSITA would have found it desirable to restrict the lateral expansion of the germanide towards the gate and neighboring transistors. SAMSUNG-1003, ¶77. Such lateral restriction would be achieved through Yu’s techniques by confining the germanide to the openings 15

in IDL 10. Therefore, a POSITA would have understood that an improved transistor structure would be attained by using Yu's germanide confinement to the openings in Tung. *Id.*

A POSITA also would have found it obvious to try forming the germanide layers 59 (and hence the germanium cap layers 55) within openings 15. SAMSUNG-1003, ¶78. Yu identifies only two options in this regard—i.e., either (i) form the germanide layers 59 (or semiconductor alloy contact layer 20) over a non-confined surface of the source/drain regions before forming the IDL 10 or (ii) form the germanide layers 59 after forming the IDL 10 within openings 15. SAMSUNG-1009, [0018] (“In comparison to metal semiconductor alloy contacts that are not formed within the trench[] ...”). It would have been obvious to try forming germanide layers 59 within the openings 15, e.g., to reduce the amount of epitaxial growth required to form cap layer 55, to better align the germanide layers 59 with contact plugs (interconnects) 55 formed within the openings 15 in a manner that avoids formation of excess germanide beyond the outer bounds of openings 15 (which would leave germanide uncontacted by the contact plugs 55), and to optimize fabrication processes and performance attributes (e.g., contact resistance) that a POSITA would have understood would be achieved by the different approaches in a given design. SAMSUNG-1003, ¶78.

Grading Germanium Content in the Source and Drain Regions

Tung describes techniques for growing a SiGe material 51 over the fins 28 of a FinFET to form source and drain regions 39. *Supra*, Section IV.A.1; SAMSUNG-1006, [0040], [0074]. Nonetheless, Tung provides no numerical values for the germanium concentration in SiGe material 51, nor does Tung describe well-known techniques for varying the germanium content in films like SiGe material 51. SAMSUNG-1003, ¶79. On the other hand, Simonelli expressly describes techniques for grading germanium within SiGe material of the source and drain regions of a FinFET such that portions of the SiGe material closest to the silicon-based growth substrate have a lower concentration of germanium and portions of the SiGe material further from the silicon-based growth substrate have increasingly higher germanium content (e.g., 50-atomic percent germanium). *Supra*, IV.A.3.

A POSITA would have found it obvious to form Tung's SiGe material 51 in the source and drain regions 39 according to Simonelli's teachings such that the concentration of germanium in the SiGe material 51 of the FinFET in the Tung-Yu-Simonelli combination would increase from a lower level near the growth substrate to a higher level near the outer surfaces further from the substrate. SAMSUNG-1003, ¶80. Multiple reasons would have motivated a POSITA to grade the germanium content in the FinFET of the Tung-Yu-Simonelli combination in this manner to a concentration in excess of 50%. *Id.*

First, it would have been obvious to grade the germanium content in the SiGe material 51 of the Tung-Yu-Simonelli FinFET to a concentration in excess of 50% to ease the transition between the bulk silicon or silicon-rich substrate material (e.g., fin 28 (*see infra* [1a])) over which material 51 is grown and the germanium material of cap layer 55 is formed. SAMSUNG-1006, [0058], [0078]; SAMSUNG-1003, ¶81. Grading the germanium content in semiconductor material 51 in this manner would have been beneficial to reduce misfit dislocations at the interface between SiGe material 51 and the silicon-rich substrate material on which material 51 is grown, to reduce defects through the entire formation of SiGe material 51, and to reduce misfit dislocations at the interface between SiGe material 51 and the germanium cap layer 55. SAMSUNG-1003, ¶81. A POSITA would have appreciated that reducing or even eliminating misfit dislocations and other defects in the growth of semiconductor material 51 would significantly improve performance of the FinFET, especially since such defects were known to produce unwanted leakage currents and parasitic capacitances. Reducing/preventing misfit dislocations also would prevent or relax forces intended to impart stress on the channel to increase the mobility of charge carriers in the channel and improve ON-currents through the transistor. SAMSUNG-1003, ¶81.

Additionally, absent grading between the silicon-rich growth substrate (e.g., fin 28) and the germanium cap layer 55, the thickness and surface area over which

semiconductor material 51 could be grown without defects would be significantly limited—i.e., a limitation that would in turn risk (i) restricting the ON-current that could flow through the transistor, (ii) increasing contact resistance at the source and drain regions due to decreased growth area, and (iii) limiting the amount of stress that could be imparted on the channel in a strained configuration. SAM-SUNG-1003, ¶82. In contrast, by grading the germanium content in SiGe material 51, lattice mismatch between the silicon-rich substrate material and SiGe material 51 would be reduced to avoid misfit dislocations by ensuring a lower germanium content near the substrate interface. *Id.* Similarly, lattice mismatch between the germanium cap layer 55 and SiGe material 51 would be reduced by ensuring a higher germanium content near the interface of cap layer 55. *Id.* For similar reasons, it would have been obvious to implement one or more transition layers in SiGe material 51 as taught in Simonelli (or to implement smooth transitional grading) to bridge the otherwise large difference in germanium content between the silicon-rich growth substrate (e.g., fin 28) and the cap layer 55. *Id.* Indeed, grading the germanium to a concentration in excess of 50% in SiGe material 51 would have been obvious to bridge the gap in germanium content between the growth substrate and cap layer 55 and to reduce lattice mismatch at the interfaces between the growth substrate, SiGe material 51, and cap layer 55. *Id.*

Second, it would have been obvious to grade the germanium content in the

material 51 of the Tung-Yu-Simonelli FinFET to a concentration in excess of 50% to increase the mobility of charge carriers in the source and drain regions 39 (i.e., in material 51), and consequently decrease parasitic resistance in the FinFET. SAMSUNG-1003, ¶83. It was well known that the mobility of electrons and holes through germanium is greater than the mobility of electrons and holes through silicon, and hence increasing the germanium content in SiGe material 51 would predictably lead to an increase in charge carrier mobilities in the source and drain regions 39. SAMSUNG-1003, ¶83. Increasing carrier mobility and decreasing parasitic resistance would improve performance of the FinFET. *Id.*

Third, it would have been obvious to grade the germanium content in the material 51 to a concentration in excess of 50% to better accommodate high dopant concentrations (e.g., boron) with greater dopant confinement and higher electrical activation than would be achieved in a matrix with a higher concentration of silicon. SAMSUNG-1003, ¶84.

Fourth, it would have been obvious to grade the germanium content in the material 51 of the Tung-Yu-Simonelli FinFET's source and drain regions 39 to a concentration in excess of 50% to induce greater stress in the channel region—i.e., a technique that was commonly employed before the '281 Patent to increase the mobility of charge carriers in the channel region of field-effect transistors (which would in turn increase drive currents). SAMSUNG-1008, [0042]; *see also id.*,

[0024], [0038], [0044], [0058]; SAMSUNG-1003, ¶85.

For example, in a p-type FET, when the channel is formed of doped silicon and the source and drain regions are formed of an oppositely doped SiGe material, a lattice mismatch results between the materials that induces compressive strain on the channel due to the presence of larger Ge atoms in the source and drain regions. SAMSUNG-1003, ¶86. Tung's FIG. 2d, for instance, shows how the source and drain regions 39 extend beneath gate spacers 36, and this configuration would have led to compression of the channel region in typical FETs. SAMSUNG-1006, FIG. 2d; *see also* SAMSUNG-1008, [0038], [0044], [0042], [0053], [0058], FIGS. 11-12 (depicting source/drain regions 1210 protruding through spacers 1010); SAMSUNG-1003, ¶86.

To the extent Tung does not expressly disclose that source and drain regions 39 are formed in a manner specifically designed to induce strain in the channel region, it would have been obvious to implement the source and drain regions 39 in this fashion in the FinFET of the Tung-Yu-Simonelli combination. SAMSUNG-1003, ¶87. FETs with strained channels were exceedingly common in both planar and non-planar designs before the '281 Patent, and a POSITA would have sought to implement a strained channel in the Tung-Yu-Simonelli FinFET to obtain well-known benefits including increased channel mobility and drive current levels.

SAMSUNG-1003, ¶87. For example, strained configurations are frequently realized by growing SiGe source and drain regions over a surface or cavity of a substrate on either side of a channel region like Simonelli's source and drain regions 1210. *See* SAMSUNG-1008, [0051], FIGS. 11-12 (depicting source and drain regions 1210 formed on either side of channel region 110); *see also id.*, [0034]-[0039], [0042], [0044]-[0051]. It would have been obvious to similarly form the source and drain regions 39 by re-growing SiGe material 51 on either side of the channel (e.g., rather than overgrowing SiGe material on fin 28) to impart strain on the channel region according to known and predictable techniques. Indeed, such techniques would have amounted to an obvious use of Simonelli's teachings to improve a similar device (i.e., Tung's FinFET) in a similar way. *KSR*, 550 U.S. at 417; SAMSUNG-1003, ¶87.

A POSITA would have had a reasonable expectation of success grading the germanium content in the SiGe material 51 of the Tung-Yu-Simonelli FinFET to a concentration in excess of 50%. Simonelli and Tung both describe non-planar FETs (e.g., FinFETs), and both describe techniques for epitaxially growing SiGe material in the source/drain regions of a device. SAMSUNG-1003, ¶88. Simonelli's teachings for grading germanium content in the source and drain regions would thus be applied to Tung's FinFET in a substantially similar context. Further, graded epitaxial growth was well known before the '281 Patent, and it would

have been well within the skill of a POSITA to vary the relative concentrations of silicon and germanium during the growth process of SiGe material 51 according to Simonelli's teachings. SAMSUNG-1003, ¶88. Moreover, for implementations of the Tung-Yu-Simonelli combination that involve modifications of Tung's FinFET to achieve a strained channel region, a POSITA would have had a reasonable expectation of success in light of the substantially similar types of FinFET devices described in each of Tung and Simonelli, the long-established practice of introducing strain in the channel regions of FETs using techniques like those disclosed in Simonelli, and Tung's own acknowledgment that a POSITA would have known how to make a range of modifications to its device. SAMSUNG-1006, [0019]-[0020], [0082]-[0084]; SAMSUNG-1003, ¶¶88-89.

The Tung-Yu-Simonelli combination would have rendered obvious each of claims 1 and 5-8 for the reasons described in detail below.

Element [1pre]

To the extent the preamble is a limitation, the Tung-Yu-Simonelli combination would have rendered obvious [1pre], e.g., in view of Tung's disclosure of an integrated circuit structure as a non-planar FET. SAMSUNG-1006, [0002]-[0004]; SAMSUNG-1003, ¶91; *see also id.*, ¶90. Tung, in FIGS. 13-16, for example, describes "various stages of manufacturing" of a non-planar transistor (e.g., a FinFET) having "a doped semiconductor layer and a metal silicide [] formed on a

raised source/drain structure.” SAMSUNG-1006, [0072]; *see also id.*, [0073]-[0082], FIGS. 13-16. Tung further explains that, although FIGS. 13-16 “illustrate the fabrication of a device with at least two fins 28,” “the method described in FIG. [sic] 13-16” can also be “used in fabrication of a device with a single fin” to form the device “corresponding to the embodiment described in FIG. 2.” *Id.*, [0082]; *see also id.*, [0032]-[0034], FIG. 2. Tung’s description of FIGS. 4a-4e provides additional detail of a single-fin embodiment consistent with the embodiments described with respect to FIGS. 13-16. *Id.*, [0039]-[0045]; FIGS. 4a-4e.

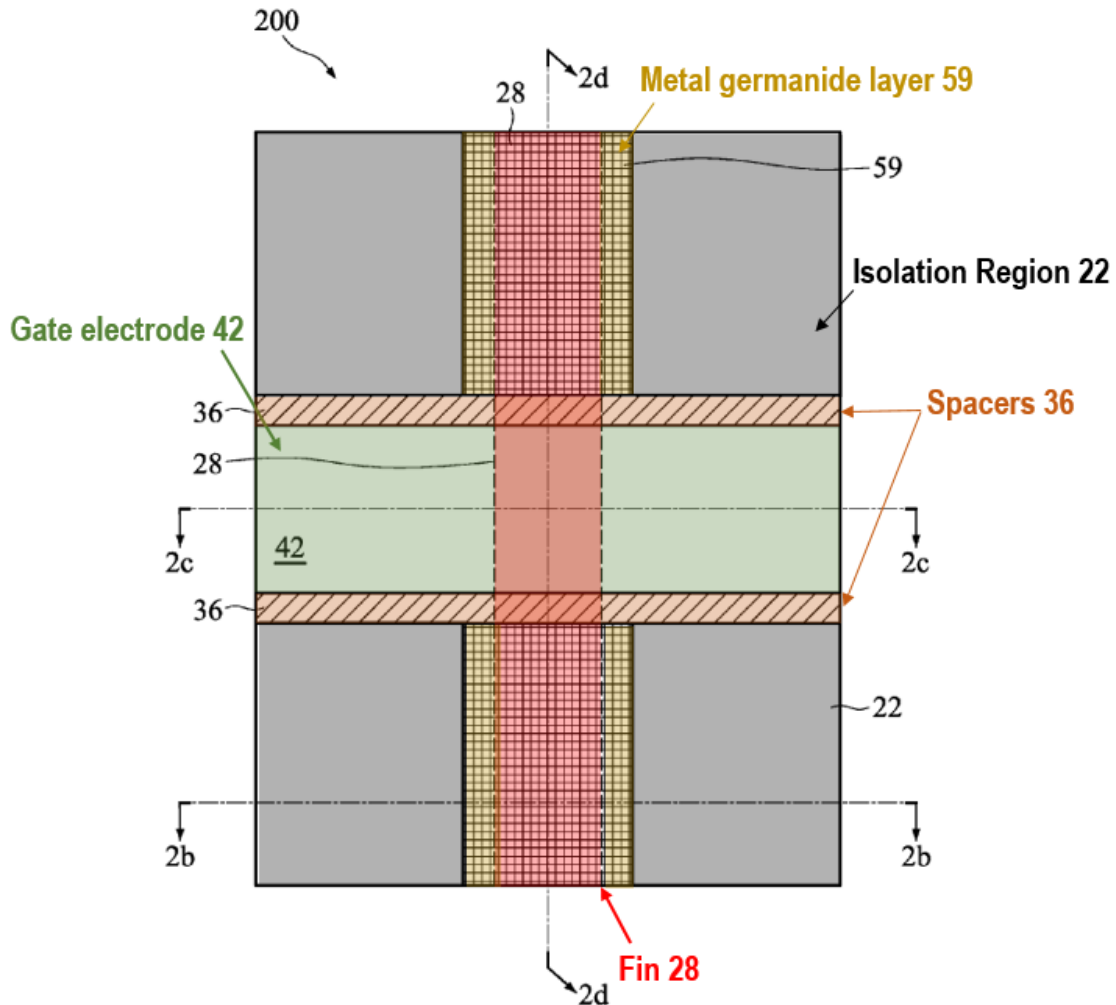


FIG. 2a

Tung, FIG. 2a (annotated)

Element [1a]

The Tung-Yu-Simonelli combination would have rendered obvious [1a], e.g., in view of Tung's disclosure of a fin 28 comprised of silicon. In particular, in various embodiments, fin 28 is formed from substrate 20, which Tung explains is made from material including silicon. SAMSUNG-1006, [0048] ("substrate 20 comprises bulk silicon" or "substrate 20 comprises bulk silicon germanium

(SiGe)), [0051] (“Fins 28 may be formed by recessing the top surfaces of the isolation regions 22, and hence leaving the fins 28” of substrate 20), [0049], FIGS. 2, 5, 6a-6b, 13-16; *supra*, [1pre]; SAMSUNG-1003, ¶92. Tung also teaches that the source and drain regions 39 can be formed in the fin, and that the source and drain regions 39 can include semiconductor material 51 including silicon. SAMSUNG-1006, [0074], [0040], [0033]; *infra*, [1c]/[1h].

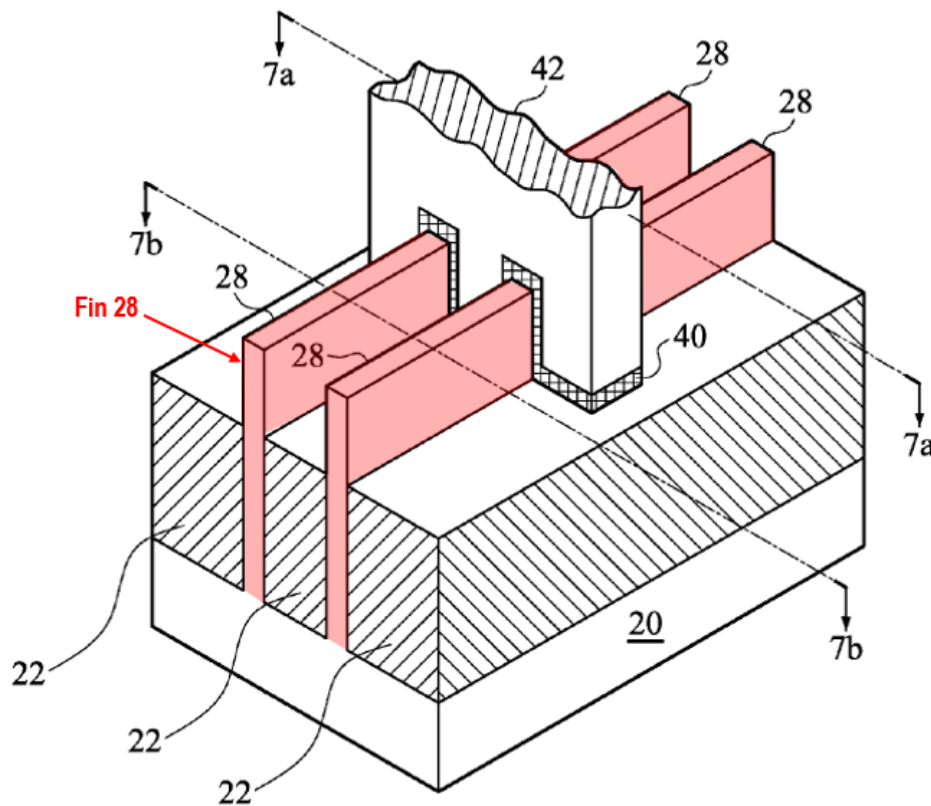


FIG. 7c

Tung, FIG. 7c (annotated)

Element [1b]

The Tung-Yu-Simonelli combination would have rendered obvious [1b],

e.g., in view of Tung's disclosure of a gate electrode 42 over fin 28. SAMSUNG-1006, [0053]-[0055], FIGS. 2a, 2c, 7c; SAMSUNG-1003, ¶¶93-94.

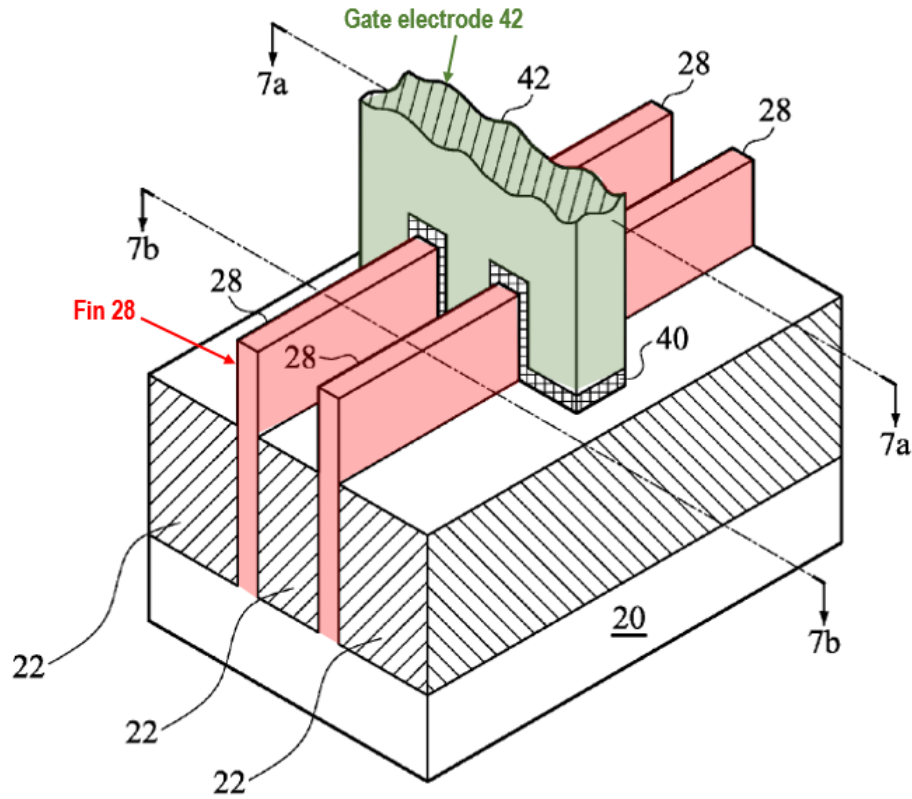


FIG. 7c

Tung, FIG. 7c (annotated)

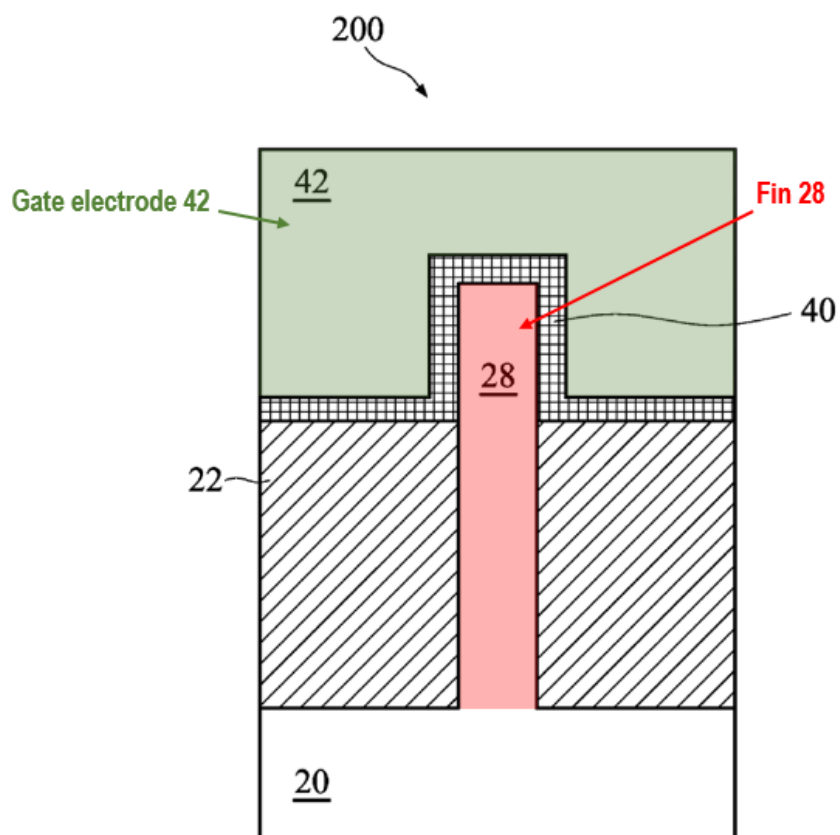


FIG. 2c

Tung, FIG. 2c (annotated)

Tung further discloses that the gate electrode 42 has a first side and a second side opposite the first side:

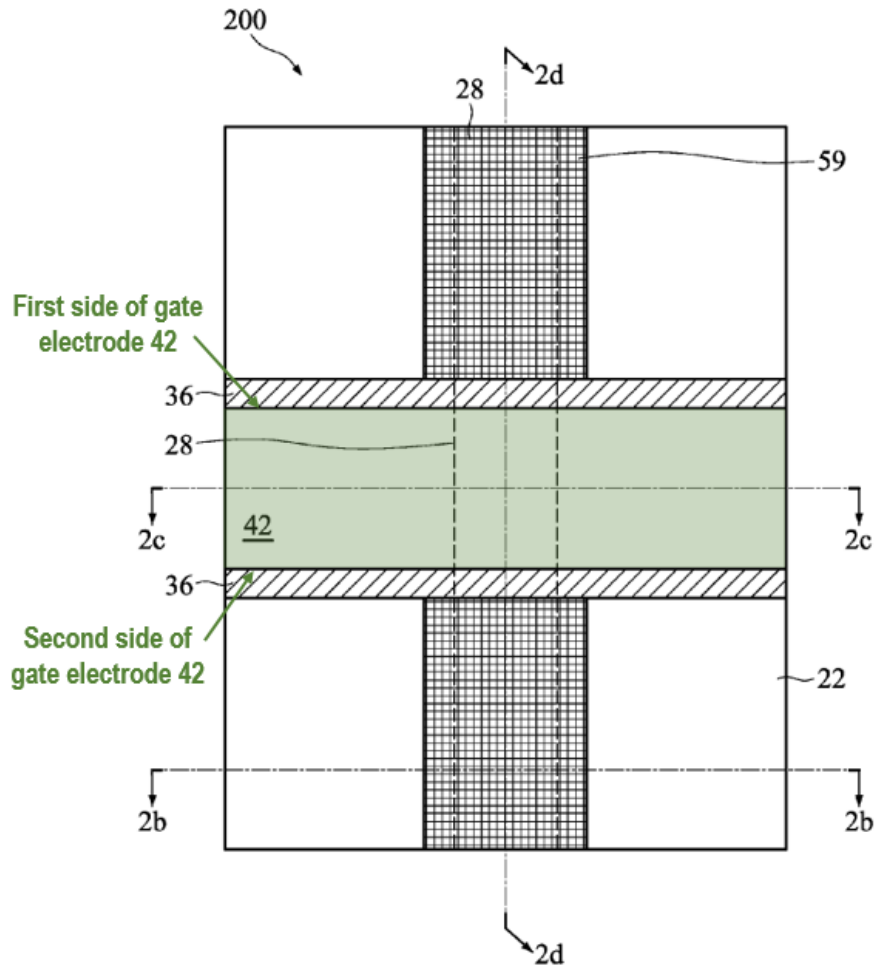


FIG. 2a

Tung, FIG. 2a (annotated)

Elements [1c], [1g]

The Tung-Yu-Simonelli combination would have rendered obvious [1c] and [1g], e.g., in view of Tung's disclosure of dielectric spacers 36 along the first and second sides of gate electrode 42. SAMSUNG-1006, [0023], [0026], [0055]-[0057], [0065], [0073]-[0074], FIGS. 2A, 2D; SAMSUNG-1003, ¶95. A POSITA would have understood and it would have been obvious, consistent with common

practices before the Critical Date, to form spacers 36 from a dielectric material to achieve predictable benefits including enhanced isolation of the gate electrode and reduced gate leakage currents. SAMSUNG-1003, ¶95.

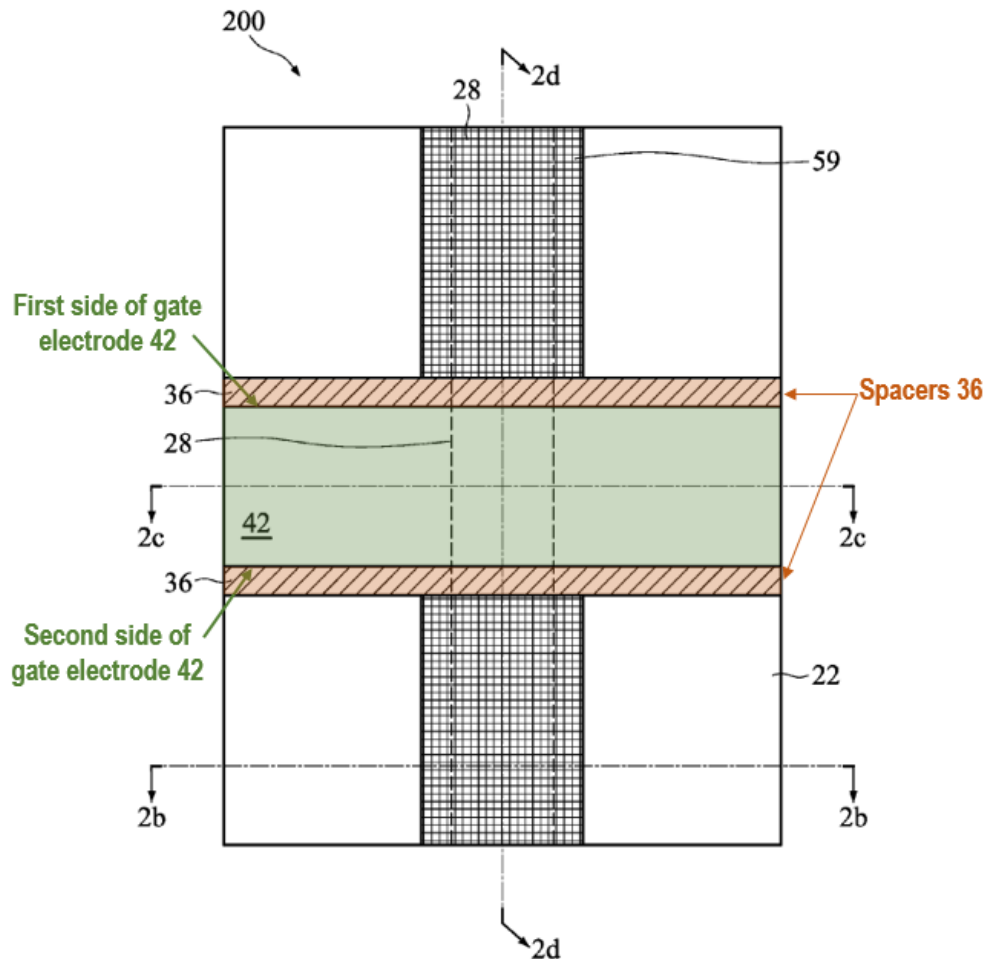


FIG. 2a

Tung, FIG. 2a (annotated)

Elements [1d], [1h]

The Tung-Yu-Simonelli combination would have rendered obvious [1d] and [1h], e.g., in view of Tung's disclosure of first and second source or drain regions

39 formed proximate either side of gate electrode 42. SAMSUNG-1006, [0032]-[0034], [0057], [0074]-[0078], FIGS. 2a, 2d, 8, 13; SAMSUNG-1003, ¶96; *see also id.*, ¶¶97-98; *cf.* SAMSUNG-1001, FIG. 6 (depicting source/drain epitaxial regions 631 similarly proximate to either side of gate electrode 640).

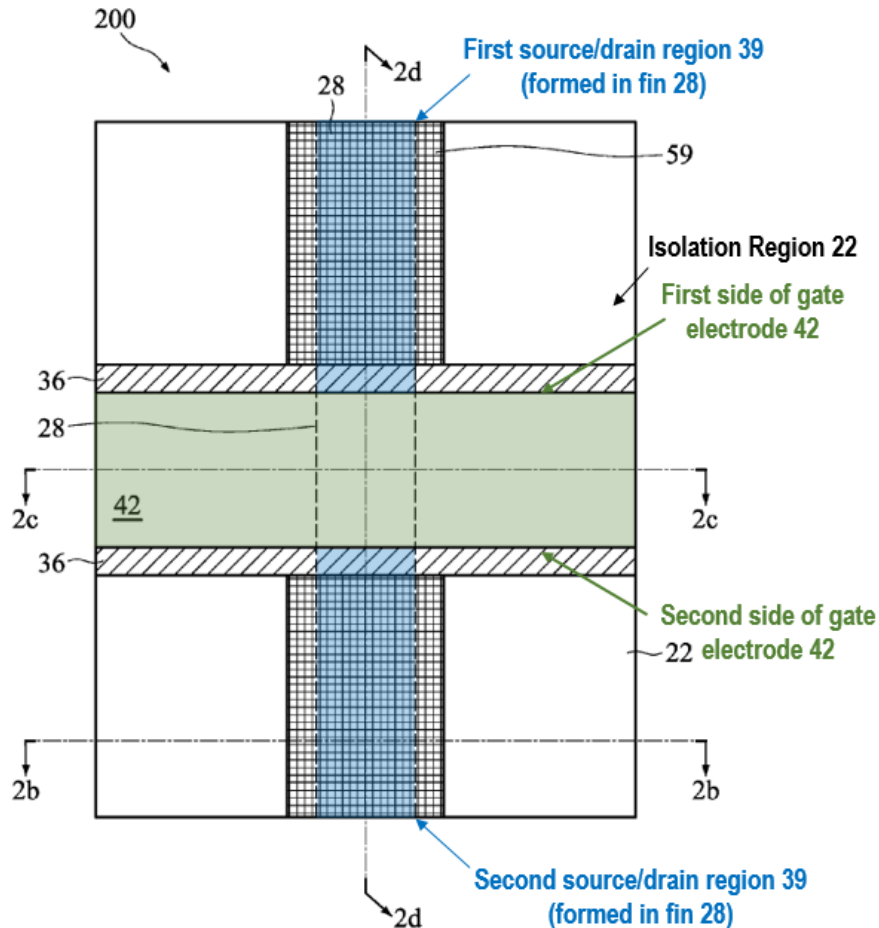


FIG. 2a

Tung, FIG. 2a (annotated)

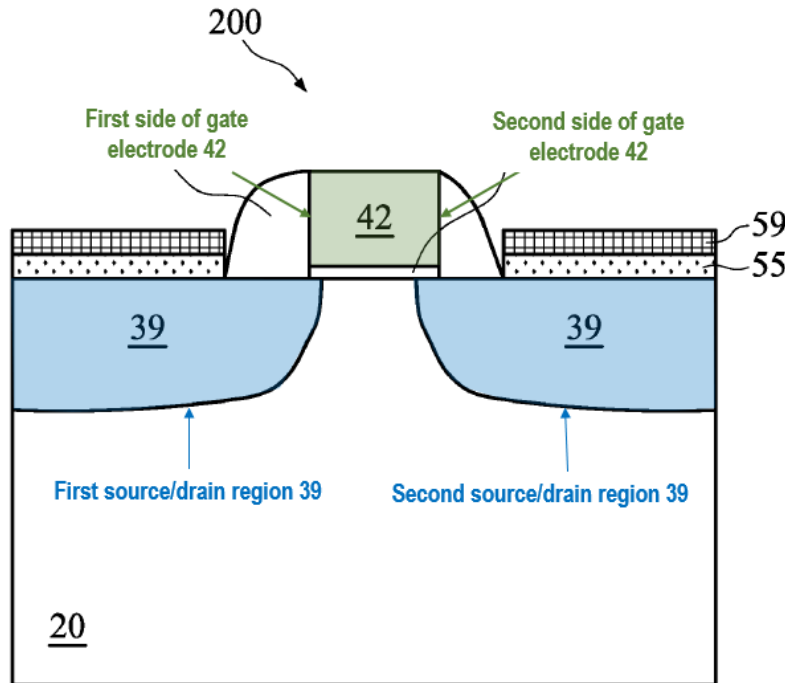


FIG. 2d

Tung, FIG. 2d (annotated)

Tung further discloses and would have rendered obvious source/drain regions 39 that are each formed “in the fin.” SAMSUNG-1006, [0033] (“source/drain regions 39 is [sic] **disposed within the fins 28**”); *see also id.*, [0057], [0074]-[0077], FIGS. 2b, 13; *supra*, Ground 1A at [1c].

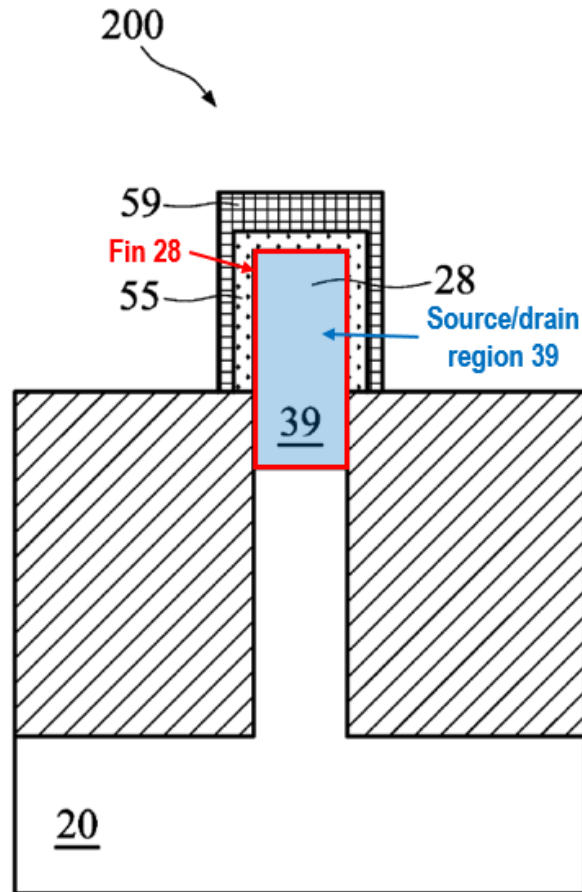


FIG. 2b

Tung, FIG. 2b (annotated)

Tung also teaches that the source and drain regions 39 can include an epitaxially grown SiGe material 51. SAMSUNG-1006, [0074], [0040]; *see also id.*, [0039]-[0045] and FIGS. 4a-4e, [0072]-[0082] and FIGS. 13-16. According to Tung's teaching that the source and drain regions 39 are disposed within the fin, semiconductor material 51 would also be disposed within the fin. *Id.*, [0033]. Moreover, it would have been obvious and a POSITA would have understood that

the epitaxially grown source/drain regions 39 adjacent to a portion of the fin in the channel region, whether formed over fin 28 or grown from the substrate 20 based on Simonelli's teachings (as described above in the overview of the Tung-Yu-Simonelli combination), to be "in the fin" consistent with a common understanding of the term "fin" by the Critical Date of the '281 Patent. SAMSUNG-1003, ¶98. Indeed, the '281 Patent embraces a similar view, which is apparent in light of the specification's disclosure of epitaxially grown source/drain regions 631 formed on opposite source/drain sidewalls of a channel body or fin 660. SAMSUNG-1001, 13:43-14:14, FIG. 6; *see also* SAMSUNG-1013, 32 (applicant's claims in a counterpart EP application refer to a "first source or drain region **in** the fin" that "compris[es] an epitaxial region (631) ... **formed on** ... one fin sidewall"); SAMSUNG-1003, ¶98. For the epitaxially grown source/drain regions 631 to be "in the fin," it would have been obvious that the claimed "fin" is not limited to a structure in the channel region like fin 660. *Id.* The claimed "fin" would instead encompass epitaxially grown source/drain regions formed on either side of a portion of the. SAMSUNG-1003, ¶98.

Elements [1e], [1i]

The Tung-Yu-Simonelli combination would have rendered obvious [1e] and [1i], e.g., in view of Tung's disclosure of a portion of the first and second source and drain regions 39 respectively beneath the first and second dielectric spacers 36.

bination overview).

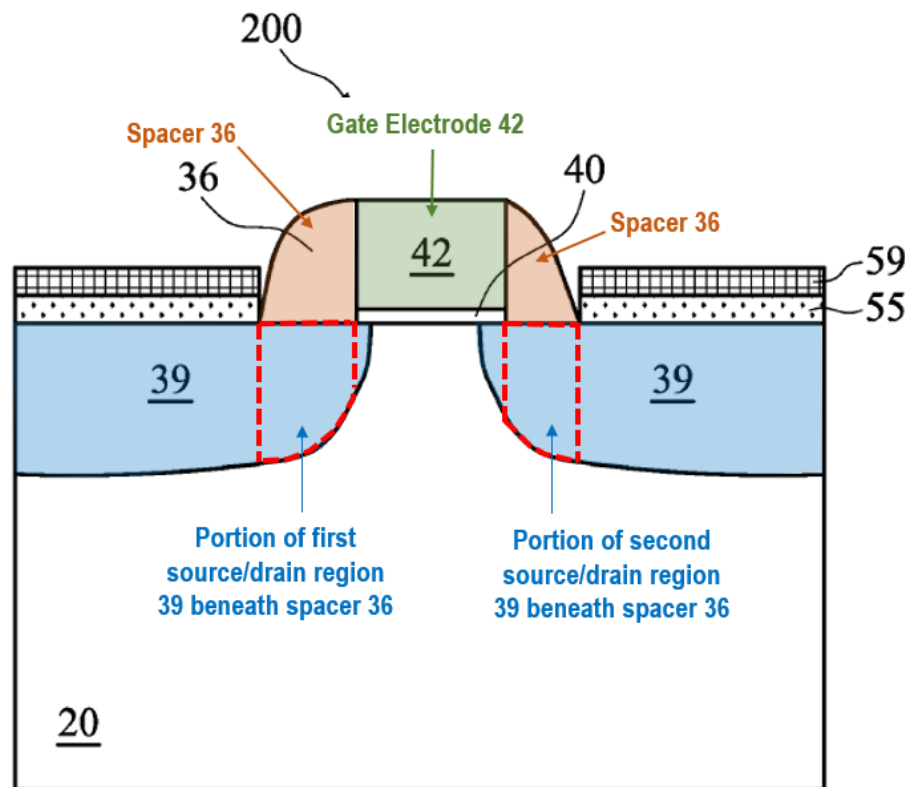


FIG. 2d

Tung, FIG. 2d (annotated)

Elements [1f], [1j]

The Tung-Yu-Simonelli combination would have rendered obvious [1f] and [1j]. SAMSUNG-1003, ¶100; *see also id.*, ¶101-106. For example, Tung teaches that “a selective epitaxial growth is performed to form semiconductor material 51” over fin 28, and the resulting structure including “semiconductor material 51 forms the source/drain regions 39.” SAMSUNG-1006, [0074], [0040]. In Tung, the substrate 20—and, hence, fin 28 (which is formed from substrate 20)—can be bulk silicon, while semiconductor material 51 can be “formed of a material different from that of substrate 20, for example, silicon germanium (SiGe)” *Id.*, [0074], [0048].

Although Tung does not expressly disclose the relative concentrations of silicon and germanium in SiGe layer 51, or whether the concentrations of silicon and germanium are uniform or graded during growth of layer 51, a POSITA would have understood that different options could be pursued to optimize one or more attributes of the device’s performance and/or fabrication. SAMSUNG-1003, ¶101. Simonelli, for example, describes solutions for achieving high concentrations of germanium in the source/drain regions of a non-planar FET through an epitaxial growth that involves increasing the germanium content in a SiGe material as

growth progresses away from the substrate (e.g., a bulk silicon substrate). SAM-SUNG-1008, [0053]-[0058]. FIG. 12, reproduced below, illustrates Simonelli's non-planar FET, similar to Tung's FinFET:

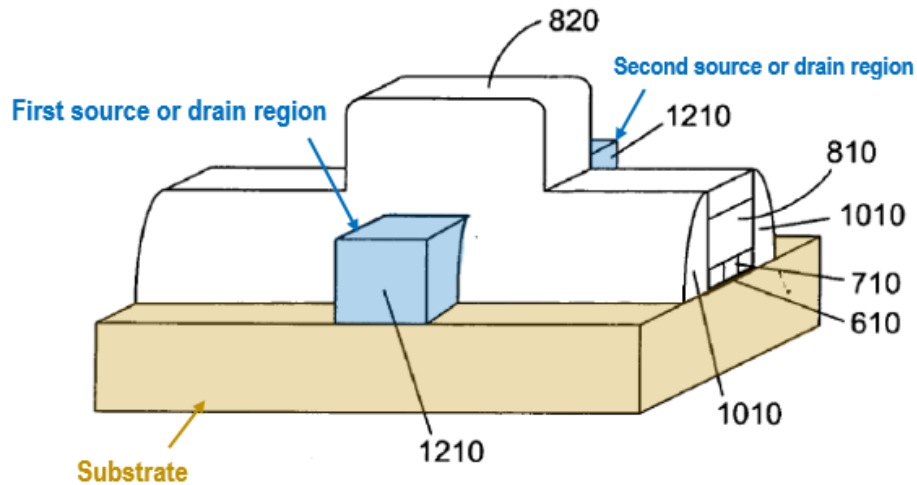


FIG. 12

Simonelli, FIG. 12 (annotated)

In Simonelli, source/drain regions 1210 are epitaxially grown “using a graded high-germanium content silicon-germanium film stack 1400.” SAM-SUNG-1008, [0051]. Film stack 1400 includes a series of layers 1410, 1420, 1430, each additional layer having higher germanium content than the preceding layer:



FIG. 14

Simonelli, FIG. 14 (annotated)

See also SAMSUNG-1008, [0053]-[0058], [0021]-[0024], FIGS. 14-15.

Simonelli further teaches that the concentration of germanium in the film stack can be graded from 20-25 atomic weight % in the seed layer 1410 to 40-55 atomic weight % in the high Ge content layer 1430. *Id.*, [0054], [0058]. As another example, Simonelli discloses that source/drain regions “may be filled with a graded germanium silicon alloy ... according to one or more methods such as the embodiment described below in FIG. 15” in which “[t]he graded germanium silicon alloy may be epitaxially deposited with a graded germanium concentration that may range from 10 atomic % to **50 atomic %.**” *Id.*, [0039].

For the reasons described in detail above in the overview of the Tung-Yu-Simonelli combination, it would have been obvious and a POSITA would have had ample motivation to grade the germanium content in material 51 of the source and drain regions 39 of the FinFET in the combination to a concentration in excess of

50%. *Supra*, Section IV.A.4; SAMSUNG-1003, ¶104.

To the extent Tung, Yu, and Simonelli do not expressly disclose a germanium concentration “**in excess of 50%**” as recited in [1f] and [1j], the claimed range nonetheless would have been obvious in view of Simonelli’s disclosure of grading to 50% germanium. SAMSUNG-1008, [0039]; SAMSUNG-1003, ¶105. As an initial matter, a POSITA would have understood that no fabrication process is perfectly controlled (nor is it possible to do so), and hence it would have been obvious that a FinFET intended to have germanium in its source and drain regions graded to a concentration of 50% as taught in Simonelli would commonly include a small or negligible amount more germanium than silicon. SAMSUNG-1003, ¶105. Even a single additional germanium atom would yield a germanium concentration in excess of 50%. *Id.*

Moreover, as described above in the overview of the Tung-Yu-Simonelli combination (*supra*, Section IV.A.4), a POSITA would have understood that the concentration of germanium in SiGe material 51 of the source and drain regions 39 impacts various properties of the FinFET, including the lattice constant at different depths of the SiGe material 51, the lattice mismatch at the interfaces on either side of SiGe material 51, the thickness and size at which the SiGe material 51 could be grown without defects, the mobility and parasitic resistance of the source and drain regions, and the amount of strain that could be imparted on a channel region. It

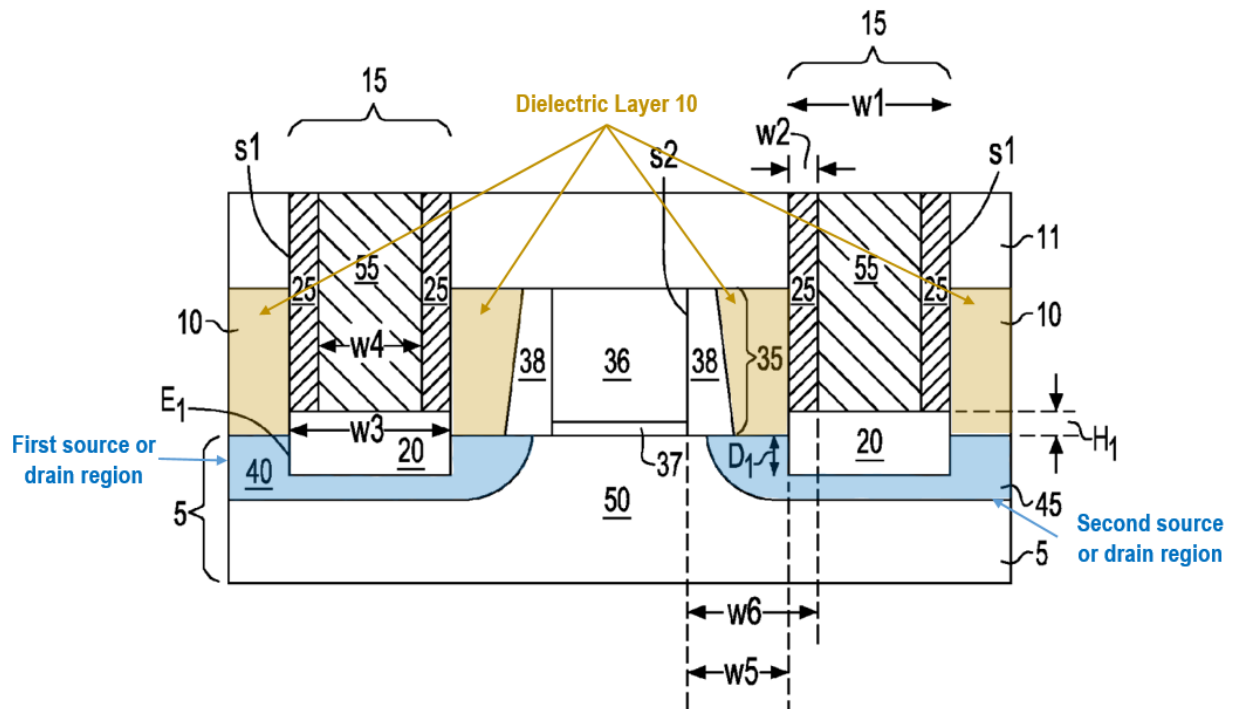
would have been obvious for a POSITA to grade germanium content in SiGe material 51 to a concentration in excess of 50% through routine experimentation to optimize one or more of these properties.⁶ SAMSUNG-1003, ¶106; *In re Peterson*, 315 F.3d 1325, 1329 (Fed. Cir. 2003) (“a *prima facie* case of obviousness exists when the claimed range and the prior art range do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties”); *du Pont*, 904 F.3d at 1006; *In re Brandt*, 886 F.3d 1171, 1176-1177 (Fed. Cir. 2018) (claimed range of “less than 6 pounds per cubic feet” rendered obvious by prior art disclosing an abutting range of “between 6lbs/ft³ and 25 lbs/ft³”); *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 783 (Fed. Cir. 1985); *In re Aller*, 220 F.2d 454, 456 (CCPA 1955)); MPEP §2144.05 (describing result-effective variables).

Element [1k]

The Tung-Yu-Simonelli combination would have rendered obvious [1k],

⁶ Notably, the '281 Patent identifies nothing critical about a germanium concentration “in excess of 50%” in source/drain regions capped with boron-doped germanium layers. SAMSUNG-1001, 3:57-62, 4:30-34, 6:48-62, 16:49-57. The '281 Patent discloses that a range of 30-70% germanium would be suitable in the source/drain regions, for example. *Id.*; SAMSUNG-1003, ¶67, FN 27.

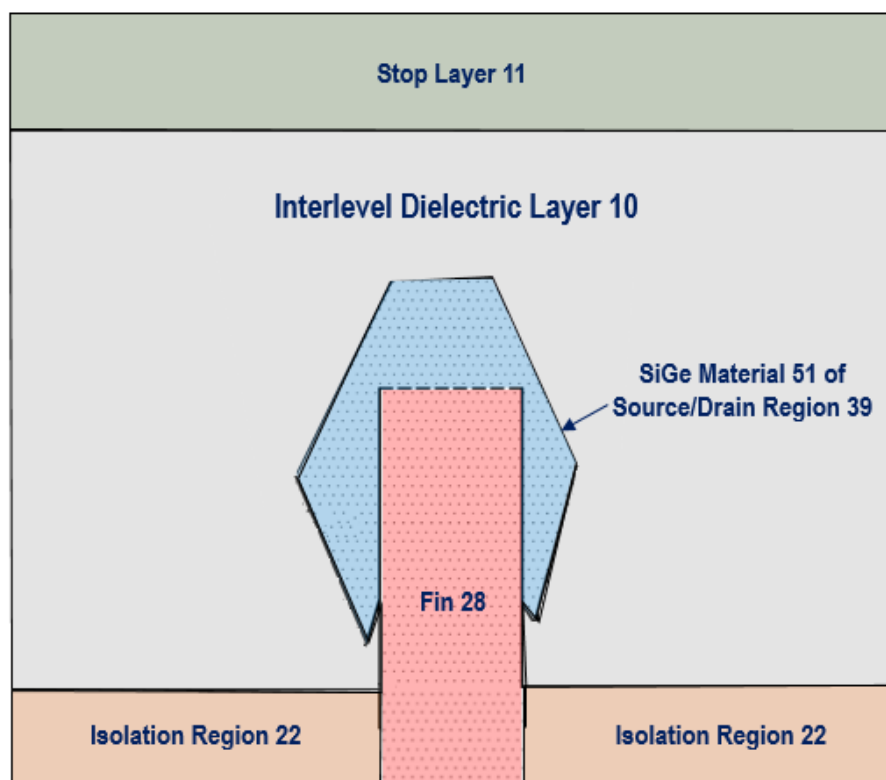
e.g., in view of Yu's disclosure of an inter-level dielectric layer ("IDL") 10 formed over the first and second source or drain regions. SAMSUNG-1009, [0030] ("An interlevel dielectric layer 50 may be formed atop the semiconductor substrate 5."), [0050], FIGS. 1, 2A, 6; SAMSUNG-1003, ¶107. For example, FIG. 1 shows IDL 10 partially covering source/drain regions 40/45. During fabrication, IDL 10 further covers the portion of the source/drain regions 40/45 exposed by openings 15 before the openings 15 are formed. SAMSUNG-1009, [0062]-[0064].



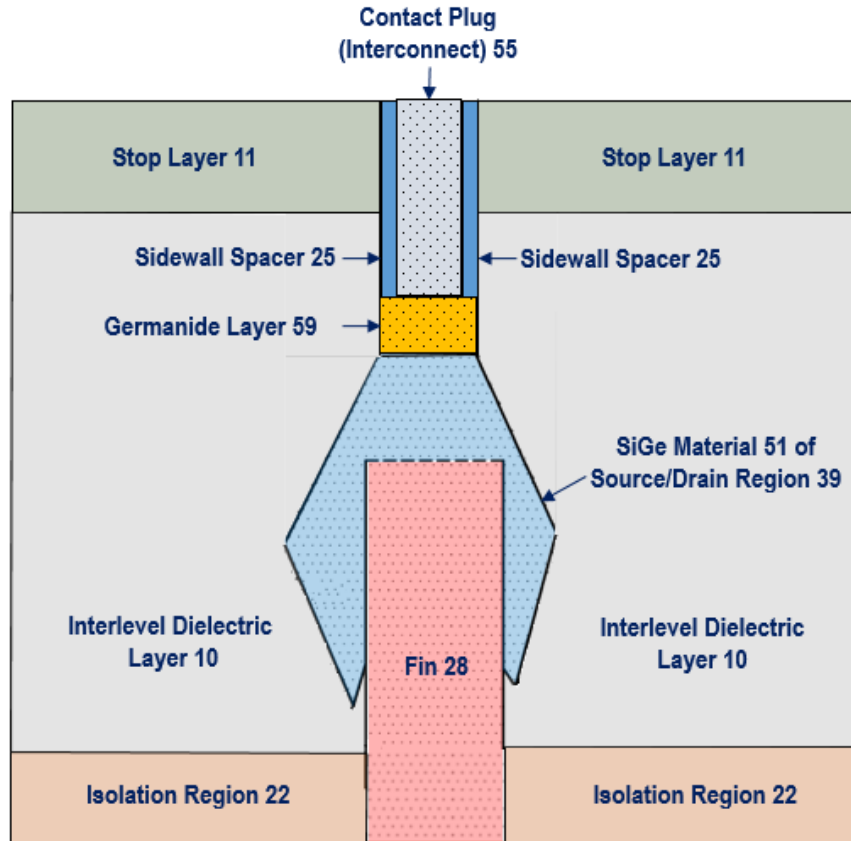
Yu, FIG. 1 (annotated)

Further, as discussed above in the overview of the combination, it would have been obvious to form interconnect structures like those described in Yu in the Tung-Yu-Simonelli transistor, and the resulting combination would have provided

and rendered obvious a dielectric layer (e.g., IDL 10) over the first and second source or drain regions 39. SAMSUNG-1003, ¶108; *supra*, Section IV.A.4 (overview).



Tung-Yu-Simonelli Example (Before Formation of IDL Opening)



Tung-Yu-Simonelli Example (After Contact Formation)

Element [11]

The Tung-Yu-Simonelli combination would have rendered obvious [11], e.g., in view of Yu's disclosure of first and second openings 15 formed in IDL 10 to expose a portion of the first and second source or drain regions 40 and 45.⁷

⁷ As another example, the narrowed portions of openings 15 that remain after forming dielectric sidewall spacers 25 additionally or alternatively would have rendered obvious the claimed first and second openings. SAMSUNG-1009, [0034], [0076]-[0078], FIGS. 5-6; SAMSUNG-1003, ¶109, FN 28.

SAMSUNG-1009, [0062]-[0064], FIGS. 2A-2B, 6; SAMSUNG-1003, ¶109. For example, Yu teaches that “openings 15 may be formed through the planarization stop layer 11 and the interlevel dielectric layer 10 to expose an upper surface of the semiconductor substrate 5 in which the source region 40 and the drain region 45 are present.” SAMSUNG-1009, [0062].

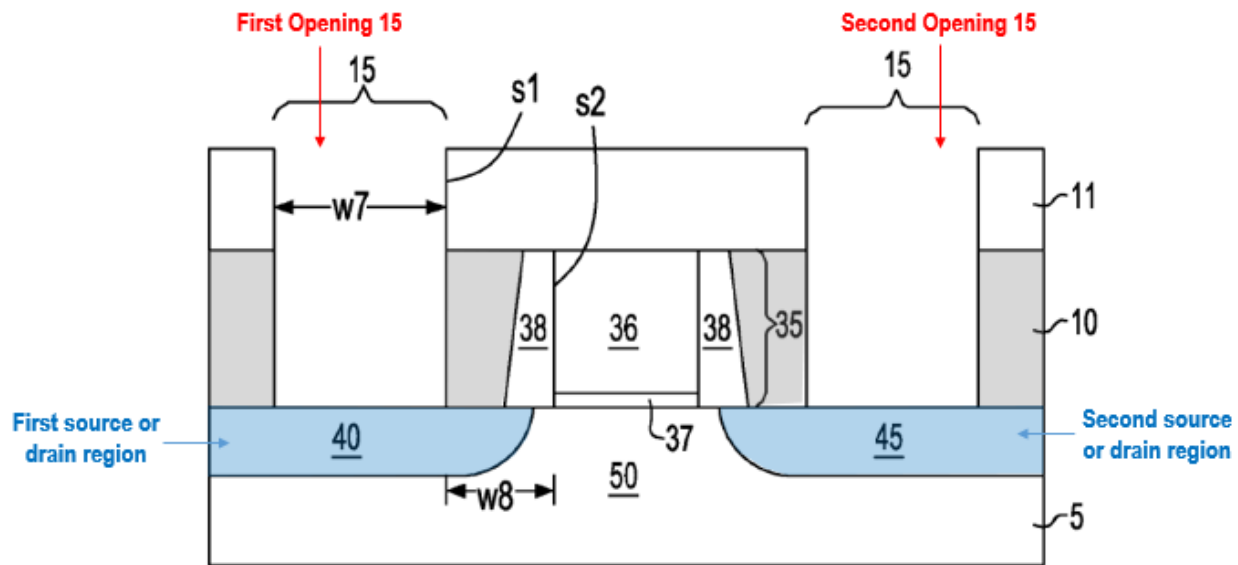
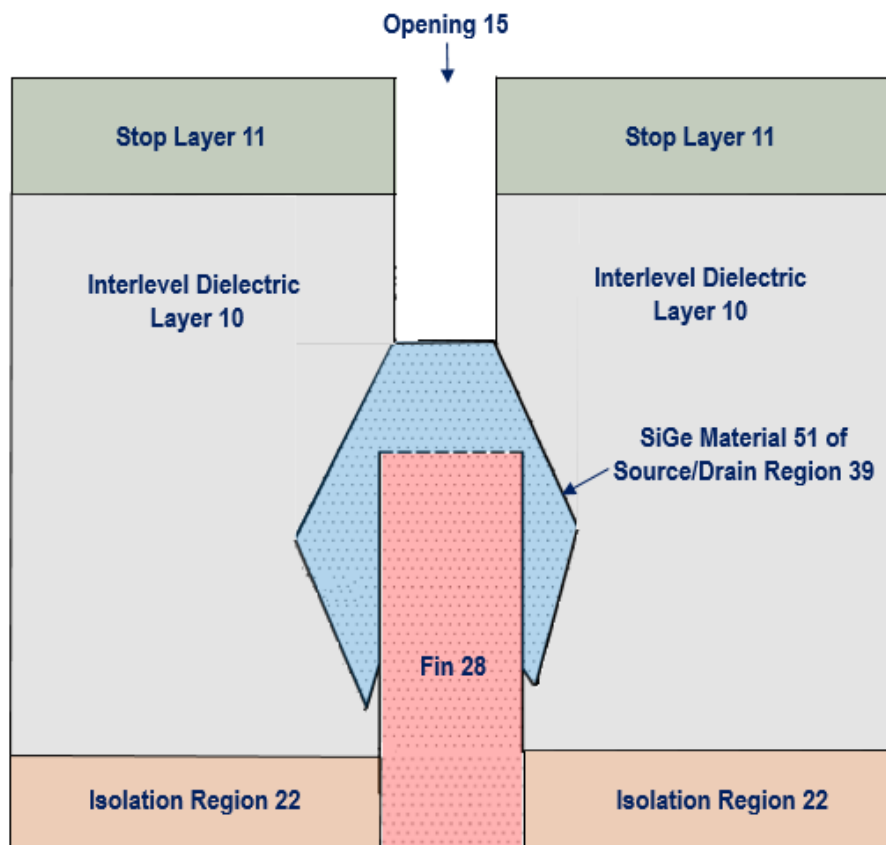


FIG. 2A

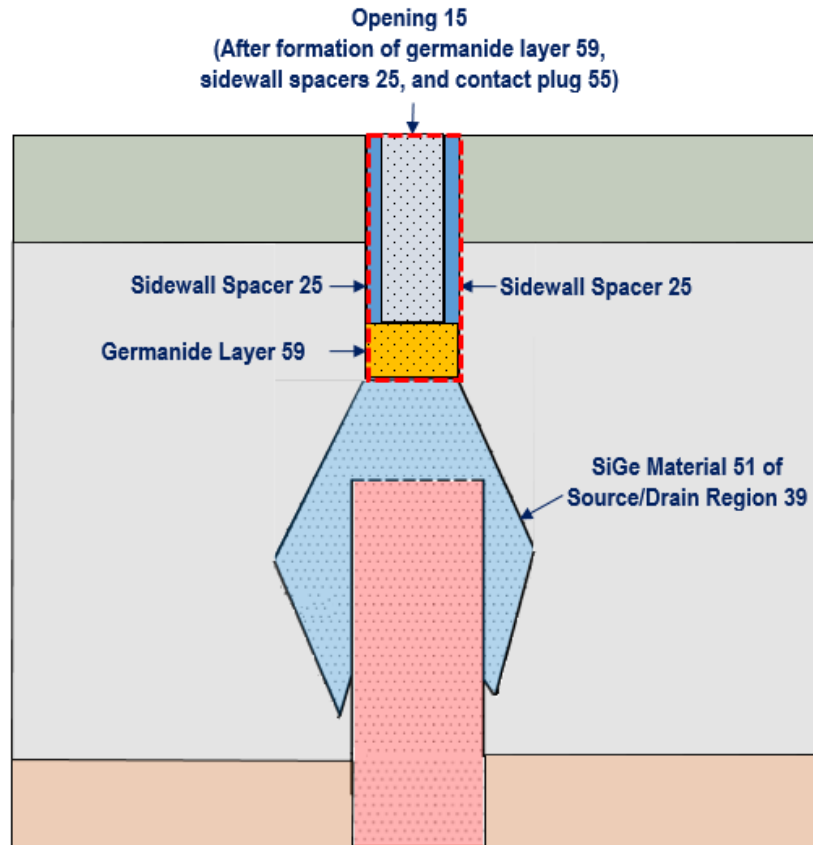
Yu, FIG. 2A (annotated)

Further, as discussed above in the overview of the combination, it would have been obvious to form interconnect structures like those described in Yu in the Tung-Yu-Simonelli FinFET, and the resulting combination would have provided and rendered obvious the recited first and second openings exposing only a portion of the respective first and second source or drain regions. SAMSUNG-1003, ¶110; *supra*, Section IV.A.4 (overview).



Tung-Yu-Simonelli Example (Before Contact Formation)⁸

⁸ Additionally or alternatively, the cavities in IDL 10 after forming sidewalls 25 within opening 15 would have rendered obvious the claimed first and second openings. SAMSUNG-1003, ¶110, FN29.



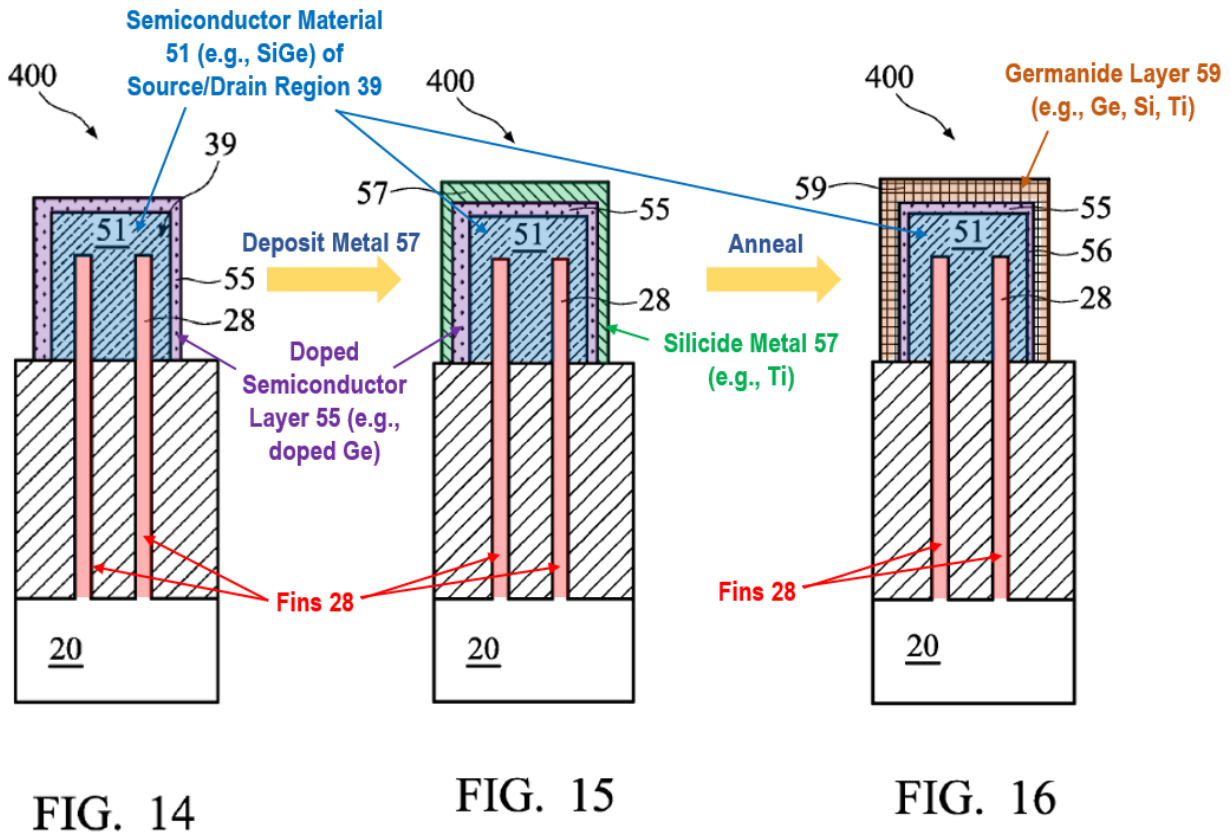
Tung-Yu-Simonelli Example (After Contact Formation)

Elements [1m], [1n]

The Tung-Yu-Simonelli combination would have rendered obvious [1m]-[1n], e.g., in view of the teachings of Tung and Yu. SAMSUNG-1003, ¶111; *see also id.*, ¶112-119.

To start, Tung describes a process for forming a germanide layer 59 that involves first forming a doped semiconductor layer 55 over a semiconductor material 51 of the source/drain regions 39, then depositing a metal 57 over the doped semiconductor layer 55, and finally annealing the metal 57 to form the germanide layer

59.⁹ SAMSUNG-1006, [0078]-[0081], FIGS. 14-16; *see also id.*, [0039]-[0045], FIGS. 4a-4e, FIG. 2a and 2d (depicting layer 59 formed over both source and drain regions 39).



Tung, FIGS. 14-16 (annotated)

FIGS. 14-16 depict the formation of germanide layer 59 on a device having multiple fins 28 spaced closely to each other such that a continuous semiconductor material 51 is grown across each fin 28. Tung also explains, however, that “the method described in FIG[S]. 13-16 is used in fabrication of a device with a single

⁹ *Supra*, Footnote 2.

fin” or fins spaced further from each other. *See* SAMSUNG-1006, [0082]. FIGS.

4b-4e depicting Tung’s process as applied to a single fin (or a fin spaced sufficiently far from others to prevent continuous SiGe and germanide formation):

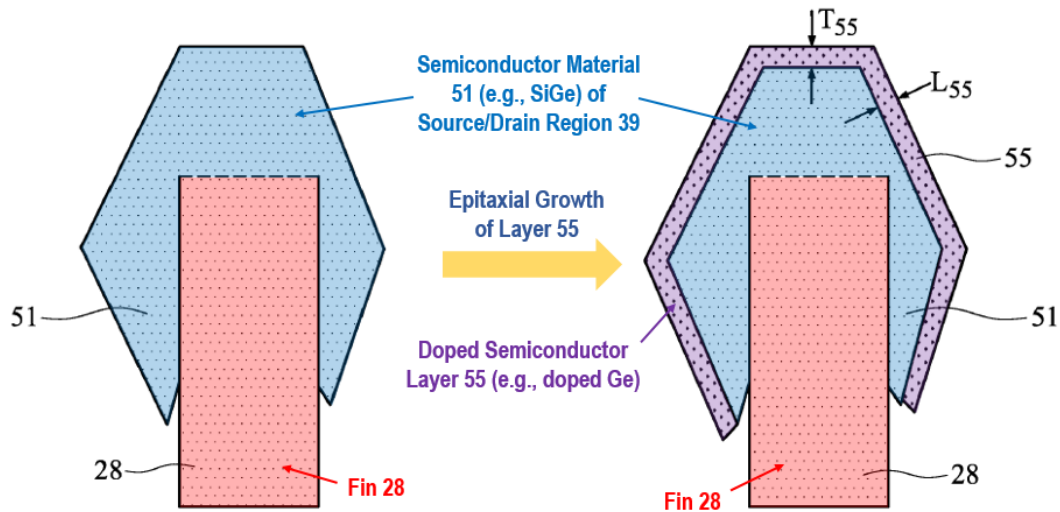
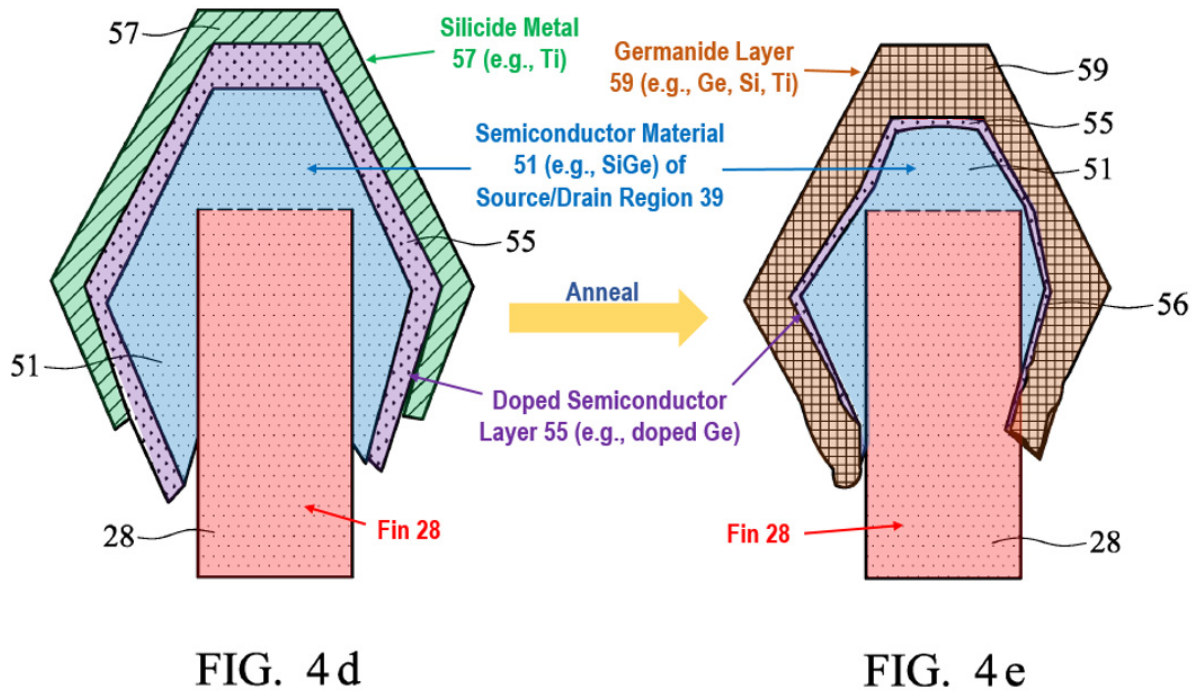


FIG. 4b

FIG. 4c



Tung, FIGS. 4b-4e (annotated)

As shown in FIG. 4e, germanide layer 59 is formed over SiGe material 51 of the source/drain region 39. And although Tung's figures show a portion of cap layer 55 that remains after annealing, Tung also describes embodiments in which "all of the doped semiconductor layer 55 [is] consumed" leaving the germanide layer 59 in direct contact with an outer surface of the SiGe material 51 of the source/drain regions 39. SAMSUNG-1006, [0045], [0081]; SAMSUNG-1003, ¶¶113-114.

According to Tung, layer 55 is a cap layer that can be formed from a germanium material such as doped Ge; semiconductor material 51 can be epitaxially

grown SiGe grown over source/drain regions 39; and metal 57 can include tita-

nium. SAMSUNG-1006, [0040], [0042], [0061], [0058], [0074], [0078], [0080].

In this context, it would have been obvious that the germanide layer 59 that results post-annealing would comprise titanium, silicon, and germanium. SAMSUNG-1003, ¶115. Indeed, titanium would be present in germanide layer 59 from the deposition of metal 57, germanium would be present at least from the germanium cap layer 55 (e.g., a doped Ge cap layer), and silicon would be present from the cap layer 55 (which can further include a small amount of silicon in addition to germanium) and/or from the underlying SiGe material 51 of the source/drain region 39. *Id.* A POSITA would have known that annealing metal with semiconductor material causes the constituent elements to mix and chemically react to form a metal compound (e.g., a germanide layer). *Id.*

More specifically, as to the presence of silicon in the germanide layers 59 of the Tung-Yu-Simonelli combination, this feature would have been obvious in several ways. SAMSUNG-1003, ¶116. In a first example, Tung teaches that the cap layer 55 can be formed from “doped Ge,” and further that germanide layer 59 is formed by annealing a metal (e.g., titanium) over cap layer 55 until the interface of germanide layer 59 extends by some distance into SiGe material 51 of the

source/drain region 39.¹⁰ SAMSUNG-1006, [0045] (“the silicide interface moves beyond the doped semiconductor layer 55 and into the semiconductor material 51”), [0081]; SAMSUNG-1003, ¶116. Consistent with these teachings, in the combination, the germanide layers 59 that result from annealing would include silicon originating from the SiGe material 51 of the source/drain regions 39 (and would further include germanium and titanium as described above). SAMSUNG-1006, [0058], [0078]; SAMSUNG-1003, ¶116.

In a second example, Tung teaches that “all of the doped semiconductor layer 55 may be consumed by the silicidation process” when annealed. SAMSUNG-1006, [0045]. When all of cap layer 55 is consumed without the interface of the germanide layer 59 extending into the SiGe material 51 of the source/drain regions themselves, the lower surface of germanide layer 59 would contact respective upper surfaces of the SiGe material 51 of the source/drain regions 39 exposed by the openings in the IDL 10. In this case, it would have been obvious that at

¹⁰ Patent Owner’s infringement charts in the co-pending ITC proceeding similarly appear to identify structures allegedly constituting germanide layers that extend at least partially beneath the top surfaces of or within the indicated source and drain regions. *See* SAMSUNG-1015, 17-20 (depicting alleged germanide layers extending into S/D regions).

least some silicon from near the upper surfaces of the SiGe material 51 in the source/drain regions 39 that contact the germanide layers 59 would migrate into the germanide layers 59 due to metal-silicon bonds being stronger and more stable than metal-germanium bonds. SAMSUNG-1003, ¶117. Here again, germanide layers 59 in the combination would include titanium, germanium, and silicon (even when cap layer 59 is formed from doped Ge). *Id.* EX1037, 2-3.

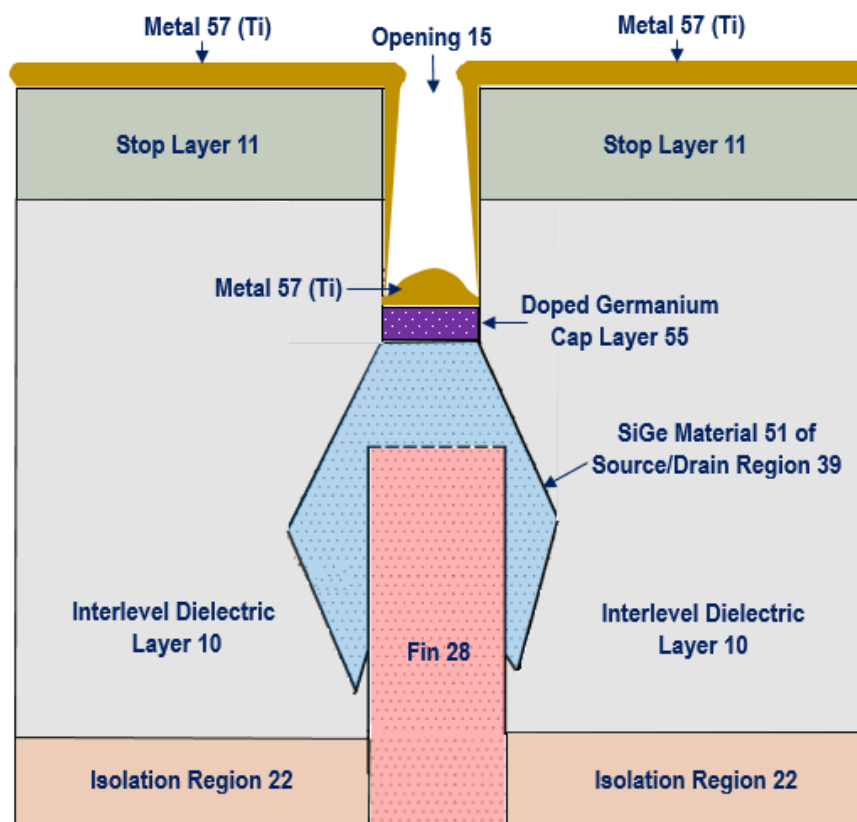
In a third example, it would have been obvious for the germanium cap layer 55 itself to include a small amount of silicon such that the germanide layers 59 formed by annealing titanium with the cap layer 55 would naturally include silicon along with titanium and germanium, regardless of whether cap layer 55 is entirely consumed by annealing. SAMSUNG-1003, ¶118. Indeed, Tung not only teaches that cap layer 55 can be “doped Ge,” but further teaches that cap layer 55 can include “doped SiGe” material. SAMSUNG-1006, [0058], [0078]. Given that both doped Ge and doped SiGe are identified in Tung as suitable materials for cap layer 55, it would have been obvious to select a material for cap layer 55 formed predominantly of Ge (e.g., in excess of 90% Ge) to make beneficial use of well-known intrinsically favorable properties of Ge (e.g., a lower band gap and Schottky barrier height that would tend to yield lower contact resistance to the source/drain regions) while still making beneficial use of Si (e.g., to lower the gap in Ge content and reduce dislocations at the interface of the resulting germanide layer 59 and the

SiGe material 51 of the source/drain regions 39). SAMSUNG-1003, ¶118. At minimum, it was known before the Critical Date that a wide range of concentrations of Ge in cap layers were suitable for forming contact structures to source/drain regions, and it would have been obvious to select a high concentration of Ge (e.g., in excess of 90%) to optimally reduce contact resistance and dislocations/defects in the contact structures to the source/drain regions. SAMSUNG-1003, ¶118.

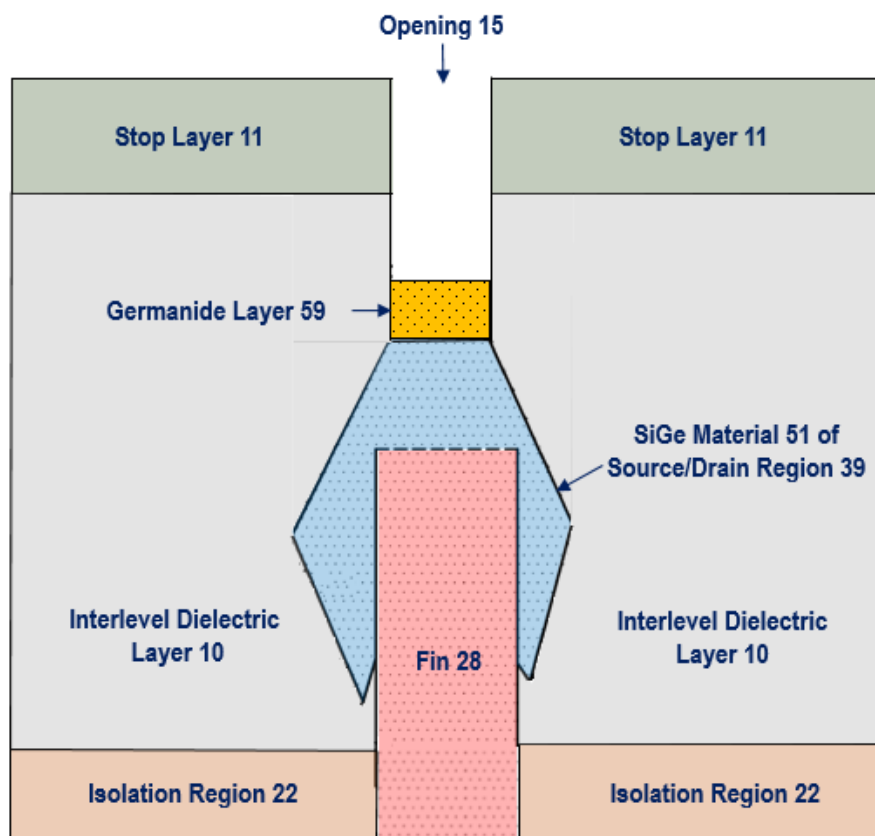
Further, as discussed above in the overview of the combination, it would have been obvious to form interconnect structures like those described in Yu with the FinFET of Tung as modified by Simonelli, and in the resulting combination, it would have been obvious to form the first and second germanide layers in the first and second openings of the dielectric layer and over the exposed portions of the first and second source or drain regions, respectively.¹¹ SAMSUNG-1003, ¶119;

¹¹ For purposes of this IPR, Petitioner interprets “**the portion** of the first source or drain region” and “**the portion** of the second source or drain region” as recited in [1m] and [1n] as referring to the portions of the first and second source or drain regions that are exposed by the openings in the dielectric layer as recited in [11]. *See* SAMSUNG-1001, FIGS. 5D-5F. Petitioner reserves all rights to raise invalidity defenses under §112 in other forums that are not available in an IPR.

supra, Section IV.A.4 (overview). For example, as shown in the post-anneal illustration below, and consistent with Yu's teachings, all or at least a portion of germanide layer 59 in the combination is in the opening 15 and remains above source/drain region 39. *See* SAMSUNG-1006, [0045]-[0081], FIGS. 4-6; *cf.* SAMSUNG-1001, 11:60-12:67, FIG. 5F; SAMSUNG-1003, ¶119.

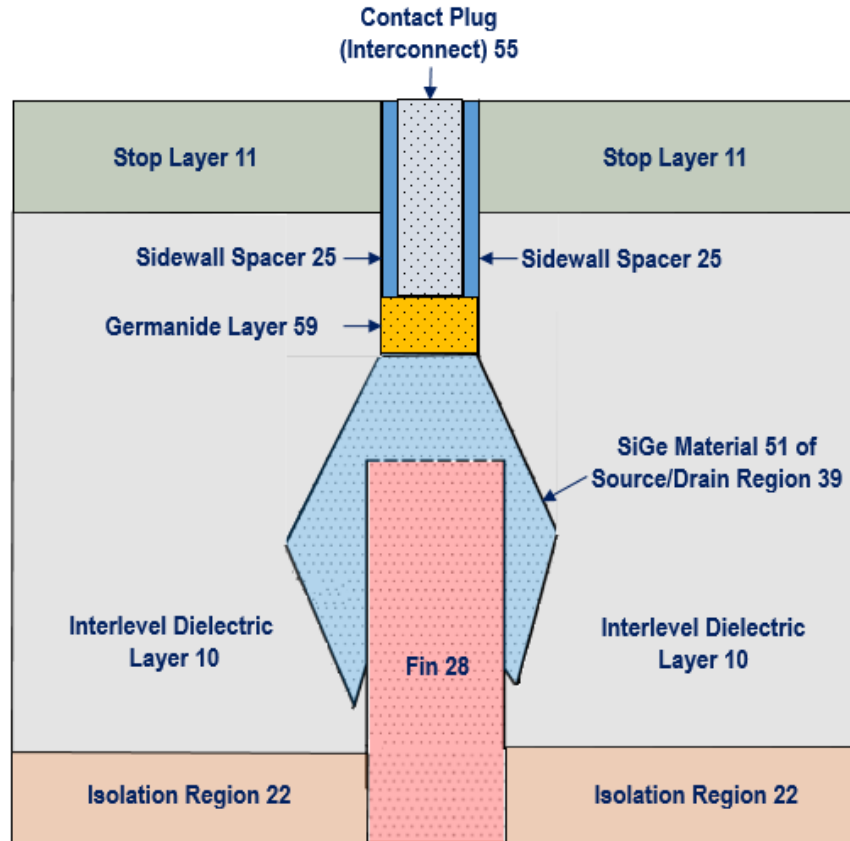


Tung-Yu-Simonelli Example (Pre-Anneal)



Tung-Yu-Simonelli (Post-Anneal and Removal of Unreacted Metal)¹²

¹² *Supra*, Footnotes 4-5.



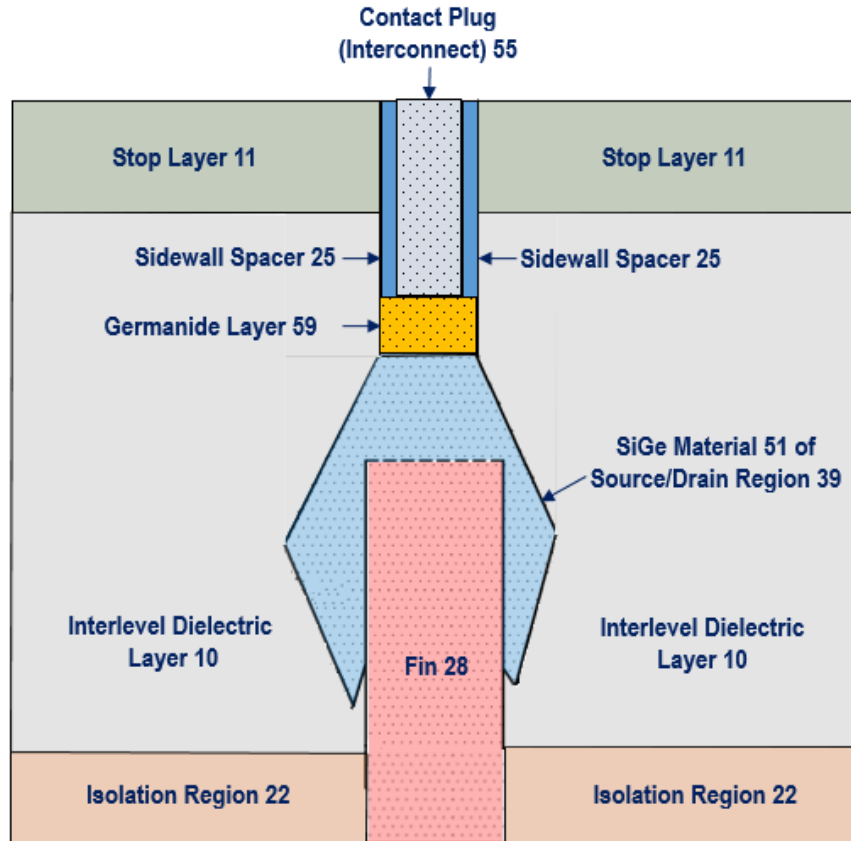
Tung-Yu-Simonelli Example (Post-Formation of Contact Plug 55)

Elements [1o], [1p]

The Tung-Yu-Simonelli combination would have rendered obvious [1o]-[1p], e.g., in view of Yu's disclosure of first and second contact plugs (interconnects) 55 formed respectively in the first and second openings 15 and on the first and second semiconductor alloy contact layers (e.g., germanide layers) 20. SAM-SUNG-1009, [0032] ("A [sic] interconnect 55 is present in the openings 15 to the source region 40 and the drain region 45 through the interval dielectric layer 10 ..."), [0035] ("electrical contact between the interconnect 55 and the source region 40 and the drain region 45 of the semiconductor substrate 5 is provided by a metal

This diagram shows a cross-sectional view of a semiconductor device with two symmetrical contact regions. The central channel region is labeled 36, flanked by gate regions 38. The substrate is 50. The top layer is 10, and the bottom layer is 5. The first contact region on the left includes a first source or drain region 40, a first semiconductor alloy contact layer 20, and a first contact plug (interconnect) 55. The second contact region on the right includes a second source or drain region 45, a second semiconductor alloy contact layer 20, and a second contact plug (interconnect) 55. Various dimensions are indicated: w_1 and w_2 for the contact plug width, w_3 and w_4 for the contact layer width, w_5 and w_6 for the alloy layer width, and H_1 for the height of the contact layer. Labels s1 and s2 indicate specific points or surfaces. The first contact plug 55 is shown with a cross-hatched pattern, and the second contact plug 55 is shown with a diagonal line pattern.

Further, as discussed above in the overview of the combination, it would have been obvious to form interconnect structures like those described in Yu in the Tung-Yu-Simonelli FinFET, and the resulting combination would have provided and rendered obvious first and second contact plugs like Yu's interconnects 55 respectively formed in the first and second openings 15 and on the first and second germanide layers 59. SAMSUNG-1003, ¶121; *see also id.*, ¶¶120-121; *supra*, Section IV.A.4 (overview).



Tung-Yu-Simonelli Example

Claim [5]

The Tung-Yu-Simonelli combination would have rendered obvious [5], e.g., in view of Tung's disclosure of a fin 28 that protrudes through an isolation region 22 of the transistor. SAMSUNG-1003, ¶¶122-124. Further, as described in Tung, a portion of the gate electrode 42 and portions of the first and second dielectric spacers are positioned over isolation region 22. SAMSUNG-1006, [0023]-[0024], [0049]-[0051], FIGS. 2a, 7c, 13-16. For example, FIG. 7c shows fins 28 protruding through isolation region 22 and a portion of the gate electrode 42 positioned over isolation region 22:

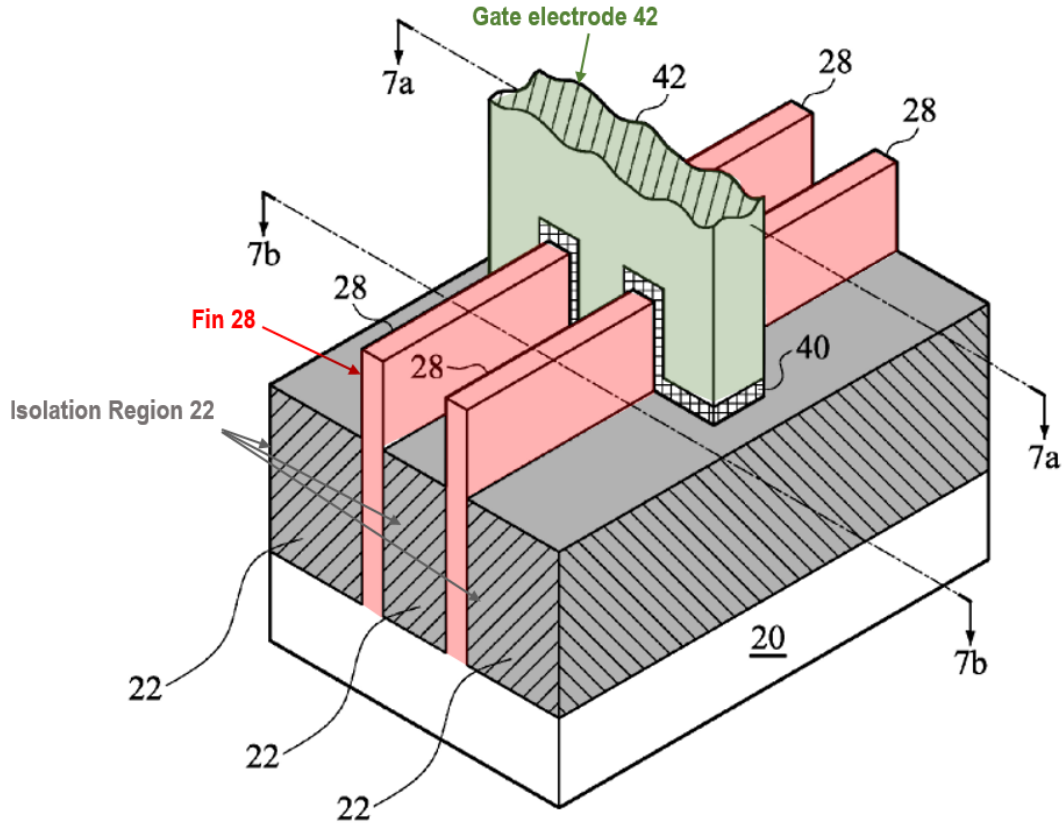


FIG. 7c

Tung, FIG. 7c (annotated)

In the view depicted in FIG. 7c, spacers 36 have not yet been formed, but Tung explains that “[t]he fin 28 ... may be disposed under the spacers 36” and that “[s]idewalls of the gate electrode 42 are isolated by spacers 36.” *Id.*, [0023], [0036]. At least a portion of the spacers 36 are thus formed over the isolation region 22, as shown in FIG. 2A:

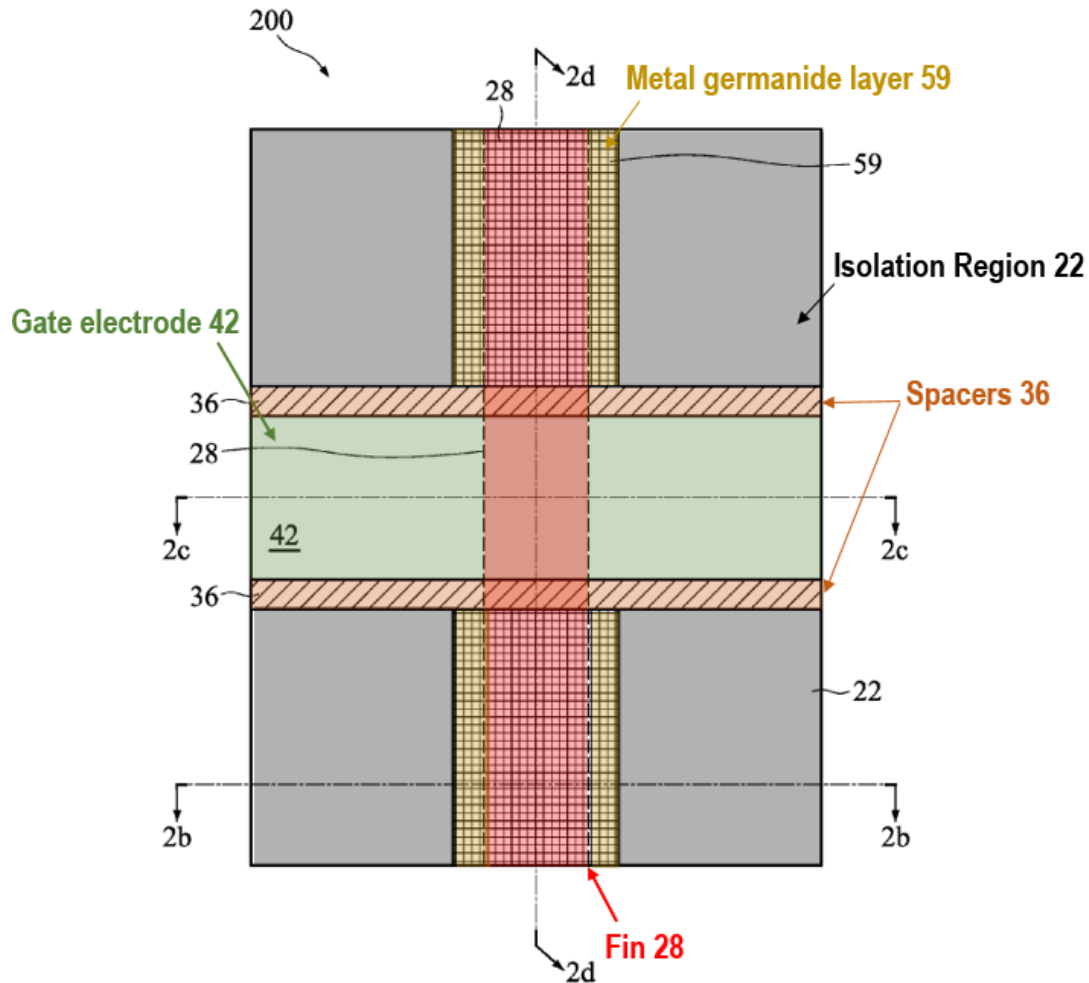
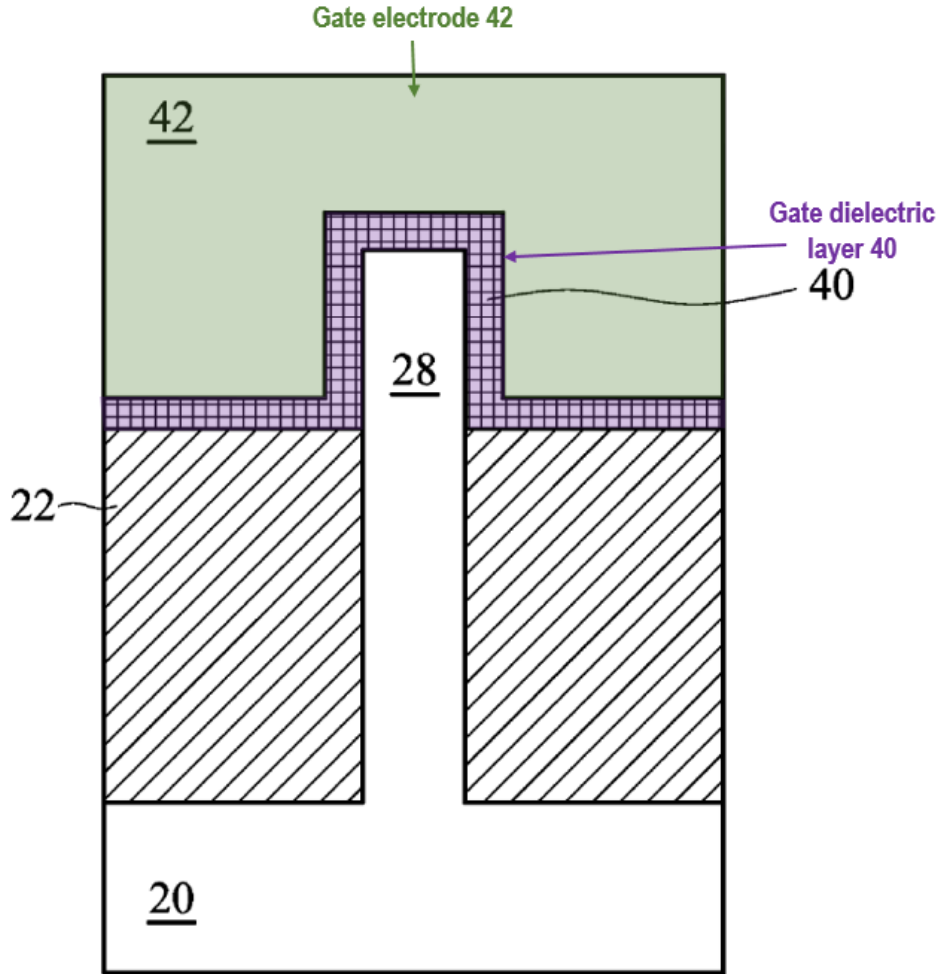


FIG. 2a

Tung, FIG. 2A (annotated)

Claim [6]

The Tung-Yu-Simonelli combination would have rendered obvious [6], e.g., in view of Tung’s disclosure of a gate electrode 42 on gate dielectric layer 40. SAMSUNG-1006, [0025] (“gate electrode layer 42 is disposed over a gate dielectric 40”), [0053]-[0055], [0070], FIGS. 2c-2d, 7c; SAMSUNG-1003, ¶126; *see also id.*, ¶¶125 and 127.



Tung, FIG. 2c (annotated)

Tung further discloses and would have rendered obvious that gate dielectric layer 40 comprises a high-k dielectric material and gate electrode 42 comprises a metal layer. SAMSUNG-1006, [0054] (“gate dielectric 40 may include commonly used dielectric materials ...”); [0055] (“gate electrode 42 may be formed of [] commonly used conductive materials, including metals ...”); SAMSUNG-1003, ¶127.

Claim [7]

The Tung-Yu-Simonelli combination would have rendered obvious [7], e.g.,

in view of Tung's disclosure of facets of semiconductor material 51 (e.g., SiGe)

epitaxially grown to form two or more facets at each of source/drain regions 39.

SAMSUNG-1006, [0074]-[0075]; *see also id.*, [0040], [0058]; SAMSUNG-1003,

¶¶128-130.

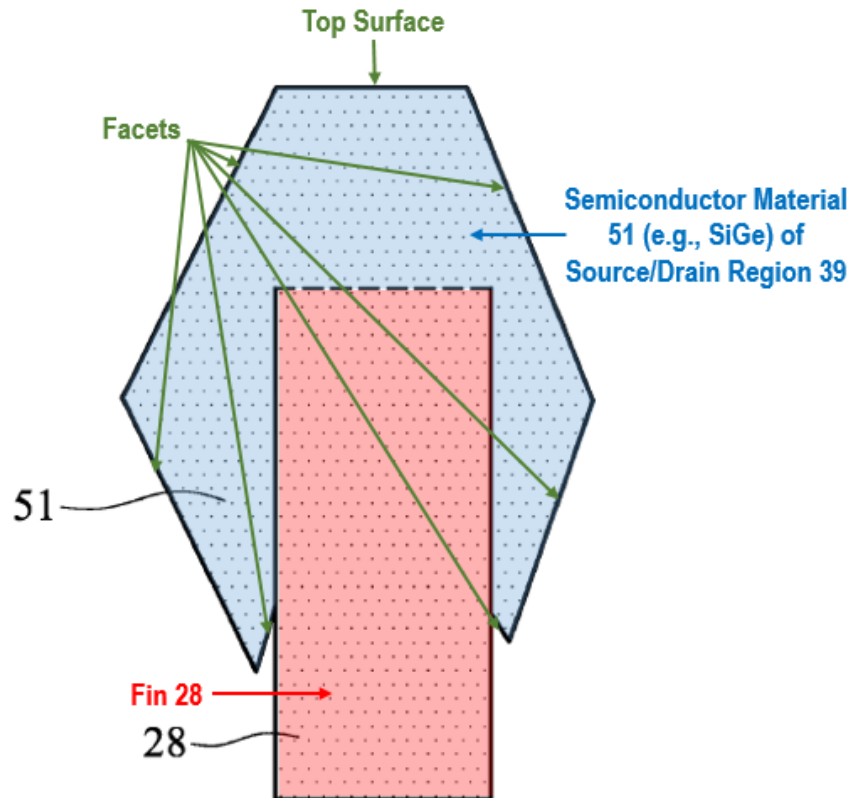


FIG. 4b

Tung, FIG. 4b (annotated)

Element [8pre]

Supra, [1pre]. SAMSUNG-1003, ¶¶131-133.

Element [8a]

Supra, [1a]. SAMSUNG-1003, ¶134. The Tung-Yu-Simonelli combination

would have rendered obvious [8a], e.g., in view of Tung's disclosure of a fin 28 in the channel region comprising silicon. *Supra*, [1a]. For example, just as the specification of the '281 Patent identifies structure 660 alternately as a "body" or a "fin," the same structures from the Tung-Yu-Simonelli combination that would have rendered obvious a "fin" also would have rendered obvious the recited "body" in Claim 8. *Cf.* SAMSUNG-1001, 13:33-42, FIG. 6; SAMSUNG-1003, ¶134.

Elements [8b]-[8p]

Supra, [1b]-[1p]. SAMSUNG-1003, ¶¶134-135.

B. [GROUND 1B] – Obviousness based on Yu in view of Tung and Simonelli (Claims 1, 5-8)

In Ground 1A, it was shown that a combination based on Tung as modified by Yu and Simonelli would have rendered obvious claims 1 and 5-8 of the '281 Patent. *Supra*, Section IV.A.

Here (Ground 1B), obviousness of the asserted claims is demonstrated where a POSITA starts with Yu as the primary reference and integrates obvious modifications to Yu based on Tung and Simonelli. In particular, and as described in further detail below, it would have been obvious (1) to form Yu's metal semiconductor alloy layer 20 as a germanide layer from a doped germanium cap as taught in Tung, (2) to apply Tung's FinFET to Yu's interconnect structures, and (3) to implement grading of the germanium content in the source and drain regions of the FinFET as

taught in Simonelli. SAMSUNG-1003, ¶¶136-137. Notably, the device that would predictably result from these modifications in the Yu-Tung-Simonelli combination provides the same structures as the device in the Tung-Yu-Simonelli combination from Ground 1A, and would have rendered each element of claims 1 and 5-8 obvious for the reasons described above with respect to Ground 1A. SAMSUNG-1003, ¶137; *see also id.*, ¶¶138-152.

Obviousness of Forming Yu's Metallized Semiconductor Alloy Layer 20 as a Germanide Layer Formed from a Doped Germanium Cap Based on Tung

As described above, Yu discloses techniques for forming interconnect structures (e.g., interlevel dielectric layer (“IDL”) 10, openings 15, interconnect 55 over a metallized semiconductor alloy layer 20). *Supra*, Section IV.A.2. In FIGS. 1-6, Yu shows the formation of semiconductor alloy contacts 20 in openings 15 of an IDL 10, the openings 15 surrounded by dielectric sidewall spacers 25 that have contact plugs (interconnects) 55 disposed within openings 15. SAMSUNG-1009, [0030]-[0038], FIGS. 1-6; SAMSUNG-1003, ¶138.

Tung describes techniques for forming an analogous metal germanide layer 59¹³ by annealing a metal over a doped germanium cap layer 55. *Supra*, Section

¹³ *Supra*, Footnote 2.

IV.A.1. Tung's process involves the growth of cap layer 55 (e.g., doped Ge¹⁴) over a surface of a SiGe material 51 of the source and drain regions 39, depositing a metal 57 over the cap layer 55, and annealing the metal 57 with the cap layer 55 to form a germanide layer 59 over the source and drain regions 39. SAMSUNG-1006, [0078]-[0082], [0039]-[0045], FIGS. 4, 13-16. Titanium is one of a multitude of metals 57 that are suitable for depositing over the cap layer 55, as acknowledged by Tung and consistent with Yu's teachings. *Id.*, [0042]; SAMSUNG-1009, [0074]; SAMSUNG-1003, ¶139.

A POSITA would have found it obvious to implement Yu's metal contact layer 20 as a germanide layer in accordance with the teachings of Tung, e.g., by annealing a metal such as titanium with a doped germanium cap layer 55 formed over a surface of the source/drain regions exposed by openings 15 as taught in Yu. SAMSUNG-1003, ¶140.

¹⁴ A doped SiGe cap layer 55 with a high concentration of germanium (e.g., in excess of 90%) also would have been suitable and obvious to a POSITA before the Critical Date. *Supra*, Elements, [1m]-[1n]; SAMSUNG-1003, ¶140, FN 37.

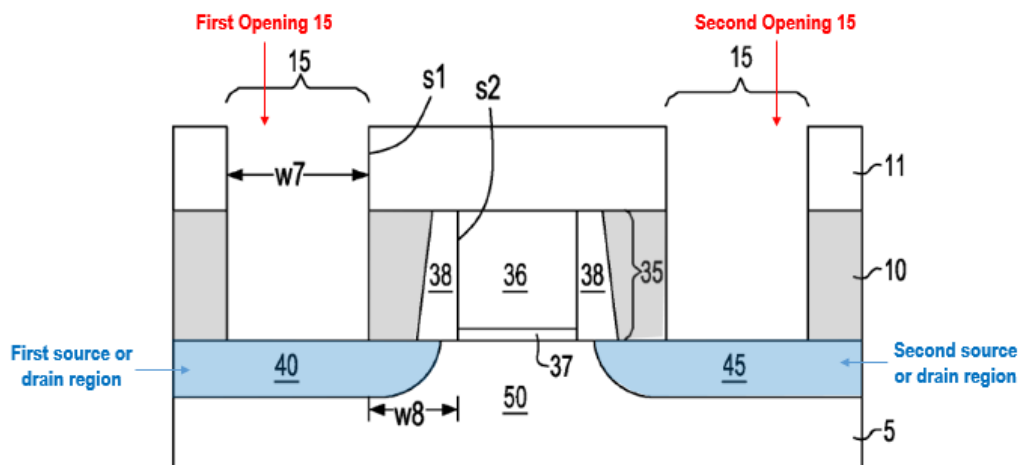


FIG. 2A

Yu, FIG. 2A (annotated)

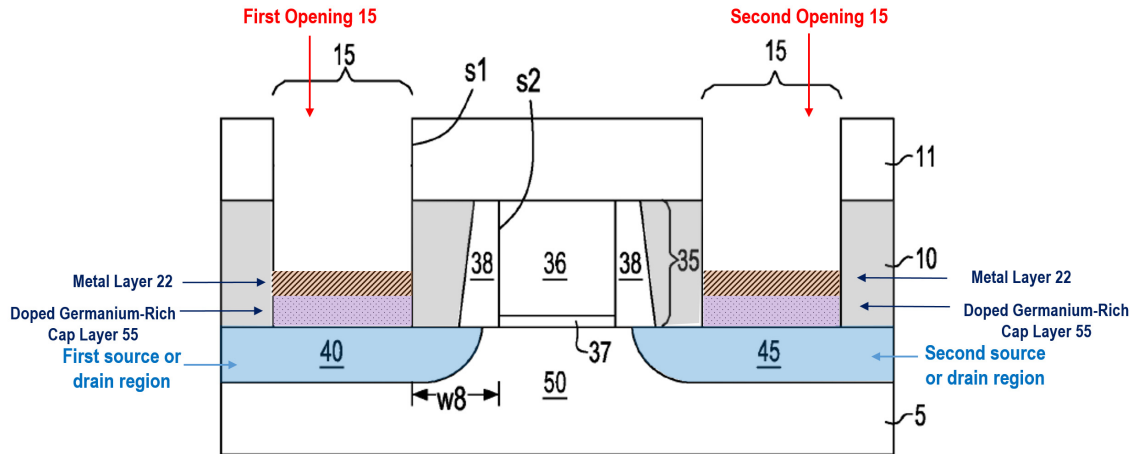


FIG. 2A

Yu-Tung (Modified to Show Ge Cap Layer 55 and Metal 22 Before Annealing)

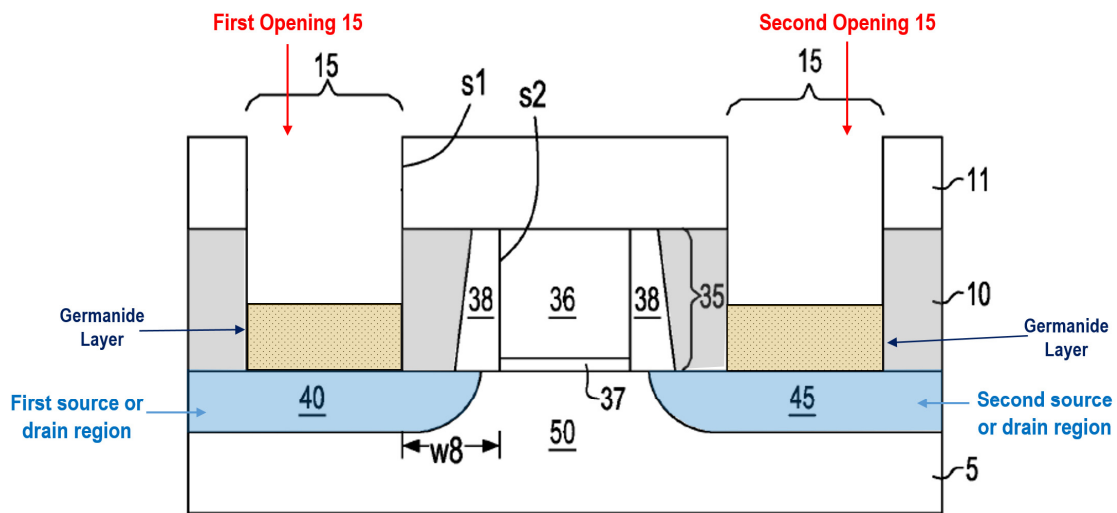


FIG. 2A

Yu-Tung (Modified to Show Ge Cap Layer 55 and Metal 22 After Annealing)

Multiple reasons would have led a POSITA to apply Tung's teachings to Yu (and to sustain these teachings in the Yu-Tung-Simonelli combination) in the manner described above. SAMSUNG-1003, ¶142. For example, a POSITA would

have sought to form Yu's metal semiconductor alloy contact layer ("MSACL") 20 as a germanide layer using a germanium cap layer so as to obtain the predictable benefits of such a cap layer as taught in Tung. SAMSUNG-1003, ¶142. These benefits would have predictably included reducing the Schottky barrier height and lowering contact resistance between the resulting germanide layer and the source and drain regions. SAMSUNG-1006, [0034]; *see also id.*, [0005]-[0006], [0032]; SAMSUNG-1003, ¶¶140-142.

According to Tung, "the low Schottky barrier height at the source of the transistor and the ultra-shallow junction depths ... achievable with metal silicides significantly improve[s] short channel effects of the transistor." SAMSUNG-1006, [0031]. A POSITA would have known that various properties of germanium render it favorable to silicon in certain respects, e.g., including germanium's higher carrier mobility and lower resistivity; accordingly, a germanium cap layer would have been obvious and beneficial to use in forming metal compound layers over the source and drain regions as germanide layers. SAMSUNG-1003, ¶143. The use of such a germanium cap layer would have allowed the device in the Yu-Tung-Simonelli combination to more fully obtain the benefits of Ge's intrinsically favorable properties as a result of its high content in the cap layer, especially when the Ge content in a SiGe material of the source/drain regions themselves is significantly lower than the Ge content in the cap layer. SAMSUNG-1003, ¶143.

Further, based on Tung, it would have been obvious to use a cap layer in forming Yu's metal so as to increase the uniformity of dopants at or near an interface to the metal from which the germanide layer is formed, as well as to reduce "residual defects that may result in poor silicide formation or result in leakage currents" that can otherwise result when implanting dopants for contact formation directly into the source/drain regions rather than in a germanium cap layer. SAMSUNG-1006, [0005], [0020]; SAMSUNG-1003, ¶144.

Moreover, as described further below, it would have been obvious to implement the Yu-Tung-Simonelli combination with a FinFET. SAMSUNG-1003, ¶145. Tung explains that its techniques are particularly suitable for FinFETs since traditional methods of dopant implantation to facilitate contact formation were not as readily performed in FinFETs, and a POSITA thus would have desired to use Tung's techniques for germanide formation in the context of a FinFET. SAMSUNG-1006, [0005]-[0006]; SAMSUNG-1003, ¶145.

The use of a doped germanium cap in the device resulting from the combination also would have amounted to an obvious use of a known technique, as taught by Tung, to improve a similar device like that taught in Yu to yield no more than predictable results. SAMSUNG-1003, ¶146; *KSR*, 550 U.S. at 417.

A POSITA would have had a reasonable expectation of success implementing the combination in light of the similar semiconductor devices described in Yu

and Tung. SAMSUNG-1003, ¶147. Notably, Yu and Tung each describe techniques for forming metallized semiconductor layers at the source and drain regions by annealing at least one metal with a semiconductor material. Moreover, Tung expressly teaches that the cap layer can be formed over an epitaxially grown SiGe source/drain region (e.g., SiGe material 51 of source/drain regions 39), which is analogous to Yu's source region 40 and drain region 45 and the SiGe material 51 in the Yu-Tung-Simonelli combination. SAMSUNG-1006, [0040], [0058], [0074], [0078]. Tung also expressly confirms that a POSITA would have known how to apply its techniques across a range of devices and integrated circuit structures. SAMSUNG-1006, [0019]-[0020], [0083]-[0084]; SAMSUNG-1003, ¶147.

Obviousness of Applying Tung's FinFET in Combination with Yu's Interconnect Structures

Yu teaches that its techniques for interconnect structures can be applied to a range of semiconductor devices, including FinFETs. SAMSUNG-1009, [0020] ("Although the semiconductor device 100 that is depicted in FIG. 1 is a field effect transistor (FET), the metal semiconductor alloy contacts 20 of the present disclosure are suitable for . . . **finFET** semiconductor devices."). Although Yu does not describe its FinFET in detail, non-planar semiconductor devices, including FinFETs, were well-known before the Critical Date, and it would have been obvious for a POSITA to turn to Tung for details of a known FinFET design to implement

in combination with Yu's interconnect structures. SAMSUNG-1003, ¶148.

Multiple reasons would have led a POSITA to modify Yu to incorporate a FinFET like that described in Tung. SAMSUNG-1003, ¶149. First, for instance, FinFETs were associated with a range of well-known performance benefits relative to traditional FETs (e.g., planar FETs), and a POSITA would have been motivated to implement a FinFET in the combination to obtain the widely recognized benefits of FinFET designs such as reduced size, increased speed, lower leakage currents, and improved gate control, *inter alia*. SAMSUNG-1006, [0004]; SAMSUNG-1003, ¶149.

Second, Yu expressly contemplates application of its techniques to FinFETs, and hence the integration of Tung's FinFET to the combination would have furthered Yu's original goal of realizing a FinFET-based implementation. SAMSUNG-1009, [0004]; SAMSUNG-1003, ¶150.

Third, the combination amounts to an obvious application of known techniques based on Tung, applied to a known device, as described in Yu (which teaches FinFETs), which was ready for improvements that would have yielded predictable results. *KSR*, 550 U.S. at 417. Yu does not impose any restrictions on the types of transistors or semiconductors that must be used in its semiconductor device, and a POSITA would have had a reasonable expectation of success implementing the combination, as FinFET design was well known by the Critical Date.

SAMSUNG-1003, ¶151.

**Obviousness of Grading Germanium in the Source and Drain Regions
Based on Simonelli**

As discussed above, Simonelli further teaches grading germanium content in the source and drain regions of a non-planar FET. SAMSUNG-1008, [0051], [0053]-[0058], FIGS. 14-15; *supra*, Section IV.A.3. It would have been obvious to further modify the FinFET in the Yu-Tung-Simonelli combination to include graded germanium content in the source and drain regions as taught in Simonelli, and a POSITA would have been motivated to do so, and would have had a reasonable expectation of success, for substantially the same reasons to those described above with respect to Ground 1A. *Supra*, Ground 1A (Section IV.A.4 combination overview); SAMSUNG-1003, ¶152.

C. [GROUND 2A] Obviousness based on Conway, Tung, Yu, and Simonelli (Claims 12-20)

1. Overview of Conway

Conway describes a computing device having a range of components implemented as integrated circuit structures “mounted on a common motherboard” SAMSUNG-1010, [0148], [0153], [0162]; *generally id.*, [0147]-[0165], FIGS. 5-8; SAMSUNG-1003, ¶¶57-58.

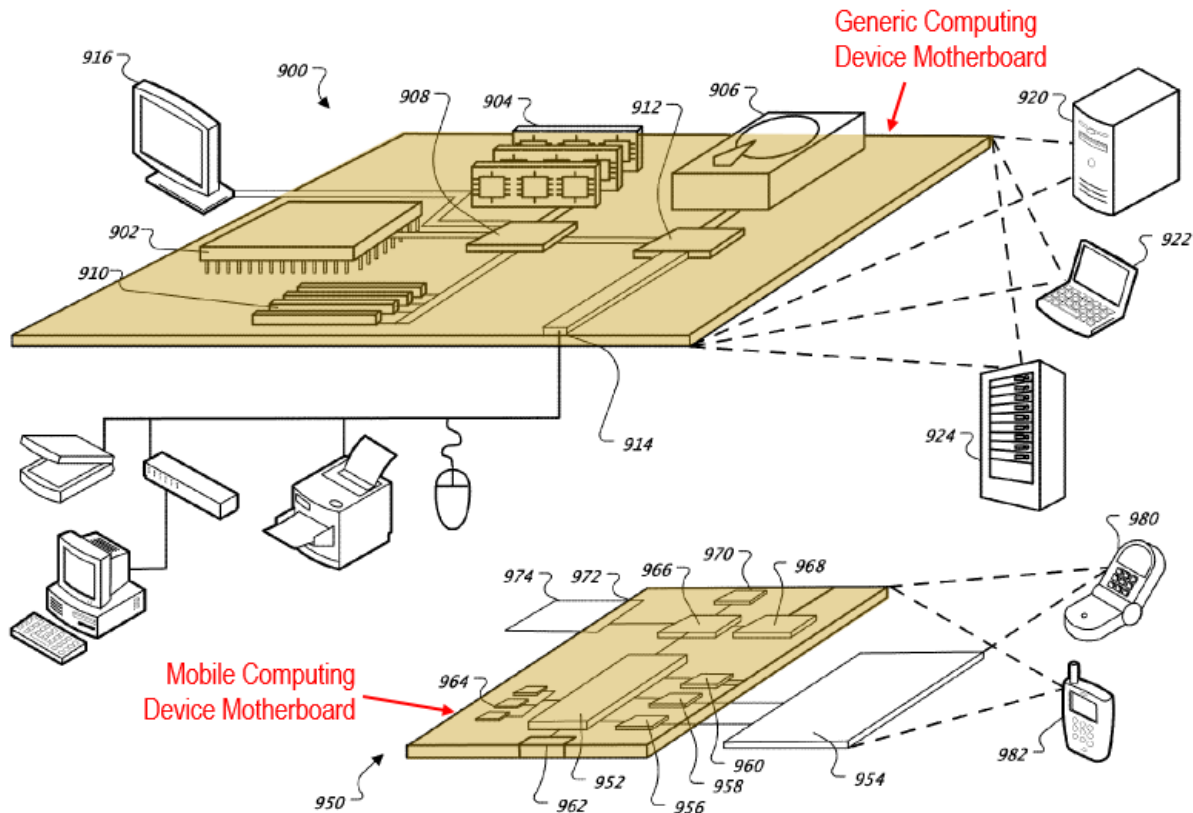


FIG. 9

SAMSUNG-1010, FIG. 9 (annotated)

2. Obviousness Analysis

A POSITA would have found it obvious and would have been motivated by multiple reasons to use a FinFET like that of the Tung-Yu-Simonelli combination of Ground 1A to implement one or more of the electronic components in Conway's computing device. SAMSUNG-1003, ¶153; *see also id.*, ¶¶154-157.

First, Conway indicates that integrated circuit structures can form the building blocks of Conway's device components, but provides little detail about these structures. It would have been obvious to look to other sources, such as Tung, Yu,

and Simonelli, for details of known and predictable transistor designs. SAMSUNG-1003, ¶154.

Second, a POSITA would have sought to exploit well-known advantages of non-planar FinFETs like those described in Tung (and similarly provided in the Tung-Yu-Simonelli combination), including improved channel control, lower leakage currents, smaller size, and increased switching speeds relative to many conventional planar devices. SAMSUNG-1003, ¶155.

Third, the combination would have amounted to a merely obvious application of the Tung-Yu-Simonelli techniques to Conway's device, which was ripe for improvement, and would have yielded no more than predictable results. *KSR*, 550 U.S. at 417. A POSITA would have had a reasonable expectation of success implementing the combination, as it was well known to use the type of integrated circuit in the Tung-Yu-Simonelli combination for the integrated circuit structures described in Conway. SAMSUNG-1003, ¶156.

The Conway-Tung-Yu-Simonelli combination would have rendered obvious each of claims 12-20. SAMSUNG-1003, ¶157.

Element [12pre]

To the extent the preamble is a limitation, the Conway-Tung-Yu-Simonelli combination would have rendered [12pre] obvious, e.g., in view of Conway's dis-

closure of various “generic” mobile and non-mobile computing devices. SAMSUNG-1010, FIG. 9 and [0147]-[0165]; *see also id.*, FIGS. 5-8 and associated text; SAMSUNG-1003, ¶160; *see also id.*, ¶¶158-159.

Element [12a]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [12a], e.g., in view of Conway’s disclosure of “a common motherboard” for mounting various components of a computing device. SAMSUNG-1010, [0148], [0153], FIG. 9; *supra*, Section IV.C.1; SAMSUNG-1003, ¶161.

Element [12b]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [12b]. SAMSUNG-1003, ¶162. Conway teaches that “the systems and techniques described here can be realized in digital electronic circuitry, integrated circuitry, specially designed ASICs (application specific integrated circuits), computer hardware, firmware, software, and/or combinations thereof.” SAMSUNG-1010, [0162]. Conway also describes various components coupled to a “common motherboard.” SAMSUNG-1010, [0148], [0153], FIG. 9; *see also id.*, FIGS. 5-8 and associated text. Further, in the combination, and as described above in the overview of the combination (Section IV.C.2), it would have been obvious to utilize the Tung-Yu-Simonelli integrated circuit structure of Ground 1 in one or more of Conway’s components coupled to the motherboard. SAMSUNG-1003, ¶162.

Elements [12c]-[12r]

Supra, Ground 1 at [1a]-[1p]; SAMSUNG-1003, ¶¶162-163.

Claim [13]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [13], e.g., in view of Conway’s disclosure of a memory coupled to the board. SAMSUNG-1010, [0148]-[0151] and FIG. 9 (memories 904, 906), [0153]-[0157] and FIG. 9 (memories 964, 974), [0123]-[0125] and FIG. 6, [0011] (“memory storing code”), [0078] (“memory devices”), [0148] and [0153] (“mounted on a common motherboard”); SAMSUNG-1003, ¶¶164-165.

Claim [14]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [14], e.g., in view of Conway’s disclosure of a “communication interface” such as interface 966 that includes “digital signal processing circuitry” for implementing various communication capabilities on the device. SAMSUNG-1005, [0152]-[0153], [0158], FIG. 9; *see also id.*, [0148] (“mounted on a common motherboard”), FIG. 6 (607); SAMSUNG-1003, ¶¶166-167. A POSITA would have understood and it would have been obvious to implement the communications circuitry on a communication chip. SAMSUNG-1003, ¶167.

Claim [15]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious

[15], e.g., in view of Conway's disclosure of a camera coupled to the board. SAMSUNG-1010, [0113] ("device 500 includes ... a camera 507"), [0118] ("camera"), [0121] ("camera 507"), [0123] ("a camera interface 608 that provides a communication interface and processing functions for capturing digital images from the camera 507"), FIG. 6; *see also id.*, [0148] ("common motherboard"), [0153], FIG. 9; SAMSUNG-1003, ¶¶168-169.

Claim [16]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [16], e.g., in view of Conway's teachings of a battery coupled to the board. SAMSUNG-1003, ¶¶170-171. For example, Conway describes that the computing device can include a "battery life indicator 516 that indicates a measurement of the remaining battery life," which a POSITA would have understood or found obvious to mean that the device includes a battery. SAMSUNG-1010, [0114], FIG. 5; SAMSUNG-1003, ¶171. Conway also discloses "a power source 619 that provides an appropriate alternating current (AC) or direct current (DC) to power components." SAMSUNG-1010, [0123], FIG. 6; SAMSUNG-1003, ¶171. In a mobile device, and other devices, it would have been obvious that the power source 619 would include a battery coupled to the board, e.g., to deliver power to components on the board. SAMSUNG-1003, ¶171; SAMSUNG-1010, [0148] ("common motherboard"), [0153], FIG. 9.

Claim [17]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [17], e.g., in view of Conway's teachings of an antenna coupled to the board. SAMSUNG-1010, [0113]-[0114], [0119], [0120], [0123], FIGS. 5-6 (antenna 505); *see also id.*, [0148] ("common motherboard"), [0153], FIG. 9; SAMSUNG-1003, ¶¶172-173.

Claim [18]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [18], e.g., in view of Conway's teachings of integrated circuit dies packaged for mounting on a motherboard. Conway describes "integrated circuitry" components, and FIG. 9 shows various integrated circuit chips mounted on a motherboard. SAMSUNG-1010, [0148], [0162], FIG. 9; SAMSUNG-1003, ¶¶174-175. A POSITA would have understood and it would have been obvious that the mounted components include a packaged integrated circuit die. SAMSUNG-1003, ¶175.

Claim [19]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [19], e.g., in view of Conway's teachings of computing device components such as a central processor 902, processor 952, or various other processing components. SAMSUNG-1010, [0148] ("device 900 includes a processor 902"), [0153] ("device 950 includes a processor 952"), FIG. 9; *see also id.*, [0162]-[0163], [0168] ("digital signal processing circuitry"); *supra*, [14]. It would have been obvious to

implement Conway's electronic components using a FinFET like that described in the Tung-Yu-Simonelli combination of Ground 1A. *Supra*, Section IV.C.2; SAMSUNG-1003, ¶¶176-177.

Claim [20]

The Conway-Tung-Yu-Simonelli combination would have rendered obvious [20], e.g., in view of Conway's disclosure of the computing device being a mobile phone, a laptop, a desktop computer, or a server. SAMSUNG-1010, [0147], FIG. 9; SAMSUNG-1003, ¶¶178-179.

D. [GROUND 2B] – Obviousness based on Conway, Yu, Tung, and Simonelli (Claims 12-20)

A POSITA would have found it obvious to use a FinFET like that of the Yu-Tung-Simonelli combination of Ground 1B to implement one or more of the electronic components in Conway's device for the reasons previously discussed in the overview of Ground 2A. *Supra*, Section IV.B; SAMSUNG-1003, ¶180.

The resulting combination would have rendered obvious each of claims 12-20, and would have provided each element of these claims for the reasons discussed above with respect to claim 1 in Grounds 1A-1B and claims 12-20 in Ground 2A. SAMSUNG-1003, ¶181.

V. DISCRETIONARY CONSIDERATIONS

A. § 325(d) – *Advanced Bionics*

Neither Tung, Yu, nor Conway were previously cited to or by the Office in

connection with the '281 Patent, let alone applied in a rejection. Simonelli was cited during original examination, but it also was not addressed substantively during original examination. *Supra*, Section II.B.

Because the '281 Patent's prosecution did not involve negotiation between the applicant and the Examiner regarding the teachings of the prior art combinations applied in the instant Petition, none of Grounds 1A-2B can be said to be the same as, or substantially similar to, art or arguments that the Office previously considered in connection with the '281 Patent. To the extent Simonelli was previously considered at all during examination, the Examiner erred in overlooking its pertinent teachings cited in this Petition. The Examiner also did not have the benefit of considering Simonelli's teachings in combination with Tung, Yu, or Conway.

Under these circumstances, Petitioner respectfully submits that exercise of the Board's discretion to deny institution under § 325(d) is unwarranted.

B. §314(a) - *Fintiv*

The '281 Patent is the subject of complaints filed by Patent Owner in both district court and the ITC on September 12, 2022. SAMSUNG-1102, SAMSUNG-1103. The district court case is currently stayed pending resolution of the ITC matter, and thus only the ITC matter is proceeding at this time. Pursuant to the Director's Interim Guidance, the "PTAB will not discretionarily deny petitions based on

applying *Fintiv* to a parallel ITC proceeding.” SAMSUNG-1104, 6-7, 9. Accordingly, the *Fintiv* factors do not provide a reason to discretionarily deny institution based on the co-pending ITC proceeding.

VI. MANDATORY NOTICES UNDER 37 C.F.R § 42.8(a)(1)

A. Real Party-In-Interest Under 37 C.F.R. § 42.8(b)(1)

Petitioner Samsung Electronics Co., Ltd. and Samsung Electronics America, Inc. (collectively, “Samsung”) are the real parties-in-interest. No other parties had access to or control over this Petition, and no other parties funded this Petition.

B. Related Matters Under 37 C.F.R. § 42.8(b)(2)

The ’281 Patent is the subject of civil actions in *In the Matter of Semiconductor Devices, Mobile Devices Containing the Same, and Components Thereof* (ITC Inv. No. 337-TA-1336) and *Daedalus Prime LLC v. Samsung Electronics Co., Ltd. et al.*, 2:22-cv-00352 (E.D. Tex.) (stayed). Taiwan Semiconductor Manufacturing Co. Ltd. has also been named as a respondent in the ITC proceeding and a defendant in the E.D. Tex. proceeding.

Petitioner is not aware of any other disclaimers, reexamination certificates, or IPR petitions addressing the ’281 Patent.

C. Lead And Back-Up Counsel Under 37 C.F.R. § 42.8(b)(3)

Petitioner provides the following designation of counsel.

Lead Counsel	Backup counsel
W. Karl Renner, Reg. No. 41,265	Jeremy J. Monaldo, Reg. No. 58,680

Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 Email: IPR39843-0154IP1@fr.com	Nicholas Stephens, Reg. No. 74,320 Patrick King, Reg. No. 60,816 Fish & Richardson P.C. 60 South Sixth Street, Suite 3200 Minneapolis, MN 55402 Tel: 202-783-5070 Fax: 877-769-7945 PTABInbound@fr.com
---	---

D. Service Information

Please address all correspondence and service to the address listed above.

Petitioner consents to electronic service by email at IPR39843-0154IP1@fr.com

(referencing No. 39843-0154IP1 and cc'ing PTABInbound@fr.com, axf-ptab@fr.com, jjm@fr.com, nstephens@fr.com, and pking@fr.com).

VII. FEES

Petitioner authorizes charge of Deposit Account No. 06-1050 for any fees.

VIII. CONCLUSION

Petitioner requests IPR and cancellation of the Challenged Claims.

Attorney Docket No. 39843-0154IP1
IPR of U.S. Patent No. 11,251,281
Respectfully submitted,

Dated: March 6, 2023

/Jeremy J. Monaldo/
W. Karl Renner, Reg. No. 41,265
Jeremy J. Monaldo, Reg. No. 58,680
Nicholas Stephens, Reg. No. 74,320
Patrick King, Reg. No. 60,816
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

(Control No. IPR2023-00653) Attorneys for Petitioner

CERTIFICATION UNDER 37 CFR § 42.24

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,974 words, which is less than the 14,000 allowed under 37 CFR § 42.24.

Dated: March 6, 2023

/Jeremy J. Monaldo/

W. Karl Renner, Reg. No. 41,265
Jeremy J. Monaldo, Reg. No. 58,680
Nicholas Stephens, Reg. No. 74,320
Patrick King, Reg. No. 60,816
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
T: 202-783-5070
F: 877-769-7945

Attorneys for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 CFR §§ 42.6(e)(4)(i) *et seq.* and 42.105(b), the undersigned certifies that on March 6, 2023, a complete and entire copy of this Petition for *Inter Partes* Review and all supporting exhibits were provided by Federal Express, to the Patent Owner, by serving the correspondence address of record as follows:

KINNEY & LANGE, P.A.
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

/Diana Bradley/
Diana Bradley
Fish & Richardson P.C.
60 South Sixth Street, Suite 3200
Minneapolis, MN 55402
(858) 678-5667