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TITLE

PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

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PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

BACKGROUND

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation Application No. 13/729,579, filed December 28, 2012, entitled as "PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES", which is herein incorporated by reference.

Field

[0002] Embodiments relate to the field of processors. In particular, embodiments relate to the field of cache management in multi-core processors.

Background Information

[0003] Advances in semiconductor processing and logic design have permitted an increase in the amount of logic that may be included in processors and other integrated circuit devices. As a result, many processors now have multiple to many cores that are monolithically integrated on a single integrated circuit or die. The multiple cores generally help to allow multiple threads or other workloads to be performed concurrently, which generally helps to increase execution throughput.

[0004] However, the multiple cores may have a downside in terms of longer hit and/or miss latencies to a shared cache. Often, the processors have a shared cache that is physically distributed across the integrated circuit or die. For example, cache slices of the distributed cache may be co-located with corresponding cores. Commonly, all of the cores are able to access all of the cache slices. The time for a core to access data from a given cache slice generally depends on the distance between the core and the given cache slice. As a result, as the number of cores on the processor increases, the average distance between cores and cache slices, as well as the average access hit and/or miss latencies, also generally increases. In addition, the multiple or many cores also tend to increase the memory address entropy at memory controllers, which may tend to result in lower effective memory bandwidth.

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BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0004] The invention may best be understood by referring to the following description and accompanying drawings that are used to illustrate embodiments of the invention. In the drawings:

[0005] Figure 1 is a block diagram of an example computer system including an embodiment of a processor.

[0006] Figure 2 is a block diagram of a first detailed example embodiment of a processor having virtual clusters.

[0007] Figure 3 is a block diagram of a second detailed example embodiment of a processor having virtual clusters.

[0008] Figure 4 is a block flow diagram of an embodiment of a method of using virtual clusters.

[0009] Figure 5 is a block diagram of an embodiment of a processor having virtual clusters having virtual sub-clusters.

[0010] Figure 6 is a block diagram of an embodiment of a processor having a first virtual cluster with a higher power consumption state and a second virtual cluster with a selectively reduced lower power consumption state.

[0011] Figure 7 is a block diagram of an embodiment of computer system including a processor having virtual clusters and a memory storing virtual cluster aware software.

[0012] Figure 8A is a block diagram illustrating both an exemplary in-order pipeline and an exemplary register renaming, out-of-order issue/execution pipeline according to embodiments of the invention.

[0013] Figure 8B is a block diagram illustrating both an exemplary embodiment of an in-order architecture core and an exemplary register renaming, out-of-order issue/execution architecture core to be included in a processor according to embodiments of the invention.

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[0014] Figure 9A is a block diagram of a single processor core, along with its connection to the on-die interconnect network and with its local subset of the Level 2 (L2) cache, according to embodiments of the invention.

[0015] Figure 9B is an expanded view of part of the processor core in **Figure 9A** according to embodiments of the invention.

[0016] Figure 10 is a block diagram of a processor that may have more than one core, may have an integrated memory controller, and may have integrated graphics according to embodiments of the invention.

[0017] Figure 11 shown is a block diagram of a system in accordance with one embodiment of the present invention.

[0018] Figure 12 shown is a block diagram of a first more specific exemplary system in accordance with an embodiment of the present invention.

[0019] Figure 13 shown is a block diagram of a second more specific exemplary system in accordance with an embodiment of the present invention.

[0020] Figure 14 shown is a block diagram of a SoC in accordance with an embodiment of the present invention.

[0021] Figure 15 is a block diagram contrasting the use of a software instruction converter to convert binary instructions in a source instruction set to binary instructions in a target instruction set according to embodiments of the invention.

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DETAILED DESCRIPTION

[0022] Disclosed herein are processors having virtually clustered cores and cache slices, methods performed by and/or within the processors, and systems incorporating one or more of such processors. In the following description, numerous specific details are set forth (e.g., specific numbers and arrangements of cores and cache slices, specific ways of groupings of cores and cache slices into clusters, specific interconnects, processor configurations, microarchitectural details, logic partitioning/integration details, sequences of operations, types, interrelationships of system components, and the like). However, it is understood that embodiments of the invention may be practiced without these specific details. In other instances, well-known circuits, structures and techniques have not been shown in detail in order not to obscure the understanding of this description.

[0023] Figure 1 is a block diagram of an example computer system 100 including an embodiment of a processor 101. In some embodiments, the processor may be a general-purpose processor (e.g., of the type used in server, desktop, laptop, netbook, tablet, smartphone, cell phone, smart television, video game console, and like computer systems). Alternatively, the processor may be a special-purpose processor. Examples of suitable special-purpose processors include, but are not limited to, network processors, communications processors, cryptographic processors, graphics processors, co-processors, embedded processors, and digital signal processors (DSPs), to name just a few examples.

[0024] The processor represents a physical processor, integrated circuit, or die. The physical processor may include any desired number of cores, other processing elements, or other logical processors. The illustrated embodiment of the physical processor is a multi-core processor including a first core 1 102-1 through an Nth core N 102-N, where N may be any appropriate number, often ranging from two to several hundred, more often on the order of tens (e.g., ten to one hundred). The cores are coupled together by one or more on-die or on-substrate interconnect structures (e.g., a ring, torus, mesh, other known interconnect structure, etc.). The core 1 includes an execution pipeline 103-1. Similarly, the core N includes an execution pipeline 103-N. Each execution pipeline may represent any known pipeline, and may include, for example, fetch logic, decode logic, allocation

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logic, renaming logic, scheduling logic, register access logic, execution logic, write back logic, and commit logic, or various combinations thereof. The cores may be either single threaded or multi-threaded. The cores 102 may be symmetric cores, asymmetric cores (e.g., heterogeneous cores), or some may be symmetric and others asymmetric.

[0025] The term core often refers to logic located on an integrated circuit that is capable of maintaining an independent architectural state (e.g., an execution state), in which the independently maintained architectural state is associated with dedicated execution resources. In contrast, the term hardware thread often refers to logic located on an integrated circuit that is capable of maintaining an independent architectural state, in which the independently maintained architectural state shares access to the execution resources it uses. When certain resources are shared by an architectural state, and others are dedicated to the architectural state, the line between a core and a hardware thread is less distinct. Nevertheless, the core and the hardware thread are often viewed by an operating system as individual processing elements or logical processors. The operating system is generally able to individually schedule operations on each of the cores, hardware threads, or other logical processors or processing elements. In other words, a processing element or logical processor, in one embodiment, may represent any on-die processor logic capable of being independently associated with code, such as a software thread, operating system, application, or other code. While many of the embodiments herein show cores as examples of the logical processors or processing elements, in other embodiments these cores may be replaced by other logical processors or processing elements. Examples of such other logical processors or processing elements include, but are not limited to, hardware threads, thread units, thread slots, process units, contexts, and/or any other logic that is capable of holding state and being independently associated with code.

[0026] Referring again to **Figure 1**, the core 1 includes one or more lower level caches 104-1. Similarly, the core N includes one or more lower level caches 104-N. In some embodiments, each core may have a single level of lower level cache. In other embodiments, each core may have two or more levels of lower level cache (e.g., a lowest level of cache closest to the core and a mid-level cache farther from the core). Each of

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the one or more lower level caches may cache recently obtained data and/or instructions. The pipelines within each core may attempt to access data and/or instructions within the one or more lower level cache(s) of the corresponding core.

[0027] The core 1 102-1 through the core N 102-N also share a higher level cache 105. The one or more lower level caches 104 are referred to as lower level because they are closer physically and/or logically to their corresponding cores (e.g., the execution logic within the cores) than the shared higher level cache. In some embodiments, the cores may check the one or more lower level caches for data and/or instructions first. Then, if the sought data is not found in the one or more lower levels of cache, the cores may proceed to check the shared higher level cache. In some embodiments, the higher level shared cache may represent a last level data and/or instruction cache (LLC). The LLC may represent the last cache in the memory hierarchy on the processor (e.g., on die).

[0028] The processor also includes a first cache coherency aware memory controller 108-1 to couple the processor with a first memory 109-1, and a second cache coherency aware memory controller 108-2 to couple the processor with a second memory 109-2. In some embodiments, each cache coherency aware memory controller may include home agent logic that is operable to perform cache coherency and second memory controller logic that is operable to interact with the memory. For simplicity, in the present description, such a home agent and memory controller functionalities will be referred to as a cache coherency aware memory controller. Other embodiments may include fewer or more cache coherency aware memory controllers. Moreover, while in the illustrated embodiment, the cache coherency aware memory controllers are on-die or on-processor, in other embodiments they may instead be off-die or off-processor (e.g., as one or more chipset components).

[0029] Conventionally, the cores would generally access the first and second memories through the first and second cache coherency aware memory controllers, as well as through any intervening cores that are coupled between the accessing cores and the cache coherency aware memory controllers. Accesses through multiple or potentially many intervening cores generally tends to take more time, resulting in greater memory access latencies, than accesses through less or no intervening cores. This generally translates to

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reduced performance in a conventional system, as well as possibly extra power consumption and heat generation (e.g., due to extra electrical signals, to wake intervening sleeping cores, etc.).

[0030] The processor also includes first optional bus interface logic 110 to couple the processor with an input/output (I/O) controller hub 111 and one or more I/O devices 112. In other embodiments, the I/O controller hub may be replaced by another type of chipset component, or the I/O controller hub may be integrated on-die. The processor also includes second optional bus interface logic 113 to couple the processor with one or more other processors 114 (e.g., in the case of a server or other multi-socket system). In the illustration, the first and second memories 109, the I/O controller hub 111, the I/O device(s) 112, and the one or more processors 114, are shown in dashed lines to indicate that, in some embodiments, they are system-level components of a system in which the processor is deployed, and are not necessarily components of the processor.

[0031] The shared higher level cache 105 is commonly implemented as a distributed cache including multiple physically distributed cache slices 107. For example, a first cache slice 1 107-1 may correspond to, and often be closely physically located on die with (e.g., co-located with), the first core 1 102-1. Similarly, an Nth cache slice N 107-N may correspond to, and often be closely physically located on die relative to (e.g., co-located with), the Nth core N 102-N. The cache slices are often in the uncore portion of the processor.

[0032] A first core-cache slice interface logic 1 106-1 may interface the cores to the first cache slice 1 107-1. Similarly, an Nth core-cache slice interface logic N 106-N may interface the cores to the Nth cache slice N 107-N. In some embodiments, each core-cache slice interface logic may include a first core interface logic (e.g., a corebo) and a second cache slice interface logic (e.g., a cachebo) that work together to provide a core-cache slice interface, although this is not required. The set of all cache slice interface logic may also be referred to herein as a caching agent. The collective set of cache slice interface logic (e.g., the set of all cachebo) may also be referred to as a caching agent of the processor or physical socket.

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[0033] As discussed above in the background section, the distributed shared cache may have a downside of longer shared cache hit and/or miss latencies especially when there are many cores. Conventionally, all of the cores of the processor usually have access to all of the cache slices on the die. The time for a core to access data from a given cache slice generally depends on the distance between the core and the given cache slice. For example, it will generally take longer for a core to access data from a remote cache slice than from a nearby cache slice. As a result, as the number of cores on the processor increases, the average distance between cores and cache slices, as well as the average access hit and/or miss latencies, also generally increases. In addition, the multiple or many cores generally tend to increase the address entropy at cache coherency aware memory controllers (e.g., different cores may be processing different workloads and accessing different pages and/or data structures in memory) which may tend to result in lower effective memory bandwidth.

[0034] In some embodiments, the cores 102 and distributed portions of the shared higher level cache 105 of the same monolithic integrated circuit, die, or semiconductor substrate may be logically or virtually partitioned, clustered, or otherwise grouped into two or more partitions, clusters, or other groups. For example, as shown in the illustrated embodiment, the first core 1 102-1, the first cache slice 1 107-1, the first interface logic 1 106-1, and the first cache coherency aware memory controller 108-1 may be logically or virtually clustered or grouped into a first virtual cluster 115-1. Similarly, the Nth core N 102-N, the Nth cache slice N 107-1, the Nth interface logic N 106-N, and the second cache coherency aware memory controller 108-1 may be logically or virtually clustered or grouped into a second virtual cluster 115-2. Other analogous components (e.g., other cores, other cache slices, etc.) may also be included in each virtual cluster. In other embodiments, instead of the cores, other logical processors and/or processing elements and their corresponding shared higher level cache slices may be similarly logically or virtually clustered. In other embodiments, instead of just two virtual clusters there may be three or more virtual clusters each having a set of one or more cores and cache slices.

[0035] In some embodiments, when an access (e.g., a memory request) misses in the one or more lower level caches 104 of a core 102, the access may be directed initially to only

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the cache slices 107 of the shared higher level cache 105 that are in the corresponding virtual cluster 115. In some embodiments, the logical or virtual partitioning, clustering, or grouping may be done to reduce average access hit and/or miss latencies. For example, in some embodiments, the grouping may be done based on physical proximity. For example, neighboring or physically proximate cores and/or their corresponding cache slices may be preferentially or predominantly clustered or grouped together. In some embodiments, the average distance between cores and/or cache slices within a virtual cluster (e.g., the intra-virtual cluster distance) may be less than the average distance between all cores and/or cache slices between virtual clusters and/or within a socket (e.g., the inter-virtual cluster distance). As another example, in some embodiments, the grouping may be done based on the coupling of the cores to interconnect structures. For example, the grouping may be done to predominantly virtually group cores on a common ring interconnect or other interconnect structure together.

[0036] Advantageously, this may help to improve performance by reducing hit and/or miss latencies for accesses to the shared higher level cache 105. For example, when neighboring or proximate cores and their corresponding cache slices are grouped, the accesses may be directed initially to only the neighboring or proximate cache slices of the shared higher level cache in the corresponding virtual cluster. Instead of having to check all of the cache slices, only those cache slices in the virtual cluster may need to be checked initially. Moreover, this may tend to increase the likelihood that the accesses are serviced by nearby/proximate cache slices instead of the accesses needing to travel all the way to the farthest or most remote cache slices on the die. This may tend to reduce the average distance the accesses need to travel in order to be serviced, which in turn may tend to reduce access hit and/or miss latencies. Moreover, when cores and/or cache slices on the same ring interconnect or other interconnect structure are grouped together, shorter ring stop hops, or other shorter interconnect accesses on average may be achieved as compared to if they were not on the same interconnect structures. This also may tend to reduce access hit and/or miss latencies.

[0037] In some embodiments, if the access also misses in the cache slices 107 in the corresponding virtual cluster 115, then the access may initially be directed only to a

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cache coherency aware memory controller 108 in the same corresponding virtual cluster 115. In some embodiments, the cache coherency aware memory controller may be the one closest to the cores and/or cache slices of that virtual cluster (e.g., closest on average, closest to the majority, or the like.). The cache coherency aware memory controller may be operable to snoop or otherwise communicate with other cache coherency aware memory controllers in order to attempt to service the request (e.g., determine where the memory address is homed).

[0038] Advantageously, this may also help to improve performance by decreasing the address entropy experienced by the cache coherency aware memory controllers. Rather than receiving addresses from all of the cores (e.g., all the different threads or other processes executing thereon), each cache coherency aware memory controllers may only receive addresses from a subset of the cores in that memory controllers virtual cluster (e.g., in some cases about half or less of the cores). As a result, each cache coherency aware memory controller may tend to see less address entropy from fewer cores serviced over a given period of time. Often, different threads or software processes tend to use different data structures in memory so reducing the number of different threads or software processes handled by a memory controller generally tends to reduce the randomness or entropy of the memory addresses it receives. This may help to improve the overall efficiency of the adaptive page open policy implemented by the cache coherency aware memory controller (e.g., resulting in improved page hit ratios). This in turn may tend to increase the effective memory bandwidth and/or memory throughput.

[0039] In some embodiments, the cache coherency aware memory controller may include logic that is operable to snoop one or more caching agents of one or more other virtual clusters of the processor (i.e., on the same die and/or within the same physical socket). In some embodiments, the cache coherency aware memory controller may include logic that is operable to indicate a particular virtual cluster and/or a particular virtual socket (e.g., by targeting a particular QPI port) when snooping a remote caching agent of a different processor (i.e., on a different die and/or in a different physical socket). Advantageously, this may help to utilize bus bandwidth efficiently (e.g., utilize QPI bandwidth in a balanced fashion). In some embodiments, the cache coherency aware memory controller

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may include logic that is operable to filter snoops to remote and/or local caching agents of virtual clusters/sockets using a snoop filter. In some embodiments, the cache coherency aware memory controller may include logic that is operable to reduce bus traffic (e.g., QPI bandwidth) and/or the associated power consumption by utilizing fanout snoops when snooping remote caching agents for virtual clusters of a different processor, as opposed to directed snoops that may result in multiple snoop messages to the same socket. In some embodiments, a single snoop fanout may arrive at a physical socket (e.g., at a QPI module) and in response to the single snoop fanout multiple directed snoops may be performed within the physical socket to multiple caching agents and/or virtual clusters within the physical socket (e.g., the QPI module may send one directed snoop to each of the caching agents in the physical socket).

[0040] In some embodiments, each virtual cluster of a processor (e.g., a physical socket or die) may have a copy of a cache line. Some other approaches only allow one copy of the cache line for the processor. Allowing each virtual cluster of the processor to have a copy of the cache line may offer an advantage if the operating system allocates memory in the adjacent cluster or the operating system migrates a process from one virtual cluster to another while the memory pages were not migrated to the cluster where the process presently resides.

[0041] In the illustrated embodiment, for simplicity, only two virtual clusters are shown. Other embodiments may include three, four, or more virtual clusters. In one aspect, there may be as many clusters as cache coherency aware memory controllers if it is desired to include a cache coherency aware memory controller within each cluster, which is often advantageous but is not required. In some embodiments, each of the virtual clusters may have the same number of cores and/or cache slices. This may offer certain advantages (e.g., in implementation efficiency). In other embodiments, each of the virtual clusters may have a different number of cores and/or cache slices.

[0042] To avoid obscuring the description, a relatively simple processor 101 has been shown and described. In other embodiments, the processor may optionally include other well-known components, such as, for example, an instruction fetch unit, an instruction scheduling unit, a branch prediction unit, instruction and data caches, instruction and data

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translation lookaside buffers, prefetch buffers, microinstruction queues, microinstruction sequencers, bus interface units, second or higher level caches, a retirement unit, a register renaming unit, other conventional components, and various combinations thereof. There are literally numerous different combinations and configurations of components in processors, and embodiments are not limited to any particular combination or configuration. The processor may represent an integrated circuit or set of one or more semiconductor dies or chips (e.g., a single die or chip, or a package incorporating two or more die or chips). In some embodiments, the processor may represent a system-on-chip (SoC) and/or a chip multi-processor (CMP).

[0043] **Figure 2** is a block diagram of a first detailed example embodiment of a processor 201 having a first virtual cluster 215-1 and a second virtual cluster 215-2. In some embodiments, the processor of **Figure 2** may be included in the system of **Figure 1**. Alternatively, the processor of **Figure 2** may be included in a similar or different system. Moreover, the system of **Figure 1** may include either the same, similar, or different processor than that of **Figure 2**.

[0044] The processor includes eighteen cores and eighteen corresponding (e.g., co-located) cache slices. Each of these is shown in the illustration as a core/slice. A leftmost eight of the cores/slices are coupled with a first ring interconnect 220-1. A rightmost ten of the cores/slices are coupled with a second ring interconnect 220-2. The first and second ring interconnects are coupled by a first inter-ring connection logic 222-1 and a second inter-ring connection logic 222-2. In some embodiments, each of the first and second inter-ring connection logics may be a switch box (Sbox), or other mechanism for coupling ring interconnects.

[0045] Also coupled with the first ring interconnect is an optional first bus interface logic 213 and an optional second bus interface logic 210. An optional third bus interface logic 224 is coupled with the second ring interconnect. In some embodiments, the first bus interface logic may be used to couple the processor with one or more other processors. Alternatively, in a single socket system, the first bus interface logic may be omitted. In some embodiments, the second bus interface logic may be used to couple the processor with an I/O hub (not shown). In other embodiments, an I/O controller may be integrated

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on processor. Examples of suitable bus interface logic include, but are not limited to, Quick Path Interconnect (QPI), other point-to-point interconnects, and other interconnects known in the arts.

[0046] A first cache coherency aware memory controller 208-1 is coupled with the first ring interconnect. A second cache coherency aware memory controller 208-2 is coupled with the second ring interconnect. The first cache coherency aware memory controller may be used to couple the processor with a first memory (not shown). The second cache coherency aware memory controller may be used to couple the processor with a second memory (not shown). In some embodiments, each of the cache coherency aware memory controllers includes a home agent including cache coherency functionality and a memory controller including memory interface functionality.

[0047] In the illustrated embodiment, the first virtual cluster includes all eight of the cores/slices (i.e., core/slice 0 through core/slice 7) coupled with the first ring interconnect as well as one core/slice (i.e., core/slice 8) coupled with the second ring interconnect. The second virtual cluster includes all remaining nine cores/slices (i.e., core/slice 0 through core/slice 8) coupled with the second ring interconnect. In other embodiments, different ways of dividing the cores/slices between the virtual clusters may be used. Notice that, in some embodiments, physically proximal cores/slices and/or cores/slices on the same interconnect structure may be preferentially or predominantly (i.e., at least a majority) included in a virtual cluster. Although this is not required, this may offer advantages of reduced hit/miss latencies, as described elsewhere herein.

[0048] Notice also that, in some embodiments, an equal number of cores/slices may be included in each of the virtual clusters. This is not required, but often offers an advantage of a simpler implementation. Commonly the memory address space of the memory may be mapped across all of the cache slices. For example, each memory address may be mapped to a cache slice through a hash function. For example, the hash of a given memory address may always provide the same value which may always map to the same cache slices. Often the hash function may attempt to approximately evenly distribute the memory addresses across the cache slices. For example, memory address A may always hash to the binary value 0111, memory address B may always hash to the binary value

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0101, and so on. Since there are fewer cores/slices in a virtual cluster (e.g., half in the illustrated embodiment), a smaller hash may be used.

[0049] Referring again to **Figure 2**, each of the cores/slices has a corresponding identifier as shown within the core/slice. These identifiers may be referred to as core/slice identifiers and/or ring stop identifiers. Each identifier uniquely identifies a corresponding core/slice (i.e., each core/slice has a different identifier). For example, the identifier value 00000 identifies core/slice 0 of the first virtual cluster, the identifier value 10000 identifies core/slice 8 of the first virtual cluster, the identifier value 00111 identifies core/slice 3 of the second virtual cluster, and so on. As shown, in one possible embodiment, the IDs for the cores/slices may be assigned starting from the lower left corner (as viewed) of the leftmost ring and moving around the leftmost ring counterclockwise, and starting from the lower left corner of the rightmost ring and moving around the rightmost ring counterclockwise.

[0050] Notice that, in some embodiments, the bit-0 (i.e., the rightmost bit) of each of the identifiers is always binary zero (i.e., 0) for the first virtual cluster and is always binary one (i.e., 1) for the second virtual cluster. In some embodiments, this bit-0 having a value of binary zero (i.e., 0) may be used as an identifier of the first virtual cluster, and this bit-0 having a value of binary one (i.e., 1) may be used as an identifier of the second virtual cluster. The remaining more significant bits of the ID uniquely identify one of the cores/slices within the virtual cluster identified by bit-0. Looking at this another way, the cores/slices of one virtual cluster may be evenly numbered (e.g., 0, 2, 4, 6, etc.) and the cores/slices of the other virtual cluster may be oddly numbered (e.g., 1, 3, 5, etc.).

[0051] In some embodiments, this may allow the hash of a given memory address to always map to the same corresponding core/slice in all of the virtual clusters. For example, the hash of a given memory address with a value of 0111 may always map to core/slice 7 in the first virtual cluster as well as core/slice 7 in the second virtual cluster. In some embodiments, this may be used to efficiently implement virtual cluster-to-virtual cluster transfers of cache data. For example, if the cache data comes from core/slice 7 of the first virtual cluster and has ring stop ID 01110, then only bit-0 of the ring stop ID may be changed/flipped to obtain the ring stop ID for the corresponding core/slice 7 of the

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second virtual cluster (i.e., changing from 01110 to 01111). Accordingly, in some embodiments, having the same number of cores/slices in each virtual cluster may simplify determining to which core/slice to forward data to in the other virtual clusters, although this is not required.

[0052] **Figure 3** is a block diagram of a second detailed example embodiment of a processor 301 having a first virtual cluster 315-1 and a second virtual cluster 315-2. In some embodiments, the processor of **Figure 3** may be included in the system of **Figure 1**. Alternatively, the processor of **Figure 3** may be included in a similar or different system. Moreover, the system of **Figure 1** may include either the same, similar, or different processor than that of **Figure 3**.

[0053] The second detailed example embodiment is similar in many ways to the first detailed example embodiment previously described. Unless otherwise specified or clearly apparent the correspondingly named components may optionally have the same or similar characteristics. To avoid obscuring the description, primarily different and/or additional structures and characteristics of the second detailed example embodiment will be described, without repeating all of the similar or same features.

[0054] The processor includes twelve cores/slices. A leftmost eight of the cores/slices are coupled with a first ring interconnect 320-1. A rightmost four of the cores are coupled with a second half-ring interconnect 320-2. The first and second interconnects are coupled by a first inter-ring connection logic 322-1 and a second inter-ring connection logic 322-2.

[0055] Also coupled with the first ring interconnect is an optional first bus interface logic 313 (e.g., to couple with one or more other processors), an optional second bus interface logic 310 (e.g., to couple with an I/O hub), and a first cache coherency aware memory controller 308-1 (e.g., to couple with a memory). Examples of suitable bus interface logic include, but are not limited to, QPI. Also coupled with the second interconnect is a second cache coherency aware memory controller 308-2 (e.g., to couple with a memory). In some embodiments, each of the cache coherency aware memory controllers includes a home agent including cache coherency functionality and a memory controller including memory interface functionality.

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[0056] In the illustrated embodiment, the first virtual cluster includes six (i.e., core/slice 0 through core/slice 5) of the eight cores/slices coupled with the first ring interconnect. The second virtual cluster includes the remaining two (i.e., core/slice 0 and core/slice 1) of the eight cores/slices coupled with the first ring interconnect and all four of the cores/slices coupled with the second interconnect (i.e., core/slice 2 through core/slice 5). In other embodiments, different ways of dividing the cores/slices between the virtual clusters may be used. Notice that, in some embodiments, physically proximal cores/slices and/or cores/slices on the same interconnect structure may be preferentially or predominantly included in a virtual cluster. Although this is not required, this may offer advantages of reduced hit/miss latencies, as described elsewhere herein. Notice also that, in some embodiments, an equal number of cores/slices may be included in each of the virtual clusters. This is not required, but often offers an advantage of a simpler implementation, as previously described.

[0057] Each of the cores/slices has a corresponding core/slice identifier and/or ring stop identifier as shown within the core/slice. Notice that, in some embodiments, the bit-0 (i.e., the rightmost bit) of each of the identifiers is always binary zero (i.e., 0) for the first virtual cluster and is always binary one (i.e., 1) for the second virtual cluster. In some embodiments, this bit-0 having a value of binary zero (i.e., 0) may be used as an identifier of the first virtual cluster, and this bit-0 having a value of binary one (i.e., 1) may be used as an identifier of the second virtual cluster. In other embodiments, if there are three or more virtual clusters, then two or more bits may be used to uniquely identify one of the virtual clusters. In some embodiments, this may allow the hash of a given memory address to always map to the same corresponding core/slice in all of the virtual clusters. In some embodiments, this may be used to efficiently implement virtual cluster-to-virtual cluster transfers of cache data.

[0058] **Figures 2-3** are illustrative examples of virtual clusters, although the scope of the invention is not limited to just these examples. Other embodiments may include other numbers of cores and/or cache slices, other couplings of cores and/or cache slices, other types of interconnects, other numbers and couplings of cache coherency aware memory controllers, may omit some of the illustrated components and/or include additional

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components, may group cores and/or slices and/or memory controllers differently into virtual clusters, may have more than two virtual clusters, etc.

[0059] Figure 4 is a block flow diagram of an embodiment of a method 440 of using virtual clusters. In some embodiments, the method may be performed by the processor of any of **Figures 1-3**. Alternatively, the method may be performed by similar or different processors. Moreover, the processors of any of **Figures 1-3** may perform the same, similar, or different methods. The features and optional details of the processors also may apply to the method, which may be performed by and/or within the processors.

[0060] The method includes virtually clustering logical processors into a virtual cluster, at block 441. In some embodiments, each of the logical processors has one or more corresponding lower level caches. The method also includes directing an access that misses in one or more lower level caches corresponding to a logical processor to a subset of distributed cache slices, of a shared higher level cache, that are in a virtual cluster that corresponds to the logical processor, at block 442.

[0061] Figure 5 is a block diagram of an embodiment of a processor 501 having virtual clusters 515 that have virtual sub-clusters 530. The processor includes first though fourth sets of cores/slices 528-1 through 528-4. The processor also includes first, second, third, and fourth cache coherency aware memory controllers 508-1 through 508-4. Each of the cores/slices and the cache coherency aware memory controllers may be substantially as described elsewhere herein aside from different features mentioned below.

[0062] The first and second sets of cores/slices 528-1, 528-2 and the first and second cache coherency aware memory controllers 508-1, 508-2 are included in a first virtual cluster 515-1. The third and fourth sets of cores/slices 528-3, 528-4 and the third and fourth cache coherency aware memory controllers 508-3, 508-4 are included in a second virtual cluster 515-2. In some embodiments, the first virtual cluster 515-1 is logically or virtually divided, partitioned, or clustered into a first virtual sub-cluster 530-1 including the first set of cores/slices 528-1 and the first cache coherency aware memory controller 508-1, and a second virtual sub-cluster 530-2 including the second set of cores/slices 528-2 and the second cache coherency aware memory controller 508-2. Likewise, the second virtual cluster 515-2 is logically or virtually divided, partitioned, or clustered into a third

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virtual sub-cluster 530-3 including the third set of cores/slices 528-3 and the third cache coherency aware memory controller 508-3, and a fourth virtual sub-cluster 530-4 including the fourth set of cores/slices 528-4 and the fourth cache coherency aware memory controller 508-4.

[0063] In some embodiments, the sub-clusters of a virtual partition are predominantly physically proximately grouped. In some embodiments, the sub-clusters of a virtual partition are part of a same interconnect ring or other interconnect structure 520-1, 520-2. In some embodiments, the cores/slices of one virtual sub-cluster of a given virtual partition are on average closer and/or on average have shorter hit/miss latencies to a memory controller of another virtual sub-cluster of the given virtual partition than virtual sub-clusters of other virtual partitions of a processor. In some embodiments, misses to a cache coherency aware memory controller of one virtual sub-cluster of a given virtual cluster may be preferentially or initially attempted to be serviced only by one or more other virtual sub-clusters of the same given virtual cluster. This may help to provide improved performance.

[0064] This is just one illustrative example of sub-clustering. Other embodiments may have other numbers of virtual clusters, other numbers of virtual sub-clusters, other numbers of memory controllers, etc.

[0065] Figure 6 is a block diagram of an embodiment of a processor 601 having a first virtual cluster with a higher power consumption state 615-1 and a second virtual cluster with a selectively reduced lower power consumption state 615-2. Each of the virtual clusters includes one or more cores 602 and one or more cache slices 607. The terms lower and higher are relative terms that are relative to one another not absolute terms. Examples of suitable ways to reduce the power consumption state include, but are not limited to, reducing the frequency of the virtual cluster, reducing the voltage of the virtual cluster, gating power to the virtual cluster, and other approaches known in the arts (e.g., selectively gating power to portions of the second virtual cluster).

[0066] In some embodiments, the power consumption of the second virtual cluster may be selectively reduced based on workload (e.g., current or estimated future). For example, when the workload is not sufficient to keep both virtual clusters busy (e.g., less

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than a threshold amount for example 30%), an operating system, virtual machine monitor (VMM), or other software, which may be aware of the virtual clustering of the processor, may migrate or move active pages from a cache coherency aware memory controller for the second virtual cluster to that of the first virtual cluster, migrate all threads, processes, or other workloads from the second virtual cluster to the first virtual cluster, and then selectively reduce the power consumption state of the second virtual cluster. For example, the software may gate power to the one or more cores 602, the one or more cache slices 607, the cache coherency aware memory controller of the second virtual cluster, put the corresponding memory to sleep, or some combination thereof. When the workload increases, the second virtual cluster may be brought back to its previous higher power consumption state.

[0067] Figure 7 is a block diagram of an embodiment of computer system 700 including a processor 701 having virtual clusters 715 and a memory 709 storing virtual cluster aware software 740. The virtual clusters include a first virtual cluster 715-1 through an Nth virtual cluster 715-N, where N may be any appropriate number, often ranging from two to on the order of around ten, or so. Each virtual cluster includes one or more cores 702 and one or more cache slices 707. The virtual cluster aware software 740 is aware of the virtual clusters 715. Examples of suitable virtual cluster aware software include, but are not limited to, an operating system, a virtual machine monitor, other privileged software, user-level applications, etc.).

[0068] In some embodiments, the virtual cluster aware software may include virtual cluster aware and Non-Uniform Memory Access (NUMA) aware software 742. NUMA recognizes that memory accesses in systems may be non-uniform. For example, memory access times may depend on the location of the memory relative to a core and/or the location of the memory controller. The processor is commonly connected with a single physical socket. The physical socket may represent the physical connector on a board (e.g., a motherboard) where the processor is connected when deployed in a system. In some embodiments, logically or virtually clustering or grouping the cores and cache slices into the virtual clusters may effectively provide multiple logical or virtual sockets.

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[0069] In some embodiments, the NUMA aware software may perform virtual cluster level NUMA improvements or optimizations. For example, the NUMA aware software may attempt to minimize or at least reduce cross-virtual-socket traffic and/or cross-physical socket traffic, which may help to achieve higher throughput. In some embodiments, the virtual clusters may be treated by the software as virtual sockets. In some embodiments, when a process of a given virtual cluster (e.g., running on a core of that given virtual cluster) needs more memory allocated, the NUMA aware software may allocate the additional memory from a portion of the overall memory corresponding to that given virtual cluster instead of from other memory not corresponding to that given virtual cluster. In addition, in the event of there being no available memory for the given virtual cluster, in some embodiments, the NUMA aware software may allocate the additional memory from a portion of the overall memory corresponding to another virtual cluster within the same physical socket instead of from memory corresponding to other physical sockets. Cache-to-cache transfers within a physical socket generally tend to be faster than cache-to-cache transfers between physical sockets.

[0070] Accordingly, in some embodiments, the NUMA aware software may allocate memory in a way that is based on and aware of the virtual clusters in order to help improve performance. For example, in some embodiments, the NUMA aware software may preferentially or initially allocate memory for a given virtual cluster (or given virtual socket) intra-virtual cluster (or intra-virtual socket), rather than inter-virtual cluster (or inter-virtual socket). In some embodiments, the NUMA aware software may preferentially or initially allocate memory for a given virtual cluster (or virtual socket) intra-physical socket (e.g., from virtual clusters within that physical socket) rather than inter-physical socket (e.g., from virtual clusters of different physical sockets).

[0071] In some embodiments, the virtual cluster aware software may also include virtual cluster aware power management software 744. The virtual cluster aware power management software may perform power management of a virtual cluster as previously described in conjunction with **Figure 6**.

[0072] In some embodiments, the features of the processors of **Figures 6-7** may be included in the processors of any of **Figures 1-3**. Alternatively, the features of the

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processors of **Figures 6-7** may be included in similar or different processors. Moreover, the processors of any of **Figure 1-3** may have the same, similar, or different features than the processors of **Figures 6-7**.

[0073] While distributed shared caches have been disclosed herein, other embodiments may use centralized shared caches. These embodiments may still benefit from reduced address entropy at the cache coherency aware memory controllers. While embodiments have shown ring-type interconnects, other embodiments may use other interconnects, such as, for example, torus, mesh, point-to-point, multi-drop, or other known types of interconnects. Exemplary Core Architectures, Processors, and Computer Architectures

[0074] Processor cores may be implemented in different ways, for different purposes, and in different processors. For instance, implementations of such cores may include: 1) a general purpose in-order core intended for general-purpose computing; 2) a high performance general purpose out-of-order core intended for general-purpose computing; 3) a special purpose core intended primarily for graphics and/or scientific (throughput) computing. Implementations of different processors may include: 1) a CPU including one or more general purpose in-order cores intended for general-purpose computing and/or one or more general purpose out-of-order cores intended for general-purpose computing; and 2) a coprocessor including one or more special purpose cores intended primarily for graphics and/or scientific (throughput). Such different processors lead to different computer system architectures, which may include: 1) the coprocessor on a separate chip from the CPU; 2) the coprocessor on a separate die in the same package as a CPU; 3) the coprocessor on the same die as a CPU (in which case, such a coprocessor is sometimes referred to as special purpose logic, such as integrated graphics and/or scientific (throughput) logic, or as special purpose cores); and 4) a system on a chip that may include on the same die the described CPU (sometimes referred to as the application core(s) or application processor(s)), the above described coprocessor, and additional functionality. Exemplary core architectures are described next, followed by descriptions of exemplary processors and computer architectures.

Exemplary Core Architectures

In-order and out-of-order core block diagram

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[0075] **Figure 8A** is a block diagram illustrating both an exemplary in-order pipeline and an exemplary register renaming, out-of-order issue/execution pipeline according to embodiments of the invention. **Figure 8B** is a block diagram illustrating both an exemplary embodiment of an in-order architecture core and an exemplary register renaming, out-of-order issue/execution architecture core to be included in a processor according to embodiments of the invention. The solid lined boxes in **Figures 8A-B** illustrate the in-order pipeline and in-order core, while the optional addition of the dashed lined boxes illustrates the register renaming, out-of-order issue/execution pipeline and core. Given that the in-order aspect is a subset of the out-of-order aspect, the out-of-order aspect will be described.

[0076] In **Figure 8A**, a processor pipeline 800 includes a fetch stage 802, a length decode stage 804, a decode stage 806, an allocation stage 808, a renaming stage 810, a scheduling (also known as a dispatch or issue) stage 812, a register read/memory read stage 814, an execute stage 816, a write back/memory write stage 818, an exception handling stage 822, and a commit stage 824.

[0077] **Figure 8B** shows processor core 890 including a front end unit 830 coupled to an execution engine unit 850, and both are coupled to a memory unit 870. The core 890 may be a reduced instruction set computing (RISC) core, a complex instruction set computing (CISC) core, a very long instruction word (VLIW) core, or a hybrid or alternative core type. As yet another option, the core 890 may be a special-purpose core, such as, for example, a network or communication core, compression engine, coprocessor core, general purpose computing graphics processing unit (GPGPU) core, graphics core, or the like.

[0078] The front end unit 830 includes a branch prediction unit 832 coupled to an instruction cache unit 834, which is coupled to an instruction translation lookaside buffer (TLB) 836, which is coupled to an instruction fetch unit 838, which is coupled to a decode unit 840. The decode unit 840 (or decoder) may decode instructions, and generate as an output one or more micro-operations, micro-code entry points, microinstructions, other instructions, or other control signals, which are decoded from, or which otherwise reflect, or are derived from, the original instructions. The decode unit 840 may be implemented using various different mechanisms. Examples of suitable

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mechanisms include, but are not limited to, look-up tables, hardware implementations, programmable logic arrays (PLAs), microcode read only memories (ROMs), etc. In one embodiment, the core 890 includes a microcode ROM or other medium that stores microcode for certain macroinstructions (e.g., in decode unit 840 or otherwise within the front end unit 830). The decode unit 840 is coupled to a rename/allocator unit 852 in the execution engine unit 850.

[0079] The execution engine unit 850 includes the rename/allocator unit 852 coupled to a retirement unit 854 and a set of one or more scheduler unit(s) 856. The scheduler unit(s) 856 represents any number of different schedulers, including reservations stations, central instruction window, etc. The scheduler unit(s) 856 is coupled to the physical register file(s) unit(s) 858. Each of the physical register file(s) units 858 represents one or more physical register files, different ones of which store one or more different data types, such as scalar integer, scalar floating point, packed integer, packed floating point, vector integer, vector floating point,, status (e.g., an instruction pointer that is the address of the next instruction to be executed), etc. In one embodiment, the physical register file(s) unit 858 comprises a vector registers unit, a write mask registers unit, and a scalar registers unit. These register units may provide architectural vector registers, vector mask registers, and general purpose registers. The physical register file(s) unit(s) 858 is overlapped by the retirement unit 854 to illustrate various ways in which register renaming and out-of-order execution may be implemented (e.g., using a reorder buffer(s) and a retirement register file(s); using a future file(s), a history buffer(s), and a retirement register file(s); using a register maps and a pool of registers; etc.). The retirement unit 854 and the physical register file(s) unit(s) 858 are coupled to the execution cluster(s) 860. The execution cluster(s) 860 includes a set of one or more execution units 862 and a set of one or more memory access units 864. The execution units 862 may perform various operations (e.g., shifts, addition, subtraction, multiplication) and on various types of data (e.g., scalar floating point, packed integer, packed floating point, vector integer, vector floating point). While some embodiments may include a number of execution units dedicated to specific functions or sets of functions, other embodiments may include only one execution unit or multiple execution units that all perform all functions. The scheduler unit(s) 856, physical register file(s) unit(s) 858, and execution cluster(s) 860

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are shown as being possibly plural because certain embodiments create separate pipelines for certain types of data/operations (e.g., a scalar integer pipeline, a scalar floating point/packed integer/packed floating point/vector integer/vector floating point pipeline, and/or a memory access pipeline that each have their own scheduler unit, physical register file(s) unit, and/or execution cluster – and in the case of a separate memory access pipeline, certain embodiments are implemented in which only the execution cluster of this pipeline has the memory access unit(s) 864). It should also be understood that where separate pipelines are used, one or more of these pipelines may be out-of-order issue/execution and the rest in-order.

[0080] The set of memory access units 864 is coupled to the memory unit 870, which includes a data TLB unit 872 coupled to a data cache unit 874 coupled to a level 2 (L2) cache unit 876. In one exemplary embodiment, the memory access units 864 may include a load unit, a store address unit, and a store data unit, each of which is coupled to the data TLB unit 872 in the memory unit 870. The instruction cache unit 834 is further coupled to a level 2 (L2) cache unit 876 in the memory unit 870. The L2 cache unit 876 is coupled to one or more other levels of cache and eventually to a main memory.

[0081] By way of example, the exemplary register renaming, out-of-order issue/execution core architecture may implement the pipeline 800 as follows: 1) the instruction fetch 838 performs the fetch and length decoding stages 802 and 804; 2) the decode unit 840 performs the decode stage 806; 3) the rename/allocator unit 852 performs the allocation stage 808 and renaming stage 810; 4) the scheduler unit(s) 856 performs the schedule stage 812; 5) the physical register file(s) unit(s) 858 and the memory unit 870 perform the register read/memory read stage 814; the execution cluster 860 perform the execute stage 816; 6) the memory unit 870 and the physical register file(s) unit(s) 858 perform the write back/memory write stage 818; 7) various units may be involved in the exception handling stage 822; and 8) the retirement unit 854 and the physical register file(s) unit(s) 858 perform the commit stage 824.

[0082] The core 890 may support one or more instructions sets (e.g., the x86 instruction set (with some extensions that have been added with newer versions); the MIPS instruction set of MIPS Technologies of Sunnyvale, CA; the ARM instruction set (with optional additional extensions such as NEON) of ARM Holdings of Sunnyvale, CA),

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including the instruction(s) described herein. In one embodiment, the core 890 includes logic to support a packed data instruction set extension (e.g., AVX1, AVX2), thereby allowing the operations used by many multimedia applications to be performed using packed data.

[0083] It should be understood that the core may support multithreading (executing two or more parallel sets of operations or threads), and may do so in a variety of ways including time sliced multithreading, simultaneous multithreading (where a single physical core provides a logical core for each of the threads that physical core is simultaneously multithreading), or a combination thereof (e.g., time sliced fetching and decoding and simultaneous multithreading thereafter such as in the Intel® Hyperthreading technology).

[0084] While register renaming is described in the context of out-of-order execution, it should be understood that register renaming may be used in an in-order architecture. While the illustrated embodiment of the processor also includes separate instruction and data cache units 834/874 and a shared L2 cache unit 876, alternative embodiments may have a single internal cache for both instructions and data, such as, for example, a Level 1 (L1) internal cache, or multiple levels of internal cache. In some embodiments, the system may include a combination of an internal cache and an external cache that is external to the core and/or the processor. Alternatively, all of the cache may be external to the core and/or the processor.

Specific Exemplary In-Order Core Architecture

[0085] Figures 9A-B illustrate a block diagram of a more specific exemplary in-order core architecture, which core would be one of several logic blocks (including other cores of the same type and/or different types) in a chip. The logic blocks communicate through a high-bandwidth interconnect network (e.g., a ring network) with some fixed function logic, memory I/O interfaces, and other necessary I/O logic, depending on the application.

[0086] Figure 9A is a block diagram of a single processor core, along with its connection to the on-die interconnect network 902 and with its local subset of the Level 2 (L2) cache 904, according to embodiments of the invention. In one embodiment, an instruction decoder 900 supports the x86 instruction set with a packed data instruction set extension.

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An L1 cache 906 allows low-latency accesses to cache memory into the scalar and vector units. While in one embodiment (to simplify the design), a scalar unit 908 and a vector unit 910 use separate register sets (respectively, scalar registers 912 and vector registers 914) and data transferred between them is written to memory and then read back in from a level 1 (L1) cache 906, alternative embodiments of the invention may use a different approach (e.g., use a single register set or include a communication path that allow data to be transferred between the two register files without being written and read back).

[0087] The local subset of the L2 cache 904 is part of a global L2 cache that is divided into separate local subsets, one per processor core. Each processor core has a direct access path to its own local subset of the L2 cache 904. Data read by a processor core is stored in its L2 cache subset 904 and can be accessed quickly, in parallel with other processor cores accessing their own local L2 cache subsets. Data written by a processor core is stored in its own L2 cache subset 904 and is flushed from other subsets, if necessary. The ring network ensures coherency for shared data. The ring network is bi-directional to allow agents such as processor cores, L2 caches and other logic blocks to communicate with each other within the chip. Each ring data-path is 1012-bits wide per direction.

[0088] Figure 9B is an expanded view of part of the processor core in **Figure 9A** according to embodiments of the invention. **Figure 9B** includes an L1 data cache 906A part of the L1 cache 904, as well as more detail regarding the vector unit 910 and the vector registers 914. Specifically, the vector unit 910 is a 16-wide vector processing unit (VPU) (see the 16-wide ALU 928), which executes one or more of integer, single-precision float, and double-precision float instructions. The VPU supports swizzling the register inputs with swizzle unit 920, numeric conversion with numeric convert units 922A-B, and replication with replication unit 924 on the memory input. Write mask registers 926 allow predicating resulting vector writes.

Processor with integrated memory controller and graphics

[0089] Figure 10 is a block diagram of a processor 1000 that may have more than one core, may have an integrated memory controller, and may have integrated graphics according to embodiments of the invention. The solid lined boxes in **Figure 10** illustrate a processor 1000 with a single core 1002A, a system agent 1010, a set of one or more bus

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controller units 1016, while the optional addition of the dashed lined boxes illustrates an alternative processor 1000 with multiple cores 1002A-N, a set of one or more integrated memory controller unit(s) 1014 in the system agent unit 1010, and special purpose logic 1008.

[0090] Thus, different implementations of the processor 1000 may include: 1) a CPU with the special purpose logic 1008 being integrated graphics and/or scientific (throughput) logic (which may include one or more cores), and the cores 1002A-N being one or more general purpose cores (e.g., general purpose in-order cores, general purpose out-of-order cores, a combination of the two); 2) a coprocessor with the cores 1002A-N being a large number of special purpose cores intended primarily for graphics and/or scientific (throughput); and 3) a coprocessor with the cores 1002A-N being a large number of general purpose in-order cores. Thus, the processor 1000 may be a general-purpose processor, coprocessor or special-purpose processor, such as, for example, a network or communication processor, compression engine, graphics processor, GPGPU (general purpose graphics processing unit), a high-throughput many integrated core (MIC) coprocessor (including 30 or more cores), embedded processor, or the like. The processor may be implemented on one or more chips. The processor 1000 may be a part of and/or may be implemented on one or more substrates using any of a number of process technologies, such as, for example, BiCMOS, CMOS, or NMOS.

[0091] The memory hierarchy includes one or more levels of cache within the cores, a set or one or more shared cache units 1006, and external memory (not shown) coupled to the set of integrated memory controller units 1014. The set of shared cache units 1006 may include one or more mid-level caches, such as level 2 (L2), level 3 (L3), level 4 (L4), or other levels of cache, a last level cache (LLC), and/or combinations thereof. While in one embodiment a ring based interconnect unit 1012 interconnects the integrated graphics logic 1008, the set of shared cache units 1006, and the system agent unit 1010/integrated memory controller unit(s) 1014, alternative embodiments may use any number of well-known techniques for interconnecting such units. In one embodiment, coherency is maintained between one or more cache units 1006 and cores 1002-A-N.

[0092] In some embodiments, one or more of the cores 1002A-N are capable of multi-threading. The system agent 1010 includes those components coordinating and

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operating cores 1002A-N. The system agent unit 1010 may include for example a power control unit (PCU) and a display unit. The PCU may be or include logic and components needed for regulating the power state of the cores 1002A-N and the integrated graphics logic 1008. The display unit is for driving one or more externally connected displays.

[0093] The cores 1002A-N may be homogenous or heterogeneous in terms of architecture instruction set; that is, two or more of the cores 1002A-N may be capable of execution the same instruction set, while others may be capable of executing only a subset of that instruction set or a different instruction set.

Exemplary Computer Architectures

[0094] **Figures 11-14** are block diagrams of exemplary computer architectures. Other system designs and configurations known in the arts for laptops, desktops, handheld PCs, personal digital assistants, engineering workstations, servers, network devices, network hubs, switches, embedded processors, digital signal processors (DSPs), graphics devices, video game devices, set-top boxes, micro controllers, cell phones, portable media players, hand held devices, and various other electronic devices, are also suitable. In general, a huge variety of systems or electronic devices capable of incorporating a processor and/or other execution logic as disclosed herein are generally suitable.

[0095] Referring now to **Figure 11**, shown is a block diagram of a system 1100 in accordance with one embodiment of the present invention. The system 1100 may include one or more processors 1110, 1115, which are coupled to a controller hub 1120. In one embodiment the controller hub 1120 includes a graphics memory controller hub (GMCH) 1190 and an Input/Output Hub (IOH) 1150 (which may be on separate chips); the GMCH 1190 includes memory and graphics controllers to which are coupled memory 1140 and a coprocessor 1145; the IOH 1150 is couples input/output (I/O) devices 1160 to the GMCH 1190. Alternatively, one or both of the memory and graphics controllers are integrated within the processor (as described herein), the memory 1140 and the coprocessor 1145 are coupled directly to the processor 1110, and the controller hub 1120 in a single chip with the IOH 1150.

[0096] The optional nature of additional processors 1115 is denoted in **Figure 11** with broken lines. Each processor 1110, 1115 may include one or more of the processing cores described herein and may be some version of the processor 1000.

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[0097] The memory 1140 may be, for example, dynamic random access memory (DRAM), phase change memory (PCM), or a combination of the two. For at least one embodiment, the controller hub 1120 communicates with the processor(s) 1110, 1115 via a multi-drop bus, such as a frontside bus (FSB), point-to-point interface such as QuickPath Interconnect (QPI), or similar connection 1195.

[0098] In one embodiment, the coprocessor 1145 is a special-purpose processor, such as, for example, a high-throughput MIC processor, a network or communication processor, compression engine, graphics processor, GPGPU, embedded processor, or the like. In one embodiment, controller hub 1120 may include an integrated graphics accelerator.

[0099] There can be a variety of differences between the physical resources 1110, 1115 in terms of a spectrum of metrics of merit including architectural, microarchitectural, thermal, power consumption characteristics, and the like.

[00100] In one embodiment, the processor 1110 executes instructions that control data processing operations of a general type. Embedded within the instructions may be coprocessor instructions. The processor 1110 recognizes these coprocessor instructions as being of a type that should be executed by the attached coprocessor 1145. Accordingly, the processor 1110 issues these coprocessor instructions (or control signals representing coprocessor instructions) on a coprocessor bus or other interconnect, to coprocessor 1145. Coprocessor(s) 1145 accept and execute the received coprocessor instructions.

[00101] Referring now to **Figure 12**, shown is a block diagram of a first more specific exemplary system 1200 in accordance with an embodiment of the present invention. As shown in **Figure 12**, multiprocessor system 1200 is a point-to-point interconnect system, and includes a first processor 1270 and a second processor 1280 coupled via a point-to-point interconnect 1250. Each of processors 1270 and 1280 may be some version of the processor 1000. In one embodiment of the invention, processors 1270 and 1280 are respectively processors 1110 and 1115, while coprocessor 1238 is coprocessor 1145. In another embodiment, processors 1270 and 1280 are respectively processor 1110 coprocessor 1145.

[00101] Processors 1270 and 1280 are shown including integrated memory controller (IMC) units 1272 and 1282, respectively. Processor 1270 also includes as part

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of its bus controller units point-to-point (P-P) interfaces 1276 and 1278; similarly, second processor 1280 includes P-P interfaces 1286 and 1288. Processors 1270, 1280 may exchange information via a point-to-point (P-P) interface 1250 using P-P interface circuits 1278, 1288. As shown in **Figure 12**, IMCs 1272 and 1282 couple the processors to respective memories, namely a memory 1232 and a memory 1234, which may be portions of main memory locally attached to the respective processors.

[00102] Processors 1270, 1280 may each exchange information with a chipset 1290 via individual P-P interfaces 1252, 1254 using point to point interface circuits 1276, 1294, 1286, 1298. Chipset 1290 may optionally exchange information with the coprocessor 1238 via a high-performance interface 1239. In one embodiment, the coprocessor 1238 is a special-purpose processor, such as, for example, a high-throughput MIC processor, a network or communication processor, compression engine, graphics processor, GPGPU, embedded processor, or the like.

[00103] A shared cache (not shown) may be included in either processor or outside of both processors, yet connected with the processors via P-P interconnect, such that either or both processors' local cache information may be stored in the shared cache if a processor is placed into a low power mode.

[00104] Chipset 1290 may be coupled to a first bus 1216 via an interface 1296. In one embodiment, first bus 1216 may be a Peripheral Component Interconnect (PCI) bus, or a bus such as a PCI Express bus or another third generation I/O interconnect bus, although the scope of the present invention is not so limited.

[00105] As shown in **Figure 12**, various I/O devices 1214 may be coupled to first bus 1216, along with a bus bridge 1218 which couples first bus 1216 to a second bus 1220. In one embodiment, one or more additional processor(s) 1215, such as coprocessors, high-throughput MIC processors, GPGPU's, accelerators (such as, e.g., graphics accelerators or digital signal processing (DSP) units), field programmable gate arrays, or any other processor, are coupled to first bus 1216. In one embodiment, second bus 1220 may be a low pin count (LPC) bus. Various devices may be coupled to a second bus 1220 including, for example, a keyboard and/or mouse 1222, communication devices 1227 and a storage unit 1228 such as a disk drive or other mass storage device which may include instructions/code and data 1230, in one embodiment. Further, an

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audio I/O 1224 may be coupled to the second bus 1220. Note that other architectures are possible. For example, instead of the point-to-point architecture of **Figure 12**, a system may implement a multi-drop bus or other such architecture.

[00106] Referring now to **Figure 13**, shown is a block diagram of a second more specific exemplary system 1300 in accordance with an embodiment of the present invention. Like elements in **Figures 12** and **13** bear like reference numerals, and certain aspects of **Figure 12** have been omitted from **Figure 13** in order to avoid obscuring other aspects of **Figure 13**.

[00107] **Figure 13** illustrates that the processors 1270, 1280 may include integrated memory and I/O control logic ("CL") 1272 and 1282, respectively. Thus, the CL 1272, 1282 include integrated memory controller units and include I/O control logic. **Figure 13** illustrates that not only are the memories 1232, 1234 coupled to the CL 1272, 1282, but also that I/O devices 1314 are also coupled to the control logic 1272, 1282. Legacy I/O devices 1315 are coupled to the chipset 1290.

[00108] Referring now to **Figure 14**, shown is a block diagram of a SoC 1400 in accordance with an embodiment of the present invention. Similar elements in **Figure 10** bear like reference numerals. Also, dashed lined boxes are optional features on more advanced SoCs. In **Figure 14**, an interconnect unit(s) 1402 is coupled to: an application processor 1410 which includes a set of one or more cores 202A-N and shared cache unit(s) 1006; a system agent unit 1010; a bus controller unit(s) 1016; an integrated memory controller unit(s) 1014; a set or one or more coprocessors 1420 which may include integrated graphics logic, an image processor, an audio processor, and a video processor; an static random access memory (SRAM) unit 1430; a direct memory access (DMA) unit 1432; and a display unit 1440 for coupling to one or more external displays. In one embodiment, the coprocessor(s) 1420 include a special-purpose processor, such as, for example, a network or communication processor, compression engine, GPGPU, a high-throughput MIC processor, embedded processor, or the like.

[00109] Embodiments of the mechanisms disclosed herein may be implemented in hardware, software, firmware, or a combination of such implementation approaches. Embodiments of the invention may be implemented as computer programs or program code executing on programmable systems comprising at least one processor, a storage

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system (including volatile and non-volatile memory and/or storage elements), at least one input device, and at least one output device.

[00110] Program code, such as code 1230 illustrated in **Figure 12**, may be applied to input instructions to perform the functions described herein and generate output information. The output information may be applied to one or more output devices, in known fashion. For purposes of this application, a processing system includes any system that has a processor, such as, for example; a digital signal processor (DSP), a microcontroller, an application specific integrated circuit (ASIC), or a microprocessor.

[00111] The program code may be implemented in a high level procedural or object oriented programming language to communicate with a processing system. The program code may also be implemented in assembly or machine language, if desired. In fact, the mechanisms described herein are not limited in scope to any particular programming language. In any case, the language may be a compiled or interpreted language.

[00112] One or more aspects of at least one embodiment may be implemented by representative instructions stored on a machine-readable medium which represents various logic within the processor, which when read by a machine causes the machine to fabricate logic to perform the techniques described herein. Such representations, known as "IP cores" may be stored on a tangible, machine readable medium and supplied to various customers or manufacturing facilities to load into the fabrication machines that actually make the logic or processor.

[00113] Such machine-readable storage media may include, without limitation, non-transitory, tangible arrangements of articles manufactured or formed by a machine or device, including storage media such as hard disks, any other type of disk including floppy disks, optical disks, compact disk read-only memories (CD-ROMs), compact disk rewritable's (CD-RWs), and magneto-optical disks, semiconductor devices such as read-only memories (ROMs), random access memories (RAMs) such as dynamic random access memories (DRAMs), static random access memories (SRAMs), erasable programmable read-only memories (EPROMs), flash memories, electrically erasable programmable read-only memories (EEPROMs), phase change memory (PCM),

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magnetic or optical cards, or any other type of media suitable for storing electronic instructions.

[00114] Accordingly, embodiments of the invention also include non-transitory, tangible machine-readable media containing instructions or containing design data, such as Hardware Description Language (HDL), which defines structures, circuits, apparatuses, processors and/or system features described herein. Such embodiments may also be referred to as program products.

Emulation (including binary translation, code morphing, etc.)

[00115] In some cases, an instruction converter may be used to convert an instruction from a source instruction set to a target instruction set. For example, the instruction converter may translate (e.g., using static binary translation, dynamic binary translation including dynamic compilation), morph, emulate, or otherwise convert an instruction to one or more other instructions to be processed by the core. The instruction converter may be implemented in software, hardware, firmware, or a combination thereof. The instruction converter may be on processor, off processor, or part on and part off processor.

[00116] **Figure 15** is a block diagram contrasting the use of a software instruction converter to convert binary instructions in a source instruction set to binary instructions in a target instruction set according to embodiments of the invention. In the illustrated embodiment, the instruction converter is a software instruction converter, although alternatively the instruction converter may be implemented in software, firmware, hardware, or various combinations thereof. **Figure 15** shows a program in a high level language 1502 may be compiled using an x86 compiler 1504 to generate x86 binary code 1506 that may be natively executed by a processor with at least one x86 instruction set core 1516. The processor with at least one x86 instruction set core 1516 represents any processor that can perform substantially the same functions as an Intel processor with at least one x86 instruction set core by compatibly executing or otherwise processing (1) a substantial portion of the instruction set of the Intel x86 instruction set core or (2) object code versions of applications or other software targeted to run on an Intel processor with at least one x86 instruction set core, in order to achieve substantially the same result as an Intel processor with at least one x86 instruction set core. The x86 compiler 1504

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represents a compiler that is operable to generate x86 binary code 1506 (e.g., object code) that can, with or without additional linkage processing, be executed on the processor with at least one x86 instruction set core 1516. Similarly, **Figure 15** shows the program in the high level language 1502 may be compiled using an alternative instruction set compiler 1508 to generate alternative instruction set binary code 1510 that may be natively executed by a processor without at least one x86 instruction set core 1514 (e.g., a processor with cores that execute the MIPS instruction set of MIPS Technologies of Sunnyvale, CA and/or that execute the ARM instruction set of ARM Holdings of Sunnyvale, CA). The instruction converter 1512 is used to convert the x86 binary code 1506 into code that may be natively executed by the processor without an x86 instruction set core 1514. This converted code is not likely to be the same as the alternative instruction set binary code 1510 because an instruction converter capable of this is difficult to make; however, the converted code will accomplish the general operation and be made up of instructions from the alternative instruction set. Thus, the instruction converter 1512 represents software, firmware, hardware, or a combination thereof that, through emulation, simulation or any other process, allows a processor or other electronic device that does not have an x86 instruction set processor or core to execute the x86 binary code 1506.

[00117] In the description and claims, the term "logic" may have been used. As used herein, the term logic may include but is not limited to hardware, firmware, software, or a combination thereof. Examples of logic include integrated circuitry, application specific integrated circuits, analog circuits, digital circuits, programmed logic devices, memory devices including instructions, etc. In some embodiments, the logic may include transistors and/or gates potentially along with other circuitry components.

[00118] In the description and claims, the terms "coupled" and "connected," along with their derivatives, may have been used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or

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more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

[00119] The term "and/or" may have been used. As used herein, the term "and/or" means one or the other or both (e.g., A and/or B means A or B or both A and B).

[00120] In the description above, for the purposes of explanation, numerous specific details have been set forth in order to provide a thorough understanding of the embodiments of the invention. It will be apparent however, to one skilled in the art, that one or more other embodiments may be practiced without some of these specific details. The particular embodiments described are not provided to limit the invention but to illustrate it. The scope of the invention is not to be determined by the specific examples provided above but only by the claims below. All equivalent relationships to those illustrated in the drawings and described in the specification are encompassed within embodiments of the invention. In other instances, well-known circuits, structures, devices, and operations have been shown in block diagram form or without detail in order to avoid obscuring the understanding of the description.

[00121] Where considered appropriate, reference numerals have been repeated among the figures to indicate components that may optionally be substantially the same and have similar characteristics. In other instances, terminal portions of reference numerals have been repeated among the figures to indicate corresponding or analogous elements, which may optionally have similar or the same characteristics unless specified or clearly apparent otherwise. In some cases, where multiple components have been shown and described, they may be incorporated into a single component. In other cases, where a single component has been shown and described, it may be separated into two or more components. In the drawings, arrows represent couplings and bidirectional arrows represent bidirectional couplings.

[00122] Various operations and methods have been described. Some of the methods have been described in a relatively basic form in the flow diagrams, but operations may optionally be added to and/or removed from the methods. In addition, while the flow diagrams show a particular order of the operations according to example embodiments, it is to be understood that that particular order is exemplary. Alternate

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embodiments may optionally perform the operations in different order, combine certain operations, overlap certain operations, etc. The components, features, and specific optional details described herein for an apparatus also optionally apply to the methods described herein which may in embodiments be performed by and/or with such an apparatus.

[00123] Some embodiments include an article of manufacture (e.g., a computer program product) that includes a machine-readable medium. The medium may include a mechanism that provides, for example stores, information in a form that is readable by the machine. The machine-readable medium may provide, or have stored thereon, one or more, or a sequence of instructions, that if executed by a machine causes the machine to perform and/or results in the machine performing one or operations, methods, or techniques disclosed herein. In some embodiments, the machine-readable medium may include a tangible non-transitory machine-readable storage media. For example, the tangible non-transitory machine-readable storage media may include a floppy diskette, an optical storage medium, an optical disk, a CD-ROM, a magnetic disk, a magneto-optical disk, a read only memory (ROM), a programmable ROM (PROM), an erasable-and-programmable ROM (EPROM), an electrically-erasable-and-programmable ROM (EEPROM), a random access memory (RAM), a static-RAM (SRAM), a dynamic-RAM (DRAM), a Flash memory, a phase-change memory, or the like. The tangible medium may include one or more solid or tangible physical materials, such as, for example, a semiconductor material, a phase change material, a magnetic material, etc. In another embodiment, the machine-readable media may include a non-tangible transitory machine-readable communication medium, for example, the electrical, optical, acoustical or other forms of propagated signals, such as carrier waves, infrared signals, digital signals, etc.

[00124] Examples of suitable machines include, but are not limited to, computer systems, desktops, laptops, notebooks, netbooks, nettops, Mobile Internet devices (MIDs), servers, network elements (e.g., routers, switches, etc.) cellular phones, media players, nettops, set-top boxes, video game controllers, and other electronic devices having one or more processors or other instruction execution apparatus. Such electronic devices typically include one or more processors coupled with one or more other

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components, such as one or more storage devices (non-transitory machine-readable storage media), user input/output devices (e.g., a keyboard, a touchscreen, and/or a display), and/or network connections. The coupling of the processors and other components is typically through one or more busses and bridges (also termed bus controllers). Thus, the storage device of a given electronic device may store code and/or data for execution on the one or more processors of that electronic device. Alternatively, one or more parts of an embodiment of the invention may be implemented using different combinations of software, firmware, and/or hardware.

[00125] It should also be appreciated that reference throughout this specification to "one embodiment", "an embodiment", or “one or more embodiments”, for example, means that a particular feature may be included in the practice of the invention. Similarly, it should be appreciated that in the description various features are sometimes grouped together in a single embodiment, Figure, or description thereof for the purpose of streamlining the disclosure and aiding in the understanding of various inventive aspects. This method of disclosure, however, is not to be interpreted as reflecting an intention that the invention requires more features than are expressly recited in each claim. Rather, as the following claims reflect, inventive aspects may lie in less than all features of a single disclosed embodiment. Thus, the claims following the Detailed Description are hereby expressly incorporated into this Detailed Description, with each claim standing on its own as a separate embodiment of the invention.

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CLAIMS

What is claimed is:

1. A system comprising:

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem to store the instructions and data, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores;

cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

power management circuitry to enable a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores, the power management circuitry to selectively gate power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions;

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory; and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory.

2. The system of claim 1 wherein the power management circuitry is to selectively gate power to one or more of the first and/or second subsets of the plurality of cores and corresponding cache portions.

3. The system of claim 1 wherein a first core of a first predetermined subset is physically proximate to a first cache portion.

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4. The system of claim 3 further comprising:

a local core-cache interconnect to couple the first core to the first cache portion; and

an on-die interconnect to couple one or more other cores to the first cache portion.

5. The system of claim 4 wherein the local core-cache interconnect and on-die interconnect provide different access latency and/or data throughput to a given cache portion.

6. The system of claim 4 wherein the local core-cache interconnect is to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first cache portion than the on-die interconnect is to provide to the one or more other cores when the one or more other cores access the first cache portion.

7. The system of claim 1 wherein, based on workload on each of the first and second subsets of the plurality of cores, a thread is to be selectively migrated from the first subset to the second subset.

8. The system of claim 1 wherein at least one of the plurality of cores comprises:

an instruction fetch circuit to fetch instructions from a corresponding first level cache or a system memory; and

a decode circuit to decode the instructions; and

an execution circuit comprising a plurality of functional units to execute the instructions.

9. The system of claim 6 wherein the first subset of the plurality of cores form a first virtual processor and the second subset of the plurality of cores form a second virtual processor.

10. The system of claim 9 wherein the execution circuit is to execute instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first subset of the plurality of cores and to form the second virtual processor by combining the second subset of the plurality of cores.

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11. The system of claim 1 further comprising a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components.

12. The system of claim 1 wherein the non-uniform access to the plurality of cache portions by the plurality of cores is based, at least in part, on each cache portion being coupled to a proximate subset of the plurality of cores over a first interconnect having first characteristics and being coupled to a non-proximate subset of the plurality of cores over a second interconnect having second characteristics.

13. A method comprising:

executing instructions and processing data with a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;

storing the instructions and the data in a cache subsystem, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores;

sharing the plurality of cache portions among the plurality of cores;

providing coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

enabling a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores;

selectively gating power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions;

controlling access by the symmetric multi-threaded cores to a first system memory with a first integrated memory controller; and

controlling access by the symmetric multi-threaded cores to a second system memory with a second integrated memory controller.

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14. The method of claim 13 further comprising selectively migrated a thread from the first subset to the second subset based on a workload on each of the first and second subsets of the plurality of cores.

15. The method of claim 13 wherein said providing the non-uniform access to the plurality of cache portions by the plurality of cores is based, at least in part, on each cache portion accessing a proximate subset of the plurality of cores over a first interconnect having first characteristics and accessing a non-proximate subset of the plurality of cores over a second interconnect having second characteristics.

16. The method of claim 13 further comprising forming the first subset of the plurality of cores as a first virtual processor and forming the second subset of the plurality of cores as a second virtual processor.

17. The method of claim 16 further comprising executing instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first subset of the plurality of cores and to form the second virtual processor by combining the second subset of the plurality of cores.

18. The system of claim 1 further comprising transmitting data between the plurality of cores and one or more system components via a Peripheral Component Interface Express (PCIe) interface.

19. A machine comprising:

a processor comprising:

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem to store the instructions and data, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores; and

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cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

an article of manufacture comprising a machine-readable storage medium storing a plurality of instructions, the plurality of instructions, if performed by a machine, to cause the machine to perform operations comprising to:

enable a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores; and

selectively gate power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions;

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory; and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory.

20. The machine of claim 19 further comprising a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components.

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ABSTRACT OF THE DISCLOSURE

A processor of an aspect includes a plurality of logical processors each having one or more corresponding lower level caches. A shared higher level cache is shared by the plurality of logical processors. The shared higher level cache includes a distributed cache slice for each of the logical processors. The processor includes logic to direct an access that misses in one or more lower level caches of a corresponding logical processor to a subset of the distributed cache slices in a virtual cluster that corresponds to the logical processor. Other processors, methods, and systems are also disclosed.

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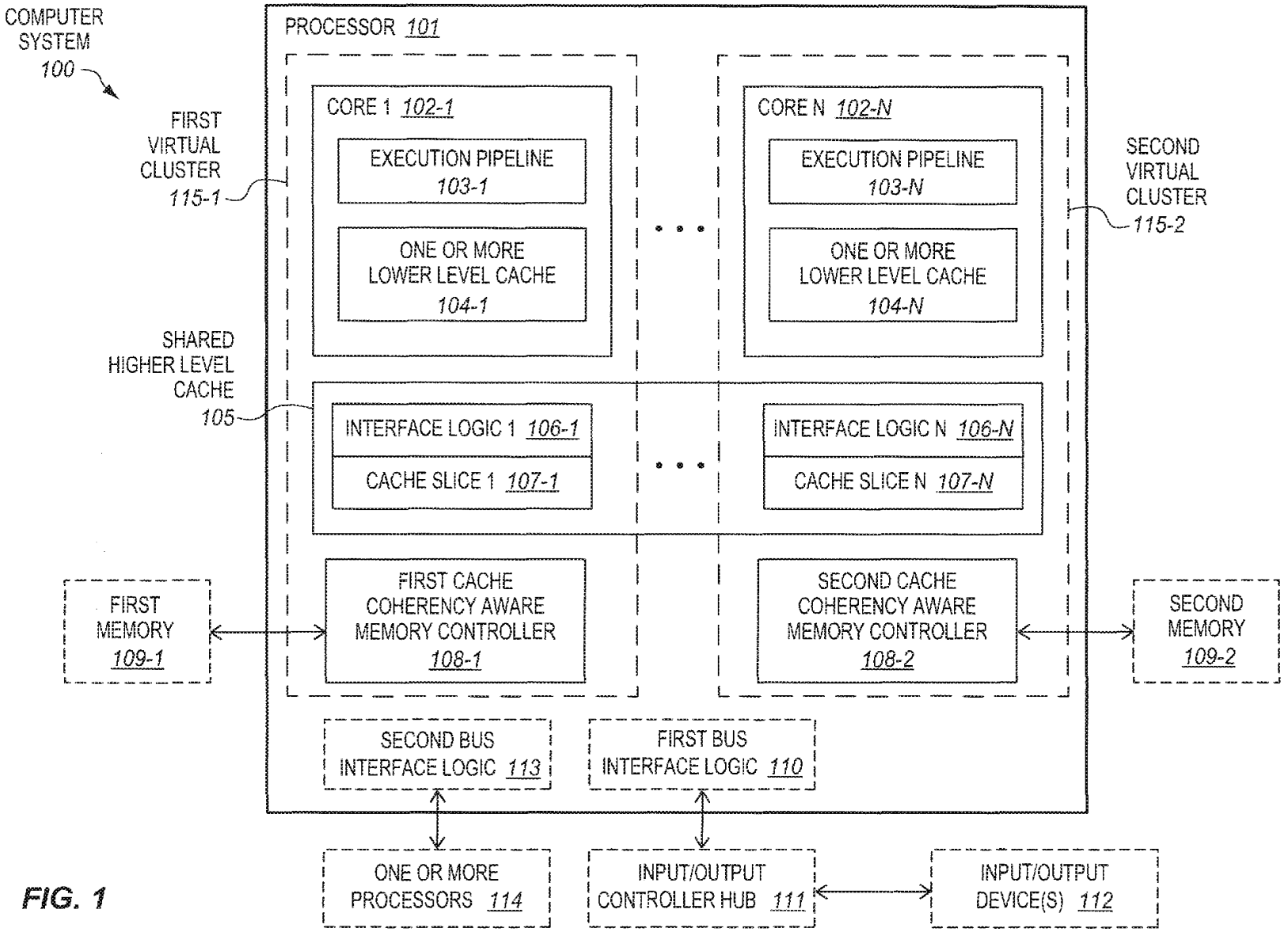


FIG. 1

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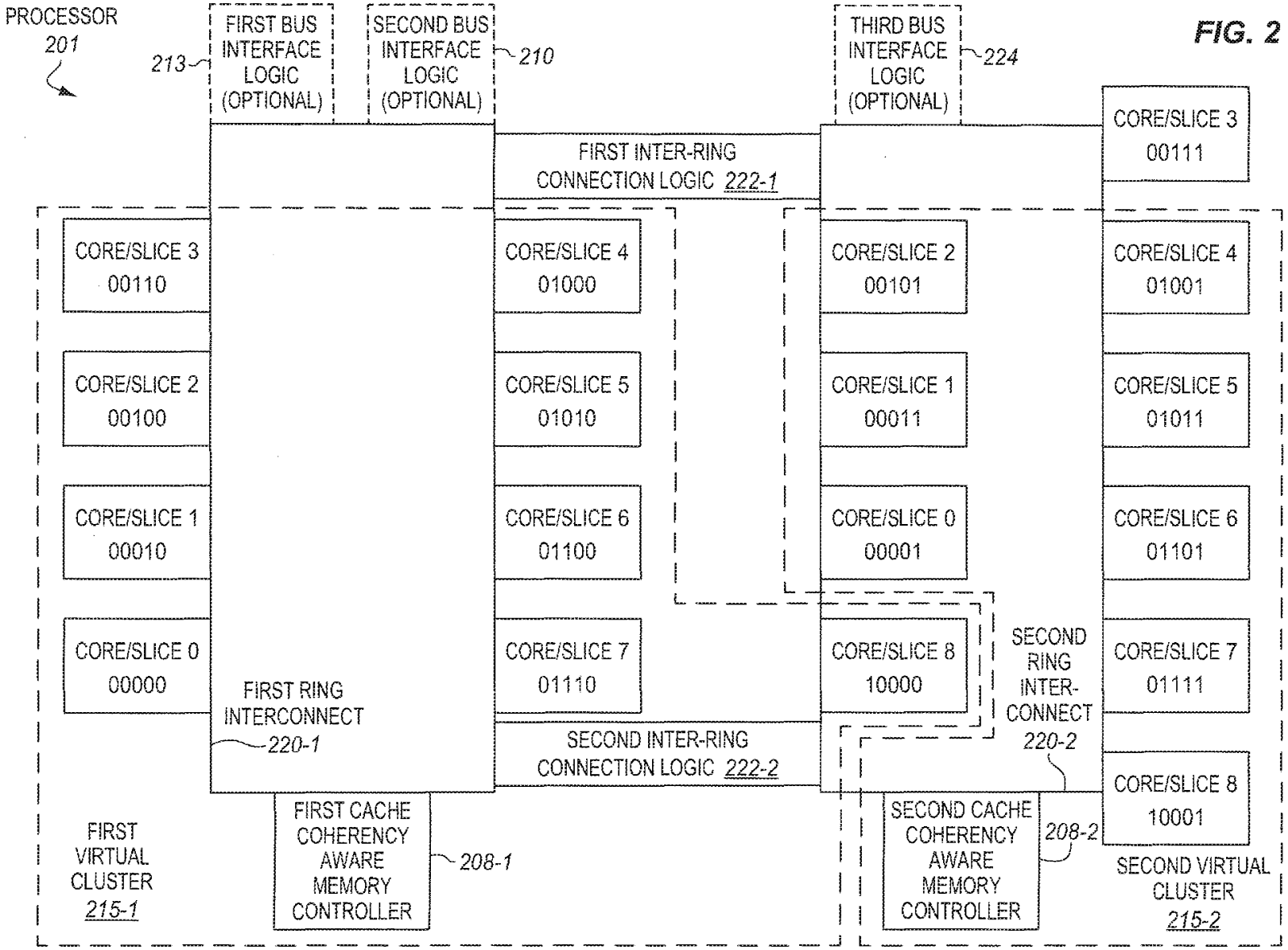


FIG. 2

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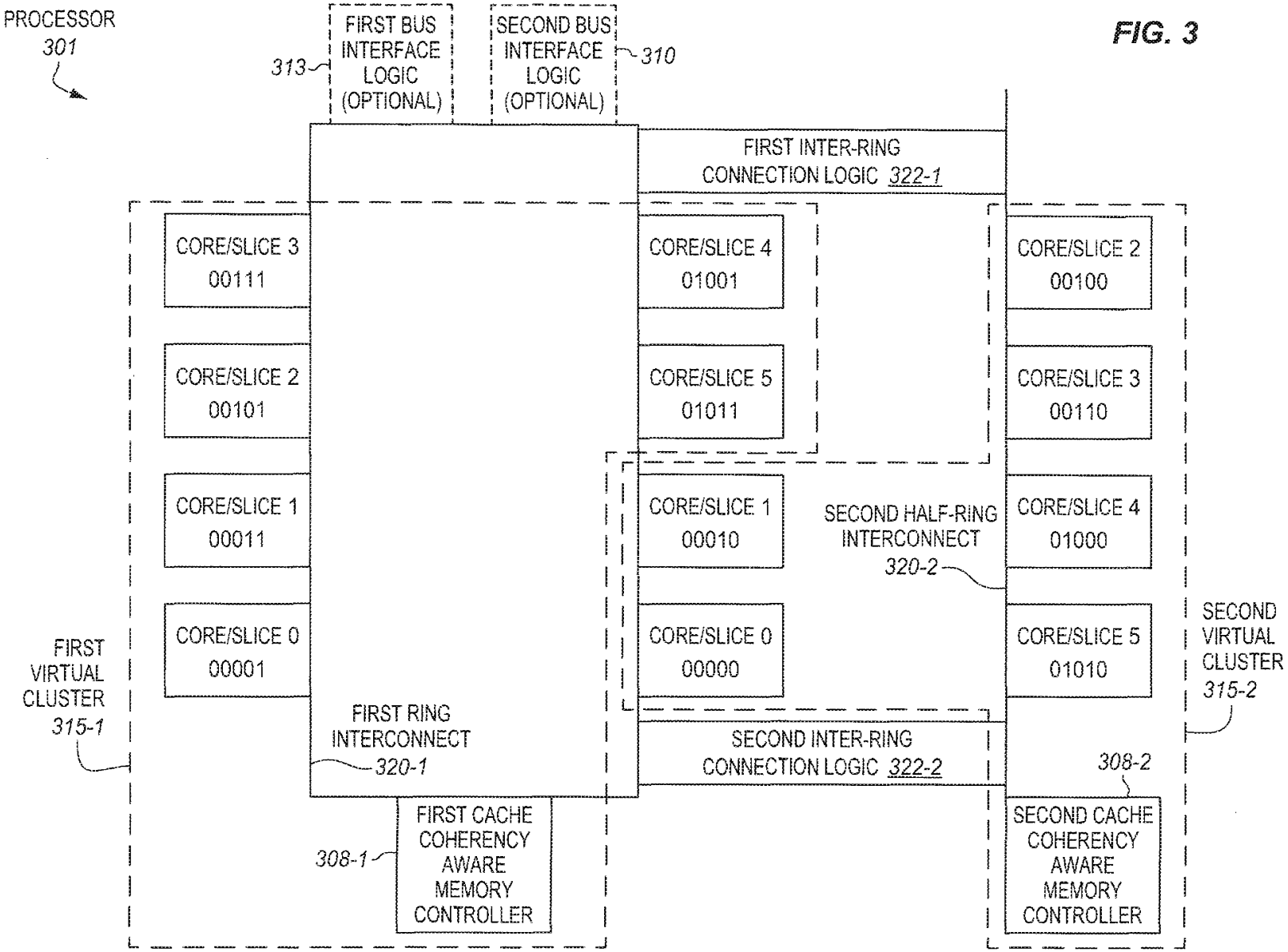


FIG. 3

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FIG. 4

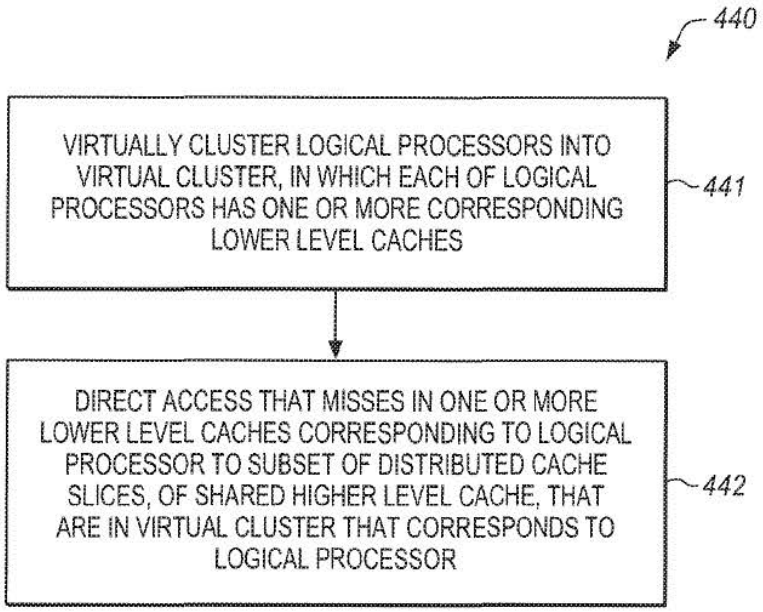
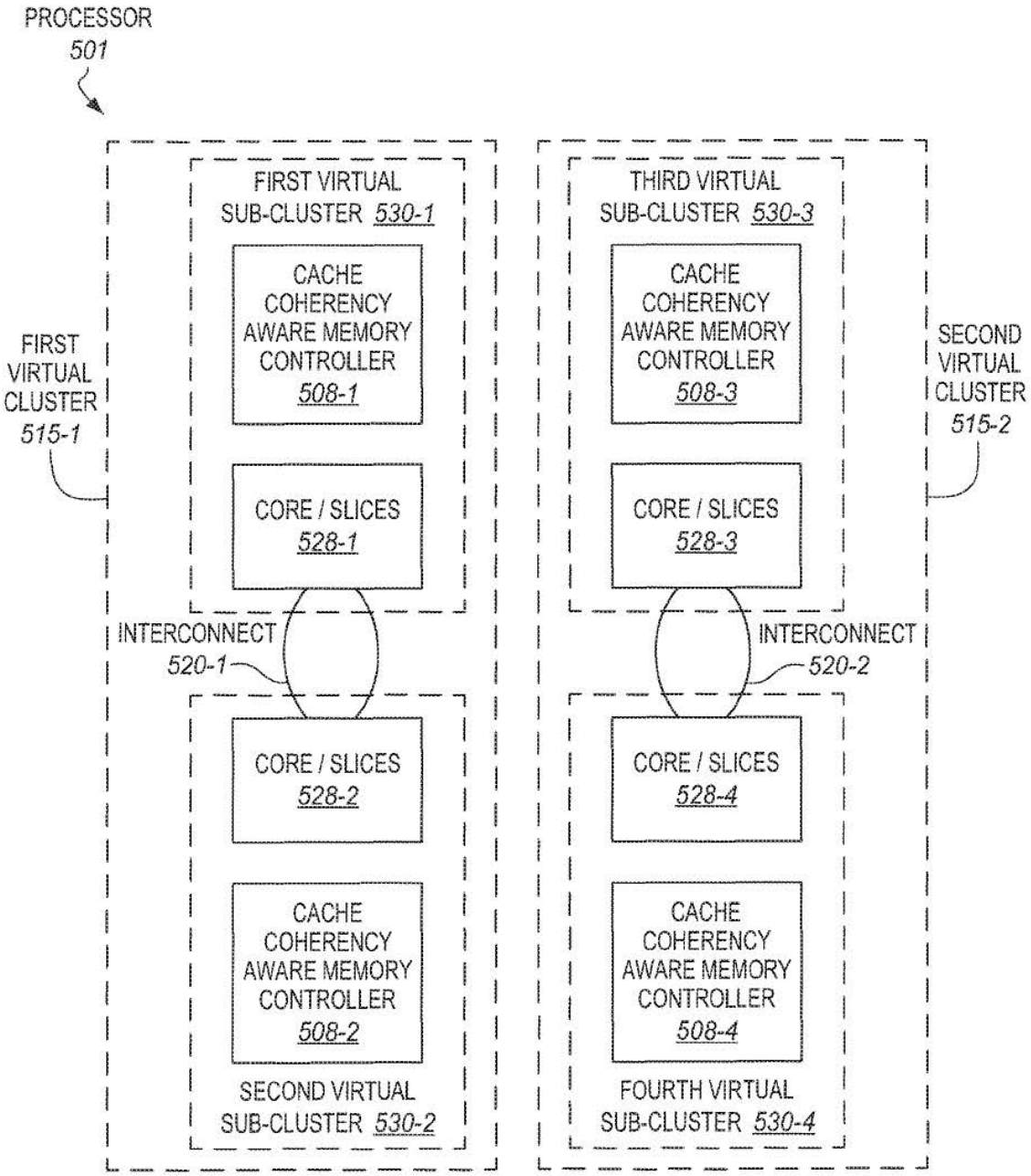

440
VIRTUALLY CLUSTER LOGICAL PROCESSORS INTO VIRTUAL CLUSTER, IN WHICH EACH OF LOGICAL PROCESSORS HAS ONE OR MORE CORRESPONDING LOWER LEVEL CACHES
441
DIRECT ACCESS THAT MISSES IN ONE OR MORE LOWER LEVEL CACHES CORRESPONDING TO LOGICAL PROCESSOR TO SUBSET OF DISTRIBUTED CACHE SLICES, OF SHARED HIGHER LEVEL CACHE, THAT ARE IN VIRTUAL CLUSTER THAT CORRESPONDS TO LOGICAL PROCESSOR
442

FIG. 5



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FIG. 6

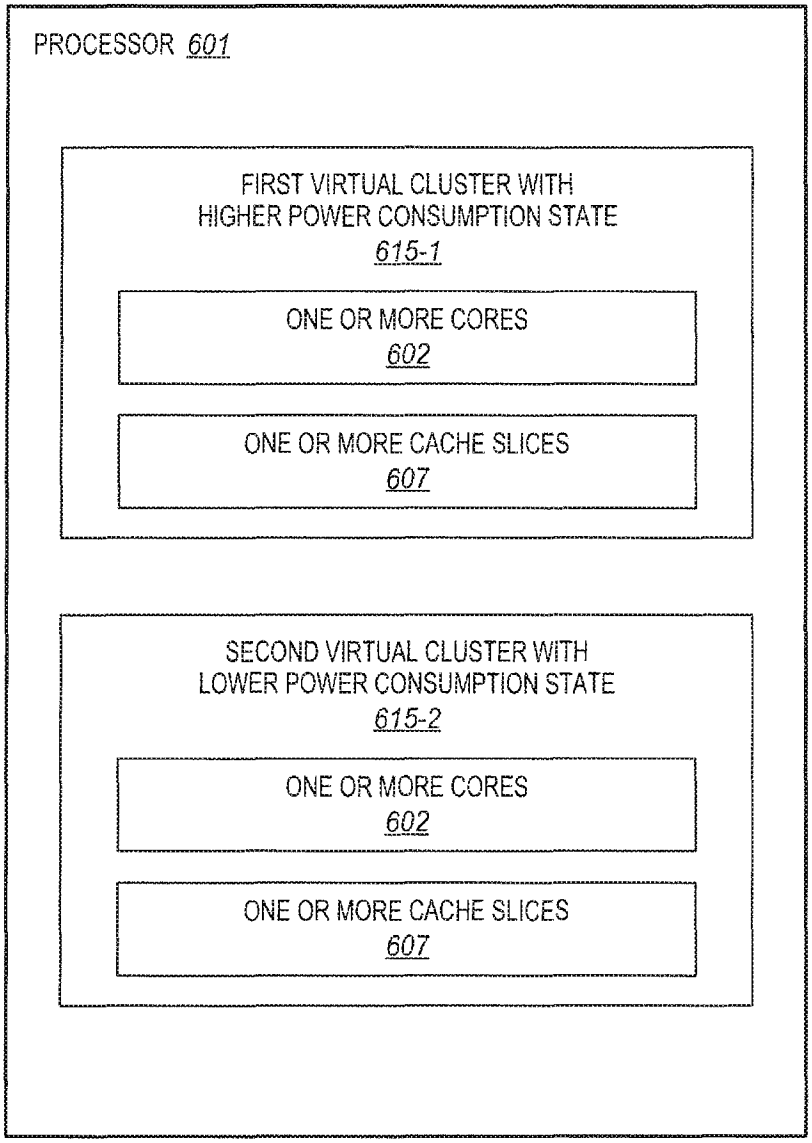
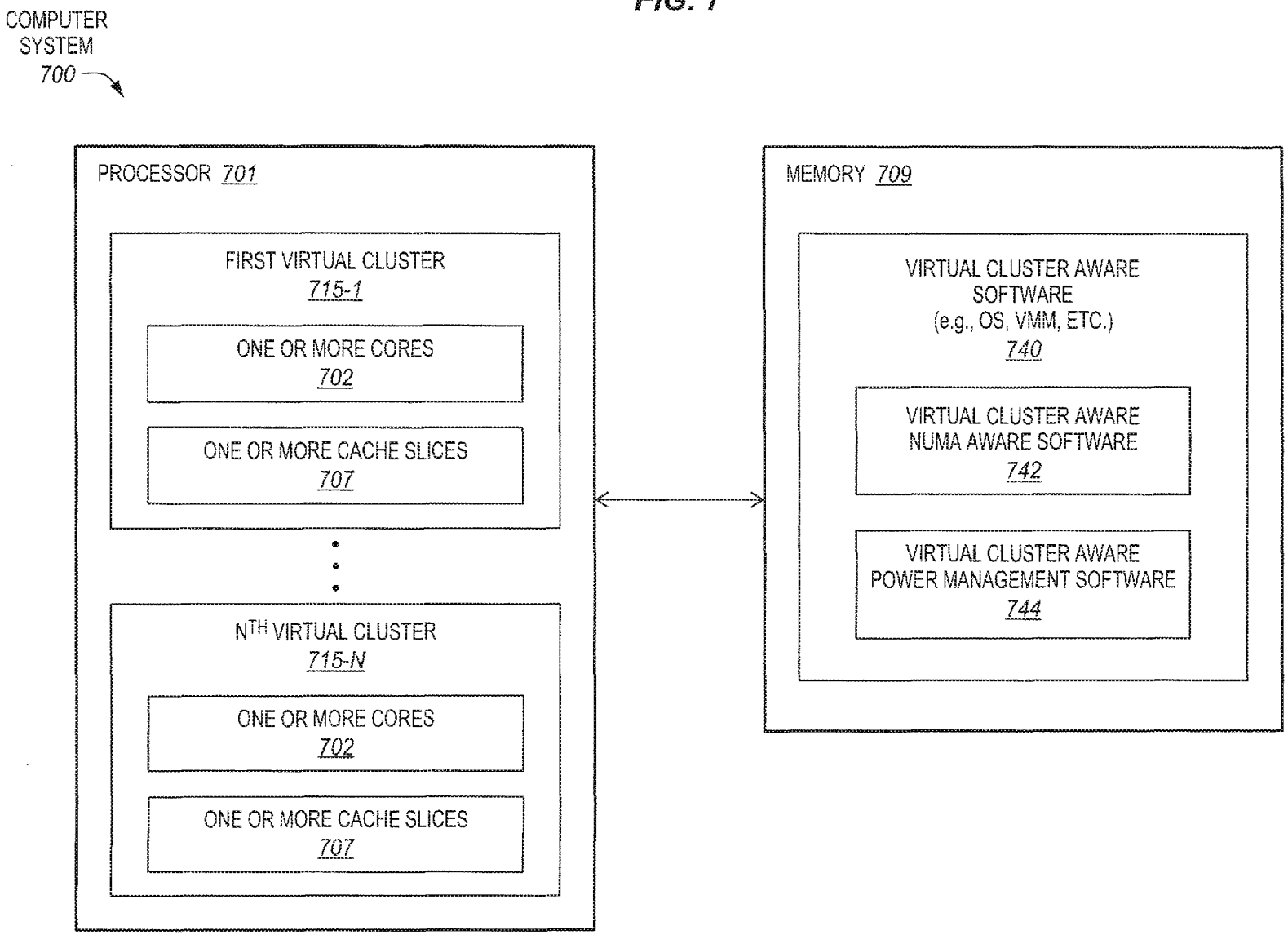

PROCESSOR 601
FIRST VIRTUAL CLUSTER WITH HIGHER POWER CONSUMPTION STATE 615-1
ONE OR MORE CORES 602
ONE OR MORE CACHE SLICES 607
SECOND VIRTUAL CLUSTER WITH LOWER POWER CONSUMPTION STATE 615-2
ONE OR MORE CORES 602
ONE OR MORE CACHE SLICES 607

FIG. 7



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FIG. 8A

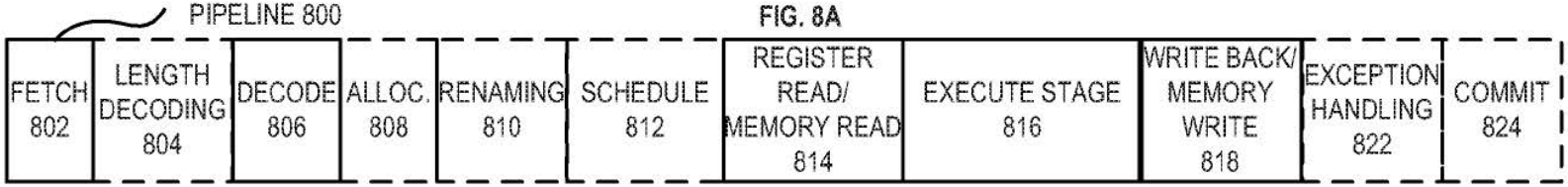
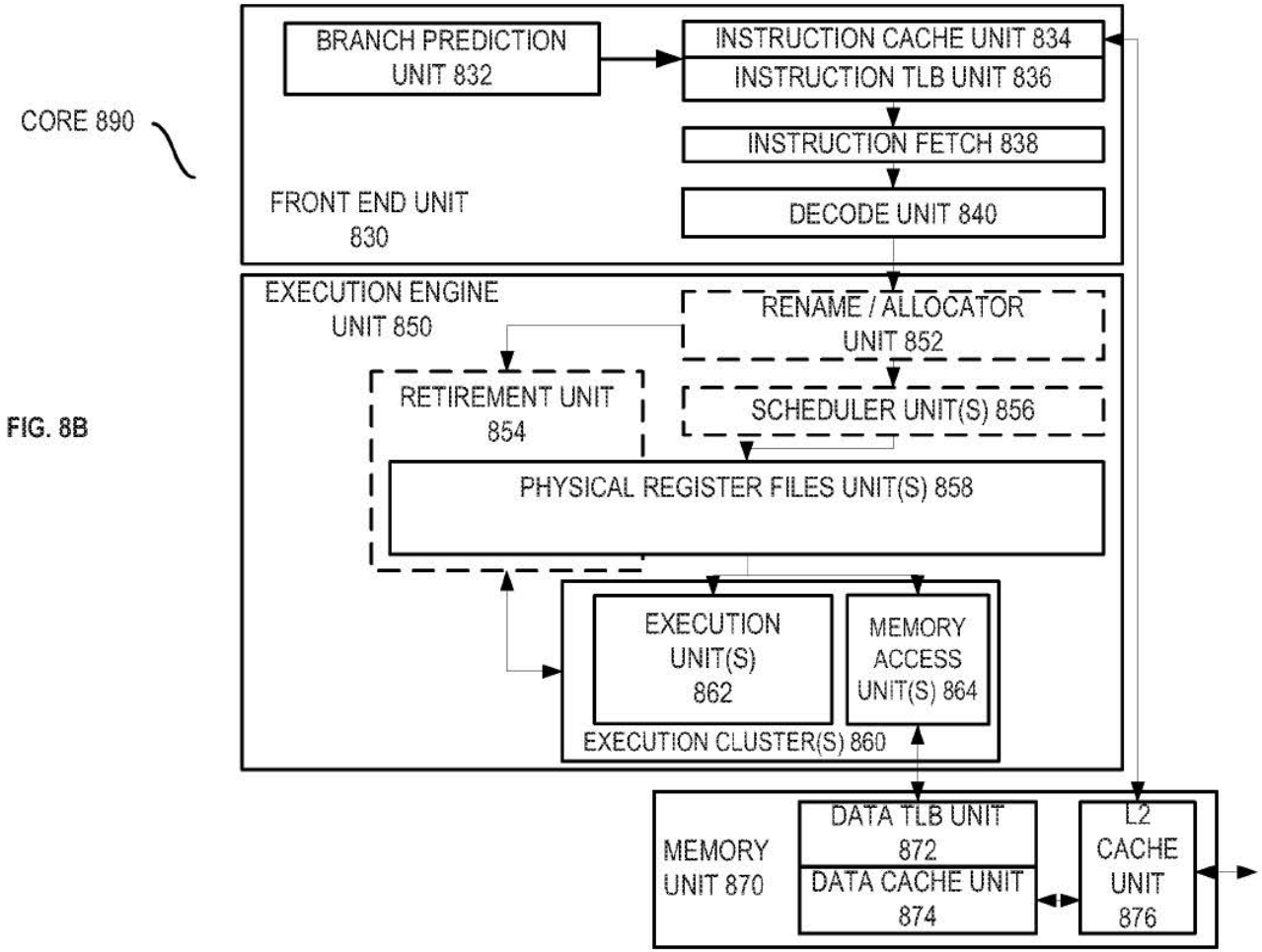


FIG. 8B



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FIG. 9A

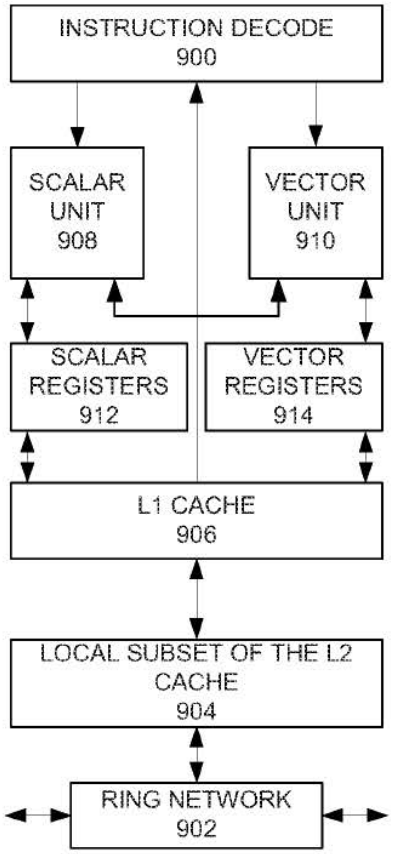
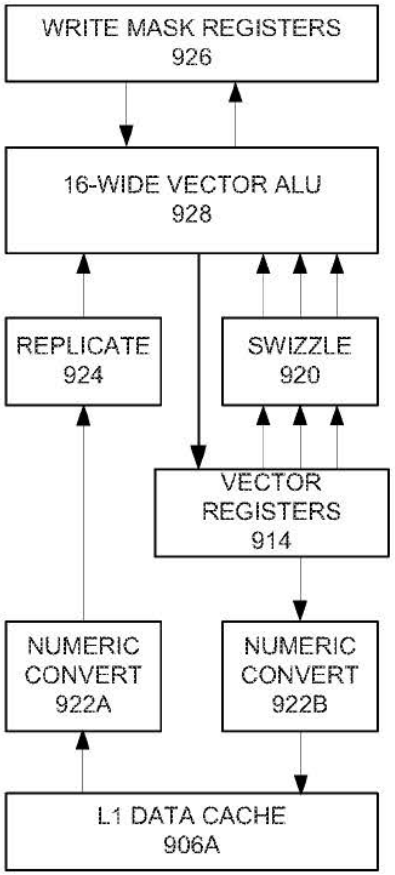


FIG. 9B



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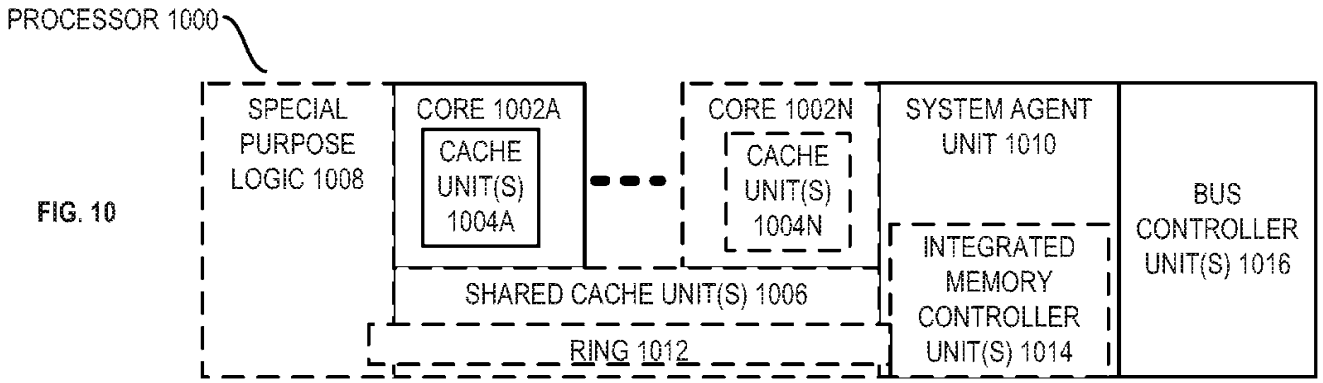


FIG. 10

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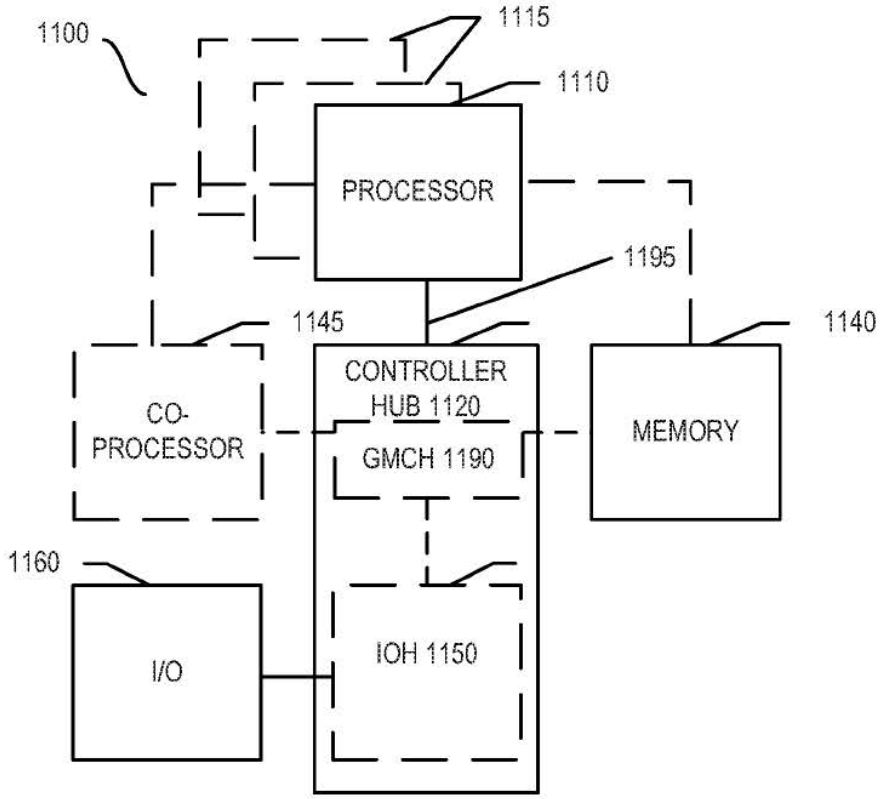

1100
1115
1110
PROCESSOR
1195
1145
1140
CONTROLLER
HUB 1120
CO-
PROCESSOR
GMCH 1190
MEMORY
1160
I/O
IOH 1150

FIG. 11

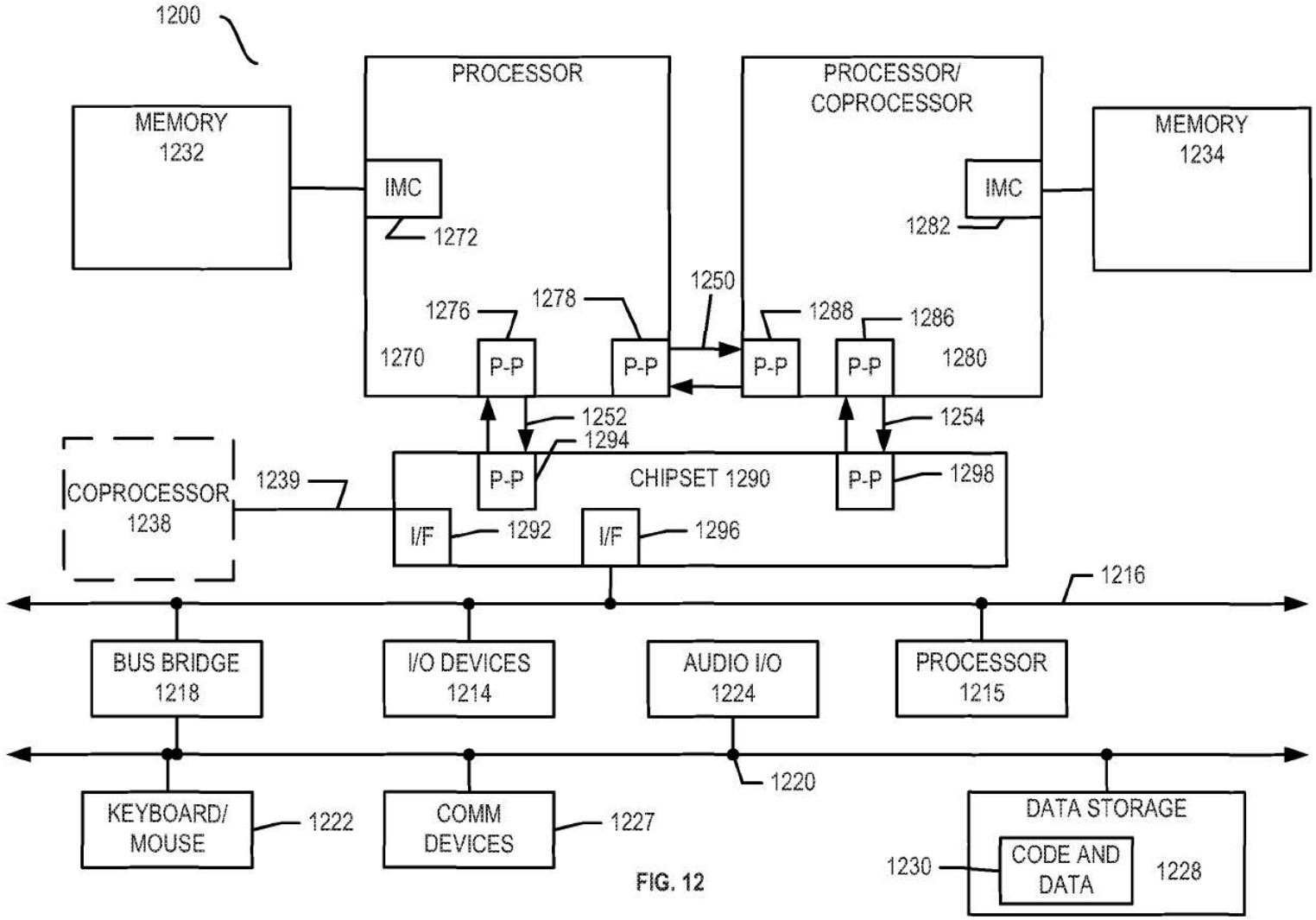


FIG. 12

Petitioner Samsung Ex-1004, 0056

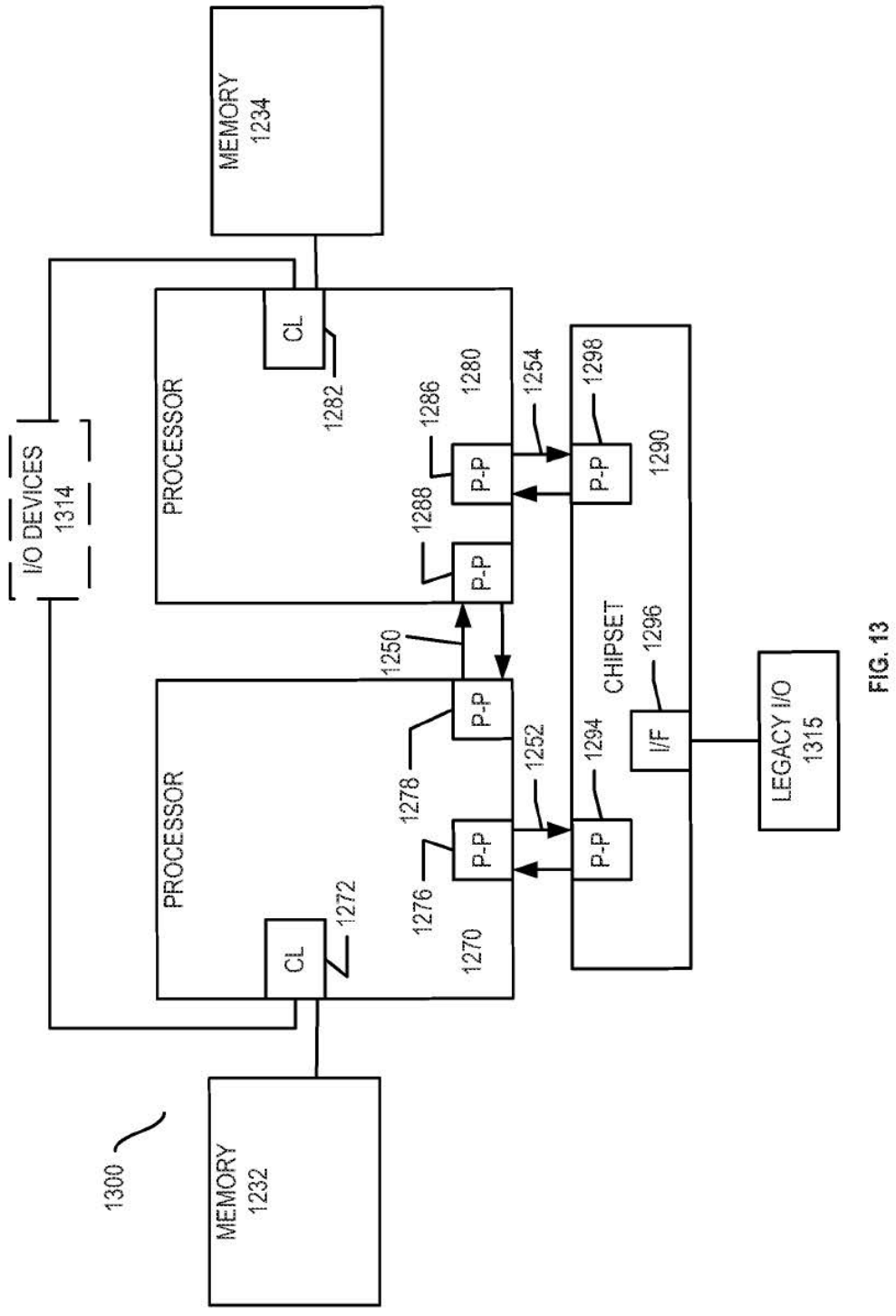
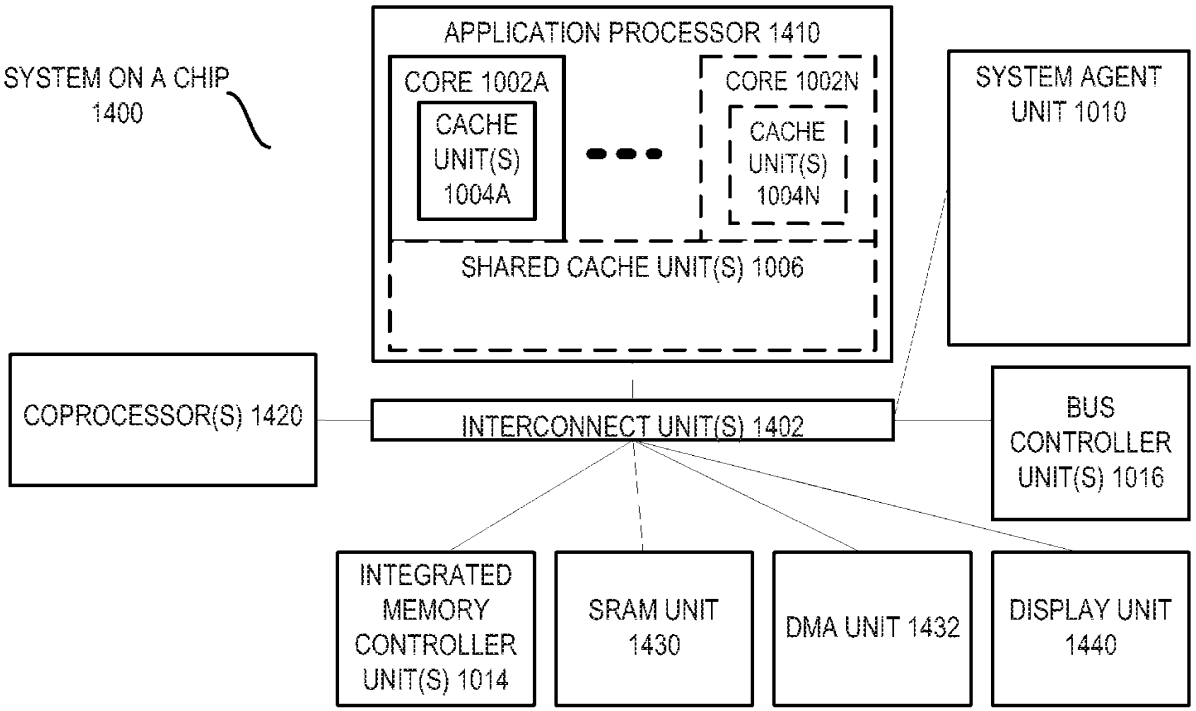


FIG. 13

Petitioner Samsung Ex-1004, 0057

FIG. 14



Petitioner Samsung Ex-1004, 0058

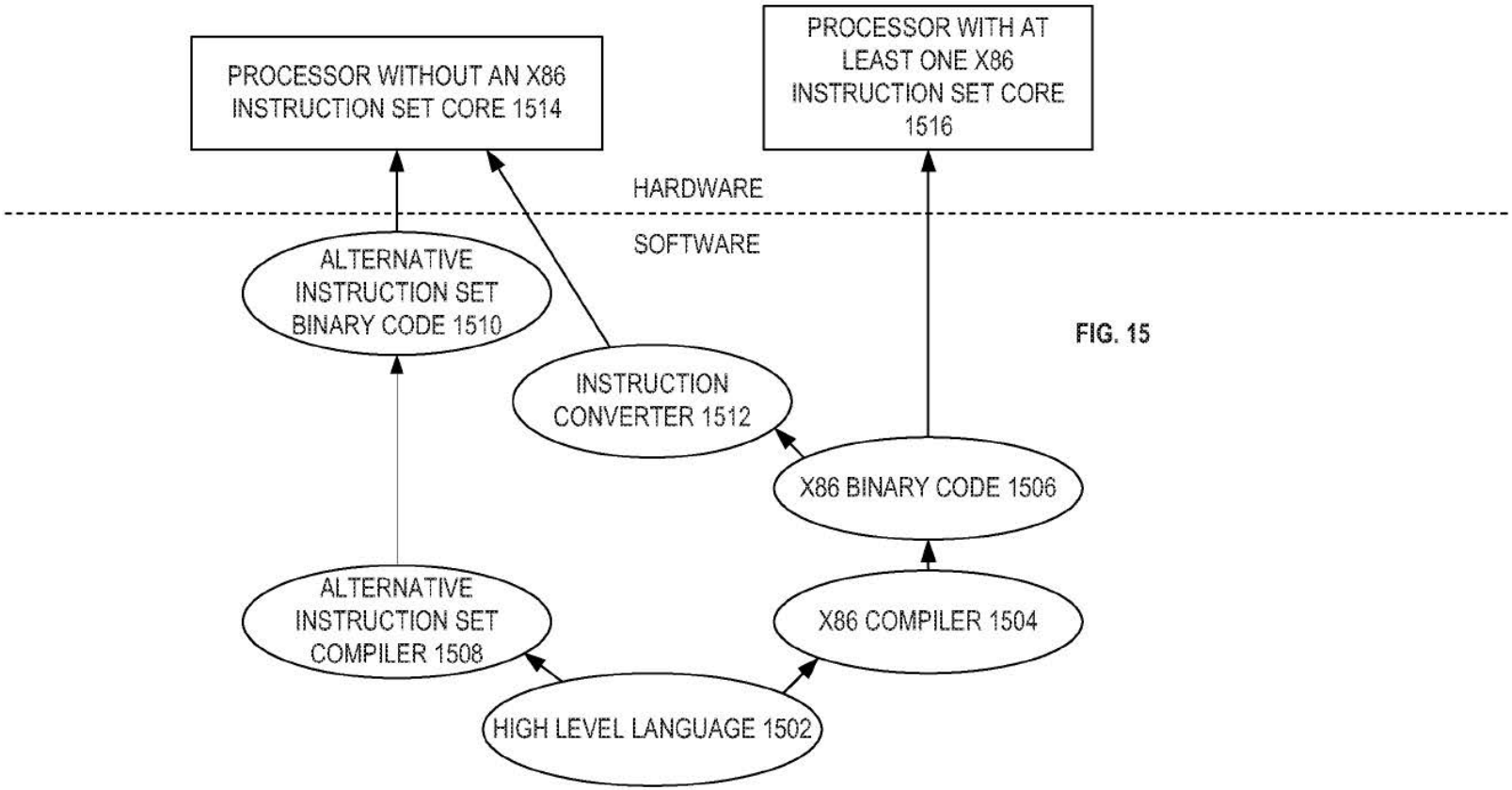


FIG. 15

Petitioner Samsung Ex-1004, 0059

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number **13/729579** filed on **12/28/2012**.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: **HERBERT H. HUM** Date (Optional): 1/18/2013

Signature: H. H. Hum

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Petitioner Samsung Ex-1004, 0060

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

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☒ United States application or PCT international application number **13/729579** filed on **12/28/2012**.

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LEGAL NAME OF INVENTOR

Inventor: **BRINDA GANESH** Date (Optional): _____

Signature: _____

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0061

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

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This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number **13/729579** filed on **12/28/2012**.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

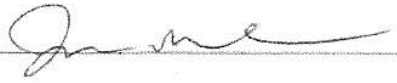
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LEGAL NAME OF INVENTOR

Inventor: **JAMES R. VASH** Date (Optional): 2/20/13

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0062

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

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This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT International application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: GANESH KUMAR Date (Optional): _____

Signature: G. Cum

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0063

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

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This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number **13/729579** filed on **12/28/2012**.

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LEGAL NAME OF INVENTOR

Inventor: **LEENA K. PUTHIYEDATH** Date (Optional): JAN 13 2013

Signature: P. Leena Keenan

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0064

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

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LEGAL NAME OF INVENTOR

Inventor: SCOTT J. ERLANGER Date (Optional): 12/24/2012

Signature: Scott J Erlanger

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0065

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LEGAL NAME OF INVENTOR

Inventor: ERIC J. DEHAEMER Date (Optional): 2/22/2013

Signature: [signature]

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0066

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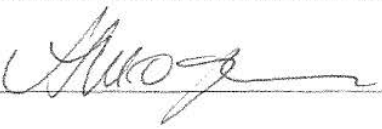
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LEGAL NAME OF INVENTOR

Inventor: **ADRIAN C. MOGA** Date (Optional): Jan 7, 2013

Signature: 

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

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Petitioner Samsung Ex-1004, 0067

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This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number **13/729579** filed on **12/28/2012**.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: **MICHELLE M. SEBOT** Date (Optional): 1/7/2013

Signature: Michelle Sebot

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Petitioner Samsung Ex-1004, 0068

Based on PTO/AIA (08-12) as modified by Blakely, Sokoloff, Taylor & Zafman
Approved for use through 01/13/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: RICHARD L. CARLSON Date (Optional): 12/20/12

Signature: Richard L Carlson

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Petitioner Samsung Ex-1004, 0069

Based on PTO/AIA (06-12) as modified by Blakely, Sokoloff, Taylor & Zafman
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 13/729579 filed on 12/28/2012.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

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LEGAL NAME OF INVENTOR

Inventor: DAVID BUBIEN Date (Optional): 2/15/2013

Signature: Dennis Bubien

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Petitioner Samsung Ex-1004, 0070

Based on PTO/AIA (08-12) as modified by Blakely, Sokoloff, Taylor & Zafman
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

As the below named inventor, I hereby declare that:

This declaration is directed to:

☒ The attached application, or

☐ United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor: ERIC DELANO Date (Optional): _____

Signature: Eric DeLano

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Petitioner Samsung Ex-1004, 0071

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Herbert	H.	HUM	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Portland	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	3924 NW Teakwood Place		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country i	US

Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Brinda		GANESH	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Hillsboro	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	179 SE 49th Ct.		
Address 2			
City	Hillsboro	State/Province	OR
Postal Code	97123	Country i	US

Inventor 3

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	James	R.	VASH	

Petitioner Samsung Ex-1004, 0072

PTO/AIA/14 (08-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Littleton	State/Province	MA	Country of Residence [i]	US

Mailing Address of Inventor:

Address 1	85 Grist Mill Rd.		
Address 2			
City	Littleton	State/Province	MA
Postal Code	01460	Country [i]	US

Inventor 4

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Ganesh		KUMAR	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Fort Collins	State/Province	CO	Country of Residence [i]	US

Mailing Address of Inventor:

Address 1	1421 Redberry Ct.		
Address 2			
City	Fort Collins	State/Province	CO
Postal Code	80525	Country [i]	US

Inventor 5

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Leena	K.	PUTHIYEDATH	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Portland	State/Province	OR	Country of Residence [i]	US

Mailing Address of Inventor:

Address 1	1592 NW Jolie PL		
Address 2			
City	Portland	State/Province	CO
Postal Code	Portland	Country [i]	US

Inventor 6

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Scott	J.	ERLANGER	

Petitioner Samsung Ex-1004, 0073

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Boston	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	221 West Newton Street, Apt. 3		
Address 2			
City	Boston	State/Province	MA
Postal Code	02116	Country i	US

Inventor 7

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Eric	J.	DEHAEMER	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Shrewsbury	State/Province	MA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	161 Floral St.		
Address 2			
City	Shrewsbury	State/Province	MA
Postal Code	01545	Country i	US

Inventor 8

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Adrian	C.	MOGA	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Portland	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	3697 NW 115th Ave.		
Address 2			
City	Portland	State/Province	OR
Postal Code	97229	Country i	US

Inventor 9

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Michelle	M.	SEBOT	

Petitioner Samsung Ex-1004, 0074

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Portland	State/Province	OR	Country of Residence i	US

Mailing Address of Inventor:

Address 1	3067 NW Wilson Street		
Address 2			
City	Portland	State/Province	OR
Postal Code	97210	Country i	US

Inventor 10

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Richard	L.	CARLSON	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Fort Collins	State/Province	CO	Country of Residence i	US

Mailing Address of Inventor:

Address 1	1443 Clementine Ct.		
Address 2			
City	Fort Collins	State/Province	CO
Postal Code	80526	Country i	US

Inventor 11

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	David		BUBIEN	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Fort Collins	State/Province	CO	Country of Residence i	US

Mailing Address of Inventor:

Address 1	412 Flagler Rd.		
Address 2			
City	Fort Collins	State/Province	CO
Postal Code	80525	Country i	US

Inventor 12

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Eric		DELANO	

Petitioner Samsung Ex-1004, 0075

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service

City	Fort Collins	**State/Province**	CO	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	6237 Eagle Ridge Ct.		
Address 2			
City	Fort Collins	**State/Province**	CO
Postal Code	80525	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	124662		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES		
Attorney Docket Number	P49345-C2	**Small Entity Status Claimed**	☐
Application Type			
Subject Matter			
Total Number of Drawing Sheets (if any)	15	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country i

Petitioner Samsung Ex-1004, 0076

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	124662		

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	13729579	2012-12-28

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

Petitioner Samsung Ex-1004, 0077

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Petitioner Samsung Ex-1004, 0078

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Petitioner Samsung Ex-1004, 0079

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

Organization Name	Intel Corporation

Mailing Address Information For Applicant:

Address 1	2200 Mission College Boulevard		
Address 2			
City	Santa Clara	**State/Province**	CA
Country[i]	US	Postal Code	95054
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Petitioner Samsung Ex-1004, 0080

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

Petitioner Samsung Ex-1004, 0081

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	P49345-C2
	Application Number	
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Brent E. Vecchia/			Date (YYYY-MM-DD)	
First Name	Brent E.	Last Name	Vecchia	Registration Number	48011

Additional Signature may be generated within this form by selecting the Add button.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Filer:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1720**

Electronic Acknowledgement Receipt	
EFS ID:	32257787
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia
Filer Authorized By:	
Attorney Docket Number:	P49345-C2
Receipt Date:	08-APR-2018
Filing Date:	
Time Stamp:	13:53:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1720
RAM confirmation Number	040918INTEFSW00007285506674
Deposit Account	506674
Authorized User	Brent Vecchia
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P49345C2_APPLICATION_04-06-2018.pdf	225530 c6f1cb8480606c90fed6ecb271c6b9feb2be662e	yes	44

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	38
Claims	39	43
Abstract	44	44

Warnings:					
Information:					
2	Drawings-only black and white line drawings	P49345_FIGS.pdf	684097 4561467f53c72d9724ccf2df73a3aedb29200b12	no	15
Warnings:					
Information:					
3	Oath or Declaration filed	P49345_DEC.pdf	1303972 a2c6f70eee041ca28de01102e5533ce077b6e05e	no	12
Warnings:					
Information:					
4	Application Data Sheet	WebADS.pdf	234038 b8e862a06773eba7ce92fc0907c9bb6d6a39fee8	no	11
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	34877 7c4436ec428269bf215aa5afcb2ec920cadf66d8	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	2482514

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/947,830

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/947,830	04/08/2018	2139	1720	P49345-C2	20	3

CONFIRMATION NO. 5561

124662
Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

FILING RECEIPT



Date Mailed: 05/04/2018

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Herbert H. HUM, Portland, OR;
Brinda GANESH, Hillsboro, OR;
James R. VASH, Littleton, MA;
Ganesh KUMAR, Fort Collins, CO;
Leena K. PUTHIYEDATH, Portland, OR;
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Michelle M. SEBOT, Portland, OR;
Richard L. CARLSON, Fort Collins, CO;
David BUBIEN, Fort Collins, CO;
Eric DELANO, Fort Collins, CO;

Applicant(s)

Intel Corporation, Santa Clara, CA;

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/729,579 12/28/2012

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Petitioner Samsung Ex-1004, 0089

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/02/2018

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/947,830**

Projected Publication Date: 08/09/2018

Non-Publication Request: No

Early Publication Request: No

Title

PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

Petitioner Samsung Ex-1004, 0090

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

Petitioner Samsung Ex-1004, 0091

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Petitioner Samsung Ex-1004, 0092

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2	5561

124662 7590 07/23/2018

Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CALIFORNIA 95113
UNITED STATES OF AMERICA

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
07/23/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ndwe_docketing@cardinal-ip.com
patent@ndwe.com

Petitioner Samsung Ex-1004, 0093

Office Action Summary	**Application No.** 15/947,830	**Applicant(s)** HUM et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 08 April 2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b)☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/08/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Petitioner Samsung Ex-1004, 0094

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

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The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

Claims 1-4, 13-16 and 19-20 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1-4, 13-16 and 21-23 of copending Application No. 13/729,579 in view of O'Connor et al. (US 2014/0089699) (hereafter O'Connor).

Claims 1-4, 13-16 and 21-23 of Application No. 13/729,579 teaches the limitations of claims 1-4, 13-16 and 19-20 of the present application.

Application No. 13/729,579 does not teach power management circuitry to enable a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores, the power management circuitry to selectively gate power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions.

However, O'Connor teaches power management circuitry to enable a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores, the power management circuitry to selectively gate power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions ([0042]).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the power management circuitry of O'Connor with the invention of Application No. 13/729,579 because it increases efficiency by performing power configuration adjustments while satisfying the memory and computational requirements of the system and while minimizing GPU power consumption and/or maximizing performance under a power constraint ([0015]).

Claims 1-20 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1-20 of copending Application No. 15/947,829. Claims 1- 20 of US Application No. 15/947,829 contains every element of claims 1-20 of the instant application and as such anticipates claims 1- 20 of the instant application.

Claims 1-20 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claim 1-20 of copending Application No. 15/947,831. Claims 1- 20 of US Application No. 15/947,831 contains every element of claims 1-20 of the instant application and as such anticipates claims 1- 20 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896,225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berq, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

This is a provisional nonstatutory double patenting rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 and 19-20 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 1, line 2 recites the limitation "a plurality of cores to execute". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Here, Applicant recites a plurality of cores to execute, but never actually recite that the cores actually perform the execution. Therefore, this language is construed to be non limiting. Applicant correction and/or clarification is required.

Claim 1, line 4 recites "a cache subsystem to store". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 9 recites "circuitry to provide". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 11 recites "circuitry to enable". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 11 recites "frequency to be set". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 12 recites "frequency to be set". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 13 recites "circuitry to selectively". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 16, recites "memory controller to couple". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 18, recites "memory controller to couple". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claims 2-12 and 19-20 recite similar language. Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 19 recites the limitation "the plurality of instructions, if performed by a machine..." Claim scope is not limited by claim language that suggests or makes optional but

does not require steps to be performed. Therefore, all steps following this language are construed to be non-limiting.

Claim 20 depend from claim 19 and is rejected for the reasons cited above.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 12, 13, 15, and 19 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 2005/0027941) (hereafter Wang), in view of O'Connor et al. (US 2014/0089699) (hereafter O'Connor).

As per claims 1, 13 and 19, Wang teaches a processor comprising:

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores ([0026]);

a cache subsystem to store the instructions and data, the cache subsystem comprising a plurality of first-level caches and at least one higher-level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first-level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores (fig. 1);

cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores ([0022] describes the use of ring topologies for a NUMA configuration);

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory (fig. 4, 105a…105n); and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory (fig. 4, 105a…105n).

Wang does not explicitly teach

power management circuitry to enable a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores, the power management circuitry to selectively gate power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions.

However, O'Connor teaches power management circuitry to enable a first frequency to be set for a first subset of the plurality of cores and a second frequency to be set for a second subset of the plurality of cores (figs. 6-9), the power management circuitry to selectively gate power to the first subset of the plurality of cores, the second subset of the plurality of cores, and/or one or more of the cache portions ([0042]).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the power management circuitry of O'Connor with the processor of Wang because it increases efficiency by performing power configuration adjustments while satisfying the memory and computational requirements of the system and while minimizing power consumption and/or maximizing performance under a power constraint ([0015]).

As per claim 2, O'Connor teaches wherein the power management circuitry is to selectively gate power to one or more of the first and/or second subsets of the plurality of cores and corresponding cache portions ([0042]).

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As per claim 3, Wang teaches wherein a first core of a first predetermined subset is physically proximate to a first cache portion (fig. 1).

As per claim 4, Wang teaches a local core-cache interconnect to couple the first core to the first cache portion; and an on-die interconnect to couple one or more other cores to the first cache portion (fig. 3, on chip).

As per claim 5, Wang teaches wherein the local core-cache interconnect and on-die interconnect provide different access latency and/or data throughput to a given cache portion (As illustrated in fig. 1, the data accessed in L2 is faster than L3).

As per claim 6, Wang teaches wherein the local core-cache interconnect is to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first cache portion than the on-die interconnect is to provide to the one or more other cores when the one or more other cores access the first cache portion (As illustrated in fig. 4 with remote fetches as response to a miss).

As per claim 8, Wang teaches wherein at least one of the plurality of cores comprises: an instruction fetch circuit to fetch instructions from a corresponding first level cache or a system memory; and a decode circuit to decode the instructions; and an execution circuit comprising a plurality of functional units to execute the instructions ([0030]).

As per claims 12 and 15, Wang teaches wherein the non-uniform access to the plurality of cache portions by the plurality of cores is based, at least in part, on each cache portion being coupled to a proximate subset of the plurality of cores over a first interconnect having first characteristics and being coupled to a non-proximate subset of the plurality of cores over a second interconnect having second characteristics ([0022] by definition of a ring interconnect this would occur).

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Claims 7 and 14 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over the combination of Wang and O'Connor as applied to claims 1 and 13 above, and further in view of Cai et al. (US 2009/0172424) (hereafter Cai).

As per claims 7 and 14, the combination of Wang and O'Connor teaches all the limitations of claims 1 and 13. The combination does not explicitly teach wherein, based on a workload on each of the first and second subsets of the plurality of cores, a thread is to be selectively migrated from the first subset to the second subset.

However, Cai teaches wherein, based on a workload on each of the first and second subsets of the plurality of cores, a thread is to be selectively migrated from the first subset to the second subset ([0022]).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the thread migration of Cai with the cores of the combination of Wang and O'Connor because it will improve thread synchronization and create opportunities to improve power efficiency ([0022]).

Claims 9-10 and 16-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over the combination of Wang and O'Connor as applied to claims 1 and 13 above, and further in view of Rajamony et al. (US 2011/0022773)(hereafter Rajamony).

As per claims 9 and 16, the combination of Wang and O'Connor teaches all the limitations of claims 6 and 13. The combination does not explicitly teach wherein the first subset of the plurality of cores form a first virtual processor and the second subset of the plurality of cores form a second virtual processor.

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However, Rajamony teaches wherein the first subset of the plurality of cores form a first virtual processor and the second subset of the plurality of cores form a second virtual processor ([0040]) .

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the virtual processors of Rajamony with the cores of the combination of Wang and O'Connor because by using virtualization, multiple operating systems can run in the same server, eliminating the need to dedicate a single machine to one application ([0006]).

As per claims 10 and 17, Rajamony teaches wherein the execution circuit is to execute instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first subset of the plurality of cores and to form the second virtual processor by combining the second subset of the plurality of cores ([0040]).

Claims 11, 18 and 20 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over the combination of Wang and O'Connor as applied to claims 1 and 19 above, and further in view of Zhu et al. (US 8,725,919) (hereafter Zhu).

As per claims 11 and 20, the combination of Wang and O'Connor teaches all the limitations of claims 1 and 19. The combination does not explicitly teach a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components.

However, Zhu teaches a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components (col. 3, lines 10-25).

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It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the PCIe interface of Zhu with the interconnect of the combination of Wang and O'Connor because it provides high speed connectivity (col. 3, lines 10-25).

As per claim 18, the combination of Wang and O'Connor teaches all the limitations of claim 1. Wang further teaches transmitting data between the plurality of cores and one or more system components (fig. 4).

The combination does not explicitly teach wherein the data is transmitted via a Peripheral Component Interface Express (PCIe) interface.

However, Zhu teaches wherein the data is transmitted via a Peripheral Component Interface Express (PCIe) interface (col. 3, lines 10-25).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the PCIe interface of Zhu with the interconnect of the combination of Wang and O'Connor because it provides high speed connectivity (col. 3, lines 10-25).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on M-F 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Notice of References Cited	Application/Control No. 15/947,830	Applicant(s)/Patent Under Reexamination HUM et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20050027941-A1	02-2005	Wang, Hong	G06F9/383	711/121
*	B	US-20110022773-A1	01-2011	Rajamony; Ramakrishnan	G06F12/084	711/3
*	C	US-20090172424-A1	07-2009	Cai; Qiong	G06F1/3203	713/300
*	D	US-20080062927-A1	03-2008	Zhu; Julianne Jiang	G06F9/3851	370/331
*	E	US-20140089699-A1	03-2014	O'Connor; James M.	G06F1/324	713/322
	F					
	G					
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FOREIGN PATENT DOCUMENTS

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	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	07/18/2018	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	07/18/2018	GB
NPL Search in Google Scholar (See Attached)	07/18/2018	GB
Inventor Search in PE2E	07/18/2018	GB
Application search in Global Dossier	07/18/2018	GB

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	07/18/2018								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
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	20	✓								

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	104	PCIe with coupl$3 with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:14
L2	3187	PCIe with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:29
L3	62	PCIe with (faster greater) with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:30
L4	90	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:37
L5	6297	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	US-PGPUB; USPAT	OR	OFF	2018/07/18 00:17
S1	2	"20140089699".pn. "20090063715".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 13:46
S2	1	"20110055482".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 15:58
S3	40667	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:01
S4	11910	cores with threads	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S5	1842	S3 and S4	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S6	71	S3 and S4 and NUMA	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S7	1	"20050027941".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 18:53
S8	26	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:43
S9	320	cores with virtual with processor and VMM	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:46

EAST Search History (Interference)

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A 1.2 TB/s on-chip **ring interconnect** for 45nm 8-**core** enterprise Xeon® processor — Full-Text @ USPTO-STIC

C Park, R Badeau, L Biro, J Chang... - Solid-State Circuits ..., 2010 - ieeexplore.ieee.org

... Figure 9.4.1 is a floorplan view of the chip design showing the relative placement of the 10 **ring** stops (Cbox, Sbox), the co-located **cores** and **cache** (LLC), and ... Figure 9.4.7: Nehalem-EX microprocessor die photo with 8 **core**/cbox slices connected by a **ring interconnect**.

Cited by 29 Related articles All 2 versions

Configurable isolation: building high availability systems with commodity multi-**core** processors — [PDF] wisc.edu Full-Text @ USPTO-STIC

N Aggarwal, P Ranganathan, NP Jouppi... - ACM SIGARCH ..., 2007 - dl.acm.org

... This configuration requires four **ring** cross connects and uses two fewer address bits for interleaving **cache** bank addresses ... If there is a **core** fault (P5 in the figure) then system software isolates the faulty **core** and continues functioning with the remaining **cores** ...

Cited by 200 Related articles All 11 versions

[PDF] Intel® Xeon Phi™ coprocessor-the architecture — [PDF] uminho.pt

G Chrysos - Intel Whitepaper, 2014 - gec.di.uminho.pt

... is 64 bytes wide to support the high bandwidth requirement due to the large number of **cores** ... Finally, the smallest **ring** and the least expensive **ring** is the acknowledgement **ring**, which sends flow ... When a **core** accesses its L2 **cache** (Figure 7) and misses, an address request is ...

Cited by 123 Related articles

A fully integrated multi-CPU, GPU and memory controller 32nm processor — Full-Text @ USPTO-STIC

M Yuffe, E Knoll, M Mehalel, J Shor... - Solid-State Circuits ..., 2011 - ieeexplore.ieee.org

... The modular **ring interconnect** enables the 4-**core** die to be easily converted into a 2-**core** die ... placed at several locations inside the **core** providing an accu- rate picture of the **core** hot spots ... GDXC), a debug bus that allows monitoring the traffic between the IA **cores**, GPU, **caches** ...

Cited by 128 Related articles All 2 versions

Power-management architecture of the intel microarchitecture code-named sandy bridge — [PDF] researchgate.net Full-Text @ USPTO-STIC

E Rotem, A Naveh, A Ananthakrishnan... - Ieee ..., 2012 - ieeexplore.ieee.org

... The second-generation Sandy Bridge **core** processor has five main domains: Intel architecture **cores**, a **ring interconnect**, a shared last-level **cache** (LLC), a system agent, and processor graphics. Figure 1 describes the Sandy Bridge die ...

Cited by 350 Related articles All 9 versions

ATAC: a 1000-**core cache**-coherent processor with on-chip optical network — [PDF] mit.edu

G Kurian, JE Miller, J Psota, J Eastep, J Liu... - Proceedings of the 19th ..., 2010 - dl.acm.org

... The **ring** resonators are not used for modulation but just for wavelength filtering ... true shared read when it reads from an address that is **cached** by at least another **core** in the ... true shared reads lead to the occurrence of frequent invalidations because a large number of **cores** try to ...

Cited by 217 Related articles All 15 versions

[PDF] Nehalem-ex cpu architecture — [PDF] hotchips.org

S Kottapalli, J Baxter - Hot chips, 2009 - hotchips.org

... Hot Chips 2009 **Cores** and Last Level **Caches** • Start with 8 Nehalem **Cores** – Modular and high throughput ... Scalable fabric – BW scales with **ring** stops – Simulated >250GB/s of **interconnect** BW ... Request to local memory controller – Direct fill to **core** for latency reduction ...

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Cited by 36 Related articles All 4 versions

No **cache**-coherence: a single-cycle **ring interconnection** for multi-**core** L1-NUCA sharing on 3D chips — Full-Text @ USPTO-STIC

SH Chou, CC Chen, CN Wen, YC Chan... - Proceedings of the 46th ..., 2009 - dl.acm.org

Consistent with the trend towards the use of many **cores** in SOC and 3D Chip techniques, this paper proposes a" single-cycle **ring**" **interconnection** (SC_Ring) with ultra-low latency and minimal complexity. The proposed SC_Ring allows multiple single-cycle transactions in ...

Cited by 17 Related articles All 3 versions

Ring interconnect with multiple coherence networks

B Tsien - US Patent 7,406,566, 2008 - Google Patents

... be used in an electronic device, such as a single **core** or multiple **core** microprocessor, or ... invention may be located within any processor having any number of processing **cores**, or within ... 7 illustrates a **ring** network of **cache** agents according to an alternative embodiment of the ...

Cited by 28 Related articles All 4 versions

Coherence ordering for **ring**-based chip multiprocessors — [PDF] wisc.edu Full-Text @ USPTO-STIC

MR Marty, MD Hill - ... , 2006. MICRO-39. 39th Annual IEEE/ACM .. , 2006 - ieeexplore.ieee.org

... bus, a crossbar is also a centralized structure that faces similar performance challenges in many-**core** CMPs ... are being considered by Intel for next-generation CMPs consisting of 8 to 16 **cores** [24 ... systems can be built by using a hierarchy, such as clustering or even a **ring**-of-**rings** ...

Cited by 61 Related articles All 11 versions

Related searches

ring interconnection cache **coherence** **coherence networks** ring interconnect

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EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	104	PCIe with coupl$3 with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:14
L2	3187	PCIe with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:29
L3	62	PCIe with (faster greater) with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:30
L4	90	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:37
S1	2	"20140089699".pn. "20090063715".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 13:46
S2	1	"20110055482".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 15:58
S3	40667	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:01
S4	11910	cores with threads	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S5	1842	S3 and S4	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S6	71	S3 and S4 and NUMA	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S7	1	"20050027941".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 18:53
S8	26	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:43
S9	320	cores with virtual with processor and VMM	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:46

EAST Search History (Interference)

< This search history is empty>

7/18/2018 12:16:49 AM
C:\Users\gbansal\Documents\EAST\Workspaces\15947830.wsp

Petitioner Samsung Ex-1004, 0113

Bibliographic Data

Application No: 15/947,830

Foreign Priority claimed: ○ Yes ◉ No

35 USC 119 (a-d) conditions met: ☐ Yes ☑ No ☐ Met After Allowance

Verified and Acknowledged: /GURTEJ BANSAL/ Examiner's Signature | Initials

Title: PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
04/08/2018	711	2139	P49345-C2
RULE			

APPLICANTS

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CONTINUING DATA

This application is a CON of 13729579 12/28/2012

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

05/02/2018

STATE OR COUNTRY

UNITED STATES

ADDRESS

Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113
UNITED STATES

FILING FEE RECEIVED

$1,720

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2

CONFIRMATION NO. 5561

124662
Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

PUBLICATION NOTICE

OC000000101594635

Title:PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

Publication No.US-2018-0225212-A1
Publication Date:08/09/2018

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Petitioner Samsung Ex-1004, 0116

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0051
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 124662

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

INTEL CORPORATION

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Lisa Hopkinson	Date (Optional)	
Name	Lisa Hopkinson		
Title	Administrator of Patents, Intel Corporation		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	33798474
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia/Richard Pagaduan
Filer Authorized By:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2
Receipt Date:	21-SEP-2018
Filing Date:	08-APR-2018
Time Stamp:	23:55:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P49345-C2_373_POA_9-21-2018.pdf	1259800 b2861525295baf5a1f18c6150e95c2a89f086a0e	yes	4

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Assignee showing of ownership per 37 CFR 3.73	1	3
	Power of Attorney	4	4
Warnings:			
Information:			
	Total Files Size (in bytes):	1259800	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: INTEL CORPORATION

Application No./Patent No.: 15/947,830 Filed/Issue Date: 04/08/2018

Titled: PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

INTEL CORPORATION, a CORPORATION

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 030114, Frame 0247, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

   1. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

      Reel _____, Frame _____, or for which a copy thereof is attached.

   2. From: _____ To: _____

      The document was recorded in the United States Patent and Trademark Office at

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This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

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The document was recorded in the United States Patent and Trademark Office at

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6. From: _____ To: _____

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Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Brent E. Vecchia/	2018-09-21
Signature	Date
Brent E. Vecchia	48011
Printed or Typed Name	Title or Registration Number

Petitioner Samsung Ex-1004, 0121

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2

CONFIRMATION NO. 5561

124662
Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

POA ACCEPTANCE LETTER

OC000000102573808

Date Mailed: 09/26/2018

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/21/2018.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/atesfai/

Petitioner Samsung Ex-1004, 0123

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6115790		2000-09-05	SCHIMMEL; Curt F.	
	2	6542966		2003-04-01	CRAWFORD; John et al.	
	3	7055007		2006-05-30	FLAUTNER; Krisztian et al.	
	4	8037476		2011-10-11	SHAVIT; Nir N. et al.	
	5	8108610		2012-01-31	GLASCO; David B. et al.	
	6	8219996		2012-07-10	MORRIS; Dale C.	
	7	8261024		2012-09-04	SHAVIT; Nir N. et al.	
	8	8429656		2013-04-23	DULUK Jr.; Jerome F. et al.	

Petitioner Samsung Ex-1004, 0124

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

	9	8725919		2014-05-13	ZHU; Julianne J. et al.	
	10	8862828		2014-10-14	SARAF; Ravindra P. et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020046324		2002-04-18	BARROSO; Luiz Andre et al.	
	2	20020049859		2002-04-25	BRUCKERT; William et al.	
	3	20030061423		2003-03-27	RANKIN; Linda J. et al.	
	4	20040226026		2004-11-11	GLASS; Adam B. et al.	
	5	20060004796		2006-01-05	NAKAMURA; Shuji	
	6	20060206635		2006-09-14	ALEXANDER; Thomas et al.	
	7	20070156964		2007-07-05	SISTLA; Krishnakanth V.	

Petitioner Samsung Ex-1004, 0125

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

	8	20080022261		2008-01-24	GOODING; Thomas Michael	
	9	20080126750		2008-05-29	SISTLA; Krishnakanth	
	10	20080195719		2008-08-14	WU; Yuguang et al.	
	11	20090037658		2009-02-05	SISTLA; Krishnakanth	
	12	20090049248		2009-02-19	CLARK; Leo James et al.	
	13	20090063715		2009-03-05	DE; Cesare Joshua et al.	
	14	20090089470		2009-04-02	VEN; Adriaan Van De et al.	
	15	20090187642		2009-07-23	MCGRATH; Michael P.	
	16	20090193064		2009-07-30	CHEN; Ying et al.	
	17	20090265514		2009-10-22	BILES; Stuart David et al.	
	18	20090271646		2009-10-29	TALWAR; Vanish et al.	

Petitioner Samsung Ex-1004, 0126

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

	19	20100074106		2010-03-25	CHOU; Ching-Tsun et al.	
	20	20100257316		2010-10-07	ARIMILLI; Ravi K. et al.	
	21	20110035555		2011-02-10	WANG; Hong et al.	
	22	20110055482		2011-03-03	SO; Kimming et al.	
	23	20110087840		2011-04-14	GLASCO; David B. et al.	
	24	20110087843		2011-04-14	ZHAO; Li et al.	
	25	20110119397		2011-05-19	EVANS; John et al.	
	26	20110153936		2011-06-23	STARKE; William J.	
	27	20110173394		2011-07-14	GARA; Alan et al.	
	28	20110179199		2011-07-21	CHEN; Dong et al.	
	29	20110219208		2011-09-08	ASAAD; Sameh et al.	

Petitioner Samsung Ex-1004, 0127

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

	30	20110252216		2011-10-13	YLONEN; Tatu J. et al.	
	31	20110296406		2011-12-01	BHANDARI; Aditya et al.	
	32	20130073811		2013-03-21	BECKMANN; Bradford M. et al.	
	33	20130085999		2013-04-04	TUNG; Teresa et al.	
	34	20130311724		2013-11-21	WALKER; William L. et al.	
	35	20140189239		2014-07-03	HUM; Herbert H. et al.	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	None						

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Petitioner Samsung Ex-1004, 0128

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

	1	Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on February 09, 2016, 14 pages.	
	2	Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on October 18, 2017, 17 pages.	
	3	Non-Final Office Action from U.S. Patent Application No. 15/947,829 (Atty. Docket No. 42P49345C1), mailed July 19, 2018, 14 pages.	
	4	Non-Final Office Action from U.S. Patent Application No. 15/947,831 (Atty. Docket No. 42P49345C3), mailed August 02, 2018, 14 pages.	
	5	Non-Final Office Action received for U.S. Patent Application No. 13/584,656, mailed on February 13, 2014, 17 pages.	
	6	Non-Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on February 07, 2017, 16 pages.	
	7	Non-Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on June 01, 2015, 13 pages.	
	8	Notice of Allowance from U.S. Patent Application No. 13/729,579 (Atty. Docket No. 42P49345), mailed May 02, 2018, 8 pages.	
	9	Notice of Allowance received for U.S. Patent Application No. 13/584,656, mailed on June 09, 2014, 11 pages.	
	10	TAM D., "Operating System Management of Shared Caches on Multicore Processors," University of Toronto, 2010, 170 pages.	

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Petitioner Samsung Ex-1004, 0129

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Petitioner Samsung Ex-1004, 0130

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Brent E. Vecchia/	Date (YYYY-MM-DD)	2018-10-24
Name/Print	Brent E. Vecchia	Registration Number	48011

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Petitioner Samsung Ex-1004, 0131

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Petitioner Samsung Ex-1004, 0132

Electronic Patent Application Fee Transmittal

Application Number:	15947830
Filing Date:	08-Apr-2018
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Filer:	David F. Nicholson/Nithya P
Attorney Docket Number:	P49345-C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	240	240
		Total in USD ($)		**240**

Electronic Acknowledgement Receipt	
EFS ID:	34095755
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	David F. Nicholson/Nithya P
Filer Authorized By:	David F. Nicholson
Attorney Docket Number:	P49345-C2
Receipt Date:	24-OCT-2018
Filing Date:	08-APR-2018
Time Stamp:	07:01:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$240
RAM confirmation Number	102418INTEFSW07024200
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	42P49345C2_IDS_20181024.pdf	1055315 e2da47201b9ae60d838825f414a0543d409a2ce5	no	9
Warnings:					
Information:					
2	Non Patent Literature	NPL01_FOA6040834681653878708_EFS.PDF	484760 997af69ea6f5100b2a894cf4c68a6c68aa34bc30	no	14
Warnings:					
Information:					
3	Non Patent Literature	NPL02_P49345_FOA_10_18_2017539410176764831 2049_EFS.PDF	595497 c85b92c02f76923963d3ac558c06fea29996765b	no	17
Warnings:					
Information:					
4	Non Patent Literature	NPL03_NFOA_15947829_19Jul2018_14pgs_EFS.pdf	556280 3ae7d19317d683529e5fc8f80fd7825b5e656f45	no	14
Warnings:					
Information:					
5	Non Patent Literature	NPL04_NFOA_US15947831_2AUG2018_14PGS_EFS.PDF	522642 e042a7f4f23d623d61a73cec61b8487030fd5064	no	14
Warnings:					
Information:					
6	Non Patent Literature	NPL05_NFOA13584656518939 0843420538525_EFS.PDF	568251 88246b9a8c1de4ddd1124908177c688f9043e4e3	no	17
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7	Non Patent Literature	NPL06_P49345_NFOA_02_07_20171999853985425871915_EFS.PDF	556063 f8aab7b66612506ad725fac57fef47669a4afe95	no	16
Warnings:					
Information:					
8	Non Patent Literature	NPL07_NFOA59808100411109 90136_EFS.PDF	436754 f90bc6cca3aa668c7869051d9828a804a60807a3	no	13
Warnings:					
Information:					
9	Non Patent Literature	NPL08_NOA_13729579_02MAY2018_8PGS_EFS.PDF	438587 7e1eb7dcd3cabfee4903bcf7b2694fbb330b67e8	no	8
Warnings:					
Information:					
10	Non Patent Literature	NPL09_NOA891207439377910 0646_EFS.PDF	490689 d39c7861766e12b4c8dc7fbdafe8975722098da5	no	11
Warnings:					
Information:					
11	Non Patent Literature	NPL10_TAM_SHAREDCACHES_2010_170PGS_PART1_EFS.pdf	22266150 721d72fb8cd708818a3d36d115d063cd7c3b0813	no	60
Warnings:					
Information:					
12	Non Patent Literature	NPL10_TAM_SHAREDCACHES_2010_170PGS_PART2_EFS.PDF	23979594 22812d4b4d3bd2a627da6e9c0b2e0f2516983617	no	60
Warnings:					
Information:					
13	Non Patent Literature	NPL10_TAM_SHAREDCACHES_2010_170PGS_PART3_EFS.pdf	21237459 49e3be6145e7ba17a2cbd72c442f14620caaa2c6	no	50
Warnings:					
Information:					

14	Fee Worksheet (SB06)	fee-info.pdf	30676 8532b00656193398f8cc166a8aeee096cd5a32e5	no	2
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			Total Files Size (in bytes):	73218717	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application:	Examiner: Gurtej BANSAL
First Named Inventor:	Art Unit: 2139
Herbert H. HUM	Confirmation No: 5561
Application No. 15/947,830	
Filed: 04/08/2018	
For: PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

EFS Filing
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

In response to the Office Action dated July 23, 2018, please amend the above-identified application as follows and consider the following remarks:

EFS WEB	**FACSIMILE**
X *submitted electronically via EFS Web to the Patent and Trademark Office.*	☐ *transmitted by facsimile to the Patent and Trademark Office.*

/Brent E. Vecchia/ 12/26/2018

Petitioner Samsung Ex-1004, 0139

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A system comprising:

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem to store the instructions and the data, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores;

cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

power management circuitry to enable a first frequency ~~to be set~~ of operation for a first ~~subset~~ cluster of the plurality of cores which are physically proximate to one another and a second frequency ~~to be set~~ of operation for a second ~~subset~~ cluster of the plurality of cores which are physically proximate to one another, the power management circuitry to selectively gate power to the first ~~subset~~ cluster of the plurality of ~~cores,~~ cores and cache portions that correspond to the first cluster and/or the second ~~subset~~ cluster of the plurality of cores and cache portions that correspond to the second cluster; ~~cores, and/or one or more of the cache portions;~~

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory; and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory.

2. (Currently Amended) The system of claim 1 wherein the power management circuitry is to selectively gate power to one or more of the first and/or second ~~subsets~~ clusters of the plurality of cores and corresponding cache portions.

Petitioner Samsung Ex-1004, 0140

3. (Currently Amended) The system of claim 1 wherein a first core of a first predetermined ~~subset~~ cluster is physically proximate to a first cache portion.

4. (Original) The system of claim 3 further comprising:

a local core-cache interconnect to couple the first core to the first cache portion; and

an on-die interconnect to couple one or more other cores to the first cache portion.

5. (Currently Amended) The system of claim 4 wherein the local core-cache interconnect and the on-die interconnect provide different access latency and/or data throughput to the first ~~a given~~ cache portion.

6. (Original) The system of claim 4 wherein the local core-cache interconnect is to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first cache portion than the on-die interconnect is to provide to the one or more other cores when the one or more other cores access the first cache portion.

7. (Currently Amended) The system of claim 1 wherein, based on workload on each of the first and second ~~subsets~~ clusters of the plurality of cores, a thread is to be selectively migrated from the first ~~subset~~ cluster to the second ~~subset~~ cluster.

8. (Original) The system of claim 1 wherein at least one of the plurality of cores comprises:

an instruction fetch circuit to fetch instructions from a corresponding first level cache or a system memory; and

a decode circuit to decode the instructions; and

an execution circuit comprising a plurality of functional units to execute the instructions.

9. (Currently Amended) The system of ~~claim 6~~ claim 8 wherein the first ~~subset~~ cluster of the plurality of cores form a first virtual processor and the second ~~subset~~ cluster of the plurality of cores form a second virtual processor.

10. (Currently Amended) The system of claim 9 wherein the execution circuit is to execute instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first ~~subset~~ cluster of the plurality of cores and to form the second virtual processor by combining the second ~~subset~~ cluster of the plurality of cores.

Petitioner Samsung Ex-1004, 0141

11. (Original) The system of claim 1 further comprising a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components.

12. (Currently Amended) The system of claim 1 wherein the non-uniform access to the plurality of cache portions by the plurality of cores is based, at least in part, on each cache portion being coupled to a proximate ~~subset~~ cluster of the plurality of cores over a first interconnect having first characteristics and being coupled to a non-proximate ~~subset~~ cluster of the plurality of cores over a second interconnect having second characteristics.

13. (Currently Amended) A method comprising:

executing instructions and processing data with a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;

storing the instructions and the data in a cache subsystem, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores;

sharing the plurality of cache portions among the plurality of cores;

providing coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

enabling a first frequency to be set for a first ~~subset~~ cluster of the plurality of cores which are physically proximate to one another and a second frequency to be set for a second ~~subset~~ cluster of the plurality of cores which are physically proximate to one another;

selectively gating power to the first ~~subset~~ cluster of the plurality of ~~cores,~~ cores and cache portions that correspond to the first cluster and/or the second ~~subset~~ cluster of the plurality of cores and cache portions that correspond to the second cluster; ~~cores, and/or one or more of the cache portions;~~

controlling access by the symmetric multi-threaded cores to a first system memory with a first integrated memory controller; and

controlling access by the symmetric multi-threaded cores to a second system memory with a second integrated memory controller.

Petitioner Samsung Ex-1004, 0142

14. (Currently Amended) The method of claim 13 further comprising selectively migrated a thread from the first ~~subset~~ cluster to the second ~~subset~~ cluster based on a workload on each of the first and second ~~subsets~~ clusters of the plurality of cores.

15. (Currently Amended) The method of claim 13 wherein said providing the non-uniform access to the plurality of cache portions by the plurality of cores is based, at least in part, on each cache portion accessing a proximate ~~subset~~ cluster of the plurality of cores over a first interconnect having first characteristics and accessing a non-proximate ~~subset~~ cluster of the plurality of cores over a second interconnect having second characteristics.

16. (Currently Amended) The method of claim 13 further comprising forming the first ~~subset~~ cluster of the plurality of cores as a first virtual processor and forming the second ~~subset~~ cluster of the plurality of cores as a second virtual processor.

17. (Currently Amended) The method of claim 16 further comprising executing instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first ~~subset~~ cluster of the plurality of cores and to form the second virtual processor by combining the second ~~subset~~ cluster of the plurality of cores.

18. (Original) The system of claim 1 further comprising transmitting data between the plurality of cores and one or more system components via a Peripheral Component Interface Express (PCIe) interface.

19. (Currently Amended) A machine comprising:

a processor comprising:

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem to store the instructions and data, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores; and

cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

Petitioner Samsung Ex-1004, 0143

an article of manufacture comprising a machine-readable storage medium storing a plurality of instructions, the plurality of instructions, ~~if performed~~ when performed by ~~a machine,~~ the machine, to cause the machine to perform operations comprising to:

enable a first frequency ~~to be set~~ of operation for a first ~~subset~~ cluster of the plurality of cores which are physically proximate to one another and a second frequency ~~to be set~~ of operation for a second ~~subset~~ cluster of the plurality of cores which are physically proximate to one another; and

selectively gate power to the first ~~subset~~ cluster of the plurality of ~~cores,~~ cores and cache portions that correspond to the first cluster and/or the second ~~subset~~ cluster of the plurality of cores and cache portions that correspond to the second cluster; ~~cores, and/or one or more of the cache portions;~~

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory; and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory.

20. (Original) The machine of claim 19 further comprising a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components.

Petitioner Samsung Ex-1004, 0144

REMARKS

The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

Double Patenting

Claims 1-4, 13-16, and 19-20 have been provisionally rejected on the ground of non-statutory double patenting as allegedly being unpatenable over claims 1-4, 13-16, and 21-23 of co-pending U.S. Patent Application Serial No. 13/729,579 in view of U.S. Patent Application Publication 2014/0089699 to O'Connor et al. (hereinafter "O'Connor").

Claims 1-20 have been provisionally rejected on the ground of non-statutory double patenting as allegedly being unpatenable over claims 1-20 of co-pending U.S. Patent Application Serial No. 15/947,829.

Claims 1-20 have been provisionally rejected on the ground of non-statutory double patenting as allegedly being unpatenable over claims 1-20 of co-pending U.S. Patent Application Serial No. 15/947,831.

Applicants respectfully submit that these rejections are provisional double-patenting rejections. Applicants will consider submitting a terminal disclaimer at another time if the double patenting rejections are maintained.

35 U.S.C. §112(b)/35 U.S.C. §112(pre-AIA), Second Paragraph - Definiteness

Claims 1-12 and 19-20 have been rejected under 35 U.S.C. §112(b)/35 U.S.C. §112(pre-AIA), Second Paragraph for allegedly being indefinite.

Applicants respectfully submit that claims 1 and 19 have has been amended to replace "*frequency to be set*" with "*frequency of operation*". Also, claim 19 has been amended to replace "*if performed*" with "*when performed*". Accordingly, Applicants respectfully request that the rejections in these regards be withdrawn.

Applicants respectfully submit that claims 1-12 and 19-20 are definite. In brief, the reasons articulated in the Office Action for the rejection of these claims is essentially that claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. However, Applicants respectfully submit that independent claim 1, and its dependent

Petitioner Samsung Ex-1004, 0145

claims, pertain to a system not to a method. Independent claim 19 and its dependent claim 20 pertain to a machine. Applicants respectfully submit that there is no requirement that a claim to a system or machine (or other apparatus) recite **that steps be performed**. Rather, system or machine (or other apparatus) claims are allowed to claim what the apparatus is capable of doing, operative to do, able to do, or otherwise "to" do, if it were in operation or use. Applicants respectfully submit that it is permissible to claim the apparatus in a way that covers the system or machine when in a powered-off or non-operational state in which no steps are being performed but rather claiming what the system or machine is capable of doing, operative to do, able to do, or otherwise "to" do if it were in operation or use. That is what is being done in claims 1-12 and 19-20. As understood by Applicants, such claims are definite and permitted. Accordingly, Applicants respectfully request that the rejection be withdrawn. Alternatively, if the Office intends to maintain the rejection, then Applicants respectfully request that the Office clearly indicate where in the laws or rules it is required that an apparatus claim recite **that steps be performed**.

35 U.S.C. §103(a) Rejection - Wang, O'Connor

Claims 1-6, 8, 12, 13, 15, and 19 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. 2005/0027941 to Wang et al (hereinafter "Wang") in view of U.S. Patent Application Publication No. 2014/0089699 to O'Connor et al. (hereinafter "O'Connor"). Without admitting that these references could or should be combined, the Applicants respectfully submit that the present claims are allowable over Wang and O'Connor.

Claim xxx recites:

"*1. A system comprising:*

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem to store the instructions and the data, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores;

Petitioner Samsung Ex-1004, 0146

cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores;

power management circuitry to enable a first frequency of operation for ***a first cluster of the plurality of cores which are physically proximate to one another*** *and a second frequency of operation for* ***a second cluster of the plurality of cores which are physically proximate to one another****, the power management circuitry to selectively gate power to the first cluster of the plurality of cores* ***and cache portions that correspond to the first cluster*** *and/or the second cluster of the plurality of cores* ***and cache portions that correspond to the second cluster****;*

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory; and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory."

Applicants respectfully submit that Wang and O'Connor do not disclose these limitations or render them obvious.

Firstly, for example, as understood by Applicants, Wang and O'Connor do not disclose or render obvious "*power management circuitry to enable a first frequency of operation for* ***a first cluster of the plurality of cores which are physically proximate to one another*** *and a second frequency of operation for* ***a second cluster of the plurality of cores which are physically proximate to one another****.*"

Secondly, for example, as understood by Applicants, Wang and O'Connor do not disclose or render obvious "*power management circuitry to selectively gate power to the first cluster of the plurality of cores* ***and cache portions that correspond to the first cluster*** *and/or the second cluster of the plurality of cores* ***and cache portions that correspond to the second cluster****.*"

For at least one or more of these reasons, independent claim 1 is believed to be allowable. The dependent claims of claim 1 each include all of the limitations of independent claim 1, and are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

Petitioner Samsung Ex-1004, 0147

Independent claims 13 and 19, and their respective dependent claims, are believed to be allowable for one or more similar reasons.

35 U.S.C. §103(a) Rejection - Wang, O'Connor, Cai

Claims 7 and 14 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wang and O'Connor as applied to claims 1 and 13 above, and in further view of U.S. Patent Application Publication No. 2009/072424 to Cai et al. (hereinafter "Cai").

Claims 7 and 14 are dependent claims. As discussed above, Wang and O'Connor do not disclose or render obvious the limitations of independent claims 1, 13, or 19. As understood by Applicants, Cai does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in Cai. Accordingly, without admitting that these references could or should be combined, Applicants respectfully submit that independent claims 1, 13, and 19 are believed to be allowable over Wang, O'Connor, and Cai. Dependent claims 7 and 14 are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims Without admitting that these references could or should be combined, the Applicants respectfully submit that the present claims are allowable over Wang, O'Connor, and Cai.

35 U.S.C. §103(a) Rejection - Wang, O'Connor, Rajamony

Claims 9-10 and 16-17 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wang and O'Connor as applied to claims 1 and 13 above, and in further view of U.S. Patent Application Publication No. 2011/0022773 to Rajamony et al. (hereinafter "Rajamony").

Claims 9-10 and 16-17 are dependent claims. As discussed above, Wang and O'Connor do not disclose or render obvious the limitations of independent claims 1, 13, or 19. As understood by Applicants, Rajamony does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in Rajamony. Accordingly, without admitting that these references could or should be combined, Applicants respectfully submit that independent claims 1, 13, and 19 are believed to be allowable over Wang, O'Connor, and Rajamony. Dependent claims 9-10 and 16-17 are believed

Petitioner Samsung Ex-1004, 0148

to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

35 U.S.C. §103(a) Rejection - Wang, O'Connor, Zhu

Claims 11, 18, and 20 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wang and O'Connor as applied to claims 1 and 19 above, and in further view of U.S. Patent 8,725,919 to Zhu et al. (hereinafter "Zhu").

Claims 11, 18, and 20 are dependent claims. As discussed above, Wang and O'Connor do not disclose or render obvious the limitations of independent claims 1, 13, or 19. As understood by Applicants, Zhu does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in Zhu. Accordingly, without admitting that these references could or should be combined, Applicants respectfully submit that independent claims 1, 13, and 19 are believed to be allowable over Wang, O'Connor, and Zhu. Dependent claims 11, 18, and 20 are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

Petitioner Samsung Ex-1004, 0149

Conclusion

In view of the foregoing, it is believed that all pending claims patentably define the subject invention over the cited art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn and the claims be allowed at the earliest possible date.

Request for Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (408) 471-9791 if there remains any issue with allowance of the case.

Request for An Extension of Time

The Applicants petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 50-6674 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage or any necessary fee, either now or during the pendency of this application, to our Deposit Account No. 50-6674.

Respectfully submitted,
Nicholson, DeVos, Webster, Elliott, LLP
Customer No. 124662

Dated: 12/26/2018

By /Brent E. Vecchia/
Brent E. Vecchia, Reg. No. 48,011
Tel.: (408) 471-9791 (Mountain Time)

Petitioner Samsung Ex-1004, 0150

Claims ******* depend from, and include all of the limitations of, independent claim XXX. As discussed above, REFERENCE1***** and REFERENCE2***** do not disclose or render obvious the limitations of independent claim XXX. As understood by Applicants, REFERENCE3***** does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in REFERENCE3*****. Accordingly, Applicants respectfully submit that independent claim XXX is believed to be allowable over REFERENCE1*****, REFERENCE2*****, and REFERENCE3*****. Dependent claims ******* are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

Petitioner Samsung Ex-1004, 0151

Electronic Patent Application Fee Transmittal

Application Number:	15947830
Filing Date:	08-Apr-2018
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Filer:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt	
EFS ID:	34698368
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia
Filer Authorized By:	
Attorney Docket Number:	P49345-C2
Receipt Date:	27-DEC-2018
Filing Date:	08-APR-2018
Time Stamp:	01:53:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$600
RAM confirmation Number	122718INTEFSW00005403506674
Deposit Account	506674
Authorized User	Brent Vecchia
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P49345C2_ROA.pdf	557814 daa131275fe94b74e9fcbda86b6981630ebe558a	yes	13

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Claims	2	6
Applicant Arguments/Remarks Made in an Amendment	7	13

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	31029 5da4500a6622e66f7732e9e5f0bd108f081525ec	no	2

Warnings:

Information:

Total Files Size (in bytes):	588843

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/947,830	Filing Date 04/08/2018	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 12/27/2018

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $100 =	0
Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $460 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
LAVINIA JOHNSON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: DIST.E.FILE **Document Description: Electronic Terminal Disclaimer - Filed**	PTO/SB/25 PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A PROVISIONAL DOUBLE PATENTING REJECTION OVER A PENDING "REFERENCE" APPLICATION AND TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15947830
Filing Date	08-Apr-2018
First Named Inventor	Herbert HUM
Attorney Docket Number	P49345-C2
Title of Invention	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
Intel Corporation	100 %

The owner(s) of percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of any patent granted on pending reference Application Number(s)

15947829 filed on 04/08/2018

15947831 filed on 04/08/2018

as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and any patent granted on the reference application are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of any patent granted on the instant application that would extend to the expiration date of the full statutory term of any patent granted on said reference application, "as the term of any patent granted on said reference application may be shortened by any terminal disclaimer filed prior to the grant of any patent on the pending reference application," in the event that any such patent granted on the pending reference application: expires for failure to pay a maintenance fee, is held unenforceable, is found invalid by a court of competent jurisdiction, is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321, has all claims canceled by a reexamination certificate, is reissued, or is in any manner terminated prior to the expiration of its full statutory term as shortened by any terminal disclaimer filed prior to its grant.

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

10073779

as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○ I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicants claims the following fee status:

○ Small Entity

○ Micro Entity

◉ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 48011

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

○ A joint inventor; all of whom are signing this request

Signature	/Brent E. Vecchia/

Name	Brent E. Vecchia

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15947830
Filing Date:	08-Apr-2018
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Filer:	Brent E. Vecchia/Richard Pagaduan
Attorney Docket Number:	P49345-C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15947830

Filing Date: 08-Apr-2018

Applicant/Patent under Reexamination: HUM

Electronic Terminal Disclaimer filed on January 4, 2019

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	34770269
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia/Richard Pagaduan
Filer Authorized By:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2
Receipt Date:	04-JAN-2019
Filing Date:	08-APR-2018
Time Stamp:	23:42:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	010719INTEFSW23423200
Deposit Account	506674
Authorized User	Richard Pagaduan
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	37018 059f2fcf9594af0d0ced30c5dda38403eb1655ca	no	3
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30611 16494d4feda4f1c5e50a3ed3addc166afb2be719	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	67629		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2	5561

124662 7590 02/26/2019

Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
02/26/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ndwe_docketing@cardinal-ip.com
patent@ndwe.com

Petitioner Samsung Ex-1004, 0166

Office Action Summary	**Application No.** 15/947,830	**Applicant(s)** HUM et al.	
	Examiner GURTEJ BANSAL	**Art Unit** 2139	**AIA Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12/27/2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-20 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-20 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/08/2018 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 10/24/2018.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Claim Rejections - 35 USC § 112

The following is a quotation of 35 U.S.C. 112(b):
(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-12 and 19-20 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

Claim 1, line 2 recites the limitation "a plurality of cores to execute". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Here, Applicant recites a plurality of cores to execute, but never actually recite that the cores actually perform the execution. Therefore, this language is construed to be non limiting. Applicant correction and/or clarification is required.

Claim 1, line 4 recites "a cache subsystem to store". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 9 recites "circuitry to provide". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 11 recites "circuitry to enable". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 13 recites "circuitry to selectively". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 16, recites "memory controller to couple". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 1, line 18, recites "memory controller to couple". Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claims 2-12 and 19-20 recite similar language. Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Applicant correction and/or clarification is required.

Claim 19 recites the limitation "the plurality of instructions, if performed by a machine..." Claim scope is not limited by claim language that suggests or makes optional but does not require steps to be performed. Therefore, all steps following this language are construed to be non-limiting.

Claim 20 depend from claim 19 and is rejected for the reasons cited above.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8, 12, 13, 15, and 19 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Wang et al. (US 2005/0027941) (hereafter Wang), in view of O'Connor et al. (US 2014/0089699) (hereafter O'Connor).

As per claims 1, 13 and 19, Wang teaches a processor comprising:

a plurality of cores to execute instructions and process data, the plurality of cores comprising symmetric multi-threaded cores ([0026]);

a cache subsystem to store the instructions and data, the cache subsystem comprising a plurality of first-level caches and at least one higher-level distributed cache comprising a plurality of cache portions shared by the plurality of cores, each first-level cache integral to one of the plurality of cores and each cache portion accessible to each of the plurality of cores (fig. 1);

cache management circuitry to provide coherent, non-uniform access to the plurality of cache portions by the plurality of cores ([0022] describes the use of ring topologies for a NUMA configuration);

a first integrated memory controller to couple the symmetric multi-threaded cores to a first system memory (fig. 4, 105a…105n); and

a second integrated memory controller to couple the symmetric multi-threaded cores to a second system memory (fig. 4, 105a…105n).

Wang does not explicitly teach

power management circuitry to enable a first frequency of operation for a first cluster of the plurality of cores which are physically proximate to one another and a second frequency of

operation for a second cluster of the plurality of cores which are physically proximate to one another, the power management circuitry to selectively gate power to the first cluster of the plurality of cores and cache portions that correspond to the first cluster and/or the second cluster of the plurality of cores and cache portions that correspond to the second cluster.

However, O'Connor teaches power management circuitry to enable a first frequency of operation for a first cluster of components which are physically proximate to one another and a second frequency of operation for a second cluster of components which are physically proximate to one another, the power management circuitry to selectively gate power to the first cluster of the plurality of components that correspond to the first cluster and/or the second cluster of components that correspond to the second cluster ([0042]; also see [0053]).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the power management circuitry of O'Connor with the processor of Wang because it increases efficiency by performing power configuration adjustments while satisfying the memory and computational requirements of the system and while minimizing power consumption and/or maximizing performance under a power constraint ([0015]).

As per claim 2, O'Connor teaches wherein the power management circuitry is to selectively gate power to one or more of the first and/or second clusters of the plurality of cores and corresponding cache portions ([0042]).

As per claim 3, Wang teaches wherein a first core of a first predetermined cluster is physically proximate to a first cache portion (fig. 1).

As per claim 4, Wang teaches a local core-cache interconnect to couple the first core to the first cache portion; and an on-die interconnect to couple one or more other cores to the first cache portion (fig. 3, on chip).

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As per claim 5, Wang teaches wherein the local core-cache interconnect and on-die interconnect provide different access latency and/or data throughput to the first cache portion (As illustrated in fig. 1, the data accessed in L2 is faster than L3).

As per claim 6, Wang teaches wherein the local core-cache interconnect is to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first cache portion than the on-die interconnect is to provide to the one or more other cores when the one or more other cores access the first cache portion (As illustrated in fig. 4 with remote fetches as response to a miss).

As per claim 8, Wang teaches wherein at least one of the plurality of cores comprises: an instruction fetch circuit to fetch instructions from a corresponding first level cache or a system memory; and a decode circuit to decode the instructions; and an execution circuit comprising a plurality of functional units to execute the instructions ([0030]).

As per claims 12 and 15, Wang teaches wherein the non-uniform access to the plurality of cache portions by the plurality of cores is based, at least in part, on each cache portion being coupled to a proximate cluster of the plurality of cores over a first interconnect having first characteristics and being coupled to a non-proximate cluster of the plurality of cores over a second interconnect having second characteristics ([0022] by definition of a ring interconnect this would occur).

Claims 7 and 14 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over the combination of Wang and O'Connor as applied to claims 1 and 13 above, and further in view of Cai et al. (US 2009/0172424) (hereafter Cai).

As per claims 7 and 14, the combination of Wang and O'Connor teaches all the limitations of claims 1 and 13. The combination does not explicitly teach wherein, based on a

workload on each of the first and second clusters of the plurality of cores, a thread is to be selectively migrated from the first cluster to the second cluster.

However, Cai teaches wherein, based on a workload on each of the first and second clusters of the plurality of cores, a thread is to be selectively migrated from the first cluster to the second cluster ([0022]).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the thread migration of Cai with the cores of the combination of Wang and O'Connor because it will improve thread synchronization and create opportunities to improve power efficiency ([0022]).

Claims 9-10 and 16-17 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over the combination of Wang and O'Connor as applied to claims 1 and 13 above, and further in view of Rajamony et al. (US 2011/0022773)(hereafter Rajamony).

As per claims 9 and 16, the combination of Wang and O'Connor teaches all the limitations of claims 6 and 13. The combination does not explicitly teach wherein the first cluster of the plurality of cores form a first virtual processor and the second cluster of the plurality of cores form a second virtual processor.

However, Rajamony teaches wherein the first cluster of the plurality of cores form a first virtual processor and the second cluster of the plurality of cores form a second virtual processor ([0040]) .

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the virtual processors of Rajamony with the cores of the combination of Wang and O'Connor because by using virtualization, multiple operating systems

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can run in the same server, eliminating the need to dedicate a single machine to one application ([0006]).

As per claims 10 and 17, Rajamony teaches wherein the execution circuit is to execute instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first cluster of the plurality of cores and to form the second virtual processor by combining the second cluster of the plurality of cores ([0040]).

Claims 11, 18 and 20 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over the combination of Wang and O'Connor as applied to claims 1 and 19 above, and further in view of Zhu et al. (US 8,725,919) (hereafter Zhu).

As per claims 11 and 20, the combination of Wang and O'Connor teaches all the limitations of claims 1 and 19. The combination does not explicitly teach a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components.

However, Zhu teaches a Peripheral Component Interface Express (PCIe) interface to couple the plurality of cores to one or more system components (col. 3, lines 10-25).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the PCIe interface of Zhu with the interconnect of the combination of Wang and O'Connor because it provides high speed connectivity (col. 3, lines 10-25).

As per claim 18, the combination of Wang and O'Connor teaches all the limitations of claim 1. Wang further teaches transmitting data between the plurality of cores and one or more system components (fig. 4).

The combination does not explicitly teach wherein the data is transmitted via a Peripheral Component Interface Express (PCIe) interface.

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However, Zhu teaches wherein the data is transmitted via a Peripheral Component Interface Express (PCIe) interface (col. 3, lines 10-25).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the PCIe interface of Zhu with the interconnect of the combination of Wang and O'Connor because it provides high speed connectivity (col. 3, lines 10-25).

Response to Arguments

In light of Terminal Disclaimer filed 01/04/2019, the Double Patenting rejection is withdrawn.

Applicant's arguments filed 12/27/2018 have been fully considered but they are not persuasive.

With respect to the 35 USC 112 rejection, the rejection is maintained. Claim scope is not limited by claim language that suggests or makes operation but does not require steps to be performed, or by claim language that does not limit a claim to a particular structure. In Applicant's arguments, Applicant explicitly states that the claimed subject matter is directed to embodiments when the system is in a power off state and not performing any instructions whatsoever. "[A]pparatus claims cover what a device is, not what a device does." Hewlett-Packard Co. v. Bausch & Lomb Inc., 909 F.2d 1464, 1469, 15 USPQ2d 1525, 1528 (Fed. Cir. 1990) (emphasis in original). In the power off state, the device is merely components which perform no steps whatsoever. Applicant never actually positively recites the steps being performed. Therefore, as applicant has clearly articulated that their intention is to have the scope of the claims covering powered off states, the actions taken by each component are merely intended uses and therefore, not limiting. For the purposes of examination, the Examiner is interpreting the claims such that the structure is limiting however, the intended uses of these

structures are nonlimiting. If Applicant would like the claims to be interpreted such that the steps recited are limiting, Examiner respectfully suggests amending the claims to positively recite the steps being performed. Applicant correction and/or clarification is required.

With respect to the prior art rejection, Applicant's arguments have been fully considered but are unpersuasive and as a result, the rejection is maintained.

Applicant argues that the combination of Wang and O'Connor does not teach "power management circuitry to enable a first frequency of operation for a first cluster of the plurality of cores which are physically proximate to one another and a second frequency of operation for a second cluster of the plurality of cores which are physically proximate to one another.

Examiner respectfully disagrees. O'Connor teaches dynamically controlling the operating frequency of a group of compute units and powering down other compute units. Therefore, one group has a dynamically adjusted first frequency and the other group has a frequency of 0. Applicant is also directed to paragraph [0053] of Wang which also teaches changing operating frequencies.

Applicant also submits that the cited prior art does not teach "power management circuitry to selectively gate power to the first cluster of the plurality of cores and cache portions that correspond to the first cluster and/or the second cluster of the plurality of cores and cache portions that correspond to the second cluster".

Examiner respectfully disagrees. Wang teaches cores with a plurality of cache portions and O'Connor teaches selectively gating power to components to reduce power consumption. Therefore, the combination does teach this limitation.

For at least these reason, the rejection is maintained.

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Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on M-F 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant				☐ CPA		☐ T.D.		☐ R.1.47		
CLAIM		DATE								
Final	Original	07/18/2018	02/21/2019							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
	8	✓	✓							
	9	✓	✓							
	10	✓	✓							
	11	✓	✓							
	12	✓	✓							
	13	✓	✓							
	14	✓	✓							
	15	✓	✓							
	16	✓	✓							
	17	✓	✓							
	18	✓	✓							
	19	✓	✓							
	20	✓	✓							

Petitioner Samsung Ex-1004, 0179

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	07/18/2018	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	07/18/2018	GB
NPL Search in Google Scholar (See Attached)	07/18/2018	GB
Inventor Search in PE2E	07/18/2018	GB
Application search in Global Dossier	07/18/2018	GB
Text Search in EAST (See Attached)	02/21/2019	GB

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioner Samsung Ex-1004, 0180

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	44	(US-15947830-$ | US-20020046324-$ | US-20020049859-$ | US-20030061423-$ | US-20040226026-$ | US-20060004796-$ | US-20060206635-$ | US-20070156964-$ | US-20080022261-$ | US-20080126750-$ | US-20080195719-$ | US-20090037658-$ | US-20090049248-$ | US-20090063715-$ | US-20090089470-$ | US-20090187642-$ | US-20090193064-$ | US-20090265514-$ | US-20090271646-$ | US-20100074106-$ | US-20100257316-$ | US-20110035555-$ | US-20110055482-$ | US-20110087840-$ | US-20110087843-$ | US-20110119397-$ | US-20110153936-$ | US-20110173394-$ | US-20110179199-$ | US-20110219208-$ | US-20110252216-$ | US-20110296406-$ | US-20130073811-$ | US-20130085999-$ | US-20130311724-$ | US-20140189239-$ | US-3037476-$ | US-3108610-$ | US-3219996-$ | US-3261024-$ | US-3429656-$ | US-3725919-$ | US-3862828-$ | US-5115790-$ | US-5542966-$).DID.	US-PGPUB; USPAT	OR	OFF	2019/02/21 00:19
S1	2	"20140089699".pn. "20090063715".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 13:46
S2	1	"20110055482".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 15:58
S3	40667	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:01
S4	11910	cores with threads	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S5	1842	S3 and S4	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S6	71	S3 and S4 and NUMA	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S7	1	"20050027941".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 18:53
S8	26	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:43
S9	320	cores with virtual with processor and VMM	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:46

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S10	104	PCIe with coupl$3 with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:14
S11	3187	PCIe with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:29
S12	62	PCIe with (faster greater) with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:30
S13	90	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:37
S14	6297	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	US-PGPUB; USPAT	OR	OFF	2018/07/18 00:17
S15	1	"20090132954".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/18 19:43
S16	154	ring with interconnect with cores with cache	US-PGPUB; USPAT	OR	OFF	2018/07/18 20:22
S17	162	ring with interconnect with cores with cache	US-PGPUB; USPAT	OR	OFF	2019/02/20 15:12
S18	44390	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2019/02/20 15:13
S19	13505	cores with threads	US-PGPUB; USPAT	OR	OFF	2019/02/20 15:13
S20	85	S18 and S19 and NUMA	US-PGPUB; USPAT	OR	OFF	2019/02/20 15:13

EAST Search History (Interference)

< This search history is empty>

2/ 21/ 2019 12:20:04 AM
C:\ Users\ gbansal\ Documents\ EAST\ Workspaces\ 15947830.wsp

Petitioner Samsung Ex-1004, 0182

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6115790		2000-09-05	SCHIMMEL; Curt F.	
	2	6542966		2003-04-01	CRAWFORD; John et al.	
	3	7055007		2006-05-30	FLAUTNER; Krisztian et al.	
	4	8037476		2011-10-11	SHAVIT; Nir N. et al.	
	5	8108610		2012-01-31	GLASCO; David B. et al.	
	6	8219996		2012-07-10	MORRIS; Dale C.	
	7	8261024		2012-09-04	SHAVIT; Nir N. et al.	
	8	8429656		2013-04-23	DULUK Jr.; Jerome F. et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

	9	8725919		2014-05-13	ZHU; Julianne J. et al.	
	10	8862828		2014-10-14	SARAF; Ravindra P. et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020046324		2002-04-18	BARROSO; Luiz Andre et al.	
	2	20020049859		2002-04-25	BRUCKERT; William et al.	
	3	20030061423		2003-03-27	RANKIN; Linda J. et al.	
	4	20040226026		2004-11-11	GLASS; Adam B. et al.	
	5	20060004796		2006-01-05	NAKAMURA; Shuji	
	6	20060206635		2006-09-14	ALEXANDER; Thomas et al.	
	7	20070156964		2007-07-05	SISTLA; Krishnakanth V.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0184

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

	8	20080022261		2008-01-24	GOODING; Thomas Michael	
	9	20080126750		2008-05-29	SISTLA; Krishnakanth	
	10	20080195719		2008-08-14	WU; Yuguang et al.	
	11	20090037658		2009-02-05	SISTLA; Krishnakanth	
	12	20090049248		2009-02-19	CLARK; Leo James et al.	
	13	20090063715		2009-03-05	DE; Cesare Joshua et al.	
	14	20090089470		2009-04-02	VEN; Adriaan Van De et al.	
	15	20090187642		2009-07-23	MCGRATH; Michael P.	
	16	20090193064		2009-07-30	CHEN; Ying et al.	
	17	20090265514		2009-10-22	BILES; Stuart David et al.	
	18	20090271646		2009-10-29	TALWAR; Vanish et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
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First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

	19	20100074106		2010-03-25	CHOU; Ching-Tsun et al.	
	20	20100257316		2010-10-07	ARIMILLI; Ravi K. et al.	
	21	20110035555		2011-02-10	WANG; Hong et al.	
	22	20110055482		2011-03-03	SO; Kimming et al.	
	23	20110087840		2011-04-14	GLASCO; David B. et al.	
	24	20110087843		2011-04-14	ZHAO; Li et al.	
	25	20110119397		2011-05-19	EVANS; John et al.	
	26	20110153936		2011-06-23	STARKE; William J.	
	27	20110173394		2011-07-14	GARA; Alan et al.	
	28	20110179199		2011-07-21	CHEN; Dong et al.	
	29	20110219208		2011-09-08	ASAAD; Sameh et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

	30	20110252216		2011-10-13	YLONEN; Tatu J. et al.	
	31	20110296406		2011-12-01	BHANDARI; Aditya et al.	
	32	20130073811		2013-03-21	BECKMANN; Bradford M. et al.	
	33	20130085999		2013-04-04	TUNG; Teresa et al.	
	34	20130311724		2013-11-21	WALKER; William L. et al.	
	35	20140189239		2014-07-03	HUM; Herbert H. et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	None						

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0187

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

	1	Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on February 09, 2016, 14 pages.	
	2	Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on October 18, 2017, 17 pages.	
	3	Non-Final Office Action from U.S. Patent Application No. 15/947,829 (Atty. Docket No. 42P49345C1), mailed July 19, 2018, 14 pages.	
	4	Non-Final Office Action from U.S. Patent Application No. 15/947,831 (Atty. Docket No. 42P49345C3), mailed August 02, 2018, 14 pages.	
	5	Non-Final Office Action received for U.S. Patent Application No. 13/584,656, mailed on February 13, 2014, 17 pages.	
	6	Non-Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on February 07, 2017, 16 pages.	
	7	Non-Final Office Action received for U.S. Patent Application No. 13/729,579, mailed on June 01, 2015, 13 pages.	
	8	Notice of Allowance from U.S. Patent Application No. 13/729,579 (Atty. Docket No. 42P49345), mailed May 02, 2018, 8 pages.	
	9	Notice of Allowance received for U.S. Patent Application No. 13/584,656, mailed on June 09, 2014, 11 pages.	
	10	TAM D., "Operating System Management of Shared Caches on Multicore Processors," University of Toronto, 2010, 170 pages.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345C2

EXAMINER SIGNATURE			
Examiner Signature	/GURTEJ BANSAL/	Date Considered	02/21/2019

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345C2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Brent E. Vecchia/	Date (YYYY-MM-DD)	2018-10-24
Name/Print	Brent E. Vecchia	Registration Number	48011

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0190

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0191

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/947,830	Filing Date 04/08/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	07/26/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 21	Minus	** 21	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/EMORY T LANE/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/947,830	Filing Date 04/08/2018	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $460 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	07/26/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 21	Minus	** 20	= 1		x $100 =	100
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	100

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TAMMY D MCBETH BROWN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	15/947,830	Filing Date	2018-04-08	Docket Number (if applicable)	P49345C2	Art Unit	2139
First Named Inventor	Herbert H. HUM			Examiner Name	Bansal GURTEJ		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☒ Other Any previously submitted but not yet considered IDSs

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 506674

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

Applicant Signature

Petitioner Samsung Ex-1004, 0194

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Brent E. Vecchia/	Date (YYYY-MM-DD)	2019-07-26
Name	Brent E. Vecchia	Registration Number	48011

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Petitioner Samsung Ex-1004, 0196

Electronic Patent Application Fee Transmittal

Application Number:	15947830
Filing Date:	08-Apr-2018
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Filer:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 2 months with $0 paid	1252	1	600	600
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1900**

Electronic Acknowledgement Receipt	
EFS ID:	36706168
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia
Filer Authorized By:	
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37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		P49345C2_RFOA.pdf	589345 5aba1ae4d8cd6aa494033736329ede8a2ea37ab8	yes	17

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
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Applicant Arguments/Remarks Made in an Amendment	10	17

Warnings:					
Information:					
2	Request for Continued Examination (RCE)	P49345C2_RCE.pdf	697647 c15d8488dba170f919850c7279d8f8e926755224	no	3
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	32678 64081fcf2a3de42192ba71a2d33e9d0992a909ac	no	2
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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RESPONSE UNDER 37 CFR § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP «2139»

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application:	Examiner: Bansal GURTEJ
First Named Inventor:	Art Unit: 2139
Herbert H. HUM	Confirmation No: 5561
Application No. 15/947,830	
Filed: 04/08/2018	

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P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION UNDER 37 CFR § 1.116

Sir:

In response to the Final Office Action mailed February 26, 2019, the Applicants respectfully request that the Examiner enter the following amendments and consider the following remarks.

CERTIFICATE OF SUBMISSION/TRANSMISSION (37 CFR 1.8A)

I hereby certify that this correspondence is, on the date shown below, being:

EFS WEB	***FACSIMILE***
X *submitted electronically via EFS Web to the Patent and Trademark Office.*	☐ *transmitted by facsimile to the Patent and Trademark Office.*

/Brent E. Vecchia/ 07/26/2019
Date

Petitioner Samsung Ex-1004, 0202

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A system comprising:

a plurality of cores, ~~cores to execute instructions and process data,~~ the plurality of cores comprising symmetric multi-threaded cores;

a cache ~~subsystem to store the instructions and the data,~~ subsystem, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of distributed cache portions that are physically distributed across a die and shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each distributed cache portion accessible to each of the plurality of cores;

cache management circuitry operative to provide coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;

power management circuitry operative to enable a first frequency of operation for a first cluster of the plurality of cores which are physically proximate to one another and a second frequency of operation for a second cluster of the plurality of cores which are physically proximate to one another, wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores, the power management circuitry operative to selectively gate power to the first cluster of the plurality of cores and distributed cache portions of the at least one higher level distributed cache that correspond to the first cluster

and/or the second cluster of the plurality of cores and distributed cache portions of the at least one higher level distributed cache that correspond to the second cluster;

a first integrated memory controller ~~to couple~~ coupled with the symmetric multi-threaded cores; and ~~cores to a first system memory; and~~

a second integrated memory controller ~~to couple~~ coupled with the symmetric multi-threaded cores. ~~cores to a second system memory.~~

2. (Cancelled)

3. (Previously Presented) The system of claim 1 wherein a first core of a first predetermined cluster is physically proximate to a first distributed cache portion.

4. (Currently Amended) The system of claim 3 further comprising:

a local core-cache interconnect ~~to couple~~ coupling the first core to the first distributed cache portion; and

an on-die interconnect ~~to couple~~ coupling one or more other cores to the first distributed cache portion.

5. (Currently Amended) The system of claim 4 wherein the local core-cache interconnect and the on-die interconnect provide different access latency and/or data throughput to the first distributed cache portion.

6. (Currently Amended) The system of claim 4 wherein the local core-cache interconnect is operative to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first distributed cache portion than the on-die interconnect is operative

to provide to the one or more other cores when the one or more other cores access the first distributed cache portion.

7. (Currently Amended) The system of claim 1 wherein, based on workload on each of the first and second clusters of the plurality of cores, the system is operative to selectively migrate a thread ~~is to be selectively migrated~~ from the first cluster to the second cluster.

8. (Cancelled)

9. (Previously Presented) The system of claim 8 wherein the first cluster of the plurality of cores form a first virtual processor and the second cluster of the plurality of cores form a second virtual processor.

10. (Currently Amended) The system of claim 9 wherein the execution circuit is operative to execute instructions to implement a virtual machine monitor (VMM), the VMM operative to ~~form the first virtual processor by combining~~ combine the first cluster of the plurality of cores into the the first virtual processor and ~~to form~~ combine ~~the second virtual processor by combining~~ the second cluster of the plurality of cores into the second virtual processor.

11. (Currently Amended) The system of claim 1 further comprising a Peripheral Component Interface Express (PCIe) interface ~~to couple~~ coupled with the plurality of cores. ~~cores to one or more system components.~~

12. (Currently Amended) The system of claim 1 wherein the non-uniform access to the plurality of distributed cache portions by the plurality of cores is based, at least in part, on each distributed cache portion being coupled to a proximate cluster of the plurality of cores over a first

interconnect having first characteristics and being coupled to a non-proximate cluster of the plurality of cores over a second interconnect having second characteristics.

13. (Currently Amended) A method comprising:

executing instructions and processing data with a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;

storing the instructions and the data in a cache subsystem, the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of distributed cache portions that are physically distributed across a die, each first level cache integral to one of the plurality of cores and each distributed cache portion accessible to each of the plurality of cores;

sharing the plurality of distributed cache portions among the plurality of cores;

providing coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;

enabling a first frequency to be set for a first cluster of the plurality of cores which are physically proximate to one another and a second frequency to be set for a second cluster of the plurality of cores which are physically proximate to one another, wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores;

selectively gating power to the first cluster of the plurality of cores and distributed cache portions that correspond to the first cluster and/or the second cluster of the plurality of cores and distributed cache portions that correspond to the second cluster;

controlling access by the symmetric multi-threaded cores to a first system memory with a first integrated memory controller; and

controlling access by the symmetric multi-threaded cores to a second system memory with a second integrated memory controller.

14. (Previously Presented) The method of claim 13 further comprising selectively migrated a thread from the first cluster to the second cluster based on a workload on each of the first and second clusters of the plurality of cores.

15. (Currently Amended) The method of claim 13 wherein said providing the non-uniform access to the plurality of distributed cache portions by the plurality of cores is based, at least in part, on each distributed cache portion accessing a proximate cluster of the plurality of cores over a first interconnect having first characteristics and accessing a non-proximate cluster of the plurality of cores over a second interconnect having second characteristics.

16. (Previously Presented) The method of claim 13 further comprising forming the first cluster of the plurality of cores as a first virtual processor and forming the second cluster of the plurality of cores as a second virtual processor.

17. (Previously Presented) The method of claim 16 further comprising executing instructions to implement a virtual machine monitor (VMM), the VMM to form the first virtual processor by combining the first cluster of the plurality of cores and to form the second virtual processor by combining the second cluster of the plurality of cores.

18. (Cancelled)

19. (Currently Amended) A machine comprising:

a processor comprising:

a plurality of cores, ~~cores to execute instructions and process data,~~ the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem, ~~subsystem to store the instructions and data,~~ the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of distributed cache portions that are physically distributed across a die and shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each distributed cache portion accessible to each of the plurality of cores; and

cache management circuitry configured to provide coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;

an article of manufacture comprising a machine-readable storage medium storing a plurality of instructions, the plurality of instructions, when performed by the machine, ~~to cause~~ causing the machine to perform operations ~~comprising to:~~ comprising:

enable a first frequency of operation for a first cluster of the plurality of cores which are physically proximate to one another and a second frequency of operation for a second cluster of the plurality of cores which are physically proximate to one another, wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores; and

selectively gate power to the first cluster of the plurality of cores and distributed cache portions that correspond to the first cluster and/or the second cluster of the plurality of cores and distributed cache portions that correspond to the second cluster;

a first integrated memory controller ~~to couple~~ coupled with the symmetric multi-threaded cores; and ~~cores to a first system memory; and~~

a second integrated memory controller ~~to couple~~ coupled with the symmetric multi-threaded cores. ~~cores to a second system memory.~~

20. (Currently Amended) The machine of claim 19 further comprising a Peripheral Component Interface Express (PCIe) interface ~~to couple~~ coupled with the plurality of cores. ~~cores to one or more system components.~~

21. (New) The system of claim 1, wherein each distributed cache portion is a cache slice and is physically co-located with one of the cores, wherein, based on workload on each of the first and second clusters of the plurality of cores, the system is operative to selectively migrate a thread from the first cluster to the second cluster, and wherein the first cluster of the plurality of cores form a first virtual processor and the second cluster of the plurality of cores form a second virtual processor.

22. (New) The system of claim 1, wherein, based on workload on each of the first and second clusters of the plurality of cores, the system is operative to selectively migrate a thread from the first cluster to the second cluster, and further comprising a Peripheral Component Interface Express (PCIe) interface coupled with the plurality of cores.

23. (New) The system of claim 1, wherein the first cluster of the plurality of cores form a first virtual processor and the second cluster of the plurality of cores form a second virtual processor, and further comprising a Peripheral Component Interface Express (PCIe) interface coupled with the plurality of cores.

24. (New) The system of claim 1, wherein each distributed cache portion is a cache slice and is physically co-located with one of the cores, wherein, based on workload on each of the first and second clusters of the plurality of cores, the system is operative to selectively migrate a thread from the first cluster to the second cluster, wherein the first cluster of the plurality of cores form a first virtual processor and the second cluster of the plurality of cores form a second virtual processor, and further comprising a Peripheral Component Interface Express (PCIe) interface coupled with the plurality of cores.

REMARKS

The Applicants respectfully request reconsideration of this application in view of the above amendments and the following remarks.

35 U.S.C. §112(b)/35 U.S.C. §112(pre-AIA), Second Paragraph - Definiteness

Claims 1-12 and 19-20 have been rejected under 35 U.S.C. §112(b)/35 U.S.C. §112(pre-AIA), Second Paragraph for allegedly being indefinite.

Without admitting the appropriateness of the rejection, Applicants respectfully submit that the claims have been amended to overcome the rejection. Accordingly, Applicants respectfully request that the rejections in these regards be withdrawn.

Additionally, Applicants respectfully clarify that claims 1-12 are directed to a system, and claims 19-20 are directed to a machine. These claims cover the system or machine, respectively, when it is in a powered-off or non-operational state. That is, these claims do not recite that any steps are actually being performed. Rather, these claims recite what the system or machine, respectively, is arranged to do, configured to do, able to do, or otherwise operative to do, if it were powered on and operational. As understood by Applicants, such claims are definite and permitted. Applicants are unaware of any requirement in the rules or laws that require an apparatus claim to recite that steps or operations are actually performed. If the rejection is maintained, Applicants respectfully request that the Examiner clearly provide a basis in the rules or laws requiring that an apparatus claim recite that steps or operations are actually performed.

35 U.S.C. §103(a) Rejection - Wang, O'Connor

Claims 1-6, 8, 12, 13, 15 and 19 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over U.S. Patent Application Publication No. US2005/0027941 to Wang et al., (hereinafter "Wang") in view of U.S. Patent Application Publication No. US2014/0089699 to O'Connor et al., (hereinafter "O'Connor"). Without admitting that these references could or should be combined, the Applicants respectfully submit that the present claims are allowable over Wang and O'Connor.

Claim 1 recites:

"*1. A system comprising:*

a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;

a cache subsystem, the cache subsystem comprising a plurality of first level caches and at least one higher level ***distributed*** *cache comprising a plurality of* ***distributed*** *cache portions* ***that are physically distributed across a die*** *and shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each distributed cache portion accessible to each of the plurality of cores;*

cache management circuitry operative to provide coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;

power management circuitry operative to enable a first frequency of operation for ***a first cluster of the plurality of cores which are physically proximate to one another*** *and a second frequency of operation for* ***a second cluster of the plurality of cores which are physically proximate to one another, wherein an average distance between cores in***

***the first cluster is less than an average distance between the plurality of cores**, the power management circuitry operative to selectively gate power to **the first cluster** of the plurality of cores **and distributed cache portions** of the at least one higher level distributed cache that correspond to the first cluster and/or **the second cluster** of the plurality of cores **and distributed cache portions** of the at least one higher level distributed cache that correspond to the second cluster;*

a first integrated memory controller coupled with the symmetric multi-threaded cores; and

a second integrated memory controller coupled with the symmetric multi-threaded cores."

Applicants respectfully submit that Wang and O'Connor do not disclose these limitations or render them obvious.

(1) Firstly, for example, as understood by Applicants, Wang and O'Connor do not disclose or render obvious "*power management circuitry operative to enable a first frequency of operation for **a first cluster of the plurality of cores which are physically proximate to one another** and a second frequency of operation for **a second cluster of the plurality of cores which are physically proximate to one another, wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores**, the power management circuitry operative to selectively gate power to **the first cluster** of the plurality of cores and distributed cache portions of the at least one higher level distributed cache that correspond to the first cluster and/or **the second cluster** of the plurality of cores and distributed cache portions of the at least one higher level distributed cache that correspond to the second cluster.*"

The Office Action has already admitted that Wang does not disclose these limitations. See e.g., the bottom of page 4 and the top of page 5 of the Office Action. The Office Action asserts that O'Connor discloses these limitations. However, O'Connor does not disclose or render obvious enabling frequencies of operation and power gating **clusters** of a plurality of cores. O'Connor discusses adjusting the frequency of compute units and disabling compute units, but does not disclose adjusting the frequency of a first **cluster** and a second **cluster** of the compute units, and does not disclose disabling power to the first **cluster** and/or the second **cluster** of the compute units. Moreover, O'Connor does not disclose or render obvious these limitations in which **an average distance between cores in the first cluster is less than an average distance between the plurality of cores**. There simply is no disclosure in O'Connor that a cluster have such an average distance.

(2) Secondly, for example, as understood by Applicants, Wang and O'Connor do not disclose or render obvious "*at least one higher level **distributed** cache comprising a plurality of **distributed** cache portions **that are physically distributed across a die***."

The Office Action has relied on Figure 1 of Wang to reject these limitations. See e.g., the middle of page 4 of the Office Action. However, Wang does not disclose or render obvious a **distributed** cache including **distributed** cache portions **that are physically distributed across a die**.

(3) Thirdly, for example, as understood by Applicants, Wang and O'Connor do not disclose or render obvious "*the power management circuitry operative to selectively gate power to the first cluster of the plurality of cores **and distributed cache portions** of the at least one higher level distributed cache that correspond to the first cluster and/or the second cluster of the plurality of*

cores ***and distributed cache portions*** *of the at least one higher level distributed cache that correspond to the second cluster*."

In the response to arguments section of the Office Action at the bottom of page 10 the Examiner asserts "*Wang teaches cores with a plurality of cache portions and O'Connor teaches selectively gating power to components to reduce power consumption. Therefore the combination does teach this limitation*." However, neither Wang or O'Connor disclose or render obvious a **distributed** cache including **distributed** cache portions **that are physically distributed across a die**. The cache portions inside the cores in Wang are not **distributed** cache portions of the at least one higher level **distributed** cache, but rather are **non-distributed L1 and L2 caches inside the cores**. Turning off cores and the **non-distributed L1 and L2 caches inside the cores** is not the same thing as, and does not render obvious, the claimed limitations of "*the power management circuitry operative to selectively gate power to the first cluster of the plurality of cores* ***and distributed cache portions*** *of the at least one higher level distributed cache that correspond to the first cluster and/or the second cluster of the plurality of cores* ***and distributed cache portions*** *of the at least one higher level distributed cache that correspond to the second cluster*."

For at least one or more of these reasons, independent claim 1 is believed to be allowable. The dependent claims of claim 1 each include all of the limitations of independent claim 1, and are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

Independent claims 13 and 19, and their respective dependent claims, are believed to be allowable for one or more similar reasons.

35 U.S.C. §103(a) Rejection - Wang, O'Connor, Cai

Claims 7 and 14 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wang and O'Connor as applied to claims 1 and 13 above, in further view of U.S. Patent Application Publication No. 2009/0172424 to Cai et al., (hereinafter "Cai"). Without admitting that these references could or should be combined, the Applicants respectfully submit that the present claims are allowable over Wang, O'Connor and Cai.

Claims 7 and 14 are dependent claims. As discussed above, Wang and O'Connor do not disclose or render obvious the limitations of independent claims 1, 13, or 19. As understood by Applicants, Cai does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in Cai. Accordingly, without admitting that these references could or should be combined, Applicants respectfully submit that independent claims 1, 13, and 19 are believed to be allowable over Wang, O'Connor, and Cai. Dependent claims 7 and 14 are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims Without admitting that these references could or should be combined, the Applicants respectfully submit that the present claims are allowable over Wang, O'Connor, and Cai.

35 U.S.C. §103(a) Rejection - Wang, O'Connor, Rajamony

Claims 9-10 and 16-17 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wang and O'Connor as applied to claims 1 and 13 above, in further view of U.S. Patent Application Publication No. 2011/0022773 to Rajamony et al., (hereinafter "Rajamony").

Claims 9-10 and 16-17 are dependent claims. As discussed above, Wang and O'Connor do not disclose or render obvious the limitations of independent claims 1, 13, or 19. As understood

by Applicants, Rajamony does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in Rajamony. Accordingly, without admitting that these references could or should be combined, Applicants respectfully submit that independent claims 1, 13, and 19 are believed to be allowable over Wang, O'Connor, and Rajamony. Dependent claims 9-10 and 16-17 are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

35 U.S.C. §103(a) Rejection - Wang, O'Connor, Cai

Claims 11, 18 and 20 have been rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wang and O'Connor as applied to claims 1 and 19 above, in further view of U.S. Patent No. 8,725,919 to Zhu et al., (hereinafter "Zhu").

Claims 11, 18, and 20 are dependent claims. As discussed above, Wang and O'Connor do not disclose or render obvious the limitations of independent claims 1, 13, or 19. As understood by Applicants, Zhu does not remedy all of what is missing from these references and/or the Examiner does not appear to have sufficiently articulated where all of these missing limitations are found in Zhu. Accordingly, without admitting that these references could or should be combined, Applicants respectfully submit that independent claims 1, 13, and 19 are believed to be allowable over Wang, O'Connor, and Zhu. Dependent claims 11, 18, and 20 are believed to be allowable for at least this reason, as well as for the recitations separately set forth in each of these dependent claims.

Conclusion

In view of the foregoing, it is believed that all pending claims patentably define the subject invention over the cited art of record and are in condition for allowance. Applicants respectfully request that the rejections be withdrawn, and the claims be allowed, at the earliest possible date.

Request for Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (408) 471-9791 if there remains any issue with allowance of the case.

Request for an Extension of Time

The Applicants petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 50-6674 to cover the necessary fee under 37 C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage or any necessary fee, either now or during the pendency of this application, to our Deposit Account No. 50-6674.

Respectfully submitted,
Nicholson, DeVos, Webster, Elliott, LLP
Customer No. 124662

Dated: 07/26/2019

By /Brent E. Vecchia/
Brent E. Vecchia, Reg. No. 48,011
Tel.: (408) 471-9791 (Mountain Time)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, Gurtej
Attorney Docket Number	P49345C2

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Petitioner Samsung Ex-1004, 0219

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, Gurtej
	Attorney Docket Number	P49345C2

	1	Final Office Action from U.S. Patent Application No. 15/947,829 (Atty. Docket No. 42P49345C1), mailed February 07, 2019, 20 pages.	
	2	Final Office Action from U.S. Patent Application No. 15/947,831 (Atty. Docket No. 42P49345C3), mailed February 28, 2019, 28 pages.	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

Petitioner Samsung Ex-1004, 0220

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, Gurtej
	Attorney Docket Number	P49345C2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Brent E. Vecchia/	Date (YYYY-MM-DD)	2019-07-31
Name/Print	Brent E. Vecchia	Registration Number	48011

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Petitioner Samsung Ex-1004, 0221

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Petitioner Samsung Ex-1004, 0222

Electronic Acknowledgement Receipt

EFS ID:	36735894
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia/Richard Pagaduan
Filer Authorized By:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2
Receipt Date:	31-JUL-2019
Filing Date:	08-APR-2018
Time Stamp:	20:18:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	P49345C2_IDS.pdf	1053199 3b505df171f9adecf73e99e0740931eaf3fa7064	no	4

Warnings:

Information:					
2	Non Patent Literature	FOA_15947829_07Feb2019_20pgs_EFS.pdf	766115 150a77713093586 1addbfad3a2e325f42fcbda34	no	20
Warnings:					
Information:					
3	Non Patent Literature	FOA_15947831_28Feb2019_pgs_EFS.pdf	1057266 c584f9acd2927be3d73a4f2b8760d1134e896db0	no	28
Warnings:					
Information:					
		Total Files Size (in bytes):	2876580		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

124662 7590 02/20/2020

Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 02/20/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2	5561

TITLE OF INVENTION: PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/20/2020

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Petitioner Samsung Ex-1004, 0225

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

124662 7590 02/20/2020
Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2	5561

TITLE OF INVENTION: PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	05/20/2020

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-122000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑Issue Fee ❑Publication Fee (if required) ❑Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

Petitioner Samsung Ex-1004, 0226

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2	5561

124662 7590 02/20/2020

Vecchia/NDWE/Intel
99 Almaden Boulevard, Suite 710
San Jose, CA 95113

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 02/20/2020

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioner Samsung Ex-1004, 0227

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/947,830	Applicant(s) HUM et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to Examiner initiated interview dated 02/14/2020.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1,3-7,9-17 and 19-24 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information , please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 07/31/2019.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☑ Interview Summary (PTO-413), Paper No./Mail Date. 02/14/20.
5. ☑ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Petitioner Samsung Ex-1004, 0229

EXAMINER'S AMENDMENT

Authorization for this examiner's amendment was given in an interview with Brent Vecchia on 02/14/2020.

The application has been amended as follows:

IN THE CLAIMS

In claim 9, line 1, replace "claim 8" with –claim 1--.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on M-F 8am-5pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)-272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

Petitioner Samsung Ex-1004, 0230

applications is available through Private PAIR only. For more information about the PAIR system, see https://ppair-my.uspto.gov/pair/PrivatePair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Examiner-Initiated Interview Summary	Application No. 15/947,830	Applicant(s) HUM et al.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA (FITF) Status No

All participants (applicant, applicant's representative, PTO personnel):

(1) GURTEJ BANSAL. (3) _____.

(2) BRENT VECCHIA. (4) _____.

Date of Interview: 14 February 2020.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☐ No.
If Yes, brief description: _____.

Issues Discussed ☐ 101 ☑ 112 ☐ 102 ☐ 103 ☐ Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 9.

Identification of prior art discussed: N/A.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Claim 9 as recited depended from claim 8 which had been previously canceled. It appeared as though claim 9 should depend from claim 1. Applicant authorized the Examiner to make the amendment via an Examiner's amendment to overcome the 112 rejection and place the Application in condition for allowance.

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioner Samsung Ex-1004, 0232

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC - Searched*		
Symbol	Date	Examiner
G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	07/18/2018	GB

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	07/18/2018	GB
NPL Search in Google Scholar (See Attached)	07/18/2018	GB
Inventor Search in PE2E	07/18/2018	GB
Application search in Global Dossier	07/18/2018	GB
Text Search in EAST (See Attached)	02/21/2019	GB
Updated Text Search in EAST (See Attached)	02/13/2020	GB
Updated NPL Search in Google Scholar (See Attached)	02/13/2020	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioner Samsung Ex-1004, 0233

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084. cpc.	02/13/2020	GB

/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	

Petitioner Samsung Ex-1004, 0234

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

CPC								
Symbol							Type	Version
G06F	/	12	/	0831			F	2013-01-01
G06F	/	12	/	0811			I	2013-01-01
G06F	/	12	/	084			I	2013-01-01

CPC Combination Sets								
Symbol							Type	Set	Ranking	Version
	/		/							

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	21	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	14 February 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200213

Petitioner Samsung Ex-1004, 0235

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

INTERNATIONAL CLASSIFICATION				
CLAIMED				
G06F	/	12	/	00

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	21	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	14 February 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office — Part of Paper No.: 20200213

Petitioner Samsung Ex-1004, 0236

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/947,830	HUM et al.
	Examiner	Art Unit
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	10	10	20	19										
	2	3	11	21	20										
11	3	4	12	5	21										
12	4	15	13	6	22										
13	5	16	14	7	23										
14	6	17	15	8	24										
2	7	18	16												
	8	19	17												
9	9		18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	21	
/GURTEJ BANSAL/ Primary Examiner, Art Unit 2139	14 February 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

U.S. Patent and Trademark Office Part of Paper No.: 20200213

Petitioner Samsung Ex-1004, 0237

Google Scholar | symmetric multithreaded cores

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Did you mean: symmetric ***multi threaded*** cores

Towards **symmetric multi-threaded** optimistic simulation kernels [PDF] ieee.org Full-Text @ USPTO-STIC
R Vitali, A Pellegrini, F Quaglia - 2012 ACM/IEEE/SCS 26th ..., 2012 - ieeexplore.ieee.org
... false cache sharing across the worker threads within the same **symmetric multi-threaded** kernel ... across different kernel instances, in our architecture they can be **symmetrically** issued by ... and fossil collection are con- cerned, we have implemented a **symmetric** scheme where ...
Cited by 59 Related articles All 14 versions

Condensed forms for the **symmetric** eigenvalue problem on **multi-threaded** architectures [PDF] epfl.ch
P Bientinesi, FD Igual, D Kressner... - Concurrency and ..., 2011 - Wiley Online Library
... A 22 − UW T − WU T where, in order to exploit the **symmetry**, only the ... The experimental results are reported for two target platforms representative of the recent **multithreaded** architectures ... Although our own implementations of the **symmetric** BLAS-3 kernels for the GPU deliver a ...
Cited by 27 Related articles All 16 versions

Method and system for managing thermal asymmetries in a multi-**core** processor [PDF] googleapis.com
DP Johnson, EC Saxe, B Smaalders - US Patent App. 11/863,010, 2009 - Google Patents
... in the multi-**core** processor thereby creating a **symmetrical** (or nearly **symmetrical** thermal profile ... Further, in order to maintain thermal **symmetry** (or near-thermal **symmetry**) of the multi ... capacity, and where migrating the load would result in a more **symmetric** thermal distribution of ...
Cited by 32 Related articles All 2 versions

Scheduling multiple **multithreaded** applications on asymmetric and **symmetric** chip multiprocessors [PDF] ieee.org Full-Text @ USPTO-STIC
TY Morad, A Kolodny, UC Weiser - 2010 3rd International ..., 2010 - ieeexplore.ieee.org
... **core** population embedded in state-of-the-art systems [17], the use of **multithreading** in applications is ... we strive to improve system performance as measured by several metrics when several **multithreaded** applications are run in parallel on **symmetric** multiprocessors, where ...
Cited by 10 Related articles All 12 versions

[BOOK] ACCMP-Asymmetric Cluster Chip Multi-Processing [PDF] technion.ac.il
TY Morad, UC Weiser, A Kolodny - 2004 - webee.eedev.technion.ac.il
... CMP processors divide the threads of **multithreaded** applications among the **symmetric cores**, exploiting their ... leading microprocessor manufacturers are either already offering CMP processors or have announced plans to do so [1]. When adding an additional **core** to a ...
Cited by 25 Related articles All 7 versions

Multi-socket **symmetric** multiprocessing (SMP) system for chip **multi-threaded** (CMT) processors [PDF] googleapis.com
RC Hetherington, SE Phillips - US Patent 7,398,360, 2008 - Google Patents
... For example, in the **symmetric** multiprocessing (SMP) model, processors are considered equals and any ... Such a **core** may also be referred to as a **multithreaded** (MT) **core** ... may help provide the higher memory bandwidth requirements often exhibited by **multi-threaded** execution ...
Cited by 9 Related articles All 4 versions

Accelerating critical section execution with asymmetric multi-**core** architectures [PDF] acm.org Full-Text @ USPTO-STIC
MA Suleman, O Mutlu, MK Qureshi... - ACM SIGARCH Computer ..., 2009 - dl.acm.org
... when MySQL is executed on multiple **cores** of a **symmetric** CMP (SCMP) ... the performance bottlenecks of critical sec- tions to improve **multi-threaded** application performance ... high-performance contexts of execution (multiple large **cores** or simultaneous **multithreading** ...

Petitioner Samsung Ex-1004, 0238

Cited by 341 Related articles All 18 versions

[PDF] Preparing for the second stage of multi-**core** hardware: Asymmetric (heterogeneous) **cores** [PDF] semanticscholar.org

M Gillespie - Intel white paper, 2008 - pdfs.semanticscholar.org

… Looking ahead to the future of **symmetric** multi-**core** processors, however, one can … EXOCHI: Architecture and programming environment for a heterogeneous multi-**core multithreaded** system … from Intel Press, helps software developers write high-performance **multi-threaded** code …

Cited by 27 Related articles All 2 versions

Load sharing for optimistic parallel simulations on multi **core** machines [PDF] acm.org Full-Text @ USPTO-STIC

R Vitali, A Pellegrini, F Quaglia - ACM SIGMETRICS Performance …, 2012 - dl.acm.org

… we need to determine how to opti- mize the usage of the assigned CPU-**cores** within each … the reduction of synchronization costs borrows from the design principles proper of multi-processor/ multi- **core** Operating Systems … **symmetric multi-threaded** kernel interrupt handling layer …

Cited by 21 Related articles All 11 versions

GenerOS: An asymmetric operating system kernel for multi-**core** systems [PDF] ieee.org Full-Text @ USPTO-STIC

Q Yuan, J Zhao, M Chen, N Sun - 2010 IEEE International …, 2010 - ieeexplore.ieee.org

… over shared data structures protected by locks, conventional sym- metric **multithreaded** operating system … of GenerOS mainly benefits from: (1) Applications run on their own **cores** with minimal … process so that there will be fewer contentions than conventional **symmetric** kernel; (3 …

Cited by 22 Related articles All 9 versions

Did you mean to search for: symmetric ***multi threaded*** cores

Petitioner Samsung Ex-1004, 0239

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	"20140089699".pn. "20090063715".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 13:46
S2	1	"20110055482".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 15:58
S3	40667	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:01
S4	11910	cores with threads	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S5	1842	S3 and S4	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S6	71	S3 and S4 and NUMA	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S7	1	"20050027941".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 18:53
S8	26	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:43
S9	320	cores with virtual with processor and VMM	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:46
S10	104	PCIe with coupl$3 with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:14
S11	3187	PCIe with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:29
S12	62	PCIe with (faster greater) with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:30
S13	90	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:37
S14	6297	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	US-PGPUB; USPAT	OR	OFF	2018/07/18 00:17
S15	1	"20090132954".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/18 19:43
S16	154	ring with interconnect with cores with cache	US-PGPUB; USPAT	OR	OFF	2018/07/18 20:22
S17	235	arbitration same distribution same memory	US-PGPUB; USPAT	OR	OFF	2018/07/26 20:09
S18	100	arbitration with unit same memory and distribution with unit same memory	US-PGPUB; USPAT	OR	OFF	2018/07/26 20:13
S19	44	(US-15947831-$ | US-20020046324-$ | US-20020049859-$ | US-20030061423-$ | US-20040226026-$ | US-20060004796-$ | US-20060206635-$ | US-20070156964-$ | US-20080022261-$ | US-20080062927-$ | US-20080126750-$ | US-20080195719-$ | US-20090037658-$ | US-20090049248-$ | US-20090063715-$ | US-20090089470-$ | US-20090187642-$ | US-20090193064-$ | US-20090265514-$ | US-20090271646-$ |	US-PGPUB; USPAT	OR	OFF	2019/02/22 13:24

Petitioner Samsung Ex-1004, 0240

		US-20100074106-$ | US-20100257316-$ | US-20110035555-$ | US-20110055482-$ | US-20110087840-$ | US-20110087843-$ | US-20110119397-$ | US-20110153936-$ | US-20110173394-$ | US-20110179199-$ | US-20110219208-$ | US-20110252216-$ | US-20110296406-$ | US-20130073811-$ | US-20130085999-$ | US-20130311724-$ | US-20140189239-$ | US-3037476-$ | US-3108610-$ | US-3219996-$ | US-3261024-$ | US-3429656-$ | US-3862828-$ | US-5115790-$ | US-5542966-$).DID.				
S20	0	arbitration same distribution same memory same count with threshold	US-PGPUB; USPAT	OR	OFF	2019/02/24 12:52
S21	2	arbitration same distribution same memory same (count number) with threshold	US-PGPUB; USPAT	OR	OFF	2019/02/24 12:52
S22	0	RAM with (tile bank) with (clash) with (count number) with threshold	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 12:54
S23	0	RAM with (tile bank) with (clash$3) with (count number) with threshold	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 12:54
S24	17	RAM with (tile bank) with (count number) with threshold	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 12:54
S25	17	RAM with (tile bank) with clash	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 13:04
S26	43935	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2019/02/24 13:21
S27	13088	cores with threads	US-PGPUB; USPAT	OR	OFF	2019/02/24 13:21
S28	82	S26 and S27 and NUMA	US-PGPUB; USPAT	OR	OFF	2019/02/24 13:21
S33	50783	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/10 00:42
S34	16258	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/10 00:42
S35	99	S33 and S34 and NUMA	US-PGPUB; USPAT	OR	OFF	2020/02/10 00:42
S36	50783	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/10 10:51
S37	16258	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/10 10:51
S38	99	S36 and S37 and NUMA	US-PGPUB;	OR	OFF	2020/02/10

Petitioner Samsung Ex-1004, 0241

			USPAT			10:51
S39	136	core with die same cluster	US-PGPUB; USPAT	OR	OFF	2020/02/10 11:14
S40	246	core with die same cluster	US-PGPUB; USPAT	OR	ON	2020/02/11 13:02
S41	81	core with die same cluster same cache	US-PGPUB; USPAT	OR	ON	2020/02/12 00:27
S42	40	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2020/02/12 00:32
S43	50924	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:26
S44	16303	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:26
S45	100	S43 and S44 and NUMA	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:26
S46	50924	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29
S47	16303	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29
S48	100	S46 and S47 and NUMA	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29
S49	646	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25865	symmetric.clm.	USPAT	OR	OFF	2020/02/13 23:33
L2	3784	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	USPAT	OR	OFF	2020/02/13 23:33
L3	29	L1 and L2	USPAT	OR	OFF	2020/02/13 23:33
L4	4	L1 and L2 and cores.clm.	USPAT	OR	OFF	2020/02/13 23:33
S29	3314	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	USPAT	OR	OFF	2019/02/24 13:29
S30	11599	tile.clm.	USPAT	OR	OFF	2019/02/24 13:30
S31	102	clash.clm.	USPAT	OR	OFF	2019/02/24 13:30
S32	0	S29 and S30 and S31	USPAT	OR	OFF	2019/02/24 13:31
S50	3784	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	USPAT	OR	OFF	2020/02/13 11:18

2/13/2020 11:35:15 PM
C:\Users\gbansal\Documents\EAST\Workspaces\15947831.wsp

Petitioner Samsung Ex-1004, 0242

EAST Search History

EAST Search History (Prior Art)

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S1	2	"20140089699".pn. "20090063715".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 13:46
S2	1	"20110055482".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 15:58
S3	40667	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:01
S4	11910	cores with threads	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S5	1842	S3 and S4	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S6	71	S3 and S4 and NUMA	US-PGPUB; USPAT	OR	OFF	2018/07/15 16:02
S7	1	"20050027941".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/15 18:53
S8	26	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:43
S9	320	cores with virtual with processor and VMM	US-PGPUB; USPAT	OR	OFF	2018/07/15 21:46
S10	104	PCIe with coupl$3 with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:14
S11	3187	PCIe with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:29
S12	62	PCIe with (faster greater) with speed	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:30
S13	90	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2018/07/17 23:37
S14	6297	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	US-PGPUB; USPAT	OR	OFF	2018/07/18 00:17
S15	1	"20090132954".pn.	US-PGPUB; USPAT	OR	OFF	2018/07/18 19:43
S16	154	ring with interconnect with cores with cache	US-PGPUB; USPAT	OR	OFF	2018/07/18 20:22
S17	235	arbitration same distribution same memory	US-PGPUB; USPAT	OR	OFF	2018/07/26 20:09
S18	100	arbitration with unit same memory and distribution with unit same memory	US-PGPUB; USPAT	OR	OFF	2018/07/26 20:13
S19	44	(US-15947831-$ | US-20020046324-$ | US-20020049859-$ | US-20030061423-$ | US-20040226026-$ | US-20060004796-$ | US-20060206635-$ | US-20070156964-$ | US-20080022261-$ | US-20080062927-$ | US-20080126750-$ | US-20080195719-$ | US-20090037658-$ | US-20090049248-$ | US-20090063715-$ | US-20090089470-$ | US-20090187642-$ | US-20090193064-$ | US-20090265514-$ | US-20090271646-$ |	US-PGPUB; USPAT	OR	OFF	2019/02/22 13:24

Petitioner Samsung Ex-1004, 0243

		US-20100074106-$ | US-20100257316-$ | US-20110035555-$ | US-20110055482-$ | US-20110087840-$ | US-20110087843-$ | US-20110119397-$ | US-20110153936-$ | US-20110173394-$ | US-20110179199-$ | US-20110219208-$ | US-20110252216-$ | US-20110296406-$ | US-20130073811-$ | US-20130085999-$ | US-20130311724-$ | US-20140189239-$ | US-3037476-$ | US-3108610-$ | US-3219996-$ | US-3261024-$ | US-3429656-$ | US-3862828-$ | US-5115790-$ | US-5542966-$).DID.				
S20	0	arbitration same distribution same memory same count with threshold	US-PGPUB; USPAT	OR	OFF	2019/02/24 12:52
S21	2	arbitration same distribution same memory same (count number) with threshold	US-PGPUB; USPAT	OR	OFF	2019/02/24 12:52
S22	0	RAM with (tile bank) with (clash) with (count number) with threshold	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 12:54
S23	0	RAM with (tile bank) with (clash$3) with (count number) with threshold	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 12:54
S24	17	RAM with (tile bank) with (count number) with threshold	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 12:54
S25	17	RAM with (tile bank) with clash	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2019/02/24 13:04
S26	43935	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2019/02/24 13:21
S27	13088	cores with threads	US-PGPUB; USPAT	OR	OFF	2019/02/24 13:21
S28	82	S26 and S27 and NUMA	US-PGPUB; USPAT	OR	OFF	2019/02/24 13:21
S33	50783	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/10 00:42
S34	16258	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/10 00:42
S35	99	S33 and S34 and NUMA	US-PGPUB; USPAT	OR	OFF	2020/02/10 00:42
S36	50783	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/10 10:51
S37	16258	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/10 10:51
S38	99	S36 and S37 and NUMA	US-PGPUB;	OR	OFF	2020/02/10

Petitioner Samsung Ex-1004, 0244

			USPAT			10:51
S39	136	core with die same cluster	US-PGPUB; USPAT	OR	OFF	2020/02/10 11:14
S40	246	core with die same cluster	US-PGPUB; USPAT	OR	ON	2020/02/11 13:02
S41	81	core with die same cluster same cache	US-PGPUB; USPAT	OR	ON	2020/02/12 00:27
S42	40	migrat$3 with thread with core with workload	US-PGPUB; USPAT	OR	OFF	2020/02/12 00:32
S43	50924	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:26
S44	16303	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:26
S45	100	S43 and S44 and NUMA	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:26
S46	50924	cache with instructions with data	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29
S47	16303	cores with threads	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29
S48	100	S46 and S47 and NUMA	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29
S49	646	PCIe with speed and PCIe with cores	US-PGPUB; USPAT	OR	OFF	2020/02/13 10:29

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S29	3314	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	USPAT	OR	OFF	2019/02/24 13:29
S30	11599	tile.clm.	USPAT	OR	OFF	2019/02/24 13:30
S31	102	clash.clm.	USPAT	OR	OFF	2019/02/24 13:30
S32	0	S29 and S30 and S31	USPAT	OR	OFF	2019/02/24 13:31
S50	3784	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	USPAT	OR	OFF	2020/02/13 11:18
S51	25865	symmetric.clm.	USPAT	OR	OFF	2020/02/13 23:33
S52	3784	G06F12/0831.cpc. G06F12/0811.cpc. G06F12/084.cpc.	USPAT	OR	OFF	2020/02/13 23:33
S53	29	S51 and S52	USPAT	OR	OFF	2020/02/13 23:33
S54	4	S51 and S52 and cores.clm.	USPAT	OR	OFF	2020/02/13 23:33

2/14/2020 8:14:57 PM
C:\Users\gbansal\Documents\EAST\Workspaces\15947829.wsp

Petitioner Samsung Ex-1004, 0245

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	HUM; Herbert H.
Art Unit	2139
Examiner Name	BANSAL, Gurtej
Attorney Docket Number	P49345C2

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	None				

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1	None						

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0246

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, Gurtej
	Attorney Docket Number	P49345C2

	1	Final Office Action from U.S. Patent Application No. 15/947,829 (Atty. Docket No. 42P49345C1), mailed February 07, 2019, 20 pages.	
	2	Final Office Action from U.S. Patent Application No. 15/947,831 (Atty. Docket No. 42P49345C3), mailed February 28, 2019, 28 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/GURTEJ BANSAL/	Date Considered	01/21/2020

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0247

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	HUM; Herbert H.
	Art Unit	2139
	Examiner Name	BANSAL, Gurtej
	Attorney Docket Number	P49345C2

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Brent E. Vecchia/	Date (YYYY-MM-DD)	2019-07-31
Name/Print	Brent E. Vecchia	Registration Number	48011

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0248

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B/

Petitioner Samsung Ex-1004, 0249

Doc Code: MFEE.C.AD
Document Description: Maintenance Fee Address Change

PTO/SB/47-EFS

FEE ADDRESS INDICATION FORM			
Application Number	15947830	Art Unit	2139
Filing Date	08-Apr-2018	Examiner Name	GURTEJ BANSAL
First Name Inventor	Herbert HUM	Attorney Doc. Number	P49345-C2

INSTRUCTIONS: In order for the fee address identified on this form to be effective, the issue fee must have been paid for the application listed on this form. Only an address represented by a customer number can be established as the fee address for maintenance fee purposes (hereafter, fee address). A fee address should be established when correspondence related to maintenance fees should be mailed to a different address than the correspondence address for the application. For more information on customer numbers, see the Manual of Patent Examining Procedure (MPEP) § 403.

Please recognize as the Fee Address under the provisions of 37 CFR 1.363 the address associated with:

Customer Number:	000197 CPA GLOBAL LIMITED 2318 Mill Road 12th Floor ALEXANDRIA VA 22314 UNITED STATES 7037392234

Signature :

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application.

Signature	/Brent E. Vecchia/	**Date**	05-20-2020
Name	Brent E. Vecchia	**Registration Number**	48011

Electronic Patent Application Fee Transmittal

Application Number:	15947830
Filing Date:	08-Apr-2018
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Filer:	Brent E. Vecchia/Richard Pagaduan
Attorney Docket Number:	P49345-C2

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt	
EFS ID:	39482574
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia/Richard Pagaduan
Filer Authorized By:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2
Receipt Date:	20-MAY-2020
Filing Date:	08-APR-2018
Time Stamp:	16:58:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	E20205JG58205709
Deposit Account	506674
Authorized User	Richard Pagaduan
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.20 (Post Issuance fees) 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Web85b.pdf	46096 69f8ca4922e2439d0abd5899888352cb0d31661a	no	2
Warnings:					
Information:					
2	Maintenance Fee Address Change	web85feeaddress.pdf	32467 8b2a4a678241aeb29a1a582d98b2226ec343353	no	1
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	31910 00efaa57b347f17985f0ba7ad001ff5b50b788cf	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	110473		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

Issue Fee Transmittal Form

Application Number	Filing Date	First Named Inventor	Atty. Docket No.	Confirmation No.
15947830	08-Apr-2018	Herbert HUM	P49345-C2	5561

TITLE OF INVENTION :

PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES

Entity Status	Application Type	Art Unit	Class - Subclass	EXAMINER
Regular Undiscounted	Utility under 35 USC 111(a)	2139	122000	GURTEJ BANSAL

Issue Fee Due	Publication Due	Total Fee(s) Due	Date Due	Prev. Paid Fee
$1000	$0	$1000	20-May-2020	$0

1.Change of Correspondence Address and/or Indication Of Fee Address (37 CFR 1.33 & 1.363)

Current Correspondence Address:	Current Indicated Fee Address :
124662 Vecchia/NDWE/Intel 99 Almaden Boulevard, Suite 710 San Jose CA 95113 UNITED STATES 408-675-0441 ndwe_docketing@cardinal-ip.com	
☐ Change of correspondence address requested, system generated AIA/122-EFS form attached	☒ Fee Address indication requested, system generated SB/47-EFS form attached

2.Entity Status

Change in Entity Status

○ Applicant certifying micro entity status; system generated Micro Entity certification form attached. See 37 CFR 1.29.
Note: Absent a valid certification of micro entity status, issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment. If this box is checked, you will be prompted to choose a micro entity status on the gross income basis (37 CFR 1.29(a)) or the institution of higher education basis (37 CFR 1.29(d)), and make the applicable certification online.

○ Applicant asserting small entity status. See 37 CFR 1.27.
Note: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

◉ Applicant changing to regular undiscounted fee status.
Note: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

Petitioner Samsung Ex-1004, 0255

Doc Code: IFEE PTOL/85B-EFS

Document Description: Issue Fee Payment (PTO-85B)

3.The Following Fee(s) Are Submitted:

☒ Issue Fee	☐ I authorize USPTO to apply my previously paid issue fee to the current fees due
☐ Publication Fee	☐ The Director is hereby authorized to apply my previously paid issue fee to the current fee due and to charge deficient fees to Deposit Account Number _____
☐ Advance Order - # of copies _____	☒ If **in addition to** the payment of the issue fee amount submitted with this form, there are any discrepancies in any amount(s) due, the Director is authorized to charge any deficiency or credit any overpayment, to Deposit Account Number 506674 . The **issue fee must be submitted** with this form. **If payment of the issue fee does not accompany this form, checking this box and providing a deposit account number will NOT be effective to satisfy full payment of the fee(s) due.**

4.Firm and/or Attorney Names To Be Printed

NOTE: If no name is listed, no name will be printed
For printing on the patent front page, list to be displayed as entered

1. NDWE, LLP
2.
3.

5.Assignee Name(s) and Residence Data To Be Printed

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

Name	City	State	Country	Category
Intel Corporation	Santa Clara	CALIFORNIA	united states	corporation

6.Signature

I certify, in accordance with 37 CFR 1.4(d)(4) that I am an attorney or agent registered to practice before the Patent and Trademark Office who has filed and has been granted power of attorney in this application. I also certify that this Fee(s) Transmittal form is being transmitted to the USPTO via EFS-WEB on the date indicated below.

Signature	/Brent E. Vecchia/	**Date**	05-20-2020
Name	Brent E. Vecchia	**Registration Number**	48011

Petitioner Samsung Ex-1004, 0256

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15947830
Filing Date	2018-04-08
First Named Inventor	Herbert H. HUM
Art Unit	2139
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	P49345-C2

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] i	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

Petitioner Samsung Ex-1004, 0257

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	Herbert H. HUM
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345-C2

	1	Notice of Allowance, US App. No. 15/947,829 (Atty. Docket No. P49345-C1), March 05, 2020, 5 pages.	
	2	Notice of Allowance, US App. No. 15/947,831 (Atty. Docket No. P49345C3), March 18, 2020, 5 pages.	

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15947830
	Filing Date	2018-04-08
	First Named Inventor	Herbert H. HUM
	Art Unit	2139
	Examiner Name	BANSAL, GURTEJ
	Attorney Docket Number	P49345-C2

CERTIFICATION STATEMENT

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☒ See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Brent E. Vecchia/	Date (YYYY-MM-DD)	2020-05-20
Name/Print	Brent E. Vecchia	Registration Number	48011

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Petitioner Samsung Ex-1004, 0260

Attorney Docket No: P49345-C2 Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application:	Examiner: Gurtej BANSAL
First Named Inventor:	Art Unit: 2139
Herbert H. HUM	Confirmation No: 5561
Application No. 15/947,830	
Filed: 04/08/2018	
For: PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES	

EFS Filing
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT PER 37 C.F.R. § 1.97(I)

Sir or Madam:

Pursuant to 37 C.F.R. § 1.97(i), this Information Disclosure Statement is being submitted to be placed in the file. Applicant understands this Information Disclosure Statement will not be considered by the Office.

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 or PTO/SB/08 together with copies of the documents cited on that form, except for copies not required to be submitted (e.g., copies of U.S. patents and U.S. published patent applications need not be enclosed).

Petitioner Samsung Ex-1004, 0261

Pursuant to 37 C.F.R. § 1.97(h), the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

If there are any additional charges, you are hereby authorized to charge Deposit Account No. 50-6674.

Respectfully submitted,
NICHOLSON DE VOS WEBSTER & ELLIOTT, LLP

Date: 5/20/2020

/Brent E. Vecchia/
Brent E. Vecchia
Reg. No. 48,011

Petitioner Samsung Ex-1004, 0262

Electronic Acknowledgement Receipt

EFS ID:	39495935
Application Number:	15947830
International Application Number:	
Confirmation Number:	5561
Title of Invention:	PROCESSORS HAVING VIRTUALLY CLUSTERED CORES AND CACHE SLICES
First Named Inventor/Applicant Name:	Herbert H. HUM
Customer Number:	124662
Filer:	Brent E. Vecchia/Richard Pagaduan
Filer Authorized By:	Brent E. Vecchia
Attorney Docket Number:	P49345-C2
Receipt Date:	20-MAY-2020
Filing Date:	08-APR-2018
Time Stamp:	16:08:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS_15947830_1.pdf	1043586 ee36c202b754b9e777b4d3af2dabe50d2332a3f5	no	4

Warnings:

Information:					
2	Transmittal Letter	Transmittal_15947830.pdf	20300 a492afd5c228b5309ec80691089269781942 1f08	no	2
Warnings:					
Information:					
3	Non Patent Literature	1_46120_408266.pdf	358976 d7cc7ecc06f1591168b8ce371618376d88d abc7b	no	5
Warnings:					
Information:					
4	Non Patent Literature	2_46811_421552.pdf	359110 6bd4cb76db4b9f13d4ff1c0afcdfb574c9eb 47ca	no	5
Warnings:					
Information:					
		Total Files Size (in bytes):	1781972		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	04/08/2018	Herbert H. HUM	P49345-C2	5561

7590 05/26/2020

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EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
05/26/2020	ELECTRONIC

NOTICE OF NON-COMPLIANT INFORMATION DISCLOSURE STATEMENT

An Information Disclosure Statement (IDS) filed 05/20/2020 in the above-identified application fails to meet the requirements of 37 CFR 1.97(d) for the reason(s) specified below. Accordingly, the IDS will be placed in the file, but the information referred to therein has not been considered.

The IDS is not compliant with 37 CFR 1.97(d) because:

☒ The IDS lacks a statement as specified in 37 CFR 1.97(e).

☐ The IDS lacks the fee set forth in 37 CFR 1.17(p).

☐ The IDS was filed after the issue fee was paid. Applicant may wish to consider filing a petition to withdraw the application from issue under 37 CFR 1.313(c) to have the IDS considered. See MPEP 1308.

/BC/
571-272-4200 or 1-888-786-0101
Application Assistance Unit
Office of Data Management

FORM PTOM327-B (Rev. 02/08)

Petitioner Samsung Ex-1004, 0265

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/947,830	07/07/2020	10705960	P49345-C2	5561

124662 7590 06/17/2020

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

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Petitioner Samsung Ex-1004, 0266