

Ex-1020: U.S. Patent No. 10,705,960 Claim Comparison Table

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| 1[preamble]: A system comprising:                                                                                                                                                                                                                                                                                                                                                                                 | 15[preamble]: A method comprising:                                                                                                                                                                                                                                                                                                                                                                                                                              | 20[preamble]: A machine comprising:                                                                                                                                                                                                                                                                                                                                                                                    |
|                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 20[a]: a processor comprising:                                                                                                                                                                                                                                                                                                                                                                                         |
| 1[a]: a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;                                                                                                                                                                                                                                                                                                                     | 15[a]: executing instructions and processing data with a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;                                                                                                                                                                                                                                                                                                                  | 20[b]: a plurality of cores, the plurality of cores comprising symmetric multi-threaded cores;                                                                                                                                                                                                                                                                                                                         |
| 1[b]: a cache subsystem,                                                                                                                                                                                                                                                                                                                                                                                          | 15[b]: storing the instructions and the data in a cache subsystem                                                                                                                                                                                                                                                                                                                                                                                               | 20[c]: a cache subsystem,                                                                                                                                                                                                                                                                                                                                                                                              |
| 1[c]: the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of distributed cache portions that are physically distributed across a die and shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each distributed cache portions accessible to each of the plurality of cores; | 15[c]: the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of distributed cache portions that are physically distributed across a die, each first level cache integral to one of the plurality of cores and each distributed cache portions accessible to each of the plurality of cores; sharing the plurality of distributed cache portions among the plurality of cores; | 20[d]: the cache subsystem comprising a plurality of first level caches and at least one higher level distributed cache comprising a plurality of distributed cache portions that are physically distributed across a die and shared by the plurality of cores, each first level cache integral to one of the plurality of cores and each distributed cache portions accessible to each of the plurality of cores; and |
| 1[d]: cache management circuitry operative to provide coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;                                                                                                                                                                                                                                                      | 15[d]: providing coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;                                                                                                                                                                                                                                                                                                                                         | 20[e]: cache management circuitry configured to provide coherent, non-uniform access to the plurality of distributed cache portions by the plurality of cores;                                                                                                                                                                                                                                                         |
|                                                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 20[f]: an article of manufacture comprising a machine-readable storage medium storing a plurality of instructions, the plurality of instructions, when performed by the machine, causing the machine to perform operations comprising:                                                                                                                                                                                 |
| 1[e]: power management circuitry operative to enable a first frequency of operation for a                                                                                                                                                                                                                                                                                                                         | 15[e]: enabling a first frequency to be set for a first cluster of the plurality of cores which are                                                                                                                                                                                                                                                                                                                                                             | 20[g]: enable a first frequency of operation for a first cluster of the plurality of cores which are                                                                                                                                                                                                                                                                                                                   |

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| first cluster of the plurality of cores which are physically proximate to one another and a second frequency of operation for a second cluster of the plurality of cores which are physically proximate to one another,                                                                                                                                                                                                     | physically proximate to one another and a second frequency to be set for a second cluster of the plurality of cores which are physically proximate to one another,                                                                                                           | physically proximate to one another and a second frequency of operation for a second cluster of the plurality of cores which are physically proximate to one another,                                                                                                      |
| 1[f]: wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores,                                                                                                                                                                                                                                                                                       | 15[f]: wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores;                                                                                                                                       | 20[h]: wherein an average distance between cores in the first cluster is less than an average distance between the plurality of cores; and                                                                                                                                 |
| 1[g]: the power management circuitry operative to selectively gate power to the first cluster of the plurality of cores and distributed cache portions of the at least one higher level distributed cache that correspond to the first cluster and/or the second cluster of the plurality of cores and distributed cache portions of the at least one higher level distributed cache that correspond to the second cluster; | 15[g]: selectively gating power to the first cluster of the plurality of cores and distributed cache portions that correspond to the first cluster and/or the second cluster of the plurality of cores and distributed cache portions that correspond to the second cluster; | 20[i]: selectively gate power to the first cluster of the plurality of cores and distributed cache portions that correspond to the first cluster and/or the second cluster of the plurality of cores and distributed cache portions that correspond to the second cluster; |
| 1[h]: a first integrated memory controller coupled with the symmetric multi-threaded cores; and a second integrated memory controller coupled with the symmetric multi-threaded cores.                                                                                                                                                                                                                                      | 15[h]: controlling access by the symmetric multi-threaded cores to a first system memory with a first integrated memory controller; and controlling access by the symmetric multi-threaded cores to a second system memory with a second integrated memory controller.       | 20[j]: a first integrated memory controller coupled with the symmetric multi-threaded cores; and a second integrated memory controller coupled with the symmetric multi-threaded cores.                                                                                    |
| 2. The system of claim 1, wherein, based on workload on each of the first and second clusters of the plurality of cores, the system is operative to selectively migrate a thread from the first cluster to the second cluster.                                                                                                                                                                                              | 16. The method of claim 15 further comprising selectively migrated a thread from the first cluster to the second cluster based on a workload on each of the first and second clusters of the plurality of cores.                                                             |                                                                                                                                                                                                                                                                            |
| 3. The system of claim 1 further comprising a Peripheral Component Interface Express (PCIe) interface coupled with the plurality of cores.                                                                                                                                                                                                                                                                                  | 21. The machine of claim 20 further comprising a Peripheral Component Interface Express (PCIe) interface coupled with the plurality of cores.                                                                                                                                |                                                                                                                                                                                                                                                                            |
| 4. The system of claim 1 wherein the non-uniform access to the plurality of cores is based,                                                                                                                                                                                                                                                                                                                                 | 17. The method of claim 15 wherein said providing the non-uniform access to the plurality                                                                                                                                                                                    |                                                                                                                                                                                                                                                                            |

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| <p>at least in part, on each distributed cache portion being coupled to a proximate cluster of the plurality of cores over a first interconnect having first characteristics and being coupled to a non-proximate cluster of the plurality of cores over a second interconnect having second characteristics.</p>                                          | <p>of distributed cache portions by the plurality of cores is based, at least in part, on each distributed cache portion accessing a proximate cluster of the plurality of cores over a first interconnect having first characteristics and accessing a non-proximate cluster of the plurality of cores over a second interconnect having second characteristics.</p>                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <p>6. The system of claim 1, wherein based on workload on each of the first and second clusters of the plurality of cores, the system is operative to selectively migrate a thread from the first cluster to the second cluster, and further comprising a Peripheral Component Interface Express (PCIe) interface coupled with the plurality of cores.</p> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <p>11. The system of claim 1 wherein a first core of a first predetermined cluster is physically proximate to a first distributed cache portion.</p>                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                  |
| <p>12. The system of claim 11 further comprising: a local core-cache interconnect coupling the first core to the first distributed cache portion; and an on-die interconnect coupling one or more other cores to the first distributed cache portion.</p>                                                                                                  | <table border="1"> <tr> <td data-bbox="592 732 1032 1201"> <p>13. The system of claim 12 wherein the local core-cache interconnect and the on-die interconnect provide different access latency and/or data throughput to the first distributed cache portion.</p> </td><td data-bbox="1039 732 1481 1201"> <p>14. The system of claim 12 wherein the local core-cache interconnect is operative to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first distributed cache portion than the on-die interconnect is operative to provide to the one or more other cores when the one or more other cores accesses the first distributed cache portion.</p> </td></tr> </table> | <p>13. The system of claim 12 wherein the local core-cache interconnect and the on-die interconnect provide different access latency and/or data throughput to the first distributed cache portion.</p> | <p>14. The system of claim 12 wherein the local core-cache interconnect is operative to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first distributed cache portion than the on-die interconnect is operative to provide to the one or more other cores when the one or more other cores accesses the first distributed cache portion.</p> |
| <p>13. The system of claim 12 wherein the local core-cache interconnect and the on-die interconnect provide different access latency and/or data throughput to the first distributed cache portion.</p>                                                                                                                                                    | <p>14. The system of claim 12 wherein the local core-cache interconnect is operative to provide relatively lower latency and/or higher data throughput to the first core when the first core accesses the first distributed cache portion than the on-die interconnect is operative to provide to the one or more other cores when the one or more other cores accesses the first distributed cache portion.</p>                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                  |