

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.
Petitioner,

v.

LIONRA TECHNOLOGIES LIMITED
Patent Owner.

Inter Partes Review No.:
IPR2023-00673
U.S. Patent No. 7,685,436

PETITIONER’S REPLY TO PATENT OWNER’S RESPONSE

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Petitioner's Exhibit List

<i>Exhibit #</i>	<i>Description</i>
1001	U.S. Patent No. 7,685,436 (“the ’436 Patent”)
1002	Select portions of prosecution history of the ’436 (“File History”)
1003	Declaration of Petitioner’s Expert Dr. Crovella (“Crovella”)
1004	U.S. 2003/0074473 (“Pham”)
1005	U.S. 7,424,744 (“Wu”)
1006	U.S. 7,996,670 (“Krishna”)
1007	U.S. 6,279,113 (“Vaidya”)
1008	U.S. Patent Publication 2002/0073316 (“Collins”)
1009	U.S. 7,181,017 (“Nagel”)
1010	US 2004/0039928A1 (“Elbe”)
1011	Related Patents
1012	Not used
1013	Not used
1014	Docket Control Order, <i>Lionra Technologies Limited v. Fortinet, Inc.</i> , Case No. 2:22-cv-00322 (E.D. Tex.) Document 55-1
1015	U.S. Patent Publication 2003/0145225A1 (“Bruton”)
1016	Deposition Transcript of Dr. Eric Cole
1017	Supplemental Declaration of Dr. Mark Crovella

I. Introduction

Patent Owner's Response (POR) confirms that the Challenged Claims are unpatentable. The POR relies on an embodiment of Pham where the ingress processor does all packet processing except for encryption and decryption. Thus, the POR ignores the broad teachings of Pham that every packet processing function except for "basic switching and routing" can be offloaded from the ingress processor to one or more packet processors. The offloaded packet processing includes compute intensive processes including compression, decompression, protocol translation, encryption, decryption, routing, load balancing, filtering and switching. Pham teaches that one or more of these packet processing functions can be performed by a data processing engine on packets that are sent from one LAN to another LAN or between a LAN and a WAN, for both clear text and encrypted packets, and thus Pham discloses the limitation that "substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines." There is no support for the POR's argument to the contrary.

As detailed in the DI, the Petition includes factual citations that fully support each ground, and the POR does not identify any additional evidence to overcome the strong showing in the Petition that all Challenged Claims are unpatentable.

II. Patent Owner Improperly Restricts The Teachings Of Pham

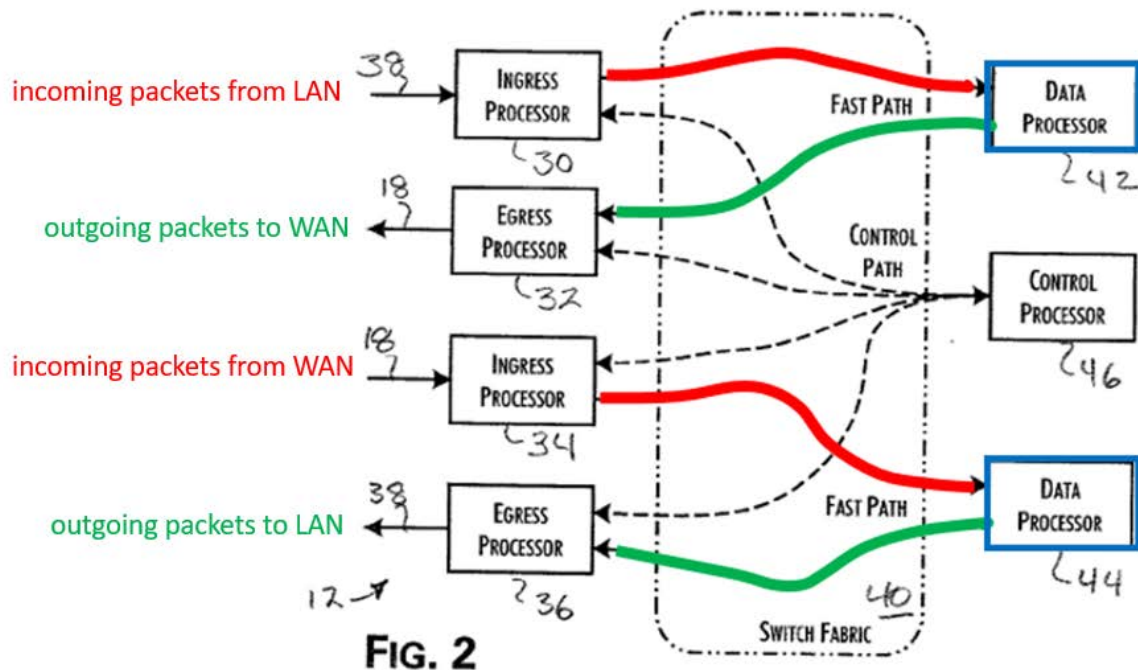
The POR main argument is that Pham fails to disclose the limitation that “substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines” because unencrypted packets bypass the packet engines. Specifically, the POR asserts that FIG. 1 of Pham shows an embodiment of transmission of clear text packets between LAN1 and LAN 2 or LAN 3 and LAN 4 and that “these unencrypted packets do not require processing through data packet (crypto) processors, so the unencrypted packets are filtered to bypass the data packet (crypto) processors and move between the ingress and egress processors that handle classification processing (highlighted in yellow) through the crossbar switch fabric.” POR 22. However, this argument lacks factual support.

As an initial matter, the POR does not dispute the Petition’s identification of “the network processors in the crypto processors as the claimed packet engines.” POR 25. Rather, the POR claims Pham does not teach “that ‘substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines.’” POR 27. The POR quibbles with the proportion of encrypted packets, but that does not negate that Pham teaches that “substantially all

of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines” in some embodiments.

Pham discloses multiple embodiments in which substantially all packets received by the security processor transit a packet engine. For example, Pham fully supports that the VPN gateways shown in FIG. 1 could work exclusively with the VPN tunnel without routing unencrypted packets to the Internet, in which case substantially all traffic would be processed by the packet engines and crypto cores identified in the Petition. The specification discusses cryptographic processing that meets or exceeds the overall throughput of the device which shows that fully saturated VPN throughput usage is disclosed. *See* [0052] (“Utilizing the BCM5840, each crypto processor 86 is capable of a minimum sustained effective IPsec encryption/decryption and IPsec authentication rate of 2.4 Gbps.”); [0045] (“For the preferred embodiment of the VPN gateway 72, which supports Gigabit Ethernet connections, each ingress and egress processor 80, 82 requires just a single port connection each to the switch fabric 78 to easily support the full bandwidth requirements of in-band network data traffic.”). The POR’s reliance on expert testimony regarding likely proportions of encrypted traffic do not negate the one hundred percent encryption capability the specification discloses. EX-1017 ¶8.

By way of another example, FIG. 2 of Pham illustrates another embodiment in which substantially all packets transit a packet engine. FIG. 2 shows incoming packets to an ingress processor from a LAN that are processed and are passed as outgoing packets through a VPN connection on the WAN. FIG. 2 also shows incoming packets from a WAN through a VPN connection that are processed and are passed as outgoing packets to a LAN. EX-1017 ¶9.



EX-1004 FIG. 2; EX-1017 ¶9.

FIG. 2 clearly shows an embodiment where all packets are being sent between LAN 38 and Internet 18, e.g., incoming packets (red) from LAN 38 and Internet 18 and outgoing packets (green) to Internet 18 and LAN 38, respectively,

transit one of the plurality of data processors 42, 44 (blue). Pham includes a very broad disclosure of the various packet processing that can be performed by the data processors. For example, Pham describes that data processors can be flexibly configured to implement any of a number of different network protocol processing functions including those that are compute intensive. EX-1004 [0017]; EX-1017 ¶10. A POSA understood that compute intensive processing would include compute intensive processes including compression, decompression, protocol translation, encryption, decryption, routing, load balancing, filtering and switching. EX-1004 [0042] EX-1016 22:19-29:25; EX-1017 ¶11. Pham also describes that data processors can perform single protocol conversion or multiple protocol conversion. For example, Pham describes that the same data processor can perform multiple protocol conversion such as compression before encryption and decompression after decryption. EX-1004 [0042]; EX-1017 ¶12. Thus, in the embodiment shown in FIG. 2 of Pham, the data processors could be crypto processors having a network processor (*packet engine*) receiving all incoming packets from LAN 38 and Internet 18 through ingress processor 30, 34, respectively, for packet processing including cryptographic processors and any other compute intensive processing. Thus, this embodiment discloses that “substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines.” EX-1017 ¶12

FIGs. 4 and 6 of Pham illustrates another example in which substantially all packets transit a packet engine in the crypto processor. FIG. 4 illustrates an example of packet processing between a single LAN 74 and WAN 76, and as discussed previously, VPN gateway 72 is capable of encrypting all traffic at line rate from the LAN side to the WAN side:

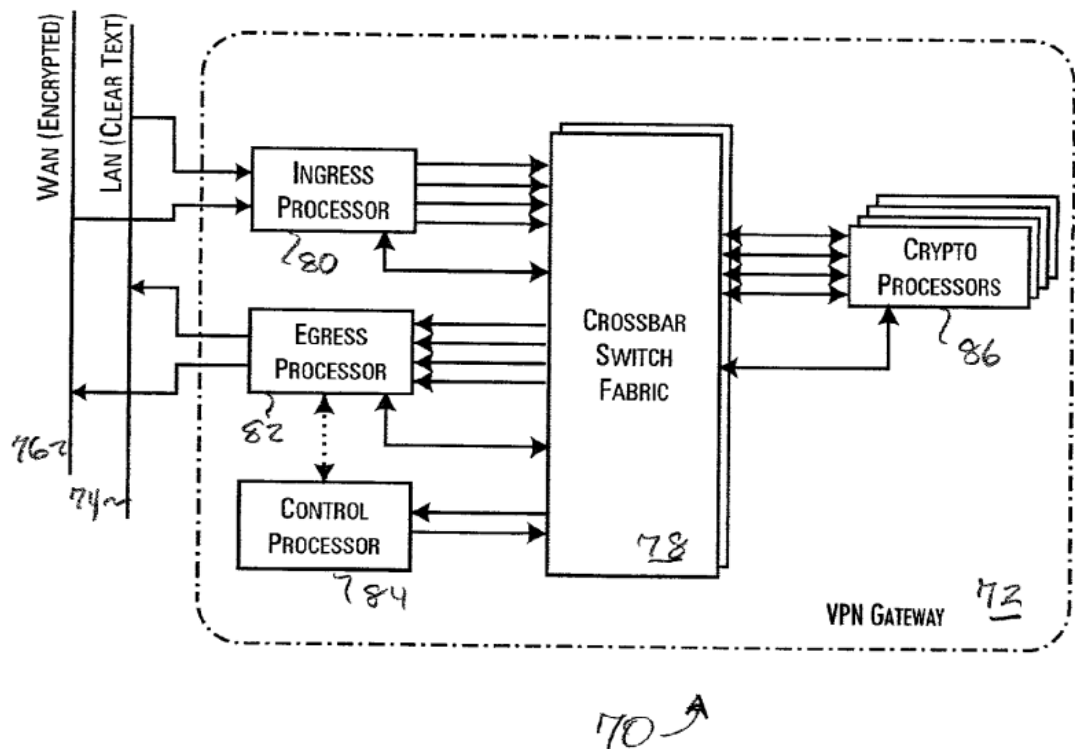


FIG. 4

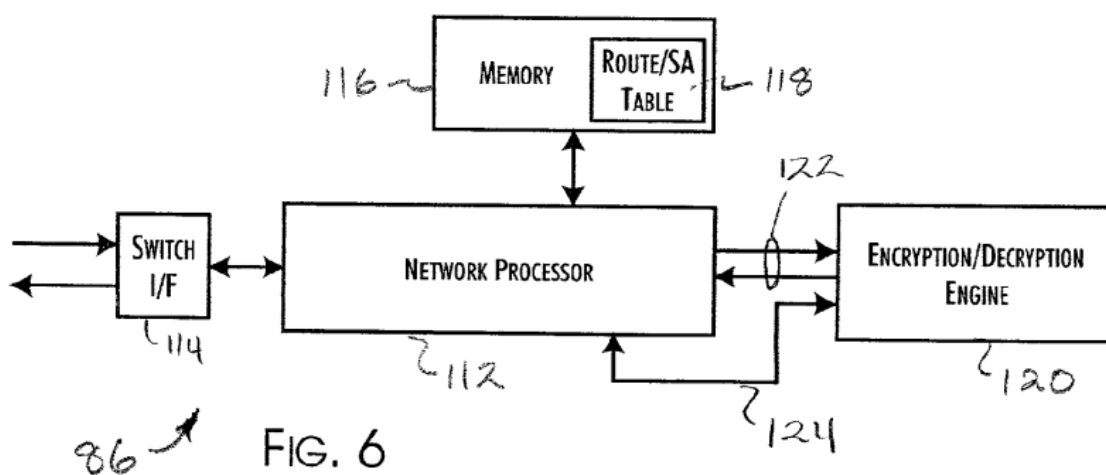
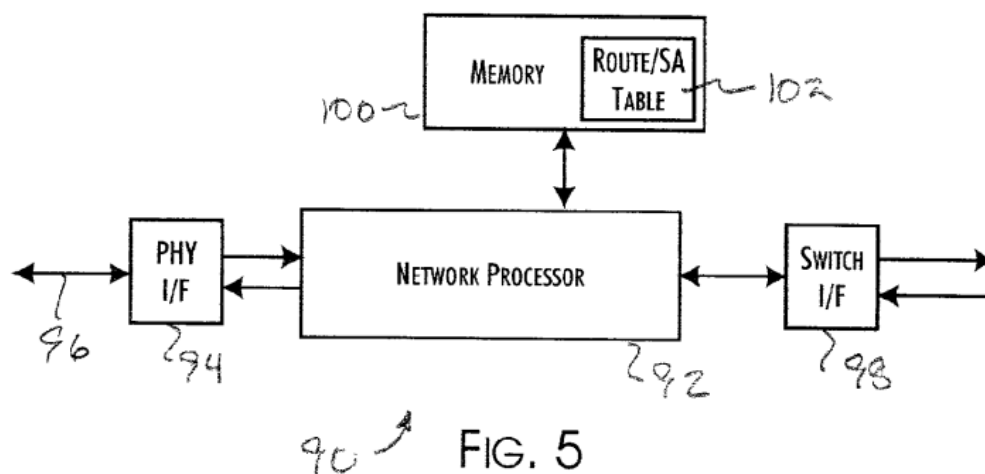
EX-1004 FIG. 4; EX-1017 ¶13.

Thus, because all traffic is encrypted, substantially all of the incoming packets and outgoing packets to the security processor transit one of the network processors (*packet engines*) in the crypto processor.

Further, Pham discloses that crypto processor 86 in FIG. 4 is a type of data processor illustrated in FIG 3¹, that can be flexibly configured to implement any of a number of different network protocol processing functions including those that are compute intensive. EX-1004 [0017], [0042] EX-1016 22:19-23:18; EX-1017 ¶14. Thus, a POSA understood crypto processor of FIG. 4 could perform packet processing functions other than encryption and decryption.

Further, FIG. 6 illustrates the crypto processor of FIG. 4 is nearly identical to the architecture used for the ingress processor shown in FIG. 5, including an identical network processor memory with route/SA table.

¹ Pham describes that FIG. 4 is a preferred VPN embodiment 70 of the present invention, representing a specific implementation of the extended protocol processor architecture 50 shown in FIG. 3. EX-1004 [0045].



EX-1004 FIGs. 5, 6; EX-1017 ¶15.

Pham discloses that in some embodiments, all packet processing except basic switching and filtering can be offloaded from the ingress processor to a data processor, which a POSA understood to mean that packet processing performed by the network processor 92 of the ingress processor 90 would be offloaded to the network processor 112 of the crypto processor 86. Thus, the crypto processor is

capable of performing any packet processing offloaded from the ingress processor, including routing, as conformed by PO's expert. EX-1016 83:13-21; EX-1017

¶16. The POR argument that "only the SA parameter association task may be offloaded to crypto processor 80" is therefore without factual support.² POR 26.

Although the POR restricts its analysis to an example where clear text packets are sent directly from LAN 1 to another LAN 2 to argue that no packet processing is needed, another packet processing function that would be performed by the crypto engine even for packets being sent from LAN 1 to LAN 2, would be protocol translation where LAN 1 uses a first protocol and LAN 2 uses a second protocol. This a common scenario, and yet PO's expert did not consider this scenario. EX-1016 88:8-13.

² PO's expert never analyzed an embodiment where packet processing other than association of SA parameters is offloaded from the ingress processor. EX-1016 52:3-22.

III. The POR Misrepresents the Scope of Claim 1

In the POR, Patent Owner takes a position that improperly narrows the claim scope of independent Claim 1 and 13. Specifically, the POR asserts that Claim 1 and 13 each recite the limitation that “substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines” and that Pham does not disclose this limitation.

PO’s argument is deficient for several reason.

First, the parties agreed that the claims should be given their plain and ordinary meaning. Yet, PO’s argument is premised on a construction that ignores the preamble which recites “[a] security processor to process incoming packets and outgoing packets, the security processor comprising:” which places no limits on the number or type of incoming packets and outgoing packets to be processed by the security processor. Thus, the preamble would read on two incoming packets that are processed by a security processor and sent as outgoing packets. Because the preamble (*a security processor to process incoming packets and outgoing packets*) provides antecedent basis for the limitation that “substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines,” this limitation would read on the same two incoming packets that are processed by a packet engine and sent as outgoing packets.

Recalling, with respect to this limitation the common adage “that which infringes if

later, would anticipate, if earlier,” nothing in the claims requires a certain number or type of packets be received by the security processor, and thus it is not sufficient for PO to limit its analysis to a scenario where incoming packets to the security processor do not require packet processing by a packet engine, as Pham identifies several embodiments where substantially all incoming packets to a security processor are sent to the network processor (*packet engine*) for packet processing.

The POR’s arguments regarding the patentability of dependent claims 2, 3, 9, 10, 12, 14, 16, 21 and 22, rely solely on the arguments discussed above with respect to the independent claims, and thus are likewise unpatentable for the reasons set forth above.

IV. The Petition Expressly Identifies the Motivation to Combine Pham and Wu

On pages 14-18, the Petition includes a section describing the State of the Art, including the common use of intrusion detection systems (IDS) having a signature database, and placing the IDS “at endpoints where encryption and decryption are performed such that it can inspect unencrypted traffic.” Pet. 18 (citing EX-1015). On pages 25-31, the Petition includes a section which details the motivation to modify the teachings of Pham to include an intrusion detection system and signature database interposed between the packet engine and the

cryptographic core, e.g., at the endpoint where encryption and decryption are performed. The POR does not address this State of the Art, nor the motivation to combine. In fact, PO's expert admitted that in his restricted analysis of the Petition, he did not did not have an opinion of the prior art cited in the state of the art. EX-1016 18:9-14; 19:24-20:6. Instead, the POR relies on its factually unsupported argument discussed above that Pham filters clear text packets. However, as discussed above, Pham provides several examples, e.g., using a VPN gateway to encrypt all traffic over the internet, that motivated a POSA to place the IDS to search for threats on the clear text side of the encrypted tunnel. Thus, the POR has not identified any evidence to rebut the strong factual showing in the Petition that demonstrates the motivation for a POSA to combine the teachings of Pham with the teachings of Wu.

In addition, the POR asserts that a POSA would not be motivated to modify the teachings of Pham with the teachings of Wu due to the increased complexity and resources required. POR 31. As an example, the POR cites to an example about adding compression and decompression. *Id.* However, Pham expressly describes the various types of packet processing that could be performed by Pham's data processors, including data compression, network data traffic switching and routing, various forms of protocol data processing and other computation intensive operations, and explains that this architecture could be employed for

reasons of architectural flexibility, simplicity, redundancy and increased capacity for handling control process flows and protocol negotiations. EX-1004 [0042]. A POSA understood the various types of packet processing would be implemented using known software algorithms, which is why Pham expressly highlights the simplicity of its architecture. EX-1017 ¶17. Thus, Pham's disclosure directly contradicts the POR argument.

V. Grounds 3 and 4 Are Fully Supported

The POR asserts that the Petition only includes a "terse discussion" of Krishna's teaching of putting security processor functions on a single chip. POR 35, 36. As an initial matter, PO's expert admitted that he restricted his review to Ground 1 and thus offered no evidence in support of PO's arguments regarding Grounds 3 and 4. EX-1016 17:23-18:14. On pages 15-19, the Petition include a section describing the State of the Art, including that it was known it was known to put security processing functions on a single chip, and that "cryptographic processing was moving away from discrete processors and was being implemented on a single chip." Pet. 17. (citing EX-1006 and EX-1010). The State of the Art includes an illustration including a packet engine, including database lookups and cryptographic engines and that these discrete processors were implemented on a single chip. As discussed in the Petition at pages 69-71, given the teaching in the State of the Art, and combined with the express teaching of Krishna that single

chip processor's overall performance can be enhanced, a POSA would be motivated to include security functions on a single chip. That rationale applies to all security functions, including an IDS, and not just those discrete elements recited in Claim 3, e.g., packet engine, cryptographic core and the modulo engine.

VI. The Petition Properly Includes Full Citations to the Expert's Declaration and Underlying Facts

The POR asserts that the Petition improperly relies on conclusory assertions that are copied verbatim from the declaration. The POR's argument is without legal or factual support.

Rule 37 CFR § 42.6(a)(3) prohibits argument that incorporate "by reference from one document into another document." Thus, in order for the expert's opinions to be considered by the Board, the opinions must be included in the Petition. The POR's three pages of citations cross-referencing Petitioner's expert's opinion to the Petition clearly demonstrates that the Petition complies with Rule 42.6(a)(3). The POR fails to acknowledge the requirements of Rule 42.6(a)(3).

The POR also mischaracterizes the precedential holding in *Xerox Corp. et al. v Bytemark, Inc.*, IPR2022-00624, Paper 9 (Aug. 24 , 2022). There, the Board found that an expert declaration was entitled to little weight because it merely repeated, *verbatim*, statements for which it was offered to support, which

the Board determined to be conclusory because the expert did not **“cite to any additional supporting evidence or provide any technical reasoning to support his statement.”** Id. at 15 (emphasis added). Although the POR asserts that the expert’s declaration is conclusory, the POR does not identify a single opinion offered by the expert that does not identify the underlying factual support or technical reasoning. To the contrary, even a cursory review of the citations identified on pages 37-40 of the POR demonstrate that the expert’s declaration, as well as the Petition, include citations to underlying factual support. For example, ¶30 of the declaration cites EX-1004 Fig. 6 as factual support, ¶31 of the declaration cites to EX-1005 4:4-7, ¶32 of the declaration cites to EX-1008 [0048] and EX-1006 FIG. 2; 3:43-50, and ¶34 of the declaration cites to EX-1001 6:38-45; EX-1012 6:38-45. Thus, the Petition fully complies with Rule 42.6(a)(3), and includes the underlying factual support or technical reasoning of its expert. The POR’s argument lacks both legal and factual support and should be rejected.

On the other hand, during the cross-examination of PO’s expert, it became clear that he was instructed to limit his analysis of the Petition, he did not consider any of the art outside of Ground 1, did not consider the prior art that Petitioners’ expert cited in support of Petitioner expert State of the Art section and failed to identify in his declaration, exactly what materials he reviewed in

support of his opinion. EX-1016 17:23-20:6; 12:11-14:6. The Board should take these consideration into account when affording PO expert's testimony the appropriate weight.

VII. Conclusion

The Petition includes factual citations that fully support each ground, and the POR does not identify any additional evidence to overcome the strong showing in the Petition that all Challenged Claims are unpatentable.

April 15, 2024

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CERTIFICATION OF SERVICE ON PATENT OWNER

Pursuant to 37 C.F.R. §§ 42.6(e), the undersigned certifies that on April 15, 2024, a complete and entire copy of Petitioner's Reply to Patent Owner's Response, was served by filing with P-TACTS along with a copy via electronic mail to the Patent Owner's counsel at the following addresses:

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April 15, 2024

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24 et seq., the undersigned certifies that this document complies with the type-volume limitations. This document contains 2870 words as calculated by the “Word Count” feature of Microsoft Word 2010, the word processing program used to create it.

Dated: April 15, 2024

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