UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CISCO SYSTEMS, INC.,

Petitioner,

v.

LIONRA TECHNOLOGIES LTD.,

Patent Owner.

Case IPR2023-00673
Patent 7,685,436

PATENT OWNER'S MOTION TO STRIKE PORTIONS OF PETITIONER'S REPLY BRIEF

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I. INTRODUCTION

Patent Owner Lionra Technologies Ltd. ("Lionra") submits this Motion to Strike Portions of Petitioner's Reply to Patent Owner's Response (Paper 16 in IPR2023-00673) authorized by the Board in an e-mail dated April 30, 2024.[1] Petitioner's Reply improperly attempts to fill holes in its original petition with new evidence and a new theory of obviousness. Rather than rebutting the substance of Patent Owner's Response ("POR"), Petitioner Cisco Systems, Inc. ("Cisco") seeks to sidestep the failures in its Petition by introducing new evidence and a new theory whose only proper place would have been the original petition. Thus, these portions of Petitioner's Reply cross the line from responsive to new, and should be struck.

II. STATEMENT OF RELIEF REQUESTED

Lionra requests that the following portions of the Reply be struck from the record:

- Petitioner's Reply, pp. 4–5
- Petitioner's Reply, pp. 13–14 ("As discussed . . . the modulo engine.")

[1] Patent Owner is filing a substantively identical motion to strike in IPR2023-00703 based on the substantively identical Reply in that proceeding.

III. PORTIONS OF PETITIONER'S REPLY ARE IMPROPER AND SHOULD BE STRUCK

In an *inter partes* review, "the Reply is limited to a true rebuttal role." *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015). The Petition must identify the specific portions of the evidence relied upon and the relevance of that evidence. These principles "reflect[] the combination of efficiency and fairness interests also embodied in the regulation limiting Reply submissions to matter responsive to the [POR]." *Ariosa*, 805 F.3d at 1368 (citing 37 CFR § 42.23(b)). A Petitioner's Reply that "crosses the line from the responsive to the new" evades these procedural safeguards and risks expunction. *See id*.

Indications that a new issue has been improperly raised include "new evidence necessary to make out a *prima facie* case for patentability or unpatentability . . . and new evidence that could have been presented in a prior filing." 77 Fed. Reg. 48,756, 48,767 (Aug. 14, 2012). Evidence submitted in rebuttal should be "limited to that which is responsive to the adversary's evidence." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1081-82 (Fed. Cir. 2015) (citation omitted).

In this proceeding, the Reply impermissibly goes beyond its rebuttal function by filling gaps in its *prima facie* case with a previously unidentified embodiment in the Pham reference (Grounds 1–4) and a theory of obviousness regarding the Pham-Wu-Collins-Krishna (Ground 3) and Pham-Wu-Krishna (Ground 4) combinations

that did not appear in the Petition.

A. Petitioner identifies a different embodiment in Pham to fill gaps in the Petition.

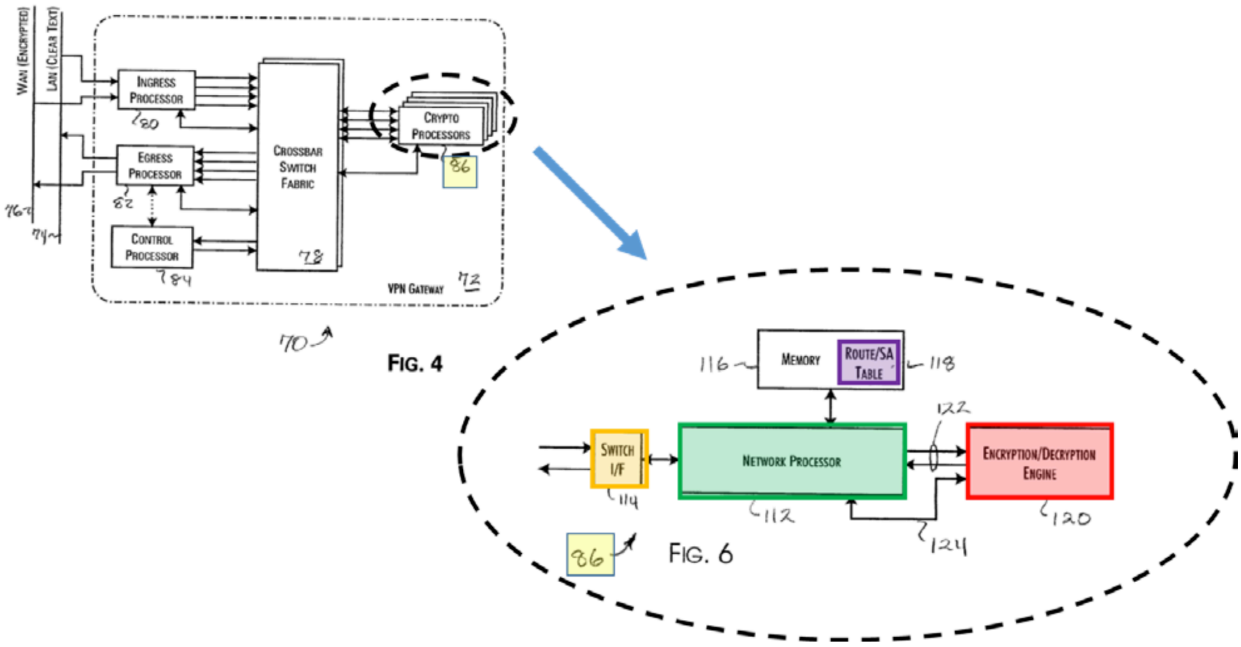
Each of the challenged independent claims recites, in part, *wherein the packet engine is one of a plurality of packet engines and substantially all of the incoming packets and outgoing packets to the security processor transit one of the plurality of packet engines.* In the Petition, Cisco identifies "network processor 112" as the alleged *packet engine*. Pet., 37. As to the *security processor*, the Petition identifies a combination of control processor 84, crossbar switch fabric 78, and crypto processors 86. Pet., 34–35 (annotating EX1004, Fig. 4 in brown to illustrate the alleged *security processor*). The Petition contends that "Pham discloses that the network processors 112 process substantial [sic] all the data packet [sic] received and transmitted by the VPN Gateway" and supports this contention by pointing to Pham's disclosure that ingress processor 80 and network processor 112 "use the identical conventional processors and identical routing and SA tables." Pet., 42 (citing EX1004 Figs. 5, 6, [0049], [0051], [0053]). Cisco also cites to paragraph 89 of its expert's declaration, which repeats Petitioner's argument word for word.

In the POR, Patent Owner rebuts Cisco's contention that substantially all of the incoming packets and outgoing packets to crossbar switch fabric 78 (the alleged *security processor*) transit network processor 112 (the alleged *packet engine*). The

POR identifies a gap in the Petition, specifically that it "does not address" the substantial number of unencrypted packets that transit crossbar switch fabric 78 but do not transit network processor 112. POR, 23–24. To further address Cisco's contention relating the "routing and SA tables" used by ingress processor 80 and network processor 112, the POR also explains that in "the embodiment that Petitioner relies on," Pham's ingress processor "filters data packets that are not going to be passed through the VPN connection on the WAN." POR, 26.

Confronted with the gap in its *prima facie* case, Cisco improperly attempts to fill the gap using its Reply. It does so by pointing to an embodiment in Pham that was **not** addressed in the Petition or the POR. Specifically, Cisco argues that Figure 2 of Pham "illustrates **another embodiment** in which substantially all packets transit a packet engine." Reply, 4 (emphasis added). This argument about "another embodiment" is not a rebuttal to Patent Owner's criticisms of the embodiment relied on in the Petition. As explained, those criticisms were directed to the theory Cisco actually presented in the Petition, where network processor 112 is the alleged *packet engine*. But Cisco's Reply does not even allege that Figure 2 shows that *substantially all packets transit* **network processor 112**. Instead, Cisco argues that the newly identified Figure 2 embodiment shows "all packets . . . transit[ing] one of the plurality of **data processors 42, 44 (blue)**." Reply, 4-5 (emphasis added). Cisco goes on to say that ". . . in the embodiment shown in FIG. 2 of Pham, the data

processors could be crypto processors having a network processor (*packet engine*) receiving all incoming packets. . . ," further demonstrating that the Reply relies on a different element of Pham as an alleged *packet engine* and presents a new theory of unpatentability. As Cisco's own annotated figures from Pham illustrate, Figure 2 does not even include crypto processors 86 or network processer 112 from Figures 4 and 6 that the Petition relies on.



Pet., 37 (citing EX1004, Figs. 4 and 6) (annotations in Petition)

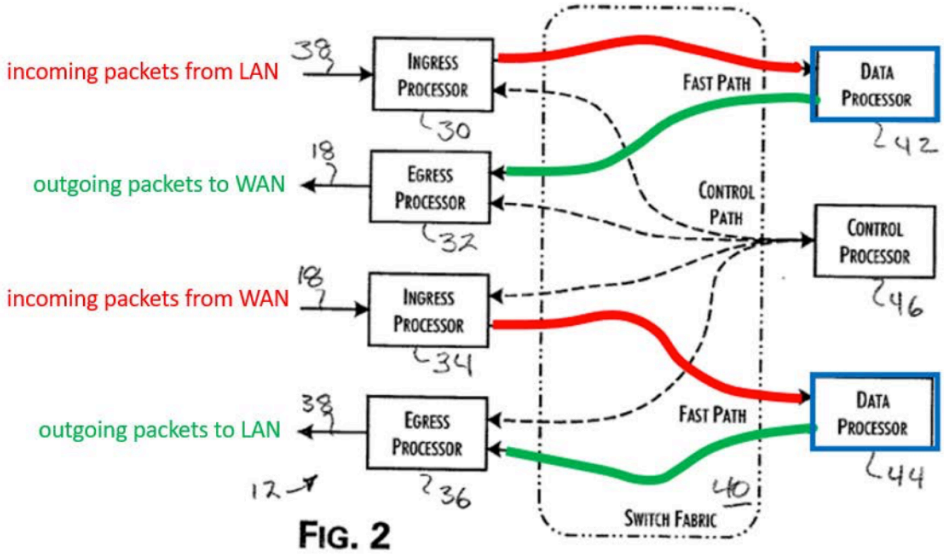


FIG. 2

Reply, 4 (citing EX1004, Fig. 2) (annotations in Reply). If Cisco wanted to argue an alternate theory, it should have done so in the Petition, not in the Reply. For these reasons, Cisco's improper reply arguments regarding Figure 2 (Reply at 4–5) should be struck from the record.

B. Petitioner's new obviousness theory is another improper attempt to fill gaps in the Petition

Cisco's Reply also seeks to fill a gap left by its Petition in Grounds 3 and 4. Each of these grounds relate to dependent claims (4, 7, and 8 in Ground 3; 17 in Ground 4) that recite *wherein the packet engine, the cryptographic core, and the modulo engine are formed on a single chip*. The underlying independent claims (1 and 13) each also recites, in part, *an intrusion detection system coupled between the cryptographic core and the packet engine*. The Petition acknowledges that the combination of references Pham, Wu, and Collins do not disclose that these claimed

elements are "formed on a single chip." Pet., 69–70. For the *single chip* limitation, the Petition relies on a fourth reference, Krishna, that allegedly discloses "incorporating components on a single chip." Pet., 70.

The obviousness theory presented in the Petition is that "[i]t would have been obvious to a POSA to form the network processor, encryption/decryption engine, and the arithmetic unit of Pham, Wu and Collins onto a single chip as taught by Krishna." Pet., 70–71. But neither of Grounds 3 or 4 makes any mention of an *intrusion detection system coupled between the cryptographic core and the packet engine*. The POR identifies this gap in Cisco's theory, i.e., that Petitioner "omits any discussion of how limitation [1.viii] of independent claim 1 [and 13] ('an intrusion detection system coupled between the cryptographic core and the packet engine') could or would be satisfied if the packet engine, cryptographic core and modulo engine are formed on a single chip." POR, 35–36.

In its Reply, Cisco improperly attempts to fill this gap with a new theory of obviousness. Whereas the Petition argued only that it would have been obvious to form three specific components—"the network processor, encryption/decryption engine, and the arithmetic unit"—onto a single chip (Pet., 70, 72–73), the Reply makes a new argument: "a POSA would be motivated to include **security functions** on a single chip" and that this "rationale applies to **all security functions, including an IDS**, and not just those discrete elements recited in Clam 3, e.g., packet engine,

cryptographic core and the modulo engine." Reply, 14 (emphasis added). Thus, by Cisco's own admission, the Reply seeks to broaden the theory presented in the Petition to include more than what Cisco originally presented. In other words, Cisco uses the Reply to fill the gap in Cisco's *prima facie* case, i.e., Cisco's failure to address how an *intrusion detection system coupled between the cryptographic core and the packet engine* could or would be satisfied if the packet engine, cryptographic core and modulo engine are formed on a single chip. Accordingly, the portion of the Reply presenting this new theory, Reply 13–14 ("As discussed . . . the modulo engine.") should be struck from the record.

Date: May 6, 2024

Respectfully submitted,

/Brett Cooper/
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Lead counsel for Patent Owner

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e)(1))

The undersigned hereby certifies that the above document was served on May 6, 2024, by filing this document through the Patent Trial and Appeal Case Tracking System as well as delivering a copy via electronic mail upon the following attorneys of record for the Petitioner:

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