

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

CURRENT LIGHTING SOLUTIONS, LLC d/b/a GE CURRENT,

Petitioner,

v.

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD.,

Patent Owner.

INTER PARTES REVIEW NO. IPR2023-00676
PATENT NO. 9,939,140

PETITION FOR *INTER PARTES* REVIEW UNDER 35 U.S.C. §312

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PETITIONER'S EXHIBIT LIST

Exhibit	Shorthand	Description
EX1001	'140 Patent	U.S. Patent No. 9,939,140
EX1002	Lebby	Declaration of Michael Lebby, Ph.D.
EX1003	'140 FH	Excerpts from File History of the '140 Patent
EX1004	'645 Application	U.S. Patent App. Pub. No. 2016/0219672
EX1005	'387 Application	U.S. Patent App. Pub. No. 2016/0091147
EX1006	'138 Application	U.S. Patent App. Pub. No. 2016/0102813
EX1007	Ivey813	U.S. Patent No. 8,596,813
EX1008	Ivey345	U.S. Patent App. Pub. No. 2014/0015345
EX1009	Sadwick	U.S. Patent App. Pub. No. 2017/0311396
EX1010	Powell	U.S. Patent No. 9,438,165
EX1011	Digi-Key	Wayback Machine capture of <i>Product Index > Discrete Semiconductor Products > FETs – Arrays</i> , Digi-Key (Apr. 10, 2014, 11:03 AM), http://www.digikey.com/product-search/en/discrete-semiconductor-products/fets-arrays/1377094 [https://web.archive.org/web/20140410110347/http://www.digikey.com/product-search/en/discrete-semiconductor-products/fets-arrays/1377094]
EX1012	Fairchild	Wayback Machine capture of <i>FDG6303N Dual N-Channel, Digital FET</i> , Fairchild Semiconductor (Mar. 8, 2014, 4:25 AM), http://www.fairchildsemi.com/ds/FD/FDG6303N.pdf [https://web.archive.org/web/20140308042522/http://www.fairchildsemi.com/ds/FD/FDG6303N.pdf]

Exhibit	Shorthand	Description
EX1013	Premier	Wayback Machine capture of <i>Should You Replace Your T8 Fluorescent Lamps with T8 LED Tubes? (updated)</i> , Premier Lighting (June 27, 2014, 9:59 PM), http://www.premierltg.com/should-you-replace-your-t8-fluorescent-lamps-with-t8-led-tubes-2/ [https://web.archive.org/web/20140627215905/http://www.premierltg.com/should-you-replace-your-t8-fluorescent-lamps-with-t8-led-tubes-2/]
EX1014	Pyeon	U.S. Patent No. 9,240,227
EX1015	Parks	Wayback Machine capture of Michael Parks, <i>Don't Burn Out! Calculating LED Current Limiting Resistor</i> , Mouser Electronics (Oct. 10, 2014, 6:43 AM), http://www.mouser.com/blog/dont-burn-out-calculating-led-current-limiting-resistor [https://web.archive.org/web/20141010064339/http://www.mouser.com/blog/dont-burn-out-calculating-led-current-limiting-resistor]
EX1016	Etkina	Eugenia Etkina & Gorazd Planinšič, <i>Light-Emitting Diodes: Exploration of Underlying Physics</i> , 52 The Physics Teacher 212 (2014)
EX1017	Briggs	U.S. Patent No. 8,564,214
EX1018	Mandal	M.K. Mandal & B.C. Sarkar, <i>Ring oscillators: Characteristics and applications</i> , 48 Indian J. of Pure & Applied Physics 136 (2010)
EX1019	Recom	Wayback Machine capture of <i>High Power LED and DC/DC-Driver Applications</i> , RECOM Power (Jan. 6, 2015, 4:09 AM) http://www.recom-power.com/fileadmin/RECOM-Downloads/Whitepaper/WP_RCD_Applications_1107_EN.pdf [https://web.archive.org/web/20150106040908/http://www.recom-power.com/fileadmin/RECOM-Downloads/Whitepaper/WP_RCD_Applications_1107_EN.pdf]
EX1020	Guang	U.S. Patent App. Pub. No. 2017/0303353
EX1021	Esaki	U.S. Patent No. 8,872,437

Exhibit	Shorthand	Description
EX1022	Physics-Classroom	Wayback Machine capture of <i>Two Types of Connections</i> , The Physics Classroom (Dec. 01, 2011, 12:54 AM), https://www.physicsclassroom.com/Class/circuits/u9l4b.cfm [https://web.archive.org/web/20111201005447/https://www.physicsclassroom.com/Class/circuits/u9l4b.cfm]
EX1023	Nave-1	Wayback Machine capture of Rod Nave, <i>OR Gate</i> , HyperPhysics (Mar. 3, 2004, 3:58 PM), http://hyperphysics.phy-astr.gsu.edu/hbase/Electronic/or.html [https://web.archive.org/web/20040303155843/http://hyperphysics.phy-astr.gsu.edu/hbase/Electronic/or.html]
EX1024	Nave-2	Wayback Machine capture of Rod Nave, <i>Relaxation Oscillator Concept</i> , HyperPhysics (May 1, 2001, 4:38 AM), http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/relaxo.html [https://web.archive.org/web/20010501043853/http://hyperphysics.phy-astr.gsu.edu/hbase/electronic/relaxo.html]
EX1025	Actel	Wayback Machine capture of <i>Using Schmitt Triggers for Low Slew-Rate Input</i> , Actel (Sept. 19, 2014, 1:18AM), http://www.microsemi.com/document-portal/doc_download/130021-ac161-using-schmitt-triggers-for-low-slew-rate-input-app-note [https://web.archive.org/web/20140919011857/http://www.microsemi.com/document-portal/doc_download/130021-ac161-using-schmitt-triggers-for-low-slew-rate-input-app-note]
EX1026		Claim Construction Order, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 57 (W.D. Tex. Oct. 24, 2020)
EX1027		Final Jury Instructions, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 226 (W.D. Tex. Nov. 4, 2021)
EX1028		Jury Trial Transcript, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 238 (W.D. Tex. Dec. 2, 2021)

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EX1029		Jury Trial Transcript, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 239 (W.D. Tex. Dec. 2, 2021)
EX1030		Defendants' Opposed Motion for Judgment as a Matter of Law Under Federal Rule of Civil Procedure 50(b), <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 294 (W.D. Tex. Aug. 31, 2022)
EX1031		Plaintiffs' Opposition to Defendants' Motion for Judgment as a Matter of Law Under Federal Rule of Civil Procedure 50(b), <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 299 (W.D. Tex. Sept. 9, 2022)
EX1032		Defendants' Reply in Support of Motion for Judgment as a Matter of Law Under Federal Rule of Civil Procedure 50(b), <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd.</i> , No. 6:20-CV-00018, Dkt. No. 308 (W.D. Tex. Sept. 20, 2022)
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EX1034		Plaintiffs Jiaxing Super Lighting Electric Appliance Co., Ltd., and Obert, Inc.'s Preliminary Infringement Contentions, Claim Chart A1, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. Oct. 19, 2022)
EX1035		Plaintiffs Jiaxing Super Lighting Electric Appliance Co., Ltd., and Obert, Inc.'s Preliminary Infringement Contentions, Claim Chart A2, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. Oct. 19, 2022)

Exhibit	Shorthand	Description
EX1036		Scheduling Order, <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA, Dkt. No. 31 (W.D. Tex. 2022)
EX1037		Draft of Defendant's Stipulation of Invalidity Contentions to be filed in <i>Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current</i> , No. 6:22-CV-00534-ADA (W.D. Tex. 2022)
EX1038		Declaration of Sylvia D. Hall-Ellis, Ph.D.

CLAIM LISTING

Claim	Limitation No.	Limitation
1	[1pre]	An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal,
	[1a]	the installation detection circuit comprising: a pulse generating circuit configured to output one or more pulse signals;
	[1b]	wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and
	[1c]	a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;
	[1d]	wherein the installation detection circuit is further configured to: when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and
	[1e]	when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,

Claim	Limitation No.	Limitation
	[1f]	wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and
	[1g]	wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal.
3	[3a]	The installation detection circuit according to claim 1, wherein when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and
	[3b]	when the detection determining circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.
4	[4pre]	An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal,
	[4a]	the installation detection circuit comprising: a pulse generating circuit configured to output one or more pulse signals;
	[4b]	wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

Claim	Limitation No.	Limitation
	[4c]	a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;
	[4d]	wherein the installation detection circuit is further configured to: when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and
	[4e]	when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state, and
	[4f]	wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit; and
	[4g]	wherein the installation detection circuit further includes a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.
5	The installation detection circuit according to claim 4, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.	

Claim	Limitation No.	Limitation
21	[21pre]	An installation detection circuit configured in a light-emitting diode (LED) tube lamp,
	[21a]	the installation detection circuit comprising: means for generating one or more pulse signals;
	[21b]	means for detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket; and
	[21c]	a switch circuit coupled to the means for generating one or more pulse signals, wherein the one or more pulse signals control turning on and off of the switch circuit;
	[21d]	wherein the installation detection circuit is further configured to: when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and
	[21e]	when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,
	[21f]	wherein the means for detecting is configured to detect a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the means for detecting, and

Claim	Limitation No.	Limitation
	[21g]	wherein the LED tube lamp is configured to receive an external driving signal and comprises a rectifying circuit for rectifying the external driving signal and a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit.
22	[22a]	The installation detection circuit according to claim 21, wherein when the means for detecting determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and
	[22b]	when the means for detecting determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.
23	The installation detection circuit according to claim 21, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the means for detecting.	
24	[24pre]	A detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket,
	[24a]	the detection method comprising: when at least one end of the LED tube lamp is installed on the lamp socket, generating one or more pulse signals by a pulse generating circuit, wherein the pulse generating circuit is configured in the LED tube lamp;
	[24b]	detecting a sampling signal on a power loop of the LED tube lamp by a detection determining circuit, to detect during the one or more pulse signals whether the other end of the LED tube lamp is properly installed on the lamp socket;

Claim	Limitation No.	Limitation
	[24c]	receiving the one or more pulse signals through a detection result latching circuit by a switch circuit, wherein the switch circuit is on the power loop; and
	[24d]	comparing the sampling signal with a predefined signal, wherein during the one or more pulse signals when the sampling signal is smaller than the predefined signal, the detection method further comprises: controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open.
25	[25a]	The detection method according to claim 24, wherein the step of controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open comprises: outputting a first low level signal by the detection determining circuit;
	[25b]	receiving the first low level signal by the detection result latching circuit and outputting a second low level signal; and
	[25c]	receiving the second low level signal by the switch circuit and maintaining an off state of the switch circuit to cause the power loop to be open.
26	The detection method according to claim 24, wherein during any of the one or more pulse signals when the sampling signal is greater than or equal to the predefined signal, the detection method further comprises: controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.	

Claim	Limitation No.	Limitation
27	[27a]	The detection method according to claim 26, wherein the step of controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state comprises: outputting a first high level signal by the detection determining circuit;
	[27b]	receiving the first high level signal by the detection result latching circuit and outputting a second high level signal; and
	[27c]	receiving the second high level signal by the switch circuit and conducting the switch circuit to cause the power loop to maintain a conducting state.
28	The detection method according to claim 24, wherein a period of each of the one or more pulse signals is between 10 microseconds and 1 millisecond.	
30	[30a]	The installation detection circuit according to claim 4, configured such that when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and
	[30b]	when the detection determining circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.
31	The installation detection circuit according to claim 1, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.	
32	The installation detection circuit according to claim 31, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.	

Claim	Limitation No.	Limitation
35		The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

I. INTRODUCTION

The '140 Patent's claims 1, 3-5, 21-28, 30-32, and 35 ("Challenged Claims") recite a circuit and related methods for preventing electric shock due to accidental user contact with a light-emitting device (LED) tube lamp's terminals during relamping. Ivey³⁴⁵, however, already disclosed such a circuit and how to use it. And to the extent any differences exist, such differences were obvious, including in view of Ivey⁸¹³, Sadwick, and Powell. The Challenged Claims are therefore unpatentable.

II. MANDATORY NOTICES

A. Real Party-in-Interest (37 C.F.R. §42.8(b)(1))

The real party-in-interest is Current Lighting Solutions, LLC d/b/a GE Current.

B. Related Matters (§42.8(b)(2))

The following proceedings involve the '140 Patent.

Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. Current Lighting Solutions, LLC d/b/a GE Current, No. 6:22-CV-00534-ADA (W.D. Tex. 2022) ("Current Action").

Jiaxing Super Lighting Elec. Appliance Co., Ltd. v. CH Lighting Tech. Co. Ltd., No. 6:20-CV-00018 (W.D. Tex. 2020) ("CH Action").

C. Lead and Back-Up Counsel (§42.8(b)(3))

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D. Service Information (§42.8(b)(4))

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Petitioner consents to electronic service.

III. REQUIREMENTS FOR IPR

A. Grounds for Standing (§42.104(a))

Petitioner certifies that the '140 Patent is available for *inter partes* review ("IPR"), and Petitioner is not barred or estopped from requesting IPR on the grounds identified in this Petition.

B. Identification of Challenge (§42.104(b)(1)-(2))

1. Claims for Which Review Is Requested

Petitioner requests cancellation of claims 1, 3-5, 21-28, 30-32, and 35.

2. *Grounds of Challenge*¹

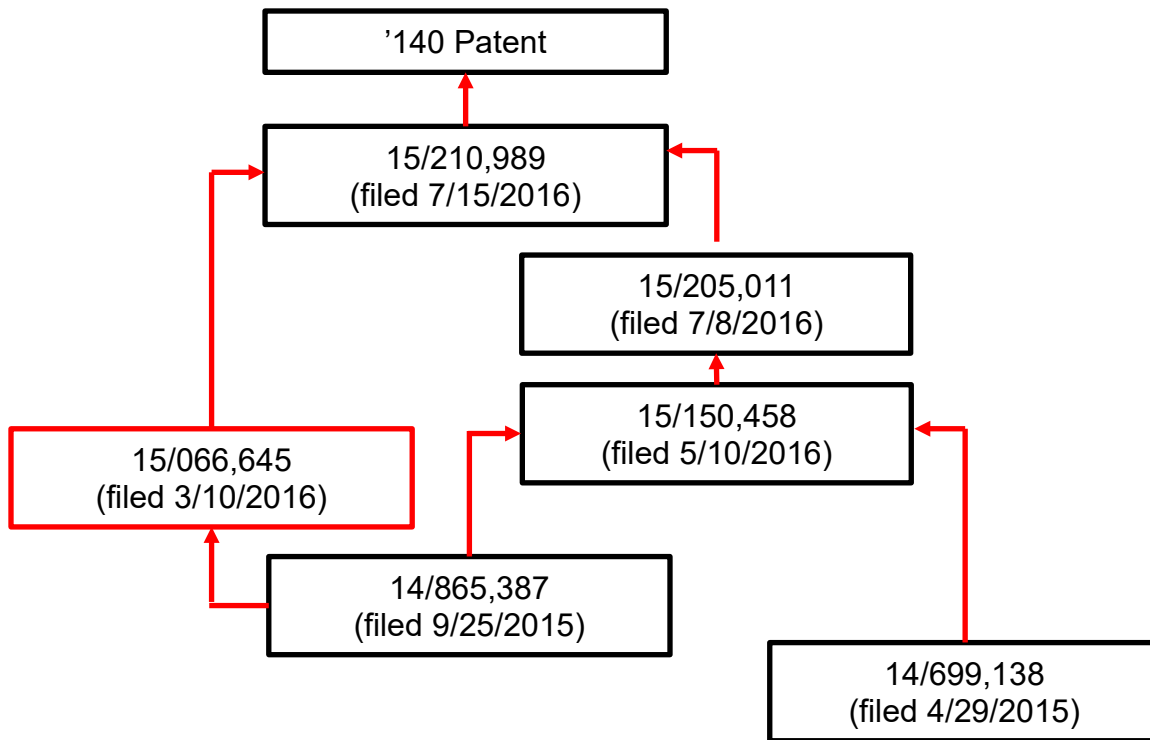
The Challenged Claims are unpatentable under the following grounds:

Ground	Claims	Statutory Basis	Prior Art
1	1, 3-4, 21-28, 30-31, and 35	§103	Ivey813, Ivey345
2	1, 3-4, 21-28, 30-31, and 35	§103	Ivey813, Ivey345, Sadwick
3	1, 4-5, and 32	§103	Ivey813, Ivey345, Powell
4	1, 4-5, and 32	§103	Ivey813, Ivey345, Sadwick, Powell

Supporting analysis is provided in the Declaration of Dr. Michael Lebby.

The '140 Patent's claims each recite an "installation detection circuit... configured to detect during... one or more pulse signals whether the LED tube lamp is properly installed" or a similar pulse-based detection limitation. EX1001, claims 1, 4, 17, 21, 24. The '140 Patent resulted from the chain of continuation-in-part applications depicted below.

¹ All Grounds are supported by a person of ordinary skill in the art's ("POSITA's") general knowledge. *Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337-38 (Fed. Cir. 2020).



Of these, the earliest to include pulse-based-detection disclosure is the '645 Application, which was filed on March 10, 2016. *Compare, e.g.,* EX1004, ¶¶[0441]-[0448], *with generally* EX1005, *and* EX1006. And given the '387 and '138 Applications lack pulse-based-detection description that would otherwise break continuity of disclosure for the '140 Patent's claims, the '140 Patent cannot reach further back than a year before the '645 Application's filing date via its priority claims to Chinese patent applications (*see* EX1004, code (30)). 35 U.S.C. §119; *Zenon Env'tl, Inc. v. U.S. Filter Corp.*, 506 F.3d 1370, 1379 (Fed. Cir. 2007). March 10, 2015 is thus the earliest claimed priority date ("ECPD") possible for the '140 Patent. Accordingly:

- Published December 3, 2013, Ivey813 is prior art under §102(a)(1).

- Published January 16, 2014, Ivey345 is prior art under §102(a)(1).
- Filed October 31, 2014, Sadwick is prior art under §102(a)(2).
- Filed October 8, 2014, Powell is prior art under §102(a)(2).

IV. LEVEL OF ORDINARY SKILL IN THE ART

In the *CH* Action, Patent Owner (“PO”) asserted “the level of ordinary skill in the field would require at least a bachelor’s degree in Electrical Engineering or a comparable field and 3 years of experience designing lighting fixtures or systems, or equivalents.” EX1027, 27. For purposes of this IPR, Petitioner adopts this definition of a POSITA, but adding that more education could have compensated for less experience, and vice versa.² EX1002, ¶¶23-25.

V. ’140 PATENT

A. Overview

The ’140 Patent explains that during relamping of an LED tube lamp, “when one end cap thereof is inserted into a lamp socket but the other is not, an electric shock situation could take place for the user touching the metal or conductive part

² All Petition statements about the knowledge and skills of, and what would have been understood by, a POSITA are from this perspective as of the ECPD. *See* EX1002, ¶18; *see also id.*, ¶¶17-22 (scope of work, legal understanding, and basis for opinions), 2-16, 26 (experience/qualifications).

of the end cap which has not been inserted into the lamp socket.” EX1001, 3:62-67; EX1002, ¶33. To prevent such a shock, the '140 Patent discloses an “installation detection circuit” configured in an LED tube lamp. EX1001, Abst., 5:7-26; EX1002, ¶33. Figure 15B depicts one embodiment:

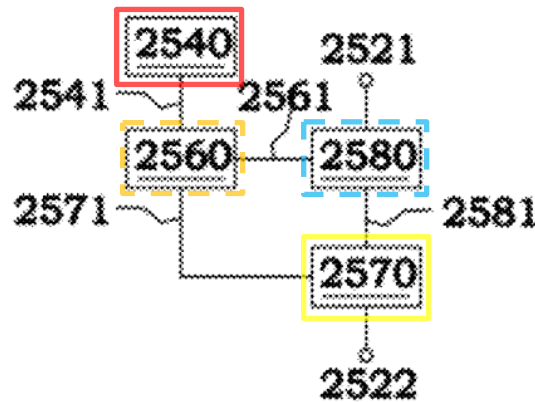


Fig. 15B

EX1001, Fig. 15B (annotated), 38:39-41; EX1002, ¶33. The depicted installation detection circuit includes “detection pulse generating module 2540” (solid-red), “detection result latching circuit 2560” (dotted-orange), “switch circuit 2580” (dotted-blue), and detection determining circuit 2570” (solid-yellow). EX1001, Fig. 15B, 38:41-44; EX1002, ¶¶33-38. Detection pulse generating module 2540 periodically outputs a “pulse signal” over “pulse signal output terminal 2541” to detection result latching circuit 2560, which may use the pulse signal as “a time point” for when to store a “detection result signal” received at “detection result terminal 2571.” EX1001, 38:58-39:6, 38:50-54, 45:50-63; EX1002, ¶¶33-34.

Detection result latching circuit 2560 outputs the stored detection result to switch circuit 2580 via “detection result latching terminal 2561” (EX1001, Fig. 15B, 38:58-39:6) and, in some embodiments, may also store and output the pulse signal itself (EX1001, 41:27-37, 39:39-47). EX1002, ¶34-35. Switch circuit 2580 controls the conducting state across the LED tube lamp—i.e., the LED tube lamp’s “power loop”—such that, when detection result latching circuit 2560’s output is high (such as when the stored detection result is high and/or, in some embodiments, when the pulse is high), the power loop conducts. EX1001, 39:44-49; EX1002, ¶35.

Detection determining circuit 2570 “detects a sampling signal on the power loop” such as “current passing through terminals 2521 and 2522” and detects whether such current “is above or below a specific current value.” EX1001, Fig. 15B, 39:49-54, 38:54-57; EX1002, ¶36. When the LED tube “is correctly installed on a lamp socket,” such current will be above the specific current value, and detection determining circuit 2570 will output a “high logic level” detection result signal to detection result latching circuit 2560 over detection result latching terminal 2561. EX1001, 42:56-43:8; EX1002, ¶36. The opposite occurs in an incorrect installation, e.g., the shock situation above. EX1001, 43:9-15; EX1002, ¶36.

B. Prosecution History

The ’140 Patent was rejected for double patenting, which Applicant obviated via terminal disclaimer, as well as under 35 U.S.C. §§102 and 103 over Sadwick.

EX1003, 176-78, 216-17, 231-34. Regarding the latter, the Office found “detection result latching circuit” to recite allowable subject matter (e.g., as-issued claims 4 and 24) (*id.*, 234, 207-15, 409, 450-464, 468) and rejected most claims lacking such a recitation (*id.*, 231-34, 207-15). Rather than amending each claim to include the above, Applicant amended one set of rejected claims to recite “the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal” (found in as-issued claim 1) and argued Sadwick did not contain this limitation. *Id.*, 377, 372-75, 409. Applicant also amended a separate set to recite instead “a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit” (found in as-issued claim 21). *See id.*, 386, 409. The Office thereafter allowed the claims. *Id.*, 399-402.

C. Claim Construction (§42.104(b)(3))

For purposes of this IPR, all terms should be given their plain and ordinary meaning unless indicated otherwise below. EX1002, ¶39.

1. “means for generating”

Claim 21 recites “means for generating.” In the *CH* Action, the parties agreed this term was subject to 35 U.S.C. §112(f). EX1026, 5. The court found, and the parties agreed, the claimed function was “generating one or more pulse signals.” *Id.* The court found the corresponding structures to be “module 2540 in Fig. 15B,

module 2740 in Fig. 15G, circuits depicted in Figs. 15C and 15H, and corresponding text, and equivalents thereof.” *Id.*

Petitioner agrees—the construed function is explicitly recited in claim 21, and the listed structures each “generate[] a pulse signal” and are thus adequate corresponding structures associated with the construed function. *E.g.*, EX1001, 38:58-62, 47:16-19; EX1002, ¶40.

2. “means for detecting”

Claims 21-23 recite “means for detecting.” In the *CH* Action, the parties agreed this term was subject to 35 U.S.C. §112(f). EX1026, 5. The court found, and the parties “largely agreed,” the recited function was “detecting a sampling signal on the power loop during the one or more pulse signals for determining whether the LED tube lamp is properly installed.” *Id.* The court found the corresponding structures to be “module 2570 in Fig. 15B, module 2770 in Fig. 15G, Figs. 15D and 15K, and corresponding text, and equivalents thereof.” *Id.*

Petitioner agrees—the construed function accurately reflects the recited functions of the “means for detecting,” including “detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket” and “detect[ing] a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket.” EX1002, ¶41. And the listed structures each “detect[] a sampling signal on the power loop” during a pulse signal

to determine whether the LED tube is installed properly and are thus adequate corresponding structures associated with the construed function. *E.g.*, EX1001, 39:44-58, 37:46-38:4, 48:19-41; EX1002, ¶41.

3. “*detection result latching circuit*”

Claims 4-5, 23-25, 27, and 31-32 recite a “detection result latching circuit.” In the *CH* Action, the court construed the term to mean “circuit that stores the detected result and outputs a high logic value when either the stored detected result *or the pulse signal output terminal (e.g., inputs 2541 or 2741 in Figs. 15E and 15I)* has a high logic value.” EX1026, 6.³ Petitioner disagrees with the *CH* Court’s construction, particularly the emphasized portion. The claims contain no requirement that the detection result latching circuit necessarily outputs a high logic value when receiving a high logic level signal from the claimed “pulse generating circuit”—i.e., a “pulse signal” (EX1001, 41:23-27). EX1002, ¶43. In fact, the ’140 Patent explains that, in some embodiments, the pulse signal can be received by the detection result latching circuit simply “to inform the detection result latching circuit 2560 of a time point for latching (storing) the detection result.” *E.g.*, EX1001, 38:58-62, claims 25, 27; EX1002, ¶43. The prior construction is thus overly narrow and, here, the term should instead be given its plain and ordinary meaning. EX1002, ¶43.

³ All emphasis added unless otherwise indicated.

VI. REASONS FOR THE RELIEF REQUESTED UNDER 37 C.F.R. §§42.22(A)(2) AND 42.104(B)(4)

A. Ground 1: Ivey813 and Ivey345 Render Obvious Claims 1, 3-4, 21-28, 30-31, and 35

1. Ivey813

Ivey813 describes “a light emitting diode (LED) based light tube,” particularly “a circuit board mount for the LED light tube and methods of mounting the circuit board.” EX1007, 1:13-16; EX1002, ¶44. Figure 1 shows an example:

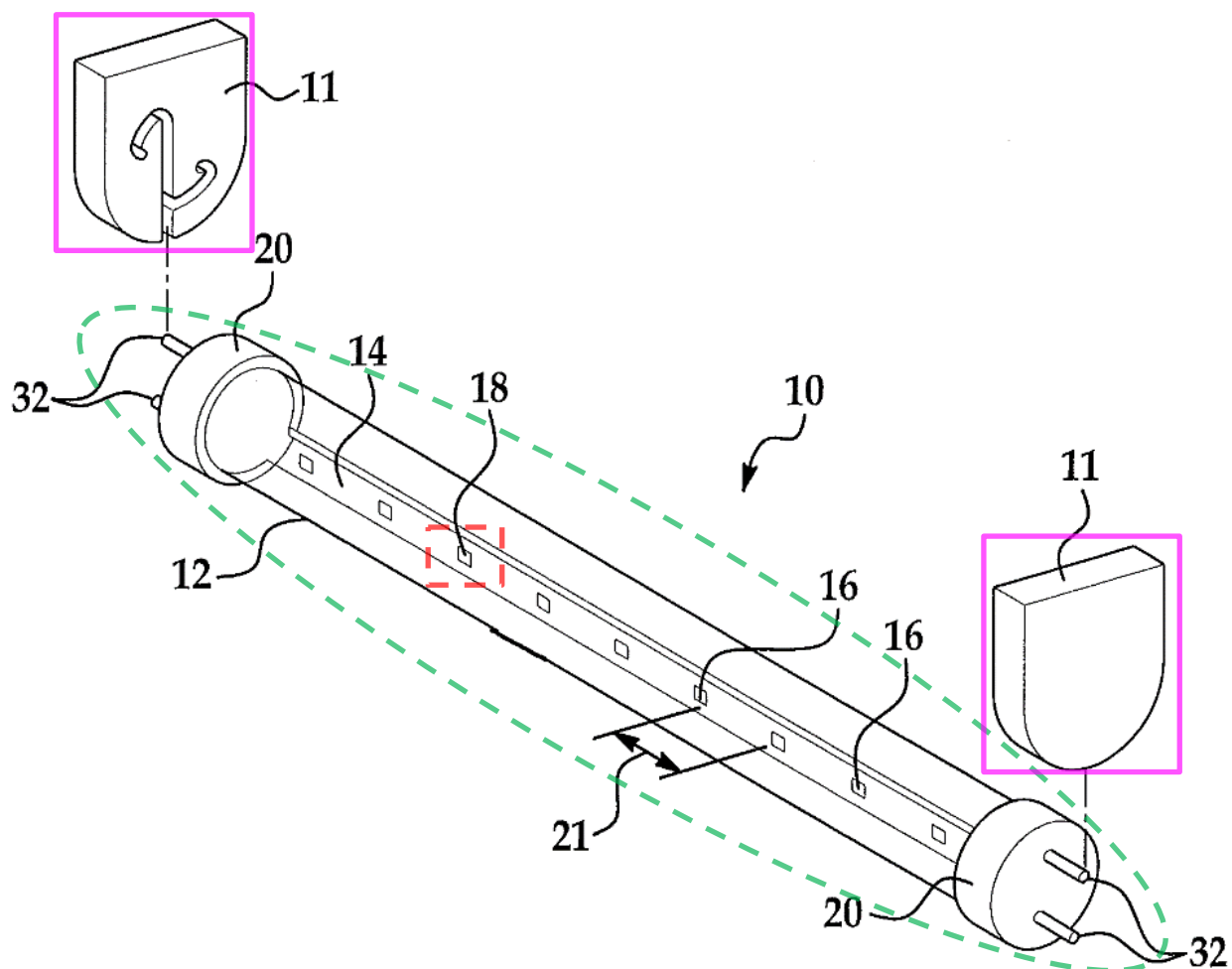


FIG. 1

EX1007, Fig. 1 (annotated); EX1002, ¶44. As Ivey813 teaches, Ivey813's Figure 1

depicts “LED light tube 10” (dotted-green) comprising an elongated “housing 12” with two “end caps 20” attached at opposing ends of housing 12. EX1007, 1:37-39, 1:50-51; EX1002, ¶44. Each end cap 20 includes “pins 32” that may electrically connect the LED light tube to fixture 11 (solid-pink). EX1007, 5:1-16; EX1002, ¶44. Fixture 11 can be, “for example, an existing fluorescent lamp fixture” and thus “can contain a ballast,” or can instead directly power the LED light tube 10 with mains line power, such as when the LED light tube 10 is a ballast-bypass (“type B”) LED tube.⁴ See EX1007, 2:51-56; EX1001, 4:1-11; EX1013, 3-4; EX1002, ¶44. The LED light tube also comprises “circuit board 14” spanning housing 12. EX1007, 1:37-39; EX1002, ¶44. Circuit board 14 has “LEDs 18” (dotted-red) mounted to its surface and conductive connections from the pins 32 to the LEDs 18. EX1007, 2:13-17, 3:27-37, 3:63-67; EX1002, ¶44.

Circuit board 14 also includes “power converters 36 and other circuitry” near end caps 20 to “convert the power received through the fixture [via the pins] into

⁴ Should Patent Owner argue LED light tube 10 is not disclosed as being a type B LED tube, a POSITA would have nevertheless been motivated to modify LED light tube 10 to be a type B LED tube to increase power efficiency and reduce maintenance cost (see EX1013, 3-4) and would have known how to do so (see EX1001, 4:1-11). EX1002, ¶44 n.1.

power usable by and suitable for the LEDs”:

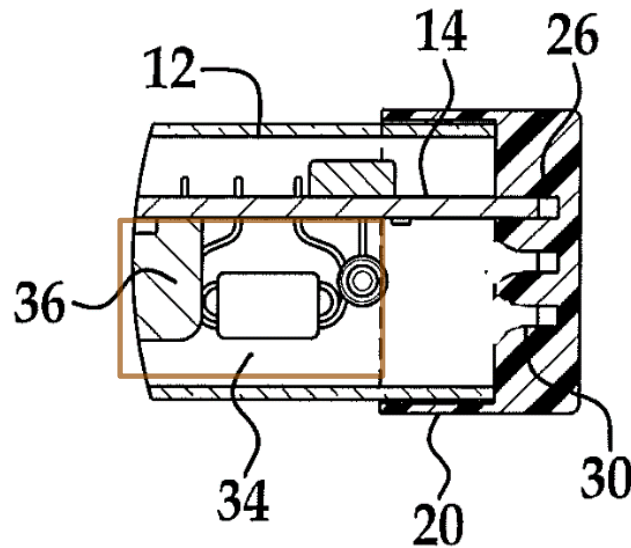


FIG. 7

EX1007, Fig. 7 (annotated), 5:31-35; EX1002, ¶45. Power converter 36 (solid-brown) includes “one or more of an inrush protection circuit, a surge suppressor circuit, a noise filter circuit, a rectifier circuit, a main filter circuit, a current regulator circuit and a shunt voltage regulator circuit.” EX1007, 5:36-39; EX1002, ¶45.

2. Ivey345

Ivey345 is directed to “a system and method for protecting a person from electrical shock when interacting with an electrical device.” EX1008, ¶[0002], code (72); EX1007, code (75); EX1002, ¶46. As Ivey345 teaches, “[c]ompact fluorescent light bulbs (CFLs) and light emitting diode based (LED-based) lights are gaining popularity,” but such “line-powered electrical devices” also carry certain “drawbacks.” EX1008, ¶[0004]; EX1002, ¶46. Particularly, “if the power terminal

is connected using one connector and the subject, for example a person installing a new bulb, comes into contact with the return terminal in another connector that has not yet been mated, the person may receive a shock by completing the circuit from the return terminal to ground.” EX1008, ¶[0005]; EX1002, ¶46.

As a solution, Ivey345 describes implementing a “current limiting circuit” that “operates to electrically detect the presence of a foreign object, for example, a person’s body, in the circuit path and limit the flow of current through the object while allowing substantially full current to flow when an intended electrical connection is established between a power source and load.” EX1008, ¶[0010]; EX1002, ¶47. Ivey345’s Figure 3 depicts one embodiment:

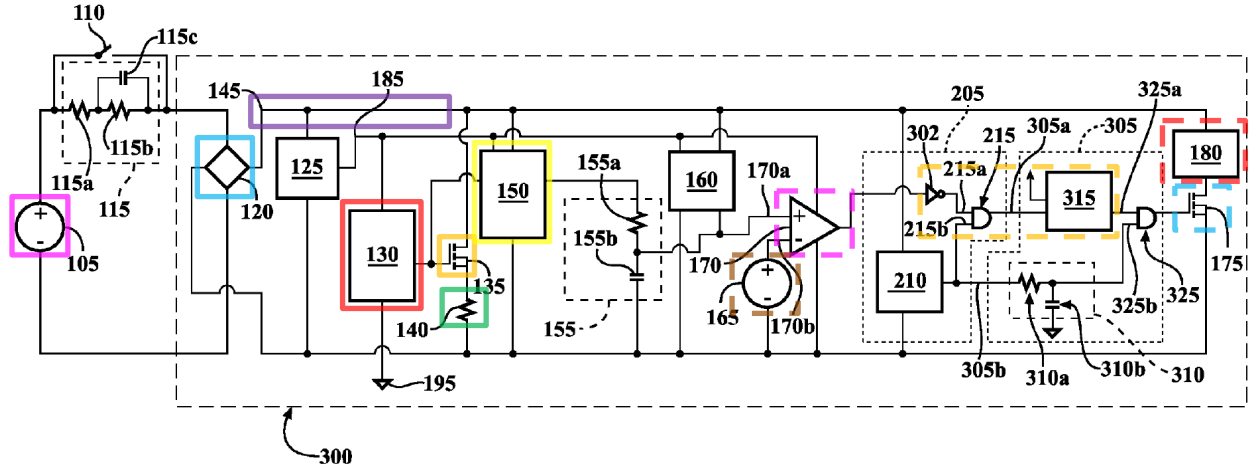


FIG. 3

EX1008, Fig. 3 (annotated); EX1002, ¶47. In this embodiment, “power input 105” (solid-pink) delivers AC line power to “current limiting circuit 300,” which includes “rectifier 120” (solid-blue) to rectify the power “from an AC wave to a DC wave.” EX1008, ¶¶[0015], [0020], [0041]; EX1002, ¶47. The rectified DC power is

provided to “device power rail 145” (purple) that connects to “main load 180” (dotted-red), which “may be an LED-based light or CFL.” EX1008, ¶¶[0016], [0037]; EX1002, ¶47.

“[L]oad switch 175” (dotted-blue) controls whether current may flow from rectifier 120 and device power rail 145 through main load 180. EX1008, ¶¶[0010], [0045]; EX1002, ¶48. In a “fault configuration” where power input 105 and the current limiting circuit are connected “through a subject, for example, a person’s body” (represented by “human body resistor-capacitor model 115”), load switch 175 “remains off” to prevent current flow through main load 180, “thereby maintaining the current flowing through the subject at a low and safe level.” EX1008, ¶¶[0013], [0010], [0035]-[0036], [0045]; EX1002, ¶48. By contrast, in a “normal circuit configuration” where power input 105 and the current limiting circuit are “connected directly” (represented by the closing of “switch 110”), load switch 175 is closed, allowing main load 180 to be powered on. EX1008, ¶¶[0013], [0010], [0035]-[0036], [0045]; EX1002, ¶48.

Ivey345’s current limiting circuit includes “auxiliary power supply 125,” which is directly powered by rectifier 120 and provides, e.g., a standard 5V digital supply voltage; and “oscillator 130” (solid-red), which is powered by auxiliary power supply 125. EX1008, ¶¶[0016]-[0017], [0019]; EX1002, ¶49. “[O]scillator 130 may be configured as a harmonic-type oscillator or a relaxation-type oscillator,

a crystal oscillator, a ring oscillator, a silicon micromechanical resonator, an oscillating output of a digital circuit or microprocessor, or any other type of oscillator.” EX1008, ¶¶[0019]; EX1002, ¶49.

Oscillator 130’s output is “electrically connected to an input of [a] test load switch 135 [(solid-orange)], such that the test load switch 135 is controlled by the oscillator 130.” EX1008, ¶¶[0021]-[0022], [0024]; EX1002, ¶50. Test load switch 135 is connected to device power rail 145 and “Z test load 140” (solid-green) such that, when test load switch 135 is closed by oscillator 130’s output, current is permitted to flow from device power rail 145 through Z test load 140. *Id.*

An auxiliary-powered “detector 150” (solid-yellow), which also receives oscillator 130’s clock signal and thus operates synchronously with test load switch 135’s activation, “detect[s] a variation in the current draw or voltage across the device power rail 145 due to the oscillating change in the current going through the Z test load 140” and “output[s] a signal in response to a change in the current of the Z test load 140.” EX1008, ¶¶[0024]-[0027]; EX1002, ¶51. Detector 150’s output signal is “a voltage, current, or other type of signal” that “decreases as the variation in the device power rail 145 increases” (i.e., a fault configuration) and “increases as the variation in the device power rail 145 decreases” (i.e., a normal configuration). EX1008, ¶¶[0024]-[0027], [0010]; EX1002, ¶51.

Detector 150’s output signal is noise-filtered by “detector low pass filter 155”

and then sent to the non-inverting input of an auxiliary-powered “comparator 170” (dotted-pink). EX1008, ¶¶[0028]-[0029], Fig. 3; EX1002, ¶52. Comparator 170 also receives the output of “detection threshold signal source 165” (dotted-brown) at comparator 170’s inverting input, compares these two inputs, “and produces an output relating to the comparison.” EX1008, ¶[0030], Fig. 3; EX1002, ¶52. Specifically, if detector 150’s output signal is lower than the threshold signal (corresponding to a fault configuration), comparator 170 outputs a “low” signal, and vice versa. EX1008, ¶¶[0030]-[0032]; EX1002, ¶52.

Comparator 170’s output is inverted by “logic inverter 302” and then sent to “main load shut-off latch 315” (together in dotted-orange), which “may be constructed from an electrical flip-flop” and, although not depicted in Figure 3, may be synchronized with oscillator 130’s clock signal. EX1008, ¶[0043]; EX1002, ¶53. The inverted comparator output is received at latch 315’s “‘clock’ input” to control whether latch 315 “should accept a state change.” EX1008, ¶[0044]; EX1002, ¶53. The output of latch 315 is connected to load switch 175’s input, which, as discussed, controls whether current may flow through main load 180. EX1008, ¶¶[0035]-[0036], [0045]-[0046], [0010]; EX1002, ¶53.

Initially, “main load shut-off latch 315 starts at power-up in the ‘on’ state” and thus latches a high output for turning on load switch 175. EX1008, ¶¶[0045]-[0046]; EX1002, ¶54. If a normal configuration is thereafter detected, then latch

315 correspondingly receives a low inverted comparator output signal, causing latch 315 to continue in the “on” state and thus current flow to be maintained through load switch 175 and main load 180. EX1008, ¶¶[0045]-[0046], [0030]-[0032]; EX1002, ¶54. However, if a fault configuration is detected at any time, then latch 315 instead receives a high inverted comparator output signal and thus changes to an off state, thereby “latching a low output” and “disabling” load switch 175. EX1008, ¶¶[0045]-[0046], [0030]-[0032]; EX1002, ¶54. Latch 315 thereafter remains in this off state until “power is removed from the circuit and reapplied.” EX1008, ¶¶[0044], [0041]; EX1002, ¶54.

3. Rationale to Combine Ivey813 with Ivey345

Ivey813 describes an “LED light tube,” which may be mains line powered. EX1007, 2:51-56; EX1002, ¶55; *see also* EX1001, 4:1-11; EX1013, 3-4. And Ivey345 teaches improving “LED-based lights[] and other line-powered electrical devices” by implementing a “current limiting circuit” within such lights for “protecting a person from electrical shock” during relamping. EX1008, ¶¶[0002], [0004]-[0005]; EX1002, ¶55. Thus, Ivey345 expressly teaches combining Ivey345’s current limiting circuit into a line-powered LED-based light, such as the mains line powered (type B) version of Ivey813’s LED-based light tube, and therefore contains an express teaching, suggestion, and motivation to combine the two references. EX1002, ¶55.

Such modification also improves user safety. As Ivey345 states, LED-based lights and other line-powered devices carry certain “drawbacks,” namely that a subject user may be electrically shocked during relamping if the subject makes contact with the bulb’s “return terminal” while the bulb’s “power terminal” is connected (a fault configuration). EX1008, ¶¶[0004]-[0005], [0013]; EX1002, ¶56; *accord* EX1013, 4. Such a risk of shock is present in Ivey813’s LED-based light tube when mains line powered. *See* EX1007, 5:33-39; EX1013, 4; EX1002, ¶56. Ivey345, however, provides a solution by disclosing a “current limiting circuit” that detects whether the above fault configuration is present and, when such is detected, prevents the LEDs in the LED-based light bulb from being energized and thus the user from being shocked. EX1008, ¶¶[0010], [0037]; EX1002, ¶56. Given such teachings, a POSITA would have thus been motivated to modify the line-powered version of Ivey813’s LED-based light tube by adding Ivey345’s current limiting circuit to power converter 36, because doing so would have enabled power converter 36 to additionally “convert the power received through the fixture” to “a low and safe level” when a fault configuration occurs, thereby improving user safety during relamping. *See* EX1007, 5:33-35; EX1008, ¶¶[0010], [0004]-[0005]; EX1002, ¶56.

4. The Resulting “Ivey Combination”

So modified, the combination of Ivey813 and Ivey345 (the “Ivey Combination”) comprises Ivey813’s “LED-based light tube,” which is mains line

powered by “fixture 11” (Ivey345’s “power source 105”) and utilizes Ivey345’s “current limiting circuit” as an additional circuit within “[p]ower converter 36” to control whether current may flow from power converter 36’s “rectifier circuit” (Ivey345’s “rectifier 120”) through the tube’s “LEDs 18” (Ivey345’s “main load 180”) based on the current draw or voltage across the tube (Ivey345’s “device power rail 145”). *See* EX1007, 5:31-40; EX1008, ¶¶[0024]-[0027], [0010]; EX1002, ¶57.

5. Element-by-Element Analysis

(a) Limitation [1pre]

To the extent claim 1’s preamble is limiting, the Ivey Combination meets it by utilizing Ivey345’s “current limiting circuit” (the claimed “installation detection circuit”) within “power converter 36” of Ivey813’s “LED-based light tube” (“configured in a light-emitting diode (LED) tube lamp”). EX1007, 5:33-35; EX1008, ¶[0010]; Section VI.A.4; EX1002, ¶58; *see also* Sections VI.A.5(b)-VI.A.5(h).

Further, the tube receives mains AC power from “fixture 11” (Ivey345’s “power source 105” (solid-pink)) (“configured to receive an external driving signal”) and, using power converter 36’s “rectifier circuit” (Ivey345’s “rectifier 120” (solid-blue)), rectifies such power “to a DC wave”:

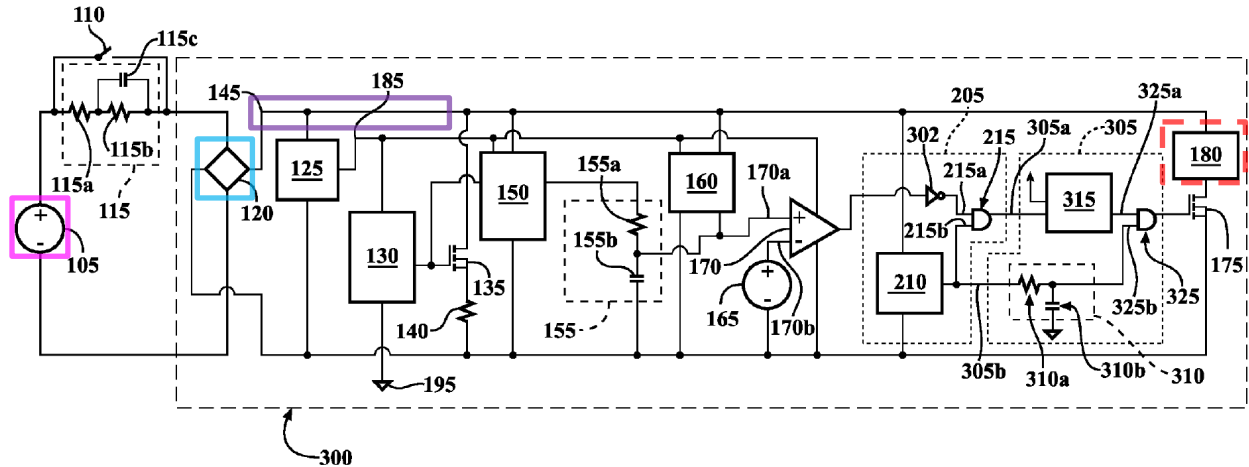


FIG. 3

EX1007, 2:51-56, 5:36-39; EX1008, Fig. 3 (annotated), ¶¶[0012], [0015]-[0016]; Section VI.A.4; EX1002, ¶59. This DC power is provided to “LEDs 18” (Ivey345’s “main load 180” (dotted-red)) from the rectifier circuit (via Ivey345’s “device power rail 145” (solid-purple)). EX1007, 5:33-35; EX1008, ¶¶[0016], [0037]; Section VI.A.4; EX1002, ¶59.

(b) Limitation [1a]

Ivey345’s current limiting circuit includes “oscillator 130” (solid-red) that outputs a clock signal that oscillates high and low, e.g., “a digital, continuous time output, a varying sinusoidal output, or another type of output” (“pulse generating circuit configured to output one or more pulse signals”):

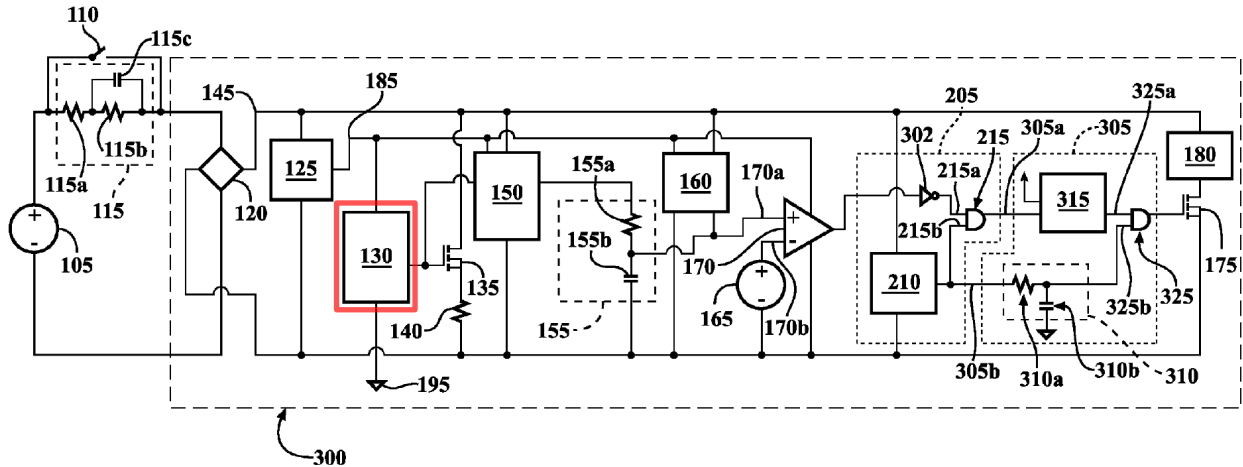


FIG. 3

EX1008, Fig. 3 (annotated), ¶¶[0019], [0044]; EX1002, ¶60; *see also* EX1001, 41:23-27 (defining a “high logic level signal” as a “pulse signal”), 41:38-43 (defining a “low logic level signal” as the “stop[]” of the output of a pulse signal).

(c) Limitation [1b]

Also included are “test load switch 135” (solid-orange) and “Z test load 140” (solid-green):

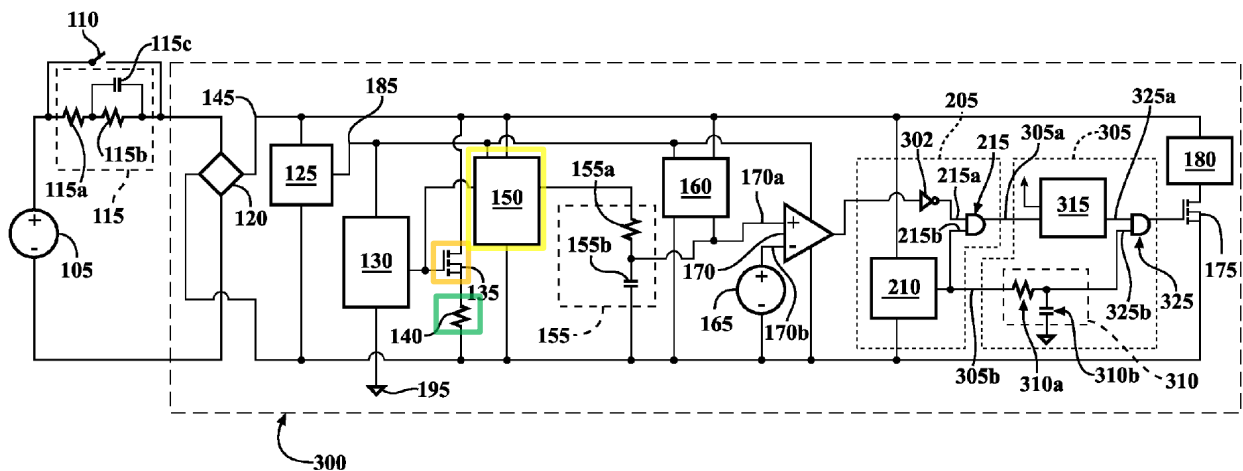


FIG. 3

EX1008, Fig. 3 (annotated), ¶¶[0021]-[0023]; EX1002, ¶61. Oscillator 130’s output

is connected to the gate of test load switch 135, which opens and closes when oscillator 130's clock signal oscillates low and high, respectively. EX1008, ¶¶[0020]-[0022], [0024], Fig. 3; EX1002, ¶61. When test load switch 135 is closed by oscillator 130's high output ("during at least one of the one or more pulse signals"), current is permitted to flow from device power rail 145 through Z test load 140. EX1008, ¶¶[0020]-[0024]; EX1002, ¶61.

The current limiting circuit further includes "detector 150" (solid-yellow), which also receives oscillator 130's clock signal and thus operates synchronously with test load switch 135's activation. EX1008, ¶[0024]; EX1002, ¶62. Detector 150 "detect[s] a variation in the current draw or voltage across the device power rail 145 due to the oscillating change in the current going through the Z test load 140" ("detecting a signal generated from the external driving signal"). EX1008, ¶¶[0024]-[0027]; EX1002, ¶62. This detected variation is used to detect whether a fault configuration exists ("detect... whether the LED tube lamp is properly installed on a lamp socket"): an "increase[d]" variation corresponds to a fault caused by "the presence of a subject," whereas a "decrease[d]" variation corresponds to a normal "metallic connection" between the tube and fixture. EX1008, ¶¶[0024]-[0026], [0010]; EX1002, ¶62; *see also infra* Sections VI.A.5(e)-VI.A.5(f).

(d) Limitation [1c]

The current limiting circuit includes not only test load switch 135 but also

“load switch 175” (dotted-blue):

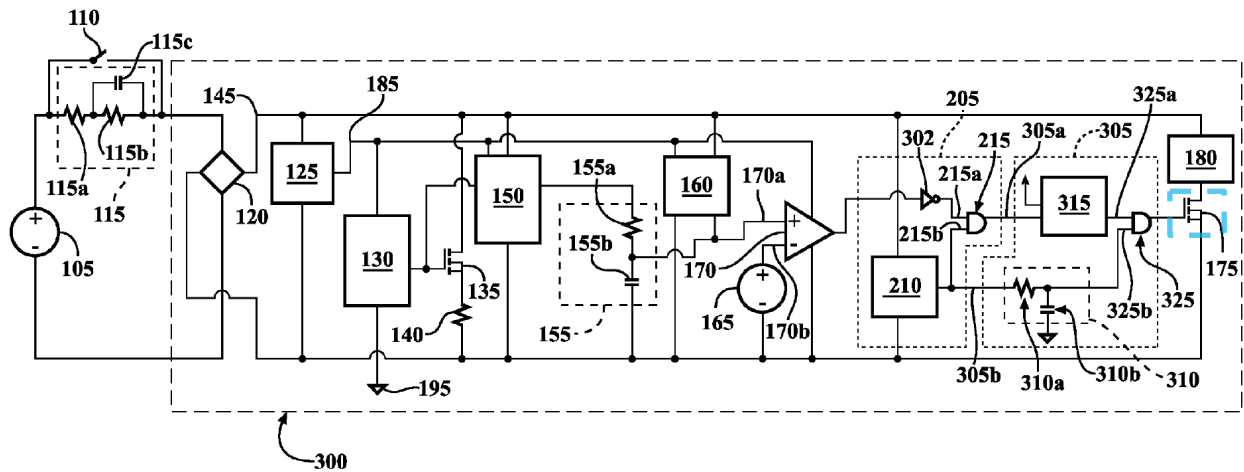


FIG. 3

EX1008, Fig. 3 (annotated) ¶¶[0010], [0035]-[0036], [0045]; EX1007, 2:57-60, 3:24-27; EX1002, ¶63. Load switch 175 meets the claimed “switch circuit.” EX1002, ¶63. Specifically, detector 150, which is synchronized with oscillator 130’s clock signal (“coupled to the pulse generating circuit”), detects a variation across device power rail 145. EX1008, ¶¶[0024]-[0027]; EX1002, ¶63. This detected variation is thus based on oscillator 130’s clock signal and ultimately determines whether load switch 175 is powered on or off. EX1008, ¶¶[0024]-[0027], [0030]-[0032], [0010], [0044]-[0045]; Section VI.A.5(c); EX1002, ¶63. Oscillator 130’s output therefore controls whether load switch 175 is powered on or off (“the one or more pulse signals control turning on and off of the switch circuit”). EX1002, ¶63.

Alternatively, load switch 175 and test load switch 135 together form the claimed “switch circuit”:

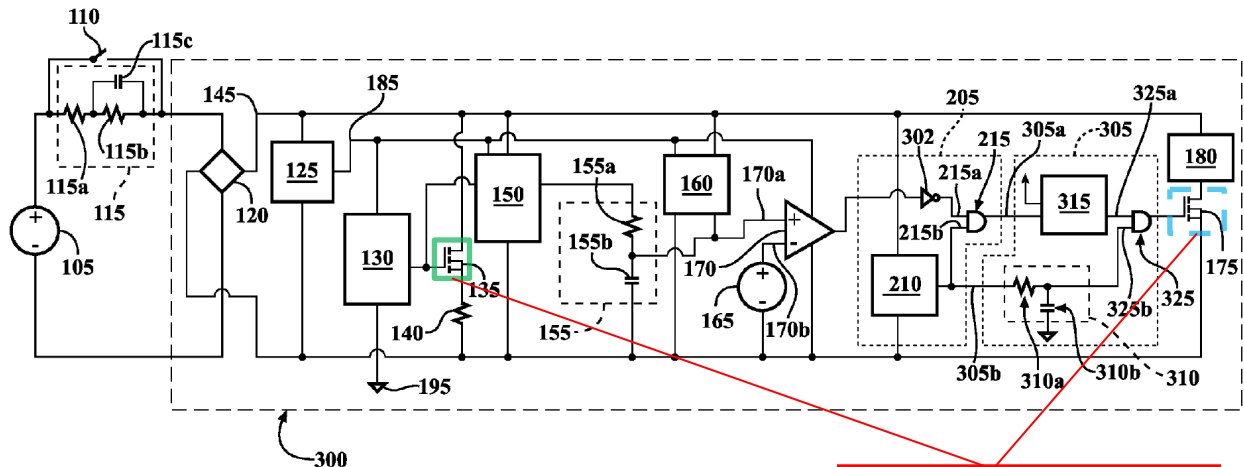


FIG. 3

Together, the claimed
“switch circuit”

EX1008, Fig. 3 (annotated); EX1002, ¶64. Specifically, test load switch 135’s gate is connected to oscillator 130’s output (“coupled to the pulse generating circuit”), causing test load switch 135 to open and close as oscillator 130’s clock signal oscillates low and high, respectively (“the one or more pulse signals control turning on and off of the switch circuit”). EX1008, ¶¶[0020]-[0022], [0024], Fig. 3; EX1002, ¶64. Further, a POSITA would have understood that a plurality of separate transistor switches that perform the claimed functions of the “switch circuit” would together meet the claimed “switch circuit.” EX1001, 9:28-51; EX1002, ¶64; *see also, e.g.*, EX1011 (showing numerous “2 N-Channel (Dual)” FET products—i.e., two n-type MOSFETs formed on one integrated **circuit**—were commercially available by the ECPD); EX1012 (datasheet for Fairchild Semiconductor FDG6303N, which is the first “2 N-Channel (Dual)” FET product listed in EX1011).

(e) Limitation [1d]

When detector 150 detects an increased variation across device power rail 145 corresponding to a fault configuration, detector 150 outputs a correspondingly “decrease[d]” signal, which is received by “comparator 170” (dotted-pink):

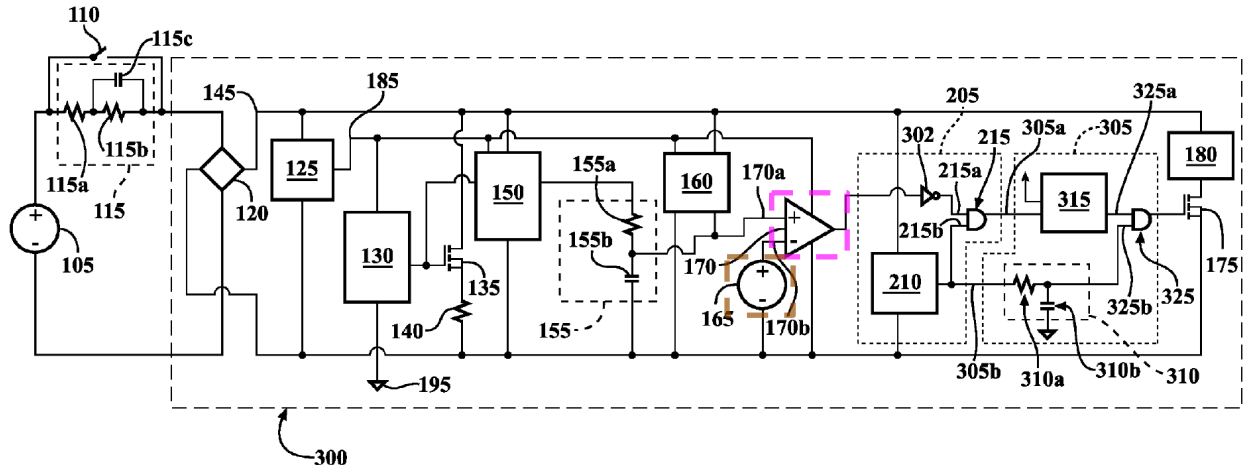


FIG. 3

EX1008, Fig. 3 (annotated), ¶¶[0024]-[0026], [0010], [0028]-[0029], [0034]; EX1002, ¶65. Comparator 170’s output ultimately determines whether load switch 175 is activated and thus whether current may flow from device power rail 145 through the LEDs. EX1008, ¶¶[0030]-[0032], [0010], [0041], [0044]-[0045]; EX1002, ¶65. Specifically, comparator 170 compares detector 150’s output signal to the output of “detection threshold signal source 165” (dotted-brown) and “produces an output relating to the comparison.” EX1008, ¶[0030]; EX1002, ¶65. When detector 150’s output signal is lower than the threshold signal (fault configuration), comparator 170 outputs a “low” signal that ultimately causes load

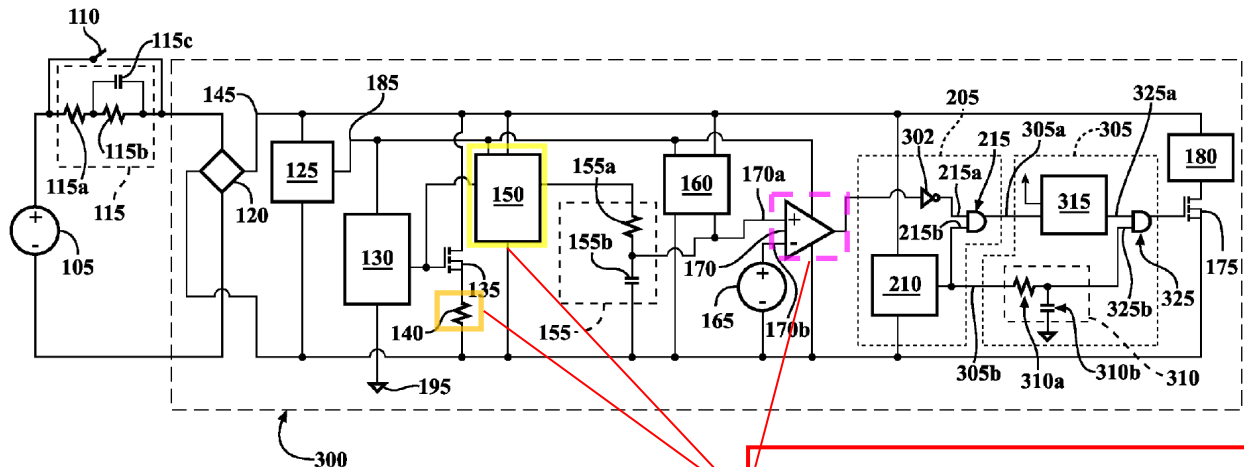
switch 175 to “remain[] off.” EX1008, ¶¶[0030]-[0032], [0010], [0044]-[0045]; EX1002, ¶65. When oscillator 130’s clock signal thereafter oscillates low, test load switch 135 likewise opens, thus opening device power rail 145. EX1008, ¶¶[0020]-[0022], [0024]; EX1002, ¶65.

(f) Limitation [1e]

By contrast, when detector 150 detects a decreased variation across device power rail 145 corresponding to a normal configuration, detector 150 outputs a correspondingly “increase[d]” signal to comparator 170. EX1008, ¶¶[0024]-[0026], [0028]-[0029], [0010]; EX1002, ¶66. When detector 150’s output signal is higher than the threshold signal (normal configuration), comparator 170 outputs a “high” signal that ultimately causes load switch 175 to remain powered on, allowing current to continue flowing through the LEDs. EX1008, ¶¶[0030]-[0032], [0041], [0044]-[0045], [0010]; EX1002, ¶66.

(g) Limitation [1f]

Detector 150, comparator 170, and Z test load 140 altogether form the claimed “detection determining circuit.” EX1002, ¶67. *Compare* EX1008, Fig. 3 (annotated below), *with, e.g.*, EX1001, Fig. 15K, 49:63-50:47.

**FIG. 3**

Together, the claimed
“detection determining circuit”

Specifically, synchronously with oscillator 130's clock signal, detector 150 detects a variation across device power rail 145—namely “a change of voltage of, or current through, the device power rail 145 and/or the Z test load 140” (“signal generated from the external driving signal is a sampling signal on the power loop”). EX1008, ¶¶[0024], [0026]-[0027]; EX1002, ¶67.

Based on the detected variation, detector 150 outputs a corresponding detection signal to comparator 170, which compares the detection signal to the threshold signal to detect whether a fault configuration exists. EX1008, ¶¶[0024]-[0032], [0010]; EX1002, ¶68.

Lastly, during operation, current flows from device power rail 145 through test load switch 135, load switch 175, and Z test load 140 (“the power loop includes the switch circuit and the detection determining circuit”). EX1008, ¶¶[0021]-[0027], [0010], [0035]-[0036], [0045]; EX1002, ¶69.

(h) Limitation [1g]

Oscillator 130's sole input is power from "auxiliary power supply 125," which simply receives DC power from 120. EX1008, ¶¶[0016], [0019]; EX1002, ¶70. Thus, oscillator 130 receives no input from, and therefore operates independently as claimed from, the current limiting circuit's downstream operations. EX1002, ¶70. Indeed, Ivey345 teaches that oscillator 130 may be "a ring oscillator," which operates simply via a DC input and thus generates an oscillating output independently from downstream devices that receive the oscillating output. *See* EX1008, ¶[0019]; EX1018,⁵ 1-3; EX1002, ¶70.

(i) Limitation [3a]

A normal configuration is detected when detector 150 detects a decreased variation across device power rail 145 and outputs a correspondingly increased signal to comparator 170, which determines that detector 150's output is higher than the threshold signal ("sampling signal is greater than or equal to a predefined signal"). EX1008, ¶¶[0024]-[0032], [0010]; EX1002, ¶71.

(j) Limitation [3b]

A fault configuration is detected when detector 150 detects an increased variation across device power rail 145 and outputs a correspondingly decreased

⁵ *See* EX1038, ¶¶45-52 (establishing public availability on or shortly after February 28, 2010).

signal to comparator 170, which determines that detector 150's output is lower than the threshold signal ("sampling signal is smaller than a predefined signal").
EX1008, ¶¶[0024]-[0032], [0010]; EX1002, ¶72.

(k) Limitation [4pre]

To the extent claim 4's preamble is limiting, the Ivey Combination meets it.
See Sections VI.A.5(a), VI.A.5(l)-VI.A.5(m).

(l) Limitations [4a]-[4f]

See Sections VI.A.5(b)-VI.A.5(g).

(m) Limitation [4g]

Comparator 170's output does not go directly to load switch 175, but is instead inverted by "logic inverter 302" and then inputted into "main load shut-off latch 315" (together in dotted-orange), which "may be constructed from an electrical flip-flop" and has its output connected to load switch 175's input:

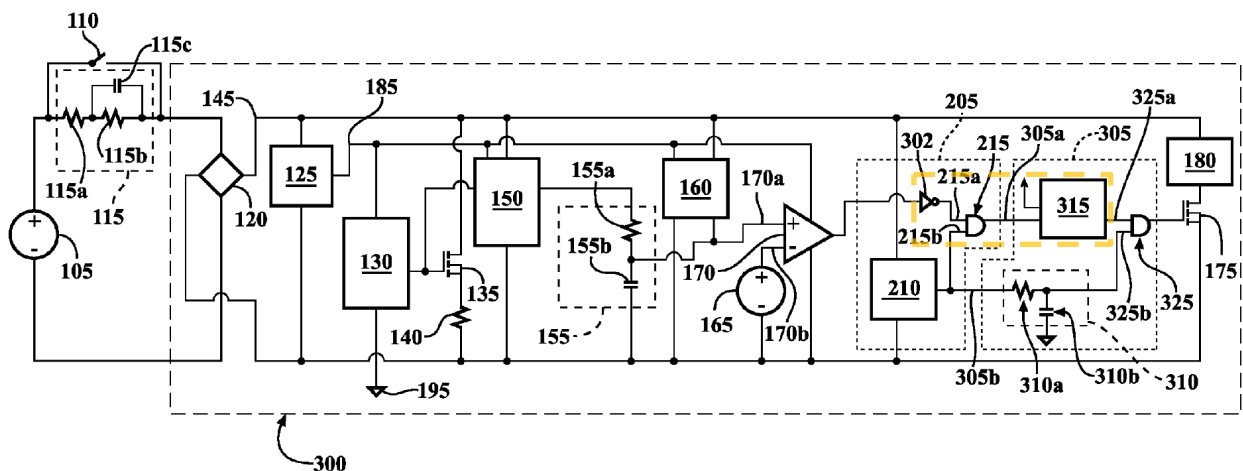


FIG. 3

EX1008, Fig. 3 (annotated) ¶¶[0039]-[0041], [0043], [0045]-[0046]; EX1002, ¶75.

Logic inverter 302 and latch 315 altogether form the claimed “detection result latching circuit.” EX1002, ¶75; *see also* EX1001, 9:28-51. Though not depicted, latch 315 receives—and thus synchronizes its operation with—oscillator 130’s clock signal (“the detection result latching circuit is configured to receive the one or more pulse signals”). EX1008, ¶¶[0043]-[0045]; EX1002, ¶75. During such synchronized operation, latch 315 also receives the inverted comparator output to control whether latch 315 should latch a “high” or “low” output to control turning on or off load switch 175. EX1008, ¶¶[0043]-[0046], [0030]-[0032]; EX1001, 38:58-62; Section V.C.3; EX1002, ¶75.

Alternatively, should the *CH* Court’s construction of “detection result latching circuit” apply (*see* EX1026, 6; Section V.C.3), Ivey345 teaches more specifically that latch 315 receives oscillator 130’s clock signal either directly from oscillator 130 or indirectly via another synchronized device, e.g., “detection validation timer 210.” EX1008, ¶¶[0043], [0039]; EX1002, ¶76. In other words, Ivey345 teaches that oscillator 130’s clock signal is outputted to each synchronized device either individually using parallel interconnections or serially using “daisy chaining”—a commonly used circuit design technique for synchronizing devices where a first device (e.g., timer 210) receives the clock signal and outputs the clock signal to a second device (e.g., latch 315), which may do the same to a third device, and so forth to establish a serial daisy chain cascade that synchronizes each connected device.

EX1008, ¶¶[0043], [0039]; EX1002, ¶76; *see also, e.g.*, EX1014, 5:36-56, Fig. 2.

And as commonly known, daisy chaining provides numerous advantages over parallel interconnections, including “utilizing fewer and shorter interconnections [to] make[] the overall implementation less vulnerable to undesirable effects, such as propagation delay and crosstalk,” thereby “allow[ing] the devices to be operated at higher speeds,” while also “reduc[ing] complexity [to] enable[] a subsystem containing the devices to be implemented in a smaller area thus allowing the subsystem to occupy a smaller footprint.” EX1014, 2:29-54; EX1002, ¶76.

To gain such advantages, a POSITA would have recognized that, while oscillator 130’s clock signal could be at least partially daisy chained as disclosed in Ivey345 by connecting oscillator 130 to timer 210 to latch 315 (EX1008, ¶¶[0039], [0043]), a more preferable configuration would have been to fully daisy chain the devices to be synchronized—e.g., by then also connecting latch 315 to test load switch 135 to detector 150 (*see id.*, ¶¶[0021], [0024], [0039], [0043])—to maximize such benefits. EX1002, ¶77. Doing so, latch 315 therefore receives and outputs oscillator 130’s clock signal to test load switch 135. EX1002, ¶77. And when oscillator 130’s clock signal oscillates high or low, this output from latch 315 to test load switch 135 would likewise be high or low, respectively. *See* EX1026, 6 (“outputs a high logic value when either... ***the pulse signal output terminal***... has a high logic value”); EX1002, ¶77. At the same time, latch 315, as discussed, also

receives the inverted comparator output to control whether latch 315 should latch a “high” or “low” output to turn on or off load switch 175.⁶ EX1026, 6 (“*stores the detected result* and outputs a high logic value when either *the stored detected result*... has a high logic value”); EX1008, ¶¶[0043]-[0046], [0030]-[0032]; EX1002, ¶77.

(n) Limitation [21pre]

To the extent claim 21’s preamble is limiting, the Ivey Combination meets it. See Sections VI.A.5(a), VI.A.5(o)-VI.A.5(u).

(o) Limitation [21a]

Oscillator 130 is an equivalent of the ’140 Patent’s module 2540—a structure corresponding to the claimed “means for generating” (Section V.C.1)—because oscillator 130 similarly is specified as an empty box (*compare* EX1008, Fig. 3, *with* EX1001, Fig. 15B), is nevertheless considered a “circuit”⁷ (*compare* EX1008, ¶[0019], *with* EX1001, 39:10-25), and performs the identical function of “generating

⁶ Should a mapping of “switch circuit” be required here, load switch 175 and test load switch 135 would thus together form the “switch circuit” (and not load switch 175 alone). See Section VI.A.5(d); EX1002, ¶77 n.2.

⁷ The word “circuit” alone sufficiently connotes structure. *MIT v. Abacus Software*, 462 F.3d 1344, 1355 (Fed. Cir. 2006).

one or more pulse signals” as claimed by producing a clock signal that oscillates high and low (*compare* EX1008, ¶¶[0019]-[0020], *with* EX1001, 38:28-62). EX1002, ¶79. By performing the identical function as claimed in substantially the same way to produce substantially the same results as module 2540, oscillator 130 therefore meets the claimed “means for generating.” EX1002, ¶79.

(p) Limitation [21b]

Structures corresponding to the claimed “means for detecting” include the ’140 Patent’s module 2570. Section V.C.2; EX1002, ¶80. Module 2570 is specified as an empty box, but it is nevertheless a “detection determining *circuit*.” EX1001, 38:39-44, Fig. 15B; EX1002, ¶80.

As discussed in Section VI.A.5(g), Ivey345’s current limiting circuit includes detector 150, comparator 170, and Z test load 140, which altogether form a detection determining *circuit*. EX1008, ¶¶[0022]-[0023], [0029]; EX1002, ¶81. Such a circuit is equivalent to module 2570, because it detects, synchronously with oscillator 130’s clock signal, a variation across device power rail 145 to detect whether a fault configuration exists, thus matching the construed function discussed in Section V.C.2 of “detecting a sampling signal on the power loop during the one or more pulse signals for determining whether the LED tube lamp is properly installed.” EX1008, ¶¶[0024]-[0027], [0010]; Sections VI.A.5(g), VI.A.5(c)-VI.A.5(e); EX1002, ¶81. By performing the identical function as claimed in

substantially the same way to produce substantially the same results as module 2570, the combined circuit of detector 150, comparator 170, and Z test load 140 oscillator 130 therefore meets the claimed “means for detecting.” EX1002, ¶81.

(q) Limitation [21c]

See Sections VI.A.5(o), VI.A.5(d).

(r) Limitation [21d]

See Section VI.A.5(e).

(s) Limitation [21e]

See Section VI.A.5(f).

(t) Limitation [21f]

See Sections VI.A.5(p), VI.A.5(g).

(u) Limitation [21g]

Within the Ivey Combination, power converter 36 of Ivey813’s LED-based light tube includes a rectifier circuit (Ivey345’s rectifier 120), which rectifies mains AC power from “fixture 11” (Ivey345’s “power source 105”) to DC power, and Ivey345’s current limiting circuit, which is powered by the rectifier circuit. EX1007, 5:33-39; EX1008, ¶¶[0012], [0015]-[0016]; Section VI.A.4; EX1002, ¶86. Power converter 36, however, also includes “a current regulator circuit” that, as a POSITA would have recognized, includes a filtering circuit and is downstream from the current limiting circuit (“filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the

filtering circuit”). *See* EX1007, 5:33-35; Section VI.A.4; EX1002, ¶86.

Specifically, a POSITA would have recognized power converter 36’s current regulator circuit to be a “constant-current power suppl[y]”—also known as a “buck converter”—that regulates LED current to be constant such that light output is also constant. *See* EX1019, 5-6; EX1020, ¶¶[0011], [0017], [0020]; EX1021, 4:66-5:2, 5:33-35; EX1009, ¶[0060]; EX1002, ¶87. Such current regulators operate on a wide input voltage range and output a constant current by utilizing an inductor and switch in series with the LED load, where the switch is periodically opened and closed to charge and discharge the inductor at a specific frequency such that the output current to the LEDs is generally constant. EX1019, 6; EX1020, ¶[0061]; EX1021, 10:15-36; EX1009, ¶[0124]; EX1002, ¶87. This periodic switching, however, also causes a “pulsation component (ripple)” to be outputted. EX1021, 5:50-57; EX1002, ¶87. To address this issue, a filter such as a “smoothing” capacitor is inserted afterwards to filter out the ripples and thus reduce flickering of the LEDs. EX1020, ¶[0038]; EX1021, 5:50-57; EX1009, ¶[0125]; EX1002, ¶87. Power converter 36’s current regulator circuit therefore would have included—and a POSITA would have otherwise been motivated to ensure such included—a filter such as a smoothing capacitor. EX1002, ¶87.

Further, a POSITA would have also recognized the current regulator circuit to be downstream from Ivey345’s current limiting circuit in the Ivey Combination—

e.g., immediately before, or part of, main load 180. EX1002, ¶88. Specifically, Ivey345 teaches, when incorporating its current limiting circuit, to directly connect the current limiting circuit's output to "a power supply that connects directly to the main load 180"—e.g., power converter 36's current regulator circuit, which, as discussed, is a "constant-current *power suppl[y]*." EX1008, ¶[0011]; EX1007, 5:33-39; EX1020, ¶[0011]; EX1002, ¶88. Indeed, a POSITA would have known to place the current limiting circuit before and not after the current regulator circuit for operability, because, while the current regulator circuit operates on a "wide input voltage range" and thus operates even when a fault configuration exists (*see* EX1019, 6; EX1007, 5:36-39; EX1008, ¶[0010]), the current regulator circuit nevertheless outputs a constant, nonvarying current (*see* EX1019, 5-6; EX1020, ¶¶[0011], [0017], [0020]; EX1021, 4:66-5:2, 5:33-35; EX1009, ¶[0060]), which, if inputted into the current limiting circuit, would prevent the detection of a fault configuration because there would be no detectable variation across device power rail 145 (*see* EX1008, ¶¶[0024]-[0026], [0010]). EX1002, ¶88. Because the current regulator circuit is downstream from the current limiting circuit and contains a filtering circuit, the Ivey Combination therefore meets limitation [21g]. EX1002, ¶88.

(v) Limitations [22a]-[22b]

Ivey345's detector 150, comparator 170, and Z test load 140 together detect

whether a fault configuration exists by detecting a variation across device power rail 145, generating a corresponding detection signal in response, and determining whether this detection signal is higher or lower than the threshold signal. EX1008, ¶¶[0024]-[0032], [0010]; Sections VI.A.5(i)-VI.A.5(j); EX1002, ¶89.

(w) Claim 23

See Sections VI.A.5(p), VI.A.5(m).

(x) Limitation [24pre]

To the extent claim 24's preamble is limiting, the Ivey Combination meets it by utilizing, within "power converter 36" of Ivey813's "LED-based light tube," Ivey345's "current limiting circuit" to detect during relamping whether a subject user is making contact with the tube's return terminal while the tube's power terminal is connected to "fixture 11" and, if such occurs, to "maintain[] the current flowing through the subject at a low and safe level." EX1007, 2:50-56, 5:33-35; EX1008, ¶¶[0010], [0004]-[0005]; Section VI.A.4; EX1002, ¶91; *see also* Sections VI.A.5(y)-VI.A.5(bb).

(y) Limitation [24a]

The current limiting circuit protects from the risk of shock when a fault configuration occurs. EX1008, ¶¶[0005], [0013]; EX1002, ¶92. The current limiting circuit includes oscillator 130 that, during operation, outputs an oscillating clock signal ("generating one or more pulse signals by a pulse generating circuit"). EX1008, ¶[0019]; EX1002, ¶92.

(z) Limitation [24b]

Also included are detector 150, comparator 170, and Z test load 140, which altogether form the claimed “detection determining circuit.” EX1008, ¶¶[0022]-[0023], [0029]; Section VI.A.5(g); EX1002, ¶93.

Oscillator 130’s output is connected to test load switch 135, which opens and closes when oscillator 130’s clock signal oscillates low and high, respectively. EX1008, ¶¶[0020]-[0022], [0024], Fig. 3; Section VI.A.5(c); EX1002, ¶94. When test load switch 135 is closed accordingly, current flows from the tube’s rectifier 120 and device power rail 145 through Z test load 140. EX1008, ¶¶[0020]-[0024]; Section VI.A.5(c); EX1002, ¶94. Then, synchronously with oscillator 130’s clock signal, detector 150 detects a variation across device power rail 145 (“detecting a sampling signal on a power loop of the LED tube lamp by a detection determining circuit”). EX1008, ¶¶[0024], [0026]-[0027]; Section VI.A.5(c); EX1002, ¶94. Detector 150 then outputs a corresponding detection signal to comparator 170, which compares this signal to the threshold signal to detect whether a fault configuration exists. EX1008, ¶¶[0024]-[0032], [0010]; Sections VI.A.5(e)-VI.A.5(f); EX1002, ¶94.

(aa) Limitation [24c]

Comparator 170’s output is inverted by logic inverter 302 and then inputted into latch 315. EX1008, ¶¶[0038]-[0041], [0043]-[0045]; EX1002, ¶95. Logic

inverter 302 and latch 315 together form the claimed “detection result latching circuit.” Section VI.A.5(m); EX1002, ¶95. Latch 315’s output is connected to the input of load switch 175 (EX1008, ¶¶[0043]-[0046]), which alone or together with test load switch 135 forms the claimed “switch circuit.” Section VI.A.5(d); EX1002, ¶95. Further, during operation, current flows from device power rail 145 through both test load switch 135 and load switch 175 (“switch circuit is on the power loop”). EX1008, ¶¶[0021]-[0024], [0010], [0035]-[0036], [0045]; Section VI.A.5(m); EX1002, ¶95; *see also* Section VI.A.5(g).

Latch 315—which receives oscillator 130’s clock signal and thus operates synchronously with test load switch 135’s activation (EX1008, ¶¶[0043], [0024])—latches either a “high” or “low” output to close or open load switch 175, respectively, depending on whether the inverted comparator output is “low” or “high” (*id.*, ¶¶[0045]-[0046], [0030]-[0032]). Section VI.A.5(m); EX1002, ¶96. Load switch 175 accordingly receives latch 315’s output, which is generated based on oscillator 130’s clock signal and the inverted comparator output, and thus, consistent with PO’s infringement contentions in the *Current* Action, load switch 175 receives oscillator 130’s output through latch 315 (“receiving the one or more pulse signals through a detection result latching circuit by a switch circuit”). EX1034, 53 (“Switch circuit CP2 receives signal S4 output from the detection result latching circuit which is generated based on the [pulse signal] signal S5 and [detection result] S9.”);

EX1035, 57 (same); EX1002, ¶96.

Alternatively, should the *CH* Court’s construction of “detection result latching circuit” be applied (*see* EX1026, 6; Section V.C.3), a POSITA would have been motivated to daisy chain oscillator 130’s output to, e.g., timer 210, latch 315, test load switch 135, and detector 150. Section VI.A.5(m); EX1002, ¶97. Latch 315 would thus output a high or low logic value signal to test load switch 135 when oscillator 130’s clock signal oscillates high or low, respectively, while at the same time latching either a “high” or “low” output to turn on or off load switch 175 based on the inverted comparator output, thereby meeting the “detection result latching circuit” as construed by the court. Section VI.A.5(m); EX1002, ¶97.

(bb) Limitation [24d]

When detector 150’s output signal is lower than the threshold signal, comparator 170 outputs a “low” signal, which is inverted by logic inverter 302 and then sent to latch 315. EX1008, ¶¶[0030]-[0032], [0038]-[0041], [0044]-[0045]; EX1002, ¶98. In response, latch 315 “latch[es] a low output,” causing load switch 175 to “remain[] off,” thereby preventing current from flowing from device power rail 145 through the LEDs. EX1008, ¶¶[0044]-[0046], [0030]-[0032], [0010]; EX1002, ¶98. When oscillator 130’s clock signal thereafter oscillates low, test load switch 135 likewise opens, causing device power rail 145 overall to be open (“controlling the switch circuit to remain in an off state to cause the power loop of

the LED tube lamp to be open.”). EX1008, ¶¶[0020]-[0022], [0024], Fig. 3; EX1002, ¶98.

(cc) Limitations [25a]-[25c]

See Section VI.A.5(bb). Comparator 170’s “low” output forms the claimed “first low level signal,” and latch 315’s “low” output forms the “second low level signal.” EX1002, ¶99.

(dd) Claim 26

By contrast, if comparator 170 determines that detector 150’s output signal is higher than the threshold signal, then comparator 170 outputs a “high” signal, which is inverted by logic inverter 302 and then sent to latch 315. EX1008, ¶¶[0030]-[0032], [0038]-[0041], [0044]-[0045]; EX1002, ¶100. In response, latch 315 continues in an “on” state and thus latches a “high” output, causing load switch 175 to remain powered on to maintain current flow from device power rail 145 through the LEDs. EX1008, ¶¶[0044]-[0046], [0030]-[0032], [0010]; EX1002, ¶100.

(ee) Limitations [27a]-[27c]

See Section VI.A.5(dd). Comparator 170’s “high” output forms the claimed “first high level signal,” and latch 315’s “high” output forms the “second high level signal.” EX1002, ¶101.

(ff) Claim 28

Oscillator 130 outputs an oscillating signal with frequency “for example at or about 1Khz” (“period... between 10 microseconds and 1 millisecond”). EX1008,

¶¶[0019]-[0020]; EX1002, ¶102.

(gg) Limitations [30a]-[30b]

See Sections VI.A.5(i)-VI.A.5(j).

(hh) Claim 31

See Section VI.A.5(m).

(ii) Claim 35

See Section VI.A.5(ff).

B. Ground 2: Ivey813, Ivey345, and Sadwick Render Obvious Claims 1, 3-4, 21-28, 30-31, and 35

Ground 2 addresses PO’s potential argument that Ground 1 fails because Ivey345’s test load switch 135 and Z test load 140 are in parallel, not series, with main load 180 (LEDs).

1. Sadwick

Sadwick is directed to a “fluorescent lamp replacement” (“FLR”) for replacing “[c]onventional fluorescent tubes.” EX1009, ¶¶[0004], [0066], [0001]; EX1002, ¶107. The FLR includes “a rectification stage” that “accepts either an AC lines input”—i.e., the FLR is a type B LED light tube that accepts a standard “100 to 300 VAC 50 Hz or 60 Hz AC line input”—“or a ballast output.” EX1009, ¶¶[0066], [0173], [0161]; EX1001, 4:1-11; EX1013, 3-4; EX1002, ¶107. The FLR also includes a “light source” such as one such “made up of LEDs.” EX1009, ¶[0066]; EX1002, ¶107.

Sadwick notes that, “when the fluorescent lamp replacement is being installed, [a] pin can be exposed and, without protection mechanisms, can shock and injure a user contacting the pin and appearing as an abnormal ground through which an electrical current can flow.” EX1009, ¶[0071] (diagram numbering omitted); EX1002, ¶108. To address this “fault hazard condition,” Sadwick’s FLR “provid[es] shock hazard protection against inadvertent contact with exposed pin(s).” EX1009, ¶¶[0082], [0073]; EX1002, ¶108. Sadwick’s Figure 14 depicts such “hazard protection circuitry”:

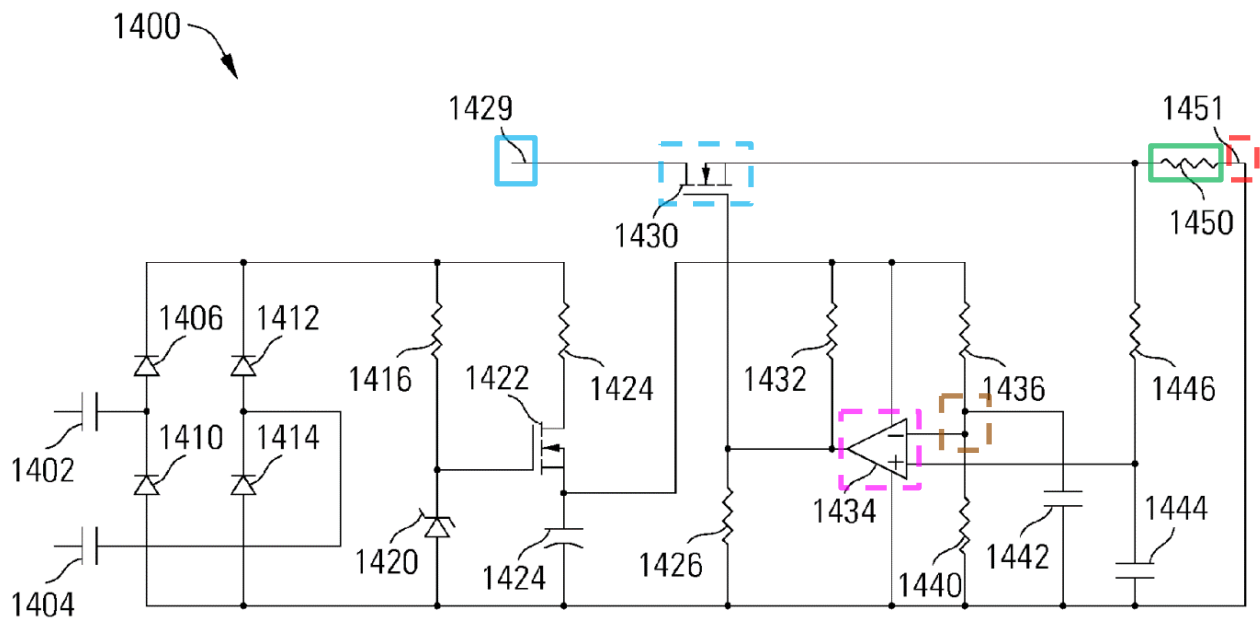


FIG. 14

EX1009, ¶¶[0080], [0082], Fig. 14 (annotated); EX1002, ¶108. As shown, an “input rectification stage of the FLR” is connected to node 1429 (solid-blue). EX1009, ¶[0080]; EX1002, ¶108. The “LED (or OLED or QD) load of the FLR” is connected

to node 1451 (dotted-red). EX1009, ¶[0080]; EX1002, ¶108. Between these nodes is “[t]ransistor/switch 1430” (dotted-blue) and “sense resistor 1450” (solid-green), which are thus “in series with” the FLR’s rectifier and LED load. EX1009, ¶[0080]; EX1002, ¶108.

Sadwick’s hazard protection circuitry detects whether the fault hazard condition above is present by feeding “the voltage across sense resistor 1450” into “the non-inverting input of [a] comparator 1434” (dotted-pink). EX1009, ¶[0080]; EX1002, ¶109. At the same time, “a reference set point” (dotted-brown) “is fed to the inverting terminal of [the] comparator 1434 such that when the signal from the sense resistor 1450 is larger than the reference set point signal, the comparator 1434 goes high and turns on transistor 1430” and thus “current/voltage is allowed to flow to the LED or OLED or QD load.” EX1009, ¶[0080]; EX1002, ¶109. By contrast, “[i]f the current through the sense resistor 14[5]0 produces too small of a voltage then transistor 1430 is turned off preventing current from flowing and thus limiting and preventing a hazard/shock/leakage current condition from occurring.” EX1009, ¶¶[0080], [0082]; EX1002, ¶109.

Once transistor 1430 is turned off, Sadwick’s hazard protection circuitry “allow[s] for diverse possible responses,” including causing transistor 1430 to be “complete[ly] turn[ed]-off (i.e., latch[ed] off) until power is cycled (i.e., turned off and then turned back on) or, as another example, periodically turned back on for a

brief moment to see if the hazard fault condition had cleared (i.e., the FLR had been correctly plugged into the ballast).” EX1009, ¶¶[0082]; EX1002, ¶110.

2. Rationale to Combine the Ivey Combination with Sadwick

First, Sadwick evidences that a POSITA would have found it “obvious to try” modifying the Ivey Combination such that Ivey345’s Z test load 140 is configured in series with the LEDs, thereby eliminating the need for test load switch 135, as load switch 175 would have been used instead to periodically permit current to flow from rectifier 120 through the Z test load 140 to be detected by detector 150.

Sadwick, like the Ivey Combination, is directed to a fluorescent-replacing LED-based light tube that may be mains line powered. EX1002, ¶112. *Compare* EX1009, ¶¶[0004], [0173], *with* EX1007, 2:11-13, 2:51-56, *and* Section VI.A.4. Sadwick’s FLR utilizes “hazard protection circuitry” that, like Ivey345’s “current limiting circuit” in the Ivey Combination, protects against the fault configuration also identified in Ivey345—that a user may be electrically shocked during relamping if the user makes contact with an “exposed pin” on one end of the FLR while the other is connected. EX1002, ¶112. *Compare* EX1009, ¶¶[0082], [0071], Fig. 8, *with* EX1008, ¶¶[0010], [0005], *and* Section VI.A.4. And Sadwick’s hazard protection circuitry does so by utilizing the same core circuit components configured in a nearly identical layout as Ivey345’s current limiting circuit. EX1002, ¶112.

Specifically, in both Sadwick’s and Ivey345’s protection circuits, current

periodically flows⁸ from a line-powered LED-based light tube's rectifier⁹ through a test resistor.¹⁰ The voltage across the test resistor represents the current exiting the rectifier, which varies depending on whether a fault configuration exists.¹¹ To detect such a fault configuration, the test resistor's voltage is fed into the non-inverting input of a comparator.¹² At the same time, a reference voltage is fed into the comparator's inverting input.¹³ The comparator then compares the voltages such that when the test resistor's voltage is respectively lower/higher than the reference

⁸ Compare EX1009, ¶[0082] with EX1008, ¶[0021]. EX1002, ¶113 n.3.

⁹ Compare EX1009, ¶[0080] (discussing an “input rectification stage”), with EX1007, 5:36-39 (discussing “a rectifier circuit”), EX1008, ¶¶[0015]-[0016] (discussing “rectifier 120”), and Section VI.A.4. EX1002, ¶113 n.4.

¹⁰ Compare EX1009, ¶[0080] (“sense resistor 1450”), with EX1008, ¶¶[0023]-[0027] (“Z test load 140”); EX1002, ¶113 n.5.

¹¹ Compare EX1009, ¶¶[0080], [0082], with EX1008, ¶¶[0010], [0024]-[0027]. EX1002, ¶113 n.6.

¹² Compare EX1009, ¶[0080] (“comparator 1434”), with EX1008, ¶¶[0024]-[0029] (“comparator 170”), Fig. 3. EX1002, ¶113 n.7.

¹³ Compare EX1009, ¶[0080] (“reference set point signal”), with EX1008, ¶¶[0030]-[0032] (“detection threshold signal”), Fig. 3. EX1002, ¶113 n.8.

voltage, a fault configuration is/is not detected by the comparator, which in response outputs a signal to open/close a transistor in series with the rectifier and LEDs.¹⁴ Further, the detection of a fault configuration may also cause this transistor to be latched open until power is cycled.¹⁵

The main difference between the two is the placement of each's test resistor. EX1002, ¶114. Specifically, Sadwick's hazard protection circuit configures its test resistor (sense resistor 1450) "in series with" the LEDs, thereby allowing a single transistor 1430 (also "in series with" the LEDs) to be used for both (1) permitting current to flow periodically from the rectifier through sense resistor 1450 to determine whether a fault configuration exists, and (2) respectively disabling/maintaining current flow through the LEDs when the fault configuration is/is not detected. EX1009, ¶¶[0080], [0082]; EX1002, ¶114. By contrast,

¹⁴ Compare EX1009, ¶¶[0080], [0082], with EX1008, ¶¶[0030]-[0032], [0010]. EX1002, ¶113 n.9.

¹⁵ Compare EX1009, ¶[0082] (transistor 1430 may be "complete[ly] turn[ed]-off (i.e., latch[ed] off) until power is cycled (i.e., turned off and then turned back on)"), with EX1008, ¶[0044] ("main load shut-off latch 315 will be triggered and produce an output that will prevent both present and future activation of the load switch 175" until "power is removed from the circuit and reapplied"). EX1002, ¶113 n.10.

Ivey345's current limiting circuit in the Ivey Combination configures its test resistor (Z test load 140) in parallel to main load 180 (LEDs), thereby requiring the use of two separate switches for controlling current flow in accordance with the above: (1) test load switch 135 (also parallel to the LEDs) permits current to flow periodically from rectifier 120 through Z test load 140, while (2) load switch 175 (in series with the LEDs) disables/maintains current flow through the LEDs. EX1008, ¶¶[0021]-[0024], [0010], [0041]-[0045], Fig. 3; Section VI.A.4, EX1002, ¶114. But the above illustrates the two and only two fundamental configurations that such a test resistor can be placed in relation to the LEDs: series or parallel. EX1002, ¶114. Indeed, that circuit components are configured either in series or parallel with one another is a core and known concept in electronics. EX1022; EX1002, ¶114.

Accordingly, Sadwick and Ivey345 together identify a finite number of predictable solutions to choose from (i.e., two protection circuit layouts utilizing a test resistor configured either in series or parallel with the LEDs) to solve the same problem in line-powered LED-based light tubes with a reasonable expectation of success (i.e., to protect a user from being shocked during relamping when accidentally touching an exposed pin), and a POSITA would have therefore found it "obvious to try" modifying Ivey345's current limiting circuit in the Ivey Combination to be in accordance with Sadwick's hazard protection circuitry (i.e., to configure Z test load 140 in series with the LEDs and to eliminate test load switch

135, as load switch 175 would be used instead for controlling current flow from rectifier 120 through Z test load 140 and the LEDs in accordance with the above). *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007); EX1009, ¶¶[0080], [0082]; EX1008, ¶¶[0021]-[0024], [0010], [0035]-[0036], [0045]; EX1002, ¶115.

Second, as explained above, Sadwick’s resistor-in-series protection circuit explicitly addresses the same problem addressed in Ivey345—a user accidentally being shocked during relamping (EX1009, ¶¶[0082], [0071]; EX1008, ¶¶[0010], [0005])—and a resistor-in-series configuration was therefore a known, suitable, and thus obvious, technique for addressing that problem. *See Intel Corp. v. PACT XPP Schweiz AG*, No. 2022-1037, 2023 WL 2469631, at *5 (Fed. Cir. Mar. 13, 2023) (“That [a first reference] and [a second reference] address the same problem and that [the second reference presents] a known way to address that problem is precisely the reason that there’s a motivation to combine [the first and second references] under *KSR* and our precedent.”); EX1002, ¶116. Given the application of Sadwick’s resistor-in-series technique to Ivey345’s protection circuit was not beyond a POSITA’s skill (*see, e.g.*, EX1009, ¶¶[0080], [0082]), this alone provides a sufficient motivation to combine the Ivey Combination with Sadwick. *Intel*, 2023 WL 2469631, at *4-5; EX1002, ¶116.

A POSITA would have also been motivated to combine the Ivey Combination with Sadwick because doing so would have (third) simplified Ivey345’s current

limiting circuit and, independently, would have (fourth) improved performance. EX1002, ¶117. As a POSITA would have recognized, modifying Ivey345's current limiting circuit in accordance with Sadwick would have allowed a switch to be deleted—specifically test load switch 135—because load switch 175 would have been used instead to control current flow through Z test load 140 and the LEDs as discussed above. *See* EX1008, ¶¶[0021]-[0024], [0010], [0035]-[0036], [0045]; EX1009, ¶¶[0080], [0082]; EX1002, ¶117.

And with test load switch 135 deleted, so too could Ivey345's "power-up reset 160." *See* EX1008, ¶¶[0033]-[0034], Fig. 3; EX1002, ¶118. That power-up reset 160, "[w]hen power is first applied to the current limiting circuit 100,... turn[s] off main load switch 175... [and] maintains this state until a stable condition is reached and a determination can be made whether a subject is present in the circuit." EX1008, ¶[0034]; EX1002, ¶118. In other words, power-up reset 160 ensures that load switch 175 remains off until the signal from detector 150, driven by test load switch 135 (*see* EX1008, ¶[0024]), permits detection of a human in the circuit (*id.*, ¶[0034]). EX1002, ¶118. But with one transistor in the Ivey-Sadwick combination—load switch 175—for performing both the load-control and human-detection functions, there would have been no need for power-up reset 160 to control a non-existent additional transistor. *Id.*

Further, the above modification would have also allowed a resistor to be

deleted. EX1002, ¶119. Specifically, although the above modification would have resulted in Z test load 140—which is simply “a resistor” (EX1008, Fig. 3, ¶[0080])—being configured in series with the LEDs rather than parallel (*see* EX1009, ¶¶[0080], [0082]), such a modification would not have required placing an additional resistor in series with the LEDs, because a resistor in series with the LEDs would have already existed. EX1002, ¶119. As generally known, LEDs must have what is known as a “current limiting resistor” placed in series, because LEDs will otherwise burn out if directly connected to a power source. EX1015; EX1020, ¶[0011]; EX1002, ¶119. Given that such a current limiting resistor would have thus already existed in series with the LEDs in Ivey345’s current limiting circuit, a POSITA would have recognized to use such a preexisting resistor as—and for carrying out the functions of—Z test load 140 when making the above modification, rather than adding a superfluous resistor in series with the LEDs for serving this same purpose. EX1002, ¶119; *see also* EX1016,¹⁶ 3 (demonstrating that current through an LED can be determined by measuring voltage across the LED’s current limiting resistor, which has a known resistance); EX1020, ¶[0035] (same).

Independently, the above modification would have improved performance.

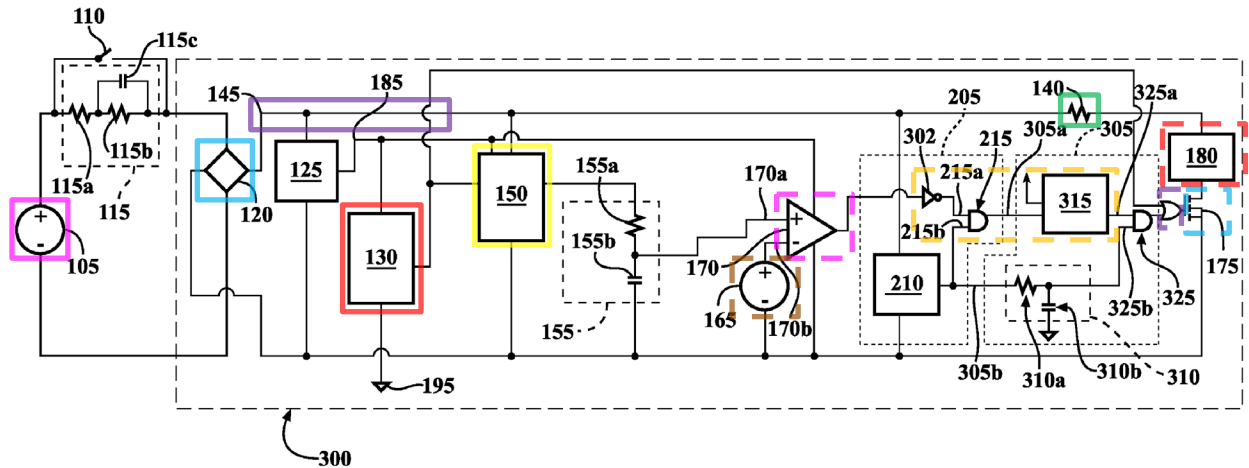
¹⁶ *See* EX1038, ¶¶36-44 (establishing public availability on or shortly after April 30, 2014).

EX1002, ¶120. Specifically, a POSITA would have recognized that, unlike in the parallel configuration, configuring Z test load 140 in series with the LEDs would have caused the current flowing through Z test load 140 to exactly equal the current flowing from rectifier 120 through the LEDs and thus more accurately represent whether a subject is present in the circuit. *See* EX1017, 3:36-44 (“[T]here are uncertainties within the forward voltages of the LEDs, which in turn creates uncertainty with respect to the current level flowing through the LEDs. To manage these uncertainties, the current flowing through the LEDs is measured by determining a voltage level across a known resistor and calculating the current level.”), 3:51-55 (“As shown, the circuit of FIG. 1 comprises a plurality of LEDs coupled in series with a channel control transistor and a current sense circuit between a supply voltage V_{DD} and a reference ground.” (diagram numbering omitted)); EX1002, ¶120. Such a modification would have thus increased the current limiting circuit’s detection accuracy of a fault configuration and therefore improved performance, motivating a POSITA to perform the modification. EX1002, ¶120.

3. The Resulting “Ivey-Sadwick Combination”

So modified, Ivey345’s current limiting circuit in the Ivey Combination (*see* Section VI.A.4) is modified to be in accordance with Sadwick (the “Ivey-Sadwick Combination”) such that Z test load 140 is configured “in series with” rectifier 120 and the LEDs (*see* EX1009, ¶[0080]; EX1008, ¶¶[0023]-[0024]). EX1002, ¶121.

Ivey345's Figure 3, modified below, illustrates the Ivey-Sadwick Combination:



EX1008, Fig. 3 (modified, annotated); EX1002, ¶121. As shown, test load switch 135 is eliminated, as load switch 175 (dotted-blue) instead performs test load switch 135's function of periodically permitting current to flow from rectifier 120 (solid-blue) and device power rail 145 (solid-purple) through Z test load 140 (solid-green), in addition to load switch 175's original function of respectively disabling/maintaining current flow through main load 180 (LEDs) (dotted-red) when a fault configuration is/is not detected. See EX1009, ¶¶[0080], [0082]; EX1008, ¶¶[0021]-[0024], [0010], [0035]-[0037], [0045]; EX1002, ¶121. As such, the output of oscillator 130 (solid-red) is connected to and controls load switch 175 rather than test load switch 135. See EX1009, ¶¶[0080], [0082]; EX1008, ¶¶[0021]-[0024], [0010], [0035]-[0036], [0045]; EX1002, ¶121. Likewise, power-up reset 160 is also eliminated. See EX1008, ¶¶[0033]-[0034]; EX1002, ¶121.

The current limiting circuit's remaining operations are unchanged. EX1002,

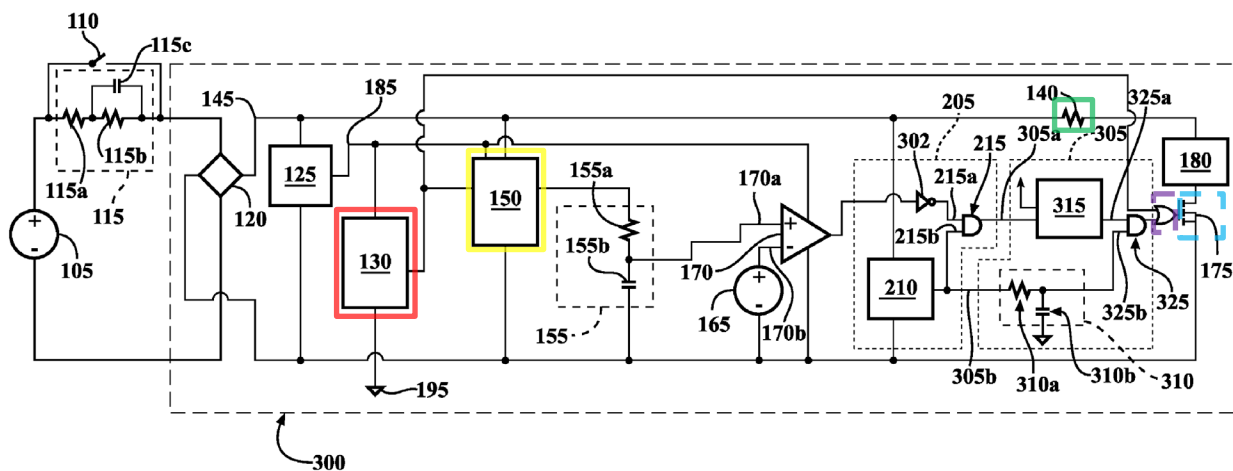
¶122. Specifically, detector 150 (solid-yellow) synchronously detects a variation across device power rail 145, and comparator 170 (dotted-pink) compares detector 150's detection result to detector threshold signal source 165's (dotted-brown) signal to detect whether a fault configuration exists. *See* EX1009, ¶¶[0080], [0082]; EX1008, ¶¶[0023]-[0032], [0034]-[0035], [0010]; EX1002, ¶122. Respectively, if a fault configuration is/is not detected, comparator 170 outputs a “low”/”high” signal to logic inverter 302 and latch 315 (together in dotted-orange), and latch 315 in response outputs a “low”/”high” signal to load switch 175 to disable/maintain current flow through the LEDs. *See* EX1009, ¶¶[0080], [0082]; EX1008, ¶¶[0034]-[0035], [0010], [0044]-[0046]; EX1002, ¶122.

Load switch 175 therefore closes when latch 315's output is high, oscillator 130's output is high, or both, and opens otherwise. EX1008, ¶¶[0035]-[0036], [0045]-[0046], [0020]-[0022], [0024], [0010]; EX1009, ¶[0082]; EX1002, ¶123. To enable such logical control of load switch 315, a POSITA would have recognized that the standard practice would have been to place a logical OR gate (dotted-purple) at the load switch 175's gate for receiving both latch 315's output and oscillator 130's output.¹⁷ *See* EX1023; EX1002, ¶123; *see also* EX1009, ¶[0212]; EX1008,

¹⁷ Should Patent Owner argue that placing this OR gate negates the circuit layout simplification benefits discussed in Section VI.B.2, a POSITA would have

See Sections VI.A.5(b), VI.B.3.

See Section VI.A.5(c). Differently here, the output of oscillator 130 (solid-red) is fed into an OR gate (dotted-purple) at the gate of load switch 175 (dotted-blue), which therefore opens and closes at least when oscillator 130's clock signal oscillates low and high, respectively:



- 57 -

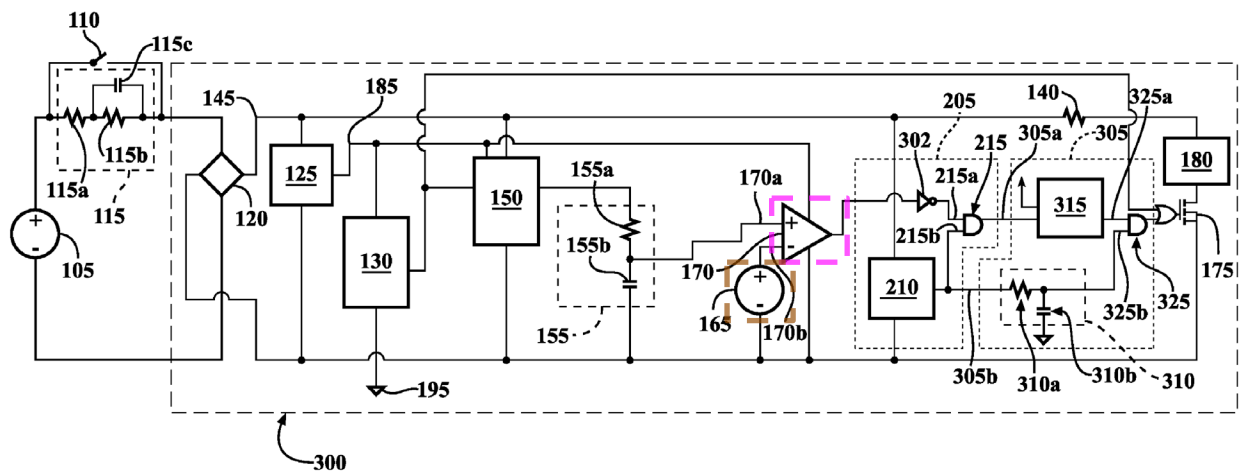
Further, in the Ivey-Sadwick Combination, Z test load 140 (solid-green) is instead configured in series with device power rail 145 and the LEDs. EX1008, ¶[0023]; EX1009, ¶[0080]; Section VI.B.3; EX1002, ¶128. Thus, when load switch 175 is closed by oscillator 130's high output accordingly, current flows through Z test load 140. EX1008, ¶¶[0020]-[0024], [0035]-[0036], [0045]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶128. Detector 150 (solid-yellow), which also receives oscillator 130's output and thus operates synchronously with load switch 175's activation, detects a variation across device power rail 145, which is used to detect whether a fault configuration exists. EX1008, ¶¶[0024], [0026]-[0027], [0010], [0035]-[0036], [0045]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶128.

(d) Limitation [1c]

See Section VI.A.5(d). Differently here, because test load switch 135 is deleted, load switch 175 alone forms the claimed "switch circuit." Section VI.B.3; EX1002, ¶129. Load switch 175 receives oscillator 130's output via the OR gate ("coupled to the pulse generating circuit"), causing load switch 175 to open and close at least when oscillator 130's output oscillates low and high, respectively. EX1008, ¶¶[0020]-[0024], [0035]-[0036], [0045]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶129.

(e) Limitation [1d]

See Section VI.A.5(e). Here, although Z test load 140 is configured in series with device power rail 145 and the LEDs, the discussed functions of detector 150, comparator 170 (dotted-pink), and detection threshold signal source 165 (dotted-brown) remain unchanged—in a fault configuration, detector 150 detects an increased variation across device power rail 145 and outputs a “decrease[d]” signal to comparator 170, which determines that detector 150’s output is lower than detection threshold signal source 165’s signal and, in response, outputs a “low” signal to ultimately cause load switch 175 to “remain[] off”:



EX1008, Fig. 3 (modified, annotated), ¶¶[0024]-[0026], [0010], [0018]-[0032], [0044]-[0045]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶130. Differently here, however, load switch 175 also receives oscillator 130's clock signal via the OR gate. Section VI.B.3; EX1002, ¶130. Thus, when comparator 170 outputs a "low" signal as discussed, and when oscillator 130's clock signal thereafter

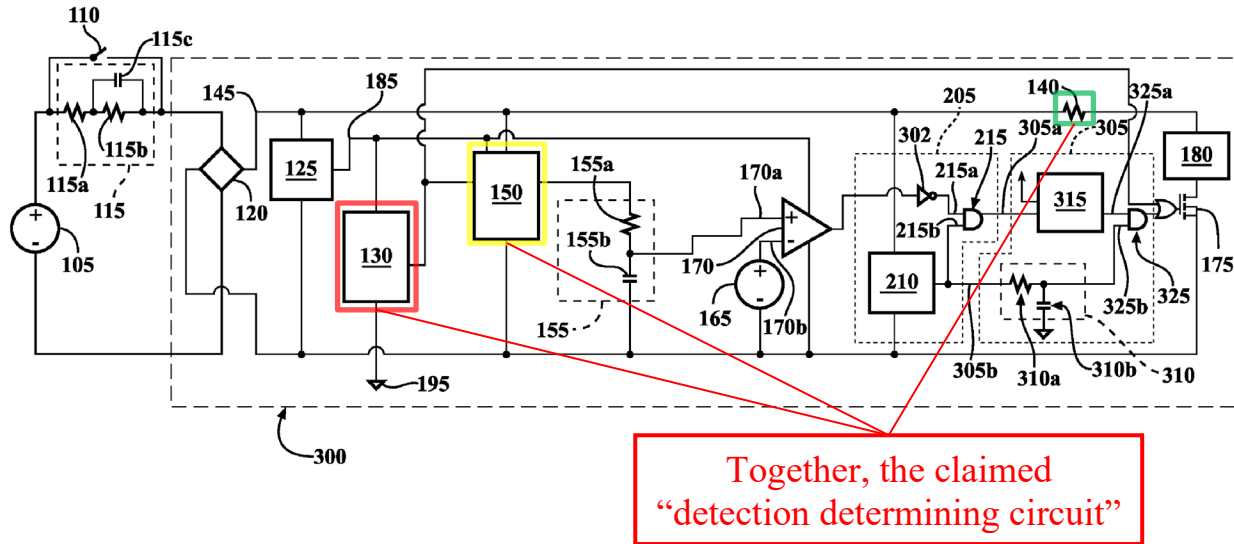
oscillates low, load switch 175 is opened, causing device power rail 145 overall to remain open. EX1008, ¶¶[0020]-[0022], [0024]-[0026], [0010], [0018]-[0032], [0044]-[0045]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶130.

(f) Limitation [1e]

By contrast, in a normal configuration, detector 150 detects a decreased variation across device power rail 145 and outputs an “increase[d]” signal to comparator 170, ultimately powering on load switch 175. EX1008, ¶¶[0024]-[0026], [0028]-[0032], [0010], [0044]-[0045]; EX1009, ¶¶[0080], [0082]; EX1002, ¶131. . EX1008, ¶¶[0030]-[0032], [0041], , [0010]; EX1009, ¶¶[0080], [0082]; Sections VI.B.3, VI.A.5(f); EX1002, ¶131.

(g) Limitation [1f]

As similarly discussed in Section VI.A.5(g), detector 150, comparator 170, and Z test load 140 altogether form the claimed “detection determining circuit.” EX1002, ¶132. *Compare* EX1008, Fig. 3 (modified, annotated below), *and* EX1009, Fig. 14, ¶¶[0080], [0082], *and* Section VI.B.3, *with, e.g.*, EX1001, Fig. 15K, 49:63-50:47.



Detector 150 detects a variation across device power rail 145 and outputs a corresponding signal to comparator 170, which compares this signal to the threshold signal to detect whether a fault configuration exists. EX1008, ¶¶[0024]-[0032], [0010]; EX1009, ¶¶[0080], [0082]; Sections VI.B.3, VI.A.5(g); EX1002, ¶132.

Lastly, load switch 175 and Z test load 140 are in series with device power rail 145 and the LEDs (“the power loop includes the switch circuit and the detection determining circuit”). EX1008, ¶¶[0021]-[0027], [0010], [0035]-[0036]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶133.

(h) Limitation [1g]

See Sections VI.A.5(h), VI.B.3.

(i) Limitations [3a]-[3b]

See Sections VI.A.5(i)-VI.A.5(j), VI.B.3.

(j) Limitation [4pre]

To the extent claim 4’s preamble is limiting, the Ivey-Sadwick Combination

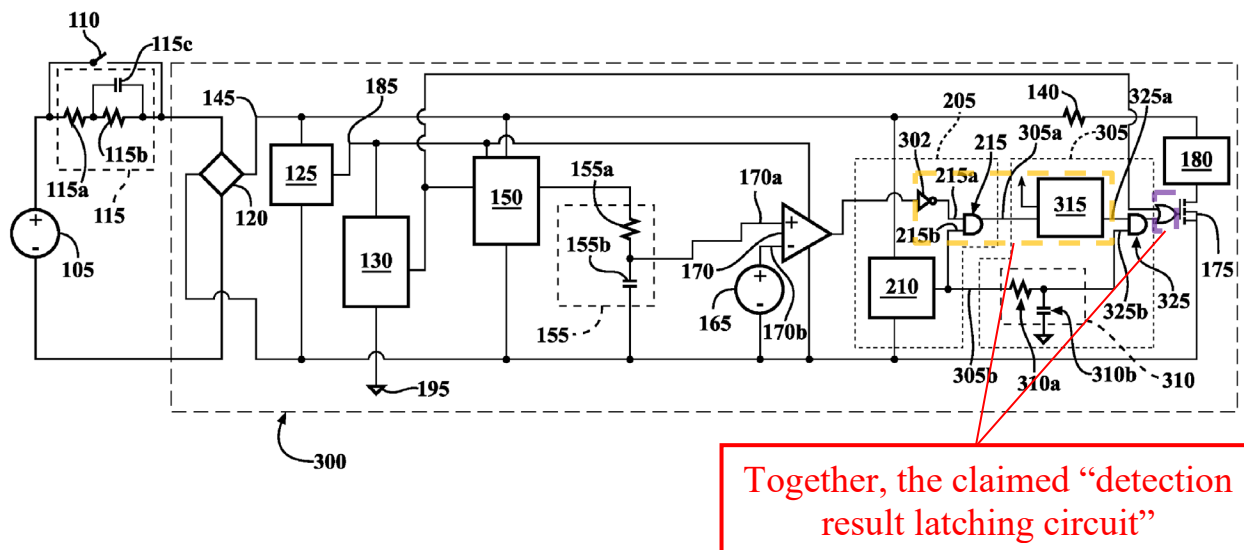
meets it. *See* Sections VI.B.4(a), VI.B.4(k)-VI.B.4(l).

(k) Limitations [4a]-[4f]

See Sections VI.B.4(c)-VI.B.4(g).

(l) Limitation [4g]

The OR gate along with logic inverter 302 and latch 315 (together in dotted-orange) meets the claimed “detection result latching circuit” under both the term’s plain and ordinary meaning and the *CH* Court’s construction (*see* EX1026, 6; Section V.C.3):



EX1008, Fig. 3 (modified, annotated); EX1002, ¶138. Specifically, the OR gate receives oscillator 130’s clock signal, causing load switch 175 to close at least when oscillator 130’s clock signal oscillates high (“detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit,” and the *CH* Court’s construction of “outputs a high logic value

when either... *the pulse signal output terminal*... has a high logic value”). Section VI.B.3; EX1026, 6; EX1002, ¶138. The OR gate also receives latch 315’s output, which as explained in Section VI.A.5(m) is latched either “high” or “low” to turn on or off load switch 175, respectively, depending on the inverted comparator output (“control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit,” and the *CH* Court’s construction of “*stores the detected result* and outputs a high logic value when either *the stored detected result*... has a high logic value”). EX1008, ¶¶[0043]-[0046], [0030]-[0032]; EX1026, 6; EX1002, ¶138.

(m) Limitation [21pre]

To the extent claim 21’s preamble is limiting, the Ivey-Sadwick Combination meets it. *See* Sections VI.B.4(a), VI.B.4(n)-VI.B.4(s).

(n) Limitation [21a]

See Sections VI.A.5(o), VI.B.3.

(o) Limitation [21b]

See Sections VI.A.5(p), VI.B.4(g).

(p) Limitation [21c]

See Sections VI.B.4(o), VI.B.4(d).

(q) Limitations [21d]-[21e]

See Sections VI.B.4(e)-VI.B.4(f).

(r) Limitation [21f]

See Sections VI.B.4(p), VI.B.4(g).

(s) Limitation [21g]

See Section VI.A.5(u). For the same discussed reasons, a POSITA would have recognized that, in the Ivey-Sadwick Combination, Ivey345's current limiting circuit as modified by Sadwick (*see* Section VI.B.3) would have been between power converter 36's rectifier circuit and current regulator circuit, the latter including the claimed "filtering circuit." *See* EX1007, 5:33-39; EX1008, ¶¶[0012], [0015]-[0016]; Section VI.A.5(u); EX1002, ¶145. As further evidence, Sadwick itself teaches that, when utilizing its series configuration, "[o]ther circuitry 914 can be included to perform other desired functions such as... constant current regulation...." EX1009, ¶[0073]; EX1002, ¶145. Sadwick illustrates these teachings in Figures 9-13, which show that such "[o]ther circuitry" are always placed downstream, and not before, its hazard protection circuitry:

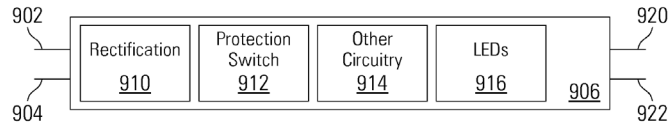


FIG. 9

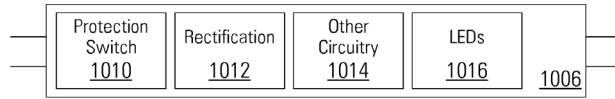


FIG. 10

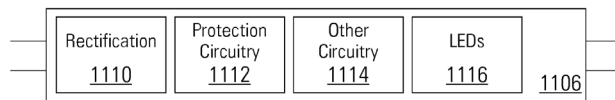


FIG. 11

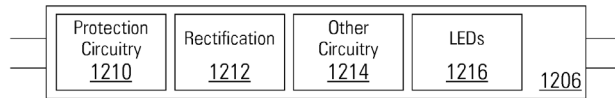


FIG. 12

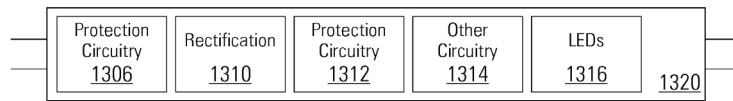


FIG. 13

EX1009, Figs. 9-13, ¶¶[0072]-[0078]; EX1002, ¶145.

(t) Limitations [22a]-[22b]

See Sections VI.A.5(v), VI.B.4(g).

(u) Claim 23

See Sections VI.B.4(o), VI.B.4(l).

(v) Limitation [24pre]

To the extent claim 24's preamble is limiting, the Ivey-Sadwick Combination

meets it by utilizing, within “power converter 36” of Ivey813’s “LED-based light tube,” Ivey345’s “current limiting circuit,” as modified in accordance with Sadwick, to detect during relamping whether a subject user is making contact with the tube’s return terminal while the tube’s power terminal is connected to “fixture 11” (Ivey345’s “power source 105”) and, if such occurs, to “maintain[] the current flowing through the subject at a low and safe level.” EX1007, 2:50-54, 5:33-35; EX1008, ¶¶[0010], [0004]-[0005]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶148; *see also* Sections VI.B.4(w)-VI.B.4(z).

(w) Limitation [24a]

See Sections VI.A.5(y), VI.B.3.

(x) Limitation [24b]

See Section VI.B.4(g). Detector 150, comparator 170, and Z test load 140 together form a “detection determining circuit” that performs the claimed “detecting.” EX1002, ¶150.

(y) Limitation [24c]

As discussed in Section VI.B.4(l), the OR gate, logic inverter 302, and latch 315 together meet the claimed “detection result latching circuit” under both the term’s plain and ordinary meaning and the *CH* Court’s construction. *See* EX1026, 6; Section V.C.3; EX1002, ¶151. Specifically, the OR gate outputs (and thus load switch 175 receives) a high signal when oscillator 130’s clock signal oscillates high (“receiving the one or more pulse signals through a detection result latching circuit

by a switch circuit” under either construction of “detection result latching circuit”) or latch 315’s output is latched high. EX1008, ¶¶[0030]-[0032], [0043]-[0046]; EX1009, ¶¶[0080], [0082]; Section VI.B.4(l); EX1002, ¶151. Further, such operation determines whether current may flow from device power rail 145 through load switch 175, which is in series with device power rail 145 and the LEDs (“switch circuit is on the power loop”). EX1008, ¶¶[0010], [0035]-[0036], [0045]; EX1009, ¶¶[0080], [0082]; Sections VI.B.4(g), VI.B.4(l); EX1002, ¶151.

(z) Limitation [24d]

See Section VI.A.5(bb). Differently here, test load switch 135 is eliminated, and oscillator 130’s output is connected to load switch 175 via an OR gate. Section VI.B.3; EX1002, ¶152. Thus, when comparator 170 outputs a low signal and oscillator 130 thereafter oscillates low as discussed, load switch 175 opens, opening device power rail 145. EX1008, ¶¶[0020]-[0022], [0024], [0030]-[0032], [0010], [0044]-[0045]; EX1009, ¶¶[0080], [0082]; Section VI.B.3; EX1002, ¶152.

(aa) Limitations [25a]-[25c]

See Sections VI.A.5(cc), VI.B.3.

(bb) Claim 26

See Sections VI.A.5(dd), VI.B.3.

(cc) Limitations [27a]-[27c]

See Sections VI.A.5(ee), VI.B.3.

(dd) Claim 28

See Sections VI.A.5(ff), VI.B.3.

(ee) Limitations [30a]-[30b]

See Section VI.B.4(i).

(ff) Claim 31

See Section VI.B.4(l).

(gg) Claim 35

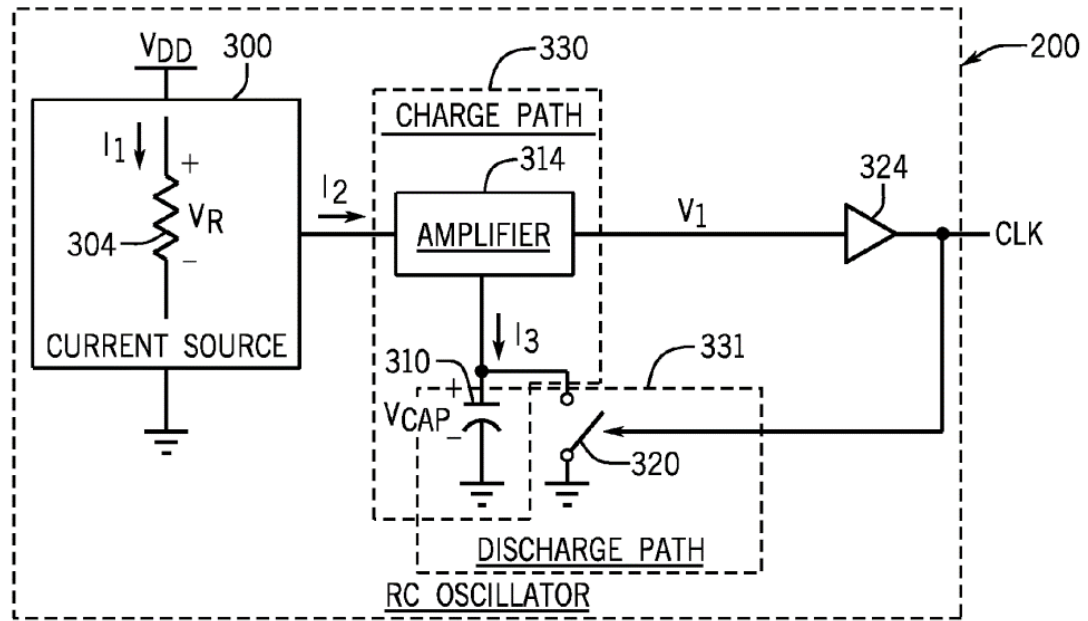
See Section VI.B.4(gg), VI.B.3.

C. Grounds 3-4: Ivey⁸¹³, Ivey³⁴⁵, and Powell—and Optionally Sadwick—Render Obvious Claims 1, 4-5, and 32

1. Powell

Powell is directed to “using a current source to provide a charging current to a capacitor of a resistor-capacitor (RC) tank of an RC oscillator.” EX1010, 1:18-22; EX1002, ¶160. Powell’s Figure 3 provides an example of such an “RC oscillator 200”:

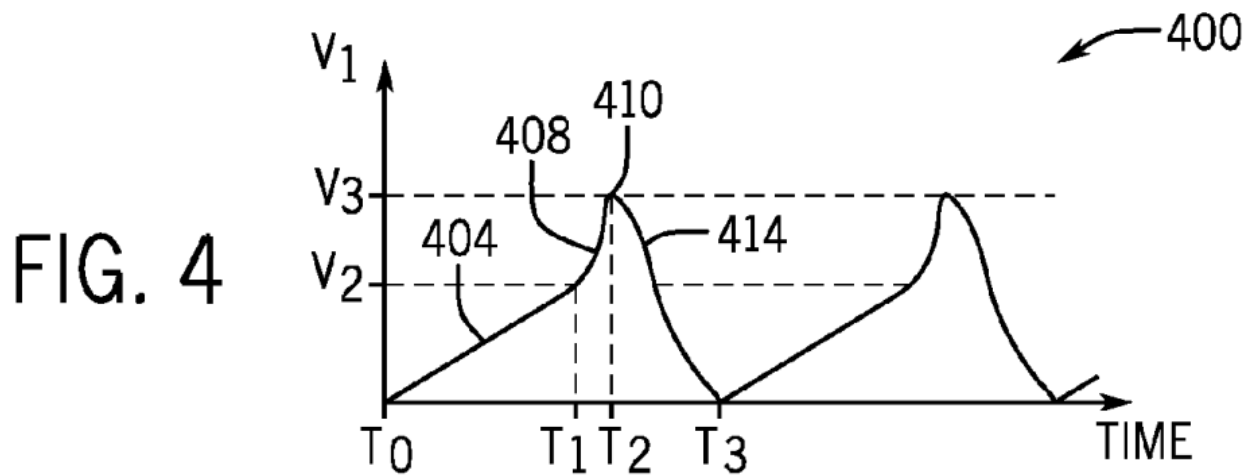
FIG. 3



EX1010, Fig. 3; EX1002, ¶160. As shown, the RC oscillator is powered by a standard “ V_{DD} supply voltage” and includes “current source 300.” EX1010, 7:23-35, 4:62-64; EX1002, ¶160. During a “charging part” of the RC oscillator’s “oscillation cycle,” current source 300 outputs constant current “ I_2 ,” which produces charging current “ I_3 ” within “charge path 330.” EX1010, 5:1-6; EX1002, ¶160. Further, “switch 320 does not conduct,” causing “capacitor 310” to charge and thus its voltage “ V_{CAP} ” to increase. EX1010, 5:9-12, 5:23-29; EX1002, ¶160. V_{CAP} is amplified by “amplifier 314” to produce a voltage “ V_1 ,” which is received by “digital buffer 324 that pulse shapes the V_1 voltage (i.e., sharpens the rising and falling edges of the V_1 voltage) to provide the CLK signal at the output of the buffer 324.” EX1010, 5:13-22, 6:1-5; EX1002, ¶160.

As capacitor 310 charges, “the V_1 voltage eventually reaches a voltage, which

causes the switch 320 to conduct, or turn on, and consequently begin [a] discharging part of the cycle in which the capacitor 310 is discharged through the switch [320] to ground.” EX1010, 5:29-34; EX1002, ¶161. Switch 320 thus forms “discharge path 331.” EX1010, 5:23-25; EX1002, ¶161. “The discharging of the capacitor 310, in turn, causes the V_1 and V_{CAP} voltages to decrease; and the lowered V_1 voltage causes the switch 320 to turn off, thereby ending the [dis]charging part of the current cycle and beginning the charging part of the next cycle.” EX1010, 5:34-39; EX1002, ¶161. Powell’s Figure 4 illustrates V_1 ’s oscillating waveform from charging (T_0 to T_2) and discharging (T_2 to T_3) capacitor 310:



EX1010, Fig. 4, 6:34-38; EX1002, ¶161.

Lastly, current source 300 includes “resistor 304,” which together with capacitor 310 form the RC oscillator’s “RC tank” that “establishes the resonance frequency for the oscillator.” EX1010, 4:62-64, 2:34-40; EX1002, ¶162. “Resistor 304 also establish[es] the current that is provided by the current source [300].”

EX1010, 2:53-58; EX1002, ¶162. Configuring resistor 304 to perform such “dual functions” allows “die area [to be] preserved (i.e., one less resistor is used),” and “current (and therefore power consumption) may be reduced....” EX1010, 2:53-58, 6:19-24; EX1002, ¶162.

2. *Rationale to Combine the Ivey and Ivey-Sadwick Combinations with Powell*

Regarding Ivey345’s current limiting circuit in the Ivey (*see* Section VI.A.4) and Ivey-Sadwick (*see* Section VI.B.3) Combinations, Ivey345 states that oscillator 130 may be, e.g., a “relaxation-type oscillator”; is auxiliary-powered by, e.g., standard 5V power; and outputs an oscillating signal (*see* EX1008, ¶¶[0019]-[0020], [0017]). EX1002, ¶163. But Ivey345 provides no specific layout for oscillator 130 and instead specifies oscillator 130 (solid-red) as an empty box:

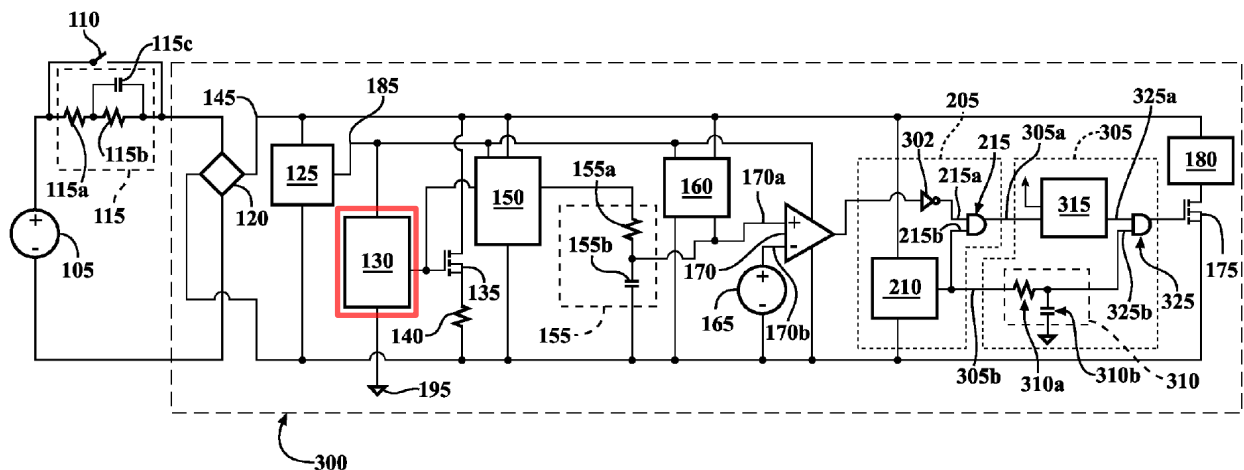


FIG. 3

EX1008, Fig. 3 (annotated); EX1002, ¶163. Such a generic description for oscillator 130 thus teaches no more than using any known oscillator capable of performing

oscillator 130's functions of outputting an oscillating signal that opens and closes test load switch 135 and, indirectly, load switch 175 in the Ivey Combination (*see* Sections VI.A.4, VI.A.5(m); EX1008, ¶¶[0020]-[0022], [0024]), or simply load switch 175 in the Ivey-Sadwick Combination (*see* Section VI.B.3; EX1008, ¶¶[0010], [0035]-[0036], [0045]; EX1009, ¶[0082]). EX1002, ¶163.

Powell's RC oscillator is such a known oscillator, as it is a "relaxation-type oscillator" as listed in Ivey345 (i.e., its output depends on charging and discharging a capacitor) (EX1010, 4:65-67; *see also* EX1024), is powered by a standard supply voltage V_{DD} (EX1010, 7:23-35), and outputs an oscillating signal V_1 (*id.*, 4:65-5:39, 6:34-38, Fig. 4). EX1002, ¶164. Thus, Ivey345 teaches using an RC oscillator like Powell's as Ivey345's oscillator 130 within the Ivey and Ivey-Sadwick Combinations. EX1002, ¶164. Further, a POSITA would have been otherwise motivated to use Powell's RC oscillator accordingly, because Powell's RC oscillator likewise generates an oscillating clock signal while providing numerous advantages, including reduced die area and power consumption. EX1010, 6:19-21; EX1002, ¶164.

3. The Resulting "Ivey-Powell" and "Ivey-Sadwick-Powell Combinations"

So modified, Powell's RC oscillator is used as oscillator 130 in Ivey345's current limiting circuit within the Ivey Combination (*see* Section VI.A.4; EX1008, ¶¶[0020]-[0022], [0024]) (the "Ivey-Powell Combination") and the Ivey-Sadwick

Combination (*see* Section VI.B.3; EX1008, ¶¶[0010], [0035]-[0036], [0045]; EX1009, ¶[0082]) (the “Ivey-Sadwick-Powell Combination”). Specifically, Powell’s RC oscillator is auxiliary-powered—it receives its “V_{DD} supply voltage” from Ivey345’s “auxiliary power supply 125” (*see* EX1010, 7:23-35; EX1008, ¶¶[0016], [0019])—and outputs an oscillating signal (V₁) to control the same circuit elements as oscillator 130 (EX1008, ¶[0019]-[0022], [0024], [0027], [0043]; EX1010, 4:65-5:39, 6:34-38, Fig. 4). EX1002, ¶165.

4. Element-by-Element Analysis

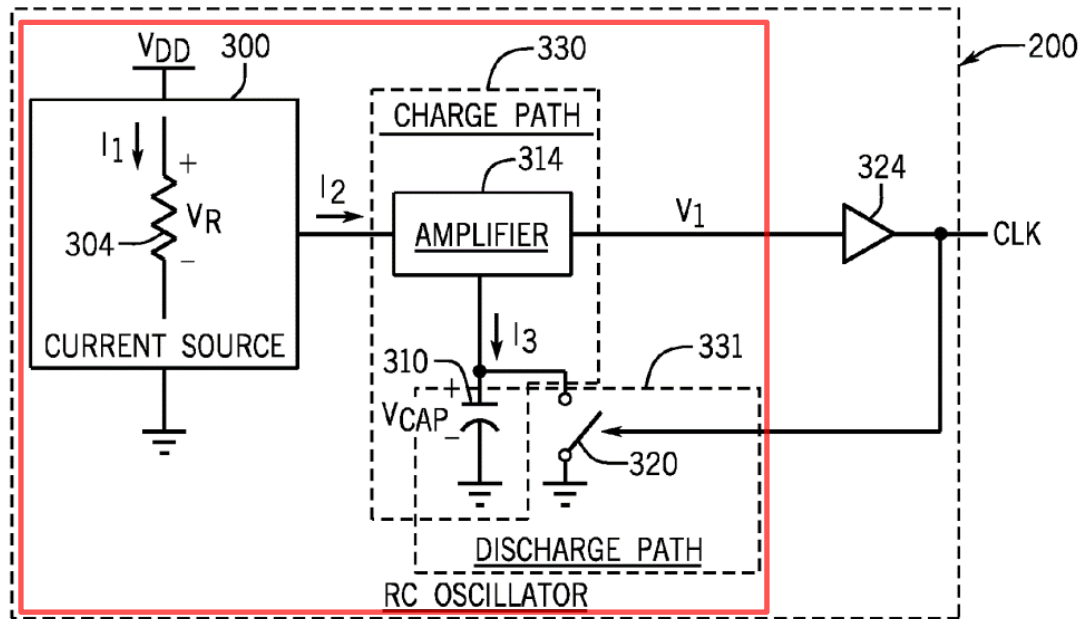
(a) Limitation [1pre]

See Sections VI.A.5(a), VI.B.4(a), VI.C.3; *see also* Sections VI.C.4(b)-VI.C.4(d).

(b) Limitation [1a]

See Sections VI.A.5(b), VI.B.4(b). Differently here, Powell’s “RC oscillator” is used as oscillator 130 in Ivey345’s current limiting circuit, which likewise outputs an oscillating signal V₁ (“a pulse generating circuit configured to output one or more pulse signals”). EX1010, 4:65-5:39, 6:34-38, Fig. 4; EX1008, ¶[0019]; EX1009, ¶[0082]; Section VI.C.3; EX1002, ¶167. Excluding “digital buffer 324,” each of the other elements in the RC Oscillator—“current source 300,” “capacitor 310,” “charge path 330,” and “discharge path 331” (together in solid-red)—form the claimed “pulse generating circuit”:

FIG. 3



EX1010, 4:65-5:39, Fig. 3 (annotated); EX1002, ¶167; *see also* EX1001, 49:1-10, Fig. 15H.

(c) Limitations [1b]-[1f]

See Sections VI.A.5(c)-VI.A.5(g), VI.B.4(c)-VI.B.4(g), VI.C.3.

(d) Limitation [1g]

See Sections VI.A.5(h), VI.B.4(h). Consistent with such discussion, Powell’s current source 300, capacitor 310, charge path 330, and discharge path 331 together receive only two inputs—a power input V_{DD} supply voltage input from auxiliary power supply 125, and a “CLK clock signal” from buffer 324—neither of which are controlled or affected by the current limiting circuit’s downstream components and operation. EX1010, 7:23-35, 6:1-5; EX1008, ¶¶[0016], [0019]; Section VI.C.3; EX1002, ¶169. Thus, such components operate independent of the current limiting

circuit's downstream operations. EX1002, ¶169; Section VI.C.3.

(e) Limitation [4pre]

See Sections VI.A.5(k), VI.B.4(j), VI.C.3, VI.C.4(f)-VI.C.4(h),

(f) Limitation [4a]

See Section VI.C.4(b).

(g) Limitations [4b]-[4f]

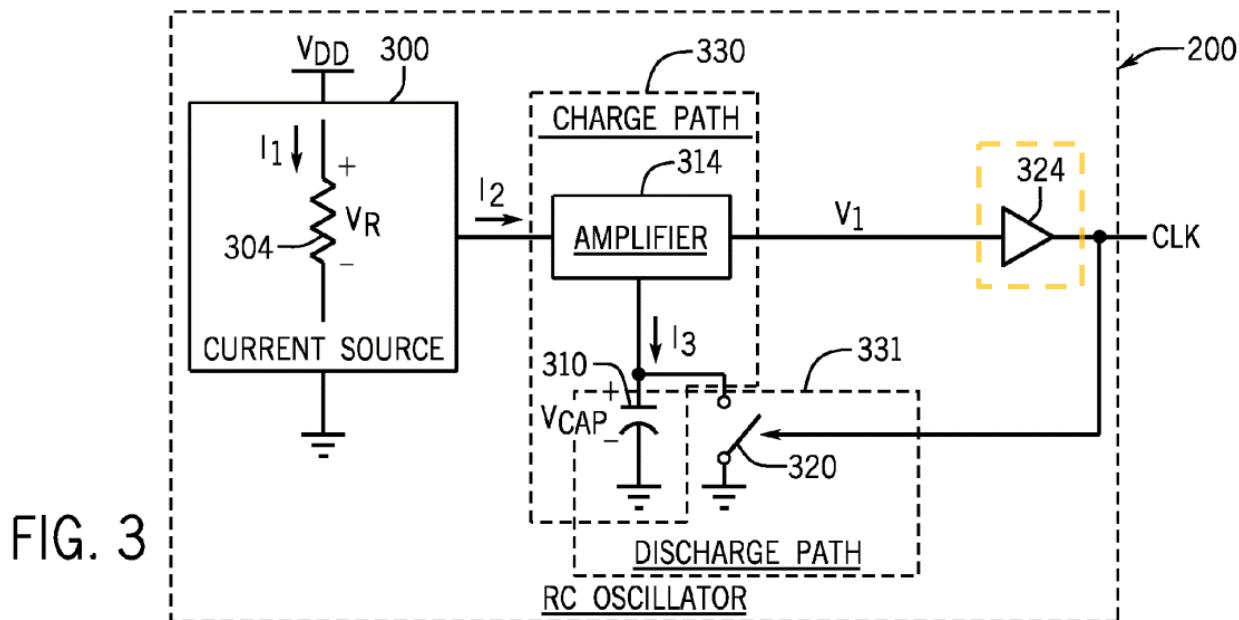
See Section VI.C.4(c).

(h) Limitation [4g]

See Sections VI.A.5(m), VI.B.4(l), VI.C.3.

(i) Claim 5

The remaining buffer 324 (dotted-orange) forms an additional portion of the claimed “detection result latching circuit”:

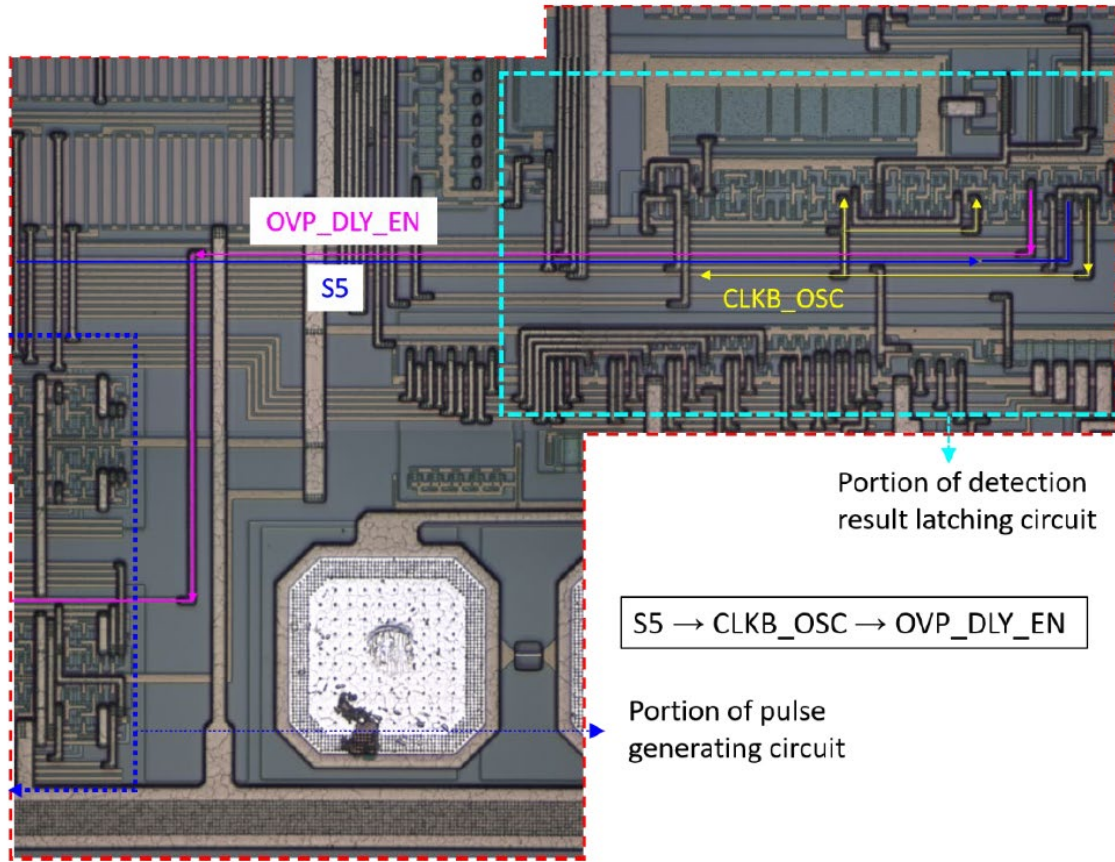


EX1010, Fig. 3 (annotated), 6:1-5; EX1002, ¶174. Thus, in the Ivey-Powell

Combination, the claimed “detection result latching circuit” comprises Powell’s buffer 324, along with Ivey345’s logic inverter 302 and latch 315. *See* Sections VI.A.5(m), VI.C.3; EX1002, ¶174. And in the Ivey-Sadwick-Powell Combination, the claimed “detection result latching circuit” comprises buffer 324, logic inverter 302, latch 315, and the OR gate. *See* Sections VI.B.4(l), VI.C.3; EX1002, ¶174.

As Powell teaches, Powell’s RC oscillator charges and discharges capacitor 310 to cause the output signal, V_1 , to increase and decrease correspondingly—i.e., oscillate. EX1010, 5:13-39; EX1002, ¶175. Specifically, V_1 is pulse shaped by buffer 324 and outputted to switch 320, which closes and opens as V_1 increases and decreases to control “when the charging and discharging parts of the oscillation cycle begin and end” (“the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals”). EX1010, 5:13-39; EX1002, ¶175; *see also* EX1001, 47:7-50.

Should PO contend that the inclusion of buffer 324 as part of the claimed “detection result latching circuit,” rather than “pulse generating circuit,” is overly arbitrary, such would be inconsistent with PO’s infringement contentions in the *Current* Action. Specifically, PO contends that Petitioner’s products include a “detection result latching circuit” (dotted-cyan) that receives pulse signal S5 (solid-blue) from a pulse generating circuit (dotted-blue) and modifies this signal using various components, e.g., “a Schmitt Trigger”:



EX1034, 38-40; EX1035, 40-42; EX1002, ¶176. Allegedly, “[m]ore than one signal is generated as an output from these components,” including an “OVP_DLY_EN” signal (magenta), “which serves as a reset signal” for the pulse generating circuit—that is, “to control the time of the one or more pulse signals.” *Id.* But, just as PO includes a “Schmitt trigger” as a portion of its mapped “detection result latching circuit” accordingly, Grounds 3-4 as discussed above likewise map Powell’s buffer

324,¹⁸ which similarly modifies the pulse signal V_1 to generate a CLK signal that is outputted to multiple paths including one leading back to switch 320, to form part of the “detection result latching circuit.” EX1010, 5:13-39; EX1002, ¶176. Therefore, buffer 324 may be considered part of the claimed “detection result latching circuit.” EX1002, ¶176; *see also* EX1001, 9:28-51.

(j) Claim 32

See Section VI.C.4(i).

VII. DISCRETIONARY DENIAL IS UNWARRANTED

A. In View of the *Current* Action (35 U.S.C. §314(a))

Factor 1¹⁹ is neutral. A stay has not been requested or denied.

Factor 2 favors institution. Trial is currently scheduled for April 17, 2024. EX1036. However, the *Current* Action involves 11 patents and the median time-to-trial for the Western District of Texas is 28.3 months,²⁰ meaning trial likely will not occur until at least October 2024—about 1 month after a decision here.

¹⁸ “A Schmitt trigger *is a buffer* used to convert a slow or noisy signal into a clean one before passing it to the FPGA.” EX1025, 3; EX1002, ¶176 n.12.

¹⁹ *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11, 5-6 (PTAB Mar. 20, 2020) (precedential).

²⁰ <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/06/30-2>.

Factor 3 favors institution. The *Current* Action is in its early stages. PO filed its original complaint on May 24, 2022 and has since amended its complaint.

Factor 4 favors institution. If IPR is instituted, Petitioner will stipulate not to rely on the same grounds in the *Current* Action. EX1037.

Factor 5. The parties are the same.

Factor 6 favors institution. This petition is filed well-within the 12-month statutory period and, for the reasons explained above, the proposed grounds’ merits are compelling.²¹

B. In View of the *CH* Action (§314(a))

With respect to *Fintiv*, a key underlying concern is whether institution will result in an inefficient use of judicial resources due to “duplication of work.” 5-6 & n.7. However, because Petitioner is not a party or related to any party in the *CH* Action, Petitioner’s invalidity arguments over the ’140 Patent have not yet been—but nevertheless will be—tried and adjudicated, regardless of the *CH* Action. In other words, it is inevitable that judicial resources will be expended on Petitioner’s invalidity arguments, either here or otherwise the *Current* Action, and thus discretionarily denying this Petition will not preserve or optimize expenditure of

²¹ See https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

judicial resources. And PO cannot assert unfairness in allowing Petitioner to mount such a defense because PO voluntarily sued Petitioner in the *Current* Action after and separate from the *CH* Action.

Additionally, no “duplication of work” will occur because this Petition’s grounds significantly differ from those presented in the *CH* Action. *See Fintiv*, 12, 14. For example, the *CH* defendant unsuccessfully relied solely on Ivey345 for limitations [1pre]’s “light-emitting diode (LED) tube lamp.” EX1028, 211:24-213:16; EX1029, 69:4-5, 92:21-94:1; EX1030, 15-16; EX1031, 22; EX1032, 9; EX1033, 13. But this Petition relies on Ivey813’s “LED-based light tube” for this claim element. *See* Sections VI.A.5(a), VI.B.4(a). As another example, the *CH* defendant unsuccessfully argued that a POSITA would have been motivated to combine Ivey345 and Sadwick simply because both are “oriented to” the same problem. EX1028, 225:20-229:4; EX1030, 17; EX1032, 9-10; EX1033, 14. This Petition, however, applies the “obvious to try,” “known-technique,” and “motivation to combine” rationales, which, unlike the defendant’s rationale, are explicitly supported by *KSR*. Section VI.C.2; *KSR*, 550 U.S. at 417-21; *Intel*, 2023 WL 2469631, at *4-5. Given these and the numerous other significant differences between the defendant’s and Petitioner’s arguments, the Board will thus be reviewing new, unadjudicated grounds upon institution and will not repeat the work of another tribunal.

C. In View of the Prosecution History (§325(d))

Ivey813, Ivey345, and Powell were not considered during prosecution (*see* EX1003, 180, 476-480), meaning Grounds 1-4 do not present substantially the same prior art or arguments previously presented to the Office.

Should PO argue otherwise, particularly for this Petition's arguments regarding Office-considered Sadwick (*see* EX1003, 231-34), unconsidered Ivey345 discloses a pulse generating circuit that outputs pulse signals independent of fault detection (*see* Section VI.A.5(h)), one or more pulse signals being received through a detection result latching circuit by a switch circuit on a power loop (*see* Section VI.A.5(aa)), and an installation detection circuit coupled between a rectifying circuit and a filtering circuit (*see* Section VI.A.5(u)), which were features the Office found lacking in the prior art—particularly, Sadwick—when allowing the claims (*see* EX1003, 400-01, 373-75, 234). If a showing of Office error is required, that error is failing to consider these teachings of Ivey345 or any reference that is allegedly cumulative thereto.

VIII. CONCLUSION

For the above reasons, institution is appropriate.

Dated: March 22, 2023

/Eagle H. Robinson/

Eagle H. Robinson (Reg. No. 61,361)

Lead Counsel for Petitioner

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(a)(1)(i), the undersigned certifies that this Paper—exclusive of the table of contents, table of authorities, mandatory notices under §42.8, certificate of service, this certificate off word count, appendix of exhibits, and claim listing—includes 13,988 words based on the word count of the word-processing system used to prepare the paper.

/Eagle H. Robinson/
Eagle H. Robinson (Reg. No. 61,361)

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §42.6(e) and 37 C.F.R. §42.105(a), the undersigned certifies that on March 22, 2023, complete copies of this Petition for *Inter Partes* Review, Petitioner's power of attorney, and all exhibits were served on Patent Owner at the correspondence address of record listed below by USPS Priority Mail Express:

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