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October 31, 2016

ATTORNEY DOCKET NO.: SUP-101C-3
CUSTOMER NO. 74,712

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

New U.S. Patent Application

Title: LED TUBE LAMP

Inventor(s): Liu, Xintong; Xiong, Aiming; Jiang, Tao; and Feng Zou.

Sir:

We enclose the following papers for filing in the United States Patent; and Trademark Office in connection with the above patent application.

1. Specification (101 pages);
2. Drawings (16 sheets);
3. Application Data Sheet (PTO/AIA/14);
4. Declaration (5 pages);
5. Power of Attorney (PTO/AIA/82B);
6. Power of Attorney Transmittal (PTO/AIA/82A).

This application is a Continuation-In-Part application of U.S. Patent Application No.: 15/210,989, filed on July 15, 2016, which is a Continuation-In-Part application of U.S. Patent Application No.: 15/066,645, filed on March 10, 2016, which is a Continuation-In-Part application of U.S. Patent Application No.: 14/865,387, filed on September 25, 2015, the disclosure of each of which is incorporated in its entirety by reference herein. U.S. Patent Application No.: 14/865,387, filed on September 25, 2015 claims priority under 35 U.S.C. 119(e) to Chinese Patent Applications No.: CN 201410507660.9 filed on 2014/9/28; CN 201410508899.8 filed on 2014/9/28; CN 201410623355.6 filed on 2014/11/6; CN 201410734425.5 filed on 2014/12/5; CN 201510075925.7 filed on 2015/2/12; CN 201510104823.3 filed on 2015/3/10; CN

201510134586.5 filed on 2015/3/26; CN 201510133689.x filed on 2015/3/25; CN 201510136796.8 filed on 2015/3/27; CN 201510155807.7 filed on 2015/4/3; CN 201510173861.4 filed on 2015/4/14; CN 201510193980.6 filed on 2015/4/22; CN 201510372375.5 filed on 2015/6/26; CN 201510259151.3 filed on 2015/5/19; CN 201510268927.8 filed on 2015/5/22; CN 201510284720.x filed on 2015/5/29; CN 201510338027.6 filed on 2015/6/17; CN 201510315636.x filed on 2015/6/10; CN 201510373492.3 filed on 2015/6/26; CN 201510364735.7 filed on 2015/6/26; CN 201510378322.4 filed on 2015/6/29; CN 201510391910.1 filed on 2015/7/2; CN 201510406595.5 filed on 2015/7/10; CN 201510482944.1 filed on 2015/8/7; CN 201510486115.0 filed on 2015/8/8; CN 201510428680.1 filed on 2015/7/20; CN 201510483475.5 filed on 2015/8/8; CN 201510555543.4 filed on 2015/9/2; CN 201510557717.0 filed on 2015/9/6; CN 201510595173.7 filed on 2015/9/18, the disclosures of each of which are incorporated herein in their entirety by reference.

In addition, U.S. Patent Application No.: 15/066,645, from which U.S. Patent Application No.: 15/210,989 claims priority as a Continuation-In-Part also claims priority under 35 U.S.C. 119(e) to Chinese Patent Applications Nos.: CN 201510530110.3 filed on 2015/8/26; CN 201510499512.1 filed on 2015/8/14; CN 201510448220.5 filed on 2015/7/27; CN 201510645134.3 filed on 2015/10/8; and CN 201510680883.x filed on 2015/10/20, the disclosures of each of which are incorporated herein in their entirety by reference.

U.S. Patent Application No.: 15/210,989 is also a Continuation-In-Part application of U.S. Patent Application No.: 15/205,011, filed on July 08, 2016, the disclosure of which is incorporated in its entirety by reference herein, which is a Continuation-In-Part application of U.S. Patent Application No.: 15/150,458, filed on May 10, 2016, the disclosure of which is incorporated in its entirety by reference herein, which is a Continuation-In-Part Application of U.S. Patent Application No. 14/865,387, filed on September 25, 2015, which claims priority under 35 U.S.C. 119(e) to the following Chinese Patent Applications filed in the Chinese Patent Office: CN 201410507660.9 filed on 2014/9/28; CN 201410508899.8 filed on 2014/9/28; CN 201410623355.6 filed on 2014/11/6; CN 201410734425.5 filed on 2014/12/5; CN 201510075925.7 filed on 2015/2/12; CN 201510104823.3 filed on 2015/3/10; CN 201510134586.5 filed on 2015/3/26; CN 201510133689.x filed on 2015/3/25; CN 201510136796.8 filed on 2015/3/27; CN 201510173861.4 filed on 2015/4/14; CN 201510155807.7 filed on 2015/4/3; CN 201510193980.6 filed on 2015/4/22; CN 201510372375.5 filed on 2015/6/26; CN 201510259151.3 filed on 2015/5/19; CN 201510268927.8 filed on 2015/5/22; CN 201510284720.x filed on 2015/5/29; CN 201510338027.6 filed on 2015/6/17; CN 201510315636.x filed on 2015/6/10; CN 201510373492.3 filed on 2015/6/26; CN 201510364735.7 filed on 2015/6/26; CN 201510378322.4 filed on 2015/6/29; CN 201510391910.1 filed on 2015/7/2; CN 201510406595.5 filed on 2015/7/10; CN 201510482944.1 filed on 2015/8/7; CN 201510486115.0 filed on 2015/8/8; CN 201510428680.1 filed on 2015/7/20; CN 201510483475.5 filed on 2015/8/8; CN 201510555543.4 filed on 2015/9/2; CN 201510557717.0 filed on

2015/9/6; and CN 201510595173.7 filed on 2015/9/18, the disclosures of which U.S. and Chinese patent applications are incorporated herein by reference in their entirety. U.S. Patent Application No. 15/150,458, filed on 2016/5/10 is also a Continuation-In-Part application of U.S. Patent Application No. 14/699,138, filed on 2015/4/29, which claims priority under 35 U.S.C. 119(e) to Chinese Patent Application No. CN 201420602526.2, filed on 2014/10/17.

In addition, U.S. Patent Application No.: 15/205,011, from which U.S. Patent Application No.: 15/210,989 claims priority as a Continuation-in-Part also claims priority under 35 U.S.C. 119(e) to Chinese Patent Application Nos.: CN 201610327806.0, filed on May 18, 2016; CN 201620089157.0, filed on January 28, 2016; and CN 201610420790.8, filed on June 14, 2016, the disclosures of each of which are incorporated herein in their entirety by reference.

In addition, U.S. Patent Application No.: 15/210,989 also claims priority under 35 U.S.C. 119(e) to Chinese Patent Application Nos.: CN 201510848766.X, filed on November 27, 2015; CN 201510903680.2, filed on December 09, 2015; CN 201610132513.7, filed on March 09, 2016; CN 201610142140.1, filed on March 14, 2016; and CN 201610452437.8, filed on June 20, 2016, the disclosures of each of which are incorporated herein in their entirety by reference. In addition, U.S. Patent Application No.: 15/210,989 also claims priority under 35 U.S.C. 119(e) to Chinese Patent Application Nos.: CN 201510530110.3, filed on August 26, 2015; CN 201510499512.1, filed on August 14, 2015; CN 201510617370.4, filed on September 25, 2015; CN 201510645134.3, filed on October 8, 2015; CN 201510716899.1, filed on October 29, 2015; CN 201510726365.7, filed on October 30, 2015; CN 201510868263.9, filed on December 2, 2015; CN 201610044148.4, filed on January 22, 2016; CN 201610051691.7, filed on January 26, 2016; CN 201610085895.2, filed on February 15, 2016; CN 201610087627.4, filed on February 16, 2016; CN201610281812.7, filed on April 29, 2016; CN 201510705222.8, filed on October 27, 2015; CN 201510726484.2, filed on October 30, 2015; CN 201610050944.9, filed on January 26, 2016; CN 201610098424.5, filed on February 23, 2016; and CN 201610120993.5, filed on March 3, 2016, the disclosures of each of which are incorporated herein by reference in their entirety.

In addition, this application claims priority under 35 U.S.C. 119(e) to Chinese Patent Application No.: CN 201610876593.7, filed on October 8, 2016, the entire contents of which are incorporated herein by reference.

Please accord this application an application number and filing date.

This application is being filed electronically. The required fees are being paid via deposit account 50-4574. The Commissioner is hereby authorized to charge any additional filing fees due and any other fees due under 37 C.F.R. § 1.16, §1.17, §1.18,

§1.19, or §1.20 during the pendency of this application, and to refund any overpayments, to our Deposit Account No. 50-4574.

Respectfully submitted,

MUIR PATENT LAW, PLLC

By: /Ali Imam/
Ali Imam
Reg. No. 58755

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
Approved for use through 11/30/2014. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 74,712

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

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☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Jiaxing Super Lighting Electric Appliance Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	Tao Jiang	Date (Optional)	Sep. 21 2015
Name	Tao Jiang		
Title	Chairman of the Board, Jiaxing Super Lighting Electric Appliance Co., Ltd.		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/82A (07-12)
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B or equivalent) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5. If the Power of Attorney by Applicant form is not accompanied by this transmittal form or an equivalent, the Power of Attorney will not be recognized in the application.

Application Number	Not Yet Assigned
Filing Date	Herewith
First Named Inventor	Liu,Xintong
Title	LED TUBE LAMP
Art Unit	Not Yet Assigned
Examiner Name	Not Yet Assigned
Attorney Docket Number	SUP-101C-3

SIGNATURE of Applicant or Patent Practitioner

Signature	/Ali Imam/	Date	October 31, 2016
Name	Ali Imam	Telephone	703-757-7880
Registration Number	58755		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

■ *Total of 1 forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/AIA/82B(07-12)
Approved for use through 11/30/2014. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

☒ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

74712

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

☒ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (*e.g.,* a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	
Name		Telephone	
Title and Company			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong LIU
Filer:	Ali M. Imam
Attorney Docket Number:	SUP-101C-3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	12	80	960
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2560**

Electronic Acknowledgement Receipt

EFS ID:	27373706
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong LIU
Customer Number:	74712
Filer:	Ali M. Imam
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	31-OCT-2016
Filing Date:	
Time Stamp:	16:42:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2560
RAM confirmation Number	110116INTEFSW16445500
Deposit Account	504574
Authorized User	Amy Dean

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUP-101C-3_Spec.pdf	823581 48be35f5db770f7d7be7dada04e2af4e1c88b5be	yes	101
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	90	
	Claims		91	100	
	Abstract		101	101	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	SUP-101C-3_Drawings.pdf	1690472 a7f9819dc03c504217d63de9bc158b00ca7ca918	no	16
Warnings:					
Information:					
3	Application Data Sheet	SUP-101C-3_ADS.pdf	1505014 2c2b56d6db082fddd5aa5e673b4c831d363f1ab0	no	13
Warnings:					
Information:					
4	Oath or Declaration filed	SUP-101C-3_Dec.pdf	1070043 29aa6df1b07d0fe9696bc61c2048fb59c5b5467f	no	5
Warnings:					
Information:					
5	Transmittal of New Application	SUP-101C-3_New_app_transmittal.pdf	77226 cd71bea31e3edf1d7031e6815f2616b4c57c6c30	no	4

Warnings:					
Information:					
6	Power of Attorney	SUP-101C-3_POA_82B.pdf	562536 32cf1a9455918880b7b5bb5ba32e450040e0d89f	no	1
Warnings:					
Information:					
7	Power of Attorney	SUP-101C-3_PoA_aia0082a.pdf	220907 4c2c7324e2b60e1fd94fb3852ef0b954529f90bf	no	3
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	36449 a60f1ef73bd1758cad08ba7d5a828229c294937e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	5986228	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

LED TUBE LAMP

RELATED APPLICATIONS

[0001] This application is a Continuation-In-Part application of U.S. Patent Application No.: 15/210,989, filed on July 15, 2016, which is a Continuation-In-Part application of U.S. Patent Application No.: 15/066,645, filed on March 10, 2016, which is a Continuation-In-Part application of U.S. Patent Application No.: 14/865,387, filed on September 25, 2015, the disclosure of each of which is incorporated in its entirety by reference herein. U.S. Patent Application No.: 14/865,387, filed on September 25, 2015 claims priority under 35 U.S.C. 119(e) to Chinese Patent Applications No.: CN 201410507660.9 filed on 2014/9/28; CN 201410508899.8 filed on 2014/9/28; CN 201410623355.6 filed on 2014/11/6; CN 201410734425.5 filed on 2014/12/5; CN 201510075925.7 filed on 2015/2/12; CN 201510104823.3 filed on 2015/3/10; CN 201510134586.5 filed on 2015/3/26; CN 201510133689.x filed on 2015/3/25; CN 201510136796.8 filed on 2015/3/27; CN 201510155807.7 filed on 2015/4/3; CN 201510173861.4 filed on 2015/4/14; CN 201510193980.6 filed on 2015/4/22; CN 201510372375.5 filed on 2015/6/26; CN 201510259151.3 filed on 2015/5/19; CN 201510268927.8 filed on 2015/5/22; CN 201510284720.x filed on 2015/5/29; CN 201510338027.6 filed on 2015/6/17; CN 201510315636.x filed on 2015/6/10; CN 201510373492.3 filed on 2015/6/26; CN 201510364735.7 filed on 2015/6/26; CN 201510378322.4 filed on 2015/6/29; CN 201510391910.1 filed on 2015/7/2; CN 201510406595.5 filed on 2015/7/10; CN 201510482944.1 filed on 2015/8/7; CN 201510486115.0 filed on 2015/8/8; CN 201510428680.1 filed on 2015/7/20; CN 201510483475.5 filed on 2015/8/8; CN 201510555543.4 filed on 2015/9/2; CN 201510557717.0 filed on 2015/9/6; CN 201510595173.7 filed on 2015/9/18, the disclosures of each of which are incorporated

herein in their entirety by reference.

[0002] In addition, U.S. Patent Application No.: 15/066,645, from which U.S. Patent Application No.: 15/210,989 claims priority as a Continuation-In-Part also claims priority under 35 U.S.C. 119(e) to Chinese Patent Applications Nos.: CN 201510530110.3 filed on 2015/8/26; CN 201510499512.1 filed on 2015/8/14; CN 201510448220.5 filed on 2015/7/27; CN 201510645134.3 filed on 2015/10/8; and CN 201510680883.x filed on 2015/10/20, the disclosures of each of which are incorporated herein in their entirety by reference.

[0003] U.S. Patent Application No.: 15/210,989 is also a Continuation-In-Part application of U.S. Patent Application No.: 15/205,011, filed on July 08, 2016, the disclosure of which is incorporated in its entirety by reference herein, which is a Continuation-In-Part application of U.S. Patent Application No.: 15/150,458, filed on May 10, 2016, the disclosure of which is incorporated in its entirety by reference herein, which is a Continuation-In-Part Application of U.S. Patent Application No. 14/865,387, filed on September 25, 2015, which claims priority under 35 U.S.C. 119(e) to the following Chinese Patent Applications filed in the Chinese Patent Office: CN 201410507660.9 filed on 2014/9/28; CN 201410508899.8 filed on 2014/9/28; CN 201410623355.6 filed on 2014/11/6; CN 201410734425.5 filed on 2014/12/5; CN 201510075925.7 filed on 2015/2/12; CN 201510104823.3 filed on 2015/3/10; CN 201510134586.5 filed on 2015/3/26; CN 201510133689.x filed on 2015/3/25; CN 201510136796.8 filed on 2015/3/27; CN 201510173861.4 filed on 2015/4/14; CN 201510155807.7 filed on 2015/4/3; CN 201510193980.6 filed on 2015/4/22; CN 201510372375.5 filed on 2015/6/26; CN 201510259151.3 filed on 2015/5/19; CN 201510268927.8 filed on 2015/5/22; CN 201510284720.x filed on 2015/5/29; CN 201510338027.6 filed on 2015/6/17; CN 201510315636.x filed on 2015/6/10; CN 201510373492.3 filed on 2015/6/26; CN 201510364735.7

filed on 2015/6/26; CN 201510378322.4 filed on 2015/6/29; CN 201510391910.1 filed on 2015/7/2; CN 201510406595.5 filed on 2015/7/10; CN 201510482944.1 filed on 2015/8/7; CN 201510486115.0 filed on 2015/8/8; CN 201510428680.1 filed on 2015/7/20; CN 201510483475.5 filed on 2015/8/8; CN 201510555543.4 filed on 2015/9/2; CN 201510557717.0 filed on 2015/9/6; and CN 201510595173.7 filed on 2015/9/18, the disclosures of which U.S. and Chinese patent applications are incorporated herein by reference in their entirety. U.S. Patent Application No. 15/150,458, filed on 2016/5/10 is also a Continuation-In-Part application of U.S. Patent Application No. 14/699,138, filed on 2015/4/29, which claims priority under 35 U.S.C. 119(e) to Chinese Patent Application No. CN 201420602526.2, filed on 2014/10/17.

[0004] In addition, U.S. Patent Application No.: 15/205,011, from which U.S. Patent Application No.: 15/210,989 claims priority as a Continuation-in-Part also claims priority under 35 U.S.C. 119(e) to Chinese Patent Application Nos.: CN 201610327806.0, filed on May 18, 2016; CN 201620089157.0, filed on January 28, 2016; and CN 201610420790.8, filed on June 14, 2016, the disclosures of each of which are incorporated herein in their entirety by reference.

[0005] In addition, U.S. Patent Application No.: 15/210,989 also claims priority under 35 U.S.C. 119(e) to Chinese Patent Application Nos.: CN 201510848766.X, filed on November 27, 2015; CN 201510903680.2, filed on December 09, 2015; CN 201610132513.7, filed on March 09, 2016; CN 201610142140.1, filed on March 14, 2016; and CN 201610452437.8, filed on June 20, 2016, the disclosures of each of which are incorporated herein in their entirety by reference. In addition, U.S. Patent Application No.: 15/210,989 also claims priority under 35 U.S.C. 119(e) to Chinese Patent Application Nos.: CN 201510530110.3, filed on August 26, 2015; CN 201510499512.1, filed on August 14, 2015; CN 201510617370.4, filed on September 25, 2015; CN 201510645134.3,

filed on October 8, 2015; CN 201510716899.1, filed on October 29, 2015; CN 201510726365.7, filed on October 30, 2015; CN 201510868263.9, filed on December 2, 2015; CN 201610044148.4, filed on January 22, 2016; CN 201610051691.7, filed on January 26, 2016; CN 201610085895.2, filed on February 15, 2016; CN 201610087627.4, filed on February 16, 2016; CN201610281812.7, filed on April 29, 2016; CN 201510705222.8, filed on October 27, 2015; CN 201510726484.2, filed on October 30, 2015; CN 201610050944.9, filed on January 26, 2016; CN 201610098424.5, filed on February 23, 2016; and CN 201610120993.5, filed on March 3, 2016, the disclosures of each of which are incorporated herein by reference in their entirety.

[0006] In addition, this application claims priority under 35 U.S.C. 119(e) to Chinese Patent Application No.: CN 201610876593.7, filed on October 8, 2016, the entire contents of which are incorporated herein by reference.

TECHNICAL FIELD

[0007] The disclosed embodiments relate to the features of light emitting diode (LED) lighting. More particularly, the disclosed embodiments describe various improvements for LED tube lamps.

BACKGROUND

[0008] LED lighting technology is rapidly developing to replace traditional incandescent and fluorescent lighting. LED tube lamps are mercury-free in comparison with fluorescent tube lamps that need to be filled with inert gas and mercury. Thus, it is not surprising that LED tube lamps are becoming a highly desired illumination option among different available lighting systems used in homes and workplaces, which used to be dominated by traditional lighting options such as compact fluorescent light bulbs (CFLs) and fluorescent tube lamps. Benefits of LED tube lamps include improved durability and longevity and far less energy consumption. Therefore, when taking into account all factors, they would typically be considered as

a cost effective lighting option.

[0009] Typical LED tube lamps have a lamp tube, a circuit board disposed inside the lamp tube with light sources being mounted on the circuit board, and end caps accompanying a power supply provided at two ends of the lamp tube with the electricity from the power supply transmitting to the light sources through the circuit board. However, existing LED tube lamps have certain drawbacks. For example, the typical circuit board is rigid and allows the entire lamp tube to maintain a straight tube configuration when the lamp tube is partially ruptured or broken, and this gives the user a false impression that the LED tube lamp remains usable and is likely to cause the user to be electrically shocked upon handling or installation of the LED tube lamp.

[0010] Conventional circuit design of LED tube lamps typically doesn't provide suitable solutions for complying with relevant certification standards. For example, since there are usually no electronic components in a fluorescent lamp, it's fairly easy for a fluorescent lamp to be certified under EMI (electromagnetic interference) standards and safety standards for lighting equipment as provided by Underwriters Laboratories (UL). However, there are a considerable number of electronic components in an LED tube lamp, and therefore consideration of the impacts caused by the layout (structure) of the electronic components is important, resulting in difficulties in complying with such standards.

[0011] Further, the driving of an LED uses a DC driving signal, but the driving signal for a fluorescent lamp is a low-frequency, low-voltage AC signal as provided by an AC powerline, a high-frequency, high-voltage AC signal provided by a ballast, or even a DC signal provided by a battery for emergency lighting applications. Since the voltages and frequency spectrums of these types of signals differ significantly, simply performing a rectification to produce the required DC driving signal in an LED tube lamp may not achieve the LED tube lamp's compatibility with traditional driving systems of a fluorescent lamp.

[0012] Moreover, when an LED tube lamp has an architecture with dual-end power supply and one end cap thereof is inserted into a lamp socket but the other is not, an electric shock situation could take place for the user touching the metal or conductive part of the end cap which has not been inserted into the lamp socket.

[0013] Currently, LED tube lamps used to replace traditional fluorescent lighting devices can be primarily categorized into two types. One is for ballast-compatible LED tube lamps, e.g., T-LED lamp, which directly replaces fluorescent tube lamps without changing any circuit on the lighting device; and the other one is for ballast by-pass LED tube lamps, which omit traditional ballast on their circuit and directly connect the commercial electricity to the LED tube lamp. The latter LED tube lamp is suitable for the new surroundings in fixtures with new driving circuits and LED tube lamps.

SUMMARY

[0014] It's specially noted that the present disclosure may actually include one or more inventions claimed currently or not yet claimed, and for avoiding confusion due to unnecessarily distinguishing between those possible inventions at the stage of preparing the specification, the possible plurality of inventions herein may be collectively referred to as "the (present) invention" herein.

[0015] Various embodiments are summarized in this section, and may be described with respect to the "present invention," which terminology is used to describe certain presently disclosed embodiments, whether claimed or not, and is not necessarily an exhaustive description of all possible embodiments, but rather is merely a summary of certain embodiments. Certain of the embodiments described below as various aspects of the "present invention" can be combined in different manners to form an LED tube lamp or a portion thereof.

[0016] The present disclosure provides a novel LED tube lamp, and aspects thereof.

[0017] According to certain embodiments, an installation detection circuit configured in the LED tube lamp configured to receive an external driving signal is disclosed. The installation detection circuit includes: a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated

from the external driving signal; and a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit; wherein the installation detection circuit is further configured to: when it is detected during one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and when it is detected during one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain conducting state.

[0018] According to certain embodiments, an installation detection circuit configured in a light-emitting diode (LED) tube lamp is disclosed. The installation detection circuit includes: means for generating one or more pulse signals; means for detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket; and a switch circuit coupled to the means for generating one or more pulse signals, wherein the one or more pulse signals control turning on and off of the switch circuit; wherein the installation detection circuit is further configured to: when it is detected during the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and when it is detected during the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

[0019] According to certain embodiments, a detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket is disclosed. The detection method includes: when at least one end of the LED tube lamp is installed on the lamp socket, generating one or more pulse signals by a pulse generating circuit, wherein the pulse generating circuit is configured in the LED tube lamp; detecting a sampling signal on a power loop of the LED tube lamp by a detection determining circuit, to detect during the one or more pulse signals whether the other end of the LED tube

lamp is properly installed on the lamp socket; receiving the one or more pulse signals through a detection result latching circuit by a switch circuit, wherein the switch circuit is on the power loop; and comparing the sampling signal with a predefined signal, wherein during the one or more pulse signals when the sampling signal is smaller than the predefined signal, the detection method further comprises: controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open.

BRIEF DESCRIPTION OF THE FIGURES

[0020] Fig. 1 is a plane cross-sectional view schematically illustrating an LED tube lamp including an LED light strip that is a bendable circuit sheet with ends thereof passing across the transition region of the lamp tube of the LED tube lamp to be connected to a power supply according to some exemplary embodiments;

[0021] Fig. 2 is a plane cross-sectional view schematically illustrating a bi-layered structure of a bendable circuit sheet of an LED light strip of an LED tube lamp according to some exemplary embodiments;

[0022] Fig. 3A is a perspective view schematically illustrating a soldering pad of a bendable circuit sheet of an LED light strip for a solder connection with a power supply of an LED tube lamp according to some exemplary embodiments;

[0023] Fig. 3B is a block diagram illustrating leads that are disposed between two end caps of an LED tube lamp according to some exemplary embodiments;

[0024] Fig. 4A is a perspective view of a bendable circuit sheet and a printed circuit board of a power supply soldered to each other in accordance with an exemplary embodiment;

[0025] Figs. 4B, 4C, and 4D are diagrams of a soldering process of the bendable circuit sheet and the printed circuit board of the power supply of Fig. 4A in accordance with an exemplary embodiment;

[0026] Fig. 5 is a perspective view schematically illustrating a circuit board assembly composed of a bendable circuit sheet of an LED light strip and a printed circuit board of a power supply according to some exemplary embodiments;

[0027] Fig. 6 is a perspective view schematically illustrating another arrangement of a circuit board assembly, according to some exemplary embodiments;

[0028] Fig. 7 is a perspective view schematically illustrating a bendable circuit sheet of an LED light strip formed with two conductive wiring layers according to some exemplary embodiments;

[0029] Fig. 8A is a block diagram of an exemplary power supply system for an LED tube lamp according to some exemplary embodiments;

[0030] Fig. 8B is a block diagram of an exemplary power supply system for an LED tube lamp according to some exemplary embodiments;

[0031] Fig. 8C is a block diagram of an exemplary LED lamp according to some exemplary embodiments;

[0032] Fig. 9 is a schematic diagram of a rectifying circuit according to some exemplary embodiments;

[0033] Figs. 10A-10C are block diagrams of exemplary filtering circuits according to some exemplary embodiments;

[0034] Figs. 11A-11B are schematic diagrams of exemplary LED modules according to some exemplary embodiments;

[0035] Figs. 11C-11E are plan views of a circuit layout of an LED module according to some exemplary embodiments;

[0036] Fig. 12A is a block diagram of an exemplary power supply module in an LED lamp according to some exemplary embodiments;

[0037] Fig. 12B is a block diagram of a driving circuit according to some exemplary embodiments;

[0038] Figs. 12C-12F are schematic diagrams of exemplary driving circuits according to some exemplary embodiments;

[0039] Fig. 13A is a block diagram of an exemplary power supply module in an LED tube lamp according to some exemplary embodiments;

[0040] Fig. 13B is a schematic diagram of an over-voltage protection (OVP) circuit according to some exemplary embodiments;

[0041] Fig. 14A is a block diagram of an exemplary power supply module in an LED tube lamp according to some exemplary embodiments;

[0042] Fig. 14B is a block diagram of an exemplary power supply module in an LED tube lamp according to some exemplary embodiments;

[0043] Fig. 14C is a schematic diagram of an auxiliary power module according to some exemplary embodiments;

[0044] Fig. 15A is a block diagram of an LED tube lamp according to some exemplary embodiments;

[0045] Fig. 15B is a block diagram of an installation detection module according to some exemplary embodiments;

[0046] Fig. 15C is a schematic detection pulse generating module according to some exemplary embodiments;

[0047] Fig. 15D is a schematic detection determining circuit according to some exemplary embodiments;

[0048] Fig. 15E is a schematic detection result latching circuit according to some exemplary embodiments;

[0049] Fig. 15F is a schematic switch circuit according to some exemplary embodiments;

[0050] Fig. 15G is a block diagram of an installation detection module according to some exemplary embodiments;

[0051] Fig. 15H is a schematic detection pulse generating module according to some exemplary embodiments;

[0052] Fig. 15I is a schematic detection result latching circuit according to some exemplary embodiments;

[0053] Fig. 15J is a schematic switch circuit according to some exemplary embodiments; and

[0054] Fig. 15K is a schematic detection determining circuit according to some exemplary embodiments.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0055] The present disclosure provides a novel LED tube lamp. The present disclosure will now be described in the following embodiments with reference to the

drawings. The following descriptions of various embodiments of this invention are presented herein for purpose of illustration and giving examples only. It is not intended to be exhaustive or to be limited to the precise form disclosed. These example embodiments are just that – examples – and many implementations and variations are possible that do not require the details provided herein. It should also be emphasized that the disclosure provides details of alternative examples, but such listing of alternatives is not exhaustive. Furthermore, any consistency of detail between various examples should not be interpreted as requiring such detail – it is impracticable to list every possible variation for every feature described herein. The language of the claims should be referenced in determining the requirements of the invention.

[0056] In the drawings, the size and relative sizes of components may be exaggerated for clarity. Like numbers refer to like elements throughout.

[0057] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items and may be abbreviated as "/".

[0058] It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers, or steps, these elements, components, regions, layers, and/or steps should not be limited by these terms. Unless the context indicates otherwise, these terms are only used to distinguish one element, component, region, layer, or step from another element, component, region, or step, for example as a naming convention. Thus, a first element, component, region, layer, or step discussed below in one section of the specification could be termed a second element, component, region, layer, or step in another section of the specification or in the claims without departing from the teachings of the present invention. In addition, in certain cases, even if a term is not described using “first,” “second,” etc., in the specification, it may still be referred to as “first” or “second” in a claim in order to distinguish different claimed elements from

each other.

[0059] It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0060] It will be understood that when an element is referred to as being "connected" or "coupled" to or "on" another element, it can be directly connected or coupled to or on the other element or intervening elements may be present. In contrast, when an element is referred to as being "directly connected" or "directly coupled" to another element, there are no intervening elements present. Other words used to describe the relationship between elements should be interpreted in a like fashion (e.g., "between" versus "directly between," "adjacent" versus "directly adjacent," etc.). However, the term "contact," as used herein refers to direct connection (i.e., touching) unless the context indicates otherwise.

[0061] Embodiments described herein will be described referring to plane views and/or cross-sectional views by way of ideal schematic views. Accordingly, the exemplary views may be modified depending on manufacturing technologies and/or tolerances. Therefore, the disclosed embodiments are not limited to those shown in the views, but include modifications in configuration formed on the basis of manufacturing processes. Therefore, regions exemplified in figures may have schematic properties, and shapes of regions shown in figures may exemplify specific shapes of regions of elements to which aspects of the invention are not limited.

[0062] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper" and the like, may be used herein for ease of description to describe one element's or feature's relationship to another element(s) or feature(s) as illustrated in the figures. It will be understood that the spatially relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. For example, if the device in the figures is turned over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the term "below" can

encompass both an orientation of above and below. The device may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein interpreted accordingly.

[0063] Terms such as "same," "equal," "planar," or "coplanar," as used herein when referring to orientation, layout, location, shapes, sizes, amounts, or other measures do not necessarily mean an exactly identical orientation, layout, location, shape, size, amount, or other measure, but are intended to encompass nearly identical orientation, layout, location, shapes, sizes, amounts, or other measures within acceptable variations that may occur, for example, due to manufacturing processes. The term "substantially" may be used herein to emphasize this meaning, unless the context or other statements indicate otherwise. For example, items described as "substantially the same," "substantially equal," or "substantially planar," may be exactly the same, equal, or planar, or may be the same, equal, or planar within acceptable variations that may occur, for example, due to manufacturing processes.

[0064] Terms such as "about" or "approximately" may reflect sizes, orientations, or layouts that vary only in a small relative manner, and/or in a way that does not significantly alter the operation, functionality, or structure of certain elements. For example, a range from "about 0.1 to about 1" may encompass a range such as a 0%-5% deviation around 0.1 and a 0% to 5% deviation around 1, especially if such deviation maintains the same effect as the listed range.

[0065] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this disclosure belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and/or the present application, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0066] As used herein, items described as being "electrically connected" are configured such that an electrical signal can be passed from one item to the other. Therefore, a passive electrically conductive component (e.g., a wire, pad, internal electrical line, etc.) physically connected to a passive electrically insulative

component (e.g., a prepreg layer of a printed circuit board, an electrically insulative adhesive connecting two devices, an electrically insulative underfill or mold layer, etc.) is not electrically connected to that component. Moreover, items that are "directly electrically connected," to each other are electrically connected through one or more passive elements, such as, for example, wires, pads, internal electrical lines, resistors, etc. As such, directly electrically connected components do not include components electrically connected through active elements, such as transistors or diodes. Directly electrically connected elements may be directly physically connected and directly electrically connected.

[0067] Components described as thermally connected or in thermal communication are arranged such that heat will follow a path between the components to allow the heat to transfer from the first component to the second component. Simply because two components are part of the same device or board does not make them thermally connected. In general, components which are heat-conductive and directly connected to other heat-conductive or heat-generating components (or connected to those components through intermediate heat-conductive components or in such close proximity as to permit a substantial transfer of heat) will be described as thermally connected to those components, or in thermal communication with those components. On the contrary, two components with heat-insulative materials therebetween, which materials significantly prevent heat transfer between the two components, or only allow for incidental heat transfer, are not described as thermally connected or in thermal communication with each other. The terms "heat-conductive" or "thermally-conductive" do not apply to any material that provides incidental heat conduction, but are intended to refer to materials that are typically known as good heat conductors or known to have utility for transferring heat, or components having similar heat conducting properties as those materials.

[0068] Embodiments may be described, and illustrated in the drawings, in terms of functional blocks, units and/or modules. Those skilled in the art will appreciate that these blocks, units and/or modules are physically implemented by electronic (or optical) circuits such as logic circuits, discrete components, analog circuits, hard-wired circuits, memory elements, wiring connections, and the like, which may be

formed using semiconductor-based fabrication techniques or other manufacturing technologies. In the case of the blocks, units and/or modules being implemented by microprocessors or similar, they may be programmed using software (e.g., microcode) to perform various functions discussed herein and may optionally be driven by firmware and/or software. Alternatively, each block, unit and/or module may be implemented by dedicated hardware, or as a combination of dedicated hardware to perform some functions and a processor (e.g., one or more programmed microprocessors and associated circuitry) to perform other functions. Also, each block, unit and/or module of the embodiments may be physically separated into two or more interacting and discrete blocks, units and/or modules. Further, the blocks, units and/or modules of the various embodiments may be physically combined into more complex blocks, units and/or modules.

[0069] If any terms in this application conflict with terms used in any application(s) from which this application claims priority, or terms incorporated by reference into this application or the application(s) from which this application claims priority, a construction based on the terms as used or defined in this application should be applied.

[0070] Applicant's prior U.S. Patent Application No. 14/724,840 (US PGPUb No. 2016/0091156, the disclosure of which is incorporated herein in its entirety by reference), as an illustrated example, has addressed certain issues associated with the occurrence of electric shock in using a conventional LED lamp by providing a bendable circuit sheet. Some of the embodiments disclosed in U.S. Patent Application No. 14/724,840 can be combined with one or more of the example embodiments disclosed herein to further reduce the occurrence of electric shock in using an LED lamp.

[0071] Referring to Fig. 1, an LED tube lamp may include an LED light strip 2. In certain embodiments, the LED light strip 2 may be formed from a bendable circuit sheet, for example that may be flexible. As described further below, the bendable circuit sheet, also described as a bendable circuit board, or a flexible or non-rigid tape. The bendable circuit sheet may have ends thereof passing across a transition region of the lamp tube of the LED tube lamp to be connected to a power supply 5. In some

embodiments, the ends of the bendable circuit sheet may be connected to a power supply in an end cap of the LED tube lamp. For example, the ends may be connected in a manner such that a portion of the bendable circuit sheet is bent away from the lamp tube and passes through the transition region where a lamp tube narrows, and such that the bendable circuit sheet vertically overlaps part of a power supply within an end cap of the LED tube lamp.

[0072] Referring to Fig. 2, to form an LED light strip 2, a bendable circuit sheet includes a wiring layer 2a with conductive effect. An LED light source 202 is disposed on the wiring layer 2a and is electrically connected to the power supply through the wiring layer 2a. Though only one LED light source 202 is shown in Fig. 2, a plurality of LED light sources 202, as shown in Fig. 1, may be arranged on the LED light strip 2. For example, light sources 202 may be arranged in one or more rows extending along a length direction of the LED light strip 2, which may extend along a length direction of the lamp tube as illustrated in Fig. 1. The wiring layer with conductive effect, in this specification, is also referred to as a conductive layer. Referring to Fig. 2 again, in one embodiment, the LED light strip 2 includes a bendable circuit sheet having a conductive wiring layer 2a and a dielectric layer 2b that are arranged in a stacked manner. In some embodiments, the wiring layer 2a and the dielectric layer 2b may have the same areas or the area of the wiring layer 2a may slightly be smaller than that of the dielectric layer 2b. The LED light source 202 is disposed on one surface of the wiring layer 2a, the dielectric layer 2b is disposed on the other surface of the wiring layer 2a that is away from the LED light sources 202 (e.g., a second, opposite surface from the first surface on which the LED light source 202 is disposed). The wiring layer 2a is electrically connected to a power supply 5 (as shown in Fig. 1) to carry direct current (DC) signals. In some embodiments, the surface of the dielectric layer 2b away from the wiring layer 2a (e.g., a second surface of the dielectric layer 2b opposite a first surface facing the wiring layer 2a) is fixed to an inner circumferential surface of a lamp tube, for example, by means of an adhesive sheet 4. The portion of the dielectric layer 2b fixed to the inner circumferential surface of the lamp tube 1 may substantially conform to the shape of the inner circumferential surface of the lamp tube 1. The wiring layer 2a can be a metal layer or a power supply

layer including wires such as copper wires.

[0073] A power supply as described herein may include a circuit that converts or generates power based on a received voltage, in order to supply power to operate an LED module and the LED light sources 202 of the LED tube lamp. A power supply, as described in connection with power supply 5, may be otherwise referred to as a power conversion module or circuit or a power module. A power conversion module or circuit, or power module, may supply or provide power from external signal(s), such as from an AC power line or from a ballast, to an LED module and the LED light sources 202. For example, a power supply 5 may refer to a circuit that converts ac line voltage to dc voltage and supplies power to the LED or LED module. The power supply 5 may include one or more power components mounted thereon for converting and/or generating power.

[0074] In some example embodiments, the outer surface of the wiring layer 2a or the dielectric layer 2b may be covered with a circuit protective layer made of an ink with function of resisting soldering and increasing reflectivity. Alternatively, in other example embodiments, the dielectric layer may be omitted and the wiring layer may be directly bonded to the inner circumferential surface of the lamp tube, and the outer surface of the wiring layer 2a may be coated with the circuit protective layer. Whether the wiring layer 2a has a one-layered, or two-layered structure, the circuit protective layer may be adopted. In some embodiments, the circuit protective layer is disposed only on one side/surface of the LED light strip 2, such as the surface having the LED light source 202. In some embodiments, the bendable circuit sheet is a one-layered structure made of just one wiring layer 2a, or a two-layered structure made of one wiring layer 2a and one dielectric layer 2b, and thus is more bendable or flexible to curl when compared with the conventional three-layered flexible substrate (one dielectric layer sandwiched with two wiring layers). As a result, the bendable circuit sheet of the LED light strip 2 may be installed in a lamp tube with a customized shape or non-tubular shape, and fitly mounted to the inner surface of the lamp tube. A bendable circuit sheet closely mounted to the inner surface of the lamp tube is desirable in some cases. In addition, using fewer layers of the bendable circuit sheet improves the heat dissipation, lowering the material cost, and is more environmental

friendly, and provides the opportunity to increase the flexible effect.

[0075] Nevertheless, the bendable circuit sheet is not limited to being one-layered or two-layered; in other embodiments, the bendable circuit sheet may include multiple layers of the wiring layers 2a and multiple layers of the dielectric layers 2b, in which the dielectric layers 2b and the wiring layers 2a are sequentially stacked in a staggered manner, respectively. These stacked layers may be between the outermost wiring layer 2a (with respect to the inner circumferential surface of the lamp tube), which has the LED light source 202 disposed thereon, and the inner circumferential surface of the lamp tube, and may be electrically connected to the power supply 5 (as shown in Fig. 1.) Moreover, in some embodiments, the length of the bendable circuit sheet (e.g., the length along a surface of the bendable circuit sheet from one end of the circuit sheet to a second end of the circuit sheet) (or an axial projection of the length of the bendable circuit sheet) is greater than the length of the lamp tube (or an axial projection of the length of the lamp tube), or at least greater than a central portion of the lamp tube between two transition regions (e.g., where the circumference of the lamp tube narrows) on either end. For example, the length following along the contours of one surface of the bendable circuit sheet (e.g., a top surface of the circuit sheet) may be longer than the length from one terminal end to an opposite terminal end of the lamp tube. Also, a length along a straight line that extends in the same direction as the direction in which the lamp tube extends, from a first end of the bendable circuit sheet to a second, opposite end of the bendable circuit sheet, may be longer than the length along the same straight line of the lamp tube.

[0076] Referring to Fig. 7, in one embodiment, an LED light strip 2 includes a bendable circuit sheet having in sequence a first wiring layer 2a, a dielectric layer 2b, and a second wiring layer 2c. In one example, the thickness of the second wiring layer 2c (e.g., in a direction in which the layers 2a through 2c are stacked) is greater than that of the first wiring layer 2a, and the length of the LED light strip 2 (or an axial projection of the length of the LED light strip 2) is greater than that of a lamp tube 1, or at least greater than a central portion of the lamp tube between two transition regions (e.g., where the circumference of the lamp tube narrows) on either end. The end

region of the LED light strip 2 extending beyond the end portion of the lamp tube 1 without having a light source 202 disposed thereon is formed with two separate through holes 203 and 204 to respectively electrically communicate the first wiring layer 2a and the second wiring layer 2c. The through holes 203 and 204 are not in communication with each other to avoid short.

[0077] In this way, the greater thickness of the second wiring layer 2c allows the second wiring layer 2c to support the first wiring layer 2a and the dielectric layer 2b, and meanwhile allows the LED light strip 2 to be mounted onto the inner circumferential surface without being liable to shift or deform, and thus the yield rate of product can be improved. In addition, the first wiring layer 2a and the second wiring layer 2c are in electrical communication such that the circuit layout of the first wiring later 2a can be extended downward to the second wiring layer 2c to reach the circuit layout of the entire LED light strip 2. Moreover, since the circuit layout becomes two-layered, the area of each single layer and therefore the width of the LED light strip 2 can be reduced such that more LED light strips 2 can be put on a production line to increase productivity.

[0078] Furthermore, in some embodiments, the first wiring layer 2a and the second wiring layer 2c of the end region of the LED light strip 2 that extends beyond the end portion of the lamp tube 1 without disposition of the light source 202 can be used to accomplish the circuit layout of a power supply module so that the power supply module can be directly disposed on the bendable circuit sheet of the LED light strip 2.

[0079] In a case where two ends of the LED light strip 2 are detached from the inner surface of the lamp tube 1 and where the LED light strip 2 is connected to the power supply 5 via wire-bonding, certain movements in subsequent transportation are likely to cause the bonded wires to break. Therefore, a desirable option for the connection between the LED light strip 2 and the power supply 5 (as shown in Fig. 1) could be soldering. Specifically, referring to Fig. 1, the ends of the LED light strip 2 including the bendable circuit sheet are arranged to pass over the strengthened transition region of a lamp tube, and to be directly solder bonded to an output terminal of the power supply 5. This may improve product quality by avoiding using wires and/or wire bonding. As discussed herein, a transition region of the lamp tube refers to regions

outside a central portion of the lamp tube and inside terminal ends of the lamp tube. For example, a central portion of the lamp tube may have a constant diameter, and each transition region between the central portion and a terminal end of the lamp tube may have a changing diameter (e.g., at least part of the transition region may become more narrow moving in a direction from the central portion to the terminal end of the lamp tube).

[0080] Referring to Fig. 3A, an output terminal of a printed circuit board of the power supply 5 may have soldering pads "a" (as shown in Fig. 1 as well) provided with an amount of solder (e.g., tin solder) with a thickness sufficient to later form a solder joint "g" (or a solder ball "g"). Correspondingly, the ends of the LED light strip 2 may have soldering pads "b" (as shown in Fig. 1 as well). The soldering pads "a" on the output terminal of the printed circuit board of the power supply 5 are soldered to the soldering pads "b" on the LED light strip 2 via the tin solder on the soldering pads "a". The soldering pads "a" and the soldering pads "b" may be face to face during soldering such that the connection between the LED light strip 2 and the printed circuit board of the power supply 5 may be the firmest. However, this kind of soldering typically includes a thermo-compression head pressing on the rear surface of the LED light strip 2 and heating the tin solder, i.e., the LED light strip 2 intervenes between the thermo-compression head and the tin solder, and therefore may cause reliability problems. In some embodiments, a through hole may be formed in each of the soldering pads "b" on the LED light strip 2 to allow the soldering pads "b" to overlay the soldering pads "a" without being face-to-face (e.g., both soldering pads "a" and soldering pads "b" can have exposed surfaces that face the same direction) and the thermo-compression head directly presses tin solders on the soldering pads "a" on surface of the printed circuit board of the power supply 5 when the soldering pads "a" and the soldering pads "b" are vertically aligned. This example provides a simple process for manufacturing.

[0081] Referring again to Fig. 3A, two ends of the LED light strip 2 detached from the inner surface of the lamp tube 1 (as shown in Fig. 7) are formed as freely extending portions 21 (as shown in Figs. 1 and 7 as well), while most of the LED light strip 2 is attached and secured to the inner surface of the lamp tube. One of the freely

extending portions 21 has the soldering pads "b" as mentioned above. Upon assembling of the LED tube lamp, the freely extending end portions 21 along with the soldered connection of the printed circuit board of the power supply 5 and the LED light strip 2 would be coiled, curled up or deformed to be fittingly accommodated inside the lamp tube as shown in Fig. 1. When the bendable circuit sheet of the LED light strip 2 includes in sequence the first wiring layer 2a, the dielectric layer 2b, and the second wiring layer 2c as shown in Fig. 7, the freely extending end portions 21, which are the end regions of the LED light strip 2 extending beyond the lamp tube without disposition of the light sources 202, can be used to accomplish the connection between the first wiring layer 2a and the second wiring layer 2c and arrange the circuit layout of the power supply 5. As described above, the freely extending portions 21 may be different from a fixed portion of the LED light strip 2 in that the fixed portion may conform to the shape of the inner surface of the lamp tube and may be fixed thereto, while the freely extending portion 21 may have a shape that does not conform to the shape of the lamp tube. As shown in Fig. 1, the freely extending portion 21 may be bent away from the lamp tube. For example, there may be a space between an inner surface of the lamp tube and the freely extending portion 21.

[0082] In designing the conductive pin or external connection terminal in the LED tube lamp, various arrangements of pins may be provided in one end or both ends of the LED tube lamp according to exemplary embodiments. For example, two pins may be provided in one end and no pins may be provided on the other end. Alternatively, in some embodiments, two pins in corresponding ends of two ends of the LED tube lamp, or four pins in corresponding ends of two ends of the LED tube lamp may be provided. When a dual-end power supply between two ends of the LED tube lamp is utilized to provide power to the LED tube lamp, at least one pin of each end of the LED tube lamp is used to receive the external driving signal from the power supply.

[0083] Fig. 3B is a block diagram illustrating leads that are disposed between two end caps of an LED tube lamp according to some exemplary embodiments.

[0084] Referring to Fig. 3B, in some embodiments, the LED tube lamp includes a lamp tube (not shown in Fig. 3B), end caps (not shown in Fig. 3B), a light strip 2, short circuit boards 253 (also referred to as right end short circuit board 253 and left end

short circuit board 253) respectively provided at two ends of the lamp tube, and an inductive element 526. Each of the lamp tube's two ends may have at least one pin or external connection terminal for receiving the external driving signal. The end caps are disposed respectively at the two ends of the lamp tube, and (at least partial electronic components of) the short circuit boards 253 shown as located respectively at the left and right ends of the lamp tube in Fig. 3B may be disposed respectively in the end caps. The short circuit boards may be, for example, a rigid circuit board such as depicted in and described in connection with Fig. 1 and the various other rigid circuit boards described herein. For example, these circuit boards may include mounted thereon one or more power supply components for generating and/or converting power to be used to light the LED light sources on the light strip 2. The light strip 2 is disposed in the lamp tube and includes an LED module, which includes an LED unit 632.

[0085] For an LED tube lamp, such as an 8 ft. 42W LED tube lamp, to receive a dual-end power supply between two ends of the LED tube lamp, two (partial) power-supply circuits (each having a power rating of e.g. 21W) are typically disposed respectively in the two end caps of the lamp tube, and a lead (typically referred to as lead Line or Neutral) disposed between two end caps of the lamp tube (e.g., between two pins or external connection terminals at respective end caps of the lamp tube) and as an input signal line may be needed. The lead Line may be disposed along an LED light strip that may include, e.g., a bendable circuit sheet or flexible circuit board, for receiving and transmitting an external driving signal from the power supply. This lead Line is distinct from two leads typically referred to as LED+ and LED- that are respectively connected to a positive electrode and a negative electrode of an LED unit in the lamp tube. This lead Line is also distinct from a Ground lead which is disposed between respective ground terminals of the LED tube lamp. Because the lead Line is typically disposed along the light strip, and because parasitic capacitance(s) (e.g., about 200pF) may be caused between the lead Line and the lead LED+ due to their close proximity to each other, some high frequency signals (not the intended frequency range of signal for supplying power to the LED module) passing through the lead LED+ will be reflected to the lead Line through the parasitic

capacitance(s) and then can be detected there as undesirable EMI effects. The unfavorable EMI effects may lower or degrade the quality of power transmission in the LED tube lamp.

[0086] Again referring to Fig. 3B, in some embodiments, the right and left short circuit boards 253 are electrically connected to the light strip 2. In some embodiments, the electrical connection (such as through soldering or bond pad(s)) between the short circuit boards 253 and the light strip 2 may comprise a first terminal (denoted by "L"), a second terminal (denoted by "+" or "LED+"), a third terminal (denoted by "-" or "LED-"), and a fourth terminal (denoted by "GND" or "ground"). The light strip 2 includes the first through fourth terminals at a first end of the light strip 2 adjacent to the right end short circuit board 253 near one end cap of the lamp tube and includes the first through fourth terminals at a second end, opposite to the first end, of the light strip 2 adjacent to the left end short circuit board 253 near the other end cap of the lamp tube. The right end short circuit board 253 also includes the first through fourth terminals to respectively connect to the first through fourth terminals of the light strip 2 at the first end of the light strip 2. The left end short circuit board 253 also includes the first through fourth terminals to respectively connect to the first through fourth terminals of the light strip 2 at the second end of the light strip 2. For example, the first terminal L is utilized to connect a lead (typically referred to as Line or Neutral) for connecting both of the at least one pin of each of the two ends of the lamp tube; the second terminal LED+ is utilized to connect each of the short circuit boards 253 to the positive electrode of the LED unit 632 of the LED module included in the light strip 2. The third terminal LED- is utilized to connect each of the short circuit boards 253 to the negative electrode of the LED unit 632 of the LED module included in the light strip 2. The fourth terminal GND is utilized to connect to a reference potential. Preferably and typically, the reference potential is defined as the electrical potential of ground. Therefore, the fourth terminal is utilized for a grounding purpose of the power supply module of the LED tube lamp.

[0087] To address the undesirable EMI effects mentioned above caused by parasitic capacitance(s) between the lead Line and the lead LED+, inductive element 526 disposed in the Ground lead serves to reduce or prevent the EMI effects by

blocking the forming of a complete circuit between the lead LED+ and the Ground lead for the high frequency signals mentioned above to pass through, since at these high frequencies inductive element 526 behaves like an open circuit. When the complete circuit is prevented or blocked by inductive element 526, the high frequency signals will be prevented on the lead LED+ and therefore will not be reflected to the lead Line, thus preventing the undesirable EMI effects. In some embodiments, the inductive element 526 is connected between two of the fourth terminals respectively of the right end and left end short circuit boards 253 at the two ends of the lamp tube. In some embodiments, the inductive element 526 may comprise an inductor such as a choke inductor or a dual-inline-package inductor capable of achieving a function of eliminating or reducing the above-mentioned EMI effects of the lead ("Line") disposed along the light strip 2 between two of the first terminals ("L") respectively at two ends of the lamp tube. Therefore, this function can improve signal transmission (which may include transmissions through leads "L", "LED+", and "LED-") of the power supply in the LED tube lamp, and thus the qualities of the LED tube lamp. Therefore, the LED tube lamp comprising the inductive element 526 may effectively reduce EMI effects of the lead "L" or "Line". Moreover, such an LED tube lamp may further comprise an installation detection circuit or module, which is described below with reference to Figs. 15, for detecting whether or not the LED tube lamp is properly installed on a lamp socket.

[0088] Referring to Figs. 5 and 6, in another embodiment, the LED light strip and the power supply may be connected by utilizing a circuit board assembly 25 configured with a power supply module 250 instead of solder bonding as described previously. The circuit board assembly 25 has a long circuit sheet 251 and a short circuit board 253 that are adhered to each other with the short circuit board 253 being adjacent to the side edge of the long circuit sheet 251. The short circuit board 253 may be provided with the power supply module 250 to form the power supply. The short circuit board 253 is stiffer or more rigid than the long circuit sheet 251 to be able to support the power supply module 250.

[0089] The long circuit sheet 251 may be the bendable circuit sheet of the LED light strip 2 including a wiring layer 2a as shown in Fig. 2. The wiring layer 2a of the LED

light strip 2 and the power supply module 250 may be electrically connected in various manners depending on the demand in practice. As shown in Fig. 5, the power supply module 250 and the long circuit sheet 251 having the wiring layer 2a on surface are on the same side of the short circuit board 253 such that the power supply module 250 is directly connected to the long circuit sheet 251. As shown in Fig. 6, alternatively, the power supply module 250 and the long circuit sheet 251 including the wiring layer 2a on surface are on opposite sides of the short circuit board 253 such that the power supply module 250 is directly connected to the short circuit board 253 and indirectly connected to the wiring layer 2a of the LED light strip 2 by way of the short circuit board 253.

[0090] The power supply module 250 and power supply 5 described above may include various elements for providing power to the LED light strip 2. For example, they may include power converters or other circuit elements for providing power to the LED light strip 2.

[0091] Fig. 4A is a perspective view of an exemplary bendable circuit sheet 200 and a printed circuit board 420 of a power supply 400 soldered to each other. Fig. 4B to Fig. 4D are diagrams illustrating an exemplary soldering process of the bendable circuit sheet 200 and the printed circuit board 420 of the power supply 400. In an embodiment, the bendable circuit sheet 200 and the freely extending end portion have the same structure. The freely extending end portion are the portions of two opposite ends of the bendable circuit sheet 200 and are utilized for being connected to the printed circuit board 420. The bendable circuit sheet 200 and the power supply 400 are electrically connected to each other by soldering. The bendable circuit sheet 200 comprises a circuit layer 200a and a circuit protection layer 200c over a side of the circuit layer 200a. Moreover, the bendable circuit sheet 200 comprises two opposite surfaces which are a first surface 2001 and a second surface 2002. The first surface 2001 is the one on the circuit layer 200a and away from the circuit protection layer 200c. The second surface 2002 is the other one on the circuit protection layer 200c and away from the circuit layer 200a. Several LED light sources 202 are disposed on the first surface 2001 and are electrically connected to circuits of the circuit layer 200a. The circuit protection layer 200c is made, for example, by polyimide

(PI) having less thermal conductivity but being beneficial to protect the circuits. The first surface 2001 of the bendable circuit sheet 200 comprises soldering pads "b" (or referred as first soldering pads). Soldering material "g" can be placed on the soldering pads "b". In one embodiment, the bendable circuit sheet 200 further comprises a notch "f". The notch "f" is disposed on an edge of the end of the bendable circuit sheet 200 soldered to the printed circuit board 420 of the power supply 400. In some embodiments instead of a notch, a hole near the edge of the end of the bendable circuit sheet 200 may be used, which may thus provide additional contact material between the printed circuit board 420 and the bendable circuit sheet 200, thereby providing a stronger connection. The printed circuit board 420 comprises a power circuit layer 420a and soldering pads "a". Moreover, the printed circuit board 420 comprises two opposite surfaces which are a first surface (or a top surface) 421 and a second surface (or a bottom surface) 422. The second surface 422 is the one on the power circuit layer 420a. The soldering pads "a" are respectively disposed on the first surface 421 (those soldering pads "a" on the first surface 421 may be referred as second soldering pads) and the second surface 422 (those soldering pads "a" on the second surface 422 may be referred as third soldering pads). The soldering pads "a" on the first surface 421 are corresponding to those on the second surface 422. Soldering material "g" can be placed on the soldering pad "a". In one embodiment, considering the stability of soldering and the optimization of automatic process, the bendable circuit sheet 200 is disposed below the printed circuit board 420 (the direction is referred to Fig. 4B). For example, the first surface 2001 of the bendable circuit sheet 200 is connected to the second surface 422 of the printed circuit board 420. Also, as shown, the soldering material "g" can contact, cover, and be soldered to a top surface of the bendable circuit sheet 200 (e.g., first surface 2001), end side surfaces of soldering pads "a," soldering pad "b," and power circuit layer 420a formed at an edge of the printed circuit board 420, and a top surface of soldering pad "a" at the top surface 421 of the printed circuit board 420. In addition, the soldering material "g" can contact side surfaces of soldering pads "a," soldering pad "b," and power circuit layer 420a formed at a hole in the printed circuit board 420 and/or at a hole or notch in bendable circuit sheet 200. The soldering material may therefore form a

bump-shaped portion covering portions of the bendable circuit sheet 200 and the printed circuit board 420, and a rod-shaped portion passing through the printed circuit board 420 and through a hole or notch in the bendable circuit sheet 200. The two portions (e.g., bump-shaped portion and rod-shaped portion) may serve as a rivet, for maintaining a strong connection between the bendable circuit sheet 200 and the printed circuit board 420.

[0092] As shown in Fig. 4C and Fig. 4D, in an exemplary soldering process of the bendable circuit sheet 200 and the printed circuit board 420, the circuit protection layer 200c of the bendable circuit sheet 200 is placed on a supporting table 42 (i.e., the second surface 2002 of the bendable circuit sheet 200 contacts the supporting table 42) in advance of soldering. The soldering pads "a" on the second surface 422 of the printed circuit board 420 contact the soldering pads "b" on the first surface 2001 of the bendable circuit sheet 200. And then a heating head 41 presses on a portion of soldering material "g" where the bendable circuit sheet 200 and the printed circuit board 420 are soldered to each other. When soldering, the soldering pads "b" on the first surface 2001 of the bendable circuit sheet 200 contact the soldering pads "a" on the second surface 422 of the printed circuit board 420, and the soldering pads "a" on the first surface 421 of the printed circuit board 420 contact the soldering material "g," which is pressed on by the heating head 41. Under the circumstance, the heat from the heating head 41 can transmit through the soldering pads "a" on the first surface 421 of the printed circuit board 420 and the soldering pads "a" on the second surface 422 of the printed circuit board 420 to the soldering pads "b" on the first surface 2001 of the bendable circuit sheet 200. The transmission of the heat between the heating heads 41 and the soldering pads "a" and "b" won't be affected by the circuit protection layer 200c which has relatively less thermal conductivity, since the circuit protection layer 200c is not between the heating head 41 and the circuit layer 200a. Consequently, the efficiency and stability regarding the connections and soldering process of the soldering pads "a" and "b" of the printed circuit board 420 and the bendable circuit sheet 200 can be improved.

[0093] As shown in the exemplary embodiment of Fig. 4C, the printed circuit board 420 and the bendable circuit sheet 200 are firmly connected to each other by the

soldering material "g". Components between the virtual line M and the virtual line N of Fig. 4C from top to bottom are the soldering pads "a" on the first surface 421 of printed circuit board 420, the power circuit layer 420a, the soldering pads "a" on the second surface 422 of printed circuit board 420, the soldering pads "b" on the first surface 2001 of bendable circuit sheet 200, the circuit layer 200a of the bendable circuit sheet 200, and the circuit protection layer 200c of the bendable circuit sheet 200. The connection of the printed circuit board 420 and the bendable circuit sheet 200 are firm and stable. The soldering material "g" may extend higher than the soldering pads "a" on the first surface 421 of printed circuit board 420 and may fill in other spaces, as described above.

[0094] In other embodiments, an additional circuit protection layer (e.g., PI layer) can be disposed over the first surface 2001 of the circuit layer 200a. For example, the circuit layer 200a may be sandwiched between two circuit protection layers, and therefore the first surface 2001 of the circuit layer 200a can be protected by the circuit protection layer. A part of the circuit layer 200a (the part having the soldering pads "b") is exposed for being connected to the soldering pads "a" of the printed circuit board 420. Other parts of the circuit layer 200a are exposed by the additional circuit protection layer so they can connect to LED light sources 202. Under these circumstances, a part of the bottom of each LED light source 202 contacts the circuit protection layer on the first surface 2001 of the circuit layer 200a, and another part of the bottom of the LED light source 202 contacts the circuit layer 200a.

[0095] According to the exemplary embodiments shown in Fig. 4A to Fig. 4D, the printed circuit board 420 comprises through holes "h" passing through the soldering pads "a". In an automatic soldering process, when the heating head 41 automatically presses the printed circuit board 420, the soldering material "g" on the soldering pads "a" can be pushed into the through holes "h" by the heating head 41 accordingly. As a result, a soldered connection may be formed as shown in Figs. 4C and 4D.

[0096] Fig. 8A is a block diagram of a system including an LED tube lamp including a power supply module according to certain embodiments. Referring to Fig. 8A, an alternating current (AC) power supply 508 is used to supply an AC supply signal, and may be an AC powerline with a voltage rating, for example, in 100-277V and a

frequency rating, for example, of 50 Hz or 60 Hz. A lamp driving circuit 505 receives the AC supply signal from the AC power supply 508 and then converts it into an AC driving signal. The power supply module and power supply 508 described above may include various elements for providing power to the LED light strip 2. For example, they may include power converters or other circuit elements for providing power to the LED light strip 2. In some embodiments, the power supply 508 and the lamp driving circuit 505 are outside of the LED tube lamp. For example, the lamp driving circuit 505 may be part of a lamp socket or lamp holder into which the LED tube lamp is inserted. The lamp driving circuit 505 could be an electronic ballast and may be used to convert the signal of commercial electricity into high-frequency and high-voltage AC driving signal. The common types of electronic ballast, such as instant-start electronic ballast, program-start electronic ballast, and rapid-start electronic ballast, can be applied to the LED tube lamp. In some embodiments, the voltage of the AC driving signal is bigger than 300V and in some embodiments 400-700V with frequency being higher than 10 kHz and in some embodiments 20-50 kHz. An LED tube lamp 500 receives the AC driving signal from the lamp driving circuit 505 and is thus driven to emit light. In the present embodiment, the LED tube lamp 500 is in a driving environment in which it is power-supplied at its one end cap having two conductive pins 501 and 502, which are used to receive the AC driving signal. The two pins 501 and 502 may be electrically coupled to, either directly or indirectly, the lamp driving circuit 505.

[0097] In some embodiments, the lamp driving circuit 505 may be omitted and is therefore depicted by a dotted line. In certain embodiments, if the lamp driving circuit 505 is omitted, the AC power supply 508 is directly coupled to the pins 501 and 502, which then receive the AC supply signal as the AC driving signal.

[0098] In some embodiments, the LED tube lamp may be power-supplied at its both end caps respectively having two conductive pins, which are coupled to the lamp driving circuit to concurrently receive the AC driving signal. However, in certain embodiments, referring to Fig. 8B, each end cap of the LED tube lamp 500 could have only one conductive pin for receiving the AC driving signal. For example, it is not required to have two conductive pins used in each end cap for the purpose of passing electricity through the both ends of the LED tube lamp. Compared to Fig. 8A, the

conductive pins 501 and 502 in Fig. 8B are correspondingly configured at the both end caps of the LED tube lamp 500, and the AC power supply 508 and the lamp driving circuit 505 are the same as those mentioned above.

[0099] Fig. 8C is a block diagram of an LED lamp according to one embodiment. Referring to Fig. 8C, the power supply module of the LED lamp includes a rectifying circuit 510, a filtering circuit 520, and may further include some parts of an LED lighting module 530. The rectifying circuit 510 is coupled to two pins 501 and 502 to receive and then rectify an external driving signal, so as to output a rectified signal at two rectifying output terminals 511 and 512. In some embodiments, the external driving signal may be the AC driving signal or the AC supply signal described with reference to Figs. 8A and 8B. In some embodiments, the external driving signal may be a direct current (DC) signal without altering the LED tube lamp. The filtering circuit 520 is coupled to the rectifying circuit for filtering the rectified signal to produce a filtered signal. For instance, the filtering circuit 520 is coupled to the rectifying circuit output terminals 511 and 512 to receive and then filter the rectified signal, so as to output a filtered signal at two filtering output terminals 521 and 522. The LED lighting module 530 is coupled to the filtering circuit 520 to receive the filtered signal for emitting light. For instance, the LED lighting module 530 may include a circuit coupled to the filtering output terminals 521 and 522 to receive the filtered signal and thereby to drive an LED unit (not shown) in the LED lighting module 530 to emit light. Details of these operations are described below in accordance with certain embodiments.

[00100] Although there are two rectifying output terminals 511 and 512 and two filtering output terminals 521 and 522 in the embodiments of these Figs., in practice the number of ports or terminals for coupling between the rectifying circuit 510, the filtering circuit 520, and the LED lighting module 530 may be one or more depending on the needs of signal transmission between the circuits or devices.

[00101] In addition, the power supply module of the LED lamp described in Fig. 8C, and embodiments of a power supply module of an LED lamp described below, may each be used in the LED tube lamp 500 in Figs. 8A and 8B, and may instead be used in any other type of LED lighting structure having two conductive pins used to conduct power, such as LED light bulbs, personal area lights (PAL), plug-in LED

lamps with different types of bases (such as types of PL-S, PL-D, PL-T, PL-L, etc.), etc. Further, the implementation for LED light bulbs may provide better effects on protecting from electric shock as combining this invention and the structures disclosed in EU patent application WO2016045631.

[00102] Fig. 9 is a schematic diagram of a rectifying circuit according to an embodiment. Referring to Fig. 9, a rectifying circuit 610, i.e. a bridge rectifier, includes four rectifying diodes 611, 612, 613, and 614, configured to full-wave rectify a received signal. The diode 611 has an anode connected to the output terminal 512, and a cathode connected to the pin 502. The diode 612 has an anode connected to the output terminal 512, and a cathode connected to the pin 501. The diode 613 has an anode connected to the pin 502, and a cathode connected to the output terminal 511. The diode 614 has an anode connected to the pin 501, and a cathode connected to the output terminal 511.

[00103] When the pins 501 and 502 receive an AC signal, the rectifying circuit 610 operates as follows. During the connected AC signal's positive half cycle, the AC signal is input through the pin 501, the diode 614, and the output terminal 511 in sequence, and later output through the output terminal 512, the diode 611, and the pin 502 in sequence. During the connected AC signal's negative half cycle, the AC signal is input through the pin 502, the diode 613, and the output terminal 511 in sequence, and later output through the output terminal 512, the diode 612, and the pin 501 in sequence. Therefore, during the connected AC signal's full cycle, the positive pole of the rectified signal produced by the rectifying circuit 610 keeps at the output terminal 511, and the negative pole of the rectified signal remains at the output terminal 512. Accordingly, the rectified signal produced or output by the rectifying circuit 610 is a full-wave rectified signal.

[00104] When the pins 501 and 502 are coupled to a DC power supply to receive a DC signal, the rectifying circuit 610 operates as follows. When the pin 501 is coupled to the positive end of the DC power supply and the pin 502 to the negative end of the DC power supply, the DC signal is input through the pin 501, the diode 614, and the output terminal 511 in sequence, and later output through the output terminal 512, the diode 611, and the pin 502 in sequence. When the pin 501 is coupled to the

negative end of the DC power supply and the pin 502 to the positive end of the DC power supply, the DC signal is input through the pin 502, the diode 613, and the output terminal 511 in sequence, and later output through the output terminal 512, the diode 612, and the pin 501 in sequence. Therefore, no matter what the electrical polarity of the DC signal is between the pins 501 and 502, the positive pole of the rectified signal produced by the rectifying circuit 610 keeps at the output terminal 511, and the negative pole of the rectified signal remains at the output terminal 512.

[00105] Therefore, the rectifying circuit 610 in this embodiment can output or produce a proper rectified signal regardless of whether the received input signal is an AC or DC signal.

[00106] Fig. 10A is a block diagram of the filtering circuit according to an embodiment. A rectifying circuit 510 is shown in Fig. 10A for illustrating its connection with other components, without intending a filtering circuit 520 to include the rectifying circuit 510. Referring to Fig. 10A, the filtering circuit 520 includes a filtering unit 523 coupled to two rectifying output terminals 511 and 512 to receive and to filter out ripples of a rectified signal from the rectifying circuit 510. Accordingly, the waveform of a filtered signal is smoother than that of the rectified signal. The filtering circuit 520 may further include another filtering unit 524 coupled between a rectifying circuit and a pin correspondingly, for example, between the rectifying circuit 510 and the pin 501, the rectifying circuit 510 and the pin 502, the rectifying circuit 540 and the pin 503, and/or the rectifying circuit 540 and the pin 504. The filtering unit 524 is used to filter a specific frequency, for example, to filter out a specific frequency of an external driving signal. In this embodiment, the filtering unit 524 is coupled between the rectifying circuit 510 and the pin 501. The filtering circuit 520 may further include another filtering unit 525 coupled between one of the pins 501 and 502 and one of the diodes of the rectifying circuit 510, or between one of the pins 503 and 504 and one of the diodes of the rectifying circuit 540 to reduce or filter out electromagnetic interference (EMI). In this embodiment, the filtering unit 525 is coupled between the pin 501 and one of diodes (not shown in Fig. 10A) of the rectifying circuit 510. Since the filtering units 524 and 525 may be present or omitted depending on actual circumstances of their uses, they are depicted by a dotted line in Fig. 10A.

[00107] Fig. 10B is a schematic diagram of the filtering unit according to an embodiment. Referring to Fig. 10B, a filtering unit 623 includes a capacitor 625 having an end coupled to the output terminal 511 and a filtering output terminal 521 and the other end thereof coupled to the output terminal 512 and a filtering output terminal 522, and is configured to low-pass filter a rectified signal from the output terminals 511 and 512, so as to filter out high-frequency components of the rectified signal and thereby output a filtered signal at the filtering output terminals 521 and 522.

[00108] Fig. 10C is a schematic diagram of the filtering unit according to an embodiment. Referring to Fig. 10C, a filtering unit 723 includes a pi filter circuit including a capacitor 725, an inductor 726, and a capacitor 727. As is well known, a pi filter circuit looks like the symbol π in its shape or structure. The capacitor 725 has an end connected to the output terminal 511 and coupled to the filtering output terminal 521 through the inductor 726, and has another end connected to the output terminal 512 and the filtering output terminal 522. The inductor 726 is coupled between output terminal 511 and the filtering output terminal 521. The capacitor 727 has an end connected to the filtering output terminal 521 and coupled to the output terminal 511 through the inductor 726, and has another end connected to the output terminal 512 and the filtering output terminal 522.

[00109] As seen between the output terminals 511 and 512 and the filtering output terminals 521 and 522, the filtering unit 723 compared to the filtering unit 623 in Fig. 10B additionally has an inductor 726 and a capacitor 727, which perform the function of low-pass filtering like the capacitor 725 does. Therefore, the filtering unit 723 in this embodiment compared to the filtering unit 623 in Fig. 10B has a better ability to filter out high-frequency components to output a filtered signal with a smoother waveform.

[00110] The inductance values of the inductor 726 in the embodiments mentioned above are chosen in the range of, for example in some embodiments, about 10 nH to 10 mH. And the capacitance values of the capacitors 625, 725, and 727 in the embodiments stated above are chosen in the range of, for example in some embodiments, about 100 pF to 1 uF.

[00111] Fig. 11A is a schematic diagram of an LED module according to an embodiment. Referring to Fig. 11A, an LED module 630 has an anode connected to a filtering output terminal 521, a cathode connected to a filtering output terminal 522, and includes at least one LED unit 632, such as the light source mentioned above. When two or more LED units are included, they are connected in parallel. The anode of each LED unit 632 is connected to the anode of LED module 630 to couple with the filtering output terminal 521, and the cathode of each LED unit 632 is connected to the cathode of LED module 630 to couple to the filtering output terminal 522. Each LED unit 632 includes at least one LED 631. When multiple LEDs 631 are included in an LED unit 632, they are connected in series with the anode of the first LED 631 connected to the anode of this LED unit 632 and the cathode of the first LED 631 connected to the next or second LED 631. And the anode of the last LED 631 in this LED unit 632 is connected to the cathode of a previous LED 631 and the cathode of the last LED 631 connected to the cathode of this LED unit 632.

[00112] In some embodiments, the LED module 630 may produce a current detection signal S531 reflecting the magnitude of current through the LED module 630 and being used for controlling or detecting the LED module 630.

[00113] Fig. 11B is a schematic diagram of an LED module according to an exemplary embodiment. Referring to Fig. 11B, an LED module 630 has an anode connected to a filtering output terminal 521, a cathode connected to a filtering output terminal 522, and includes at least two LED units 732 with the anode of each LED unit 732 connected to the anode of LED module 630 and the cathode of each LED unit 732 connected to the cathode of LED module 630. Each LED unit 732 includes at least two LEDs 731 connected in the same way as those described in Fig. 11A. For example, the anode of the first LED 731 in an LED unit 732 is connected to the anode of this LED unit 732, the cathode of the first LED 731 is connected to the anode of the next or second LED 731, and the cathode of the last LED 731 is connected to the cathode of this LED unit 732. Further, LED units 732 in an LED module 630 are connected to each other in this embodiment. All of the n-th LEDs 731 in the related LED units 732 thereof are connected by their anodes and cathodes, such as those shown in Fig. 8B but not limit to, where n is a positive integer. In this way, the LEDs in

the LED module 630 of this embodiment are connected in the form of a mesh.

[00114] In some embodiments, the LED lighting module 530 in the above embodiments includes the LED module 630, but doesn't include a driving circuit for the LED module 630.

[00115] Also, the LED module 630 in this embodiment may produce a current detection signal S531 reflecting the magnitude of current through the LED module 630 and being used for controlling or detecting the LED module 630.

[00116] In some embodiments, the number of LEDs 731 included by an LED unit 732 is in the range of 15-25, and may be in some embodiments in the range of 18-22.

[00117] Fig. 11C is a plan view of a circuit layout of the LED module according to an embodiment. Referring to Fig. 11C, in this embodiment, multiple LEDs 831 are connected in the same way as described in Fig. 11B, and three LED units are assumed in the LED module 630 and described as follows for illustration. A positive conductive line 834 and a negative conductive line 835 are to receive a driving signal for supplying power to the LEDs 831. For example, the positive conductive line 834 may be coupled to the filtering output terminal 521 of the filtering circuit 520 described above, and the negative conductive line 835 coupled to the filtering output terminal 522 of the filtering circuit 520 to receive a filtered signal. For the convenience of illustration, all three of the n-th LEDs 831 in the three related LED units thereof are grouped as an LED set 833 in Fig. 11C.

[00118] The positive conductive line 834 connects the three first LEDs 831 of the leftmost three related LED units thereof, that is, connects the anodes on the left sides of the three first LEDs 831 as shown in the leftmost LED set 833 of Fig. 11C. The negative conductive line 835 connects the three last LEDs 831 of the rightmost three corresponding LED units thereof, that is, connects the cathodes on the right sides of the three last LEDs 831 as shown in the rightmost LED set 833 of Fig. 11C. The cathodes of the three first LEDs 831, the anodes of the three last LEDs 831, and the anodes and cathodes of all the remaining LEDs 831 are connected by conductive lines or parts 839.

[00119] For example, the anodes of the three LEDs 831 in the leftmost LED set

833 may be connected together by the positive conductive line 834, and their cathodes may be connected together by a leftmost conductive part 839. The anodes of the three LEDs 831 in the second, next-leftmost LED set 833 are also connected together by the leftmost conductive part 839, whereas their cathodes are connected together by a second, next-leftmost conductive part 839. Since the cathodes of the three LEDs 831 in the leftmost LED set 833 and the anodes of the three LEDs 831 in the second, next-leftmost LED set 833 are connected together by the same leftmost conductive part 839, the cathode of the first LED 831 in each of the three LED units is connected to the anode of the next or second LED 831. As for the remaining LEDs 831 are also connected in the same way. Accordingly, all the LEDs 831 of the three LED units are connected to form the mesh as shown in Fig. 11B.

[00120] In this embodiment, the length 836 of a portion of each conductive part 839 that connects to the anode of an LED 831 is smaller than the length 837 of another portion of each conductive part 839 that connects to the cathode of an LED 831. This makes the area of the latter portion connecting to the cathode larger than that of the former portion connecting to the anode. Moreover, the length 837 may be smaller than a length 838 of a portion of each conductive part 839 that connects the cathode of an LED 831 and the anode of the next LED 831 in two adjacent LED sets 833. This makes the area of the portion of each conductive part 839 that connects a cathode and an anode larger than the area of any other portion of each conductive part 839 that connects to only a cathode or an anode of an LED 831. Due to the length differences and area differences, this layout structure improves heat dissipation of the LEDs 831.

[00121] In some embodiments, the positive conductive line 834 includes a lengthwise portion 834a, and the negative conductive line 835 includes a lengthwise portion 835a, which are conducive to make the LED module have a positive "+" connective portion and a negative "-" connective portion at each of the two ends of the LED module, as shown in Fig. 11C. Such a layout structure allows for coupling any of other circuits of the power supply module of the LED lamp, including e.g. the filtering circuit 520 and the rectifying circuits 510 and 540, to the LED module through the positive connective portion and/or the negative connective portion at each or both

ends of the LED lamp. Thus the layout structure increases the flexibility in arranging actual circuits in the LED lamp.

[00122] Fig. 11D is a plan view of a circuit layout of the LED module according to another embodiment. Referring to Fig. 11D, in this embodiment, multiple LEDs 931 are connected in the same way as described in Fig. 11A, and three LED units each including 7 LEDs 931 are assumed in the LED module 630 and described as follows for illustration. A positive conductive line 934 and a negative conductive line 935 are to receive a driving signal for supplying power to the LEDs 931. For example, the positive conductive line 934 may be coupled to the filtering output terminal 521 of the filtering circuit 520 described above, and the negative conductive line 935 is coupled to the filtering output terminal 522 of the filtering circuit 520, so as to receive a filtered signal. For the convenience of illustration, all seven LEDs 931 of each of the three LED units are grouped as an LED set 932 in Fig. 11D. Thus there are three LED sets 932 corresponding to the three LED units.

[00123] The positive conductive line 934 connects the anode on the left side of the first or leftmost LED 931 of each of the three LED sets 932. The negative conductive line 935 connects the cathode on the right side of the last or rightmost LED 931 of each of the three LED sets 932. In each LED set 932 of each two adjacent LEDs 931, the LED 931 on the left has a cathode connected by a conductive part 939 to an anode of the LED 931 on the right. By such a layout, the LEDs 931 of each LED set 932 are connected in series.

[00124] In some embodiments, the conductive part 939 may be used to connect an anode and a cathode of two consecutive LEDs 931 respectively. The negative conductive line 935 connects the cathode of the last or rightmost LED 931 of each of the three LED sets 932. And the positive conductive line 934 connects the anode of the first or leftmost LED 931 of each of the three LED sets 932. Therefore, as shown in Fig. 11D, the length of the conductive part 939 is larger than that of the portion of negative conductive line 935 connecting to a cathode, which length is then larger than that of the portion of positive conductive line 934 connecting to an anode. For example, the length 938 of the conductive part 939 may be larger than the length 937 of the portion of negative conductive line 935 connecting a cathode of an LED 931,

which length 937 is then larger than the length 936 of the portion of the positive conductive line 934 connecting an anode of an LED 931. Such a layout structure improves heat dissipation of the LEDs 931 in LED module 630.

[00125] The positive conductive line 934 may include a lengthwise portion 934a, and the negative conductive line 935 may include a lengthwise portion 935a, which are conducive to make the LED module have a positive "+" connective portion and a negative "-" connective portion at each of the two ends of the LED module, as shown in Fig. 11D. Such a layout structure allows for coupling any of other circuits of the power supply module of the LED lamp, including e.g. the filtering circuit 520 and the rectifying circuits 510 and 540, to the LED module through the positive connective portion 934a and/or the negative connective portion 935a at each or both ends of the LED lamp. Thus the layout structure increases the flexibility in arranging actual circuits in the LED lamp.

[00126] Further, the circuit layouts as shown in Figs. 11C and 11D may be implemented with a bendable circuit sheet or substrate, which may even be called flexible circuit board depending on its specific definition used. For example, the bendable circuit sheet may comprise one conductive layer where the positive conductive line 834, the positive lengthwise portion 834a, the negative conductive line 835, the negative lengthwise portion 835a, and the conductive parts 839 shown in Fig. 11C, and the positive conductive line 934, the positive lengthwise portion 934a, the negative conductive line 935, the negative lengthwise portion 935a, and the conductive parts 939 shown in Fig. 11D are formed by the method of etching.

[00127] Fig. 11E is a plan view of a circuit layout of the LED module according to another embodiment. The layout structures of the LED module in Figs. 11E and 11C correspond to the same way of connecting the LEDs 831 as those shown in Fig. 11B, but the layout structure in Fig. 11E comprises two conductive layers instead of only one conductive layer for forming the circuit layout as shown in Fig. 11C. Referring to Fig. 11E, the main difference from the layout in Fig. 11C is that the positive conductive line 834 and the negative conductive line 835 have a lengthwise portion 834a and a lengthwise portion 835a, respectively, that are formed in a second conductive layer instead. The difference is elaborated as follows.

[00128] In certain embodiments, referring to Fig. 7 again at the same time, a bendable circuit sheet of the LED module includes a first conductive layer 2a and a second conductive layer 2c electrically insulated from each other by a dielectric layer 2b. Of the two conductive layers, the positive conductive line 834, the negative conductive line 835, and the conductive parts 839 in Fig. 11E are formed in first conductive layer 2a by the method of etching for electrically connecting the plurality of LED components 831 e.g. in a form of a mesh, whereas the positive lengthwise portion 834a and the negative lengthwise portion 835a are formed in second conductive layer 2c by etching for electrically connecting (the filtering output terminal of) the filtering circuit. Further, the positive conductive line 834 and the negative conductive line 835 in the first conductive layer 2a have via points 834b and via points 835b, respectively, for connecting to second conductive layer 2c. And the positive lengthwise portion 834a and the negative lengthwise portion 835a in second conductive layer 2c have via points 834c and via points 835c, respectively. The via points 834b are positioned corresponding to the via points 834c, for connecting the positive conductive line 834 and the positive lengthwise portion 834a. The via points 835b are positioned corresponding to the via points 835c, for connecting the negative conductive line 835 and the negative lengthwise portion 835a. An exemplary desirable way of connecting the two conductive layers 2a and 2c is to form a hole connecting each via point 834b and a corresponding via point 834c, and to form a hole connecting each via point 835b and a corresponding via point 835c, with the holes extending through the two conductive layers 2a and 2c and the dielectric layer 2b in-between. And the positive conductive line 834 and the positive lengthwise portion 834a can be electrically connected by welding metallic part(s) through the connecting hole(s), and the negative conductive line 835 and the negative lengthwise portion 835a can be electrically connected by welding metallic part(s) through the connecting hole(s).

[00129] Similarly, the layout structure of the LED module in Fig. 11D may alternatively have the positive lengthwise portion 934a and the negative lengthwise portion 935a disposed in a second conductive layer to constitute a two-layered layout structure.

[00130] The positive conductive lines (834 or 934) may be characterized as including two end terminals at opposite ends, a plurality of pads between the two end terminals and for contacting and/or supplying power to LEDs (e.g., anodes of LEDs), and a wire portion, which may be an elongated conductive line extending along a length of an LED light strip and electrically connecting the two end terminals to the plurality of pads. Similarly, the negative conductive lines (835 or 935) may be characterized as including two end terminals at opposite ends, a plurality of pads between the two end terminals and for contacting and/or supplying power to LEDs (e.g., cathodes of LEDs), and a wire portion, which may be an elongated conductive line extending along a length of an LED light strip and electrically connecting the two end terminals to the plurality of pads.

[00131] The circuit layouts may be implemented for one of the exemplary LED light strips described previously, for example, to serve as a circuit board or sheet for the LED light strip on which the LED light sources are disposed.

[00132] As described herein, an LED unit may refer to a single string of LEDs arranged in series, and an LED module may refer to a single LED unit, or a plurality of LED units connected to a same two nodes (e.g., arranged in parallel). For example, the LED light strip 2 described above may be an LED module and/or LED unit.

[00133] In some embodiments, the thickness of the second conductive layer of a two-layered bendable circuit sheet is, in some embodiments, larger than that of the first conductive layer in order to reduce the voltage drop or loss along each of the positive lengthwise portion and the negative lengthwise portion disposed in the second conductive layer. Compared to a one-layered bendable circuit sheet, since a positive lengthwise portion and a negative lengthwise portion are disposed in a second conductive layer in a two-layer bendable circuit sheet, the width (between two lengthwise sides) of the two-layered bendable circuit sheet is or can be reduced. On the same fixture or plate in a production process, the number of bendable circuit sheets each with a shorter width that can be laid together at most is larger than the number of bendable circuit sheets each with a longer width that can be laid together at most. Thus adopting a bendable circuit sheet with a shorter width can increase the efficiency of production of the LED module. And reliability in the production process,

such as the accuracy of welding position when welding (materials on) the LED components, can also be improved, because a two-layer bendable circuit sheet can better maintain its shape.

[00134] As a variant of the above embodiments, a type of an exemplary LED tube lamp is provided that may have at least some of the electronic components of its power supply module disposed on a light strip of the LED tube lamp. For example, the technique of printed electronic circuit (PEC) can be used to print, insert, or embed at least some of the electronic components onto the LED light strip (e.g., as opposed to being on a separate circuit board connected to the LED light strip).

[00135] In one embodiment, all electronic components of the power supply module are disposed on the light strip. The production process may include or proceed with the following steps: preparation of the circuit substrate (e.g. preparation of a flexible printed circuit board); ink jet printing of metallic nano-ink; ink jet printing of active and passive components (as of the power supply module); drying/sintering; ink jet printing of interlayer bumps; spraying of insulating ink; ink jet printing of metallic nano-ink; ink jet printing of active and passive components (to sequentially form the included layers); spraying of surface bond pad(s); and spraying of solder resist against LED components. The production process may be different, however, and still result in some or all electronic components of the power supply module being disposed directly on the LED light strip.

[00136] In certain embodiments, if all electronic components of the power supply module are disposed on the LED light strip, electrical connection between the terminal pins of the LED tube lamp and the light strip may be achieved by connecting the pins to conductive lines which are welded with ends of the light strip. In this case, another substrate for supporting the power supply module is not required, thereby allowing of an improved design or arrangement in the end cap(s) of the LED tube lamp. In some embodiments, (components of) the power supply module are disposed at two ends of the light strip, in order to significantly reduce the impact of heat generated from the power supply module's operations on the LED components. Since no substrate other than the light strip is used to support the power supply module in this case, the total amount of welding or soldering can be significantly reduced,

improving the general reliability of the power supply module.

[00137] Another case is that some of all electronic components of the power supply module, such as some resistors and/or smaller size capacitors, are printed onto the light strip, and some bigger size components, such as some inductors and/or electrolytic capacitors, are disposed in the end cap(s). The production process of the light strip in this case may be the same as that described above. And in this case disposing some of all electronic components on the light strip is conducive to achieving a reasonable layout of the power supply module in the LED tube lamp, which may allow of an improved design in the end cap(s).

[00138] As a variant embodiment of the above, electronic components of the power supply module may be disposed on the LED light strip by a method of embedding or inserting, e.g. by embedding the components onto a bendable or flexible light strip. In some embodiments, this embedding may be realized by a method using copper-clad laminates (CCL) for forming a resistor or capacitor; a method using ink related to silkscreen printing; or a method of ink jet printing to embed passive components, wherein an ink jet printer is used to directly print inks to constitute passive components and related functionalities to intended positions on the light strip. Then through treatment by ultraviolet (UV) light or drying/sintering, the light strip is formed where passive components are embedded. The electronic components embedded onto the light strip include for example resistors, capacitors, and inductors. In other embodiments, active components also may be embedded. Through embedding some components onto the light strip, a reasonable layout of the power supply module can be achieved to allow of an improved design in the end cap(s), because the surface area on a printed circuit board used for carrying components of the power supply module is reduced or smaller, and as a result the size, weight, and thickness of the resulting printed circuit board for carrying components of the power supply module is also smaller or reduced. Also in this situation since welding points on the printed circuit board for welding resistors and/or capacitors if they were not to be disposed on the light strip are no longer used, the reliability of the power supply module is improved, in view of the fact that these welding points are most liable to (cause or incur) faults, malfunctions, or failures.

Further, the length of conductive lines needed for connecting components on the printed circuit board is therefore also reduced, which allows of a more compact layout of components on the printed circuit board and thus improving the functionalities of these components.

[00139] As mentioned above, electronic components of the power supply module 5 or 250 may be disposed either on the light strip 2 or on a circuit board (such as a printed circuit board) in the end cap(s) of one or two ends of the lamp tube. For improving benefits or advantages of embodiments of the power supply module or the general LED tube lamp, in some embodiments, capacitor(s) in the power supply module may be chip capacitor(s), such as multilayer ceramic chip capacitor(s), disposed either on the light strip 2 or on the short circuit board 253. However, such disposed chip capacitor(s) in use is likely to produce or incur distinct noises due to piezoelectric effects, which may adversely affect the comfort level of using the LED tube lamp by consumers. To address and reduce this problem, in the LED tube lamp of this disclosure, a hole or groove may be disposed (directly) below the chip capacitor by drilling or boring, to significantly reduce the noise by changing the vibration system formed under piezoelectric effects between the chip capacitor and the circuit board carrying the chip capacitor. The shape of the circumference of the hole or groove may be substantially close to, for example, a circle or round, an oval or ellipse, or a rectangle. In some embodiments, the hole or groove is formed in a conductive or wire layer in the light strip 2, or in the short circuit board 253 in the end cap(s), and (directly) below the chip capacitor.

[00140] Next, methods to produce embedded capacitors and resistors are explained as follows.

[00141] Usually, methods for manufacturing embedded capacitors employ or involve a concept called distributed or planar capacitance. The manufacturing process may include the following step(s). On a substrate of a copper layer a very thin insulation layer is applied or pressed, which is then generally disposed between a pair of layers including a power conductive layer and a ground layer. The very thin insulation layer makes the distance between the power conductive layer and the ground layer very short. A capacitance resulting from this structure can also be

realized by a conventional technique of a plated-through hole. Basically, this step is used to create this structure comprising a big parallel-plate capacitor on a circuit substrate.

[00142] Of products of high electrical capacity, certain types of products employ distributed capacitances, and other types of products employ separate embedded capacitances. Through putting or adding a high dielectric-constant material, such as barium titanate, into the insulation layer, the high electrical capacity is achieved.

[00143] A usual method for manufacturing embedded resistors employ conductive or resistive adhesive. This may include, for example, a resin to which conductive carbon or graphite is added, which may be used as an additive or filler. The additive resin is silkscreen printed to an object location, and is then after treatment laminated inside the circuit board. The resulting resistor is connected to other electronic components through plated-through holes or microvias. Another method is called Ohmega-Ply, by which a two metallic layer structure of a copper layer and a thin nickel alloy layer constitutes a layer resistor relative to a substrate. Then through etching the copper layer and nickel alloy layer, different types of nickel alloy resistors with copper terminals can be formed. These types of resistor are each laminated inside the circuit board.

[00144] In an embodiment, conductive wires/lines are directly printed in a linear layout on an inner surface of the LED glass lamp tube, with LED components directly attached on the inner surface and electrically connected by the conductive wires. In some embodiments, the LED components in the form of chips are directly attached over the conductive wires on the inner surface, and connective points are at terminals of the wires for connecting the LED components and the power supply module. After being attached, the LED chips may have fluorescent powder applied or dropped thereon, for producing white light or light of other color by the operating LED tube lamp.

[00145] In some embodiments, luminous efficacy of the LED or LED component is 80 lm/W or above, and in some embodiments, it may be 120 lm/W or above. Certain more optimal embodiments may include a luminous efficacy of the LED or LED component of 160 lm/W or above. White light emitted by an LED component in

the invention may be produced by mixing fluorescent powder with the monochromatic light emitted by a monochromatic LED chip. The white light in its spectrum has major wavelength ranges of 430-460 nm and 550-560 nm, or major wavelength ranges of 430-460 nm, 540-560 nm, and 620-640 nm.

[00146] Fig. 12A is a block diagram of a power supply module in an LED lamp according to an embodiment. As shown in Fig. 12A, the power supply module of the LED lamp includes a rectifying circuit 510, a filtering circuit 520, and may further include some parts of an LED lighting module 530. The LED lighting module 530 in this embodiment comprises a driving circuit 1530 and an LED module 630. The driving circuit 1530 comprises a DC-to-DC converter circuit, and is coupled to the filtering output terminals 521 and 522 to receive a filtered signal and then perform power conversion for converting the filtered signal into a driving signal at the driving output terminals 1521 and 1522. The LED module 630 is coupled to the driving output terminals 1521 and 1522 to receive the driving signal for emitting light. In some embodiments, the current of LED module 630 is stabilized at an objective current value. Descriptions of this LED module 630 are the same as those provided above with reference to Figs. 11A-11E.

[00147] In some embodiments, the LED lighting module 530 shown in Fig. 8C may include the driving circuit 1530 and the LED module 630 as shown in Fig. 12A. Thus, the power supply module for the LED lamp in the present embodiment can be applied to the single-end power supply structure, such as LED light bulbs, personal area lights (PAL), and so forth.

[00148] Fig. 12B is a block diagram of the driving circuit according to an embodiment. Referring to Fig. 12B, a driving circuit includes a controller 1531, and a conversion circuit 1532 for power conversion based on a current source, for driving the LED module to emit light. The conversion circuit 1532 includes a switching circuit 1535 and an energy storage circuit 1538. And the conversion circuit 1532 is coupled to the filtering output terminals 521 and 522 to receive and then convert a filtered signal, under the control by the controller 1531, into a driving signal at the driving output terminals 1521 and 1522 for driving the LED module. Under the control by the controller 1531, the driving signal output by the conversion circuit 1532 comprises a

steady current, making the LED module emitting steady light.

[00149] Fig. 12C is a schematic diagram of the driving circuit according to an embodiment. Referring to Fig. 12C, a driving circuit 1630 in this embodiment comprises a buck DC-to-DC converter circuit having a controller 1631 and a converter circuit. The converter circuit includes an inductor 1632, a diode 1633 for "freewheeling" of current, a capacitor 1634, and a switch 1635. The driving circuit 1630 is coupled to the filtering output terminals 521 and 522 to receive and then convert a filtered signal into a driving signal for driving an LED module connected between the driving output terminals 1521 and 1522.

[00150] In this embodiment, the switch 1635 includes a metal-oxide-semiconductor field-effect transistor (MOSFET) and has a first terminal coupled to the anode of freewheeling diode 1633, a second terminal coupled to the filtering output terminal 522, and a control terminal coupled to the controller 1631 used for controlling current conduction or cutoff between the first and second terminals of switch 1635. The driving output terminal 1521 is connected to the filtering output terminal 521, and the driving output terminal 1522 is connected to an end of the inductor 1632, which has another end connected to the first terminal of switch 1635. The capacitor 1634 is coupled between the driving output terminals 1521 and 1522 to stabilize the voltage between the driving output terminals 1521 and 1522. The freewheeling diode 1633 has a cathode connected to the driving output terminal 1521.

[00151] Next, a description follows as to an exemplary operation of the driving circuit 1630.

[00152] The controller 1631 is configured for determining when to turn the switch 1635 on (in a conducting state) or off (in a cutoff state) according to a current detection signal S535 and/or a current detection signal S531. For example, in some embodiments, the controller 1631 is configured to control the duty cycle of switch 1635 being on and switch 1635 being off in order to adjust the size or magnitude of the driving signal. The current detection signal S535 represents the magnitude of current through the switch 1635. The current detection signal S531 represents the magnitude of current through the LED module coupled between the driving output

terminals 1521 and 1522. The controller 1631 may control the duty cycle of the switch 1635 being on and off, based on, for example, a magnitude of a current detected based on current detection signal S531 or S535. As such, when the magnitude is above a threshold, the switch may be off (cutoff state) for more time, and when magnitude goes below the threshold, the switch may be on (conducting state) for more time. According to any of current detection signal S535 and current detection signal S531, the controller 1631 can obtain information on the magnitude of power converted by the converter circuit. When the switch 1635 is switched on, a current of a filtered signal is input through the filtering output terminal 521, and then flows through the capacitor 1634, the driving output terminal 1521, the LED module, the inductor 1632, and the switch 1635, and then flows out from the filtering output terminal 522. During this flowing of current, the capacitor 1634 and the inductor 1632 are performing storing of energy. On the other hand, when the switch 1635 is switched off, the capacitor 1634 and the inductor 1632 perform releasing of stored energy by a current flowing from the freewheeling diode 1633 to the driving output terminal 1521 to make the LED module continuing to emit light.

[00153] In some embodiments, the capacitor 1634 is an optional element, so it can be omitted and is thus depicted in a dotted line in Fig. 12C. In some application environments, the natural characteristic of an inductor to oppose instantaneous change in electric current passing through the inductor may be used to achieve the effect of stabilizing the current through the LED module, thus omitting the capacitor 1634.

[00154] As described above, because the driving circuit 1630 is configured for determining when to turn a switch 1635 on (in a conducting state) or off (in a cutoff state) according to a current detection signal S535 and/or a current detection signal S531, the driving circuit 1630 can maintain a stable current flow through the LED module. Therefore, the color temperature may not change with current to some LED module, such as white, red, blue, green LED modules. For example, an LED can retain the same color temperature under different illumination conditions. In some embodiments, because the inductor 1632 playing the role of the energy-storing circuit releases the stored power when the switch 1635 cuts off, the voltage/current flowing

through the LED module remains above a predetermined voltage/current level so that the LED module may continue to emit light maintaining the same color temperature. In this way, when the switch 1635 conducts again, the voltage/current flowing through the LED module does not need to be adjusted to go from a minimum value to a maximum value. Accordingly, the LED module lighting with flickering can be avoided, the entire illumination can be improved, the lowest conducting period can be smaller, and the driving frequency can be higher.

[00155] Fig. 12D is a schematic diagram of the driving circuit according to an embodiment. Referring to Fig. 12D, a driving circuit 1730 in this embodiment comprises a boost DC-to-DC converter circuit having a controller 1731 and a converter circuit. The converter circuit includes an inductor 1732, a diode 1733 for "freewheeling" of current, a capacitor 1734, and a switch 1735. The driving circuit 1730 is configured to receive and then convert a filtered signal from the filtering output terminals 521 and 522 into a driving signal for driving an LED module coupled between the driving output terminals 1521 and 1522.

[00156] The inductor 1732 has an end connected to the filtering output terminal 521, and another end connected to the anode of freewheeling diode 1733 and a first terminal of the switch 1735, which has a second terminal connected to the filtering output terminal 522 and the driving output terminal 1522. The freewheeling diode 1733 has a cathode connected to the driving output terminal 1521. And the capacitor 1734 is coupled between the driving output terminals 1521 and 1522.

[00157] The controller 1731 is coupled to a control terminal of switch 1735, and is configured for determining when to turn the switch 1735 on (in a conducting state) or off (in a cutoff state), according to a current detection signal S535 and/or a current detection signal S531. When the switch 1735 is switched on, a current of a filtered signal is input through the filtering output terminal 521, and then flows through the inductor 1732 and the switch 1735, and then flows out from the filtering output terminal 522. During this flowing of current, the current through the inductor 1732 increases with time, with the inductor 1732 being in a state of storing energy, while the capacitor 1734 enters a state of releasing energy, making the LED module continuing to emit light. On the other hand, when the switch 1735 is switched off, the

inductor 1732 enters a state of releasing energy as the current through the inductor 1732 decreases with time. In this state, the current through the inductor 1732 then flows through the freewheeling diode 1733, the capacitor 1734, and the LED module, while the capacitor 1734 enters a state of storing energy.

[00158] In some embodiments the capacitor 1734 is an optional element, so it can be omitted and is thus depicted in a dotted line in Fig. 12D. When the capacitor 1734 is omitted and the switch 1735 is switched on, the current of inductor 1732 does not flow through the LED module, making the LED module not emit light; but when the switch 1735 is switched off, the current of inductor 1732 flows through the freewheeling diode 1733 to reach the LED module, making the LED module emit light. Therefore, by controlling the time that the LED module emits light, and the magnitude of current through the LED module, the average luminance of the LED module can be stabilized to be above a defined value, thus also achieving the effect of emitting a steady light.

[00159] As described above, because the controller 1731 included in the driving circuit 1730 is coupled to the control terminal of switch 1735, and is configured for determining when to turn a switch 1735 on (in a conducting state) or off (in a cutoff state), according to a current detection signal S535 and/or a current detection signal S531, the driving circuit 1730 can maintain a stable current flow through the LED module. Therefore, the color temperature may not change with current to some LED modules, such as white, red, blue, or green LED modules. For example, an LED can retain the same color temperature under different illumination conditions. In some embodiments, because the inductor 1732 playing the role of the energy-storing circuit releases the stored power when the switch 1735 cuts off, the voltage/current flowing through the LED module remains above a predetermined voltage/current level so that the LED module may continue to emit light maintaining the same color temperature. In this way, when the switch 1735 conducts again, the voltage/current flowing through the LED module does not need to be adjusted to go from a minimum value to a maximum value. Accordingly, the LED module lighting with flickering can be avoided, the entire illumination can be improved, the lowest conducting period can be smaller, and the driving frequency can be higher.

[00160] Fig. 12E is a schematic diagram of the driving circuit according to an exemplary embodiment. Referring to Fig. 12E, a driving circuit 1830 in this embodiment comprises a buck DC-to-DC converter circuit having a controller 1831 and a converter circuit. The converter circuit includes an inductor 1832, a diode 1833 for "freewheeling" of current, a capacitor 1834, and a switch 1835. The driving circuit 1830 is coupled to the filtering output terminals 521 and 522 to receive and then convert a filtered signal into a driving signal for driving an LED module connected between the driving output terminals 1521 and 1522.

[00161] The switch 1835 has a first terminal coupled to the filtering output terminal 521, a second terminal coupled to the cathode of freewheeling diode 1833, and a control terminal coupled to the controller 1831 to receive a control signal from the controller 1831 for controlling current conduction or cutoff between the first and second terminals of the switch 1835. The anode of freewheeling diode 1833 is connected to the filtering output terminal 522 and the driving output terminal 1522. The inductor 1832 has an end connected to the second terminal of switch 1835, and another end connected to the driving output terminal 1521. The capacitor 1834 is coupled between the driving output terminals 1521 and 1522 to stabilize the voltage between the driving output terminals 1521 and 1522.

[00162] The controller 1831 is configured for controlling when to turn the switch 1835 on (in a conducting state) or off (in a cutoff state) according to a current detection signal S535 and/or a current detection signal S531. When the switch 1835 is switched on, a current of a filtered signal is input through the filtering output terminal 521, and then flows through the switch 1835, the inductor 1832, and the driving output terminals 1521 and 1522, and then flows out from the filtering output terminal 522. During this flowing of current, the current through the inductor 1832 and the voltage of the capacitor 1834 both increase with time, so the inductor 1832 and the capacitor 1834 are in a state of storing energy. On the other hand, when the switch 1835 is switched off, the inductor 1832 is in a state of releasing energy and thus the current through it decreases with time. In this case, the current through the inductor 1832 circulates through the driving output terminals 1521 and 1522, the freewheeling diode 1833, and back to the inductor 1832.

[00163] In some embodiments the capacitor 1834 is an optional element, so it can be omitted and is thus depicted in a dotted line in Fig. 12E. When the capacitor 1834 is omitted, no matter whether the switch 1835 is turned on or off, the current through the inductor 1832 will flow through the driving output terminals 1521 and 1522 to drive the LED module to continue emitting light.

[00164] As described above, because the controller 1831 included in the driving circuit 1830 is configured for controlling when to turn a switch 1835 on (in a conducting state) or off (in a cutoff state) according to a current detection signal S535 and/or a current detection signal S531, the driving circuit 1730 can maintain a stable current flow through the LED module. Therefore, the color temperature may not change with current to some LED modules, such as white, red, blue, or green LED modules. For example, an LED can retain the same color temperature under different illumination conditions. In some embodiments, because the inductor 1832 playing the role of the energy-storing circuit releases the stored power when the switch 1835 cuts off, the voltage/current flowing through the LED module remains above a predetermined voltage/current level so that the LED module may continue to emit light maintaining the same color temperature. In this way, when the switch 1835 conducts again, the voltage/current flowing through the LED module does not need to be adjusted to go from a minimum value to a maximum value. Accordingly, the LED module lighting with flickering can be avoided, the entire illumination can be improved, the lowest conducting period can be smaller, and the driving frequency can be higher.

[00165] Fig. 12F is a schematic diagram of the driving circuit according to an exemplary embodiment. Referring to Fig. 12F, a driving circuit 1930 in this embodiment comprises a buck DC-to-DC converter circuit having a controller 1931 and a converter circuit. The converter circuit includes an inductor 1932, a diode 1933 for "freewheeling" of current, a capacitor 1934, and a switch 1935. The driving circuit 1930 is coupled to the filtering output terminals 521 and 522 to receive and then convert a filtered signal into a driving signal for driving an LED module connected between the driving output terminals 1521 and 1522.

[00166] The inductor 1932 has an end connected to the filtering output terminal 521 and the driving output terminal 1522, and another end connected to a first end of

the switch 1935. The switch 1935 has a second end connected to the filtering output terminal 522, and a control terminal connected to controller 1931 to receive a control signal from controller 1931 for controlling current conduction or cutoff of the switch 1935. The freewheeling diode 1933 has an anode coupled to a node connecting the inductor 1932 and the switch 1935, and a cathode coupled to the driving output terminal 1521. The capacitor 1934 is coupled to the driving output terminals 1521 and 1522 to stabilize the driving of the LED module coupled between the driving output terminals 1521 and 1522.

[00167] The controller 1931 is configured for controlling when to turn the switch 1935 on (in a conducting state) or off (in a cutoff state) according to a current detection signal S531 and/or a current detection signal S535. When the switch 1935 is turned on, a current is input through the filtering output terminal 521, and then flows through the inductor 1932 and the switch 1935, and then flows out from the filtering output terminal 522. During this flowing of current, the current through the inductor 1932 increases with time, so the inductor 1932 is in a state of storing energy; but the voltage of the capacitor 1934 decreases with time, so the capacitor 1934 is in a state of releasing energy to keep the LED module continuing to emit light. On the other hand, when the switch 1935 is turned off, the inductor 1932 is in a state of releasing energy and its current decreases with time. In this case, the current through the inductor 1932 circulates through the freewheeling diode 1933, the driving output terminals 1521 and 1522, and back to the inductor 1932. During this circulation, the capacitor 1934 is in a state of storing energy and its voltage increases with time.

[00168] In some embodiments the capacitor 1934 is an optional element, so it can be omitted and is thus depicted in a dotted line in Fig. 12F. When the capacitor 1934 is omitted and the switch 1935 is turned on, the current through the inductor 1932 doesn't flow through the driving output terminals 1521 and 1522, thereby making the LED module not emit light. On the other hand, when the switch 1935 is turned off, the current through the inductor 1932 flows through the freewheeling diode 1933 and then the LED module to make the LED module emit light. Therefore, by controlling the time that the LED module emits light, and the magnitude of current through the LED module, the average luminance of the LED module can be stabilized

to be above a defined value, thus also achieving the effect of emitting a steady light.

[00169] As described above, because the controller 1931 included in the driving circuit 1930 is configured for controlling when to turn a switch 1935 on (in a conducting state) or off (in a cutoff state) according to a current detection signal S535 and/or a current detection signal S531, the driving circuit 1930 can maintain a stable current flow through the LED module. Therefore, the color temperature may not change with current to some LED modules, such as white, red, blue, or green LED modules. For example, an LED can retain the same color temperature under different illumination conditions. In some embodiments, because the inductor 1932 playing the role of the energy-storing circuit releases the stored power when the switch 1935 cuts off, the voltage/current flowing through the LED module remains above a predetermined voltage/current level so that the LED module may continue to emit light maintaining the same color temperature. In this way, when the switch 1935 conducts again, the voltage/current flowing through the LED module does not need to be adjusted to go from a minimum value to a maximum value. Accordingly, the LED module lighting with flickering can be avoided, the entire illumination can be improved, the lowest conducting period can be smaller, and the driving frequency can be higher.

[00170] With reference to Figs. 5 and 6, a short circuit board 253 includes a first short circuit substrate and a second short circuit substrate respectively connected to two terminal portions of a long circuit sheet 251, and electronic components of the power supply module are respectively disposed on the first short circuit substrate and the second short circuit substrate. The first short circuit substrate and the second short circuit substrate may have roughly the same length, or different lengths. In general, the first short circuit substrate (i.e. the right circuit substrate of short circuit board 253 in Fig. 5 and the left circuit substrate of short circuit board 253 in Fig. 6) has a length that is about 30% - 80% of the length of the second short circuit substrate (i.e. the left circuit substrate of short circuit board 253 in Fig. 5 and the right circuit substrate of short circuit board 253 in Fig. 6). In some embodiments the length of the first short circuit substrate is about 1/3 - 2/3 of the length of the second short circuit substrate. For example, in one embodiment, the length of the first short circuit substrate may be about half the length of the second short circuit substrate. The

length of the second short circuit substrate may be, for example in the range of about 15 mm to about 65 mm, depending on actual application occasions. In certain embodiments, the first short circuit substrate is disposed in an end cap at an end of the LED tube lamp, and the second short circuit substrate is disposed in another end cap at the opposite end of the LED tube lamp.

[00171] For example, capacitors of the driving circuit, such as the capacitors 1634, 1734, 1834, and 1934 in Figs. 12C - 12F, in practical use may include two or more capacitors connected in parallel. Some or all capacitors of the driving circuit in the power supply module may be arranged on the first short circuit substrate of short circuit board 253, while other components such as the rectifying circuit, filtering circuit, inductor(s) of the driving circuit, controller(s), switch(es), diodes, etc. are arranged on the second short circuit substrate of short circuit board 253. Since the inductors, controllers, switches, etc. are electronic components with higher temperature, arranging some or all capacitors on a circuit substrate separate or away from the circuit substrate(s) of high-temperature components helps prevent the working life of capacitors (especially electrolytic capacitors) from being negatively affected by the high-temperature components, thus improving the reliability of the capacitors. Further, the physical separation between the capacitors and both the rectifying circuit and filtering circuit also contributes to reducing the problem of EMI.

[00172] In certain exemplary embodiments, the conversion efficiency of the driving circuits is above 80%. In some embodiments, the conversion efficiency of the driving circuits is above 90%. In still other embodiments, the conversion efficiency of the driving circuits is above 92%. The illumination efficiency of the LED lamps is above 120 lm/W. In some embodiments, the illumination efficiency of the LED lamps is above 160 lm/W. The illumination efficiency including the combination of the driving circuits and the LED modules is above 120 lm/W * 90% = 108 lm/W. In some embodiments, the illumination efficiency including the combination of the driving circuits and the LED modules is above 160 lm/W * 92% = 147.21 lm/W.

[00173] In some embodiments, the transmittance of the diffusion film in the LED tube lamp is above 85%. As a result, in certain embodiments, the illumination efficiency of the LED lamps is above 108 lm/W * 85% = 91.8 lm/W. In some

embodiments, the illumination efficiency of the LED lamps is above 147.21 lm/W * 85% = 125.12 lm/W.

[00174] Fig. 13A is a block diagram of a power supply module in an LED tube lamp according to an exemplary embodiment. Compared to that shown in Fig. 8C, the present embodiment comprises a rectifying circuit 510, a filtering circuit 520, and a driving circuit 1530, and further comprises an over voltage protection (OVP) circuit 1570. In this embodiment, a driving circuit 1530 and an LED module 630 compose the LED lighting module 530. The OVP circuit 1570 is coupled to the filtering output terminals 521 and 522 for detecting the filtered signal. The OVP circuit 1570 clamps the logic level of the filtered signal when determining the logic level thereof higher than a defined OVP value. Hence, the OVP circuit 1570 protects the LED lighting module 530 from damage due to an OVP condition.

[00175] Fig. 13B is a schematic diagram of an overvoltage protection (OVP) circuit according to an exemplary embodiment. An OVP circuit 1670 comprises a voltage clamping diode 1671, such as zener diode, coupled to the filtering output terminals 521and 522. The voltage clamping diode 1671 is conducted to clamp a voltage difference at a breakdown voltage when the voltage difference of the filtering output terminals 521 and 522 (i.e., the logic level of the filtered signal) reaches the breakdown voltage. In some embodiments, the breakdown voltage may be in a range of about 40 V to about 100 V. In certain embodiments, the breakdown voltage may be in a range of about 55 V to about 75V.

[00176] Fig. 14A is a block diagram of a power supply module in an LED tube lamp according to an exemplary embodiment. Compared to that shown in Fig. 8C, the present embodiment comprises a rectifying circuit 510, a filtering circuit 520, and a driving circuit 1530, and further comprises an auxiliary power module 2510. The auxiliary power module 2510 is coupled between the filtering output terminals 521 and 522. The auxiliary power module 2510 detects the filtered signal in the filtering output terminals 521 and 522, and determines whether providing an auxiliary power to the filtering output terminals 521 and 522 based on the detected result. When the supply of the filtered signal is stopped or a logic level thereof is insufficient, i.e., when a drive voltage for the LED module is below a defined voltage, the auxiliary power

module provides auxiliary power to keep the LED lighting module 530 continuing to emit light. The defined voltage is determined according to an auxiliary power voltage of the auxiliary power module 2510.

[00177] Fig. 14B is a block diagram of a power supply module in an LED tube lamp according to an exemplary embodiment. Compared to that shown in Fig. 14A, the present embodiment comprises a rectifying circuit 510, a filtering circuit 520, and may further include some parts of an LED lighting module 530, and an auxiliary power module 2510, and the LED lighting module 530 further comprises a driving circuit 1530 and an LED module 630. The auxiliary power module 2510 is coupled between the driving output terminals 1521 and 1522. The auxiliary power module 2510 detects the driving signal in the driving output terminals 1521 and 1522, and determines whether to provide an auxiliary power to the driving output terminals 1521 and 1522 based on the detected result. When the driving signal is no longer being supplied or a logic level thereof is insufficient, the auxiliary power module 2510 provides the auxiliary power to keep the LED module 630 continuously light.

[00178] Fig. 14C is a schematic diagram of an auxiliary power module according to an embodiment. The auxiliary power module 2610 comprises an energy storage unit 2613 and a voltage detection circuit 2614. The auxiliary power module further comprises an auxiliary power positive terminal 2611 and an auxiliary power negative terminal 2612 for being respectively coupled to the filtering output terminals 521 and 522 or the driving output terminals 1521 and 1522. The voltage detection circuit 2614 detects a logic level of a signal at the auxiliary power positive terminal 2611 and the auxiliary power negative terminal 2612 to determine whether releasing outward the power of the energy storage unit 2613 through the auxiliary power positive terminal 2611 and the auxiliary power negative terminal 2612.

[00179] In some embodiments, the energy storage unit 2613 is a battery or a supercapacitor. When a voltage difference of the auxiliary power positive terminal 2611 and the auxiliary power negative terminal 2612 (the drive voltage for the LED module) is higher than the auxiliary power voltage of the energy storage unit 2613, the voltage detection circuit 2614 charges the energy storage unit 2613 by the signal in the auxiliary power positive terminal 2611 and the auxiliary power negative terminal

2612. When the drive voltage is lower than the auxiliary power voltage, the energy storage unit 2613 releases the stored energy outward through the auxiliary power positive terminal 2611 and the auxiliary power negative terminal 2612.

[00180] The voltage detection circuit 2614 comprises a diode 2615, a bipolar junction transistor (BJT) 2616 and a resistor 2617. A positive end of the diode 2615 is coupled to a positive end of the energy storage unit 2613 and a negative end of the diode 2615 is coupled to the auxiliary power positive terminal 2611. The negative end of the energy storage unit 2613 is coupled to the auxiliary power negative terminal 2612. A collector of the BJT 2616 is coupled to the auxiliary power positive terminal 2611, and an emitter thereof is coupled to the positive end of the energy storage unit 2613. One end of the resistor 2617 is coupled to the auxiliary power positive terminal 2611 and the other end is coupled to a base of the BJT 2616. When the collector of the BJT 2616 is a cut-in voltage higher than the emitter thereof, the resistor 2617 conducts the BJT 2616. When the power source provides power to the LED tube lamp normally, the energy storage unit 2613 is charged by the filtered signal through the filtering output terminals 521 and 522 and the conducted BJT 2616 or by the driving signal through the driving output terminals 1521 and 1522 and the conducted BJT 2616 until that the collector-emitter voltage of the BJT 2616 is lower than or equal to the cut-in voltage. When the filtered signal or the driving signal is no longer being supplied or the logic level thereof is insufficient, the energy storage unit 2613 provides power through the diode 2615 to keep the LED lighting module 530 or the LED module 630 continuously light.

[00181] In some embodiments, the maximum voltage of the charged energy storage unit 2613 is at least one cut-in voltage of the BJT 2616 lower than the voltage difference applied between the auxiliary power positive terminal 2611 and the auxiliary power negative terminal 2612. The voltage difference provided between the auxiliary power positive terminal 2611 and the auxiliary power negative terminal 2612 is a turn-on voltage of the diode 2615 lower than the voltage of the energy storage unit 2613. Hence, when the auxiliary power module 2610 provides power, the voltage applied at the LED module 630 is lower (about the sum of the cut-in voltage of the BJT 2616 and the turn-on voltage of the diode 2615). In the embodiment shown in the

Fig. 14B, the brightness of the LED module 630 is reduced when the auxiliary power module supplies power thereto. Thereby, when the auxiliary power module is applied to an emergency lighting system or a constant lighting system, the user realizes the main power supply, such as commercial power, is abnormal and then performs necessary precautions therefor.

[00182] Referring to Fig. 15A, a block diagram of an LED tube lamp including a power supply module in accordance with certain embodiments is illustrated. Compared to the LED lamp shown in Fig. 8C, the LED tube lamp of Fig. 15A includes a rectifying circuit 510, a filtering circuit 520, and an LED lighting module 530, and further includes an installation detection module 2520. The installation detection module 2520 is coupled to the rectifying circuit 510 via an installation detection terminal 2521 and is coupled to the filtering circuit 520 via an installation detection terminal 2522. The installation detection module 2520 detects the signal passing through the installation detection terminals 2521 and 2522 and determines whether to cut off an LED driving signal (e.g., an external driving signal) passing through the LED tube lamp based on the detected result. The installation detection module 2520 includes circuitry configured to perform the steps of detecting the signal passing through the installation detection terminals 2521 and 2522 and determining whether to cut off an LED driving signal, and thus may be referred to as an installation detection circuit, or more generally as a detection circuit or cut-off circuit. When an LED tube lamp is not yet installed on a lamp socket or holder, or in some cases if it is not installed properly or is only partly installed (e.g., one side is connected to a lamp socket, but not the other side yet), the installation detection module 2520 detects a smaller current compared to a predetermined current (or current value) and determines the signal is passing through a high impedance through the installation detection terminals 2521 and 2522. In this case, in certain embodiments, the installation detection circuit 2520 is in a cut-off state to make the LED tube lamp stop working. Otherwise, the installation detection module 2520 determines that the LED tube lamp has already been installed on the lamp socket or holder (e.g., when the installation detection module 2520 detects a current equal to or larger than a predetermined current and determines the signal is passing through a low impedance

through the installation detection terminals 2521 and 2522), and maintains conducting state to make the LED tube lamp working normally.

[00183] For example, in some embodiments, when a current passing through the installation detection terminals 2521 and 2522 is greater than or equal to a specific, defined installation current (or a current value), which may indicate that the current supplied to the LED lighting module 530 is greater than or equal to a specific, defined operating current, the installation detection module 2520 is conducting to make the LED tube lamp operate in a conducting state. For example, a current greater than or equal to the specific current value may indicate that the LED tube lamp has correctly been installed in the lamp socket or holder. When the current passing through the installation detection terminals 2521 and 2522 is smaller than the specific, defined installation current (or the current value), which may indicate that the current supplied to the LED lighting module 530 is less than a specific, defined operating current, the installation detection module 2520 cuts off current to make the LED tube lamp enter in a non-conducting state based on determining that the LED tube lamp has been not installed in, or does not properly connect to, the lamp socket or holder. In certain embodiments, the installation detection module 2520 determines conducting or cutting off based on the impedance detection to make the LED tube lamp operate in a conducting state or enter non-conducting state. The LED tube lamp operating in a conducting state may refer to the LED tube lamp including a sufficient current passing through the LED module to cause the LED light sources to emit light. The LED tube lamp operating in a cut-off state may refer to the LED tube lamp including an insufficient current or no current passing through the LED module so that the LED light sources do not emit light. Accordingly, the occurrence of electric shock caused by touching the conductive part of the LED tube lamp which is incorrectly installed on the lamp socket or holder can be efficiently avoided.

[00184] Referring to Fig. 15B, a block diagram of an installation detection module in accordance with certain embodiments is illustrated. The installation detection module includes a switch circuit 2580, a detection pulse generating module 2540, a detection result latching circuit 2560, and a detection determining circuit 2570. Certain of these circuits or modules may be referred to as first, second, third, etc.,

circuits as a naming convention to differentiate them from each other.

[00185] The detection determining circuit 2570 is coupled to and detects the signal between the installation detection terminals 2521 (through a switch circuit coupling terminal 2581 and the switch circuit 2580) and 2522. The detection determining circuit 2570 is also coupled to the detection result latching circuit 2560 via a detection result terminal 2571 to transmit the detection result signal to the detection result latching circuit 2560. The detection determining circuit 2570 may be configured to detect a current passing through terminals 2521 and 2522 (e.g., to detect whether the current is above or below a specific current value).

[00186] The detection pulse generating module 2540 is coupled to the detection result latching circuit 2560 via a pulse signal output terminal 2541, and generates a pulse signal to inform the detection result latching circuit 2560 of a time point for latching (storing) the detection result. For example, the detection pulse generating module 2540 may be a circuit configured to generate a signal that causes a latching circuit, such as the detection result latching circuit 2560 to enter and remain in a state that corresponds to one of a conducting state or a cut-off state for the LED tube lamp. The detection result latching circuit 2560 stores the detection result according to the detection result signal (or detection result signal and pulse signal), and transmits or provides the detection result to the switch circuit 2580 coupled to the detection result latching circuit 2560 via a detection result latching terminal 2561. The switch circuit 2580 controls the state between conducting or cut off between the installation detection terminals 2521 and 2522 according to the detection result.

[00187] In some embodiments, the detection pulse generating module 2540 may be referred to as a first circuit 2540, the detection result latching circuit 2560 may be referred to as a second circuit 2560, the switch circuit 2580 may be referred to as a third circuit 2580, the detection determining circuit 2570 may be referred to as a fourth circuit 2570, the switch circuit coupling terminal 2581 may be referred to as a first terminal 2581 and the detection result terminal 2571 may be referred to as a second terminal 2571, the pulse signal output terminal 2541 may be referred to as a third terminal 2541, the detection result latching terminal 2561 may be referred to as a fourth terminal 2561, the installation detection terminal 2521 may be referred to as a

first installation detection terminal 2521, and the installation detection terminal 2522 may be referred to as a second installation detection terminal 2522. In this exemplary embodiment, the fourth circuit 2570 is coupled to the third circuit 2580 and the second circuit 2560 via the first terminal 2581 and the second terminal 2571, respectively, the second circuit 2560 is also coupled to the first circuit 2540 and the third circuit 2580 via the third terminal 2541 and the fourth terminal 2561, respectively.

[00188] In some embodiments, the fourth circuit 2570 is configured for detecting a signal between the first installation detection terminal 2521 and the second installation detection terminal 2522 through the first terminal 2581 and the fourth circuit 2580. For example, because of the above configuration, the fourth circuit 2570 is capable of detecting and determining whether a current passing through the first installation detection terminal 2521 and the second installation detection terminal 2522 is below or above a predetermined current value and transmitting or providing a detection result signal to the second circuit 2560 via the second terminal 2571.

[00189] In some embodiments, the first circuit 2540 generates a pulse signal through the second circuit 2560 to make the third circuit 2580 working in a conducting state during the pulse signal. Meanwhile, as a result, the power loop of the LED tube lamp between the installation detection terminals 2521 and 2522 is thus conducting as well. The fourth circuit 2570 detects a sampling signal on the power loop and generates a signal based on a detection result to inform the second circuit 2560 of a time point for latching (storing) the detection result received by the second circuit 2560 from the fourth circuit 2570. For example, the fourth circuit 2570 may be a circuit configured to generate a signal that causes a latching circuit, such as the second circuit 2560 to enter and remain in a state that corresponds to one of a conducting state or a cut-off state for the LED tube lamp. The second circuit 2560 stores the detection result according to the detection result signal (or detection result signal and pulse signal), and transmits or provides the detection result to the third circuit 2580 coupled to the second circuit 2560 via the fourth terminal 2561. The third circuit 2580 receives the detection result transmitted from the second circuit 2560 and controls the state between conducting or cut off between the installation detection terminals 2521 and 2522 according to the detection result. It should be noted that the labels "first,"

"second," "third," etc., described in connection with these embodiments can be interchangeable and are merely used here in order to more easily differentiate the different circuits, nodes, and other components from each other.

[00190] Referring to Fig. 15C, a block diagram of a detection pulse generating module in accordance with certain embodiments is illustrated. A detection pulse generating module 2640 may be a circuit that includes multiple capacitors 2642, 2645, and 2646, multiple resistors 2643, 2647, and 2648, two buffers 2644 and 2651, an inverter 2650, a diode 2649, and an OR gate 2652. The capacitor 2642 may be referred to as a first capacitor 2642, the capacitor 2645 may be referred to as a second capacitor 2645, and the capacitor 2646 may be referred to as a third capacitor 2646. The resistor 2643 may be referred to as a first resistor 2643, the resistor 2647 may be referred to as a second resistor 2647, and the resistor 2648 may be referred to as a third resistor 2648. The buffer 2644 may be referred to as a first buffer 2644 and the buffer 2651 may be referred to as a second buffer 2651. The diode 2649 may be referred to as a first diode 2649 and the OR gate 2652 may be referred to as a first OR gate 2652. With use or operation, the capacitor 2642 and the resistor 2643 connect in series between a driving voltage (e.g., a driving voltage source, which may be a node of a power supply), such as VCC usually defined as a high logic level voltage, and a reference voltage (or potential), such as ground potential in this embodiment. The connection node between the capacitor 2642 and the resistor 2643 is coupled to an input terminal of the buffer 2644. In this exemplary embodiment, the buffer 2644 includes two inverters connected in series between an input terminal and an output terminal of the buffer 2644. The resistor 2647 is coupled between the driving voltage, e.g., VCC, and an input terminal of the inverter 2650. The resistor 2648 is coupled between an input terminal of the buffer 2651 and the reference voltage, e.g. ground potential in this embodiment. An anode of the diode 2649 is grounded and a cathode of the diode 2649 is coupled to the input terminal of the buffer 2651. First ends of the capacitors 2645 and 2646 are jointly coupled to an output terminal of the buffer 2644, and second, opposite ends of the capacitors 2645 and 2646 are respectively coupled to the input terminal of the inverter 2650 and the input terminal of the buffer 2651. In this exemplary embodiment, the buffer 2651

includes two inverters connected in series between an input terminal and an output terminal of the buffer 2651. An output terminal of the inverter 2650 and an output terminal of the buffer 2651 are coupled to two input terminals of the OR gate 2652. According to certain embodiments, the voltage (or potential) for "high logic level" and "low logic level" mentioned in this specification are all relative to another voltage (or potential) or a certain reference voltage (or potential) in circuits, and further may be described as "logic high logic level" and "logic low logic level."

[00191] When an end cap of an LED tube lamp is inserted into a lamp socket and the other end cap thereof is electrically coupled to a human body, or when both end caps of the LED tube lamp are inserted into the lamp socket, the LED tube lamp is conductive with electricity. At this moment, the installation detection module (e.g., the installation detection module 2520 as illustrated in Fig. 15A) enters a detection stage. The voltage on the connection node of the capacitor 2642 and the resistor 2643 is high initially (equals to the driving voltage, VCC) and decreases with time to zero finally. The input terminal of the buffer 2644 is coupled to the connection node of the capacitor 2642 and the resistor 2643, so the buffer 2644 outputs a high logic level signal at the beginning and changes to output a low logic level signal when the voltage on the connection node of the capacitor 2642 and the resistor 2643 decreases to a low logic trigger logic level. As a result, the buffer 2644 is configured to produce an input pulse signal and then remain in a low logic level thereafter (stops outputting the input pulse signal.) The width for the input pulse signal may be described as equal to one (initial setting) time period, which is determined by the capacitance value of the capacitor 2642 and the resistance value of the resistor 2643.

[00192] Next, the operations for the buffer 2644 to produce the pulse signal with the initial setting time period will be described below. Since the voltage on a first end of the capacitor 2645 and on a first end of the resistor 2647 is equal to the driving voltage VCC, the voltage on the connection node of both of them is also a high logic level. The first end of the resistor 2648 is grounded and the first end of the capacitor 2646 receives the input pulse signal from the buffer 2644, so the connection node of the capacitor 2646 and the resistor 2648 has a high logic level voltage at the beginning but this voltage decreases with time to zero (in the meantime, the capacitor

stores the voltage being equal to or approaching the driving voltage VCC.) Accordingly, initially the inverter 2650 outputs a low logic level signal and the buffer 2651 outputs a high logic level signal, and hence the OR gate 2652 outputs a high logic level signal (a first pulse signal) at the pulse signal output terminal 2541. At this moment, the detection result latching circuit 2560 (as illustrated in Fig. 15B) stores the detection result for the first time according to the detection result signal received from the detection determining circuit 2570 (as illustrated in Fig. 15B) and the pulse signal generated at the pulse signal output terminal 2541. During that initial pulse time period, as illustrated in Fig. 15B, the detection pulse generating module 2540 outputs a high logic level signal, which results in the detection result latching circuit 2560 outputting the result of that high logic level signal.

[00193] When the voltage on the connection node of the capacitor 2646 and the resistor 2648 decreases to the low logic trigger logic level, the buffer 2651 changes to output a low logic level signal to make the OR gate 2652 output a low logic level signal at the pulse signal output terminal 2541 (stops outputting the first pulse signal.) The width of the first pulse signal output from the OR gate 2652 is determined by the capacitance value of the capacitor 2646 and the resistance value of the resistor 2648.

[00194] The operation after the buffer 2644 stops outputting the pulse signal is described as below. For example, the operation may be initially in an operating stage. Since the capacitor 2646 stores the voltage being almost equal to the driving voltage VCC, and when the buffer 2644 instantaneously changes its output from a high logic level signal to a low logic level signal, the voltage on the connection node of the capacitor 2646 and the resistor 2648 is below zero but will be pulled up to zero by the diode 2649 rapidly charging the capacitor 2646. Therefore, the buffer 2651 still outputs a low logic level signal.

[00195] In some embodiments, when the buffer 2644 instantaneously changes its output from a high logic level signal to a low logic level signal, the voltage on the one end of the capacitor 2645 also changes from the driving voltage VCC to zero instantly. This makes the connection node of the capacitor 2645 and the resistor 2647 have a low logic level signal. At this moment, the output of the inverter 2650 changes to a high logic level signal to make the OR gate output a high logic level signal (a

second pulse signal) at the pulse signal output terminal 2541. The detection result latching circuit 2560 as illustrated in Fig. 15B stores the detection result for a second time according to the detection result signal received from the detection determining circuit 2570 (as illustrated in Fig. 15B) and the pulse signal generated at the pulse signal output terminal 2541. Next, the driving voltage VCC charges the capacitor 2645 through the resistor 2647 to make the voltage on the connection node of the capacitor 2645 and the resistor 2647 increase with time to the driving voltage VCC. When the voltage on the connection node of the capacitor 2645 and the resistor 2647 increases to reach a high logic trigger logic level, the inverter 2650 outputs a low logic level signal again to make the OR gate 2652 stop outputting the second pulse signal. The width of the second pulse signal is determined by the capacitance value of the capacitor 2645 and the resistance value of the resistor 2647.

[00196] As those mentioned above, in certain embodiments, the detection pulse generating module 2640 generates two high logic level pulse signals in the detection stage, which are the first pulse signal and the second pulse signal. These pulse signals are output from the pulse signal output terminal 2541. Moreover, there is an interval with a defined time between the first and second pulse signals (e.g., an opposite-logic signal, which may have a low logic level when the pulse signals have a high logic level), and the defined time is determined by the capacitance value of the capacitor 2642 and the resistance value of the resistor 2643.

[00197] From the detection stage entering the operating stage, the detection pulse generating module 2640 does not produce the pulse signal any more, and keeps the pulse signal output terminal 2541 on a low logic level potential. As described herein, the operating stage is the stage following the detection stage (e.g., following the time after the second pulse signal ends). The operating stage occurs when the LED tube lamp is at least partly connected to a power source, such as provided in a lamp socket. For example, the operating stage may occur when part of the LED tube lamp, such as only one side of the LED tube lamp, is properly connected to one side of a lamp socket, and part of the LED tube lamp is either connected to a high impedance, such as a person, and/or is improperly connected to the other side of the lamp socket (e.g., is misaligned so that the metal contacts in the

socket do not contact metal contacts in the LED tube lamp). The operating stage may also occur when the entire LED tube lamp is properly connected to the lamp socket.

[00198] Referring to Fig. 15D, a detection determining circuit in accordance with certain embodiments is illustrated. An exemplary detection determining circuit 2670 includes a comparator 2671 and a resistor 2672. The comparator 2671 may also be referred to as a first comparator 2671 and the resistor 2672 may also be referred to as a fifth resistor 2672. A negative input terminal of the comparator 2671 receives a reference logic level signal (or a reference voltage) Vref, a positive input terminal thereof is grounded through the resistor 2672 and is also coupled to a switch circuit coupling terminal 2581. Referring to Figs. 15B and 15D, the signal flowing into the switch circuit 2580 from the installation detection terminal 2521 outputs to the switch circuit coupling terminal 2581 to the resistor 2672. When the current of the signal passing through the resistor 2672 reaches a certain level (for example, bigger than or equal to a defined current for installation, (e.g. 2A) and this makes the voltage on the resistor 2672 higher than the reference voltage Vref (referring to two end caps inserted into the lamp socket,) the comparator 2671 produces a high logic level detection result signal and outputs it to the detection result terminal 2571. For example, when an LED tube lamp is correctly installed on a lamp socket, the comparator 2671 outputs a high logic level detection result signal at the detection result terminal 2571, whereas the comparator 2671 generates a low logic level detection result signal and outputs it to the detection result terminal 2571 when a current passing through the resistor 2672 is insufficient to make the voltage on the resistor 2672 higher than the reference voltage Vref (referring to only one end cap inserted into the lamp socket.) Therefore, in some embodiments, when the LED tube lamp is incorrectly installed on the lamp socket or one end cap thereof is inserted into the lamp socket but the other one is grounded by an object such as a human body, the current will be too small to make the comparator 2671 output a high logic level detection result signal to the detection result terminal 2571.

[00199] Referring to Fig. 15E, a schematic detection result latching circuit according to some embodiments of the present invention is illustrated. A detection result latching circuit 2660 includes a D flip-flop 2661, a resistor 2662, and an OR

gate 2663. The D flip-flop 2661 may also be referred to as a first D flip-flop 2661, the resistor 2662 may also be referred to as a fourth resistor 2662, and the OR gate 2663 may also be referred to as a second OR gate 2663. The D flip-flop 2661 has a CLK input terminal coupled to a detection result terminal 2571, and a D input terminal coupled to a driving voltage VCC. When the detection result terminal 2571 first outputs a low logic level detection result signal, the D flip-flop 2661 initially outputs a low logic level signal at a Q output terminal thereof, but the D flip-flop 2661 outputs a high logic level signal at the Q output terminal thereof when the detection result terminal 2571 outputs a high logic level detection result signal. The resistor 2662 is coupled between the Q output terminal of the D flip-flop 2661 and a reference voltage, such as ground potential. When the OR gate 2663 receives the first or second pulse signals from the pulse signal output terminal 2541 or receives a high logic level signal from the Q output terminal of the D flip-flop 2661, the OR gate 2663 outputs a high logic level detection result latching signal at a detection result latching terminal 2561. The detection pulse generating module 2640 only in the detection stage outputs the first and the second pulse signals to make the OR gate 2663 output the high logic level detection result latching signal, and thus the D flip-flop 2661 decides the detection result latching signal to be the high logic level or the low logic level the rest of the time, e.g., including the operating stage after the detection stage. Accordingly, when the detection result terminal 2571 has no high logic level detection result signal, the D flip-flop 2661 keeps a low logic level signal at the Q output terminal to make the detection result latching terminal 2561 also keep a low logic level detection result latching signal in the detection stage. On the contrary, once the detection result terminal 2571 has a high logic level detection result signal, the D flip-flop 2661 outputs and keeps a high logic level signal (e.g., based on VCC) at the Q output terminal. In this way, the detection result latching terminal 2561 keeps a high logic level detection result latching signal in the operating stage as well.

[00200] Referring to Fig. 15F, a schematic switch circuit according to some embodiments is illustrated. A switch circuit 2680 includes a transistor, such as a bipolar junction transistor (BJT) 2681, as being a power transistor, which has the ability of dealing with high current/power and is suitable for the switch circuit. The BJT

2681 may also be referred to as a first transistor 2681. The BJT 2681 has a collector coupled to an installation detection terminal 2521, a base coupled to a detection result latching terminal 2561, and an emitter coupled to a switch circuit coupling terminal 2581. When the detection pulse generating module 2640 produces the first and second pulse signals, the BJT 2681 is in a transient conduction state. This allows the detection determining circuit 2670 to perform the detection for determining the detection result latching signal to be a high logic level or a low logic level. When the detection result latching circuit 2660 outputs a high logic level detection result latching signal at the detection result latching terminal 2561, the BJT 2681 is in the conducting state to make the installation detection terminals 2521 and 2522 conducting. In contrast, when the detection result latching circuit 2660 outputs a low logic level detection result latching signal at the detection result latching terminal 2561 and the output from detection pulse generating module 2640 is a low logic level, the BJT 2681 is cut-off or in the blocking state to make the installation detection terminals 2521 and 2522 cut-off or blocking.

[00201] Since the external driving signal is an AC signal and in order to avoid the detection error resulting from the logic level of the external driving signal being just around zero when the detection determining circuit 2670 detects, the detection pulse generating module 2640 generates the first and second pulse signals to let the detection determining circuit 2670 perform two detections. So the issue of the logic level of the external driving signal being just around zero in a single detection can be avoided. In some cases, the time difference between the productions of the first and second pulse signals is not multiple times of half one cycle of the external driving signal. For example, it does not correspond to the multiple phase differences of 180 degrees of the external driving signal. In this way, when one of the first and second pulse signals is generated and unfortunately the external driving signal is around zero, it can be avoided that the external driving signal is again around zero when the other pulse signal is generated.

[00202] The time difference between the productions of the first and second pulse signals, for example, an interval with a defined time between both of them can be represented as following:

[00203] the interval = (X+Y)(T/2),

[00204] where T represents the cycle of an external driving signal, X is a natural number, $0 < Y < 1$, with Y in some embodiments in the range of 0.05 - 0.95, and in some embodiments in the range of 0.15 - 0.85.

[00205] Furthermore, in order to avoid the installation detection module entering the detection stage from misjudgment resulting from the logic level of the driving voltage VCC being too small, the first pulse signal can be set to be produced when the driving voltage VCC reaches or is higher than a defined logic level. For example, in some embodiments, the detection determining circuit 2670 works after the driving voltage VCC reaching a high enough logic level in order to prevent the installation detection module from misjudgment due to an insufficient logic level.

[00206] According to the examples mentioned above, when one end cap of an LED tube lamp is inserted into a lamp socket and the other one floats or electrically couples to a human body or other grounded object, the detection determining circuit outputs a low logic level detection result signal because of high impedance. The detection result latching circuit stores the low logic level detection result signal based on the pulse signal of the detection pulse generating module, making it as the low logic level detection result latching signal, and keeps the detection result in the operating stage, without changing the logic value. In this way, the switch circuit keeps cutting-off or blocking instead of conducting continually. And further, the electric shock situation can be prevented and the requirement of safety standard can also be met. On the other hand, when two end caps of the LED tube lamp are correctly inserted into the lamp socket, the detection determining circuit outputs a high logic level detection result signal because the impedance of the circuit for the LED tube lamp itself is small. The detection result latching circuit stores the high logic level detection result signal based on the pulse signal of the detection pulse generating module, making it as the high logic level detection result latching signal, and keeps the detection result in the operating stage. So the switch circuit keeps conducting to make the LED tube lamp work normally in the operating stage.

[00207] In some embodiments, when one end cap of the LED tube lamp is inserted into the lamp socket and the other one floats or electrically couples to a

human body, the detection determining circuit outputs a low logic level detection result signal to the detection result latching circuit, and then the detection pulse generating module outputs a low logic level signal to the detection result latching circuit to make the detection result latching circuit output a low logic level detection result latching signal to make the switch circuit cutting-off or blocking. As such, the switch circuit blocking makes the installation detection terminals, e.g. the first and second installation detection terminals, blocking. As a result, the LED tube lamp is in non-conducting or blocking state.

[00208] However, in some embodiments, when two end caps of the LED tube lamp are correctly inserted into the lamp socket, the detection determining circuit outputs a high logic level detection result signal to the detection result latching circuit to make the detection result latching circuit output a high logic level detection result latching signal to make the switch circuit conducting. As such, the switch circuit conducting makes the installation detection terminals, e.g. the first and second installation detection terminals, conducting. As a result, the LED tube lamp operates in a conducting state.

[00209] Thus, according to the operation of the installation detection module, a first circuit, upon connection of at least one end of the LED tube lamp to a lamp socket, generates and outputs two pulses, each having a pulse width, with a time period between the pulses. The first circuit may include various of the elements described above configured to output the pulses to a base of a transistor (e.g., a BJT transistor) that serves as a switch. The pulses occur during a detection stage for detecting whether the LED tube lamp is properly connected to a lamp socket. The timing of the pulses may be controlled based on the timing of various parts of the first circuit changing from high to low logic levels, or vice versa.

[00210] The pulses can be timed such that, during that detection stage time, if the LED tube lamp is properly connected to the lamp socket (e.g., both ends of the LED tube lamp are correctly connected to conductive terminals of the lamp socket), at least one of the pulse signals occurs when an AC current from a driving signal is at a non-zero level. For example, the pulse signals can occur at intervals that are different from half of the period of the AC signal. For example, respective start points or mid

points of the pulse signals, or a time between an end of the first pulse signal and a beginning of the second pulse signal may be separated by an amount of time that is different from half of the period of the AC signal (e.g., it may be between 0.05 and 0.95 percent of a multiple of half of the period of the AC signal). During a pulse that occurs when the AC signal is at a non-zero level, a switch that receives the AC signal at the non-zero level may be turned on, causing a latch circuit to change states such that the switch remains permanently on so long as the LED tube lamp remains properly connected to the lamp socket. For example, the switch may be configured to turn on when each pulse is output from the first circuit. The latch circuit may be configured to change state only when the switch is on and the current output from the switch is above a threshold value, which may indicate a proper connection to a light socket. As a result, the LED tube lamp operates in a conducting state.

[00211] On the other hand, if both pulses occur when a driving signal at the LED tube lamp has a near-zero current level, or a current level below a particular threshold, then the state of the latch circuit is not changed, and so the switch is only on during the two pulses, but then remains permanently off after the pulses and after the detection mode is over. For example, the latch circuit can be configured to remain in its present state if the current output from the switch is below the threshold value. In this manner, the LED tube lamp remains in a non-conducting state, which prevents electric shock, even though part of the LED tube lamp is connected to an electrical power source.

[00212] It is worth noting that according to certain embodiments, the width of the pulse signal generated by the detection pulse generating module is between 10 μs to 1 ms, and it is used to make the switch circuit conducting for a short period when the LED tube lamp conducts instantaneously. In some embodiments, a pulse current is generated to pass through the detection determining circuit for detecting and determining. Since the pulse is for a short time and not for a long time, the electric shock situation will not occur. Furthermore, the detection result latching circuit also keeps the detection result during the operating stage (e.g., the operating stage being the period after the detection stage and during which part of the LED tube lamp is still connected to a power source), and no longer changes the detection result stored

previously complying with the circuit state changing. A situation resulting from changing the detection result can thus be avoided. In some embodiments, the installation detection module, such as the switch circuit, the detection pulse generating module, the detection result latching circuit, and the detection determining circuit, could be integrated into a chip and then embedded in circuits for saving the circuit cost and layout space.

[00213] As discussed in the above examples, in some embodiments, an LED tube lamp includes an installation detection circuit comprising a first circuit configured to output two pulse signals, the first pulse signal output at a first time and the second pulse signal output at a second time after the first time, and a switch configured to receive an LED driving signal and to receive the two pulse signals, wherein the two pulse signals control turning on and off of the switch. The installation detection circuit may be configured to, during a detection stage, detect during each of the two pulse signals whether the LED tube lamp is properly connected to a lamp socket. When it is not detected during either pulse signal that the LED tube lamp is properly connected to the lamp socket, the switch may remain in an off state after the detection stage. When it is detected during at least one of the pulse signals that the LED tube lamp is properly connected to the lamp socket, the switch may remain in an on state after the detection stage. The two pulse signals may occur such that they are separated by a time different from a multiple of half of a period of the LED driving signal, and such that at least one of them does not occur when the LED driving signal has a current value of substantially zero. It should be noted that although a circuit for producing two pulse signals is described, the disclosure is not intended to be limiting as such. For example, a circuit may be implemented such that a plurality of pulse signals may occur, wherein at least two of the plurality of pulse signals are separated by a time different from a multiple of half of a period of the LED driving signal, and such that at least one of the plurality of pulse signals does not occur when the LED driving signal has a current value of substantially zero.

[00214] Referring to Fig. 15G, an installation detection module according to an exemplary embodiment is illustrated. The installation detection module includes a detection pulse generating module 2740 (which may also be referred to as a

detection pulse generating circuit or a first circuit), a detection result latching circuit 2760 (which may also be referred to as a second circuit), a switch circuit 2780 (which may also be referred to as a third circuit), and a detection determining circuit 2770 (which may also be referred to as a fourth circuit). The detection pulse generating module 2740 is coupled (e.g., electrically connected) to the detection result latching circuit 2760 via a path 2741, and is configured to generate at least one pulse signal. A path as described herein may include a conductive line connecting between two components, circuits, or modules, and may include opposite ends of the conductive line connected to the respective components, circuits or modules. The detection result latching circuit 2760 is coupled (e.g., electrically connected) to the switch circuit 2780 via a path 2761, and is configured to receive and output the pulse signal(s) from the detection pulse generating module 2740. The switch circuit 2780 is coupled (e.g., electrically connected) to one end (e.g., a first installation detection terminal 2521) of a power loop of an LED tube lamp and the detection determining circuit 2770, and is configured to receive the pulse signal(s) output from the detection result latching circuit 2760, and configured to conduct (or turn on) during the pulse signal(s) so as to cause the power loop of the LED tube lamp to be conducting. The detection determining circuit 2770 is coupled (e.g., electrically connected) to the switch circuit 2780, the other end (e.g., a second installation detection terminal 2522) of the power loop of the LED tube lamp and the detection result latching circuit 2760, and is configured to detect at least one sampling signal on the power loop when the switch circuit 2780 and the power loop are conductive, so as to determine an installation state between the LED tube lamp and a lamp socket. The detection determining circuit 2770 is further configured to transmit detection result(s) to the detection result latching circuit 2760 for next control. In some embodiments, the detection pulse generating module 2740 is further coupled (e.g., electrically connected) to the output of the detection result latching circuit 2760 to control the time of the pulse signal(s).

[00215] In some embodiments, one end of a first path 2781 is coupled to a first node of the detection determining circuit 2770 and the opposite end of the first path 2781 is coupled to a first node of the switch circuit 2780. In some embodiments, a second node of the detection determining circuit 2770 is coupled to the second

installation detection terminal 2522 of the power loop and a second node of the switch circuit 2780 is coupled to the first installation detection terminal 2521 of the power loop. In some embodiments, one end of a second path 2771 is coupled to a third node of the detection determining circuit 2770 and the opposite end of the second path 2771 is coupled to a first node of the detection result latching circuit 2760, one end of a third path 2741 is coupled to a second node of the detection result latching circuit 2760 and the opposite end of the third path 2741 is coupled to a first node of the detection pulse generating circuit 2740. In some embodiments, one end of a fourth path 2761 is coupled to a third node of the switch circuit 2780 and the opposite end of the fourth path 2761 is coupled to a third node of the detection result latching circuit 2760. In some embodiments, the fourth path 2761 is also coupled to a second node of the detection pulse generating circuit 2740.

[00216] In some embodiments, the detection determining circuit 2770 is configured for detecting a signal between the first installation detection terminal 2521 and the second installation detection terminal 2522 through the first path 2781 and the switch circuit 2780. For example, because of the above configuration, the detection determining circuit 2770 is capable of detecting and determining whether a current passing through the first installation detection terminal 2521 and the second installation detection terminal 2522 is below or above a predetermined current value and transmitting or providing a detection result signal to the detection result latching circuit 2760 via the second path 2771.

[00217] In some embodiments, the detection pulse generating circuit 2740, also referred to generally as a pulse generating circuit, generates a pulse signal through the detection result latching circuit 2760 to make the switch circuit 2780 remain in a conducting state during the pulse signal. For example, the pulse signal generated by the detection pulse generating circuit 2740 controls turning on the switch circuit 2780 which is coupled to the detection pulse generating circuit 2740. As a result of maintaining a conducting state of the switch circuit 2780, the power loop of the LED tube lamp between the installation detection terminals 2521 and 2522 is also maintain a conducting state. The detection determining circuit 2770 detects a sampling signal on the power loop and generates a signal based on a detection result to inform the

detection result latching circuit 2760 of a time point for latching (storing) the detection result received by the detection result latching circuit 2760 from the detection determining circuit 2770. For example, the detection determining circuit 2770 may be a circuit configured to generate a signal that causes a latching circuit, such as the detection result latching circuit 2760 to enter and remain in a state that corresponds to one of a conducting state (e.g., "on" state) or a cut-off state for the LED tube lamp. The detection result latching circuit 2760 stores the detection result according to the detection result signal (or detection result signal and pulse signal), and transmits or provides the detection result to the switch circuit 2780 coupled to the third node of the detection result latching circuit 2760 via the fourth path 2761. The switch circuit 2780 receives the detection result transmitted from the detection result latching circuit 2760 via the third node of the switch circuit 2780 and controls the state between conducting or cut off between the installation detection terminals 2521 and 2522 according to the detection result. For example, when the detection determining circuit 2770 detects during the pulse signal that the LED tube lamp is not properly installed on the lamp socket, the pulse signal controls the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open, and when the detection determining circuit 2770 detects during the pulse signal that the LED tube lamp is properly installed on the lamp socket, the pulse signal controls the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to a maintain conducting state.

[00218] The detail circuit architecture and the entire operation thereof of each of the detection pulse generating module 2740 (or circuit), the detection result latching circuit 2760, the switch circuit 2780, and the detection determining circuit 2770 will be described below.

[00219] Referring to Fig. 15H, a detection pulse generating module according to an exemplary embodiment is illustrated. The detection pulse generating module 2740 includes: a resistor 2742 (which also may be referred to as a sixth resistor), a capacitor 2743 (which also may be referred to as a fourth capacitor), a Schmitt trigger 2744, a resistor 2745 (which also may be referred to as a seventh resistor), a transistor 2746 (which also may be referred to as a second transistor), and a resistor

2747 (which also may be referred to as an eighth resistor).

[00220] In some embodiments, one end of the resistor 2742 is connected to a driving signal, for example, Vcc, and the other end of the resistor 2742 is connected to one end of the capacitor 2743. The other end of the capacitor 2743 is connected to a ground node. In some embodiments, the Schmitt trigger 2744 has an input end and an output end, the input end connected to a connection node of the resistor 2742 and the capacitor 2743, the output end connected to the detection result latching circuit 2760 via the third path 2741 (Fig. 15G). In some embodiments, one end of the resistor 2745 is connected to the connection node of the resistor 2742 and the capacitor 2743 and the other end of the resistor 2745 is connected to a collector of the transistor 2746. An emitter of the transistor 2746 is connected to a ground node. In some embodiments, one end of the resistor 2747 is connected to a base of the transistor 2746 and the other end of the resistor 2747 is connected to the detection result latching circuit 2760 (Fig. 15G) and the switch circuit 2780 (Fig. 15G) via the fourth path 2761. In certain embodiments, the detection pulse generating module 2740 further includes: a Zener diode 2748, having an anode and a cathode, the anode connected to the other end of the capacitor 2743 to the ground, the cathode connected to the end of the capacitor 2743 (the connection node of the resistor 2742 and the capacitor 2743).

[00221] Referring to Fig. 15I, a detection result latching circuit according to an exemplary embodiment is illustrated. The detection result latching circuit 2760 includes: a D flip-flop 2762 (which also may be referred to as a second D flip-flop), having a data input end D, a clock input end CLK, and an output end Q, the data input end D connected to the driving signal mentioned above (e.g., Vcc), the clock input end CLK connected to the detection determining circuit 2770 (Fig. 15G); and an OR gate 2763 (which also may be referred to as a third OR gate), having a first input end, a second input end, and an output end, the first input end connected to the output end of the Schmitt trigger 2744 (Fig. 15H), the second input end connected to the output end Q of the D flip-flop 2762, the output end of the OR gate 2763 connected to the other end of the resistor 2747 (Fig. 15H) and the switch circuit 2780 (Fig. 15G).

[00222] Referring to Fig. 15J, a switch circuit according to an exemplary

embodiment is illustrated. The switch circuit 2780 includes: a transistor 2782 (which also may be referred to as a third transistor), having a base, a collector, and an emitter, the base connected to the output of the OR gate 2763 via the fourth path 2761 (Fig. 15I), the collector connected to one end of the power loop, such as the first installation detection terminal 2521, the emitter connected to the detection determining circuit 2770 (Fig. 15G). In some embodiments, the transistor 2782 may be replaced by other equivalently electronic parts, e.g., a MOSFET.

[00223] Referring to Fig. 15K, a detection determining circuit according to an exemplary embodiment is illustrated. The detection determining circuit 2770 includes: a resistor 2774 (which also may be referred to as a ninth resistor), one end of the resistor 2774 connected to the emitter of the transistor 2782 (Fig. 15J), the other end of the resistor 2774 connected to the other end of the power loop, such as the second installation detection terminal 2522; a diode 2775 (which also may be referred to as a second diode), having an anode and a cathode, the anode connected to an end of the resistor 2744 that is not connected to a ground node; a comparator 2772 (which also may be referred to as a second comparator), having a first input end, a second input end, and an output end; a comparator 2773 (which also may be referred to as a third comparator), having a first input end, a second input end, and an output end; a resistor 2776 (which also may be referred to as a tenth resistor); a resistor 2777 (which also may be referred to as an eleventh resistor); and a capacitor 2778 (which also may be referred to as a fifth capacitor).

[00224] In some embodiments, the first input end of the comparator 2772 is connected to a predefined signal, for example, a reference voltage, Vref = 1.3V, but the reference voltage value is not limited thereto, the second input end of the comparator 2772 is connected to the cathode of the diode 2775, and the output end of the comparator 2772 is connected to the clock input end of the D flip-flop 2762 (Fig. 15I). In some embodiments, the first input end of the comparator 2773 is connected to the cathode of the diode 2775, the second input end of the comparator 2773 is connected to another predefined signal, for example, a reference voltage, Vref = 0.3V, but the reference voltage value is not limited thereto, and the output end of the comparator 2773 is connected to the clock input end of the D flip-flop 2762 (Fig. 15I).

In some embodiments, one end of the resistor 2776 is connected to the driving signal mentioned above (e.g., Vcc) and the other end of the resistor 2776 is connected to the second input end of the comparator 2772 and one end of the resistor 2777 that is not connected to a ground node and the other end of the resistor 2777 is connected to the ground node. In some embodiments, the capacitor 2778 is connected to the resistor 2777 in parallel. In certain embodiments, the diode 2775, the comparator 2773, the resistors 2776 and 2777, and the capacitor 2778 may be omitted, and the second input end of the comparator 2772 may be directly connected to the end of the resistor 2774 (e.g., the end of the resistor 2774 that is not connected to the ground node) when the diode 2775 is omitted. In certain embodiments, the resistor 2774 may include two resistors connected in parallel based on the consideration of power consumption having an equivalent resistance value ranging from about 0.1 ohm to about 5 ohm.

[00225] In some embodiments, some parts of the installation detection module may be integrated into an integrated circuit (IC) in order to provide reduced circuit layout space resulting in reduced manufacturing cost of the circuit. For example, the Schmitt trigger 2744 of the detection pulse generating module 2740, the detection result latching circuit 2760, and the two comparators 2772 and 2773 of the detection determining circuit 2770 may be integrated into an IC, but the disclosure is not limited thereto.

[00226] An operation of the installation detection module will be described in more detail in accordance with some example embodiments. In one exemplary embodiment, the capacitor voltage may not mutate; the voltage of the capacitor in the power loop of the LED tube lamp before the power loop being conductive is zero and the capacitor's transient response may appear to have a short-circuit condition; when the LED tube lamp is correctly installed to the lamp socket, the power loop of the LED tube lamp in transient response may have a smaller current-limiting resistance and a bigger peak current; and when the LED tube lamp is incorrectly installed to the lamp socket, the power loop of the LED tube lamp in transient response may have a bigger current-limiting resistance and a smaller peak current. This embodiment may also meet the UL standard to make the leakage current of the LED tube lamp less than 5

MIU. The following table illustrates the current comparison in a case when the LED tube lamp works normally (e.g., when the two end caps of the LED tube lamp are correctly installed to the lamp socket) and in a case when the LED tube lamp is incorrectly installed to the lamp socket (e.g., when one end cap of the LED tube lamp is installed to the lamp socket but the other one is touched by a human body).

	Correct installation	Incorrect installation
Maximum transient current		$i_{pk\_\max} = \frac{V_{in\_pk}}{R_{fuse} + 500} = \frac{305 \times 1.414}{10 + 500} = 845mA$
Minimum transient current	$i_{pk\_\min} = \frac{\Delta V_{in}}{R_{fuse}} = \frac{50}{10} = 5A$	

[00227] As illustrated in the above table, in the part of the denominator: R_{fuse} represents the resistance of the fuse of the LED tube lamp. For example, 10 ohm may be used, but the disclosure is not limited thereto, as resistance value for R_{fuse} in calculating the minimum transient current i_{pk_min} and 510 ohm may be used as resistance value for R_{fuse} in calculating the maximum transient current i_{pk_max} (an additional 500 ohms is used to emulate the conductive resistance of human body in transient response). In the part of the numerator: maximum voltage from the root-mean-square voltage (Vmax = Vrms * 1.414 = 305 * 1.414) is used in calculating the maximum transient current i_{pk_max} and minimum voltage difference, for example, 50V (but the disclosure is not limited thereto) is used in calculating the minimum transient current i_{pk_min}. Accordingly, when the LED tube lamp is correctly installed to the lamp socket (e.g., when two end caps of the LED tube lamp are installed to the lamp socket correctly) and works normally, its minimum transient current is 5A. But, when the LED tube lamp is incorrectly installed to the lamp socket (e.g., when one

end cap is installed to the lamp socket but the other one is touched by human body), its maximum transient current is only 845 mA. Therefore, certain examples of the disclosed embodiments use the current which passes transient response and flows through the capacitor in the LED power loop, such as the capacitor of the filtering circuit, to detect and determine the installation state between the LED tube lamp and the lamp socket. For example, such embodiments may detect whether the LED tube lamp is correctly installed to the lamp socket. Certain examples of the disclosed embodiments further provide a protection mechanism to protect the user from electric shock caused by touching the conductive part of the LED tube lamp which is incorrectly installed to the lamp socket. The embodiments mentioned above are used to illustrate certain aspects of the disclosed invention but the disclosure is not limited thereto.

[00228] Further, referring to Fig. 15G again, in some embodiments, when an LED tube lamp is being installed to a lamp socket, after a period (e.g., the period utilized to determine the cycle of a pulse signal), the detection pulse generating module 2740 outputs a first high level voltage rising from a first low level voltage to the detection result latching circuit 2760 through a path 2741 (also referred to as a third path). The detection result latching circuit 2760 receives the first high level voltage, and then simultaneously outputs a second high level voltage to the switch circuit 2780 and the detection pulse generating module 2740 through a path 2761 (also referred to as a fourth path). In some embodiments, when the switch circuit 2780 receives the second high level voltage, the switch circuit 2780 conducts to cause the power loop of the LED tube lamp to be conducting as well. In this exemplary embodiment, the power loop at least includes the first installation detection terminal 2521, the switch circuit 2780, the path 2781 (also referred to as a first path), the detection determining circuit 2770, and the second installation detection terminal 2522. In the meantime, the detection pulse generating module 2740 receives the second high level voltage from the detection result latching circuit 2760, and after a period (e.g., the period utilized to determine the width (or period) of pulse signal), its output from the first high level voltage falls back to the first low level voltage (the first time of the first low level voltage, the first high level voltage, and the second time of

the first low level voltage form a first pulse signal). In some embodiments, when the power loop of the LED tube lamp is conductive, the detection determining circuit 2770 detects a first sampling signal, such as a voltage signal, on the power loop. When the first sampling signal is greater than or equal to a predefined signal, such as a reference voltage, the installation detection module determines that the LED tube lamp is correctly installed to the lamp socket according to the application principle of this disclosed embodiments described above. Therefore, the detection determining circuit 2770 included in the installation detection module outputs a third high level voltage (also referred to as a first high level signal) to the detection result latching circuit 2760 through a path 2771 (also referred to as a second path). The detection result latching circuit 2760 receives the third high level voltage (also referred to as the first high level signal) and continues to output a second high level voltage (also referred to as a second high level signal) to the switch circuit 2780. The switch circuit 2780 receives the second high level voltage (also referred to as the second high level signal) and maintains conducting state to cause the power loop to remain conducting. The detection pulse generating module 2740 does not generate any pulse signal while the power loop remains conductive.

[00229] However, in some embodiments, when the first sampling signal is smaller than the predefined signal, the installation detection module, according to certain exemplary embodiments as described above, determines that the LED tube lamp has not been correctly installed to the lamp socket. Therefore, the detection determining circuit 2770 outputs a third low level voltage (also referred to as a first low level signal) to the detection result latching circuit 2760. The detection result latching circuit 2760 receives the third low level voltage (also referred to as the first low level signal) and continues to output a second low level voltage (also referred to as a second low level signal) to the switch circuit 2780. The switch circuit 2780 receives the second low level voltage (also referred to as the second low level signal) and then keeps blocking to cause the power loop to remain open. Accordingly, the occurrence of electric shock caused by touching the conductive part of the LED tube lamp which is incorrectly installed on the lamp socket can be sufficiently avoided.

[00230] In some embodiments, when the power loop of the LED tube lamp

remains open for a period (a period that represents the cycle of pulse signal), the detection pulse generating module 2740 outputs the first high level voltage rising from the first low level voltage to the detection result latching circuit 2760 through the path 2741 once more. The detection result latching circuit 2760 receives the first high level voltage, and then simultaneously outputs a second high level voltage to the switch circuit 2780 and the detection pulse generating module 2740. In some embodiments, when the switch circuit 2780 receives the second high level voltage, the switch circuit 2780 conducts again to cause the power loop of the LED tube lamp (in this exemplary embodiment, the power loop at least includes the first installation detection terminal 2521, the switch circuit 2780, the path 2781, the detection determining circuit 2770, and the second installation detection terminal 2522) to be conducting as well. In the meantime, the detection pulse generating module 2740 receives the second high level voltage from the detection result latching circuit 2760, and after a period (a period that is utilized to determine the width (or period) of pulse signal), its output from the first high level voltage falls back to the first low level voltage (the third time of the first low level voltage, the second time of the first high level voltage, and the fourth time of the first low level voltage form a second pulse signal). In some embodiments, when the power loop of the LED tube lamp is conductive again, the detection determining circuit 2770 also detects a second sampling signal, such as a voltage signal, on the power loop yet again. When the second sampling signal is greater than or equal to the predefined signal, the installation detection module determines, according to certain exemplary embodiments described above, that the LED tube lamp is correctly installed to the lamp socket. Therefore, the detection determining circuit 2770 outputs a third high level voltage (also referred to as a first high level signal) to the detection result latching circuit 2760 through the path 2771. The detection result latching circuit 2760 receives the third high level voltage (also referred to as the first high level signal) and continues to output a second high level voltage (also referred to as a second high level signal) to the switch circuit 2780. The switch circuit 2780 receives the second high level voltage (also referred to as the second high level signal) and maintains a conducting state to cause the power loop to remain conducting. The detection pulse generating module 2740 does not generate

any pulse signal while the power loop remains conductive.

[00231] In some embodiments, when the second sampling signal is smaller than the predefined signal, the installation detection module determines, according to certain exemplary embodiments described above, that the LED tube lamp has not been correctly installed to the lamp socket. Therefore, the detection determining circuit 2770 outputs the third low level voltage (also referred to as the first low level signal) to the detection result latching circuit 2760. The detection result latching circuit 2760 receives the third low level voltage (also referred to as the first low level signal) and continues to output the second low level voltage (also referred to as the second low level signal) to the switch circuit 2780. The switch circuit 2780 receives the second low level voltage (also referred to as the second low level signal) and then keeps blocking to cause the power loop to remain open.

[00232] Next, referring to Fig. 15H – Fig. 15K at the same time, in some embodiments when an LED tube lamp is being installed to a lamp socket, the capacitor 2743 is charged by the driving signal, for example, Vcc, through the resistor 2742. And when the voltage of the capacitor 2743 rises enough to trigger the Schmitt trigger 2744, the Schmitt trigger 2744 outputs a first high level voltage rising from a first low level voltage in an initial state to an input end of the OR gate 2763. After the OR gate 2763 receives the first high level voltage from the Schmitt trigger 2744, the OR gate 2763 outputs a second high level voltage to the base of the transistor 2782 and the resistor 2747. When the base of the transistor 2782 receives the second high level voltage from the OR gate 2763, the collector and the emitter of the transistor 2782 are conducting to further cause the power loop of the LED tube lamp (in this exemplary embodiment, the power loop at least includes the first installation detection terminal 2521, the transistor 2782, the resistor 2744, and the second installation detection terminal 2522) to be conducting as well. In the meantime, the base of the transistor 2746 receives the second high level voltage from the OR gate 2763 through the resistor 2747, and then the collector and the emitter of the transistor 2746 are conductive and grounded to cause the voltage of the capacitor 2743 to be discharged to the ground through the resistor 2745. In some embodiments, when the voltage of the capacitor 2743 is not enough to trigger the Schmitt trigger 2744, the Schmitt

trigger 2744 outputs the first low level voltage falling from the first high level voltage (a first instance of a first low level voltage at a first time, followed by a first high level voltage, followed by a second instance of the first low level voltage at a second time form a first pulse signal). When the power loop of the LED tube lamp is conductive, the current passing through the capacitor in the power loop, such as, the capacitor of the filtering circuit, by transient response flows through the transistor 2782 and the resistor 2774 and forms a voltage signal on the resistor 2774. The voltage signal is compared to a reference voltage, for example, 1.3V, but the reference voltage is not limited thereto, by the comparator 2772. When the voltage signal is greater than and/or equal to the reference voltage, the comparator 2772 outputs a third high level voltage to the clock input end CLK of the D flip-flop 2762. In the meantime, since the data input end D of the D flip-flop 2762 is connected to the driving signal, the D flip-flop 2762 outputs a high level voltage (at its output end Q) to another input end of the OR gate 2763. This causes the OR gate 2763 to keep outputting the second high level voltage to the base of the transistor 2782, and further results in the transistor 2782 and the power loop of the LED tube lamp remaining in a conducting state. Besides, since the OR gate 2763 keeps outputting the second high level voltage to cause the transistor 2746 to be conducting to the ground, the capacitor 2743 is unable to reach an enough voltage to trigger the Schmitt trigger 2744.

[00233] However, when the voltage signal on the resistor 2774 is smaller than the reference voltage, the comparator 2772 outputs a third low level voltage to the clock input end CLK of the D flip-flop 2762. In the meantime, since the initial output of the D flip-flop 2762 is a low level voltage (e.g., zero voltage), the D flip-flop 2762 outputs a low level voltage (at its output end Q) to the other input end of the OR gate 2763. Moreover, the Schmitt trigger 2744 connected by the input end of the OR gate 2763 also restores outputting the first low level voltage, the OR gate 2763 thus keeps outputting the second low level voltage to the base of the transistor 2782, and further results in the transistor 2782 to remain in a blocking state (or an off state) and the power loop of the LED tube lamp to remain in an open state. Still, since the OR gate 2763 keeps outputting the second low level voltage to cause the transistor 2764 to remain in a blocking state (or an off state), the capacitor 2743 is charged by the

driving signal through the resistor 2742 once again for next (pulse signal) detection.

[00234] In some embodiments, the cycle (or interval) of the pulse signal is determined by the values of the resistor 2742 and the capacitor 2743. In certain cases, the cycle of the pulse signal may include a value ranging from about 3 milliseconds to about 500 milliseconds or may be ranging from about 20 milliseconds to about 50 milliseconds. In some embodiments, the width (or period) of the pulse signal is determined by the values of the resistor 2745 and the capacitor 2743. In certain cases, the width of the pulse signal may include a value ranging from about 1 microsecond to about 100 microseconds or may be ranging from about 10 microseconds to about 20 microseconds. The Zener diode 2748 provides a protection function but it may be omitted in certain cases. The resistor 2744 may include two resistors connected in parallel based on the consideration of power consumption in certain cases, and its equivalent resistance may include a value ranging from about 0.1 ohm to about 5 ohm. The resistors 2776 and 2777 provides the function of voltage division to make the input of the comparator 2773 bigger than the reference voltage, such as 0.3V, but the value of the reference voltage is not limited thereto. The capacitor 2778 provides the functions of regulation and filtering. The diode 2775 limits the signal to be transmitted in one way. In addition, the installation detection module disclosed by the example embodiments may also be adapted to other types of LED lighting equipment with dual-end power supply, e.g., the LED lamp directly using commercial power as its external driving signal, the LED lamp using the signal outputted from the ballast as its external driving signal, etc. However, the invention is not limited to the above example embodiments.

[00235] According to some embodiments, the present invention further provides a detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket. The detection method includes: generating a first pulse signal by a detection pulse generating module, wherein the detection pulse generating module is configured in the LED tube lamp; receiving the first pulse signal through a detection result latching circuit by a switch circuit, and making the switch circuit conducting during the first pulse signal to cause a power loop of the LED tube lamp to be

conducting, wherein the switch circuit is on the power loop; and detecting a first sampling signal on the power loop by a detection determining circuit as the power loop being conductive, and comparing the first sampling signal with a predefined signal, wherein when the first sampling signal is greater than or equal to the predefined signal, the detection method further includes: outputting a first high level signal by the detection determining circuit; receiving the first high level signal by the detection result latching circuit and outputting a second high level signal; and receiving the second high level signal by the switch circuit and conducting to cause the power loop to remain conductive.

[00236] In some embodiments, when the first sampling signal is smaller than the predefined signal, the detection method further includes: outputting a first low level signal by the detection determining circuit; receiving the first low level signal by the detection result latching circuit and outputting a second low level signal; and receiving the second low level signal by the switch circuit and maintaining an off state of the switch circuit to cause the power loop to remain open.

[00237] In some embodiments, when the power loop remains open, the detection method further includes: generating a second pulse signal by the detection pulse generating module; receiving the second pulse signal through the detection result latching circuit by the switch circuit, and changing an off state of the switch circuit to a conducting state again during the second pulse signal to cause the power loop to be conducting once more; and detecting a second sampling signal on the power loop by the detection determining circuit as the power loop being conductive once more, and comparing the second sampling signal with the predefined signal, wherein when the second sampling signal is greater than or equal to the predefined signal, the detection method further includes: outputting the first high level signal by the detection determining circuit; receiving the first high level signal by the detection result latching circuit and outputting the second high level signal; and receiving the second high level signal by the switch circuit and maintaining a conducting state of the switch circuit to cause the power loop to remain conducting.

[00238] In some embodiments, when the second sampling signal is smaller than the predefined signal, the detection method further includes: outputting the first low

level signal by the detection determining circuit; receiving the first low level signal by the detection result latching circuit and outputting the second low level signal; and receiving the second low level signal by the switch circuit and maintaining an off state of the switch circuit to cause the power loop to remain open.

[00239] In some embodiments, a period (or a width) of the first pulse signal is between 10 microseconds – 1 millisecond, a period (or a width) of the second pulse signal is between 10 microseconds – 1 millisecond.

[00240] In some embodiments, a time interval between the first and the second pulse signals (or a cycle of the pulse signal) includes (X+Y)(T/2), where T is the cycle of the driving signal, X is an integer which is bigger than or equal to zero, $0<Y<1$.

[00241] In some embodiments, a period (or a width) of the first pulse signal is between 1 microsecond – 100 microseconds, a period (or a width) of the second pulse signal is between 1 microsecond – 100 microseconds.

[00242] In some embodiments, a time interval between the first and the second pulse signals (or a cycle of the pulse signal) is between 3 milliseconds – 500 milliseconds.

[00243] In some embodiments, at least two protection elements, such as two fuses, are respectively connected between the internal circuits of the LED tube lamp and the conductive pins of the LED tube lamp, and which are on the power loop of the LED tube lamp. In some embodiments, four fuses are used for an LED tube lamp having power-supplied at its both end caps respectively having two conductive pins. In this case, for example, two fuses are respectively connected between two conductive pins of one end cap and between one of the two conductive pins of this end cap and the internal circuits of the LED tube lamp; and the other two fuses are respectively connected between two conductive pins of the other end cap and between one of the two conductive pins of the other end cap and the internal circuits of the LED tube lamp. In some embodiment, the capacitance between a power supply (or an external driving source) and the rectifying circuit of the LED tube lamp may be ranging from 0 to about 100 pF. In some embodiments, the abovementioned installation detection module may be configured to use an external power supply.

[00244] According to the design of the power supply module, the external

driving signal may be a low frequency AC signal (e.g., commercial power), a high frequency AC signal (e.g., that provided by an electronic ballast), or a DC signal (e.g., that provided by a battery or external configured driving source), input into the LED tube lamp through a drive architecture of dual-end power supply. For the drive architecture of dual-end power supply, the external driving signal may be input by using only one end thereof as single-end power supply.

[00245] The LED tube lamp may omit the rectifying circuit in the power supply module when the external driving signal is a DC signal.

[00246] According to the design of the rectifying circuit in the power supply module, there may be a dual rectifying circuit. First and second rectifying circuits of the dual rectifying circuit are respectively coupled to the two end caps disposed on two ends of the LED tube lamp. The dual rectifying circuit is applicable to the drive architecture of dual-end power supply. Furthermore, the LED tube lamp having at least one rectifying circuit is applicable to the drive architecture of a low frequency AC signal, high frequency AC signal or DC signal.

[00247] The dual rectifying circuit may comprise, for example, two half-wave rectifier circuits, two full-wave bridge rectifying circuits or one half-wave rectifier circuit and one full-wave bridge rectifying circuit.

[00248] According to the design of the pin in the LED tube lamp, there may be two pins in single end (the other end has no pin), two pins in corresponding ends of two ends, or four pins in corresponding ends of two ends. The designs of two pins in single end and two pins in corresponding ends of two ends are applicable to a signal rectifying circuit design of the rectifying circuit. The design of four pins in corresponding ends of two ends is applicable to a dual rectifying circuit design of the rectifying circuit, and the external driving signal can be received by two pins in only one end or any pin in each of two ends.

[00249] According to the design of the filtering circuit of the power supply module, there may be a single capacitor, orπ filter circuit. The filtering circuit filers the high frequency component of the rectified signal for providing a DC signal with a low ripple voltage as the filtered signal. The filtering circuit also further comprises the LC filtering circuit having a high impedance for a specific frequency for conforming to

current limitations in specific frequencies of the UL standard. Moreover, the filtering circuit according to some embodiments further comprises a filtering unit coupled between a rectifying circuit and the pin(s) for reducing the EMI resulted from the circuit(s) of the LED tube lamp. The LED tube lamp may omit the filtering circuit in the power supply module when the external driving signal is a DC signal.

[00250] According to the design of the LED lighting module in some embodiments, the LED lighting module may comprise the LED module and the driving circuit or only the LED module. The LED module may be connected with a voltage stabilization circuit in parallel for preventing the LED module from over voltage. The voltage stabilization circuit may be a voltage clamping circuit, such as Zener diode, DIAC and so on. When the rectifying circuit has a capacitive circuit, in some embodiments, two capacitors are respectively coupled between two corresponding pins in two end caps and so the two capacitors and the capacitive circuit as a voltage stabilization circuit perform a capacitive voltage divider.

[00251] If there are only the LED module in the LED lighting module and the external driving signal is a high frequency AC signal, a capacitive circuit (e.g., having at least one capacitor) is in at least one rectifying circuit and the capacitive circuit is connected in series with a half-wave rectifier circuit or a full-wave bridge rectifying circuit of the rectifying circuit and serves as a current modulation circuit (or a current regulator) to modulate or to regulate the current of the LED module due to that the capacitor equates a resistor for a high frequency signal. Thereby, even different ballasts provide high frequency signals with different voltage logic levels, the current of the LED module can be modulated into a defined current range for preventing overcurrent. In addition, an energy-releasing circuit is connected in parallel with the LED module. When the external driving signal is no longer supplied, the energy-releasing circuit releases the energy stored in the filtering circuit to lower a resonance effect of the filtering circuit and other circuits for restraining the flicker of the LED module. In some embodiments, if there are the LED module and the driving circuit in the LED lighting module, the driving circuit may be a buck converter, a boost converter, or a buck-boost converter. The driving circuit stabilizes the current of the LED module at a defined current value, and the defined current value may be

modulated based on the external driving signal. For example, the defined current value may be increased with the increasing of the logic level of the external driving signal and reduced with the reducing of the logic level of the external driving signal. Moreover, a mode switching circuit may be added between the LED module and the driving circuit for switching the current from the filtering circuit directly or through the driving circuit inputting into the LED module.

[00252] A protection circuit may be additionally added to protect the LED module. The protection circuit detects the current and/or the voltage of the LED module to determine whether to enable corresponding over current and/or over voltage protection.

[00253] According to the design of the auxiliary power module of the power supply module, the energy storage unit may be a battery or a supercapacitor, connected in parallel with the LED module. The auxiliary power module is applicable to the LED lighting module having the driving circuit.

[00254] According to the design of the LED module of the power supply module, the LED module comprises plural strings of LEDs connected in parallel with each other, wherein each LED may have a single LED chip or plural LED chips emitting different spectrums. Each LEDs in different LED strings may be connected with each other to form a mesh connection.

[00255] In other words, the abovementioned features can be implemented in any combination to improve the LED tube lamp.

[00256] The above-mentioned exemplary features of the present invention can be accomplished in any combination to improve the LED tube lamp, and the above embodiments are described by way of example only. The present invention is not herein limited, and many variations are possible without departing from the spirit of the present invention and the scope as defined in the appended claims.

CLAIMS

What is claimed is:

1. An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

2. The installation detection circuit according to claim 1, wherein the pulse generating circuit comprises:

a first capacitor, one end connected to a driving signal;

a first resistor, one end connected to the other end of the first capacitor, the other

end the first resistor connected to a reference voltage;

a first buffer, having an input end and an output end, the input end connected to the other end of the first capacitor;

a second capacitor, one end connected to the output end of the first buffer;

a third capacitor, one end connected to the output end of the first buffer;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

3. The installation detection circuit according to claim 1, wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit.

4. The installation detection circuit according to claim 3, wherein when the detection determining circuit determines that the sampling signal is greater than or

equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

5. The installation detection circuit according to claim 3, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

6. The installation detection circuit according to claim 5, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.

7. The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a second capacitor, one end coupled to a driving signal;

a third capacitor, one end coupled to the driving signal;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end,

the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

8. The installation detection circuit according to claim 7, wherein the second buffer comprises two inverters connected in series.

9. The installation detection circuit according to claim 7, wherein the detection result latching circuit comprises:

a first D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit;

a fourth resistor, one end connected to the output end of the first D flip-flop, the other end of the fourth resistor connected to a reference voltage; and

a second OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first OR gate, the second input end connected to the output end of the first D flip-flop, the output end of the second OR gate connected to the switch circuit.

10. The installation detection circuit according to claim 7, wherein the switch circuit comprises:

a first transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

11. The installation detection circuit according to claim 7, wherein the detection determining circuit comprises:

a fifth resistor, one end connected to the switch circuit, the other end of the fifth resistor connected to a second end of the power loop; and

a first comparator, having a first input end, a second input end, and an output end, the first input end connected to the predefined signal, the second input end

connected to the one end of the fifth resistor, the output end of the first comparator connected to the detection result latching circuit.

12. The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a sixth resistor, one end connected to a driving signal;

a fourth capacitor, one end connected to the other end of the sixth resistor, the other end of the fourth capacitor connected to a reference voltage;

a Schmitt trigger, having an input end and an output end, the input end connected to the one end of the fourth capacitor, the output end connected to the detection result latching circuit;

a seventh resistor, one end connected to the one end of the fourth capacitor;

a second transistor, having a base, a collector, and an emitter, the collector connected to the other end of the seventh resistor, the emitter connected to a reference voltage; and

an eighth resistor, one end connected to the base of the second transistor, the other end of the eighth resistor connected to the detection result latching circuit and the switch circuit.

13. The installation detection circuit according to claim 12, wherein the pulse generating circuit further comprises:

a Zener diode, having an anode and a cathode, the anode connected to the other end of the fourth capacitor, the cathode connected to the one end of the fourth capacitor.

14. The installation detection circuit according to claim 12, wherein the detection result latching circuit comprises:

a second D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit; and

a third OR gate, having a first input end, a second input end, and an output end,

the first input end connected to the output end of the Schmitt trigger, the second input end connected to the output end of the second D flip-flop, the output end of the third OR gate connected to the other end of the eighth resistor and the switch circuit.

15. The installation detection circuit according to claim 12, wherein the switch circuit comprises:

a third transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

16. The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop; and

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to the predefined signal, the second input end connected to the one end of the ninth resistor, the output end of the second comparator connected to the detection result latching circuit.

17. The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop;

a second diode, having an anode and a cathode, the anode connected to the one end of the ninth resistor;

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to the predefined signal, the second input end connected to the cathode of the second diode, the output end of the second comparator connected to the detection result latching circuit;

a third comparator, having a first input end, a second input end, and an output end, the first input end connected to the cathode of the second diode, the second input

end connected to another predefined signal, the output end of the third comparator connected to the detection result latching circuit;

a tenth resistor, one end connected to the driving signal;

an eleventh resistor, one end connected to the other end of the tenth resistor and the second input end of the second comparator, the other end of the eleventh resistor connected to a reference voltage; and

a fifth capacitor, connected to the eleventh resistor in parallel.

18. The installation detection circuit according to claim 1, wherein the LED tube lamp comprises a lamp tube and a circuit board, and comprises an inductive element connected between two terminals respectively at two ends of the lamp tube for grounding or connecting to a reference potential, wherein one of the two terminals is connected to the circuit board.

19. The installation detection circuit according to claim 18, wherein the inductive element is an inductor.

20. The installation detection circuit according to claim 19, wherein one end of the inductor is directly electrically connected to the circuit board.

21. The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

22. An installation detection circuit configured in a light-emitting diode (LED) tube lamp, the installation detection circuit comprising:

means for generating one or more pulse signals;

means for detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket; and

a switch circuit coupled to the means for generating one or more pulse signals, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

23. The installation detection circuit according to claim 22, wherein the means for detecting is configured to detect a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the means for detecting.

24. The installation detection circuit according to claim 23, wherein when the means for detecting determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the means for detecting determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

25. The installation detection circuit according to claim 23, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the means for detecting.

26. The installation detection circuit according to claim 23, wherein the LED tube lamp is configured to receive an external driving signal and comprises a rectifying circuit for rectifying the external driving signal and a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit.

27. A detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket, the detection method comprising:

when at least one end of the LED tube lamp is installed on the lamp socket, generating one or more pulse signals by a pulse generating circuit, wherein the pulse generating circuit is configured in the LED tube lamp;

detecting a sampling signal on a power loop of the LED tube lamp by a detection determining circuit, to detect during the one or more pulse signals whether the other end of the LED tube lamp is properly installed on the lamp socket;

receiving the one or more pulse signals through a detection result latching circuit by a switch circuit, wherein the switch circuit is on the power loop; and

comparing the sampling signal with a predefined signal, wherein during the one or more pulse signals when the sampling signal is smaller than the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open.

28. The detection method according to claim 27, wherein the step of controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open comprises:

outputting a first low level signal by the detection determining circuit;

receiving the first low level signal by the detection result latching circuit and outputting a second low level signal; and

receiving the second low level signal by the switch circuit and maintaining an off state of the switch circuit to cause the power loop to be open.

29. The detection method according to claim 27, wherein during any of the one or more pulse signals when the sampling signal is greater than or equal to the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in a conducting state to cause the power

loop of the LED tube lamp to maintain a conducting state.

30. The detection method according to claim 29, wherein the step of controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state comprises:

outputting a first high level signal by the detection determining circuit;

receiving the first high level signal by the detection result latching circuit and outputting a second high level signal; and

receiving the second high level signal by the switch circuit and conducting the switch circuit to cause the power loop to maintain a conducting state.

31. The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 10 microseconds and 1 millisecond.

32. The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 1 microsecond and 100 microseconds.

ABSTRACT

An LED tube lamp is disclosed. An installation detection circuit is configured in the LED tube lamp configured to receive an external driving signal. The installation detection circuit includes: a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit. The installation detection circuit is further configured to: when it is detected during one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and when it is detected during one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

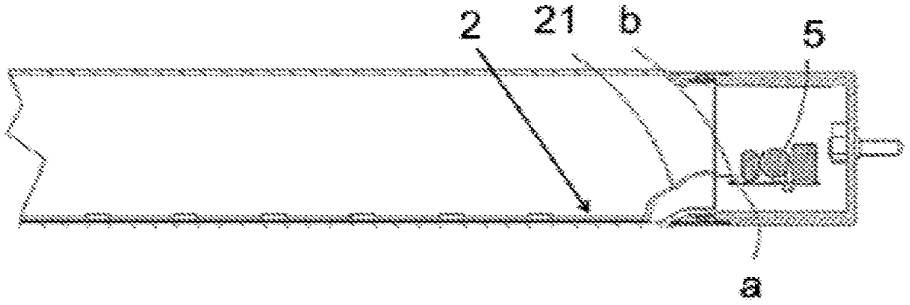


Fig. 1

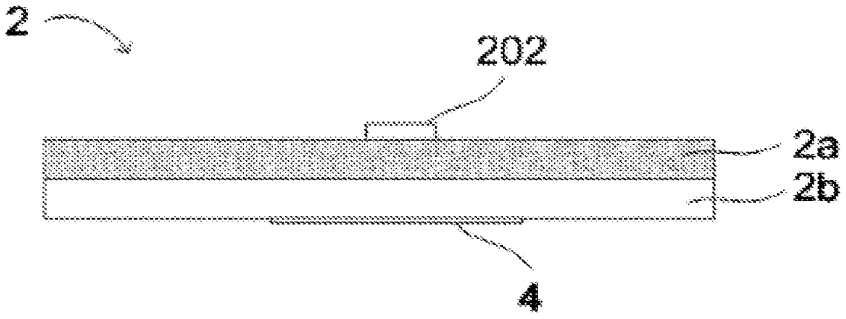


Fig. 2

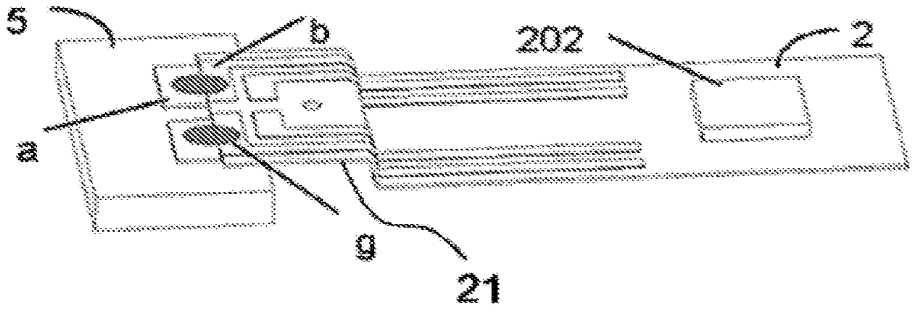


Fig. 3A

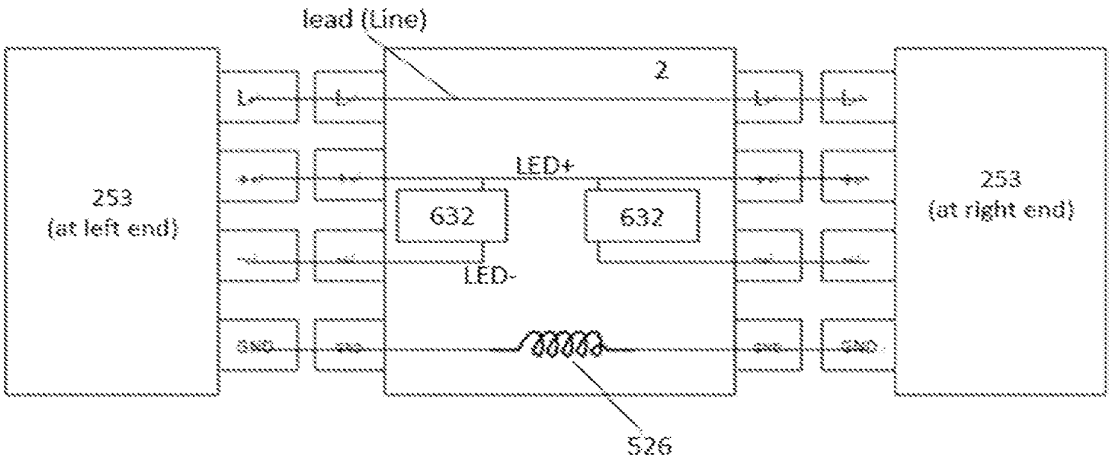


Fig. 3B

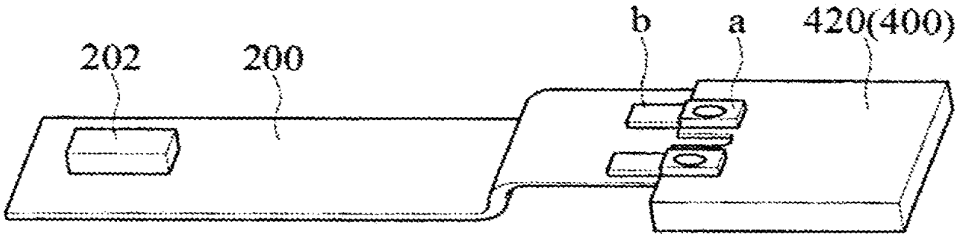


Fig. 4A

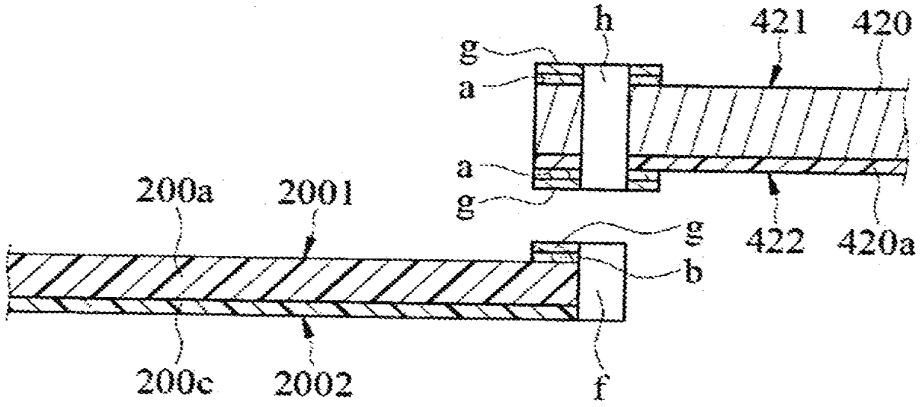


Fig. 4B

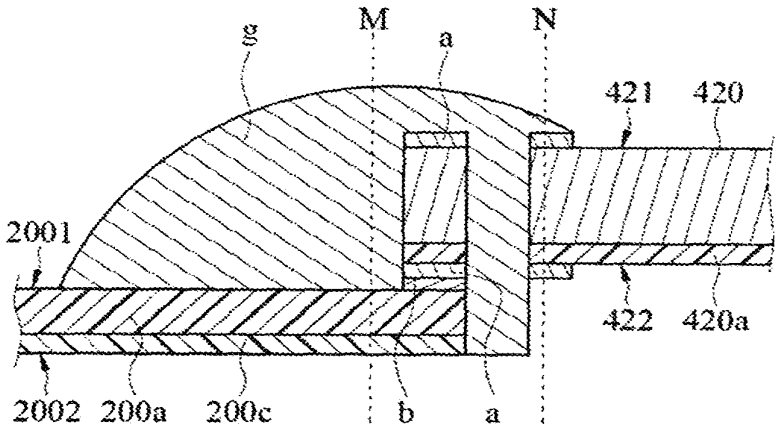

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N
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a

Fig. 4C

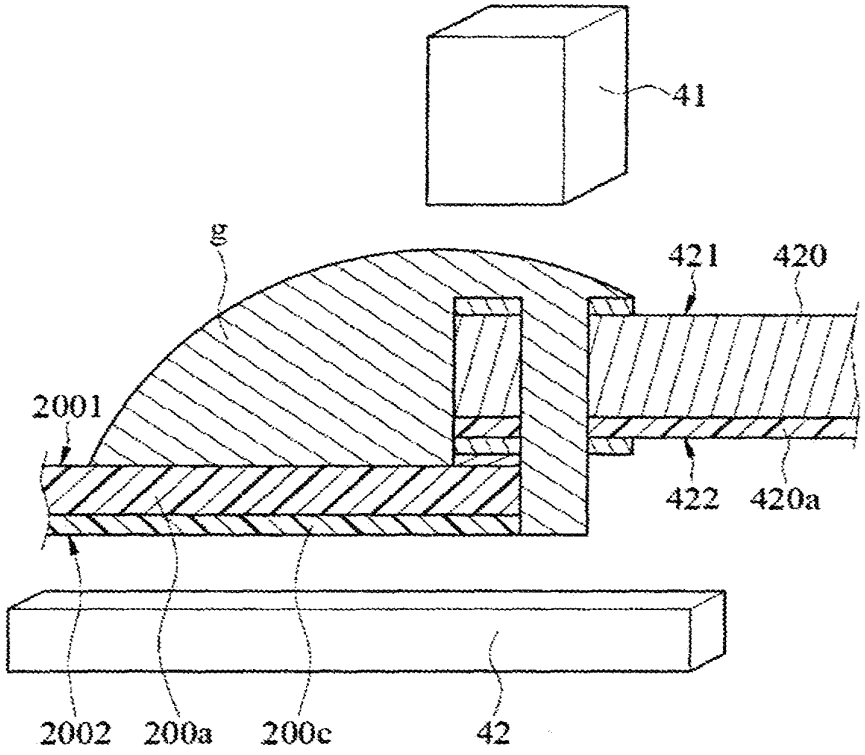

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200c
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Fig. 4D

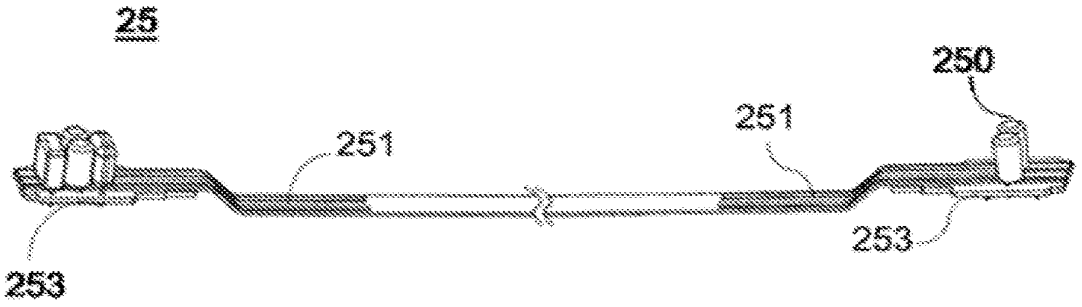


Fig. 5

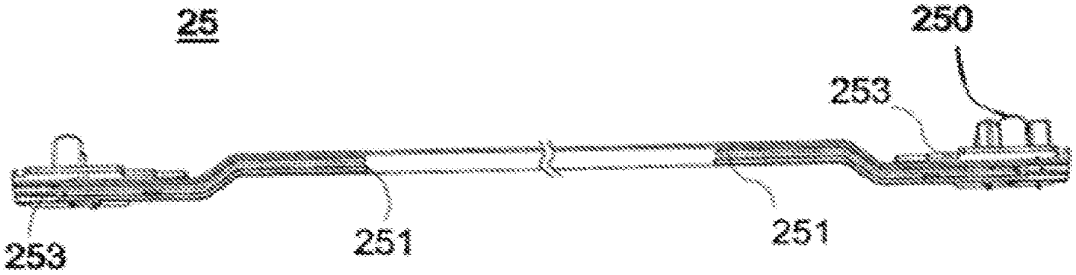


Fig. 6

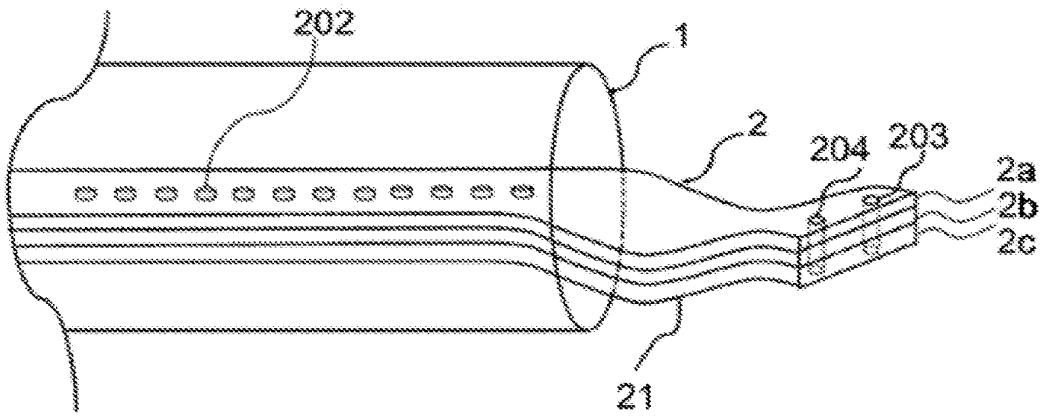


Fig. 7

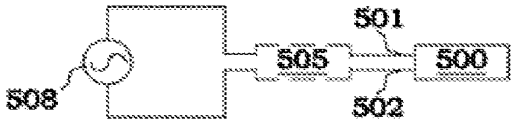


Fig. 8A



Fig. 8B

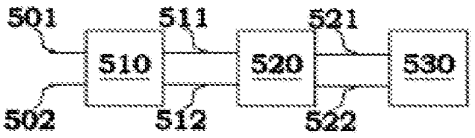


Fig. 8C

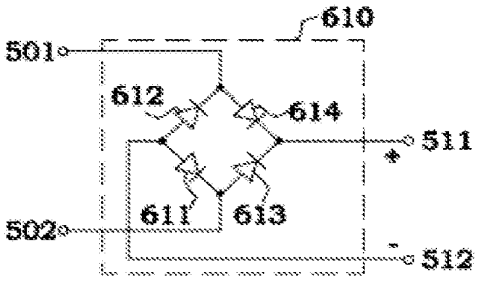


Fig. 9

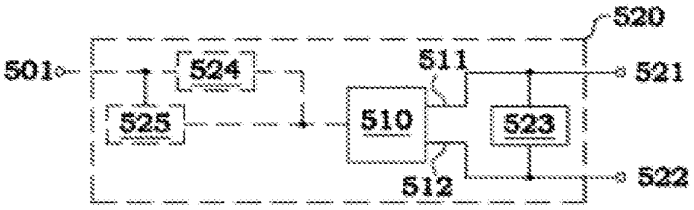


Fig. 10A

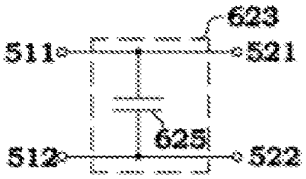


Fig. 10B

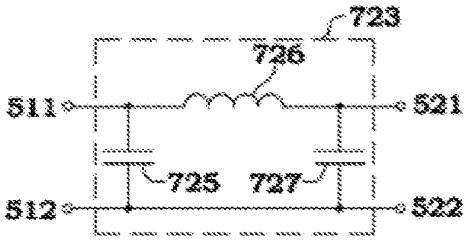


Fig. 10C

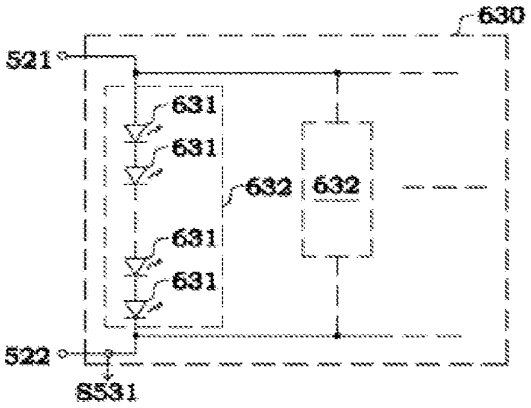


Fig. 11A

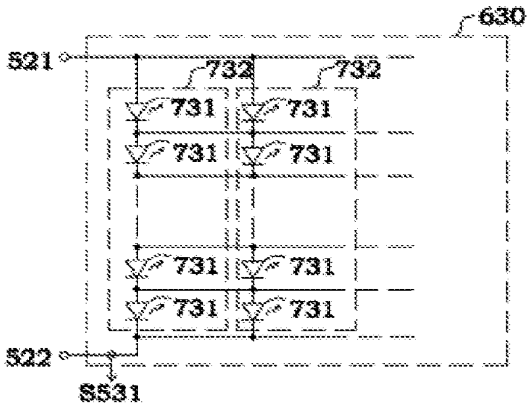


Fig. 11B

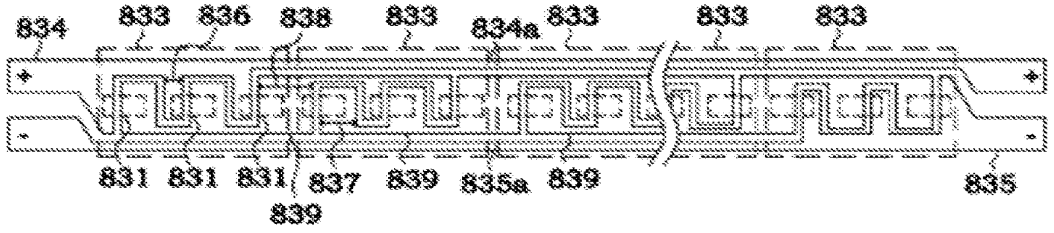


Fig. 11C

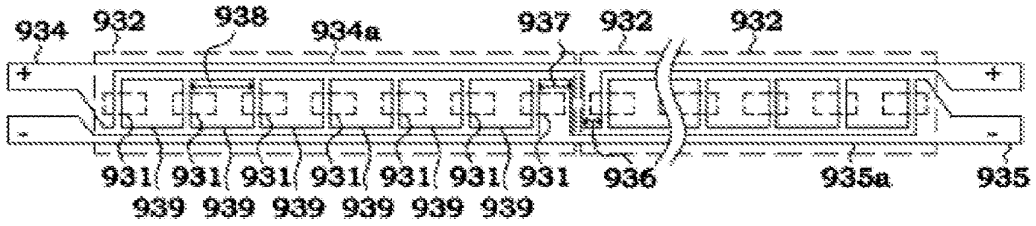


Fig. 11D

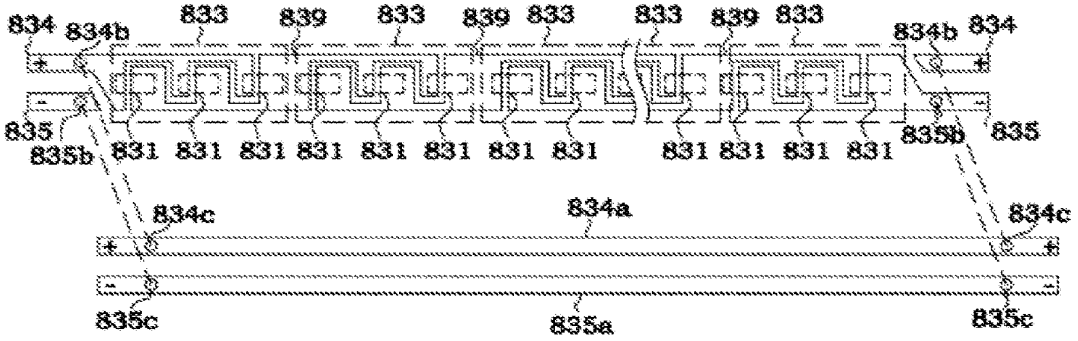


Fig. 11E

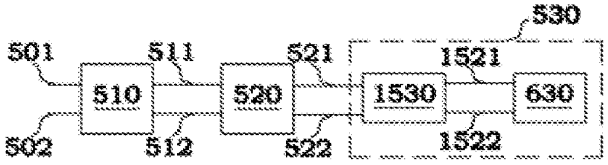


Fig. 12A

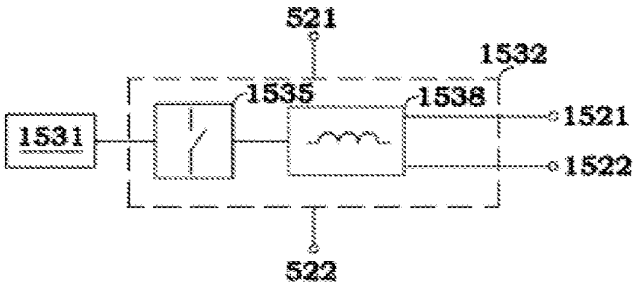


Fig. 12B

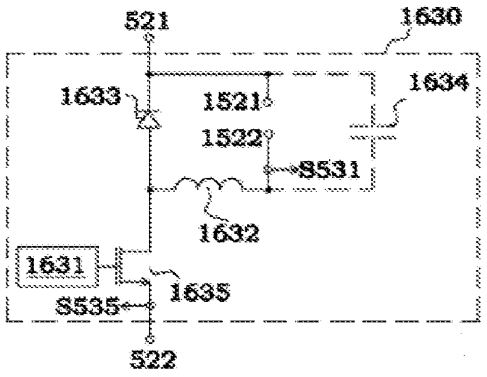


Fig. 12C

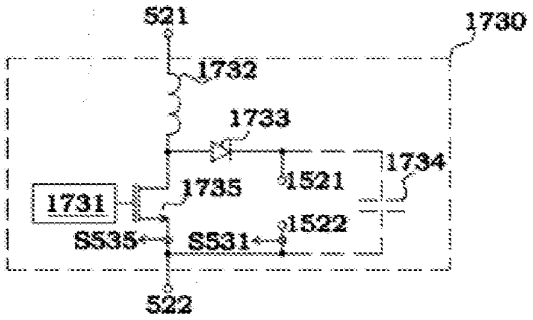


Fig. 12D

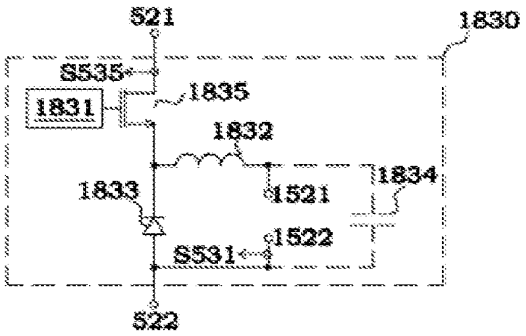


Fig. 12E

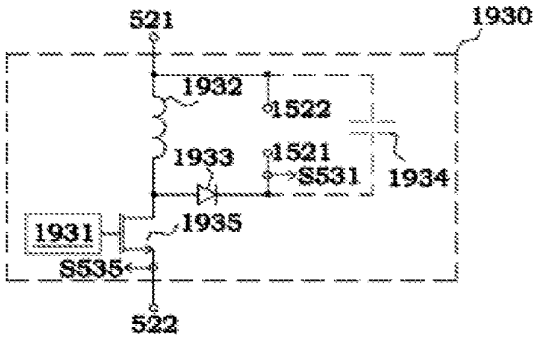


Fig. 12F

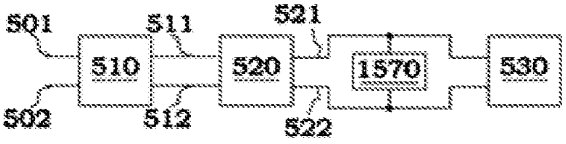


Fig. 13A

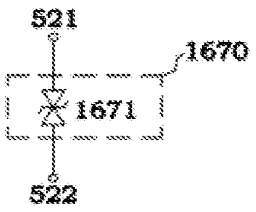


Fig. 13B

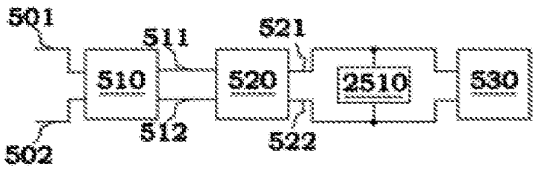


Fig. 14A

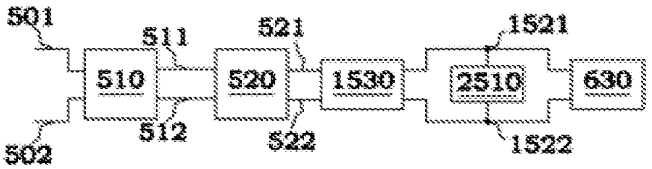


Fig. 14B

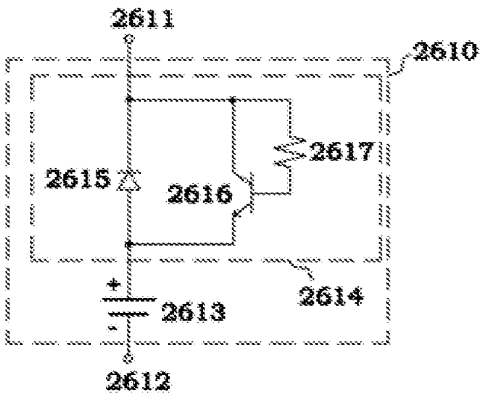


Fig. 14C

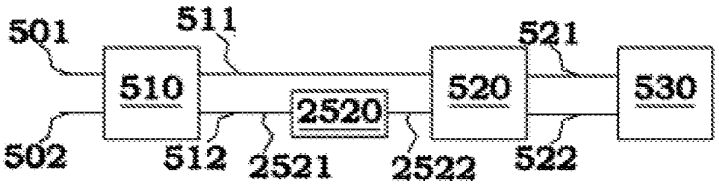


Fig. 15A

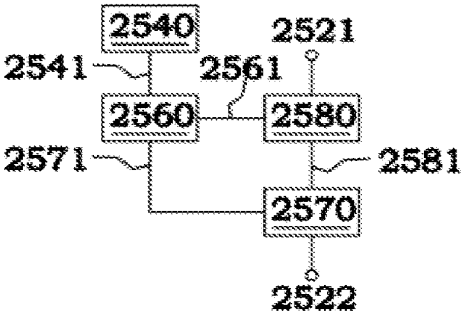


Fig. 15B

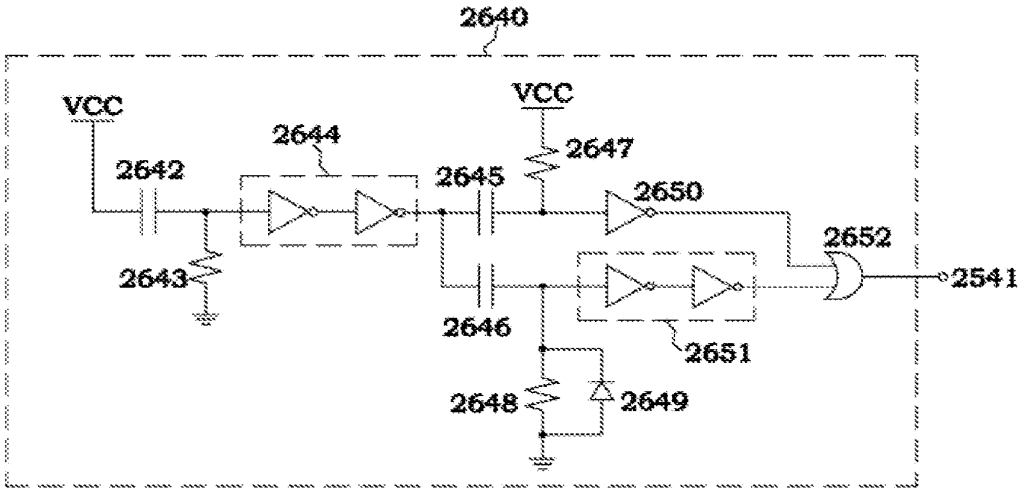


Fig. 15C

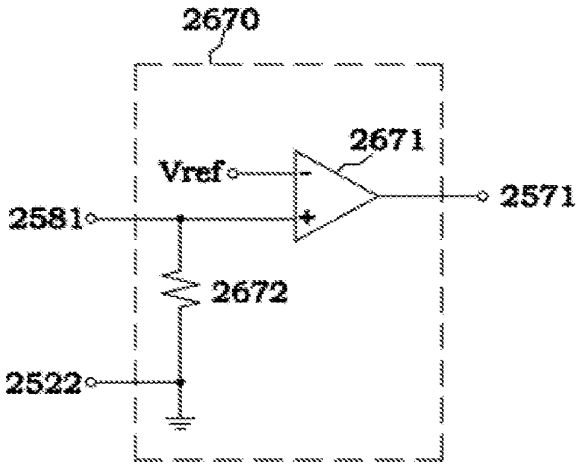


Fig. 15D

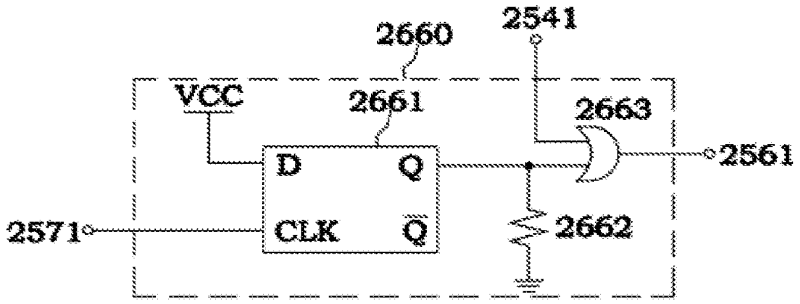


Fig. 15E

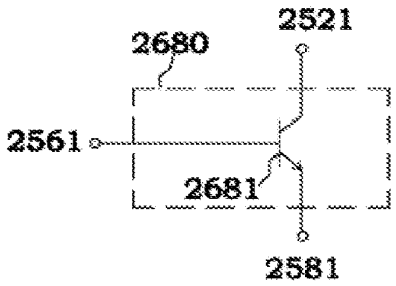


Fig. 15F

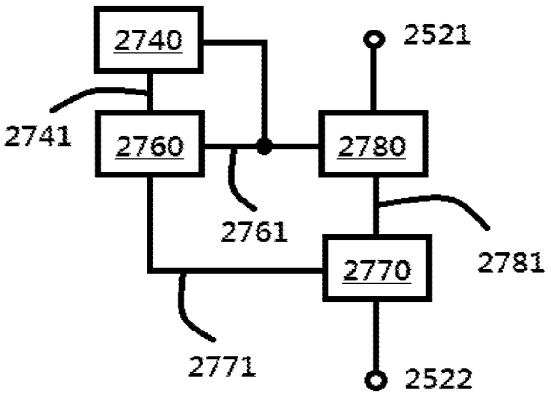


Fig. 15G

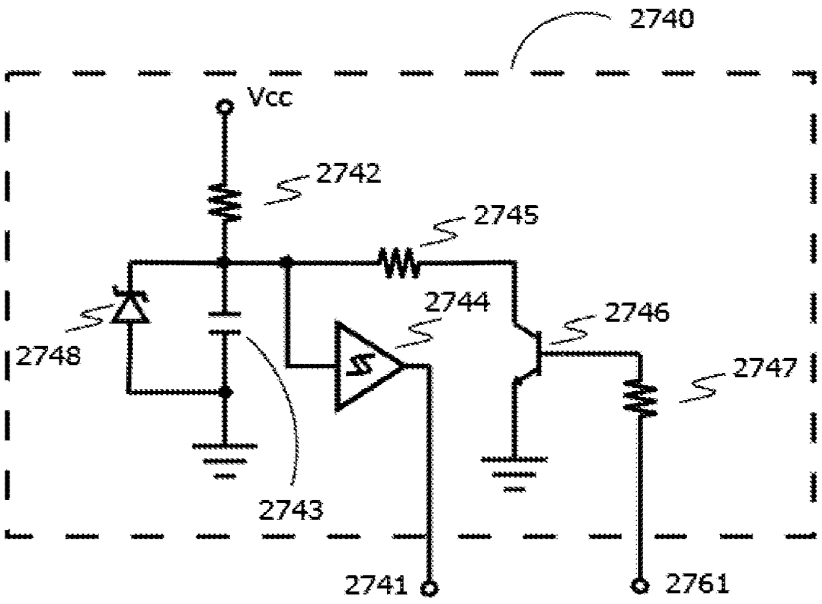


Fig. 15H

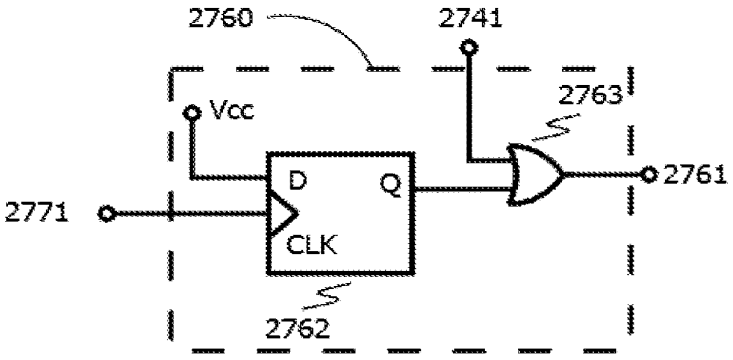


Fig. 15I

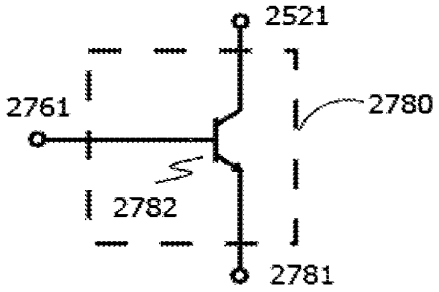


Fig. 15J

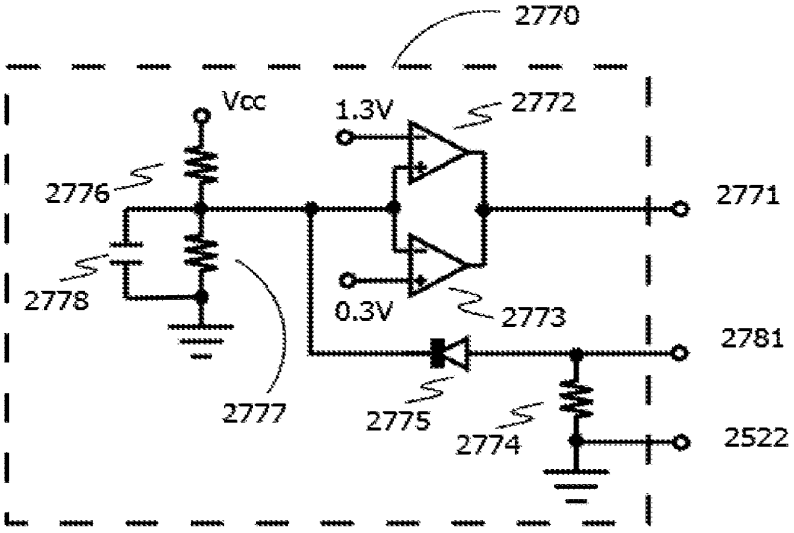


Fig. 15K

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xintong		Liu	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Jiaxing	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country i	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Aiming		Xiong	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Jiaxing	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country i	CN

Inventor 3 Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tao		Jiang	

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City	Jiaxing	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country [i]	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Feng		Zou	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Jiaxing	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country [i]	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	74712		
Email Address	pto@muirpatentlaw.com	Add Email	Remove Email

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Information:

Title of the Invention	LED TUBE LAMP		
Attorney Docket Number	SUP-101C-3	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	74712		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	15210989	2016-07-15
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15210989	Continuation in part of	15066645	2016-03-10
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15066645	Continuation in part of	14865387	2015-09-25

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15210989	Continuation in part of	15205011	2016-07-08
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15205011	Continuation in part of	15150458	2016-05-10
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15150458	Continuation in part of	14865387	2015-09-25
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15150458	Continuation in part of	14699138	2015-04-29

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410507660.9	CN	2014-09-28	

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410508899.8	CN	2014-09-28	

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410623355.6	CN	2014-11-06	

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410734425.5	CN	2014-12-05	

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510075925.7	CN	2015-02-12	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510104823.3	CN	2015-03-10	
201510134586.5	CN	2015-03-26	
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201510136796.8	CN	2015-03-27	
201510173861.4	CN	2015-04-14	
201510155807.7	CN	2015-04-03	
201510193980.6	CN	2015-04-22	
201510372375.5	CN	2015-06-26	
201510259151.3	CN	2015-05-19	
201510268927.8	CN	2015-05-22	
201510284720.x	CN	2015-05-29	
201510338027.6	CN	2015-06-17	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510315636.x	CN	2015-06-10	
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201510364735.7	CN	2015-06-26	
201510378322.4	CN	2015-06-29	
201510391910.1	CN	2015-07-02	
201510406595.5	CN	2015-07-10	
201510482944.1	CN	2015-08-07	
201510486115.0	CN	2015-08-08	
201510428680.1	CN	2015-07-20	
201510483475.5	CN	2015-08-08	
201510555543.4	CN	2015-09-02	
201510557717.0	CN	2015-09-06	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510595173.7	CN	2015-09-18	
201510530110.3	CN	2015-08-26	
201510499512.1	CN	2015-08-14	
201510448220.5	CN	2015-07-27	
201510645134.3	CN	2015-10-08	
201510680883.x	CN	2015-10-20	
201610327806.0	CN	2016-05-18	
201620089157.0	CN	2016-01-28	
201610420790.8	CN	2016-06-14	
201510848766.X	CN	2015-11-27	
201510903680.2	CN	2015-12-09	
201610132513.7	CN	2016-03-09	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201610142140.1	CN	2016-03-14	
201610452437.8	CN	2016-06-20	
201420602526.2	CN	2014-10-17	
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201510716899.1	CN	2015-10-29	
201510726365.7	CN	2015-10-30	
201510868263.9	CN	2015-12-02	
201610044148.4	CN	2016-01-22	
201610051691.7	CN	2016-01-26	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201610085895.2	CN	2016-02-15	
201610087627.4	CN	2016-02-16	
201610281812.7	CN	2016-04-29	
201510705222.8	CN	2015-10-27	
201510726484.2	CN	2015-10-30	
201610050944.9	CN	2016-01-26	
201610098424.5	CN	2016-02-23	
201610120993.5	CN	2016-03-03	
201610876593.7	CN	2016-10-08	

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Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD		
Mailing Address Information For Applicant:			
Address 1	No.1288 Jiachuang Rd. Xiuzhou Area		
Address 2	Jiaxing, Zhejiang, People's Republic of China.		
City	Jiaxing	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Mailing Address Information For Non-Applicant Assignee:			
Address 1			
Address 2			
City		**State/Province**	
Country [i]		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

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NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ali Imam/			Date (YYYY-MM-DD)	2016-10-31
First Name	Ali	Last Name	Imam	Registration Number	58755

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Co o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

COMBINED DECLARATION (37 CFR §1.63) FOR UTILITY PATENT APPLICATION AND ASSIGNMENT FORM[1]

The undersigned acknowledge that this document is being used both as an assignment of the invention and as the declaration (37 CFR 1.63) for a Utility or Design Application.

WHEREAS, the undersigned inventors have invented:

Title: LED TUBE LAMP

for which Inventors are about to make or have made a United States or International application for patent.

WHEREAS, as a below named inventor(s), I/(we) hereby declare that:

Section I. Declaration

This declaration is directed to:

☒ The attached U.S. non-provisional patent application, or

☐ U.S. non-provisional patent application number _____, filed on _____, or

☐ PCT international patent application number _____, filed on _____.

The above-identified application was made or authorized to be made by me (us).

[1] This form requires the use of an Application Data Sheet.

I (we) believe that I am (we are) the original inventor (original joint inventors) of a claimed invention in the above-identified application.

I (we) hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims.

I acknowledge that I am aware of the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

Section II. Assignment

In consideration of good and valuable consideration paid to each of the undersigned, collectively referred to in Section II as Assignors in this section, hereby sell(s) and assign(s) to

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD.

having an address at **No.1288 Jiachuang Rd. Xiuzhou Area, Jiaxing, Zhejiang, China** (hereinafter designated in this section as the Assignee), the entire (100%) right, title and interest for the United States as defined in 35 USC §100, in the invention described in the application identified in Section I of this document.

Assignor hereby confirms any prior assignment to Assignee, and to the extent that Assignor has not already done so, agrees to assign, and hereby does, sell, assign and transfer unto Assignee and its successors in interest, the full and exclusive right, title and interest in the United States of America and throughout the world, including the right to claim priority under the laws of the United States, the Paris Convention, and any foreign countries, to the inventions as described in the aforesaid application, to the aforesaid application itself, and all divisions, continuations, continuations-in-part, or other applications claiming priority directly or indirectly from the aforesaid application, and any United States or foreign Letters Patent, utility model, or other similar rights which may be granted thereon, including

reissues, reexaminations and extensions thereof, and all copyright rights throughout the world in the aforesaid application and the subject matter disclosed therein, these rights, title and interest to be held and enjoyed by Assignee to the full end of the term for which the Letters Patent, utility model, or other similar rights, are granted and any extensions thereof as fully and entirely as the same would have been held by Assignor had this assignment and sale not been made, and the right to sue for, and recover for past infringements of, or liabilities for, any of the rights relating to any of the applications, patents, utility models, or other similar rights, resulting therefrom, and the copyright rights;

Assignor hereby covenants and agrees to execute all instruments or documents required or requested for the making and prosecution of any applications of any type for patent, utility model, or other similar rights, and for copyright, in the United States and in all foreign countries including, but not limited to, any provisional, continuation, continuation-in-part, divisional, renewal or substitute thereof, and as to letters patent any reissue, re-examination, or extension thereof, and for litigation regarding, or for the purpose of protecting title and to the said invention, the United States application for patent, or Letters Patent therefor, and to testify in support thereof, for the benefit of Assignee without further or other compensation than that above set forth;

Assignor hereby covenants that no assignment, sale, license, agreement or encumbrance has been or will be entered into which would conflict with this Assignment; and

Assignor hereby requests the United States Patent and Trademark Office to issue the Letters Patent of the United States of America to Assignee, and requests that any official of any country or countries foreign to the United States, whose duty it is to issue or grant patents and applications as aforesaid, to issue the Letters Patent, Utility Model Registration or other similar right to Assignee.

The undersigned hereby grant(s) the law firm of **Muir Patent Law, PLLC**, the power to insert on this Declaration and Assignment any further identification or formal correction which may be necessary or desirable in order to comply with the rules of the U.S. Patent and Trademark Office for filing and recordation of this document.

Inventor(s)/Assignor(s) Signature(s) for Section II.

LEGAL NAME OF FIRST INVENTOR/ASSIGNOR	Family Name	First Given Name	Second Given Name
	Liu	Xintong	

SIGNATURE Liu Xintong DATE 10/27/2016

LEGAL NAME OF SECOND INVENTOR/ASSIGNOR	Family Name	First Given Name	Second Given Name
	Xiong	Aiming	

SIGNATURE Xiong Aiming DATE 10/27/2016

LEGAL NAME OF THIRD INVENTOR/ASSIGNOR	Family Name	First Given Name	Second Given Name
	Jiang	Tao	

SIGNATURE Jiang Tao DATE 10/26/2016

LEGAL NAME OF FIRST INVENTOR/ASSIGNOR	Family Name	First Given Name	Second Given Name
	Zou	Feng	

SIGNATURE Zou Feng DATE 12-27/2014

SCORE Placeholder Sheet for IFW Content

Application Number: 15339221 Document Date: 10/31/2016

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

To access the documents in the SCORE database, refer to instructions below.

At the time of document entry (noted above):

- Examiners may access SCORE content via the eDAN interface.
- Other USPTO employees can bookmark the current SCORE URL (http://Score.uspto.gov/ScoreAccessWeb/).
- External customers may access SCORE content via the Public and Private PAIR interfaces.

Form Revision Date: September 30, 2013

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/339,221

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	32 minus 20 =	* 12			OR	x 80 =	960
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 420 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2560

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/339,221	10/31/2016	1629	2560	SUP-101C-3	32	3

CONFIRMATION NO. 3876

FILING RECEIPT

74712
Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

OC000000087514175

Date Mailed: 12/01/2016

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Xintong Liu, Jiaxing, CHINA;
Aiming Xiong, Jiaxing, CHINA;
Tao Jiang, Jiaxing, CHINA;
Feng Zou, Jiaxing, CHINA;

Applicant(s)

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD, Jiaxing, CHINA;

Power of Attorney: The patent practitioners associated with Customer Number 74712

Domestic Priority data as claimed by applicant

This application is a CIP of 15/210,989 07/15/2016
which is a CIP of 15/066,645 03/10/2016 PAT 9497821
which is a CIP of 14/865,387 09/25/2015
and said 15/210,989 07/15/2016
is a CIP of 15/205,011 07/08/2016
which is a CIP of 15/150,458 05/10/2016
which is a CIP of 14/865,387 09/25/2015
and is a CIP of 14/699,138 04/29/2015 PAT 9480109

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201410507660.9 09/28/2014
CHINA 201410508899.8 09/28/2014
CHINA 201410623355.6 11/06/2014
CHINA 201410734425.5 12/05/2014
CHINA 201510075925.7 02/12/2015

CHINA 201510104823.3 03/10/2015
CHINA 201510134586.5 03/26/2015
CHINA 201510133689.X 03/25/2015
CHINA 201510136796.8 03/27/2015
CHINA 201510173861.4 04/14/2015
CHINA 201510155807.7 04/03/2015
CHINA 201510193980.6 04/22/2015
CHINA 201510372375.5 06/26/2015
CHINA 201510259151.3 05/19/2015
CHINA 201510268927.8 05/22/2015
CHINA 201510284720.X 05/29/2015
CHINA 201510338027.6 06/17/2015
CHINA 201510315636.X 06/10/2015
CHINA 201510373492.3 06/26/2015
CHINA 201510364735.7 06/26/2015
CHINA 201510378322.4 06/29/2015
CHINA 201510391910.1 07/02/2015
CHINA 201510406595.5 07/10/2015
CHINA 201510482944.1 08/07/2015
CHINA 201510486115.0 08/08/2015
CHINA 201510428680.1 07/20/2015
CHINA 201510483475.5 08/08/2015
CHINA 201510555543.4 09/02/2015
CHINA 201510557717.0 09/06/2015
CHINA 201510595173.7 09/18/2015
CHINA 201510530110.3 08/26/2015
CHINA 201510499512.1 08/14/2015
CHINA 201510448220.5 07/27/2015
CHINA 201510645134.3 10/08/2015
CHINA 201510680883.X 10/20/2015
CHINA 201610327806.0 05/18/2016
CHINA 201620089157.0 01/28/2016
CHINA 201610420790.8 06/14/2016
CHINA 201510848766.X 11/27/2015
CHINA 201510903680.2 12/09/2015
CHINA 201610132513.7 03/09/2016
CHINA 201610142140.1 03/14/2016
CHINA 201610452437.8 06/20/2016
CHINA 201420602526.2 10/17/2014
CHINA 201510617370.4 09/25/2015
CHINA 201510716899.1 10/29/2015
CHINA 201510726365.7 10/30/2015
CHINA 201510868263.9 12/02/2015
CHINA 201610044148.4 01/22/2016
CHINA 201610051691.7 01/26/2016

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: No

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 11/29/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/339,221**

Projected Publication Date: 03/09/2017

Non-Publication Request: No

Early Publication Request: No

Title

LED TUBE LAMP

Preliminary Class

514

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Liu et al.		Attorney Docket:	SUP-101C-3
Serial Number:	15/339,221	Group Art Unit:	2844
Filed:	October 31, 2016	Examiner:	TBD

Confirmation Number: 3876

Title: LED TUBE LAMP

REQUEST FOR A FILING RECEIPT CORRECTION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/Madam:

This is a request for a filing receipt correction to list all priority claims filed with original ADS on October 31, 2016. The filing receipt received on December 1, 2016 includes a partial list.

Applicant herewith submits the original Application Data Sheet filed on December 1, 2016.

Should the Examiner wish to further discuss this application with Applicant, the Examiner is encouraged to contact applicant's representative whose telephone number is listed below.

In the event any fees are required in connection with this paper, please charge the Deposit Account No. 50-4574.

Respectfully submitted,

/Ali Imam /

MUIR PATENT LAW, PLLC.
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

Ali Imam
Registration No. 58,755
Tel: (703) 757-7880
Fax: (703) 757-7447

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xintong		Liu	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	Jiaxing	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country i	CN

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Aiming		Xiong	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Jiaxing	Country of Residence i	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country i	CN

Inventor 3 Remove

Legal Name

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tao		Jiang	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Jiaxing	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country [i]	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Feng		Zou	

Residence Information (Select One) US Residency ◉ Non US Residency Active US Military Service

City	Jiaxing	Country of Residence [i]	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China
City	Jiaxing City
State/Province	
Postal Code	
Country [i]	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	74712		
Email Address	pto@muirpatentlaw.com	Add Email	Remove Email

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Information:

Title of the Invention	LED TUBE LAMP		
Attorney Docket Number	SUP-101C-3	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	74712		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	15210989	2016-07-15
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15210989	Continuation in part of	15066645	2016-03-10
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15066645	Continuation in part of	14865387	2015-09-25

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15210989	Continuation in part of	15205011	2016-07-08
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15205011	Continuation in part of	15150458	2016-05-10
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15150458	Continuation in part of	14865387	2015-09-25
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15150458	Continuation in part of	14699138	2015-04-29
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.			Add

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410507660.9	CN	2014-09-28	
			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410508899.8	CN	2014-09-28	
			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410623355.6	CN	2014-11-06	
			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201410734425.5	CN	2014-12-05	
			Remove
Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510075925.7	CN	2015-02-12	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510104823.3	CN	2015-03-10	
201510134586.5	CN	2015-03-26	
201510133689.x	CN	2015-03-25	
201510136796.8	CN	2015-03-27	
201510173861.4	CN	2015-04-14	
201510155807.7	CN	2015-04-03	
201510193980.6	CN	2015-04-22	
201510372375.5	CN	2015-06-26	
201510259151.3	CN	2015-05-19	
201510268927.8	CN	2015-05-22	
201510284720.x	CN	2015-05-29	
201510338027.6	CN	2015-06-17	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510315636.x	CN	2015-06-10	
201510373492.3	CN	2015-06-26	
201510364735.7	CN	2015-06-26	
201510378322.4	CN	2015-06-29	
201510391910.1	CN	2015-07-02	
201510406595.5	CN	2015-07-10	
201510482944.1	CN	2015-08-07	
201510486115.0	CN	2015-08-08	
201510428680.1	CN	2015-07-20	
201510483475.5	CN	2015-08-08	
201510555543.4	CN	2015-09-02	
201510557717.0	CN	2015-09-06	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201510595173.7	CN	2015-09-18	
201510530110.3	CN	2015-08-26	
201510499512.1	CN	2015-08-14	
201510448220.5	CN	2015-07-27	
201510645134.3	CN	2015-10-08	
201510680883.x	CN	2015-10-20	
201610327806.0	CN	2016-05-18	
201620089157.0	CN	2016-01-28	
201610420790.8	CN	2016-06-14	
201510848766.X	CN	2015-11-27	
201510903680.2	CN	2015-12-09	
201610132513.7	CN	2016-03-09	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201610142140.1	CN	2016-03-14	
201610452437.8	CN	2016-06-20	
201420602526.2	CN	2014-10-17	
201510530110.3	CN	2015-08-26	
201510499512.1	CN	2015-08-14	
201510617370.4	CN	2015-09-25	
201510645134.3	CN	2015-10-08	
201510716899.1	CN	2015-10-29	
201510726365.7	CN	2015-10-30	
201510868263.9	CN	2015-12-02	
201610044148.4	CN	2016-01-22	
201610051691.7	CN	2016-01-26	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)
201610085895.2	CN	2016-02-15	
201610087627.4	CN	2016-02-16	
201610281812.7	CN	2016-04-29	
201510705222.8	CN	2015-10-27	
201510726484.2	CN	2015-10-30	
201610050944.9	CN	2016-01-26	
201610098424.5	CN	2016-02-23	
201610120993.5	CN	2016-03-03	
201610876593.7	CN	2016-10-08	

Remove

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date o f filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD		
Mailing Address Information For Applicant:			
Address 1	No.1288 Jiachuang Rd. Xiuzhou Area		
Address 2	Jiaxing, Zhejiang, People's Republic of China.		
City	Jiaxing	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Mailing Address Information For Non-Applicant Assignee:			
Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Ali Imam/			Date (YYYY-MM-DD)	2016-10-31
First Name	Ali	Last Name	Imam	Registration Number	58755

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Co o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	28274515
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman/Amy Dean
Filer Authorized By:	Bradley E. Edelman
Attorney Docket Number:	SUP-101C-3
Receipt Date:	06-FEB-2017
Filing Date:	31-OCT-2016
Time Stamp:	15:25:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	SUP-101C-3_filing_receipt_correction_signed.pdf	61535 402589183fe771f76bfc7346f30d7c169c40fb90	no	2

Warnings:

Information:					
2	Application Data Sheet	SUP-101C-3_ADS.pdf	1505014 2c2b56d6db082fddd5aa5e673b4c831d363f1ab0	no	13
Warnings:					
Information:					
			Total Files Size (in bytes):	1566549	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3

CONFIRMATION NO. 3876

PUBLICATION NOTICE

74712
Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

OC00000089782732

Title:LED TUBE LAMP

Publication No.US-2017-0067627-A1
Publication Date:03/09/2017

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

74712 7590 04/04/2017

Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

EXAMINER
TRAN, ANH Q

ART UNIT	PAPER NUMBER
2844	

NOTIFICATION DATE	DELIVERY MODE
04/04/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
pto@muirpatentlaw.com

Office Action Summary	Application No. 15/339,221	Applicant(s) LIU ET AL.	
	Examiner ANH TRAN	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10/31/2016*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-32* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-7,9-11 and 21-32* is/are rejected.

8)☒ Claim(s) *8 and 12-20* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *10/31/16* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☒ All b)☐ Some** c)☐ None of the:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file

provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(l)(1) - 706.02(l)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

3. Claims 1-7, 9-11, 21-32 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-29 of U.S. Patent No. 9,497,821. Although the claims at issue are not identical, they are not patentably distinct from each other because the claim recitations are merely reworded to recite the same limitation in different language and some of the limitations have been grouped in a slightly different manner but still overall set forth the same limitations. All the recited elements and limitations can be found in claims 1-29 of U.S. Patent No. 9,497,821. For examples:

1) all the elements and limitations of claim 1 can be found in claims 1, 2, 23 and 24, also, in claims 33 and 35 of U.S. Patent No. 9,497,821.

2) all the elements and limitations of claims 2 and 7 can be found in claims 3 and 13 of U.S. Patent No. 9,497,821.

3) all the elements and limitations of claims 3 and 4 can be found in claims 1, 2, 15, 23 and 24 of U.S. Patent No. 9,497,821.

Furthermore, the U.S. Patent No. 9,497,821 did not discloses in the claims, wherein a period of each of the one or more pulse signals is between 10 microseconds and 1 millisecond or 1 microsecond and 100 microseconds. It would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a period of each of the one or more pulse signals between 10 microseconds and 1 millisecond or 1 microsecond and 100 microseconds, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Allowable Subject Matter

4. Claims 8, 12-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH TRAN whose telephone number is (571)272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Taningco can be reached on 571-272-2048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ANH TRAN/
Primary Examiner, Art Unit 2844
3/28/17

Notice of References Cited	Application/Control No. 15/339,221	Applicant(s)/Patent Under Reexamination LIU ET AL.	
	Examiner ANH TRAN	Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9,497,821 B2	11-2016	Liu; Xintong	F21K9/27	1/1
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/28/2017								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	O								
	9	✓								
	10	✓								
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	21	✓								
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	27	✓								
	28	✓								
	29	✓								
	30	✓								
	31	✓								
	32	✓								

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	35	liu-xintong.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2016/07/28 15:10
S2	93	US-20020044456-$.DID. OR US-20020176262-$.DID. OR US-20030102819-$.DID. OR US-20030231485-$.DID. OR US-20040095078-$.DID. OR US-20040189218-$.DID. OR US-20050128751-$.DID. OR US-20050162850-$.DID. OR US-20050207166-$.DID. OR US-20050213321-$.DID. OR US-20070001709-$.DID. OR US-20070145915-$.DID. OR US-20070210687-$.DID. OR US-20070274084-$.DID. OR US-20080030981-$.DID. OR US-20080192476-$.DID. OR US-20080278941-$.DID. OR US-20090161359-$.DID. OR US-20100253226-$.DID. OR US-20110090684-$.DID. OR US-20110148313-$.DID. OR US-20110216538-$.DID. OR US-20120069556-$.DID. OR US-20120106157-$.DID. OR US-20120153873-$.DID. OR US-20130170245-$.DID. OR US-20130182425-$.DID. OR US-20130200797-$.DID. OR US-20140071667-$.DID. OR US-20140153231-$.DID. OR US-20140226320-$.DID. OR US-20150009688-$.DID. OR US-5575459-$.DID. OR US-5921660-$.DID. OR US-6127783-$.DID. OR US-6609813-$.DID. OR US-6796680-$.DID. OR US-7033239-$.DID. OR US-8360599-$.DID. OR US-8579463-$.DID. OR US-20110038146-$.DID. OR US-20130050998-$.DID. OR US-20110057572-$.DID. OR US-20120235578-$.DID. OR WO-2013125803-$.DID. OR WO-2014001475-$.DID. OR WO-2015036478-$.DID. OR WO-2011132120-$.DID.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT	OR	OFF	2016/07/28 15:12
S3	26728	((LED.u/c. or light or lamp or bulb) NEAR1 (tube or tubular)) SAME (LED.u/c. or (light	US-PGPUB; USPAT;	OR	ON	2016/07/28 16:09

		adj emitting adj diode) or (light-emitting adj diode))	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S4	393	S3 and ((end$2 adj1 cap) SAME (pin or bi-pin or bipin))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/28 16:10
S5	151	S4 and (rectif$4 or rectific$5)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/28 16:12
S6	0	S5 and ((detect$3 or sens$3 or monitor$3) WITH ((connect$3 or contact$3 or install$4) NEAR2 electric$4 NEAR2 (good or bad or proper$4 or correct$4 or incorrect$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/28 16:17
S7	29	S5 and ((detect$3 or sens$3 or monitor$3) NEAR3 (connect$3 or contact$3 or install$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/28 16:18
S8	2	("8459831" | "8749167").PN. OR ("9163818").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/28 17:07
S9	13	("20100045187" | "20100156324" | "20110068703" | "20110176297" | "20120032610" | "20120126703" | "20120139421" | "20120181952" | "6525914" | "7800316" | "7994725" | "8147091").PN. OR ("8749167").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/28 17:12
S10	88	((LED.u/c. or light or lamp or bulb) NEAR1 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)) SAME ((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/28 20:18
S11	16	S10 AND ((current or volt$3) NEAR2 (sens$3 or detect$3 or monitor$3 or measur$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/28 20:20
S12	17	("20050162101" | "20110149563" | "20110149564" | "20110176297" | "20110228526" | "20120051040" | "20120146513" | "20120155074" | "20120181952" | "20120235556" |	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/28 21:29

		"20120242241" | "20130127327" | "20130241443" | "20140055029" | "5691603" | "6100644" | "6144445").PN. OR ("9277604").URPN.				
S13	17	("20050162101" | "20110149563" | "20110149564" | "20110176297" | "20110228526" | "20120051040" | "20120146513" | "20120155074" | "20120181952" | "20120235556" | "20120242241" | "20130127327" | "20130241443" | "20140055029" | "5691603" | "6100644" | "6144445").PN. OR ("9277604").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/28 21:47
S14	4	("20140225519" | "8664880" | "8760064" | "9232578").PN. OR ("9277603").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/28 21:47
S16	2	(("20130147350") or ("20110260622")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/28 22:00
S17	1139	315/$.ccls. AND (((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 14:36
S18	1	S17 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME ((volt$3 or current) NEAR3 (sens$3 or detect$3 or monitor$3 or measur$3 or determin$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 14:41
S19	10	("20100289419" | "20110149563" | "20110176297" | "20120043892" | "3685003" | "5412550" | "5752842" | "7530833" | "8147091" | "8459831").PN. OR ("8847475").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/07/29 15:38
S20	6	S17 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME (install$5 or insert$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 16:07
S21	15	S17 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) NEAR3 (circuit or element or device or unit or module or switch$2)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 16:08
S22	9	S17 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) SAME ((install$5 or insert$4)) WITH (lampholder or socket or ((lamp or light or bulb) adj1 holder) or lamp-holder)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 16:20
S23	1915	H05B$/$.CPC. AND (((LED.u/c. or light or	US-PGPUB;	OR	ON	2016/07/29

		lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			16:59
S24	1	S23 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME ((volt$3 or current) NEAR3 (sens$3 or detect$3 or monitor$3 or measur$3 or determin$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:00
S25	12	S23 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME (install$5 or insert$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:01
S26	22	S23 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) NEAR3 (circuit or element or device or unit or module or switch$2)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:12
S27	4834	(F21V$/$.CPC. or F21K9/$.CPC. or F21Y$/$.CPC.) AND (((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:14
S28	1	S27 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME ((volt$3 or current) NEAR3 (sens$3 or detect$3 or monitor$3 or measur$3 or determin$4)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:15
S29	18	S27 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME (install$5 or insert$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:15
S30	40	S27 AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) NEAR3 (circuit or element or device or unit or module or switch$2)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/07/29 17:17
S31	9	315/$.ccls. AND (((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2016/07/29 17:36

		eliminat$4 or safety or risk$2 or hazard$4) SAME ((install$5 or insert$4)) WITH (lampholder or socket or ((lamp or light or bulb) adj1 holder) or lamp-holder)))	IBM_TDB			
S36	1	("9497821").PN.	USPAT; USOCR	OR	OFF	2016/12/02 13:37
S37	48	("20020044456" | "20020176262" | "20030102819" | "20030231485" | "20040095078" | "20040189218" | "20050128751" | "20050162850" | "20050207166" | "20050213321" | "20070001709" | "20070145915" | "20070210687" | "20070274084" | "20080030981" | "20080192476" | "20080278941" | "20090161359" | "20100253226" | "20110038146" | "20110057572" | "20110090684" | "20110148313" | "20110216538" | "20110260614" | "20120069556" | "20120106157" | "20120153873" | "20120235578" | "20130050998" | "20130170245" | "20130182425" | "20130200797" | "20130320869" | "20140055029" | "20140071667" | "20140153231" | "20140226320" | "20150009688" | "5575459" | "5921660" | "6127783" | "6609813" | "6796680" | "7033239" | "8360599" | "8579463" | "8749167").PN. OR ("9497821").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/02 13:47
S38	27302	((tub$4 or straight or retrofit$4 or replacement) NEAR5 (lamp or bulb) NEAR5 (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 15:42
S39	10	S38 and ((detect$3 or sens$3 or monitor$3) WITH ((connect$3 or contact$4 or install$5) NEAR3 (good or bad or proper$4 or correct$4 or incorrect$4)) WITH ((lamp or bulb) adj1 (socket or holder)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 15:46
S40	13	S38 and ((detect$3 or sens$3 or monitor$3) SAME ((connect$3 or contact$4 or install$5) NEAR5 (good or bad or proper$4 or correct$4 or incorrect$4)) SAME ((lamp or bulb) adj1 (socket or holder)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 15:52
S41	202	S38 and ((detect$3 or sens$3 or monitor$3) SAME (connect$3 or contact$4 or install$5) SAME ((lamp or bulb) adj1 (socket or holder)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 15:55
S42	69	S41 and puls$3	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2016/12/02 15:56

			EPO; JPO; DERWENT; IBM_TDB			
S43	4	("20140028211" | "7898237" | "8525501" | "9112426").PN. OR ("9288867").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/02 16:13
S44	179	S41 and ((connect$4 or contact$4 or install$5 or remov$4 or replac$4) WITH ((lamp or bulb) adj1 (socket or holder)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 16:25
S45	2	("8459831" | "8749167").PN. OR ("9163818").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/02 17:23
S46	20	("20090219713" | "5118301" | "6061243" | "7147041" | "7470055" | "7665862" | "7674016" | "7722221" | "7744252" | "7974099" | "7976196" | "8147091" | "8262249").PN. OR ("8459831").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/02 17:24
S47	6	("20040202011" | "20050190553" | "20110050124" | "4375607" | "5309062" | "6667623").PN. OR ("8860314").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/02 17:58
S48	3557	S38 and (315/$.ccls. or 362/$.ccls.)	US-PGPUB; USPAT; USOCR	OR	ON	2016/12/02 18:02
S49	56	S48 and ((detect$3 or sens$3 or monitor$3) SAME (connect$3 or contact$4 or install$5) NEAR3 ((lamp or bulb) adj1 (socket or holder or plug)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 18:03
S50	5836	S38 AND (F21V$/$.CPC. or F21K9/$.CPC. or F21Y$/$.CPC. or H05B$/$.CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 18:07
S51	105	S50 and ((detect$3 or sens$3 or monitor$3) SAME (connect$3 or contact$4 or install$5) NEAR5 ((lamp or bulb) adj1 (socket or holder or plug)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 18:08
S52	16	S38 AND (((electric$4 or hazard$3 or protect$4 or safe$3 or prevent$3 or elimiat$3 or limit$3) NEAR2 shock$2) SAME ((lamp or bulb) NEAR1 (socket or plug or holder)) SAME ((sens$3 or detect$3 or monitor$3 or measur$3 or determin$4) NEAR2 (volt$3 or current)) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 18:18
S53	4	("20140225519" | "8664880" | "8760064" | "9232578").PN. OR ("9277603").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/02 18:20
S54	11	("20070133202" | "20070183156" |	US-PGPUB;	OR	OFF	2016/12/02

		"20070223225" | "20090290334" | "20100002439" | "20110260614" | "20110260622" | "20120299494" | "7611260" | "8147091").PN. OR ("8622571").URPN.	USPAT; USOCR			18:21
S55	16	S38 AND ((electric$4 or hazard$3 or protect$4 or safe$3 or prevent$3 or elimiat$3 or limit$3) NEAR2 shock$2) AND (((lamp or bulb) NEAR1 (socket or plug or holder)) SAME ((sens$3 or detect$3 or monitor$3 or measur$3 or determin$4) NEAR2 (volt$3 or current)) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 18:26
S56	24	S38 AND ((electric$4 or hazard$3 or protect$4 or safe$3 or prevent$3 or elimiat$3 or limit$3) NEAR2 shock$2) AND (((lamp or bulb) NEAR1 (socket or plug or holder)) SAME ((sens$3 or detect$3 or monitor$3 or measur$3 or determin$4) NEAR2 (volt$3 or current)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/12/02 18:37
S59	11	(("20110260614") or ("8749167") or ("20150223303") or ("20150181661") or ("20130335959") or ("9480123") or ("9163818") or ("8858248") or ("8847475") or ("20110228526") or ("20140225519") or ("20110260614")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/03 10:59
S60	11	("20070253137" | "20110187271" | "20120062114" | "20130147350" | "3365625" | "8147091" | "8322878" | "8339761" | "8459831" | "8749167").PN. OR ("9480123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2016/12/03 13:06
S61	1	("9587817").PN.	USPAT; USOCR	OR	OFF	2017/03/28 11:56
S62	81	("20020044456" | "20020176262" | "20030102819" | "20030231485" | "20040095078" | "20040189218" | "20050128751" | "20050162850" | "20050207166" | "20050213321" | "20060028837" | "20070001709" | "20070145915" | "20070210687" | "20070274084" | "20080030981" | "20080192476" | "20080278941" | "20090161359" | "20100102729" | "20100253226" | "20110038146" | "20110057572" | "20110090684" | "20110121756" | "20110148313" | "20110181190" | "20110216538" | "20110228526" | "20120069556" | "20120106157" | "20120153873" | "20120169968" | "20120181952" | "20120235578" | "20120293991" | "20120299501" | "20120313540" | "20120319150" | "20130033888" | "20130050998" | "20130170245" | "20130182425" | "20130200797" | "20130256704" | "20140071667" | "20140153231" | "20140226320" | "20140265900" | "20150009688" | "20150077001" | "20150173138" | "20150181661" | "20150351171" | "20160081147" | "20160091147" |	US-PGPUB; USPAT; USOCR	OR	OFF	2017/03/28 12:02

		"20160091156" | "20160091179" | "20160102813" | "20160178135" | "20160178137" | "20160178138" | "3294518" | "4647399" | "5575459" | "5921660" | "6118072" | "6127783" | "6211262" | "6609813" | "6796680" | "6936855" | "7033239" | "7067032" | "8360599" | "8525427" | "8579463" | "8648542" | "9210744" | "9480123").PN. OR ("9587817").URPN.				
S63	1	("9497821").PN.	USPAT; USOCR	OR	OFF	2017/03/28 12:50
S65	6	liu-xintong.in. and xiong-aiming.in. and jiang-tao.in.	US-PGPUB; USPAT	OR	ON	2017/03/28 13:05
S66	12	((LED.u/c. OR (light adj emitting adj diode) OR (light-emitting adj diode)) AND installation AND (pulse ADJ1 generat$4)).clm.	USPAT	OR	ON	2017/03/28 13:14
S67	18	((LED.u/c. OR (light adj emitting adj diode) OR (light-emitting adj diode)) AND installation AND (pulse ADJ1 generat$4)).clm.	US-PGPUB; USPAT	OR	ON	2017/03/28 13:46

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S32	1	315/$.ccls. AND (((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME ((volt$3 or current) NEAR3 (sens$3 or detect$3 or monitor$3 or measur$3 or determin$4)))	US-PGPUB; USPAT	OR	ON	2016/07/29 17:34
S33	9	315/$.ccls. AND (((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4) SAME ((install$5 or insert$4)) WITH (lampholder or socket or ((lamp or light or bulb) adj1 holder) or lamp-holder)))	US-PGPUB; USPAT	OR	ON	2016/07/29 17:37
S34	1	(((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4) NEAR3 (circuit or element or device or unit or module or switch$2)) SAME ((volt$3 or current) NEAR3 (sens$3 or detect$3 or monitor$3 or measur$3 or determin$4)))	US-PGPUB; USPAT	OR	ON	2016/07/29 18:06
S35	48	(((LED.u/c. or light or lamp or bulb) NEAR2 (tube or tubular)) SAME (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((electric$4 adj1 shock$2) NEAR3 (protect$4 or limit$4 or prevent$4 or eliminat$4 or safety or risk$2 or hazard$4)	US-PGPUB; USPAT	OR	ON	2016/07/29 18:07

		SAME ((install$5 or insert$4)) WITH (lampholder or socket or ((lamp or light or bulb) adj1 holder) or lamp-holder)))				
S57	46	(315/$.ccls. or 362/$.ccls.) AND ((tub$4 or straight or retrofit$4 or replacement) NEAR5 (lamp or bulb) NEAR5 (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((detect$3 or sens$3 or monitor$3) SAME (connect$3 or contact$4 or install$5 or remov$4 or replac$4) WITH (switch$2 or transistor)) SAME ((lamp or bulb) adj1 (socket or holder or plug)))	US-PGPUB; USPAT	OR	ON	2016/12/02 18:48
S58	8	((tub$4 or straight or retrofit$4 or replacement) NEAR5 (lamp or bulb) NEAR5 (LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode))) AND (((detect$3 or sens$3 or monitor$3) WITH pulse WITH (switch$2 or transistor)) SAME (connect$3 or contact$4 or install$5 or remov$4 or replac$4) SAME ((lamp or bulb) adj1 (socket or holder or plug)))	US-PGPUB; USPAT	OR	ON	2016/12/02 18:54

3/28/2017 9:22:43 PM
C:\Users\atran1\Documents\EAST\Workspaces\15066645-15210989.wsp

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B$/$, F21V$/$, F21K9/$, F21Y$/$ text search- see printout	12/02/16 & 7/29/16	AT

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
315 & 362	all- text search- see printout	12/02/16 & 7/29/16	AT

SEARCH NOTES		
Search Notes	Date	Examiner
east search- see printout	12/02/16 & 7/29/16	AT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	Anh Q. TRAN
Sheet	1	of	3	*Attorney Docket Number*	SUP-101C-3 (S16100US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20020176262	11-28-2002	Ajay Tripathi	
		US20030102819	06-05-2003	Young-Kee Min	
		US20110148313	06-23-2011	Antonius Everardus Theodorus Ramaker	
		US20100102729	04-29-2010	Katzir	
		US20160081147	03-17-2016	Guang	
		US20150077001	03-19-2015	Takahashi	
		US20140265900	09-18-2014	Sadwick et al.	
		US20120313540	12-13-2012	Lin	
		US20120181952	07-19-2012	Rooer	
		US7380961	12-16-2004	Hideo Moriyama	
		US20160219672	07-28-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160270163	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160356472	12-08-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20170094736A1	03-30-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20170089525A1	03-30-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20110260614	10-27-2011	Hartikka et al.	
		US8749167	06-10-2014	Hsia et al.	
		US20140055029	02-27-2014	William Peter Mechtildis Marie Jans	
		US8796943	02-06-2014	MIYAMICHI SABURO	
		US9521718	12-13-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20170105263	04-13-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20130127327	05-23-2013	Fraunhofer-Gesellschaft Zur Forderung	

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	Anh Q. TRAN
Sheet	2	of	3	*Attorney Docket Number*	SUP-101C-3 (S16100US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
		US20130147350	06-13-2013	Gio Optoelectronics Corp.	
		US20130335959	12-19-2013	Lightel Technologies Inc.	
		US20110228526	09-22-2011	Teknoware Oy	
		US20160219658	07-28-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	
		US20160270165	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		CN102155642	08-17-2011	CHANGGUI LIU		
		CN200965185	10-24-2007	YAOHAN LIU		
		CN102932997	02-13-2013	ZHEJIANG HENGMAN PHOTOELECTRIC TECHNOLOGY CO LTD		
		CN101715265	05-26-2010	OCEANS KING LIGHTING SCIENCE		
		CN102355780	02-15-2012	ZHEJIANG SHIMING OPTICS TECHNOLOGY CO LTD		
		CN106015996A	10-16-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO LTD		
		WO2017012514A1	01-26-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD		
		WO2013150417A1	10-10-2013	Koninklijke Philips N.V.		
		WO2015028329A1	03-05-2015	Koninklijke Philips N.V.		
		WO2015028639A1	03-05-2015	Koninklijke Philips N.V.		

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	Anh Q. TRAN
Sheet	3	of	3	*Attorney Docket Number*	SUP-101C-3 (S16100US)

NONPATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]

Examiner Signature		Date Considered	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Electronic Patent Application Fee Transmittal

Application Number:	15339221
Filing Date:	31-Oct-2016
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Filer:	Bradley E. Edelman
Attorney Docket Number:	SUP-101C-3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	29055714
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	27-APR-2017
Filing Date:	31-OCT-2016
Time Stamp:	20:02:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$180
RAM confirmation Number	042817INTEFSW20033400
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	SUP-101C-3_IDS_transmittal-1.pdf	59491 20239b79bcd59f8ee895610a2d3cddedcf1729ab	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	SUP-101C-3_S16100US_IDS_sb08.pdf	90017 91a7e88eb23a00cb2b13d71286f696fd0059c0d2	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	WO2017012514A1.pdf	6341108 0041dd72b60aa52928424bcfbcaae9c53ec979be	no	112
Warnings:					
Information:					
4	Foreign Reference	WO2013150417A1.pdf	1039373 80795097b2f04436056faba00938b56840b06bab	no	22
Warnings:					
Information:					
5	Foreign Reference	WO2015028329A1.pdf	1357353 f8722cc9075d9fa733243c2a3e70bb53580da6d5	no	31
Warnings:					
Information:					
6	Foreign Reference	WO2015028639A1.pdf	1203190 046b028989a1ca4cb90c2721f3890b02e4425870	no	29
Warnings:					

Information:					
7	Foreign Reference	WO2017012514.pdf	451670 7826b846a89922f1228d49da7c058f5294416f5a	no	1
Warnings:					
Information:					
8	Foreign Reference	WO2015028629.pdf	147265 5adb27e237eb06d7aacd0cb866e8f6f9672694ba	no	1
Warnings:					
Information:					
9	Foreign Reference	WO2015028329_.pdf	260917 fca5b9970bb6355d6f91ffcf59ce74321dc7c08a	no	1
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Information:					
10	Foreign Reference	CN106015996A.pdf	5747110 6601293aec1f1827f8a6ed377046784a0a2957f0	no	83
Warnings:					
Information:					
11	Foreign Reference	CN106015996.pdf	476085 dea4496b5f9a5f4ee2d11d9a8d37b1f0aa729a9f	no	1
Warnings:					
Information:					
12	Foreign Reference	CN102355780A.pdf	509541 383d4906995a4eb4ce80563fb562380a4cf69e9c	no	8
Warnings:					
Information:					
13	Foreign Reference	CN101715265A.pdf	649537 654c6e12bdb2a12f98673e9bc2f5aad71d8f1564	no	11
Warnings:					
Information:					

14	Foreign Reference	CN102932997A.pdf	1132594 9ba266e3eb502554722f3d20d4924ec4f63be58a	no	17
Warnings:					
Information:					
15	Foreign Reference	CN200965185Y.pdf	278728 0c7c30665a1bd4ef09c99449937e24642adcf93f	no	7
Warnings:					
Information:					
16	Foreign Reference	CN200965185Abst.pdf	133018 4af36911c2a400fecb3fe3bf74050fad11859c0	no	2
Warnings:					
Information:					
17	Foreign Reference	CN102932997Abst.pdf	111205 9017980ff320a0e7e8965d9946d18941f97fb671	no	2
Warnings:					
Information:					
18	Foreign Reference	CN102355780AAbst.pdf	110057 bc7c7ac64b80feda2a11997e8b75f79340d6ac13	no	2
Warnings:					
Information:					
19	Foreign Reference	CN102155642Abst.pdf	131467 1821aaf7a993abe99628aae762dbe623d53bc877	no	2
Warnings:					
Information:					
20	Foreign Reference	CN101715265Abst.pdf	122696 e444fc3e5276197b11c5ee8b1f752058b684a327	no	2
Warnings:					
Information:					

21	Fee Worksheet (SB06)	fee-info.pdf	30189 321268f7415c272146ccbf6396fc385594ef5ea0	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	20382611

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Liu et al.	Attorney Docket:	SUP-101C-3
Serial Number:	15/339,221	Group Art Unit:	2844
Filed:	October 31, 2016	Examiner:	Anh Q. TRAN
Confirmation Number:	3876		

Title: LED TUBE LAMP

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/Madam:

Pursuant to 37 C.F.R. 1.56 and 1.97(c), Applicant brings to the attention of the Examiner the listed documents on the attached SB/08 Form. This Information Disclosure Statement is being after a first office action on the merits of this application, and along with a $180 fee. Copies of any non-patent or foreign patent documents that were already submitted in a parent application may not be re-submitted herewith.

Applicant respectfully requests that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art". If the Examiner applies any of the documents as prior art

against any claim in the application and Applicant determines that the cited documents do not constitute "prior art" under United States law, Applicant reserves the right to present to the U.S. Patent and Trademark Office the relevant facts and law regarding the appropriate status of such documents.

Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

In the event any fees are required in connection with this paper, please charge the Deposit Account No. 50-4574.

Respectfully submitted,

/Bradley Edelman/

Bradley Edelman
Registration No. 57,648
Fax: (703) 757-7447
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Liu et al.

Serial Number: 15/339,221

Filed: October 31, 2016

Confirmation Number: 3876

Title: **LED TUBE LAMP**

Attorney Docket: SUP-101C-3

Group Art Unit: 2844

Examiner: Anh Q. TRAN

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This is a response to the Office Action of April 4, 2017. Amendments to the claims begin on page 2 of this paper. Remarks follow the amendment sections of this paper.

It is respectfully requested that the amendment be entered, the outstanding rejection of the above-identified patent application be reconsidered.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

What is claimed is:

1. (Original) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

2. (Original) The installation detection circuit according to claim 1, wherein the pulse generating circuit comprises:

a first capacitor, one end connected to a driving signal;

a first resistor, one end connected to the other end of the first capacitor, the other end

the first resistor connected to a reference voltage;

a first buffer, having an input end and an output end, the input end connected to the other end of the first capacitor;

a second capacitor, one end connected to the output end of the first buffer;

a third capacitor, one end connected to the output end of the first buffer;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

3. (Original) The installation detection circuit according to claim 1, wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit.

4. (Original) The installation detection circuit according to claim 3, wherein when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

5. (Original) The installation detection circuit according to claim 3, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

6. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.

7. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a second capacitor, one end coupled to a driving signal;

a third capacitor, one end coupled to the driving signal;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

8. (Original) The installation detection circuit according to claim 7, wherein the second buffer comprises two inverters connected in series.

9. (Original) The installation detection circuit according to claim 7, wherein the detection result latching circuit comprises:

a first D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit;

a fourth resistor, one end connected to the output end of the first D flip-flop, the other end of the fourth resistor connected to a reference voltage; and

a second OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first OR gate, the second input end connected to the output end of the first D flip-flop, the output end of the second OR gate connected to the switch circuit.

10. (Original) The installation detection circuit according to claim 7, wherein the switch circuit comprises:

a first transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the

emitter connected to the detection determining circuit.

11. (Currently Amended) The installation detection circuit according to claim 7, wherein the detection determining circuit comprises:

a fifth resistor, one end connected to the switch circuit, the other end of the fifth resistor connected to a second end of the power loop; and

a first comparator, having a first input end, a second input end, and an output end, the first input end connected to ~~the~~ a predefined signal, the second input end connected to the one end of the fifth resistor, the output end of the first comparator connected to the detection result latching circuit.

12. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a sixth resistor, one end connected to a driving signal;

a fourth capacitor, one end connected to the other end of the sixth resistor, the other end of the fourth capacitor connected to a reference voltage;

a Schmitt trigger, having an input end and an output end, the input end connected to the one end of the fourth capacitor, the output end connected to the detection result latching circuit;

a seventh resistor, one end connected to the one end of the fourth capacitor;

a second transistor, having a base, a collector, and an emitter, the collector connected to the other end of the seventh resistor, the emitter connected to a reference voltage; and

an eighth resistor, one end connected to the base of the second transistor, the other end of the eighth resistor connected to the detection result latching circuit and the switch circuit.

13. (Original) The installation detection circuit according to claim 12, wherein the

pulse generating circuit further comprises:

a Zener diode, having an anode and a cathode, the anode connected to the other end of the fourth capacitor, the cathode connected to the one end of the fourth capacitor.

14. (Original) The installation detection circuit according to claim 12, wherein the detection result latching circuit comprises:

a second D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit; and

a third OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the Schmitt trigger, the second input end connected to the output end of the second D flip-flop, the output end of the third OR gate connected to the other end of the eighth resistor and the switch circuit.

15. (Original) The installation detection circuit according to claim 12, wherein the switch circuit comprises:

a third transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

16. (Currently Amended) The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop; and

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to ~~the~~ a predefined signal, the second input end connected to the one end of the ninth resistor, the output end of the second comparator connected to the detection result latching circuit.

17. (Currently Amended) The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop;

a second diode, having an anode and a cathode, the anode connected to the one end of the ninth resistor;

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to ~~the~~ a predefined signal, the second input end connected to the cathode of the second diode, the output end of the second comparator connected to the detection result latching circuit;

a third comparator, having a first input end, a second input end, and an output end, the first input end connected to the cathode of the second diode, the second input end connected to another predefined signal, the output end of the third comparator connected to the detection result latching circuit;

a tenth resistor, one end connected to the driving signal;

an eleventh resistor, one end connected to the other end of the tenth resistor and the second input end of the second comparator, the other end of the eleventh resistor connected to a reference voltage; and

a fifth capacitor, connected to the eleventh resistor in parallel.

18. (Original) The installation detection circuit according to claim 1, wherein the LED tube lamp comprises a lamp tube and a circuit board, and comprises an inductive element connected between two terminals respectively at two ends of the lamp tube for grounding or connecting to a reference potential, wherein one of the two terminals is connected to the circuit board.

19. (Original) The installation detection circuit according to claim 18, wherein the

inductive element is an inductor.

20. (Original) The installation detection circuit according to claim 19, wherein one end of the inductor is directly electrically connected to the circuit board.

21. (Original) The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

22. (Original) An installation detection circuit configured in a light-emitting diode (LED) tube lamp, the installation detection circuit comprising:

means for generating one or more pulse signals;

means for detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket; and

a switch circuit coupled to the means for generating one or more pulse signals, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

23. (Original) The installation detection circuit according to claim 22, wherein the means for detecting is configured to detect a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket, and the

power loop includes the switch circuit and the means for detecting.

24. (Original) The installation detection circuit according to claim 23, wherein when the means for detecting determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the means for detecting determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

25. (Original) The installation detection circuit according to claim 23, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the means for detecting.

26. (Original) The installation detection circuit according to claim 23, wherein the LED tube lamp is configured to receive an external driving signal and comprises a rectifying circuit for rectifying the external driving signal and a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit.

27. (Original) A detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket, the detection method comprising:

when at least one end of the LED tube lamp is installed on the lamp socket, generating one or more pulse signals by a pulse generating circuit, wherein the pulse generating circuit is configured in the LED tube lamp;

detecting a sampling signal on a power loop of the LED tube lamp by a detection

determining circuit, to detect during the one or more pulse signals whether the other end of the LED tube lamp is properly installed on the lamp socket;

receiving the one or more pulse signals through a detection result latching circuit by a switch circuit, wherein the switch circuit is on the power loop; and

comparing the sampling signal with a predefined signal, wherein during the one or more pulse signals when the sampling signal is smaller than the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open.

28. (Original) The detection method according to claim 27, wherein the step of controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open comprises:

outputting a first low level signal by the detection determining circuit;

receiving the first low level signal by the detection result latching circuit and

outputting a second low level signal; and

receiving the second low level signal by the switch circuit and maintaining an off state of the switch circuit to cause the power loop to be open.

29. (Original) The detection method according to claim 27, wherein during any of the one or more pulse signals when the sampling signal is greater than or equal to the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

30. (Original) The detection method according to claim 29, wherein the step of controlling the switch circuit to remain in a conducting state to cause the power loop of the

LED tube lamp to maintain a conducting state comprises:

outputting a first high level signal by the detection determining circuit;

receiving the first high level signal by the detection result latching circuit and outputting a second high level signal; and

receiving the second high level signal by the switch circuit and conducting the switch circuit to cause the power loop to maintain a conducting state.

31. (Original) The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 10 microseconds and 1 millisecond.

32. (Original) The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 1 microsecond and 100 microseconds.

REMARKS

Status of the Claims

Claims 1-32 are now present in this application. Claims 1, 22, and 27 are independent.[1]

Claims 11, 16, and 17 have been amended via this amendment. It is respectfully submitted that no new matter has been added to the application via this amendment. Reconsideration and allowance of this application, as amended, is respectfully requested.

Claim Amendments

Applicant have amended the claims in order to correct minor typographical errors, and to place the claims in better form. The claim amendments are not being made in response to any statutory requirement for patentability, and have not been narrowed in scope. Instead, the claims have been amended merely to recite the subject matter therein more clearly.

Obviousness-Type Double Patenting Rejection

Claims 1-7, 9-11, and 21-32 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-29 of U.S. Patent No. 9,497,821. This rejection is respectfully traversed.

A complete discussion of the Examiner's rejection is set forth in the Office Action, and is not being repeated here.

While not conceding the appropriateness of the Examiner's rejection, but merely to advance prosecution of the instant application, Applicant are herewith submitting a Terminal Disclaimer disclaiming the terminal portion of any patent granted on the present application which would extend beyond the expiration of U.S. Patent No. 9,497,821.

Accordingly, reconsideration and withdrawal of this rejection are respectfully

[1] Unless expressly stated herein, Applicant declines to necessarily subscribe to any of the Examiner's characterizations of Applicant's specification, the claims, or the prior art made in the Office Action.

requested.

Allowable Subject Matter

The Examiner states that claims 8 and 12-20 would be allowable if rewritten in independent form.

Applicant thanks the Examiner for the early indication of allowable subject matter in this application. However, claims 8 and 12-20 have not been rewritten in independent form at this time, since it is believed that independent claim 1 from which these claims depend is allowable.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Ali Imam, Registration No. 58755, at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

In the event any additional fees are required in connection with this paper, or in the event of an overpayment, please charge or credit the Deposit Account No. 50-4574.

Respectfully submitted,

/Ali M. Imam/

_____

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Electronic Acknowledgement Receipt

EFS ID:	29125004
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Ali M. Imam
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	05-MAY-2017
Filing Date:	31-OCT-2016
Time Stamp:	11:08:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUP-101C-3_Response_to_OA.pdf	136838 6d2f0478b8a3c2e5680f4177e35c059784d0d36a	yes	15

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	15
Warnings:			
Information:			
	Total Files Size (in bytes):	136838	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/26 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT**
Application Number	15339221
Filing Date	31-Oct-2016
First Named Inventor	Xintong Liu
Attorney Docket Number	SUP-101C-3
Title of Invention	LED TUBE LAMP

☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action

☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.

Owner	Percent Interest
JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	100%

The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)

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as the term of said prior patent is presently shortened by any terminal disclaimer. The owner hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the prior patent are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

In making the above disclaimer, the owner does not disclaim the terminal part of the term of any patent granted on the instant application that would extend to the expiration date of the full statutory term of the prior patent, "as the term of said prior patent is presently shortened by any terminal disclaimer," in the event that said prior patent later:
- expires for failure to pay a maintenance fee;
- is held unenforceable;
- is found invalid by a court of competent jurisdiction;
- is statutorily disclaimed in whole or terminally disclaimed under 37 CFR 1.321;
- has all claims canceled by a reexamination certificate;
- is reissued; or
- is in any manner terminated prior to the expiration of its full statutory term as presently shortened by any terminal disclaimer.

◉ Terminal disclaimer fee under 37 CFR 1.20(d) is included with Electronic Terminal Disclaimer request.

○	I certify, in accordance with 37 CFR 1.4(d)(4), that the terminal disclaimer fee under 37 CFR 1.20(d) required for this terminal disclaimer has already been paid in the above-identified application.

Applicant claims the following fee status:

○ Small Entity

○ Micro Entity

◉ Regular Undiscounted

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES

I certify, in accordance with 37 CFR 1.4(d)(4) that I am:

◉ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application

Registration Number 58755

○ A sole inventor

○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application

○ A joint inventor; all of whom are signing this request

Signature	/Ali M. Imam/
Name	Ali M. Imam

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal

Application Number:	15339221
Filing Date:	31-Oct-2016
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Filer:	Ali M. Imam
Attorney Docket Number:	SUP-101C-3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**160**

Doc Code: DISQ.E.FILE
Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 15339221

Filing Date: 31-Oct-2016

Applicant/Patent under Reexamination: Liu

Electronic Terminal Disclaimer filed on May 5, 2017

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

Approved/Disapproved by: Electronic Terminal Disclaimer automatically approved by EFS-Web

U.S. Patent and Trademark Office

Electronic Acknowledgement Receipt

EFS ID:	29125126
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Ali M. Imam
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	05-MAY-2017
Filing Date:	31-OCT-2016
Time Stamp:	11:17:10
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$160
RAM confirmation Number	050517INTEFSW11170700
Deposit Account	504574
Authorized User	Amy Dean

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Electronic Terminal Disclaimer-Filed	eTerminal-Disclaimer.pdf	33427 35338d124165eceebea884493dee5c1f3bc22b94	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30302 4abfe7b57843ebc9d0654c6d4a0ee0038b4e1d28	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	63729		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/339,221	Filing Date 10/31/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	05/05/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 32	Minus	** 32	= 0	X $80 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
NICOLE NICHOLSON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

74712 7590 08/07/2017

Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

EXAMINER
TRAN, ANH Q

ART UNIT	PAPER NUMBER
2844	

NOTIFICATION DATE	DELIVERY MODE
08/07/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
pto@muirpatentlaw.com

Office Action Summary	Application No. 15/339,221	Applicant(s) LIU ET AL.	
	Examiner ANH TRAN	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/05/17*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-32* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☒ Claim(s) *27-32* is/are allowed.

7)☒ Claim(s) *1,3,4 and 22-24* is/are rejected.

8)☒ Claim(s) *2,5-20,25 and 26* is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Claim Rejections - 35 USC § 102

2. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

4. Claim(s) 1, 3-4, 22-24 is/are rejected under 35 U.S.C. 102(a)(2) as being anticipated by Sadwick, Laurence, P. (WO 2015/066566 A1).

Claim 1, Sadwick shows an installation detection circuit configured in a light-emitting diode (LED) tube lamp (see Figs. 9-13) configured to receive an external driving signal (902-922, Fig. 9), the installation detection circuit (Fig. 21) comprising:

a pulse generating circuit (2124, 2126, 2130, 2132, 2128, and 3134, Fig. 21) configured to output one (output at 3134 and see P[0096]…Capacitor 2130 and resistor 2132 form an RC time constant that is used to temporarily turn on transistor 2128 resulting in optocoupler 2134 being shorted out for a relatively short period of time

during the initial turn-on phase…; therefore, the optocoupler is on and off which is a pulse signal) or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal (Fig. 21 is shock hazard control, see P[0096]-[0097]; and

a switch circuit (1430, Fig. 14 or 2022, Fig. 20) coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit (…optocoupler 2134 to short out the gate to source of transistor 2022 in Fig. 20…see P[0096] and [0097]…In addition to or in place of the sense circuit a switch can be used to, for example, short out the voltage across the Zener diode 2046 in Fig. 20 so as to turn off transistor 2022...);

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket (not fully installed), control the switch circuit (1430, Fig. 14 or 2022, Fig. 20) to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket (fully installed), control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state (1430, Fig. 14 or 2022, Fig. 20).

Claim 3, Sadwick shows the installation detection circuit according to claim 1, wherein the signal generated from the external driving signal is a sampling signal (sampling signal at node 2112, Fig. 21 connected to a node between resistor 1446 and capacitor 1444, Fig. 14) on the power loop (e.g., power loop in Fig. 14 included: 1430, 1446, 1444, 11451 and circuit of Fig. 21) the installation detection circuit further comprises a detection determining circuit (2110, Fig. 21) configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit (1430, Fig. 14) and the detection determining circuit (2110, Fig. 21).

Claim 4, Sadwick shows the installation detection circuit according to claim 3, wherein when the detection determining circuit determines that the sampling signal (2112, Fig. 21) is greater than or equal to a predefined signal (2104, Fig. 21), it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining circuit determines that the sampling signal (2112) is smaller than a predefined signal (2104), it is detected that the LED tube lamp is not properly installed on the lamp socket.

Claims 22-24 are rejected as above since the elements and limitations are similar.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have

> been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 21 is/are rejected under 35 U.S.C. 103 as being unpatentable over Sadwick, Laurence, P. (WO 2015/066566A1).

7. Sadwich discloses the claimed invention except for wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond. It would have been obvious to one having ordinary skill in the art at the time the effective filing date of the invention was made to modify a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Allowable Subject Matter

8. Claims 2, 5-20, 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 27-32 are allowed.

The following is an examiner's statement of reasons for allowance:

receiving the one or more pulse signals through a detection result latching circuit by a switch circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH TRAN whose telephone number is (571)272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Taningco can be reached on 571-272-2048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ANH TRAN/
Primary Examiner, Art Unit 2844
7/13/17

Notice of References Cited	Application/Control No. 15/339,221	Applicant(s)/Patent Under Reexamination LIU ET AL.	
	Examiner ANH TRAN	Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A	US-				
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	WO 2015066566 A1	05-2015	UNITED STATES	SADWICK LAURENCE P	F21V25/00
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/28/2017	07/13/2017							
	1	✓	✓							
	2	✓	O							
	3	✓	✓							
	4	✓	✓							
	5	✓	O							
	6	✓	O							
	7	✓	O							
	8	O	O							
	9	✓	O							
	10	✓	O							
	11	✓	O							
	12	O	O							
	13	O	O							
	14	O	O							
	15	O	O							
	16	O	O							
	17	O	O							
	18	O	O							
	19	O	O							
	20	O	O							
	21	✓	✓							
	22	✓	✓							
	23	✓	✓							
	24	✓	✓							
	25	✓	O							
	26	✓	O							
	27	✓	=							
	28	✓	=							
	29	✓	=							
	30	✓	=							
	31	✓	=							
	32	✓	=							

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	Anh Q. TRAN
Sheet	1	of	3	*Attorney Docket Number*	SUP-101C-3 (S16100US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20020176262	11-28-2002	Ajay Tripathi	
		US20030102819	06-05-2003	Young-Kee Min	
		US20110148313	06-23-2011	Antonius Everardus Theodorus Ramaker	
		US20100102729	04-29-2010	Katzir	
		US20160081147	03-17-2016	Guang	
		US20150077001	03-19-2015	Takahashi	
		US20140265900	09-18-2014	Sadwick et al.	
		US20120313540	12-13-2012	Lin	
		US20120181952	07-19-2012	Rooer	
		US7380961	12-16-2004	Hideo Moriyama	
		US20160219672	07-28-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160270163	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160356472	12-08-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
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		US20110260614	10-27-2011	Hartikka et al.	
		US8749167	06-10-2014	Hsia et al.	
		US20140055029	02-27-2014	William Peter Mechtildis Marie Jans	
		US8796943	02-06-2014	MIYAMICHI SABURO	
		US9521718	12-13-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20170105263	04-13-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20130127327	05-23-2013	Fraunhofer-Gesellschaft Zur Forderung	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	Anh Q. TRAN
Sheet	2	of	3	Attorney Docket Number	SUP-101C-3 (S16100US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
		US20130147350	06-13-2013	Gio Optoelectronics Corp.	
		US20130335959	12-19-2013	Lightel Technologies Inc.	
		US20110228526	09-22-2011	Teknoware Oy	
		US20160219658	07-28-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	
		US20160270165	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		CN102155642	08-17-2011	CHANGGUI LIU		
		CN200965185	10-24-2007	YAOHAN LIU		
		CN102932997	02-13-2013	ZHEJIANG HENGMAN PHOTOELECTRIC TECHNOLOGY CO LTD		
		CN101715265	05-26-2010	OCEANS KING LIGHTING SCIENCE		
		CN102355780	02-15-2012	ZHEJIANG SHIMING OPTICS TECHNOLOGY CO LTD		
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		WO2017012514A1	01-26-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD		
		WO2013150417A1	10-10-2013	Koninklijke Philips N.V.		
		WO2015028329A1	03-05-2015	Koninklijke Philips N.V.		
		WO2015028639A1	03-05-2015	Koninklijke Philips N.V.		

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
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				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	Anh Q. TRAN
Sheet	3	of	3	*Attorney Docket Number*	SUP-101C-3 (S16100US)

NONPATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]

Examiner Signature	/ANH Q TRAN/	Date Considered	07/13/2017

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B$/$, F21V$/$, F21K9/$, F21Y$/$ text search- see printout	12/02/16 & 7/29/16	AT
H05B$/$, F21V$/$, F21K9/$, F21Y$/$ text search- see printout	6/1/17	AT

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
315 & 362	all- text search- see printout	12/02/16 & 7/29/16	AT
315 & 362	all- text search- see printout	6/1/17	AT

SEARCH NOTES		
Search Notes	Date	Examiner
east search- see printout	12/02/16 & 7/29/16	AT
east search- see printout	6/1/17	AT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
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(43) International Publication Date
7 May 2015 (07.05.2015)

WIPO | PCT

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H05B 33/08 (2006.01)

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31 October 2014 (31.10.2014)

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61/898,357 31 October 2013 (31.10.2013) US
61/908,074 20 December 2013 (20.12.2013) US
62/001,048 20 May 2014 (20.05.2014) US

(71) Applicant: **INNOSYS, INC.** [US/US]; 2900 South Main Street, Salt Lake City, Utah 84115 (US).

(72) Inventor: **SADWICK, Laurence, P.**; 3767 E. Brockbank Drive, Salt Lake City, Utah 84124 (US).

(74) Agent: **CLINGER, Guy, K.**; 99 Viewcrest Circle, Bountiful, Utah 84010 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *of inventorship (Rule 4.17(iv))*

Published:

— *with international search report (Art. 21(3))*

WO 2015/066566 A1

(54) Title: FLUORESCENT LAMP REPLACEMENT LED PROTECTION

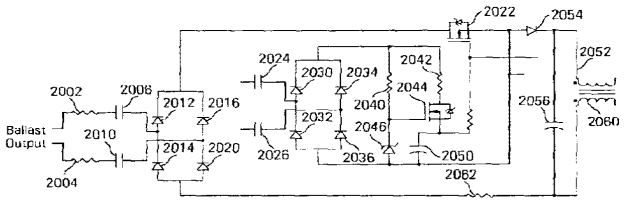


FIG. 20

(57) Abstract: A fluorescent lamp replacement may include one or more LED drivers and lamps in various embodiments, as well as a shock hazard/pin safety circuit. The present invention provides a fluorescent lamp replacement that, for example, powers an LED and/or OLED and/or QD lamp from a fluorescent fixture, including operating 5 and being powered by electronic ballasts. In some embodiments, a fluorescent lamp replacement includes a number of pins configured to electrically connect to a fluorescent lamp fixture, at least one non-fluorescent light source, a transistor between at least one of the pins and the at least one non-fluorescent light source, and a shock hazard protection circuit configured to disable the transistor to limit current flowing through at least some of the pins.

Fluorescent Lamp Replacement LED Protection

BACKGROUND

[0001] Fluorescent lamps are widely used in a variety of applications, such as for general purpose lighting in commercial and residential locations, in backlights for liquid crystal displays in computers and televisions, etc. Conventional fluorescent tubes used for general lighting cannot, in general, be directly plugged into alternating current (AC) voltage lines. Fluorescent lamps generally include a glass tube, circle, spiral or other shaped bulb containing a gas at low pressure, such as argon, xenon, neon, or krypton, along with low pressure mercury vapor. A fluorescent coating is deposited on the inside of the lamp. As an electrical current is passed through the lamp, mercury atoms are excited and photons are released, most having frequencies in the ultraviolet spectrum. These photons are absorbed by the fluorescent coating, causing it to emit light at visible frequencies.

[0002] Electronic ballasts convert the input AC voltage supplied (typically at a low AC frequency of 50 or 60 Hz) power into generally a sinusoidal AC output waveform typically designed for a constant current output in the frequency range of above 20 to 40 kHz to typically less than 100 kHz and sometimes greater than 100 kHz.

[0003] Fluorescent lamps can suffer from a number of disadvantages, such as a relatively short life span, flickering, and noisy ballasts, etc. However there are many high quality electronic ballasts that are available. Although the ballasts may be of high quality and long life, often the

florescent tubes that are powered by the ballasts, suffer from a number of undesirable effects including reduced lifetime due, for example, to being switched on and off too often. Therefore it would be desirable to have a replacement for fluorescent tubes that are not susceptible and immune from such effects or at least not so susceptible to these undesirable issues and effects. Furthermore, as replacements for fluorescent tubes are installed, the electrical contacts or pins at the ends of the tube replacements are exposed, which can carry dangerously high electrical currents.

SUMMARY

[0004] The present invention provides a fluorescent lamp replacement that, for example, powers an LED and/or OLED and/or QD lamp from a fluorescent fixture, including operating and being powered by electronic ballasts.

[0005] In some embodiments, a fluorescent lamp replacement includes a number of pins configured to electrically connect to a fluorescent lamp fixture, at least one non-fluorescent light source, a transistor between at least one of the pins and the at least one non-fluorescent light source, and a shock hazard protection circuit configured to disable the transistor to limit current flowing through at least some of the pins. In some embodiments, the shock hazard protection circuit is a mechanical switch, which in some cases is normally closed, and in others is normally open. In some embodiments, the shock hazard protection circuit comprises an under-current detection circuit configured to detect a lower than expected current to the plurality of pins. In some cases, the shock hazard protection circuit comprises an optocoupler connected across a control input of the transistor and another lead of the transistor, or across a gate and a source of the transistor or other control voltage of the transistor, which is much lower than the voltage across the plurality of pins. In some cases, the shock hazard protection circuit is configured to short out a power source for the transistor.

[0006] In some embodiments, the fluorescent lamp replacement includes a ballast short circuit connected across the plurality of pins, and a fault detection circuit configured to control the ballast short circuit. In some cases, the fault detection circuit comprises an over-voltage detection circuit,

over-current detection circuit, and/or over-temperature detection circuit. In some embodiments, the fault detection circuit is configured to short an AC current across the plurality of pins. Some embodiments include a diode connected between the transistor and the at least one non-fluorescent light source, and the fault detection circuit is configured to short a DC current between the transistor and the at least one non-fluorescent light source. Some embodiments include at least one capacitor connected in parallel with the at least one non-fluorescent light source downstream from the diode.

[0007] In some embodiments, the transistor comprises a common-gate, common-source, common-drain MOSFET pair.

[0008] Some embodiments include a constant-current regulation circuit. Some of these embodiments also include a processor having a remote control interface. The processor can be configured to transmit status information through the remote control interface, and/or to receive dimming commands through the remote control interface and to control the constant-current regulation circuit based at least in part on the dimming commands. In some of these instances, the shock hazard protection circuit is implemented at least in part by the processor.

[0009] This summary provides only a general outline of some particular embodiments. Many other objects, features, advantages and other embodiments will become more fully apparent from the following detailed description. Nothing in this document should be viewed as or considered to be limiting in any way or form.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] A further understanding of the various exemplary embodiments may be realized by reference to the figures which are described in remaining portions of the specification. In the figures, like reference numerals may be used throughout several drawings to refer to similar components. The words LED and LEDs are also used to describe and include OLED and OLEDs and QDs, or any other non-fluorescent light source.

[0011] Fig. 1 depicts a florescent lamp replacement (FLR).

[0012] Fig. 2 depicts a block diagram of an example embodiment of a fluorescent lamp fixture with ballast and a fluorescent lamp replacement.

[0013] Fig. 3 depicts a block diagram of an example embodiment of a fluorescent lamp ballast with two fluorescent lamp replacements.

[0014] Fig. 4 depicts a fluorescent lamp replacement with one of the connections to fluorescent lamp replacement connections connected to ground.

[0015] Fig. 5 depicts a fluorescent ballast with a connection to a florescent lamp replacement with one of the connections to fluorescent lamp replacement connections connected to ground.

[0016] Fig. 6 depicts a fluorescent ballast with a connection to a florescent lamp replacement with one or more of the connections to fluorescent lamp replacement connections connected to ground.

[0017] Fig. 7 depicts a fluorescent ballast with a connection to a florescent lamp replacement with one of the connections to fluorescent lamp replacement connections connected to ground.

[0018] Fig. 8 depicts a fluorescent ballast with a connection to a florescent lamp replacement with one of the connections

to fluorescent lamp replacement connections connected via a human to ground.

[0019] Fig. 9 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement where the protection, or at least part of the protection, is after the rectification stage.

[0020] Fig. 10 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement with protection in which the protection or at least part of the protection is in front of the rectification stage.

[0021] Fig. 11 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement where the protection includes additional circuitry typically more than a switch and where the protection, or at least part of the protection, is after the rectification stage.

[0022] Fig. 12 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement where the protection includes additional circuitry typically more than a switch and where the protection, or at least part of the protection, is before the rectification stage.

[0023] Fig. 13 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement where various parts of the protection includes additional circuitry typically more than a switch and where the protection, or at least part of the protection, is both before and after the rectification stage.

[0024] Fig. 14 depicts a circuit diagram of an example embodiment of a fluorescent lamp LED replacement with hazard/leakage protection.

[0025] Fig. 15 depicts a circuit diagram of an example embodiment of a fluorescent lamp LED replacement having protection and detection that allows a periodic, short turn-on (hiccup mode).

[0026] Fig. 16 depicts a circuit diagram of an example embodiment of a fluorescent lamp LED replacement having protection and detection including over-voltage protection with a shunt regulator and associated feedback and control.

[0027] Fig. 17 depicts a circuit diagram of an example embodiment of a fluorescent lamp LED replacement with over-voltage protection.

[0028] Fig. 18 depicts an example embodiment that can be used to reduce, limit or effectively short out the output voltage of a ballast.

[0029] Fig. 19 depicts another example of an implementation of the present invention that can be used to reduce, limit or effectively short out the output voltage of the ballast in which a bidirectional switch can be used.

[0030] Fig. 20 depicts an example embodiment of the present invention for a fluorescent lamp LED replacement.

[0031] Fig. 21 depicts an example embodiment of one type of detection circuit for a fluorescent lamp LED replacement.

[0032] Fig. 22 depicts an example embodiment of a shock hazard control circuit for a fluorescent lamp LED replacement.

[0033] Fig. 23 depicts an example embodiment of an over voltage and over temperature protection for a fluorescent lamp LED replacement.

[0034] Fig. 24 depicts an example embodiment of a fluorescent lamp LED replacement with capacitors for EMI/EMC filter components.

[0035] Fig. 25 depicts a version of the present invention that implements and allows for current transformation and also allows for emulation of the heater/cathodes.

[0036] Fig. 26 depicts another implementation of the present invention in which a center tapped secondary is used such that only two diodes or synchronous transistors are needed to realize and attain full wave rectification.

[0037] Fig. 27 depicts a version of the present invention that allows for current limit and protection.

[0038] Fig. 28 depicts a version of the present invention that allows for current limit and protection.

[0039] Fig. 29 depicts another version of a detection circuit for a fluorescent lamp LED replacement that provides current limit and protections.

[0040] Fig. 30 depicts an example embodiment of one type of detection circuit for a fluorescent lamp LED replacement.

[0041] Figs. 31A-C depict versions of the present invention illustrating physically split apart high frequency rectification components that also can provide current limit and protections.

[0042] Fig. 32 depicts a block diagram of a microcontroller with a variety of inputs and outputs configured to control shock hazard or pin safety protection in a fluorescent lamp replacement in accordance with some embodiments of the invention.

[0043] Fig. 33 depicts a block diagram of a microcontroller with a variety of inputs and outputs configured to control shock hazard or pin safety protection in a fluorescent lamp replacement, with bidirectional remote control in accordance with some embodiments of the invention.

[0044] Fig. 34 depicts a block diagram of a fluorescent lamp replacement circuit that can be used with shock hazard/pin safety protection.

[0045] Fig. 35 depicts a block diagram of a fluorescent lamp replacement circuit that can be used with shock hazard/pin safety protection, including dimming control.

[0046] Fig. 36 depicts a block diagram of a fluorescent lamp replacement circuit that can be used with shock hazard/pin safety protection, including bidirectional dimming control and status feedback.

[0047] Fig. 37 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement with hazard/leakage protection and with inductor-driven load output.

[0048] Fig. 38 depicts a block diagram of an example embodiment of a fluorescent lamp LED replacement with hazard/leakage protection and with transformer-driven load output.

[0049] Fig. 39 depicts an example embodiment of a shock hazard control circuit for a fluorescent lamp LED replacement.

[0050] Fig. 40 depicts an example embodiment of a ballast over-voltage protection and over-temperature protection circuit for a fluorescent lamp LED replacement.

[0051] Fig. 41 depicts an example ballast shorting circuit that can be controlled by an over-voltage, over-current, and/or over-temperature or other fault detection circuit in a fluorescent lamp LED replacement.

[0052] Fig. 42 depicts an example embodiment of a fluorescent lamp LED replacement with dual MOSFET switch for shock hazard protection.

[0053] Figs. 43A-43E depict various views of an end cap for a fluorescent lamp LED replacement with spring-mounted pins for shock hazard protection.

[0054] Figs. 44A-44D depict various views of an end cap for a fluorescent lamp LED replacement with slide-switch activated pins with shock hazard protection.

[0055] Figs. 45A-45C depict various views of a rotating end cap for a fluorescent lamp LED replacement with rotation-activated pins with shock hazard protection.

DESCRIPTION

[0056] Brief definitions of terms used throughout this document are given below. The phrases "in one embodiment," "according

to one embodiment," and the like generally mean the particular feature, structure, or characteristic following the phrase is included in at least one embodiment of the present invention, and may be included in more than one embodiment of the present invention. Importantly, such phrases do not necessarily refer to the same embodiment.

[0057] If the specification states a component or feature "may", "can", "could", or "might" be included or have a characteristic, that particular component or feature is not required to be included or have the characteristic. When referring to light emitting diodes (LEDs) it is to be understood that LED can refer to any type of LED, any color or colors of LED (including white and any type or color temperature of white, for example cool white, warm white, daylight white, etc. and 6000k, 2700k, etc., respectively) including any type of organic LED (OLED) and, similarly, to quantum dot (QD)-based lighting.

[0058] A fluorescent replacement is disclosed herein that may be used to power one or more LED or OLED or QD or combination of these lamps from an electric ballast typically in a fluorescent fixture. An LED driver typically only requires two inputs from the electronic ballast source, which are then rectified typically using a bridge rectifier. Other types of rectification can also be used with the present invention.

[0059] The present invention can also use heater emulation circuits that allow, for example, rapid start, programmable start, programmed start, pre-start, dimmable ballasts, etc. warm, and other similar types of ballasts to work with the present invention by providing sufficient stimuli in response to the heater/cathode leads and associated circuits in the these ballasts which could be either low frequency magnetic or high frequency electronic and still be compatible with instant-start, cold-start, low frequency (i.e., 50/60 Hz and

400 Hz) AC universal voltage and higher voltage range ballasts.

[0060] A circuit that dynamically adjusts such that the output current to a load such as an LED and/or OLED and/or a QD array is essentially kept constant by, for example, in some embodiments of the present invention shorting or shunting current from the ballast as needed to maintain the output current to a load such as a LED and/or OLED and/or a QD array essentially constant. In other embodiments and implementations a switching circuit that contains, for example, one or more each of inductors, diodes, switching elements such as a transistor switch which could, for example, form a buck, buck-boost, boost, boost-buck, fly back, forward converter, push-pull, SEPIC, Cuk, etc. Some embodiments of the present invention may use time constants as part of the circuit. Embodiments of the present invention include buck (or buck-boost, boost-buck, boost) inductors, diodes, switches, etc. along with associated EMI filters and protection circuits that can be used with AC lines and magnetic and electronic ballasts including instant (cold) start, rapid (hot or warm) start, programmed start, dimmable, pre-start, etc. ballasts. In some embodiments the FLR or FLRs that are powered by AC lines, magnetic or electronic ballasts can be remotely (e.g., wirelessly and/or wired) dimmed, controlled, monitored, etc.

[0061] In some embodiments, a circuit powers a protection device/switch such that the switch is on unless commanded or controlled to be set off in the event/situation/condition of a fault hazard. Such a control can be implemented in various and diverse forms and types including, but not limited to, latching, hiccup mode, etc. In some embodiments of the present invention such a circuit may have a separate rectification stage. In other embodiments of the present

invention the protection device/switch may be off unless commanded or controlled to be set on. In and for various embodiments of the present invention, the device/switch may be of any type or form or function and includes but is not limited to, semiconductor switches, vacuum tube switches, mechanical switches, relays, etc. This and other protection mechanisms disclosed herein can be applied to fluorescent lamp replacements such as, but not limited to, those disclosed in US Patent 8,502,454 to Sadwick, which is incorporated herein by reference for all purposes.

[0062] In some embodiments, an over voltage protection (OVP) circuit shunts/shorts or limits the ballast output and/or the output to the load such as an LED and/or OLED and/or QD array in the event that the output voltage exceeds a set value.

[0063] In some embodiments, an over-temperature protection (OTP) circuit shunts/shorts or limits the ballast output and/or the output to the load such as an LED and/or OLED and/or QD array in the event that the temperature at one or more locations exceeds a set value or set values.

[0064] Embodiments of the present invention may also include short circuit protection (SCP) and other forms of protection including protection against damage due to other sources of power including but not limited to AC mains power lines and/or other types of devices, circuits, etc. Some embodiments of the present invention may use, for example, but are not limited to capacitors to limit the low frequency (examples include, but are not limited to, AC line mains at 50 Hz, 60 Hz, 400 Hz) voltage and/or current that can be applied to the load. In addition to capacitors, inductors and resistors may also be used in some embodiments of the present invention.

[0065] Embodiments of the present invention include, but are not limited to, having a rectification stage (such as, but not limited to) consisting of a single full wave rectification

stage to provide power/current to the output load such as an LED and/or OLED output load and a rectification stage (such as, but not limited to) consisting of a single full wave rectification stage to provide power to, for example, the hazard protection circuit.

[0066] Fig. 1 shows an illustration of a florescent lamp replacement 100 (FLR) which may typically have up to four connections 102, 104, 106, 107 with two connections typically being the minimum needed. The FLR 100 in general consists of a rectification stage and some form of light source such as a light source made up of LEDs including organic light emitting diodes (OLEDs).

[0067] Turning now to Fig. 2, an example configuration of an electronic ballast 200 connected to two fluorescent lamp replacements 202, 204, in this case replacements for rapid start or program start fluorescent lamps, which include a heater. The ballast 200 is powered by an AC input 206, 208, and grounded by ground connection 210. Although two fluorescent lamp replacements 202, 204 are shown in Fig. 2, any number can be connected to a single ballast 200; in general up to N FLRs (i.e., 1 to N) can be connected to a single ballast 200 that is designed to support and power up to N florescent lamps. An example embodiment of a simple configuration places the ballast 200 in series with a bridge rectifier, which drives DC terminals (plus and minus, respectively) to the LED or OLED light source with or without optional capacitor(s).

[0068] Turning now to Fig. 3, an example embodiment of the present invention is shown with N = 2 fluorescent lamp replacements 302, 304 attached to a single ballast 306. In this case, the fluorescent lamp replacements 302, 304 are adapted to replace instant start fluorescent lamps. More than one rectification unit such as a rectification full-bridge or

a rectification synchronous full bridge or half-bridge may be used with the present invention. In addition, a transformer may also be used with the present invention to, for example, transform current and voltage from the output of the ballast to the rectification stage(s) connected either directly or indirectly to the LED or OLED lighting/lamps/arrays/etc.

[0069] Other embodiments of the present invention may use a second bridge rectifier or synchronous rectifier stage, or, for example, a total of 8 (or more or, in some cases, with shared diodes, greater than 4 and less than 8) discrete diodes to rectify the input. In general, the diodes should have a high frequency response in order to efficiently. The present invention provides a drop-in replacement(s) for fluorescent lamp(s). It also leaves the fixture unmodified, allowing the fixture to be used again at a later time for fluorescent lamps or to have people unskilled in electrical matters replace the fluorescent lamps with the FLRs. In particular, implementations and embodiments of the present invention allows for greater flexibility and potentially reduced EMI/EMC reducing potential EMI/EMC issues while also increasing the flexibility of the FLRs. Additional benefits of the present invention may be realized such as modularity and flexibility of design, construction, manufacturing, dimming, protection, safety, ease of use, non-skilled installation and replacement, etc. In addition, the present invention can, in general, be made to be an add-on feature to many existing AC to DC power supplies and, with proper adaptions and modifications, DC to DC power supplies. In addition, the present invention may be used and modified as needed with DC primary input power, constant current input power and can be optimized to operate over a wide range of input conditions, voltages and currents.

[0070] Turning now to Fig. 4, an example is shown where the FLR 406 may present a safety hazard or risk to people during

installation such that one end/pins 402, 404 of the FLR 406 may come in contact with an abnormal ground while the other end/pins 410, 412 are connected to one lead/wire of the ballast thus permitting a current to flow between the output of the ballast and ground sufficient in many cases for there to be enough current to light, for example, the LEDs or OLEDs or QDs and also cause injury including fatal injury to a person or persons who may come in contact between the end/pin(s) 410, 412 of the FLR 406 that are not connected to the ballast wire(s)/lead(s)/output and ground - essentially in series with the right-side end 410, 412 of the FLR 406 and ground.

[0071] Figs. 5 through 7 show other examples, illustrations and representations of potential hazard conditions and situations. In Fig. 5, a fluorescent lamp replacement 500 is connected to a ballast 502 at one end. The ballast 502 is powered by an AC input 504, 506, and grounded by ground connection 508. An electrical connection 510, typically housed safely within a fluorescent tube fixture, is intended to electrically connect to pin 512 on the fluorescent lamp replacement 502. As with other embodiments, the ballast 502 can be an instant start ballast as in Fig. 5, or a rapid start or program start ballast with additional heater connectors, or any other type of ballast. When the fluorescent lamp replacement 502 is fully connected within the fluorescent tube fixture, pin 512 is safely connected to electrical connection 510, protecting the user from electrical shock. However, when the fluorescent lamp replacement 502 is being installed, pin 512 can be exposed and, without protection mechanisms, can shock and injure a user contacting the pin 512 and appearing as an abnormal ground 514 through which an electrical current can flow. As shown in Fig. 6, the fixture 600 can have any number of configurations. While the exposed pin 602 of the

fluorescent lamp replacement 604 is accessible, it is protected as disclosed herein to substantially or completely prevent current from flowing when connected to an abnormal ground, such as when a grounded user contacts the pin 602. As generalized in Fig. 7, the fluorescent lamp replacement 700 is not limited to use with any particular type of power source, ballast or fixture. As long as power is supplied to one pin 702 of the fluorescent lamp replacement 700, other pin(s) 704 should be protected as disclosed herein from inadvertent contact with an abnormal ground. This is illustrated explicitly in Fig. 8, in which one pin 802 of a fluorescent lamp replacement 804 is connected to a ballast or other power source, and another pin 806 is contacted by a person 810 who is grounded 812 or effectively may be in contact with ground 812. In the absence of a protection mechanism in the fluorescent lamp replacement 804, current would flow from the output of the ballast 802 through the fluorescent lamp replacement 804 and through the person 810 or living creature to ground. Such a current could be of sufficient level to cause harm, injury or even death to the human(s) or living creature/entity in between the end of the ballast and ground.

[0072] Turning to Fig. 9, a fluorescent lamp replacement 906 is depicted in accordance with some embodiments of the invention. The fluorescent lamp replacement 906 includes a rectification circuit 910, such as, but not limited to, a full or partial diode bridge to rectify an AC current at input pins 902, 904, one of which, in this example, is a rapid start heater connection. In other embodiments of the fluorescent lamp replacement 906 of Fig. 9, as well as variations of the fluorescent lamp replacements 1006, 1106, 1206, and 1320 of Figs. 10-13, the fluorescent lamp replacements can be designed, for example but not limited to, to be connected to

and/or powered by an instant start ballast, a rapid start, or other ballast or power source.

[0073] The fluorescent lamp replacement 906 includes a protection switch 912 following the rectification circuit 910, providing shock hazard protection against inadvertent contact with exposed pin(s) 920, 922. Such a protection switch 912 can be a switch such as a transistor of any type and form or any other type of switch such as a relay or other semiconductor device or devices with a suitable breakdown/hold-off/standoff/blocking/etc. voltage such that little or no (or an acceptable amount of current) can flow from the output of the ballast. Other circuitry 914 can be included to perform other desired functions such as over-voltage protection, over-current protection, constant current regulation and/or dimming circuitry, etc. Loads such as light emitting diodes 916 of one or more colors are powered by the current through rectification circuit 910.

[0074] Fig. 10 shows an example embodiment of a fluorescent lamp replacement 1006 including a protection circuit 1010 in which the protection or at least part of the protection is electrically in front of the rectification stage 1012. Such protection 1010 could consist of switch that allows current to flow in both directions (i.e., positive and negative directions from the output of the ballast to, for example, short out the output of the ballast or redirect the current from the output of the ballast. Other circuitry 1014 can be included in addition to light emitting diodes 1016.

[0075] Fig. 11 shows an example embodiment where the protection circuit 1112 in a fluorescent lamp replacement 1106 includes additional circuitry typically more than a switch and where the protection, or at least part of the protection, is after the rectification stage 1110. Such a protection circuit 1112 could consist of a switch such as a transistor of any type and

form or any other type of switch with a suitable breakdown/hold-off/standoff/ blocking/etc voltage and detection, monitoring and/or control circuitry for the switch such that little or no (or an acceptable amount of current) can flow from the output of the ballast. Other circuitry 1114 can be included in addition to light emitting diodes 1116.

[0076] Fig. 12 shows an example embodiment in which the protection circuit 1210 in a fluorescent lamp replacement 1206 includes additional circuitry typically more than a switch and where the protection circuit 1210, or at least part of the protection, is before the rectification stage 1212. Other circuitry 1214 can be included in addition to light emitting diodes 1216.

[0077] Fig. 13 shows an example embodiment where various parts of the protection circuit 1306, 1312 in a fluorescent lamp replacement 1320 includes additional circuitry typically more than a switch and where the protection circuit 1306, 1312, or at least part of the protection, is both before and after the rectification stage 1310. Other circuitry 1314 can be included in addition to light emitting diodes 1316.

[0078] The fluorescent lamp replacement protection of, for example, Figs. 9 through 13 may be used with any suitable LED or OLED driver and/or LED or OLED lamp or other types of loads, and is not limited to any examples set forth herein. For example, the fluorescent lamp replacement of Figs. 1 through 13 may be used with any of the embodiments described in U.S. Patent Application No. 12/422,258 entitled "Dimmable Power Supply", filed April 11, 2009, U.S. Patent Application No. 12,776/435 entitled "Universal Dimmer", filed May 10, 2010, US Patent Application 61/646,289 filed May 12, 2012 for a "Current Limiting LED Driver", and in US Patent 8,148,907 issued April 3, 2012 for a "Dimmable Power Supply", the entirety of each of which is incorporated herein by reference

for all purposes. The invention disclosed herein can also be used in connection with circuits and applications disclosed in the following, which are incorporated herein by reference for all purposes: U.S. Patent Application No. 61/776,671 entitled "Fluorescent Lamp LED Replacement" filed March 11, 2013, U.S. Patent Application No. 61/786,047 entitled "Digital Dimmable Driver" filed March 14, 2013, U.S. Patent Application No. 61/786,406 entitled "Powerline Control Interface" filed March 15, 2013, U.S. Patent Application No. 61/786,415 entitled "Ripple Reducing LED Driver" filed March 15, 2013, U.S. Patent Application No. 61/800,677 entitled "Linear LED Driver" filed March 15, 2013, and U.S. Patent Application No. 61/800,837 entitled "Fluorescent Lamp LED Replacement" filed March 15, 2013.

[0079] Other components may also be placed in series or parallel with the bridge rectifiers including an input fuse, in certain cases, a varistor, a spark gap, other transistors, etc. Alternatively, the diode bridge(s) could also be implemented with an appropriate number of individual diodes having the appropriate characteristics including high frequency diode performance.

[0080] Turning now to Fig. 14, an embodiment of a fluorescent lamp LED replacement 1400 is depicted in which the hazard/leakage protection has a power supply source that consists of capacitors 1402, 1404 which perform AC coupling and current limiting, and of diodes 1406, 1410, 1412, 1414 which form a rectified floating power supply that is further regulated using the regulator consisting of resistors 1416, 1424, capacitor 1424, Zener diode 1420 and transistor 1422. A time constant can be included in the rectified floating power supply, for example, using resistor 1424 and capacitor 1424. Resistors 1436, 1440 form a voltage divider that acts as a reference set point which is filtered by optional capacitor

1442 that is fed to the inverting terminal of a comparator 1434 (or similar function such as an op amp) with the voltage from a sense resistor 1450 being fed to the non-inverting input of the comparator 1434 via an optional filter/time constant consisting of resistor 1446 and capacitor 1444 such that when the signal from the sense resistor 1450 is larger than the reference set point signal, the comparator 1434 goes high and turns on transistor 1430 which allows (not shown in Fig. 14) the output of the ballast (which is the input to the FLR) to flow through a rectification stage that may contain optional capacitors at the input (similar to the input stage consisting of capacitors 1402, 1404, diodes 1406, 1410, 1412, 1414) to the rest of the FLR including to the LED and/or OLED and/or QD load. Feedback resistors and pullup/pulldown resistors (e.g., 1432, 1426) can be included as needed or desired. Transistor/switch 1430 is in series with (and in between) the input rectification stage of the FLR connected to node 1429 and the LED (or OLED or QD) load of the FLR connected to node 1451. When the voltage across sense resistor 1450 is above the reference set point voltage, transistor 1430 is turned on and current/voltage is allowed to flow to the LED or OLED or QD load. If the current through the sense resistor 1430 produces too small of a voltage then transistor 1430 is turned off preventing current from flowing and thus limiting and preventing a hazard/shock/leakage current condition from occurring.

[0081] Additional circuitry not shown allows transistor 1430 to be initially turned on even when the current is well below the set point. Such additional circuitry can be accomplished in many ways including a simple RC time constant properly inserted and located such that it initially allows transistor 1430 to be turned on for a relatively short, momentary amount of time so as to allow current to flow and achieve normal

operating conditions if the FLR is connected to the ballast correctly.

[0082] If the FLR is not connected to the ballast correctly (examples of such shown in Figs. 5 through 8) then a lower current will in general be obtained resulting in the hazard protection circuitry turning off transistor 1430 and essentially eliminating or substantially reducing the hazard/leakage current and threat of harm and injury to people and other living creatures. Various embodiments and implementations of the protection circuitry allow for diverse possible responses to the detection of the fault hazard condition including, but certainly not limited to, a complete turn-off (i.e., latch off) until power is cycled (i.e., turned off and then turned back on) or, as another example, periodically turned back on for a brief moment to see if the hazard fault condition had cleared (i.e., the FLR had been correctly plugged into the ballast).

[0083] Such a periodic, short turn-on (hiccup mode) can be accomplished by a number of means and methods including, but not limited to, the example circuit 1500 shown in Fig. 15 where the integrated timer circuit 1506 and resistors 1512, 1514, and capacitor 1516 form a timing sequence that periodically sends a pulse through resistor 1502 to periodically pull transistor 1522 low to allow the transistor 1430 in Fig. 14 to be turned on. (Note, in this embodiment, the comparator 1434 and associated components in the right side of Fig. 14 are replaced with the timer circuit 1506 and associated resistors and capacitor of the left side of Fig. 15. In addition, a second circuit consisting of resistor 1524, optocoupler 1526 and resistor 1530 can be used that allow an isolated control and turn-off of transistor 1522 in Fig. 15. By applying a sufficient signal to the input of the optocoupler 1526 at node 1523, transistor 1522 is turned off,

thus allowing transistor 1434 in Fig. 14 to turn on and permit current to flow to the LED or OLED load should a fault condition not exist permitting an autostart/hiccup mode of operation to take place should a fault condition occur. The circuit 1500 of Fig. 15 can be applied to that of Fig. 14 by connecting the drain 1523 of transistor 1522 to the gate of transistor 1430 of Fig. 14.

[0084] Figure 16 shows an example over-voltage protection (OVP) embodiment of the present invention. As shown in Fig. 16, the over-voltage protection circuit has an optional power supply source that consists of AC coupling and current limiting capacitors 1602, 1614 (which can have resistors connected in parallel to provide a DC path), and diodes 1604, 1606, 1610, 1612 which form a rectified floating power supply that is further regulated using the regulator consisting of resistors 1616, 1624, capacitor 1628, Zener diode 1620 and transistor 1622. Optional resistors (not shown) can be connected in parallel with AC coupling capacitors 1602, 1614 if desired to provide a DC path, in embodiments in which the ballast connected to AC coupling capacitors 1602, 1614 checks for a DC path before enabling normal operation.

[0085] Resistors 1630, 1626 form a voltage divider that acts as a reference set point which can also be filtered by, for example, a capacitor (not shown). The resulting reference set point is fed to the non-inverting terminal of a comparator 1634 (or similar function such as an op amp) with the voltage from a sense resistor (represented by a voltage V1 1632 in Fig. 16) being fed to the inverting input of the comparator 1634 via an optional filter/time constant (not shown). When the signal from the sense resistor, represented by voltage V1 1632, is larger than the reference set point signal, the comparator 1634 goes low and turns off transistor 1650 which, in turn, turns on transistor 1656 and turns off transistor

1662, which acts as the over-voltage protection (OVP) transistor, shunting the current through optional resistors 1666, 1670 (which in many embodiments can be shorted) of the rectified ballast output. In the event that the current sensed is too small, then the comparator output goes high which turns on transistor 1650 and turns off transistor 1656 (assuming that transistor 1652 is also turned on) which allows the OVP transistor 1662 to be turned on and therefore the current to be shunted through transistor 1662.

[0086] An optional one-shot circuit 1636, or timer circuit, monostable multivibrator, pulse generator, etc. and associated transistor 1652 act so as to provide an example mechanism to periodically turn on the auto-restart/hiccup mode such that in the event OVP is triggered, the optional one-shot circuit 1636 which drives transistor 1652 can be set to periodically turn off allowing transistor 1656 to be turned on and thus turning off transistor 1662. Resistor 1672 represents the rest of the FLR including the LED (or OLED) load. Removing the optional example one-shot circuit 1636 and transistor 1652 can in some cases result in a potentially latched OVP circuit.

[0087] Other embodiments of the present invention reverse the input to the comparator 1634 with the reference connected to the inverting input of the comparator and a voltage divider attached to the output of the diode bridge shown in Fig. 16 (which could be replaced by a synchronous transistor bridge) with the center of the voltage divider connected to the non-inverting input of the comparator 1634 such that when an over-voltage condition exists, the comparator 1634 goes high and turns on transistor 1650 which turns off transistor 1656 allowing the over-voltage transistor 1662 to be turned on resulting in the current being shunted through transistor 1662. In this case the optional one-shot circuit 1636 and associated transistor 1652 are connected in an OR

configuration with/in some embodiments of the present invention having a timer circuit with some additional components including diode(s), resistor(s), capacitor(s), transistors, etc. In general, embodiments of the present invention can use AND, OR, NAND, NOR, and/or other types of Boolean Algebra operations and operations to accomplish various types of functions including but not limited to the optional hiccup mode, OVP, OTP, shock hazard, etc.

[0088] Turning now to Fig. 17, an example embodiment of the OVP is shown in which a NAND two input gate 1755 is explicitly shown. In this particular embodiment, the over-voltage protection has an optional power supply source that consists of AC coupling and current limiting capacitors 1702, 1714 (which can have resistors connected in parallel to provide a DC path), and diodes 1704, 1706, 1710, 1712 which form a rectified floating power supply that is further regulated using the regulator consisting of resistors 1716, 1724, capacitor 1728, Zener diode 1720 and transistor 1722. Optional resistors (not shown) can be connected in parallel with AC coupling capacitors 1702, 1714 if desired to provide a DC path, in embodiments in which the ballast connected to AC coupling capacitors 1702, 1714 checks for a DC path before enabling normal operation.

[0089] Resistors 1730, 1726 form a voltage divider that acts as a reference set point which can also be filtered by, for example, a capacitor (not shown). The resulting reference set point is fed to the non-inverting terminal of a comparator 1734 (or similar function such as an op amp) with the voltage from a sense resistor (represented by a voltage V1 1732 in Fig. 17) being fed to the inverting input of the comparator 1734 via an optional filter/time constant (not shown). When the signal from the sense resistor, represented by voltage V1 1732, is larger than the reference set point signal, the

comparator 1734 goes low and turns off transistor 1756 which, in turn, turns on transistor 1762, which acts as the over-voltage protection (OVP) transistor, and thus not shunting the current through optional resistors 1766, 1770 (which in many embodiments can be shorted) of the rectified ballast output. In the event that the current sensed is too small, then the comparator output goes high which turns off transistor 1756 which allows the OVP transistor 1762 to be turned on and therefore the current to be shunted through transistor 1762 and optional resistors 1766, 1770.

[0090] The optional one-shot circuit 1736 acts to provide an example method of a periodically turning on the auto-restart/hiccup mode such that in the event OVP is triggered, the one-shot circuit 1736 which is connected to the other input of the NAND gate 1755 can be set to periodically set the output of the NAND 1755 high for a relatively short duration (but long enough to turn on the FLR if the condition resulting in the over-voltage has cleared) allowing transistor 1756 to be turned on and thus turning off transistor 1762. Resistor 1772 represents the rest of the FLR including the LED (or OLED) load. Other embodiments of the present invention reverse the input to the comparator 1734 with the reference connected to the inverting input of the comparator and a voltage divider attached to the output of the diode bridge shown in Fig. 17 (which could be replaced by a synchronous transistor bridge) with the center of the voltage divider connected to the non-inverting input of the comparator 1734 such that when an over-voltage condition exists, the comparator 1734 goes high and turns off transistor 1756 allowing the over-voltage transistor 1762 to be turned on resulting in the current being shunted through transistor 1762 and any components attached/connected to transistor 1762 such as optional resistors 1766, 1770. Again, in general,

embodiments of the present invention can use AND, OR, NAND, NOR, and/or other types of Boolean Algebra operations and operations to accomplish various types of functions including but not limited to the optional hiccup mode all or some of which can be incorporated and built into an ASIC or IC, etc.

[0091] Fig. 18 shows an example of an implementation of the present invention that can be used to reduce, limit or effectively short out the output voltage of the ballast. Capacitor 1802 and optional capacitor 1814, connected across the ballast output, are used to short out the ballast voltage using transistor 1820 which can effectively block the high frequency DC voltage due to the AC to DC rectification of diodes 1804, 1806, 1810, 1812. When a voltage (or current for current-controlled devices such as bipolar transistors) high enough to turn on transistor 1820 is applied between the gate and source of transistor 1820, as represented by voltage V3 in Fig. 18, where V3 can be supplied by a control and/or one or more hazard/fault detection circuits, the output voltage of the ballast can be shorted.

[0092] Fig. 19 shows another example of an implementation of the present invention that can be used to reduce, limit or effectively short out the output voltage of the ballast in which a bidirectional switch can be used. In this embodiment, the shorting is performed on the AC side of a rectifier. As shown and illustrated in the example embodiment of Fig. 19, capacitor 1902 and optional capacitor 1910 can via a bidirectional (+/−) composite transistor made up of transistors 1914, 1906 with the gates and sources of tied together can be used to short out the output voltage of the ballast when an appropriate voltage/signal is applied to the gates of transistors transistors 1914, 1906. Note that although only one transistor (MOSFET) is shown in Fig. 18 and two transistors (MOSFETs) are shown in Fig. 19, any

combination of transistors in series and/or parallel that achieve an appropriate or needed voltage may be used including, but not limited to, cascoded/stacked transistors including FETs of any appropriate type such as N-type and/or P-type MOSFETs, JFETs, MESFETs, GaN FETs, SiC FETs, BJTs, Darlington BJTs, HBTs, etc.

[0093] Now turning to Fig. 20, an example embodiment of the present invention is depicted and illustrated. Resistors 2002, 2004 connected to the ballast output can either be optional fuses, act as an optional fuse (i.e., a fuse resistor) or be shorted out and omitted; capacitors 2006, 2010 and diodes 2012, 2014, 2016, 2020 form an illustrative example embodiment of a current limiter/protection and rectification stage. Transistor 2022 acts as a protection in terms of hazard and leakage current and is designed and intended to prevent leakage current from passing through the present invention through a human or animal, etc. to ground when transistor 2022 is off. In other embodiments and implementations of the present invention, a signal that for example, is either mechanical (including but not limited to motion and rotation based) or electrical or both can be used to turn off the switching element or switching elements in, for example, a buck (or buck-boost, boost-buck, boost, SEPIC, fly back, forward converter, push-pull, etc.) converter and therefore turn off the switching converter action until the present invention is properly inserted into the respective light fixture as a FLR. Transistor 2022 is powered by the ballast output via a floating power supply consisting of capacitors 2024, 2026 and diodes 2030, 2032, 2034, 2036 that is further optionally regulated by resistors 2040, 2042, transistor 2044, Zener diode 2046 and capacitor 2050.

[0094] A mechanical switch can be used to short out the gate to source voltage of transistor 2022 when pins on the fluorescent

lamp replacement are exposed, turning off transistor 2022 and preventing current from flowing through the pins to load output 2052 through diode 2054. In such an embodiment, when the fluorescent lamp replacement was fully installed and the pins are no longer exposed, the mechanical switch would open, allowing transistor 2022 to conduct. In other embodiment, an optocoupler (e.g., 2134, Fig. 21) is connected across the gate and source of transistor 2022 to short out the gate to source voltage when, for example, a fault condition is detected.

[0095] Diode 2054 allows the voltage at the anode of diode 2054, which is the rectified input voltage, to be pulled down and the ballast current shunted through a shunt transistor such as transistor 2262, Fig. 22 or transistor 2322, Fig. 23 without also pulling the voltage down across capacitor 2056 and the output of the optional choke and/or inductor 2060 and/or transformer which is connected to the LED or OLED load. Resistor 2062 in Fig. 20 is used as a current sense resistor and is fed to other parts of the present invention.

[0096] Turning now to Fig. 21, an example embodiment of one type of detection circuit for shock hazard control is depicted. Op amp (or comparator) 2110 drives transistor 2124 via resistor 2122 if the non-inverting input which is, for the example shown, a voltage divider consisting of resistors 2104, 2106 and optional capacitor 2108 which provides a voltage reference to compare against the inverting input signal coming from feedback signal 2112 representing the voltage across resistor 2062 which, for example, senses and measures the current of Fig. 20 via optional filter consisting of resistor 2114 and capacitor 2116. In the event that the signal from resistor 2062 in Fig. 20 is low, then Op amp (or comparator) 2110, Fig. 21 puts out a low signal that turns off transistor 2124 which allows the input current to optocoupler 2134 to flow via resistor 2126 thus allowing optocoupler 2134 to short

out the gate to source of transistor 2022 in Fig. 20. Capacitor 2130 and resistor 2132 form an RC time constant that is used to temporarily turn on transistor 2128 resulting in optocoupler 2134 being shorted out for a relatively short period of time during the initial turn-on phase - i.e., the turn-on/supplying of power/current to the FLR.

[0097] In addition to or in place of the sense circuit a switch can be used to, for example, short out the voltage across the Zener diode 2046 in Fig. 20 so as to turn off transistor 2022; such a switch could be normally closed (NC) and, in many cases, be a low voltage switch that, for example, is momentarily closed, a two position single pole slide or rotary switch, a switch that is normally closed and then opened by rotation or depression of springs, etc. In general most types of switches are suitable for use with the present invention as the voltage is low - typically less than 30 volts and often around 15 to 16 V and the current is also typically very low. In some embodiments of the present invention the switch may be also used to turn off the buck (or buck-boost, boost-buck, boost, fly back, forward converter, push-pull, etc.) switching device or devices (i.e., transistors) by, for example, and not limited in any way or form, shorting the gate to source of, for example a MOSFET or MOSFETs. The switch may be used with single direction (i.e., DC) switching elements or bidirectional (i.e., AC) switching elements in any appropriate manner. In addition, other configurations may use normally open switches for the shock hazard/pin safety protection in which, for example, the switch is set from protect mode to operation mode such that transistor 2022 and/or the switching elements are able to be switched on and off at typically relatively high frequencies again in the range of typically 20 kHz to over 100 kHz. In some embodiments of the present invention a microcontroller or microcontrollers (and/or FPGAs,

microprocessors, DSPs, CLDs, etc.) can, for example, use an input to detect the state of a switch (e.g., normally open (NO) or normally closed (NC)) and, for example, set transistor 2022 and/or other switching devices/transistors to the on/operational state or the off/gate-to-source shorted state depending on the state of the operate/protect state of the switch and, for example, the associated signal(s).

[0098] Turning to Fig. 22, an example embodiment of a ballast control circuit is illustrated and depicted. The control circuit has an optional power supply source that takes power from a rectified power supply at node 2220 that is optionally further regulated using the regulator consisting of resistors 2222, 2224, Zener diode 2226, capacitor 2230 and transistor 2232. Resistor 2234 and Zener diode 2236 along with optional capacitor 2240 form an example voltage reference (although other types of voltage references can be used to achieve a stable voltage reference including, but not limited to, bandgap references, precision voltage references, etc.). Resistors 2242, 2244 form a voltage divider that acts as a reference set point which could also be filtered by, for example, a capacitor (not shown) that is fed to the non-inverting terminal of a comparator 2246 (or similar function such as an op amp). The voltage from a sense resistor (e.g., resistor 2062 in Fig. 20) is fed to the inverting input of the comparator 2246 via an optional filter/time constant consisting of resistor 2250 and capacitor 2252 such that when the signal from the sense resistor (e.g., resistor 2062 in Fig. 20) is larger than the reference set point signal, the comparator 2246 goes low and provides a negative pulse.

[0099] The negative pulse from comparator 2246 triggers, for example, a one-shot circuit 2260, or timer circuit, monostable multivibrator, pulse generator, etc., which in turn, generates a pulse that turns on transistor 2262 for a predetermined time

duration. In some embodiments, one-shot circuit 2260 is replaced with an inverter such as, but not limited to, a series bipolar junction transistor and resistor, with the base of the BJT controlled by the output of the comparator 2246, and with the inverter output between the BJT and resistor driving the gate of transistor 2262. In some embodiments, one-shot circuit 2260 is replaced with an inverter such as, but not limited to, a series field effect transistor transistor and resistor, with the gate of the FET controlled by the output of the comparator 2246, and with the inverter output between the FET and resistor driving the gate of transistor 2262. A time constant can be included to control the rise and/or fall time at the gate of the FET.

[0100] The drain of transistor 2262 is attached between the source of transistor 2022 and diode 2054 in Fig. 20 and acts as a shunting transistor, shunting the current of the rectified ballast output through resistor 2264 which in some embodiments may be replaced by a short. Again, this shorts out the ballast and prevents current from reaching the load or capacitor 2056, while diode 2054 prevents capacitor 2056 from being discharged and also turning off the load. Optional resistors may be used between the drain of transistor 2262 and the source of transistor 2022 and diode 2054 of Fig. 20. In the event that the current sensed is too high, then the output of the comparator 2246 (or op amp) goes low which results in turning on transistor 2262 and allows the current to be shunted through transistor 2262 and any optional resistors for a prescribed amount of time. Other embodiments of the present invention may use different implementations, circuits, etc. that perform the same/similar function/operation, etc. Again, in general, embodiments of the present invention can use any type or form of circuit, implementation, design, etc.

[0101] Turning now to Fig. 23, another example embodiment of an over-voltage protection (OVP) and over-temperature protection (OTP) is shown and illustrated. In this particular embodiment, the over-voltage protection has a voltage reference such as, but not limited to, resistor 2302 and Zener diode 2304 that acts as a reference set point which could also be filtered by, for example, a capacitor (not shown) that is fed to the non-inverting terminal of a comparator 2306 (or similar function such as an op amp). The reference set point is compared in comparator 2306 with, for example, a voltage, scaled in voltage divider 2310, 2312, at node 2308, which is the voltage used to drive the LED or OLED or QD load (e.g., node 2052, Fig. 20). The scaled voltage is fed to the inverting input of the comparator/op amp 2306. An optional filter/time constant (not shown) may be used but is not required such that filtering output voltage takes place. When the scaled voltage is larger than the reference set point signal, the comparator 2306 goes low with a negative pulse, discharging capacitor 2314 and turning off transistor 2316, allowing the gate of transistor 2322 to be pulled up through resistor 2324 and turning on OVP transistor 2322. When the comparator 2306 goes high, capacitor 2314 is charged through resistor 2320, turning on transistor 2316 and shorting the gate of transistor 2322, turning off OVP transistor 2322.

[0102] OVP transistor 2322 shunts the current of the rectified ballast output that drives/supplies the LED or OLED or QD load, shutting off the current through the exposed pin(s) of the fluorescent lamp replacement. The drain of transistor 2322 may be connected between the source of transistor 2022 and diode 2054 of Fig. 20. Other embodiments of the present invention can perform current shunting such that when an over-voltage condition exists, the output voltage is limited to an appropriate value allowing the over-voltage transistor to be

turned on resulting in the current being shunted through the OVP and/or away from the output of the FLR driver or to block the current from flowing using, for example, but not limited to, transistor 2022 of Fig. 20. In addition, other protection circuits, functions and features can be added/incorporated into the present invention. For example, Fig. 23 also contains an over-temperature protection function - such a function is performed by, for example, but not limited to, a thermistor 2326 in parallel with Zener diode 2304 with both in series with resistor 2302. For example, thermistor 2326 can be but is not limited to a negative temperature coefficient (NTC) thermistor such that the resistance of thermistor 2326 decreases as the temperature increases thus eventually dropping the voltage across thermistor 2326 in parallel with Zener diode 2304, below the Zener voltage of diode 2304 which can be used to turn on the OTP circuit via the series resistance voltage divider of resistor 2302 and thermistor 2326 at a lower voltage and even turn-off the output current of the FLR to the LED and/or OLED and/or QD load. Again, in general, embodiments of the present invention can use AND, OR, NAND, NOR, and/or other types of Boolean Algebra operations and operations to accomplish various types of functions including but not limited to the optional hiccup mode.

[0103] Fig. 24 shows and depicts another example embodiment similar to that of Fig. 20. In this embodiment, resistors 2406, 2408 are shown in parallel with current limiting capacitors 2402, 2404, providing a DC current path to cause particular ballasts to operate correctly. Optional capacitors 2410, 2412, 2414, 2416 are connected in parallel across corresponding high-frequency rectification diodes diodes 2420, 2422, 2424, 2426 (which could be replaced or augmented by synchronous transistors to form the rectification process). One or more (or less) capacitors can be added to each of the

diodes 2420-2426 (or synchronous transistors) to achieve benefits in performance including reduced electromagnetic interference/electromagnetic compatibility (EMI/EMC) including, but not limited to, radiated EMI. Although only capacitors 2410-2416 are shown, other components including resistors, snubbers, clamps, etc. of any type or form may also be used.

[0104] Transistor 2430 acts as a protection in terms of hazard and leakage current and is designed and intended to prevent leakage current from passing through the present invention through a human or animal, etc. to ground when transistor 2022 is off. Transistor 2430 is powered by the ballast output via a floating power supply consisting of capacitors 2432, 2434 and diodes 2436, 2440, 2442, 2444 that is further optionally regulated by resistor 2446, capacitor 2450 and Zener diode 2452.

[0105] A mechanical switch can be used to short out the gate to source voltage of transistor 2430 when pins on the fluorescent lamp replacement are exposed, turning off transistor 2430 and preventing current from flowing through the pins to load output 2460 through diode 2454. In such an embodiment, when the fluorescent lamp replacement was fully installed and the pins are no longer exposed, the mechanical switch would open, allowing transistor 2430 to conduct. In other embodiment, an optocoupler (e.g., 2134, Fig. 21) is connected across the gate and source of transistor 2430 to short out the gate to source voltage when, for example, a fault condition is detected.

[0106] Diode 2454 allows the voltage at the anode of diode 2454, which is the rectified input voltage, to be pulled down and the ballast current shunted through a shunt transistor such as transistor 2262, Fig. 22 or transistor 2322, Fig. 23 without also pulling the voltage down across capacitor 2456 and the load output 2460 or any optional choke and/or inductor

(not shown) which may be connected to node 2460 to power the LED or OLED or QD load. Resistor 2462 is used as a current sense resistor and is fed to other parts of the present invention.

[0107] Fig. 25 shows and depicts a version of the present invention suitable for use with both instant start and rapid start ballasts, that implements and allows for current transformation and also allows for emulation of the heater/cathodes in conventional hot cathode florescent tube lamps (HCFL) including, for example, but not limited to less than 1 ft to greater than 8 ft long T5, T8, T9, T10, T12, etc. HCFLs, FLs, CFLs, CCFLs, etc. for use in and with all types of ballasts including, but not limited to, instant-on, instant start, rapid start, programmed start, programmable start, pre-heat, etc. ballasts and any type and form including magnetic and/or electronic ballast(s).

[0108] In Fig. 25, a hazard protection circuit includes a transistor 2576 that turn off current through load output 2594, and thus through the exposed pins of the fluorescent lamp replacement. Capacitors 2502, 2504 and resistor 2512, and capacitors 2506, 2510 and resistor 2522 form a pair of heater emulation circuits, respectively, with capacitors 2504 and/or 2510 (or 2502 and/or 2506) being optional capacitors. In some embodiments 2512, 2522 can be set to very small values or completely shorted out. In other embodiments resistors can be each individually placed in parallel with capacitors 2502, 2504, respectively as well as capacitors 2506, 2510. Resistors 2514, 2520 could be fuses or fuse resistors or thermistors to protect or current limit in conjunction with capacitors 2524, 2526. Capacitors 2524, 2526 can also provide additional protection including protection from AC line and/or, for example in certain specific applications, magnetic ballasts in certain embodiments of the present invention. In certain

embodiments of the present invention, resistors can also be placed in parallel with capacitors 2524 and 2526, respectively. An optional varistor 2516 of any type or form including metal oxide varistors (MOVs), etc. can also be used to limit the voltage that the FLR experiences and/or may be subjected to - however in many embodiments and implementations of the present invention these are not used. Optional transformer 2528 provides current to current and/or voltage to voltage transformation allowing the LED or OLED or QD load connected to load output 2594 to be an appropriate value with for, example, a higher or lower current than typically supplied by the ballast. In some cases and embodiments transformer 2528 is not used. Diodes 2530, 2532, 2534, 2536 form a full wave rectification bridge (which could also consist of synchronous transistors). Capacitors 2540, 2542, diodes 2546, 2562 and resistors 2544, 2560, 2564, 2566 and Zener diode 2570 along with optional capacitor 2572 form a floating power supply connected to the ballast output that can be used to provide the gate turn-on voltage to transistor 2576, a hazard/leakage/fault protection transistor/switch, as well as providing current, voltage and power to other parts of the FLR. Other circuits and implementations can be used for this power supply including some additional examples discussed herein. Diode 2582 is used to isolate the optional output load capacitors 2584, 2592, optional choke 2596 connected to load output 2594, and any LED or OLED or QD load connected to optional choke 2596 or load output 2594 from events including control and protection/limit events that shunt and bring down/reduce the voltage at the anode of diode 2582 in Fig. 25. Resistor 2590 represents the current sense which could be a resistor, current transformer, inductor, sense element of any type or form, etc. Transistor 2574 is turned on to shunt and short the gate of 2576 during fault conditions. Optional

transistor 2586 can be used to connect the floating supply ground to the ground of the FLR. Transistors 2574, 2586 can share the same control and protection signals as shown in Fig. 25 or may have separate signals or a subset of shared signals, etc.

[0109] Turning now to Fig. 26 which illustrates and depicts another implementation of the present invention in which a transformer 2629 with a center tapped secondary is used such that only two diodes 2530, 2532 or synchronous transistors are needed to realize and attain full wave rectification. Note that the primary of the transformer 2528 in various implementations may also be center tapped. Again resistors can be added or remove, put in parallel or series including being put in parallel with capacitors 2524 and 2526. In addition other windings may be used with the present invention to provide power including, but not limited to, bias and auxiliary power, current, voltage, etc. including isolated power, current, voltage, etc. as needed. These other power supplies may be isolated and may be of any type including, but not limited to, forward, flyback, resonant, current-mode, voltage-mode, current-fed, voltage-fed, etc.

[0110] Hazard/leakage/shock protection can be implemented as discussed, illustrated, shown, depicted, discussed, etc. herein including before (for example, using a bidirectional switch to stop/block/etc. the current/voltage from the ballast), after the rectification stage, transformer, etc.

[0111] The example heater/cathode emulation circuits shown in Figs. 25 and 26 in which capacitors 2502, 2504 and resistor 2512, and capacitors 2506, 2510 and resistor 2522 form an example pair of heater emulation circuits, respectively, with capacitors 2504 and/or 2510 (or 2502 and/or 2506) being optional capacitors can also be used with the present invention including but not limited to the figures,

illustrations and discussions presented herein. In addition, circuit functions and features illustrated, depicted, discussed, etc. herein that use analog and/or digital circuits may be implemented using microcontrollers, microprocessors, digital signal processors (DSPs), field programmable gate arrays (FPGAs), etc.

[0112] Hazard/leakage/shock protection can also be accomplished by inserting a bidirectional switch (i.e., in either or both legs of the primary of the transformer. For example, an example embodiment of the present invention would include inserting the primary of the transformer 2704 in between capacitor 2702 and transistor 2706 or in between capacitor 2712 and transistor 2710 as illustrated and depicted in Figs. 27 and 28. The gates of the bidirectional switches can be powered from a floating power supply such as illustrated and depicted in, for example, Figs. 14, 25 and 26 with, for example, a similar detect/monitor and control approach as described herein and depicted, for example, in Figs. 14, 15, 16, 25 and 26.

[0113] The use of capacitors, a switch with capacitors, capacitors and diode bridge or other method of rectification including synchronous transistors, bidirectional switch(es)without the need for a rectifier, including versions that use digital and/or analog and/or microcontrollers, microprocessors, DSPs, FPGAs, etc. can be used to short out the ballast. Capacitors 1402 and/or 1404 (Fig. 14) can also be used to limit the maximum current from the ballast and provide protection including, but not limited to protection from damage to the ballast due to voltage and/or current levels from or across the 50 or 60 Hz AC lines. In some embodiments of the present invention only one capacitor (i.e., 1402 or 1404) is included which could consist of a single capacitor or multiple capacitors that could for example be put in series,

in parallel, in combinations of series and parallel, etc. In other embodiments of the present invention two or more capacitors are used. In some embodiments of the present invention, use of capacitors such as 1402 and/or 1404 in Fig. 14 or corresponding capacitors in other Figs. or any subset or combinations of these may result or assist/aid in increased efficiency. The impedance of these capacitors, for example, can be used to increase the effective AC resistance at the ballast frequency to reduce the voltage (and current) burden while also limiting or assisting in limiting the short circuit current through the ballast in the case of a shorting or shunting event or abnormality.

[0114] Fig. 29 depicts another example embodiment of a detection circuit for shock hazard control is depicted. Op amp (or comparator) 2910 drives transistor 2924 via resistor 2922 if the non-inverting input which is, for the example shown, a voltage divider consisting of resistors 2904, 2906 and optional capacitor 2908 which provides a voltage reference to compare against the inverting input signal coming from feedback signal 2912 representing the voltage across resistor 2062 of Fig. 20 via optional filter consisting of resistor 2914 and capacitor 2916. In the event that the signal from resistor 2062 in Fig. 20 is low, then Op amp (or comparator) 2910 puts out a high signal that drives and turns on transistor 2924 which shorts out the input current to optocoupler 2942 via optional diode 2940 thus preventing optocoupler 2942 from shorting out the gate to source of transistor 2022 in Fig. 20 using output 2944 of optocoupler 2942. The use of diodes, for example, permits multiple outputs to potentially be connected to the optocoupler allowing shutdown of the optocoupler due potentially to multiple reasons and also allowing on/off sequencing which can be helpful with certain types of ballasts. When the voltage

at feedback signal 2912 representing the voltage across resistor 2062 of Fig. 20 is too low, the comparator 2910 turns off transistor 2924, the current through resistor 2926 from Vdd_15 2928 flows through optocoupler 2942, shorting out the gate to source of transistor 2022 in Fig. 20 and turning off the current through the load and therefore through the pins of the fluorescent lamp replacement. In other embodiments, the inverter of transistor 2924 and resistor 2926 is replaced with a one-shot circuit, or timer circuit, monostable multivibrator, pulse generator, etc.

[0115] Turning now to Fig. 30, another example embodiment of an over-voltage protection (OVP) and over-temperature protection (OTP) is shown and illustrated. In this particular embodiment, the over-voltage protection has a voltage reference such as, but not limited to, resistor 3002 and Zener diode 3004 that acts as a reference set point based on voltage rail Vdd_15 3003 which could also be filtered by, for example, a capacitor (not shown) that is fed to the inverting terminal of a comparator 3006 (or similar function such as an op amp). The reference set point is compared in comparator 3006 with, for example, a voltage, scaled in voltage divider 3010, 3012, at node 3008, which is the voltage used to drive the LED or OLED or QD load (e.g., node 2052, Fig. 20). The scaled voltage is fed to the non-inverting input of the comparator/op amp 3006. An optional filter/time constant (not shown) may be used but is not required such that filtering output voltage takes place. When the scaled voltage is lower than the reference set point signal, the comparator 3006 goes low with a negative pulse, discharging capacitor 3014 and turning off the current through resistor 3030, diode 3032 to shutdown signal 3034. When the scaled voltage is higher than the reference set point signal, the comparator 3006 goes high, turning on the current through resistors 3020, 3030, diode

3032 to shutdown signal 3034. Shutdown signal 3034 can be used to drive an optocoupler to short the drain to source of transistor 2022 of Fig. 20, or of transistor 2430 of Fig. 24, or of transistor 2576 of Fig. 25, or of transistor 2676 of Fig. 26.

[0116] In addition, other protection circuits, functions and features can be added/incorporated into the present invention. For example, Fig. 30 also contains an over-temperature protection function – such a function is performed by, for example, but not limited to, a thermistor 3026 in parallel with Zener diode 3004 with both in series with resistor 3002. Again, in general, embodiments of the present invention can use AND, OR, NAND, NOR, and/or other types of Boolean Algebra operations and operations to accomplish various types of functions including but not limited to the optional hiccup mode.

[0117] Figs. 31A–C depict versions of the present invention illustrating physically split apart high frequency rectification components that also can provide current limit and protections. In other words, the embodiments of Figs. 31A-C comprise divided rectifier bridges, each having two halves that can be physically located in the end caps of the fluorescent lamp replacement. Turning to Fig. 31A, capacitors 3102, 3104 are connected to the ballast output at opposite ends of the fluorescent lamp replacement. Capacitor 3102 is followed by diodes 3106, 3110 as a first half of the rectified bridge. At the other end of the fluorescent lamp replacement, capacitor 3104 is followed by diodes 3112, 3114 as the second half of the rectified bridge. LED's (e.g., 3116, 3120, 3122, 3124) are powered by the rectified current from the divided rectifier bridge. Other components can be included as desired, such as, but not limited to, current control circuits, current to current converters, (not shown), fault

detection circuits, etc., diode 3130, capacitor 3132 in parallel with the load, current sense resistor 3134, other protection, etc. A load current switch 3136 can be included in series with the load, hazard protection switch 3140 can be included at any suitable location to shunt current to prevent current from flowing to an abnormal ground in contact with an external pin, etc.

[0118] Turning now to Fig. 32, some embodiments of the present invention may use and/or incorporate microcontrollers (e.g., 3200), FPGAs, microprocessors, DSPs, CLDs, etc. to perform some or all of the functions and capabilities of the present invention including but not limited to detecting and asserting control signals identifying: over voltage 3202, over temperature 3204, shock hazard/pin safety 3206, current control 3210 (i.e., constant current, overcurrent, current to current conversion, etc.), under voltage protection 3212, transient protection, etc. by using signals either directly or derived, filtered, modified, scaled, etc. from voltage(s) 3214, current(s) 3216, temperature(s) 3220, etc. associated, for example, with the ballast and the present invention. A switch 3222 or switches may be directly or indirectly (i.e., isolated, through other circuits, scaled, etc.) connected to the microcontroller, etc. or may be directly connected to the microcontroller, etc. with or without additional components and used to detect the state of the switch (i.e., open or closed including fixed, CW, momentary, 1, 2 or more pole, 1, 2 or more throw, etc.) in terms of enabling or disabling or taking other action(s) when it comes to shock hazard. The microcontroller 3200, etc. can work in conjunction with other components, circuits, switches, devices, etc. including but not limited to those discussed herein. In addition, although not shown in Figs. 32 and 33, the frequency of the ballast or AC line can be detected, measured, sampled, sensed, analyzed,

recorded, stored, etc. for a number of purposes and uses including but not limited to determining whether an electronic ballast is connected to the present invention and making and taking appropriate decisions and actions based on the frequency information/signal. Note: the switch or switches used for shock hazard/pin safety protection of embodiments of the present invention protection can include any suitable semiconductor transistor, including but not limited to bipolar, MOSFET, IGBT, JFET, etc., relay(s) including but not limited to coil, contact, mechanical, electromechanical, Reed, mercury, mercury-wetted, vacuum, solid state, semiconductor, etc. in single, parallel, series, stacked, etc., combinations of these, etc. A remote control signal 3224 can be used to signal to the microcontroller 3200 that the fluorescent lamp replacement has been correctly installed and that pins are enclosed in the fixture. The microcontroller 3200 can then disable the shock hazard/pin safety 3206 system to enable current to flow through the pins to power the load. Turning to Fig. 33, in some embodiments, the remote control signal 3324 is bi-directional, allowing the microcontroller 3200 to transmit status information to a remote device such as a computer, tablet, phone, etc. about the fluorescent lamp replacement. Again, in addition, although not shown in Figs. 32 and 33, the frequency of the ballast or AC line can be detected, measured, sampled, sensed, analyzed, recorded, stored, etc. for a number of purposes and uses including but not limited to determining whether an electronic ballast is connected to the present invention and making and taking appropriate decisions and actions based on the frequency information/signal.

[0119] Turning now to Fig. 34, a block diagram of a fluorescent lamp replacement circuit is depicted that can be used with shock hazard/pin safety protection. An emulation circuit 3402

can be included to emulate various characteristics of an instant start, rapid start, prestart phases of operation in a replaced fluorescent lamp in order that the corresponding ballast operate correctly with the fluorescent lamp replacement. An EMI filter 3406 can be included to manage electromagnetic interference. A power supply such as, but not limited to, a buck converter 3412 or, for example, a buck-boost, boost-buck, boost, fly back, forward converter of any type and kind, push-pull, etc. can be included to power an LED load 3416 from the ballast output.

[0120] The buck converter 3412 can also be a boost-buck, buck-boost, boost, etc. converter. The LED load 3416 may comprise LEDs, OLEDs, QDs, combinations of these, etc. A circuit as disclosed elsewhere herein that contains at least one diode, at least one inductor, and/or at least one switching element/switch can also be included to provide AC line and ballast current control operation and also to manage shock hazard/pin safety. The buck converter 3412 can have OVP, OTP, OCP, shock hazard/pin safety protection, constant current, etc. Normally on (NO) and normally closed (NC) mechanical switches that are, for example single or double (or higher) and single (or higher) pole can be used to indicate when external pins on the fluorescent lamp replacement are exposed.

[0121] The present invention including the figures depicted above can be used with AC line voltage including but not limited to 80 to 305 VAC 50/60 Hz, 347 VAC 50/60 Hz, other 50/60 Hz voltages, magnetic and electronic ballasts, low frequency and high frequency ballasts, instant start, rapid start, programmed start, program start, pre-start, warm, cold, hot types of ballasts, etc.

[0122] Many embodiments and implementations of the present invention use the ballast itself to set the frequencies and time periods rather than using internally generated

frequencies or periods. Some embodiments and implementations of the present invention use both the ballast generated signals and frequencies (and periods) and internally generated frequencies and periods as well as combinations of these, etc. Other embodiments and implementations may use internal signals, frequencies, periods, etc.

[0123] As shown in Fig. 35, the buck converter 3412 or other power supply can be controlled by a dimming signal 3422 as described herein. A dimming controller 3426 can also receive status information as shown in Fig. 36 and as described herein.

[0124] Turning now to Fig. 37, an example embodiment of a fluorescent lamp LED replacement is depicted with hazard/leakage protection and with inductor-driven load output. Constant current can be supplied to the load 3722 from an input current 3700 through diode 3702, resistor 3724, inductor 3716, and transistor 3712. When a control circuit 3710 turns on switch 3712, current is allowed to flow through the load 3722 and to charge the inductor 3716. When current begins to rise as measured using sense resistor 3724, the control circuit 3710 turns off switch 3712, and stored energy from the inductor 3716 flows through diode 3714 and through the load 3722. The control circuit 3710 can thus regulate and control the current through the load 3722 by turning on and off the transistor 3712. The control circuit 3710 can use reference voltages and/or currents from any suitable sources, and time constants can be applied as desired, for example with resistor 3704 and capacitor 3706. Note that the positions of the switching transistor or transistors (e.g., 3712 and 3812) shown in Figs. 37 and 38 along with the respective storage/switching inductors 3716 and 3836 (or transformers, etc.) and buck (or buck-boost, boost-buck, boost) diode 3714, 3842) in Figs. 37 and 38 may be, in general, located in

different positions in the respective schematic drawings and perform the same buck, buck-boost, boost-buck, or boost functions and operations, all of which, for example, can also be used to perform current to current conversion. An example of current to current conversion is, for example, when the ballast output current is different than the load current.

[0125] When an over-voltage, over-current, over-temperature or other condition is detected, the control circuit 3710 can short out the current from the ballast output at node 3700 using transistor 3726, preventing current from node 3700 from reaching the load 3722. Diode 3702 prevents capacitor 3720 from being discharged by the short.

[0126] Turning now to Fig. 38, an example embodiment of a fluorescent lamp LED replacement is depicted with hazard/leakage protection and with transformer-driven load output. Constant current can be supplied to the load 3822 from an input current 3800 through diode 3802, transistor 3812, resistor 3834, and transformer or inductor with a tagalong winding 3836. When a control circuit 3810 turns on switch 3812, current is allowed to flow through the transformer or inductor with a tagalong winding 3836 and load 3822, charging the inductive winding of transformer or inductor with a tagalong winding 3836. When current begins to rise as measured using sense resistor 3834 or in other manners, or in response to other conditions, the control circuit 3810 turns off switch 3812, and stored energy from the transformer or inductor with a tagalong winding 3836 flows through diode 3842 and through the load 3822. The control circuit 3810 can thus regulate and control the current through the load 3822 by turning on and off the transistor 3812. The control circuit 3810 can use reference voltages and/or currents from any suitable sources, and time constants can be applied as desired, for example with resistor 3804 and

capacitor 3806, and feedback from transformer or inductor with a tagalong winding 3836 through diode 3832 and resistor 3830.

[0127] When an over-voltage, over-current, over-temperature or other condition is detected, the control circuit 3810 can short out the current from the ballast output at node 3800 using transistor 3826, preventing current from node 3800 from reaching the load 3822. Diode 3802 prevents capacitors 3820, 3840 from being discharged by the short. A wireless or wired signal can be sent and via reference set point which for example but is not limited to, could be a voltage, the output current to the LED, OLED and/or QD could be reduced or increased as desired. In general, the load current can be higher than the current supplied by the ballast using buck, buck-boost, boost, boost-buck, fly back, forward converters. Cuk, push pull, SEPIC, etc. Also, in general, a voltage can be used to set the dimming level by, for example, decreasing or increasing the voltage with, for example, but not limited to, the voltage being used as a reference and/or set point.

[0128] Turning to Fig. 39, an example embodiment of a ballast control circuit is illustrated and depicted. The control circuit has an optional power supply source that takes power from a rectified power supply at node 3920 that is optionally further regulated using the regulator consisting of resistors 3922, 3924, Zener diode 3926, capacitor 3930 and transistor 3932. Resistor 3934 and Zener diode 3936 along with optional capacitor 3940 form an example voltage reference (although other types of voltage references can be used to achieve a stable voltage reference including, but not limited to, bandgap references, precision voltage references, etc.). Resistors 3942, 3944 form a voltage divider that acts as a reference set point which could also be filtered by, for example, a capacitor (not shown) that is fed to the non-inverting terminal of a comparator 3946 (or similar function

such as an op amp). The voltage from a sense resistor (e.g., resistor 2062 in Fig. 20) is fed to the inverting input of the comparator 3946 via an optional filter/time constant consisting of resistor 3950 and capacitor 3952 such that when the signal from the sense resistor (e.g., resistor 2062 in Fig. 20) is larger than the reference set point signal, the comparator 3946 goes low and provides a negative pulse.

[0129] The negative pulse from comparator 3946 is fed to an inverter made up of MOSFET 3966 and resistor 3970. A time constant can be included to control the rise and/or fall time at the gate of the MOSFET 3966, for example with resistor 3954 and capacitor 3956 and can act, behave and perform as a one-shot. The inverter output is fed to the base of a Darlington pair made up of bipolar junction transistors 3972, 3974 which acts as a shunting transistor. The collector of the Darlington pair at node 3976 can be connected, for example, between the transistor 2022 and the diode 2054 of Fig. 20, or between the transistor 2430 and diode 2454 of Fig. 24, or between the transistor 2576 and diode 2582 of Fig. 25, or between the transistor 2676 and diode 2682 of Fig. 26, shunting the current of the rectified ballast output through the Darlington pair. In other embodiments of the present invention, other types of transistors, including but not limited to, MOSFETs, IGBTs, GaNFETs, SiCFETs, BJTs, etc. can be used in place of the Darlington transistor. Again, this shorts out the ballast and prevents current from reaching the load or capacitor 2056, while diode 2054 prevents capacitor 2056 from being discharged and turning off the load. In the event that the current sensed is too high, then the output of the comparator 3946 (or op amp) goes low which results in turning on the Darlington pair 3972, 3974 (or other types of transistor(s)) to shunt the ballast output current. Other embodiments of the present invention may use different

implementations, circuits, etc. that perform the same/similar function/operation, etc. Again, in general, embodiments of the present invention can use any type or form of circuit, implementation, design, etc.

[0130] Turning now to Fig. 40, another example embodiment of an over-voltage protection (OVP) and over-temperature protection (OTP) circuit is shown and illustrated. Over-temperature protection is provided by voltage divider resistors 4002, 4004, bipolar junction transistor 4006, resistor 4010 and in some embodiments thermistor 4012 can be used with or in place of voltage divider resistors 4002, 4004, bipolar junction transistor (BJT) 4006, resistor 4010 wherein the decrease in the BJT emitter-base voltage of approximately - 2 mV/C is used to reduce the voltage at the inverting pin of comparator 4026. Voltage divider resistors 4002, 4004 and transistor 4006 connect resistor 4010 in parallel with optional thermistor 4012 when the supply voltage (e.g., 15V) at node 4000 based on the ballast output is at the desired level, creating an over-temperature reference voltage across resistor and thermistor 4012 that is temperature dependent. A reference voltage for the over-voltage protection is provided in parallel using, for example, resistor 4014 and Zener diode 4016 that act as a reference set point which could also be filtered by, for example, capacitor 4018. The reference voltage for the over-voltage protection, modified by the over-temperature circuit, is fed to the non-inverting terminal of a comparator 4026 (or similar function such as an op amp).

[0131] The over-voltage and over-temperature reference set point is compared in comparator 4026 with, for example, a voltage, scaled in voltage divider 4022, 4024, at node 4020, which is the voltage used to drive the LED or OLED or QD load (e.g., node 2052, Fig. 20). The scaled voltage is fed to the non-inverting input of the comparator/op amp 4026.

Gain/hysteresis setting resistors 4030, 4032 can be used with the comparator 4026. When the thermistor 4012 gets hot, its resistance decreases, lowering the over-voltage and over-temperature reference set point, which would turn on the comparator 4026 and allow current to flow to shutdown signal 4036. When BJT 4006 gets hot, the base to emitter voltage drops and the collector conducts more current eventually turning on BJT 4006 stronger as the temperature increases and reducing the voltage at the inverting input of comparator 4026.

[0132] When the scaled voltage is higher than the reference set point signal either because of an over-voltage condition at node 4020 or because of an over-temperature condition lowering the reference set point signal, the comparator 4026 goes high, powering the shutdown signal 4036. Shutdown signal 4036 can also be used to drive an optocoupler to short the drain to source of transistor 2022 of Fig. 20, or of transistor 2430 of Fig. 24, or of transistor 2576 of Fig. 25, or of transistor 2676 of Fig. 26, etc.

[0133] In some embodiments, over-voltage protection is provided by a Zener diode 4040 and resistor 4042, transistor 4044 and resistor 4046. If the voltage at node 4000 rises too high, the Zener diode 4040 breaks down and turns on transistor 4042, turning on transistor 4050, which turns off the shutdown signal 4036 and any optocoupler driven by the shutdown signal 4036.

[0134] Turning to Fig. 41, an example ballast shorting circuit is depicted that can be controlled by an over-voltage, over-current, and/or over-temperature or other fault detection circuit in a fluorescent lamp LED replacement. Capacitors 4104, 4110 are connected to the left ballast output, with optional resistors 4102, 4106 in parallel with capacitors 4104, 4110, with a common AC node 4108 between them.

Capacitors 4114, 4120 are connected to the right ballast output, with optional resistors 4112, 4116 in parallel with capacitors 4114, 4120, with a common AC node 4118 between them.

[0135] A resistor 4122 and a common-source MOSFET pair 4124, 4126 are connected between AC nodes 4108, 4118. When the common-source MOSFET pair 4124, 4126 is turned on, it shorts AC nodes 4108, 4118, shorting across the ballast output and preventing current from the ballast output from flowing to a load or other circuits in the fluorescent lamp replacement.

[0136] The common-source MOSFET pair 4124, 4126 is powered by a circuit connected across the common source and the gates of the common-source MOSFET pair 4124, 4126. In some embodiments, this power circuit includes capacitors 4130, 4132 connected to the AC nodes 4108, 4118, followed by a diode bridge 4134, voltage reference circuit including resistor 4136, capacitor 4140, and Zener diode 4142, and voltage divider resistor 4144 that limits or drops the gate voltage.

[0137] An optocoupler 4146 is connected across the common source and the gates of the common-source MOSFET pair 4124, 4126. When the optocoupler 4146 is turned on, it shorts out the common source and gates, turning off common-source MOSFET pair 4124, 4126 and disabling the shorting function of common-source MOSFET pair 4124, 4126. Thus, current is allowed to flow to the load and other circuits in the fluorescent lamp replacement when the optocoupler 4146 is turned on. The optocoupler 4146 can be powered by any suitable circuit, such as, for example, resistors 4156, 4160, capacitor 4162, transistor 4164 and diode 4152, which draws power from Vdd_15 node 4154.

[0138] In the absence of faults such as over-voltage, over-current, or over-temperature, the optocoupler 4146 is turned on to disable the shorting of the ballast by common-source

MOSFET pair 4124, 4126. Such faults can be detected, for example, by the circuits of Figs. 21, 23, 29 or 30, with their output signals connected to node 4150 to turn off the optocoupler 4146 during fault conditions, allowing common-source MOSFET pair 4124, 4126 to conduct and short across the ballast.

[0139] Turning now to Fig. 42, an example embodiment of a fluorescent lamp LED replacement is depicted with a common-gate, common-drain and common-source MOSFET pair for shock hazard protection. The fluorescent lamp LED replacement draws power from a ballast through capacitors 4206, 4212 with optional resistors 4204, 4210, which can be connected, for example, to the AC nodes 4108, 4118 of Fig. 41. A diode bridge 4214 rectifies the AC signal. Such a power connection and diode bridge can be repeated in parallel and/or series as desired to meet power handling requirements.

[0140] A common-gate, common-drain and common-source MOSFET pair 4216, 4220 selectively allows current to flow from the power input and diode bridge 4214, through a diode 4224 to a load output 4226 and parallel capacitors 4230, 4232. One or more current sense resistors 4234 can be connected in series to allow measurement of the load current. When the MOSFET pair 4216, 4220 is turned on, current is allowed to flow to the load output 4226 from the ballast output. During fault conditions, such as when the pins of the fluorescent lamp replacement contact an abnormal ground, the MOSFET pair 4216, 4220 can be turned off by shorting the common gate and common source, blocking current from the ballast output to the load output 4226. Diode 4224 prevents capacitors 4230, 4232 from being shorted and drained during such fault conditions.

[0141] The MOSFET pair 4216, 4220 is powered, for example, from AC nodes 4108, 4118, Fig. 41, by a power supply circuit as

shown in Fig. 42 including capacitors 4240, 4242, diode bridge 4244, resistor 4246, capacitor 4250 and Zener diode 4252.

[0142] As disclosed above, shock hazard/pin safety protection transistors such as, but not limited to, transistor 2202, Fig. 20, or transistor 2430, Fig. 24, or transistor 2576, Figs. 25-26, or MOSFET pair 4216, 4220, Fig. 42, can be turned off using electronic circuits to short the gate to source voltage, and/or by mechanical switches that turn off the shock hazard/pin safety protection transistors when external pins of the fluorescent lamp replacement are exposed.

[0143] Turning to Figs. 43A-43E, an end cap 4300 for a fluorescent lamp LED replacement is depicted with spring-mounted pins 4302, 4304 for shock hazard protection. The pins 4302, 4304 are always electrically connected with main tabs 4306, 4310. The ballast output connections referred to in various circuits disclosed herein are connected to main tabs 4306, 4310, such as, for example, capacitors 4104, 4110, 4114, 4120 of Fig. 41.

[0144] Shock hazard protection tabs 4312, 4314 are floating and disconnected from pins 4302, 4304 when the pins 4302, 4304 the pins are pressed slightly into the end cap 4300 against the springs 4316, 4320, such as when the fluorescent lamp replacement is correctly installed in a fluorescent lamp fixture. When the pins 4302, 4304 are exposed, the springs 4316, 4320 push the pins 4302, 4304 into a fully extended position, where they contact tabs 4312, 4314. This connection between the pins 4302, 4304, tabs 4312, 4314 and main tabs 4306, 4310 when the pins 4302, 4304 are exposed can be used to short across the gate and source of shock hazard/pin safety protection transistors such as, but not limited to, transistor 2202, Fig. 20, or transistor 2430, Fig. 24, or transistor 2576, Figs. 25-26, or MOSFET pair 4216, 4220, Fig. 42, or

across the corresponding Zener diodes used to power those transistors.

[0145] Turning to Figs. 44A-44D, an end cap 4400 for a fluorescent lamp LED replacement is depicted with slide-switch activated pins 4402, 4404 with shock hazard protection. In this embodiment, a mechanical switch 4406 is included in the end cap 4400, which is set to Protect until the fluorescent lamp replacement is correctly installed in a fixture. The Protect setting closes the mechanical switch, for example shorting across the gate and source of shock hazard/pin safety protection transistors such as, but not limited to, transistor 2202, Fig. 20, or transistor 2430, Fig. 24, or transistor 2576, Figs. 25-26, or MOSFET pair 4216, 4220, Fig. 42, or across the corresponding Zener diodes used to power those transistors. When the fluorescent lamp replacement is correctly installed in a fixture, the mechanical switch 4406 is set to Operate, opening the mechanical switch 4406 and allowing shock hazard/pin safety protection transistors such as, but not limited to, transistor 2202, Fig. 20, or transistor 2430, Fig. 24, or transistor 2576, Figs. 25-26, or MOSFET pair 4216, 4220, Fig. 42, to conduct.

[0146] Turning to Figs. 45A-45C, a rotating end cap 4500 for a fluorescent lamp LED replacement is depicted with rotation-activated pins 4502, 4504 with shock hazard protection. In this embodiment, a mechanical switch is included in the end cap 4400 and is actuated by rotating a cuff 4506 on the end cap 4500 in relation to a fixed cuff 4510 (or vice versa). The rotating cuff 4506 is set to Protect until the fluorescent lamp replacement is correctly installed in a fixture. The Protect setting closes the mechanical switch, for example shorting across the gate and source of shock hazard/pin safety protection transistors such as, but not limited to, transistor 2202, Fig. 20, or transistor 2430, Fig. 24, or transistor

2576, Figs. 25-26, or MOSFET pair 4216, 4220, Fig. 42, or across the corresponding Zener diodes used to power those transistors. When the fluorescent lamp replacement is correctly installed in a fixture, the rotating cuff 4506 is set to Operate, opening the mechanical switch 4406 and allowing shock hazard/pin safety protection transistors such as, but not limited to, transistor 2202, Fig. 20, or transistor 2430, Fig. 24, or transistor 2576, Figs. 25-26, or MOSFET pair 4216, 4220, Fig. 42, to conduct.

[0147] The present invention supports all forms and types of dimming of the FLR including by wired and wireless methods for example, but not limited to, controlling the set point/reference for the current or voltage of the FLR. Radio frequency identification (RFID) and similar such systems can be used with the present invention to turn on or off or dim embodiments and implementations of the present invention remotely, voice commands and voice recognition, sound, motion, gesturing, speaking, etc.

[0148] The present invention provides protection against damage and injury to the driver and LED array and damage and injury to the user, installer, other personnel and humans in general

[0149] The switches including the transistor switches may consist of transistors in series or in parallel or both to electrically inhibit/disrupt/break the path/etc. of the ballast current.

[0150] In some embodiments of the present invention, one or more mechanical switches which could be in forms including, but not limited to, a push-button or momentary switch(es) or on-off switch that, for example, when depressed makes contact and completes the circuit may be used with the present invention. The switch can either hold off/disrupt/block/etc. the output voltage of the ballast or be used in conjunction with one or more electronic devices to hold off/block/disrupt

the path of electrical conduction from the ballast output to, for example, to the FLR including to ground in the case of a fault or hazard condition or situation. Embodiments of the present invention can use low voltage switches including, but not limited to, mechanical low voltage switches that typically have no more than 15 to 20 volts potential/voltage difference across the switch contacts to complete, for example, the gate drive to FET or IGBT, etc., including, but not limited to, MOSFETs, JFETs, depletion mode FETs, enhancement mode FETs, MESFETs, HEMTs, MODFETs, GaNFETs, SiCFETs, etc.

[0151] With many common electronic ballasts, including instant start, rapid start, programmed start, programmable start, pre-start, dimmable including wall, triac, wired, wireless, powerline control ballasts, etc., the current typically may be greater than 100 mA and equal to or less than 200 mA with a value typically in the range of 130 mA to 160 mA or slightly less or slightly greater than these values results in uniform performance for most ballasts except for ballasts designed with, for example, a low ballast factor specifically designed to require and supply lower output power to a florescent tube thereby requiring less power and saving energy. In some embodiments which, for example, do not directly shunt the current, the LED or OLED or QD current can be higher, for example in the range of 200 mA to 400 mA or higher for example with inductor (and/or inductor with one or more tag-along winding(s) or transformers, etc.), diode, capacitor circuits such as, but not limited to, buck, buck-boost, boost-buck, boost, fly back, forward converters, push pull, etc.

[0152] Warning of a danger/hazard condition to exist may include a warning light or sound or other means of warning/alerting of such a potential condition/situation. Such a warning may be optional.

[0153] Heater emulators could include incandescent light bulbs, lamps, MEMS resistors, bridges, heaters, filaments, thermostructures, thermocouples, capacitors, resistors, other passive components, inductors, any types of combinations of these, etc.

[0154] Dimming can be accomplished for any type of control including pulsing including but not limited to duty cycle variation, frequency variation, PWM, burp, hiccup, voltage controlled/referenced, etc. in either a shunt or series or combination by, for example, changing the set point that controls, limits, sets, etc. the current or voltage for the florescent tube replacement to the LEDs or OLEDs or QDs. Such control could be, for example, a smaller or larger voltage. Such emulation circuits could also consist of, for example, capacitors and resistors, for example, as shown in Figs. 25, 26 for both rapid and instant-start, programmed start, programmable start, dimmable, pre-start and other types of ballasts. Such circuits could have symmetrical or asymmetrical components and component values. Low pass and or high pass circuit can also be used including for frequency detection/sensing, measuring, etc.

[0155] The series switch for hazard/leakage current protection can also be used to turn off the ballast mode of an universal and ballast mode FLR that can accept, for example, both AC line and electronic ballast output to power the light source/load such as LEDs and OLEDs and quantum dot (QD)-based light sources.

[0156] In some of the particular embodiments, a FET is utilized, however the present invention is not limited to the use of a FET or FETs and other types of switches such as, but not limited to, bipolar junction transistors (BJTs) including all types of BJTs such as npn and pnp, npn Darlingtons and pnp Darlingtons, n-channel or p-channel junction FETs (JFETs),

insulated gate bipolar transistors (IGBTs), all types of MOSFETs including p-channel and n-channel MOSFETs, NFETs, unijunction transistors, etc. made from any type of materials including semiconductors such as silicon, silicon carbide, gallium arsenide, gallium nitride, silicon germanium, indium phosphide, gallium aluminum arsenide, gallium aluminum nitride, etc.

[0157] Note, additional diodes or bridges as illustrated and depicted in the figures may be used in any of the embodiments depicted in the remaining figures and previous figures.

[0158] For example a simple example embodiment of the present invention could include a high frequency diode bridge (or bridges) and a shunt regulator along with protection switch(es) and circuitry. Dithering of, for example, but not limited to, frequency, duty cycle, width, etc. may be used with the example embodiments shown herein and in general for the present invention to, for, example, but not limited to, to provide EMI dithering and reduction.

[0159] Another example embodiment of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges), a shunt regulator and current feedback along with protection switch(es) and circuitry.

[0160] An example embodiment of the present invention includes a fluorescent lamp LED (or OLED or QD) replacement with a high frequency diode bridge (or bridges), a shunt regulator and current feedback and additional over-protection and current control feedback.

[0161] The present invention can also be used with example embodiments of a fluorescent lamp LED replacement that can operate and receive power either from a ballast or from the AC line voltage with a high frequency diode bridge (or bridges) and a current to voltage converter that can be switched to operate a LED driver should a ballast be used with the present

invention or used with AC input voltage applied to the fluorescent fixture terminals.

[0162] The present invention can also be used with example embodiments of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges) and a current to current transformer (or transformation) with a shunt regulator and associated feedback and control to set the current of a LED or OLED, or QD or combinations of these output load.

[0163] The present invention can also be used with example embodiment of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges) and a current to current transformer (or transformation) that feeds a rectification stage with a shunt regulator and associated feedback and control to set the current of a LED or OLED, or QD or combinations of these output load where the feedback and control information is fed back to the shunt regulator.

[0164] The present invention can also be used with an example embodiment of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges) and a current to current transformer (or transformation) with a shunt regulator and associated feedback and control to set the current of a LED or OLED, or QD or combinations of these output load where the feedback and control information is also fed back to the current to current transformation stage and the rectification stage.

[0165] The present invention can also be used with an example embodiment of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges) and a current to current transformer (or transformation) with a shunt regulator and associated feedback and control to set the current of a LED output load where the feedback and control information is also fed back to the current to current transformation stage and the shunt regulator.

[0166] The present invention can also be used with an example embodiment of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges) and a current to current transformer (or transformation) having protection and detection with a shunt regulator and associated feedback and control to set the current of a LED output load where the feedback and control information is also fed back to the current to current transformation stage and the shunt regulator.

[0167] The present invention can also be used with an example embodiment of a fluorescent lamp LED replacement with a high frequency diode bridge (or bridges) and a current to current transformer (or transformation) having protection and detection with a shunt regulator and associated feedback and control to set the current of a LED output load where the feedback and control information is also fed back to the current to current transformation stage and the shunt regulator as well as from the protection and detection stage. Feedback, protection response, etc. can come from and go to one or more of the stages. Features, functions, circuits, operations, etc. discussed and shown herein can also be performed using microcontrollers, microprocessors, DSPs, FPGAs, etc.

[0168] The present invention can also be used with an example embodiment of a ballast driver for a fluorescent lamp LED replacement. High frequency diodes form a high frequency full wave rectification bridge. Additional diodes or bridges may be included as needed or desired. The shunt transistor acts as a shunt switch to shunt current from the ballast as needed or required for a particular application and also serves as a protection against over-current including over-current transients. An additional diode prevents the shorting of the

load (LEDs) when the transistor is turned on and shorts (shunts) the ballast.

[0169] The present invention can also be used with an example embodiment of a ballast driver for a fluorescent lamp LED replacement. High frequency diodes form a high frequency full wave rectification bridge. Additional diodes or bridges may be included as needed or desired. A transistor or transistors acts as a shunt switch to shunt current from the ballast as needed or required for a particular application and also serves as a protection against over-current including over-current transients. An additional diode prevents the shorting of the load (LEDs and/or OLEDs and/or QDs) when the transistor is turned on and shorts (shunts) the ballast. Optional capacitance may be added and may consist of one or more capacitors. An optional resistor acts as a current sense and could be replaced with any other type of current sense element including but not limited to current sense transformers, current transformers, sense transistors, etc.

[0170] Optional capacitance may be added and may consist of one or more capacitors as well as adding an optional inductor and/or an optional sense element which could be a resistor that acts as a current sense or could be any type of current sense element including but not limited to current sense transformers, current transformers, sense transistors, etc.

[0171] The present invention can also be used with an example embodiment of a ballast driver for a fluorescent lamp LED replacement. High frequency diodes form a high frequency full wave rectification bridge. Additional diodes or bridges may be included as needed or desired. Capacitors attached to the input of the high frequency bridge act as a current limiter and also present high impedance elements at low frequencies including, for example, at or around 50 or 60 Hz and limit the current that can be passed to the high frequency bridge and

the rest of the circuit/driver of the FLR so as to protect the circuit from high voltage AC inputs. A shunt switch can be used to shunt current from the ballast as needed or required for a particular application and also serves as a protection against over-current including over-current transients. A diode prevents the shorting of the load (LEDs) when the switch is turned on and shorts (shunts) the ballast by, for example, a Controller, which for the present invention can be used to both regulate and control the protection. Optional capacitance may be added and may consist of one or more capacitors. One or more optional sense elements which could be resistors act as current sense(s) and could also be any type of current sense element including but not limited to current sense transformers, current transformers, sense transistors, etc. Any type of switch, transistor, vacuum tube, semiconductor device, etc. may be used. A resistor and Zener diode may provide a voltage limit protection. Additional elements including but not limited to additional diodes may be added/incorporated/etc. and may also include/incorporate any type of circuit, integrated circuit (IC), microchip(s), microcontroller, microprocessor, digital signal processor (DSP), application specific IC (ASIC), field gate programmable array (FPGA), complex logic device (CLD), analog and/or digital circuit, system, component(s), filters, etc. including, but not limited to, any method to detect frequency including low-pass, high-pass, band-pass, notch filters of any order. Audio detectors, frequency to voltage converters, tone detectors, any form and type of frequency detection, etc. and combinations of these may be used. In other embodiments, circuits that can be either powered or not powered, as the case may be, can be used to enable either ballast circuits or AC line circuits. In addition, voltage and/or current detect circuits may be used in place of or to

augment the frequency detect circuit. The frequency detect circuit can detect and discriminate low frequency (i.e., 47 to 63 Hz, 400 Hz) AC input line frequencies from, for example, kHz (i.e., typically above 32 kHz and often above 40 kHz electronic ballast output frequencies).

[0172] The present invention can also be used with an example embodiment of a ballast and universal AC input driver for a fluorescent lamp LED replacement. Additional diodes or bridges may be included as needed or desired. Inductors along with capacitors can be used as an EMI filter which could also include chokes, resistors, other capacitors, inductors, etc. and other arrangements, implementations, etc. Other EMI filters could be used as needed on other parts of the input or output. An inductor, transistor and a diode can form, for example, a buck or buck-boost converter. Although a buck-boost is mentioned, any type of converter, including, but not limited to, buck, boost, boost-buck, Cuk, SEPIC, flyback, forward-converter, fly-back converter, etc. may be used. High frequency diodes or synchronous transistors can be used to form a high frequency full wave rectification bridge. Capacitors at the input of the high frequency full wave rectification bridge provide both current limiting to the FLR and also act as high impedance elements at low frequencies including, for example, at or around 50 or 60 Hz and limit the current that can be passed to the high frequency bridge and the rest of the circuit/driver even for AC input voltages typically up to 480 VAC and higher if necessary. A transistor can act as a shunt switch to shunt current from the ballast as needed or required for a particular application and also serves as a protection against over-current including over-current transients. A diode prevents the shorting of the load (LEDs or OLEDs or QDs or combinations of these) when either the shunt control transistor or a second over voltage

protection shunt transistor is turned on and shorts (shunts) the ballast. Optional capacitance may be added and may consist of one or more capacitors along with optional resistors in parallel or series or both and, in some embodiments, inductors. Optional sense elements which could be resistors that act as a current sensor or could also be any type of current sense element including but not limited to current sense transformers, current transformers, sense transistors, etc. may also be added. Capacitors and diodes and other elements may be used to form a circuit such that an appreciable and useful voltage is developed, for example, across a resistor and capacitor in parallel with an optional protection device or devices such as a Zener diode to drive and turn on a transistor when the input can provide a high enough drive (i.e., kHz) and has little voltage insufficient to drive and turn on a transistor for frequencies, for example, in the range of 47 to 63 Hz or, also for example, 400 Hz. Although a MOSFET is typically used for the transistor, any type of switch, transistor, vacuum tube, semiconductor device, etc. may be used. Again a Zener diode along with other components can provide, for example, voltage limit protection and also in certain embodiments current limiting. Other transistors may be used in the ballast mode to, for example, provide the return path for the ballast mode if needed. Additional elements including but not limited to additional diodes or other elements including but not limited to resistors, capacitors and/or inductors may be added/incorporated/etc. into the circuitry. The circuit may be any type of circuit, and may contain, for example, integrated circuit (IC), microchip(s), microcontroller, microprocessor, digital signal processor (DSP), application specific IC (ASIC), field gate programmable array (FPGA), complex logic device (CLD), analog and/or digital circuit,

system, component(s), filters, etc. including, but not limited to, any method to detect frequency including low-pass, high-pass, band-pass, notch filters of any order. In addition, voltage and/or current detect circuits may be used in place of or to augment the frequency detect circuit. The frequency detect circuit can detect and discriminate low frequency (i.e., 47 to 63 Hz, 400 Hz) AC input line frequencies from, for example, kHz (i.e., typically above the audio frequencies and usually above 32 kHz and often above 40 kHz electronic ballast output frequencies).

[0173] The present invention can also be used with an example embodiment of a fluorescent lamp LED replacement that accepts either an AC lines input or a ballast output including magnetic (normally low frequency) and electronic (normally high frequency) and supplies a constant current (or constant voltage) to the load (which typically is a LED or OLED array) with the switch(es) set for boost-buck mode with ballast detect and switches, a high frequency diode bridge (or bridges) and a boost-buck (which could also be a buck, boost, buck-boost, Cuk, SEPIC, flyback, forward-converter, etc.) of any type, architecture, topology, etc. including, but not limited to, discontinuous conduction mode (DCM), continuous conduction mode (CCM), critical conduction mode (CRM), resonant conduction mode (RCM), synchronous, etc., a ballast accept circuit including those illustrated in the previous figures, and a load (i.e., LED or OLED). This example embodiment could also include items such as a current to current transformer (or transformation) having protection and detection with a shunt regulator and associated feedback and control to set the current of a LED output load where the feedback and control information is also fed back to other parts of the driver.

[0174] While illustrative embodiments have been described in detail herein, it is to be understood that the concepts disclosed herein may be otherwise variously embodied and employed. In addition, the present invention is applicable to both non-isolated and isolated circuits, including, buck, boost, buck-boost, boost-buck, cuk, fly-back, forward transformers, etc. in, for example, but not limited to, continuous conduction, critical conduction, discontinuous conduction, etc. including resonant approaches, topologies and designs. The present invention can be used in replacement lamps including linear replacement lamps that are designed to provide cool white, bright white, warm white, soft white, etc. (i.e., color ranges that typically span from less than 2700 Kelvin to greater than 6500 Kelvin color temperature with appropriate color rendering index (CRI) and other such optical desired optical performance and perception, etc. The present invention may also be used with multi-color LEDs and organic LEDs (OLEDs) including but not limited to red-green-blue (RGB) LEDs with or without white LEDs, etc. Nothing in this document should be viewed as limiting in any way or form the present invention as applied to protection for LED replacement lamps for fluorescent lamps. For example, some embodiments of the present invention may use color changing, color tunable, color changing with or without white light, color rendering, etc. lighting including red blue green (RGB) with or without white LEDs, OLEDs, QDs or other light sources that can be controlled, tuned, monitored, adjusted, changed, set, etc. using, for example, but not limited to, wireless, wired, powerline control, etc. where the wireless can be, but is not limited to radio frequency (RF) such as WiFi, ZigBee, IEEE 801, ISM bands, and any frequency and/or standard from less than 1 MHz to greater than 1 THz, etc. In addition analytics including input and output power, current, voltage, power

factor, color settings, color rendering, temperature, color temperature, color adjustment, humidity, signal strength, etc. The present invention can also be used in conjunction with dimmers of all types and forms including but not limited to solar dimmers as described in US Patent Application 13/795,149 for a "Solar Powered Portable Control Panel", filed March 12, 2013, which is incorporated herein by reference for all purposes.

[0175] The present invention may also be powered directly from, for example, 100 to 300 VAC 50 Hz or 60 Hz AC line input using any two input wires and, in general, powered from 100 to 277 VAC or higher voltage with a magnetic ballast using, for example, in some embodiments all 4 wires.

[0176] With embodiments of the present invention, the starter will automatically be left unpowered using the present invention by the additional two wires thus the removal of the starter is now unnecessary and optional. Should there be a power factor (PF) capacitor (if applicable) it is now rendered unnecessary with the present invention which can have a very high power factor and the capacitor may, under certain circumstances, actually lower power factor. However the phase and power factor of the present invention can be adjusted as needed. Removal of the capacitor would typically be recommended, but is optional. Any fixture with a magnetic ballast may be left completely unmodified so that either a fluorescent or the present invention may be used interchangeably in such a fixture with a magnetic ballast. In other embodiments of the present invention, where the embodiment(s) is/are only designed for electronic ballasts, the present invention can protect against inadvertent 'plugging in' to AC lines or magnetic ballasts in a number of ways and methods including the use of current limiting devices and components such as capacitors which can also serve as

current/voltage limiting elements to protect electronic only FLRs. In dimming applications, the protection detection/monitoring/control/etc. can interact and know about the dimming requests, level and/or other parameters and adjust and respond accordingly. In one embodiment of the present invention, dimming can only be effected and accomplished after the FRL is safely put into operation so as to offer full protection during the installation process against injuries, harm and fatalities to the installing person or personnel. Such a feature can be made to be automatic each time the lamp is disconnected/ reconnected/installed/etc.

[0177] The present invention supports power factor correction (PFC) especially for the universal AC input mode. The present invention in various embodiments supports all types of dimming including, but not limited, Triac, other types of forward and reverse phase dimming, 0 to 10 V dimming, other remote control, dimming and monitoring including powerline, wired and wireless control, etc. and also allows and supports analytics including data logging of any and all input and output parameters and values including but not limited to power factor, input and output voltage and current, efficiency, VAR, input and output power, input and output real power, etc.

[0178] In some embodiments the same controller can be used for both the series (input voltage controlled mode - IVCM) and shunt (input current controlled mode - ICCM) with, for example, an inversion of the IVCM PWM output for the ICCM. ICCM can be used for constant current control (CCC) implementations and applications.

[0179] The present invention can be used with all types of ballasts including instant-on, pre-heat, rapid start, programmed start, etc. Implementations can be with or without heater connections, can use multiple diodes, heater emulation circuits including both passive and active heater emulation

circuits that can be analog, digital, or combinations of the analog and digital. Such heater circuits can contain resistors, capacitors, inductors, transformers, transistors, switches, diodes, silicon controlled rectifiers (SCR), triacs, other types of semiconductors and ICs including but not limited to op amps, comparators, timers, counters, microcontroller(s), microprocessors, DSPs, FPGAs, ASICs, CLDs, AND, NOR, Inverters and other types of Boolean logic digital components, combinations of the above, etc.

[0180] EMI filters can be included as needed to comply with regulatory and safety agencies. For example, an EMI filter may be required for AC line operation mode or for the ballast operation mode. Such filters can be switched in or out as needed as part of the present invention and can include one or more of the following capacitor, resistors, diodes, inductors, coupled inductors, transformers, etc. In some embodiments of the present invention, a current shunt can be used to convert the current (I) effectively to a voltage (V). In addition the circuits to perform this conversion can work with typical voltage mode circuits and should also work without issue with a DC input. As discussed above, the I-V circuit can be in some embodiments replaced/bypassed or connected through with the EMI filter for standard AC input operation. This switchover and detection can be accomplished by, for example but not limited to, manual switching, automatic switching, detection and switching, analog or digital switching, remote control, remote sensing and control, remote monitoring and control, by frequency detection/selection, current detection/selection, voltage/detection selection, waveform detection/selection, waveform shape, etc. detection/selection, a combination of the above, etc. In some embodiments of the present invention, the manual or autodetect/select can use conventional, mechanical, solid-state, hybrid relays, SCRs,

triacs, transistors including MOSFETs and/or BJTs and other switchable elements. In yet other embodiments, switches, jumpers, cables, matrices, reconfigurable switches and related elements, etc. can be employed. Embodiments of the present invention may include a current limit or limits both for the ballast mode and the AC line mode.

[0181] In some embodiments and applications, there may be a need to have a feedback connection from certain parts of the circuit to the I-V section. For example, if the voltage of the I-V output is set too high it may needlessly circulate current, which would lower the efficiency. This can be addressed with proper detection and feedback to ensure high efficiency.

[0182] Some embodiments of the present invention essentially act and/or perform as a current to current converter in which the constant current from the ballast is fed to the current converter which then converts the current to desired output with the ballast voltage complying with the current and power requirement so long as it does not exceed the operational maximum voltage/power/performance of the ballast.

[0183] In general, the ballast should supply a decent to high quality +/- AC sine wave and, for many electronic ballasts, if the sine wave current is interrupted/stopped, the ballast, especially for electronic ballasts that are considered 'smart' and should be able to detect and capable of detecting faults, will try to respond by taking an appropriate action such as, for example, trying to restart the ballast lamp load or shutting down. The present invention is able to faithfully emulate a fluorescent lamp and provide the necessary performance and behavior for the electronic ballast to operate correctly.

[0184] The current [input] constant current [output] (CCC) shunt design (i.e., ballast mode) of the present invention

works with both ~20 to greater than 100 kHz (typical 40 kHz to 80 kHz) and 50/60/400 Hz constant current input. Embodiments of the present invention can be both low parts count and high efficiency. Some embodiments may include a sine or square-wave conversion stage. The shunt regulator is quite efficient also. In many embodiments of the present invention, at full LED current, little current goes to the shunt, so then the efficiency is very high. With the voltage [input] constant current [output] (i.e., universal AC input mode), the efficiency can also be very high as well as having a very high to ultra high power factor correction/power factor.

[0185] For universal CCC/VCC embodiments, the input terminals can be the same. As illustrated in some of the figures, for some of the embodiments only two blocks are added: a high-frequency bridge rectifier and a Zener including a lossless Zener (shunt regulator).

[0186] In some embodiments of the present invention, when in Line (V) mode the shunt is set to control point could be set to, for example, ~400 V or ~450 V. When in Ballast (I) mode the shunt is set to a lower voltage, corresponding to the designed power of the LED. For example, if the AC line is under ~400 V (or ~450 V) peak, the shunt stays off, so no power or otherwise from the shunt is drawn. This example scheme can also be used with (or without) the frequency detection mode.

[0187] In the event that, for example the manual switching was left in the incorrect configuration, the shunt would use some power and possibly produce some EMI, however the driver would still work and function.

[0188] In Ballast (I) mode the shunt could be set to, for example, ~100V. This would draw less idle power from the ballast, and when the LED was at full power the shunt would typically barely be running/on. If the switch was left in the

wrong position, the shunt would regulate at 400V, resulting in potentially more power loss (which could be addressed and eliminated with appropriate detection and correction), however the driver would still work and operate properly.

[0189] With the present invention, the feedback from the output demand would, in effect, increase the effective resistance/impedance of the converter, thus if the current source went up, the voltage draw would go down thus acting like a negative resistance.

[0190] In some embodiments of the present invention, one or more inductors (as well as and/or in addition to capacitors and other passive and active elements) can be used to keep the LED voltage from going to zero when OVP, OCP, OTP shunt transistors are shorted. Such inductor(s) allows for OVP, OCP, OTP shunt transistors to act as a variable current shunt to ground, with low power loss. With capacitance on the output, capacitance can also be placed on the input to cut down on spurious signals including noise and spikes and to also help with and reduce EMI including radiated EMI. In some embodiments of the present invention, an inductor can also be put in series with the MOSFET, and a clamp diode to contain the flyback voltage. In some embodiments of the present invention, inductors can be put on either or both the input and/or output to also provide filtering to reduce the ripple to the load (i.e., LED array). The switching frequency of, for example, OVP, OCP, OTP shunt transistors could typically be in the range of 20 kHz or higher (i.e., typically above the human audio range) or, in the case of overcurrent or overvoltage conditions, possibly lower and even much lower than 20 kHz or higher. For dimming, and for example, when using PWM dimming, the frequency of the PWM dimming can be much lower and typically in the range of ~100 Hz and higher. For switching and dimming switching, switching can be done on

either side of the transformer for embodiments of the present invention depending on considerations that, for example, determine the appropriate placement.

[0191] Embodiments of the present invention allow for no, passive and/or active control. Some embodiments of the present invention provide in the matching circuit, for example, a chopper that typically can be switching in a frequency range of less than 20 kHz to greater than 100 kHz, either free running, self-oscillating or controlled, so that the transformer or equivalent current to current transformer and/or converter can be small even with a 60 Hz ballast. In addition, by providing a regulator circuit, can make, for example, the LED independent of the ballast, and therefore universal.

[0192] In some embodiments of the present invention, the converter used for the series regulation from the AC lines can also be used for the shunt regulation from the ballast output, with the control inverted from a normal voltage-in/voltage-out converter or voltage-in/current-out operation.

[0193] With a ballast, the present some implementations of the present invention utilize current output control with a shunt regulator with switching mode regulation chosen to keep it efficient. In this case, the regulator switches to effective/local ground (low voltage drop equals low power dissipation) or open (no current equals low power dissipation). In addition to the passive and active components mentioned previously, other protection and detection devices and components can be used with the present invention including but not limited to tranzorbs, transient voltage suppressors (TVSs), Varistors, metal oxide varistors (MOVs), surge absorbers, surge arrestors, and other transients detection and protection devices, thermistors or other thermal devices, fuses, resettable fuses, circuit breakers, solid-

state circuit breakers and relays, other types of relays including mechanical relays and circuit breakers, etc.

[0194] In embodiments of the present invention that include or involve buck, buck-boost, boost, boost-buck, etc. inductors, one or more tagalong inductors such as those disclosed in US Patent Application 13/674,072, filed November 11, 2012 by Sadwick et al. for a "Dimmable LED Driver with Multiple Power Sources", which is incorporated herein for all purposes, may be used and incorporated into embodiments of the present invention. Such tagalong inductors can be used, among other things and for example, to provide power and increase and enhance the efficiency of certain embodiments of the present invention. In addition, other methods including charge pumps, floating diode pumps, level shifters, pulse and other transformers, bootstrapping including bootstrap diodes, capacitors and circuits, floating gate drives, carrier drives, etc. can also be used with the present invention.

[0195] Programmable soft start including being able to also have a soft short at turn-on which then allows the input voltage to rise to its running and operational level can also be included in various implementations and embodiments of the present invention.

[0196] Some embodiments of the present invention utilize high frequency diodes including high frequency diode bridges and/or synchronous transistor rectifier bridges and current to voltage conversion to transform the ballast output into a suitable form so as to be able to work with existing AC line input PFC-LED circuits and drivers. Some other embodiments of the present invention utilize high-frequency diodes and/or synchronous transistor rectifier bridges to transform the AC output of the electronic ballast (or the low frequency AC output of a magnetic ballast into a direct current (DC) format that can be used directly or with further current or voltage

regulation to power and driver LEDs for a fluorescent lamp replacement. In some embodiments of the present invention, snubber and/or clamp circuits may be used with the rectification stages (which, for example, could be diodes or transistors operating in a synchronous mode); such snubbers could typically include capacitors, resistors and/or diodes or be of a lossless type of snubber where the energy is recycled or be made of capacitors only or resistors only, etc. Such snubbers can be of benefit in reducing radiated emissions. Some embodiments of the present invention can use lossless snubbers. Embodiments of the present invention can be used to convert the low frequency (i.e., typically 50 or 60 Hz) AC line and/or magnetic ballast AC as well as electronic higher frequency AC output to an appropriate current or voltage to drive and power LEDs using either or both shunt or series regulation. Some other embodiments of the present invention combine one or more of these. In some embodiments of the present invention, one or more switches can be used to clamp the output compliance current and/or voltage of the ballast. Various implementations of the present invention can involve voltage or current forward converters and/or inverters, square-wave, sine-wave, resonant-wave, etc. that include, but are not limited to, push pull, half-bridge, full-bridge, square wave, sine wave, fly-back, resonant, synchronous, linear regulation, buck, buck-boost, boost buck, boost, etc.

[0197] For the present invention, in general, any type of transistor or vacuum tube or other similarly functioning device can be used including, but not limited to, MOSFETs, JFETs, GANFETs, depletion or enhancement FETs, N and/or P FETs, CMOS, NPN and/or PNP BJTs including Darlington transistors, triodes, etc. which can be made of any suitable material and configured to function and operate to provide the performance, for example, described above. In addition, other

types of devices and components can be used including, but not limited to transformers, transformers of any suitable type and form, coils, level shifters, digital logic, analog circuits, analog and digital, mixed signals, microprocessors, microcontrollers, FPGAs, CLDs, PLDs, comparators, op amps, instrumentation amplifiers, and other analog and digital components, circuits, electronics, systems etc. For all of the example figures shown, the above analog and/or digital components, circuits, electronics, systems etc. are, in general, applicable and usable in and for the present invention.

[0198] The example figure and embodiments shown are merely intended to provide some illustrations of the present inventions and not limiting in any way or form for the present inventions.

[0199] Using digital and/or analog designs and/or microcontrollers and /or microprocessors any and all practical combinations of control, sequencing, levels, etc., some examples of which are listed below for the present invention, can be realized.

[0200] In addition to these examples, a potentiometer or similar device such as a variable resistor may be used to control the dimming level. Such a potentiometer may be connected across a voltage such that the wiper of the potentiometer can swing from minimum voltage (i.e., full dimming) to maximum voltage(i.e., full light). Often the minimum voltage will be zero volts which may correspond to full off and, for the example embodiments shown here, the maximum will be equal to or approximately equal to the voltage on the negative input of the comparator. In addition wireless control including dimming may be used to, for example, set the reference current setpoint used, for example, to control the current supplied to the LEDs or OLEDs or QDs, etc.

[0201] Current sense methods including resistors, current transformers, current coils and windings, etc. can be used to measure and monitor the current of the present invention and provide both monitoring and protection.

[0202] In addition to dimming by adjusting, for example, a potentiometer, the present invention can also support all standards, ways, methods, approaches, techniques, etc. for interfacing, interacting with and supporting, for example, 0 to 10 V dimming by, for example, using a suitable reference voltage that can be remotely set or set via an analog or digital input such as illustrated in patent application 61/652,033 filed on May 25, 2012, for a "Dimmable LED Driver", which is incorporated herein by reference for all purposes.

[0203] The present invention supports all standards and conventions for 0 to 10 V dimming or other dimming techniques. In addition the present invention can support, for example, overcurrent, overvoltage, short circuit, and over-temperature protection. The present invention can also measure and monitor electrical parameters including, but not limited to, input current, input voltage, power factor, apparent power, real power, inrush current, harmonic distortion, total harmonic distortion, power consumed, watthours (WH) or killowatt hours (kWH), etc. of the load or loads connected to the present invention. In addition, in certain configurations and embodiments, some or all of the output electrical parameters may also be monitored and/or controlled directly for, for example, LED drivers and FL ballasts. Such output parameters can include, but are not limited to, output current, output voltage, output power, duty cycle, PWM, dimming level(s), etc.

[0204] In place of the potentiometer, an encoder or decoder can be used. The use of such also permits digital signals to be used and allows digital signals to either or both locally or

remotely control the dimming level and state. A potentiometer with an analog to digital converter (ADC) or converters (ADCs) could also be used in many of such implementations of the present invention.

[0205] The above examples and figures are merely meant to provide illustrations of the present and should not be construed as limiting in any way or form for the present invention.

[0206] In addition to the examples above and any combinations of the above examples, the present invention can have multiple dimming levels set by the dimmer in conjunction with the motion sensor and photosensor/photodetector and/or other control and monitoring inputs including, but not limited to, analog (e.g., 0 to 10 V, 0 to 3 V, etc.), digital (RS232, RS485, USB, DMX, SPI, SPC, UART, other serial interfaces, etc.), a combination of analog and digital, analog-to-digital converters and interfaces, digital-to-analog converters and interfaces, wired, wireless (i.e., RF, WiFi, ZigBee, Zwave, ISM bands, 2.4 GHz, etc.), powerline (PLC) including X-10, Insteon, HomePlug, etc.), etc.

[0207] The present invention is highly configurable and words such as current, set, specified, etc. when referring to, for example, the dimming level or levels, may have similar meanings and intent or may refer to different conditions, situations, etc. For example, in a simple case, the current dimming level may refer to the dimming level set by, for example, a control voltage from a digital or analog source including, but not limited to digital signals, digital to analog converters (DACs), potentiometer(s), encoders, etc.

[0208] The present invention can have embodiments and implementations that include manual, automatic, monitored, controlled operations and combinations of these operations. The present invention can have switches, knobs, variable

resistors, encoders, decoders, push buttons, scrolling displays, cursors, etc. The present invention can use analog and digital circuits, a combination of analog and digital circuits, microcontrollers and/or microprocessors including, for example, DSP versions, FPGAs, CLDs, ASICs, etc. and associated components including, but not limited to, static, dynamic and/or non-volatile memory, a combination and any combinations of analog and digital, microcontrollers, microprocessors, FPGAs, CLDs, etc. Items such as the motion sensor(s), photodetector(s)/photosensor(s), microcontrollers, microprocessors, controls, displays, knobs, etc. may be internally located and integrated/incorporated into the dimmer or externally located. The switches/switching elements can consist of any type of semiconductor and/or vacuum technology including but not limited to triacs, transistors, vacuum tubes, triodes, diodes or any type and configuration, pentodes, tetrodes, thyristors, silicon controlled rectifiers, diodes, etc. The transistors can be of any type(s) and any material(s) – examples of which are listed below and elsewhere in this document.

[0209] The dimming level(s) can be set by any method and combinations of methods including, but not limited to, motion, photodetection/light, sound, vibration, selector/push buttons, rotary switches, potentiometers, resistors, capacitive sensors, touch screens, touch sensor(s), wired, wireless, PLC interfaces, etc. In addition, both control and monitoring of some or all aspects of the dimming, motion sensing, light detection level, sound, etc. can be performed for and with the present invention.

[0210] Other embodiments can use other types of comparators and comparator configurations, other op amp configurations and circuits, including but not limited to error amplifiers, summing amplifiers, log amplifiers, integrating amplifiers,

averaging amplifiers, differentiators and differentiating amplifiers, etc. and/or other digital and analog circuits, microcontrollers, microprocessors, complex logic devices (CLDs), field programmable gate arrays (FPGAs), etc.

[0211] The dimmer for dimmable drivers may use and be configured in continuous conduction mode (CCM), critical conduction mode (CRM), discontinuous conduction mode (DCM), resonant conduction modes, etc., with any type of circuit topology including but not limited to buck, boost, buck-boost, boost-buck, cuk, SEPIC, flyback, forward-converters, linear regulators, etc. The present invention works with both isolated and non-isolated designs including, but not limited to, buck, boost-buck, buck-boost, boost, cuk, SEPIC, flyback and forward-converters. The present invention itself may also be non-isolated or isolated, for example using a tagalong inductor or transformer winding or other isolating techniques, including, but not limited to, transformers including signal, gate, isolation, etc. transformers, optoisolators, optocouplers, etc.

[0212] The present invention may include other implementations that contain various other control circuits including, but not limited to, linear, square, square-root, power-law, sine, cosine, other trigonometric functions, logarithmic, exponential, cubic, cube root, hyperbolic, etc. in addition to error, difference, summing, integrating, differentiators, etc. type of op amps. In addition, logic, including digital and Boolean logic such as AND, NOT (inverter), OR, Exclusive OR gates, etc., complex logic devices (CLDs), field programmable gate arrays (FPGAs), microcontrollers, microprocessors, application specific integrated circuits (ASICs), etc. can also be used either alone or in combinations including analog and digital combinations for the present invention. The

present invention can be incorporated into an integrated circuit, be an integrated circuit, etc.

[0213] The present invention can also incorporate at an appropriate location or locations one or more thermistors (i.e., either of a negative temperature coefficient [NTC] or a positive temperature coefficient [PTC]) to provide temperature-based load current limiting.

[0214] As an example, when the temperature rises at the selected monitoring point(s), the phase dimming of the present invention can be designed and implemented to drop, for example, by a factor of, for example, two. The output power, no matter where the circuit was originally in the dimming cycle, will also drop/decrease by some factor. Values other than a factor of two (i.e., 50%) can also be used and are easily implemented in the present invention by, for example, changing components of the example circuits described here for the present invention. As an example, a resistor change would allow and result in a different phase/power decrease than a factor of two. The present invention can be made to have a rather instant more digital-like decrease in output power or a more gradual analog-like decrease, including, for example, a linear decrease in output phase or power once, for example, the temperature or other stimulus/signal(s) trigger/activate this thermal or other signal control.

[0215] In other embodiments, other temperature sensors may be used or connected to the circuit in other locations. The present invention also supports external dimming by, for example, an external analog and/or digital signal input. One or more of the embodiments discussed above may be used in practice either combined or separately including having and supporting both 0 to 10 V and digital dimming. The present invention can also have very high power factor. The present invention can also be used to support dimming of a number of

circuits, drivers, etc. including in parallel configurations. For example, more than one driver can be put together, grouped together with the present invention. Groupings can be done such that, for example, half of the dimmers are forward dimmers and half of the dimmers are reverse dimmers. Again, the present invention allows easy selection between forward and reverse dimming that can be performed manually, automatically, dynamically, algorithmically, can employ smart and intelligent dimming decisions, artificial intelligence, remote control, remote dimming, etc.

[0216] The present invention may be used in conjunction with dimming to provide thermal control or other types of control to, for example, a dimming LED driver. For example, embodiments of the present invention may also be adapted to provide overvoltage or overcurrent protection, short circuit protection for, for example, a dimming LED or OLED or QD driver, etc., or to override and cut the phase and power to the dimming LED driver(s) based on any arbitrary external signal(s) and/or stimulus. The present invention can also be used for purposes and applications other than lighting - as an example, electrical heating where a heating element or elements are electrically controlled to, for example, maintain the temperature at a location at a certain value. The present invention can also include circuit breakers including solid state circuit breakers and other devices, circuits, systems, etc. that limit or trip in the event of an overload condition/situation. The present invention can also include, for example analog or digital controls including but not limited to wired (i.e., 0 to 10 V, RS 232, RS485, IEEE standards, SPI, I2C, other serial and parallel standards and interfaces, etc.), wireless, powerline, etc. and can be implemented in any part of the circuit for the present invention. The present invention can be used with a buck, a

buck-boost, a boost-buck and/or a boost, flyback, or forward-converter design, topology, implementation, etc.

[0217] A dimming voltage signal, VDIM, which represents a voltage from, for example but not limited to, a 0-10 V Dimmer can be used with the present invention; when such a VDIM signal is connected, the output as a function time or phase angle (or phase cut) will correspond to the inputted VDIM.

[0218] Other embodiments can use comparators, other op amp configurations and circuits, including but not limited to error amplifiers, summing amplifiers, log amplifiers, integrating amplifiers, averaging amplifiers, differentiators and differentiating amplifiers, etc. and/or other digital and analog circuits, microcontrollers, microprocessors, complex logic devices, field programmable gate arrays, etc.

[0219] The present invention includes implementations that contain various other control circuits including, but not limited to, linear, square, square-root, power-law, sine, cosine, other trigonometric functions, logarithmic, exponential, cubic, cube root, hyperbolic, etc. in addition to error, difference, summing, integrating, differentiators, etc. type of op amps. In addition, logic, including digital and Boolean logic such as AND, NOT (inverter), OR, Exclusive OR gates, etc., complex logic devices (CLDs), field programmable gate arrays (FPGAs), microcontrollers, microprocessors, application specific integrated circuits (ASICs), etc. can also be used either alone or in combinations including analog and digital combinations for the present invention. The present invention can be incorporated into an integrated circuit, be an integrated circuit, etc.

[0220] The present invention described above primarily for motion and light/photodetection control, can and may also use other types of stimuli, input, detection, feedback, response, etc. including but not limited to sound, voice, voice control,

motion, gesturing, vibration, frequencies above and below the typical human hearing range, temperature, humidity, pressure, light including below the visible (i.e., infrared, IR) and above the visible (i.e., ultraviolet, UV), radio frequency signals, combinations of these, etc. For example, the motion sensor may be replaced or augmented with a sound sensor (including broad, narrow, notch, tuned, tank, etc. frequency response sound sensors), a voice sensor and/or detector, voice recognition, and the light sensor could consist of one or more of the following: visible, IR, UV, etc. sensors. In addition, the light sensor(s)/detector(s) can also be replaced or augmented by thermal detector(s)/sensor(s), etc.

[0221] The example embodiments disclosed herein illustrate certain features of the present invention and not limiting in any way, form or function of present invention. The present invention is, likewise, not limited in materials choices including semiconductor materials such as, but not limited to, silicon (Si), silicon carbide (SiC), silicon on insulator (SOI), other silicon combination and alloys such as silicon germanium (SiGe), etc., diamond, graphene, gallium nitride (GaN) and GaN-based materials, gallium arsenide (GaAs) and GaAs-based materials, etc. The present invention can include any type of switching elements including, but not limited to, field effect transistors (FETs) of any type such as metal oxide semiconductor field effect transistors (MOSFETs) including either p-channel or n-channel MOSFETs of any type, junction field effect transistors (JFETs) of any type, metal emitter semiconductor field effect transistors, etc. again, either p-channel or n-channel or both, bipolar junction transistors (BJTs) again, either NPN or PNP or both including, but not limited to, Darlington transistors, heterojunction bipolar transistors (HBTs) of any type, high electron mobility transistors (HEMTs) of any type, unijunction transistors of

any type, modulation doped field effect transistors (MODFETs) of any type, etc., again, in general, n-channel or p-channel or both, vacuum tubes including diodes, triodes, tetrodes, pentodes, etc. and any other type of switch, etc.

[0222] While detailed descriptions of one or more embodiments of the invention have been given above, various alternatives, modifications, and equivalents will be apparent to those skilled in the art without varying from the spirit of the invention. Therefore, the above description should not be taken as limiting the scope of the invention, which is defined by the appended claims.

What is claimed is:

1. An apparatus for replacing a fluorescent lamp, comprising:

a plurality of pins configured to electrically connect to a fluorescent lamp fixture;

at least one non-fluorescent light source;

a transistor between at least one of the plurality of pins and the at least one non-fluorescent light source; and

a shock hazard protection circuit configured to disable the transistor to limit current flowing through at least some of the plurality of pins.

2. The apparatus of claim 1, wherein the shock hazard protection circuit comprises a mechanical switch.

3. The apparatus of claim 2, wherein the mechanical switch is normally open.

4. The apparatus of claim 2, wherein the mechanical switch is normally closed.

5. The apparatus of claim 1, wherein the shock hazard protection circuit comprises an under-current detection circuit configured to detect a lower than expected current to the plurality of pins.

6. The apparatus of claim 1, wherein the shock hazard protection circuit comprises an optocoupler connected across a control input of the transistor and another lead of the transistor.

7. The apparatus of claim 1, wherein the shock hazard protection circuit comprises an optocoupler connected across a gate and a source of the transistor.

8. The apparatus of claim 1, further comprising a ballast short circuit connected across the plurality of pins, and a fault detection circuit configured to control the ballast short circuit.

9. The apparatus of claim 8, wherein the fault detection circuit comprises an over-voltage detection circuit.

10. The apparatus of claim 8, wherein the fault detection circuit comprises an over-current detection circuit.

11. The apparatus of claim 8, wherein the fault detection circuit comprises an over-temperature detection circuit.

12. The apparatus of claim 8, wherein the fault detection circuit is configured to short an AC current across the plurality of pins.

13. The apparatus of claim 8, further comprising a diode connected between the transistor and the at least one non-fluorescent light source, wherein the fault detection circuit is configured to short a DC current between the transistor and the at least one non-fluorescent light source.

14. The apparatus of claim 13, further comprising at least one capacitor connected in parallel with the at least one non-fluorescent light source downstream from the diode.

15. The apparatus of claim 1, wherein the transistor comprises a common-gate, common-source, common-drain MOSFET pair.

16. The apparatus of claim 1, further comprising a constant-current regulation circuit.

17. The apparatus of claim 16, further comprising a processor having a remote control interface.

18. The apparatus of claim 17, wherein the processor is configured to transmit status information through the remote control interface.

19. The apparatus of claim 17, wherein the processor is configured to receive dimming commands through the remote control interface and to control the constant-current regulation circuit based at least in part on the dimming commands.

20. The apparatus of claim 17, wherein the shock hazard protection circuit is implemented at least in part by the processor.

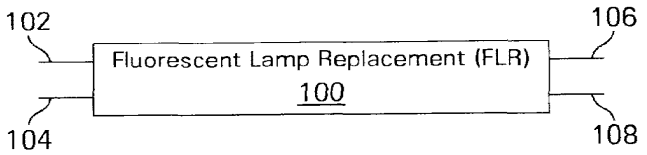


FIG. 1

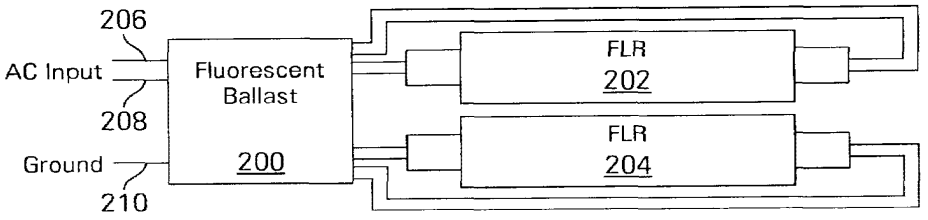


FIG. 2

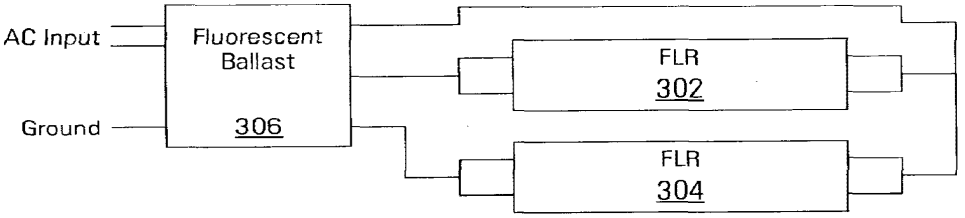


FIG. 3

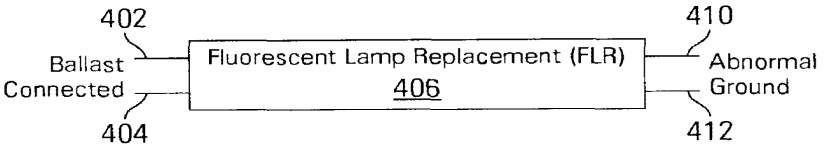


FIG. 4

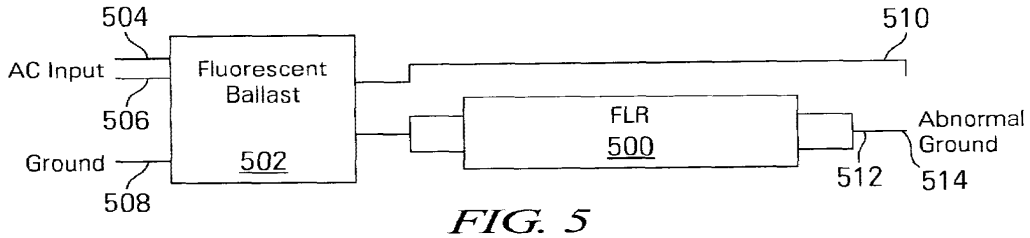


FIG. 5

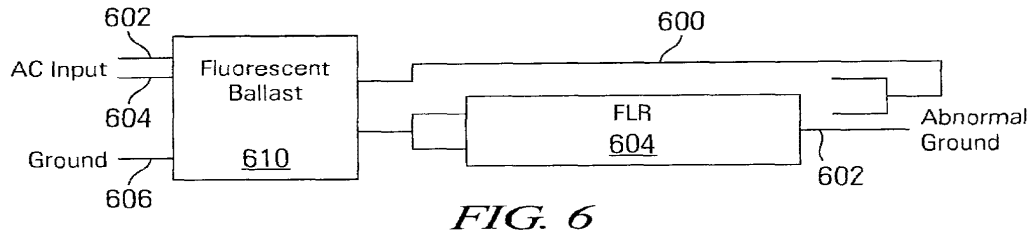


FIG. 6

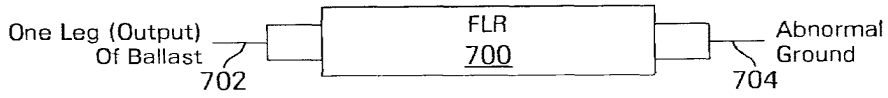


FIG. 7

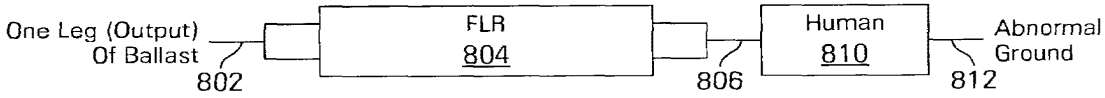


FIG. 8

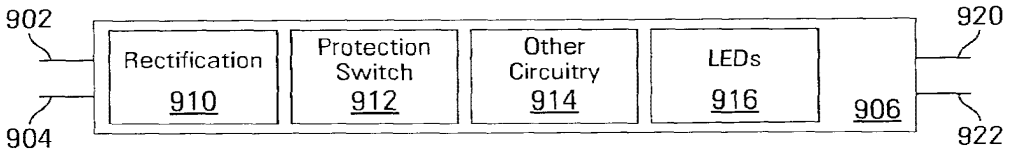


FIG. 9

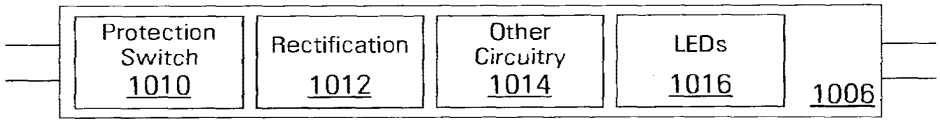


FIG. 10

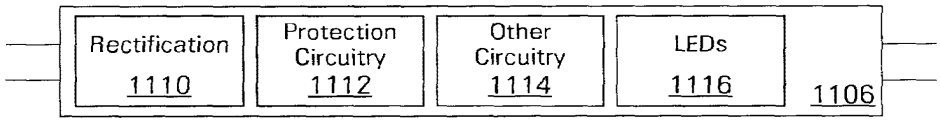


FIG. 11

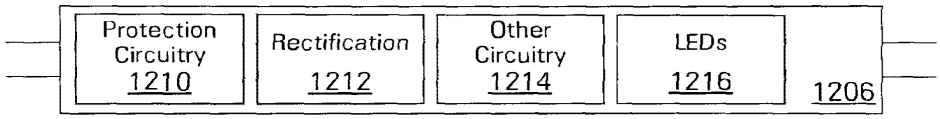


FIG. 12

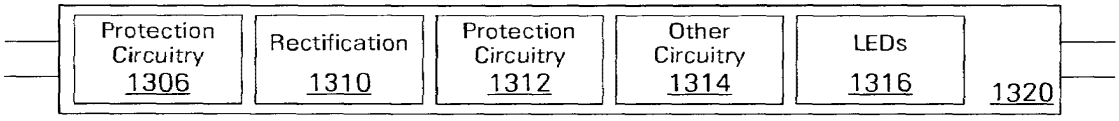


FIG. 13

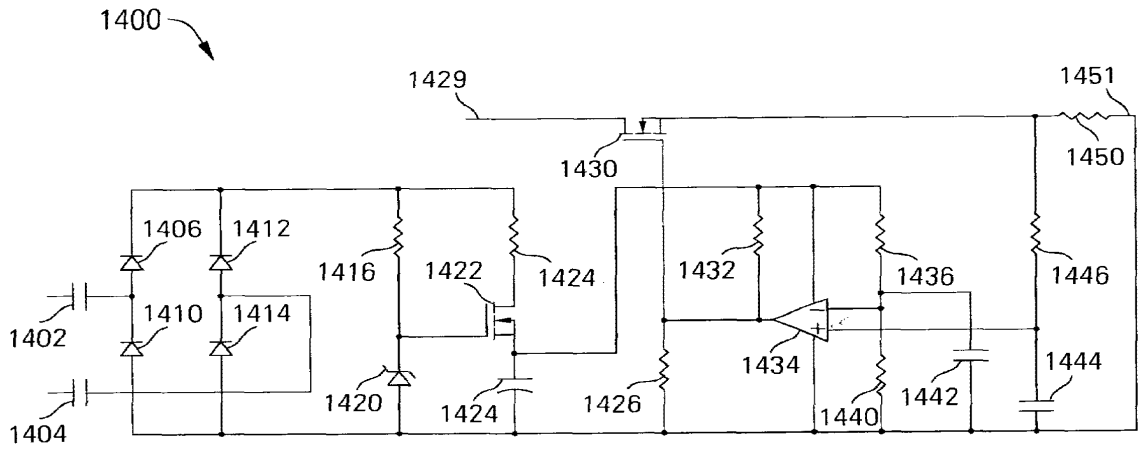

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FIG. 14

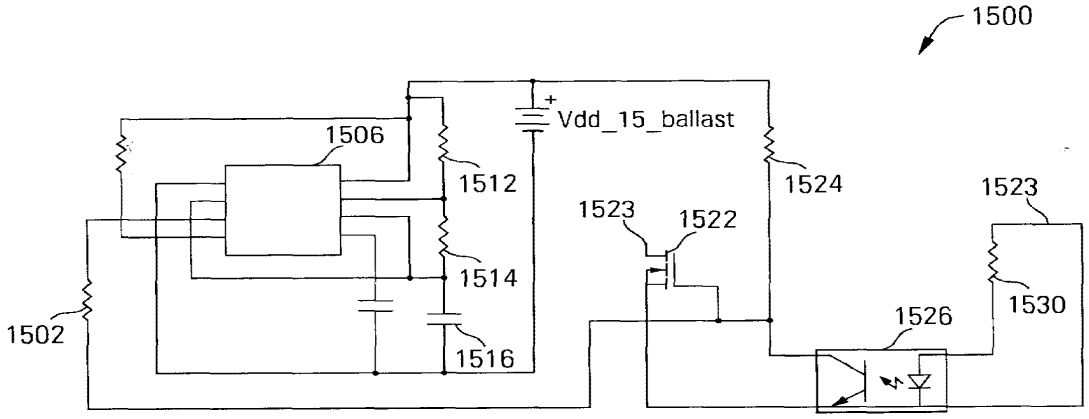

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FIG. 15

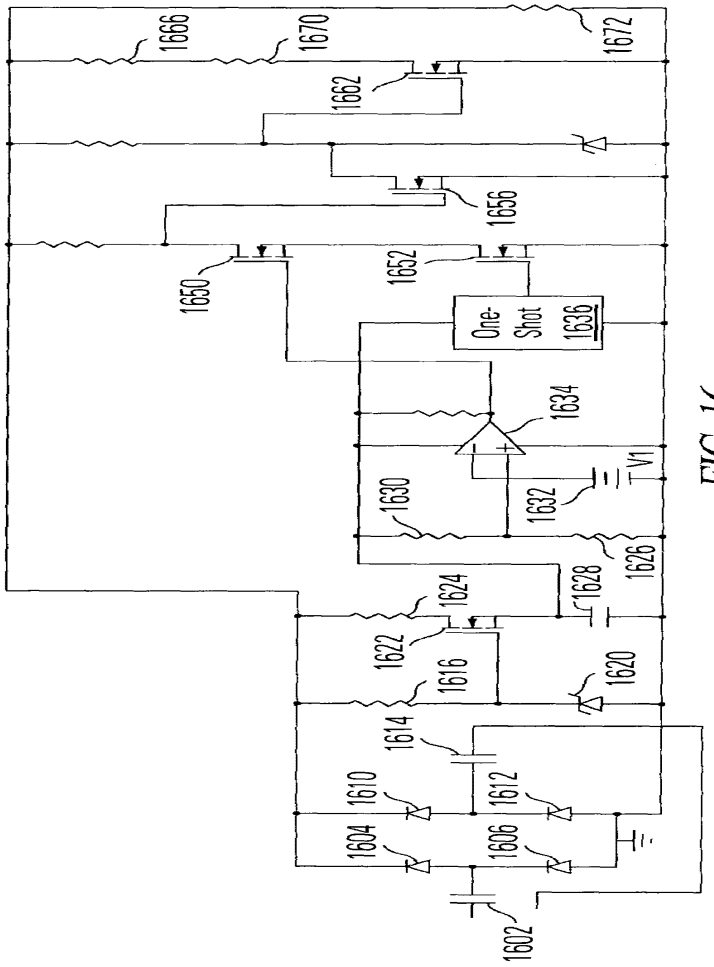

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FIG. 16

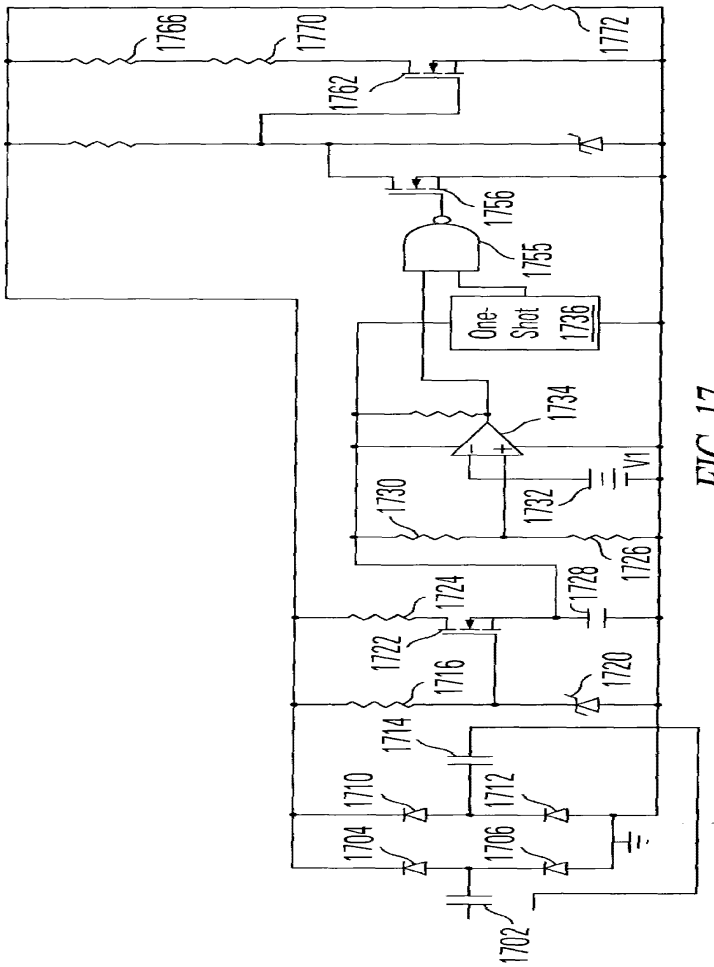

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FIG. 17

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FIG. 18

FIG. 19

FIG. 20

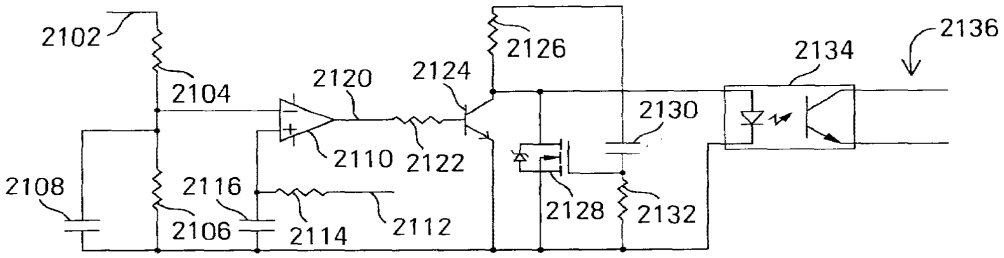


FIG. 21

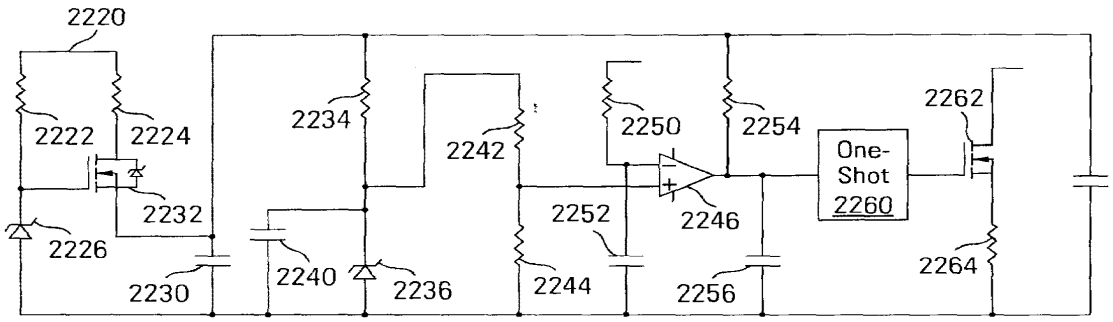


FIG. 22

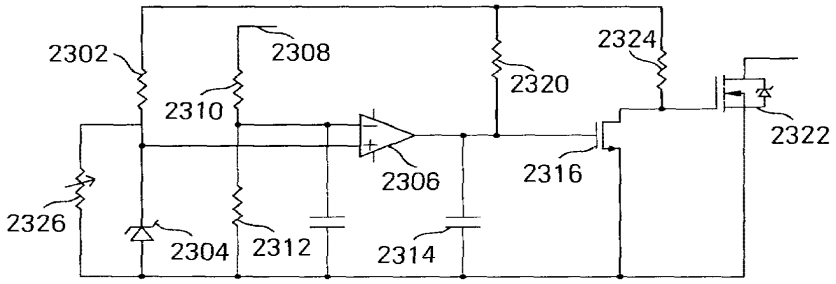


FIG. 23

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FIG. 24

FIG. 25

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FIG. 26

FIG. 27

FIG. 28

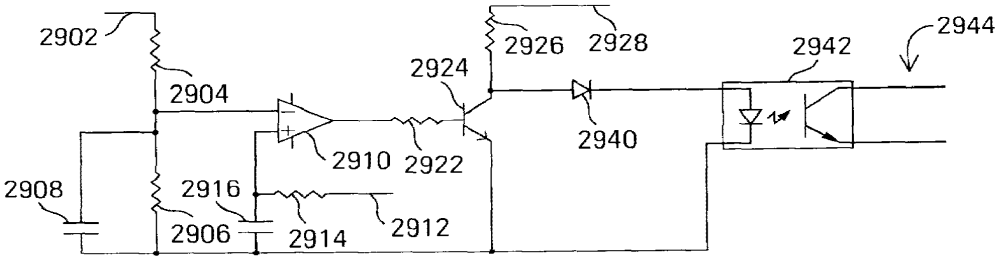


FIG. 29

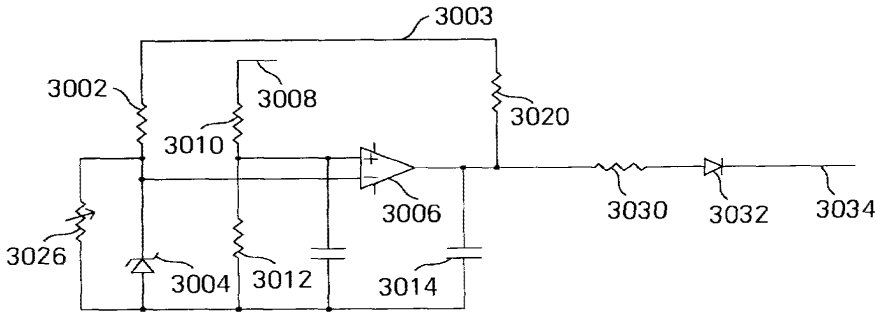


FIG. 30

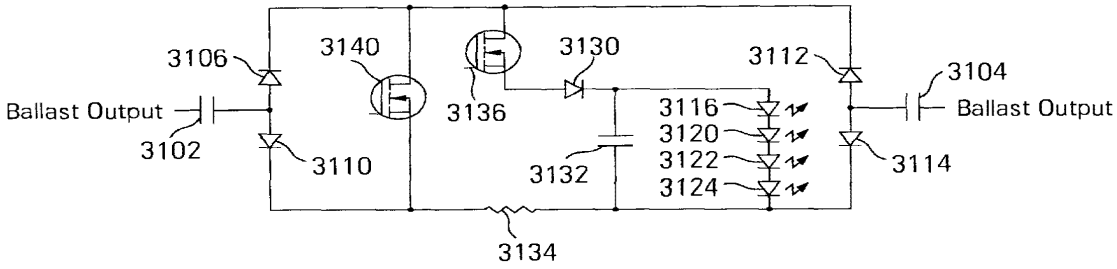


FIG. 31A

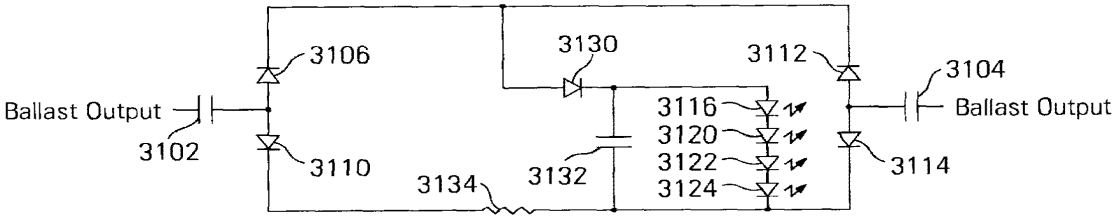


FIG. 31B

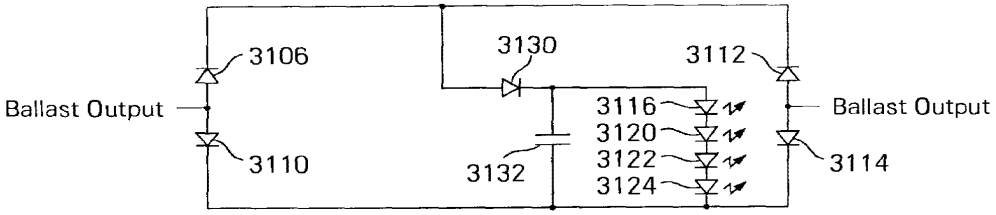


FIG. 31C

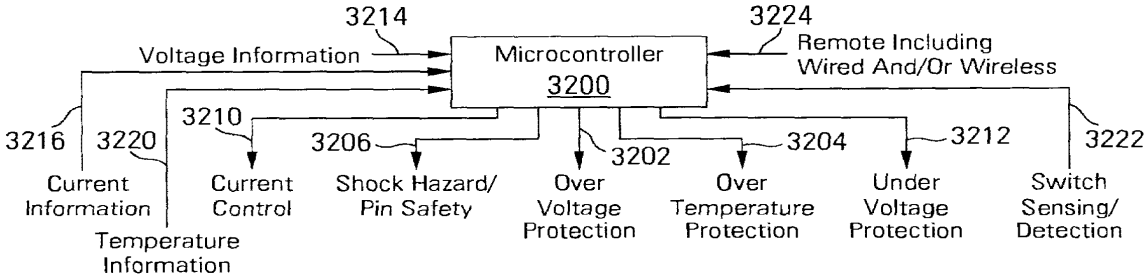


FIG. 32

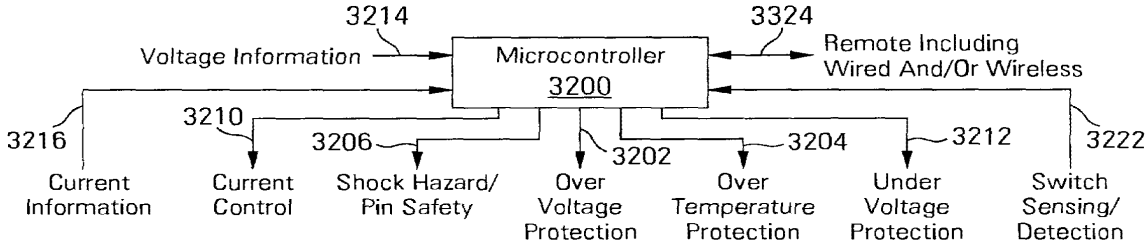


FIG. 33

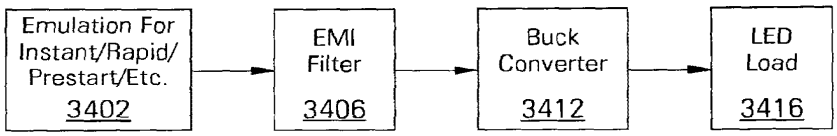


FIG. 34

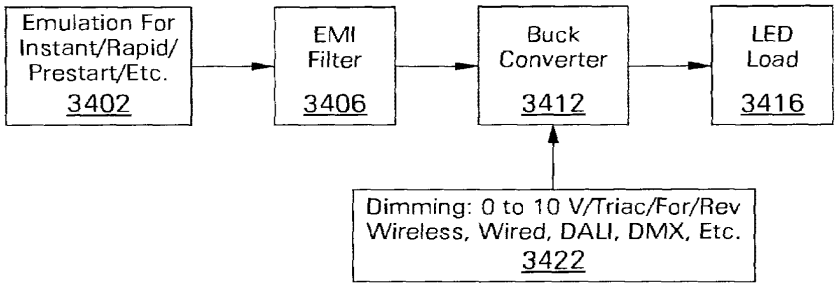


FIG. 35

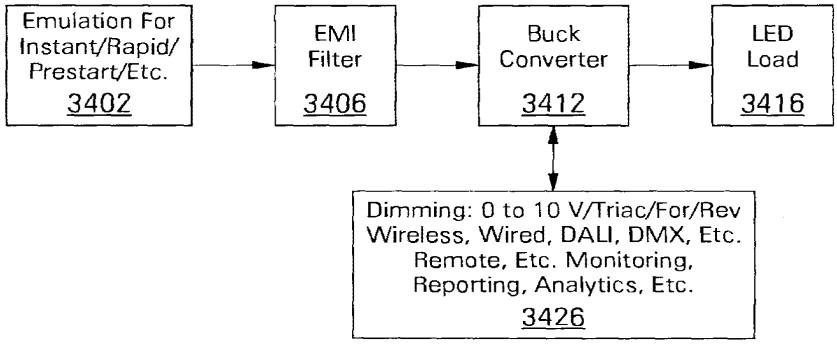


FIG. 36

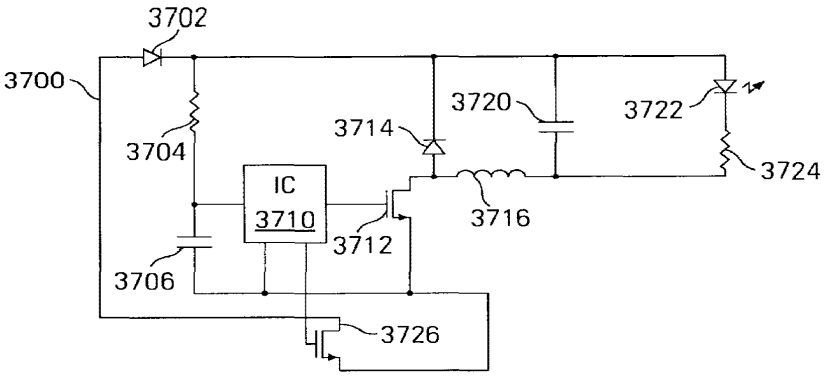

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FIG. 37

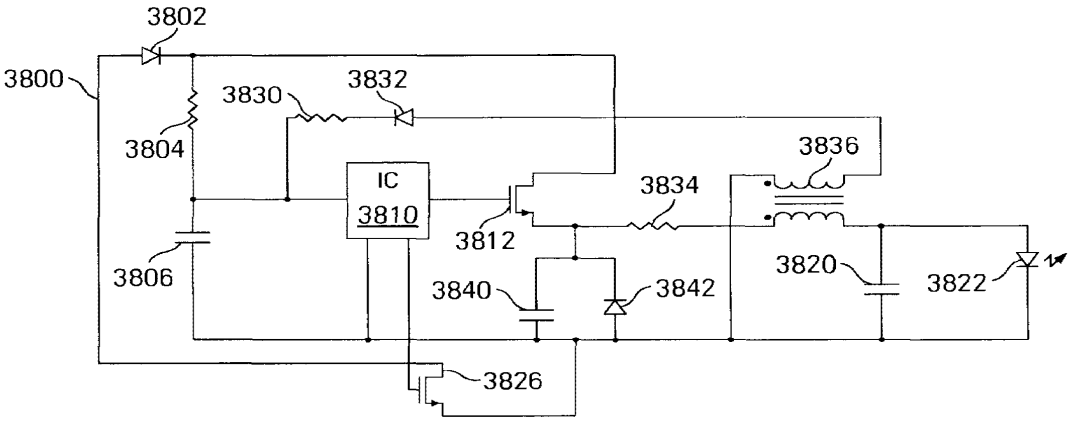

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FIG. 38

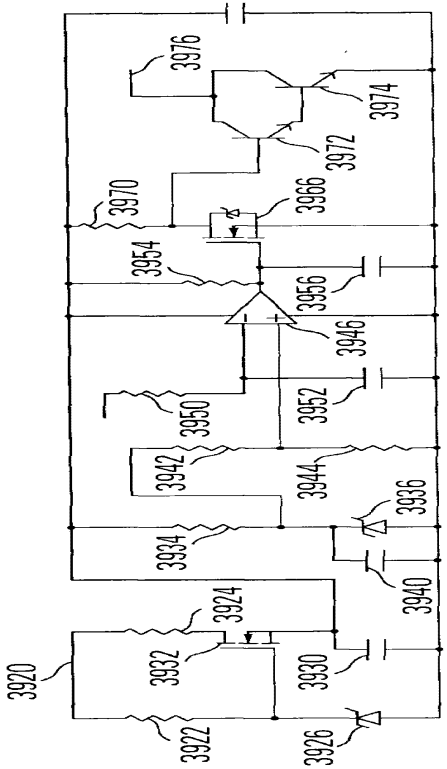

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FIG. 39

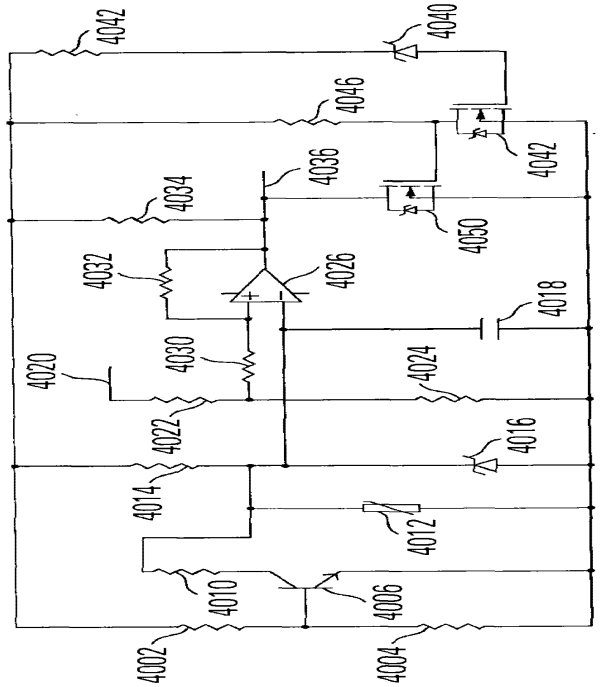

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FIG. 40

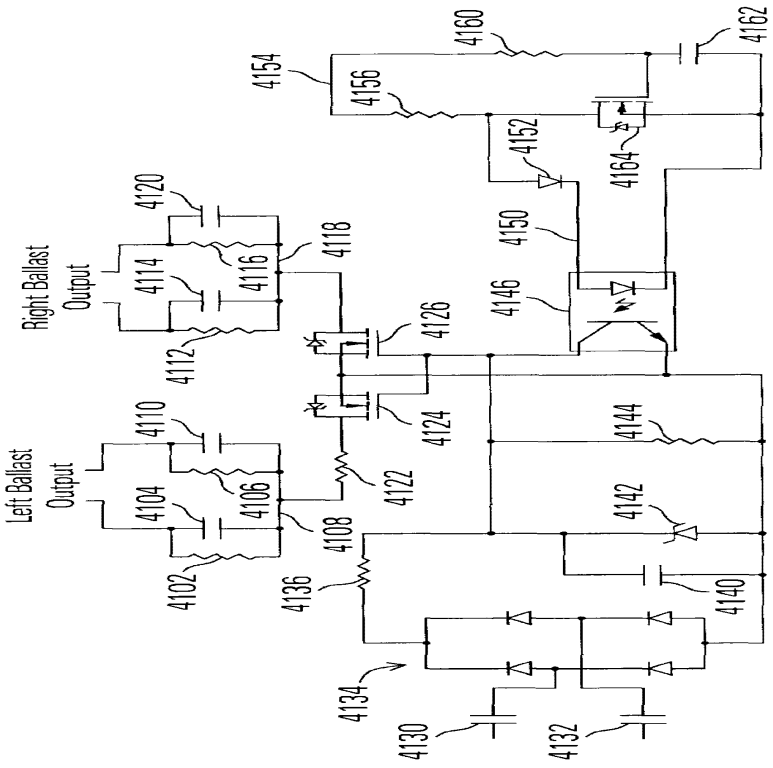

Left Ballast Output
Right Ballast Output
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FIG. 41

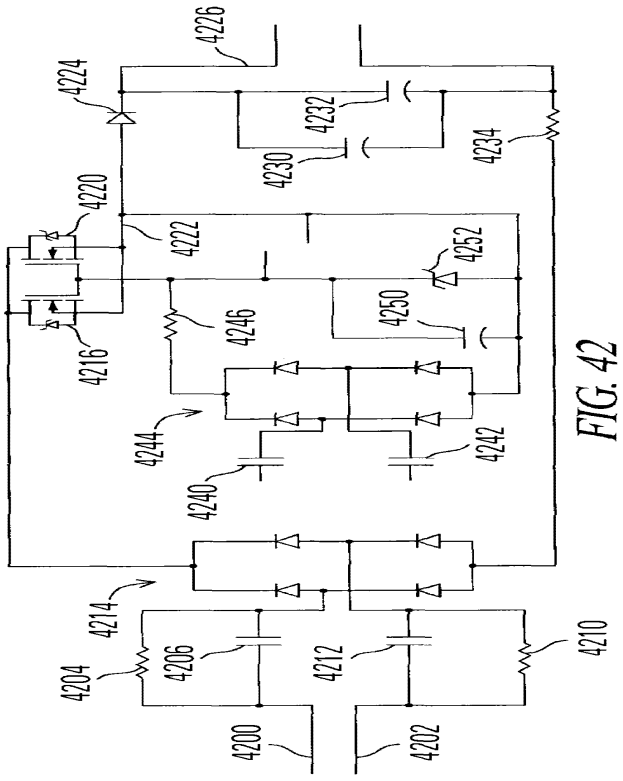

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FIG. 42

5/31/2017, EAST Version: 3.3.1.2

FIG. 43A

FIG. 43B

FIG. 43C

FIG. 43D

FIG. 43E

FIG. 44A

5/31/2017, EAST Version: 3.3.1.2

FIG. 44B

FIG. 44C

FIG. 44D

FIG. 45A

FIG. 45C

FIG. 45B

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	14	liu-xintong.in. and xiong-aiming.in. and jiang-tao.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:32
S2	3	S1 and (installation SAME ((power adj1 loop) or power-loop) SAME pulse).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:37
S3	3	S1 and (((power adj1 loop) or power-loop) SAME pulse).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:55
S4	3	S1 and (MIU.u/c. or (measurement adj1 indication adj1 unit))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:57
S5	2876	((LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)) SAME (tub$4 or retrofit$4 or replacement or straight or fluorescen$4)) AND (shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 14:15
S6	636	S5 and (315/$.ccls. or 362/$.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 14:16
S7	27	S6 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (pin or terminal or bipin or bi-pin) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 14:19
S8	20	("20100045187" | "20100156324" |	US-PGPUB;	OR	OFF	2017/05/31

		"20110068703" | "20110176297" | "20120032610" | "20120126703" | "20120139421" | "20120181952" | "6525914" | "7800316" | "7994725" | "8147091").PN. OR ("8749167").URPN.	USPAT; USOCR			15:02
S9	8	("20130076466" | "20130093309" | "8680958" | "8749167" | "8845127" | "8860312" | "8917020" | "9095023").PN. OR ("9622317").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:09
S10	12	("20070253137" | "20110187271" | "20120062114" | "20130147350" | "3365625" | "8147091" | "8322878" | "8339761" | "8459831" | "8749167").PN. OR ("9480123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:19
S11	9	("20070183156" | "20070223225" | "20090237007" | "20100002439" | "7441922" | "7611260" | "8314564").PN. OR ("8624509").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:35
S12	7	("20100020574" | "20110149563" | "20120299494" | "4211958" | "7852011" | "8314564" | "8624509").PN. OR ("9288879").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:40
S13	13	("20070133202" | "20070183156" | "20070223225" | "20090290334" | "20100002439" | "20110260614" | "20110260622" | "20120299494" | "7611260" | "8147091").PN. OR ("8622571").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:41
S14	46	S6 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 15:43
S15	11	("20100289419" | "20110149563" | "20110176297" | "20120043892" | "3685003" | "5412550" | "5752842" | "7530833" | "8147091" | "8459831").PN. OR ("8847475").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:51
S16	55	S5 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (pin or terminal or bipin or bi-pin) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 15:54
S17	148	S5 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:12
S18	771	S5 AND (F21V$/$.CPC. OR H05B$/$.CPC. OR F21K9/$.CPC. OR F21Y2103/10.CPC. OR F21Y2115/10)	US-PGPUB; USPAT	OR	ON	2017/05/31 16:39
S19	35	S18 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (pin or terminal or bipin	US-PGPUB; USPAT; USOCR;	OR	ON	2017/05/31 16:41

		or bi-pin) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S20	285	S18 AND ballast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:43
S21	55	S20 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:43
S22	15	S20 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (compar$4 or amplif$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:47
S23	90	S20 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:49
S24	81	("20020044456" | "20020176262" | "20030102819" | "20030231485" | "20040095078" | "20040189218" | "20050128751" | "20050162850" | "20050207166" | "20050213321" | "20060028837" | "20070001709" | "20070145915" | "20070210687" | "20070274084" | "20080030981" | "20080192476" | "20080278941" | "20090161359" | "20100102729" | "20100253226" | "20110038146" | "20110057572" | "20110090684" | "20110121756" | "20110148313" | "20110181190" | "20110216538" | "20110228526" | "20120069556" | "20120106157" | "20120153873" | "20120169968" | "20120181952" | "20120235578" | "20120293991" | "20120299501" | "20120313540" | "20120319150" | "20130033888" | "20130050998" | "20130170245" | "20130182425" | "20130200797" | "20130256704" | "20140071667" | "20140153231" | "20140226320" | "20140265900" | "20150009688" | "20150077001" | "20150173138" | "20150181661" | "20150351171" | "20160081147" | "20160091147" | "20160091156" | "20160091179" | "20160102813" | "20160178135" |	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 18:46

		"20160178137" | "20160178138" | "3294518" | "4647399" | "5575459" | "5921660" | "6118072" | "6127783" | "6211262" | "6609813" | "6796680" | "6936855" | "7033239" | "7067032" | "8360599" | "8525427" | "8579463" | "8648542" | "9210744" | "9480123").PN. OR ("9587817").URPN.				
S25	8	("20110205770" | "20110248637" | "20130026926" | "8508151" | "8537574").PN. OR ("8749140").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 19:09
S28	13	(("20110260622") or ("20110260614") or ("20120181952") or ("20160227622") or ("20160174326") or ("20130147350") or ("20070223225") or ("20150061520") or ("8897475") or ("20130127327") or ("20170142787") or ("20170079115") or ("20120313540")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/06/01 09:39
S30	114	sadwick-$.in.	US-PGPUB; USPAT	OR	OFF	2017/06/01 12:14
S31	3	(("9497821") or ("9587817") or ("9629211") or ("9587817")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/06/02 13:08

EAST Search History (Interference)

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7/ 13/ 2017 6:00:13 PM
C:\ Users\ atran1\ Documents\ EAST\ Workspaces\ 15426785.wsp

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	TRAN, ANH Q
Sheet	1	of	2	*Attorney Docket Number*	SUP-101C-3

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110121756	05-26-2011	Thomas et al.	
		US20110057572	03-10-2011	Kit et al.	
		US20150173138	06-18-2015	General Electric Company	
		US20120299501	11-29-2012	Kost et al.	
		US9210744	10-24-2013	Carmen et al.	
		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110176297	07-21-2011	Hsia et al.	
		US20100220469	09-02-2010	Ivey et al.	
		US20120300445	11-29-2012	Chu et al.	
		US20150176770	06-25-2015	Wilcox et al.	
		US20100181925	07-22-2010	Ivey et al.	
		US20140035463	02-06-2014	MIYAMICHI SABURO	
		US20110043127	02-24-2011	Yamasaki	
		US20140239834	08-28-2014	Choi et al	
		US9609711	03-28-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160198535	07-07-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US9629215	04-18-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US9629216	04-18-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160270165	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160270164	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160309550	10-20-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160381760	12-29-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US9,756,698	09-05-2017	JIAXING SUPER	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	TRAN, ANH Q
Sheet	2	of	2	Attorney Docket Number	SUP-101C-3

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

				LIGHTING ELECTRIC APPLIANCE CO.	
		US20170164434A1	06-08-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	
		US20170159923A1	06-08-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		CN104735873	06-24-2015	JINGSAM ILLUMINATION CO LTD		
		GB2533683	06-29-2016	Richo Co Ltd		
		EP2914065	09-02-2015	Richo Co Ltd		
		WO2012139691	10-18-2012	LEUCHTMITTELWERKE GMBH et al.		
		WO2014206785A1	12-31-2014	Philips (inventor: Haimin Tao)		
		WO2015074917	05-28-2015	Tao et al.		
		WO2015/066566 A1	05-07-2015	INNOSYS, INC.		
		WO2017012512A	01-26-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.,LTD		
		WO2016/187846A1	01-12-2016	Dialog Semiconductor		

NONPATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]

Examiner Signature		Date Considered	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	TRAN, ANH Q
Sheet	3	of	2	*Attorney Docket Number*	SUP-101C-3

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[3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3).
[4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.
[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

Electronic Patent Application Fee Transmittal

Application Number:	15339221
Filing Date:	31-Oct-2016
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Filer:	Bradley E. Edelman
Attorney Docket Number:	SUP-101C-3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	30537207
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	02-OCT-2017
Filing Date:	31-OCT-2016
Time Stamp:	14:25:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$180
RAM confirmation Number	100317INTEFSW14274200
Deposit Account	
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	SUP-101C-3_IDS_transmittal.pdf	69869 4b9008551d32f9a08f9082d886f8e457875c4dbb	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	SUP-101C-3_IDS_sb08.pdf	91030 69cb14477c3ce4f07d279e1296f704f6607279d6	no	4
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Foreign Reference	CN101715265A.pdf	649537 654c6e12bdb2a12f98673e9bc2f5aad71d8f1564	no	11
Warnings:					
Information:					
4	Foreign Reference	CN102155642A.pdf	1765901 e06c44a5c67cdb5343f4c9edd453e7718300f436	no	37
Warnings:					
Information:					
5	Foreign Reference	CN102355780A_.pdf	509541 383d4906995a4eb4ce80563fb562380a4cf69e9c	no	8
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6	Foreign Reference	CN102932997A__.pdf	1132594 9ba266e3eb502554722f3d20d4924ec4f63be58a	no	17
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Information:					
7	Foreign Reference	CN200965185Y.pdf	278728 0c7c30665a1bd4ef09c99449937e24642adcf93f	no	7
Warnings:					
Information:					
8	Foreign Reference	CN104735873A.pdf	861821 fa27d151a7e2368f2908fa8ea9afdeed2aebda64	no	13
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9	Foreign Reference	EP2914065A2.pdf	784474 bd3bcda616ea7566a16eec08daa3b00d272a909a	no	19
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10	Foreign Reference	GB2533683A.pdf	1670176 ea6edd85c67917130799cc523355cf260b3fadaa	no	60
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11	Foreign Reference	WO2012139691A1.pdf	827502 dd67c515be160cf24f2c9b050e2b4e7f268f3a58	no	20
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12	Foreign Reference	CN101715265_.pdf	713060 b760a3a8a26ac3bf873a2851eb8db8171bb08388	no	2
Warnings:					
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13	Foreign Reference	CN102155642_.pdf	580962 d6f83797918402f1bc07bf5d531c9c5430e229d9	no	2
Warnings:					
Information:					

14	Foreign Reference	CN102355780Aa.pdf	425719 d6d8679dfc7a21f9429a12fb4293589ac06a697b	no	2
Warnings:					
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15	Foreign Reference	CN102932997a_.pdf	475353 f97f8766f54b4d78a7cf571c74ba0623d2977533	no	2
Warnings:					
Information:					
16	Foreign Reference	CN200965185_.pdf	610737 0a045dd9e96cf1e773bad140c37ad668887e697c	no	2
Warnings:					
Information:					
17	Foreign Reference	EngAbst_CN104735873.pdf	245074 533b5577d6ef0d4935ca827d3e69e87d16b134ef	no	1
Warnings:					
Information:					
18	Foreign Reference	EngAbst-EP2914065.pdf	529553 7d78c550c16d07785f0c5f90d39c3bac2f96653e	no	2
Warnings:					
Information:					
19	Foreign Reference	EngAbst-GB2533683.pdf	531463 eb3a3a09b45d53d3c1c8fcc891874adb4288b74e	no	2
Warnings:					
Information:					
20	Foreign Reference	EngAbst-WO2012139691.pdf	521814 5483113679cc1f21721981c4065f3cbbd0181995	no	2
Warnings:					
Information:					

21	Fee Worksheet (SB06)	fee-info.pdf	30189 e42acb95f3aadb53504ec7f45053184e0098b0be	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	13305097	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	LIU, et al.	Attorney Docket:	SUP-101C-3
Serial Number:	15/339,221	Group Art Unit:	2844
Filed:	10-31-2016	Examiner:	TRAN, ANH Q

Confirmation Number: 3876

Title: **LED TUBE LAMP**

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.97(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

Pursuant to 37 C.F.R. 1.56 and 1.97(c), Applicant brings to the attention of the Examiner the listed documents on the attached SB/08 Form. This Information Disclosure Statement is being filed after a first office action but before a final office action or allowance in this application. A fee of $180 is being submitted herewith.

Applicant respectfully requests that the Examiner consider the listed documents and indicate that they were considered by making appropriate notations on the attached form.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art". If the Examiner applies any of the documents as prior art

against any claim in the application and Applicant determines that the cited documents do not constitute "prior art" under United States law, Applicant reserves the right to present to the U.S. Patent and Trademark Office the relevant facts and law regarding the appropriate status of such documents.

Applicant further reserves the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

In the event any fees are required in connection with this paper, please charge the Deposit Account No. 50-4574.

Respectfully submitted,

/Ali Imam/, Reg. No. 58,755

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Liu et al.

Serial Number: 15/339,221

Filed: October 31, 2016

Confirmation Number: 3876

Title: **LED TUBE LAMP**

Attorney Docket: SUP-101C-3

Group Art Unit: 2844

Examiner: Anh Q. TRAN

AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

This is a response to the Office Action of August 7, 2017. Amendments to the specification begin on page 2 and amendments to the claims begin on page 4 of this paper. Remarks follow the amendment sections of this paper.

It is respectfully requested that the amendment be entered, the outstanding rejection of the above-identified patent application be reconsidered.

Electronic Patent Application Fee Transmittal

Application Number:	15339221
Filing Date:	31-Oct-2016
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Filer:	Ali M. Imam
Attorney Docket Number:	SUP-101C-3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	3	80	240
INDEPENDENT CLAIMS IN EXCESS OF 3	1201	2	420	840
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1080**

Electronic Acknowledgement Receipt

EFS ID:	30872728
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Ali M. Imam
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	07-NOV-2017
Filing Date:	31-OCT-2016
Time Stamp:	10:29:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1080
RAM confirmation Number	110717INTEFSW10305300
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUP-101C-3_Response_to_OA.pdf	198818 e80e356107dfee9cbea5d57c1fe2cd8b6931b441	yes	22

Multipart Description/PDF files in .zip description

Document Description	Start	End
Applicant Arguments/Remarks Made in an Amendment	18	22
Claims	4	17
Specification	2	3
Amendment/Req. Reconsideration-After Non-Final Reject	1	1

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	31644 a98baf1784217e0de8bd2e9e6209aed3dc99f7f9	no	2

Warnings:

Information:

Total Files Size (in bytes):	230462

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

Status of the Claims

Claims 1, 2, 4-22, 24, 25, and 27-38 are now present in this application. Claims 1, 5, 18, 22, and 27 are independent.[1]

Claims 1, 4, 5, 18, 22, 24, and 25 have been amended, claims 3, 23, and 26 have been canceled, and claims 33-38 have been added via this amendment. The specification has also been amended to correct minor typographical errors. It is respectfully submitted that no new matter has been added to the application via this amendment. Reconsideration and allowance of this application, as amended, is respectfully requested.

Allowable Subject Matter

Applicant thanks the Examiner for allowing claims 27-32.

Applicant also thanks the Examiner for indicating that claims 2, 5-20, and 25-26 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. As set forth above, claims 5 and 18 have been rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claim 22 has been amended to incorporate the allowable subject matter of claims 23 and 26. Accordingly, Applicant respectfully submits that claims 5, 18, and 22 and any claim depending therefrom are allowable.

Prior Art Rejections Under 35 USC §§ 102, 103

Claims 1, 3-4, 22-24 were rejected under 35 U.S.C. 102(a)(2) as allegedly being anticipated by Sadwick, Laurence, P. (WO 2015/066566 A1; hereinafter "Sadwick") and claim 21 was rejected under 35 U.S.C. 103 as allegedly being unpatentable over Sadwick. These rejections are respectfully traversed.

[1] Unless expressly stated herein, Applicant declines to necessarily subscribe to any of the Examiner's characterizations of Applicant's specification, the claims, or the prior art made in the Office Action.

While not conceding the appropriateness of the Examiner's rejection, as mentioned above, claim 22 has been amended to recite the allowable subject matter of claims 23 and 26, rendering the rejection of claims 22 and 24 moot.

In addition, while not conceding the appropriateness of the Examiner's rejection, as set forth above, claim 1 has been amended to recite the subject matter of previously presented claim 3 and further amended to recite that "***wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal***." (Emphasis added.) More specifically, claim 1 now recites, *inter alia*, "wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises ***a detection determining circuit*** configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and ***wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal***." (Emphasis added.)

It is respectfully submitted that Sadwick fails to teach or suggest the above-noted amended feature of claim 1 for the following reasons.

In the Office Action, the Examiner relies on elements 2124, 2126, 2128, 2130, 2132, and 2134 (rather than the typo 3134 in the Office Action) as illustrated in Fig. 21 of Sadwick as disclosing the claimed "pulse generating circuit." The Examiner also alleges that the output of element 2134 corresponds to the output of the claimed pulse generating circuit. The Examiner relies on element 2022 in Fig. 20 of Sadwick (or element 1430 in Fig. 14 of Sadwick) as disclosing the claimed "switch circuit," relies on element Op amp (or comparator) 2110 in Fig. 21 of Sadwick as disclosing the claimed "detection determining circuit" and alleges that a signal at node 2112 in Fig. 21 (connected to a node between 1446 and 1444 in Fig. 14 of Sadwick) corresponds to the "sampling signal" as now recited in claim 1. Applicant respectfully disagrees with the Examiner's alleged mapping of claim elements.

As taught by Sadwick, element 2134 is an optocoupler which is connected across the gate and source of transistor 2022 to short out the gate to source voltage when, for example, a fault condition is detected. (See, e.g., paragraph [94] of Sadwick.) Applicant respectfully

submits that the output of this optocoupler 2134 does not correspond to the output of the claimed pulse generating circuit. According to at least the cited Figs. 20-21 and corresponding paragraphs [96-97] of Sadwick, the alleged pulse as output at 2134 is generated ***after*** Op amp (or comparator) 2110 in Fig. 21 determines whether the current of Fig. 20 is low by comparing a voltage reference against "the voltage across resistor 2062 which, for example, senses and measures the current of Fig. 20 via optional filter consisting of resistor 2114 and capacitor 2116." If the current of Fig. 20 is low, Op amp (or comparator) 2110 in Fig. 21 will turn off "transistor 2124 which allows the input current to optocoupler 2134 to flow via resistor 2126 thus allowing optocoupler 2134 to short out the gate to source of transistor 2022 in Fig. 20." Thus, it is evident that generation of the alleged pulse as output at 2134 is ***dependent on whether the*** Op amp (or comparator) 2110 in Fig. 21 (the alleged detection determining circuit) determines whether the current of Fig. 20 is low. Accordingly, it is evident that Sadwick fails to teach or suggest, *inter alia*, "***wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal***." (Emphasis added.)

In addition, according to other embodiments illustrated in Figs. 14-15 and their corresponding description in Sadwick, whether transistor 1430 is turned on or off is controlled by the signal at 1523 of the circuit 1500 (alleged pulse generating circuit) when the comparator 1434 (the alleged detection determining circuit) which measures the signal at the common node connecting 1430, 1446, and 1450, is not present, since paragraph [83] of Sadwick states "[n]ote, in this embodiment, the comparator 1434 and associated components in the right side of Fig. 14 are replaced with the timer circuit 1506 and associated resistors and capacitor of the left side of Fig. 15." Furthermore, even when the comparator 1434 (the alleged detection determining circuit) which measures the signal at the common node connecting 1430, 1446, and 1450, is present instead of the circuit 1500 (alleged pulse generating circuit), this implies in Sadwick that generation of the pulse at the gate of transistor 1430 ***is dependent on detection performed by*** the comparator 1434 (the alleged detection determining circuit) which measures the signal at the common node connecting 1430, 1446, and 1450.

Contrary to Sadwick, as illustrated in the exemplary, non-limiting embodiments illustrated by at least Figs. 15B and 15G of the present disclosure, generation of the pulse by 2540/2740 is independent of the detection determining circuit 2570/2770, and whether the

switch circuit in present claim 1 is turned on or off is controlled in the presence of both the pulse generating circuit (e.g., detection pulse generating module 2540/2740) and the detection determining circuit (e.g., 2570/2770).

At least based on the above, it is respectfully submitted that Sadwick fails to teach or suggest, *inter alia*, "wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises ***a detection determining circuit*** configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and ***wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal***" as now recited in claim 1. (Emphasis added.)

Accordingly, reconsideration and withdrawal of the rejection of claims 1, 4, and 21 based on Sadwick are respectfully requested.

New Claims

New claims 33-38 are allowable at least by virtue of their dependency from claim 1, directly or indirectly, and further in view of novel features recited therein.

Conclusion

All of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding rejections and that they be withdrawn. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Ali Imam, Registration No. 58755, at the telephone number of the undersigned below to conduct an interview in an effort to expedite prosecution in connection with the present application.

In the event any additional fees are required in connection with this paper, or in the

event of an overpayment, please charge or credit the Deposit Account No. 50-4574.

Respectfully submitted,

/Ali Imam/

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Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

What is claimed is:

1. (Currently Amended) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,

wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and

wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal.

2. (Original) The installation detection circuit according to claim 1, wherein the pulse generating circuit comprises:

a first capacitor, one end connected to a driving signal;

a first resistor, one end connected to the other end of the first capacitor, the other end the first resistor connected to a reference voltage;

a first buffer, having an input end and an output end, the input end connected to the other end of the first capacitor;

a second capacitor, one end connected to the output end of the first buffer;

a third capacitor, one end connected to the output end of the first buffer;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

3. (Canceled)

4. (Currently Amended) The installation detection circuit according to ~~claim 3~~claim 1, wherein when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

5. (Currently Amended) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state, and

wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and

the detection determining circuit; and

~~The~~ wherein the installation detection circuit ~~according to claim 3,~~ further ~~comprising~~ includes a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

6. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.

7. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a second capacitor, one end coupled to a driving signal;

a third capacitor, one end coupled to the driving signal;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end

connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

8. (Original) The installation detection circuit according to claim 7, wherein the second buffer comprises two inverters connected in series.

9. (Original) The installation detection circuit according to claim 7, wherein the detection result latching circuit comprises:

a first D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit;

a fourth resistor, one end connected to the output end of the first D flip-flop, the other end of the fourth resistor connected to a reference voltage; and

a second OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first OR gate, the second input end connected to the output end of the first D flip-flop, the output end of the second OR gate connected to the switch circuit.

10. (Original) The installation detection circuit according to claim 7, wherein the switch circuit comprises:

a first transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

11. (Previously Presented) The installation detection circuit according to claim 7, wherein the detection determining circuit comprises:

a fifth resistor, one end connected to the switch circuit, the other end of the fifth resistor connected to a second end of the power loop; and

a first comparator, having a first input end, a second input end, and an output end, the first input end connected to a predefined signal, the second input end connected to the one end of the fifth resistor, the output end of the first comparator connected to the detection result latching circuit.

12. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a sixth resistor, one end connected to a driving signal;

a fourth capacitor, one end connected to the other end of the sixth resistor, the other end of the fourth capacitor connected to a reference voltage;

a Schmitt trigger, having an input end and an output end, the input end connected to the one end of the fourth capacitor, the output end connected to the detection result latching circuit;

a seventh resistor, one end connected to the one end of the fourth capacitor;

a second transistor, having a base, a collector, and an emitter, the collector connected to the other end of the seventh resistor, the emitter connected to a reference voltage; and

an eighth resistor, one end connected to the base of the second transistor, the other end of the eighth resistor connected to the detection result latching circuit and the switch circuit.

13. (Original) The installation detection circuit according to claim 12, wherein the pulse generating circuit further comprises:

a Zener diode, having an anode and a cathode, the anode connected to the other end of the fourth capacitor, the cathode connected to the one end of the fourth capacitor.

14. (Original) The installation detection circuit according to claim 12, wherein the detection result latching circuit comprises:

a second D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit; and

a third OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the Schmitt trigger, the second input end connected to the output end of the second D flip-flop, the output end of the third OR gate connected to the other end of the eighth resistor and the switch circuit.

15. (Original) The installation detection circuit according to claim 12, wherein the switch circuit comprises:

a third transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

16. (Previously Presented) The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop; and

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to a predefined signal, the second input end connected to the one end of the ninth resistor, the output end of the second comparator connected to the detection result latching circuit.

17. (Previously Presented) The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop;

a second diode, having an anode and a cathode, the anode connected to the one end

of the ninth resistor;

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to a predefined signal, the second input end connected to the cathode of the second diode, the output end of the second comparator connected to the detection result latching circuit;

a third comparator, having a first input end, a second input end, and an output end, the first input end connected to the cathode of the second diode, the second input end connected to another predefined signal, the output end of the third comparator connected to the detection result latching circuit;

a tenth resistor, one end connected to the driving signal;

an eleventh resistor, one end connected to the other end of the tenth resistor and the second input end of the second comparator, the other end of the eleventh resistor connected to a reference voltage; and

a fifth capacitor, connected to the eleventh resistor in parallel.

18. (Currently Amended) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state, and

~~The installation detection circuit according to claim 1,~~ wherein the LED tube lamp comprises a lamp tube and a circuit board, and comprises an inductive element connected between two terminals respectively at two ends of the lamp tube for grounding or connecting to a reference potential, wherein one of the two terminals is connected to the circuit board.

19. (Original) The installation detection circuit according to claim 18, wherein the inductive element is an inductor.

20. (Original) The installation detection circuit according to claim 19, wherein one end of the inductor is directly electrically connected to the circuit board.

21. (Original) The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

22. (Currently Amended) An installation detection circuit configured in a light-emitting diode (LED) tube lamp, the installation detection circuit comprising:

means for generating one or more pulse signals;

means for detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket; and

a switch circuit coupled to the means for generating one or more pulse signals, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube

lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,

wherein the means for detecting is configured to detect a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the means for detecting, and

wherein the LED tube lamp is configured to receive an external driving signal and comprises a rectifying circuit for rectifying the external driving signal and a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit.

23. (Canceled)

24. (Currently Amended) The installation detection circuit according to ~~claim 23~~claim 22, wherein when the means for detecting determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the means for detecting determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

25. (Currently Amended) The installation detection circuit according to ~~claim 23~~claim 22, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the means for detecting.

26. (Canceled)

27. (Original) A detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket, the detection method comprising:

when at least one end of the LED tube lamp is installed on the lamp socket, generating one or more pulse signals by a pulse generating circuit, wherein the pulse generating circuit is configured in the LED tube lamp;

detecting a sampling signal on a power loop of the LED tube lamp by a detection determining circuit, to detect during the one or more pulse signals whether the other end of the LED tube lamp is properly installed on the lamp socket;

receiving the one or more pulse signals through a detection result latching circuit by a switch circuit, wherein the switch circuit is on the power loop; and

comparing the sampling signal with a predefined signal, wherein during the one or more pulse signals when the sampling signal is smaller than the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open.

28. (Original) The detection method according to claim 27, wherein the step of controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open comprises:

outputting a first low level signal by the detection determining circuit;

receiving the first low level signal by the detection result latching circuit and

outputting a second low level signal; and

receiving the second low level signal by the switch circuit and maintaining an off

state of the switch circuit to cause the power loop to be open.

29. (Original) The detection method according to claim 27, wherein during any of the one or more pulse signals when the sampling signal is greater than or equal to the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

30. (Original) The detection method according to claim 29, wherein the step of controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state comprises:

outputting a first high level signal by the detection determining circuit;

receiving the first high level signal by the detection result latching circuit and outputting a second high level signal; and

receiving the second high level signal by the switch circuit and conducting the switch circuit to cause the power loop to maintain a conducting state.

31. (Original) The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 10 microseconds and 1 millisecond.

32. (Original) The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 1 microsecond and 100 microseconds.

33. (New) The installation detection circuit according to claim 1, configured such that when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining circuit determines that

the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

34. (New) The installation detection circuit according to claim 1, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

35. (New) The installation detection circuit according to claim 34, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.

36. (New) The installation detection circuit according to claim 34, wherein the pulse generating circuit comprises:

a second capacitor, one end coupled to a driving signal;

a third capacitor, one end coupled to the driving signal;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

37. (New) The installation detection circuit according to claim 34, wherein the pulse generating circuit comprises:

a sixth resistor, one end connected to a driving signal;

a fourth capacitor, one end connected to the other end of the sixth resistor, the other end of the fourth capacitor connected to a reference voltage;

a Schmitt trigger, having an input end and an output end, the input end connected to the one end of the fourth capacitor, the output end connected to the detection result latching circuit;

a seventh resistor, one end connected to the one end of the fourth capacitor;

a second transistor, having a base, a collector, and an emitter, the collector connected to the other end of the seventh resistor, the emitter connected to a reference voltage; and

an eighth resistor, one end connected to the base of the second transistor, the other end of the eighth resistor connected to the detection result latching circuit and the switch circuit.

38. (New) The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

Amendments to the Specification:

Please amend paragraph [00101] bridging pages 30-31 of the originally filed specification as follows:

[00101] In addition, the power supply module of the LED lamp described in Fig. 8C, and embodiments of a power supply module of an LED lamp described below, may each be used in the LED tube lamp 500 in Figs. 8A and 8B, and may instead be used in any other type of LED lighting structure having two conductive pins used to conduct power, such as LED light bulbs, personal area lights (PAL), plug-in LED lamps with different types of bases (such as types of PL-S, PL-D, PL-T, PL-L, etc.), etc. Further, the implementation for LED light bulbs may provide better effects on protecting from electric shock as combining this invention and the structures disclosed in PCT~~EU~~ patent application WO2016045631.

Please amend paragraph [00113] bridging pages 34-35 of the originally filed specification as follows:

[00113] FIG. 11B is a schematic diagram of an LED module according to an exemplary embodiment. Referring to FIG. 11B, an LED module 630 has an anode connected to a filtering output terminal 521, a cathode connected to a filtering output terminal 522, and includes at least two LED units 732 with the anode of each LED unit 732 connected to the anode of LED module 630 and the cathode of each LED unit 732 connected to the cathode of LED module 630. Each LED unit 732 includes at least two LEDs 731 connected in the same way as those described in FIG. 11A. For example, the anode of the first LED 731 in an LED unit 732 is connected to the anode of this LED unit 732, the cathode of the first LED 731 is connected to the anode of the next or second LED 731, and the cathode of the last LED 731 is connected to the cathode of this LED unit 732. Further, LED units 732 in an LED module 630 are connected to each other in this embodiment. All of the n-th LEDs 731 in the related LED units 732 thereof are connected by their anodes and cathodes, such as those shown in FIG. 11B~~8B~~ but not limit to, where n is a positive integer. In this way, the LEDs in the LED module 630 of this embodiment

are connected in the form of a mesh.

Please amend paragraph [00188] in page 61 of the originally filed specification as follows:

[00188] In some embodiments, the fourth circuit 2570 is configured for detecting a signal between the first installation detection terminal 2521 and the second installation detection terminal 2522 through the first terminal 2581 and the third~~fourth~~ circuit 2580. For example, because of the above configuration, the fourth circuit 2570 is capable of detecting and determining whether a current passing through the first installation detection terminal 2521 and the second installation detection terminal 2522 is below or above a predetermined current value and transmitting or providing a detection result signal to the second circuit 2560 via the second terminal 2571.

PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/339,221	Filing Date 10/31/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **11/07/2017**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 35	Minus	** 32	= 3	X $80 =	240
Independent (37 CFR 1.16(h))	* 5	Minus	***3	= 2	X $420 =	840
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**1080**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
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*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/339,221	Filing Date 10/31/2016	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	11/07/2017	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 35	Minus	** 32	= 3	X $80 =	240
	Independent (37 CFR 1.16(h))	* 5	Minus	***3	= 2	X $420 =	840
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	**1080**

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

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NOTICE OF ALLOWANCE AND FEE(S) DUE

74712 7590 12/11/2017

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P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

EXAMINER
TRAN, ANH Q

ART UNIT	PAPER NUMBER
2844	

DATE MAILED: 12/11/2017

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

TITLE OF INVENTION: LED TUBE LAMP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	03/12/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

TITLE OF INVENTION: LED TUBE LAMP

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	03/12/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
TRAN, ANH Q	2844	315-127000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
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- ❑ Publication Fee (No small entity discount permitted)
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- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

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- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
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- ❑ Applicant asserting small entity status. See 37 CFR 1.27
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- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

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Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

74712 7590 12/11/2017

Muir Patent Law, PLLC
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9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2844	

DATE MAILED: 12/11/2017

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/339,221	Applicant(s) LIU ET AL.	
	Examiner ANH TRAN	Art Unit 2844	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/07/17*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-2, 4-22, 24-25, 27-38*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☒ All b) ☐ Some *c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION

Allowable Subject Matter

2. Claims 1-2, 4-22, 24-25, 27-38 are allowed.

3. The following is an examiner's statement of reasons for allowance: with respect to claims 1, 5, 18, 22, and 27, in addition to other limitations in the claims, the prior art fails to teach, disclose or render obvious the applicant's invention as claimed, particularly the feature describing:

Claim 1, wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal.

Claim 5, wherein the installation detection circuit, further includes a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

Claim 18, wherein the LED tube lamp comprises a lamp tube and a circuit board, and comprises an inductive element connected between two terminals respectively at two ends of the lamp tube for grounding or connecting to a reference potential, wherein one of the two terminals is connected to the circuit board.

Claim 22, wherein the means for detecting is configured to detect a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the means for detecting, and wherein the LED tube lamp is configured to receive an external driving signal and comprises a rectifying circuit for rectifying the external driving signal and a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit.

Claim 27, see previous office action.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ANH TRAN whose telephone number is (571)272-1813. The examiner can normally be reached on M-Th (8:00-6:30).

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an

interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alexander Taningco can be reached on 571-272-2048. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ANH TRAN/
Primary Examiner, Art Unit 2844

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

CPC- SEARCHED		
Symbol	Date	Examiner
H05B$/$, F21V$/$, F21K9/$, F21Y$/$ text search- see printout	12/02/16 & 7/29/16	AT
H05B$/$, F21V$/$, F21K9/$, F21Y$/$ text search- see printout	6/1/17	AT

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
315 & 362	all- text search- see printout	12/02/16 & 7/29/16	AT
315 & 362	all- text search- see printout	6/1/17	AT

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
east search- see printout	12/02/16 & 7/29/16	AT
east search- see printout	6/1/17	AT
update- east search- see printout	11/21/17	AT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
all	all- text search- see printout	11/21/17	AT

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 3876

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/339,221	10/31/2016	315	2844	SUP-101C-3
	RULE			

APPLICANTS

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD, Jiaxing, CHINA;

INVENTORS

Xintong Liu, Jiaxing, CHINA;
Aiming Xiong, Jiaxing, CHINA;
Tao Jiang, Jiaxing, CHINA;
Feng Zou, Jiaxing, CHINA;

**** CONTINUING DATA ***************************

This application is a CIP of 15/210,989 07/15/2016 PAT 9587817
which is a CIP of 15/066,645 03/10/2016 PAT 9497821
which is a CIP of 14/865,387 09/25/2015 PAT 9609711
and said 15/210,989 07/15/2016 /AT/
is a CIP of 15/205,011 07/08/2016 PAT 9629211
which is a CIP of 15/150,458 05/10/2016 PAT 9794990
which is a CIP of 14/865,387 09/25/2015 PAT 9609711
and is a CIP of 14/699,138 04/29/2015 PAT 9480109

**** FOREIGN APPLICATIONS ***************************

CHINA 201410507660.9 09/28/2014
CHINA 201410508899.8 09/28/2014
CHINA 201410623355.6 11/06/2014
CHINA 201410734425.5 12/05/2014
CHINA 201510075925.7 02/12/2015
CHINA 201510104823.3 03/10/2015 /AT/
CHINA 201510134586.5 03/26/2015
CHINA 201510133689.X 03/25/2015
CHINA 201510136796.8 03/27/2015
CHINA 201510173861.4 04/14/2015
CHINA 201510155807.7 04/03/2015
CHINA 201510193980.6 04/22/2015
CHINA 201510372375.5 06/26/2015
CHINA 201510259151.3 05/19/2015
CHINA 201510268927.8 05/22/2015
CHINA 201510284720.X 05/29/2015
CHINA 201510338027.6 06/17/2015
CHINA 201510315636.X 06/10/2015
CHINA 201510373492.3 06/26/2015
CHINA 201510364735.7 06/26/2015
CHINA 201510378322.4 06/29/2015
CHINA 201510391910.1 07/02/2015
CHINA 201510406595.5 07/10/2015
CHINA 201510482944.1 08/07/2015
CHINA 201510486115.0 08/08/2015
CHINA 201510428680.1 07/20/2015

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	**Art Unit**
	ANH TRAN	2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/28/2017	07/13/2017	11/21/2017						
1	1	✓	✓	=						
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	3	✓	✓							
3	4	✓	✓	=						
4	5	✓	O	=						
5	6	✓	O	=						
6	7	✓	O	=						
7	8	O	O	=						
8	9	✓	O	=						
9	10	✓	O	=						
10	11	✓	O	=						
11	12	O	O	=						
12	13	O	O	=						
13	14	O	O	=						
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17	18	O	O	=						
18	19	O	O	=						
19	20	O	O	=						
20	21	✓	✓	=						
21	22	✓	✓	=						
	23	✓	✓							
22	24	✓	✓	=						
23	25	✓	O	=						
	26	✓	O							
24	27	✓	=	=						
25	28	✓	=	=						
26	29	✓	=	=						
27	30	✓	=	=						
28	31	✓	=	=						
29	32	✓	=	=						
30	33			=						
31	34			=						
32	35			=						
33	36			=						

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	03/28/2017	07/13/2017	11/21/2017						
34	37			=						
35	38			=						

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	**Art Unit**
	ANH TRAN	2844

CPC								
Symbol							**Type**	**Version**
F21V		25	/	02			F	2013-01-01
H05B		33	/	0857			I	2013-01-01
H05B		33	/	0884			I	2013-01-01
H05B		33	/	0815			I	2013-01-01
F21K		9	/	278			I	2016-08-01
F21V		23	/	005			I	2013-01-01
F21V		3	/	0418			A	2013-01-01
F21K		9	/	272			I	2016-08-01
F21Y		2115	/	10			A	2016-08-01
F21Y		2103	/	10			A	2016-08-01
F21V		23	/	02			A	2013-01-01
H05B		33	/	0803			I	2013-01-01
F21V		29	/	83			A	2015-01-15
H05B		33	/	0887			I	2013-01-01
Y02B		20	/	346			A	2013-01-01

CPC Combination Sets									
Symbol							**Type**	**Set**	**Ranking**	**Version**
			/							
			/							

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	35	
/ANH TRAN/ Primary Examiner.Art Unit 2844	11/21/17	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	15B & 15C

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	**Art Unit**
	ANH TRAN	2844

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
315	127	H 0 5 B 37 / 00 (2006.01.01)	
		H 0 5 B 41 / 00 (2006.01.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
315	119	121	128	201	

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	35	
/ANH TRAN/ Primary Examiner.Art Unit 2844	11/21/17	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	15B & 15C

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15339221	LIU ET AL.
	Examiner	**Art Unit**
	ANH TRAN	2844

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	16	17	30	33										
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	3	18	19	32	35										
3	4	19	20	33	36										
4	5	20	21	34	37										
5	6	21	22	35	38										
6	7		23												
7	8	22	24												
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9	10		26												
10	11	24	27												
11	12	25	28												
12	13	26	29												
13	14	27	30												
14	15	28	31												
15	16	29	32												

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 35	
/ANH TRAN/ Primary Examiner.Art Unit 2844 (Primary Examiner)	11/21/17 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 15B & 15C

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	52	((LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)) SAME (tub$4 or retrofit$4 or replacement or straight or fluorescen$4)) AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (puls$3 NEAR3 (circuit or generat$3 or unit or regulat$3)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/21 11:29
L2	7143	((LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)) SAME (tub$4 or retrofit$4 or replacement or straight or fluorescen$4)) AND ((shock$2 or install$5) NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/21 11:39
L3	68	L2 AND ((pin or terminal or bipin or bi-pin or socket) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (puls$3 NEAR2 (generat$4 or regulat$3 or circuit or unit or module)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/21 11:45
S1	14	liu-xintong.in. and xiong-aiming.in. and jiang-tao.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:32
S2	3	S1 and (installation SAME ((power adj1 loop) or power-loop) SAME pulse).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:37
S3	3	S1 and (((power adj1 loop) or power-loop) SAME pulse).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:55
S4	3	S1 and (MIU.u/c. or (measurement adj1 indication adj1 unit))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 11:57
S5	2876	((LED.u/c. or (light adj emitting adj diode)	US-PGPUB;	OR	ON	2017/05/31

		or (light-emitting adj diode)) SAME (tub$4 or retrofit$4 or replacement or straight or fluorescen$4)) AND (shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:15
S6	636	S5 and (315/$.ccls. or 362/$.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 14:16
S7	27	S6 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (pin or terminal or bipin or bi-pin) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 14:19
S8	20	("20100045187" | "20100156324" | "20110068703" | "20110176297" | "20120032610" | "20120126703" | "20120139421" | "20120181952" | "6525914" | "7800316" | "7994725" | "8147091").PN. OR ("8749167").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:02
S9	8	("20130076466" | "20130093309" | "8680958" | "8749167" | "8845127" | "8860312" | "8917020" | "9095023").PN. OR ("9622317").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:09
S10	12	("20070253137" | "20110187271" | "20120062114" | "20130147350" | "3365625" | "8147091" | "8322878" | "8339761" | "8459831" | "8749167").PN. OR ("9480123").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:19
S11	9	("20070183156" | "20070223225" | "20090237007" | "20100002439" | "7441922" | "7611260" | "8314564").PN. OR ("8624509").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:35
S12	7	("20100020574" | "20110149563" | "20120299494" | "4211958" | "7852011" | "8314564" | "8624509").PN. OR ("9288879").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:40
S13	13	("20070133202" | "20070183156" | "20070223225" | "20090290334" | "20100002439" | "20110260614" | "20110260622" | "20120299494" | "7611260" | "8147091").PN. OR ("8622571").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:41
S14	46	S6 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 15:43
S15	11	("20100289419" | "20110149563" | "20110176297" | "20120043892" | "3685003" | "5412550" | "5752842" | "7530833" | "8147091" | "8459831").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 15:51

		OR ("8847475").URPN.				
S16	55	S5 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (pin or terminal or bipin or bi-pin) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 15:54
S17	148	S5 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:12
S18	771	S5 AND (F21V$/$.CPC. OR H05B$/$.CPC. OR F21K9/$.CPC. OR F21Y2103/10.CPC. OR F21Y2115/10)	US-PGPUB; USPAT	OR	ON	2017/05/31 16:39
S19	35	S18 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (pin or terminal or bipin or bi-pin) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:41
S20	285	S18 AND ballast	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:43
S21	55	S20 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (switch$2 or transistor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:43
S22	15	S20 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3) SAME (compar$4 or amplif$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:47
S23	90	S20 AND ((shock$2 NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (detect$4 or sens$3 or monitor$3 or measur$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/05/31 16:49
S24	81	("20020044456" | "20020176262" | "20030102819" | "20030231485" | "20040095078" | "20040189218" | "20050128751" | "20050162850" | "20050207166" | "20050213321" | "20060028837" | "20070001709" | "20070145915" | "20070210687" | "20070274084" | "20080030981" |	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 18:46

		"20080192476" | "20080278941" | "20090161359" | "20100102729" | "20100253226" | "20110038146" | "20110057572" | "20110090684" | "20110121756" | "20110148313" | "20110181190" | "20110216538" | "20110228526" | "20120069556" | "20120106157" | "20120153873" | "20120169968" | "20120181952" | "20120235578" | "20120293991" | "20120299501" | "20120313540" | "20120319150" | "20130033888" | "20130050998" | "20130170245" | "20130182425" | "20130200797" | "20130256704" | "20140071667" | "20140153231" | "20140226320" | "20140265900" | "20150009688" | "20150077001" | "20150173138" | "20150181661" | "20150351171" | "20160081147" | "20160091147" | "20160091156" | "20160091179" | "20160102813" | "20160178135" | "20160178137" | "20160178138" | "3294518" | "4647399" | "5575459" | "5921660" | "6118072" | "6127783" | "6211262" | "6609813" | "6796680" | "6936855" | "7033239" | "7067032" | "8360599" | "8525427" | "8579463" | "8648542" | "9210744" | "9480123").PN. OR ("9587817").URPN.				
S25	8	("20110205770" | "20110248637" | "20130026926" | "8508151" | "8537574").PN. OR ("8749140").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/05/31 19:09
S28	13	(("20110260622") or ("20110260614") or ("20120181952") or ("20160227622") or ("20160174326") or ("20130147350") or ("20070223225") or ("20150061520") or ("8897475") or ("20130127327") or ("20170142787") or ("20170079115") or ("20120313540")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/06/01 09:39
S30	114	sadwick-$.in.	US-PGPUB; USPAT	OR	OFF	2017/06/01 12:14
S31	3	(("9497821") or ("9587817") or ("9629211") or ("9587817")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/06/02 13:08

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	43	((LED.u/c. or (light adj emitting adj diode) or (light-emitting adj diode)) SAME (tub$4 or retrofit$4 or replacement or straight or fluorescen$4)) AND (((shock$2 or install$5) NEAR3 (limit$3 or protect$3 or safety or electric$4 or hazard$3)) SAME (puls$3 NEAR3 (circuit or generat$3 or unit or regulat$3)) SAME (detect$3 or monitor$3 or sens$3 or measur$3))	US-PGPUB; USPAT	OR	ON	2017/11/21 12:14

11/21/2017 12:17:49 PM
C:\Users\atran1\Documents\EAST\Workspaces\15426785.wsp

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	TRAN, ANH Q
Sheet	1	of	2	Attorney Docket Number	SUP-101C-3

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110121756	05-26-2011	Thomas et al.	
		US20110057572	03-10-2011	Kit et al.	
		US20150173138	06-18-2015	General Electric Company	
		US20120299501	11-29-2012	Kost et al.	
		US9210744	10-24-2013	Carmen et al.	
		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110176297	07-21-2011	Hsia et al.	
		US20100220469	09-02-2010	Ivey et al.	
		US20120300445	11-29-2012	Chu et al.	
		US20150176770	06-25-2015	Wilcox et al.	
		US20100181925	07-22-2010	Ivey et al.	
		US20140035463	02-06-2014	MIYAMICHI SABURO	
		US20110043127	02-24-2011	Yamasaki	
		US20140239834	08-28-2014	Choi et al	
		US9609711	03-28-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160198535	07-07-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US9629215	04-18-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US9629216	04-18-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160270165	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160270164	09-15-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160309550	10-20-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US20160381760	12-29-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.	
		US9,756,698	09-05-2017	JIAXING SUPER	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	TRAN, ANH Q
Sheet	2	of	2	Attorney Docket Number	SUP-101C-3

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

				LIGHTING ELECTRIC APPLIANCE CO.	
		US20170164434A1	06-08-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	
		US20170159923A1	06-08-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD	

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		CN104735873	06-24-2015	JINGSAM ILLUMINATION CO LTD		
		GB2533683	06-29-2016	Richo Co Ltd		
		EP2914065	09-02-2015	Richo Co Ltd		
		WO2012139691	10-18-2012	LEUCHTMITTELWERKE GMBH et al.		
		WO2014206785A1	12-31-2014	Philips (inventor: Haimin Tao)		
		WO2015074917	05-28-2015	Tao et al.		
		WO2015/066566 A1	05-07-2015	INNOSYS, INC.		
		WO2017012512A	01-26-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.,LTD		
		WO2016/187846A1	01-12-2016	Dialog Semiconductor		

NONPATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]

Examiner Signature	/ANH Q TRAN/	Date Considered	11/21/2017

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IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				*Application Number*	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				*Examiner Name*	TRAN, ANH Q
Sheet	3	of	2	*Attorney Docket Number*	SUP-101C-3

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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PTO Notes regarding this form:

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[2] See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04.
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[5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible.
[6] Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/339,221	10/31/2016	2844	3640	SUP-101C-3	32	3

CONFIRMATION NO. 3876

CORRECTED FILING RECEIPT

74712
Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

OC000000098154280

Date Mailed: 12/19/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Xintong Liu, Jiaxing, CHINA;
Aiming Xiong, Jiaxing, CHINA;
Tao Jiang, Jiaxing, CHINA;
Feng Zou, Jiaxing, CHINA;

Applicant(s)

JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD, Jiaxing, CHINA;

Power of Attorney: The patent practitioners associated with Customer Number 74712

Domestic Priority data as claimed by applicant

This application is a CIP of 15/210,989 07/15/2016 PAT 9587817
which is a CIP of 15/066,645 03/10/2016 PAT 9497821
which is a CIP of 14/865,387 09/25/2015 PAT 9609711
and said 15/210,989 07/15/2016
is a CIP of 15/205,011 07/08/2016 PAT 9629211
which is a CIP of 15/150,458 05/10/2016 PAT 9794990
which is a CIP of 14/865,387 09/25/2015 PAT 9609711
and is a CIP of 14/699,138 04/29/2015 PAT 9480109

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)
CHINA 201410507660.9 09/28/2014
CHINA 201410508899.8 09/28/2014
CHINA 201410623355.6 11/06/2014
CHINA 201410734425.5 12/05/2014
CHINA 201510075925.7 02/12/2015

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CHINA 201510134586.5 03/26/2015
CHINA 201510133689.X 03/25/2015
CHINA 201510136796.8 03/27/2015
CHINA 201510173861.4 04/14/2015
CHINA 201510155807.7 04/03/2015
CHINA 201510193980.6 04/22/2015
CHINA 201510372375.5 06/26/2015
CHINA 201510259151.3 05/19/2015
CHINA 201510268927.8 05/22/2015
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CHINA 201510373492.3 06/26/2015
CHINA 201510364735.7 06/26/2015
CHINA 201510378322.4 06/29/2015
CHINA 201510391910.1 07/02/2015
CHINA 201510406595.5 07/10/2015
CHINA 201510482944.1 08/07/2015
CHINA 201510486115.0 08/08/2015
CHINA 201510428680.1 07/20/2015
CHINA 201510483475.5 08/08/2015
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CHINA 201510557717.0 09/06/2015
CHINA 201510595173.7 09/18/2015
CHINA 201510530110.3 08/26/2015
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CHINA 201620089157.0 01/28/2016
CHINA 201610420790.8 06/14/2016
CHINA 201510848766.X 11/27/2015
CHINA 201510903680.2 12/09/2015
CHINA 201610132513.7 03/09/2016
CHINA 201610142140.1 03/14/2016
CHINA 201610452437.8 06/20/2016
CHINA 201420602526.2 10/17/2014
CHINA 201510617370.4 09/25/2015
CHINA 201510716899.1 10/29/2015
CHINA 201510726365.7 10/30/2015
CHINA 201510868263.9 12/02/2015
CHINA 201610044148.4 01/22/2016
CHINA 201610051691.7 01/26/2016

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: No

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Request to Retrieve - This application either claims priority to one or more applications filed in an intellectual property Office that participates in the Priority Document Exchange (PDX) program or contains a proper **Request to Retrieve Electronic Priority Application(s)** (PTO/SB/38 or its equivalent). Consequently, the USPTO will attempt to electronically retrieve these priority documents.

If Required, Foreign Filing License Granted: 11/29/2016

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/339,221**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

LED TUBE LAMP

Preliminary Class

315

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of:	Liu et al.	Attorney Docket:	SUP-101C-3
Serial Number:	15/339,221	Group Art Unit:	2844
Filed:	October 31, 2016	Examiner:	Anh Q. TRAN
Confirmation Number:	3876		

Title: LED TUBE LAMP

REQUEST FOR CORRECTED FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir/Madam:

The original filing receipt mailed December 1, 2016 and corrected filing receipt mailed December 19, 2017 both failed to recognize the foreign priority claims made upon filing of this application. Please see the original ADS filed on October 31, 2016. Applicant hereby submits an ADS listing the same foreign priority references listed on the ADS filed October 31, 2016. Applicant has underlined the priority references that are NOT listed on the ADS, which is also shown below, and respectfully requests that they be included in a corrected Filing Receipt.

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201610085895.2	CN	2016-02-15	
201610097627.4	CN	2016-02-16	
201510281812.7	CN	2016-04-28	
201610708222.8	CN	2016-10-27	
201610728484.2	CN	2016-10-20	
201610050944.8	CN	2016-01-26	
201610296424.8	CN	2016-05-27	
201610120883.6	CN	2016-03-03	
201610628602.7	CN	2016-10-08	

Note: this is not a delayed claim to priority. Priority was properly claimed upon filing this application, but the USPTO made an error when printing the Filing Receipt. So this is merely a request to correct the USPTO error on the original and corrected filing receipts.

Respectfully submitted,

/Bradley Edelman/

MUIR PATENT LAW, PLLC.
9913 Georgetown Pike, Suite 200
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Fax: (703) 757-7447
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Xintong		Liu	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Jiaxing	Country of Residence	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd, Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China

City	Jiaxing City	State/Province	
Postal Code		Country	CN

Inventor 2 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Aiming		Xiong	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Jiaxing	Country of Residence	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd, Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China

City	Jiaxing City	State/Province	
Postal Code		Country	CN

Inventor 3 — Remove

Legal Name

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	

Title of Invention	LED TUBE LAMP

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tao		Jiang	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Jiaxing	Country of Residence	CN

Mailing Address of Inventor:

Address 1	No 1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China

City	Jiaxing City	State/Province	
Postal Code		Country	CN

Inventor 4 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Feng		Zou	

Residence Information (Select One) ○ US Residency ◉ Non US Residency ○ Active US Military Service

City	Jiaxing	Country of Residence	CN

Mailing Address of Inventor:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area,
Address 2	Jiaxing City, Zhejiang, China

City	Jiaxing City	State/Province	
Postal Code		Country	CN

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application.

Customer Number	74712		
Email Address	pto@muirpatentlaw.com	Add Email	Remove Email

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Information:

Title of the Invention	LED TUBE LAMP		
Attorney Docket Number	SUP-101C-3	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)		**Suggested Figure for Publication (if any)**	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	74712		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	15210989	2016-07-15
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15210989	Continuation in part of	15066645	2016-03-10
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15066645	Continuation in part of	14865387	2015-09-25

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15210989	Continuation in part of	15205011	2016-07-08
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15205011	Continuation in part of	15150458	2016-05-10
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15150458	Continuation in part of	14865387	2015-09-25
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
15150458	Continuation in part of	14699138	2015-04-29

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[1] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

			Remove
Application Number	Country[1]	Filing Date (YYYY-MM-DD)	Access Code[1] (if applicable)
201410507660.9	CN	2014-09-28	
			Remove
Application Number	Country[1]	Filing Date (YYYY-MM-DD)	Access Code[1] (if applicable)
201410508899.8	CN	2014-09-28	
			Remove
Application Number	Country[1]	Filing Date (YYYY-MM-DD)	Access Code[1] (if applicable)
201410623355.6	CN	2014-11-06	
			Remove
Application Number	Country[1]	Filing Date (YYYY-MM-DD)	Access Code[1] (if applicable)
201410734425.5	CN	2014-12-05	
			Remove
Application Number	Country[1]	Filing Date (YYYY-MM-DD)	Access Code[1] (if applicable)
201510075925.7	CN	2015-02-12	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510104823.3	CN	2015-03-10	
201510134586.5	CN	2015-03-26	
201510133689.x	CN	2015-03-25	
201510136796.8	CN	2015-03-27	
201510173861.4	CN	2015-04-14	
201510155807.7	CN	2015-04-03	
201510193980.6	CN	2015-04-22	
201510372375.5	CN	2015-06-26	
201510259151.3	CN	2015-05-19	
201510268927.8	CN	2015-05-22	
201510284720.x	CN	2015-05-29	
201510338027.6	CN	2015-06-17	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510315636.x	CN	2015-06-10	
201510373492.3	CN	2015-06-26	
201510364735.7	CN	2015-06-26	
201510378322.4	CN	2015-06-29	
201510391910.1	CN	2015-07-02	
201510406595.5	CN	2015-07-10	
201510482944.1	CN	2015-08-07	
201510486115.0	CN	2015-08-08	
201510428680.1	CN	2015-07-20	
201510483475.5	CN	2015-08-08	
201510555543.4	CN	2015-09-02	
201510557717.0	CN	2015-09-06	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510595173.7	CN	2015-09-18	
201510530110.3	CN	2015-08-26	
201510499512.1	CN	2015-08-14	
201510448220.5	CN	2015-07-27	
201510645134.3	CN	2015-10-08	
201510680883.x	CN	2015-10-20	
201610327808.0	CN	2016-05-18	
201620089157.0	CN	2016-01-28	
201610420790.8	CN	2016-06-14	
201510848768.X	CN	2015-11-27	
201510903680.2	CN	2015-12-09	
201610132513.7	CN	2016-03-09	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201610142140.1	CN	2016-03-14	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201610452437.8	CN	2016-06-20	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201420602526.2	CN	2014-10-17	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510530110.3	CN	2015-08-26	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510499512.1	CN	2015-08-14	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510617370.4	CN	2015-09-25	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510645134.3	CN	2015-10-08	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510716899.1	CN	2015-10-29	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510726365.7	CN	2015-10-30	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201510868263.9	CN	2015-12-02	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201610044148.4	CN	2016-01-22	

Remove

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201610051691.7	CN	2016-01-26	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)
201610085895.2	CN	2016-02-15	
201610087627.4	CN	2016-02-16	
201610281812.7	CN	2016-04-29	
201510705222.8	CN	2015-10-27	
201510726484.2	CN	2015-10-30	
201610050944.9	CN	2016-01-26	
201610098424.5	CN	2016-02-23	
201610120993.5	CN	2016-03-03	
201610876593.7	CN	2016-10-08	

Remove

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

PTO/AIA/14 (03-13)
Approved for use through 01/31/2014. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	

Title of Invention	LED TUBE LAMP

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD

Mailing Address Information For Applicant:

Address 1	No.1288 Jiachuang Rd. Xiuzhou Area		
Address 2	Jiaxing, Zhejiang, People's Republic of China.		
City	Jiaxing	**State/Province**	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

If the Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	SUP-101C-3
	Application Number	
Title of Invention	LED TUBE LAMP	

Mailing Address Information For Non-Applicant Assignee:			
Address 1			
Address 2			
City		State/Province	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button.

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Signature	/Bradley Edelman/			Date (YYYY-MM-DD)	2017-12-20
First Name	Bradley	Last Name	Edelman	Registration Number	57648

Additional Signature may be generated within this form by selecting the Add button.

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses.

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Co o p eration Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	31288762
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	20-DEC-2017
Filing Date:	31-OCT-2016
Time Stamp:	14:11:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	SUP-101C-3_Req_Corrected_Filing_Rct.pdf	224667 f3ee0f6e7a84df4f12f0ac4fa6669327d699b98e	no	3

Warnings:

Information:					
2	Application Data Sheet	SUP-101C-3_ADS.pdf	4537497 9eb91687b3e88b1f2a09a879ae2298606c2e713b	no	13
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
			Total Files Size (in bytes):	4762164	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/38 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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Request to Retrieve Electronic Priority Application(s)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

COMPLETE IF KNOWN	
Application Number	15/339,221
Filing Date	October 31, 2016
First Named Inventor	Xintong Liu
Art Unit	2844
Examiner Name	Ahn Q. Tran
Attorney Docket Number	SUP-101C-3

The undersigned hereby requests the USPTO retrieve an electronic copy of each of the following foreign applications for which priority has been claimed under 35 U.S.C. 119(a)-(d) from a foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement:

Please retrieve (*check all that apply*)

☑ From EPO, JPO, or KIPO (participating foreign intellectual property office) a priority application
Column A. Participating office where application was originally filed
Column B. Application number and filing date of the application
From WIPO (participating foreign intellectual property office) a DAS registered priority application
Column A. DAS Depositing Office where application was originally filed
Column B. Application number and filing date of the application

☐ Copy of certified copy of non-participating office priority document from within a participating foreign intellectual property office application (EPO or JPO)
Column A. Participating office where certified copy of priority document is located
Column B. Application number and filing date of the EPO/JPO application
Column C. Two letter country code and application number of the non-EPO/JPO priority document

	A	B		C	
	Participating Office (e.g., EPO, JPO, KIPO) or DAS Depositing Office (e.g., IB)	Application to be retrieved or application containing the non-participating priority application		Non-participating priority application to be retrieved	
		App. No.	Filing Date	Country Code	App. No.
1	SIPO	201610085895.2	02-15-2015		
2	SIPO	201610087627.4	02-16-2016		
3	SIPO	201610281812.7	04-29-2016		
4	SIPO	201510705222.8	10-27-2015		
5	SIPO	201510726484.2	10-30-2015		
6	SIPO	201610050944.9	01-26-2016		

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This Request should be submitted concurrently with the claim for priority, or thereafter. The USPTO will not attempt to retrieve the identified priority application(s) until applicant indicates the identified priority application(s) on the oath or declaration or an application data sheet in compliance with 37 CFR 1.63(c).

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I hereby declare that I have the authority to grant access to the above-identified foreign application(s).

/Bradley Edelman/	12-21-2017
Signature	Date
Bradley Edelman	703-757-7449
Printed or Typed Name	Telephone Number
Attorney of Record	57,648
Title	Registration Number, if applicable

This collection of information is required by 37 CFR 1.55(d). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process an application). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PTO/SB/38 (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
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COMPLETE IF KNOWN	
Application Number	15/339,221
Filing Date	October 31, 2016
First Named Inventor	Xintong Liu
Art Unit	2844
Examiner Name	Ahn Q. Tran
Attorney Docket Number	SUP-101C-3

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	A	B		C	
	Participating Office (e.g., EPO, JPO, KIPO) or DAS Depositing Office (e.g., IB)	Application to be retrieved or application containing the non-participating priority application		Non-participating priority application to be retrieved	
		App. No.	Filing Date	Country Code	App. No.
1	SIPO	201610098424.5	02-23-2016		
2	SIPO	201610120993.5	03-03-2016		
3	SIPO	201610876593.7	10-08-2016		
4					
5					
6					

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Signature	Date
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4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	31299730
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	21-DEC-2017
Filing Date:	31-OCT-2016
Time Stamp:	10:31:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for USPTO to retrieve priority docs	SUP-101C-3_Request_to_Retrieve_Electronic_Priority_Applications__1.pdf	199820 5d16660339fda2b7b8051489ad647d7100f64edd	no	2

Warnings:

Information:					
2	Request for USPTO to retrieve priority docs	SUP-101C-3_Request_to_Retrieve_Electronic_Priority_Applications__2.pdf	199424 3097e44aac174120687a3b6a5f520b1ba5b22adc	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	399244	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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UNITED STATES PATENT AND TRADEMARK OFFICE

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www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

7590 01/08/2018

Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

EXAMINER	
TRAN, ANH Q	
ART UNIT	PAPER NUMBER
2844	
NOTIFICATION DATE	DELIVERY MODE
01/08/2018	ELECTRONIC

ACKNOWLEDGEMENT OF REQUEST

Notice of Allowance/Allowability Mailed

The request for a corrected notice of allowance/allowability, dated 12-20-17, has been received by the U.S.Patent and Trademark Office. A corrected notice of allowance/allowability will not be mailed, but the Office has verified the following information, and made any necessary corrections to Office computer data:

- **Applicant claims "Foreign Priority" (benefit of an earlier Foreign application pursuant to 35 U.S.C. 119(a)-(d) or (f)).**

☑ Certified copies of the priority documents have been received.

☐ Certified copies of priority documents have been received in Application No.

Only the first 50 foreign appls. will appear on a printout, but Chinese applications #51-59 (of 59) will appear in the upcoming U.S. patent when this appl. 15/339,221 is issued (patented).

A. Marty Willis
571-272-4200 or 1-888-786-0101
Application Assistance Unit
Office of Data Management

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Liu et al.

Serial Number: 15/339,221

Filed: October 31, 2016

Confirmation Number: 3876

Title: **LED TUBE LAMP**

Attorney Docket: SUP-101C-3

Group Art Unit: 2844

Examiner: Anh Q. TRAN

AMENDMENT FILED UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

Dear Sir:

In response to the Notice of Allowance mailed December 11, 2017, Applicant hereby submits this Amendment.

It is respectfully requested that the amendment be entered.

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

What is claimed is:

1. (Previously Presented) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,

wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the detection determining circuit, and

wherein the pulse generating circuit is configured to output one or more pulse signals independent of whether the detection determining circuit detects the sampling signal.

2. (Original) The installation detection circuit according to claim 1, wherein the pulse generating circuit comprises:

a first capacitor, one end connected to a driving signal;

a first resistor, one end connected to the other end of the first capacitor, the other end the first resistor connected to a reference voltage;

a first buffer, having an input end and an output end, the input end connected to the other end of the first capacitor;

a second capacitor, one end connected to the output end of the first buffer;

a third capacitor, one end connected to the output end of the first buffer;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

3. (Canceled)

4. (Previously Presented) The installation detection circuit according to claim 1, wherein when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

5. (Previously Presented) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state, and

wherein the signal generated from the external driving signal is a sampling signal on the power loop, the installation detection circuit further comprises a detection determining circuit configured to detect the sampling signal for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and

the detection determining circuit; and

wherein the installation detection circuit further includes a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

6. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.

7. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a second capacitor, one end coupled to a driving signal;

a third capacitor, one end coupled to the driving signal;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for

outputting the one or more pulse signals.

8. (Original) The installation detection circuit according to claim 7, wherein the second buffer comprises two inverters connected in series.

9. (Original) The installation detection circuit according to claim 7, wherein the detection result latching circuit comprises:

a first D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit;

a fourth resistor, one end connected to the output end of the first D flip-flop, the other end of the fourth resistor connected to a reference voltage; and

a second OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first OR gate, the second input end connected to the output end of the first D flip-flop, the output end of the second OR gate connected to the switch circuit.

10. (Original) The installation detection circuit according to claim 7, wherein the switch circuit comprises:

a first transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

11. (Previously Presented) The installation detection circuit according to claim 7, wherein the detection determining circuit comprises:

a fifth resistor, one end connected to the switch circuit, the other end of the fifth resistor connected to a second end of the power loop; and

a first comparator, having a first input end, a second input end, and an output end, the first input end connected to a predefined signal, the second input end connected to the one end of the fifth resistor, the output end of the first comparator connected to the detection result latching circuit.

12. (Original) The installation detection circuit according to claim 5, wherein the pulse generating circuit comprises:

a sixth resistor, one end connected to a driving signal;

a fourth capacitor, one end connected to the other end of the sixth resistor, the other end of the fourth capacitor connected to a reference voltage;

a Schmitt trigger, having an input end and an output end, the input end connected to the one end of the fourth capacitor, the output end connected to the detection result latching circuit;

a seventh resistor, one end connected to the one end of the fourth capacitor;

a second transistor, having a base, a collector, and an emitter, the collector connected to the other end of the seventh resistor, the emitter connected to a reference voltage; and

an eighth resistor, one end connected to the base of the second transistor, the other end of the eighth resistor connected to the detection result latching circuit and the switch circuit.

13. (Original) The installation detection circuit according to claim 12, wherein the pulse generating circuit further comprises:

a Zener diode, having an anode and a cathode, the anode connected to the other end of the fourth capacitor, the cathode connected to the one end of the fourth capacitor.

14. (Original) The installation detection circuit according to claim 12, wherein the detection result latching circuit comprises:

a second D flip-flop, having a data input end, a clock input end, and an output end, the data input end connected to the driving signal, the clock input end connected to the detection determining circuit; and

a third OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the Schmitt trigger, the second input end connected to the output end of the second D flip-flop, the output end of the third OR gate connected to the other end of the eighth resistor and the switch circuit.

15. (Original) The installation detection circuit according to claim 12, wherein the switch circuit comprises:

a third transistor, having a base, a collector, and an emitter, the base connected to the detection result latching circuit, the collector connected to one end of the power loop, the emitter connected to the detection determining circuit.

16. (Previously Presented) The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop; and

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to a predefined signal, the second input end connected to the one end of the ninth resistor, the output end of the second comparator connected to the detection result latching circuit.

17. (Previously Presented) The installation detection circuit according to claim 12, wherein the detection determining circuit comprises:

a ninth resistor, one end connected to the switch circuit, the other end of the ninth resistor connected to a second end of the power loop;

a second diode, having an anode and a cathode, the anode connected to the one end

of the ninth resistor;

a second comparator, having a first input end, a second input end, and an output end, the first input end connected to a predefined signal, the second input end connected to the cathode of the second diode, the output end of the second comparator connected to the detection result latching circuit;

a third comparator, having a first input end, a second input end, and an output end, the first input end connected to the cathode of the second diode, the second input end connected to another predefined signal, the output end of the third comparator connected to the detection result latching circuit;

a tenth resistor, one end connected to the driving signal;

an eleventh resistor, one end connected to the other end of the tenth resistor and the second input end of the second comparator, the other end of the eleventh resistor connected to a reference voltage; and

a fifth capacitor, connected to the eleventh resistor in parallel.

18. (Previously Presented) An installation detection circuit configured in a light-emitting diode (LED) tube lamp configured to receive an external driving signal, the installation detection circuit comprising:

a pulse generating circuit configured to output one or more pulse signals; wherein the installation detection circuit is configured to detect during at least one of the one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket, based on detecting a signal generated from the external driving signal; and

a switch circuit coupled to the pulse generating circuit, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state, and

wherein the LED tube lamp comprises a lamp tube and a circuit board, and comprises an inductive element connected between two terminals respectively at two ends of the lamp tube for grounding or connecting to a reference potential, wherein one of the two terminals is connected to the circuit board.

19. (Original) The installation detection circuit according to claim 18, wherein the inductive element is an inductor.

20. (Original) The installation detection circuit according to claim 19, wherein one end of the inductor is directly electrically connected to the circuit board.

21. (Original) The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

22. (Previously Presented) An installation detection circuit configured in a light-emitting diode (LED) tube lamp, the installation detection circuit comprising:

means for generating one or more pulse signals;

means for detecting during one or more pulse signals whether the LED tube lamp is properly installed on a lamp socket; and

a switch circuit coupled to the means for generating one or more pulse signals, wherein the one or more pulse signals control turning on and off of the switch circuit;

wherein the installation detection circuit is further configured to:

when it is detected during one of the one or more pulse signals that the LED tube

lamp is not properly installed on the lamp socket, control the switch circuit to remain in an off state to cause a power loop of the LED tube lamp to be open; and

when it is detected during one of the one or more pulse signals that the LED tube lamp is properly installed on the lamp socket, control the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state,

wherein the means for detecting is configured to detect a sampling signal on the power loop for determining whether the LED tube lamp is properly installed on the lamp socket, and the power loop includes the switch circuit and the means for detecting, and

wherein the LED tube lamp is configured to receive an external driving signal and comprises a rectifying circuit for rectifying the external driving signal and a filtering circuit coupled to the rectifying circuit, wherein the installation detection circuit is coupled between the rectifying circuit and the filtering circuit.

23. (Canceled)

24. (Previously Presented) The installation detection circuit according to claim 22, wherein when the means for detecting determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the means for detecting determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

25. (Previously Presented) The installation detection circuit according to claim 22, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the means for detecting.

26. (Canceled)

27. (Original) A detection method adopted by a light-emitting device (LED) tube lamp for preventing a user from electric shock when the LED tube lamp is being installed on a lamp socket, the detection method comprising:

when at least one end of the LED tube lamp is installed on the lamp socket, generating one or more pulse signals by a pulse generating circuit, wherein the pulse generating circuit is configured in the LED tube lamp;

detecting a sampling signal on a power loop of the LED tube lamp by a detection determining circuit, to detect during the one or more pulse signals whether the other end of the LED tube lamp is properly installed on the lamp socket;

receiving the one or more pulse signals through a detection result latching circuit by a switch circuit, wherein the switch circuit is on the power loop; and

comparing the sampling signal with a predefined signal, wherein during the one or more pulse signals when the sampling signal is smaller than the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open.

28. (Original) The detection method according to claim 27, wherein the step of controlling the switch circuit to remain in an off state to cause the power loop of the LED tube lamp to be open comprises:

outputting a first low level signal by the detection determining circuit;

receiving the first low level signal by the detection result latching circuit and

outputting a second low level signal; and

receiving the second low level signal by the switch circuit and maintaining an off

state of the switch circuit to cause the power loop to be open.

29. (Original) The detection method according to claim 27, wherein during any of the one or more pulse signals when the sampling signal is greater than or equal to the predefined signal, the detection method further comprises:

controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state.

30. (Original) The detection method according to claim 29, wherein the step of controlling the switch circuit to remain in a conducting state to cause the power loop of the LED tube lamp to maintain a conducting state comprises:

outputting a first high level signal by the detection determining circuit;

receiving the first high level signal by the detection result latching circuit and outputting a second high level signal; and

receiving the second high level signal by the switch circuit and conducting the switch circuit to cause the power loop to maintain a conducting state.

31. (Original) The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 10 microseconds and 1 millisecond.

32. (Original) The detection method according to claim 27, wherein a period of each of the one or more pulse signals is between 1 microsecond and 100 microseconds.

33. (Currently Amended) The installation detection circuit according to claim [[1]]5, configured such that when the detection determining circuit determines that the sampling signal is greater than or equal to a predefined signal, it is detected that the LED tube lamp is properly installed on the lamp socket; and when the detection determining

circuit determines that the sampling signal is smaller than a predefined signal, it is detected that the LED tube lamp is not properly installed on the lamp socket.

34. (Previously Presented) The installation detection circuit according to claim 1, further comprising a detection result latching circuit coupled to the switch circuit, wherein the detection result latching circuit is configured to receive the one or more pulse signals to control turning on and off of the switch circuit based on a detection result signal from the detection determining circuit.

35. (Previously Presented) The installation detection circuit according to claim 34, wherein the pulse generating circuit is coupled to an output of the detection result latching circuit to control the time of the one or more pulse signals.

36. (Previously Presented) The installation detection circuit according to claim 34, wherein the pulse generating circuit comprises:

a second capacitor, one end coupled to a driving signal;

a third capacitor, one end coupled to the driving signal;

a second resistor, one end connected to the driving signal, the other end of the second resistor connected to the other end of the second capacitor;

a third resistor, one end connected to the other end of the third capacitor, the other end of the third resistor connected to a reference voltage;

a first diode, having an anode and a cathode, the anode connected to the other end of the third resistor, the cathode connected to the one end of the third resistor that is not connected to a reference voltage;

a first inverter, having an input end and an output end, the input end connected to the other end of the second capacitor;

a second buffer, having an input end and an output end, the input end connected to the other end of the third capacitor; and

a first OR gate, having a first input end, a second input end, and an output end, the first input end connected to the output end of the first inverter, the second input end connected to the output end of the second buffer, the output end of the first OR gate for outputting the one or more pulse signals.

37. (Previously Presented) The installation detection circuit according to claim 34, wherein the pulse generating circuit comprises:

a sixth resistor, one end connected to a driving signal;

a fourth capacitor, one end connected to the other end of the sixth resistor, the other end of the fourth capacitor connected to a reference voltage;

a Schmitt trigger, having an input end and an output end, the input end connected to the one end of the fourth capacitor, the output end connected to the detection result latching circuit;

a seventh resistor, one end connected to the one end of the fourth capacitor;

a second transistor, having a base, a collector, and an emitter, the collector connected to the other end of the seventh resistor, the emitter connected to a reference voltage; and

an eighth resistor, one end connected to the base of the second transistor, the other end of the eighth resistor connected to the detection result latching circuit and the switch circuit.

38. (Previously Presented) The installation detection circuit according to claim 1, wherein a period of each of the one or more pulse signals is between 1 microsecond and 1 millisecond.

REMARKS

This Amendment is filed to correct an error in the previously-filed amendment. In the Amendment filed on November 7, 2017, new claim 33 depended from claim 1. However, this was essentially a duplicate of claim 4, which already depended from claim 1. So, to correct this error, claim 33 is now amended to depend from independent claim 5. No further review or search is believed to be necessary, and so Applicant requests that this Amendment be entered at this time.

In the event any fees are required in connection with this paper, or in the event of an overpayment, please charge or credit the Deposit Account No. 50-4574.

Respectfully submitted,

/Bradley Edelman/

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Electronic Acknowledgement Receipt

EFS ID:	31657971
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman
Filer Authorized By:	
Attorney Docket Number:	SUP-101C-3
Receipt Date:	31-JAN-2018
Filing Date:	31-OCT-2016
Time Stamp:	12:45:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		SUP-101C-3_312_Amendment.pdf	131129 8d85ae2858d9026e0d821b7586a311846cc582ca	yes	16

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment after Notice of Allowance (Rule 312)	1	1
	Claims	2	15
	Applicant Arguments/Remarks Made in an Amendment	16	16
Warnings:			
Information:			
	Total Files Size (in bytes):	131129	

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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

74712 7590 02/22/2018

Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

EXAMINER
TRAN, ANH Q

ART UNIT	PAPER NUMBER
2844	

NOTIFICATION DATE	DELIVERY MODE
02/22/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
pto@muirpatentlaw.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	15/339,221	LIU ET AL.
	Examiner	Art Unit
	ANH TRAN	2844

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

1. ☒ The amendment filed on *31 January 2018* under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

2/16/18	/ANH TRAN/ Primary Examiner, Art Unit 2844

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Liu et al.

Serial Number: 15/339,221

Filed: October 31, 2016

Confirmation Number: 3876

Title: **LED TUBE LAMP**

Attorney Docket: SUP-101C-3

Group Art Unit: 2844

Examiner: Anh Q. TRAN

AMENDMENT FILED UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313

OK TO ENTER: /A.Q.T/
02/16/2018

Dear Sir:

In response to the Notice of Allowance mailed December 11, 2017, Applicant hereby submits this Amendment.

It is respectfully requested that the amendment be entered.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Muir Patent Law, PLLC
9913 Georgetown Pike, Suite 200
P.O. Box 1213
Great Falls, VA 22066

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	10/31/2016	Xintong Liu	SUP-101C-3	3876

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	no	960	0	960	03/12/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Jiaxing Super Lighting Electric Appliance Co.,Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): No. 1288 Jiachuang Rd. Xiuzhou Area, Jiaxing, Zhejiang, People's Republic of China

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☑ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☑ Issue Fee
☑ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☑ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 50-4574 .

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Bradley Edelman/ Date February 22, 2018

Typed or printed name Bradley Edelman Registration No. 57,648

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal	
Application Number:	15339221
Filing Date:	31-Oct-2016
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Filer:	Bradley E. Edelman/Amy Dean
Attorney Docket Number:	SUP-101C-3

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
UTILITY APPL ISSUE FEE	1501	1	960	960
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**960**

Electronic Acknowledgement Receipt

EFS ID:	31860905
Application Number:	15339221
International Application Number:	
Confirmation Number:	3876
Title of Invention:	LED TUBE LAMP
First Named Inventor/Applicant Name:	Xintong Liu
Customer Number:	74712
Filer:	Bradley E. Edelman/Amy Dean
Filer Authorized By:	Bradley E. Edelman
Attorney Docket Number:	SUP-101C-3
Receipt Date:	22-FEB-2018
Filing Date:	31-OCT-2016
Time Stamp:	14:57:42
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$960
RAM confirmation Number	022318INTEFSW14584300
Deposit Account	504574
Authorized User	Amy Dean

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SUP-101C-3_Issue_Fee_SIGNED.pdf	221076 4ff3d32b8afeead80f794d96592cee95d1611d5a	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31947 5f89fda2465aa28fb66d1c1f49a465519a1cd009	no	2
Warnings:					
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		Total Files Size (in bytes):	253023		

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Notice of References Cited	Application/Control No. 15/339,221	Applicant(s)/Patent Under Reexamination LIU ET AL.	
	Examiner ANH TRAN	Art Unit 2844	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
	A	US-				
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N	WO 2015066566 A1	05-2015	~~UNITED STATES~~	SADWICK LAURENCE P	F21V25/00
	O			WO		
	P					
	Q					
	R					
	S					
	T					

Change(s) applied to document, /D.W./ 12/18/2017

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	TRAN, ANH Q
Sheet	2	of	2	Attorney Docket Number	SUP-101C-3

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Change(s) applied to document. /D.W./ 12/18/2017

				~~LIGHTING ELECTRIC APPLIANCE CO.~~	
		US20170164434A1	06-08-2017	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD~~	Xiong et al.
		US20170159923A1	06-08-2017	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD~~	Liu et al.

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document: Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		CN104735873	06-24-2015	JINGSAM ILLUMINATION CO LTD		
		GB2533683	06-29-2016	Richo Co Ltd		
		EP2914065	09-02-2015	Richo Co Ltd		
		WO2012139691	10-18-2012	LEUCHTMITTELWERKE GMBH et al.		
		WO2014206785A1	12-31-2014	Philips (inventor: Haimin Tao)		
		WO2015074917	05-28-2015	Tao et al.		
		WO2015/066566 A1	05-07-2015	INNOSYS, INC.		
		WO2017012512A	01-26-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.,LTD		
		WO2016/187846A1	01-12-2016	Dialog Semiconductor		

NONPATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation[6]

Examiner Signature	/ANH Q TRAN/	Date Considered	11/21/2017

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	Anh Q. TRAN
Sheet	2	of	3	Attorney Docket Number	SUP-101C-3 (S16100US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Change(s) applied to document, /D.W./ 12/18/2017

		US20130147350	06-13-2013	~~Gio Optoelectronics Corp.~~	Yang
		US20130335959	12-19-2013	~~Lightel Technologies Inc.~~	Hsia et al.
		US20110228526	09-22-2011	~~Teknoware Oy~~	Hartikka et al.
		US20160219658	07-28-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD~~	Xiong et al.
		US20160270165	09-15-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD~~	Xiong et al.

Note: Submission of copies of U.S. Patents and published U.S. Patent Applications is not required.

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation[6]
		CN102155642	08-17-2011	CHANGGUI LIU		
		CN200965185	10-24-2007	YAOHAN LIU		
		CN102932997	02-13-2013	ZHEJIANG HENGMAN PHOTOELECTRIC TECHNOLOGY CO LTD		
		CN101715265	05-26-2010	OCEANS KING LIGHTING SCIENCE		
		CN102355780	02-15-2012	ZHEJIANG SHIMING OPTICS TECHNOLOGY CO LTD		
		CN106015996A	10-16-2016	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO LTD		
		WO2017012514A1	01-26-2017	JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD		
		WO2013150417A1	10-10-2013	Koninklijke Philips N.V.		
		WO2015028329A1	03-05-2015	Koninklijke Philips N.V.		
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	10-31-2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	TRAN, ANH Q
Sheet	1	of	2	Attorney Docket Number	SUP-101C-3

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110121756	05-26-2011	Thomas et al.	
		US20110057572	03-10-2011	Kit et al.	
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		US20120299501	11-29-2012	Kost et al.	
		US9210744 12/2015	~~10-24-2013~~	~~Carmen et al.~~ Del Carmen, Jr. et al.	
Change(s) applied to document, /C.F./ 12/27/2017		US20160081147	03-17-2016	Luo Hua GUANG	
		US20110176297	07-21-2011	Hsia et al.	
		US20100220469	09-02-2010	Ivey et al.	
		US20120300445	11-29-2012	Chu et al.	
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		US20110043127	02-24-2011	Yamasaki	
		US20140239834	08-28-2014	Choi et al	
		US9609711	03-28-2017	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Jiang et al.
		US20160198535	07-07-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Ye et al.
		US9629215	04-18-2017	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
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		US20160270165	09-15-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
		US20160270164	09-15-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
		US20160309550	10-20-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

IDS Form PTO/SB/08: Substitute for form 1449A/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	15/339,221
				Filing Date	October 31, 2016
				First Named Inventor	XINTONG LIU
				Art Unit	2844
(Use as many sheets as necessary)				Examiner Name	Anh Q. TRAN
Sheet	1	of	3	Attorney Docket Number	SUP-101C-3 (S16100US)

U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US20020176262	11-28-2002	Ajay Tripathi	
		US20030102819	06-05-2003	Young-Kee Min	
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		US20140265900	09-18-2014	Sadwick et al.	
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		US20120181952	07-19-2012	Rooer	
Change(s) applied to document, /C.C.B./ 1/4/2018		US7380961 06/2008	~~12-16-2004~~	Hideo Moriyama	
		US20160219672	07-28-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Liu
Change(s) applied to document, /D.W./ 12/18/2017		US20160270163	09-15-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Hu et al.
		US20160356472	12-08-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Liu et al.
		US20170094736A1	03-30-2017	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
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		US8796943 08/2014	~~02-06-2014~~	MIYAMICHI SABURO	
		US9521718	12-13-2016	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
		US20170105263	04-13-2017	~~JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO.~~	Xiong et al.
		US20130127327	05-23-2013	~~Fraunhofer-Gesellschaft~~ Zur Forderung	Heil et al.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.Q.T/

UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/339,221	04/10/2018	9939140	SUP-101C-3	3876

74712 7590 03/21/2018

Muir Patent Law, PLLC
P.O. Box 1213
9913 Georgetown Pike, Suite 200
Great Falls, VA 22066

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Xintong Liu, Jiaxing, CHINA;
JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD, Jiaxing, CHINA;
Aiming Xiong, Jiaxing, CHINA;
Tao Jiang, Jiaxing, CHINA;
Feng Zou, Jiaxing, CHINA;

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AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:20-cv-00018-ADA	1/10/2020	Western District of Texas

PLAINTIFF	DEFENDANT
JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD. AND OBERT, INC.	CH LIGHTING TECHNOLOGY CO., LTD., ELLIOTT ELECTRIC SUPPLY INC. AND SHAOXING RUISING LIGHTING CO., LTD.

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	10,295,125	5/21/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
2	10,342,078	7/2/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
3	10,352,540	7/16/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
4	10,426,003	9/24/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
5			

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY
3/16/2020	☑ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,939,140	4/10/2018	Jiaxing Super Lighting Electric Appliance Co., Ltd.
2	10,378,700	8/13/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
3	10,448,479	10/15/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
4	10,560,989	2/11/2020	Jiaxing Super Lighting Electric Appliance Co., Ltd.
5			

In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy

AO 120 (Rev. 08/10)

TO:	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☑ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO.	DATE FILED	U.S. DISTRICT COURT
6:22-cv-00534	5/24/2022	Western District of Texas

PLAINTIFF	DEFENDANT
JIAXING SUPER LIGHTING ELECTRIC APPLIANCE CO., LTD. AND OBERT, INC.	CURRENT LIGHTING SOLUTIONS, LLC D/B/A GE CURRENT

	PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1	9,841,174	12/12/2017	Jiaxing Super Lighting Electric Appliance Co., Ltd.
2	9,939,140	4/10/2018	Jiaxing Super Lighting Electric Appliance Co., Ltd.
3	10,295,125	5/21/2019	Jiaxing Super Lighting Electric Appliance Co., Ltd.
4	11,112,068	9/7/2021	Jiaxing Super Lighting Electric Appliance Co., Ltd.
5			

In the above---entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above---entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT

CLERK	(BY) DEPUTY CLERK	DATE

Copy 1---Upon initiation of action, mail this copy to Director Copy 3---Upon termination of action, mail this copy to Director
Copy 2---Upon filing document adding patent(s), mail this copy to Director Copy 4---Case file copy